Aging analysis of circuit timing considering NBTI and HCI

We present an aging analysis flow able to calculate the degraded circuit timing. To the best of our knowledge it is the first approach on gate level so far capable of analyzing the impact of the two dominant drift-related aging effects - NBTI and HCI - on complex digital circuits. The aging-aware gate model used to compute the aged circuit timing provides not just the cell delay degradation, but also the degradation of the output slope. To get more accurate results, the individual workload of a gate can be considered.

Stichworte:
digital circuits, logic circuits, timing circuits, HCI, NBTI, aging analysis, aging-aware gate model, cell delay degradation, circuit timing, complex digital circuits, hot carrier injection, negative bias temperature instability, output slope degradation


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