The Sizing Rules Method for CMOS and Bipolar Analog Integrated Circuit Synthesis

Abstract:
This paper presents the sizing rules method for basic building blocks in analog CMOS and bipolar circuit design. It consists of the development of a hierarchical library of transistor-pair groups as basic building blocks for analog CMOS and bipolar circuits, the derivation of a hierarchical generic list of constraints that must be satisfied to guarantee the function and robustness of each block, and the development of a reliable automatic recognition procedure of building blocks in a circuit schematic. Sizing rules efficiently capture design knowledge on the technology-specific level of transistor-pair groups. This reduces the effort and improves the resulting quality for analog circuit synthesis. Results of applications like circuit sizing, design centering, response surface modeling or analog placement show the benefits of the sizing rules method.

Stichworte:
Sizing Rules, Bipolar, CMOS, Analog Design, Circuit Sizing, Analog Synthesis

Zeitschriftentitel:
IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems

Jahr: 2008
Band: 27
Jahr / Monat: 2008-12