Abstract:

In high-performance integrated circuits manufactured in CMOS deep sub-micron technology, the speed of global information exchange on the chip has developed into a bottleneck, that limits the effective information processing speed. This is caused by standard on-chip communication based on multi-conductor interconnects, e.g., implemented as parallel interconnect buses. The supported clock frequency of such wired interconnects - at best - remains constant under scaling, but - for global interconnects - reduces by a factor of four, as the structure size is reduced by half. Such multi-conductor interconnects also exhibit some undesirable properties when used for chip-to-chip communication. The much larger distances that have to be bridged, force the clock frequencies for the chip-to-chip interconnects to much lower values than those for on-chip circuitry. In widening up this bottleneck by increasing the number of parallel wires, the separation between the wires has to decrease. This causes increased mutual coupling between neighboring wires, which reduces the supported clock frequency and counters the effect of having more wires in the first place.