Abstract: Commercial o-the-shelf multi-core architectures could significantly reduce costs and time to market of hard real-time systems. However, due to the unpredictable interference on the shared memory, the worst case execution time is either non-deterministic or overly pessimistic. Typically, the pessimism originates from the conservative assumption of maximum interference for each memory access. This paper analyzes the shared memory interference under o-the-shelf round-robin arbiter. Rather than estimating a single worst case bound for the execution time, distribution of execution times along their weights is derived. The analysis results are compared with observed execution time of the benchmark applications on a multi-core platform.

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