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Titel des Beitrags: Adaptive Voltage Scaling by In-Situ Delay Monitoring for an Image Processing Circuit
Abstract: The proposed voltage scheme adaptively tunes the supply voltage of digital circuits, according to PVTA variations. By exploiting unused timing margin, produced by state-of-the-art worst-case designs, energy efficiency is significantly increased. In-situ delay monitoring is performed by enhanced flip-flops, observing signal delays in critical paths. We introduce a novel methodology to analyze the closed-loop behavior of the overall control scheme by a Markov approach, based on extensive transistor simulations. The digital logic and the AVS control circuitry are designed in 65nm CMOS for an image processing application. The AVS approach optimizes dynamic and leakage power dependent on the user-defined image quality requirements.
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