Due to the time-to-market pressure, it is highly desirable to design hardware and software of embedded systems in parallel. However, hardware and software are developed mostly using very different methods, so that performance evaluation and validation of the whole system is not an easy task. In this paper, we propose a simulation approach to bridge the gap between model-driven software development and simulation based hardware design, by merging hardware and software models into a SystemC based simulation environment. An automated procedure has been established to generate software simulation models from formal models, while the hardware design is originally modeled in SystemC. As the simulation models are annotated with timing information, performance issues are tackled in the same pass as system functionality, rather than in a dedicated approach. For designing real-time systems, although performance evaluation based on simulation cannot provide guarantees of safety, it can provide realistic performance values to validate whether the performance requirements are really satisfied or not and show how pessimistic the static analysis is. Further, the simulative approach is also able to provide the developers an insight into the system architecture to help find bottlenecks of the system. We use the simulative approach as a complement of static analysis in order to combine them in an integral development cycle.
Occurences:

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