System specification by state machines together with property specification and verification by temporal logics are by now standard techniques to reason about the control flow of hardware components, embedded systems and communication protocols. The techniques to reason about the dataflow within a system, however, are less well developed. This report adapts a UNITY-like formalism for specification and verification to systems of asynchronously communicating components. The components themselves are specified as state machines. The resulting proof techniques allows abstract and compositional reasoning about dataflow properties of systems.

Stichworte: state machines; communication histories; verification; compositionality

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