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An Improved Single-Phase Multiple DC Source Inverter Topology for Distributed Energy System Applications

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Abstract: This work presents an improved structure of a single-phase muti-input multilevel inverter (MIMLI) for distributed energy resources, which is capable of producing a nine-level output in symmetric mode and 21 levels in asymmetrical mode. The topology uses four DC sources and ten switches, with four switches being bidirectional and the remaining unidirectional. The operation of the circuit is analyzed in an asymmetrical mode, and switching signals are accomplished using the Nearest Level Control (NLC) PWM technique. Depending on the value of the DC sources used, the number of levels can vary. In this work, different DC source algorithms were also proposed, and the analysis of the inverter has been carried out considering the algorithms producing the maximum number of levels. The inverter was simulated in MATLAB/Simulink under steady state and dynamic conditions, achieving a 3.89% THD in output. The thermal analysis was conducted using PLECS software 4.1.2 to assess losses and efficiency. A laboratory prototype of the proposed topology was developed and tested, confirming its performance through simulation results and proving it economically viable for medium- and high-power applications.

Keywords: distributed energy resource (DERs); multilevel inverter; asymmetrical; reduced device count; TSV; Nearest Level Control (NLC); cost factor (CF)

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1. Introduction

The integration of interface converters in environmentally friendly distributed energy resources (DERs) is crucial for delivering high-efficiency, reliable, and high-quality electric power. A DC/AC power processing interface is needed to meet grid standards. Advancements in semiconductor technologies and power electronic techniques have led to the introduction of multilevel inverters (MLIs) to limit the constraints of standard two- or three-level inverters, offering advantages such as reduced voltage stress, higher efficiency, and less electromagnetic interference [1,2]. MLIs are popular due to their high-quality output voltage at a nominal cost. Researchers aim to reduce inverter costs by using overall components effectively and conforming to IEEE 519 [3] guidelines. MLIs are useful in high-power UPS, traction drives, renewable energy integration, and aircraft [4,5].

Conventional multilevel inverters (MLI) such as cascaded H-Bridge (CHB), Neutral Point Clamped (NPC-MLI), and Flying Capacitors (FC-MLI) are widely used in current systems due to their modularity and ease of control [6]. However, they are disadvantaged due to the high number of power switches required to obtain multiple voltage levels and

the complexity of voltage control mechanisms. The large switch count in the converter system makes it bulky, costly, and complex due to its inclusion of gate driver, protection, and heat sink units [7,8]. Reducing power switch count is a growing research area in MLIs. The literature presents many topologies of MLIs to address these issues, categorized into symmetric and asymmetric. Symmetric topologies offer equal magnitude of DC sources, simplified control, and high modularity; but they necessitate additional semiconductor devices for improved power quality [9,10]. In asymmetric topologies, DC sources are of different magnitude, producing higher voltage levels with a reduced device but losing modularity and increasing switching stress on switches [11,12].

The topology in [13] uses three asymmetrical DC sources to provide 55 output voltage levels, but uses 44 switches and seven capacitors. Consequently, the number of devices is still high, and the capacitors require a complicated control mechanism. To reduce complexity, the authors of [14] developed a topology without capacitors. Nevertheless, the increased device count and switching stress are due to the need for an additional H-Bridge to create negative levels. Another asymmetric topology was introduced by the authors of [15], which resulted in a significant reduction in switching stress but an increase in device count. The authors of [16] suggested a topology with fewer devices, but an H-Bridge was needed to achieve negative levels. The H-Bridge switches must tolerate all DC sources, increasing the total standing voltage (TSV) and cost.

The author proposed a nine-level output unit in [17], which can be extended to provide 25-level output, with seven DC sources and 10 switches, six of which are bidirectional. The topology in [18] utilized isolated DC sources and bidirectional switches to reach appropriate output voltage levels, although the voltage stress was significant. The structure proposed in [19] utilizes a basic unit of a cascading H-bridge circuit, which employs 10 switches and three DC sources to provide a 13-level output. More components are required if more units are added to reach the desired levels, increasing the cost. Another MLI topology proposed in [20] generates voltage levels and polarity separately, requiring more DC sources and increased costs. The author of [21] developed a ladder-shaped topology for higher voltage levels with fewer devices but faced issues with a separate polarity generation unit, leading to increasing cost and less reliability. A new topology in [22] for renewable energy applications provides seven levels of output voltage in a symmetrical mode and 11 levels in an asymmetrical mode using six unidirectional and one bidirectional switch. This topology is extended for more voltage levels in cascaded connections. The modified MLI topology proposed in [23], featuring ten switches and four DC sources, achieves 21-level output, claiming modularity and impacting high-power quality. The authors in [24] introduce a novel inverter with a series cascade unit and bidirectional switches, which reduces overall blocking voltages and gate driver circuit requirements, reducing the failure rate of switches and allowing it for medium- and high-voltage applications.

Considering the above discussion, the aim is to develop a multilevel inverter with reduced device count, fewer On-state switches, and less blocking voltage; and operate in symmetrical and asymmetrical modes. This work proposes a multi-input multilevel inverter topology (MIMLI) for DERs, utilizing four DC sources and 10 switches; four of which are bidirectional and the rest are unidirectional. The topology operates in both symmetrical and asymmetrical modes, generating negative voltage levels inherently, reducing stress on switches, and improving inverter efficiency. The paper is organized as follows: Section 2 describes the proposed topology, which includes a circuit configuration, DC source selection, operation, switching technique, total standing voltage, and cost analysis. Section 3 discusses the simulation and experimental results for different loading conditions. The power loss and efficiency of the inverter are discussed in Section 4. Section 5 compares the proposed topology with other topologies. The application of the proposed topology is discussed in Section 6. Finally, Section 7 will conclude the work.

2. Description of the Proposed Topology

2.1. Circuit Configuration

The circuit configuration of the proposed topology is shown in Figure 1. It uses four DC sources and 10 semiconductor switches, four out of 10 switches are bidirectional, with two IGBTs coupled in a common emitter arrangement and fed by the same gate driver. The remaining switches are unidirectional. The proposed topology can be configured in symmetric and asymmetric configurations based on the magnitudes of the DC voltage sources V_1, V_2, V_3, and V_4. Energy storage, PV, batteries, and other renewable energy sources may be utilized as DC sources with a precise controller to maintain each voltage source at an appropriate level.

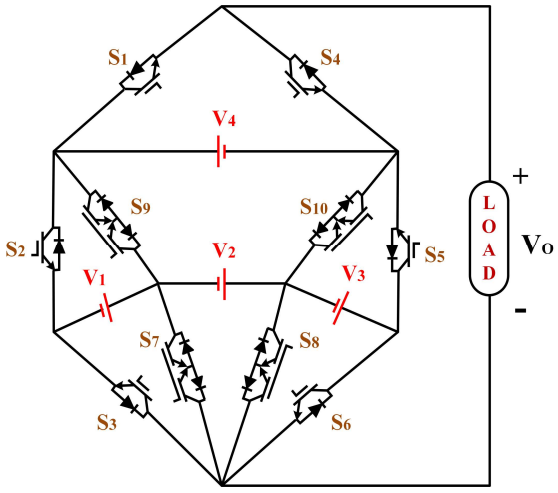


Figure 1. Circuit diagram of the proposed topology.

2.2. Proposed DC Source Selection Algorithm

The proposed topology generates nine levels at the output voltage in a symmetrical configuration, with equal magnitude for all DC sources. However, a symmetrical arrangement requires a large device count for higher voltage levels. To address this, an asymmetrical operation is needed. The topology may provide six distinct output levels by adjusting the magnitude of the DC source. The information on the magnitude of DC sources and the number of output voltage levels, ranging from nine to 21, is provided in Table 1. The performance of the proposed topology is considerably improved by selecting the proper magnitude of DC sources to generate higher voltage levels with reduced device count.

Table 1. Selection of DC Source.

Algorithm	Magnitude of DC Voltage Source	Output Voltage Levels, (N_L)
I	$V_1 = V_2 = V_3 = V_4 = \frac{N_L-1}{8}V$	9
II	$V_1 = V_2 = V_3 = \frac{N_L-1}{10}V$, $V_4 = \frac{N_L-1}{5}V$	11
III	$V_1 = V_3 = \frac{N_L-3}{10}V$, $V_2 = V_4 = \frac{N_L-3}{5}V$	13
IV	$V_1 = \frac{N_L-5}{10}V$, $V_2 = V_3 = V_4 = \frac{N_L-5}{5}V$	15
V	$V_1 = \frac{N_L-7}{10}V$, $V_2 = V_3 = \frac{N_L-7}{5}V$, $V_4 = \frac{N_L-2}{5}V$	17
VI	$V_1 = \frac{N_L-9}{10}V$, $V_2 = V_4 = \frac{N_L-4}{5}V$, $V_3 = \frac{N_L-9}{5}V$	19
VII	$V_1 = \frac{N_L-11}{10}V$, $V_2 = \frac{N_L-11}{5}V$, $V_3 = \frac{N_L-6}{5}V$, $V_4 = \frac{N_L-1}{5}V$	21

2.3. Operation of the Proposed Topology

The proposed topology generates 21 levels with fewer components. The DC sources are used in a ratio V_1:V_2:V_3:V_4 = 1:3:2:4, allowing for 10 positive, 10 negative, and zero levels

at the output. Table 2 displays a topology's switching modes and source combinations for an asymmetrical configuration, allowing for simplified switching. Switches in the conducting state have 1 against them, while the off state has 0. The conduction diagram for the positive half cycle is shown in Figure 2. Level 1V can be generated at the output by bringing V_1 into the conduction path through S_1, S_3, and S_9. Level 2V can be achieved by introducing V_3 through S_4, S_5, and S_8, or by V_4-V_3 source combination by turning on S_1, S_6, and S_{10}. The voltage source V_2 is used to generate Level 3V by turning on S_4, S_7, and S_{10}. Level 4V can be obtained by introducing V_4 into the conduction path through S_1, S_5, and S_6 or turning on S_3, S_4, and S_{10}. Level 5V can be produced by bringing the $V_2 + V_3$ source combination by turning on S_4, S_5, and S_7. Level 6V can be generated by bringing $V_1 + V_2 + V_3$ through switches S_1, S_4, and S_5 or by bringing the $V_3 + V_4$ source combination through switches S_1, S_5, and S_8. Level 7V can be generated by bringing the $V_2 + V_4$ source combination into the conduction path through switches S_1, S_7, and S_{10}. Level 8V can be generated by bringing source combination $V_1 + V_2 + V_4$ into the conduction path through switches S_1, S_3, and S_{10}. Level 9V can be generated by bringing source combination $V_2 + V_3 + V_4$ into the conduction path through switches S_1, S_5, and S_7. Level 10V can be generated by bringing source combination $V_1 + V_2 + V_3 + V_4$ into the conduction path through switches S_1, S_3, and S_5. Zero level can be produced in S_1, S_2, S_3, or S_4, S_5, and S_6. In the proposed topology at any given voltage level, only 3 switches are conducting, resulting in higher efficiency due to lower conduction losses, and redundant states provide more reliable and fault-tolerant topology.

Table 2. Switching States For 21-Level Asymmetrical Configuration.

V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	V_{in}	
1 V	1	0	1	0	0	0	0	0	1	0	V_1	Positive Levels
2 V	0	0	0	1	1	0	0	1	0	0	V_3	
	1	0	0	0	0	1	0	0	0	1	$V_4 - V_3$	
3 V	0	0	0	1	0	0	1	0	0	1	V_2	
4 V	1	0	0	0	1	1	0	0	0	0	V_4	
	0	0	1	1	0	0	0	0	0	1	$V_1 + V_2$	
5 V	0	0	0	1	1	0	1	0	0	0	$V_2 + V_3$	
6 V	0	0	1	1	1	0	0	0	0	0	$V_1 + V_2 + V_3$	
	1	0	0	0	1	0	0	1	0	0	$V_3 + V_4$	
7 V	1	0	0	0	0	0	1	0	0	1	$V_2 + V_4$	
8 V	1	0	1	0	0	0	0	0	0	1	$V_1 + V_2 + V_4$	
9 V	1	0	0	0	1	0	1	0	0	0	$V_2 + V_3 + V_4$	
10 V	1	0	1	0	1	0	0	0	0	0	$V_1 + V_2 + V_3 + V_4$	
0	1	1	1	0	0	0	0	0	0	0	–	Zero Level
	0	0	0	1	1	1	0	0	0	0	–	
−1 V	1	1	0	0	0	0	1	0	0	0	$-V_1$	Negative Levels
−2 V	0	0	0	1	0	1	0	0	0	1	$-V_3$	
−3 V	1	0	0	0	0	0	0	1	1	0	$-V_2$	
−4 V	0	0	0	1	0	0	1	0	1	0	$-V_4$	
	1	1	0	0	0	0	0	1	0	0	$-V_1 - V_2$	
−5 V	1	0	0	0	0	1	0	0	1	0	$-V_2 - V_3$	
−6 V	1	1	0	0	0	1	0	0	0	0	$-V_1 - V_2 - V_3$	
−7 V	0	0	0	1	0	0	0	1	1	0	$-V_2 - V_4$	
−8 V	0	1	0	1	0	0	0	1	0	0	$-V_1 - V_2 - V_3$	
−9 V	0	0	0	1	0	1	0	0	1	0	$-V_2 - V_3 - V_4$	
−10 V	0	1	0	1	0	1	0	0	0	0	$-V_1 - V_2 - V_3 - V_4$	

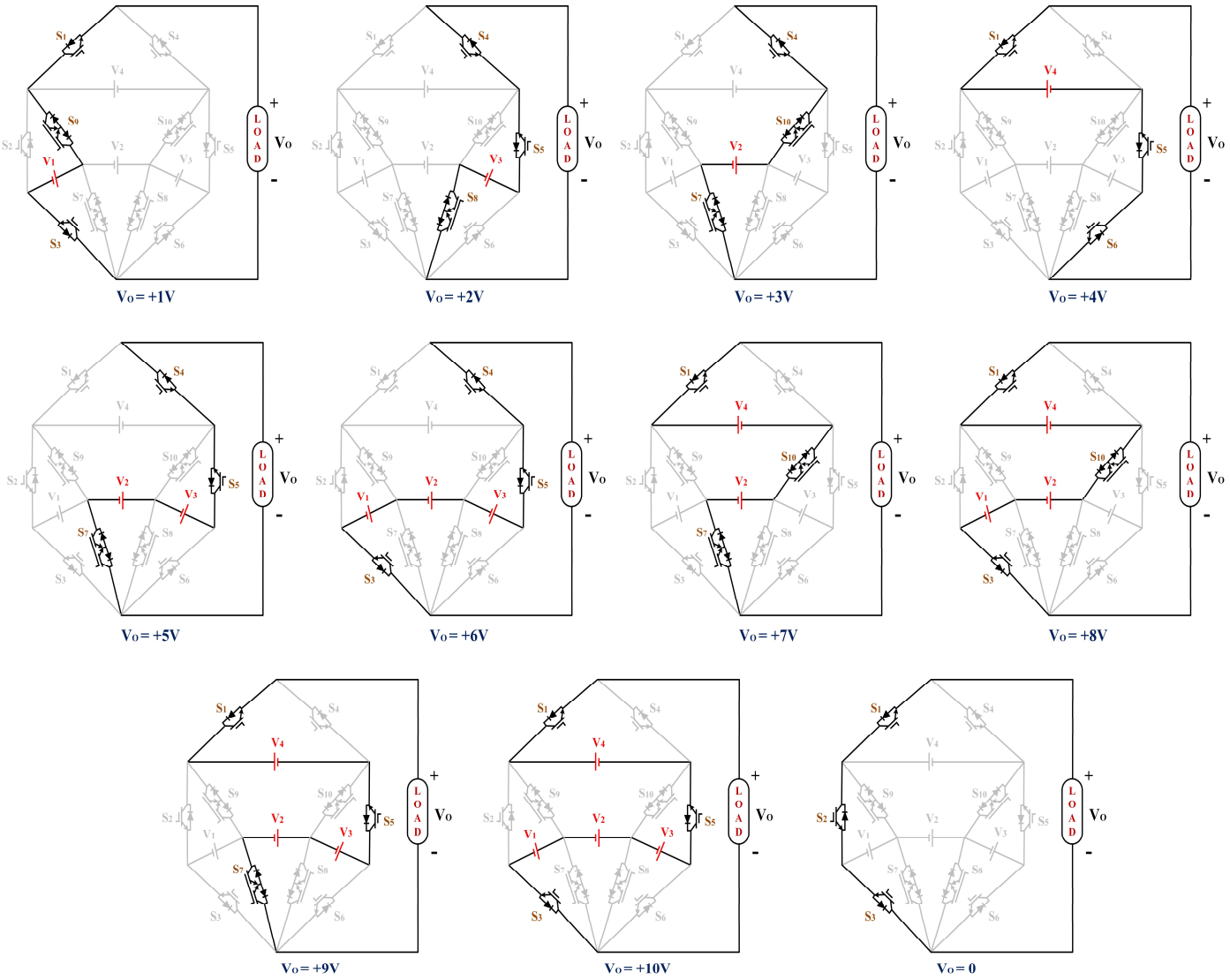


Figure 2. Current conduction path during the positive half-cycle.

2.4. Switching Technique

To generate the staircase output waveform, switches require pulses, which are generated using the pulse width modulation (PWM) technique. The proposed topology employs a low-frequency Nearest Level Control (NLC) PWM technique to implement switching operations [25]. Figure 3 shows the NLC PWM technique. The technique compares the reference waveform (a sine wave with a frequency of 50 Hz) with constant signals to get the appropriate voltage levels at the output. The switching state is changed using the switching logic given in Table 2. The reference waveform magnitude is determined by $0 \leq \mathrm{Vm} \leq (\mathrm{N_{Level}} - 1)/2$ as described in Equation (1). The proposed topology is not limited by modulation techniques, and other techniques can be effectively applied to the converter, ensuring minimal switching losses.

$$\mathrm{V_{Ref}} = 10 \sin (2\pi \times 50\, \mathrm{t}) \quad (1)$$

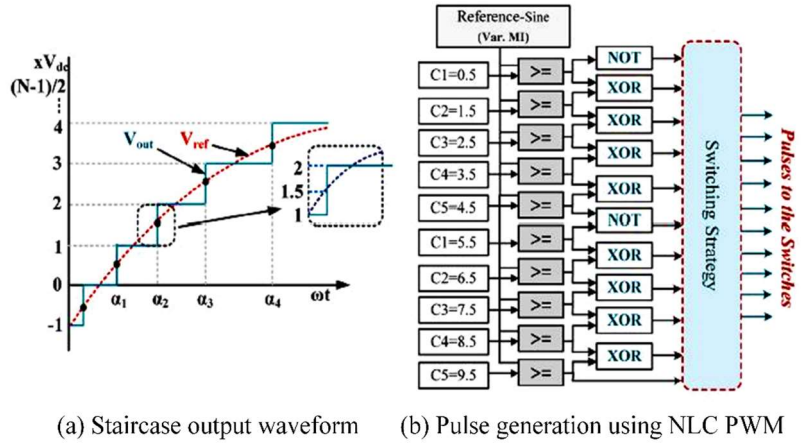


Figure 3. NLC PWM modulation technique.

2.5. Total Standing Voltage (TSV)

Total standing voltage (TSV) is a crucial factor in determining the feasibility of a topology and the appropriate switch ratings. The cost of switches and driver circuits primarily determines the cost of an MLI. The converter with a high value of TSV requires expensive switches, whereas low TSV allows the use of lower-rated switches, which makes the system more economical. The highest voltage across switches during the blocking state is added up mathematically to determine the TSV of MLI, which is calculated using the following relation [26]:

$$\mathrm{TSV} = \sum_{i=1}^{k} \mathrm{V_{max}}(\mathrm{S_i}) \tag{2}$$

where $\mathrm{S_i}$ is the i-th switch and $\mathrm{V_{max}}(\mathrm{S_i})$ is the highest voltage across the i-th switch. Figure 4 shows the voltage stress distribution across the switches. For the proposed topology, switches $\mathrm{S_2}$, $\mathrm{S_5}$, $\mathrm{S_9}$, and $\mathrm{S_{10}}$ must endure the highest stress of 10 V, and $\mathrm{S_1}$ and $\mathrm{S_4}$ experience the least stress of 4 V.

$$\mathrm{TSV} = (2 \times 4\,\mathrm{V_{DC}}) + (4 \times 6\,\mathrm{V_{DC}}) + (4 \times 10\,\mathrm{V_{DC}}) = 72\,\mathrm{V_{DC}} \tag{3}$$

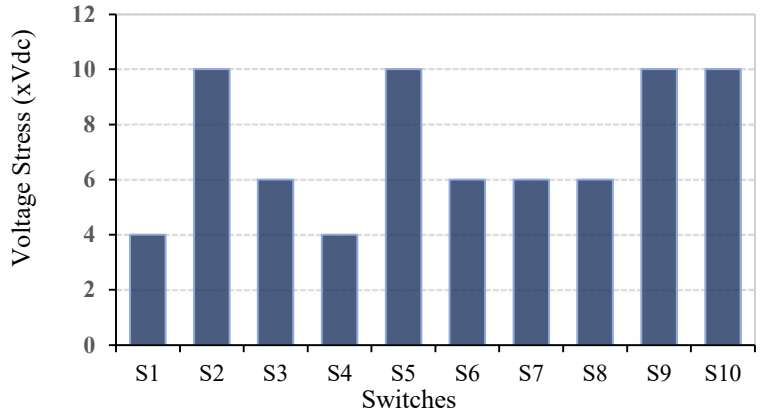


Figure 4. Voltage stress across each switch.

To calculate the per-unit TSV, divide the absolute value of TSV by the peak value of output voltage. The per-unit TSV may be computed as:

$$\mathrm{TSVpu} = \frac{\mathrm{TSV}}{\mathrm{Vo,max}} = 7.2 \tag{4}$$

2.6. Cost Analysis

The cost factor (CF) provides the economic feasibility of the converter. A topology with a high-cost factor indicates less feasibility. It depends on the number of IGBT, driver circuits, capacitors, diodes, TSV, and total DC sources. Since there are no capacitors or diodes in the proposed topology, the cost factor can be evaluated as:

$$CF = N_{DC} + N_{IGBT} + N_{GD} + N_D + N_{Cap} + TSVpu \quad (5)$$

$$CF = 4 + 14 + 10 + 0 + 0 + 7.2 = 35.2 \quad (6)$$

$$CF/Level = 35.2/21 = 1.67 \quad (7)$$

3. Results and Discussion

3.1. Simulation Results

The performance of the proposed topology is studied using MATLAB/Simulink in an asymmetrical mode of operation. The static performance is tested for constant R and RL load, while its dynamic performance is tested for varying R, RL, load power factor, and modulation index. The simulation parameters are listed in Table 3.

Table 3. Simulation parameters.

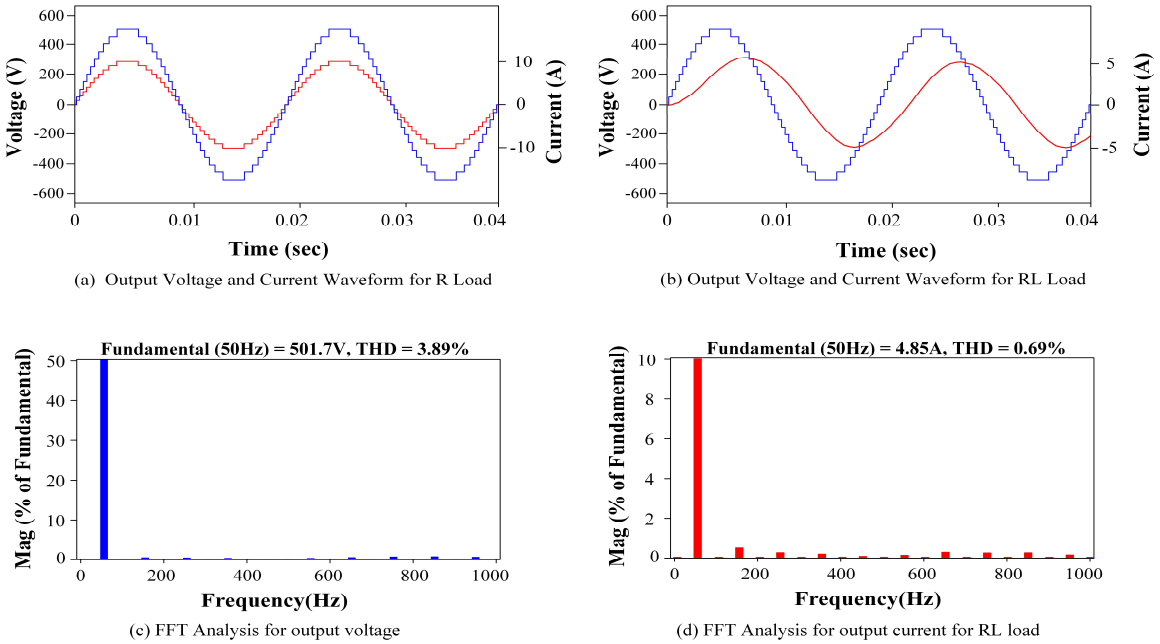
Parameter/Device	Value
DC Sources	V_1 = 50 V, V_2 = 150 V, V_3 = 100 V, V_4 = 200 V
Switches	IGBT
Load Resistance	100 Ω, 50 Ω
Load Inductance	80 mH, 40 mH
Modulation Index	1, 0.6, 0.4

The simulation results for constant loads are shown in Figure 5. For a purely resistive load of 50 Ω, the output voltage and current waveform are shown in Figure 5a. The converter achieves a maximum output voltage of 500 V and a load current of 10 A. For an RL load of 100 Ω + 40 mH, shown in Figure 5b, the output voltage generates 21 levels with a peak value of 500 V and a sinusoidal load current with a peak value of 5 A. Figure 5c depicts the FFT analysis of output voltage for constant load conditions. The output voltage offers a 3.89% THD with a fundamental value of 501.7 V. Figure 5d shows the harmonic profile of output current for RL load. The load current offers a 0.69% THD with a fundamental value of 4.85 A. It can be seen that all the harmonics are below 5%, which satisfies the IEEE-519 standard.

The dynamic performance of the proposed topology is also assessed to make sure it can tolerate sudden variations in load. As seen in Figure 6a, the converter was tested with a varying R load from 100 Ω to 50 Ω. The output voltage remains constant at 21 levels while the load current increases from 5 A to 10 A as the load changes, and the current waveform transitions are smooth without disturbance or transient. When the RL load is changed from 100 Ω + 80 mH to 50 Ω + 40 mH, the current increases with the load current being more sinusoidal due to the inductive effect shown in Figure 6b. The output voltage waveform remains constant and shows all desired voltage levels, indicating proper circuit operation.

When the power factor changes from unity to a lagging power factor, as seen in Figure 6c, the output current changes from stepped to sinusoidal waveform due to load inductance, while the output voltage remains constant. The topology is also tested for varying Modulation Index (MI) from 1 to 0.6 and then to 0.4, as shown in Figure 6d. The results indicate that some voltage levels were not generated when the modulation index decreased from 1 to 0.4, and the output voltage levels dropped from 21 to 9. The modulation index also affects the THD. As the modulation index decreases, the output voltage may not closely resemble a sine wave, which increases the presence of higher-order harmonics, resulting in increased THD. Figure 7 shows the effects of change in modulation. The

simulation results show that the proposed topology effectively performs under both fixed and variable load conditions.



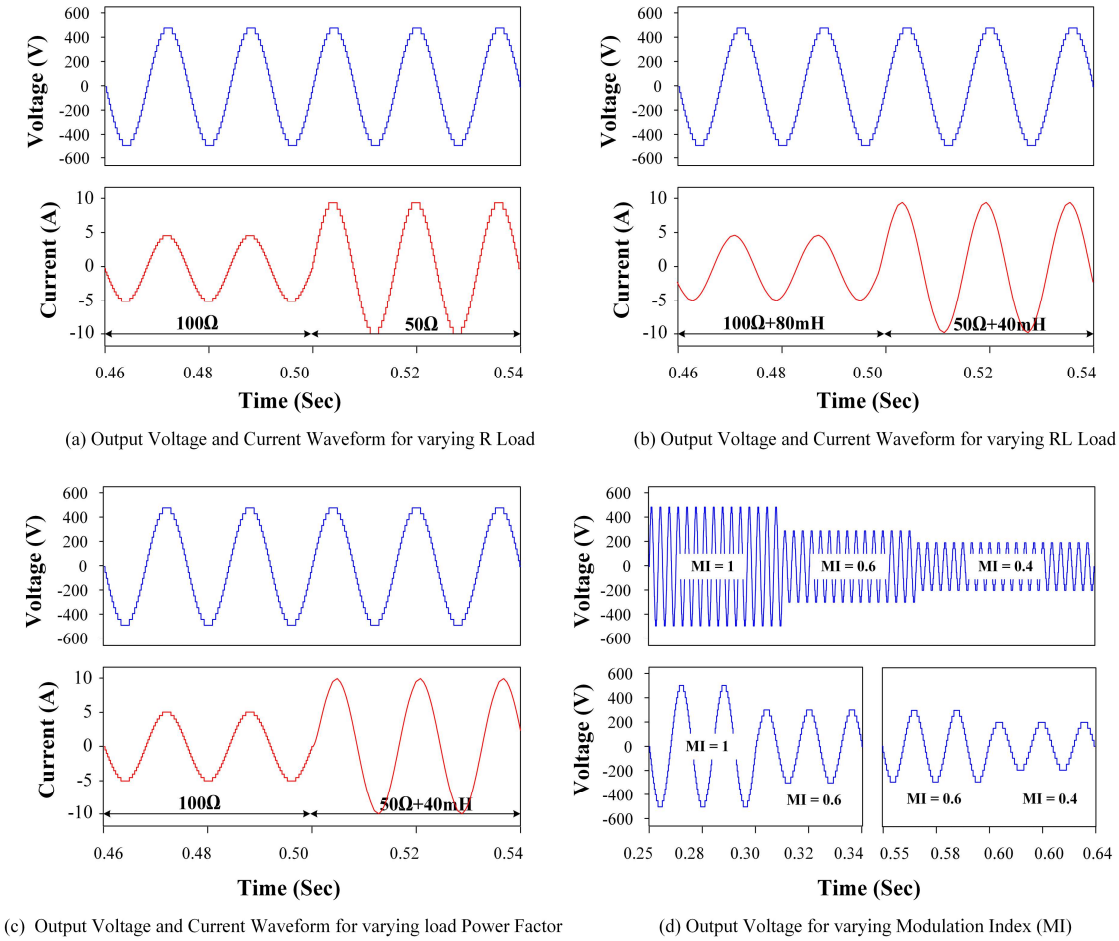
(a) Output Voltage and Current Waveform for R Load

(b) Output Voltage and Current Waveform for RL Load

(c) FFT Analysis for output voltage

(d) FFT Analysis for output current for RL load

Figure 5. Simulation results under constant loading conditions (blue for voltage, red for current).



(a) Output Voltage and Current Waveform for varying R Load

(b) Output Voltage and Current Waveform for varying RL Load

(c) Output Voltage and Current Waveform for varying load Power Factor

(d) Output Voltage for varying Modulation Index (MI)

Figure 6. Simulation results under dynamic loading conditions.

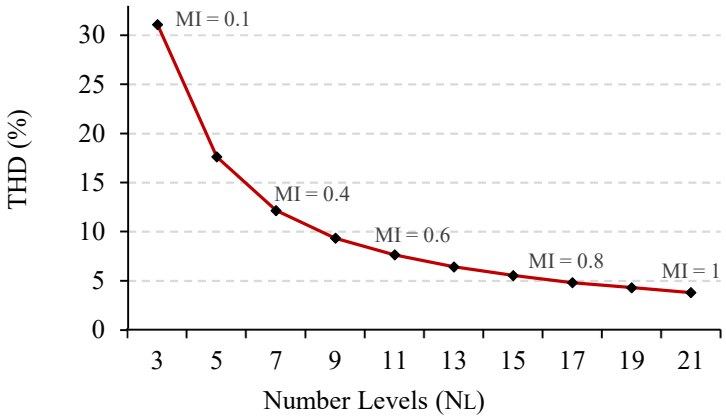


Figure 7. Effect of change in Modulation Index (MI).

3.2. Experimental Results

The real-time performance of the proposed topology is validated through laboratory testing. The hardware prototype is developed, as shown in Figure 8. The circuit uses IGBT FGA25N120 as a switch and a DSP board TMS320F28379D for PWM control signals. A driver circuit uses a TLP 250 optocoupler IC to drive the IGBTs. The circuit's experimental testing involves four DC sources in the ratio of V_1:V_2:V_3:V_4 = 1:3:2:4, voltage and current waveforms recorded using a Yokogawa DL 1640 digital oscilloscope. A power quality analyzer, Fluke 435-II, is used to observe the harmonics content in the output. Table 4 provides information on the parameters and equipment used for hardware testing.

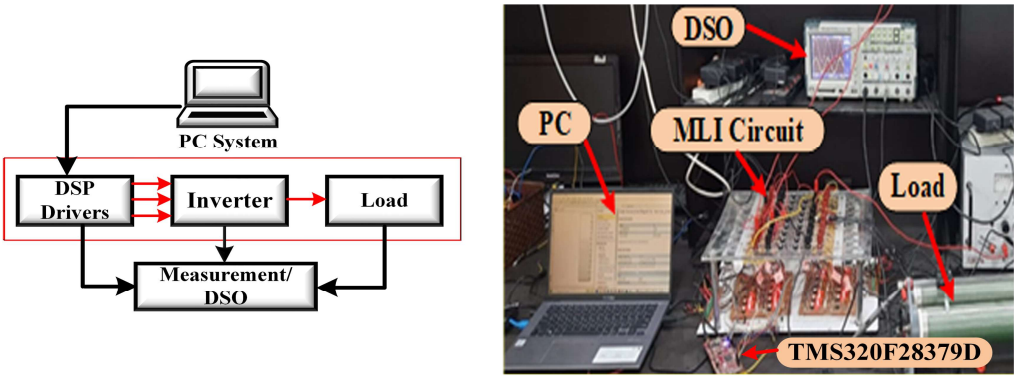


Figure 8. Experimental setup of the proposed MI-MLI Circuit.

Table 4. Experimental parameters and equipment.

Parameter/Device	Value/Type/Rating
DC Sources	V_1 = 6 V, V_2 = 18 V, V_3 = 12 V, V_4 = 24 V
Switches	IGBT, FGA25N120, 1200 V/25 A
Microcontroller	TMS320F28379D, 200 MHz
Driver IC	TLP 250
Digital Signal Oscilloscope	Yokogawa DL1640
Power Quality Analyzer	Fluke 435-II
Load Resistance	100 Ω, 200 Ω
Load Inductance	90 mH, 120 mH
Modulation Index	1, 0.8

The hardware results for constant and dynamic loading conditions are presented in Figure 9. The 21-level output voltage for a constant R load of 200 Ω with a peak value

of 60 V is shown in Figure 9a. The THD in output voltage is found to be 3.4%, as shown in Figure 9b. Figure 9c,d show the waveforms obtained at constant loading conditions. The R-load was set at 200 Ω, and the RL load was set at 100 Ω + 120 mH. The nature of the output current is sinusoidal for RL load, and the output voltage remains constant with a peak value of 60 V. The hardware result for dynamic loading conditions, depicted in Figure 9e, demonstrates the change in load from 200 Ω to 100 Ω. The load current smoothly increases while the output voltage remains constant. The effect of variation in the modulation index is depicted in Figure 9f. The modulation index was changed from 1 to 0.8, and the resulting waveform showed reduced voltage levels as the modulation index decreased. The results align with the simulation analysis, proving that the proposed topology performs satisfactorily in all conditions. The modulation index was changed from 1 to 0.8, and the resulting waveform showed reduced voltage levels as the modulation index decreased. The hardware results support the simulation analysis, demonstrating the satisfactory performance of the proposed topology under all loading conditions.

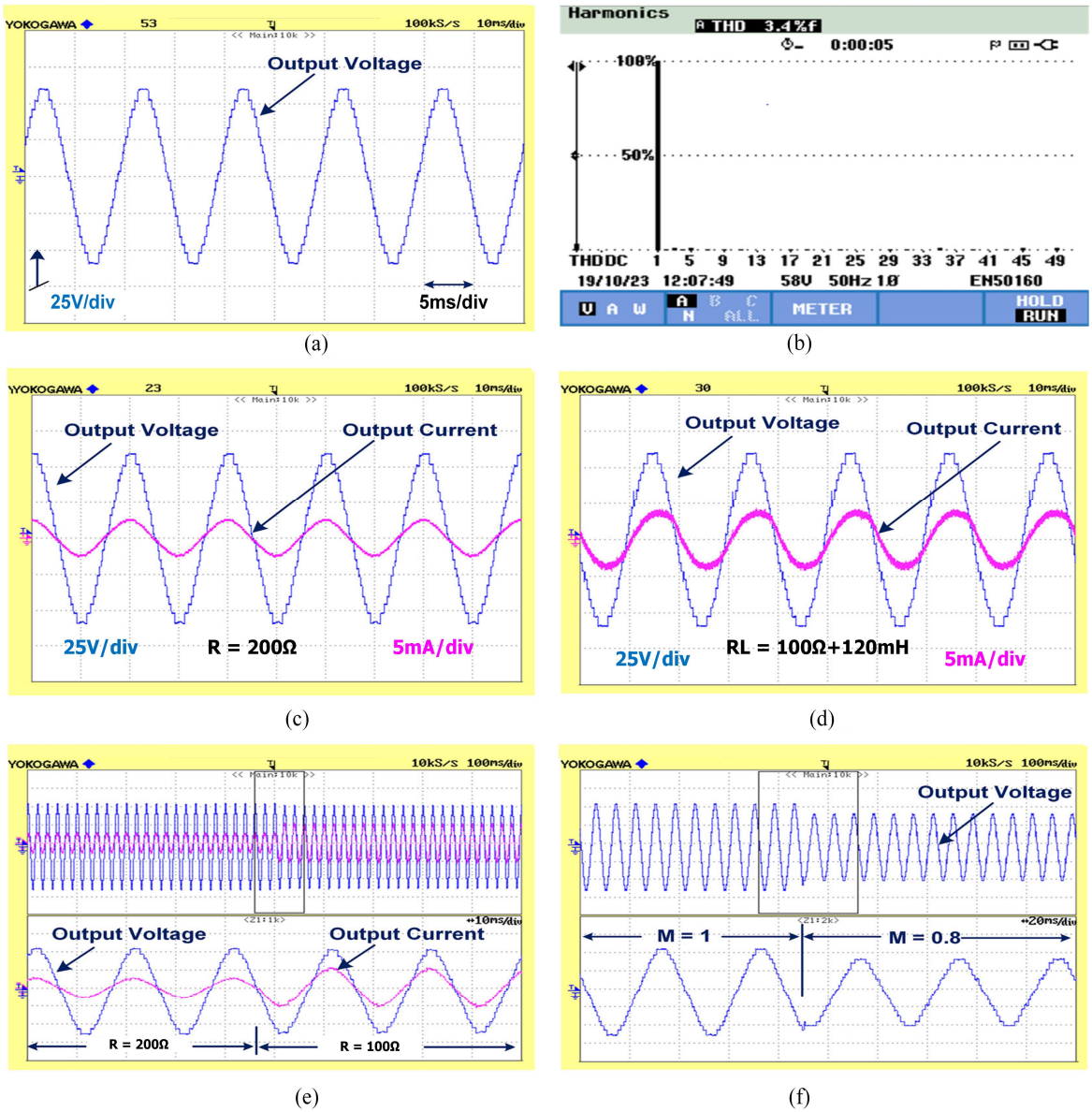


Figure 9. Experimental results of the proposed topology under constant and dynamic loading conditions.

4. Power Loss Analysis

Power loss analysis is crucial for the power converter design as it affects the performance. The main losses in the proposed circuit are the conduction loss (P_C) and switching loss (P_S). Conduction losses are more effective at low frequencies, while switching losses dominate at high frequencies. The conduction losses that occur during the conduction time of the switches can be calculated as [27];

$$P_{CS} = V_s i(t) + R_s i^{\beta}(t) \tag{8}$$

$$P_{Cd} = V_d i(t) + R_d i^2(t) \tag{9}$$

V_S and V_d indicate the On-state voltage drop and R_S and R_d represent the equivalent resistance of the switch and its antiparallel diode. The datasheet provides information on the value of constant β, which is affected by many factors. The total conduction loss of a switch is computed as:

$$P_C = Psc + Pcd \tag{10}$$

The average conduction loss of a converter is determined by the number of switches (N_S) and diodes (N_d) conducting at an instant 't', which can be calculated as:

$$P_C = \frac{1}{\pi}\int_0^{\pi} [Ns(t)\left\{V_s i(t) + R_s i^{\beta}(t)\right\} + N_d(t)\{V_d i(t) + R_d i^2(t)\}]dt \tag{11}$$

The energy loss is caused by turning ON and OFF, and the non-ideal operation of switches produces switching loss. The technique of nearest level modulation is implemented in this work to minimize switching frequency, hence lowering switching losses. The switching loss of semiconductors is affected by the voltage across the switch (V_{sw}), current flow through it (I_{sw}), switching frequency (f), turn ON (T_{on}), and turn OFF (T_{off}) time of the switch [28,29]. The switching loss Ps is evaluated as:

$$P_s = \frac{1}{6} f V_{sw} I_{sw} (T_{on} + T_{off}) \tag{12}$$

The proposed circuit's total power loss can be expressed as:

$$P_T = P_c + P_s \tag{13}$$

The efficiency is calculated as:

$$\eta = \frac{Pout}{Pout + P_T} \times 100\% \tag{14}$$

The proposed circuit's efficiency and power loss are calculated using PLECS software. The IGBT datasheet is utilized for the PLECS lookup table data with real loss statistics, while the IGBT IKW40N65ES5 is used for thermal analysis and loss computation. As can be seen in Figure 10a and b, respectively, the study computes conduction and switching loss at different loads (1 KW. 2 KW, 3 KW). Switching losses occur when voltage and current take a longer time to drop to zero during turns ON and OFF—higher switching frequency resulting in more loss. The proposed converter's low switching losses are attributed to its use of the low-frequency NLC PWM. Figure 10c depicts the variation of efficiency with total power losses. The efficiency of a converter is affected by total power losses, with higher power leading to increased conduction current and conduction losses, resulting in a decline in the converter efficiency. The proposed topology efficiency curve at different loads is shown in Figure 10d.

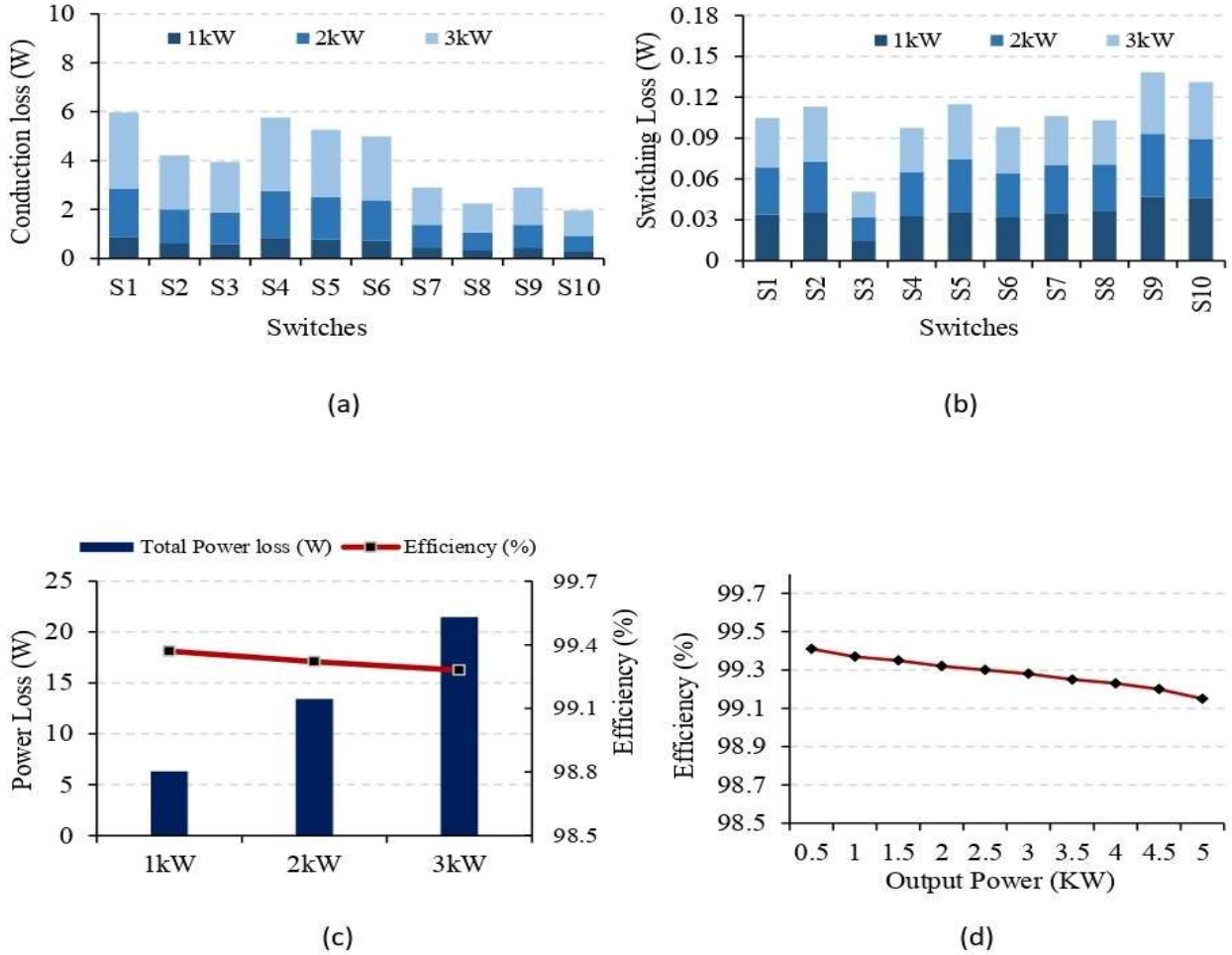


Figure 10. Power loss and efficiency curve under different loading conditions (**a**) Conduction losses (**b**) Switching Losses (**c**) Total Power Loss and Efficiency Curve and (**d**) Output Power v/s Efficiency Curve.

5. Comparative Analysis

This section compares the proposed topology with other similar asymmetrical multi-input multilevel inverter topologies available in the literature. The analysis considers parameters such as the number of output voltage levels (N_L), number of DC sources (N_{DC}), number of switches (N_{SW}), number of IGBTs (N_{IGBT}), gate driver circuits (N_{GD}), number of capacitors (N_{cap}), number of diodes (N_d), switch per level (N_{sw}/N_L), and cost factor per level (CF/Level). Table 5 summarizes the comparative analysis data and reveals that the proposed topology generates 21 levels of output voltage utilizing less device count and outperforms other MLIs due to its minimal value in the N_{SW}/N_L ratio and cost factor per level among all discussed topologies.

The topologies in [30–34] generate lower output voltage levels utilizing the same number of DC sources with a high switch per level ratio and cost factor per level. The topology in [31] required 12 IGBTs and 11 gate driver circuits for 15 levels of output, while the topology in [32] required 16 IGBTs and 14 gate driver circuits for 17 levels. The device count of these topologies is relatively high for less voltage-level topologies. If these topologies are cascaded for higher voltage levels, the device count increases significantly, affecting the inverter's cost. Another 17-level topology with four DC sources utilizing less device count is proposed in [33], but the cost factor per level of the topology is high. The 19-level topology proposed in [16] required three DC sources, 13 IGBTs, and 13 gate drive circuits. The device count of the topology is very high and also has a high value of switch per level and cost factor. Another topology in [34] generates 19-level output voltage

utilizing 4 DC sources and three capacitors. Due to the capacitors, the voltage balancing problem occurs, and the cost per level of the topology is high. The topology in [35] required six DC sources, 10 IGBTs, and three capacitors for 21 levels. However, the cost factor per level is higher than the proposed topology, making it less feasible. The topology in [36] required the same number of DC sources as the proposed topology for generating 21-level output voltage. However, they utilize a large device count with a high switch-per-level ratio and cost factor. Another 21-level topology with the same cost per level and switch per level ratio is proposed in [27]. However, the device count of the topology is higher than the proposed topology. From the above discussion, the proposed topology is suitable for medium and high voltage applications as it requires the least device count, a good switch per level ratio, and a cost factor for generating higher voltage levels. It outperforms other parameters and has less control complexity, demonstrating superior performance, economic viability, and increased stability despite potential outperformance in certain departments.

Table 5. Comparison with other asymmetrical Muti-Input Multilevel Inverter (MIMLI) topologies.

Topology	N_L	N_{DC}	N_{SW}	N_{IGBT}	N_{GD}	N_{Cap}	N_d	N_{SW}/N_L	CF/Level
[30]	15	4	8	10	8	0	0	0.53	1.78
[31]	15	4	11	12	11	0	0	0.73	2.14
[32]	17	4	14	16	14	2	0	0.82	1.97
[33]	17	4	9	12	9	0	0	0.53	1.76
[16]	19	3	13	13	13	0	0	0.68	1.69
[34]	19	4	10	11	10	3	2	0.53	1.79
[35]	21	6	10	10	10	3	0	0.48	1.57
[36]	21	4	12	16	12	4	0	0.67	1.88
[27]	21	4	12	12	12	0	2	0.48	1.53
Proposed	**21**	**4**	**10**	**14**	**10**	**0**	**0**	**0.48**	**1.53**

6. Application of the Proposed Topology

Distributed Energy Resources (DERs) [37–39], also referred to as DERs, are small-scale power generation and storage devices, including solar photovoltaic systems, hydroelectric generators, fuel cells, micro-turbines, wind turbines, and energy storage systems. Integrating DERs into the power grid is crucial due to the growing demand for renewable energy, improved grid resilience, and reduced greenhouse gas emissions [40–42]. Multilevel inverters convert DC power from renewable sources or energy storage systems [43] into AC power that is compatible with the grid. Unlike traditional two-level inverters, multiple DC source multilevel inverters use multiple voltage levels to synthesize an AC waveform, resulting in reduced harmonic distortion and improved efficiency. However, connecting multiple sources to a multi-input multilevel inverter (MIMLI) presents some challenges. The main challenge is to synchronize the incoming power, as sources may have variable voltage levels, which can cause distorted output waveforms, stress on the inverter, and uneven power distribution. To address the issues, DC–DC converter interfaces are required at each input source to maintain the desired voltage and current, and advanced control algorithms are designed to maintain complex power distribution and desired output voltage profile. The schematic diagram of the proposed multiple DC source inverter topology fed with different distributed resources is shown in Figure 11. Furthermore, the proposed topology can be used in electric vehicles [44–46].

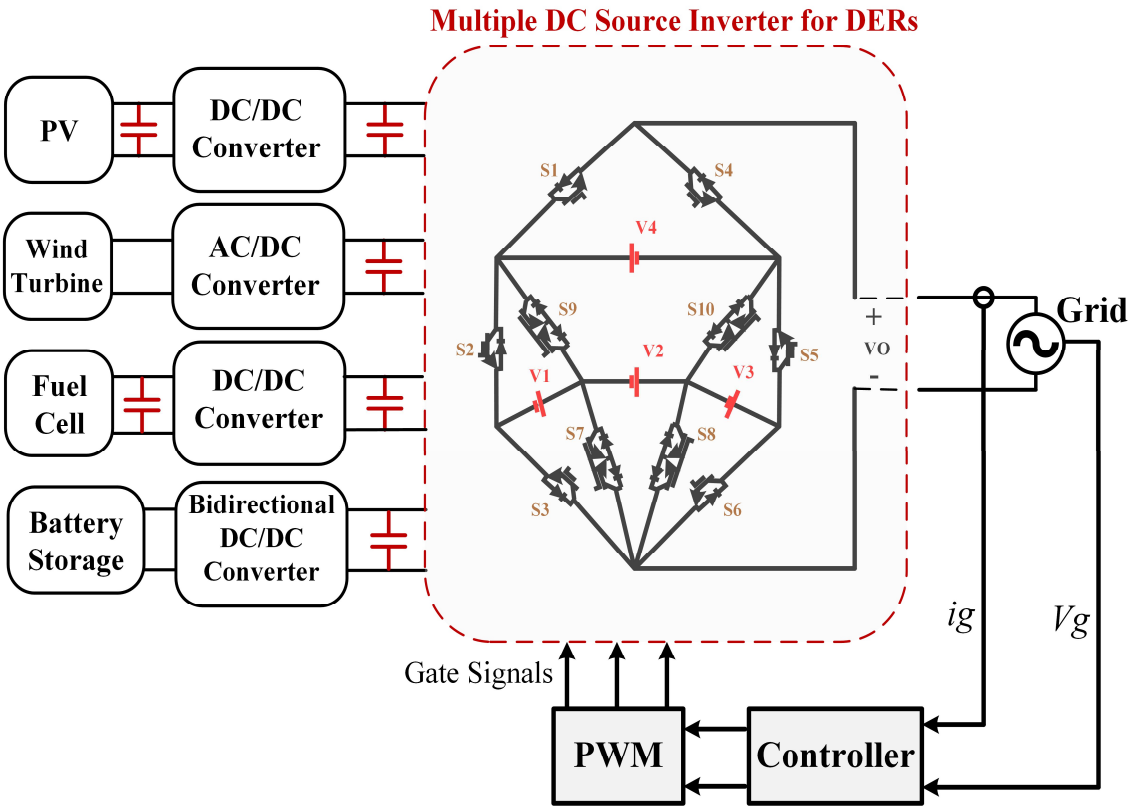


Figure 11. Schematic diagram of the proposed topology fed with different distributed resources.

7. Conclusions

This work presents a multi-input multilevel inverter topology (MIMLI) for distributed energy resources suitable for both symmetric and asymmetric configurations. The asymmetric configuration offers 21 output levels, requiring four DC sources in a 1:3:2:4 ratio, and 10 switches. The topology is evaluated in MATLAB under both static and dynamic loading conditions in an asymmetrical mode of operation using the low-frequency PWM technique. The proposed topology achieves less than 5% THD in output voltage and current, making it suitable for grid-tried applications. The conduction and switching losses are calculated using PLECS software, and an efficiency curve is presented to demonstrate implementation feasibility. Comparative analysis is conducted using recent literature to validate the proposed topology regarding device count for inverter design. The proposed circuit demonstrates its ability to generate desired voltage levels with fewer components and validate proper functioning through simulation and experimental results.

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