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Simulation and Modelling for SiC High Power Diodes

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Abstract

Simulation and Modelling for SiC High Power Diodes

by Yaren HUANG

The excellent electrical and thermal material properties of SiC and the rapid advances in SiC process technology made it a promising and favorite candidate as a functional material for SiC high power devices, among others, for SiC MPS diodes, which play a decisive role in energy conversion and transmission using electric power facilities.

However, restricted by the nature of the unipolar current operation, SiC MPS diodes have been considered to be the optimum structure for a blocking voltage up to 3.3kV. This work focuses on the optimization of 4.5kV SiC MPS diodes, especially on the trade-off between the nominal and the surge current operation modes. Through the physical insights gained by extensive numerical simulations, an analytical compact model describing the impact of the geometrical and physical parameters on this trade-off has been developed and shows a high degree of accuracy in the verification with physical device simulation results obtained by the commercial TCAD software package *Sentaurus*®.

Inspired by this compact model, we propose several novel device structures aiming at an improved trade-off relationship between high nominal current density and high surge current capability.

In parallel with the theoretical investigations, test samples of new SiC MPS diodes were fabricated and experimentally characterized. However, due to the non-ideal Ohmic contacts of the samples under test, the fabricated devices were found to operate in unipolar mode only, with negligible resistance modulation even under high forward voltage. We offer physical explanations of these non-ideal behaviors and a potential solution to be realized in the next re-design cycle.

Robustness against cosmic radiation is one of the essential topics that are crucial for ensuring the reliability of high power facilities. We performed a numerical analysis comparing Si and SiC PiN diodes with the same blocking voltage of 1.5kV. This comparison reveals that, in contrast to Si diodes, the peak current originating from the impact of a cosmic particle is nearly independent of the applied reverse voltage in SiC diodes. The consequence is a lower threshold reverse voltage, above which the cosmic ray-induced damage occurs, but also a lower failure rate at high reverse voltage. This conforms with experimental findings recently reported for such SiC diodes [1].

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Kurzzusammenfassung

Simulation und Modellierung für SiC-Hochleistungsdioden

von Yaren HUANG

Die herausragenden elektrischen und thermischen Materialeigenschaften von SiC und der rasante Fortschritt in der SiC-Prozesstechnologie haben es zu einem vielversprechenden und favorisierten Funktionsmaterial für SiC-Hochleistungsbauelemente gemacht, unter anderem für SiC-MPS-Dioden, die bei Energiewandlung und Energieübertragung mit Hilfe von elektrischen Hochleistunganlagen eine wichtige Rolle spielen.

Bedingt durch die Natur unipolarer Stromleitung wurden SiC-MPS-Dioden bis jetzt als optimal geeignet für Blockierspannungen bis zu 3,3 kV betrachtet. Diese Arbeit konzentriert sich auf die Optimierung von 4,5 kV-SiC-MPS-Dioden, mit Blick auf einen guten Kompromiss zwischen dem Nenn- und dem Stoßstrom-Betriebsmodus. Aufgrund der aus umfangreichen numerischen Simulationen gewonnenen physikalischen Erkenntnisse wurde ein analytisches Kompaktmodell entwickelt, das den Einfluss der geometrischen und physikalischen Parameter auf diesen Trade-off beschreibt. Dessen Verifizierung anhand physikalischer Bauelementsimulationsergebnisse, die mit der kommerziellen TCAD-Plattform *Sentaurus*® errechnet wurden, beweist seine hohe Genauigkeit und Zuverlässigkeit.

Basierend auf unserem Kompaktmodell schlagen wir einige neuartige Bauelementstrukturen vor, die auf einen verbesserten Trade-off zwischen hoher Nennstromdichte und großer Stoßstromfähigkeit hoffen lassen.

Parallel zu den theoretischen Untersuchungen wurden Labormuster von neuartigen SiC-MPS-Dioden hergestellt und vermessen. Wegen der nichtidealen ohmschen Kontakte bei den getesteten Baumustern können diese jedoch nur im unipolaren Modus bei vernachlässigbarer Widerstandsmodulation auch bei hoher angelegter Vorwärtsspannung betrieben werden. Wir geben für dieses nichtideale Verhalten eine physikalische Erklärung und zeigen eine mögliche Lösung auf, die beim nächsten Redesignzyklus realisiert werden kann.

Die Robustheit gegenüber kosmischer Strahlung ist eines der wesentlichen Probleme, um die Zuverlässigkeit von Hochleistungsanlagen sicher zu stellen. Wir haben einen numerischen Vergleich zwischen Si- und SiC-PiN-Dioden mit der gleichen Sperrspannung von 1,5 kV durchgeführt. Dieser Vergleich zeigt, dass der Spitzenstrom, der duch den Einschlag eines kosmischen Teilchens verursacht wird, bei SiC-Dioden nahezu unabhängig von der angelegten Sperrspannung ist, im Gegensatz zu Si-Dioden. Hieraus ergibt sich ein niedrigerer Schwellwert für die Sperrspannung, ab der eine Schädigung des Bauelements zu erwarten ist, aber gleichzeitig eine geringere Ausfallrate bei hoher Sperrspannung. Dies deckt sich mit experimentellen Ergebnissen, die unlängst über derartige SiC-Dioden publiziert worden sind [1].

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Chapter 1

Introduction

1.1 Silicon Carbide Material

For more than 30 years, silicon carbide (SiC) material has been given particular attention as an advanced material for power electronics [2]. However, difficulties with the fabrication of high-quality SiC wafers imposed obstacles to the development of SiC power devices [3]. Today, after continuous improvements in the process technology, SiC power devices play an increasingly important role, especially in energy conversion, transmission, and distribution, where we encounter rising challenges with the handling of high power, high temperature and high operating frequency [4].

The outstanding performance of SiC power devices originates from its advanced material properties. A simple comparison of the key material properties between Si and SiC is shown in Table1.1. SiC can occur in a multitude of different crystalline polytypes, out of which very few are suitable for electronic devices, such as 4H-SiC, 6H-SiC, 3C-SiC. 4H-SiC has substantially higher carrier mobility than 6H-SiC and 3C-SiC, making it the most attractive for functional device material. Hence, we refer to 4H-SiC throughout this work when we use the term "SiC".

The wide energy bandgap E_g in SiC results in a very low intrinsic concentration n_i and a high critical electric field E_{crit} for the onset of impact ionization. The first one facilitates a low mobile charge carrier concentration, and consequently, a low leakage current in the blocking state (especially for Schottky diodes), while the second one allows for a high breakdown voltage even with a higher doping concentration N_{epi} in a thinner epitaxial layer (short L_{epi}). Although SiC has slightly lower carrier mobility than Si, SiC power devices can own a higher forward conductivity than Si power devices with the same blocking voltage, utilizing the high N_{epi} and short L_{epi}.

In high power applications, Si bipolar device structures, such as IGBT and PiN diodes, are predominantly used because Si unipolar devices cannot exhibit high forward conductivity if a high reverse

TABLE 1.1: Wide band-gap material properties of SiC in comparison with Si.

Material	**Si**	**4H-SiC**	**Unite**
Energy band gap E_g	1.12	3.26	eV
Intrinsic concentration n_i	$1.4 \cdot 10^{10}$	$8.2 \cdot 10^{-9}$	cm^{-3}
Critical field E_{crit}	0.23	2.2	MV/cm
Electron mobility μ_n	1400	950	$cm^2/(Vs)$
Relative Permitivity ε_r	11.8	9.7	1
Thermal Conductivity λ	1.5	3.8	$W/(cmK)$

blocking voltage is required. However, bipolar devices, in consequence of their operational principle, have the drawbacks of lower switching speed and higher power losses during the switching process.

The excellent material properties of SiC make unipolar devices competitive with respect to the reverse characteristics, and let them outperform Si bipolar devices with a view of faster switching speed and lower switching losses. Their superiority eventually allows for the optimization of the performance of the whole power system, such as minimizing the weight and size of cooling components and, consequently, a reduced cost for the power system as a whole.

As one of the most successful SiC power devices, the SiC merged PiN Schottky (MPS) diodes can provide breakthrough performance for a wide range of applications [5]. In our work, the merged PiN Schottky (MPS) structure rectifiers are extensively investigated.

1.2 SiC MPS Diodes

A very successful structure variant of Schottky diodes is the junction barrier Schottky (JBS) diode proposed in 1984 [6]. It has been experimentally proven that JBS diodes have dramatically reduced leakage current in the reverse operation. However, in consequence of unipolar conductivity, it shows a very limited capability under surge current conditions. As a result of the positive temperature coefficient of the forward resistivity, a surge current stress can easily lead to thermal runaway and device failure or destruction.

With a device structure similar to that of a JBS diode, the silicon-based Merged PiN Schottky (MPS) rectifier was first proposed and experimentally demonstrated in 1998 [7]. It features a superior reverse recovery behavior in comparison with PiN diodes. In 2006, with a view to improving the surge current capability, SiC MPS diodes had been realized using an industrial fabrication process; they show excellent performance. Hence, they are considered the 2nd generation of SiC Schottky diodes [8].

A 2-D cross-section of a conventional structure of MPS diodes is displayed in Fig. 1.1. It consists of two functional parts: A Schottky diode (Schottky contact) connected in parallel with a PiN diode (Ohmic contact). Combining the inherent advantages of each of the diode, MPS diodes are able to feature, at the same time, a low threshold voltage and a high surge current capability in the forward direction as well as a high breakdown voltage and low leakage current in the reverse direction, and besides a fast switching speed.

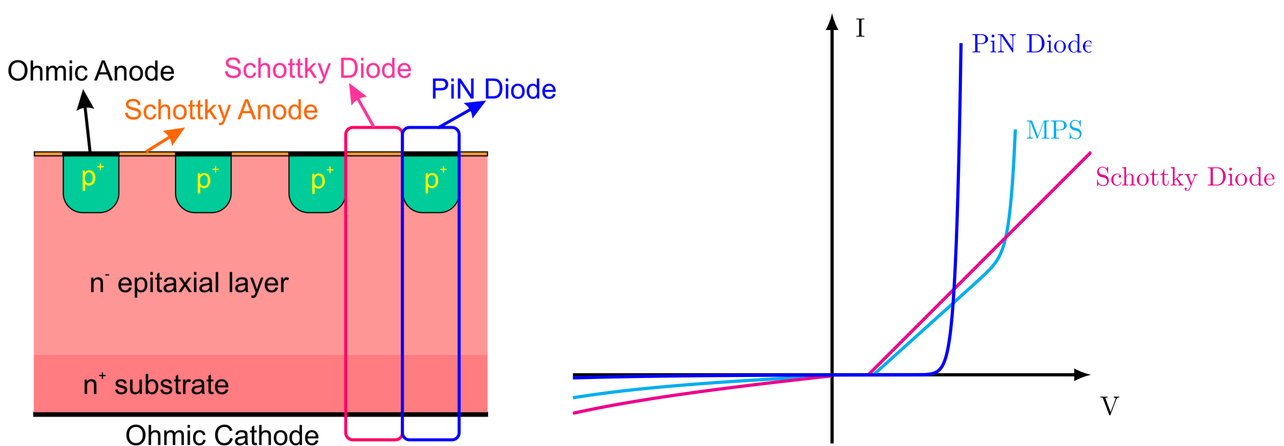


FIGURE 1.1: 2-D cross-section of a conventional structure of MPS diodes and the comparison of typical I-V characteristics among PiN diode, Schottky diode, and MPS diode.

In the forward characteristics of MPS diodes, we find two operating regimes: the unipolar mode under a relatively low forward voltage and the bipolar mode under a higher forward voltage. The unipolar operation of the Schottky diode substructure leads to a low threshold voltage for the onset of the forward conduction and, thus, low power losses. The bipolar operation of the PiN diodes enables a high surge current capability, avoiding premature heating that may lead to thermal runaway. In the nominal operation mode of MPS diodes, the current is mainly conducted by the majority charge carriers in the intrinsic epitaxial layer (= electrons). As long as the applied voltage is larger than the threshold voltage of the Schottky contact, MPS diodes are forward-conductive with the current flowing through the Schottky contacts. The inherent p^+n^- junctions keep still because the forward bias voltage is not high enough to trigger carrier injection by the p^+-islands. This situation changes once the anode voltage is further increased and exceeds a certain value V_{turn}. The p^+n^-junctions become forward biased and start injecting minority carriers (holes), leading to a drastic increase of the density of electrons and holes in the epitaxy layer, forming a highly conductive plasma. As a consequence, we observe a substantial reduction of the electro resistance of the epitaxial layer. This combination of unipolar and bipolar operation makes MPS diodes feasible with a forward threshold voltage similar to that of JBS diodes, but a much higher surge current capability and thermal robustness [9] [10] [11].

Concerning the reverse characteristics, MPS diodes operate in the same way as JBS diodes. The MPS concept has been adopted and implemented in many commercially available devices. The underlying key idea is to reverse bias the p^+n^-junctions between neighboring Schottky contacts, when the device is in the blocking state. Under reverse bias, the depletion regions around the p^+n^-junctions expand into the n^- region to such an extension that the depletion regions of two neighboring p^+n^- junctions can pinch off the channels of leakage current flowing through the Schottky contacts. As a result, the leakage current caused by the undesigned barrier lowering in the Schottky contacts is drastically reduced.

Considering the switching characteristics, SiC MPS diodes show similar excellent dynamic behavior as it is known from SiC Schottky diodes. This is a consequence of the low level of stored plasma charge, which leads to a low reverse recovery current compared to PiN diodes. The stored plasma charge density depends on the total effective percentage of p^+- junction area, which should be tailored with respect to the trade-off between surge current capability and reverse recovery leakage current. Additionally, the regions aside from the Schottky contacts speed up the removal of stored charge during the turn-off process, leading to a faster switching speed.

1.2.1 Nominal Current vs. Surge Current Capability for 4.5kV SiC MPS Diodes

Due to their excellent device performance, SiC MPS diodes have been investigated intensively. The blocking voltage has been upgraded from 600V in 2006 [8], over 1.2kV in 2014 [12] and up to 1.7kV in 2018 [11]. However, the MPS structure is considered as the best concept only for blocking voltage up to 3.3kV [13], where the forward on-state resistance of unipolar devices is still acceptable. With increasing blocking voltage and, hence, epitaxial layer thickness, the trade-off between nominal current and surge current capability is becoming a more and more demanding challenge [14]. In order to exceed this limit, 4.5kV SiC MPS diodes need novel device structures [15].

1.2.2 Nonideal Ohmic Contact

The two major challenges in the fabrication process of SiC power devices are producing a top-quality epitaxial layer and incorporating low-resistance Ohmic contact, in particular in the p-type material [16]. Nonideal Ohmic contacts have quite detrimental impacts on the device performance of 4.5kV SiC MPS diodes [17].

1.3 Cosmic Radiation Reliability of SiC Diodes

Cosmic radiation has been identified as a decisive factor for power device reliability, especially for high power devices [18]. Due to its wideband gap material properties, SiC power devices are supposed to exhibit higher robustness against single-event burnout (SEB). However, many reported experiments revealed that SiC Schottky diodes experience SEB at unexpectedly low reverse bias voltage and low linear energy transfer (LET) value. In contrast to Si power devices, permanent damage leading to increased leakage current is observed in SiC devices [19]. Predictive device simulation models have to be developed so that the failure and destruction mechanisms can be analyzed in detail and identified for the relevant device structures, with a view to designing novel device structures with harder ruggedness against SEB.

1.4 Scope of this Work

The purpose of this work is to gain reliable insights into the inner electronic behavior of state-of-the-art SiC power devices, in particular SiC MPS diodes, with a view to enhancing their performance in the next device generation. To this end, comprehensive predictive-numerical simulation and analytical compact modeling have been employed, based on high-fidelity physical device models, which have been validated with reference to fabricated test samples and industrial prototypes. The scope of all these analyses comprises of the exploration of the safe-operating area of such devices, including the confinements and limitations. The required computer simulations were performed using the well-proven commercial TCAD platform Synopsys *Sentaurus*®.

Chapter 2 introduces the device structure of the 4.5kV SiC MPS diodes under investigation. Furthermore, it addresses the particular numerical challenges in the view of the peculiarities of SiC modeling, which required dedicated simulation strategies concerning convergence, accuracy, and spatial resolution by adaptive griddling.

In chapter 3, the dependence of the forward I-V characteristics on the physical and geometrical parameters of 4.5kV SiC MPS diodes is analyzed. Based thereon, an analytical compact model is formulated and validated to obtain a systematic summary of all these dependencies.

In chapter 4, the compact model is employed to deduce and illustrate the operation of a number of novel advanced device structures, aiming to improve the trade-off between nominal operation and surge current capability. These structures' superior performance, reflected in their forward characteristics, is demonstrated in comparison with the conventional structure of SiC MPS diodes.

In chapter 5 the discrepancy between simulated results and measured results obtained from the fabricated 4.5kV SiC MPS diodes is investigated. In order to identify the cause, physical device simulations, including the effects of degraded electric conductivity on the Ohmic contact and low minority carrier lifetime, are performed. It showed that the simulated results conform to the measured data, providing physical insights and explanations of the observed effects.

Chapter 6 deals with a highly topical problem, which is of critical importance to the reliability and robustness of any semiconductor device: single event burnout (SEB) caused by cosmic radiation. To this end, a detailed numerical analysis is presented, providing a comparative study of Si and SiC PiN diodes with the ion-induced current.

Finally, chapter 7 summarizes the most relevant findings and conclusions of this work and gives an outlook on future perspectives and topics.

Chapter 2

Numerical Simulation

All device simulations reported in this work were performed using the commercial simulation platform, Synopsys *Sentaurus*® TCAD. A typical sequence of the steps of a physics-based simulation comprises:

- Definition of a proper unit cell (SDE):
  Extract the smallest periodically repeatable unit cell from the real cell-arrayed device structure, according to its symmetry and periodicity. Build the unit cell structure with Structure Editor (SDE) or Process Simulator.
- Generation of a discretization mesh (Snmesh):
  Divide the unit cell into several domains with different spacing of the grid points, according to the gradients of the doping concentration and/or the electric field distribution.
- Physics-based continuous field simulation (Sdevice):
  Specify all relevant physical models, such as mobility and carrier generation/recombination, and their model parameters. Define the computation accuracy and the number of steps or simulation speeds of stationary or transient simulations.
- Post-processing of simulated results (Svisual):
  Visualize the numerical simulation results, such as charge carrier density and electric field profiles, using a graphical user interface (GUI). Analyze the physical effects governing the simulated phenomena and gain physical insights.

Following the sequence of the simulation step listed above, this chapter first introduces the simulation structure of the 4.5kV SiC MPS diode under investigation and the distribution of mesh nodes. Then we discuss several measures for avoiding convergence problems caused by the specific material properties of SiC. In the end, some recommendations for a judicious interpretation of the simulation results are given.

2.1 Simulation Structure

We start with the conventional stripe-shaped device structure of MPS diodes. The structure exhibits a long p^+-stripes in a periodic array alternating with the n^--doping below the anode contacts, as displayed in Fig. 2.1. In order to extract the 2D domain for simulation, the 3D device structure is first projected onto a 2D cross-section, which fully reflects all geometrical features of the original 3D structure. According to the symmetry and periodicity of the 2-D cross-section, it is further reduced to an elementary unit cell containing a half of the Schottky diode and a half of the PiN diode, as shown on the right side of Fig. 2.1. One should note that the simulation domain shown here contains the main functional parts only because the simulations based on it primarily refer to the forward characteristics.

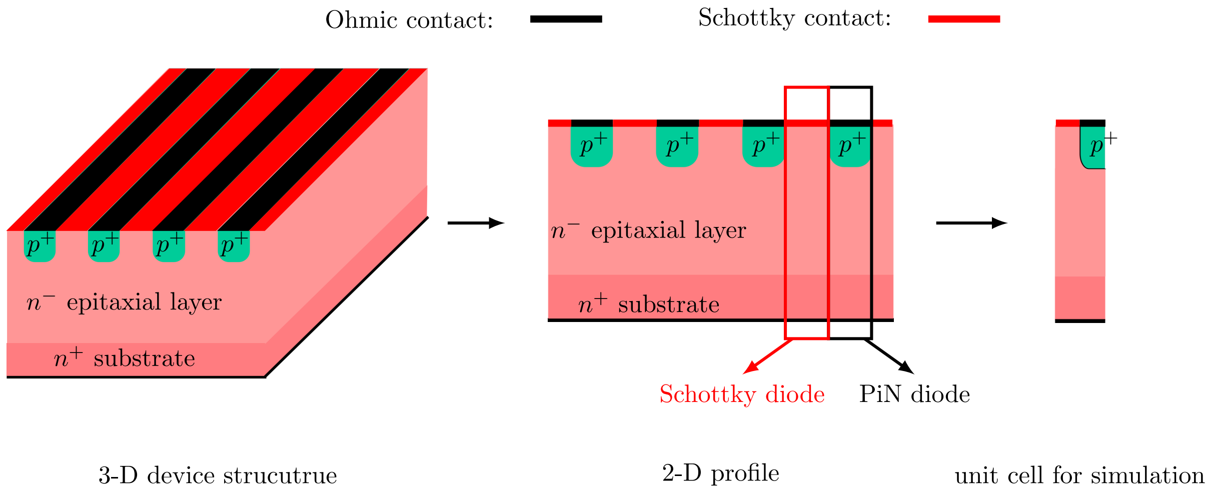


FIGURE 2.1: The 2D simulation domain is extracted by taking the smallest periodically repeatable unit cell of a 2D cross-section that is cut from the 3-D device structure. In such a way, the simulation domain is minimized and the computational expense stays affordable.

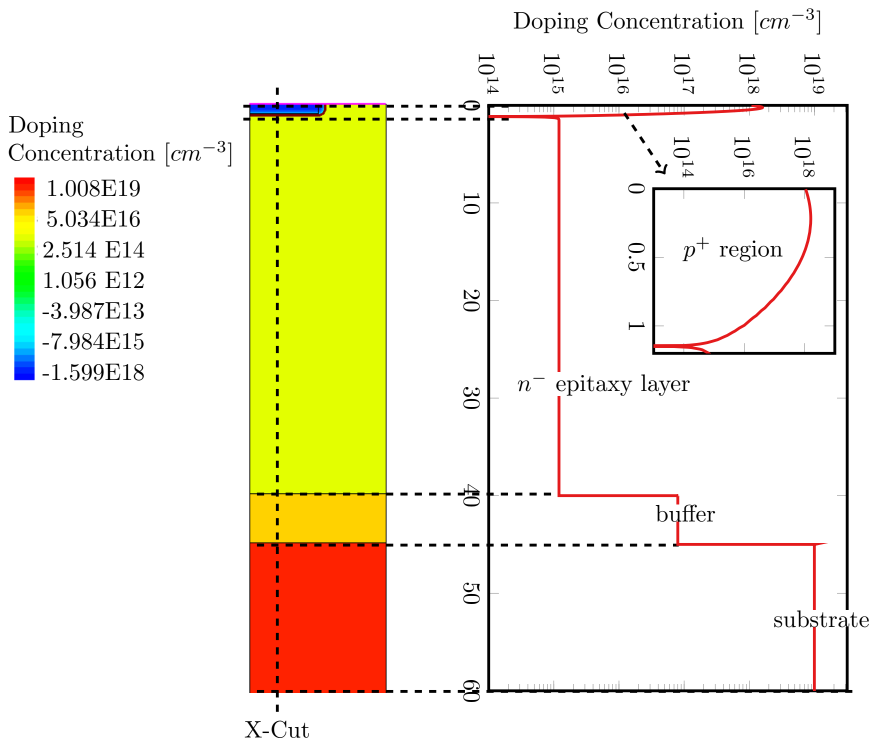


FIGURE 2.2: The unit cell for simulation built by the simulation tool "Seditor" and "Smash" is presented with a color bar indicating the doping profile inside the device. At the right-hand side the doping profile along an X-Cut is displayed.

In order to use the elementary unit cell for physical simulation, boundary conditions have to be specified using the structure editor SDE, including the real "physical" boundaries, such as Schottky contact and Ohmic contact, as well as the artificial boundaries, which are introduced to separate two neighboring elementary cells.

Next, the doping profile inside the elementary cell must be specified. Fig. 2.2 shows the 2-D distribution of the doping concentration for the 4.5kV SiC MPS diodes under investigation, where negative

values (blue) denote p-doping concentration and positive values (red) denote n-doping concentration. Obviously, the doping profile partitions the structure into four parts: p^+-region, n^--epitaxial layer, buffer layer and substrate. Each of them serves a specific function. For example, the p^+ region, which has a depth of only around 1.1 μm and is located underneath the contact metallization, is used to form a good Ohmic contact and to inject minority carriers in the bipolar operation mode. The 40 μm long n^--epitaxial layer with a constant doping concentration of $1.2 \times 10^{15} cm^{-3}$ has to sustain the high electric field in reverse operation mode. Below the epitaxial layer is a 5 μm long and $2 \times 10^{16} cm^{-3}$ doped buffer layer, the so-called field-stop layer. The substrate exhibits the highest doping level of $10^{19} cm^{-3}$ and a thickness of 360μm in the real device structure, forming a good ohmic contact on the cathode side and providing solid support to the whole device. In the simulation, the thickness of the substrate is reduced to 20 μm to avoid unnecessary computation expense since the electric resistance of the substrate is negligibly small.

In contrast to the other three domains with constant doping level, the p^+-region has an analytical doping profile defined by a Gaussian distribution function to approximate the actual doping profile generated by ion implantation. Although using an analytical doping profile avoids convergence problems arising in the simulation when we consider the sub-threshold low current regime, a more realistic doping profile obtained by the Monte Carlo method by employing the process simulation should be favored [20].

2.2 Numerical Implementations

In the physical simulations of 4.5kV SiC MPS diodes, numerical convergence problems originate from three sources mainly: the extremely low intrinsic carrier concentration n_i, the snap-back branch in the I-V characteristics, and the conflicts of the boundary conditions between the Schottky contact and the Ohmic contact. We suggest the following solutions for these three issues:

2.2.1 Additional Constant Carrier Generation Model

Due to its wide energy bandgap, SiC material has an extremely low intrinsic carrier concentration n_i ($\approx 10^{-8} cm^{-3}$) at room temperature. This leads to extremely varying values (by many orders of magnitude) of the charge carrier concentration encountered inside SiC devices under reverse bias. While the concentration of the charge carrier in the depletion region is approximately at the same order of magnitude as n_i, the carrier density in the substrate or p^+ regions can attain values as high as $10^{18} cm^{-3}$. Such a wide contrast ($10^{26} cm^{-3}$) in the order of magnitude causes a scaling problem in the numerical computation, resulting in inaccurate or non-convergent simulation results.

Therefore, in order to avoid this problem in reverse bias simulations, an additional constant charge carrier generation rate G_{cc} was added to the generation-recombination model used in "Sdevice". The value of G_{cc} has to be carefully selected according to the targeted simulated current density level. Fig. 2.3 shows the reverse characteristics of the SiC PiN diode obtained with three different values of G_{cc}, confirming that the leakage current is, as expected, proportional to the value of G_{cc}.

The reason is as following: From the 1-D current balance equation $\frac{dJ_n}{dy} = q(R - G_{cc})$ with the assumptions that $G_{cc} >> R$ and $J = J_n(y = L_{de}) = J_p(y = 0)$, the leakage current can be calculated as:

$$\frac{dJ_n}{dy} = q(R - G_{cc}) \quad \Rightarrow \quad I = J \cdot A = q \int_0^{L_{de}} -G_{cc} dy \cdot A = -qG_{cc} L_{de} A, \tag{2.1}$$

where L_{de} is the length of the depletion region and A is the total area of the device considered. Hence, the proportionality between G_{cc} and the leakage current can be well understood. Inserting the exact

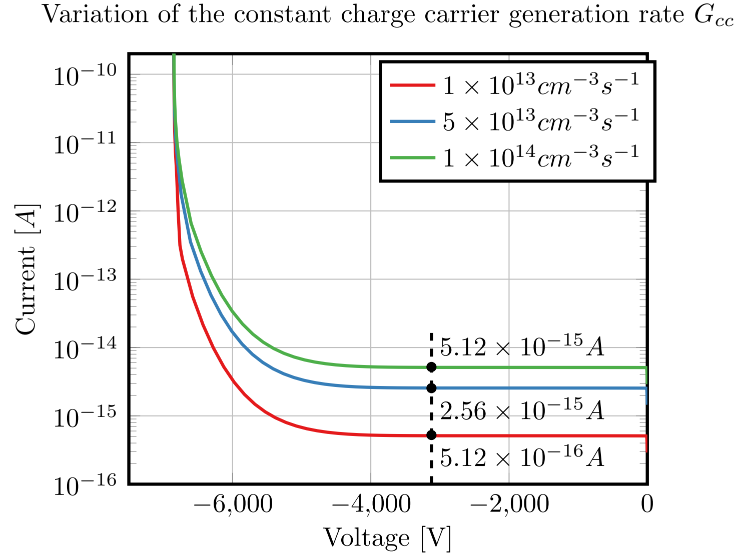


FIGURE 2.3: The simulated reverse characteristics with different values of G_{cc} of the artificial generation rate added to the physical carrier generation model.

value of L_{de} and A into this relation yields a leakage current that confirms well with the simulated values.

One may question whether this artificial constant carrier generation might impact the simulated breakdown voltage V_B, and not just slightly lifts the simulated reverse leakage current. However, as shown in Fig. 2.3, V_B stays the same for three different values of G_{cc}. Unlike the impact ionization rate, which strongly depends on the electric field, G_{cc} is fixed to the same value regardless of the applied reverse voltage and other operating parameters. Therefore, G_{cc} plays a perceptible role only in the calculation of the leakage current and becomes negligible compared to the rapidly increasing impact ionization rate once the avalanche breakdown is triggered.

2.2.2 External Series Resistance

In a quasi-stationary simulation with voltage-controlled, one needs to specify the maximum and the minimum value of the bias voltage step ΔV. Of course, a large step size is desirable since it accelerates the simulation speed. On the other hand, a small step size is required to obtain convergence and high accuracy of the numerical solution, in particular when the simulated quantity, such as the avalanche current in reverse-biased power devices (see Fig. 2.4.I), dramatically rises with the bias voltage. In this case, ΔV_{n+1} must be chosen by several orders of magnitude lower than ΔV_n.

Fig. 2.4.II shows an even more extreme case where a snap-back forward characteristic has to be calculated. ΔV_{n+1} does not only become infinitely small; it even takes a negative value. But with bias voltage ramping as a control condition, a negative step size $\Delta V_{n+1} < 0$ is prohibited.

One solution consists of attaching an external series resistor to the device contact. Instead of directly ramping the bias voltage at the contact of the simulated device, the value of $V_{applied}$ at the external terminal of the series circuit device/resistor is used for control. This means that the operating point is now determined by the intersection of the S-shaped device characteristic point with the load line.

$$\Delta V = \Delta V_{applied} - R_{ext} \cdot \Delta I. \tag{2.2}$$

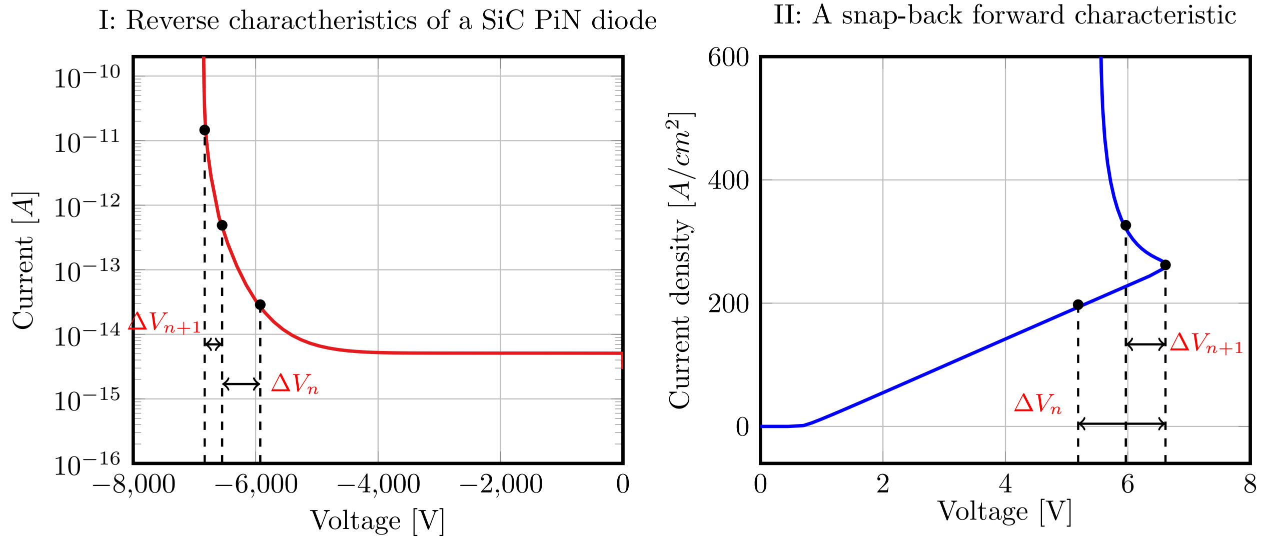


FIGURE 2.4: The simulation step ΔV_n and ΔV_{n+1} in the case of avalanche breakdown in reverse mode (left) and in the case of snap-back in forward mode (right).

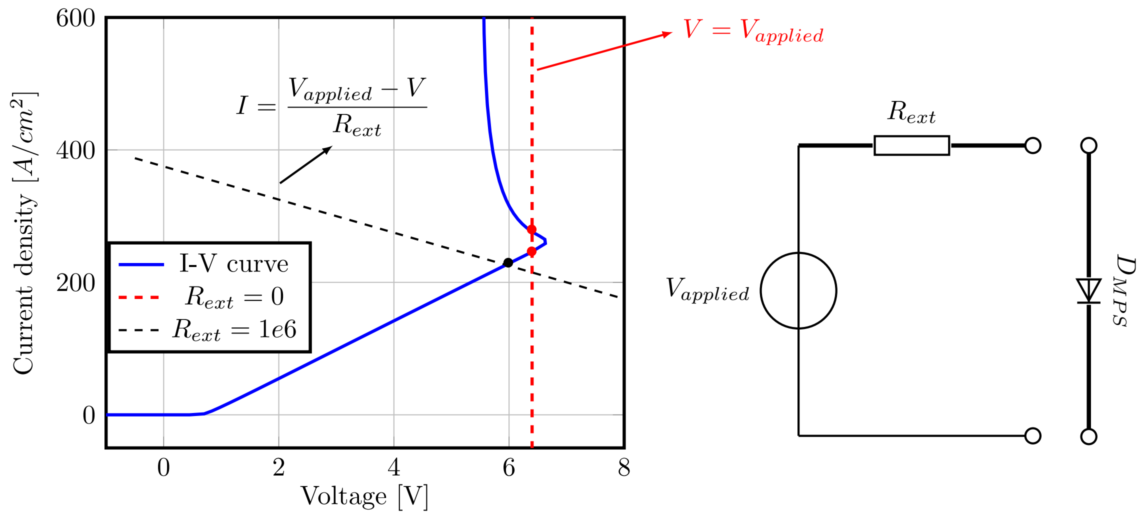


FIGURE 2.5: S-shaped I-V curve with snap-back branch and the series circuit with an external resistor to stabilize the operating point.

From this follows the ramping step

$$\Delta V = \Delta V_{applied} \cdot \frac{1}{1 + R_{ext} \cdot \Delta I / \Delta V}. \tag{2.3}$$

This means that ΔV is not controlled by $\Delta V_{applied}$ alone, but has a second increment $\frac{1}{1 + R_{ext} \cdot \alpha}$ where α denotes the respective slope $\alpha = \frac{\Delta I}{\Delta V}$ of the I-V characteristics. In the case of a small slope α, as encountered on the I-V branch before the onset of avalanche breakdown, we get $\Delta V \approx \Delta V_{applied}$. However, ΔV becomes several orders of magnitude lower than $\Delta V_{applied}$ in case of an extremely larger α (a steep curve) or even negative when α is negative.

Fig. 2.5 shows another illustration of how the operating points on the branch with negative differential resistance (NDR) may be stabilized by attaching an external load resistor. Each calculated

operating point (J, V) in the simulated I-V curve is the intersection point of two curves: $V = V_{applied}$ (marked with red color) and the I-V curve of the simulated device (marked with blue color). Under voltage control, the I-V curve is computed by varying the control quantity of $V_{applied}$ in each simulation step, shifting from minimum to maximum voltage. However, in the case of NDR, there may exist two intersection points so that the calculated result is not unique, which causes convergence problems in the computation. By attaching an external load resistor R_{ext}, the dashed load line is tilted (marked with black color), resulting in one intersection point solely. The value of R_{ext} should be carefully adjusted so that there is one intersection point only for all possible values of $V_{applied}$.

2.2.3 Decoupling of the Two Contact Models

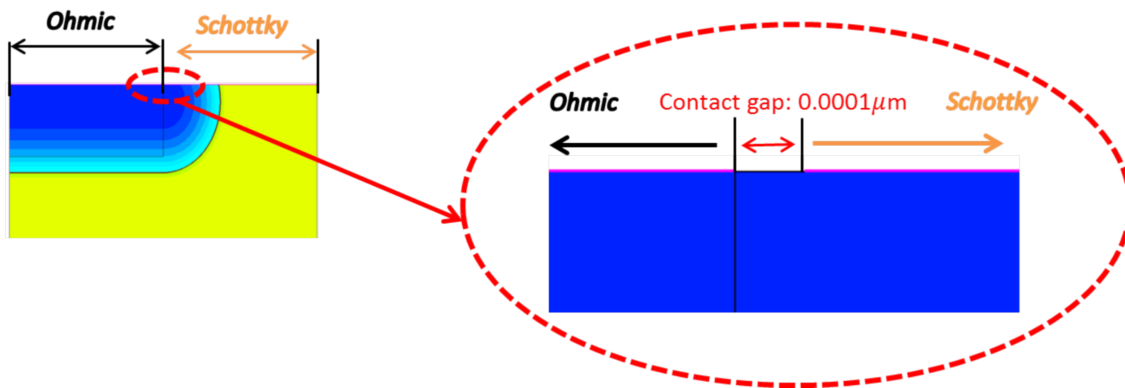


FIGURE 2.6: The MPS diode design involves two types of contact: Schottky and Ohmic contact co-exist at the anode of devices. Between these two contacts, a gap space of 0.1 nm is inserted to avoid non-convergence in the simulation.

Although the anode contact of a real MPS diode consists of one continuously connected metallization layer, we have to split this layer into two separate parts in the simulation model and use an Ohmic contact model and a Schottky contact model separately for each of them (see Fig. 2.6). This avoids numerical convergence problems caused by a physical inconsistency between the model assumptions leading to rapid variations of the electric field between these two neighboring contacts. To this end, we introduce a thin artificial contact gap, where no metallization and no electrical potential are assigned, placed between the Schottky contact and the Ohmic contact. This gap should be as small as possible to avoid any corruption in the simulation results. Therefore the numerically smallest possible gap size of 1nm was chosen in this work.

One should note that the boundary between Schottky contact and Ohmic contact is not exactly above the junction line between the p^+ and n^- region. The Schottky contact is applied to the whole n^--region and a small part of the p^+-region. This is made because of the lateral under-diffusion of the p^+-islands into the adjacent areas aside where the doping concentration is not very high and, hence, the Schottky contact model has to be favored. Consequently, the contact gap was placed on top of the p^+-regions.

The Schottky contact model and Ohmic contact models, describing two distinct physical situations, are formulated as two different boundary conditions for the electrical potential V. As shown in Fig. 2.7, assuming the same external voltage V_{ext} applied to them, the electrical potential at the boundary in the case of the Schottky contact on top of the n-type doping is $\phi_{schottky} \approx V_{ext} + \frac{1}{2}E_g - \phi_{BD}$, while the one in the case of the Ohmic contact above the p-type doping amount to $\phi_{ohmic} = V_{ext} - \frac{1}{2}E_g + (E_F - E_v) \approx V_{ext} - \frac{1}{2}E_g$. As a consequence, a jump in the electric potential

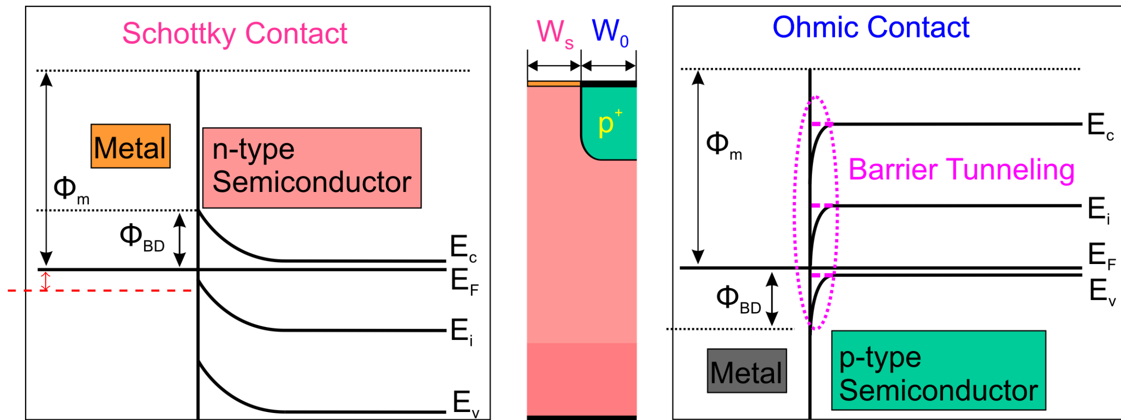


FIGURE 2.7: Energy band diagram for Schottky contact and Ohmic contact when $V_{applied}$=0 with ϕ_m as the work-function of metal, E_c as the energy for conduction band, E_v as the energy for valence band, E_i as the intrinsic energy level, E_F as the femi-energy level, ϕ_{BD} as the potential barrier at the contact boundary.

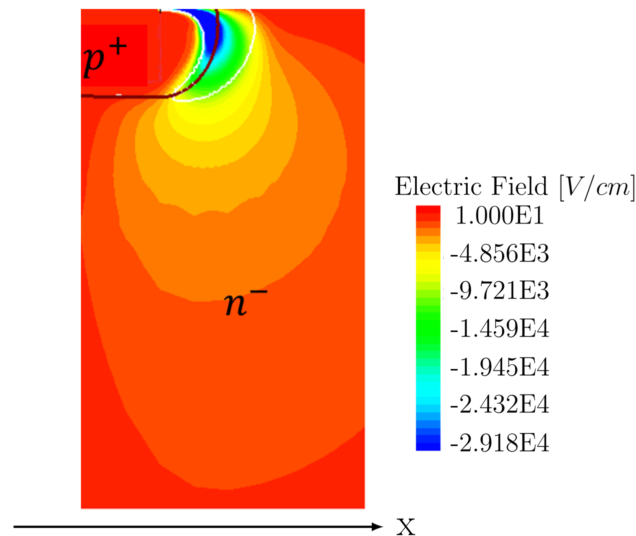


FIGURE 2.8: Electric field profile when the same bias voltage is applied to the Schottky contact and the Ohmic contact.

$\triangle V \approx E_g - \phi_{BD}$ occurs along the interface between these two contacts. Therefore, in device simulation, the Ohmic contact area and Schottky contact area should not overlap; instead, a small gap should be inserted between them.

Fig. 2.8 displays the electric field profile in horizontal direction inside a SiC MPS diode. It can be clearly recognized that there exists a strong electric field pointing from the Schottky contact to the ohmic contact in the vicinity of the p^+n^- interface. This electric field prevents holes from being injected from the p^+ region into the n^- region, which will be discussed in detail in Chapter 3.

2.3 Judicious Interpretation of Simulation Results

Sentaurus TCAD uses the well-established 'finite box discretization' method [21] [22] to solve Poisson's equation and the current continuity equations on a discrete network of sampling points. The numerical values of electron density, hole density, and electrical potential are calculated on a large but finite number of nodes, such as A, B in Fig. 2.9, in a 2D or 3D semiconductor device structure.

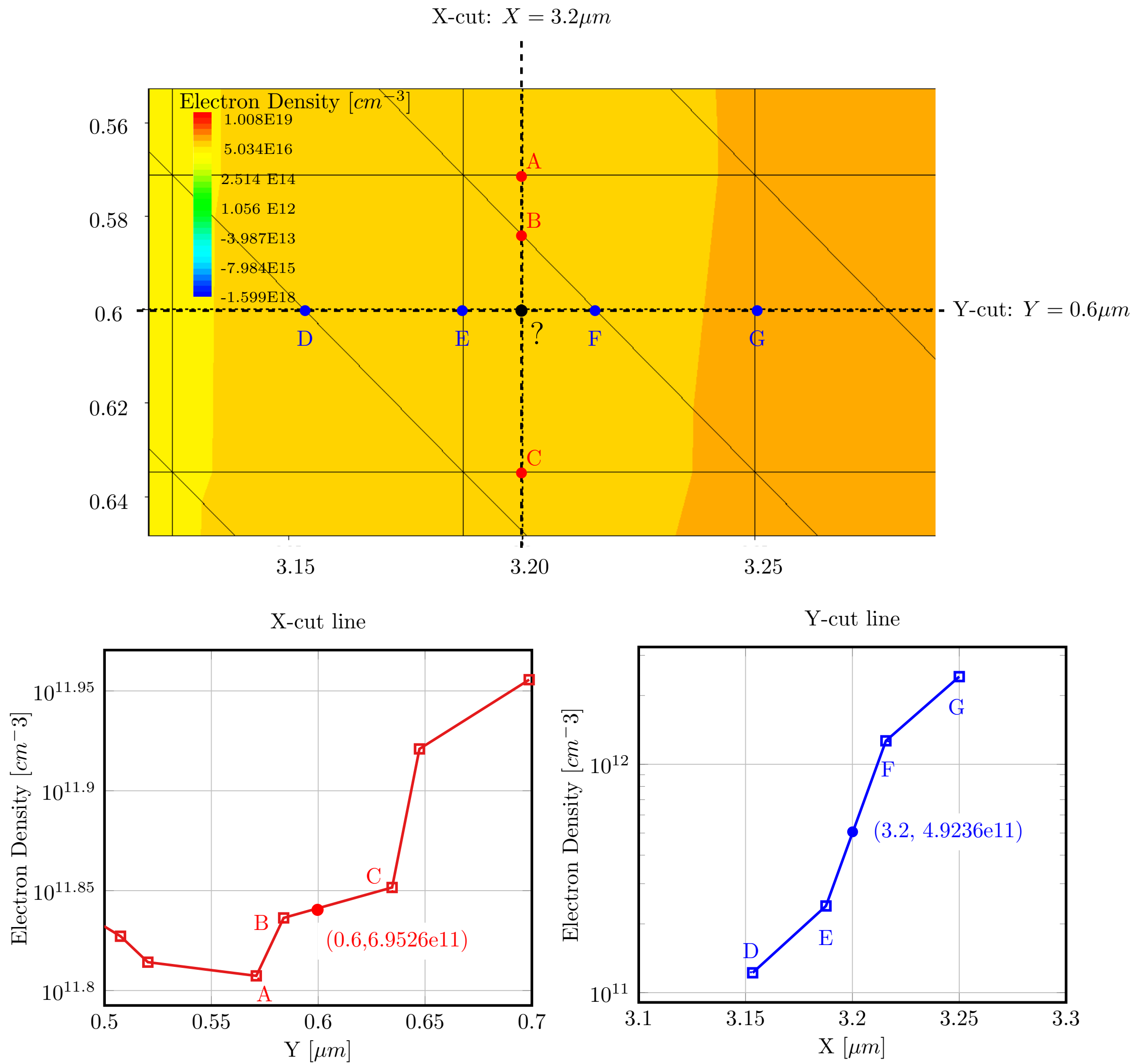


FIGURE 2.9: Different values of the electron density are obtained at the same position by taking an X-cut and a Y-cut.

For the points between nodes, such as the one marked with "?" in Fig. 2.9, the values of charge carrier density and electrical potential are interpolated in a post-processing step using their values on the grid nodes. However, different interpolation schemes used in the GUI Svisual result in different numerical values.

Fig. 2.9 exhibits an example of exploring the electron density at position $(3.2\mu m, 0.6\mu m)$. A plot of the electron density distribution along an X-cut line ($X = 3.2\mu m$) crossing Point A, B, and C is shown at the left lower corner. As mentioned above, only the values (marked with the square symbol) at the nodes and diagonal lines of the triangular elements are calculated. In order to complete the plot, linear interpolation is made among those calculated values. The probed value of the electron density at the position $(3.2\mu m, 0.6\mu m)$ is given as 6.9526e11 cm^{-3}.

However, when we follow the same above-mentioned procedure, but changing from an X-cut to a Y-cut, a much lower value of 4.9236e11 cm^{-3} is obtained. So the question arises: What is, within machine accuracy, a reliable value of the electron density at position $(3.2\mu m, 0.6\mu m)$? In order to find this out, one needs to probe the position in the 2-D displayed result directly.

This finding helped me resolve a confusion that puzzled me when I found that the post-processed values of the electron current density J_n' obtained using equation

$$J_n' = \mu_n n q \nabla E_{Fn}, \tag{2.4}$$

where the gradient of the quasi-Fermi potential ∇E_{Fn}, the carrier density n and carrier mobility μ_n are on the same cut line, did not confirm with the one directly acquired in GUI Svisual on the same cut line.

Another misinterpretation could occur when locating the peak value of a physical quantity, since the peak value may actually sit between two nodes instead of at one node. Of course, one may argue that this will happen only if the mesh spacing is not fine enough. However, there are simulations where the mesh will never be fine enough unless it moves time-adaptively to the areas where steep gradients of field quantities require an ultra-fine resolution. An example of this is described in Chapter 6 of this thesis.

Chapter 3

Analytical Models for 4.5kV SiC MPS Diodes

This chapter focuses on the forward characteristics of 4.5kV SiC MPS diodes, where two key parameters, $J_{F,nom}$ and V_{turn}, representing the nominal operating current density and the surge current capability of MPS diodes are crucial for an optimized design. An optimum forward characteristic of SiC MPS diodes should exhibit a high $J_{F,nom}$ for low forward voltage, and a sufficiently low V_{turn} at which the bipolar operation mode is triggered in order to avoid thermal runaway.

With a view to finding the optimum device structure, comprehensive device simulations were performed to explore the dependence of V_{turn} and $J_{F,nom}$ on the relevant geometrical and physical parameters. A trade-off relationship between V_{turn} and $J_{F,nom}$ was found.

Based on a high amount of collected data, analytical models for $J_{F,nom}$ and V_{turn} were formulated, and their accuracy was validated by comparison with the results from device simulation. One should keep in mind that these analytical models refer to the conventional stripe-array structure of 4.5kV SiC MPS diodes, as displayed in Fig. 2.1.

3.1 Features of Typical Forward I-V Characteristics

As expressed by its name, an MPS diode features both unipolar operation like a Schottky diode and bipolar operation as it is typical for a PiN diode. Fig. 3.1 shows a typical forward I-V characteristic of 4.5kV SiC MPS diodes. It consists of two connected branches: One starts from the origin with a nearly linear increase of the unipolar current density up to the turning point B, where the transition from unipolar to bipolar current flow occurs; The second branch starts from B to C with an exponential increase of the forward current. These S-shaped I-V characteristics can be proper quantitatively described with three parameters: $J_{F,nom}$, V_{turn} and V_{surge}.

- $J_{F,nom}$: Forward-biased current density in nominal unipolar operation mode.

In consequence of the nature of unipolar current flow, there is a linear increase of current with rising forward voltage. $J_{F,nom}$ characterizes the nominal conduction capability of an MPS diode. It is defined as the current density obtained for a forward voltage of 2V that is roughly the double of the threshold voltage of the Schottky contact, but distinctly lower than the built-in potential of the p^+n^- junction, so that the device is still operating in the unipolar mode.

In the nominal unipolar operation mode, the incorporated PiN structure can be neglected. The MPS diode operates as a pure Schottky diode, except for the slightly higher forward resistance due to the loss of the conducting area consumed by the p^+ islands. From the 2D distribution of the hole density displayed in Fig. 3.1 (lower half), it is evident that a nearly negligible amount of minority carrier (hole) is presented in the n^--epitaxial layer. Therefore, the current flow is primarily sustained by the majority carriers (electron) passing the Schottky contact.

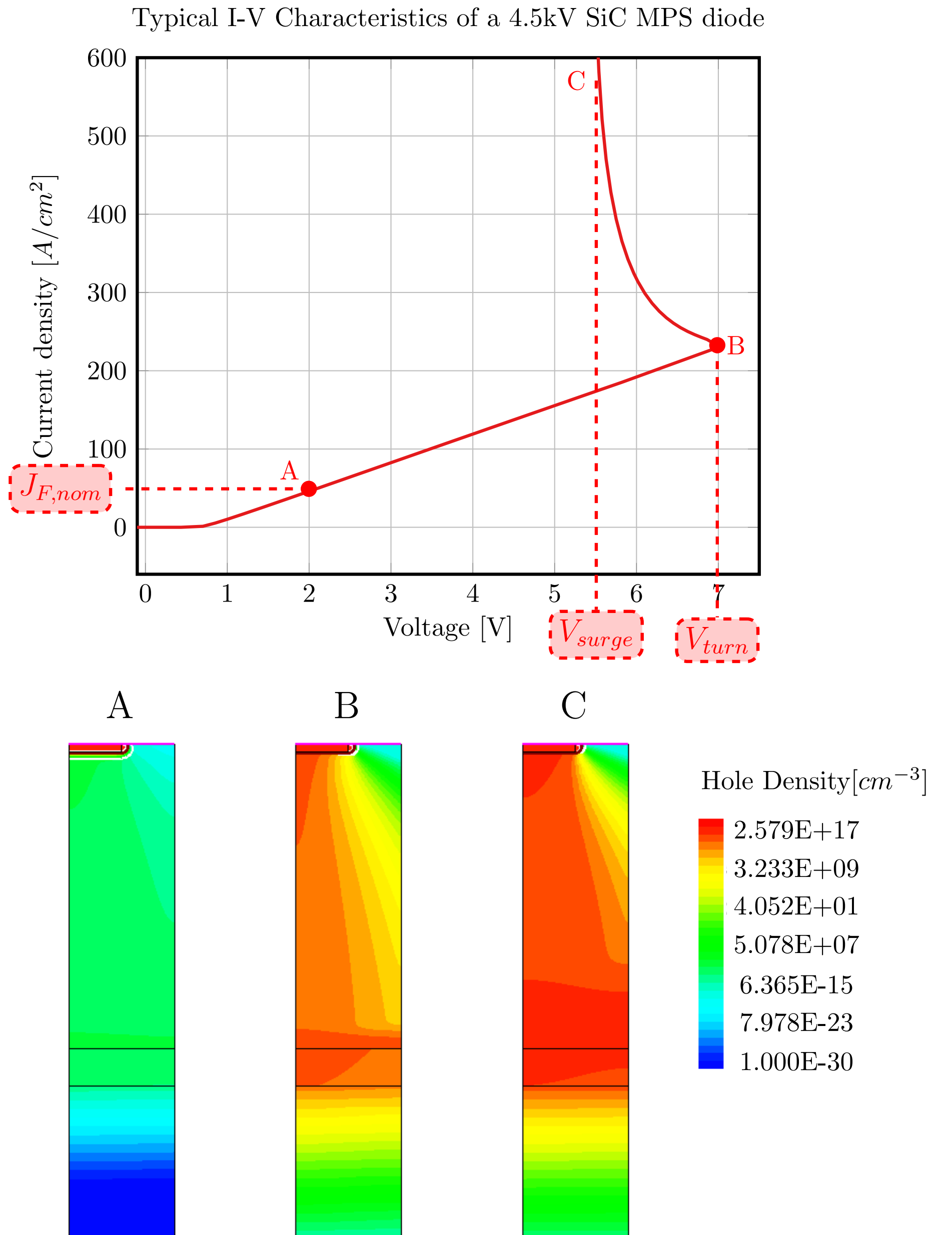


FIGURE 3.1: With increasing forward voltage, MPS diodes operate first with unipolar conduction and then switch to bipolar conduction. Here the hole density is boosted from a negligible amount up to a level that exceeds the majority electron density by a factor of 20, which results in a snap-back of the I-V curve.

- V_{turn}: Forward-voltage at which the MPS diode switches into bipolar operation mode;

With increasing forward bias voltage, where I-V curve reaches the turning point B in Fig. 3.1 (upper part), current density stops increasing linearly. From here on, the current density shows a steep exponential increase, while the voltage remains nearly the same or even snaps back. The underlying physical mechanism is as following: Once the applied voltage is large enough to forward-bias the incorporated p^+n^--junctions, the p^+ stripes start injecting minority carriers (holes) into the n^--epitaxial layer. Consequently, we observe a significant increase of the current density (see Fig. 3.1, upper part), as it is the characteristic of a PiN diode. The current is now sustained by an electron-hole plasma (see Fig. 3.1, lower part), which dramatically reduces the epitaxial resistance and leads to an exponential growth of current which now flows through both the Ohmic and the Schottky contact in

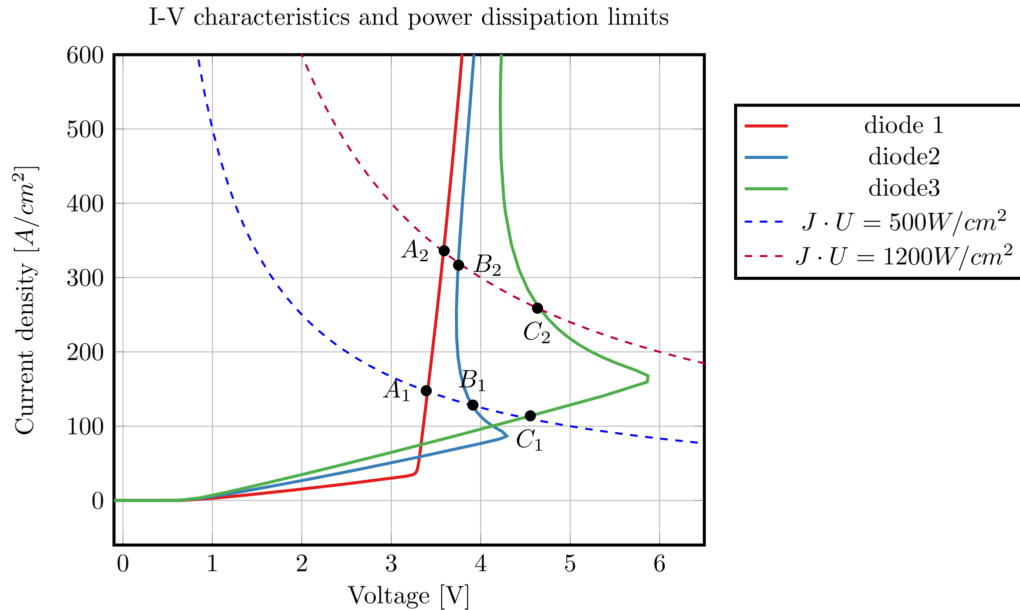


FIGURE 3.2: Forward I-V characteristics for three different 4.5kV SiC MPS diodes with various area ratios of Schottky contact and Ohmic contact, together with two different (fictitious) power dissipation limits. The intersection points A_1, B_1 and C_1 indicate the surge current limitation for these three diodes.

parallel.

V_{turn} is defined as the threshold which the bias voltage must exceed in order to trigger the hole injection by the p^+ emitters and to flood the interior of the device with an electron-hole plasma and, thus, to turn the device into the bipolar mode. For applications which require a high surge current capability, V_{turn} must be low enough to prevent a thermal damage of the devices.

- V_{surge}: The forward voltage attained after the MPS diode has been completely flooded with electron-hole plasma.

After entering the bipolar operation mode, different current-voltage relationships are possible. Some of them exhibit a negative differential resistance (NDR) branch, like the one shown in Fig. 3.1. Such a snap-back characteristic is to be expected if the hole injection rate is exceptionally high. Some of them feature a quasi-linear relationship, but with a lower forward resistance above V_{turn}. This happens if the hole injection rate is so poor that the decrease of the resistance of the epitaxial layer stops up to a certain level, despite of the further increasing forward bias voltage. V_{surge} is a figure of merit to quantify the surge current capability of the device under test. However, one should note that this quantity very sensitively depends on the minority carrier lifetime in the bulk material and, therefore, on the fabrication process. But designing an analytical model for V_{surge} was out of the scope of this work.

3.1.1 Power Dissipation

Low V_{turn} and V_{surge} are required for conducting a high surge current density to avoid thermal runaway that eventually leads to thermal destruction. Fig 3.2 demonstrates I-V curves of three different 4.5kV SiC MPS diodes, which have different values of V_{turn} and V_{surge}. Under the power limit of $500W/cm^2$, only diode 1 and 2 can enter into bipolar operation mode, and as a consequence, they have higher surge current limits ($A1$ and B_1) than diode 3 (C_1). Diode 3 can be prematurely destroyed before entering into bipolar protection mode. Furthermore, in the case of higher power limitation of $1200W/cm^2$, although all diodes have the chance to enter into bipolar operation mode, diode 1 has

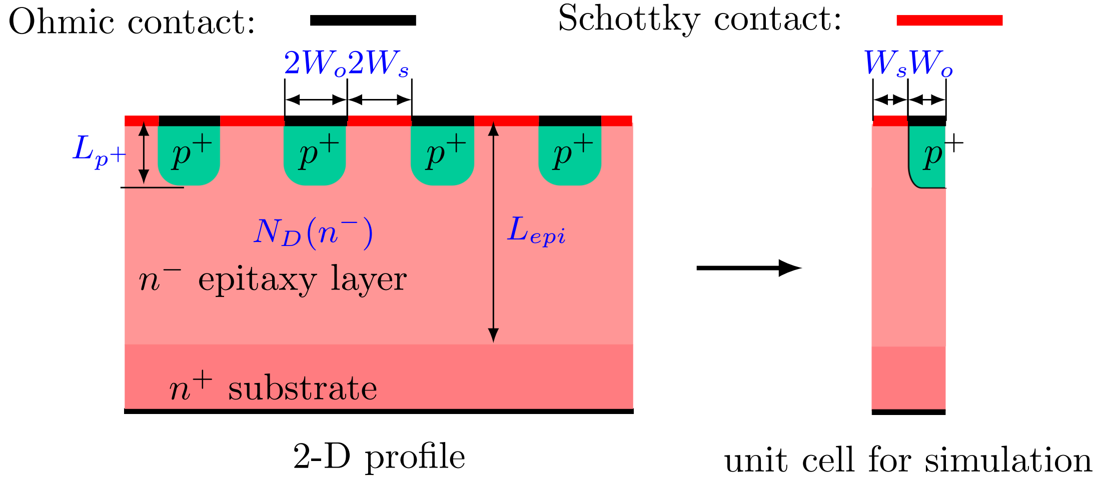


FIGURE 3.3: Left: the 2D cross-section of a conventional device structure of a SiC MPS diode; Right: Elementary half-cell used as simulation domain.

the highest surge current limits (A_2), followed by diode 2 (B_2) and diode 3 (C_2). Therefore a high surge current capability requires a small value of V_{turn}.

It is clear that a high $J_{F,nom}$ is desired to have low power dissipation during the nominal operation. However, high $J_{F,nom}$ and high V_{turn} often accompany each other, meaning a trade-off relationship exists between them [14].

3.2 Dependence of the Forward Characteristics of MPS Diodes on Various Parameters

In order to obtain an optimum 4.5kV SiC MPS diode, we studied the dependence of the trade-off relationships between $J_{F,nom}$ and V_{turn} on the geometrical and physical parameters.

3.2.1 Geometrical Parameters

The geometrical parameters under consideration are highlighted with blue color in Fig. 3.3, and their detailed definitions are as followed:

- W_o: Area of the Ohmic contact in one unit cell;
- W_s: Area of the Schottky contact in one unit cell;
- L_{p^+}: Depth of the p^+ implantation region;
- $N_D(n^-)$: Doping concentration of the n^- epitaxial layer ;
- L_{epi}: Length of the n^- epitaxial layer.

The variations of these geometrical parameters mentioned above lead to different forward I-V characteristics shown in Fig. 3.4. According to their influences on $J_{F,nom}$ and V_{turn}, we categorize them into the following three groups:

- $W_s \uparrow, N_D(n^-) \uparrow \quad \Rightarrow \quad V_{turn} \uparrow \text{ \& } J_{F,nom} \uparrow$

Increasing W_s makes the I-V characteristics of MPS diodes more similar to the ones of Schottky diodes, meaning a higher nominal current density $J_{F,nom}$, and less similar to the ones of PiN diodes, thus a higher value of V_{turn}. This could be easily understood, if one images a Schottky diode is the

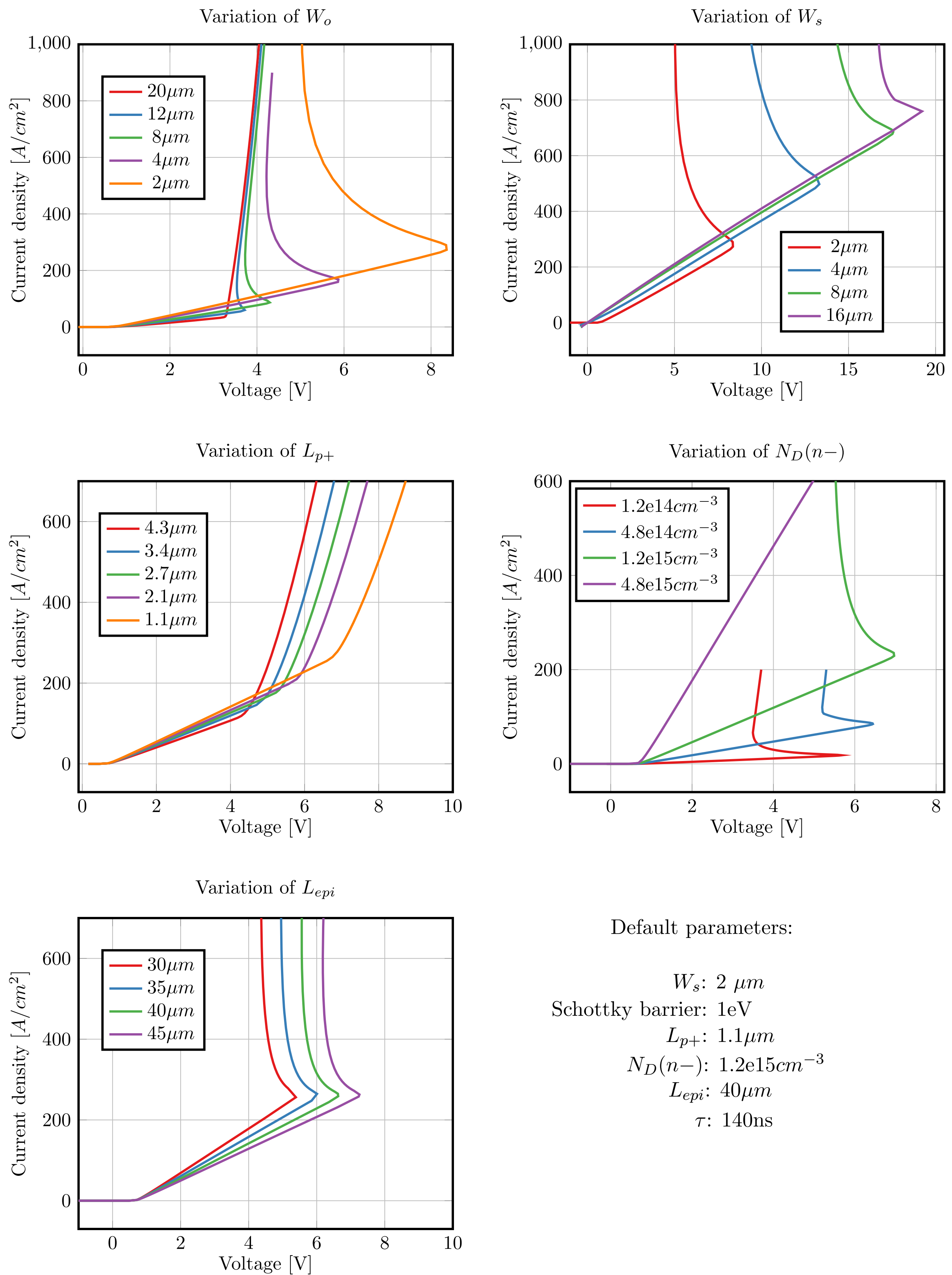


FIGURE 3.4: Dependence of forward characteristics of MPS diodes on geometrical parameters: W_o, W_s, L_{p+}, $N_D(n^-)$ and L_{epi}.

MPS diode with the Schottky area ratio $\frac{W_s}{W_s + W_o} = 1$, and an PiN diode is the one with $\frac{W_s}{W_s + W_o} = 0$. Besides, increasing W_s is increasing the cross-section of the unipolar current at the anode contact, resulting in a higher nominal current density $J_{F,nom}$.

An increasing $N_D(n^-)$ provides a higher majority carrier density for conducting the unipolar current, therefore a low resistance of the epitaxial layer and a high $J_{F,nom}$. However, a higher value of $N_D(n^-)$ leads to a higher built-in potential of the p^+n^- junction. A slight increment of V_{turn} is observed as well.

- $W_o \uparrow$,$L_{p^+}\uparrow \quad \Rightarrow \quad V_{turn} \downarrow$ & $J_{F,nom} \downarrow$

In contrast to the increment of W_s, an increment of W_o leads to a smaller Schottky area ratio of $\frac{W_s}{W_s + W_o}$, which certainly results in a lower value of V_{turn} and $J_{F,nom}$.

L_{p^+} is a geometrical parameter in the vertical direction, in parallel with the direction of the unipolar current flowing out of the Schottky anode. when L_{p^+} increases, more geometrical space is consumed by the p^+ islands, and less conducting area for the unipolar current remains, therefore $J_{F,nom}$ decreases.

However, a growing L_{p^+} brings a deeper p^+ junction, and therefore, the location of the initial injection of the minority carrier (hole) is further away from the anode where the potential boundary difference of $\Delta\phi$ (see Equation 3.10) is set. The location of the initial injection of the minority carrier is referred to as spot N in this thesis and sitting at the middle of the bottom of p^+ junctions. As a result, when L_{p^+} increases, the electrical potential ϕ_{n^-} around spot N decreases, promoting the forward bias of the p^+n^- junction and eventually offering a lower value of V_{turn}.

- $L_{epi} \downarrow \quad \Rightarrow \quad V_{turn} \downarrow$ & $J_{F,nom} \uparrow$

Unlike the other two groups, decreasing L_{epi} brings benefits to both surge current capability and nominal operation conductivity, namely a smaller value of V_{turn} and a larger value of $J_{F,nom}$. This is because the decreasing L_{epi} leads to a lower body-resistance shared by the Schottky diode and the PiN diode functional part. However, L_{epi} is predefined by the blocking voltage and there is limited space to be adjusted.

3.2.2 Physical Parameters

During the fabrication of the device, there are two physical parameters ϕ_{BD} and τ which can be adjusted according to the specific application requirements. The influences of ϕ_{BD} and τ on the forward characteristics of 4.5kV SiC MPS diodes are plotted in Fig. 3.5.

- ϕ_{BD}: Schottky barrier height of Schottky contact
- τ: Carrier lifetime in the epitaxial layer (Here the same value is taken for electron and hole.)

As a decisive parameter of the threshold voltage for nominal operation, Schottky barrier height has very limited choices and is normally set to be 1eV. However, such low Schottky barrier height leads to the dominance of the Schottky diode functional part in the MPS diode and, consequently, results in a high value of V_{turn}.

Carrier lifetime τ mainly influences the V_{surge}. During the bipolar operation mode, a longer lifetime promotes a higher minority carrier injection rate, and thus a higher bipolar current density and lower V_{surge}. Before bipolar operation is triggered, carrier lifetime τ has negligible influence on the device performance and consequently V_{turn} and $J_{F,nom}$ are barely affected. However, longer carrier lifetime causes higher switching power lost during the reverse recovery, another trade-off that designers should consider.

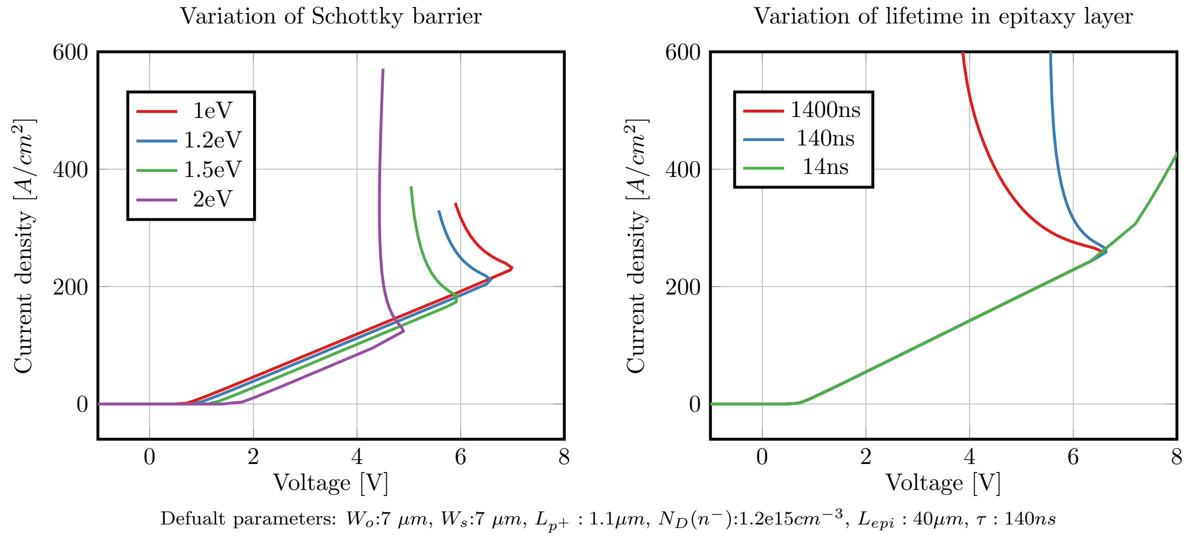


FIGURE 3.5: Dependence of the forward characteristics of MPS diodes on the Schottky barrier height and τ in epitaxial layer.

In summary, there is no simply adjustment of any geometrical parameter to achieve concurrently a lower V_{turn} and a higher $J_{F,nom}$. Further details and deeper physical insight understandings are necessary for optimizing the overall performance of the SiC MPS diodes.

3.3 Analytical Model of V_{turn}

Based on the physical mechanisms of unipolar and bipolar operations inside SiC MPS diodes, we provide an analytical compact model including the influences of all relevant physical or geometrical parameters for V_{turn}.

V_{turn} is the voltage drop on the MPS diode when the bipolar operation mode is turned on, i.e., the minority carrier injection is ignited. However, the minority carrier injection is a rapid process with positive feedback loops. The injection of holes irritates the injection of electrons from n^+ field-stop layer or n^{++} substrate, which accelerates the reduction of resistance in the epitaxial layer, and thus promotes the increment of V_{pn}, resulting in a further forward bias of the p^+n^- junction and exponential growth of electron-hole plasma density in the epitaxial layer. Therefore, if we can locate the spot (referred to as N) where the initial injection of holes occurs, we can know what conditions should to be fulfilled at this spot N for injecting the holes from p^+ region to n^- region. Then according to the required conditions, the required external applied voltage V_{turn} triggering the bipolar operation can be calculated.

3.3.1 Location of the Initial Injection of Minority Carriers: Point N

In a unit cell of the MPS diode, point N is the one who has the lowest electrical potential among those points sitting on the p^+n^- junction line. Therefore, it is essential to have an overview of the electrical potential distribution, which is constrained by the built-in potential of the p^+n^- junction and the potential boundaries at the anode and cathode.

The Built-in Potential V_{bi} of the p^+n^- Junction

The built-in potential V_{bi} of a p^+n^- junction is determined by the energy band gap of the semiconductor material and the doping concentration of p^+ and n^- regions. As shown in Fig.3.6, the built-in

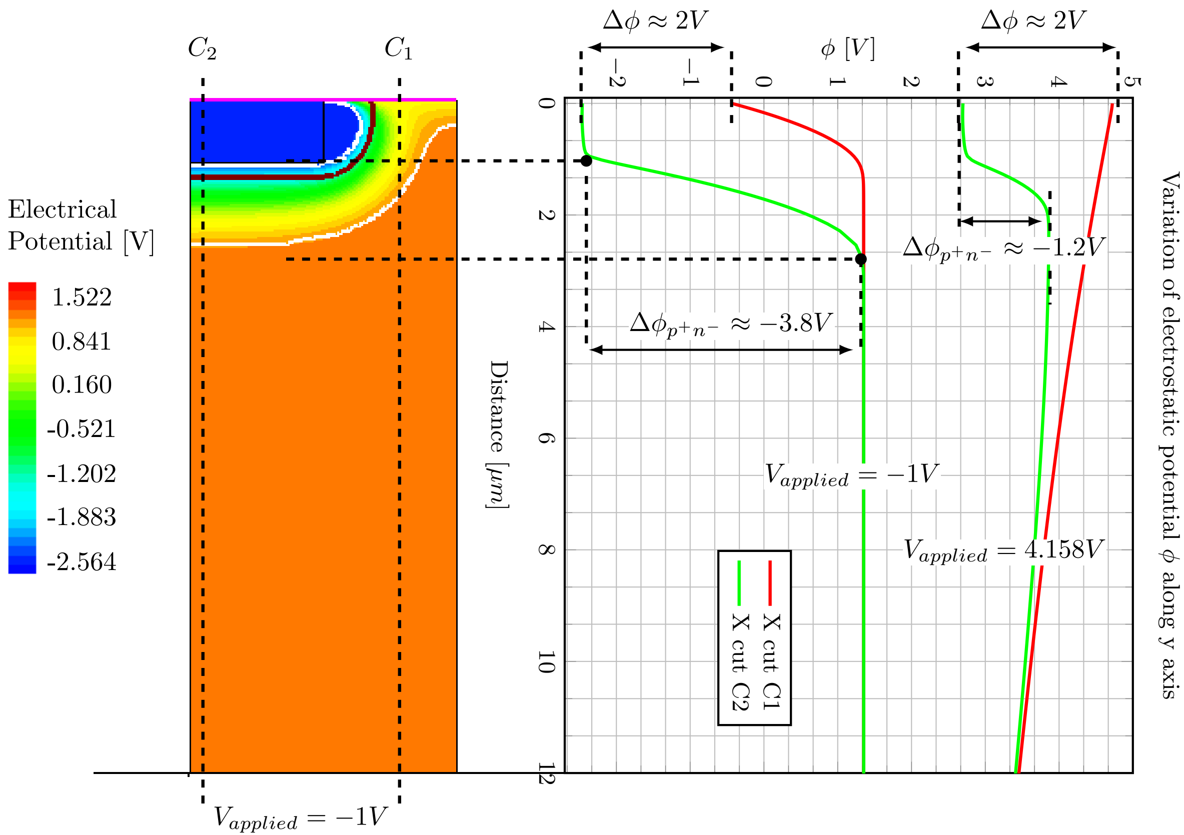


FIGURE 3.6: Different potential boundaries for Schottky contact and Ohmic contact, and the distribution of electrical potential inside an unit cell of the MPS diode. The white line indicates the depletion region around the p^+n^- junction.

potential V_{bi} forces a depletion region (space charge region) indicated by the white line around the p^+n^- junction. Inside the depletion region, the electrical potential has the most rapid variation along the cut line C_2, especially in case of a reverse bias p^+n^- junction.

Here we define a new quantity $\Delta\phi_{p^+n^-}$ as

$$\Delta\phi_{p^+n^-} == \phi_{p^+} - \phi_{n^-}, \tag{3.1}$$

where ϕ_{p^+} and ϕ_{n^-} are the electrical potential at the depletion lines in the p^+ and n^- region, respectively. The value of $\Delta\phi_{p^+n^-}$ can indicate to which extend the p^+n^- junction is forward or reverse bias. Different from the voltage drop V_{pn} on the p^+n^- junction, $\Delta\phi_{p^+n^-}$ can be directly extracted from the electrical potential distribution line shown in Fig. 3.6. And once $\Delta\phi_{p^+n^-}$ is known, V_{pn} can be calculated with

$$V_{pn} = \Delta\phi_{p^+n^-} - V_{bi}, \tag{3.2}$$

where V_{bi} can be calculated with the help of the example with $V_{applied} = -1V$ in Fig.3.6. In this case, p^+n^- junction is reverse bias and we can consider that the voltage drop V_{pn}=$V_{applied}$, and thus, V_{bi} is

$$V_{bi} = \Delta\phi_{p^+n^-} - V_{pn} = \Delta\phi_{p^+n^-} - V_{applied} = -3.8V + 1V = -2.8V. \tag{3.3}$$

With this calculated value of V_{bi}, the voltage drop V_{pn} in the case of $V_{applied} = 4.158V$ can also be known with

$$V_{pn} = \Delta\phi_{p^+n^-} - V_{bi} = -1.2V + 2.8V = 1.6V. \tag{3.4}$$

In this case, the p^+n^- junction is only slightly forward bias. In order to trigger an evident minority carrier injection, it requires $V_{pn}\approx V_{bi}$, i.e. $\Delta\phi_{p^+n^-} \approx 0$. Therefore, the location of the initial injection of minority carrier should be the one having the largest V_{pn}, meaning the highest $\Delta\phi_{p^+n^-}$=V_{pn}+V_{bi} (or lowest absolute value of $\Delta\phi_{p^+n^-}$), i.e. the lowest electrostatic potential ϕ_{n^-}.

The Potential Constraint Imposed by The Schottky Contact and The Ohmic Contact

The most important distinction between MPS diodes and other rectifiers is the co-existence of the Schottky and the Ohmic contact at the anode. These two contact models, as depicted in Fig. 2.7, have different conditions for the electrical potential at the boundary. Here, it is necessary to point out that the conventional reference of the electrical potential ϕ inside the semiconductor is the intrinsic energy level E_i [23]. That is

$$\phi = \frac{E_i}{-q}, \tag{3.5}$$

where q is the elementary charge.

- ***Assumption 1: Ideal Ohmic contact above p^+ region.***

In the Ohmic contact model, due to the extremely high recombination rate or barrier tunnelling rate at the boundary, no voltage drop between metal and semiconductor is assumed, i.e.

$$V_{applied} = \phi_m = \frac{E_{Fp}}{-q}, \tag{3.6}$$

where E_{Fp} is the Fermi-level in the p-type semiconductor and ϕ_m is the electrical potential in metal. The electrical potential ϕ_{ohmic} inside the p-type semiconductor at the boundary of the Ohmic contact is

$$\phi_{ohmic} = \frac{E_{Fp}}{-q} + \frac{E_i - E_{Fp}}{-q} = V_{applied} + \frac{E_i - E_{Fp}}{-q}. \tag{3.7}$$

At the boundary of Schottky contact, there is a Schottky barrier height ϕ_{BD} between the metal and conduction band (E_c) of semiconductor, written as

$$\phi_{BD} = \phi_m - \frac{E_c}{-q} = V_{applied} - \frac{E_c}{-q}. \tag{3.8}$$

The electrical potential $\phi_{schottky}$ at the boundary of Schottky contact for n-type semiconductor is

$$\phi_{schottky} = V_{applied} - \phi_{BD} + \frac{E_i - E_c}{-q}. \tag{3.9}$$

Consequently, the electrical potential difference $\Delta\phi$ between the two contact models at the anode, or more precisely, between p^+ and n^- region right below the anode is

$$\Delta\phi = \phi_{schottky} - \phi_{ohmic} = \frac{E_c - E_{Fp}}{q} - \phi_{BD}. \tag{3.10}$$

$\Delta\phi$ plays a particular important role in our analytical model and Equation 3.10 indicates several important properties of $\Delta\phi$:

- No dependence on the applied voltage;
  The electrostatic potential difference $\Delta\phi$ has no dependence on the applied voltage $V_{applied}$, the current density flowing through, or any other conditions. And this originates from the fact that the Schottky contact and the Ohmic contact are formed within the same anode metal, which forces synchronized steps of electrical potential to increase or decrease. This is proved

in Fig .3.6 where the same value $\Delta\phi \approx 2V$ between the cut line C_1 and C_2 under two different applied voltage $V_{applied} = -1V$ and $V_{applied} = 4.158V$ is found.

- A wider energy bandgap E_g results in a higher value of $\Delta\phi$;
  The dependence of the electrical potential difference $\Delta\phi$ on E_c and E_{Fp} in Equation 3.10 can well explains this point, which also reveals why the conflicts between Schottky contact and Ohmic contact is more severe in the SiC MPS diode than in the Si MPS diode.
- A high ϕ_{BD} leads to a low value of $\Delta\phi$.
  This explains why in Fig. 3.5, a high Schottky barrier height results in a small value of V_{turn}.

The electrical potential difference $\Delta\phi$ forces a reverse-bias state of the p^+n^- junction underneath the anode, and thus preventing the hole injection from the p^+ islands to the n^- epitaxial layer. This is especially the case for the region close to the anode contact, where the electrical potential difference between p^+ and n^- regions $\Delta\phi_{p^+n^-}$ is forced to stay at $\Delta\phi$. However, this constraint gets weaker with the increasing distance from the Schottky contact.

In Fig. 3.8, it is obvious that electrostatic potential underneath (or close to) the Schottky contact is the highest (indicated by red color). Along the current flowing path to the left and downwards, it decreases gradually to yellow or further to green color. Consequently, the location of the initial injection, called spot N in our work, should be the point furthest away from Schottky contact, thus, having the lowest electrostatic potential ϕ_N= min(ϕ_{n^-}) at the interface of p^+n- junction. As shown in Fig.3.7 or Fig. 3.8, the coordinate of N should be (0, L_{epi}-L_1) with L_1 calculated as

$$L_1 = D_j + W_{depletion} \xrightarrow{V_{applied}=V_{turn}, D_{depletion}=0} D_j, \tag{3.11}$$

where D_j is the p^+ junction depth, and $W_{depletion}$ is the width of the depletion region.

The Electrical Potential at Point N

- ***Assumption 2: Minority carrier injection starts when voltage drop V_{pn} on the p^+n^- junction counteracts the built-in potential V_{bi}.***
- ***Assumption 3 There is no voltage drop on the heavily doped p^+ region.***

Combining Assumption 2 and equation 3.2, we get $\phi_N = \phi_{p^+}$. When neglecting the small voltage drop consumed inside the highly doped p^+ region, the relation

$$\phi_N = \phi_{p^+} = \phi_{ohmic} \tag{3.12}$$

can be obtained. Together with equation 3.7, V_{turn} can be calculated as

$$V_{turn} = V_{applied} = \phi_{ohmic} + \frac{E_{Fp} - E_i}{-q} = \phi_N + \frac{E_{Fp} - E_i}{-q}. \tag{3.13}$$

Since the value of $\frac{E_{Fp} - E_i}{-q}$ is known, the electrical potential ϕ_N becomes critical.

By integrating the electrical field E_y along the y-axis shown in Fig. 3.7, Another expression of ϕ_N is as followed:

$$\phi_N = \phi_{cathode} + \int_0^{L_{epi}-L_1} E_y \cdot dy = \frac{E_i - E_{Fn}}{-q} + \int_0^{L_{epi}-L_1} E_y \cdot dy \tag{3.14}$$

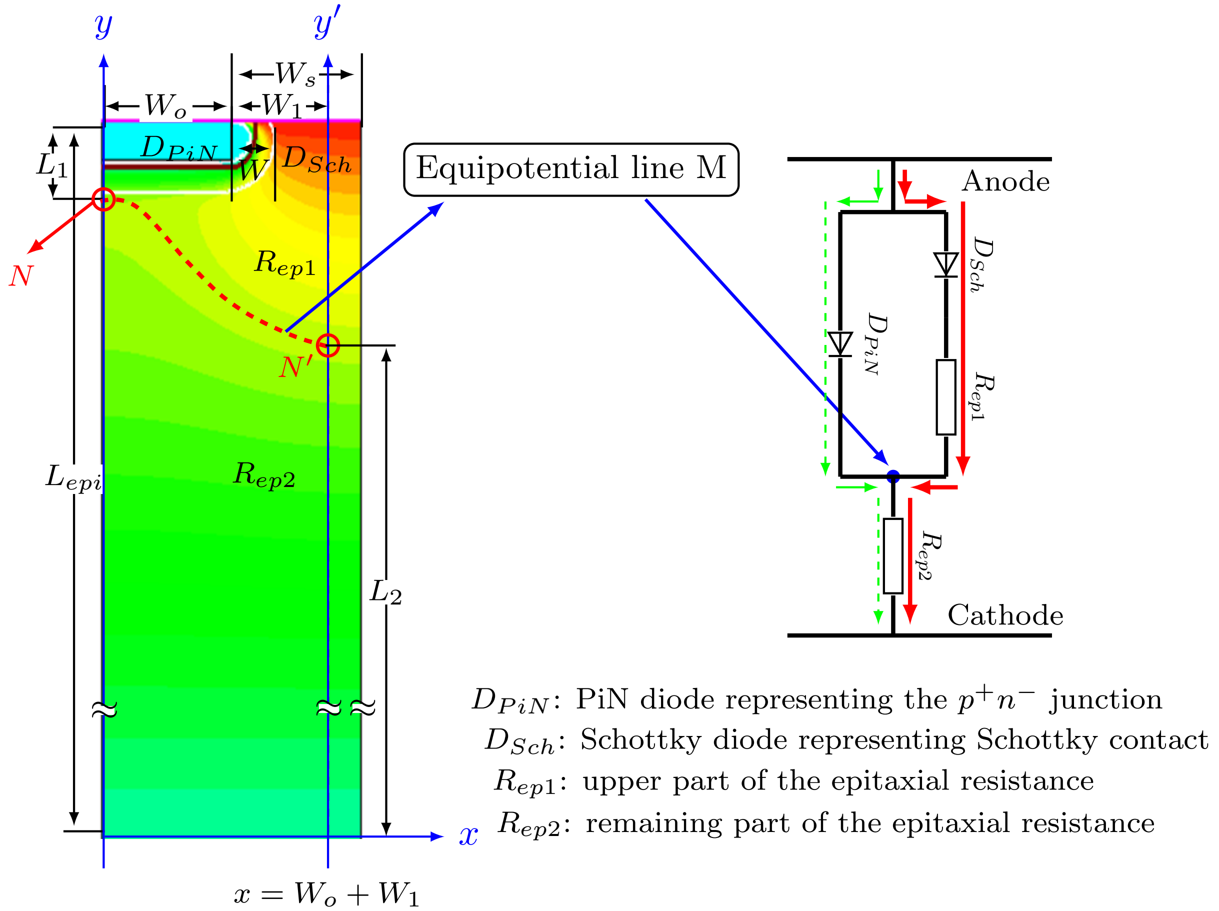


FIGURE 3.7: Electrostatic potential distribution inside the MPS diode structure. The dashed equipotential line separates the epitaxial layer regions with lumped resistance R_{ep1} and R_{ep2}, respectively. The simplified equivalent circuit gives an intuitive interpretation of the functional components of a SiC MPS diode.

where E_{Fn} is the Fermi-energy of the n^+ substrate. Inserting equation 3.14 into equation 3.13, we get an expression

$$V_{turn} = \frac{E_{Fn} - E_{Fp}}{q} + \int_0^{L_{epi}-L_1} E_y \cdot dy = V_{bi} + \int_0^{L_{epi}-L_1} E_y \cdot dy \tag{3.15}$$

without the electrical potential quantity, such as E_F or E_i, inside the semiconductor, but containing the quantities of voltage drop $V_{pn} = V_{bi}$ and $\int_0^{L_{epi}-L_1} E_y{\cdot}dy$. Equation 3.15 gives us a new inspiration: to calculate V_{turn} in an equivalent circuit.

3.3.2 The Simplified Equivalent Circuit

Quantity $\int_0^{L_{epi}-L_1} E_y \cdot dy$ can not be directly calculated, as E_y has a strong dependence on y. However, the result of the integration can become straightforward, if we could make a transfer

$$\int_0^{L_{epi}-L1} E_y \cdot dy = \int_0^{L_2} E_{y'} \cdot dy', \tag{3.16}$$

where $E_{y'}$ is the electric field along the line $x = W_o + W_1$ (see Fig. 3.7), along which we assume $E_x = 0$.

- ***Assumption 4: Electric field E_x in the horizontal direction is negligible for area $x \geq W_o + W_1$.***

The electric field $E_{y'}$ can be easily estimated, since there is only unipolar current flowing inside the MPS diode, before the injection of minority carrier.

As a result, we can get additionally a second formula for V_{turn},

$$V_{turn} = V_{Sch} + \int_0^{L_2} E_{y'} \cdot dy' + \int_{L_2}^{L_{epi}} E_{y'} \cdot dy'. \tag{3.17}$$

.

Based on Equation 3.15 and 3.17 which indicates two current paths inside the MPS diode, we build a simplified equivalent circuit shown on the right side of Fig. 3.7.

Starting from the anode, current flows parallel into the Schottky diode (marked as D_{Sch}) and the PiN diode (marked as D_{PiN}). Below the Schottky diode is a resistor marked as R_{ep1}, the voltage drop of which corresponds to the difference of the voltage drop between the Schottky and Ohmic diode. An equipotential line M, where spots N and N' sit on, splits the epitaxial layer into two regions, represented by two lump resistance R_{ep1} and R_{ep2}. R_{ep2} is in series connection with the parallel circuit mentioned above.

This simplified equivalent circuit provides a direct and intuitive view of the current path inside the devices. When the applied voltage is larger than the threshold voltage V_{th} of the Schottky contact ($V_{th} \leq V_{applied} \leq V_{turn}$), current only flows through the Schottky contact, along the path marked by the red arrow. The dashed green current path becomes active when forward applied voltage reaches the value of V_{turn}. With a large amount of holes injected from p^+ region, electrons are encouraged to inject from the high doped substrate; thus, the resistance R_{ep2} is greatly reduced. This sudden reduction of R_{ep2} can even bring a snap-back behavior in the forward characteristics of MPS diodes.

Based on this equivalent circuit, V_{turn} can be considered as:

$$\begin{aligned} V_{turn} &= V_{Sch} + V_{R_{ep1}} + V_{R_{ep2}} = V_{pn} + V_{R_{ep2}} \\ &= \frac{R_{ep1} + R_{ep2}}{R_{ep1}} \cdot (V_{pn} - V_{Sch}) + V_{Sch} \\ &= \frac{R_{ep2}}{R_{ep1}} \cdot (V_{pn} - V_{Sch}) + V_{pn}, \end{aligned} \tag{3.18}$$

where $V_{R_{ep2}}$, $V_{R_{ep1}}$ and V_{Sch} are the voltage drop on resistor R_{ep2}, R_{ep1} and Schottky contact. Equation 3.18 indicates several important points.

- Voltage V_{turn} will be always larger than V_{pn}, since a negative value of (V_{pn}-V_{Sch}) is not applicable.
- The requirement of a high blocking voltage of the power diode results in a high V_{turn} because the resulting long drift layer introduces a large resistance R_{ep2}.
- A high Schottky barrier height V_{Sch} leads to a low V_{turn}. This again indicates the trade-off relationship between V_{turn} and $J_{F,nom}$.
- Since V_{Sch} can not be changed due to the requirement of the low threshold voltage in unipolar operation mode, the ratio of $\frac{R_{ep1}}{R_{ep2}}$ becomes decisive for the value of V_{turn}, meaning the position of the equipotential line M is important.

3.3.3 Calcuation of V_{turn}

- ***Assumption 5: Electric field $E_{y'}$ along the line $x = W_o + W_1$ is constant for range $0 < y' \leq L_{epi} - L_1$.***

This assumption is proved to be reasonable by Gauss's law. Combining Assumption 4, the divergence of electrostatic field $\vec{E}$ is

$$\nabla \cdot \vec{E} = \frac{\partial E_x}{\partial x} + \frac{\partial E_y}{\partial y} \approx \frac{\partial E_y}{\partial y} = \frac{\rho}{\epsilon} = \frac{n \cdot q}{\epsilon}, \tag{3.19}$$

where ϵ is $9.76 \times 8.854 \times 10^{-12} \frac{As}{Vm}$, q is the elementary charge $1.6 \times 10^{-19} C$ and n is the charge carrier density. Inserting these constant values into the equation above we get

$$\nabla \cdot \vec{E} = \frac{1.6 \times 10^{-19} n}{8.8 \times 10^{-14}} \cdot \frac{C}{cm^3} \cdot \frac{Vcm}{As} = 1.8 \times 10^{-6} n \cdot \frac{V}{cm^2} = 1.8 \times 10^{-14} n \cdot \frac{V}{\mu m^2}. \tag{3.20}$$

The calculations above indicate electric field E_y can be considered as constant if the space charge density nearby is less than $10^{12} cm^{-3}$. In the unipolar conduction mode, this condition apparently can be fulfilled in the rage $0 < y \leq L_{epi} - L_1$ along the line $x = W_o + W_1$.

The Ratio of $\frac{V_{R_{ep1}}}{V_{R_{ep2}}}$

The assumption of the constant electric field, labelled as $E_{y'2}$ in the range $0 < y \leq L_{epi} - L_1$ makes the calculation of the voltage drop $V_{R_{ep2}}$ straightforward:

$$V_{R_{ep2}} = \int_0^{L_2} E_{y',2} \cdot dy = E_{y',2} \cdot L_2. \tag{3.21}$$

However, in the range of $y > L_{epi} - L_1$ along line $x = W_o + W_1$, the increment of the electric field referred to as $E_{y',1}$ caused by the accumulation of electron between p^+ islands due to the reduction of conducting area cannot be ignored. The resulting high electric field $E_{y',1}$ was calculated in a approximation:

$$E_{y',1} = \frac{W_s + W_o}{W_s - W} \cdot E_{y',2}, \tag{3.22}$$

where W is the depletion region extended in the horizontal direction shown in Fig. 3.7, considering the current flowing area decreases from W_o+W_s to $W_s - W$. As a result, the voltage drop $V_{R_{ep2}}$ is calculated with

$$\begin{aligned} V_{R_{ep1}} &= \int_{L_2}^{L_{epi}-L_1} E_{y',2} \cdot dy + \int_{L_{epi}-L_1}^{L_{epi}} E_{y',1} \cdot dy \\ &= E_{y',2} \cdot (L_{epi} - L_1 - L_2) + \frac{W_s + W_o}{W_s - W} \cdot E_{y',2} \cdot L_1. \end{aligned} \tag{3.23}$$

Summing up, the ratio of $\frac{V_{R_{ep1}}}{V_{R_{ep2}}}$ is

$$\frac{V_{R_{ep1}}}{V_{R_{ep2}}} = \frac{L_{epi} - L_2 - L_1 + L_1 \times \frac{W_s + W_o}{W_s - W}}{L_2}. \tag{3.24}$$

Calculation of L_2

The question now is how L_2 can be calculated.

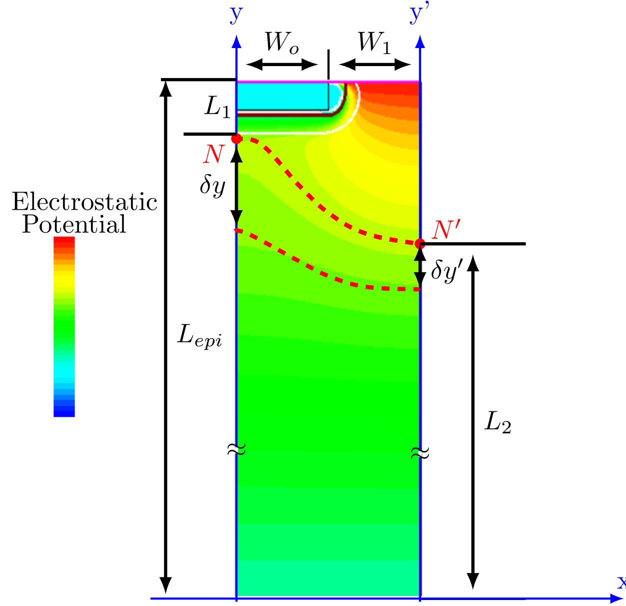


FIGURE 3.8: Equipotential lines inside the MPS diode structure.

As illustrated in Fig. 3.8, we assume that spots located every distance δy downwards from N have the same electrostatic potential as spots located every distance $\delta y'$ downwards from N'. As a result, summing up all δy gives

$$\sum \delta y = L_{epi} - L_1, \tag{3.25}$$

and summing up all $\delta y'$ brings

$$\sum \delta y' = L_2. \tag{3.26}$$

From equation 3.16, we get

$$\sum E_y \cdot \delta y = \sum E'_y \cdot \delta y', \tag{3.27}$$

therefore L_2 can be calculated with

$$L_2 = \sum \frac{E_y}{E'_y} \delta y. \tag{3.28}$$

As the electrostatic potential distribution looks quite similar to the one generated by a point charge located at coordinate $W_o + W_1, L_{epi}$, we consider $\dfrac{E_y}{E'_y}$ as

$$\frac{E(y)}{E(y')} = \frac{(L_{epi} - y)^2}{(L_{epi} - y)^2 + (W_o + W_1)^2}. \tag{3.29}$$

Combining the Equation3.29 and 3.28, we get

$$\begin{aligned} L_2 = \int dy' &= \int_0^{L_{epi}-L_1} \frac{(L_{epi} - y)^2}{(L_{epi} - y)^2 + (W_o + W_1)^2} \dot{d}y \\ &= (W_o + W_1) arctan(\frac{L_{epi} - y}{W_o + W_1}) + y \Big|_0^{L_{epi}-L_1} \\ &= (W_o + W_1) \left[arctan(\frac{L_1}{W_o + W_1}) - arctan(\frac{L_{epi}}{W_o + W_1}) \right] + (L_{epi} - L_1). \end{aligned} \tag{3.30}$$

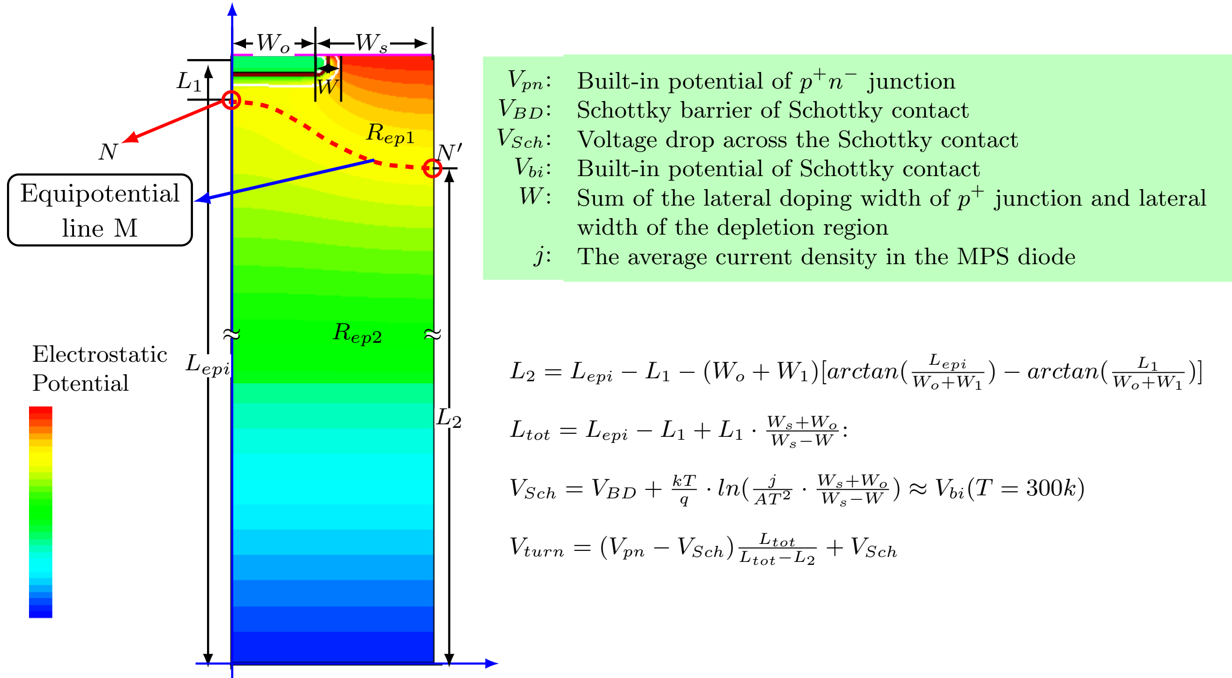


FIGURE 3.9: A summary of all the equations above to calculate V_{turn}

In the MPS diode with ultra-high blocking voltage, such as our targeted device, 4.5kV SiC MPS diodes, $L_{epi} \gg W_o, L_1$ and W_1 Equation 3.30 can be approximated as

$$L_2 \approx L_{epi} - L_1 - W_o - W_1. \tag{3.31}$$

The Voltage Drop Across the Schottky Contact: V_{Sch}

According to the thermionic emission theory, the voltage drop V_{Sch} on the Schottky contact is determined by the current flowing through, the operating temperature, and the Schottky barrier height:

$$V_{Sch} = \phi_{BD} + \frac{kT}{q} \cdot ln(\frac{j}{AT^2} \cdot \frac{W_s + W_o}{W_s - W}) \tag{3.32}$$

where j is the average current density and A is the effective Richardson constant. As our targeted device has a thick epitaxial layer, the average current density flowing through the Schottky contact is considered to be less than the value of AT^2 ($A = 146A/(cm^2 \cdot K^2)$ [24]). This means the last product of the equation above is negative, i.e. $V_{Sch} < \phi_{BD}$. Additionally, a flat energy band diagram around the Schottky contact is observed in the simulation result, i.e., the potential barrier hindering electrons moving from n^- doped region to the Schottky contact almost disappears when the bipolar operation is triggered. Therefore we can make a reasonable approximation

$$V_{Sch} \approx V_{bi_{Sc}} = \phi_{BD} - \frac{E_c - E_{Fn}}{q}, \tag{3.33}$$

where $V_{bi_{Sc}}$ is the built-in potential of the Schottky contact. For the devices investigated in our work, $V_{bi_{Sc}}$ is around 0.8V when the Schottky barrier height $\phi_{BD} = 1eV$.

Combining the equation 3.18, 3.24 and 3.33, a final representation of V_{turn} is obtained and shown in Fig. 3.9.

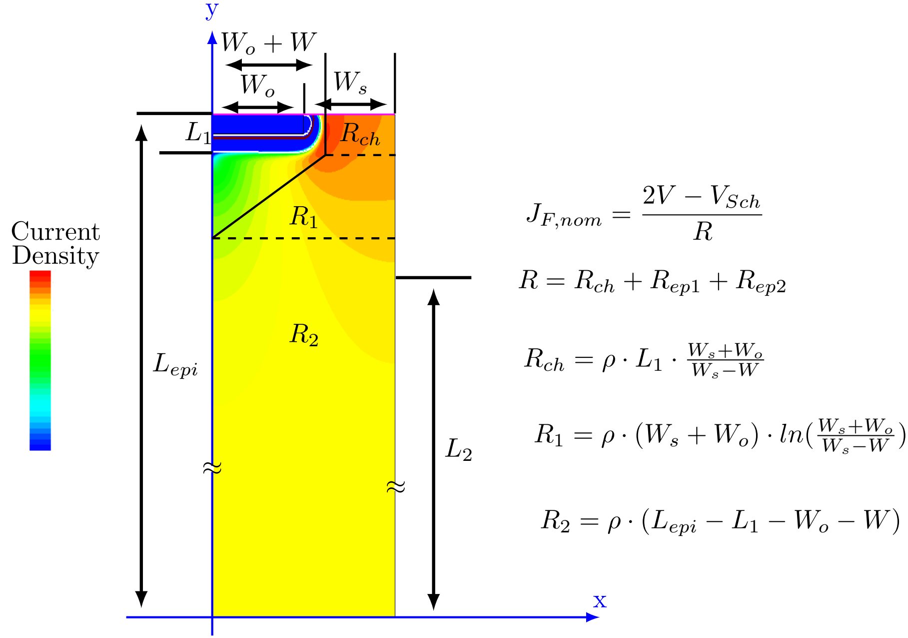


FIGURE 3.10: According to the distribution of the conduction current density, the total resistance of 4.5kV SiC MPS diode is roughly divided into three parts : R_{ch}, R_1 and R_2. Furthermore, the complete analytical model is listed on the right side.

3.4 The Nominal Operation Current Density $J_{F,nom}$

According to our targeted device structure, we adapted the analytical model of $J_{F,nom}$ reported in [25]. As it is defined, $J_{F,nom}$ is the conduction current density when the applied voltage is 2V,

$$J_{F,nom} = \frac{2V - V_{Sch}}{R}, \tag{3.34}$$

where V_{Sch} is approximated to be 0.7V obtained by inserting all the simulated values of $J_{F,nom}$ into equation 3.32. R is the total resistance consisting of three parts:

$$R = R_{ch} + R_1 + R_2, \tag{3.35}$$

The corresponding regions and equations of R_{ch}, R_1 and R_2 are shown in Fig. 3.10.

3.5 Validation of the Analytical Model

The analytical model was validated with reference to the 2D physical simulation results in TCAD. We obtained an amazingly good agreement between simulated and analytical results when varying parameters of Schottky barrier height, Ohmic contact area W_o, and Schottky contact area W_s. One should note that the default parameters for the following comparison is: W_o: 7 μm, W_s: 7 μm, Schottky barrier: 1eV, L_{p^+}: 1.1μm, $N_D(n^-)$: 1.2e15cm^{-3}, L_{epi}: 40μm, τ: 140ns.

3.5.1 Schottky Barrier Height

As the the comparison shown in Fig. 3.11, we observe only a very small discrepancy between the simulated results and the calculated ones of the compact model. This is because the assumptions made in the analytical model are not related to the Schottky barrier height. The linear relationship between V_{turn} and Schottky barrier height confirms well with the equation 3.18. A higher Schottky barrier

height leads to a lower voltage V_{turn} but sacrifices the nominal operation current $J_{F,nom}$. This again indicates that the trade-off relationship between $J_{F,nom}$ and V_{turn} originates from the competition between the Schottky functional part and the PiN functional part.

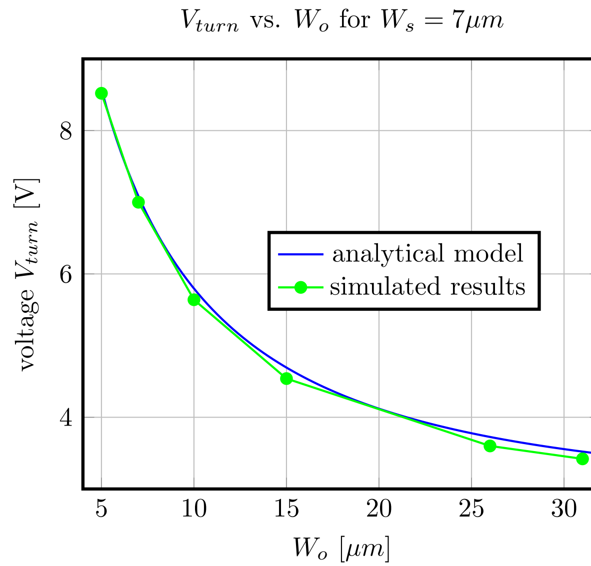


FIGURE 3.12: Comparison of V_{turn} obtained from TCAD simulations and the analytical model for $W_s = 7\mu m$.

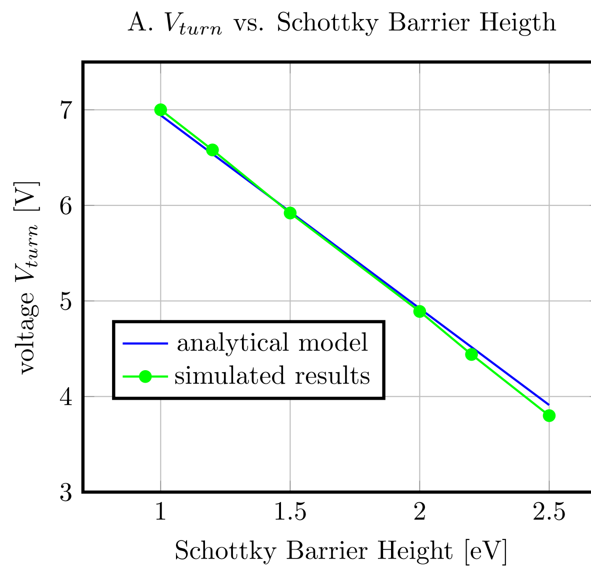


FIGURE 3.11: The calculated values of V_{turn} using the analytical model is compared with the ones obtained from the physical simulations, when varying the Schottky barrier heights.

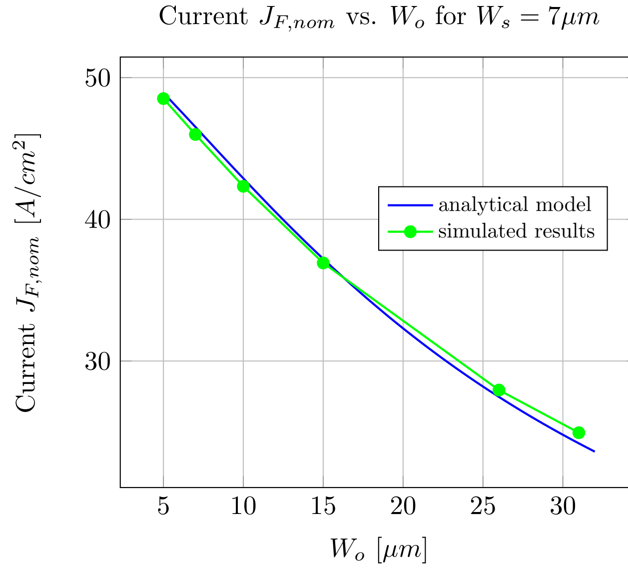


FIGURE 3.13: Comparison of $J_{F,nom}$ obtained from TCAD simulations and the analytical model for $W_s = 7\mu m$.

3.5.2 Variation of W_o

By fixing W_s to $2\mu m$, $4\mu m$, $7\mu m$ and $20.5\mu m$, and varying W_o for each W_s variant, we obtain four groups of data listed in Table 3.1 for the validation of the analytical model. For a fixed W_s, when varying the value of W_o, the calculated V_{turn} and $J_{F,nom}$ via analytical model have an excellent agreement with the simulated results. The data in the group $W_s = 7\mu m$ are plotted in Fig. 3.12 and Fig. 3.13 to show the high accuracy of the analytical model.

3.5.3 Variation of W_s

However, when taking the value of W_s as the variate, the comparison between the analytical model and the simulated results shows a discrepancy if the same V_{pn} is used. This originates from the ***Assumption* 2** made for the analytical models. The value of V_{turn} is identified in the simulated I-V curve as the point having a clear change on the slop of dI/dV. Consequently, with a larger W_s, a higher injection level is necessary in order to have an evident slop change in the I-V curve. This means V_{pn}, instead of equals to V_{bi} of the p^+n^- junction, should be higher than V_{bi}. The other way around, smaller W_s needs a lower V_{pn} to trigger this bipolar operation mode.

In addition, the diffusion motion of holes injected from the p^+ junction is limited within a certain area because its diffusion direction is opposed to the one of the drift motion for the area underneath the Schottky contact. Consequently, a higher minority injection rate, and thus a higher V_{turn}, is needed to reach an obvious resistance modulation of the whole diode, i.e., to observe a turning point in the I-V curve.

Fig. 3.14 illustrates four curves with different values of V_{pn}, aiming to explain why larger values of V_{pn} should be used in the analytical model for larger Schottky area W_s.

3.6 A Plot of the Trade-off Between V_{turn} and $J_{F,nom}$

In order to quantize the trade-off relation between V_{turn} and $J_{F;nom}$, we introduce a new plot by taking the $J_{F;nom}$ and V_{turn} extracted from forward I-V characteristic curves as its x-axis and y-axis. Fig. 3.15 takes the group data with $W_s = 7\mu m$ from Table 3.1 as an example to show this typical

TABLE 3.1: The calculated data of V_{turn} and $J_{F,nom}$ for various W_s and W_o in comparison with the simulated data, with the fitting parameters $W_1 = 2\mu m$, $W = 1.2\mu m$, $L_1 = 1.15\mu m$.

setting		simulated data		analytical data					
W_s	W_o	V_{turn}	$J_{F,nom}$	L_2	L_{tot}	V_{pn}	V_{Sch}	V_{turn}	$J_{F,nom}$
2	2.00	8.36	40.72	34.08	44.6			8.43	42.64
2	4.00	5.87	34.82	31.45	47.47			6.13	36.48
2	6.00	4.84	30.38	29.00	50.35			5.04	31.56
2	7.00	4.78	-	27.85	51.79	2.6		4.69	-
2	8.00	4.13	26.80	26.73	53.22			4.41	27.63
2	12.00	3.63	21.59	22.71	58.97			3.72	21.87
2	16.00	3.43	17.96	19.33	64.72			3.36	17.93
2	20.00	3.28	15.34	16.50	70.47			3.15	15.09
4	4.00	8.43	46.12	31.45	42.13			8.49	46.57
4	7.00	6.20	-	27.85	43.36			6.25	-
4	16.00	4.00	29.78	19.33	47.06			4.10	29.36
4	20.00	3.69	26.26	16.50	48.70	2.75		3.74	25.55
4	24.00	3.50	23.39	14.14	50.35			3.51	22.46
4	28.00	3.34	21.00	12.18	51.99		0.8	3.34	19.93
4	32.00	3.26	19.00	10.54	53.63			3.22	17.84
7	5.00	8.52	48.52	30.20	41.22			8.58	48.91
7	7.00	7.00	45.99	27.84	41.62			7.08	46.52
7	10.00	5.64	42.33	24.64	42.22	2.88		5.79	42.88
7	15.00	4.54	36.92	20.12	43.21			4.69	37.21
7	26.00	3.60	27.95	13.11	45.39			3.72	27.46
7	31.00	3.42	24.94	10.92	46.38			3.52	24.18
20.5	6.00	8.48	50.05	29.00	40.42			8.47	52.08
20.5	7.00	7.76	-	27.85	40.49			7.75	-
20.5	12.50	5.60	47.65	22.26	40.81			5.57	48.10
20.5	19.50	4.31	42.09	16.83	41.23	2.97		4.46	43.18
20.5	24.00	3.92	39.00	14.14	41.50			4.09	40.02
20.5	28.00	3.68	36.47	12.18	41.73			3.86	37.33
20.5	32.00	3.52	34.17	10.54	41.97			3.69	34.80

trade-off curve. The black arrow indicates the optimal direction that this trade-off curve should shift to obtain concurrently a high nominal current density $J_{F,nom}$ and a low voltage V_{turn}. This trade-off

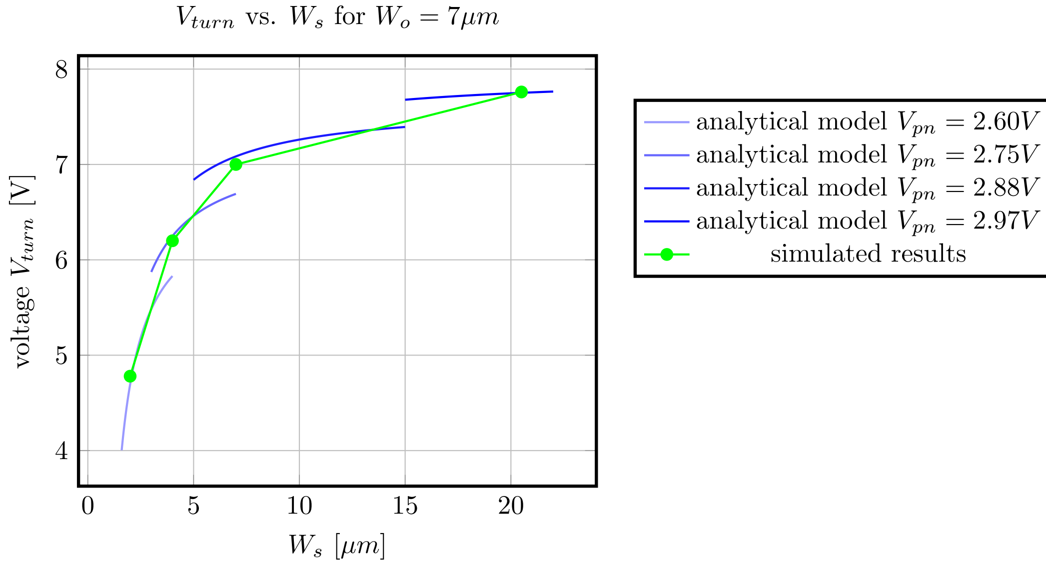


FIGURE 3.14: Comparison of V_{turn} between the one from simulation and the one obtained using analytical model for $W_o = 7\mu m$.

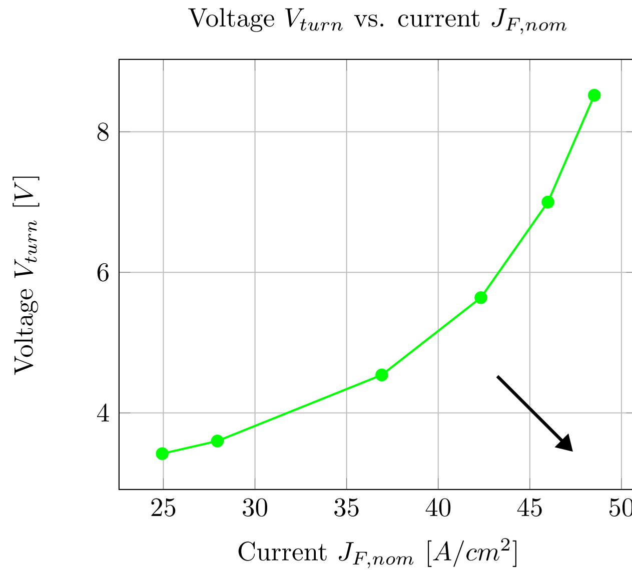


FIGURE 3.15: Voltage V_{turn} increases with the increasing nominal current $J_{F,nom}$.

curve will be presented several times in Chapter 4 to judge which topology can offer a better trade-off relation between V_{turn} and $J_{F,nom}$.

Summing up the information provided by the analytical model discussed in this chapter, there are several ways to get a win-win-situation for V_{turn} and $J_{F,nom}$.

- Reducing the resistance R_{ep2};
- Increasing the ratio $\frac{R_{ep1}}{R_{ep2}}$;
- Reducing the built-in potential of p^+n^- junction.

In the next Chapter, novel device structures aiming to improve this trade-off relation will be discussed.

Chapter 4

Superior Device Structures

Combining the inherent advantages of Schottky diodes and PiN diodes, MPS diodes are able to exhibit, at the same time, a low threshold voltage and a high surge current capability in the forward direction as well as a high breakdown voltage and low leakage current in the reverse direction [8]. The multi-targeted optimization in this chapter consists of achieving high $J_{F,nom}$ and, concurrently, low V_{turn} avoiding premature overheating, and maximum J_{surge}.

In order to support the high blocking voltage, our targeted devices, 4.5 kV SiC MPS diodes, have a relatively long drift layer that introduces a high forward on resistance R_{on}. The high R_{on} and the wide bandgap E_g of SiC lead to a high voltage V_{turn} triggering the bipolar mode. However, a too-high V_{turn} can cause premature overheating and result in thermal runaway as well known from Schottky diodes. Modifications of the device structure can reduce V_{turn}, but also force a lower value of the nominal operating current density $J_{F,nom}$. We found out there is a trade-off between V_{turn} and $J_{F,nom}$ [14].

One of the most flexible modifications of the device structure is to variate the ratio of the Ohmic contact area (W_o) to the Schottky contact area (W_s), and it brings no change to the blocking voltage of devices. Early work on Si JBS diodes [26] and 600V SiC MPS diodes [27] have reported detailed investigation on that and illustrated the dependence ofV_{turn} and $J_{F,nom}$ on the ratio of W_s/W_o. However, these studies focus on the nominal ratio of the contact area only and do not consider alternative contact topography variants, as we attempted in this chapter.

This chapter discusses several new layout variants aiming to provide a lower V_{turn} and a higher $J_{F,nom}$. Based on the conventional striped structure, we introduce a new variant with a various area ratio of W_s/W_o in one unit cell. After that, considering the trade-off relationship between V_{turn} and $J_{F,nom}$ originates from the conflict between the Schottky functional part and the Ohmic functional part, our proposal is to isolate these two parts. One is the electrical decoupling of Schottky contact and Ohmic contact; the other one is geometrical isolation, placing an additional oxide interlayer between the Schottky diode part and the Ohmic diode part. For sure, one can imagine other geometrical isolation, such as the buried p^+ junction design used in the commercial production of *Ascatron* company. Another example of the geometrical isolation is the super-junction structure that is formed by the alternate p^- and n^- pillars in the epitaxial layer. In this structure, there is a larger vertical distance between N (where holes are injected) and the Schottky contact. In the end, we give a brief discussion of 3D structures.

In order to quantify the trade-off relation between V_{turn} and $J_{F,nom}$, we introduce a new plot by taking the $J_{F,nom}$ and V_{turn} extracted from forward I-V characteristic curves as x-axis and y-axis. Fig. 3.15 is the first example of this plot. Four trade-off curves of the conventional strip topologies are shown in Fig. 4.1. Each curve has a fixed Schottky area width and the different values of V_{turn} and $J_{F,nom}$ are obtained by altering the value of W_o. We can observe that increasing the area ratio of W_s/W_o brings a higher value of $J_{F,nom}$ and V_{turn}, regardless of the different size of the fixed Schottky area. This plot gives a direct comparison and overview for identifying which topology can offer

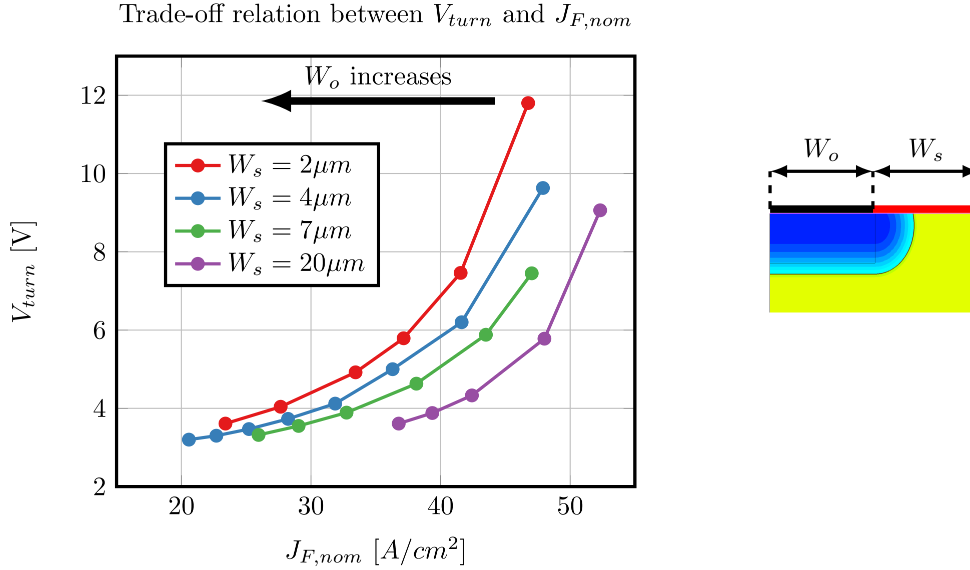


FIGURE 4.1: Curves representing the trade-off relation between V_{turn} and $J_{F,nom}$ are plotted using the data extracted from the I-V curves of conventional strip structure shown at the right side. Larger unit cells show a better trade-off relation.

lower V_{turn} for the same nominal current density $J_{F,nom}$. In the following section, we frequently use this plot as a direct quantitative measure to assess the optimization degree of the resulting trade-off relationship between V_{turn} and $J_{F,nom}$, when varying one design parameter for a given topology or comparing different device designs.

4.1 Various Area Ratio of W_s/W_o in One Unit Cell

As mentioned before, a higher area ratio of W_s/W_o inclines the forward characteristics of MPS diodes to that of Schottky diodes, i.e., large $J_{F,nom}$ and high V_{turn}. However, one should notice that even for the same area ratio W_s/W_o, the trade-off relations for a different total size of $W_s + W_o$ are yet different. This means that the area ratio W_s/W_o alone can not determine the value of V_{turn} and $J_{F,nom}$. Simulation results show that a large unit cell can provide a better trade-off relation. For the same $J_{F,nom}$, Fig. 4.1 shows that the SiC MPS diodes with $W_s = 20\mu m$ have the lowest value of V_{turn}.

This finding is confirmed by another comparison of the simulated results shown in Fig. 4.2. Here, we compare the I-V characteristics of four different contact topographies with the same total contact area and ratio of W_s/W_o. To give a systematic explanation, we introduce these four contact topographies (A to C) sequentially.

Topography A has a constant area ratio and exhibits the highest V_{turn} and a slightly higher value of $J_{F,nom}$. Then by splitting the unit cell into two parts with different area ratios of W_s/W_o at the left half-side and at the right half-side, through which the total value of W_s/W_o keeps the same, we get topology B. Its minority carrier injection sets on at a much lower value and starts at the leftmost p^+-junction of B. After that, the minority carriers diffuse from the leftmost top corner towards the right-down side. Consequently, the resistance of the drift layer is significantly reduced, which further promotes the bipolar injection from the rest of p^+-junctions in the structure and eventually brings the whole device into complete bipolar operation mode.

Being surprised by the improved results in topography B, we tried to build an extreme case of topography B, which is topography C, generated by changing the left half part to a complete large p+-region (W_s/W_o = 0) and the right half part to a complete n^--region (W_s/W_o = 1). The trade-off

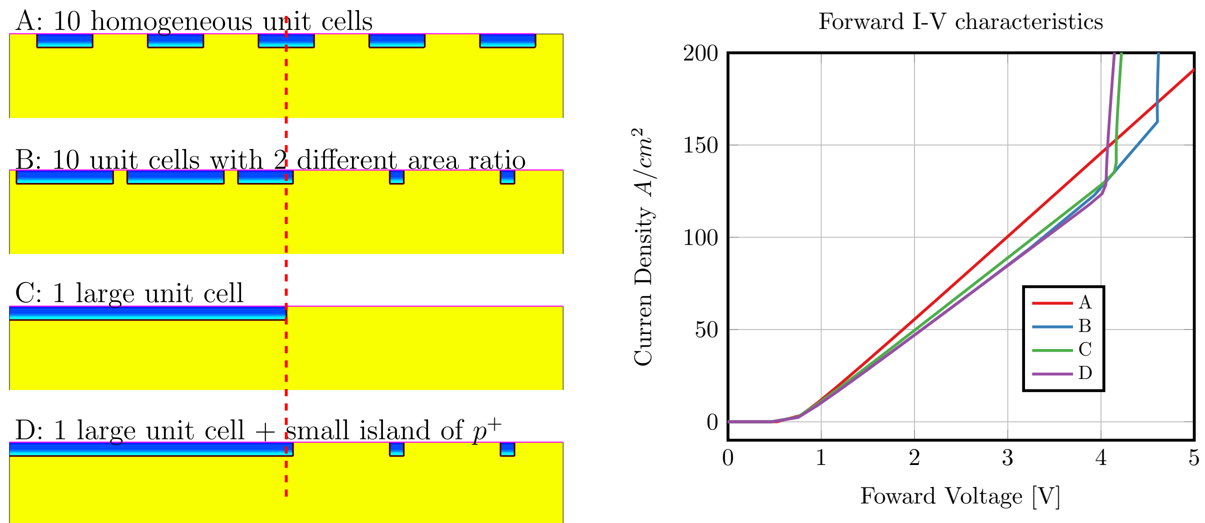


FIGURE 4.2: Device structures with four different contact topographies and their I-V characteristics are compared, indicating structures C and D are superior.

relation on the right side shows that topography C brings almost no change on $J_{F,nom}$ but a further reduced V_{turn}. At this point, we can come to the comparison between A and C. They both have the same area ratio of W_s/W_o, but topology C, having a larger unit cell, offers a much lower V_{turn} and almost the same $J_{F,nom}$. This conclusion is the same as the one shown in Fig. 4.1.

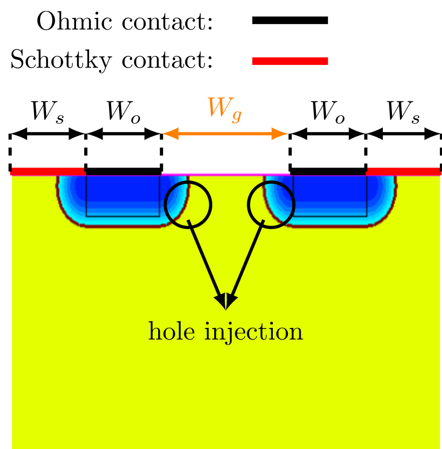
In the end, considering the leakage current in the reverse characteristics, topography C has to be enhanced to topography D, because a high density of p^+-islands is required to provide an electric field shielding in the blocking state to reduce the leakage current caused by Schottky barrier lowering. There are two ways to interpret the topography D. We can consider it as one unit cell consisting of two different area ratios of W_s/W_o, corresponding to the high surge current capability in the conduction mode and the low leakage current in the blocking mode, respectively. Alternatively, one may interpret it as an array of large unit cells containing an embedded array of small unit cells, where the larger unit cells ensure optimum forward characteristics, while the small unit cells keep the leakage current low in blocking direction.

4.2 Electrical Decoupling

Inspired by the fact that the trade-off between V_{turn} and $J_{F,nom}$ originates from the strong interference between Schottky contact and Ohmic contact, we proposed a novel contact topography with contact gaps, as shown in Fig. 4.3. The basic idea is to utilize the electrical decoupling, instead of placing a Schottky contact between two Ohmic contacts, a non-metallic layer is formed on the top of the n^- region between two p^+ islands. Consequently, the electrical potential difference $\Delta\phi$ (in Equation 3.10) between the Ohmic contact and the Schottky contact is not forced to be kept, posing less constraint on the forward bias of the p^+n^- junction. Therefore, the bipolar operation mode can be triggered with a lower voltage of V_{turn}, starting from the location marked in Fig. 4.3.

Fig. 4.3 shows several I-V forward characteristics obtained by enlarging W_g from $1\mu m$ to $6\mu m$, revealing a negative relation between voltage V_{turn} and W_g. However, when enlarging W_g, the total percentage of Schottky contact that allows the unipolar current flowing through is lower, resulting in lower $J_{F,nom}$.

Placing contact gaps essentially serves the same purpose as enlarging the W_o or p^+-regions, leading to a reduction of V_{turn} or decrease of $J_{F,nom}$. Fig. 4.4 exhibits the comparison of three topologies for



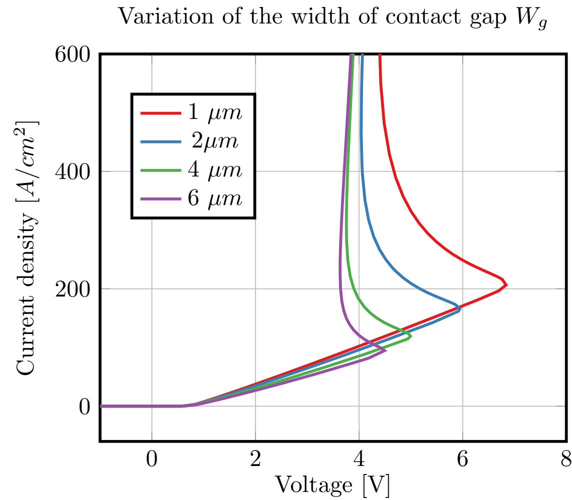
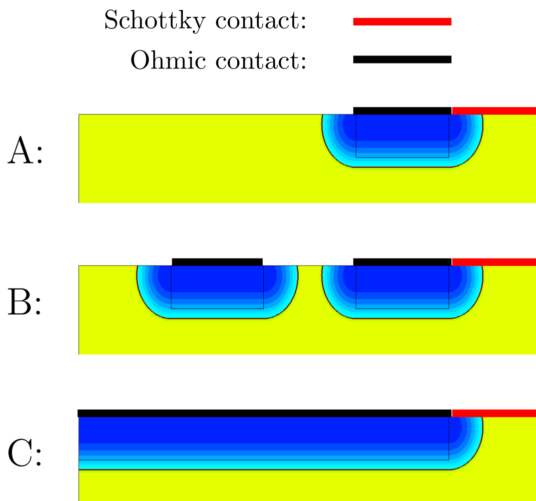


FIGURE 4.3: A small unit cell realizing the new concept of "contact gap" is shown at the left upper corner. The plot illustrates the dependence of forward I-V characteristics on the width of the contact gap W_g.



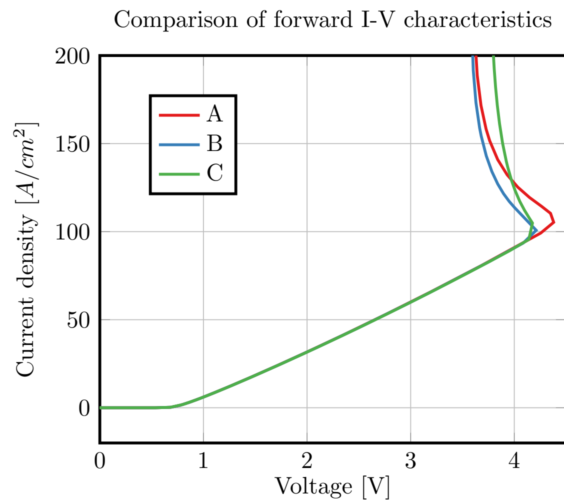


FIGURE 4.4: Comparison of I-V characteristics among three structures having different numbers of p^+ island in on unit cell: A has 1, B has 2, and C has 0.5.

discussing the influence of the placing contact gaps, the density of p^+ islands, and the enlarging p^+-region on $J_{F,nom}$ and V_{turn}. It turns out that topology A with one contact gaps has a slight higher V_{turn} compared to topology C with a long p^+ region. Nevertheless, this disadvantage can be eliminated if we enhance topology A to B by increasing the density of p^+ islands. Moreover, topology B has an even higher surge current density than C after entering bipolar operation mode.

The higher surge current density in topology C can be explained by the enhanced emitter efficiency due to the increment of the cross-sectional area of the minority carrier injection. As shown in Fig. 4.5, the high density of p^+ islands with contact gaps above them in the novel structure turn the cross-sectional area of hole injection into a wavy shape, instead of a flat and single arc shape as in the conventional structure, and consequently a larger cross-sectional area for injection is gained. Another difference is the location (N) of the initial minority carrier injection. Instead of at the middle-bottom of a p^+-region, N is shifted upwards and close to the contact gap, which gains additionally resistance R_2 due to the extra vertical distance between the initial injection point N and Schottky contact, and this can lead to even less V_{turn}.

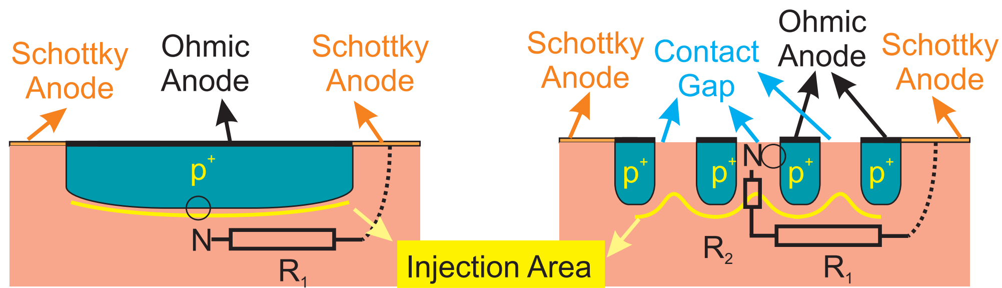
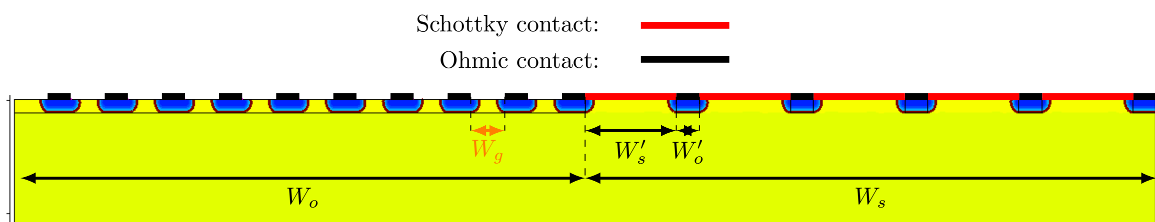


FIGURE 4.5: Different effective injection areas are shown between the topology with one large unit cell and the topology with the electrical decoupling.



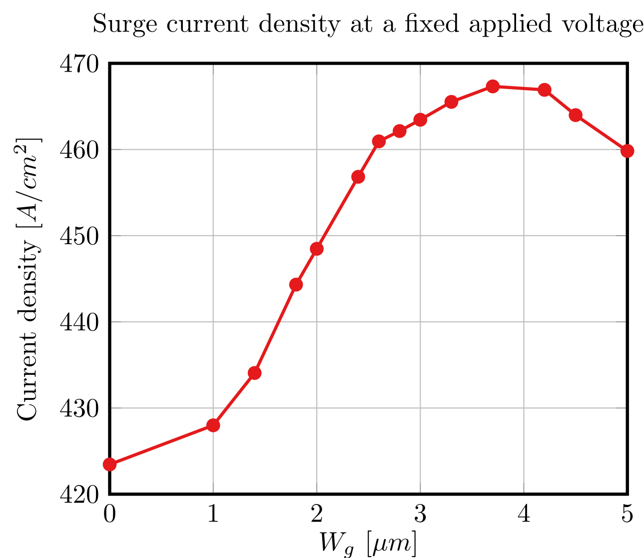


FIGURE 4.6: We combined the ideal in Fig. 4.2, and proposed a novel structure using electrical decoupling. The plot underneath illustrates the relationship between the increment of surge current density and the contact gap width.

Combining the idea proposed in Fig. 4.2 and the idea of placing contact gaps, we propose the final topography shown in Fig. 4.6 . In order to study the dependence of the increase of the surge current density on the width of the contact gap W_g, a series of simulations have been implemented by taking $W_s = 50\mu m$, $W_o = 50\mu m$, $W_o' = 2\mu m$, $W_s' = 8\mu m$ and W_g as variant. The simulated results are plotted in Fig. 4.6. With the growing W_g, the surge current density first rises, reaching a peak value when $W_g = 3.75\mu m$, and then degrades. The optimum value of W_g can be estimated as the sum of one W_o' and a double of the horizontal diffusion extension of p^+-regions because this combination brings the maximum ruggedness of the effective injection area.

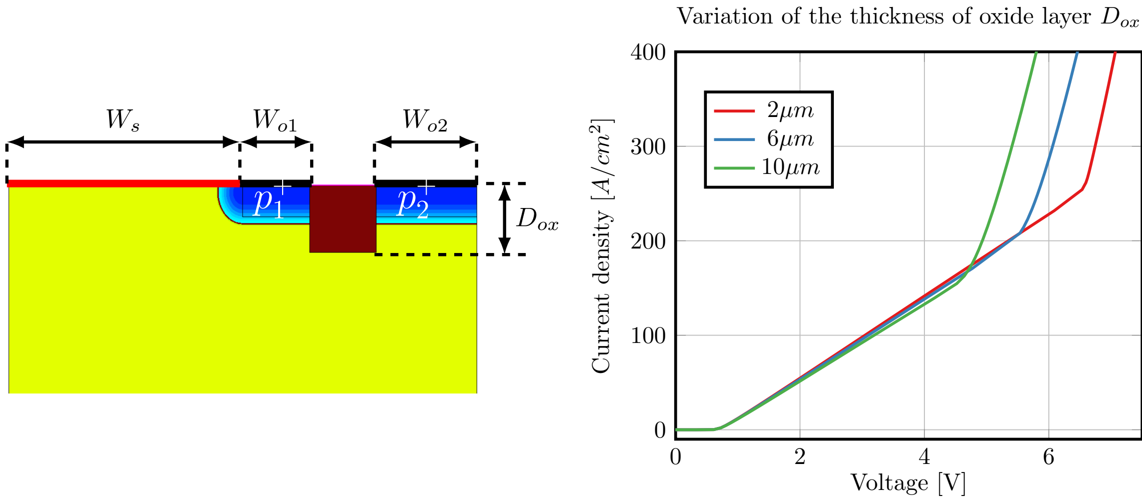


FIGURE 4.7: A sketch of the MPS diode with an oxide interlayer is presented at the left side. The I-V forward characteristics are plotted for three different depths of the oxide layer.

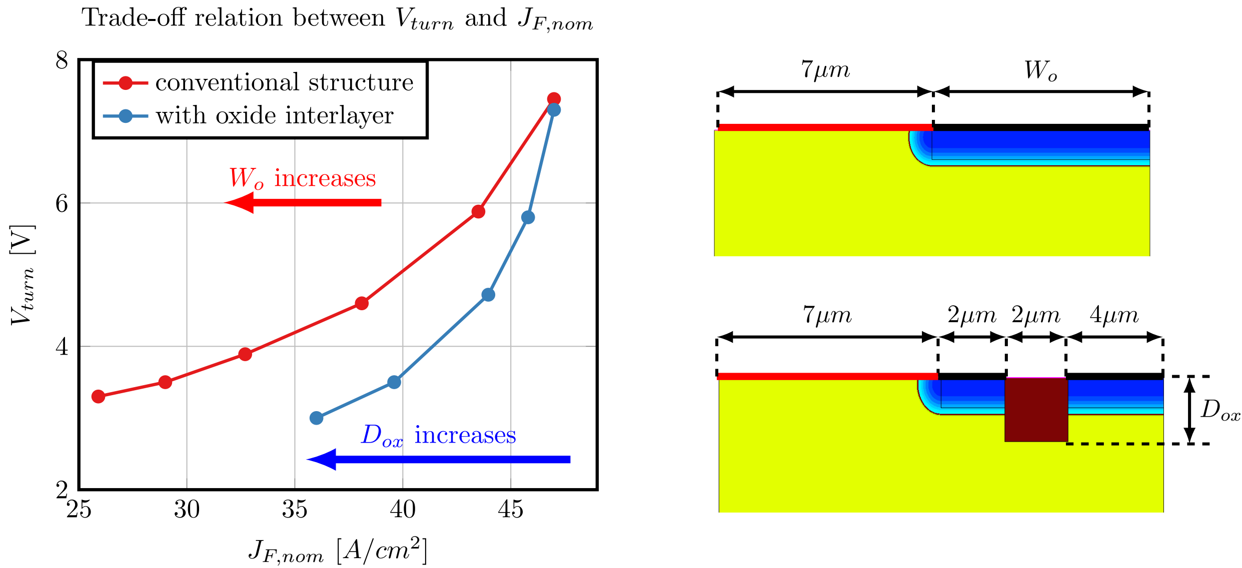


FIGURE 4.8: The trade-off relations between V_{turn} and $J_{F,nom}$ for the conventional structure with varying W_o are plotted in comparison with the ones for the novel structure with an altering depth D_{ox} oxide interlayer.

4.3 Oxide Interlayer

With the same intention as in the previously proposed structure, minimizing the interaction between the Schottky diode functional part and PiN diode functional part, we place an oxide interlayer dividing the p^+ region into tow parts p_1^+ and p_2^+, so that p_2^+ is "isolated" from Schottky contact in order to improve the surge current capability. The p_1^+ takes the responsibility of reducing leakage current in the blocking state. As shown in Fig. 4.7, a geometrical decoupling in both vertical and horizontal direction is gained in this proposed structure, instead of an electrical decoupling in the horizontal direction as in the previous structure. As a result, the bipolar operation is triggered at a lower value of V_{turn}. Forward I-V characteristics of three different device structures by varying the depth of oxide layer D_{ox} are plotted. It turns out that the depths of the oxide interlayer influences the amount of V_{turn}, i.e. the deeper the oxide interlayer is , the lower is V_{turn}. Additionally, the reduction of $J_{F,nom}$

due to the additional oxide interlayer is negligible because there is no direct change made in the Schottky contact area and the unipolar current path.

However, supposing D_{ox} keeps increasing up to a certain value, one can see an evident impact on $J_{F,nom}$, due to the reduction of the effective cross-sectional area underneath the p^+ region that the unipolar current flows through. In order to quantize the improvement in surge current capability brought by the proposed structure with oxide interlay and its impact on nominal current density, we plot the trade-off curves between V_{turn} and $J_{F,nom}$ with the increasing depths of the oxide interlayer Fig. 4.8. For comparison purposes, the trade-off curve of the conventional structure with increasing W_o is plotted as well. These two curves have the same starting point at the top-right corner. This starting point corresponds to $W_o = 7\mu m$ in the conventional structure and $D_{ox} = 0\mu m$ in the novel design. By enlarging W_o and increasing D_{ox} in these two structures, respectively, two trade-off curves extend towards to left-down corner. The structure with an oxide interlayer shows a better trade-off relation because it can provide much lower V_{turn} when the values $J_{F,nom}$ are the same.

4.4 Super-junction

Based on the simplified equivalent circuit in Fig. 3.7, it is clear that minimizing R_{ep2} can lead to a lower V_{turn} and concurrently a higher $J_{F,nom}$. However, how can R_{ep2} be reduced while maintaining the same blocking voltage? One obvious answer is the super-junction structure. Fig. 4.9 displays its elementary unit cell which was developed based on the conventional structure with a replacement of the n^- doping by p^- doping in the left half-side in the epitaxial layer.

The electric field strength E_y along a vertical cut line C_1 is plotted at the right side of Fig. 4.9. The super-junction structure has a quasi-homogeneous distribution of E_y, in contrast to the conventional structure having a much higher peak value of E_y close to the anode contact, and this peak value limits the doping concentration in the epitaxial layer. The secrete of constant E_y along the cut line C_1 is having the same doping concentration for p^- and n^- regions. When the devices are reverse

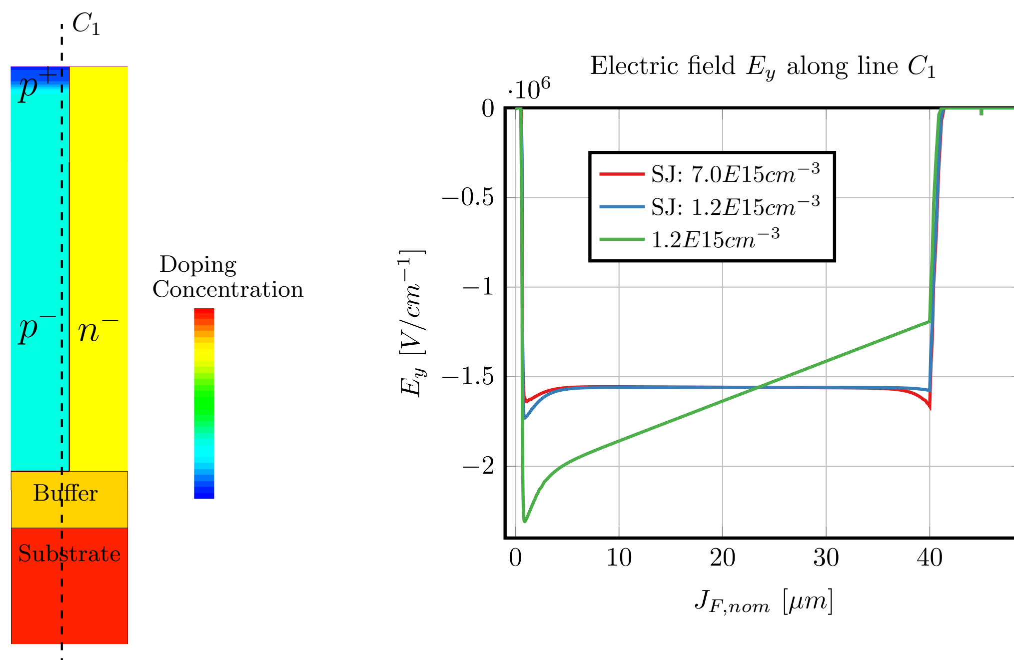


FIGURE 4.9: Left: An overview of the super-junction structure; Right: A comparison of the distribution of electric field along a cut line C_1 in the super-junction structures with different doping concentrations and in a conventional structure of MPS diodes.

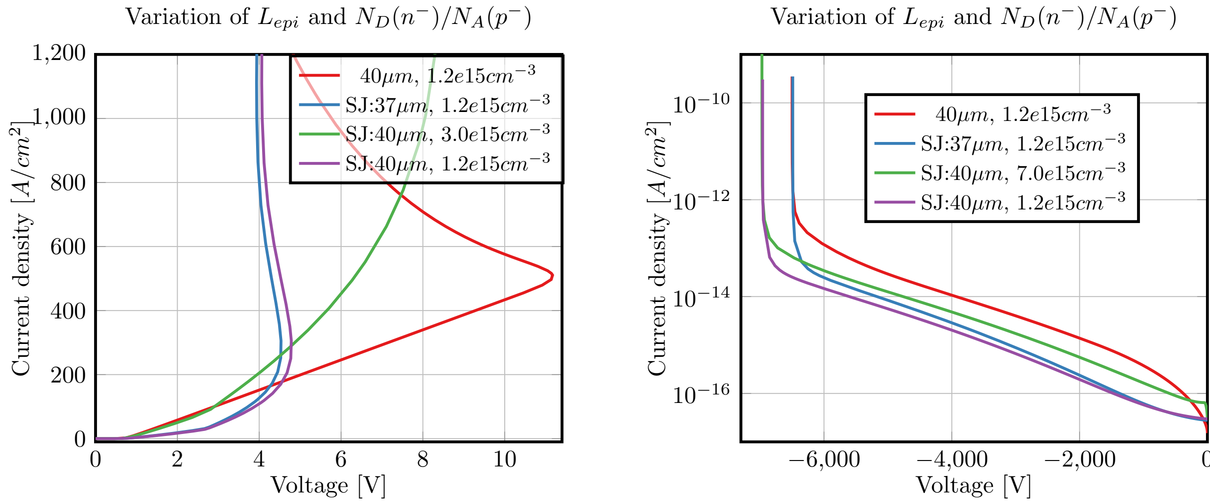


FIGURE 4.10: Forward and reverse characteristics of super-junction structures with variations of L_{epi} and $N_D(n^-)/N_A(p^-)$.

bias, the same size of depletion region (the same amount of N_A^- and N_D^+) are formed in the p^- and n^- regions. Consequently, the directions of electric field lines in the epitaxial layer are all horizontal, i.e. there are no gains in the electric field portion in the vertical direction, meaning E_y keeps constant through the whole epitaxial layer.

Another conclusion one can draw from the plots in Fig. 4.9 is that different levels of doping concentration (the red and the blue curves) in the super-junction lead to the same E_y distribution. This characteristic allows a higher level of doping concentration in the epitaxial layer, and thus reducing the on-resistance, when keeping the same blocking voltage.

Fig. 4.10 displays the comparison of the forward and reverse characteristics of super-junction structures with two different designs and the conventional structure. At the right-hand side is the plot of reverse characteristics, showing that keeping the same $L_{epi} = 40\mu m$ but a higher doping concentration of $7.0e15cm^{-3}$ in the epitaxial layer can result in an even higher blocking voltage in the super-junction structure. Furthermore, the same blocking voltage as the conventional structure can be achieved with a shorter L_{epi} of $37\mu m$, instead of $40\mu m$.

In case of the forward characteristics, a comparison between the conventional structure (red line) and super-junction structure (purple line) with the same L_{epi} and $N_D(n^-)$ indicates that the reduction of half area in the n^- region leads to a very high forward on-resistance in the nominal operation mode. In order to compensate for this, a higher doping concentration $N_D(n^-)$ and a shorter L_{epi} must be taken in the super-junction structure. However, due to the limited reduction of L_{epi}, the device (blue line) having $37\mu m$ junction depth shows a similar forward characteristic with the one having $40\mu m$. The green line representing the super-junction structure with the more than twice higher doping concentration ($3.0e15cm^{-3}$) shows the most advanced forward characteristics. However, its surge current density still needs to be improved.

Why does a higher doping concentration in the n^- and p^- region lead to a lower surge current density? This is related to the important material property of SiC, incomplete ionization. Fig. 4.11 shows the distributions of actual ionized doping concentration (above) and the increasing hole injection level (below) inside the super-junction structure with increasing applied voltage. With the increasing injection rate of hole carriers into the n^- region, the hole carrier density starts to accumulate at the bottom of p^- region, leading to a high incomplete ionization rate of the acceptor N_A, and consequently a reduced p^- junction depth. The upwards shifting of the p^- region introduces a wider spreading range of electron-hole plasma, bringing a large resistance modulation in the epitaxial layer,

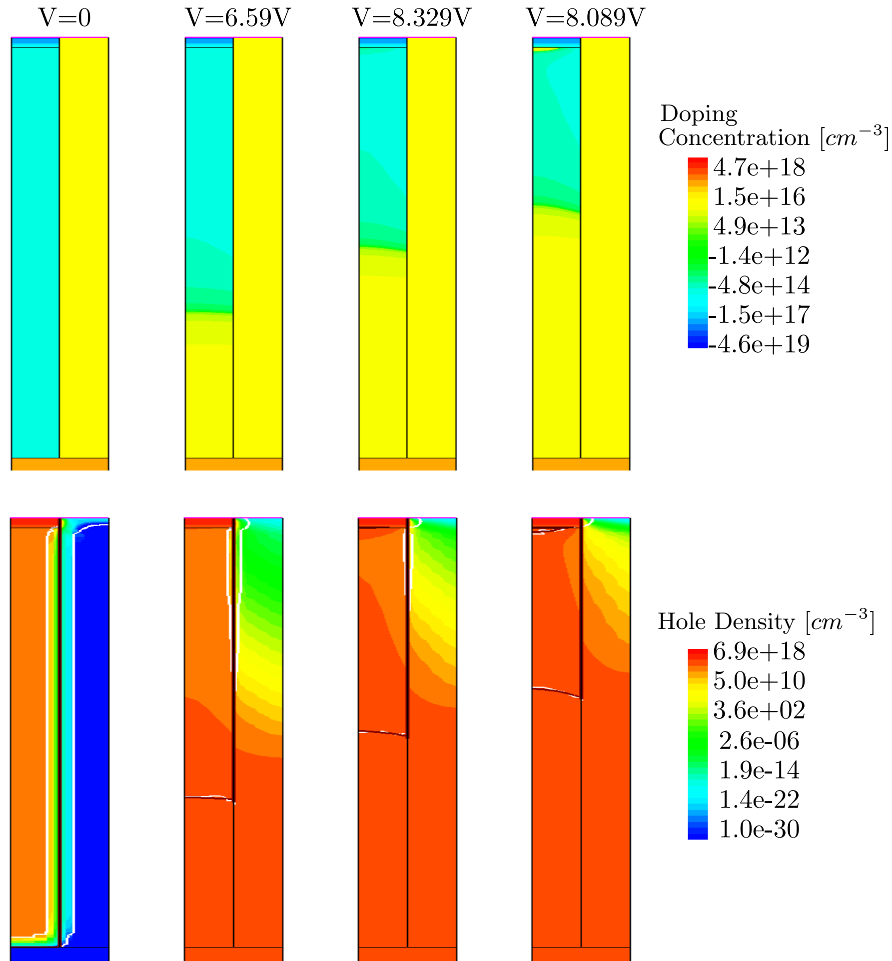


FIGURE 4.11: Modification of the junction depth of the low doped p^- region due to the high incomplete ionization rate at high injection levels ($N_D(n^-) = 1.2e15cm^{-3}$).

i.e. a high surge current density. However, in the case of high doping concentration ($3.0e15cm^{-3}$), the incomplete ionization rate cannot reach a level that alters the p^- junction depth. Accordingly, the injected hole can not spread upwards, and the mobile charge carrier density underneath the Schottky contact remains low. Therefore, very limited surge current density can be achieved.

4.5 3D Structures

So far, we considered stripe-shape MPS structures only, which are properly modeled using 2D cross-sections and Cartesian coordinates (Fig. 4.12.a). With the same cross-section, but using cylindrical coordinates, we extended our trade-off study to a 3D elementary cell of cylindrical structure (Fig. 4.12.b). In order to compare the stripe-shaped structures with the cylindrical structures, different trade-off relations with a fixed value of W_s for each curve are plotted in Fig. 4.13. It indicates that the cylindrical structures outperform the stripe-shaped arrays.

Simplified explanations are offered as follows. As introduced before, both V_{turn} and $J_{F,nom}$ have a close relationship with the area ratio W_s/W_o in the strip-shaped structure. However, this should be re-clarified in the cylindrical structure, where the $J_{F,nom}$ has a close relationship with the effective contact area ratio $A_s/(A_s + A_o)$, instead of the one dimensional ratio W_s/W_o. In case of the same W_s/W_o (the same cross-section) in cylindrical structures as in strip structures , the effective area ratio $A_s/(A_s + A_o)$ is larger in cylindrical structures, since the Schottky contact is the outer ring of the

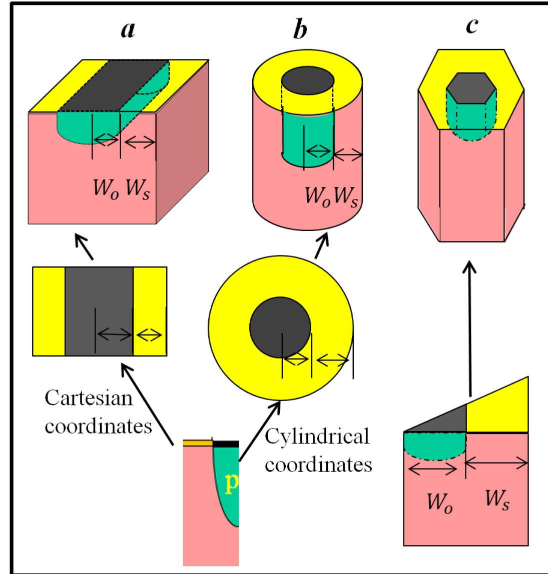


FIGURE 4.12: Three different 3D structures of the MPS diode and their respective simulation domains.

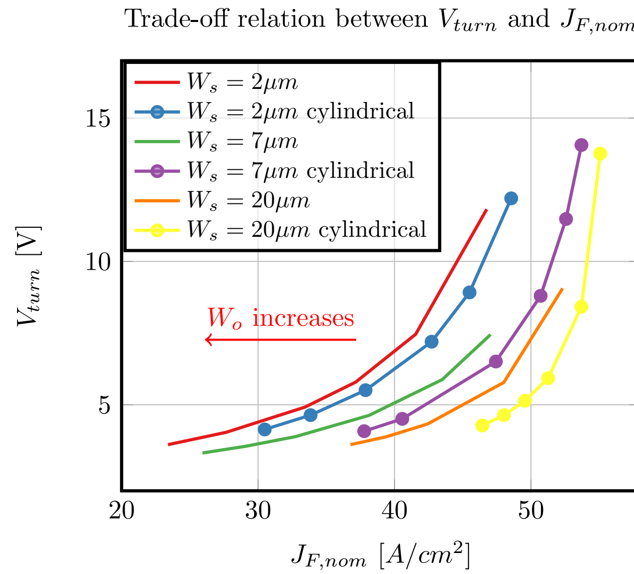


FIGURE 4.13: Cylindrical structures feature a better trade-off between V_{turn} and $J_{F,nom}$ than the conventional stripe-shaped structures.

unit cell. If W_s/W_o is defined as r, an ideal estimation of the effective area ratio of $A_s/(A_s + A_o)$ for cylindrical structure is

$$\frac{2r + r^2}{(1 + r)^2}. \tag{4.1}$$

This is larger than the one in the stripe-shaped structure,

$$\frac{r}{r + 1} = \frac{r^2 + r}{(r + 1)^2}. \tag{4.2}$$

Therefore cylindrical structures are able to provide a higher $J_{F,nom}$ with a comparable V_{turn}.

However, in the practical realization, hexagonal cells (Fig. 4.12.c) should be preferred because they

feature the highest package density of unit cells in a 2D plane and at the same time own the similarity of cylindrical structures. For example, commercial 600V SiC MPS diodes manufactured by Infineon Technologies, are in hexagonal cell array topography [8].

Chapter 5

Nonideal Ohmic Contact

This chapter introduces one of the main issues for SiC semiconductor devices: the non-ideal Ohmic contact on the top of the p-type doping region. We first explain why fabricating an ideal Ohmic contact on the top of the p^+ doping region is a challenge. Then, based on the comparison between measured data of the Schottky diodes and their simulated results, we extracted the potential barrier height between the metallization layer and the semiconductor, and the work-function $q\Phi_m$ of the metallization layer. With the extracted value of $q\Phi_m$, we were able to calibrate the Ohmic contact model of the PiN diodes fabricated with the same metallization process on the same wafer as the Schottky diodes. In the end, both the calibrated and adapted Schottky contact model and Ohmic contact model are applied in the simulation of SiC MPS diodes to analyze the influence of non-ideal Ohmic contact on IV characteristics.

The key concept of MPS diodes implies the parallel integration of two different contact metallizations: the Schottky contacts on top of the n^- epitaxial layer and the Ohmic contacts above the p^+ implantation region. Due to the fabrication technology employed, these two different contacts are formed at the same time by the same metallization process, which inherently results in either an undesired high Schottky barrier in the Schottky contact or a poorly conductive Ohmic contact.

5.1 Ohmic Contact in P-type SiC

An Ohmic contact for a p-type semiconductor can be built in two ways. One consists in depositing a metal with a work-function Φ_m larger than the work-function Φ_p of the p-type semiconductor, while the other one is forming an Ohmic tunnel contact by introducing a highly doped region at the interface between metal and semiconductor [28].

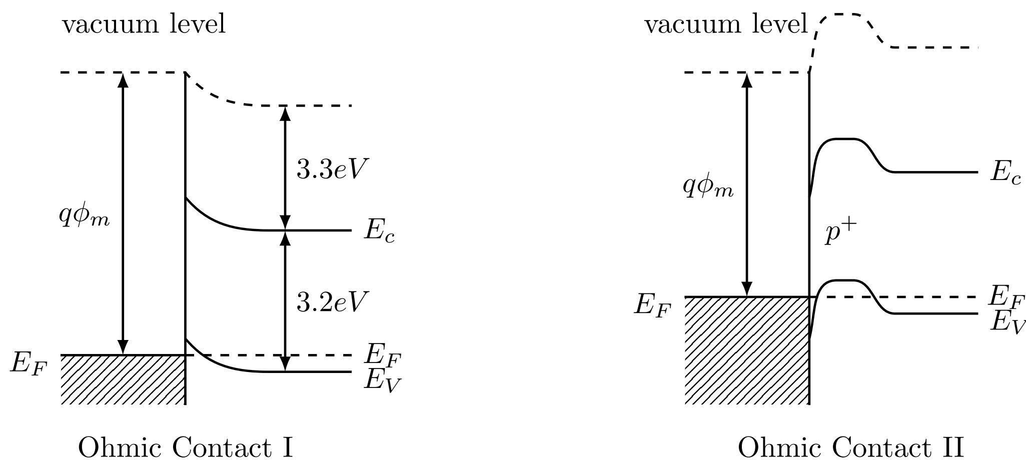


FIGURE 5.1: Energy band diagrams for the two types of Ohmic cntact on the p-type SiC.

The energy band diagram of the first method is displayed on the left side of Fig. 5.1. The wide bandgap (around 3.2 eV) of SiC, together with the high electron affinity (around 3.3 eV), leads to around 6.5 eV between the Fermi-level in p-type SiC and the vacuum level. Since most metals have a work-function in the range of 4-5.5 eV, the condition $\Phi_m > \Phi_p$ can hardly be satisfied.

Hence, the second-mentioned method of building an Ohmic contact above p-type SiC is commonly used. As the Ohmic contact II shown in Fig. 5.1, the high doping concentration p^+ impose a very steep energy bending at the interface between metal and SiC, leading to a high tunneling rate. However, producing a good Ohmic contact is extremely sensitive to the control of high doping concentration close to the metallization layer and the temperature during the process [29].

Furthermore, in the case of SiC MPS diodes, this issue becomes more critical since it involves two types of contact. In order to facilitate a high conductive Ohmic contact, i.e., a high tunneling rate through the potential barrier, the potential barrier height $\Phi_p - \Phi_m$ should be controlled to be as low as possible, meaning a metallization layer with high Φ_m should be used. However, this is in contradiction to the requirement of building a low Schottky barrier height $q\phi_{BD} = q\Phi_m - q\chi$ on top of the n- epitaxial layer, where a low Φ_m is required. Summing up the potential barrier height $(\Phi_p - \Phi_m)$ in p-type SiC semiconductor and the Schottky barrier height $q\phi_{BD} = q\Phi_m - q\chi$ in n-type SiC semiconductor equals to $q\Phi_p - q\chi$, which is approximately equal to E_g, a parameter that can be considered as constant for a specified temperature. This implies that when the same metallization layer is used, a low potential barrier in the p-type SiC doping inevitably leads to a high Schottky barrier height in the n-type doping SiC, and vice versa. This theory will be fully proved in the following.

5.2 Calibration of Simulation Models

We analyzed I-V characteristics of three types of diodes: Schottky diodes, PiN diodes, and MPS diodes located on two wafers, Wafer #1 and #2. These two wafers are fabricated using different metallization processes. Wafer #1 has a 100 nm direct deposition of Ti as anode contact, while Wafer #2 has a 20 nm deposition of Ti followed by a 75 nm deposition of Al. Both of them were alloyed for 30 mins at 680°C followed by 2 mins RTP (rapid thermal processing) at 980°C. This results in different work-function values Φ_m of the anode contact and, consequently, in different quality levels of the Ohmic contact. Except for the metallization process, the rest of the fabrication processes are identical for these two wafers.

To simulate and characterize the non-ideal behaviors of the Ohmic contact in the SiC diodes, the combination of the Schottky contact model and barrier tunneling model is used to replace the ideal Ohmic contact model in the simulation. The essential parameter in the Schottky contact model is the Schottky barrier height, which is decided by the work-function $q\Phi_m$ of the metal. The Schottky barrier height on the top of n-type doping was identified by comparing measured and simulated data of the Schottky n-type diodes. As a result, the work-function $q\Phi_m$ can be obtained and used to estimate the barrier height between the metallization layer and the p-type doping region on the same wafer. Then, with reference to the data measured on the SiC PiN diodes, the tunneling rate, or to be more specific, the so-called carrier tunneling mass (m_t), was diagnosed. Finally, equipped with these two essential calibrated physical models, non-ideal Ohmic contact behavior was simulated, and its influences on the I-V characteristics of the SiC MPS diodes are analyzed and discussed.

5.2.1 Schottky Diodes

Fig. 5.2 shows the comparison between the measured data and the simulation results for n-type Schottky diodes located on Wafer #1 and #2. The diodes on Wafer #1 have a much lower threshold voltage than those on Wafer #2. By adjusting the Schottky barrier height in the simulation setting,

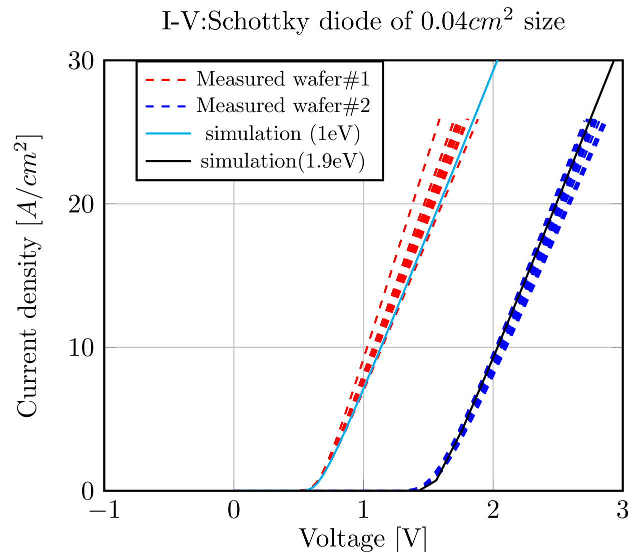


FIGURE 5.2: Comparison between the measured data and the simulated results for SiC Schottky diodes, showing that Wafer#1 and #2 have a Schottky barrier of 1 eV and 1.9 eV, respectively.

the simulated forward I-V characteristics have a high level of matching to the measured data of both wafers. The Schottky barrier height ϕ_{BD} is found to be around 1 eV in Wafer #1 and 1.9 eV in Wafer #2. Once the Schottky barrier height for the n-type semiconductor material is determined, the workfunction of the anode metal can be estimated by $q\Phi_m = \phi_{BD} + q\chi$. With the approximation $q\chi \approx 3.2eV$, we get metal workfunction values of 4.2eV and 5.1eV for Wafer #1 and #2, respectively.

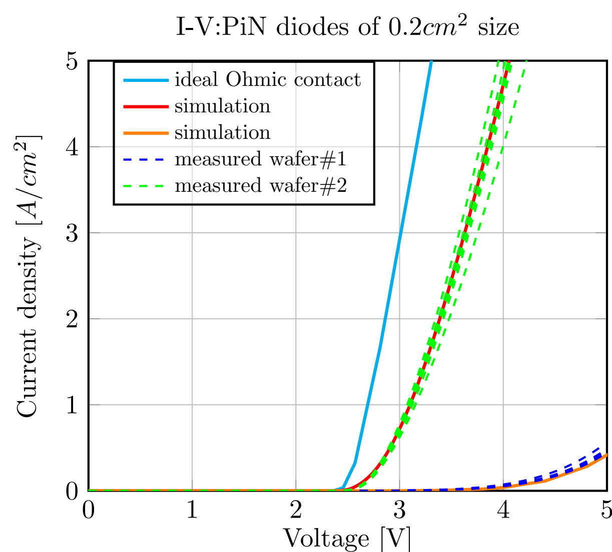


FIGURE 5.3: Comparison between measured data and the simulated results for SiC PiN diodes, showing that Wafer #2 has a superior quality of the Ohmic contact than Wafer #1.

5.2.2 PiN Diodes

The physical mechanism of an Ohmic tunnel contact is a combination of thermionic emission and field emission, called "thermionic field emission" [30]. In our simulations, we employed the Schottky contact model for describing the thermionic emission and the contact barrier tunneling model for describing the field emission, replacing the commonly used ideal Ohmic contact model.

The measured data obtained from the PiN diodes are shown in Fig. 5.3. In contrast to Schottky diodes, SiC PiN diodes located on Wafer #2 have a lower threshold voltage, reflecting the better quality of the Ohmic contact. This meets our expectations, when we calculated the barrier height $q\Phi_{Bp}$ with the relation $q\Phi_{Bp} = q\Phi_p - q\Phi_m$, and found out that a lower barrier height (1.2eV) is formed on Wafer #2 than that (2.1eV) on Wafter #1. Furthermore, this exactly matches with what was mentioned before, a low Schottky barrier height in the n-type SiC doping region leads to a poor Ohmic contact on the top of the p^+ doping region.

Despite of the low barrier height for tunneling, the anode contact of the SiC PiN diodes on Wafer #2 is still different from an ideal Ohmic contact, since there are still lifetimes of the charge carriers and other physical parameters that influence the quality of the contact. Nevertheless, we obtain a better Ohmic contact for p-type SiC material, but a higher Schottky contact threshold voltage in Wafer #2.

5.3 Impact on the I-V Characteristics of MPS Diodes

As a consequence of poor Ohmic contacts, we have to cope with serious problems, namely a shifting threshold voltage, low conductivity, and no noticeable resistance modulation by minority carrier injection, when we attempt to match the measured real-life data to the simulated results of SiC MPS diodes. Based on detailed simulation insights, we provide deep physical understandings and qualitative explanations of the observed phenomena.

5.3.1 Shift of the Threshold Voltage (V_{th})

Ideal MPS diodes should have a similar V_{th} as Schottky diodes taking the same metallization process. However, a shift of V_{th} to a much higher value than that of Schottky diodes was observed on the MPS diodes with a topology of $2\mu m$ long Schottky contact and $2\mu m$ long Ohmic contact (represented as $W_o + W_s = 2\mu m + 2\mu m$ in a 2D layout) in Fig. 5.4. A comparison of measured data of the MPS diodes between Wafer #1 and Wafer #2 reveals that ΔV, the shift of V_{th}, is larger in Wafer #1 than in Wafer #2. This is caused by different conductivity of Ohmic contact in Wafer #1 and #2.

The clear discrepant shifting of the threshold voltage does not only show in the comparison between Wafer #1 and #2, but is also observed when comparing MPS diodes with different topologies of W_s and W_o located on the same Wafer #2. As seen in Fig. 5.5, the MPS diodes ($W_o + W_s = 2\mu m + 4\mu m$) with a larger Schottky contact area exhibit a smaller ΔV then the MPS diodes ($W_o+W_s = 2\mu m+2\mu m$). In order to explore the physical reasons that cause the variance of ΔV, simulations with different conductivity of the Ohmic contact and lengths of the Schottky contact were implemented.

The simulation results reveal that the shifting of V_{th} is caused by the retarded shrinking of the depletion layer built along the p^+n^- junction. Fig. 5.6 illustrates the shifting of the position of the depletion line (white) in the n^- region in the SiC MPS diodes ($W_o + W_s = 2\mu m + 2\mu m$), with an increasing applied voltage. Although the depletion line keeps withdrawing towards the p^+n^- junction line, the shrinking of the depletion region is not large enough to allow the electron current to flow through until the applied voltage is more than 2V. Therefore, even though the applied voltage already exceeds the threshold voltage of the Schottky contact, devices are still not conducting current.

For an ideal Ohmic contact, there is no additional voltage drop across the Ohmic contact. Before the increasing applied voltage reaches the threshold voltage V_{th} of the Schottky contact, the depletion layer has already shrunk down to a size that enables the electron current flow through the Schottky contact. As a consequence of poor conductivity of the Ohmic contact, an additional voltage drop is spent across the Ohmic contact and less applied voltage works on the forward bias of the p^+n^- junction. As a consequence, the depletion layer shrinks less or even stays the same size as the forward applied voltage increases. Thus, the current channel underneath the Schottky contact is pinched off by the depletion regions of the neighboring p^+n^- junctions, leading to the shifting of V_{th} to a much larger value.

On the other hand, a larger W_s means a wider distance between the neighboring p^+n^- junctions, and consequently, less shrinking of the size of the depletion regions is required to allow for a current path

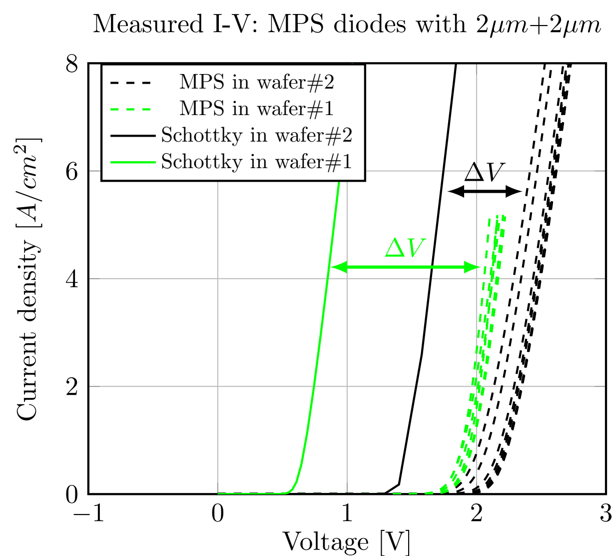


FIGURE 5.4: Comparison between Wafer #1 and #2 with respect to the shifting ΔV of the threshold voltage of the MPS diodes with the same topology $W_o+W_s = 2\mu m+2\mu m$.

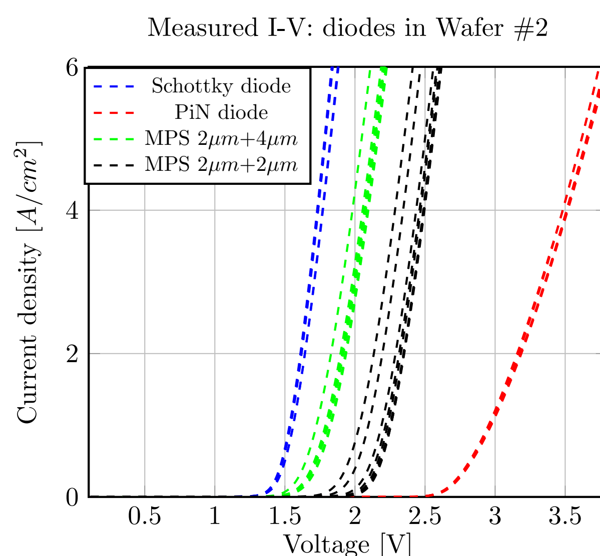


FIGURE 5.5: Measured data: The MPS diodes with $W_o + W_s = 2\mu m + 4\mu m$ exhibit a less threshold voltage shifting than the MPS diodes with $W_o + W_s = 2\mu m + 2\mu m$ on the same wafer.

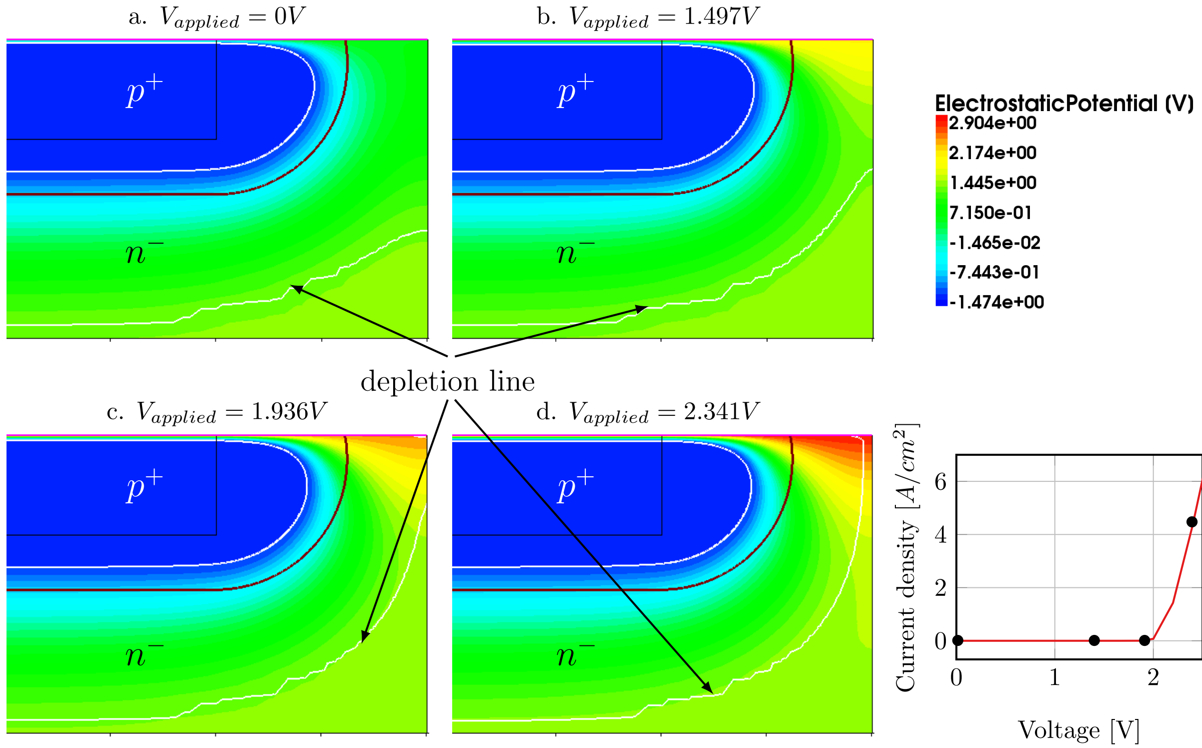


FIGURE 5.6: The depletion region of the p^+n^- junction is, with the increasing forward voltage, not reduced enough to open the bypass for the current flowing towards the Schottky contact. Consequently, the threshold voltage of the MPS diode is shifted to a higher value.

through the Schottky contact. Therefore MPS diodes with topology $W_o + W_s = 2\mu m + 4\mu m$ have a less ΔV than the ones with topology $W_o + W_s = 2\mu m + 2\mu m$.

5.3.2 Shift of the Trigger Voltage (V_{turn}) for Bipolar Operation

The trigger voltage V_{turn} is defined as the value of the externally applied bias voltage at which the bipolar operation of an MPS diode sets on. Assuming the evident bipolar injection occurs when the concentration of the injected minority carriers attains a double value of the background doping concentration, the shifting of the trigger voltage δV_{turn} can be estimated as $R_{con} * 2qD_pN_{epi}/L_p$, where R_{con} is the additional contact resistance of the non-ideal Ohmic contact and $2qD_pN_{epi}/L_p$ is the current density across the p^+n^- junction. Consequently, a larger R_{con} can cause a larger δV_{turn}. One should note that, in some cases, R_{con} even proves to be a voltage-dependent quantity.

5.3.3 Degradation of the Surge Current Capability

The surge current capability of MPS diodes refers to the quick response of the device to an over-current pulse by switching to a highly conductive state in bipolar operation mode, thus preventing destruction by self-heating or thermal runaway after the on-set of surge current. A high surge current capability implies and requires a steep slope dI/dU requiring a high injection rate of the minority carrier, i.e., $\partial p/\partial U$.

However, the non-ideal Ohmic contact reduces the injection rate $\partial p/\partial U$ from $\partial p/\partial(V_j + V_{epi2})$ [14] to a lower value as $\partial p/\partial(V_j + V_{epi2} + V_{con})$, where V_{epi2} and V_j are the voltage drops along the epitaxial layer and the p^+n^- junction. Thus the reduced carrier injection rate $\partial p/\partial V$ impedes or even prevents

the rapid rise of current density and, therefore, can only produce a moderate slope dI/dV, instead of exponential growth.

5.4 Possible Solutions of the Contact Pattern

The requirement on the workfunction of metal to form a low Schottky barrier height on the top of n-type doping conflicts with the one facilitating a low potential barrier height on the top of p-type doping SiC, ensuring high tunneling rate. There are two possible solutions:

- Separated fabrication processes to form the Schottky contact and Ohmic contact.
- Avoiding Ohmic contact on the top of p-type doping SiC by adding an n^- layer on top of the whole MPS structure. Thus, a homogeneous uniform Schottky contact is obtained [31].

Chapter 6

Analysis of Cosmic Ray Induced Current

In the early 1990s, spontaneous failures in Si high power devices were found and have been proved to be caused by cosmic radiation [32]. Since then, cosmic radiation-induced failures in semiconductor power devices have been extensively studied.

Due to its excellent material properties, such as high breakdown electric field and high thermal conductivity, SiC is expected to exhibit higher robustness against cosmic radiation-induced failure than Si. However, the sensitivity of SiC power devices to cosmic radiation has been found to be higher than expected [1][19].

A physics-based accurate numerical analysis of the reaction of SiC diodes after the impact of a heavy ion can provide valuable insights into how to utilize the specific material properties of SiC to a maximal extent.

With the target of extending the predictive high-fidelity simulation technique for cosmic ray-induced failure analysis from Si PiN [33] to SiC PiN diodes, this chapter compares simulated ion-induced current transients between Si and SiC PiN diode with the same blocking voltage. The differences of the ion-induced current transients were identified and the physical effects causing the differences are analyzed. In the meanwhile, the density of mesh grids and transient simulation steps are adapted with several variants in order to explore their influence on the simulated ion-induced current transients.

All simulation results presented in this chapter are based on quasi-3D cylindrical symmetric device structures.

6.1 Heavy Ion Generation Model

When high power semiconductor devices are exposed to real-world cosmic radiation, neutrons have been identified as the major threat, since they can easily penetrate the atmosphere, walls, and the device housing and, and after that, undergo a nuclear reaction with the Si or C nuclei inside the devices [34]. The spallation products are high-energetic heavy ions, which, in turn, generate a tube of electron-hole plasma that can lead to a short-circuit between anode and cathode across the intrinsic region, and eventually thermal damage of semiconductor devices.

In experimental investigations, however, it is preferable to trigger the failure process by the heavy ions directly generated in an ion accelerator, which allows one to exactly control the species and the energy of the heavy ions, and thus the amount and the distribution of the deposited initial electron-hole pairs inside the devices. In the corresponding computer simulations of TCAD, the product of the high-energetic heavy ions, i.e. the initial tube-shaped electron-hole plasma, is directly used to explore the internal reaction of the charge carriers and the influences on the electric field distribution and temperature, etc. inside the semiconductor devices. The model describing the transient amount in an ultra-short time scale of the deposited electron-hole plasma and its spatial distribution is called

the heavy ion model. The mathematical expression is as followed:

$$\begin{aligned} G(W,l,t) &= G_{LET}(l)\cdot R(W,l)\cdot T(t) \\ &= LET_f \cdot exp(-\frac{W}{W_t(l)})\cdot \frac{2\cdot exp(-(\frac{t-t_0}{\sqrt{2}\cdot s_{hi}})^2)}{\sqrt{2}\cdot s_{hi}\sqrt{\pi}(1+erf(\frac{t_0}{\sqrt{2}S_{hi}}))}, \end{aligned} \tag{6.1}$$

where $G_{LET}(l)$ is the electron-hole pairs generation rate, while $R(W,l)$ and $T(t)$ are the functions describing the spatial and temporal variations of the generation rate. One should note that l and W are the variables representing the distance along and perpendicular to the central track of the heavy ion. LET stands for linear energy transfer, while t_0 indicates the moment when the generation rate of the electron-hole plasma reaches its peak value, and $W_t(l)$ and S_{hi} are the characteristic width and the characteristic time.

Table 6.1 lists the parameters that have been well-proven in the predictive simulations of Si PiN diodes and conformed well with measured data [33]. This model assumes a constant linear energy transfer (LET) along the track of the heavy ion travelling with a length of 19.8 μm until it stops. The peak value of LET (Linear Energy Transfer) is 0.07 $pC/\mu m$ at the moment of 5 ps. Gaussian distributions are used in space and in duration with the characteristic values of 20 nm and 1ps, respectively.

TABLE 6.1: Model parameters of the initial charge deposition caused by the spallation products (heavy ions).

Length	LET	Charact.Width	Charact.Time	Peak Generation time
19.8 μm	0.07$pC/\mu m$	20 nm	1ps	5 ps

The spectrum of heavy ions emerging as spallation products after the impact of a cosmic particle on a nucleus of the crystalline lattice of Si or SiC devices is diverse [35]. Their variation is mainly reflected by different values of LET and Length. Table 6.2 gives five ion species used in the experiments of SiC devices as examples to show different energy levels and LET values.

TABLE 6.2: Characteristics of ion species used for the experiments of SiC devices from report [19].

Ion Specy	Energy [MeV]	LET [$MeVcm^2/mg$]	LET [$pC/\mu m$]	Length[μm]
$^{15}N^{3+}$	53.2	3.6	0.025	33.7
$^{20}Ne^{4+}$	69.7	6.9	0.047	25.9
$^{40}Ar^{8+}$	137	16.7	0.11	23.9
$^{84}Kr^{17+}$	289	42.7	0.29	24.7
$^{129}Xe^{23+}$	394	73.1	0.50	23.1

The corresponding values of LET are given in two units, $MeVcm^2/mg$ and $pC/\mu m$ (the one is used our TCAD simulation). The equation to exchange these two units is as following,

$$\begin{aligned} 1MeVcm^2/mg\cdot \rho_{SiC}/E_{SiC}\cdot q &= 1MeVcm^2/mg\cdot 3210mg/cm^3/7.5eV\cdot 1.6\cdot 10^{-19}C \\ &= 6.84\cdot 10^{-11}C/cm \\ &= 6.84\cdot 10^{-3}pC/\mu m, \end{aligned} \tag{6.2}$$

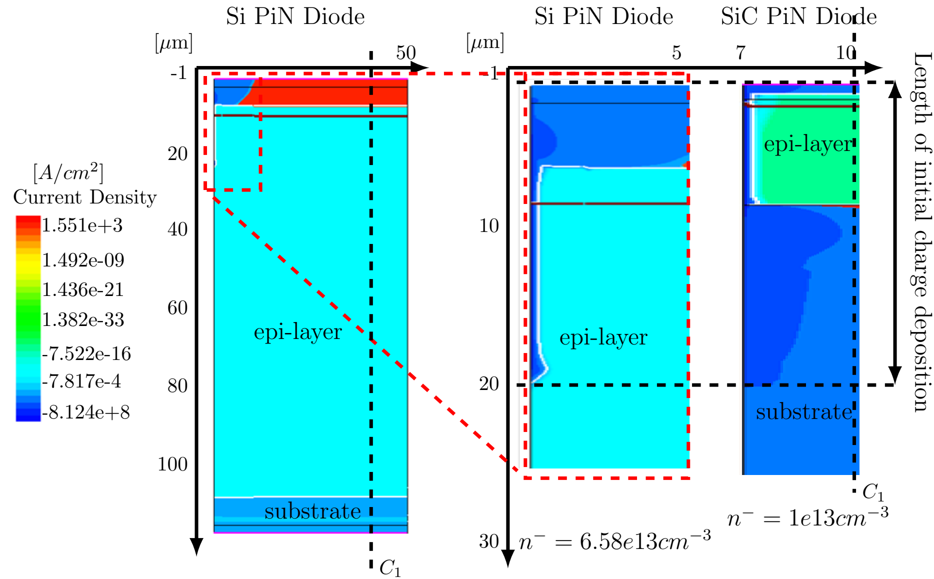


FIGURE 6.1: The device structure of the Si PiN diode and the SiC PiN diode designed for the same nominal blocking voltage of 1.5kV, and the distribution of the conduction current density at t = 5ps are plotted.

where ρ_{SiC} is the mass density of silicon carbide and E_{SiC} is the electron-hole pair creation energy.

In order to reveal the influence of the material properties, such as impact ionization and incomplete ionization of the dopants, on the robustness against cosmic radiation, we compared the internal physical behavior of Si PiN diodes and SiC PiN diodes having identical device structure and being exposed to the same initial charge deposition.

6.2 Device Structure

Our comparative study refers to a Si and a SiC PiN diode designed for the same nominal blocking voltage of 1.5kV. The major difference between these two targeted diodes is the thickness of the epitaxial layer. As shown in Fig.6.1, the thickness of the n^--epitaxial layer is $8\mu m$ for the SiC PiN diode and $110\mu m$ for the SiC PiN diode. Their doping concentrations in the n^- epitaxial layer are on a comparable level, with $6.58 \times 10^{13} cm^{-3}$ in the Si PiN diodes and $1 \times 10^{13} cm^{-3}$ in the SiC PiN diodes.

Under a pre-bias reverse voltage of 900V, the electric field distributions in these two devices along a cut-line C_1 (see Fig. 6.1) are plotted in Fig. 6.2. The peak value of the electric field strength in the SiC PiN diode is approximately 10 times the one in the Si PiN diode.

In order to give a direct comparison, we applied the same heavy ion model parameters listed in Table 6.1 for both Si and SiC PiN Diodes. As indicated by the parameter of length in the table, the electron-hole plasma deposited by the spallation products reaches a depth of around $20\mu m$ (counting from anode contact into the bulk), a value shorter than the depth of the epitaxial layer in the Si PiN diode, but longer than the one in the SiC PiN diode, as shown in Fig. 6.1. Consequently, this leads to two different mechanisms of the ion-induced current generated in the SiC and the Si PiN diodes, reflected not only on two different levels of the maximum ion-induced current but also on the different total duration of the ion-induced current (see Fig. 6.3).

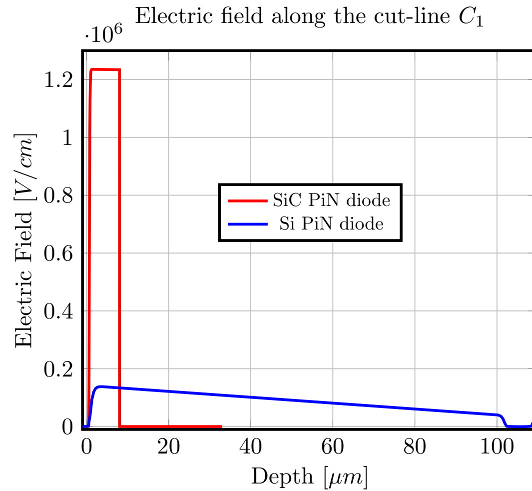


FIGURE 6.2: The electric field distributions along a cut-line C_1 (see Fig. 6.1) in the SiC and Si PiN diodes are plotted.

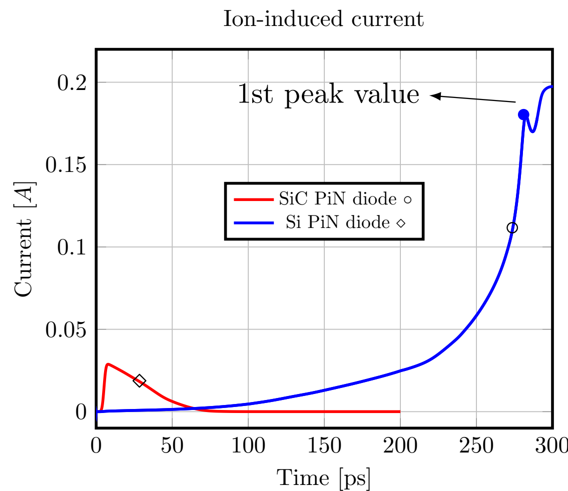


FIGURE 6.3: Transient ion-induced current after the impact of a cosmic particle (reverse bias voltage 900V).

6.3 Physical Mechanisms of the Ion-induced Current

Before the impact of a cosmic particle, semiconductor devices are in blocking mode. The epitaxial layers are completely depleted, meaning there are no mobile charge carriers. This situation is changed immediately after the creation of electron-hole plasma by the heavy ions.

In the case of the Si PiN diode, due to the wide epitaxial layer, the initial charge deposited by the heavy ion cannot build an immediate plasma channel between anode and cathode. As illustrated in Fig.6.1, a high current density (indicated by dark blue) appears only in the non-depleted region, such as the substrate close to the cathode and the p^+ region below the anode, and the partial epitaxial layer where the plasma charges are deposited. For the remaining part of the epitaxial layer, there is only negligible current flow. The discontinuity in the current distribution indicates that the Si PiN diode is operating like a capacitor, instead of a conductor where the plasma channel is fully developed.

However, if the applied voltage is high enough, as the evolution of plasma filament outlined in Fig.6.4, the plasma channel would be built connecting the anode and cathode.

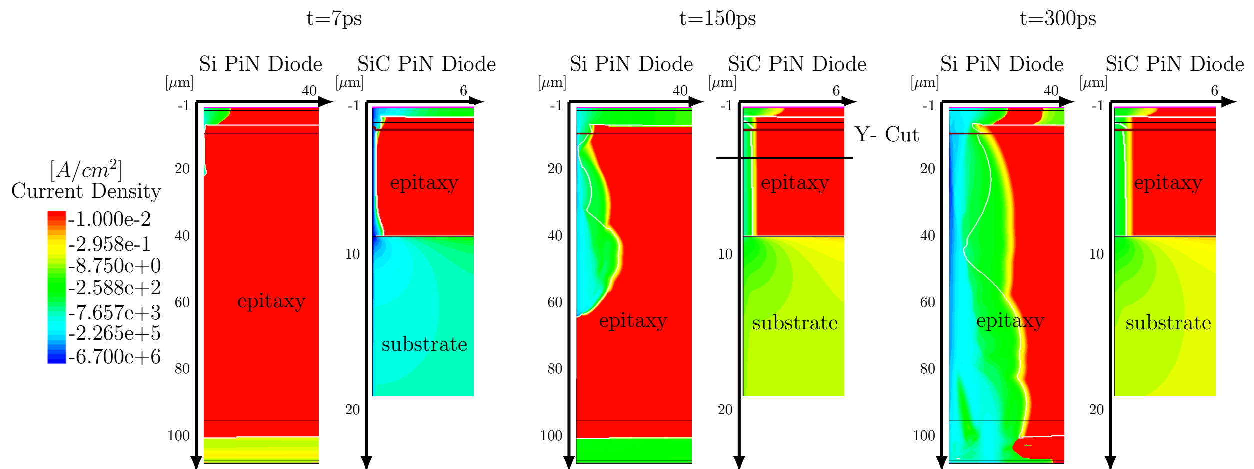


FIGURE 6.4: Distribution of the current density in SiC and Si PiN diodes at time moments of 8ps, 150 ps, and 300ps.

At t=7ps, the initially deposited electrons and holes only appear around the track of the heavy ion. Nevertheless, due to their different polarity, the deposited electrons and holes are pulled to opposite directions, towards the cathode and the anode, respectively. As a result, electrons accumulate at the rim of the lower part of the plasma region, resulting in a high electron density and a consequent high electric field. At certain circumstances, this localized high electric field is high enough to cause impact ionization, which, in turn, generates extra electron-hole pairs, leading to an even higher electron density at the rim of the plasma region. In such a way, a positive feedback loop between the generation of electron-hole pairs and the resulted high electric field is formed.

This positive feedback enables the plasma region to penetrate rapidly into the bulk (t=150ps) and eventually reach the substrate (t=300ps), building a complete current path (a plasma channel) between the anode and cathode. This whole process is analogous to streamer discharge, a type of transient electrical discharge which forms at the surface of a conductive electrode carrying a high voltage in an insulating medium, such as air. Until now, all what have been described happen in "Phase 1". The Si diode enters “Phase 2” only after a fully conductive current filament is formed.

One should note that right before the streamer arrives at the cathode, the electric field peak attains its peak value, which results in the 1st peak value in the ion-induced current transient shown in Fig.6.3.

In contrast to that, the SiC PiN diode enters “Phase 2” immediately after the impact of a cosmic particle. Regardless of the strength of the local electric field (i.e. the pre-bias reverse voltage), a connected plasma filament is formed as an ion-induced current path (see Fig.6.4). As a result, the ion-induced current rises dramatically and rapidly attains its peak value at 7ps (see Fig.6.3). The time scale of the current rise is in the same order of magnitude as the characteristic time of the heavy ion model in Table 1. This indicates that the current in the SiC PiN is mainly contributed by the initially deposited electron-hole plasma charges, not by the subsequent charge carriers generated by the impact ionization. As a consequence of the short carrier lifetime in the SiC epitaxial layer, the ion-induced current shows a quick fall down. Furthermore, the plasma region does not show a significant expansion in the SiC PiN diode, when we compare the current density distribution at 7ps, 150ps, and 300ps displayed in Fig.6.4.

Despite of the fact that the same amount of charge is deposited by the spallation products, there is a large difference in the peak values of the ion-induced current between the SiC diode and Si diode. This is caused by the large amount of additional carrier charge generated by impact ionization in the Si PiN diode during the continuous expansion of the plasma streamer until a fully connected current filament between anode and cathode is formed. Furthermore, in consequence of both charge carrier

diffusion and local impact ionization, the resulting current path has a larger cross-section than that encountered in the SiC diode. Therefore, Si PiN diodes conduct a higher ion-induced current than SiC PiN diodes, where we see negligible local impact ionization only.

6.3.1 Dependence on the LET

One may argue that SiC has a much higher ionization energy than Si, so the assumption of the same LET for the comparison would be inappropriate. But one should note that our comparative study focuses on the physical mechanisms of the ion-induced transient current, and not on the open question of whether SiC or Si devices exhibit better robustness against cosmic radiation. Furthermore, the lengths of the initial charge deposition reported in the previous study [19] [35] is at least $23\mu m$, a distance much longer than the thickness of the epitaxial layer in the SiC PiN diode considered here. In this case, the influence of the LET on the ion-induced current transients is no longer significant. Fig.6.5 shows the current transients for three different LET values. These three current curves show the same shape and duration. The peak values of the current transients are proportional to the LET values, i.e.

$$\frac{0.0419A}{0.1pC/\mu m} \approx \frac{0.0290A}{0.07pC/\mu m} \approx \frac{0.0103A}{0.025pC/\mu m}. \tag{6.3}$$

6.3.2 Dependence on the pre-bias Voltage

As well known, the failure rate of single event burnout (SEB) increases dramatically for Si PiN diodes, when the reverse voltage exceeds a certain value. Different from that, SiC PiN diodes are reported to have a leakage current degradation (a new phenomenon) at medium and low reverse voltage, in addition to the SEB occurring at relatively high voltage [1] [36].

Fig.6.6 illustrates the dependence of the ion-induced transient current in SiC (I) and Si PiN diodes (II) on the reverse bias voltage. In the case of Si PiN diodes, there is a distinct difference in the transient current between the bias voltage 700V and 600V, indicating the threshold voltage for the onset of localized charge multiplication due to impact ionization. On the other hand, SiC PiN diodes have similar current transients for a wide range (500V-900V) of the varying bias voltages. At the same low reverse voltage level, such as 600V, the ion-induced current in SiC PiN diodes is much higher than that in Si PiN diodes. This finding partly explains why SiC devices have been seriously

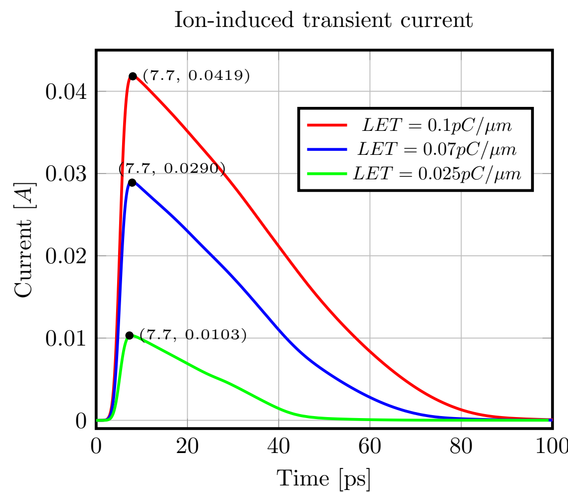


FIGURE 6.5: Ion-induced transient current of SiC PiN diodes with different LET values in the heavy ion model.

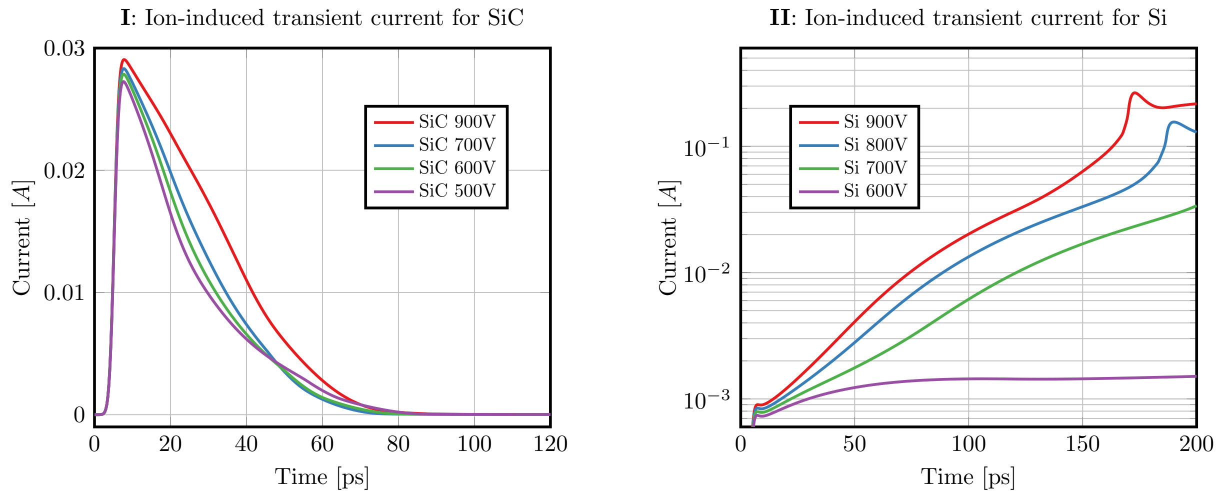


FIGURE 6.6: The simulated ion-induced current transients of SiC and Si PiN diode under different pre-biased reverse voltage.

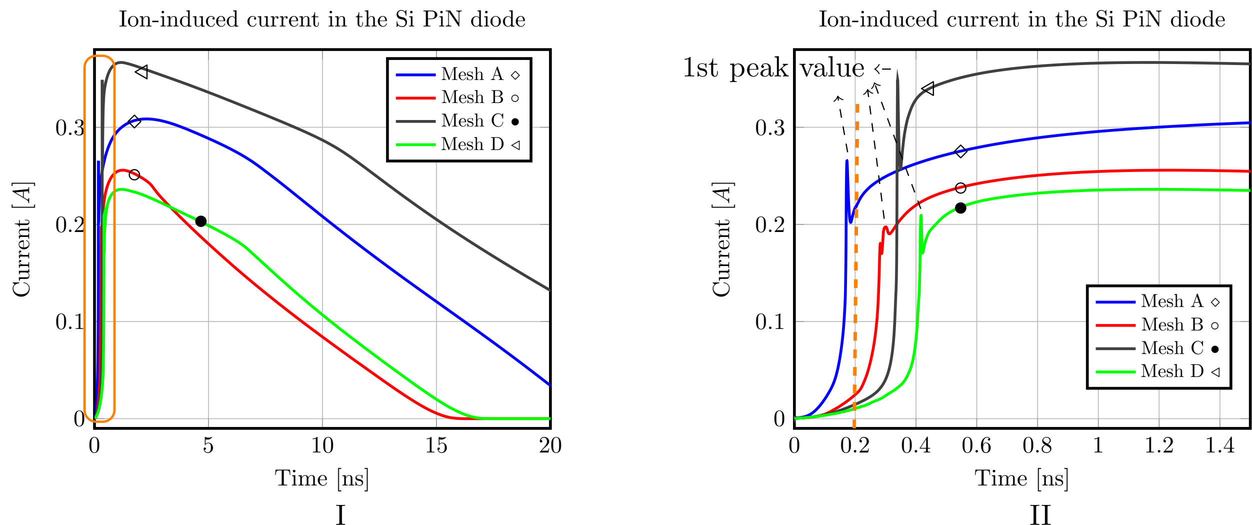


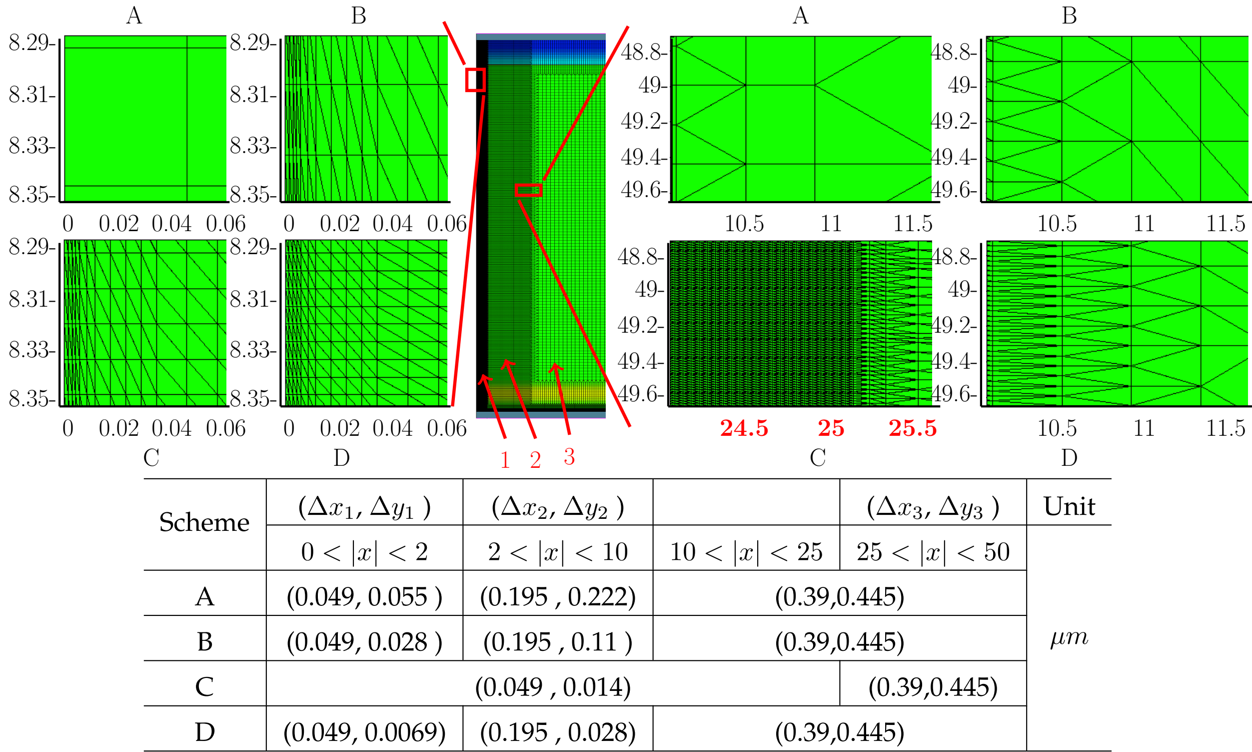
FIGURE 6.7: Different ion-induced current transients obtained from simulations with four different meshes. II is the zoom-in of the rectangular window highlighted in orange in I.

damaged even at a quarter of the rated reverse voltage under ion irradiation with energy at an order of magnitude of $10MeV \cdot cm^2/mg$ [1].

6.3.3 Sensitivity to Mesh Adaptation and Refinement

In order to ensure the high accuracy of the transient simulations, the dependence of the simulated results on the meshing scheme and time stepping has been explored. We found that the simulation results are highly sensitive to the discretization grid in the plasma region and its dynamically developing rim during the development of a current filament in the Si PiN diodes.

We compared four different mesh schemes (A, B, C, D) shown in Fig. 6.8. The mesh in Si PiN diode consists of three regions with the finest one "1" located at position "$0 < |x| < 2\mu m$"(in cylindrical coordinates), within which the initial charge is deposited by the heavy ions, and the second finest "2" located at position "$2\mu m < |x| < 10\mu m$" in the cases A, B, and D, and "$2\mu m < |x| < 25\mu m$" in the case C. The simulated ion-induced current transients obtained with these four different mesh adaptation



Scheme	$(\Delta x_1, \Delta y_1)$	$(\Delta x_2, \Delta y_2)$		$(\Delta x_3, \Delta y_3)$	Unit
	$0 < \lvert x \rvert < 2$	$2 < \lvert x \rvert < 10$	$10 < \lvert x \rvert < 25$	$25 < \lvert x \rvert < 50$	
A	(0.049, 0.055)	(0.195 , 0.222)	(0.39,0.445)		μm
B	(0.049, 0.028)	(0.195 , 0.11)	(0.39,0.445)		
C	(0.049 , 0.014)			(0.39,0.445)	
D	(0.049, 0.0069)	(0.195 , 0.028)	(0.39,0.445)		

FIGURE 6.8: Overview of four different mesh adaptation schemes.

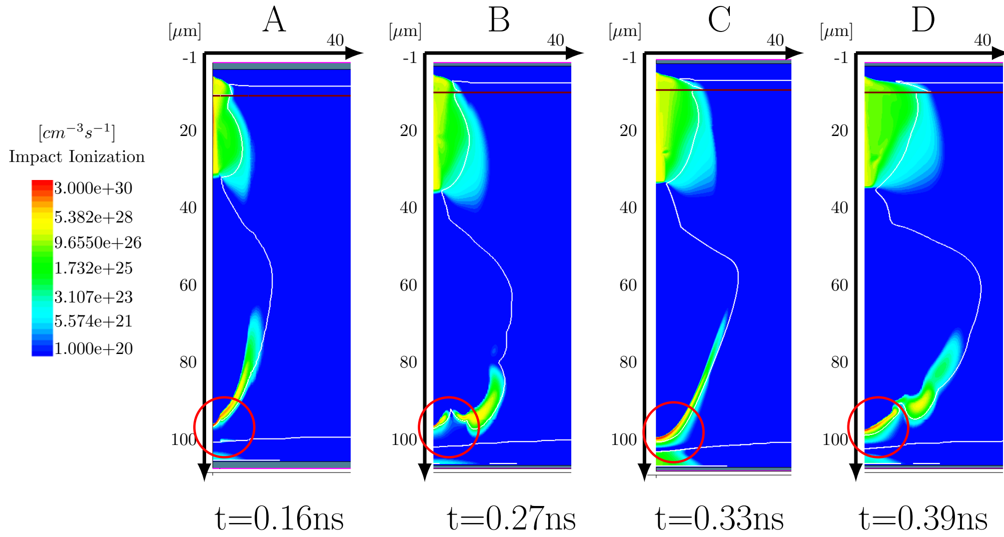


FIGURE 6.9: The impact ionization distribution for the four mesh schemes at the moment of reaching their peak value of the transient current. The white lines are the boundary of plasma charge region.

schemes are shown in Fig. 6.7. *I*. Fig. 6.7. *II* displays a zoom-in of the slope of the rising transient current so that one can see clearly the differences among these four curves.

The densities of the mesh grids in region "1" are reflected by the distance between the nearest nodes, such as the $\Delta y_{1,A}$ in the mesh schemes A. From the table listed in Fig. 6.8, we see that $\Delta y_{1,A} > \Delta y_{1,B} > \Delta y_{1,C} > \Delta y_{1,D}$, meaning the density of the mesh grids in mesh schemes A, B, C, and D are in a sequence from low to high. And this sequence is reflected in the curves of the transient current in Fig. 6.7: With mesh A the peak value is attained fastest, while with mesh D we find a 2 times slower

rise of the ion-induced current. Large Δy overestimates the expansion of the plasma charge region in the vertical direction and, consequently, a faster evolution of the fully developed plasma channel reflected in the peak value of the transient current.

Another major difference in the ion-induced transient currents shown in Fig.6.7 is visible in their peak values. Mesh C has the maximum one, followed by mesh A and D, while mesh B has the lowest one. This is because mesh A and C have a sharper downward-impinging angle α of the plasma region (highlighted with red circles in Fig. 6.9), resulting in a localized high electric field peak that excessively generates plasma charge by impact ionization and, consequently, a higher ion-induced current density during the development of the current filament. Mesh B, on the other hand, has the bluntest downward-impinging angle of the plasma region and consequently a lower transient current.

The downward-impinging angle α of the plasma region is influenced by two values:

- $\Delta x/\Delta y$

  Compared with other mesh schemes, mesh A has the smallest values of $\Delta x_1/\Delta y_1$ and $\Delta x_2/\Delta y_2$, and consequently the least expansion of the plasma region in the x direction and the sharpest angle α. Therefore, as indicated by the areas enclosed by the white line shown in Fig. 6.9, mesh A has the narrowest plasma channel. Furthermore, due to the least expansion of the plasma region in the x direction, the second value $\Delta y_2 - \Delta y_1$ plays less importance in the case of mesh A.

- $\Delta y_2 - \Delta y_1$

  The value of $\Delta y_2 - \Delta y_1$ plays a decisive role in the comparison among mesh B, C, and D. A large value of $\Delta y_2 - \Delta y_1$ may even fake a faster expansion (in the y-direction) of the plasma charge in region "2" than in "1", as we can see from the rim of the plasma region in mesh B high lighted by the red circle in Fig. 6.9. Mesh C, on the other hand, has the same value of Δy_2 and Δy_1, has the sharpest angle α.

In summary, an accurate transient simulation of the evolution of a "streamer" inside a semiconductor device requires a high density of grid nodes with the proper values of $\Delta x/\Delta y$ and $\Delta y_2 - \Delta y_1$ in the plasma charge region. However, the requirements on mesh size and time stepping constitute a virtually prohibitive computational expense to obtain predictive high fidelity simulation results. Taking mesh scheme C for the Si PiN diode (which has the largest number of grid nodes) as an example, a 20ns transient simulation took more than 20 days of the wall clock and 10 times more of the CPU time on a high-performance computer cluster. The optimum mesh setting should be decided and calibrated according to experiments and investigation targets.

On the other hand, the simulated ion-induced current curves obtained from different mesh scheme adaptations are found to be similar in SiC PiN diodes (see Fig.6.10), because the ion-induced current is mainly contributed by the initial charge deposition, while local impact ionization is negligible. On the right-hand side of Fig.6.10, the impact ionization rate distributions at t=7.5ps (the moment of the peak current) and t=18.75ps are displayed. The plasma charge region expands along the direction marked by the red arrow. However, the impact ionization rate decreases during the expansion of the plasma charge region, since the expansion direction is not the same as the direction of the electric field forced by the reverse voltage. Therefore, the amount of generated electron-hole pairs is not large enough to cause a significant increase in the transient current. As a result, the transient current shows a similar time-dependence controlled by the initial charge deposition.

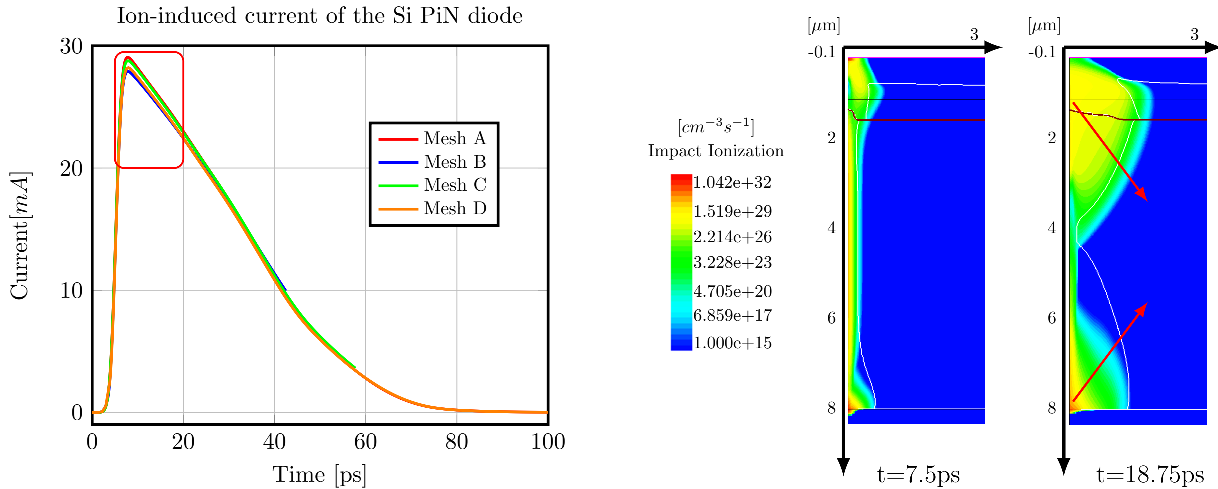


FIGURE 6.10: Left: Dependence of ion-induced current transients in SiC PiN diodes on the mesh settings; Right: Distributions of impact ionization inside the device at time 0.75ps and 18.75ps.

6.3.4 Electro-Thermal Simulation

It has been reported that in the simulations of cosmic radiation-induced failures in Si devices, there is no significant difference between the isothermal simulation at elevated temperature and the electrothermally coupled simulation [33] [37]. In order to explore that in SiC devices, isothermal and electrothermally coupled simulations were performed using the SiC PiN diode considered above. In the electrothermal simulation, the temperature dependence of the physical model parameters, such as energy bandgap E_g [38], mobility [39], and impact ionization rate [40], have been carefully selected. It should be mentioned that the minority carrier lifetime, a quantity that is strongly dependent on the technology process, has been chosen to be around 140ns in the intrinsic region. The decisive parameter (power factor) for the temperature dependence of the carrier lifetime is set to be 1.72. As it is reported in [41], it still needs to be calibrated with reference to recent experimental findings. In addition, the physical models describing the temperature-dependence of heat capacity and thermal conductivity have been adjusted to fit the experimental data up to 3000K [42], close to the melting point.

Fig. 6.11. A shows the comparison of the ion-induced current between the isothermal (S_1) and the electrothermally coupled (S_2) simulations. The discrepancies of the ion-induced current between $S_1$and S_2 start to become evident after the temperature exceeds 500K. In order to identify which physical properties of the material have the dominant influence on the simulation results, several test simulations were done. We disabled the temperature dependence of each physical property individually one by one and compared them with S_1 and S_2 as reference. In the end, we found that the simulation with disabled temperature-dependence in the mobility model nearly completely coincides with the isothermal simulation S_1 (see Fig. 6.11. A).

In order to explore it in more details, we made a cutline ("Y-Cut") at a vertical position $y = 4\mu m$ as shown in Fig. 6.4, so that we can clearly discriminate along this cut line (the cross-section of current flow), which physical parameter causes the difference in the ion-induced current. As mentioned above, the current filament is formed immediately after the impact of a cosmic particle. Therefore, the ion-induced current is mainly a drift current, in which mobility and carrier density are the key parameters. In contrast to the Si PiN diode, where the temperature-dependence of impact ionization is the key factor to be focused on [33], we find a different situation in the SiC diode. Taking the hole current density as an example, Fig. 6.11. B displays the hole mobility and the hole density along the cutline "Y-Cut". Although the intrinsic concentration rises at high temperature and, thus, also the

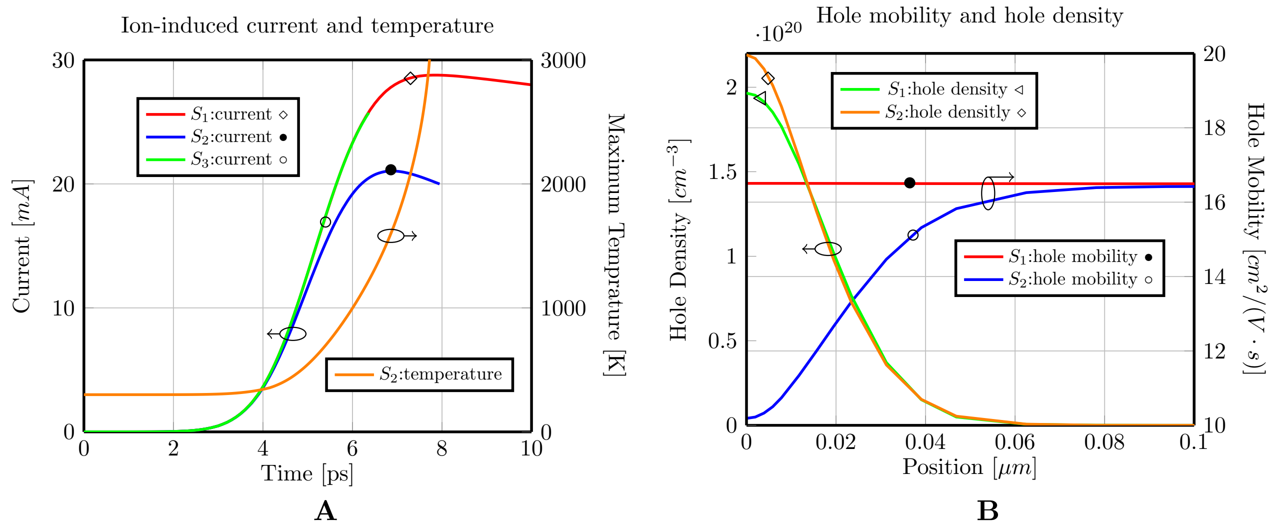


FIGURE 6.11: **A**: Comparison of the ion-induced current among S_1, S_2 and S_3. **B**: Comparison between S_1 and S_2 along the Y-cutline (cf. Fig. 6.4). S_1: isothermal simulation, S_2: electrothermal simulation, and S_3: electrothermal simulation with temperature-dependence in the mobility model disabled.

hole density, the thermal degradation of mobility is yet the dominating effect. The increase of the hole density cannot compensate the reduction of hole mobility, which degrades from around $16cm^2/(V \cdot s)$ to $10cm^2/(V \cdot s)$. Therefore the electrothermal simulation yields a lower current density.

In the case of Si PiN, it has been identified that localized high Joule heating $|\vec{E}| \cdot |\vec{J}|$ is dramatically increased in such a short time that heat conduction within the device itself, the temperature dependence of carrier ionization and carrier mobility model can be neglected.[33]

6.4 Summary

We performed high-fidelity simulations of Si and SiC PiN diodes with the same blocking voltage of 1.5kV with a view to investigating the cosmic ray-induced high transient current. Due to the different thicknesses of the epitaxial layers, the physical mechanisms underlying the ion-induced current are different. Using the same model for the initial charge deposition after the impact of a cosmic particle and the same reverse voltage of 900V, a higher ion-induced current is observed in the Si PiN diode due to the additional impact ionization caused by the local high electric field. In the SiC diode, an immediate current channel is formed after the impact of a cosmic particle, exhibiting mainly drift current in a short duration. In addition, the influence of mesh adaptations on the simulated results has been illustrated. In the end, the comparison between isothermal and electrothermally coupled simulation results for a SiC PiN diode indicates again that current transport in SiC PiN diodes is dominated by the drift model.

Chapter 7

Summary & Outlook

SiC MPS diodes with blocking voltage of 600V or 1.2kV are showing excellent device performance, such as their low on-resistance in nominal operation, high surge current capability, and high avalanche ruggedness, superior to Si power diodes in a wide range of applications. However, when the target blocking voltage is increased to 4.5kV, the question arises if whether the conventional MPS structure can continue with its advantages, or if it will reach its limit and novel device structures should be applied?

Our simulation and modeling works were in progress in parallel with the fabrication work done by our cooperation partners. Measured data of the fabricated devices facilitate the calibration of the simulation setups and physical models for 4.5kV SiC MPS diodes. On the other hand, the physical insights obtained from extensive simulations allowed us to find out one of the issues causing unsatisfactory I-V characteristics measured on the fabricated SiC MPS samples is the nonideal Ohmic contact on the top of the p-doping regions. In the end, technical solutions are suggested.

Furthermore, our work contributes to gain a thorough physical understanding of the electrical conduction mechanisms inside 4.5kV SiC MPS diodes, focusing on the transition from the unipolar to the bipolar operation mode. Equipped with this knowledge, analytical compact models describing the impact of the geometrical and physical device parameters on the device characteristics have been formulated. The accuracy of the analytical models have been verified with reference to massive TCAD simulation results. The assumptions used in the analytical model and its limitation have been clarified.

The analytical model reveals that the high blocking voltage of 4.5kV makes the trade-off between nominal operation ($J_{F,nom}$) and surge current mode (V_{turn}) more aggressive. Due to their thick epitaxial layer, 4.5kV SiC MPS diodes with the conventional stripe-shape MPS structure have high epitaxial resistance, and the bipolar operation can be only be triggered with a high voltage V_{turn}. Based on the essential idea of minimizing the interaction between the Schottky functional part and the PiN functional part, we proposed novel device structures, such as the one with oxide interlayers or the one with electrical decoupling. They proved their advantages in the simulation results. On the other hand, considering a reduction in the epitaxial resistance in 4.5kV SiC MPS diode can benefit both the nominal operation and the surge current capability, a super-junction structure has been proposed and analyzed.

However, more research work lies still ahead in the future:

- Calibrate the analytical compact model with reference to the measured data from real devices.

  An extended analysis of the performance of the real-life devices under test is required. There are still a number of open questions, such as the short carrier lifetime in the implanted region, which should be taken into account in the analytical model.

- Extend the analytical compact model to other novel device structure.

The current analytical model is based on the conventional MPS structure. That is to say, the fitting parameters or physical assumptions and approximations are only available for the conventional MPS structure and should be renewed when considering other novel device structures. Furthermore, the extension of the current analytical model should be implemented individually for each of the other novel device structure variants. How many modifications of the current analytical mode should be done depends on the geometrical difference between the novel device structures and the conventional MPS structure, since the distribution of the electrical potential has a close connection with the geometry of the device structure.

- Fabricate and characterize the proposed novel device structures.

  Although all these designs show attractive promising I-V characteristics in the simulation, several challenges in the fabrication process must be mastered on the way of these devices to play a superior role in power applications. Taking the super-junction structure as an example, it is still an open question how to fabricate a deep p^--pillar into the n^--epitaxial layer. In contrast to Si, the hardness of SiC is even comparable to that of Diamond. Regardless of chemical etching or high energy implantation, only a shallow junction can be obtained.

The second scientific achievement presented in this work is the numerical analysis of the transient current flowing in SiC PiN diodes triggered by the impact of a cosmic particle, in comparison with the same event encountered in Si PiN diodes with the same blocking voltage. Due to the different thicknesses of the epitaxial layer, the ion-induced current has two different physical mechanisms in the aforementioned SiC PiN diodes and Si PiN diodes, leading to different dependence on the prebias reverse voltage, and consequently different failure mechanism. In another perspective, although the excellent material properties provided by SiC, the device design still plays an indispensable role in determining the robustness against cosmic radiation. Furthermore, our study reveals that in the case of a developing "streamer" inside the semiconductor devices, highly sophisticated simulation techniques, such as a careful adaptive gridding scheme, are required to obtain a fine spatial resolution.

Future research work may include:

- Investigate more general situations in the SiC devices exposed to cosmic radiation.

  The comparison reported in this work intentionally selected the SiC and Si PiN diodes with the same blocking voltage (1.5kV) and exposed to the same ion penetration length & electron/hole plasma deposition. Consequently, the SiC PiN diode has a very thin epitaxial layer. The high energetic ion originating from the initial nuclear spallation penetrates the whole epitaxial layer, resulting in a situation completely different from that in Si diodes. Hence, a further comparison should be made between Si and SiC diodes having the same thickness of the epitaxial layer, but much longer than the track of high energetic particles.

- Improve the numerical accuracy and, thus, the predictiveness of the transient simulations by employing a time-adaptive "moving" grid.

  The dynamic avalanche breakdown caused by the localized high electric field peaks requires a highly dense and fine discretization mesh at the boundary of the streamer shifting from the top to the bottom of the device. Therefore, the grid spacing around the streamer should follow its motion and be adapted after each time step to preserve the numerical accuracy required for high-fidelity simulation. However, such a "moving grid" algorithm is not yet implemented in the software platform used in this work and needs to be still developed.

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Glossary

D_j	Junction depth of the p^+ region.
E_c	Band edge of the conduction band.
E_g	Energy gap between conduction and valence band.
χ	Electron affinity.
E_F	Femi-energy level in the energy band diagram.
E_{crit}	Critical electric field for hte onset of impact ionization.
E_{Fn}	Fermi-energy level for n-type semiconductor.
E_{Fp}	Fermi-energy level for p-type semiconductor.
E_i	Intrinsic Energy level in the energy band diagram.
E_v	Band edge of the valence band.
ε_r	Electrical permittivity.
G_{cc}	Constant carrier generation.
$J_{F,nom}$	Current density in nominal operation mode.
J_n	Electric current density of electrons.
J_{surge}	Surge current density.
L_1	A length used to label the location of point N, see Fig.3.8.
L_2	A length used to label the location of point N', see Fig.3.7.
L_{epi}	Depth of the n^- epitaxial layer.
L_{p^+}	Depth of the p^+-implantation region.
λ	Thermal conductivity.
L_{de}	Extension of the depletion region.
μ_n	Electron mobility.
N	The location where the initial injection of holes takes place.
$N_A(p^-)$	Doping concentration in the p^- area.
$N_D(n^-)$	Doping concentration in the n^- area.
N_A^-	Concentration of ionized accptors.
N_D^+	Concentration of ionized donors.
n_i	Intrinsic carrier concentration.

Φ_m	Workfunction of the metal.
Φ_p	Workfunction of the p−type semiconductor.
ϕ_N	Electrical potential at point N.
ϕ_m	Electrical potential in the metal.
ϕ_{n^-}	Electrical potential in the n^- region.
$\Delta\phi_{p^+n^-}$	Electrical potential difference between p^+ and n^- region.
ϕ_{p^+}	Electrical potential in the p^+ region.
$\Delta\phi$	Electrical potential difference.
ϕ	Electrical potential inside the semiconductor.
ϕ_{BD}	Schottky barrier height of Schottky contact.
ϕ_{Fp}	Fermi potential for p-type semiconductor.
q	Positive elementary charge.
R_{ep1}	Resistance of the first part of the epitaxial layer.
R_{ep2}	Resistance of the second part of the epitaxial layer.
R_{ext}	External resistor.
R	Carrier recombination rate.
τ	Carrier lifetime.
ΔV	Voltage step attained after ramping up the voltage source (boundary condition).
$V_{applied}$	Applied electrical bias potential.
V	Electrical potential.
V_B	Breakdown/ blocking voltage of power devices.
V_{Sch}	Voltage drop on the Schottky contact.
$V_{bi_{Sc}}$	Built-in potential of the Schottky contact.
V_{bi}	Built-in potential of p^+n^- junction.
V_{ext}	External electrical potential.
V_{pn}	Voltage drop across p^+n^- junction.
V_{th}	The threshold voltage of the Schottky contact.
ϕ_{ohmic}	Electrical potential at the boundary of an Ohmic contact.
V_{surge}	Voltage of power devices to be sustained under surge current conditions.
$\phi_{schottky}$	Electrical potential at the boundary of Schottky contact.
V_{turn}	Voltage for triggering the bipolar operation mode.
W_g	Width of the gap between two neigboring Ohmic contacts.
W_o	Area of the Ohmic contact in the unit cell of a MPS diode.
W_s	Area of the Schottky contact in the unit cell of a MPS diode.