



Characterization of a novel DePFET based sensor for an ultra-fast Transmission Electron Microscopy application

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Abstract

Transmission electron microscopy was so-far missing out on the high-intensity real-time real-space imaging of ultra-fast dynamic processes due to technological barriers in the electron detection hardware. This, however, is about to change with the EDET DH80k camera system. The system will feature multiple state-of-the-art technologies in order to achieve an unprecedented 80 kHz full frame peak readout frequency of a 1 Mpixel array. The pixels are based on the advanced depleted p-channel field effect transistor (DePFET) technology that incorporates an extremely thin body of only 30 μm and an enormous dynamic range in combinations with signal compression. This results in the optimized point spread function, and in the optimized response function that provides a high amplification of small input signals and a low amplification of big input signals.

As the combination of all technologies is unprecedented, the foremost part of this work is based on the full understanding of operational parameters and of the behaviour of multiple prototype devices. This is achieved through quasi-static and dynamic characterization, as well as through comparison of measured results to the expected behaviour from simulation data. The quasi-static characterization yields fundamental DePFET parameters, such as threshold voltage and internal gate potential, and the dynamic characterization gives insights on the operation window, on the signal response function and on the interplay of signal charge collection efficiency and biasing conditions. It was concluded that the operation window is large enough to operate the devices meant for the final experiment and that their implemented design is in fact the best available at this point. Additionally, the optimal operation parameters were deduced in the scope of this work and they will serve as a starting point for optimization of the final camera system.

Energetic electrons cause radiation damage in silicon sensors. To quantify those damaging effects, the DePFET's radiation hardness was investigated. The EDET DH80k DePFET structures were intentionally damaged with 55 keV electrons up to the total ionizing dose of almost 1 Mrad. Based on the obtained results, the investigation of the influence of different transistor geometries on the long term operation was conducted in the form of a simulation study. The measured rates of radiation damage are worse than those anticipated from the preliminary studies but still sufficient for an extrapolated life expectancy of the EDET DH80k camera to a minimum of 5 Mrad of total ionizing dose. Two concepts to deal with those increased radiation damaged were proposed and will be implemented into the final camera system. Firstly, a laser annealing system which should prolong the life time of the camera and secondly, a calibration system for systematic pixel calibrations to better cope with changes arising from the increased radiation damage.

Zusammenfassung

Transmissionselektronenmikroskopie war bisher aufgrund technologischer Barrieren in der Detektionshardware nicht in der Lage, ultra-schnelle dynamische Prozesse mit hoher Intensität in Echtzeit räumlich abzubilden. Mit dem Kamerasystem EDET DH80k wird sich dies ändern. Das System kombiniert mehrere hochmoderne Technologien, um eine noch nie dagewesene Auslesefrequenz von 80 kHz für ein 1-MPixel-Array zu erreichen. Die Pixel basieren auf der fortschrittlichen DePFET-Technologie, die ein extrem dünnes Substrat von nur 30 μm und einen enormen Dynamikbereich in Kombination mit Signalkompression ermöglicht. Dies führt zu einer optimierten Punktspreizungsfunktion und zu einer optimierten Signalantwort, die eine hohe Verstärkung kleiner Eingangssignale und eine niedrige Verstärkung großer Eingangssignale ermöglicht.

Da die Kombination aller Technologien beispiellos ist, besteht der wichtigste Teil dieser Arbeit auf der Untersuchung der verschiedenen Betriebsparameter auf das Verhalten mehrerer Prototyp-Bauteile. Dies wird durch quasistatische und dynamische Charakterisierung sowie durch den Vergleich von Messergebnissen mit dem erwarteten Verhalten aus Simulationsdaten erreicht. Die quasistatische Charakterisierung liefert grundlegende DePFET-Parameter wie Schwellenspannung und internes Gate-Potenzial, und die dynamische Charakterisierung gibt Aufschluss über das Betriebsfenster, die Signalantwortfunktion und das Zusammenspiel von Ladungssammeleffizienz und angelegten Betriebsspannungen. Es wurde festgestellt, dass die verschiedenen Betriebsfenster groß genug sind, um die für das abschließende Experiment vorgesehenen Bauelemente zu betreiben. Außerdem wurde gezeigt, dass das für diese Bauelemente implementierte Design tatsächlich das Beste ist, das derzeit verfügbar ist. Des Weiteren wurden im Rahmen dieser Arbeit die optimalen Betriebsparameter abgeleitet, die als Ausgangspunkt für die Optimierung des endgültigen Kamerasystems dienen werden.

Energetische Elektronen verursachen Strahlungsschäden in Siliziumsensoren. Um diese schädlichen Effekte zu quantifizieren, wurde die Strahlungshärte des DePFETs untersucht. Die EDET DH80k DePFET-Strukturen wurden mit 55 keV Elektronen bis zu einer ionisierenden Gesamtdosis von fast 1 Mrad beschädigt. Auf der Grundlage der erzielten Ergebnisse wurde die Untersuchung des Einflusses verschiedener Transistorgeometrien auf den Langzeitbetrieb in Form einer Simulationsstudie durchgeführt. Die gemessenen Raten der Strahlungsschäden sind schlechter als die aus den Vorstudien erwarteten, aber immer noch ausreichend für eine extrapolierte Lebenserwartung der EDET DH80k Kamera bis zu einem Minimum von 5 Mrad ionisierender Gesamtdosis. Es wurden zwei Konzepte zur Bewältigung dieser erhöhten Strahlungsschäden vorgeschlagen, die in das endgültige Kamerasystem integriert werden sollen. Erstens ein System zum Lasertempern, das die Lebensdauer der Kamera verlängern soll, und zweitens ein

Zusammenfassung

Kalibrierungssystem für systematische Pixelkalibrierungen, um die durch die erhöhten Strahlenschäden entstehenden Veränderungen besser bewältigen zu können.

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Introduction

The first chapter of this work starts with a brief overview of light microscopy and its shortcomings. Afterwards, it continues with the essentials of physics behind imaging with electrons. Those essentials show the particle-wave duality and different ways through which the electrons interact with matter. After this point, the focus turns towards the transmission electron microscope and how it is used for imaging. This eventually leads to the actual state of the commercial electron detector market, and introduces a niche for the EDET DH80k project.

As the EDET DH80k electron sensor is a silicon semiconductor sensor, the second chapter provides essentials of silicon semiconductor physics. This is necessary in order to understand how the electron sensors work. The essentials cover the grounds from an intrinsic silicon crystal, to the pn-junction, and in the end to the metal-oxide-semiconductor field effect transistors.

The theoretical part is furthered in the third chapter with an in-depth look into the depleted p-channel field effect transistor (DePFET). This is an actual design that the EDET DH80k electron sensor is based on. The chapter explains how a general DePFET sensor is built and operated, how it measures the signals that passing radiation leaves in its volume, what are its limitation, how it gets damaged, and how an actual EDET DH80k DePFET based electron sensor looks like.

The fourth chapter presents all devices that were produced in the scope of the EDET DH80k project, and also used in the scope of this work.

The fifth chapter starts with an introduction to the measurement systems that were used for measurements in this work. Afterwards, all characterization measurements and results are presented. In addition, chapter five explains problems that were found during the operation of these novel sensors, and also offers the optimization of operating parameters.

As the electrons are an ionizing form of radiation, they do not leave their trace only where it is convenient, but also where it is not. Therefore, the sixth chapter focuses on the radiation damage that the DePFET based EDET DH80k electron sensors will face during their lifetime. Initially, the measurement system is presented, followed by the methods, results and extrapolations on the future performance.

The work is concluded in the chapters seven and eight. The former offers a summary of this work and the latter connects the main points that were discovered during this PhD work in a form of a conclusion.

1 Transmission Electron Microscopy

Through millions of years of evolution of life on Earth – nowadays a commonly accepted theory first postulated by Charles R. Darwin [1] – most of the advanced species developed multiple senses to interact with the surrounding world, e.g., sight, smell, hearing, taste, and touch. The better the senses, the better the chance for survival. This was valid until the cognitive revolution of Homo Sapiens [2], when we started to change on a much faster time scale and evolutionary advancements could not follow. In some tens of thousands of years we became the predominant species on Earth. People started

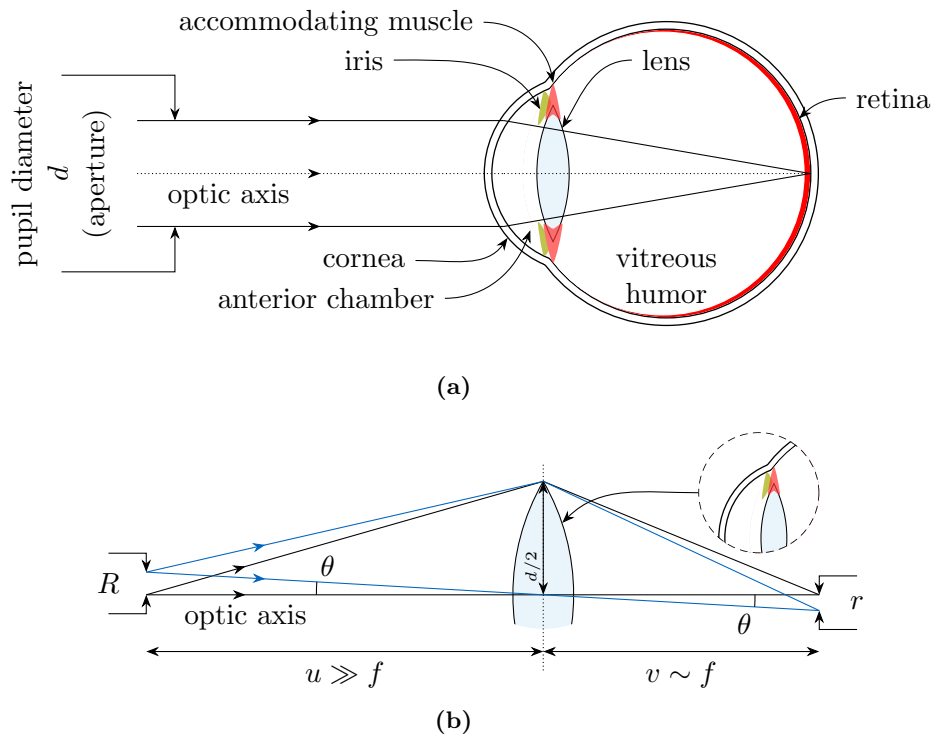


Figure 1.1: (a) A simplified illustration of the human eye, with some of the key components and multiple parallel light rays that are being focused to a single point on the retina. (b) Physicist's view of a close looking eye where all focusing components are replaced with a single thin lens. The object and its corresponding image are located respectively at positions u and v , and f is a focal point of the lens. Adapted from refs. [3, 4].

to gaze towards the stars in search of the biggest of objects, or look into the grains of sand. Both, however, stumbled upon the limits of an evolutionary human eye.

A brief overview of the working principle of the human eye (hereinafter referred to as the “eye”) will be presented in the next few paragraphs. The eye serves as an optical system that translates the information carried by a visible light to the electrical impulses which can be later interpreted by the human brain. Fig. 1.1a shows a simplified illustration of the eye. Different parts of the eye can be grouped together by the tasks that they are performing: intensity, focus, and detection.

Intensity regulating part Regulation of the intensity is needed due to the limited sensitivity and dynamic range in the detection part. To avoid under or overexposure the eye has a circular diaphragm of variable diameter called the iris. Its inner diameter controls the size of the pupil that acts as an aperture. The variability ranges from 1.5 mm to 8 mm [4]. There is, however, a side effect of this mechanism. When light travels through an aperture, diffraction patterns are formed in the detection plane [5]. For the discussion here, it is sufficient to know that a light source from one side of the circular aperture translates to a bright disk with evermore fading concentric rings around it. This pattern is usually called an Airy disk [6]. Minimal angular resolution of the two comparably bright light sources is given by the Rayleigh criterion [7] in the form of

$$\theta_{\text{dif}} \approx 1.22 \frac{\lambda}{d}, \quad (1.1)$$

where θ_{dif} represents the angular radius of the central Airy disk as seen from the centre of the circular aperture, λ the wavelength of light, and d the diameter of the circular aperture. The Rayleigh criterion sets the lowest limit on achievable resolution in most of the optical systems, and is called a diffraction limit. If θ from Fig. 1.1b is greater or equal to θ_{dif} , one is able to differentiate between the light sources, otherwise they are interpreted as one.

Focusing part In order to produce a clear image, the eye needs to focus the light onto the detection part. This is where the cornea and the crystalline lens come in effect. In a relaxed state the eye is focused for distant objects. However, it can change the focus through a process called accommodation. The maximum accommodation an eye can achieve changes with age, but on average it is around 25 cm [4]. In reality the focusing is never perfect, and the deviations from the perfect focusing are called aberrations. The two most known problems of lens systems are spherical and chromatic aberrations [5]. The former is when light rays are focused to different points, and the latter when some wavelengths are refracted more than the others.

Detection part The conversion from light to electrical impulses happens on the retina, which is comprised of millions of sensitive receptors called cones and rods. They have a diameter in the order of 2 μm to 6 μm [3], and therefore also contribute to image blurring.

A simplified resolution that the eye can achieve at a given distance can now be calculated. With a monochromatic 500 nm illumination through the pupil with 4 mm diameter, a diffraction limited angular resolution of $1.5 \cdot 10^{-4}$ rad (eq. 1.1) is obtained. This can be converted to the diffraction limited image resolution (r_{dif}) with

$$\tan(\theta_{\text{dif}}) \approx \theta_{\text{dif}} = r_{\text{dif}}/v, \quad (1.2)$$

where v is the position of image (Fig. 1.1b). Since the image is formed on the retina, it stands that $v \approx f \approx 20$ mm and $r_{\text{dif}} = 3 \mu\text{m}$. Aberrations of the focusing system (r_{abe}) contribute an equal amount to the image blurring as r_{dif} [3], and the finite sizes of receptor cells (r_{ret}) blur the image further for another $4 \mu\text{m}$ [3]. The final resolution of the image is then

$$r = (r_{\text{dif}}^2 + r_{\text{abe}}^2 + r_{\text{ret}}^2)^{1/2} \approx 6 \mu\text{m}. \quad (1.3)$$

As such, the smallest object (R) an unaided eye can resolve at a maximum accommodation ($u \sim 25$ cm) is on the level of $75 \mu\text{m}$. Consequently, magnification is needed to see the structures beyond the calculated limit.

The first recorded microscope-like devices were built in the early 17th century. The two names that pushed the field of light microscopy are Anton van Leeuwenhoek and Robert Hooke. While van Leeuwenhoek used a simple device with a single lens, Hooke employed a compound microscope much like the ones used today. Despite its inferior design, van Leeuwenhoek was able to achieve much higher magnifications due to his precise lens grinding and sample mounting skills, while spherical aberrations rendered Hooke's compound microscopes useless at higher magnifications. Van Leeuwenhoek managed to observe blood cells, bacteria, and structures within the cells of animal tissue, all unprecedented revelations at that time [3, 8]. As time passed, scientists managed to increase the magnification of light microscopes by

- increasing the number of more accurate lenses,
- correcting for always smaller aberration,
- using the immersion methods to collect more light, ...

Nevertheless, the fundamental diffraction limit remained. Eqs. 1.1 and 1.2 can be joined and rewritten for microscopes as

$$r_{\text{dif}} \approx 0.61 \frac{\lambda}{n \sin \alpha} = 0.61 \frac{\lambda}{\text{NA}}, \quad (1.4)$$

where n is the refractive index of the medium in front of the first microscope lens (objective lens), and α is the opening half-angle of the objective lens. Together, those two factors are usually called a numerical aperture (NA), and the best objectives on the market usually go up to the NA of 1.5 [4]. By the use of the shortest visible wavelength and the best NA, the resolution of optical microscopes is limited to the level of about 100 nm. However, a lot of the work was done on developing methods that improve the resolution of light microscopy for 1 to 2 orders of magnitude beyond the diffraction limit

1 Transmission Electron Microscopy

[9, 10]. But to improve it even further, radiation of shorter wavelength altogether needs to be employed.

In 1923 Louis de Broglie postulated a hypothesis that just like photons, all forms of matter are subject to the particle-wave duality [5]. He wrote it in the form of

$$\lambda = \frac{h}{p}, \quad (1.5)$$

where λ and p denote the de Broglie wavelength and momentum of the particle, and h is the Planck constant ($4.1357 \cdot 10^{-15}$ eV s [11]). The hypothesis was confirmed only 3 years later by C. J. Davisson and L. H. Germer in their experiment of diffraction measurements on electrons (e^-) scattered from single-crystal targets. Eq. 1.5 can be modified to have the kinetic energy dependence by the use of relativistic energy-momentum relation

$$E^2 = (pc)^2 + (m_0c^2)^2, \quad (1.6)$$

and energy conservation relation

$$E = E_{\text{kin}} + m_0c^2. \quad (1.7)$$

The E , E_{kin} and m_0 respectively denote the total energy, kinetic energy and rest mass of the particle, and c is the speed of light in vacuum ($2.998 \cdot 10^8$ m/s [11]). Kinetic energy for a charged particle with an elementary charge (e), that is accelerated over a potential difference (U), is calculated as

$$E_{\text{kin}} = -eU. \quad (1.8)$$

For an e^- with the rest mass of $511 \text{ keV}/c^2$ [11] and an elementary charge of $-1e$ [11], that is accelerated over a potential difference of 50 kV , a wavelength of 5.4 pm is

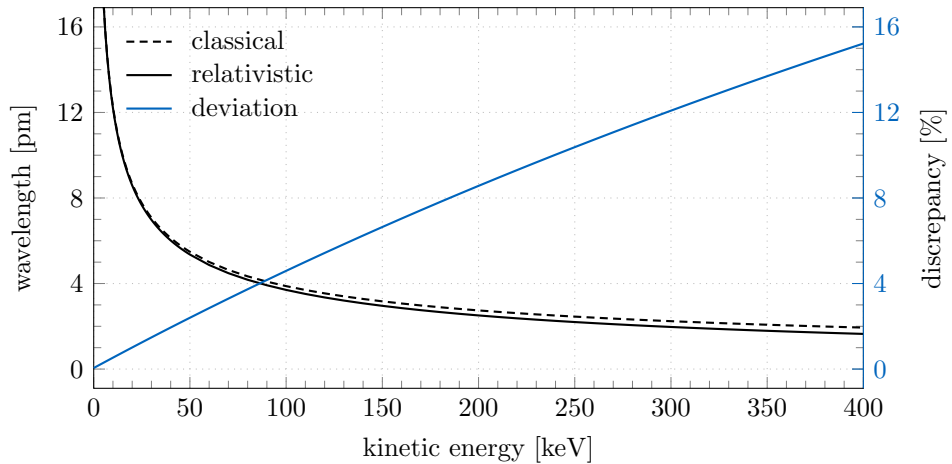


Figure 1.2: Electron wavelength as a function of its kinetic energy for relativistic (—) and classical (----) model on the left, and their discrepancy (—) on the right. Calculated from the equations presented in this section.

achieved. By omitting relativistic corrections and using the classical energy–momentum relation

$$p = \sqrt{2(-eU)m_0}, \quad (1.9)$$

an error of the order of a few percent would be introduced, and it would only increase with rising E_{kin} . This can be seen in Fig. 1.2, where a comparison of both models and their discrepancy is shown. Since the wavelength of e^- is significantly smaller than that of visible light (400 nm to 700 nm [5]), many scientists of the early 20th century accepted the challenge of creating the world’s first electron microscope (EM).

The first to succeed were two Germans, the physicist Ernst A. F. Ruska and the electrical engineer Max Knoll. They managed to achieve a magnification factor of 17.4 with an e^- beam in April of 1931 [14]. A fun fact in the history of e^- microscopy is that the two scientists invented the EM as a side product, while developing an efficient cathode-ray oscillograph, and having no clue about de Broglie’s (already confirmed) theory on particle-wave duality. To quote Ruska from his Nobel Prize Lecture in 1986 [14]:

Knoll and I simply hoped for extremely low dimensions for the electrons. As engineers we did not yet know about the thesis on the “material wave” by the French physicist de Broglie that had been put forward several years earlier (1925). Even physicists only reluctantly accepted this new thesis. When I first heard of it in summer 1931, I was very much disappointed that even for electron microscopy the resolution should be limited again by a wavelength (of the “Materiestrahlung”).

The initial success of e^- microscopy was hindered by unavoidable spherical and chromatic aberrations, arising from rotationally symmetric electro-magnetic lenses. The

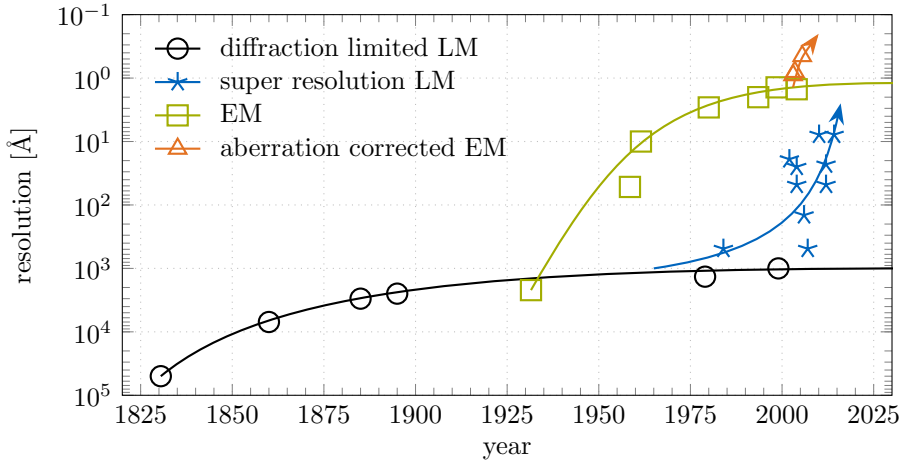


Figure 1.3: Resolution improvements through history for diffraction limited light microscopy (\ominus), super resolution light microscopy (\star), electron microscopy (\square), and aberration corrected electron microscopy (\triangle). Adapted from refs. [9, 12, 13].

limitation, known as Scherzer's theorem [15], sets an upper bound of the resolution to two orders of magnitude above the e^- wavelength. Recent advancements in technology, however, enable to largely suppress the aberrations by means of monochromators, imaging energy filters, and multi-pole corrector lenses [12, 13, 16, 17]. Therefore, a resolution of sub 0.5 \AA is achievable by state of the art EM. This can be seen in Fig. 1.3, which shows the improvements in resolution of light and e^- microscopy through history. So it is of no surprise that the e^- microscopy established itself as the go-to method over a variety of research fields when in need of high magnification factors, e.g., in biology, physics, and material sciences.

1.1 Interaction of electrons with matter

As e^- impinge upon matter (e.g., a specimen under investigation, a detector, a molecule of air) they can traverse it without any interactions, or be scattered by it. Either way, they always carry bits and parts of the information about the matter they just traversed. This section will present an overview of the signals, a group name for everything that is generated by an incident e^- beam, that can be seen in Fig. 1.4. Primarily, the focus will be on the elastic and inelastic scattering, as the former is a main source of contrast in transmission electron microscopy (TEM) images, whereas the latter is the origin of all other signals and the reason why e^- can be easily detected.

The derivations and explanations in the rest of this section follow refs. [17, 18, 19].

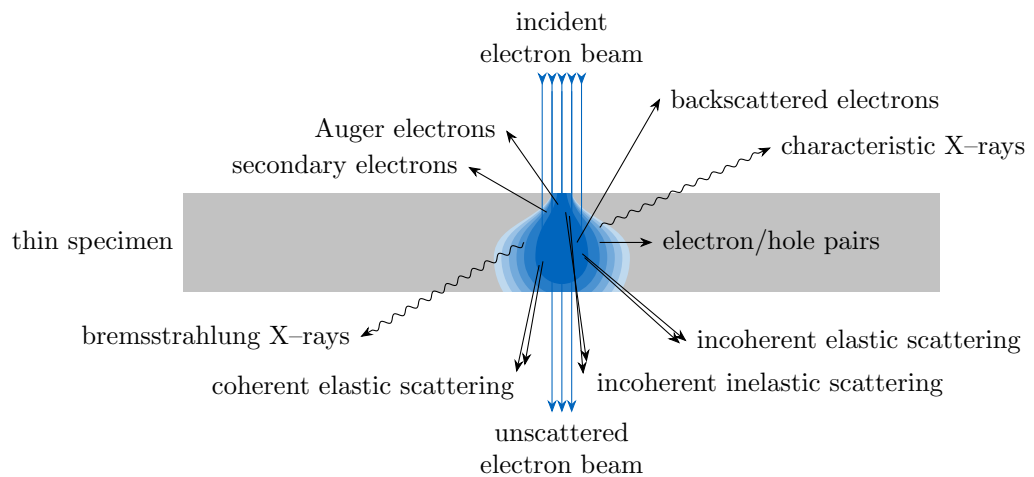


Figure 1.4: Signals generated through interaction of e^- with matter. Directions of signals represent in relative manner where they are the strongest. The blue colour inside the thin specimen represents an interaction volume. Adapted from ref. [17].

1.1.1 Elastic scattering

For the elastic scattering process it is usually assumed that the energy of an incident e^- remains unchanged. But with the calculation of a kinetic energy before and after the collision of an incident e^- with a stationary massive nucleus, obeying the energy and momentum conservation laws, a small transfer of the kinetic energy (ΔE) is possible

$$\Delta E = \frac{2E_{\text{kin}}(E_{\text{kin}} + 2m_0c^2)}{Mc^2} \sin^2(\theta/2). \quad (1.10)$$

M denotes the rest mass of a nucleus, and θ is an e^- scattering angle. Tab. 1.1 shows the calculated kinetic energy transfer for e^- with two different kinetic energies, in three materials, at four scattering angles.

Table 1.1: Kinetic energy transfers between an incident e^- with a kinetic energy E and three different types of nuclei, calculated for four different scattering angles θ (eq. 1.10). The atomic mass number (A) can be converted to the M by a multiplication with the unified atomic mass unit $u = 931.5 \text{ MeV}/c^2$ [11].

E	100 keV			1 MeV		
	Carbon ($A = 12$)	Copper ($A = 63.5$)	Gold ($A = 197$)	Carbon	Copper	Gold
θ						
0.5°	0.38 meV	0.07 meV	0.02 meV	7.00 meV	1.30 meV	0.42 meV
10°	152 meV	29 meV	9 meV	2.75 eV	0.52 eV	0.17 eV
90°	10 eV	1.9 eV	0.6 eV	181 eV	34 eV	11 eV
180°	20 eV	3.8 eV	1.2 eV	362 eV	68 eV	22 eV

For small scattering angles the ΔE is tiny, but with an increased energy and angle it raises to levels greater than the displacement energy (10 eV to 30 eV [19]). At those energies, an irreversible structural damage can be inflicted to the sample. Therefore, to minimize the problem an upper E_{kin} restriction for e^- in modern TEM to 400 keV seems reasonable. However, a few older MeV capable EMs are still in operation, mostly to study thicker inorganic specimen. For more insights, it is useful to have a look into the differential cross-section for elastic electron-nucleus scattering ($d\sigma_{\text{el}}/d\Omega$). Sadly, there is no analytical expression for an exact $d\sigma_{\text{el}}/d\Omega$, i.e., Mott differential cross-section, therefore, a Rutherford differential cross-section for elastic electron-nucleus scattering ($d\sigma_{\text{r}}/d\Omega$) will be used. The $d\sigma_{\text{r}}/d\Omega$ can be derived through classical mechanics by treating the e^- as a particle that is scattered by electric field of a nucleus. But this method fails to include the screening effect of atomic e^- on nuclear charge, therefore it is convenient to treat e^- as waves. Far from the nucleus, after scattering, the total scattered wave field (ψ_{sc}) is a superposition of the unscattered planar wave ($\psi(z)$) and the scattered spherical wave ($\psi(r, \theta)$)

$$\psi_{\text{sc}} = \psi(z) + \psi(r, \theta) = \psi_0 e^{2\pi i k z} + \psi_0 f(\theta) \frac{e^{2\pi i k r}}{r}, \quad (1.11)$$

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where ψ_0 is the amplitude of the unscattered wave, k its wave number, and $f(\theta)$ the scattering amplitude in dependence on the scattering angle θ . The $f(\theta)$ is in general defined as a complex quantity, to allow for phase shifts ($\eta(\theta)$)

$$f(\theta) = |f(\theta)|e^{-i\eta(\theta)}. \quad (1.12)$$

It can be shown that the differential cross-section is [19]

$$\frac{d\sigma}{d\theta} = |f(\theta)|^2. \quad (1.13)$$

Therefore, to calculate the analytical relativistic $d\sigma_r/d\Omega$ for a screened nucleus, one needs to solve the relativistic Schrödinger equation in the Born approximation for a Wentzel atom model which yields $f(\theta)$ as a real quantity. This means that $\eta(\theta)$ is zero and there is no phase shift, limiting the model to low atomic number (Z) materials. $d\sigma_r/d\Omega$ is therefore [18]

$$\frac{d\sigma_r}{d\Omega} = \left(\frac{Ze^2}{8\pi\epsilon_0}\right)^2 \left(\frac{m_0c^2 + E_{\text{kin}}}{E_{\text{kin}}(2m_0c^2 + E_{\text{kin}})}\right)^2 \left[\frac{1}{\sin^2(\theta/2) + \sin^2(\theta_0/2)}\right]^2, \quad (1.14)$$

where all quantities apart from the vacuum permittivity constant (ϵ_0) and characteristic angle θ_0 have been previously defined. θ_0 is introduced as

$$\sin(\theta_0/2) \simeq \theta_0/2 = \lambda/4\pi R \quad \text{with} \quad R = a_{\text{H}}Z^{-1/3}, \quad (1.15)$$

with $a_{\text{H}} = h^2\epsilon_0/\pi m_0e^2 = 0.0569 \text{ nm}$ being the Bohr radius. If one were to neglect screening, θ_0 would go to zero and a classical large angle $d\sigma_r/d\Omega$ with a singularity at $\theta = 0^\circ$ would be obtained.

A graphical representation of the small-angle $d\sigma_r/d\Omega$ (eq. 1.14) for three different energies of incident e^- being scattered on two kinds of nuclei is shown in Fig. 1.5. Whereas Fig. 1.6 shows the difference between the classical and screened $d\sigma_r/d\Omega$, and the comparison to Mott differential cross-section. From this comparison it is clear that the $d\sigma_r/d\Omega$ can be used to describe elastic scattering in biological samples, usually comprised from low- Z atoms, but more complex methods have to be used for material sciences where one can stumble upon higher- Z materials. Both figures show that the elastic scattering is mainly oriented in the forward direction, meaning that the high scattering angles which cause structural damage (Tab. 1.1) play a minor role. By interpreting the figures and eq. 1.14, it is apparent that the e^- beam will widen by increasing the Z or decreasing the E_{kin} . As elastically scattered e^- contribute the most to the image contrast in TEM, one can control the quality of images by knowing which beam parameters to set.

In general, scattering also decreases the coherence of the e^- beam through $\eta(\theta)$. To understand this, one needs to use complex methods to calculate $d\sigma_{\text{el}}/d\Omega$, multiple of them are described in refs. [18, 19, 20]. However, for the scope of this thesis it is sufficient to know that the low angle ($<3^\circ$) elastic scattering is coherent, whereas at high angles it becomes incoherent. It will later be shown (sec. 1.2) that both can be used to obtain the image of the sample.

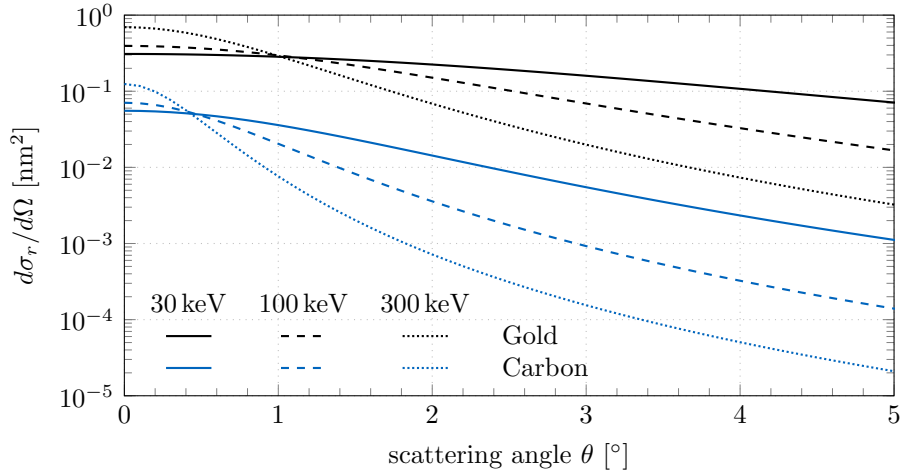


Figure 1.5: A screened relativistic $d\sigma_r/d\Omega$ for three different incident e^- energies on two types of nuclei. Calculated by eq. 1.14.

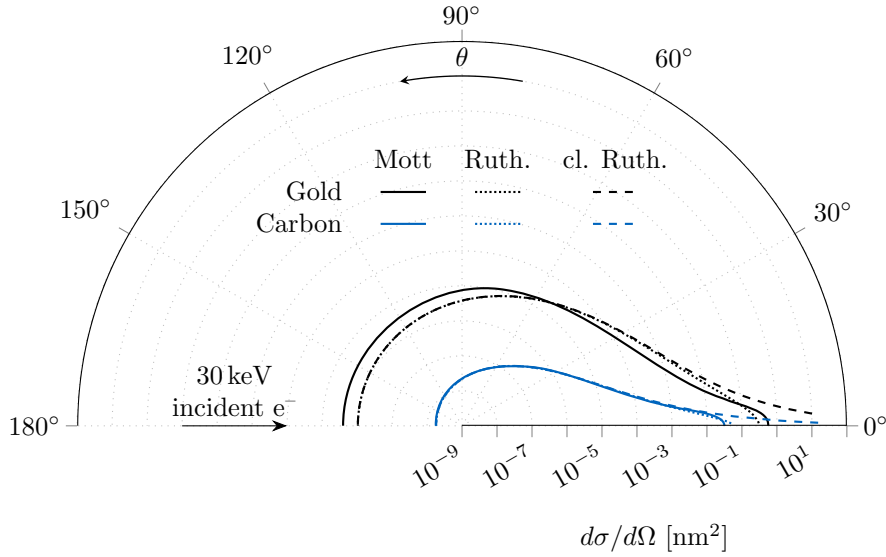


Figure 1.6: Comparison of the elastic differential cross-sections derived by Mott (solid lines) [18] and Rutherford (screened in dotted lines and classical in dashed lines; eq. 1.14) for 30 keV e^- in two different materials.

1.1.2 Inelastic scattering

The term inelastic scattering is generally used when an incident e^- interacts with the specimen and deposits a part of its kinetic energy. Consequently, its wavelength changes. The amount of energy lost in a single inelastic collision depends on the type of interaction. It can range from meV to eV by excitation of oscillations [19], up to

$0.5 \cdot E_{\text{kin}}$ for interactions with atomic e^- [18], or even to a complete E_{kin} in the case of a deceleration in the Coulomb field of an atomic nucleus (Bremsstrahlung) [17, 21, 22]. The energy loss of e^- in matter will be described in sec. 1.1.3, whereas this section will focus on the interactions and the angular distribution of inelastically scattered e^- .

The total differential cross-section for inelastic scattering ($d\sigma_{\text{in}}/d\Omega$) can be approximated by [19]

$$\frac{d\sigma_{\text{in}}}{d\Omega} = \left(\frac{e^2}{2\pi\epsilon_0} \right)^2 \left(\frac{m_0c^2 + E_{\text{kin}}}{E_{\text{kin}}(2m_0c^2 + E_{\text{kin}})} \right)^2 Z \frac{1 - [1 + (\theta^2 + \theta_E^2)/\theta_0^2]^{-2}}{(\theta^2 + \theta_E^2)^2}, \quad (1.16)$$

where θ_E denotes the characteristic angle responsible for the decrease of inelastic scattering, and is equal to $J/4E_{\text{kin}}$ with J being the mean ionization energy of the atom ($\simeq 13.5 \text{ eV} \cdot Z$). As θ_E is 1 to 2 orders of magnitude smaller than θ_0 , the $d\sigma_{\text{in}}/d\Omega$ is much more concentrated in smaller angles compared to $d\sigma_{\text{el}}/d\Omega$ (Fig. 1.7). The two limiting cases of eq. 1.16 yield

$$\frac{d\sigma_{\text{in}}}{d\Omega} > \frac{d\sigma_{\text{el}}}{d\Omega} \quad \text{for small } \theta, \text{ and}$$

$$\frac{d\sigma_{\text{in}}}{d\Omega} = \frac{1}{Z} \frac{d\sigma_{\text{el}}}{d\Omega} \quad \text{for } \theta \gg \theta_0 \gg \theta_E.$$

Inelastic scattering has a few unwanted properties for TEM. Because of the energy loss, inelastically scattered e^- are always incoherent, give rise to chromatic aberrations, and cause radiation damage in the sample. Due to their concentration in small scattering angles they contribute to the image noise in TEM. To decrease their contribution energy filters, such as MANDOLINE filter, can be employed to filter the e^- contributing to

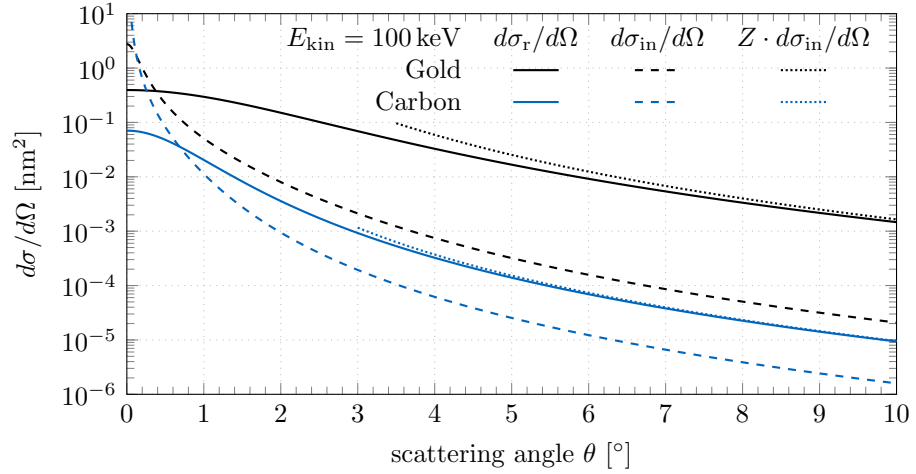


Figure 1.7: Comparison of the $d\sigma_{\text{el}}/d\Omega$ (solid lines, eq. 1.14) and the $d\sigma_{\text{in}}/d\Omega$ (dashed lines, eq. 1.16) for 100 keV incident e^- in two different materials, with an additional high angle limit for the $d\sigma_{\text{in}}/d\Omega$ (dotted lines).

the image [19, 23]. On the other hand, they can be used to characterize the sample by various e^- energy-loss spectrometry methods.

1.1.2.1 Secondary signals

Inelastic scattering gives rise to secondary signals through which the sample can be characterised (e.g., secondary e^- , Auger e^- , characteristic X-rays, bremsstrahlung X-rays), or the incident e^- can be easily detected in semiconductor detectors (e.g., electron/hole pairs (e^-/h^+ pairs)). All secondary signals are shown in Fig. 1.4, and are further explained in Fig. 1.8. However, secondary signals are not used in the typical TEM imaging, but are used in their own versions like scanning electron microscopy or analytical electron microscopy. Even so, it is useful to understand the physics of those signals, as they are generally used for the characterization of sensors.

A free e^- with sufficient kinetic energy can ionize an atom by ejecting one of its shell e^- (Fig. 1.8a) or excite it by pushing one of its shell e^- to a higher atomic shell. In this process, the free e^- loses a part of its energy and the shell e^- gains it. Both of them continue the process of losing kinetic energy, until they are eventually thermalized. An atom, however, is left in an excited energy state with a vacancy in one of its atomic shells. As the described atom state is not stable, it will eventually relax by filling the vacancy with one of its higher shell e^- and emitting an excess energy by emission

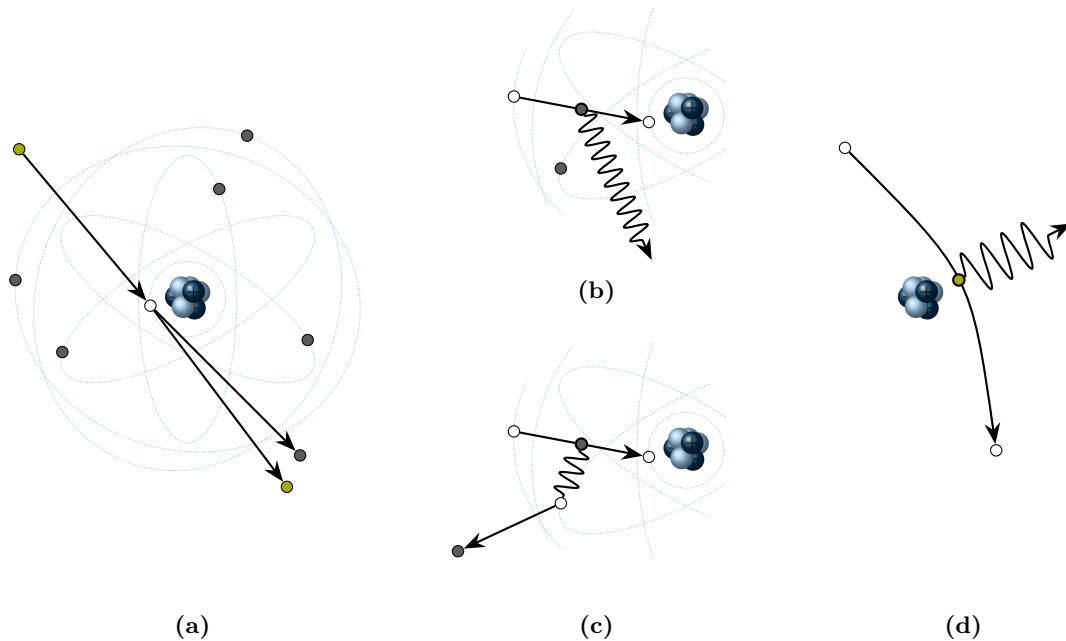


Figure 1.8: A collection of processes that give rise to secondary signals which can be used to characterize the sample: (a) ionization of an atom; (b) relaxation by emission of a characteristic X-ray radiation; (c) Auger e^- emission; (d) bremsstrahlung X-ray production.

of an X-ray radiation (Fig. 1.8b) [24]. The X-ray radiation produced in this way is a characteristic radiation as it is of an exactly specified energy, that is the difference between the atomic shell energies. The timing of this process, predicted with quantum mechanical perturbation theory [25], depends on the atomic shell and can range between μs and ns [26] for outer atomic shells, and all the way to sub-fs for inner atomic shells [27]. A general name for the described process of producing the X-rays is particle induced X-ray emission. The following paragraph will explain the nomenclature used to denote the characteristic X-rays.

In the atom there can be only one e^- for each energy state that is characterised by four quantum numbers (QNs) [5]:

- Principal QN (n) – represents the atomic shell and is marked with positive integer numbers starting with 1. Can also be denoted with capital letters starting from the letter K.
- Orbital QN (l) – represents the atomic sub-shell and is marked with a non-negative integer numbers up to the $n - 1$. Can also be denoted with letters (s, p, d, f, ...) due to historical reasons.
- Magnetic QN (m_l) – represents the splitting of energy levels under the influence of magnetic field, and is marked with integer numbers between $-l$ and l .
- Spin QN (m_s) – represents the e^- spin states ($\pm 1/2$).

In addition to that, the l and m_s QNs together form the total angular momentum QN (j) as $|l \pm m_s|$. The conventional naming of atomic shells consists of the integer n , letter l and a subscript j as shown on the right side in Fig. 1.9a. The so-called selection rules [5] must be obeyed in e^- transitions between the atomic shells and therefore each element comes with its own characteristic X-ray spectrum. A subset of all allowed transitions up to the principal QN of 4 is shown in Fig. 1.9a. The naming convention still commonly used, albeit being inconsistent (as shown in Fig. 1.9a), is the Siegbahns naming [28]. It comprises of a capital letter denoting the principal QN that marks the end atomic shell of the transitioning shell e^- , and a Greek letter with an additional numeric index. The former tells how many atomic shells higher than the end atomic shell did the transitioning shell e^- originate from, with α denoting 1 and increasing alphabetically, and the latter indicates the atomic sub-shell. The $K\alpha_1$ name denotes the characteristic X-ray where the vacancy in the K shell was filled with an e^- from the L shell or specifically from the $2p_{3/2}$ sub-shell.

Excited or ionized atoms relax to the lower energetic state through emission of radiation. However, experiments showed (Fig. 1.9b) that the probability of a characteristic X-ray emission is very low in low- Z materials. Consequently, the emitted energy is not always carried away by characteristic X-rays. The emitted radiation can be reabsorbed by another shell e^- of the same atom, and the relaxation process starts anew. An e^- that gains enough energy to escape the atom through characteristic X-ray absorption is usually referred to as an Auger e^- [30, 31] (Fig. 1.8c).

A completely separate mechanism by which a free energetic e^- can lose its energy is the production of bremsstrahlung X-rays [21, 22]. In this case, the e^- is decelerated in a

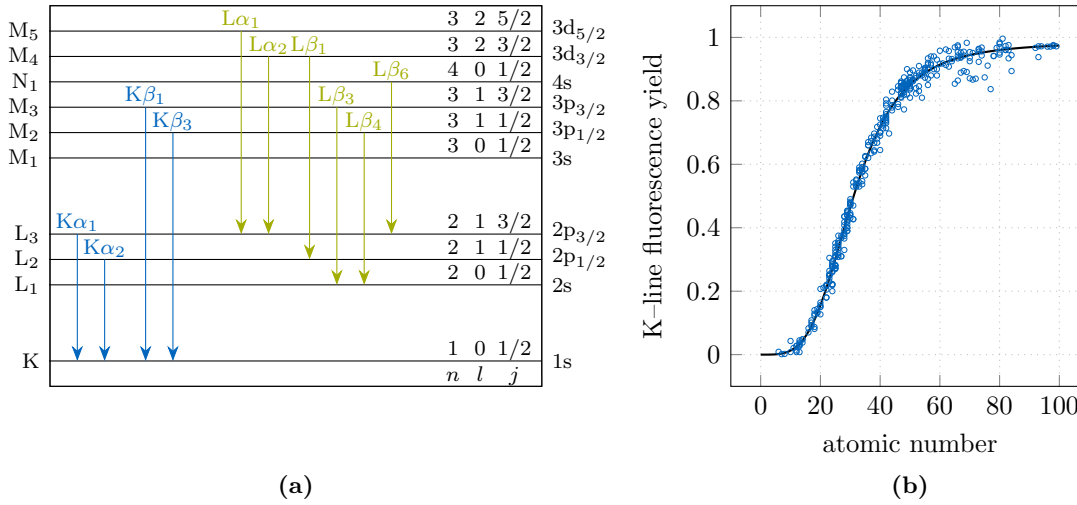


Figure 1.9: (a) A subset of allowed shell e^- transitions that generate the characteristic X-rays in Siegbahn naming convention. The y-axis represents the atomic shells in fine structure (left) and atomic (right) notation. In addition, QNs n, l and j are shown as well on the right side. (b) Distribution of the experimental K-shell fluorescence yield as a function of the atomic number. Adapted from ref. [29]

Coulomb field of an atomic nucleus or shell e^- , and it emits the energy in a form of X-ray radiation (Fig. 1.8d). However, X-rays produced in this way are not of characteristic energies, but can range from almost zero up to the complete energy of the initial e^- .

Absorption of X-ray radiation The X-rays do not play an important role in classical TEM imaging. However, the mono-energetic property of characteristic X-rays is very useful for the energy calibration of radiation detectors. Characteristic X-ray energies span from some 10 eV in light elements, and to around 100 keV for heavy elements [32]. Additionally, they also occur naturally in radioactive decays.

In general, the absorption of X-ray photons follows the so-called Beer-Lamberts law [33]

$$I(z) = I_0 e^{-(\mu/\rho)z}, \quad (1.17)$$

where $I(z)$ and I_0 are the current and initial intensity, z is the depth, and μ/ρ is the so-called mass attenuation coefficient of the material that can be found tabulated for many materials and compounds in ref. [34]. As the e^- sensors for TEM are usually thin, only the energies of up to few 10 keV are useful. Beyond those energies the sensor material quickly becomes transparent for X-rays. Fig. 1.10 shows the cross-section for interactions between photons and e^- in silicon for four major contributions. In the useful energy range the most probable effect is the photoelectric effect. The photoelectric effect is very similar to the process described in Fig. 1.8a, with the difference that an energetic photon is causing the ionization or excitation. The minimum energy needed for the

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emission of the shell e^- is the binding energy E_{bin} , whereas the excess energy is imparted to the e^- as the kinetic energy

$$E_{\text{kin}} = E_{\text{photon}} - E_{\text{bin}} = h\nu - E_{\text{bin}} . \quad (1.18)$$

The h represents the Planck constant and ν the photons' frequency. The ejected, now free, e^- behaves in the matter just like the e^- described before.

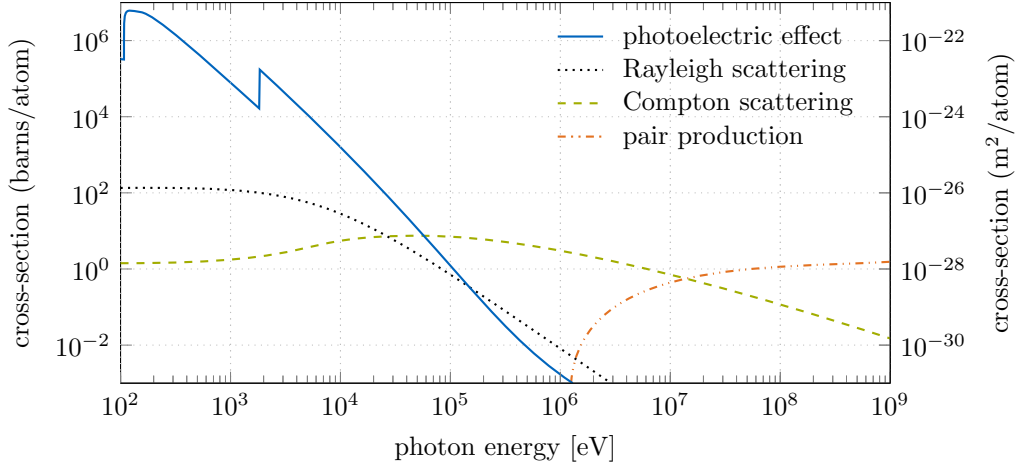


Figure 1.10: Cross-section for interactions between photons and e^- in silicon. Adapted from ref. [35].

1.1.3 Energy loss of electrons

The e^- , upon traversing matter, interact elastically and inelastically. The former type of interaction contributes mainly to big angle deviations, whereas the latter is almost solely responsible for the loss of kinetic energy. Even though the complete kinetic energy can be lost in a single inelastic interaction, the majority of interactions occur with only a tiny part of energy being transferred. However, the amount of interactions per unit path length can be so large that substantial changes in kinetic energy can occur in relatively thin samples. A good measure for the amount of interactions is the mean-free-path length (x_t) defined as

$$\frac{1}{x_t} = \frac{\rho N_A}{A} \sigma_t = \frac{\rho N_A}{A} 2\pi \int_0^\pi \left(\frac{d\sigma_{\text{el}}}{d\Omega} + \frac{d\sigma_{\text{in}}}{d\Omega} \right) \sin \theta d\theta , \quad (1.19)$$

where N_A and ρ are, respectively, Avogadro's number [11] and specimen density, and σ_t is the total cross-section. For e^- with kinetic energy of 100 keV in organic materials ($\rho \sim 1 \text{ g/cm}^3$) an x_t of 120 nm is calculated, whereas for evaporated nickel and iron films the same is achieved in only ~ 12 nm [19]. Because the x_t is tiny, the usual approach to energy loss is via the average energy loss per unit path ($\langle -dE/dx \rangle$), as the fluctuations are small due to many interactions. The $\langle -dE/dx \rangle$ for heavier particles was first derived

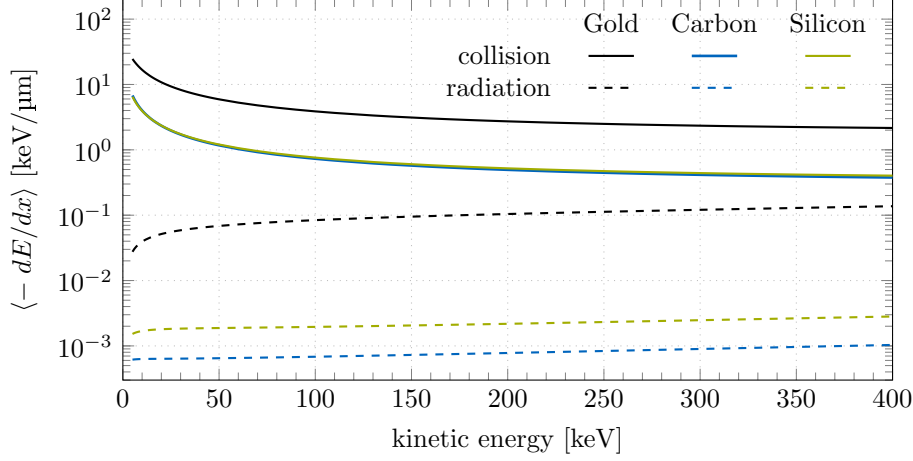


Figure 1.11: Collision and radiation contributions to the $\langle -dE/dx \rangle$ for three different elements at typical TEM energies. Data obtained from an online NIST ESTAR calculator [39].

by Bethe [36, 37] and later rewritten for e^- as the Møller cross-section [38]. In general it can be written as

$$\langle -\frac{dE}{dx} \rangle = \langle -\frac{dE}{dx} \rangle_c + \langle -\frac{dE}{dx} \rangle_r, \quad (1.20)$$

where indices c and r respectively represent collision and radiative (bremsstrahlung) losses. Fig. 1.11 shows both contributions to the $\langle -dE/dx \rangle$ for three different elements at typical TEM energies. The radiative losses are more than an order of magnitude smaller, and can henceforth be (for the purposes of this thesis) ignored. Physical dependencies of collision losses can be seen from the Bethe equation for e^- [11]

$$\langle -\frac{dE}{dx} \rangle_c = \frac{1}{2} K \rho \frac{Z}{A} \frac{1}{\beta^2} \left[\ln \frac{m_0 c^2 \beta^2 \gamma^2 E_{\text{kin}}}{2I^2} + (1 - \beta^2) - \frac{2\gamma - 1}{\gamma^2} \ln 2 + \frac{1}{8} \left(\frac{\gamma - 1}{\gamma} \right)^2 - \delta \right], \quad (1.21)$$

where

- K is the $4\pi N_A r_e^2 m_0 c^2$ coefficient,
- r_e is the classical electron radius of $e^2/(4\pi\epsilon_0 m_0 c^2)$ [11],
- γ is the Lorentz factor of $1 + E_{\text{kin}}/m_0 c^2$,
- β is the speed of an e^- divided by c or $(1 - 1/\gamma^2)^{1/2}$,
- I is the mean excitation energy [39, 40], and
- δ is the density correction factor, that becomes important at energies well beyond TEM.

The e^- with higher kinetic energy lose less energy per unit path. Therefore, it is beneficial to keep the energy high, but below the level where one would start seeing a lot of atom displacement damage.

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If a number of e^- with E_{kin} were sent through the specimen, an energy loss distribution ($f(t, \Delta)$) would be measured on the other side. The $f(t, \Delta)$ is a function of the specimen thickness (t) and of the energy imparted to the specimen (Δ). In case of e^- with E_{kin} large enough to penetrate the sample with only small losses, the shape of this distribution depends heavily on t . Two limits that can be looked at, with the region of application parametrized as

$$\kappa = \Delta_{\text{m}}/W_{\text{max}} = \Delta_{\text{m}}/(E_{\text{kin}}/2) , \quad (1.22)$$

are thick ($\kappa > 10$) and thin ($\kappa < 0.01$) specimen. The κ represents the ratio between the mean energy loss in specimen (Δ_{m}) and the maximum energy transfer allowed in a single collision (W_{max}) [33]. For a thick specimen a Gaussian shaped distribution would be measured with the centre at Δ_{m} and the standard deviation σ

$$f_{\text{thick}}(t, \Delta) \propto \exp\left(-\frac{(\Delta - \Delta_{\text{m}})^2}{2\sigma^2}\right) , \quad (1.23)$$

following from the central limit theorem. With the thin specimen the central limit theorem cannot be applied, and the measured distribution would have a skewed, asymmetric form with a long tail as a consequence of a probability of high energy transfers in single collision. The theory for thin specimen was first developed by Landau [41], and the distribution for it is given as [33]

$$f_{\text{thin}}(t, \Delta) = \frac{1}{\xi(t)} \frac{1}{\pi} \int_0^\infty e^{-u \ln u - u\lambda(\Delta)} \sin(\pi u) du , \quad (1.24)$$

where $\xi(t)$ is derived from the Rutherford cross-section and is equal to the pre-bracket term of eq. 1.21 multiplied by t , and

$$\lambda(\Delta) = \frac{1}{\xi(t)} \left[\Delta - \xi(t) (\ln \xi(t) - \ln \varepsilon + 1 - C) \right] , \quad (1.25)$$

where C is the Euler constant, and

$$\ln \varepsilon = \ln \frac{(1 - \beta^2)I^2}{2m_0c^2\beta^2} + \beta^2 . \quad (1.26)$$

This distribution, in contrast to the Gaussian, is characterized by the most probable energy loss in the specimen (Δ_{mp}) as [33, 42]

$$\Delta_{\text{mp}} = \xi(t) [\ln \xi(t) - \ln \varepsilon + 0.2] , \quad (1.27)$$

which can be seen in Fig. 1.12.

Energy loss distributions for intermediate ranges were developed by Vavilov and Symon, and are not included in the scope of this work. The calculations can be found in refs. [43, 42].

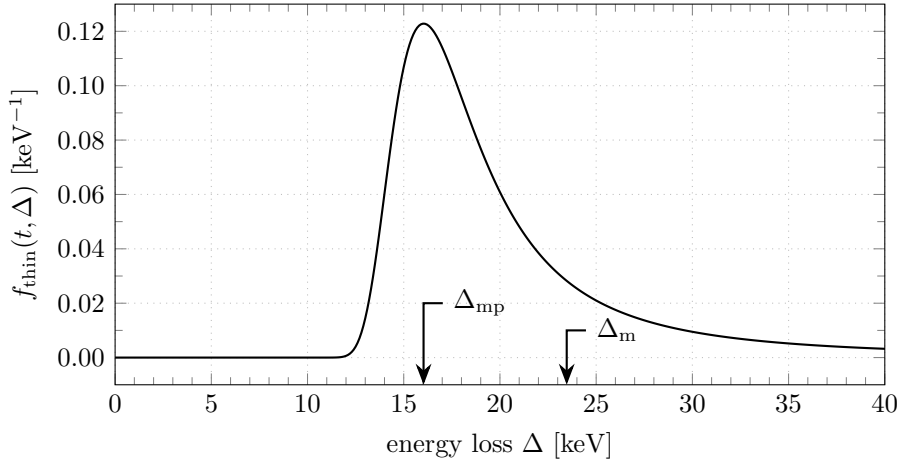


Figure 1.12: Landau distribution of a 300 keV incident e^- after passing through 50 μm of silicon. The distribution is normalized so that the $\int_0^{150} f_{\text{thin}}(t, \Delta) = 1$ and is plotted by the *pylandau* Python3 package which implements numerical solutions to the above equations as described in ref. [44].

1.2 Image formation by mass-thickness contrast

Image contrast is defined as the difference in intensity between two neighbouring areas. However, the image contrast originates from the specimen's mass-thickness contrast, the source of which is an incoherent elastic scattering. The amount of scattering interactions between a monochromatic incident e^- beam and a specimen (sec. 1.1) is a function of specimen's atomic number (Z), density (ρ) and thickness (t). The former two are influencing a mean-free-path (eq. 1.19) parameter and the latter one the amount of interactions. Any variation in those parameters will cause a change in the contrast. At a constant t , parts of the specimen with higher Z will scatter more e^- than the parts with lower Z . The same is true for a thicker versus thinner part of the fixed Z specimen.

Two different imaging modes use the mass-thickness contrast method: bright field and dark field. They can be selectively chosen via different positions of the object aperture (OA). In the bright field mode (Fig. 1.13), OA is positioned on the central axis. Therefore, it allows the unscattered e^- beam to pass, as well as a part of scattered e^- that are scattered at angles lower than the limit set by the OA. Consequently, the image of the specimen is dark on the bright, high intensity background. The lack of incoherent elastic scattering, i.e., lack of e^- scattered at high angles, is the main source of image contrast in this mode. The e^- from the coherent elastic scattering and inelastic scattering, that manage to pass through the OA, are the main sources of image noise. The darker (low intensity) spots appear on the places where more scattering occurred. In the dark field mode the story is reversed. Now the OA is positioned off axis, allowing only e^- scattered in the specific range of angles to pass. The image of the specimen is bright on the dark background. Brighter parts are therefore from the places where more scattering at higher angles occurred. More about this mode can be found in ref. [45].

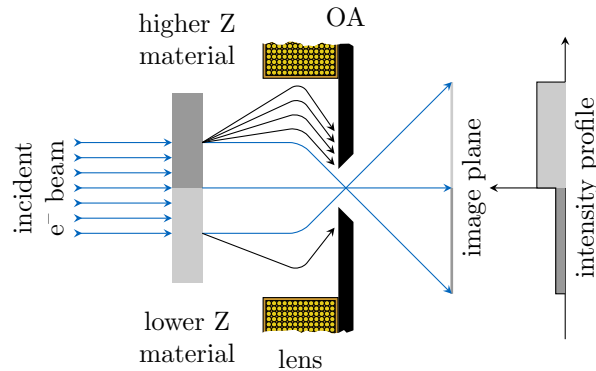


Figure 1.13: Bright field imaging of a specimen consisting of two different parts. In a part of higher Z material more scattering occurs and as consequence it appears of lower intensity in the picture. Vice versa is true for a part with lower Z material. Adapted from ref. [17].

1.3 Building blocks of a transmission electron microscope

Transmission electron microscope (tEM) as a machine did not change much since its invention in 1931. To build one, a 1 m to 2 m long vacuum vessel, an e^- source, a series of electromagnetic lenses and apertures, a specimen holder, and a viewing screen or a camera are needed (Fig. 1.14). However, for every one of the named components, there is a multitude of options, each with its own characteristic that impacts the overall performance of the machine.

To start at the top, an e^- source controls the intensity, spatial coherence and temporal coherence of the generated e^- beam. Currently there are two widely accessible types of e^- sources that work either on the thermionic or the field emission principles. With the former, the material, such as a v-shaped tungsten filament, is heated to temperatures at which e^- can gather enough kinetic energy to overcome the material work function and be emitted into vacuum. The latter principle is based on the lowering of the material work function by increasing the electric field at the surface. This is possible by shaping the tungsten filament in a needle with a tip radius of less than $0.1 \mu\text{m}$, so that the applied potential difference can generate electric fields greater than 10^9Vm^{-1} . At this point, the work function is reduced so much that e^- can be emitted into the vacuum via a quantum-mechanical tunnelling effect at room temperatures. After the emission, e^- are accelerated to kinetic energies up to 400 keV, and shaped by the series of electromagnetic lenses and apertures.

From the design of the electromagnetic lens [3, 14, 19, 48, 49] (hereinafter referred to as the “lens”) and electro-dynamics it is apparent that the focusing power of a lens can be varied. Therefore, it is of no surprise that modern tEMs can vary the magnification factor, typically between 50 and 10^6 . As the e^- are a form of ionizing radiation (sec. 1.1) it is beneficial to irradiate only the fraction of a specimen that will in the end appear on the image. With the final image (Fig. 1.14, full orange arrow) being limited by

1.3 Building blocks of a transmission electron microscope

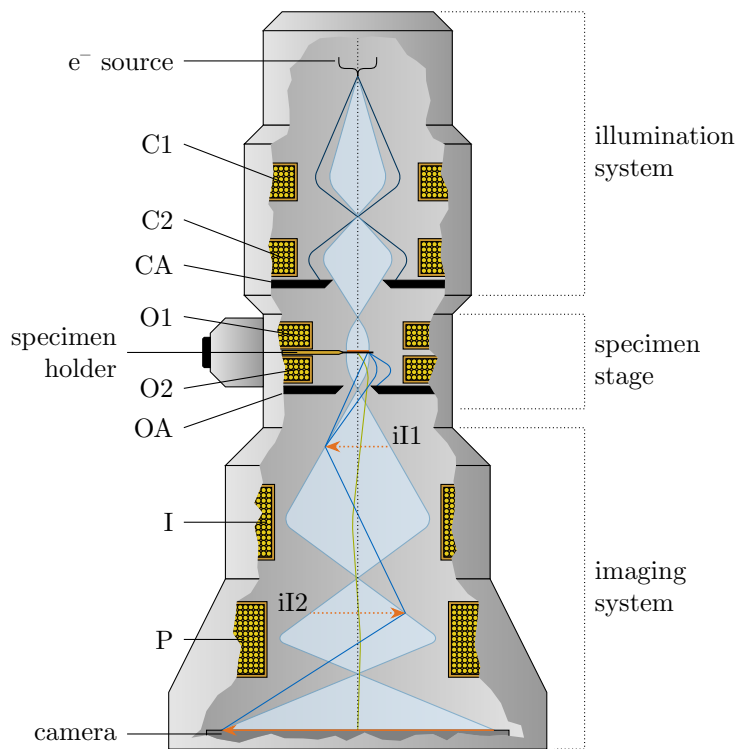


Figure 1.14: Schematic of a tEM. The beam (blue colour), which is coming down from an e^- source at the top, is shaped by the series of lenses (C1, C2, O1) before passing through a specimen (orange colour) in the specimen holder and being magnified by another series of lenses (O2, I, P). The aperture CA controls the beam diameter, whereas the OA is used for the removal of scattered e^- (blue and green lines) from the image (orange arrow). Dotted orange arrows denote intermediate images (iI1, iI2). Adapted after refs. [46, 47]

the camera size (e.g., 5 cm), the irradiation spot has to be adjustable between 50 nm and 50 μm . Consequently, the tEM needs to be equipped with lenses already before the specimen. Modern tEMs are equipped with at least two condenser lenses (C1, C2) and a condenser aperture (CA) to control the size and intensity of an incident e^- beam at the specimen, via the demagnification of the e^- source image and limitation of the convergence semi-angle of radiation. After this, the e^- beam leaves what is usually called an illumination system and enters the specimen stage. This stage is comprised of an objective twin lens (O1, O2), an objective aperture (OA) and a specimen holder. The upper lens gives more control over the beam before the specimen, whereas the lower one produces a magnified (factor of 20 to 50) intermediate real image (iI1) of a sample [19, 46]. The OA is used to reduce the amount of scattered e^- that contribute to the contrast in the final image, by limiting the maximum allowed scattering angle. To further magnify the iI1, more lenses are needed. Usually a series of intermediate lenses (denoted

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together in Fig. 1.14 with I) and a last projector lens (P) are used to increase the i11 in multiple steps, to the size of the camera at the bottom.

However, a tEM built in the above configuration would be far from the quality of the modern tEMs. This is because they additionally include

- a monochromator, to further reduce an energy spread of e^- at the source,
- astigmatism correctors, to correct for asymmetries in lenses,
- spherical correctors, to correct for imperfect focusing as described by Scherzer's theorem [15], and
- an imaging energy filter, to remove e^- that lost a part of their energy in a specimen through inelastic interactions.

An overview of these important improvements can be found in ref. [50].

1.3.1 Specimen

The design of a modern transmission electron microscope (tEM) allows for imaging of specimen ranging in dimensions over a few orders of magnitude, i.e., one can image a whole cell [53, 54], or atoms in crystalline structures [55, 56]. However, there is a prerequisite that the specimen is sufficiently thin to allow for enough e^- to pass through it without interactions (sec. 1.1), and that it can be placed in high vacuum. Consequently, the specimen needs to be prepared before it can be mounted to the specimen holder and imaged.

For material sciences this is of no concern, as the specimen are insensitive to vacuum and can be thinned by techniques such as electropolishing or chemical or ion etching. Specimens are typically mounted on copper grids [19] which are in turn placed in a specimen holder. Investigation of biological samples (e.g., micro-organisms, viruses, proteins), however, poses a particular challenge in the transmission electron microscopy

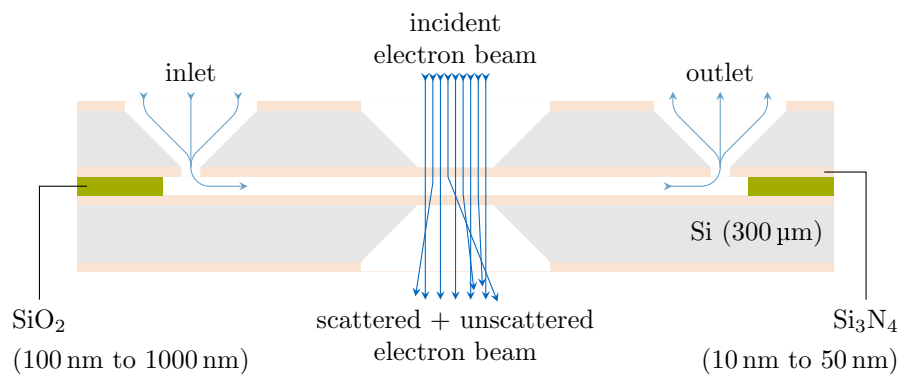


Figure 1.15: Schematic of a nanofluidic device created through bonding of two silicon (Si) wafers over a silicon dioxide (SiO₂) spacer with etched nano channel. At the illumination spot only a thin layer of silicon nitride (Si₃N₄) is between the liquid specimen and the tEM vacuum. Adapted from refs. [51, 52].

(TEM). In their elementary form they are hydrated, with water playing a key role in many of their processes [57]. Forms of life are typically incompatible with vacuum environments. To prepare such specimen for these harsh conditions multiple methods were developed [58], with one of the most successful being via the vitrification of water [59, 60]. This method resulted in images with an unprecedented resolution for biological samples. However, the limitation of this method is solidification and hence inability to record the dynamic processes occurring when biological samples are in their natural aqueous environment. This recently became possible by the use of nanofluidic devices [51, 52], where a specimen is dissolved in liquid and pumped through the nano channels in silicon under e^- illumination as seen in Fig. 1.15. In this scenario the aqueous state is maintained and a sufficiently thin target for TEM is introduced.

1.3.2 Detection of electrons

Until 30 years ago all transmission electron microscopes (tEMs) used either a photographic emulsion (film) or an imaging plate (IP) to record the images. Both need to be placed inside the tEM's vacuum chamber, and use chemical reactions triggered by e^- to store information in their media. After the illumination, additional steps outside the tEM are required to reveal the recorded information. The former needs to be developed much like a photographic film, whereas the latter has to be scanned with a small-spot helium–neon laser and digitized with a photomultiplier. Despite additional steps, which make the use of films and IPs very slow, they feature an excellent spatial resolution [17, 19] which was only recently surpassed by more advanced semiconductor detectors.

Charge coupled device (CCD) cameras were the first to be used as an alternative to the previous two visualisation methods. Due to the sensitivity to radiation defects caused by e^- , they were used in an indirect mode. This means that they were optically coupled with a scintillating material, where e^- generated photons, which were afterwards detected by a CCD camera. Generally, images recorded in this configuration were of lower quality due to multiple scattering of e^- in the scintillating material, isotropic generation of photons, and photon losses on boundaries of optical couplers. The upside, however, was a possibility to quickly record multiple images of a sample and have them instantaneously show up on a computer screen. Benefits and drawbacks of such detector designs are nicely described in refs. [61, 62].

Advancements in the commercial complementary metal-oxide-semiconductor (CMOS) technology made it possible to design CMOS cameras with enough resistance to radiation damage to be used in the direct mode where e^- generate the signal directly in the CMOS camera. The imaging speed of CMOS cameras was of the same level as in CCD cameras, but in spatial resolution they still lagged behind film and IP. This was because the initial devices were so thick that e^- underwent a multitude of scattering events in the camera's material, which in consequence resulted in a lateral spread of an interaction point. By thinning of the CMOS cameras down to the level of some tens of μm [63, 64] this limitation was overcome, and modern detectors in tEMs offer unprecedented spatial resolutions. Some key properties of commercially available detectors are collected in Tab. 1.2. A detailed evolution of the tEM e^- detectors is described in refs. [65, 66].

Table 1.2: Commercially available state-of-the-art detectors for TEM. All detectors are built in the CMOS technology and operated in the direct mode unless specified differently. Data taken from refs. [67, 68, 69, 70].

Detector	Pixel pitch [μm]	Array size [pixel ²]	Record speed [fps]
ThermoFischer Scientific Falcon 4	14	4096 \times 4096	250
Gatan K3	5 [†]	5760 \times 4096	1500
Direct Electron DE-64	6.5	8192 \times 8192	42
AMT NanoSprint43 Mk-II (indirect mode)	8.2	7915 \times 5436	10

[†] Acquired through an email exchange with Gatan.

1.4 EDET DH80k project

In recent years, there were many attempts to record dynamic processes [71, 72, 73] to help with the derivation of physical models. However, the bottleneck was always the underlying camera system in transmission electron microscopes (tEMs).

Development of commercially available state-of-the-art cameras (sec. 1.3.2) was pushed by fields like electron cryo-microscopy (cryo-EM) [74], which sets some of the most demanding requirements for detector performance. As the specimen in cryo-EM are radiation sensitive, there is a finite number of e^- that can be used to produce an image. In addition to that, the interaction between e^- beam and specimen also causes a specimen drift. Therefore, the cameras are highly specialized and take a multitude of consecutive intermediate images shot with a low intensity e^- beam, that are afterwards aligned and integrated together in the final, high resolution sharp image. In this kind of operation, the temporal resolution or underlying readout frequency plays a minor role. Consequently, cameras like this are not particularly suited to gain insights into dynamic processes (e.g., chemical processes or protein folding) to a great level of detail. On one hand, even with the recent improvements in the full frame readout frequency from some 10 Hz to about 1500 Hz, for instance, only the slowest parts of the protein folding dynamics (Fig. 1.16) starts to show. And on the other, there is a problem of inherently low contrast of biological specimen, as they are mainly comprised of low Z elements (hydrogen, carbon, nitrogen, oxygen). Therefore, a high intensity e^- beam is needed for illumination of the specimen in order to generate enough image contrast to distinguish different features in the specimen on every image, and not only on the integrated image as done in cryo-EM. Consequently, the camera system needs to be faster and feature an enormous dynamic range.

As there is currently no camera on the market that would fulfil all requirements needed for an investigation of dynamic processes, the EDET collaboration was formed with the purpose of developing and producing the EDET DH80k camera system.

The EDET collaboration consists of three institutes, namely, the Semiconductor Laboratory of the Max Planck Society (HLL MPG), the Max Planck Institute for the Structure and Dynamics of Matter (MPSD), and the Institute for Data Processing and Electronics (IPE) of the Karlsruhe Institute of Technology (KIT). Its plan is to provide a novel direct e^- detection EDET DH80k camera system based on depleted p-channel field effect transistor (DePFET) technology with the emphasis on high frame rate, high granularity and high contrast images. It will contribute the most to the time-resolved imaging experiments and to the study of fast dynamics in biological systems.

The EDET DH80k camera system (Fig. 1.17, 1.18) will consist of a single control computer, a power supply unit (PSU) and four identical modules, each capable of standalone operation. Each module will be comprised of an all silicon module (ASM), silicon support structure for mechanical and thermal stability, and a module interface circuitry (MIC) with a storage server for saving the recorded data. A PSU will provide two, galvanically decoupled 12 V power supplies to the MIC, which will afterwards generate all the necessary supplies to operate the module. In addition to that, MIC will also communicate with the control computer using a standard 1 Gbps ethernet connection, a trigger system, and a readout system to forward the data generated at the ASM to the

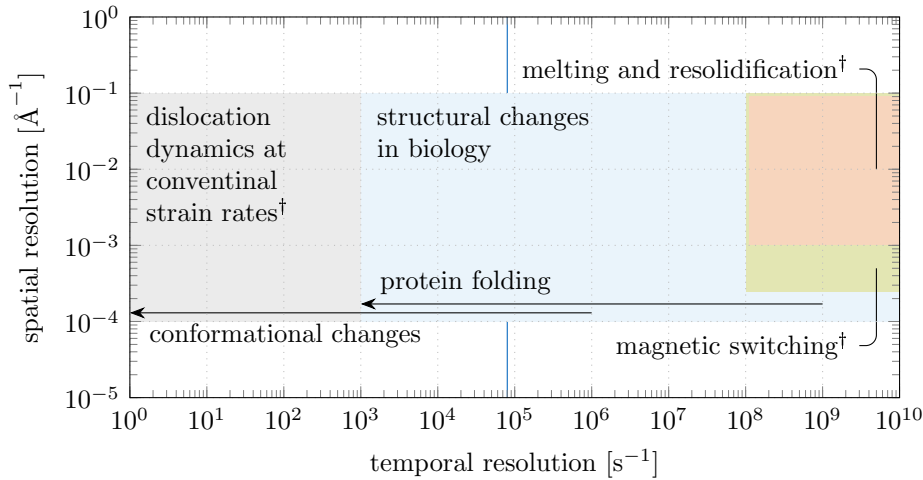


Figure 1.16: Spatial and temporal scales of the phenomena occurring in biology and material science (denoted by †). The arrows are indicating the time scales on which protein folding and conformational changes are occurring, and the blue line shows the maximum accessible temporal resolution for a camera operating at 80 kHz. Limits of the spatial resolution are showing the smallest resolvable feature (upper) and the typical field of view of interest (lower). The temporal resolution is defined as a single-shot investigation of an irreversible process. Adapted from refs. [75, 76, 77, 78, 79]

storage server over two standard 10 Gbps ethernet connections. At the time of writing, two different system topologies are being discussed for the inter-module communication, i.e. a master/slave (Fig. 1.18) and a star topology. In the former mode, clock and timing informations are generated and afterwards passed to a single (master) module, which then distributes it to the remaining (slave) modules via the inter module link (IML).

For the maximum integration density the ASM (Fig. 1.19) integrates a sensory part and its frontend electronics (readout and control), together with a lithography level aluminium–copper based interconnect system, on a common silicon substrate. Optimization steps were performed to minimize the backscattering of an e^- beam from an underlying silicon support structure and a beam stop. This in turn lowers the background level and improves the performance [81, 82]. By back-thinning [83] of the sensory part to $50\ \mu\text{m}$ or $30\ \mu\text{m}$, the amount of e^- interactions in the sensor will be reduced (sec. 1.1). In turn, this will offer an optimized line spread function [81, 82].

The focal plane of the EDET DH80k camera system will host a 1 Mpixel e^- sensitive array split over four ASMs assembled in such a way as to achieve a sensitivity gap of only

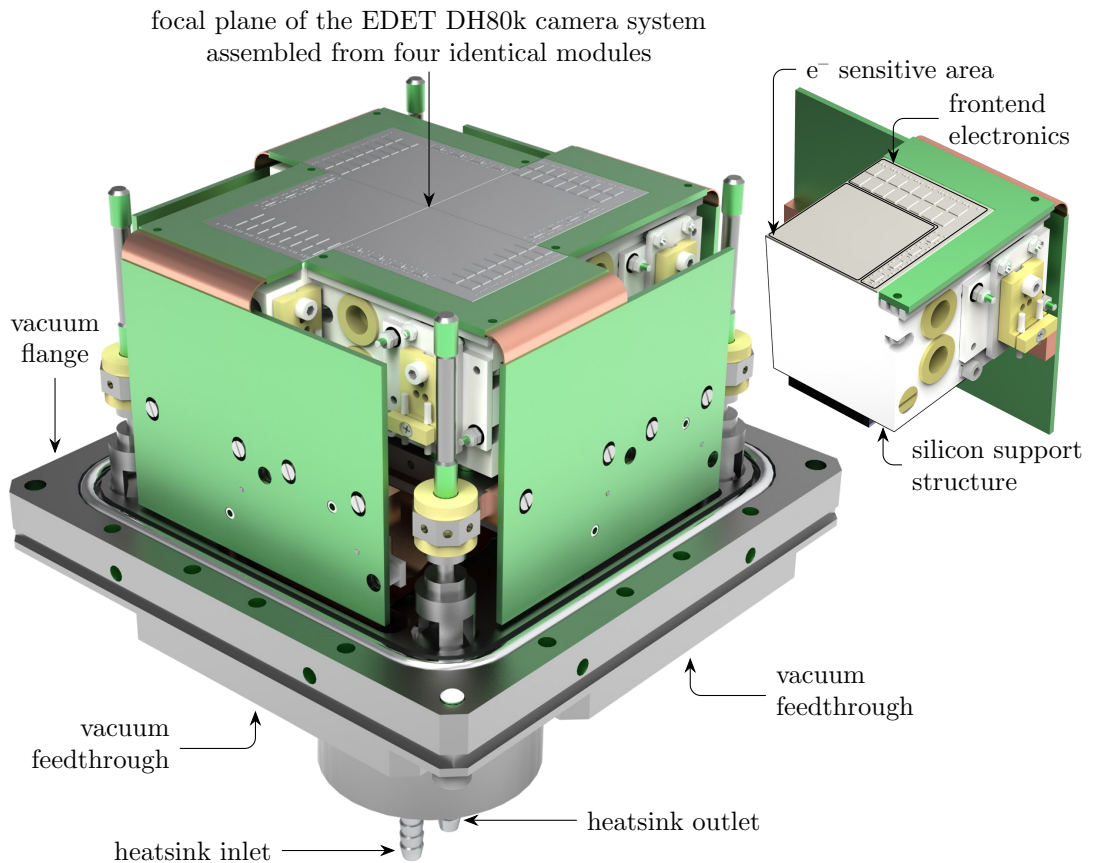


Figure 1.17: Computer aided design representation of a tEM part of the EDET DH80k camera system (left) assembled from four identical modules (right) [80].

1.2 mm. Consequently, each ASM will host 512×512 pixels, each covering $60 \mu\text{m} \times 60 \mu\text{m}$ for a total sensitive area of about $3 \text{ cm} \times 3 \text{ cm}$. In order to record single shot high contrast images at an ultra fast repetition rate, special care has been devoted to the pixel design and the e^- source design. As a result, each pixel will be able to store the signal from a minimum of $100 e^-$ impinging at a kinetic energy of 300 keV , that will be produced in the extremely short high luminosity pulse. This will allow for a stroboscopic mode of imaging, where the image blur, arising from sample movements, is minimized and the observation of the dynamics is limited by the full frame readout frequency of the camera. At a magnification factor of $50\,000$, $70 e^-/\text{nm}^2$ will hit the specimen at the specimen stage. In order to overcome the low signal to noise ratio at low signals, a non-linear response function is implemented on a pixel level. This means that the first few e^- hitting the pixel produce a higher response than the rest.

To achieve the most outstanding feature of the EDET DH80k camera system, i.e., a readout frequency of 80 kHz , multiple application-specific integrated circuits (ASICs)

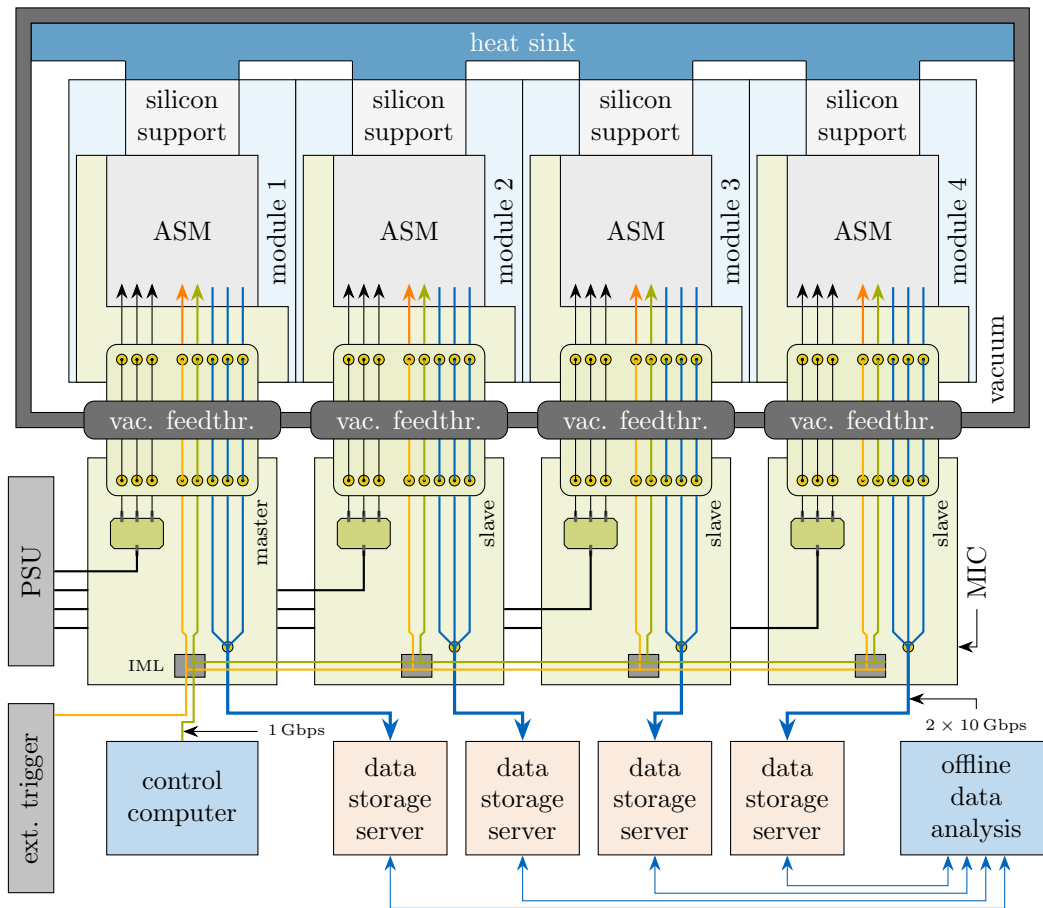


Figure 1.18: A simplified block schematic of the complete EDET DH80k camera system assembled from four modules as predicted in the final mode of operation. All abbreviations are defined in the paragraph around the figure.

will be used. As the readout will be done in the rolling-shutter mode, a minimum of two ASICs types will be needed – one to turn on the specific row, and the other to digitize the signal. The latter one, the so-called drain current digitizer (DCD) ASIC [84, 85] needs 100 ns for each digitization step with 8 bit precision.¹ Therefore, a special readout scheme, where all pixels in four rows are digitized in parallel [86], will be incorporated in combination with the SwitcherB ASICs [87]. This way a readout frequency of almost 80 kHz will be achieved. The biggest challenge at this point would be an enormous data transfer rate between the camera and the storage server. Since the EDET DH80k camera system will produce real images in integration mode, no data reduction will be possible. Therefore, the continuous mode of operation would produce 84 GB of data every second. Due to the fact that fast dynamic processes do not take very long to be completed, a continuous imaging like this is in fact not needed. Consequently, it is sufficient to record the short series of images that are recorded with a high intensity stroboscopic e^- beam of desired temporal resolution. Therefore, a third type of an ASIC will be implemented. The so-called DePFET movie chip (DMC) ASIC will serve as a fast memory buffer. It will record a movie consisting of 100 images recorded with a frame rate of 80 kHz. After this there will be an operational break of about 10 ms, to allow for the data transfer between the DMC and the storage server, before repeating the step. The current configuration allows for a repetition rate of 100 Hz, reducing the data rate to 11 GB/s. The above numbers can of course be subject to change, as the DMC ASIC is still under development.

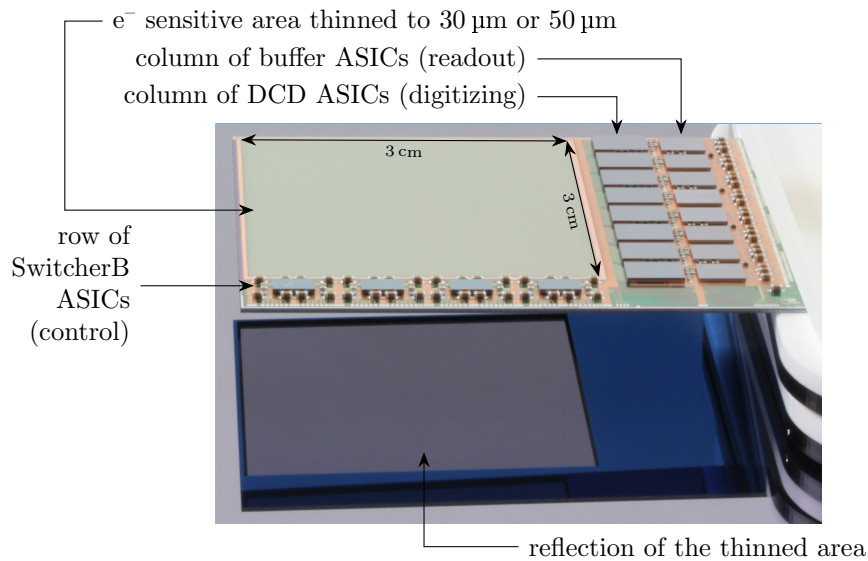


Figure 1.19: Picture of a fully populated dummy ASM.

¹A modified version of the DCD referenced in [84, 85] with increased input dynamic range will be used.

2 Essentials of semiconductor physics

A DePFET based radiation sensor is a flavour of silicon (Si) based radiation sensor that includes a few metal-oxide-semiconductor field effect transistor (MOSFET) elements. Therefore, in order to understand the functionality it is best to have a look in how Si based radiation sensors and MOSFETs function.

In the scope of this chapter, only the necessary parts of the semiconductor physics needed to understand how DePFETs function will be presented. Therefore, Si will be treated as a direct band gap semiconductor with abrupt junctions when speaking about impure material. For a complete overview ref. [88] or similar literature can be used.

2.1 Silicon properties

Silicon (Si) is a tetravalent element with an atomic number (Z) of 14. It can form a crystalline structure via four covalent bonds with neighbouring Si atoms in a so-called cubic diamond unit cell structure. A two-dimensional representation of such crystalline structure is shown in Fig. 2.1a. When atoms are closely packed they exhibit different properties as when they are isolated. In an isolated state, the energy states of shell e^- are discrete. However, when atoms are brought closer and closer, the energy states of least bound (valence) e^- become more and more degenerate due to the Pauli exclusion principle [89].¹ Therefore, when many atoms are close to each other it is necessary to speak in terms of energy bands, which form due to the periodically repeating potentials formed by the atoms. In case of Si atoms, packed in the cubic diamond unit cell with the length of 5.43 Å [88] an overlap of the valence e^- energy bands occurs. This results in the formation of valence and conduction bands, with an energy gap (E_G) of 1.12 eV between them. E_V denotes the top edge of the valence band, E_C the bottom edge of the conduction band, and $E_G = E_C - E_V$ represents a minimum necessary energy to break a covalent bond and raise an e^- from the valence band to the conduction band.² At the temperature of 0 K all e^- are in the valence band, meaning that all e^- are used to form covalent bonds. With increasing temperature, e^- forming the covalent bonds can gather enough energy to overcome the E_G and break the covalent bond (Fig. 2.1b). When the bond is broken the crystal is left with two things: an almost free e^- and a void instead of

¹The Pauli exclusion principle states that each quantum state can be occupied at most by a single identical fermion. Consequently, only one e^- can occupy one state.

²The described process is true for a direct band gap semiconductor. However, Si is an indirect band gap semiconductor – minimums of the E_C and the E_V are not vertically aligned in the energy–crystal momentum representation. Consequently, an additional momentum transfer to the crystal is necessary besides the E_G to raise the e^- from the valence to the conduction band [88, 90]. However, for the scope of this thesis a direct treatment is sufficient.

the covalent bond. The former can now move almost freely in the crystalline structure, and the latter is usually referred to as a hole (h^+), which can be mathematically treated as a quasiparticle of positive charge that moves in the opposite direction of a bound e^- that fill its place (Fig. 2.1c). In terms of energy bands (Fig. 2.1d), the e^- is raised from the valence to the conduction band, and the h^+ is generated in its place in the valence band. Both of those particles can conduct the electrical current. As the amount of broken bonds increases with the temperature, the electrical conductivity of crystalline Si in its intrinsic form increases as well.

The probability that the electronic state with an energy E is occupied is given by the Fermi-Dirac distribution function [88]

$$F(E) = \frac{1}{e^{(E-E_F)/k_B T} + 1} . \quad (2.1)$$

The variables k_B and T respectively denote the Boltzmann constant ($8.617 \cdot 10^{-23} \text{ eVK}^{-1}$ [11]) and the absolute temperature on the Kelvin scale, and E_F is the Fermi energy. E_F is defined as the E at which the probability for the electronic state to be occupied is exactly 1/2. In thermal equilibrium there is always the same concentration of e^- in the conduction band and h^+ in the valence band.

By adding impurities (doping) to the intrinsic Si, the crystal becomes extrinsic. This means that a part of Si atoms in the crystalline lattice is exchanged with atoms that have more (or less) valence e^- in comparison to the Si. Through this, the crystalline properties can be changed significantly, as the additional allowed energy states are introduced inside the band gap. Albeit the crystalline structure is still electrically neutral, additional charge carriers (e^- or h^+ – depending on the type of impurities) are introduced into it. Consequently, the concentrations of e^- in the conduction band and h^+ in the valence band at thermal equilibrium are not equal any more. Therefore, the terms *majority* and *minority* charge carriers are used.

By adding pentavalent atoms (for instance, phosphorous or arsenic) an n-type Si is obtained. Four valence e^- are used to make covalent bonds, whereas the fifth is only loosely bound to its nucleus (Fig. 2.2a). The energy state of the loosely bound e^- is slightly below the lower edge of the conduction band. Consequently, it can be easily ionized (donated) to the conduction band. Therefore, atoms like this are usually called donors and their energy level state is usually denoted with the E_D . For phosphorous and arsenic, the E_D is respectively 45 meV and 54 meV below the E_C [88]. Due to a small difference between the two energy states, many e^- are introduced to the conduction band and e^- become the majority charge carriers and h^+ the minority charge carriers. The story is reversed in case of trivalent atoms like boron or gallium. Those atoms lack one valence e^- in comparison to the intrinsic Si. They are named acceptors, because they can easily accept e^- from the Si valence band and, consequently, introduce h^+ into it (Fig. 2.2b). This type of Si is a p-type Si, and it has an additional allowed energy state just above the valence band. In the case of boron (gallium) dopant that state is 45 meV (72 meV) above the E_V and is usually denoted with E_A . In the p-type Si, h^+ are the majority charge carriers and e^- the minority charge carriers.

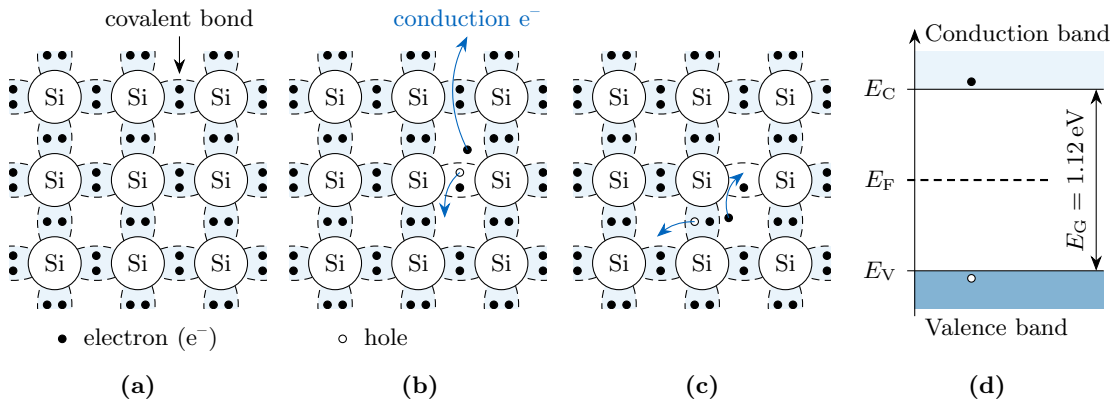


Figure 2.1: (a) Si crystalline structure represented in the two-dimensional schematic. (b) A broken covalent bond results in an e^- with enough energy to move to the conduction band, where it is mobile and can conduct an electrical current. In its place, a void is left which can be mathematically treated as a quasi-particle moving in the opposite direction of e^- , as shown in (c). (d) Schematic energy band diagram with a single state occupied in the conduction band. $E_G = E_C - E_V$ and it denotes the minimum energy necessary for an e^- to jump from the valence band to the conduction band. Adapted from ref. [88].

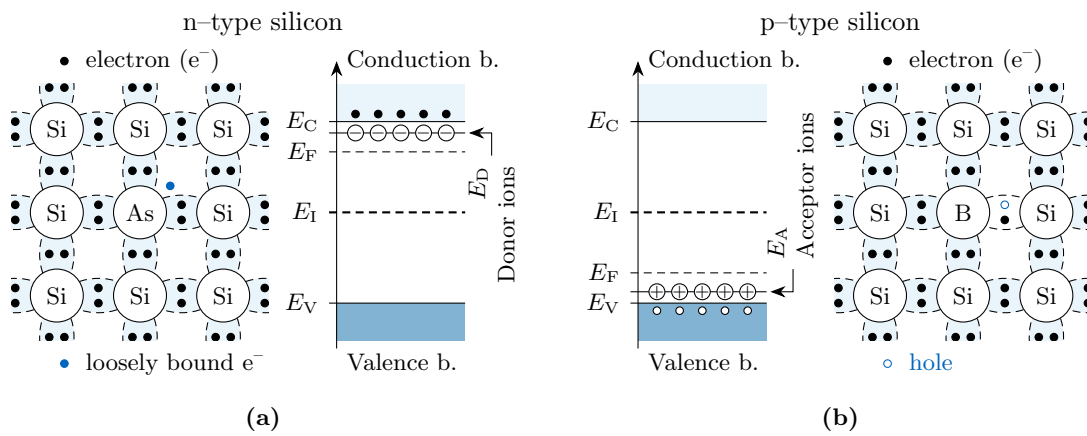


Figure 2.2: (a) n-type Si with an arsenic (As) as a donor. Two-dimensional representation (left) and the energy band diagram with completely ionized donor atoms (right). (b) p-type Si with a boron (B) as an acceptor. Two-dimensional representation (right) and the energy band diagram with completely ionized acceptor atoms (left). The E_I represents a Fermi energy of an intrinsic Si. Adapted from ref. [88].

Due to the difference between filled states in extrinsic and intrinsic Si crystal the Fermi energy level shifts when impurities are introduced (Fig. 2.2).

On the topic of nomenclature in literature: in addition to p and n notations for the extrinsic types of Si, one can also find the n^+ , n^- , p^+ , p^- notations, where + and – respectively describe the higher and lower density of dopants.

The charge transport in Si is governed by two mechanisms, namely diffusion and drift. In the former, the movement is governed by thermal motion with the addition of a spatial variation in carrier concentration. Therefore, the carriers diffuse from places with higher concentrations towards the places with lower concentrations. If many e^- were injected at a single tiny spot in the intrinsic Si, the diffusion would cause them to diffuse apart uniformly in all directions. The second transport mechanism, i.e., the drift, is caused by the electrical field (\mathcal{E}) in Si crystal. This field can either be of an external or internal nature. In contrast to the diffusion, the charge carriers move in the net direction specified by the \mathcal{E} , i.e., h^+ drift in the \mathcal{E} direction and e^- against it. In general it can be written that the drift velocity (v) of either e^- or h^+ is [88]

$$v = \mu \mathcal{E} , \quad (2.2)$$

where the μ represents the mobility of either e^- or h^+ . Charge carrier mobility is limited due to the scattering events with the crystal lattice (and its defects) and ionized doped atoms, and it also depends on the temperature. In general, mobility is higher at lower temperatures and at lower dopant densities. Additionally, the above eq. 2.2 is valid only for small \mathcal{E} ($\leq 10^3$ V/cm at 300 K [88]). With higher \mathcal{E} , charge carriers are accelerated to higher velocities but they also dissipate more energy in scattering events. Therefore, there exists a terminal velocity called a saturation velocity (v_s) of about 10^7 cm/s for Si at 300 K [88]. The empirical formula for drift velocity that approximates the experimental results over a wide range of \mathcal{E} is [88]

$$v = v_s \left[1 + (\mathcal{E}^0 / \mathcal{E})^\gamma \right]^{-1/\gamma} . \quad (2.3)$$

The \mathcal{E}^0 and γ are constants for e^- (h^+) in high purity Si of respectively $7 \cdot 10^3$ V/cm ($2 \cdot 10^4$ V/cm) and 2 (1) [88].

2.2 Detection of ionizing radiation

When a part or the complete energy of incoming ionizing radiation is absorbed in the Si bulk, it generates a cloud of e^- and h^+ in it. On average, a single e^-/h^+ pair is created for every 3.66 eV [91] of absorbed energy (E_{abs}).³ The average number of e^-/h^+ pairs (N_p) is therefore equivalent to

$$N_p = \frac{E_{\text{abs}}}{3.66 \text{ eV}} . \quad (2.4)$$

³This number deviates from the band gap energy (E_G) of 1.12 eV due to phonon creation.

After a sufficiently long period of time, the system will remove all created pairs through the mechanism of recombination, in order to return to the thermal equilibrium. But as the idea is to measure the amount of generated pairs, this process needs to be suppressed. By applying a potential difference (ϕ) over the facing borders of a Si crystal, the generated \mathcal{E} separates the e^-/h^+ pairs, diminishes the recombination and causes a flow of charge carriers, i.e., a current. Even by exclusion of the thermally generated e^-/h^+ pairs, no Si crystal is perfectly intrinsic. Consequently, its majority charge carriers contribute an additional component to the drift current, and both contributions are measured at the same time. In order to circumvent this problem, it is convenient to join the p- and n-types of Si together, as depicted in Fig. 2.3a. The result of this is the majority charge carrier diffusion in vicinity of the metallurgical junction, from one type of Si into the other, where they essentially recombine. A small region around the metallurgical junction consequently becomes depleted of majority charge carriers, and charged with stationary ionized dopant atoms. A region like this is usually called a depleted region (DR). Charged stationary ionized dopant atoms in the DR generate the built-in electric field (\mathcal{E}_{bi}), which opposes the diffusion. Consequently, the probability of majority carrier diffusion from one type of the Si into the other, over the DR, is reduced. However, the process continues until a thermal equilibrium is reached. An interesting property of this combination is that it conducts the current under an external bias only in one direction (so-called forward bias), whereas in the other only a constant tiny amount can flow (so-called reverse bias). The tiny amount of current flow in the reverse bias condition is a consequence of the thermally generated e^-/h^+ pairs in the

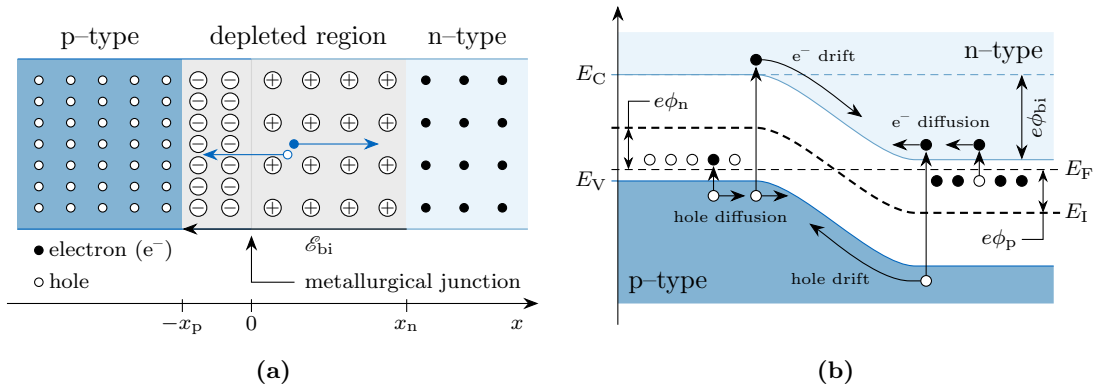


Figure 2.3: An abrupt pn-junction without external biasing in a schematic representation (a) and an energy band representation (b). Due to the diffusion and recombination of the majority charge carriers at the pn-junction a DR is formed. This region is free of charge carriers but charged due to the ionized dopant atoms that are fixed in the crystal lattice. Consequently, there is a built-in potential difference (ϕ_{bi}) and a corresponding built-in electric field (\mathcal{E}_{bi}) over the length of this region. If an e^-/h^+ pair (\bullet) is generated in this region, it is separated due to the drift caused by the \mathcal{E}_{bi} . Adapted from ref. [88].

DR, and charge carrier diffusion from non-depleted regions. In the scope of this work work, this contribution will be measured in terms of leakage current.

A note on the creation of pn-junctions: they are usually not created by metallurgical joining of two extrinsic types of Si as presented in this section. The base material to be used is an intrinsic Si bulk that has an either n- or p-type base doping from the fabrication process. In order to achieve a different type or a different concentration of the dopant different methods can be used, such as ion implantation or ion diffusion. In the case of the ion implantation, the bulk material is implanted with the desired dopant from the side.⁴ Consequently, a change in material type or dopant concentration is achieved on the side of the implantation. Through this method, a precise control of the dopant's concentration and depth can be achieved. The former is defined by the duration and current of an ion implantation process, and the latter with the selection of the appropriate energy of ions. An additional step after the ion implantation process is required to mitigate the problem of lattice displacements, and to move the dopants from interstitial to substitutional lattice sites.⁵ This is performed through heating of material [88].

The e^-/h^+ pairs generated in the DR are separated by the \mathcal{E}_{bi} and they contribute to the current, without the majority carrier contribution as in the above case. Therefore, by measuring the current generated in the DR this device can be used as a sensor for the ionizing radiation. An active volume of this kind of a sensor is the full DR with an addition of a volume at its edges, from where the e^-/h^+ pairs can diffuse into the DR and contribute to the current.

The size of DR is calculated by Poisson's equation [33]

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_{Si}\varepsilon_0}, \quad (2.5)$$

by knowing the charge density distribution ($\rho(x)$) and the relative Si permittivity (ε_{Si}) of 11.9 [90]. As an example, the size of the built-in DR with the uniform $\rho(x)$ on each side of an abrupt metallurgical junction will be calculated.

$$\rho(x) = \begin{cases} -eN_A & -x_p \leq x < 0, \\ eN_D & 0 < x \leq x_n, \end{cases} \quad (2.6)$$

where N_A (N_D) is a concentration of acceptor (donor) atoms with which the Si is doped with, and x is the position where 0 denotes the location of metallurgical junction (Fig. 2.3a). The d is evaluated as

$$d = x_p + x_n = \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0}{e} \left(\frac{N_A + N_D}{N_A N_D} \right) \phi_{bi}}, \quad (2.7)$$

where ϕ_{bi} represents a built-in potential difference over the pn-junction. The ϕ_{bi} can be visualised in the energy band representation (Fig. 2.3b). It is calculated as the difference

⁴Selected ions are accelerated to the desired energy and shoot into the bulk material.

⁵Process of dopant activation.

between the intrinsic Fermi energy (E_I) of each part and the Fermi energy of the common system (E_F) [88]:

$$\phi_{bi} = \phi_n - \phi_p = \frac{k_B T}{e} \ln \left(\frac{N_A N_D}{n_i^2} \right). \quad (2.8)$$

The n_i represents a charge carrier concentration in the intrinsic Si, which is $9.65 \cdot 10^9 \text{ cm}^{-3}$ at the temperature of 300 K [92]. With typical N_D and N_A values for donor and acceptor concentrations ($1 \cdot 10^{13} \text{ cm}^{-3}$ and $5 \cdot 10^{19} \text{ cm}^{-3}$) a ϕ_{bi} of 0.76 V and a depletion width of 10 μm are obtained, both calculated at the temperature of 300 K.⁶ As it is impractical to be limited by a sensitive volume of only 10 μm , it needs to be increased.

2.2.1 Extending the sensitive volume

The simplest way to extend the sensitive volume is to bias the pn-junction in a reverse bias mode, i.e., grounding the n-type side of the pn-junction and biasing the p-type side with a negative voltage (U). This way, the built-in DR will be increased, as the ϕ_{bi} contribution in eq. 2.7 is substituted with $\phi_{bi} - U$. Consequently, the sensitive volume can span the complete material. In addition to an increased sensitive volume, this mode of operation decreases the capacitance and with it influences the level of noise (sec. 3.2) [33]. Moreover, the smaller the capacitance, the smaller the capacitive loading that slows the electrical circuits.

The limiting factor to the maximum applied U is the so-called break-down voltage which generates a break-down electric field in the sensitive volume. At this field, the probability for e^- to gather enough energy between scattering events to ionize further e^-/h^+ pairs becomes significant. The consequence is a self-sustaining flow of charge carriers through the material. Despite this, it is possible to deplete the Si up to the level of multiple mm [33].

In addition to front and backside biasing approach, as in sec. 2.2.1, a sideways depletion approach and a punch-through depletion approach are used as well. They are described in the following paragraphs.

Sideways depletion The sideways depletion approach was first proposed by E. Gatti and P. Rehak in 1984 [93] in order to decouple the detector size and the capacitance of its readout node.

In order to fully deplete the sensitive volume of the sensor through this approach, the configuration as presented in Fig. 2.4 is needed. The sensor comprises of the n-type Si bulk with two large p^+ -type implantations, one on the frontside and the other on the backside, and a small n^+ -type implantation that serves as a readout node. The small readout node is the reason that this configuration has a much smaller capacitance compared to the standard pn-junction. However, there is another additional benefit of this configuration. As the size of the depletion region is proportional to \sqrt{U} for $U \gg \phi_{bi}$, the U needed to deplete the complete Si is effectively reduced by a factor of four. This in

⁶For DePFETs used in this work.

turn lowers the \mathcal{E} and reduces the probability of the break-down effect when depleting a volume of the same thickness.

The potential distribution for a fully depleted Si bulk can be calculated by double integration of eq. 2.5. For the uniform charge distribution of $\rho(x) = eN_D$, with an approximation of $N_A \gg N_D$ a parabolic potential distribution is obtained

$$\phi(y) = y^2 \left(-\frac{eN_D}{2\varepsilon_{\text{Si}}\varepsilon_0} \right) + y \left(\frac{U_{\text{BACK}} - U_{\text{FRONT}}}{t} - \frac{eN_D}{2\varepsilon_{\text{Si}}\varepsilon_0} t \right) + U_{\text{FRONT}} . \quad (2.9)$$

The t denotes the sensor thickness and the potential minimum is formed at the position y_{min} in the Si bulk

$$y_{\text{min}} = \frac{t}{2} + \frac{\varepsilon_{\text{Si}}\varepsilon_0}{eN_D} \frac{U_{\text{BACK}} - U_{\text{FRONT}}}{t} . \quad (2.10)$$

A problem of the design as presented in Fig. 2.4 would be the missing lateral gradient in the potential distribution. The e^-/h^+ pairs created in the lower left half of the sensor in Fig. 2.4c would get separated by the drift \mathcal{E} pointing perpendicular from the potential minimum to the p^+ implantations. Therefore, h^+ would drift up or down to the p^+ -type implantation (depending on the generation point in respect to the e^- potential minimum) and e^- up towards their potential minimum. At this point they would be stuck and could only reach the readout node via diffusion. In order to prevent this, the front implantation can be segmented and connected together through the voltage divider ladder. That way the most negative voltage is applied to the first p^+ -type implantation, with a gradual increase as the implantations get closer to the readout node. That way, the potential minimum is sloped and the e^- drift towards the readout node.

Punch-through depletion The punch-through (PT) method to deplete the complete Si volume only became popular in recent years. The mechanism was first noticed in MOSFETs where it appeared as an unwanted consequence of the lowering of transistor dimensions [88]. At one point, one implant started to influence (bias) the second one through the Si bulk. If used with detector devices, this parasitic effect can be useful if a physical contact to the implant cannot be placed. For instance, the backside of the future Si sensor needs to be free of any excess material, as it would cause additional scattering effects (sec. 1.1) and signal losses, or it simply cannot be reached by the electrical wire [95]. In that case, the n-type Si bulk can be depleted by placing a big floating (unconnected) p^+ -type implantation on the backside that stretches over the complete sensor, and a small PT p^+ -type implantation on the frontside (called PT node). In addition, the readout n^- -type nodes are needed on the frontside, that are biased with respect to ground. The described structure and depletion process is graphically represented in Fig. 2.5. By negatively biasing the PT node the DR is formed below it (Fig. 2.5a). When the bias is negative enough for the DR to span through the complete Si bulk it joins with the built-in DR of the backside p^+ -type implantation (Fig. 2.5b). By further decreasing the PT node bias, the backside p^+ -type implantation gets more and more negative (due to punch-through biasing), and the now joined DR

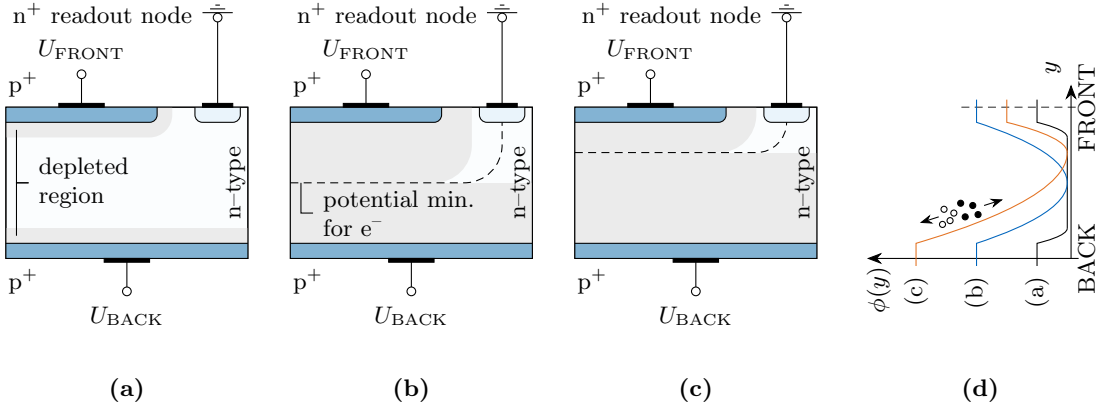


Figure 2.4: Sideways depletion approach to deplete the n-type Si bulk through biasing of the two p⁺-type implantations. (a) U_{FRONT} and U_{BACK} are not negative enough for the DRs to join. (b) Merged DRs with $U_{\text{FRONT}} = U_{\text{BACK}}$ form a potential minimum for e⁻ in the middle of the Si bulk (---). (c) By applying $U_{\text{BACK}} < U_{\text{FRONT}}$ the potential minimum can be moved closer to the top of the sensor. (d) Potential distribution through the Si bulk for the described three cases. Adapted from ref. [93].

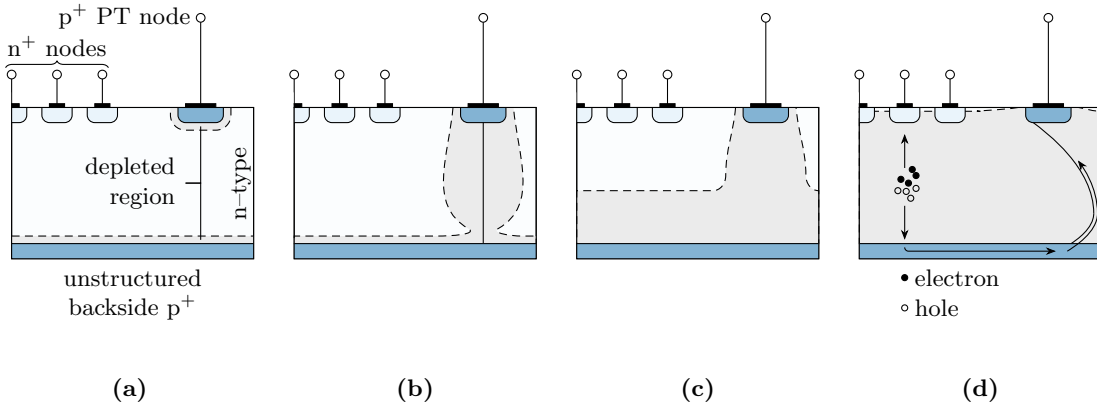


Figure 2.5: Punch-through (PT) depletion approach to deplete the n-type Si bulk by biasing a single p⁺-type implantation. (a) p⁺-type PT node is biased too positive for the DR to join the built-in DR from the p⁺-type implantation on the backside (backside DR). (b) PT node is negative enough for the DR to span over the complete thickness of the Si bulk and connect to the backside DR. (c) By biasing the PT node more and more negative the joint DR grows from the backside towards to the frontside. (d) Fully depleted Si bulk in which the e⁻ drift towards the closest n⁺-type implantation node and h⁺ drift first to the backside and then towards the side below the PT node. Here they need to overcome a small potential barrier before they get extracted from the system by the PT node. Adapted from ref. [94].

starts increasing from the backside towards the frontside (Fig. 2.5c). Full Si bulk is depleted at roughly twice the potential needed to deplete a pn-junction (sec. 2.2) with the same thickness (Fig. 2.5d). The e^-/h^+ pairs generated in the Si bulk drift apart due to the \mathcal{E} , e^- drift towards the frontside to the closest readout node, whereas the h^+ drift towards the p^+ -type implantation at the backside. Afterwards, they continue drifting towards the side of the Si bulk, where they have to overcome a small potential barrier, before they can drift towards the PT node at the frontside where they get extracted from the system.

In order to completely deplete the Si bulk via the punch-through method, an increase of about 2 to the applied voltage is necessary. Therefore, this method is only useful when the Si bulk is very thin (e.g., less than 100 μm).

The mechanism of a punch-through depletion is described in more detail in ref. [94].

2.3 MOSFET structure

A transistor is essentially a voltage controlled current amplification structure. A metal-oxide-semiconductor field effect transistor (MOSFET) name can be split into two halves. The first half is indicating that the structure is comprised of a stack of metal, oxide and silicon (MOS), whereas the second half is suggesting the mechanism used by the device to steer the current (FET). In the scope of this thesis a p-type MOSFET structure will be presented (Fig. 2.6). It is comprised from a gate structure (historically made from a metal material, but nowadays a heavily doped polycrystalline-silicon (poly-Si) is a standard), an insulator layer (e.g., silicon oxide (SiO_2)), and an n-type Si bulk with p^+ -type implantations on each side of the gate. One of the implantations is usually referred to as a source, and the other as a drain.

Biasing of the described device is done through the bulk, source, drain and gate contacts via respective U_B , U_S , U_D and U_G voltages. In usual biasing conditions the U_S and U_B are grounded, U_D is more negative than the U_S , and the level of U_G controls the

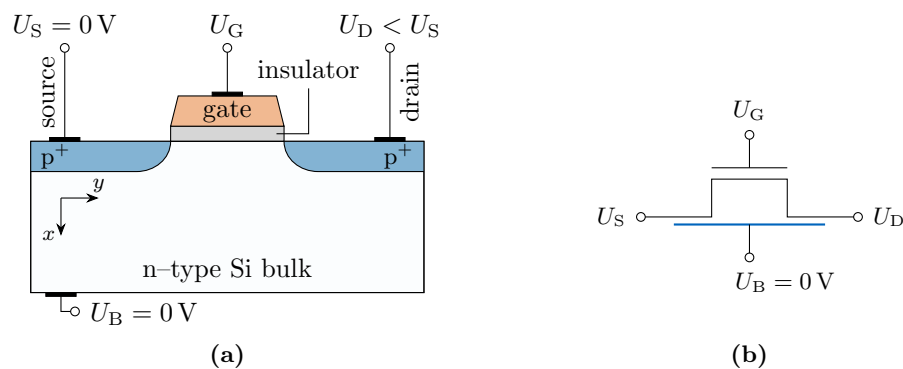


Figure 2.6: A p-type MOSFET structure with general biasing conditions represented in a two-dimensional schematic (a), and as an electrical symbol (b).

current between the source and drain nodes. A common notation is that all voltages are given with respect to U_S , and this will also, hereinafter, be true for any given voltage or potential reported in this thesis, unless explicitly specified otherwise. Therefore, the notations of $U_D = -5\text{ V}$ and $U_G = 3\text{ V}$ mean that the drain and gate nodes are respectively -5 V lower and 3 V higher than the U_S .

Prior to describing the relation between current flow and applied voltages, it is useful to investigate a field effect caused by the MOS structure operated as a capacitor. Fig. 2.7 shows three different states of the system, that can be obtained by changing the U_G . The changes between the states are characterised with respect to the so-call flat-band potential (U_{FB}) and the threshold voltage (U_T). The former is a potential at which there is no band bending in Si and consequently no electric field in the oxide, whereas the latter is a condition at which the surface of the semiconductor changes its type, i.e., for n-type Si the concentration of minority charge carriers (h^+) at the surface surpasses that of the majority charge carriers (e^-). In general, the voltage that is applied to the gate has to equal the sum of the flat-band voltage, the band curving potential (ϕ_S), and

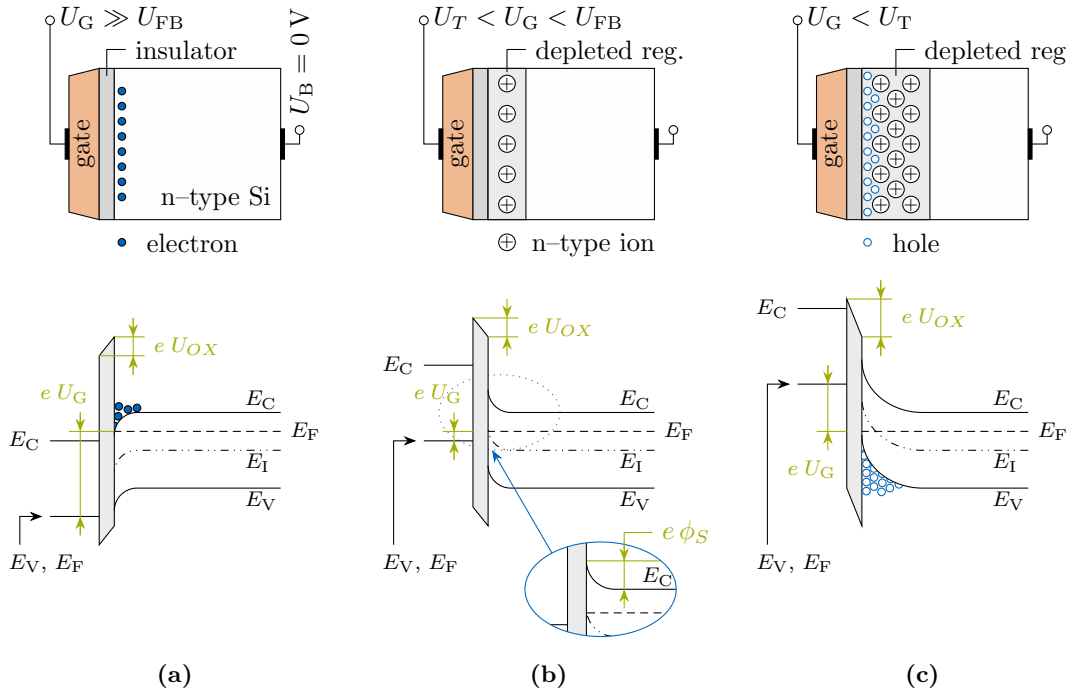


Figure 2.7: A metal-oxide-semiconductor structure operated as a capacitor represented with two-dimensional schematic (upper half) and energy band diagram (lower half). For the gate material a p^+ -type poly-Si is used. By changing the gate voltage the system can be put to accumulation (a), depletion (b) or inversion (c) mode of operation.

the oxide potential (U_{OX}):

$$U_G = U_{FB} + \phi_S + U_{OX} . \quad (2.11)$$

The graphical explanation to the two newly introduced terms can be found in Fig. 2.7b.

Accumulation mode (Fig. 2.7a) Applying a more positive U_G than the U_{FB} will bend the energy bands at the surface of the Si downward. Consequently, it will bring this part of the conduction band of Si closer to its Fermi potential. This means that there will be more states in the conduction band that are occupied with e^- . In other words, e^- are accumulated close to the Si surface. Therefore, in the first approximation, this configuration can be treated as a plate capacitor where voltage is applied on one side of the insulator and the surface charge (Q_{ACC} in units of C/cm^2) is accumulated on the other. Voltage drop over the insulator (U_{OX}) is therefore

$$U_{OX} \doteq U_G - U_{FB} = -\frac{Q_{ACC}}{C_{OX}} = -\varepsilon_{OX}\varepsilon_0 \frac{Q_{ACC}}{t_{OX}} , \quad (2.12)$$

where C_{OX} is the insulator capacitance per unit area (F/cm^2). The C_{OX} is calculated as the $t_{OX}/\varepsilon_{OX}\varepsilon_0$, where t_{OX} is the thickness of the insulator material and ε_{OX} its relative permittivity. The approximation here is that the ϕ_S (eq. 2.11) is neglected due to being small. Additionally, any fixed charges in the insulator material are neglected as well.

Depletion mode (Fig. 2.7b) By applying the U_G that is slightly more negative than the U_{FB} , the system is brought in a mode where the Fermi level at Si surface is far away from both allowed Si energy bands. Consequently, the probability to find any charge carriers near the Si surface is very small. Effectively, a part of the volume near the surface is depleted of charge carriers. The potential depleting the Si is the potential of the energy band bending (ϕ_S). Width of the depleted region (d_{Si}) can be calculated by the Poisson equation (eq. 2.5). For the n-type of Si under the assumption of uniform charge distribution (eN_D) it is

$$d_{Si} = \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0|\phi_S|}{eN_D}} . \quad (2.13)$$

From here eq. 2.11 can be solved in the same way as before, with the difference that the charge on the imaginary plate capacitor is the charge from the depleted region's stationary ion charges (Q_{DEP})

$$Q_{DEP} = eN_D d_{Si} , \quad (2.14)$$

and the gate potential is therefore

$$U_G = U_{FB} + \phi_S - \frac{Q_{DEP}}{C_{OX}} = U_{FB} - \frac{eN_D d_{Si}^2}{2\varepsilon_{Si}\varepsilon_0} - \frac{eN_D d_{Si} t_{OX}}{\varepsilon_{OX}\varepsilon_0} . \quad (2.15)$$

Inversion mode (Fig. 2.7c) Further reduction of the U_G increases the energy band bending. The interesting effect happens when the $(E_V - E_F)_{\text{surface}}$ equals the $(E_F - E_C)_{\text{Si bulk}}$. At that point, the concentration of minority charge carriers (h^+) at the surface equals the concentration of majority charge carriers (e^-). Effectively, the Si surface changes from the n-type to the p-type. Afterwards, the energy band bending saturates at the value of

$$\phi_{S, \text{sat}} = -2 \frac{(E_I - E_F)_{\text{Si bulk}}}{e} = -2\phi_B = -2 \frac{k_B T}{e} \ln \frac{N_D}{n_i}. \quad (2.16)$$

Consequently, the depleted region reaches its maximum depth ($d_{\text{Si, sat}}$) and any additional decrease of the gate potential changes only the amount of h^+ at the surface (Q_{INV}). The gate voltage equals

$$\begin{aligned} U_G &= U_{\text{FB}} + \phi_{S, \text{sat}} - \frac{Q_{\text{DEP}}}{C_{\text{OX}}} - \frac{Q_{\text{INV}}}{C_{\text{OX}}} \\ &= U_{\text{FB}} - 2\phi_B - \frac{\sqrt{2\varepsilon_{\text{Si}}\varepsilon_0 e N_D 2\phi_B}}{C_{\text{OX}}} - \frac{Q_{\text{INV}}}{C_{\text{OX}}} \\ &= U_T - \frac{Q_{\text{INV}}}{C_{\text{OX}}}, \end{aligned} \quad (2.17)$$

where the U_T defines a point at which the surface changes from depletion to inversion.

Notes on the derivation For the derivation of the above equations, multiple assumptions were used. In the first approximation the possibility of fixed charges being present in the insulator material is neglected. They can be included in the U_{FB} by mapping the $U_{\text{FB}} \rightarrow U_{\text{FB}} - Q_{\text{OX}}/C_{\text{OX}}$. More about the so-called oxide charges will be presented at a later point when the effects of radiation damage will be investigated (sec. 3.3).

The next simplification was done by omitting the possibility of energy band bending in the poly-Si. By taking it into account one would need to allow for a small depletion layer being formed in the poly-Si. This leads to the increase of a C_{OX} by the capacitance of the depleted poly-Si layer.

In addition, it was assumed that the h^+ will appear at the surface as soon as the surface E_F is close enough to the surface E_V . However, as the h^+ are a minority charge carrier in the n-type Si bulk they need to be thermally generated and this takes time. This is, however, not the case in the MOSFET structures, as they are supplied from the neighbouring p-type implantations.

To get a complete overview of the MOS capacitor of MOSFET structure characteristics, one can take a look in the standard semiconductor physics textbooks like ref. [90] or more application specific textbooks like refs. [88, 96].

2.3.1 Current-voltage characteristics

In the inversion mode of the MOSFET structure, the p-type implantations on both sides of the gate, namely source and drain, supply the h^+ that form the inversion layer

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at the surface of the Si. This inversion layer is usually referred to as a channel, through which the h^+ can flow if the source and drain are kept at different potentials. The source and drain potentials also change the surface potential ϕ_S , as it needs to be continuous at the boundaries

$$\phi_S(y) = U_{CH}(y) + \phi_B = U_{CH}(y) - 2\phi_B, \quad (2.18)$$

where U_{CH} denotes the potential in the channel, and y is the coordinate along the channel between the source and drain implantations. By grounding the source and applying the U_D on the drain, the $\phi_S(0) = 0$ and $\phi_S(L) = U_D$ conditions are obtained, with L denoting the length of the channel. By insetting this mapping to eq. 2.11 a position dependent charge in the channel $Q_{INV}(y)$ is derived. The channel current or drain current can be written as a

$$I_D = -v_h(y) Q_{INV}(y) W, \quad (2.19)$$

where $v_h(y)$ is the h^+ velocity in channel that depends on the channel $\mathcal{E}_y(y)$ caused by the potential difference between drain and source (eq. 2.2), and W is the width of the channel. W should be imagined in the third dimension in Fig. 2.6 coming out of the paper. Writing everything together under the assumption of constant mobility and neglecting the velocity saturation the I_D becomes

$$\begin{aligned} I_D &= -\mu_h \mathcal{E}_y(y) Q_{INV}(y) W = \mu_h \frac{dU_{CH}}{dy} Q_{INV}(y) W \\ &= -\mu_h \frac{dU_{CH}}{dy} \left[C_{OX}(U_G - U_{FB} - U_{CH} + 2\phi_B) \right. \\ &\quad \left. + \sqrt{2\varepsilon_{Si}\varepsilon_0 eN_D(-U_{CH}(y) + 2\phi_B)} \right] W. \end{aligned} \quad (2.20)$$

The final result for the I_D is obtained by solving the following

$$\int_{y=0}^{y=L} I_D dy = \mu_h W \int_{U_{CH}=0}^{U_{CH}=U_D} Q_{INV}(U_{CH}) dU_{CH},$$

and it yields

$$\begin{aligned} I_D &= -\frac{W}{L} \mu_h \left[C_{OX} \left(U_G - U_{FB} + 2\phi_B - \frac{U_D}{2} \right) U_D \right. \\ &\quad \left. - \frac{2}{3} \sqrt{2\varepsilon_{Si}\varepsilon_0 eN_D} \left((-U_D + 2\phi_B)^{3/2} - (2\phi_B)^{3/2} \right) \right]. \end{aligned} \quad (2.21)$$

In the beginning I_D increases linearly with drain voltage, whereas for larger drain voltages the I_D follows a quadratic U_D behaviour until it reaches the saturation point ($\partial I_D / \partial U_D = 0$). At this point the $Q_{INV}(y)$ at the drain end becomes 0, and further decreases of the U_G cause a so-called pinch-off effect⁷ on the MOSFET channel, which

⁷Shortening of the channel length to $L' < L$.

prevents further increase of the I_D [88, 90, 96].⁸ $U_{D, \text{sat}}$ can be calculated from eq. 2.17 with the condition that the Q_{INV} at drain end is 0 and ϕ_S at the drain end equals $U_D - 2\phi_B$ (eq. 2.18). With this the $I_{D, \text{sat}}$ can be calculated by the substitution of the U_D in eq. 2.21. The next effect that limits the I_D is the channel h^+ velocity saturation (sec. 2.1). When h^+ reach their maximum velocity, any further decrease of the U_D will not result in more current flow. The third effect, that was already mentioned in sec. 2.2.1 under the punch-through depletion paragraph, is the punch-through effect. At short gate lengths, drain potential can influence I_D even in the saturation mode through an effect called drain-induced barrier lowering [88, 90]. However, in the scope of this thesis this effect brings no additional value and it can be ignored. Consequently, simplified expressions for I_D will be used:

$$I_D = \begin{cases} 0 & U_G > U_T, \\ -\frac{W}{L} \mu_h C_{\text{OX}} \left[(U_{G, \text{eff}} - \frac{U_D}{2}) U_D \right] & U_{D, \text{sat}} < U_G < U_T, \\ -\frac{W}{L} \mu_h C_{\text{OX}} \frac{U_{D, \text{sat}}^2}{2} = -\frac{W}{L} \mu_h C_{\text{OX}} \frac{U_{G, \text{eff}}^2}{2} & U_{D, \text{sat}} > U_G \end{cases} . \quad (2.22)$$

The $U_{G, \text{eff}}$ represents a $U_G - U_T$, and $U_{D, \text{sat}}$ equals the $U_{G, \text{eff}}$ as calculated from the $\partial I_D / \partial U_D = 0$ condition.

The three different I_D characteristic regions that depend on the U_G are named cut-off, linear, and saturation region. In the first one, U_G is above U_T and the MOS structure is in depletion mode which prevents the current flow between source and drain. In this simple theory the I_D should be 0, but in practice it has a finite small value due to the diffusion of charge carriers and the thermal generation. By lowering the U_G to the vicinity of the U_T a transition to the linear region occurs. This transition region is usually referred to as the subthreshold region, where the Si surface gets only weakly inverted and the current is dominated by diffusion. Even a tiny change in the U_G has a huge impact on the I_D , i.e., I_D changes for several orders of magnitude in a few 100 mV of U_G change before reaching the linear region. In general, the current in the subthreshold region follows expression given in ref. [88]

$$I_D \sim e^{-e(U_G - U_T)/k_B T}, \quad (2.23)$$

and is important for the characterization of switching behaviour between the regions where the channel conducts and where it does not.

In the linear region the I_D has, as the name suggests, a linear dependence on the U_G , whereas in the saturation region the dependence is quadratic. The U_T , as characterized in eq. 2.22, can now be easily measured both in linear and saturation region, through measurements of the I_D at different U_G voltages while keeping the U_D fixed. In the linear region, the I_D is plotted against the U_G , and the linear extrapolation of the slope

⁸This holds in the first approximation of the derivation. However, a reduced channel length has an influence on the I_D , and in reality I_D still increases with U_G .

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to $I_D = 0 \mu\text{A}$ yields the U_T shifted by the $U_D/2$. The same can be achieved in the saturation region, with the difference of plotting the $\sqrt{I_D}$ in dependence of U_G . The $I_D = 0 \mu\text{A}$ point of the linear extrapolation now directly yields the U_T .

3 DePFET sensor

An overview of the depleted p-channel field effect transistor (DePFET) type of a silicon (Si) semiconductor radiation sensor will be presented in this chapter.

The DePFET radiation sensor was proposed in 1987 by J. Kemmer and G. Lutz [97]. Currently, the DePFET's are manufactured exclusively at HLL MPG. In addition to manufacturing, the HLL MPG also takes care of the designs, so that the DePFETs are tailored to the specific requirements of an experiment. As the manufacturing process is substantially more complex, transfer of the technology to commercial vendors was not yet successful, although tried [98]. Consequently, they are not readily available, but require a certain time buffer before they can be delivered. The size of the buffer depends on the scale and complexity of the project. Nevertheless, the DePFETs have been a part of a variety of successful projects:

- The BepiColombo mission from the European Space Agency (ESA) [99] that employs the DePFET based MIXS instrument for imaging of the fluorescent X-ray emissions from the surface of Mercury in the energy range from 0.5 keV to 7.5 keV [100].
- The SCS and SQS instruments at the European X-ray Free-Electron Laser (EU XFEL) [101] which utilize the DePFET based sensors with signal compression (DSSC) to record the X-rays from 0.5 keV to 10 keV at the frequency of 4.5 MHz with the ability to count single photon events as well as events consisting of multiple thousand photons at once [102, 103].
- The Belle II project at the High Energy Accelerator Research Organization (KEK) [104] which is using the DePFET based PXD instrument to precisely reconstruct the vertices and track ionising particles in the vicinity of the interaction point in a high luminosity environment of the SuperKEKB collider [105].

In addition to the EDET DH80k project, other projects that will include DePFET sensors are:

- The ESA's ATHENA mission that is planned to launch to space in 2031 [106]. It will include a DePFET based WFI instrument for an X-ray spectroscopy over an energy range of 0.2 keV to 15 keV, at a near Fano-limit energy resolution (sec 3.2.1) [107, 108].
- The DANAE project is planned to look for dark matter particles on a MeV energy scale through their direct detection in the Si bulk. It will employ repetitive non-destructive readout DePFETs with which a sub- e^- root mean square readout noise can be achieved [109, 110].

3.1 DePFET structure

To maximize the amount of generated e^-/h^+ pairs by the passing ionizing radiation (such as electrons, protons, pions), or to increase the detection probability for a single interaction particles like photons, the Si bulk has to be depleted. The e^-/h^+ pairs generated in the depleted Si bulk get separated by the electric field (\mathcal{E}) and they drift along the field lines to either a potential minimum, readout node, or a highly doped region where they are effectively removed from the system. To create an operational sensor, one needs to be able to measure the amount of e^-/h^+ pairs that were generated in the first place.

What was conveniently left out in the previous section on the topic of MOSFETs is that their drain current (I_D) characteristics do not only depend on the gate (U_G), source (U_S) and drain (U_D) voltage, but also on the biasing of the Si bulk (U_B). As the U_B is usually fixed, it does not change the I_D . However, if the e^- generated in the Si bulk would be collected in a potential minimum below the gate of a p-channel MOSFET, they would change the potential in the vicinity of the channel. Consequently, they would also modulate the I_D . In essence, this is how a DePFET structure non-destructively determines the amount of generated e^-/h^+ pairs. As only e^- , of the generated e^-/h^+ pairs, are used to modulate the I_D , the term *signal e^-* will be used hereinafter.

Essentially, a DePFET is a combination of two adjacent structures that are built on a fully depleted Si bulk (Fig. 3.1). The first structure is very similar to the MOSFET structure (sec. 2.3), with one key difference: it has an additional doping variation in the Si bulk, so that a potential minimum for e^- generated in the Si bulk is formed below the gate structure, namely a charge storage region. This minimum is called an internal gate (IG), because the e^- that are collected in it modulate the I_D much like the (external) gate does. Consequently, the DePFET structure acts as a first stage amplifier that is implemented directly on the sensitive volume. Two big benefits of this design are the preservation of the sensed signal e^- , and a very good signal to noise performance due to the minimized input capacitance.

The second structure is a so-called clear structure. It comprises of the highly doped n^+ clear implant and of the clear gate (CG). It operates like an n-channel MOSFET with the clear implant as drain, the previously described IG as source, and the CG controlling the connection between the two. By turning this transistor ON at a specific time, by applying the correct CG (U_{CG}) and clear (U_C) voltages, e^- can be removed from their potential minimum in the IG on demand. However, when the removal of e^- is unwanted, namely the OFF state of this transistor, the highly doped clear implant can cause two kinds of problems, that depend on the U_C . When biasing is too negative it can emit e^- to the IG (so-called back-emission), and when biasing is too positive it can lead to the loss of signal e^- . To circumvent this problem, a potential barrier below the clear implantation is needed. This is achieved by an additional implantation – a so-called deep p region below the clear contact. When depleted, that implant provides the negative space charge which in turn generates a potential barrier for e^- . Consequently, the probability for the loss of signal e^- is reduced, and the back-emission of e^- to the IG is suppressed. More on the biasing conditions will be explained in sec. 3.1.2.

3.1 DePFET structure

The pixel size DePFETs can vary over multiple orders of magnitude, from the smallest $500 \mu\text{m}^2/\text{pixel}$ [111], up to $10 \text{mm}^2/\text{pixel}$ [112], all depending on project requirements. In addition to that, sideways or punch-through depletion enable the backside of the DePFET to be completely unstructured, resulting in a 100% fill factor. As such, there is no unnecessary scattering events of the incoming radiation occur when irradiating from that side. One thing needed on the backside of the Si bulk is a highly doped p-type implantation, used to deplete the Si bulk. This implantation can be made very thin, in order to reduce the depth where signal charge can be lost, and consequently achieve a high quantum efficiency.

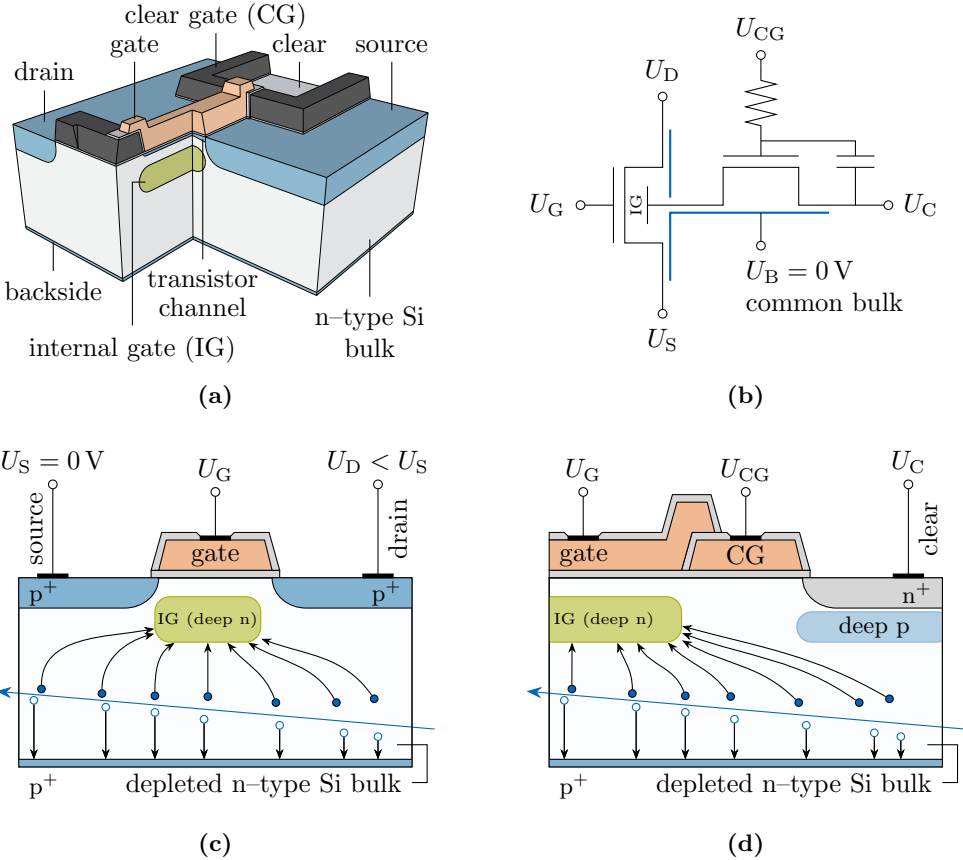


Figure 3.1: A simplified DePFET structure in the three-dimensional representation (a) and its equivalent electrical circuit (b). Additionally, the cuts along the transistor channel in the length L dimension (c) and the width W dimension (d) are shown. The cuts also show a charged ionising particle traversing the Si bulk, where the generated e^-/h^+ pairs are collected in their respective potential minimums, as indicated with the arrows.

A common way to operate a DePFET structure like the one presented in Fig. 3.1, is to statically bias the source (U_S), drain (U_D) and bulk (U_B) nodes. Additionally, the node used to deplete the Si bulk (either through the sideways depletion or punch-through depletion) is also biased statically. The biasing of the CG (U_{CG}) depends on the design of the DePFET. It can either be statically biased or dynamically switched between the two static voltages $U_{CG}^{ON} \leftrightarrow U_{CG}^{OFF}$. The gate (U_G) and clear (U_C) are, however, always dynamically switched between their own two static voltages. The U_G can therefore be set to U_G^{ON} or U_G^{OFF} , and the U_C to the U_C^{ON} or U_C^{OFF} . The ON index denotes the state in which the corresponding transistor channel conducts, and the OFF denotes the state where it does not conduct. As the DePFETs produced in the scope of the EDET DH80k project have a statically biased CG, the four operational modes achieved by different biasing states of the gate and clear structures will be further described in sec. 3.1.2.

Charge storage region(s) In order to understand how the charge storage region is formed one needs to look into the manufacturing process of DePFETs. The complete process has a multitude of steps and is beyond the scope of this thesis. However, a simplified overview will be given in order to grasp the basics. To generate a charge storage region in a DePFETs three different implantations are used: the medium-dose deep n implantation (MDDN), the high-dose shallow p implantation (HDSP1) and the low-dose shallow p implantation (LDSP). The low and medium-dose implantations can be fully depleted, whereas the ones with the high-dose cannot. Consequently, regions with the former two implantations leave behind charged regions with stationary ion charges, and in locations of the latter implantations, the majority charge carriers exist. The second implication the dose level has, is its influence on the depth of the implantation itself. Despite the depth of both the HDSP1 and the LDSP is marked as shallow, the high-dose of the former causes it to diffuse deeper into the Si than the latter. All this is important as the three implantations are implanted on more or less the same area and in effect they partially compensate each other.

The simplified manufacturing sequence is as follows. Initially, the first poly-Si layer, that forms the CG, is structured on the Si bulk. Afterwards, the MDDN and the LDSP are implanted. The former is implanted in the regions that will later be denoted with source, drain and gate, and is used as a base for the charge storage region(s). That is because this implantation, when depleted, leaves behind the positive space charge in form of stationary ions, which act attractively for the e^- . The latter, however, is placed everywhere but where the clear implantation will be located, and is used to adjust the DePFET's threshold voltage to the vicinity of 0 V.¹ Partial compensation between the two implantations pushes the charge storage region(s) deeper in the Si bulk, as the negative space charges from the LDSP implantation partially compensate the space charges from the MDDN close to the surface. Now, the second poly-Si layer that forms the gate is structured, and the HDSP1 is implanted over the same area as the MDDN.

¹This is needed as the positive potential caused by the stationary ion charges of the depleted MDDN would shift the U_T towards a very negative potential (~ -6 V in case of the EDET DH80k [113]). Negative stationary charges of the depleted LDSP are used to screen this potential so that the U_T is around 0 V.

Implanting the HDSP1 through the gate structure has two consequences. Firstly, the gate structure acts as a self-aligned mask for the implanting ions which in turn create two separate p^+ regions, that form the source and drain. Secondly, the MDDN region below the gate is not compensated with the HDSP1, and it remains attractive for e^- generated in the Si bulk. The region below the gate is usually referred to as the IG. The amount of e^- that can be stored in it depends on the area of the gate, the potential distribution in the Si bulk below the gate, drain and source, and the applied voltages to the source and drain. Common DePFET implantation parameters are chosen so that:

- The empty charge storage region below the gate, namely the IG, is at a potential of 3 V to 5 V.
- The region below source, commonly biased at 0 V, is more negative than the IG at around 1 V.
- The region below drain is even more negative than the one beneath the source, as the drain is biased negatively with respect to the source.

The dimensions of pixels are usually limited with the project requirements. Therefore, the charge handling capacity of the IG, i.e., the maximum amount of e^- that can be stored in the IG, cannot be arbitrarily scaled through gate dimensions. Ergo, it has to be done through the change in implantation parameters or implantations themselves. Since the potential below the source is still positive, one possible way is through the additional charge storage region below it. This can be implemented through a change in implantations.

To generate a second charge storage region, two implantations for the source are necessary: the already known HDSP1 and the second high-dose shallow p implantation (HDSP2). Despite having very similar names and implantation parameters, the exact implantation process of the HDSP2 is changed so that it results in a much shallower depth. Consequently, the HDSP2 partially compensates a much smaller fraction of the MDDN as the HDSP1. This can be seen in Fig. 3.2. The potential of this second charge storage region is therefore between the IG potential and the potential caused by HDSP1

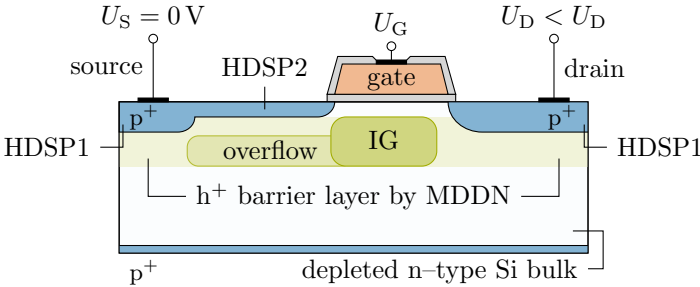


Figure 3.2: Formation of the overflow region below the source through the use of multiple implantations for the source. The stationary ion charges of the MDDN region around the overflow and IG regions form the potential barrier for h^+ that prevents them from drifting towards the backside p^+ implantation.

implantation – usually at 2 V to 3 V. Consequently, the e^- first completely fill the IG, and afterwards overflow to the second charge storage region – hence the name overflow region. In addition to the increased charge handling capacity, the overflow region brings additional implications. One of them is a different strength in the current modulation, see sec. 3.1.1, which results in a non-linear amplification of the collected e^- .

3.1.1 Current modulation

The usual derivation of the DePFET set of equations for the modulation of the I_D current follows ref. [96]. It corrects the equations obtained in sec. 2.3.1 by doing the transformation

$$U_{G, \text{eff}} \rightarrow f \frac{Q_{\text{SIG}}}{C_G} + U_{G, \text{eff}},$$

where fQ_{SIG}/C_G essentially represents a change in the gate potential. The reasoning behind this is that the e^- collected in the IG (Q_{SIG}) induce a mirror charge in all neighbouring conductors (for instance drain, source and channel). The sum of mirror charges is equal to Q_{SIG} but of opposite charge. A fraction f of the Q_{SIG} , that is induced in the channel, can be mirrored again to the gate over the gate–channel capacitance (C_G) which equals WLC_{OX} . The W and L are respectively the gate width and length dimensions, and the C_{OX} is the oxide sheet capacitance.

The only change that can be measured is the change in I_D . Consequently, under the assumption that the induced charge is equally spread over the channel, the same amount can be generated by varying the U_G , and the above transformation makes sense.

For the saturation mode of operation this yields

$$I_{D, \text{sat}} = -\frac{W}{L}\mu_h C_{\text{OX}} \frac{1}{2} \left(f \frac{Q_{\text{SIG}}}{C_G} + U_{G, \text{eff}} \right)^2, \quad (3.1)$$

and the $I_{D, \text{sat}}$ has two dependencies. The dependency on the U_G , characterised as an amplification of the gate (transconductance)

$$g_m = \frac{\partial I_{D, \text{sat}}}{\partial U_G} = -\frac{W}{L}\mu_h C_{\text{OX}} \left(f \frac{Q_{\text{SIG}}}{C_G} + U_{G, \text{eff}} \right) = \sqrt{\frac{2W\mu_h C_{\text{OX}}}{L}} \|I_{D, \text{sat}}\|, \quad (3.2)$$

and the dependency on the collected charge in the IG, characterised as an amplification of the internal gate

$$g_q = \frac{\partial I_{D, \text{sat}}}{\partial Q_{\text{SIG}}} = -\frac{1}{L^2}\mu_h f \left(f \frac{Q_{\text{SIG}}}{C_G} + U_{G, \text{eff}} \right) = f \sqrt{\frac{2\mu_h}{WL^3 C_{\text{OX}}}} \|I_{D, \text{sat}}\|, \quad (3.3)$$

The g_q represents the charge amplification of a DePFET in the units of pA/e^- , and every e^- collected in the IG modifies the I_D by this amount. However, the problem with the above equations is that they show the quadratic dependence of the $I_{D, \text{sat}}$ on the signal charge collected in the IG, and the square of the fraction factor f in the g_q . No measurement so far supported the described behaviour [113].

An alternative model was recently proposed by R. Richter [114]. In it, the I_D is considered as a superposition of the offset current I_{OFFS} (standard MOSFET current steered by the gate, eq. 2.22) and the signal current I_{SIG} influenced by the charge in the IG:

$$I_D = I_{\text{OFFS}} + I_{\text{SIG}} = I_{\text{OFFS}} + g'_q Q_{\text{SIG}} . \quad (3.4)$$

The g'_q in this case represents a charge amplification factor in terms of frequency. If there would be a single e^- collected in the IG, that would induce a mirror charge – a h^+ – only in the channel, the g_q would depend solely on the transit time τ of that h^+ between the source and drain

$$g'_q = \frac{1}{\tau} = \frac{v_h}{L} = \frac{\mu_h \mathcal{E}_y}{L} . \quad (3.5)$$

However, due to stray capacitances to other conductors, only a fraction $f < 1$ of the mirror charge is induced in the channel. For the saturation mode of operation it can be written that the electric field in the channel \mathcal{E}_y is proportional to the $L^{-1}U_{G, \text{eff}}$, due to the channel pinch-off effect.² The final, corrected amplification factor in terms of frequency is therefore

$$g'_{q, \text{corr}} = \frac{f \mu_h U_{G, \text{eff}}}{L^2} . \quad (3.6)$$

In order to obtain the previously known charge amplification factor in units of pA/e^- , the $g'_{q, \text{corr}}$ needs to be multiplied by $1 = 1.6 \cdot 10^{-19} \text{As}/e^-$.

The appropriate model, where the discrepancies between measurements and theory are corrected, is therefore

$$\begin{aligned} I_{D, \text{sat}} &= -\frac{1}{2} \frac{W}{L} \mu_h C_{\text{OX}} U_{G, \text{eff}}^2 + g'_{q, \text{corr}} Q_{\text{SIG}} \\ &= -\frac{1}{2} \frac{W}{L} \mu_h C_{\text{OX}} U_{G, \text{eff}}^2 + f \sqrt{\frac{2\mu_h}{WL^3 C_{\text{OX}}}} \|I_{D, \text{sat}}\| Q_{\text{SIG}} . \end{aligned} \quad (3.7)$$

In case of additional charge storage regions located below the source, the I_{SIG} can be split to multiple contributions. The first contribution from the e^- in the IG remains as described above, whereas the contribution from the e^- in the overflow region is offset by a different factor $f_{\text{OF}} < f < 1$. The assumption that most electric field lines from e^- collected in the overflow region end up in the channel is not valid any more, as the stray capacitance of the overflow region to the source is bigger than that of the IG region. Consequently, the charge amplification of e^- collected in the overflow region is smaller. In the approximation it can be characterised as the capacitive divider

$$f_{\text{OF}} = \frac{C_{\text{CSR-ch}}}{C_{\text{CSR-ch}} + C_{\text{CSR-S}}} , \quad (3.8)$$

²In general the pinch-off effect also depends on the insulator thickness, and the \mathcal{E}_y should be corrected with a factor k .

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where the $C_{CSR\text{-ch}}$ and $C_{CSR\text{-S}}$ are respective stray capacitances of both charge storage regions (overflow and IG) to the DePFET channel and the source.

The response of a DePFET with two storage regions to the collected e^- is presented in Fig. 3.3. The gate is biased in such a way that the I_{OFFS} , which is I_D when the charge storage regions are completely empty, equals $100\ \mu\text{A}$.

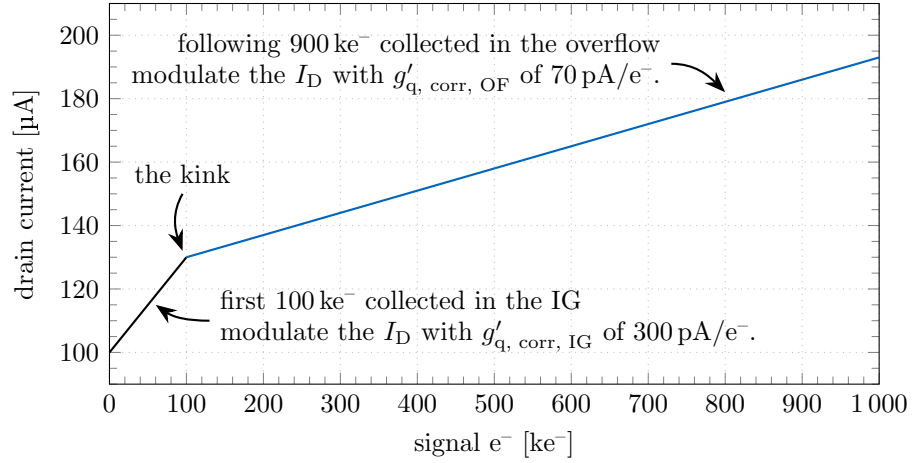


Figure 3.3: Non-linear response of a DePFET with two storage regions. The I_{OFFS} is tuned to $100\ \mu\text{A}$ by the appropriate gate voltage. The kink denotes the point at which the IG is full and all further e^- are collected in the overflow region.

3.1.2 Operating conditions

The DePFETs offer a non-destructive readout of the e^- collected in charge storage regions, with an on-demand removal of those e^- . This is achieved by applying different biasing conditions to the two adjacent structures forming the DePFET. A common way is to switch a single voltage, between two values, on each structure.³ Therefore, each of the two structures essentially has two eigenstates – the ON and the OFF state. Consequently, there exist four states the DePFET pixel, as described in this chapter, can be put in. All of them are presented in Fig. 3.4. The first structure – the MOSFET part – is controlled by the U_G , and the second structure – the clear part – is controlled by the U_C with the U_{CG} regulating the potential barrier for e^- between the charge storage regions and clear implantation.

Collection mode (Fig. 3.4a) The collection mode is used whenever it is desired to collect the e^- , generated in the Si bulk, in the charge storage regions. In that mode both DePFET structures are in their OFF states, and the global minimum for e^- generated in the Si bulk is in the IG. For the MOSFET structure this means that the U_G^{OFF} is more positive than the threshold voltage (U_T) in order to suppress the current between source

³In some use cases more than one voltage was selectively switched on the clear structure.

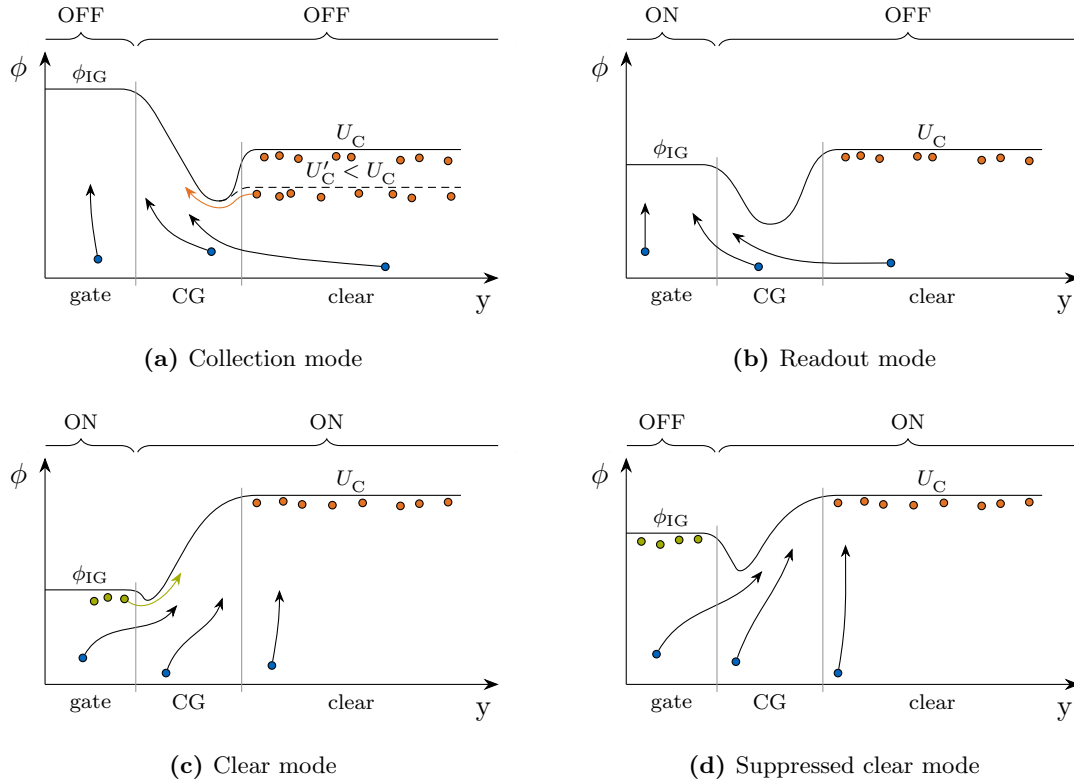


Figure 3.4: Four operational modes of DePFET pixels. \bullet are the e^- generated in Si bulk with arrows indicating the drift direction. \circ are the majority charge carriers of a non-depleted n^+ clear implantation. Orange arrow in (a) depicts the possible back-emission of \circ to the IG in case of poorly biased U_C or U_{CG} . \circ are the e^- collected in the IG. Those e^- stay there until the DePFET is put to the clear mode and they are cleared away, as shown with the green arrow on (c). The ϕ_{IG} denotes the IG potential, and OFF/ON labels show the state of the corresponding structure.

and drain. That way the IG potential (ϕ_{IG}) is coupled to the U_G^{OFF} , and through it raised to a more positive value. The clear structure has to be biased in a way that U_C^{OFF} is close to U_S , and U_{CG} needs to be more negative than U_C^{OFF} . The limiting conditions on the U_C^{OFF} are:

- A too positive voltage can overcompensate the potential barrier formed by the negative space charge from the deep p implantation and thus cause the loss of signal e^- to the clear implant.
- A too negative voltage can in extreme cases open a current path between clear and source nodes (forward biased pn-junction) and in a less extreme case (dashed line, Fig. 3.4a) causes a back-emission of e^- from the clear to the IG (orange arrow, Fig. 3.4a).

The limiting conditions on the U_{CG} are:

- The U_{CG} voltage too close to that of the U_C^{OFF} (or even higher) generates a weak (or non-existing) potential barrier between the IG and the clear. Consequently, the e^- from the clear can overcome it and be collected in the IG (back-emission).
- A too negative U_{CG} can in turn generate an inversion layer below the CG, and open up a parasitic current path between the source and drain. The level of this current is no longer controlled by the gate.

The benefit of this mode is that it efficiently collects e^- in DePFET's charge storage regions with almost no power consumption. Consequently, large area integration detectors with low power consumption and sequential readout can be built.

Readout mode (Fig. 3.4b)

The readout mode is applied when it is desired to non-destructively readout the amount of e^- collected in charge storage regions. In that mode the status of the clear structure remains unchanged. The gate voltage, however, is changed to a specific predetermined U_G^{ON} that is more negative than U_T , so that a predetermined offset current (I_{OFFS}) flows between the source and the drain. The I_{OFFS} is determined in the state, where there is no e^- in the IG, and is usually in the range of 100 μA . Due to the current flow, the ϕ_{IG} is decoupled from the U_G^{ON} and is at the predetermined level set by the implantation parameters. With the correctly set U_C^{OFF} the deep p implantation is preventing the loss of signal e^- , and in combination with the correctly set U_{CG} the back-emission of e^- is suppressed as well. This means that all e^- generated in the Si bulk are still collected in the charge storage regions.

Clear mode (Fig. 3.4c)

This mode is used to clear away e^- collected in the charge storage regions from the previous two modes of operation. The clearing process happens by switching the U_C to a more positive U_C^{ON} when the gate is in the U_G^{ON} state. Usual step in the clear voltage ($\Delta U_C = U_C^{\text{ON}} - U_C^{\text{OFF}}$) needed for the complete removal of collected e^- is in the range of 10 V to 15 V, depending on the design parameters. The ON state of the MOSFET structure is needed because the ϕ_{IG} is lower, and consequently the collected e^- are less tightly bound in the IG. However, despite the new global minimum for e^- generated in the Si bulk, i.e., the clear contact, the collected e^- still need to overcome the potential barrier set by the CG. As this would require long clear times, or even cause incomplete removal of collected e^- , it is necessary to reduce it. This can be done in two ways, either by increasing the U_C^{ON} to a very positive voltage or by varying the U_{CG} . The former way is possible, but limited with the break-down fields on the border between CG and clear implantations. The latter option can be implemented by separately changing the U_{CG} voltage or by the so-called AC capacitive coupling of the CG to the clear (Fig. 3.1b). The step in clear voltage ΔU_C is consequently represented on the CG as well

$$\Delta U_{CG} = \Delta U_C \frac{C_{C-CG}}{\sum_i C_{C-i}}. \quad (3.9)$$

The C_{C-CG} represents the capacitive coupling between clear and CG, and the $\sum_i C_{C-i}$ is the sum of all other capacitive couplings of the clear including that of the CG (e.g., source, drain, gate, backside). The limiting conditions on the U_C^{ON} are:

- A voltage too close to that of the U_C^{OFF} can result in the too small ΔU_{CG} . Consequently, the CG barrier is not weakened enough to remove all collected e^- .
- A too positive voltage can lead to high electric fields on the border between the clear implantation and the CG. In extreme cases this can lead to break-down effects caused by impact ionization.

Suppressed clear mode (Fig. 3.4d) If, for some reason, the collection of e^- must be paused, the DePFET can be put in the suppressed clear mode. That way the already collected e^- remain in the charge storage regions, whereas the newly generated e^- in the Si bulk drift straight to the clear. This mode is for example needed in the Belle II Pixel Detector after the injection of highly energetic e^- into the storage rings [115]. It is achieved by applying the U_C^{ON} to the clear node while the MOSFET structure is in the OFF state. Despite the temporary lowering of the CG barrier, the already collected e^- stay in the charge storage regions as they are much more tightly bound in them due to the more positive U_G . The detailed investigation of this mode is presented in ref. [116].

3.1.3 Array operation

As already stated, a single DePFET structure, as presented in this section, can cover an area from $500 \mu\text{m}^2$ to 10mm^2 . However, in order to cover a larger area it is possible to build multiple DePFET pixels side by side, and connect them in an array. The biggest DePFET array built until now cover an area of $66 \text{mm} \times 66 \text{mm}$ with 512×512 pixels in it [117]. In addition to covering a bigger area, a structure like this also offers a 2D event reconstruction. When a charged particle traverses the array it leaves a cloud of e^-/h^+ pairs in it. The signal e^- drift towards their closest charge storage region. By finding the pixel, or pixels, where they were collected, a pixelated position of particle's trajectory can be determined. The resolution of such reconstruction in each dimension is

$$\sigma_{\text{pix}} = \frac{a}{\sqrt{12}}, \quad (3.10)$$

where a represents the pixel dimension, and the $\sqrt{12}$ factor is derived from the assumption of the uniform detection probability over the complete pixel. This resolution can be improved by making the pixels small enough, so that a signal e^- are shared over more pixels. From here, the precise location can be calculated by the means of the weighted average.

An electrical example of such structure is presented in Fig. 3.5, where $N \times M$ DePFETs are connected together. To connect every pixel, two aluminium layers on the frontside of the array are used in the production. The static voltages are shared over all pixels in the array, for instance, source implantations from all pixels are connected to the same electrical line, and the same is true for the CG structures. If the same were true for the gate, clear and drain contacts of each pixel, the whole array would behave as a single pixel. Therefore, a special connection scheme is employed for those contacts. All gate (clear) nodes from a single row are connected together to a switching circuitry, which on

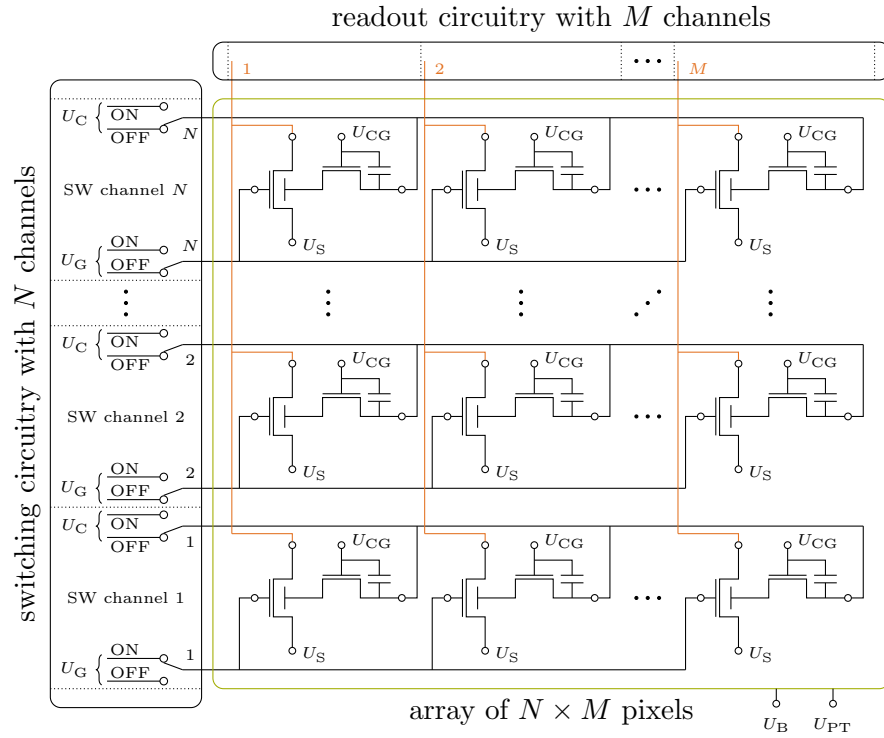


Figure 3.5: An array of DePFET pixels consisting of N rows and M columns built on a common Si bulk. The switching circuitry with N channels on the left, is controlling the gate and clear voltages. Only one channel can be activated at the time. The readout circuitry reads the outputs of all M activated pixels in parallel. Named nodes, kept at static voltages, are for simplicity not connected together with lines.

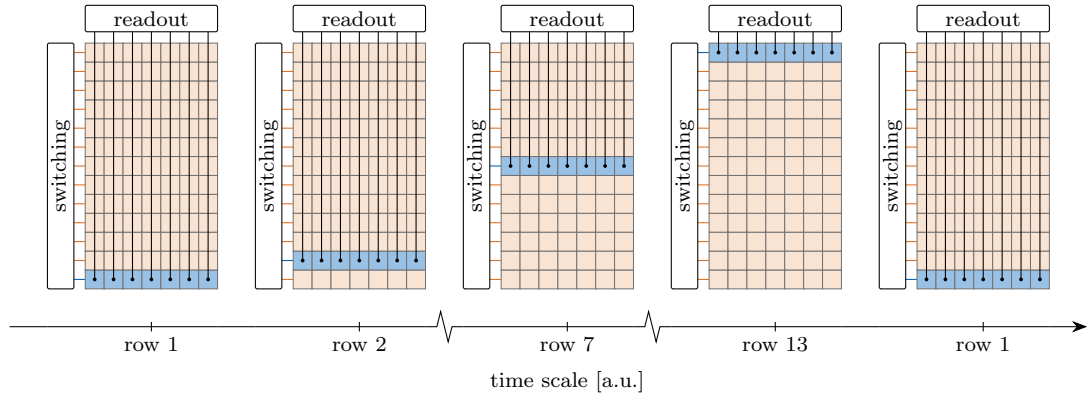


Figure 3.6: Graphical representation of the rolling shutter readout mode. One row is in the readout mode (blue colour) and all of the pixels from it are readout at the same time. The rest of the array is in collection mode (orange colour). The x axis represents the steps in the time domain of a single full frame readout procedure.

demand switches the gate (clear) voltage between OFF and ON states.⁴ Therefore, when a single gate switch of the switching circuitry is turned ON, all DePFETs connected to it simultaneously start conducting the current. Consequently, the outputs of all those DePFETs must be measured at the same time. This is achieved by connecting together the drain nodes of all DePFETs in the same column. The described readout procedure is the so-called column-parallel row-wise rolling shutter mode. In it, a single row of DePFETs is activated, measured and afterwards cleared, before the process is repeated in the next row. The time necessary for a complete readout is therefore the amount of rows (N) times the time it takes to measure a single row (t_0). The t_0 can range from as little as 100 ns up to multiple μ s, all depending on the project requirements. The graphical representation of the described rolling shutter readout mode is presented in Fig. 3.6.

The connections to the structures that are common to all DePFETs in the array are implemented on the edges of the array. Those are for example the contacts to fix the bulk potential (U_B) and deplete the sensitive volume through punch-through method (U_{PT}).

To cope with the high density of the arrays, the switching circuitry is usually integrated on a dedicated control application-specific integrated circuits (ASICs), that need to be able to drive relatively high voltages, most common types of which are the SwitcherS [118] and SwitcherB [87] ASICs.

3.1.4 Readout

Two well established readout modes of DePFETs are the so-called drain current readout mode and source follower mode. As the former is implemented on the EDET DH80k sensors, it will be further discussed in this work. For the latter method, the description can be found in ref. [118].

In a drain current readout, the U_S , U_D and U_G^{ON} are kept constant when the DePFET is in the readout mode of operation (sec. 3.1.2). Consequently, the drain current of a DePFET pixel depends only on the amount of charge collected in the storage regions (Q_{SIG}), as described in sec. 3.1.1. By measuring the drain current it is possible to determine the Q_{SIG} . Two DePFET readout ASICs exist that perform this measurement on multiple channels in parallel, specifically VERITAS ASIC [119] and DCD ASIC [84, 85]. By omitting the timing and noise properties, a pre-requirement for the use of the already available readout ASICs is that the input dynamic range of a selected readout ASIC fits the output range of the DePFET's signal current.

In essence, a circuit like the one presented in Fig. 3.7 is used to convert the change in the current to the change in voltage. The U_D is fixed by the operational amplifier (OpAMP), and the drain current (I_D) originating from the DePFET is a superposition of the offset current (I_{OFFS}) and the signal current (I_{SIG}). The first contribution gets subtracted by the subtraction part of the circuitry, comprising of a resistor (R_{SUB}) and a correctly applied subtraction voltage (U_{SUB}). In other words, to subtract I_{OFFS} of

⁴The same is true for the CG node in some implementations of the DePFET structure.

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100 μA one can use a 10 k Ω subtraction resistor with the U_{SUB} being 1 V more negative than the U_{D} (Ohm's law). After this, the OpAMP needs to compensate only the I_{SIG} in order to keep the voltage at drain side constant. It does so by sourcing the current through the feedback loop by changing of the output voltage (U_{OUT})

$$U_{\text{OUT}} = \left[I_{\text{D}} - \frac{U_{\text{SUB}} - U_{\text{D}}}{R_{\text{SUB}}} \right] R_{\text{F}} . \quad (3.11)$$

The feedback resistor (R_{F}) and capacitor (C_{F}) influence the secondary gain, time constant and stability, and have to be chosen accordingly to the specifications of the OpAMP. The change of the U_{OUT} can now be tracked by the use of commercially available analogue-to-digital converters (ADCs).

Signal determination Different methods can be used to determine the signal level. The two commonly used are the correlated double sampling (CDS) and the single sampling (SS). The former will be widely used in device testing throughout this thesis, whereas the latter will be used in the EDET DH80k camera.

The CDS is graphically presented in Fig. 3.8. The bottom plot shows the ADC values as obtained through the circuitry presented in Fig. 3.7 in a continuous sampling mode.⁵ Those values are linearly proportional to the DePFET's I_{D} , and in turn to the amount of e^{-} collected in the charge storage region(s). The ADC values are integrated for a specific amount of time before ($t_{1^{\text{st}} \text{ INT}}$) and after ($t_{2^{\text{nd}} \text{ INT}}$) the clear pulse, with the settling time (t_{settling}) in-between. The signal level is determined as a difference between the two integrations. If there was some amount of e^{-} stored in the charge storage regions, the result from the first integration ($S_{1^{\text{st}} \text{ INT}}$) is higher than that of the second integration ($S_{2^{\text{nd}} \text{ INT}}$) when the charge storage regions are ideally empty.

The time duration of such procedure is determined as the

$$t_{\text{CDS}} = t_{1^{\text{st}} \text{ INT}} + t_{\text{settling}} + t_{2^{\text{nd}} \text{ INT}} .$$

At a minimum, a single point has to be measured before and after the clear pulse in order to determine the signal level

$$S_{\text{CDS}} = S_{1^{\text{st}} \text{ INT}} - S_{2^{\text{nd}} \text{ INT}} .$$

In case one needs to reduce the readout time by using the same OpAMP, the only way is to switch to the SS. That way the $t_{2^{\text{nd}} \text{ INT}}$ is removed and the duration is reduced to the

$$t_{\text{SS}} = t_{1^{\text{st}} \text{ INT}} + t_{\text{settling}} .$$

In order to determine the signal level in this mode it is necessary to measure the I_{D} of an empty DePFET in advance. This is done under controlled conditions prior to the

⁵The maximum amount of points in a given time is directly connected to the maximum sampling rate that the ADC can offer.

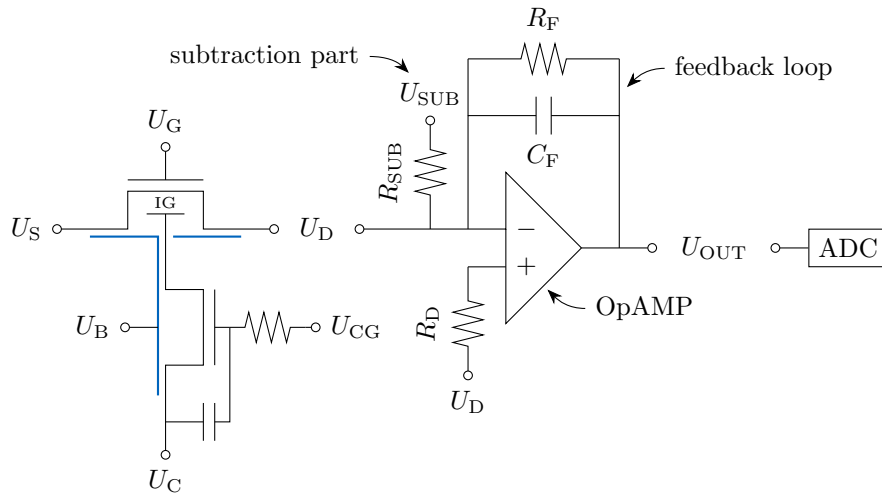


Figure 3.7: Simplified circuitry used to convert the change in drain current, originating from the DePFET, to the change in voltage, that can be digitized with a commercial ADC.

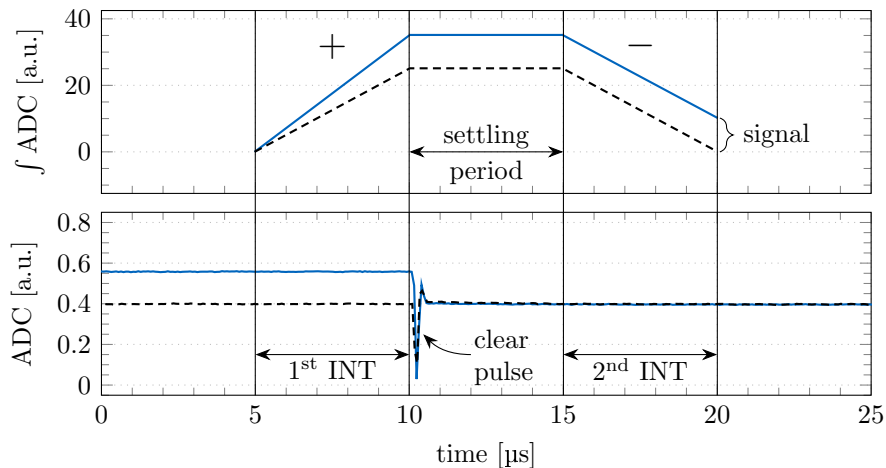


Figure 3.8: The lower plot shows the measured ADC value of the U_{OUT} that is linearly proportional to the I_D ; with (—) and without (----) signal e^- in the charge storage regions. The upper plot shows the output from the correlated double sampling of the two signals presented in the lower plot. The difference between the two integrations is the signal.

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actual use of the sensor. When it is certain that no charge was generated in the Si bulk by ionizing radiation, a multitude of integrations (S_{empty}) are performed to obtain their distribution. As it is a normal distribution, its mean value ($\langle S_{\text{empty}} \rangle$) is taken as the base for the I_{OFFS} . The signal level is consequently determined as

$$S_{SS} = S_{1^{\text{st}} \text{ INT}} - \langle S_{\text{empty}} \rangle.$$

In this mode it is imperative that the I_{OFFS} is stable and does not fluctuate with time.

The usual trade-off of the two methods is speed versus noise. The CDS offers a noise suppression for low frequency contributions (sec. 3.2) but is slower. On the other hand, the SS can be much faster but is also more susceptible to noise that the previous method suppresses.

The problem of the above readout methods is that the DePFET in readout mode still collects the e^- in its charge storage regions. Consequently, the I_D can change during the integration period and an incorrect signal level is measured. The following case is true for both readout methods. If the e^- arrive to the charge storage regions during the $t_{1^{\text{st}} \text{ INT}}$ they are incorrectly integrated. This results in the $S' = f_1 S$, where $1 \geq f_1 \geq 0$. 1 denotes the e^- arriving at or before the start of integration, and 0 at or after the end. The other possibility, valid only for the CDS method, is the arrival of e^- during the $t_{2^{\text{nd}} \text{ INT}}$. This results in the negative measured signal scaled with the f_2 for which the same rules apply as for the f_1 . Those two types of events are called misfits, and are presented on the CDS example in Fig. 3.9. The amount of misfits increases proportionally with the ratio of the total integration time and the time between two consecutive clear pulses. In the stroboscopic transmission electron microscopy applications the misfits can be completely

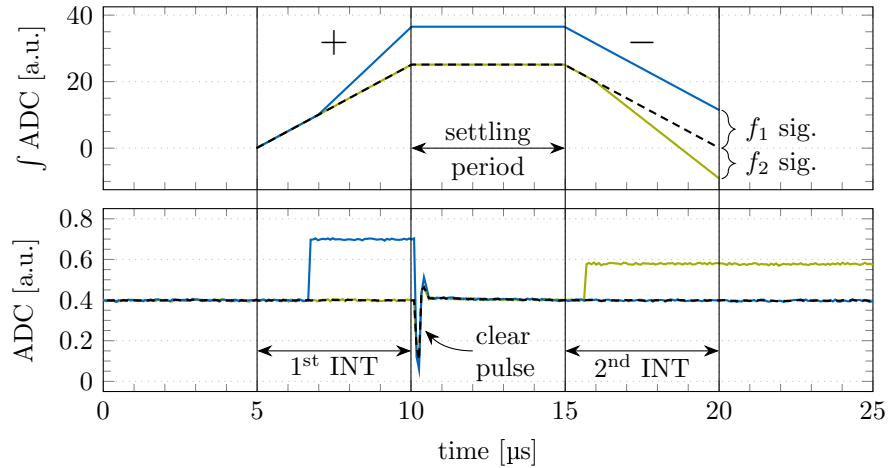


Figure 3.9: Incorrectly measured signal due to the signal e^- arriving to the charge storage regions during the 1st integration period (—) and 2nd integration period (—), in comparison to the empty charge storage regions (----). The upper plot shows the output from the correlated double sampling of the signals presented in the lower plot.

avoided with the appropriate synchronisation of the timing between the e^- emission and readout. However, for spectroscopic applications, where the timing cannot be controlled, the signal e^- arising from misfits are measured incorrectly, and consequently increase the background level of the recorded spectra.

3.2 Energy resolution

When illuminating the sensor with the test charge, calibration source or calibrated light pulse, the recorded integrated energy spectrum yields the distribution centred around the input energy. The energy resolution (R) of the system is defined as the full width at half maximum (FWHM) of the recorded peak centred around the input energy, divided by the input energy (E) [33]

$$R(E) = \frac{\text{FWHM}}{E}. \quad (3.12)$$

The noise contributions causing the spreading of the peak can be split in different categories. The first category can be set by the physical limits when particles hit the sensor. In case of e^- , the limits arise from variations in their energy, intensity and different interactions inside the Si (sec. 1.1), and in case of X-rays there is the Fano statistics [120]. Those are the noise sources that cannot be influenced by the sensor design. However, even with the removal of those influences one would still not receive a single delta function like peak at a given energy. The second group of noise sources that is due to the current fluctuations in the DePFET and in the readout system. This group is commonly named as electronic noise, and was first described by Schottky [121]. The total noise that limits the energy resolution is consequently the square root of all contributions summed in quadrature.

3.2.1 Fano noise

The Fano noise was first described by U. Fano in ref. [120]. He showed that when a fixed amount of energy is deposited in the sensor, the interaction processes that occur afterwards are not independent but correlated due to the limited amount of energy [33]. This means that the amount of produced signal in a sensor can vary due to the variation in the interaction processes. The contribution of this variation is included via the Fano factor (F) which encompasses all ionizing processes as well as processes that do not lead to charge generation but to the heating of the sensor, for instance phonon excitations. Consequently, this leads to the variation of the amount of e^-/h^+ pairs (eq. 2.4) that are produced by the same amount of radiation absorbed in the sensor. The variance is described as

$$\sigma_F^2 = F \frac{E_{\text{abs}}}{3.66 \text{ eV}}, \quad (3.13)$$

where F is an intrinsic constant of the detecting medium. In the case of Si close to room temperature it is measured to be 0.118 [122].

3 DePFET sensor

The Fano noise does not play a significant role in e^- imaging as the initial premise for the fixed amount of energy to be absorbed does not hold, essentially a contribution from the variance of Landau distribution generated from e^- passing through the sensor (sec. 1.1.3) is much greater than that of σ_F^2 . However, for the purpose of the sensor characterization characteristic X-rays will be used as well. With them, the Fano factor sets the ultimate achievable energy resolution for the DePFETs.

3.2.2 Electronic noise

There are multiple sources of noise in every electronic circuit and they cause the fluctuation of the signal ranging over a wide range of frequencies. The level of this noise is usually described by the equivalent noise charge (ENC) at the input node. This means that the measured root mean square noise is backward calculated to the amount of signal charges (Q_{SIG}) that would cause the same level of change in the signal. Consequently, the level of this noise depends on all stages used in the circuitry, from the DePFET itself, to the current voltage conversion circuitry, and in the end to the ADC used for the digitization

$$\begin{aligned} \text{ENC}^2 &= \text{ENC}_{\text{DePFET}}^2 + \text{ENC}_{\text{I-U conv}}^2 + \dots + \text{ENC}_{\text{ADC}}^2 \\ &\approx \text{ENC}_{\text{DePFET}}^2 + \text{ENC}_{\text{I-U conv}}^2 . \end{aligned}$$

From here it follows that it is important to design the circuitry in a way that the initial signal (Q_{SIG}) is amplified in the least amount of stages to levels beyond the noise level of following stages. For the DePFETs this usually means that the first two stages (built-in amplification plus the current to voltage conversion circuitry) are the dominating part in the ENC.

3.2.2.1 Fundamental contributions

The fundamental contributions to the ENC of the system can be written as [123, 124]

$$\text{ENC}_S^2 = \underbrace{\frac{1}{\tau} C_{\text{DET}}^2 a_1 A_1}_{\text{thermal}} + \underbrace{2\pi C_{\text{DET}}^2 a_2 A_2}_{1/f} + \underbrace{\tau a_3 A_3}_{\text{shot}} , \quad (3.14)$$

where τ is the integration time of the readout electronics and C_{DET} the capacitance of the detector. Different contributions of the noise densities are denoted with the a_i , and the corresponding shaping factors of the filtering functions for those contributions are denoted with A_i . The essentials of each noise density contributions will be described following ref. [96].

Thermal noise The Brownian motion of charge carriers in a conductor causes fluctuations in the current. Those fluctuations can be measured in terms of the noise current

(I_n) even without applied voltage difference. They only depend on the conductor's resistance (R) and its temperature (T), and their spectral density is given as

$$\frac{d\overline{I_n^2}}{df} = \frac{4k_B T}{R}, \quad (3.15)$$

where f denotes the frequency. Since the contribution is independent of f it follows a uniform distribution over the complete frequency spectrum. For the MOSFET channel the above eq. 3.15 is rewritten in accordance to the g_m of the channel ($1/R$ of the channel) as⁶

$$a_1 = \frac{d\overline{I_n^2}}{df} = 4k_B T g_m. \quad (3.16)$$

Low-frequency voltage noise The low-frequency voltage noise ($1/f$) cannot be calculated analytically as it depends on the geometry, technology and also operating parameters.⁷ It may originate from different reasons in different electronic elements. Consequently, it has to be measured for each circuitry separately. In general it has an approximate $1/f$ dependency as

$$\frac{d\overline{I_n^2}}{df} \propto \frac{A_n}{f^\alpha}, \quad \text{with } \alpha \approx 1. \quad (3.17)$$

Two models generally used to describe the $1/f$ noise of MOSFET transistors are the conduction fluctuation model and the number fluctuation model [109]. The former seeks the reason in the changes of the channel conductivity due to the carrier scattering on lattice vibrations, whereas the latter assumes changes in the number of carriers due to the defects in the crystal lattice that act as charge traps.

Shot noise This contribution has an origin in the quantized nature of the e^- charge. When a constant amount of charges flows through a boundary in pn-junction its fluctuation follows a Poisson distribution. Consequently, the mean-square variation of this current in a frequency spectrum equals

$$a_3 = \frac{d\overline{I_n^2}}{df} = 2I_L e. \quad (3.18)$$

In the case of the DePFETs the origin of this current is in lattice defects and impurities. They generate additional energy states either in the Si bulk or at its surface, through which the so-called leakage current (I_L) is generated. The amount of the I_L is heavily dependent on the sensor temperature and is in general halved for every 7°C of temperature reduction [109].

The shot noise in a DePFET can also originate from improper biasing conditions on the clear structure, as it can inject e^- to the Si bulk. However, this can be easily avoided with proper characterization studies.

⁶For a MOSFET with source and drain biased at the same voltage. Otherwise $g_m \rightarrow \gamma g_m$, where γ is a complex function of biasing and MOSFET parameters [115] according to ref. [125].

⁷Also holds for the a_2 as it is proportional to the $1/f$.

3.2.2.2 Other contributions

Other sources of noise can originate from the DePFET sensor itself, or from external influences.

Incomplete clear An incomplete removal of the e^- stored in the charge storage regions is one of the contribution originating from the DePFET. The reason for it can be a wrongly biased U_{CG} or U_C^{ON} , or a too short clear pulse duration. Either way the result is the same: a fixed amount of e^- is left in the IG. Although the average value of remaining e^- is constant and does not influence the measured Q_{SIG} , its variance fluctuates with Poisson's statistics and consequently contributes to the overall ENC. This noise contribution is comparable to the kTC noise [126] in e.g. CMOS or CCD sensors. However, under the correct biasing conditions it should not be present in DePFETs.

Leakage current In sec. 3.2.2.1 that follows refs. [123, 124], the ENC is derived for the time continuous readout. However, DePFET's feature the readout on demand. Consequently, another contribution has to be added to the overall ENC. In addition to the original leakage current noise, the thermally generated e^- that arrive to the charge storage regions in the time between two consecutive readouts (t_{EXP}) shift the drain current of the DePFET and increase the noise. The average number of e^- , arriving in a fixed time, is constant

$$\langle N_L \rangle = \frac{I_L t_{EXP}}{e},$$

but due to Poisson's distribution their statistical fluctuations follow the $\sqrt{\langle N_L \rangle}$. From here it follows that the overall ENC is

$$ENC^2 = ENC_S^2 + \left(\sqrt{\langle N_L \rangle} \right)^2 = ENC_S^2 + \frac{I_L t_{EXP}}{e}. \quad (3.19)$$

Common mode noise One of the external causes can be a so-called common mode noise. It is a low-frequency noise (~ 100 Hz) that causes shifts in the global power (or ground) supply lines. It can originate from multiple causes, some of them being:

- the so-called pick-up effect (e.g., coupling of the 50 Hz frequency from the electrical grid), or
- voltage level converters used to generate multiple voltages from a single 12 V supply line, or
- ground loops which cause the shifts of the referencing potential.

Consequently, it reveals itself in a frequency dependent I_D shift (I_{CM}) that is common for the complete electrical row currently in the readout mode. This creates a special challenge in the bright field transmission electron microscopy imaging with SS of the signal, as the common mode correction algorithms (CMCs) cannot be applied if all pixels in the readout mode have the I_{CM} superimposed to the sum of the I_{OFFS} and I_{SIG} .

From here it follows that the $I_{\text{SIG}} + I_{\text{CM}}$ is wrongly interpreted as the I_{SIG} . However, in the scope of this thesis CDS will be used as the drain readout method. With it, the additional I_{CM} contribution gets filtered away automatically.⁸

3.2.2.3 Readout contributions

By the appropriate choice or design of the OpAMP used in the current to voltage converter (sec. 3.1.4) its noise contribution can be much smaller than the thermal noise contributions of the associate resistors (R_{F} and R_{SUB}). Those, however, have to be chosen to match the expected signal from the DePFET to the dynamic range of the rest of the readout system, namely the OpAMP's operation range and ADC input range. Additional analysis of those contributions was performed in the appendix B of ref. [109].

To estimate the thermal noise generated by the two mentioned resistors the following needs to be done. Contrary to the detectors described in refs. [123, 124], where signal charge is converted to voltage by the detectors capacity, the DePFET in a drain readout mode provides a I_{SIG} proportional to the number of e^- in the IG. Assuming all stages after the first OpAMP can be neglected, the ENC of the DePFET can be calculated from the current noise densities at the OpAMP's input. Similar to refs. [123, 124], the thermal ENC contribution can be calculated to be

$$\text{ENC}_{\text{S, thermal}}^2 = \frac{1}{\tau} \frac{1}{g_{\text{q}}^2} a_1 A_1 .$$

Behind the DePFET itself, the relevant noise sources in this case are the I_{n} of the resistors R_{F} and R_{SUB} . The resistors thermal noise (a_1) is given by eq. 3.15:

- For the subtraction of 100 μA offset current (I_{OFFS}), at a reasonable voltage difference of 10 V, a 100 k Ω resistor is needed for R_{SUB} .
- For the amplification of up to 100 μA of signal current (I_{SIG}), the minimum input dynamic range of a chosen OpAMP has to be 5 V (1 V), if the R_{F} is 50 k Ω (10 k Ω).

The thermal noise contribution of the described configuration, at the temperature of 300 K and integration time τ of 5 μs , yields 1.5 e^- (7.4 e^-) of thermal noise.⁹ This is comparable to the ENC of the DePFETs used for the spectroscopic purposes [127] without the high dynamic range condition.

3.3 Radiation damage

Different lattice structures of the crystalline Si and amorphous SiO₂ make the transition between the two imperfect. Differences at the transition can strain the bonds of crystalline Si at the interface or even make their breaking energetically preferable,

⁸In essence, a part of the common mode noise can still couple through the CDS, as will be shown at a later point in the thesis when presenting results.

⁹Calculation done under the assumption that the shaping factor A_1 in eq. 3.14 does not change much when switching between time continuous readout and readout on demand.

i.e., create dangling bonds [129]. Consequently, close to the interface there exist additional energy states that are located inside of the Si energy band gap. Those additional states, namely interface traps, influence the behaviour of a transistor channel, and depend heavily on the manufacturing process [90, 130]. The dangling bonds in particular can be neutralized with, for instance, hydrogen annealing where a hydrogen bonds to the Si that is missing a missing bond.

The SiO₂/Si transition differences also cause problems for a few nm into the SiO₂. After this SiO₂ becomes stoichiometric, strain-free and amorphous [90]. But before this occurs, there exists a thin strained layer of the SiO₂ with many oxygen vacancies. Those vacancies occur due to the oxygen out-diffusion during the growth of oxide [128] and act as oxide traps states. Charges trapped in these states generally cannot exchange e⁻ or h⁺ with the crystalline lattice, but they can cause threshold voltage shifts (U_T) of the transistor curves due to the charge build-up in the SiO₂.

During the transmission electron microscopy imaging with the EDET DH80k camera system all but one row of DePFETs are in the OFF state. This means that a voltage more positive than the U_T is applied to the gate structure. Consequently, the band diagram is as the one presented in Fig. 3.10. When an ionizing radiation with sufficient energy impinges on the SiO₂, it can, just like in crystalline Si, ionize the atoms and generate the e⁻/h⁺ pairs.¹⁰ A part of the generated e⁻/h⁺ pairs instantaneously recombines and the rest gets separated by the electric field pointing from the poly-Si gate structure towards

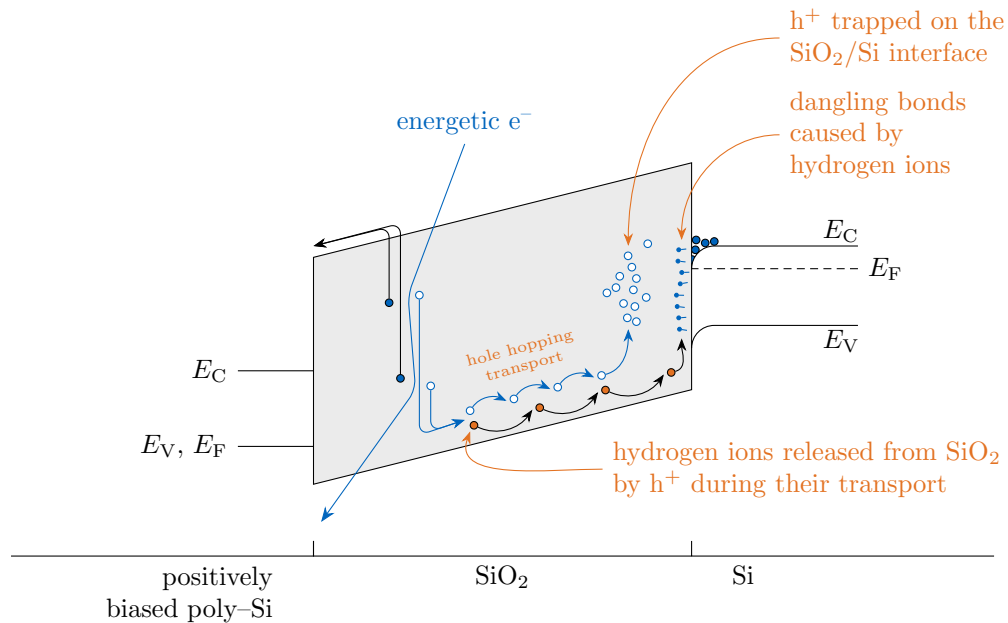


Figure 3.10: Energy band diagram of a metal-oxide-semiconductor structure, with the additional charge transport schematic and trap states close to and on the SiO₂/Si interface. Adapted from ref. [128].

¹⁰The threshold energy for e⁻/h⁺ pair generation is measured at 18 eV [131, 132].

the crystalline Si. High mobility of e^- in the SiO_2 ($20 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) [133] makes it so that they are quickly (within picoseconds) removed from the system [128]. Holes, on the other side, move much slower. Their movement is governed by the mechanism of polaron hopping with a mobility of only $2 \cdot 10^{-7} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [132].¹¹ Despite this, their life time is long enough to arrive to the SiO_2/Si interface, where a fraction of them gets trapped in the oxide traps states and from now on influences the transistor channel potential.

Additionally, it is believed that holes on their way towards the SiO_2/Si interface release hydrogen ions (H^+) from the the SiO_2 [128]. Afterwards, H^+ drift under the influence of the electrical field towards the same interface where they can de-passivate hydrogen bonds [128, 130]. This results in Si atoms with dangling bonds and molecules of hydrogen that can easily escapes the material. Therefore, the ionizing radiation also contributes to an increase in the number of interface traps.

As the oxide traps are always positive, and interface traps of the p-channel transistors are predominantly positive they both sum together to change the channel potential [128]. An important thing for radiation damage is therefore the amount of h^+ produced in the SiO_2 that escape initial recombination (N_h). This was researched in ref. [135] and evaluated to

$$N_h = g_0 t_{\text{OX}} D f(E_{\text{OX}}) . \quad (3.20)$$

The g_0 is the initial e^-/h^+ pair density of $8.1 \cdot 10^{12} \text{ cm}^{-3}\text{rad}^{-1}$ for SiO_2 [135], the t_{OX} is the SiO_2 thickness, the D is the SiO_2 total ionising dose in rad units, and the $f(E_{\text{OX}})$ is the fraction of h^+ that escape recombination. In order to minimize this number one can tune the thickness of the SiO_2 or with the $f(E_{\text{OX}})$. For the current design of EDET DH80k sensors the t_{OX} is already fixed and the only variable left is the $f(E_{\text{OX}})$. According to ref. [136], the smallest fraction of h^+ escape recombination when the electric field in SiO_2 is minimized. Therefore, in order to minimize the radiation damage, the DePFETs in collection mode should be biased with the U_G^{OFF} and U_{CG} of around 0 V. However, the effect of the electric field in the SiO_2 should be much smaller for the DePFETs than for the MOSFETs. In the collection mode the capacitive voltage divider between the poly-Si potential and the Si bulk potential comprises of the two serial capacitances, i.e., the SiO_2 capacitance below the poly-Si and the capacitance of the depleted region in Si. The latter contribution is much smaller than the former, as the thickness of the depleted region is much bigger that the thickness of the SiO_2 . Consequently, most of the voltage drop happens in the Si and the electric field in the SiO_2 should always be small. Nonetheless, it is preferable to minimize the voltage applied to the poly-Si structures in order to avoid high electric fields on their edges, where they overlap the regions with well defined potentials, such as source, drain, clear and drift regions.

¹¹Due to the electric charge of the particle moving in the dielectric material, atoms that are normally ordered in the short-range dielectric lattice move in order to screen the moving charge. Because of this the effective mass is increased and mobility decreased [134]. As the atoms move they can temporarily trap the moving charge until it gains enough energy to escape and move to the next place where it gets trapped again [128] – movement by hopping.

Fig. 3.11 shows three transfer characteristics of a single transistor at three different levels of radiation damage in both linear and logarithmic scale. All curves follow eq. 2.22 but are shifted with respect to each other. The threshold voltage shifts (ΔU_T) between the curves are a consequence of the charge build-up in the SiO_2 . As more and more positive charges are trapped in the SiO_2 , more and more negative gate voltage is needed to turn the transistor on. In addition to the threshold voltage shifts, the curves also exhibit different subthreshold characteristics (sec. 2.3.1). As the number of interface traps increases, h^+ mobility in the channel decreases and the transistor turns on slower. This is the reason that the aligned curves from the right plot do not overlap in the region where the drain current starts to increase. Therefore, the interface traps also influence the amplification of the gate, namely the transconductance (sec. 3.1.1).

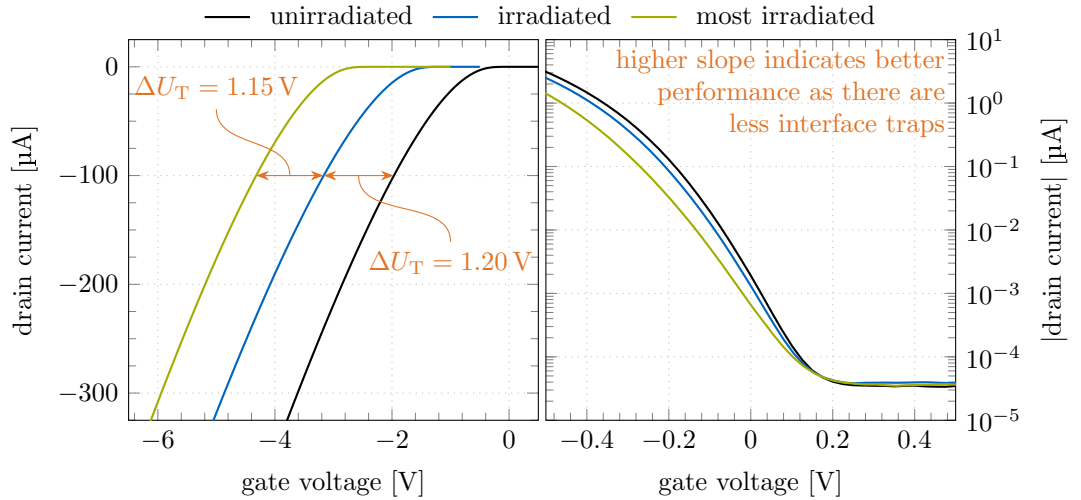







Figure 3.11: Transfer characteristic of a transistor for three different levels of radiation damage. The left plot is in linear scale from which the shifts of the curves can be inferred, namely the threshold voltage shifts (ΔU_T). The shifts are a consequence of the positive charge build-up in the SiO_2 . The right plot is showing the same curves in a logarithmic scale. Additionally, the curves were corrected for the threshold voltage shifts (ΔU_T). From here it can be inferred that the more the transistor is damaged, the poorer is its subthreshold behaviour and lower is the gate amplification, namely the transconductance (eq. 3.2).

3.4 EDET DH80k sensor

The all silicon modules (ASMs) for the EDET DH80k camera system are comprised of the DePFET arrays with 512 physical rows and 512 physical columns. Electrically, the pixels area connected as shown in Fig. 3.5. However, to achieve the required frequency of almost 80 kHz in the column-parallel row-wise rolling shutter mode, there would be only 25 ns available for switching between different operating conditions (sec. 3.1.2) in each of the 512 rows. As this is not enough, the array is actually split in 128 electrical

rows and 2048 electrical columns. Consequently, when a single electrical row is set to the readout mode, drain currents of 2048 DePFET pixels, from four physical rows, must be measured in parallel. This allows for 100 ns to be spent per each electrical row, which corresponds with the speed of the readout DCD ASIC [84, 85].

The average widening of the interaction point for 300 keV e^- impinging on a 50 μm thick block of Si is of the order of 60 μm [82, 137]. Consequently, sampling with a smaller step yields little to no improvements. Therefore, a pixel size of 60 $\mu\text{m} \times 60 \mu\text{m}$ was selected, as it offers a compromise between the granularity and feasibility of the manufacturing process. A group of 2×2 EDET DH80k pixels is graphically presented in Fig. 3.12, and is comprised of the following structures:

- The clear gate (CG) structure () – built from the first poly-Si layer.
- The gate structure () – built from the second poly-Si layer.
- The clear implantation () – the non-depleted high-dose shallow n implantation (HDSN) with the corresponding low-dose deep p implantation below it to thwart the back-emission of e^- from the HDSN and prevent the loss of signal e^- to the HDSN.
- The source implantation ( and ) – combined from the two non-depleted high-dose shallow p implantations (HDSP1 and HDSP2) as described in sec. 3.1.

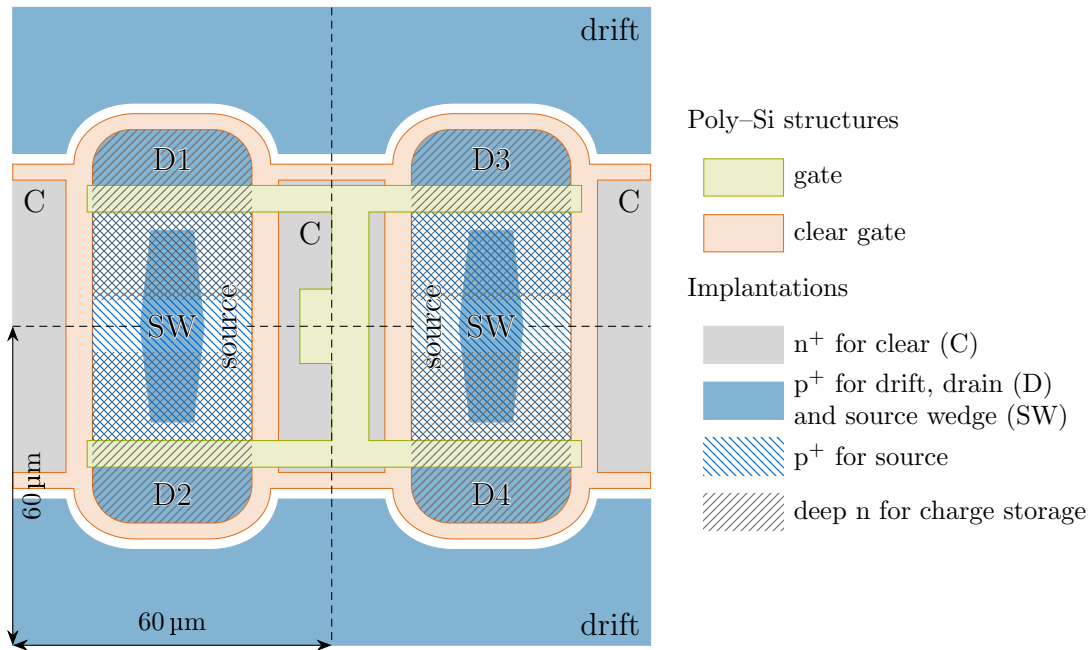


Figure 3.12: The EDET DH80k DePFET pixel layout, where the source is shared between two neighbouring pixels. Multiple charge storage regions are created with a single deep n implantation whose effective dopant concentrations are partly compensated with the different p⁺-type implantations implanted over the same area.

The HDSP2 is implanted over the complete source area, and afterwards the HDSP1 is implanted only in the central region creating the so-called source wedge (SW).

- The drain implantation (■) – the non-depleted HDSP1 implantation.
- The drift implantation (■) – the only new addition to the already known DePFET structure. Built from the non-depleted HDSP1 implantation to which the negative drift voltage (U_{DRI}) is applied ($U_{\text{DRI}} \lesssim U_{\text{D}}$). It is there to enlarge the collection area of a single pixel and assure the horizontal drift from the pixel border towards the internal gate.

A group of pixels presented in Fig. 3.12 is the minimum cell that is repeated throughout the array. However, electrical rows actually control two adjacent rows of such groups.

The technology in which the EDET DH80k DePFET sensors were built, allows for the use of only two aluminium layers. In order to be able to electrically connect all structures, an intricate design plan was devised. In it some DePFET structures are shared between the pixels of the group. Without it, it would be technologically impossible to contact each and every pixel separately. Between four pixels in the presented group, the gate and clear structures are completely shared, whereas the source is only shared between the two adjacent pixels encapsulated by the CG. The CG structure, however, is shared between all pixels in one row, and needs to be electrically connected only on the edges of the array.

The dimensions of DePFET transistors on the main EDET DH80k devices are set at the length of $5\ \mu\text{m}$ (the 2nd poly-Si dimension between the source and drain) and the width of $28\ \mu\text{m}$.

In the scope of this thesis, no work was performed on the main devices as they are intended for the final EDET DH80k camera system which is still in development. However, in addition to main devices, multiple prototyping matrices and smaller single pixel devices were produced on each wafer in the first EDET production run. Those devices feature a design that is similar to the one implemented on the main devices. Consequently, they are perfect for the performance studies. The specifics of each device measured in the scope of this work will be presented in the following chapter.

Multiple charge storage regions are created by the procedure described in sec. 3.1. In the EDET DH80k DePFET pixel design there are three charge storage regions, as shown in Fig. 3.13:

- The internal gate (IG) region (▨) – region below the gate structure where the MDDN implantation is partly compensated only by the LDSP implantation.
- The overflow 1 (OF1) region (▧) – region where the MDDN implantation is partially compensated by the LDSP and HDSP2 implantations.
- The overflow 2 (OF2) region (▩) – region where the MDDN implantation is partially compensated by the LDSP, HDSP2 and HDSP1 implantations.

The physical dimensions of charge storage regions in Fig. 3.13 intentionally do not coincide with the geometrical borders of the two poly-Si structures. This is because the voltages applied to the neighbouring structures make the potential in their vicinity

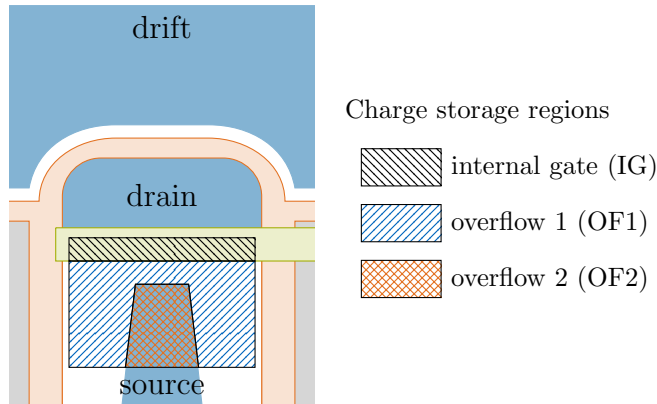


Figure 3.13: Multiple charge storage regions in the EDET DH80k DePFET pixel are created by the use of MDDN, HDSP2 and HDSP1 implantations. The first is implanted before the structuring of gate poly-Si structure and the other two after. Partial compensation between different implantations is what leads to the generation of multiple charge storage regions.

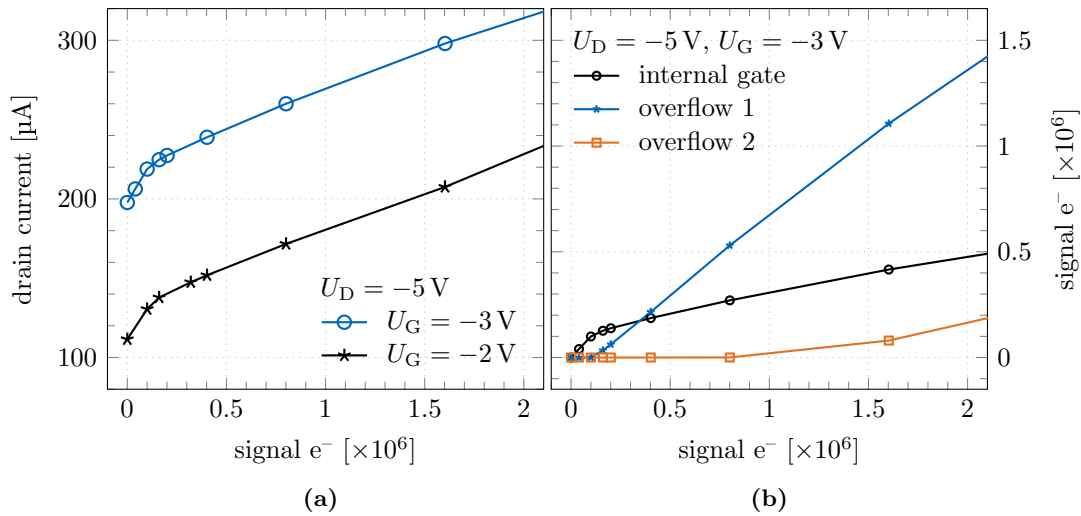


Figure 3.14: (a) Simulated response of the EDET DH80k pixel to the injected signal e^- for two different gate voltages. (b) Simulated distribution of the signal e^- collected in the charge storage regions of the EDET DH80k pixel. Simulated by R. Richter and K. Gärtner [113].

repelling for the e^- . Consequently, the borders, where e^- are stored, are pushed slightly inwards. The offsets in normal operating conditions are in the range of $2\ \mu\text{m}$ for the north border towards the drain, $1\ \mu\text{m}$ for the east and west borders set by the CG, and $0.5\ \mu\text{m}$ for the south border where the MDDN implantation is omitted [113].

Simulation studies for the presented design were performed in the 3D simulating software Oskar3 [138] by R. Richter and K. Gärtner [113]. Some of the results from those simulations are presented in Figs. 3.14 and 3.15. Firstly, the response function of the EDET DH80k DePFET pixel up to the $2 \cdot 10^6$ signal e^- is shown in Fig. 3.14a for two different gate voltage conditions. Two different charge storage areas and consequently two different amplification factors are clearly seen. The first $100\ \text{ke}^-$ are collected solely in the IG and are amplified with the maximum g_q^{IG} of around $210\ \text{pA}/e^-$. After this, new e^- arriving to the charge storage regions are mainly collected in the OF1, and consequently their amplification factor g_q^{OF1} is much lower in the range of $70\ \text{pA}/e^-$. The third section of the response function, corresponding with the e^- arriving to the OF2, is not seen as that region would become important at much higher numbers of collected e^- . Simulation results of the e^- distribution between different charge storage regions is presented in Fig. 3.14b. It can be seen that the OF2 charge storage region is more or less irrelevant in the operation regime as intended for the EDET DH80k project, where the plan is to image with up to $800\ \text{ke}^-$ stored in each pixel [82]. At that point almost no e^- are stored there as the other two regions are not yet full. Even by doubling the intended stored charge, only a tiny fraction of e^- end in the OF2.

Fig. 3.15 shows the simulated trajectories of e^- injected at specific (x, y) coordinates in two different injection z -planes. End coordinates on the plot are marked with arrow heads. Because of the symmetric boundary conditions only one half of a single DePFET pixel is simulated. From the figure it is apparent that no matter at which point the e^- are injected, they always end up in the IG. Consequently, it can be concluded that under normal biasing conditions there is no local potential minimums where signal e^- can get lost or trapped.¹²

The potential distribution, in the Si bulk of the EDET DH80k DePFET pixel, was obtained by the Oskar3 simulation software. Electric field lines, interpolated from the obtained potential distribution, are perpendicular to the equipotential surfaces, and their direction points from the highest to the lowest potential. The injected e^- follow the interpolated electric field lines in the opposite direction until they arrive to the point with highest potential. In this simulation, injected e^- do not actually change the potential distribution. Therefore, they always end up in the IG and never in the overflow regions.

¹²The loss of signal charge occurs when a part of the generated charge does not end in the charge storage regions. Consequently, this fraction of charge cannot modulate the I_D in the readout mode of operation.

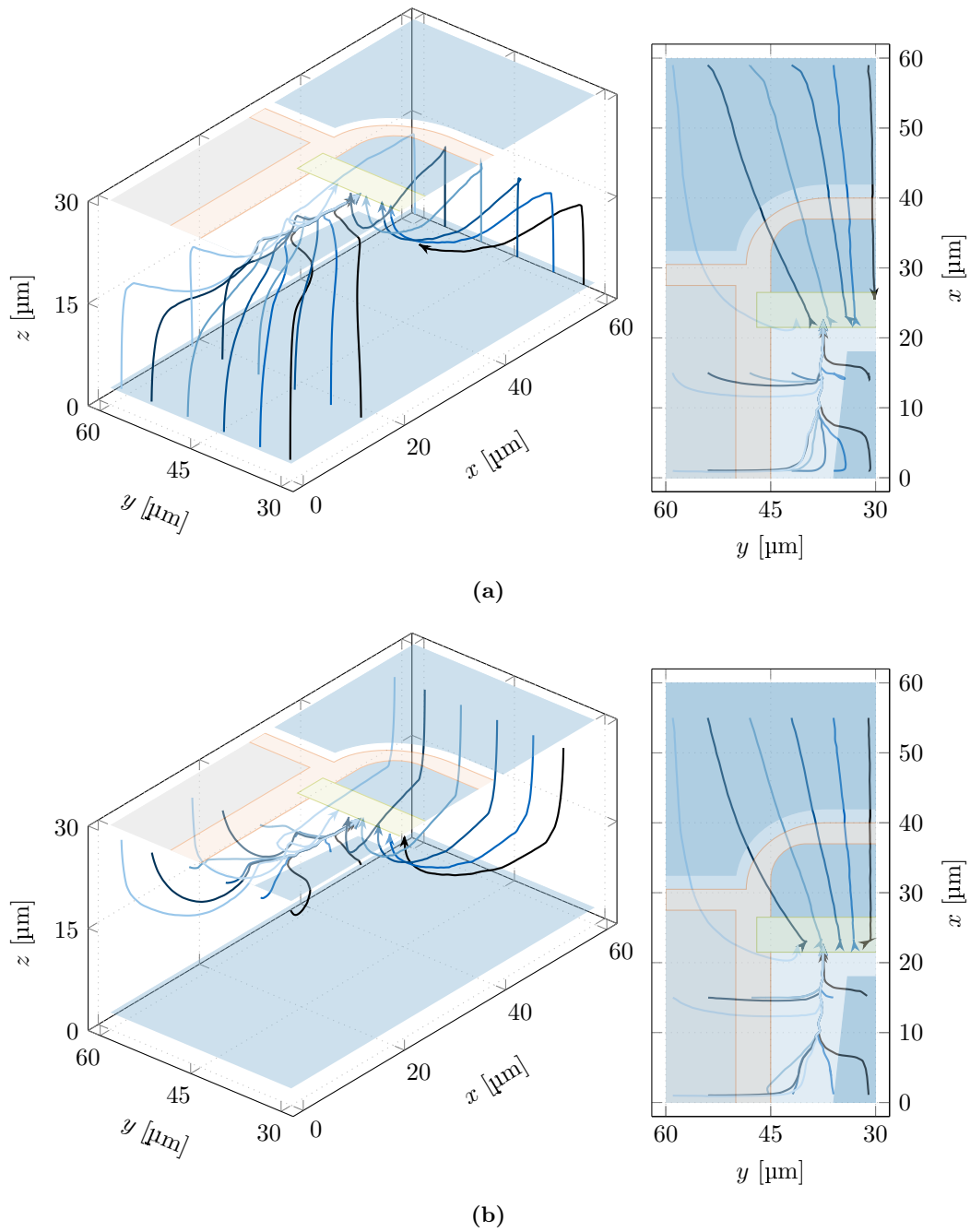


Figure 3.15: Simulated trajectories of the signal e^- injected at different coordinates in the EDET DH80k DePFET pixel. Injections close to the (a) backside and (b) frontside. All trajectories end up in the IG. Simulated with the Oskar3 software [138] by R. Richter and K. Gärtner [113].

4 Available devices

The devices that were produced for the EDET DH80k project will be presented in this chapter.

As described in sec. 1.4, the design, production and test facility is located at the HLL MPG, where a single (first) batch¹ of devices intended for the EDET DH80k project was finalized.² A unique identifier for this batch is PXD10-1, and it consists of four 6 inch wafers. Two of them are the silicon-on-insulator (SOI) wafers with respective thicknesses of 50 μm (W09) and 30 μm (W10) after back-thinning [83], and the other two are the standard 450 μm thick wafers (W11 and W12). The former two are intended for use in the transmission electron microscopy (TEM) environment during the final experiment, whereas the latter two are useful for the project development.

Main steps of the device building on the SOI wafer are recapped from ref. [139] and are presented in Fig. 4.1. Manufacturing starts at the HLL MPG with two n-type wafers of standard 450 μm thicknesses (Fig. 4.1a). One of them is a high-purity n-type wafer, designated as a top wafer, that gets its backside structured with the p⁺-type implantations. The other wafer is designated as a handle wafer and is, as the name suggest, meant for the handling stability. Both designated types of wafers are afterwards shipped to external contractors for bonding, grinding and polishing. First they bond the

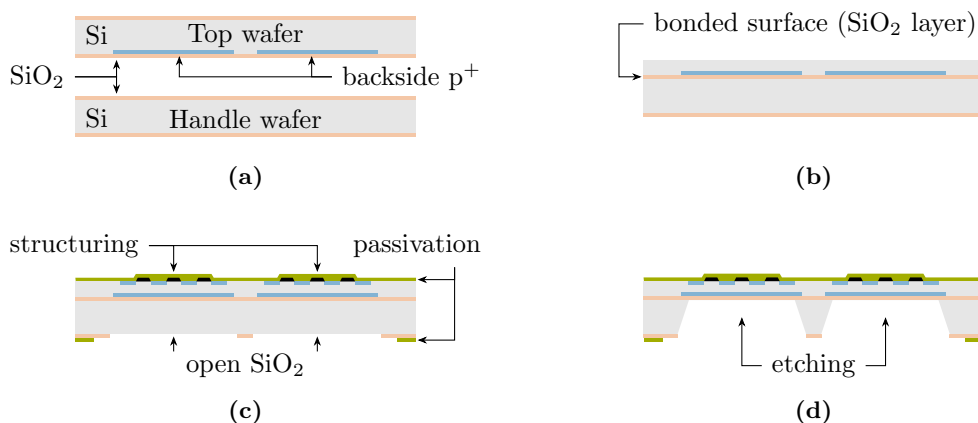


Figure 4.1: Sequence overview of the DePFET device manufacturing on SOI wafers. Adapted from ref. [139].

¹A group of wafers intended for a specific project that goes through all the manufacturing steps together.

²As of 14th of June 2021.

4 Available devices

backside of the top wafer, over the oxidized surfaces, to the handle wafer [140], and afterwards they grind and polish the top wafer, from its frontside, down to the desired thickness (Fig. 4.1b). In case of the EDET DH80k project two different thicknesses were chosen, namely $30\ \mu\text{m}$ and $50\ \mu\text{m}$, because of fears that the thinner one might be too fragile and could break. The wafer-sandwiches, i.e., SOI wafers, are then returned to the HLL MPG where the DePFET devices are structured on the frontside as described throughout chapter 3. After the frontside structuring, a passivation layer is put over the frontside and edges of the backside, and the backside SiO_2 layer is removed underneath the regions that need to be back-thinned [83] (Fig. 4.1c). One of the last steps before wafer cutting is the etching process (Fig. 4.1d), where a chemical etchant removes the

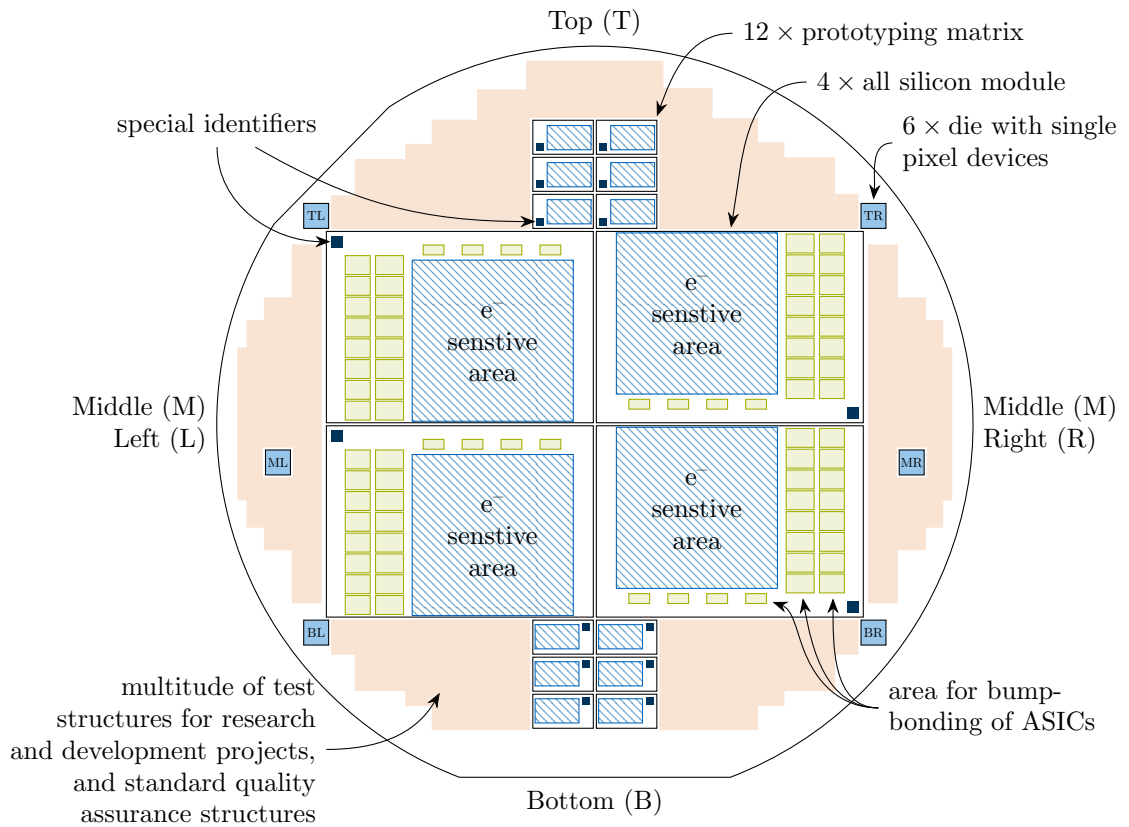


Figure 4.2: Graphical representation of a wafer layout on which the EDET DH80k devices are produced. Each wafer holds four ASMs for the final camera design, twelve prototyping matrices with minor design changes, and six single pixel devices (SPDs). As the SPDs do not have a special identifier they are tracked via their position on the wafer through the use of two letters. The first letter denotes their vertical position – top (T), middle (M), bottom (B) – and the second one their horizontal position – left (L), right (R).

Si from the bottom of the handle wafer until the process is inherently stopped by the inner SiO₂ layer.

When it comes to the frontside structuring, the manufacturing process is essentially the same on SOI and standard wafers. Consequently, the frontside layout of each wafer in the PXD10–1 production batch is identical. Graphical representation of a wafer layout from that production batch is displayed in Fig. 4.2, which shows multiple devices. A total of 22 devices, covering most of the wafer, are related to the EDET DH80k project and will be presented in the following sections of this chapter. The remaining space is occupied with

- prototyping devices for research and development projects taking place at the HLL MPG, and
- simple technology verification devices and standard quality assurance structures.

4.1 Main devices

Four main devices that are implemented on the all silicon modules (ASMs), located in the centre of the wafer, are the workhorses intended for the final EDET DH80k camera system. Their overall description is found in sec. 1.4, and their DePFET pixel design is presented in sec. 3.4. Their overall pixel dimension are 60 μm \times 60 μm with the DePFET’s gate covering the area that is 6 μm long and 27.2 μm wide.

4.2 Prototyping matrices

Twelve prototyping matrices (PMATs), found above and below the ASMs, are the work horses for the EDET DH80k system development. All of them host 8192 DePFET pixels connected in the array with 64 physical columns and 128 physical rows. Electrically, this translates to 256 electrical columns and 32 electrical rows. This was deliberately chosen so that only one of each kind of peripheral application-specific integrated circuits (ASICs), to be used with the final system (sec. 1.4), is enough for a complete control of a PMAT.³ In addition to their smaller size, the PMATs also do not feature the complete ASM design found on the main devices, but host only the DePFET array with corresponding bonding pads for electrical connections. Consequently, this allows for more flexibility, as the PMAT can be wire-bonded [141] to an arbitrary measurement system that supports the DePFET operation.

In regards to the DePFET pixel design implemented on the PMATs, there are three different design versions as presented in Fig. 4.3. The main design (Fig. 4.3a) is identical to the one implemented on the main devices, and it has been thoroughly described in sec. 3.4. The difference between the main and the second, the so-called fallback design (Fig. 4.3b), is only in the dimensions of the DePFET structures. The overall pixel dimensions are still 60 μm \times 60 μm , but the poly-Si structures forming the gate and clear gate (CG) are shrunk in order to make the source region smaller. This is due to

³Peripheral ASICs are the digitizing ASICs, readout ASICs and control ASICs.

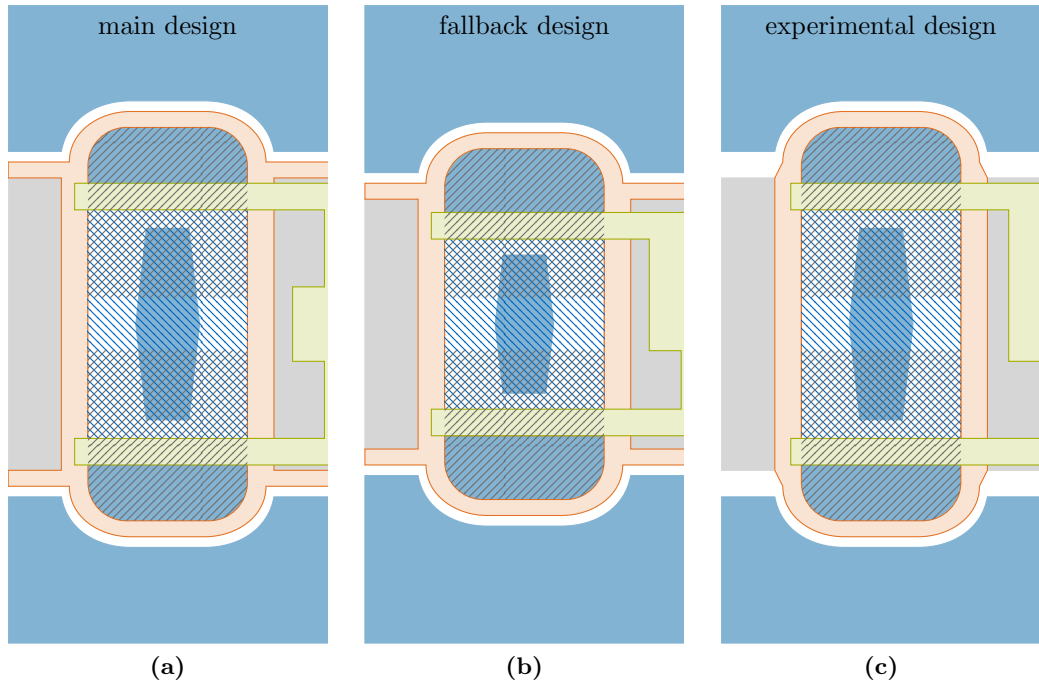


Figure 4.3: Three different DePFET pixel design versions implemented on the PMATs; a main design as implemented on big devices (a), a fallback design with smaller DePFET structures (b), and an experimental design with omitted CG connections around clear regions (c).

the simulations showing that a smaller source region copes better with the variations in the doping of the Si bulk [113]. The third design, the so-called experimental design (Fig. 4.3c), keeps the same dimensions as the main design, but omits the poly-Si bridges around the clear region that are connecting the CG together. Consequently, there is a need for the additional aluminium lines to bias all CG islands. The reason for the change is in the collection of e^- from under the drift regions. In order for them to be collected in the charge storage regions, they first have to traverse under the CG, and afterwards either under the drain or clear regions. However, the potential under the CG can become more positive during the e^- irradiation (sec. 3.3). Correspondingly, a potential pocket for e^- can be formed below the CG. This is not a problem in the vicinity of the drain, as the potential there is very negative and the e^- drift sideways towards the clear region. There, however, they could potentially get trapped – hence the removal of CG bridges. Despite the possible benefits, the missing potential barrier could allow for the unwanted effects like the current flow between the source and drift implantations. Therefore, this design is, as the name suggest, experimental.

In addition to the design variations, there are also different gate lengths implemented on PMATs. The number of devices of a certain type in dependence of the gate length is presented in Tab. 4.1.

In this thesis the measurements results from three different PMATs will be presented:

1. A PMAT with a $50\ \mu\text{m}$ thin sensitive area, on which the main design is implemented with a $5\ \mu\text{m}$ gate length. Unique identifier W09 F07.
2. A PMAT with a $30\ \mu\text{m}$ thin sensitive area, on which the main design is implemented with a $5\ \mu\text{m}$ gate length. Unique identifier W10 F07.
3. A PMAT with a $50\ \mu\text{m}$ thin sensitive area, on which the experimental design is implemented with a $5\ \mu\text{m}$ gate length. Unique identifier W09 B07.

A unique identifier is assembled from two parts; first is the wafer number and second the device identifier. The wafer numbers were already presented in the beginning of this chapter. The device identifier is physically present on the majority of devices, including the PMATs, as shown in Fig. 4.2.

Table 4.1: PMAT design frequency in dependence of the gate length that is represented on each wafer in the PXD10–1 production batch.

gate length	design versions		
	main	fallback	experimental
$4\ \mu\text{m}$		1	
$5\ \mu\text{m}$	3	3	2
$6\ \mu\text{m}$	1	2	

4.3 Single pixel devices

Last but not least, a variation of the EDET DH80k DePFET pixel design is also implemented on six dies from the periphery of each wafer in the PXD10–1 production batch. Each die covers an area of $5\ \text{mm} \times 5\ \text{mm}$, and is different to all other described devices in this chapter as it hosts four different DePFET arrays. Only two of those arrays, henceforth called the single pixel devices (SPDs), are related to the EDET DH80k project. A single die, with two SPDs that are a part of the EDET DH80k project, is presented in Fig. 4.4a. Each SPD is comprised of 24 DePFET pixels (Fig. 4.4b) that are electrically connected together to a single array (Fig. 4.4c). The DePFET pixels are still covering an area of $60\ \mu\text{m} \times 60\ \mu\text{m}$ and are most similar to the fallback design version seen in the PMATs. They feature a narrower gate width of $21.2\ \mu\text{m}$ in comparison to the $27.2\ \mu\text{m}$ as implemented on other described devices. The difference is compensated with wider clear regions. Additionally, three groups of eight DePFET pixels are implemented inside each SPD array (Fig. 4.4c). The groups differentiate between themselves in different gate lengths. The first group, namely pixels from 0 to 7, has pixels with the gate length of $3.8\ \mu\text{m}$, the second group, namely pixels from 8 to

15, has pixels with the gate length of $4.8\ \mu\text{m}$, and the last group, namely pixels from 16 to 23, has pixels with the gate length of $5.8\ \mu\text{m}$. Each group of pixels also features three different shapes of source source wedges that vary in inclination, length and width. The idea was to test the influence of those changes to the charge collection efficiency and charge amplification.

All dies from the two standard wafers are identical, whereas the dies from the SOI wafers come in two different flavours. As the SOI wafers have a different backside manufacturing process and the described dies are positioned on the very edge of the wafer, four dies from the top and bottom locations on the wafer are missing their backside p^+ -type implantations. Consequently, it is not possible to fully deplete their Si bulk. In every other aspect those dies feature fully functional DePFET pixels. Another consequence arising from their edge placement on the wafer is that none of the devices are back-thinned, albeit being on the SOI wafers. This is a precautionary measure, as the back-thinning on the very edge of the wafer could result in the leakage of the chemical etchant from the backside of the wafer to its frontside, which would result in irreversible damage to the structures built on the frontside.

Due to space constraints, the SPDs are missing a physically present unique device identifier. Therefore, their naming convention is based on the wafer name, position of the die on the wafer, and the quarter of the die from which the SPD originates, i.e., wafer die quarter. The wafer names were already explained in the beginning of this chapter. The position of the die on the wafer is denoted through the use of two letters. The first letter denotes the vertical position, namely top (T), middle (M) or bottom (B), and the second letter denotes the horizontal position, namely left (L) or right (R). Graphical explanation of the die positions is found in Fig. 4.2. The quarter names of the two SPDs from the same die are the 80k1, for the SPD close to the punch-through (PT) bonding pad, and the 80k2 for the other (Fig. 4.4b).

Initially, the SPDs were thought to be the main point of interest for all measurements in the scope of this thesis. However, because of the two unfortunate layout errors their dynamic performance became very limited. The mistakes were:

- A missing connection between the drift bonding pad and drift p^+ -type implantation, which results in the floating drift region. In consequence, the operational parameter window in which the charge storage regions collect the e^- with significant efficiency is noticeably reduced.
- The PT bonding pad is covered with a protection layer which prevents electrical contact. Consequently, it is not possible to deplete the Si bulk of the SPDs.

Despite the impediments it is still possible to use the SPDs for measurements. The quasi-static measurements were performed on all SPDs, and their result were compared over the complete production batch – shown in sec. 5.3. For the dynamic measurements, a limited set of results is presented in sec. 5.2.2. Those results initially revealed the shortcomings of SPDs and lead to the discovery of aforementioned mistakes.

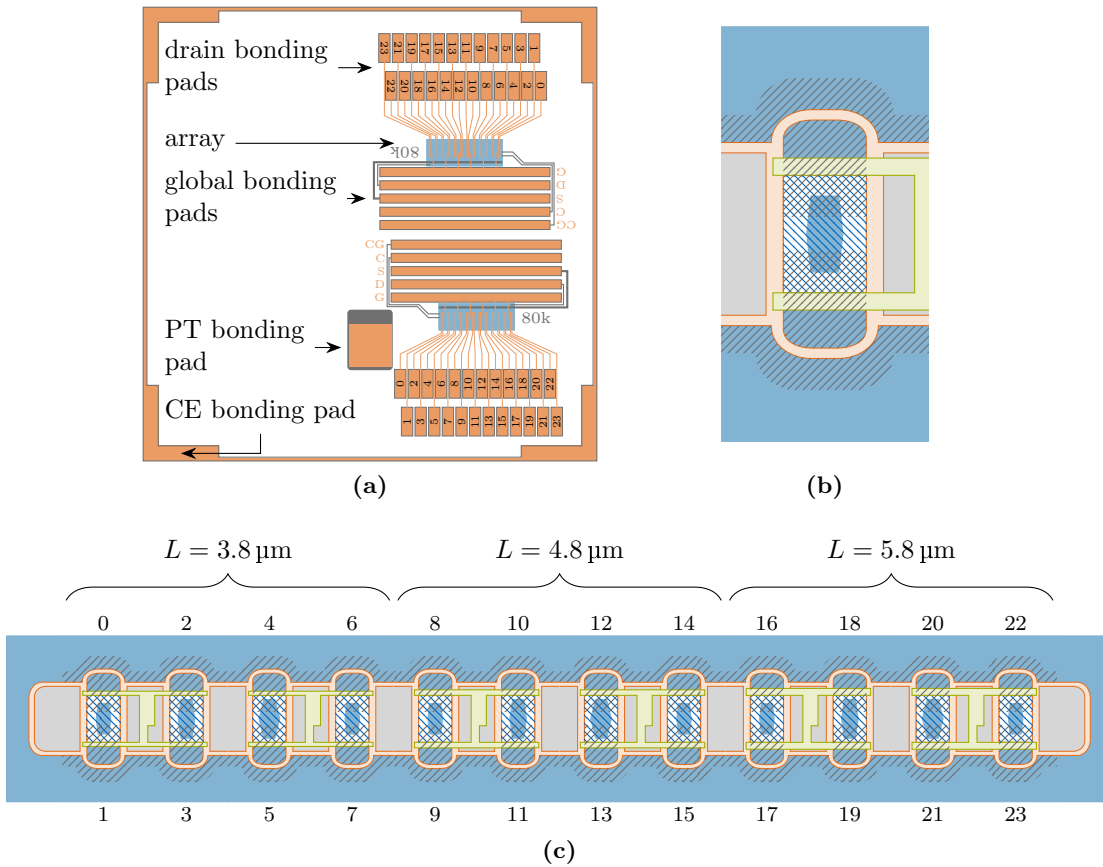


Figure 4.4: Graphical representation of the die containing two SPDs related to the EDET DH80k project (a), a close up of the first pixel pair (b), and a close up of the complete 24 pixel array (c). 5 global bonding pads are connection points for the clear gate, clear, source, drift and gate.

5 Characterization measurements

In this chapter the results from characterization measurements performed on different DePFET structures in the scope of the EDET DH80k project will be presented. Those measurements can in general be split in two groups: quasi-static measurements and dynamic measurements.

The former group represents the measurements that are evaluated in a thermal equilibrium, i.e., when applying the same conditions (e.g., biasing potentials, temperature, brightness) to the device the result is always the same. However, in the scope of the measurement one or more parameters can still be varied in order to quantify their impact on the measured quantity. For instance, to measure the drain current vs. gate voltage characteristics of a MOSFET device (sec. 2.3.1) all voltages but the gate voltage are fixed in order to obtain the measurement that is described by eq. 2.22. Measurements of this kind are extremely useful for the fundamental parametrization of produced devices. In the case of DePFETs this means measurements of the threshold voltage and the subthreshold behaviour when the internal gate is empty (sec. 2.3), and measurements of the empty internal gate potential. Extracted parameters can be the foundation for changes in future production runs if they do not fit the project specifications or if room for improvement is identified. In addition, they can also serve as a quality control feature through the comparison of devices from different wafer locations, and through the comparison of different production batches manufactured with the same technology.

In addition to the fundamental parametrization, the quasi-static measurements are also used to pre-characterize the devices in order to check for tolerable or lethal defects. Afterwards, known good dies are permanently connected with multiple application-specific integrated circuits (ASICs) to function within the scope of a specific measurement system. As the process of assembly is expensive and time consuming, pre-characterization step is mandatory. In addition, the pre-characterization is not only used to check devices themselves, but also to determine how broad is the operation parameter space over the complete production.

In the group of dynamic measurements, the device is operated much like the final system will be (described in sec. 3.1.2). The twist here is that for each measurement at least one operating parameter (e.g., any of the operating voltages, duration of a clear pulse, length of a sequence) is varied and the influence of this variation is evaluated. Consequently, the intent of those measurements is the determination of optimum parameters for a given device in the scope of its project.

The systems used for the characterization measurements will be presented prior to the measurements and their results.

5.1 Measurement systems

For the measurements presented in this chapter two different types of measurement systems were utilized. The first type is used for the quasi-static measurements, and the second for the dynamic measurements.

Within the scope of pre-characterization measurements two measurement systems were used. Initially, all but one single pixel device (SPD) dies were tested with the industry standard probe station used for semiconductor pre-characterization measurements. This system is highly flexible and can be used for a variety of different devices. With it, metal probe needles are used in order to reversibly connect the electrical contact pads of the device to the measurement system. However, DePFET devices require a large number of electrical contacts on a small area. Consequently, spatial constraints prevent contacts to all electrical pads on the device with bulky probe needles. This in turn limits the significance of the measurements. Therefore, a second pre-characterization system was developed in the scope of this work. This one works around the contact problems, and is able to provide the needed quality of measurements. However, this system is specialized to work only with the SPDs, and on top of that the SPD die needs to be permanently connected to a part of this system. Consequently, only the SPD dies that were not needed for any other measurements were tested with this system. Both systems are presented in sec. 5.1.1.

For the dynamic measurements a highly specialized and yet extremely flexible measurement system was developed in the scope of this work. This system is presented in sec. 5.1.2.

5.1.1 Quasi-static measurements

Quasi-static measurements for device pre-characterization are usually performed on the general purpose semiconductor test systems. The benefits of such systems are that they are highly flexible and can measure different semiconductor characteristics without the need of any hardware changes. Essentially, they can be split into two general parts. The first being the probe station, where the electrical contact pads of the device are reversibly contacted through the use of tiny contact needles. Those contact needles are coupled to a bulky precision positioning mechanism. The second part consists of the electrical system that is capable of measuring the response of the device under different biasing conditions.

A general purpose pre-characterization measurement system (generalPCMS), like the one described above, was used for the initial characterization of SPDs in the scope of this thesis. It is presented in pictures in Fig. 5.1, and is comprised of the SÜSS's PA200N semiautomatic probe station (PA200N) and the Keithley's 4200A-SCS Parameter Analyzer (4200A-SCS) [142]. The former is placed in a light tight dark box to remove the interference originating from external illumination, and is comprised of the

- anti-vibration system,
- alignment microscope,

5.1 Measurement systems

- multiple contact needles for electrical connections with the device that can be finely controlled either electronically or manually in all three physical dimensions,
- and a chuck holder that is used for placing of the whole wafer or a single die on it.

The position of the chuck holder is electronically adjustable in all three physical dimensions – two of them are controlled by linear movements whereas the third is accessed

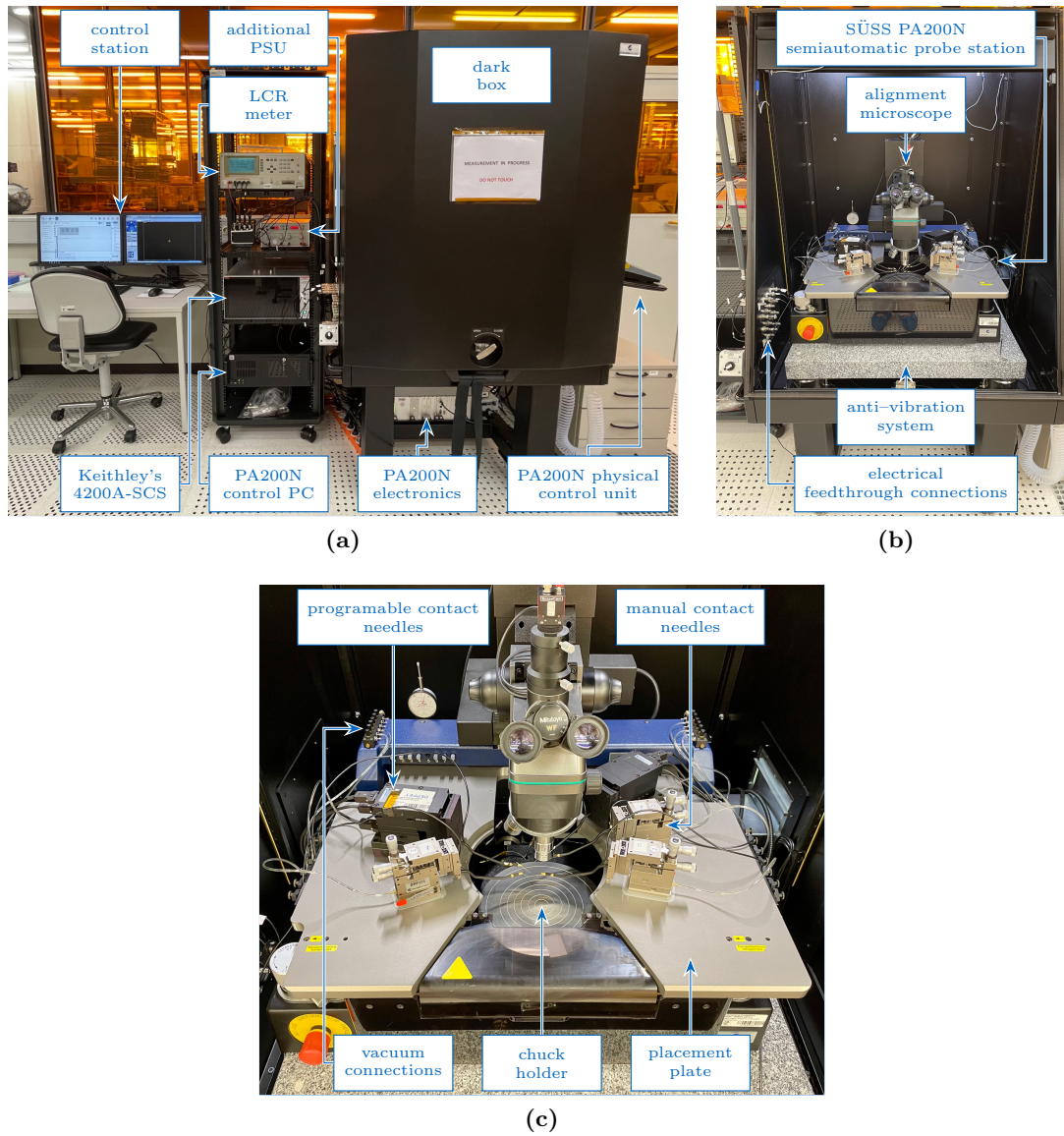


Figure 5.1: Pictures of the general PCMS; the system is a fusion of the SÜSS's PA200N semi-automatic probe station located in the dark box and the Keithley's 4200A-SCS Parameter Analyzer.

by the rotation around the centre. Placements of the contact needles on the placement plate and wafers or dies onto the chuck holder is secured by the vacuum connections.

The electrical connection from the contact needles to the 4200A-SCS, the hearth of every measurement system used for quasi-static pre-characterization in this work, is made by the use of coaxial and triaxial cables [143]. The 4200A-SCS is a mainframe with 9 empty slots that can be occupied with different extension units in order to measure a required quantity, e.g., measuring the current or capacity at an arbitrary applied voltage. Additionally, the 4200A-SCS includes a built-in computer with Windows 10 operating system that runs the Keithley's Clarius+ Software Suite which simplifies the measurements. In case of the DePFETs it is interesting to measure the drain current vs. voltage characteristics. Therefore, the 4200A-SCS was used in combination with multiple Keithley's 4200 Source-Measure Units (4200-SMUs).¹ The 4200-SMU is a very precise instrument capable of sourcing (or sinking) power and simultaneously measuring current and voltage levels. Each 4200-SMU features a 20 bit analogue-to-digital converter (ADC) so that the measurements are instantaneously available in the digital format. It can measure currents in seven different current ranges from the smallest of up to 100 nA to the biggest of up to 100 mA. Smallest measurement error in the lowest current range is ± 30 pA [142]. It limits the 4200-SMU's usage in the low current range down to level of about 100 pA. Beyond this point the measurement error rises above $\pm 30\%$ and the data becomes insignificant. In general it is possible to increase the sensitivity and resolution at the very bottom of the spectrum with preamplifier units [142], however this was not needed for the measurements performed within the scope of this thesis.

Custom built pre-characterization system As already mentioned, the downside of the previously presented generalPCMS is the inability to fully bias the complete device due to spatial constraints. Therefore, a specialized secondary measurement system was developed in the scope of this work to fully characterize the parameter space of the SPDs. This so-called custom built pre-characterization measurement system (customPCMS) is presented in pictures in Fig. 5.2 and in schematics in Fig. 5.3. The customPCMS allows to precisely measure quasi-static characteristics of a fully biased SPD. A disadvantage of this system, when compared to the generalPCMS, is that the SPD die needs to be permanently glued and wire-bonded to the ceramic printed circuit board (PCB) (shown in the bottom right corner of Fig 5.2b). Consequently, only the SPD dies not intended for any other purpose were tested with this system. Apart from this, it should offer a superior performance in terms of quality and duration of the measurements. Both SPDs from the SPD dies are fully wire-bonded to the ceramic PCB, which is afterwards reversibly connected to the die carrier PCB (Fig. 5.3a). This means that the ceramic PCBs can be easily exchanged. Afterwards, the die carrier PCB is connected to the breakout PCB, which is used to select which SPD from the connected SPD die will be

¹In the scope of this thesis two different 4200A-SCS mainframes were used to perform the quasi-static measurements. One was populated with six and the other with nine 4200-SMUs. Two of the populated 4200-SMUs in both mainframes were additionally equipped with preamplifier modules in order to improve their sensitivity in the fA current range.

measured, and for electrical connections to the measurement part of the system. The SPD contacts are electrically connected to the following components (Fig. 5.3):

- source and cutting edge (CE) are biased by a Rohde & Schwarz HMP4030 power supply unit (PSU) [144],
- clear gate (CG), gate and clear nodes are separately connected to three 4200-SMUs in the 4200A-SCS, and lastly the
- 24 pixel drains are connected to the two Keithley’s 7174A switching matrix cards (7174As) [145] located in the Keithley’s 707B 6 slot switching matrix mainframe (707B) [145]. From there connections to the five 4200-SMUs, located in the 4200A-SCS, are made.

Switching matrices are needed in order to avoid physical swapping of the cables. The used 4200A-SCS has nine 4200-SMUs installed in it, but due to the software limitations it is only capable of performing parallel measurements on eight. Three of them (SMU1–3) are occupied by the global DePFET’s CG, gate and clear nodes – as each will be varied in their own quasi-static measurement – and the remaining five (SMU5–9) are used to measure the drain currents of the pixels. However, in order to always have identical biasing conditions for all pixels, twenty drains are connected together to the SMU5, and the remaining four drains get their own 4200-SMUs (SMU6–9). This is shown with the filled blue dots on the right side in Fig. 5.3b. For each condition applied on the SMU1–3 the measurement is repeated six times, always with a different connection scheme on the 707B. That way, individual drain current measurements are obtained for each pixel.

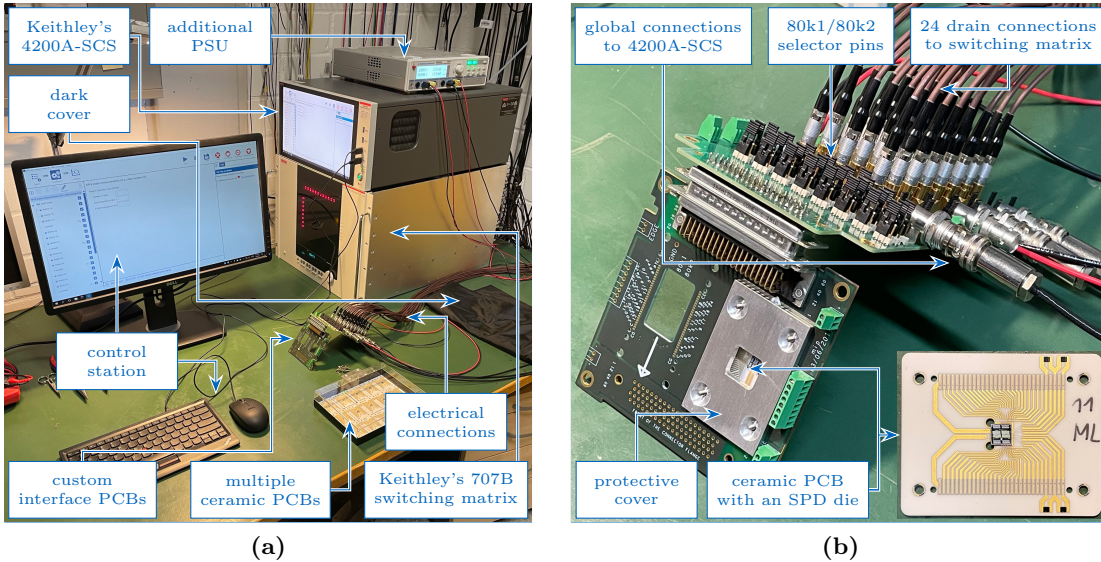


Figure 5.2: Pictures of the customPCMS for quasi-static measurements on the EDET DH80k SPDs; general overview of all components (a), close-up to the specially designed PCBs (b).

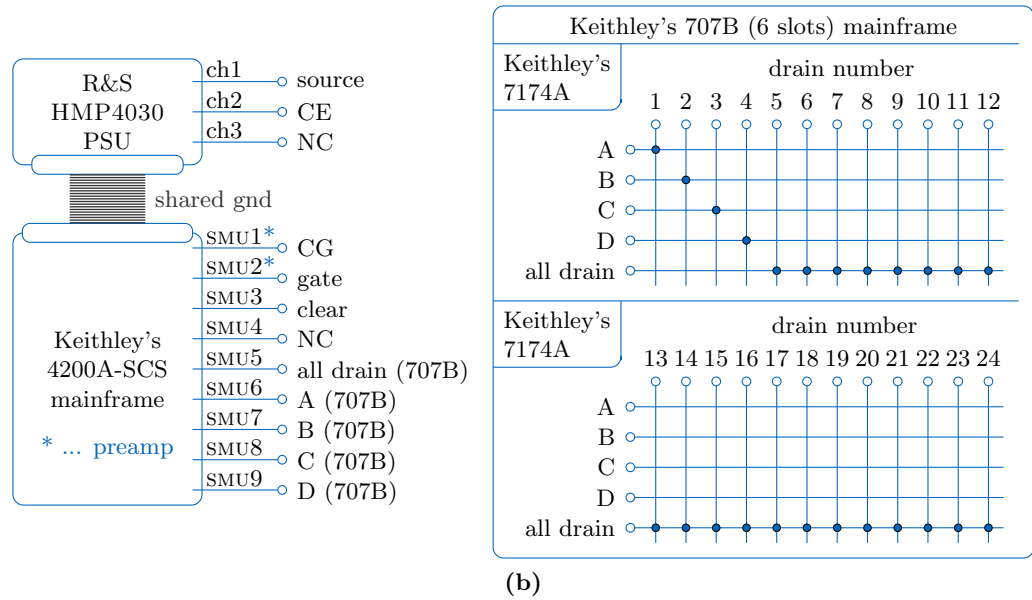
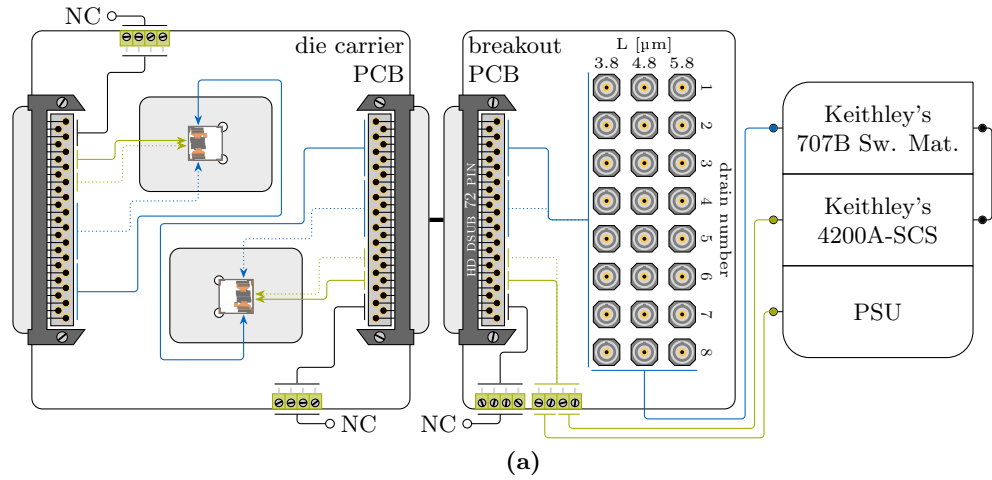


Figure 5.3: Schematic view of the customPCMS for quasi-static measurements on the EDET DH80k SPDs. (a) Overall view of all components in the system, with green and blue lines respectively being the DePFET's global and drain connections. Solid lines represent the connections to the 80k1 quarter on the connected SPD die and dotted lines to the 80k2 quarter, with only one of them being biased at the same time. (b) The electrical connection diagram for biasing of the selected 80k quarter on the mounted SPD die, with the readout of the first four drains as selected by the Keithley's 707B 6 slot switching matrix mainframe.

By measuring the responses of four pixels in parallel, and removal of the initial position calibration as needed with the generalPCMS, the measurements are performed much faster.

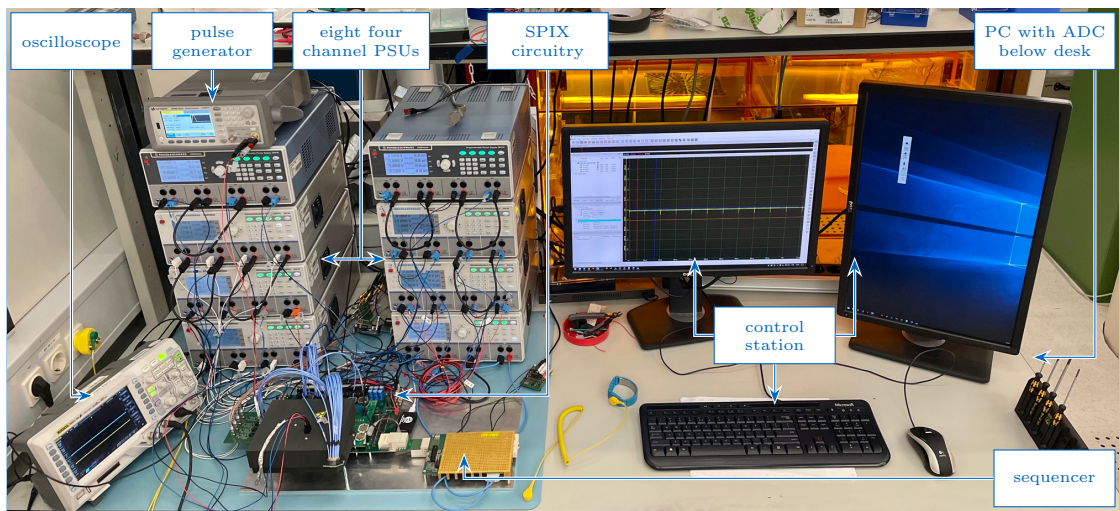
5.1.2 Dynamic measurements

The system used to perform dynamic measurements in the scope of this thesis has nothing in common with the EDET DH80k camera system presented in sec. 1.4. The first question that presents itself at this point is: Why the need for two different measurement systems? To understand this an analogy with Formula One cars can be made – they are arguably the most high-tech cars that exist. However, they are specialized for a single task, specifically for racing on the tarmac tracks. Consequently, one would have a lot of troubles to go, for instance grocery shopping with it. Equally, the EDET DH80k camera system is a highly specialized and complex system designed to record high frame rate bursts of images. It does that with the help of specifically developed control and readout ASICs. Now coupling the specialized ASICs with a novel DePFET sensor design, and one is left with a very limited parameter space for detailed studying and understanding of the sensor performance. Additionally, as all the components in that system are new and they can only be tested when connected together, it can be extremely difficult to look for possible improvements or pinpoint the source of potential problems. Consequently, there exist a need for a highly flexible system that can be used for an in-depth analysis of the DePFET sensor. The system should offer a very high degree of modularity on each and every parameter, and be able to measure the DePFET's response with high accuracy and low noise.

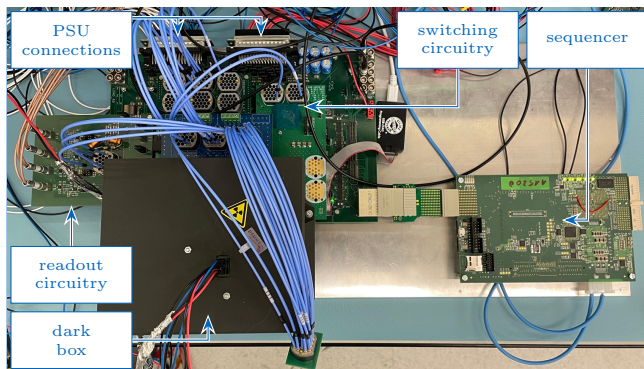
In the scope of this work, a so-called single pixel measurement system (SPIX) was developed. The system can be seen in pictures in Fig. 5.4 and in schematics in Fig. 5.5. It was not developed in order to measure the response of hundreds of pixels at once (e.g., measure the complete pixel arrays), but to offer precise measurements of a handful of pixels with a high degree of flexibility. Additionally, the system offers a high degree of modularity with a small degree of work needed in order to implement the changes. The complete system is built around the SPIX mainboard PCB (Fig. 5.5) that serves as a main connection hub. In the upper left corner in Fig. 5.5 the sequencer PCB is connected to the SPIX mainboard via the CompactPCI Express connector (cPCIe). As this part connects two different circuitries, it is galvanically isolated from the rest of the SPIX mainboard in order to break ground loops and avoid digital crosstalk. This is achieved by the use of multiple optocouplers (Ⓞ). Afterwards, the digital signals, originating from the sequencer, are connected to either the field programmable gate array (FPGA) state machine or the LEMO connectors (Ⓞ). The former allows for more flexibility in connection routing on the mainboard, since it can be digitally programmed to distribute the digital signals as needed, and the latter allows an easy distribution of the digital signals to the external pieces of hardware, like pulse generator, oscilloscope, ADC, laser, pulsed light-emitting diode (LED). Downstream of the FPGA, the digital signals go to the switching and readout parts of the system. Those parts are located on their respective child PCBs (Switcher PCB and Readout PCB), and they both connect

5 Characterization measurements

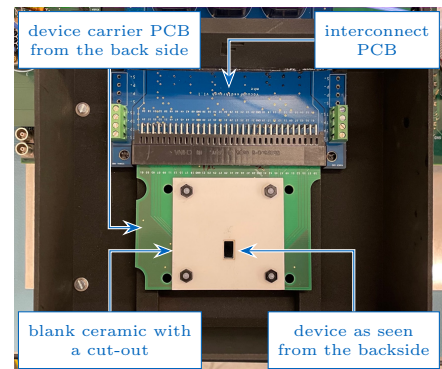
to the SPIX mainboard PCB by the use of the spring compression connectors that are not visible in Fig. 5.5 as they are already covered by the respective child PCBs. The same is true for the third child PCB, namely the Sensor PCB. The child PCBs are one of the main features of this system. They allow for a higher degree of modularity in the system, without the need to redesign it completely in case of minor changes. Consequently, if for an instance a new steering ASIC becomes available, only the Switcher PCB needs to be redesigned and the system can be used in the new configuration. The same holds true for the other two child PCBs as well. The remaining parts of the SPIX mainboard are the parts with additional LEMO connectors and the power supply unit (PSU) part. The former are used for the connections to (or from) different components on the SPIX mainboard (e.g., FPGA, Sensor PCB, Readout PCB) meant for additional external signals or debugging features. The latter part uses two connectors in order to provide



(a)



(b)



(c)

Figure 5.4: Pictures of the highly modular SPIX measurement system used for dynamic measurements in the scope of this thesis.

each component with its own power supply line connected to the PSU stack. In other words, if a component (for instance, a DePFET sensor) needs 9 different nodes biased it is supplied with 9 power supply lines that occupy 9 channels in the PSU stack – this results in an extremely good flexibility as every parameter can be varied in the search of the best operating conditions. Additionally, all power supply lines are equipped with buffering capacitors that also act as low pass filters.

The child PCBs (Switcher child PCB, Sensor child PCB and Readout child PCB) are supplied with their power lines and digital signals over the spring compression connectors. However, they also feature connectors for the direct transfers of analogue signals between themselves.

Sequencer A sequencer board is used for the coordinated switching of DePFET control signals synchronous with potential ASIC readout control signals. For the implementation

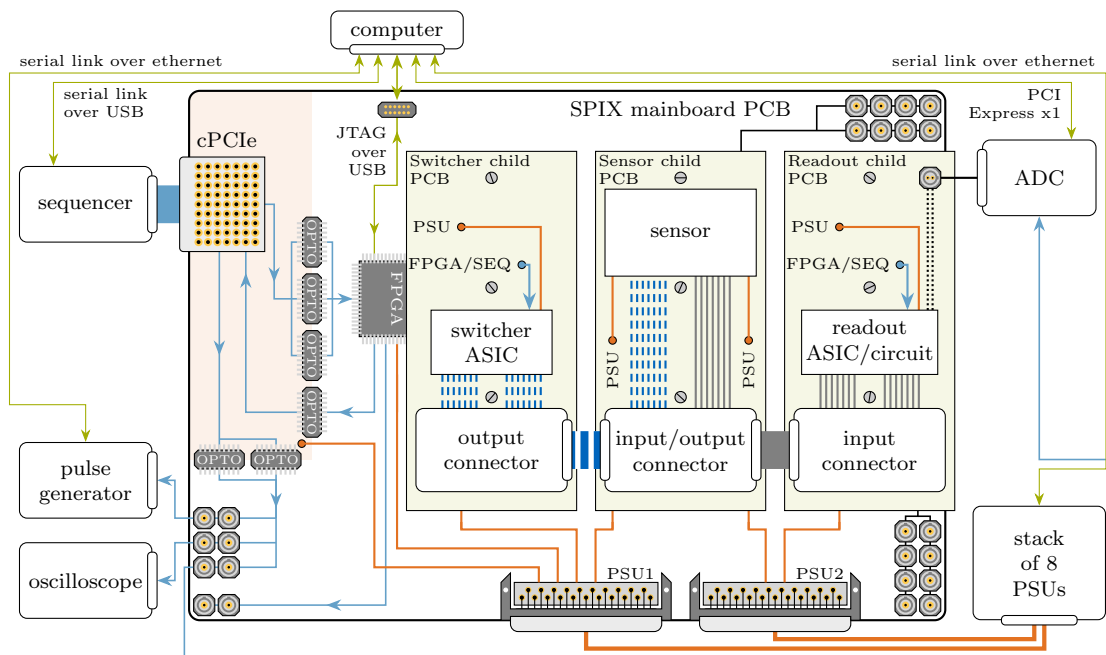


Figure 5.5: Schematic overview of a highly modular SPIX measurement system. The orange lines (—) represent the analogue biasing connections that originate from the PSU stack, the dark blue arrows (→) are the low voltage differential or single-ended digital control signals that originate from the galvanically isolated sequencer, and the green arrows (↔) are the communication and data transfer connections between the computer and connected components. The blue dashed lines (---) are the analogue signals generated by the switcher ASIC on the Switcher PCB in order to control the DePFET gate and clear structures, whereas the gray lines (—) are the DePFET drain lines connected to the readout circuitry. The last type of the shown connections is presented with dotted black lines (⋯). They represent the DePFET drain signals, converted and amplified by the readout circuitry, that are fed into the ADC for digitization.

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of the sequencer functionality, a multi-purpose FPGA board with the cPCIe interface is used. This so-called IgelLight Board is an in-house development of the HLL MPG, and features 8 independent user programmable digital channels with the time resolution of 10 ns. The sequence can be programmed on the control computer and transferred to the board through the serial link connection.

Power supply units In order to bias all components of the SPIX measurement system, a minimum of 31 separate PSU channels are needed. The Rohde & Schwarz HMP4040 PSUs [144] that offer four galvanically isolated channels with low residual ripple, were already used and verified at the HLL MPG. Consequently, they were chosen as the PSUs for this system. A total of eight HMP4040 PSUs are featured in the SPIX measurement system, and all of them are remotely controllable by the control computer.

Analogue-to-digital converter With the selection of the ADC a compromise between the sampling speed and sampling resolution had to be made. In the end, the four channel M2i.4961-Exp ADC from Spectrum Instrumentation [146] was selected. It offers a 16 bit sampling resolution over 6 different voltage ranges between ± 200 mV and ± 10 V at a maximum frequency of 62.5 MHz (sampling every 16 ns) with a bandwidth of 30 MHz.

Pulse generator In order to trigger additional components that are not shown in Fig. 5.5 (laser, pulsed LED) the Keysight Technologies 33511B pulse generator was used. It is triggered by the sequencer's digital signal and it provides a signal pulse with a selected pulse height and duration to the connected device. The reason for such configuration is to convert the digital trigger pulse from the sequencer to a custom analogue driving pulse for the downstream receiving device.

Oscilloscope The Rigol Technologies 1104Z oscilloscope does not play a major role in the SPIX measurement system itself. It is needed for the verification and debugging of the signals.

5.1.2.1 Switcher child PCB

The intention of the Switcher child PCB is to host a steering ASIC that employs the sequencer's control signals to selectively switch between different voltages that are then applied to the DePFETs. The Switcher child PCB, developed in the scope of this work, is capable of hosting one SwitcherB ASIC [87] and one SwitcherS ASIC [118]. It essentially serves as a connection hub which enables an easy access to the switching channels that are packed with high integration density on mentioned ASICs. Both switcher ASICs are suitable for the dynamic measurements performed in the scope of this thesis. However, to fully control the SwitcherB ASIC the additional implementation of JTAG communication is needed. As this adds an additional layer of complexity to the system, only the SwitcherS was used. Summation of its complete functionality can be found below, and it follows ref. [147].

As the SPIX measurement system is intended for the use with only a handful of pixels at once, the full potential of the switcher ASICs is not realized on the Switcher child PCBs. The SwitcherS part of the PCB is limited to control a maximum of 18 gate and clear rows, whereas the limitation on the SwitcherB is set at number 15.

SwitcherS ASIC The SwitcherS ASICs are produced in the AMS 0.35 μm HV CMOS technology. They feature 64 channels with two ports, A and B, per channel. The control over the channels and its ports is performed by a combination of:

- The 64 bit bidirectional shift register – each bit in this register is associated to a certain channel with the logic that the bit value 1 selects the associated channel for switching. Bit or bits in the shift register that have the value 1 are called active bits, and the corresponding channels are called activated channels.
- The *clock* and *serial.in* digital signals – the *clock* is used for shifting of the active bits by one position in the shift register, and the level on *serial.in* sets the state of the now vacant first bit in the shift register. The direction of shifting is selected through biasing of the corresponding configuration inputs.
- The *load* digital control signal – used to transfer the state of the channel from the shift register to the integrated logic controlling that channel.
- Two digital control signals – one digital control signal controls the output state of the port A in all activated channels, and the other digital control signal does the same for the output state of the port B in all activated channels.

All A ports share the two input voltages between which they switch their output level, and the same goes for all B ports. The difference between the two input voltage levels on both ports can be of the order of 30 V [118]. The switching rise time is on the order of a few ns [148] and its settling time is below 20 ns [118]. By default, ports of all inactive channels are in their OFF states. Which of the two input voltages corresponds to the OFF state, and which to the ON, on each port is set by applying the required biasing level to the corresponding configuration inputs.

By clocking through the shift register one by one a rolling shutter mode of operation can be achieved (sec. 3.1.3), and by correctly applying the levels on the two digital control signals all operation modes described in sec. 3.1.2 can be realized.

5.1.2.2 Readout child PCB

In regards to the DePFET's drain readout method (sec. 3.1.4) with readout ASICs: there are only two that support it, one being the highly specialized DCD ASIC, and the other the VERITAS ASIC [119]. The former is specialized for speed and not precision, and it also includes the ADC unit – these features make it undesirable for an in-depth analysis, as its 8 bit digitizing resolution is too low and the direct digitization makes it impossible to track the original analogue signals. Consequently, the DCD ASIC was not used in combination with the SPIX system. The ideal option for the SPIX system would be the VERITAS ASIC. It is sufficiently fast, with a low level of noise, and multiple

debugging features. The purpose of that ASIC is to amplify the input signal of each connected pixel, perform the correlated double sampling and multiplex the results to a single analogue differential output which has to be digitized at a later stage. However, the VERITAS ASIC was not developed for such high input signals as are the case with EDET DH80k DePFET's. It can only work with $25\ \mu\text{A}$ of the input signal current (I_{SIG}), which is way below the planned I_{SIG} of the EDET DH80k pixels (Fig. 3.14a). In addition, both ASICs provide a much higher number of channels (respectively 256 and 64) than required for the SPIX based investigations.

The chosen solution for a given problem was to create the discrete drain current readout board (DROB) from of-the-shelf components. The complete electrical circuitry for a single pixel readout is presented in Fig. 5.6. The first stage of circuitry and its transfer characteristic was already described in sec. 3.1.4 (Fig. 3.7). The second stage OpAMP is added to convert the single ended analogue signal, from the first stage, to the differential one in order to avoid the pickup that can occur in analogue transmission lines. The DROB child PCB and its circuitry was designed by A. Bähr, and afterwards qualified with different OpAMPs in the scope of this work. Due to the relatively big sizes of of-the-shelf components and space constraints of the readout board, the DROB comprises of four identical electrical circuits (Fig. 5.6). Consequently, only four pixels can be simultaneously connected to it.

The analogue signal after the first stage ($U_{1\text{st}}$) is calculated as described in eq. 3.11. In addition to converting the single ended signal to a differential one, the second stage can also influence the gain of the circuitry via the input ($R_{2, \text{IN}}$), feedback ($R_{2, \text{F}}$) and termination (R_{T}) resistors. Generally, the signal after the second stage OpAMP ($U_{2\text{nd}}$) is calculated as

$$U_{2\text{nd}} = \frac{R_{2, \text{F}}}{R_{2, \text{IN}}} U_{1\text{st}} . \quad (5.1)$$

To convert the $U_{2\text{nd}}$ to the U_{OUT} it is necessary to know the size of the termination resistor inside the ADC. Two general termination options are either low ohmic, for instance, $50\ \Omega$ or high ohmic, for instance, $1\ \text{M}\Omega$. In combination with $50\ \Omega$ termination resistor, the $U_{\text{OUT}} = 0.5U_{2\text{nd}}$ in the low ohmic case, and $U_{\text{OUT}} = U_{2\text{nd}}$ in the high ohmic one.

Components used in the first stage of DROB circuitry For the first stage $I-U$ converter an ADA4817 OpAMP [149] was selected after being tested against the THS4631 [150], THS4151 [151] and THS4141 [152] OpAMPs. It features low input noise and a huge operation window of $\pm 5\ \text{V}$, which can cope with high signal currents from the DePFET's even when coupled with the relatively big feedback resistor (R_{F}) of $50\ \text{k}\Omega$. For the system's ENC the bigger resistor values are preferred, as the resistor current noise contribution scales as $1/R$ (sec. 3.2.2). Other components from the first stage were a $100\ \text{k}\Omega$ subtraction resistor (R_{SUB}), a $100\ \Omega$ drain resistor (R_{D}), and a $2\ \text{pF}$ feedback capacitor (C_{F}).

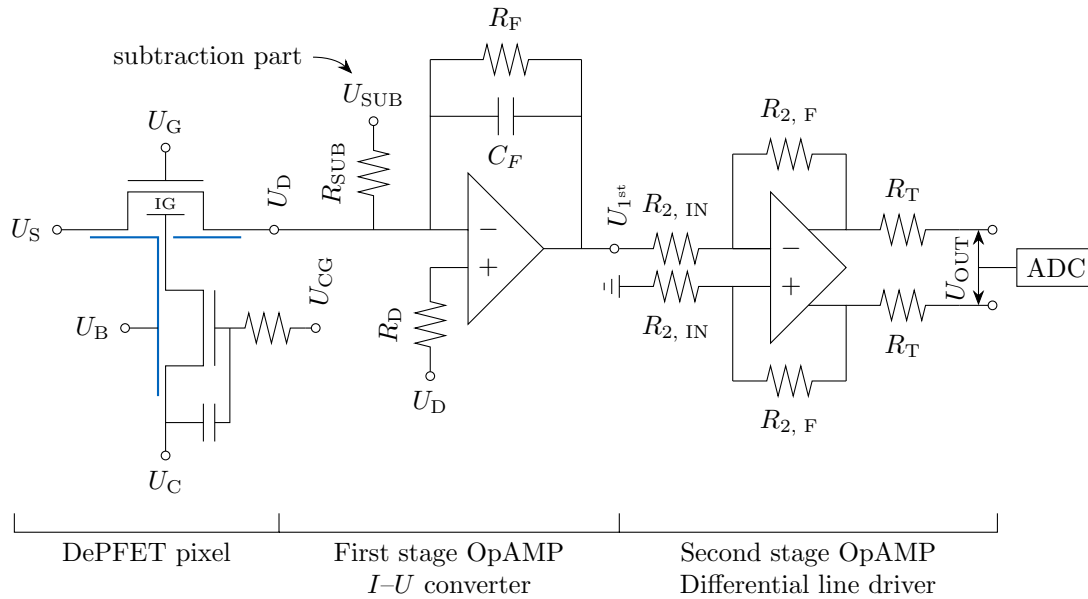


Figure 5.6: Complete electrical schematic of a single pixel readout chain.

Components used in the second stage of DROB circuitry For the second stage differential line drive an AD8138 OpAMP [153] was chosen due to its low distortions, matching operational range to the first stage, and good previous experiences of A. Bähr. As the U_{1st} was amplified enough no further gain changes were necessary and consequently the $R_{2, IN}$ and $R_{2, F}$ were all populated with 1 k Ω resistors. The 50 Ω termination resistors were selected to match the impedance of the cables and ADC in order to minimize signal reflections.

5.1.2.3 Radiation sources

In the scope of this thesis two different radiation sources were used to stimulate the pixels. The first source was an encapsulated radioactive isotope iron-55 (^{55}Fe). Because of its relatively low X-ray energies the ^{55}Fe is relatively safe to handle, and is consequently often used for the energy calibration of radiation detectors. However, due to the specific non-linear response of the EDET DH80k DePFET sensor and statistical nature of X-ray emissions, a ^{55}Fe source alone is not enough for energy calibration of the complete dynamic range. Therefore, the second radiation source, a pulsed linear high-speed LED, was used for energy calibration of the complete dynamic range.

Radioactive isotope iron-55 ^{55}Fe is a radioactive isotope that decays to a stable isotope manganese-55 (^{55}Mn) with a half life of 2.747 years. The decay happens via the process of electron capture [33] which leaves a vacancy in one of the isotope's inner shells. The vacancy is soon-after filled by one of the higher shell e^- (sec. 1.1.2.1) and the excess energy is released through the emission of a characteristic X-ray or through the ejection

of an Auger electron.² As the source is encapsulated in a stainless steel body with a beryllium window, only the characteristic X-rays can escape. The respective energies of characteristic X-rays used in this thesis are 5.895 keV and 6.490 keV for the K_α and K_β lines (Fig. 1.9), with their emissions ratio (K_β/K_α) being 0.136. A complete overview can be found in ref. [154].

Linear high-speed LED Single K_β X-ray from the ^{55}Fe source generates on average 1773 e^-/h^+ pairs in the Si bulk (eq. 2.4). With this the charge storage regions of the EDET DH80k pixel design are filled only to about 0.2% of the minimum planed charge handling capacity of 800 ke^- . In order to measure the response function beyond the K_β line a linear high-speed LED source was employed. The design and qualification of the circuitry used is presented in ref. [155]. In order to achieve these fast optical rise and fall times, the turn-on and turn-off of the LED are respectively supported with one capacitor and one inductor. Additionally, the switching of the LED does not rely on an externally generated voltage pulse, but is switched directly on the circuitry by a transistor [156] that is connecting the LED's cathode side to the ground. The complete control chain is as follows: sequencer (Fig. 5.5) triggers the pulse generator (Fig. 5.5) which in turn triggers the transistor driver [157] that controls the above mentioned transistor which controls the LED.

The circuitry was used with two LEDs featuring different wavelengths. One was an infrared LED with a peak wavelength of 850 nm [158], and the other was a green LED with a peak wavelength of 520 nm [159]. The reason behind using two different wavelengths was in different absorption properties. Photons from the former leave their footprint throughout the complete thickness of thin devices (following the Beer-Lambert's law, eq. 1.17) whereas the latter one is almost fully absorbed in first few μm of Si.

5.2 Characterization of single pixel devices

In this section the methods and results from both the quasi-static and the dynamic characterization measurements performed on single pixel devices (SPDs) will be presented.

5.2.1 Transfer characteristics

Quasi-static measurements, presented in this section, were performed on the SPDs from PXD10-1 production by the use of the generalPCMS and customPCMS measurement systems. The measurements, biasing conditions and their respective sweeps performed with the former measurement system are shown in Tab. 5.1, whereas Tab. 5.2 shows the same for the latter system. Measurements in those two tables are named after the DePFET contact which is quasi-statically varied. The optional appendix 'linear' infers to a linear mode of operation. If the appendix is omitted the measurement is performed in the saturation mode of operation.

²Excluding the extremely rare events of gamma emissions.

Table 5.1: Biasing of quasi-static measurements performed on the SPDs with the generalPCMS. The three numbers in one cell indicate the start, stop and step size of the sweep range for the indicated quasi-static voltage sweep measurement.

	U_S	U_D^a	U_G	U_{CG}	U_C	U_{CE}	U_{DRI}
	[V]	[V]	[V]	[V]	[V]	[V]	[V]
gate sweep linear	0	-0.50	(2, -5, 0.2)	5	15	NC	-3
gate sweep	0	-5.00	(2, -5, 0.2)	5	15	NC	-3

^a Only the drain under investigation is biased and the rest are floating.

Table 5.2: Biasing of quasi-static measurements performed on the SPDs with the customPCMS. The three numbers in one cell are indicate the start, stop and step size of the sweep range for the indicated quasi-static voltage sweep measurement. For all measurements the CE was biased at 10 V, and the drift was not connected due to the issues described in sec. 4.3.

	U_S	U_D^a	U_G	U_{CG}	U_C
	[V]	[V]	[V]	[V]	[V]
gate sweep linear	0	-0.25	(1, -2, -0.025)	5	15
gate sweep	0	-5.00	(1, -3, -0.025)	5	15
clear gate sweep	0	-5.00	2	(-1, -5, -0.05)	10
clear sweep	0	-5.00	varied ^b	5	(0, 20, 0.1)

^a Drains from all DePFET pixels are biased.

^b The DePFET needs to be biased in the readout mode for this measurement. Due to multiple different gate lengths implemented in a single SPDs array, different gate voltages are required; -2.50 V was used for the 3.8 μm gate length group, -3.00 V for the 4.8 μm , and -3.50 V for the 5.8 μm .

Initial plan for the SPDs was that the majority of the work would be done in the dynamic operation mode. Consequently, only the gate sweeps in both linear and saturation mode of operation were performed on all SPDs with the generalPCMS. In order to speed up the measurements, a coarse granularity of 0.2 V big steps was selected to determine if the devices are working as expected, or not. However, the plan for the SPDs changed when their problems were revealed (chapter 4). Therefore, all unused SPDs at that point were connected with the customPCMS and remeasured with finer granularity. The measurements themselves are presented in the following subsections.

The gate sweep measurements were used in order to evaluate the following parameters: the threshold voltage (sec. 5.2.1.1), the OFF state drain current and the subthreshold voltage swing (sec. 5.2.1.3), and the yield of pixels (sec. 5.2.1.5). The clear gate sweep

measurements were used to evaluate the threshold voltage (sec. 5.2.1.2) and the sub-threshold voltage swing (sec. 5.2.1.3) parameters of the parasitic channel that connects source and drain underneath the clear gate structure. The clear sweep measurements were used to evaluate the IG potential (sec. 5.2.1.4).

5.2.1.1 Threshold voltage

The threshold voltage (U_T) is one of the fundamental MOSFET parameters. It quantifies at which point, under the specific biasing conditions, the drain current draw in a transistor becomes significant. The position of this point can vary due to a different underlying definition or a different method of extraction. One simple definition of the drain current versus gate voltage behaviour (I_D vs. U_G) was already presented in sec. 2.3 with the final result being eq. 2.22.

Fig. 5.7 shows the measured I_D vs. U_G behaviour of all 24 DePFET pixels located on the W10 BR 80k2 SPD in linear and saturation region. For those measurements, the clear transistor of the DePFET pixel is biased so that the IG is always empty, i.e., the clear gate (CG) and clear nodes are positive enough so that all e^- generated in the bulk are collected by the clear contact, and the DePFET behaves as a MOSFET. The exact biasing values for Fig. 5.7 are shown in Tab. 5.2 under the 'gate sweep linear' for the linear region of operation and under the 'gate sweep' for the saturation region of operation. Three groups of eight different curves represent the three groups of pixels with different gate lengths implemented on the SPD. The measurements were performed with the customPCMS.

The evaluation of the U_T from the definition (sec. 2.3.1) is very straightforward in both operation regimes. In the linear regime one works with the I_D vs. U_G characteristics and in the saturation regime with the $I_D^{0.5}$ vs. U_G characteristics. In both cases a linear extrapolation at the maximum slope is made to the point of crossing the $I_D = 0\mu A$ axis. For the saturation regime the crossing point is defined as the U_T , and the complete procedure is called linear extrapolation method in the saturation operation region (ESR). In the linear regime, however, the crossing point needs to be shifted by an additional $U_D/2$ in order to obtain the U_T . The procedure in that case is called linear extrapolation method in the linear operation region (ELR). An example of the U_T extraction by both methods is shown in Fig. 5.8.

There exists a small deviation between described methods for the U_T extraction and their implemented version in programming. In the description an ideal behaviour is assumed and a tangent for linear extrapolation can be drawn from a single point at the maximum slope. However, in reality this would lead to a high sensitivity of extracted U_T to the measurement noise. In order to circumvent this problem a fit range is selected and upon it the linear regression is performed in order to obtain the tangent. As the ELR and ESR methods rely on the linearity, the fit range is selected as the flattest part of the first order derivative. In case of the ELR the first order derivative yields the transconductance

$$g_m = \frac{dI_D}{dU_G}, \quad (5.2)$$

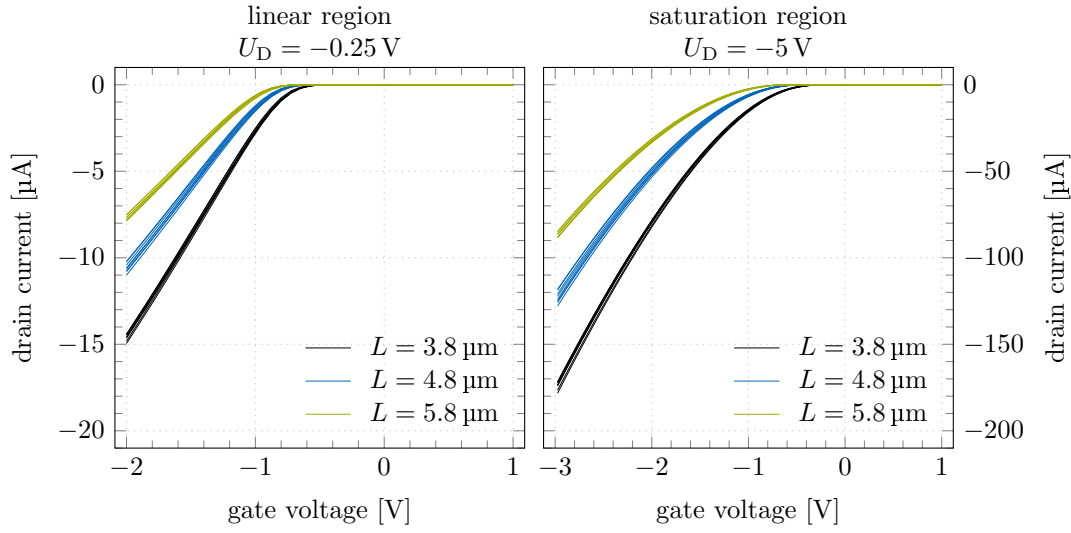


Figure 5.7: The drain current vs. gate voltage characteristic for 24 pixels, 8 from each unique gate length group, from the W10 BR 80k2 SPD measured with the customPCMS; linear operation mode (left), saturation operation mode (right). Complete biasing conditions are gathered in Tab. 5.2.

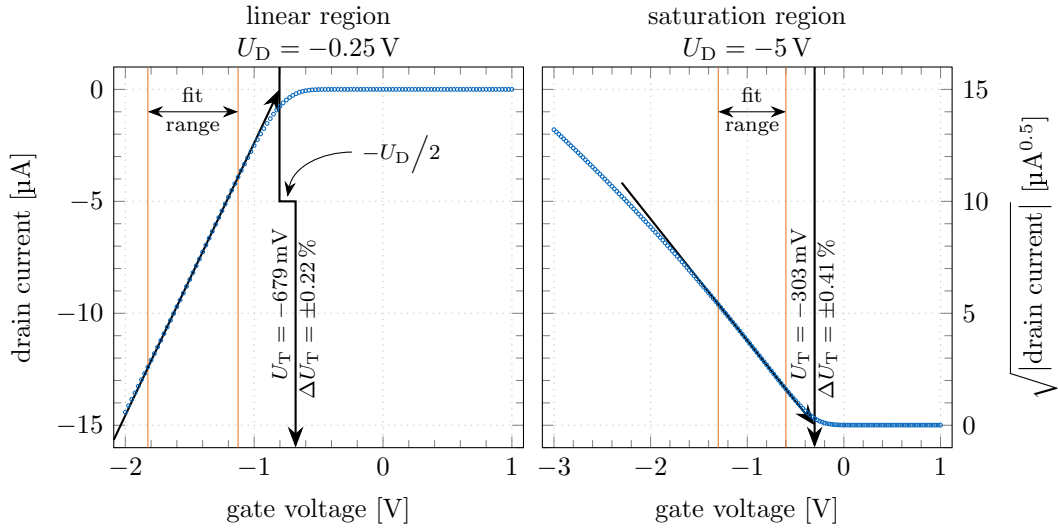


Figure 5.8: Example of the U_T extraction; linear region with the ELR method (left), and saturation region with the ESR method (right). The data points are for the pixel 0 from the W10 BR 80k2 SPD.

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whereas in the ESR it has no physical meaning. The flatness condition was set to be a minimum of 90 % of the absolute maximum value of the first order derivative. For the ELR this can be written as

$$\text{fit range} = [0.9 \max(|g_m|), \max(|g_m|)] ,$$

which means that all measurement points selected with the above range are used for the linear regression.

Two additional methods that were also tested in the scope of this thesis are graphically presented in Fig. 5.9. They are namely the transconductance linear extrapolation method and the second derivative method [160, 161]. In the former method the U_T is

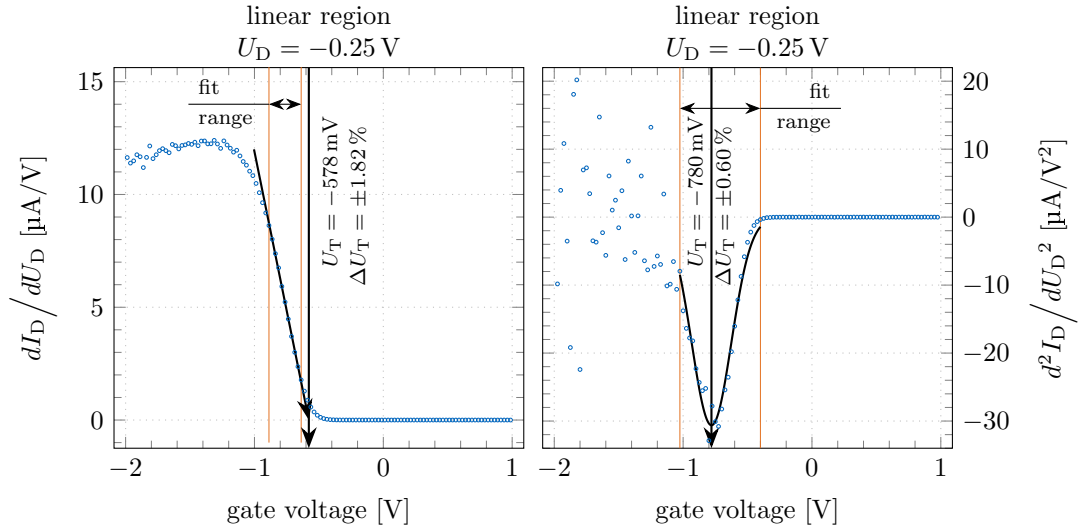


Figure 5.9: Examples of the additional U_T evaluation methods tested in the scope of this thesis; transconductance linear extrapolation method (left), second derivative method (right). The data points are for the pixel 0 from the W10 BR 80k2 SPD.

defined in the same way as with the ELR and ESR as a point where the tangent at the maximum slope crosses the x-axis, and with the derivative method the U_T is defined as the point where the second derivative is at the minimum. For the latter method the minimum is extracted from the Gaussian fit that is interpolated on the data points inside the fit range. The fit range is selected between the first measurement point where the I_D is smaller than -1 nA and the point that is located at 250 mV more negative gate voltage than the minimum of d^2I_D/dU_D^2 . Those two methods, however, proved to feature higher sensitivity to the measurement jitter and required more manual interactions when automatically analysing big dataset of pixels. The methods of choice for the U_T comparison over different devices therefore became the ELR and ESR methods. Inclusion of all methods in this work was to show the ambiguity of the U_T definition. Three methods used to extract the U_T from the linear operation region yield three different values that are separated beyond the extraction error. The same is true for compari-

son with the ESR method which is used when the DePFET structure is biased in the saturation regime.

Measurement errors Measurement errors arising from the 4200-SMU are not included on the plots in this section, as their size is much too small to be seen. Neither are they included in the analysis as their influence on the evaluated parameter is minuscule. Consequently, all measurement points in the fit ranges contribute to the result with an equal weight. Additionally, interesting part is in the comparison of evaluated parameters from multiple pixels or even SPDs. The width of such distribution will be influenced by the manufacturing process variations much more, than from the measurement errors. The U_T for new devices is generally a function of the following parameters [113]:

- Oxide capacitance (C_{OX}) – scales only with the oxide thickness which is very well defined and homogenous over the complete wafer. Consequently, no major contribution to the variations as well.
- Gate length (L) – measurements show a mean sigma deviation (σ_L) of 40 nm in the gate lengths. The devices with shorter L inhibit larger relative deviations which represents itself in larger U_T spreads [162].
- Doses of the MDDN and LDSP implantations (D_{MDDN} and D_{LDSP}) – the implanter used to create the mentioned implantation is generally very precise with mean sigma deviation of around 1% [162]. However, those two implantations effectively compensate each other, and consequently a small variance in the two can lead to a significant shift in the U_T . With $1.3 \cdot 10^{12} \text{ cm}^{-2}$ and $0.9 \cdot 10^{12} \text{ cm}^{-2}$ for the D_{MDDN} and D_{LDSP} the above mentioned mean sigma deviation grows to the level of 4% after effective compensation [114].
- Interface charge due to sputtering³ (Q_S) – sputtering can cause charge build-up in oxide which shifts the measured U_T . If it is not uniform, devices from different positions can exhibit different U_T .

Variances in the above parameters that stem from the manufacturing process are the reason that the 4200-SMU measurement errors can be neglected.

Results In this part, the U_T results from the measurements described above will be presented. As the final plot is dense with information, there is an introductory plot (Fig. 5.10) compiled only from the 'gate sweep' measurements (Tab. 5.2) performed with the customPCMS on the SPDs from the wafer W09. On it are four fully measured SPD dies (namely BL, BR, MR, TL) which expand to eight measured SPD arrays from different die quarters (four 80k1 and four 80k2). The remaining SPD dies (namely ML and TR) were not available for tests with this measurement system.

Each of the measured SPDs is represented in its own separate column, and in every column there are three differently coloured box plots representing the groups of pixels

³Physical process used in a multitude of steps in the production process of DePFETs. Used for deposition of very thin layers of material onto the surface. Details in ref. [88]

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with unique gate lengths. The black one (—) is for the gate length of $3.8\ \mu\text{m}$, the blue one (—) for $4.8\ \mu\text{m}$, and the green one (—) for $5.8\ \mu\text{m}$. The graphical explanation of different box plot components is shown with a single orange coloured box plot (—) in the upper left part in figure:

- First quartile (Q1) – 25th percentile of the dataset.
- Median – the middle value of the dataset, i.e., 50th percentile of the dataset.
- First quartile (Q3) – 75th percentile of the dataset.
- Whiskers – calculated from the interquartile range (IQR) that is defined as $Q3 - Q1$. The whiskers span from the first to the last data point inside the $[Q1 - 1.5\text{IQR}, Q3 + 1.5\text{IQR}]$ range, with the first data point named the minimum (min), and the last the maximum (max).
- Outliers – all data points that are beyond the limits set by whiskers.

All quartiles were calculated with the percentile function from the NumPy Python3 package. As the sample sizes are very small the box plot representation was chosen as opposed to the usual $\text{mean} \pm 1$ standard deviation representation. Due to the small

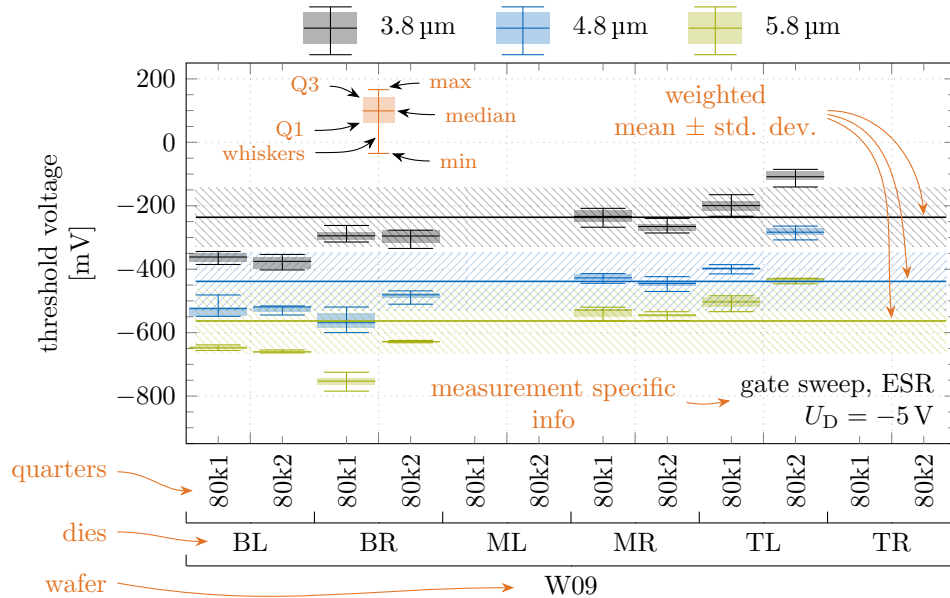





Figure 5.10: Threshold voltage results from the 'gate sweep' measurements performed with the customPCMS on all SPDs from the wafer W09. For each die there are two columns representing the quarters – 80k1 and 80k2. Different colours represent pixels grouped together by their gate lengths. Empty columns represent the SPDs that were not available for the measurements with the named measurement system. Explanation of a box plot is presented with a single orange coloured box plot (—) in the upper left part of figure, and is further explained in the text around figure. Additionally, mean ± 1 standard deviation bands are added for each pixel group in their respective colours with ,  and .

sample size the mean value can significantly deviate from the median value already because of one statistical outlier.




From all single measurements gathered together in the box plots, the weighted mean and standard deviation values [33] are calculated wafer-wise for each pixel gate length group.⁴ They are plotted on top of everything as mean ± 1 standard deviation bands with ,  and .

Fig. 5.11 shows two complete overviews of the U_T results from measurements performed with the customPCMS are shown. The upper plot shows the results from the

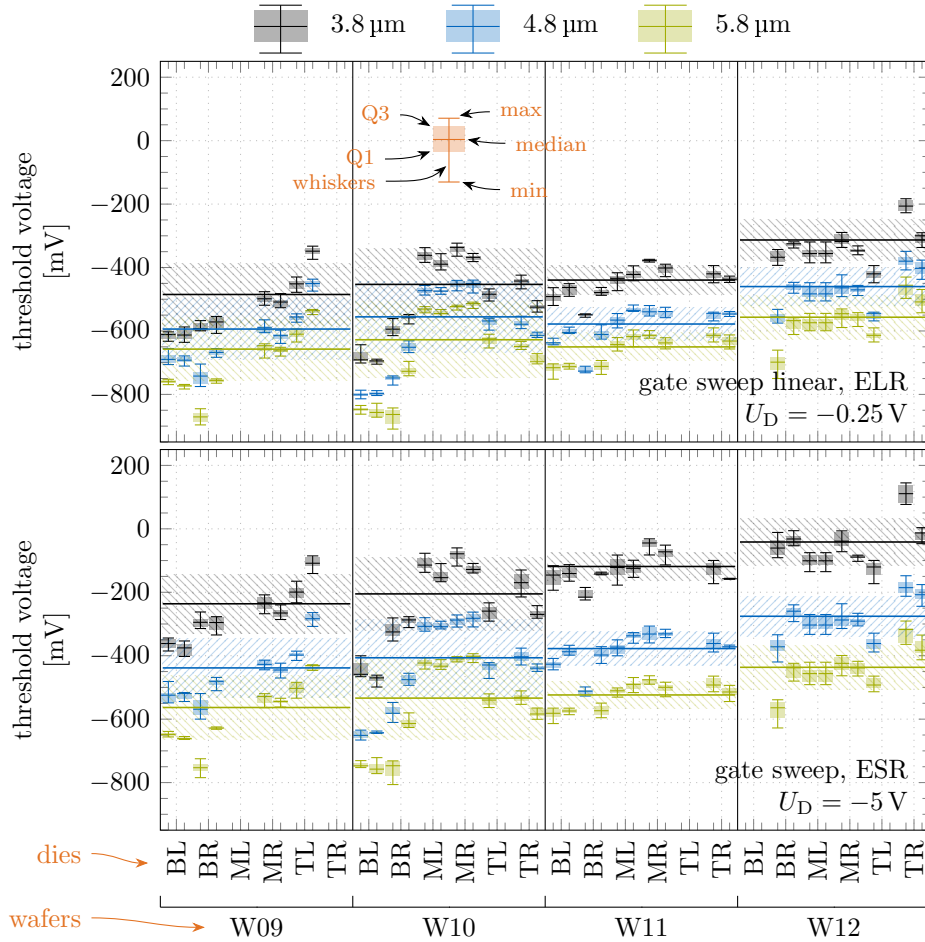


Figure 5.11: Threshold voltage results from the 'gate sweep linear' (upper) and 'gate sweep' (lower) measurements performed with the customPCMS on all available SPDs across four wafers. The quarter layer of x -axis is removed in order to avoid cluttering. Each die still has two columns where the left one represents the 80k1 quarter and the right one the 80k2 quarter of the die. The weighted mean and standard deviation values are gathered in Tab. 5.3.

⁴As weights the extraction errors (ΔU_T) presented on U_T extraction plots are used.

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'gate sweep linear' measurements obtained by the ELR method, and the lower plot shows the results from the 'gate sweep' measurements obtained by the ESR method. There are now four plots like the one shown in Fig. 5.10 placed side by side. In order to avoid cluttering the x -axis, the names of the quarters were removed from it, but the data structure remained the same. This means that for every SPD die there are still two columns in which the measurements from two different quarters are located. The left one represents the 80k1 quarter, and the right one the 80k2.

The results for mean and standard deviation values from the threshold voltage measurements in both operation regimes are gathered in Tab. 5.3. As all U_T values are between 0 V and -1 V this already yields one of the positive results for this production, since the parameters used for the PXD10-1 production were set so that the U_T of unirradiated pixels would be around 0 V. The reason for this is better radiation hardness as shown in ref. [163].

Three additional analyses will be made with the results presented in Fig. 5.11. Firstly, the dependence of the U_T on the gate length will be checked. Secondly, the correlations between the U_T results obtained in both measurement regimes will be investigated. And lastly the position dependent variations in the U_T will be examined, since the standard deviation values in Tab. 5.3 suggest a different behaviour between the SPDs from the SOI and standard wafers. First part will be performed because the presented simple MOSFET theory does not predict the U_T dependence on the gate length. Whereas the

Table 5.3: Mean ($\overline{U_T}$) and standard deviation (σ) values as obtained from the measurements presented in Fig. 5.11.

	3.8 μm		4.8 μm		5.8 μm	
	$\overline{U_T}$	σ	$\overline{U_T}$	σ	$\overline{U_T}$	σ
	[mV]	[mV]	[mV]	[mV]	[mV]	[mV]
gate sweep linear; $U_D = -0.25$ V						
W09 (SOI wafer)	-485	(± 99)	-594	(± 95)	-657	(± 100)
W10 (SOI wafer)	-453	(± 113)	-556	(± 112)	-628	(± 120)
W11 (standard wafer)	-440	(± 46)	-578	(± 52)	-650	(± 44)
W12 (standard wafer)	-313	(± 66)	-460	(± 60)	-557	(± 70)
gate sweep; $U_D = -5$ V						
W09 (SOI wafer)	-236	(± 93)	-438	(± 92)	-563	(± 102)
W10 (SOI wafer)	-205	(± 116)	-406	(± 122)	-534	(± 129)
W11 (standard wafer)	-119	(± 45)	-378	(± 54)	-524	(± 41)
W12 (standard wafer)	-42	(± 74)	-276	(± 64)	-437	(± 69)

other two parts will be performed to check for the differences between the two SOI and standard wafer types in the PXD10–1 batch production.

Gate length dependence of the threshold voltage As stated, the definition used to derive the U_T (eq. 2.17) does not predict its dependence on the gate length. This is because the definition does not include any short-channel effects. However, the device is considered short when the channel length is of the same order of magnitude as the depletion depths caused by source and drain [164]. The built-in depletion depth, as calculated in sec. 2.2 for the devices used in this thesis, is on the level of 10 μm . Consequently, all devices used in the scope of this thesis are in fact short-channel devices. In order to explain the dependency of the U_T in the linear regime, the charge-sharing model [165] can be used. In it the edges of the channel depletion region are overlapping the depletion regions formed by source and drain. This means that there is less stationary ions that belong to the channel. Consequently, in order to bring the channel to inversion one needs to induce less charges carriers by the gate potential. The effect is scaling with channel length. The shorter the channel the bigger is the effect of the overlap, and vice versa. As seen in Fig. 5.11 and also predicted with the charge-sharing model, the U_T becomes less negative with the decrease of the gate length, as effectively less charge carriers are needed to bring the channel to inversion. By increasing the voltage difference between source and drain nodes, another effect can influence the U_T – the drain-induced barrier lowering [88, 90]. This effect causes the lowering of potential barrier between source and drain nodes due to the high potential at the drain side. The smaller the potential barrier, the higher the subthreshold current and consequently the U_T becomes less negative. The shorter the channel the bigger the effect, and the same is true for higher voltage differences between source and drain nodes.

Correlations between the measurement regimes By calculating and plotting the differences between the U_T measured in the saturation and linear regime

$$\Delta U'_T = U_T \Big|_{\text{saturation}} - U_T \Big|_{\text{linear}}$$

plot as shown in Fig. 5.12 is obtained. The mean and standard deviation values, calculated separately for different pixel groups and different wafer types, are gathered together in Tab. 5.4. The plot shows that the U_T in saturation and linear regimes are simply offset by a mean value ($\overline{\Delta U'_T}$), i.e., they are correlated. This is expected as the measurements from the same pixels are compared to each other. However, two additional observations can be made. First, the standard deviation (σ) size depends on the gate length, and second, there is a $\overline{\Delta U'_T}$ discrepancy between the two wafers types. By comparing the σ values of SOI wafers between different gate lengths, the following scaling factors ($S_{\Delta U'_T}$) are obtained

$$S_{\Delta U'_T} = \frac{\sigma|_L}{\sigma|_{L+1\mu\text{m}}} = 1.481 \Big|_{L=3.8\mu\text{m}} \text{ and } 1.365 \Big|_{L=4.8\mu\text{m}},$$

where L represents different gate length groups. The same can be done for gate length

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variations arising from the manufacturing process variations. The scaling factors (S_L) in that case are

$$S_L = \frac{\sigma_L / (L - o)}{\sigma_L / (L - o + 1 \mu\text{m})} = \frac{L - o + 1 \mu\text{m}}{L - o}.$$

The only unknown in this equation is the so-called offset parameter o which is used to convert the design gate length to the measured gate length.⁵ The difference is that the first is the gate length on the etching mask and the second the actual gate length. For plasma etching at HLL MPG the mean offset is around $0.6 \mu\text{m}$ [113, 162]. The σ_L is the measured mean standard deviation in gate lengths which is $0.04 \mu\text{m}$ [162]. This together yields the SOI wafer S_L scaling factors of

$$S_L = 1.313 \Big|_{L=3.8 \mu\text{m}} \quad \text{and} \quad 1.238 \Big|_{L=4.8 \mu\text{m}}.$$

The missing fractions from the S_L to the $S_{\Delta U'_T}$ scaling factors are 13% in first and 10% in second case. They are most likely caused by the secondary short-channel effects which cause non-linearities. The second difference in Fig. 5.12, the discrepancy in $\Delta U'_T$ between different wafer types, however, should not exist. This is because the front side part of the production process at HLL MPG was identical [113, 162, 166]. The only conclusion that can be drawn from here is that there is a global difference inflicted to the SOI

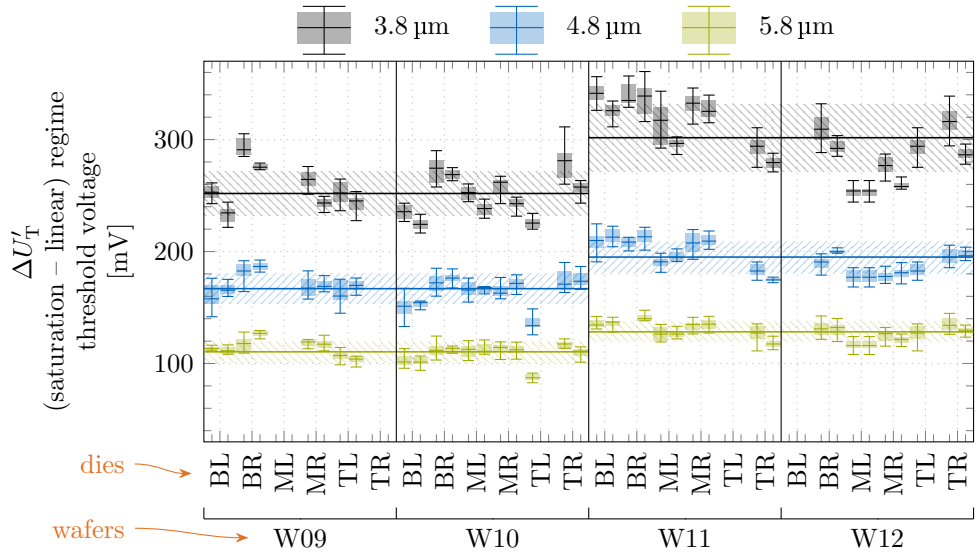


Figure 5.12: Differences between the evaluated U_T measured in the saturation and linear modes of operation in dependence of the gate lengths. The SOI and standard wafer types are treated separately. The mean and standard deviation values are gathered in Tab. 5.4.

⁵All values for the gate length (L) presented in this work are the design values.

Table 5.4: Mean ($\overline{\Delta U'_T}$) and standard deviation (σ) values for the evaluated threshold voltage difference between the saturation and linear mode of operation ($\Delta U'_T$) compared between the SOI and standard wafer types. Numerical results from Fig. 5.12.

	3.8 μm		4.8 μm		5.8 μm	
	$\overline{\Delta U'_T}$	σ	$\overline{\Delta U'_T}$	σ	$\overline{\Delta U'_T}$	σ
	[mV]	[mV]	[mV]	[mV]	[mV]	[mV]
SOI wafers	252	(± 19)	167	(± 13)	110	(± 10)
standard wafers	301	(± 30)	195	(± 14)	128	(± 9)

wafers by external suppliers before they arrive back to the HLL MPG (chapter 4). The global difference can be explained in way of the radiation damage inflicted to the SiO_2 (sec. 3.3). Thereby, positive charges get stuck on the SiO_2/Si interface and cause the U_T shifts.

Position dependent variations of the threshold voltage As shown in the previous paragraph, the gate sweep measurements performed in saturation and linear regime are correlated. Therefore, the following analysis will be performed only on the data set from the saturation regime. Fig. 5.13 shows the test procedure for the position dependent variations of the threshold voltage with two examples. All pixels with the gate length of 3.8 μm from the wafer W09 are shown on the left side in figure, and the same pixel gate

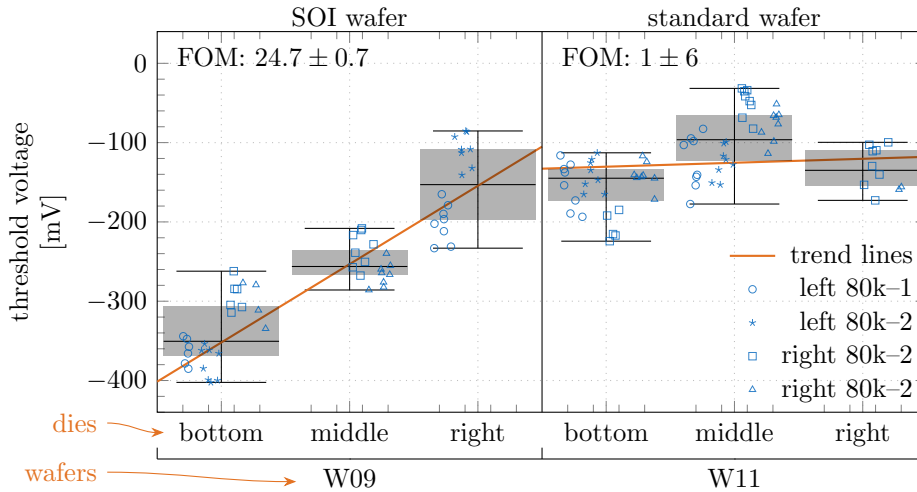


Figure 5.13: Testing for the threshold voltage differences in dependence of the vertical position of SPDs from the same wafer. The two examples are showing very different trend lines that are obtained by performing a linear regression on grouped box plot data from 3.8 μm gate length groups on wafers W09 and W11. The FOM for comparison is the slope of the trend line.

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length group from the wafer W11 is shown on the right. As the testing is done in the vertical direction, the SPDs are grouped together in the following way. All pixels with the specific gate length from BL and BR dies are jointly used to calculate a single box plot labelled bottom. The same is done for pixels from ML and MR dies under the label middle, and for the pixels from TL and TR dies under the label top. Afterwards, a linear trend line is fitted over their median values by the use of linear regression. The slope of the trend line represents the figure of merit (FOM) in the scope of this hypothesis. If there are tiny (statistical) differences between different vertical positions the FOM is small. However, if there are significant first order differences the FOM is increased. The results of this analysis are gathered together in Tab. 5.5. From here another difference between the SOI and standard wafers can be observed. The SPDs from SOI wafers are showing higher FOMs than the ones from the standard wafers. This means that the SPDs located at the bottom of the SOI wafers exhibit more negative U_T than the ones located at the top. The same effect is much less pronounced on standard wafers. In order to explain the differences one would again need to look into the details of SOI wafer manufacturing steps performed at external contractors, as all other steps on the front side manufacturing chain were identical for all wafers. However, big errors of the

Table 5.5: Results for the observed trends in the position dependent threshold voltage differences as explained in Fig. 5.13 caption. The results are obtained by performing the linear regression with the linear trend line. The FOM is the slope of the trend line and error is the error of that same slope.

	3.8 μm		4.8 μm		5.8 μm	
	FOM	error	FOM	error	FOM	error
W09 (SOI wafer)	24.7	(± 0.7)	22	(± 1)	24	(± 3)
W10 (SOI wafer)	15	(± 28)	24	(± 33)	24	(± 33)
W11 (standard wafer)	1	(± 6)	6	(± 7)	9	(± 6)
W12 (standard wafer)	4	(± 8)	13	(± 5)	15.7	(± 0.1)

Table 5.6: Results for the observed trends in the position dependent threshold voltage differences as obtained from the dataset measured with the generalPCMS.

	3.8 μm		4.8 μm		5.8 μm	
	FOM	error	FOM	error	FOM	error
W09 (SOI wafer)	23	(± 6)	22	(± 4)	20	(± 8)
W10 (SOI wafer)	17	(± 24)	24	(± 27)	25	(± 27)
W11 (standard wafer)	4	(± 10)	11	(± 6)	12	(± 7)
W12 (standard wafer)	16	(± 1)	20.2	(± 0.1)	17.0	(± 0.4)

FOM values from the wafer W10, and just three different vertical positions with only a few SPDs at each one, paint this analysis as inconclusive.

In order to shed more light on the root cause of the above observation, the same analysis can be performed on the second dataset that was obtained through the measurements performed with the generalPCMS. The results from that dataset are presented in Fig. 5.14, and its biasing conditions are located in Tab. 5.1. The upper plot is showing the measured U_T with mean ± 1 standard deviation bands for all pixels from the same wafer with identical gate lengths. On average, the measured U_T values from this data set are for $117\text{ mV} \pm 34\text{ mV}$ more positive than the ones measured with the customPCMS. This is shown on the lower plot in Fig. 5.14, where measurement values from quarters that appear in both data sets are subtracted from one another. The difference is due to different biasing and measurement conditions, and as a consequence the datasets are not

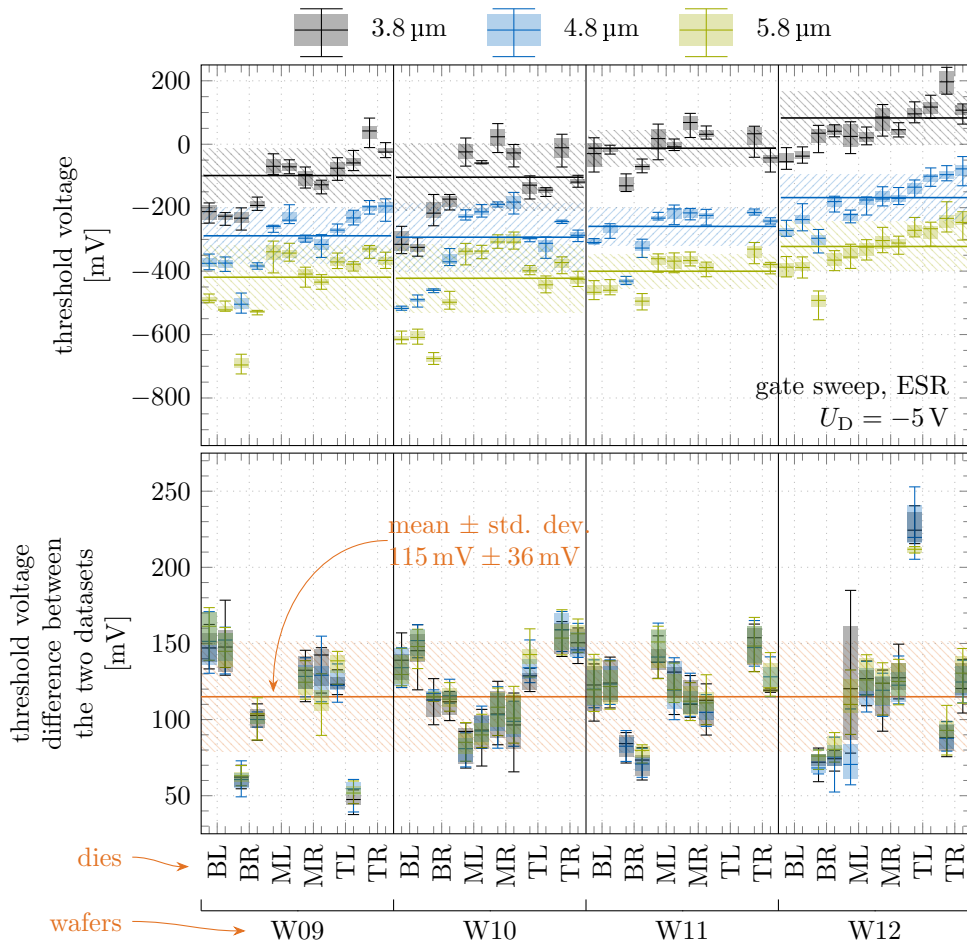


Figure 5.14: Threshold voltage results as obtained with the generalPCMS (upper), and the threshold voltage difference between the datasets obtained with two different measurement systems (lower).

directly comparable between themselves. The trends, however, can still be compared. With the same procedure as explained in Fig. 5.13, the FOM values and their errors are extracted from the second dataset. The results are collected together in Tab. 5.6, and they show that there exist a general trend where devices from the bottom part of wafers exhibit more negative U_T than those from the top. The only wafer that shows smaller variations is wafer W11. The existence of such trend means that one or more of the manufacturing process variations, described under the paragraph named “Measurement errors”, has or have positional dependence. However, due to two different datasets showing different results a more thorough investigation would be needed. That investigation should be carried out with more devices positioned on more than three different vertical positions on the wafer.

5.2.1.2 Parasitic threshold voltage

The clear gate (CG) structure, encapsulating the source and drain implantations, opens up a possibility for a secondary current path between source and drain. This is an unwanted path that opens up if the voltage applied to the CG becomes too negative. In that case an inversion layer is formed underneath it (sec. 3.1.2) and holes can flow from source to drain through that layer regardless to the voltage applied to the gate. The channel that is controlled by the CG is called the parasitic channel. As the CG is global to the complete array, so is its parasitic channel. A small parasitic current on a pixel level can already cause a big global current draw as it is multiplied by the number of pixels in the array. This in combination with very thin devices can lead to an unwanted thermo-mechanical stress which needs to be avoided. Additionally, the current through the parasitic channel also contributes to the overall noise of the detector and can reduce the charge handling capability of pixels. Therefore, this current should be prevented.

As the effect of the parasitic channel scales with the size of the array its effect is mostly negligible in the SPDs. However, those devices can still provide a good studying point for the CG operation voltage limits. In the end, those limits provide a starting point for the investigation of CG limits in bigger devices.

In order to characterize the parasitic current onset point, the so-called ‘clear gate sweep’ measurements were performed (Tab. 5.2). This time the DePFET is biased in the saturation region with the gate fixed in the OFF state while the CG is quasi-statically swept. To avoid the formation of a break-down field on the border between clear implantation and CG, the clear voltage is lowered by 5 V in comparison to the ‘gate sweep’ measurements. From here the parasitic threshold voltage ($U_{T, CG}$) is evaluated in the same way as the U_T via the ESR method. Fig. 5.15 is shows the drain currents arising from the parasitic channel (left) and the ESR method of $U_{T, CG}$ extraction for a single pixel (right). The ESR method is used as the difference between source and drain voltages puts the transistor in the saturation mode of operation. In order to avoid the problems arising from the parasitic channel, the CG should be biased at least 0.5 V above the highest measured $U_{T, CG}$ for normal operation.

The results obtained through the ESR method from ‘clear gate sweep’ measurements are presented on the upper plot in Fig. 5.16. Majority of the SPDs showed a uniform

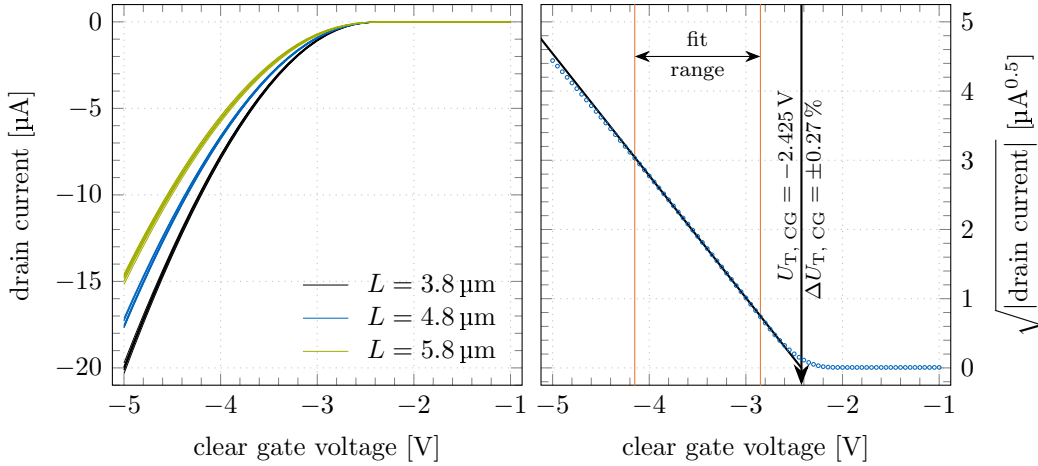


Figure 5.15: Drain current as a function of clear gate voltage for 24 pixels from the W10 BR 80k2 SPD measured with the customPCMS (left), and extraction of the $U_{T, CG}$ for the first pixel from the same device (right). Complete biasing conditions are gathered in Tab. 5.2.

response with a clean transition between the states where both transistors are OFF and where the parasitic transistor starts to conduct. However, a part of the SPDs from the SOI wafer W09 (i.e., BL 80k1, BR 80k1, BR 80k2, and MR 80k1) exhibited a deviating transition between the two states that is not clearly understood at this point in time. Nonetheless, with the mean $U_{T, CG}$ value of (-2260 ± 150) mV all measured $U_{T, CG}$ are negative enough to not cause any problems in the normal operation of DePFETs in the scope of EDET project. This is due to the fact that in the dynamic operation the EDET DH80k devices will have the most negative CG voltage limited to around -1 V, as more negative CG voltages could potentially cause problems with the removal of e^- from the charge storage regions which needs to be avoided. Limits of the CG voltage parameters will be further discussed in sec. 5.3.1.

An additional method through which one can determine the lower operation limit for the CG voltage is through the constant current method [160, 161]. With this method one decides upon an acceptable level of the additional drain current arising from the parasitic channel. By setting the limit to 1% of the base drain current, the per pixel contribution can be calculated. In the case of the main EDET DH80k devices, 128 pixels share the same drain line. This means that the additional $1 \mu\text{A}$ is split over those pixels, and per pixel contribution is roughly 8 nA . The worst case scenario would mean that on a global scale an additional 2.6 mA of current is constantly flowing on top of 205 mA of the active row baseline current.

From the same 'clear gate sweep' the results for a lower operation limit obtained through the constant current method can be extracted without the use of the linear regression. This makes the method much faster. Results of this procedure are presented on the lower plot in Fig. 5.16. In this case the $U_{T, CG}$ values are spread around -2.2 V , which is in accordance to what was measured with the ESR method.

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The mean $U_{T,CG}$ value +5 standard deviations evaluates to the worst case $U_{T,CG}$ voltage that could be featured in some DePFET pixels. At -1.5 V with the ESR method and at -1.3 V with the constant current method, the previously stated most negative limit for the CG voltage of -1 V should prevent all parasitic channels. Therefore, the parasitic channel should not cause any problems in normal operation of the EDET DH80k DePFETs.

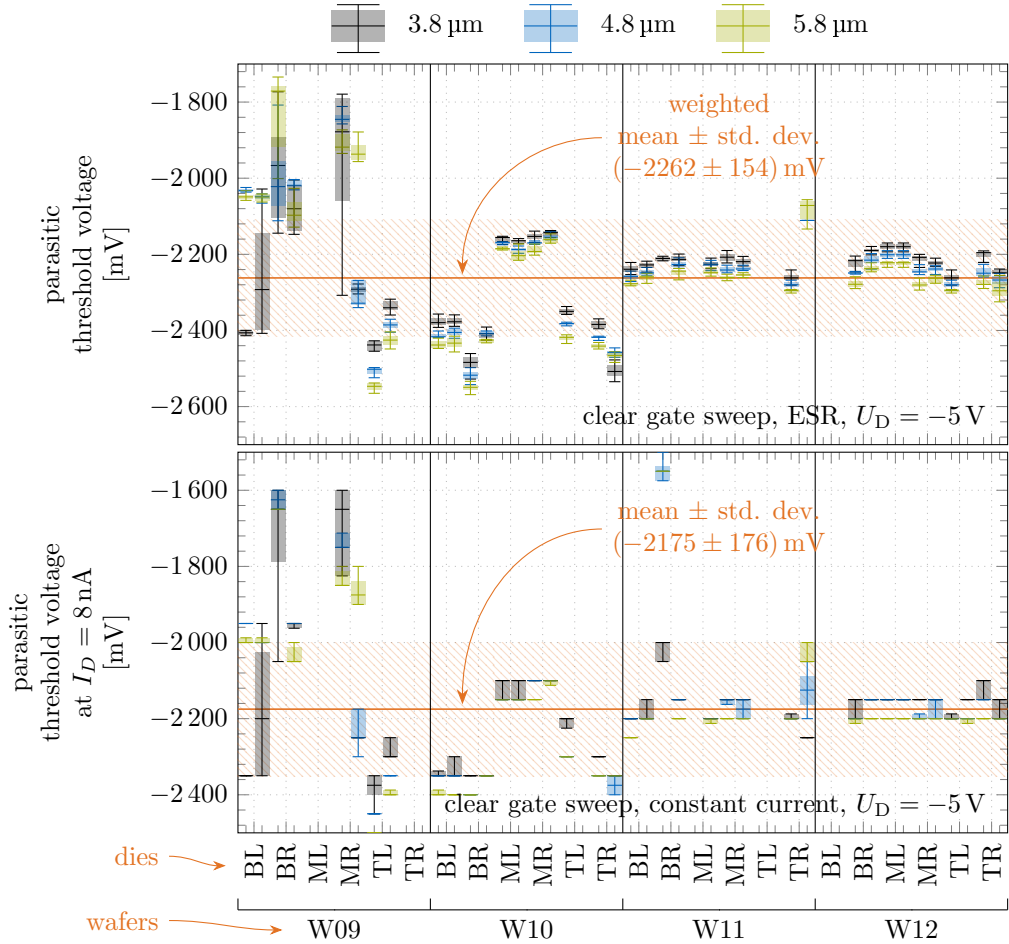


Figure 5.16: The parasitic threshold voltages evaluated from the 'clear gate sweep' measurements performed with the customPCMS on all available SPDs; the ESR method (upper) and the constant current method (lower). The mean ± 1 standard deviation bands are shown on both plots (shaded orange). Some SPDs from the wafer W09 feature more positive $U_{T,CG}$ with bigger spreads. They are commented in the text before the figure.

5.2.1.3 Subthreshold behaviour

The subthreshold region of operation gives two new parameters that can be used to characterize the transistor devices. Despite the fact that the transistor is in its OFF state when gate is biased more positive than the U_T , a tiny drain current between source and drain still exists. This is because in this region the surface is weakly inverted and majority charge carriers that diffuse from the source node have a path to the drain. The first interesting parameter is the level of that current. This determines the OFF state characteristics and tells the minimum level of the current between source and drain when all transistors are in their OFF state. The second parameter is the so-called subthreshold voltage swing (SVS). This parameter defines how quickly the transistor switches between its OFF and ON states, and is measured when the gate is biased in the vicinity of the threshold voltage. It is defined from eq. 2.23 following ref. [90]

$$\text{SVS} = \ln 10 \left[\frac{d(\ln I_D)}{dU_G} \right]^{-1} \Bigg|_{\text{max slope}}. \quad (5.3)$$

Both parameters can be visualised by observing the I_D vs. U_G characteristic in the logarithmic scale. Fig. 5.17 shows the mentioned characteristic for a single pixel as obtained from the 'gate sweep' measurement performed with the customPCMS on the W10 BR 80k2 SPD. The basis for evaluation of both parameters is the fit range. It is initially evaluated as a 0.55 V big interval around the maximum slope. Afterwards, the interval is (if needed) manually adjusted in order to remove the possible artefacts. The best fitting straight line is interpolated on the measurement points inside the determined fit range by the use of the linear regression. Voltage change in one decade of the drain current from that straight line is determined as the SVS. For the OFF state drain current,

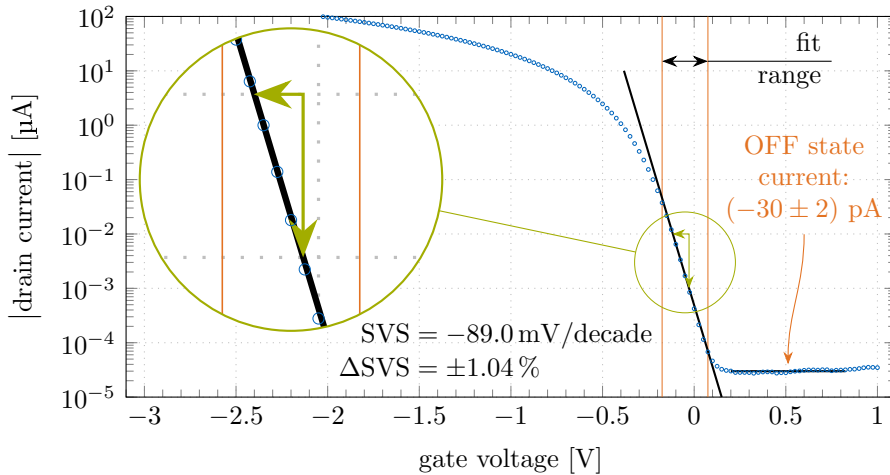


Figure 5.17: Extraction of the SVS and the OFF state drain current parameters from a 'gate sweep' measurement. The data is taken from pixel 0 located on the W10 BR 80k2 SPD.

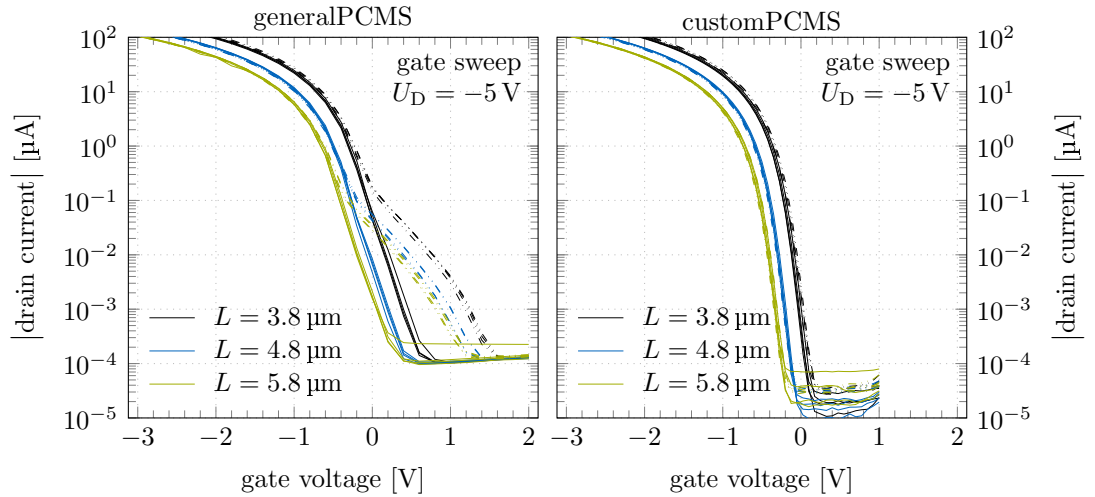


Figure 5.18: Logarithmic plots of drain currents in dependence of the applied gate voltage as measured with the generalPCMS (left) and the customPCMS (right). Three different colours represent three groups of pixels separated by the gate length (L). Two different line styles are used for separation between even and odd pixels (Fig. 4.4a). The full line style (\equiv) represents even numbers and the dash dot dot style (\dashdot) the odd ones. The data is taken from the measurements performed on the W10 BR 80k2 SPD.

median and standard deviation values are calculated on all measurement points that are measured at 0.25 V higher gate voltage than the high limit of the previous fit range. Based on the median ± 1 standard deviation a new interval is selected. All points that are between the first and last point inside the mentioned interval are used to calculate the mean and standard deviation value. Those two values then represent the mean OFF state current and its standard deviation value.

Fig. 5.18 shows the I_D vs. U_G characteristic as obtained from the 'gate sweep' measurements performed with both measurement systems on a single W10 BR 80k2 SPD. The measurements obtained by the generalPCMS (Tab. 5.1) are shown on the left side, and the ones obtained by the customPCMS (Tab. 5.2) on the right. Two differences can be observed. The OFF state drain current is higher with the first system than with the second one. This is due to the differences in biasing conditions during the measurements. With the first system only a single drain is biased and the rest are floating, whereas with the second one there is a much more realistic case where all drains are always biased. The second difference is the strange and unexpected behaviour of the odd numbered pixels that are drawn with the dash dot dot line style (\dashdot). With them, the start of the transition between the OFF and ON state of the transistor occurs roughly 1 V sooner. One probable explanation lies in contact problems. The multi-needle measurements – four manual contact needles and one semi-automatic movable contact needle – were performed on an unstable surface of a gel-pak [167]. Gel-pak is an extremely versatile soft tray without pockets that securely holds bare die (or dies) during the shipping,

handling and processing. However, as the surface of the gel-pak is soft it can easily tilt under pressure. Therefore, when a semi-automatic movable needle, that contacts drain by drain, changes its position it can also change the tilt of the measured SPD. In turn, this can influence the contact quality of the other four manual contact needles, and consequently the biasing conditions. The alternating (even-odd) behaviour can be caused because the drain contacts for even and odd pixels are physically located in two different rows (Fig. 4.4). Different biasing conditions can cause that the IG was not completely emptied on odd pixels. Therefore, when switching the transistor from OFF to ON state, the collected charge causes the transition to happen earlier. But as the transistor starts to conduct and the gate potential is lowered, the IG gets less positive and the collected e^- are cleared away. Consequently, the measured curve from then on follows the same pattern as the ones measured on pixels that do not show this strange artefact.

Due to the problems described above, and additional coarse granularity in voltage sweeps, the measurements performed with the generalPCMS cannot be used in this section. Therefore, all results presented in this section are derived from measurements that were performed with the customPCMS.

OFF state drain current The collected results for the OFF state drain currents are presented in Fig. 5.19. The upper plot shows the complete range of the data and the lower one offers a close up to the region where the results from a vast majority of pixels are located. Few outliers are exhibiting higher levels of the OFF state drain current that scale to the level of a few nA. From the 866 pixels for which the OFF state drain current was measured, only 64 show absolute OFF state currents higher than 200 pA. This is enough to significantly skew the mean value (-148 pA) of the distribution from its median (-54 pA). However, pixels with the high mean value of the OFF state current feature a high variance as well. Consequently, the weighted mean [33] fixes this problem, and the result is the OFF state current of (54 ± 33) pA.

One important thing to note at this point is that for 738 pixels the measured absolute OFF state drain current is smaller than 100 pA. Due to the limitations of the 4200-SMU measurement units, the measurement error in this range starts to dominate the measurements. Therefore, it can be trusted that the OFF state drain currents are small, however the uncertainty of measurements is around 30 pA (sec. 5.1.1).

From these measurements it can be concluded that a fully operational main EDET DH80k device with a single row of pixels activated will see an average additional 19 nA (7 nA) per drain line in case of the mean (median) OFF state drain current. This contribution is superimposed on the active DePFET's offset and signal currents which are at minimum on the order of 100 μ A. Consequently, the OFF state drain current contribution of the non-activate pixels is negligible.

There is no discernible difference between pixels with different gate lengths or devices coming from different wafer types.

Subthreshold voltage swing The 'gate sweep' measurements (Tab. 5.2) were used for the extraction of the SVS parameter, and the upper plot in Fig. 5.20 shows its results.

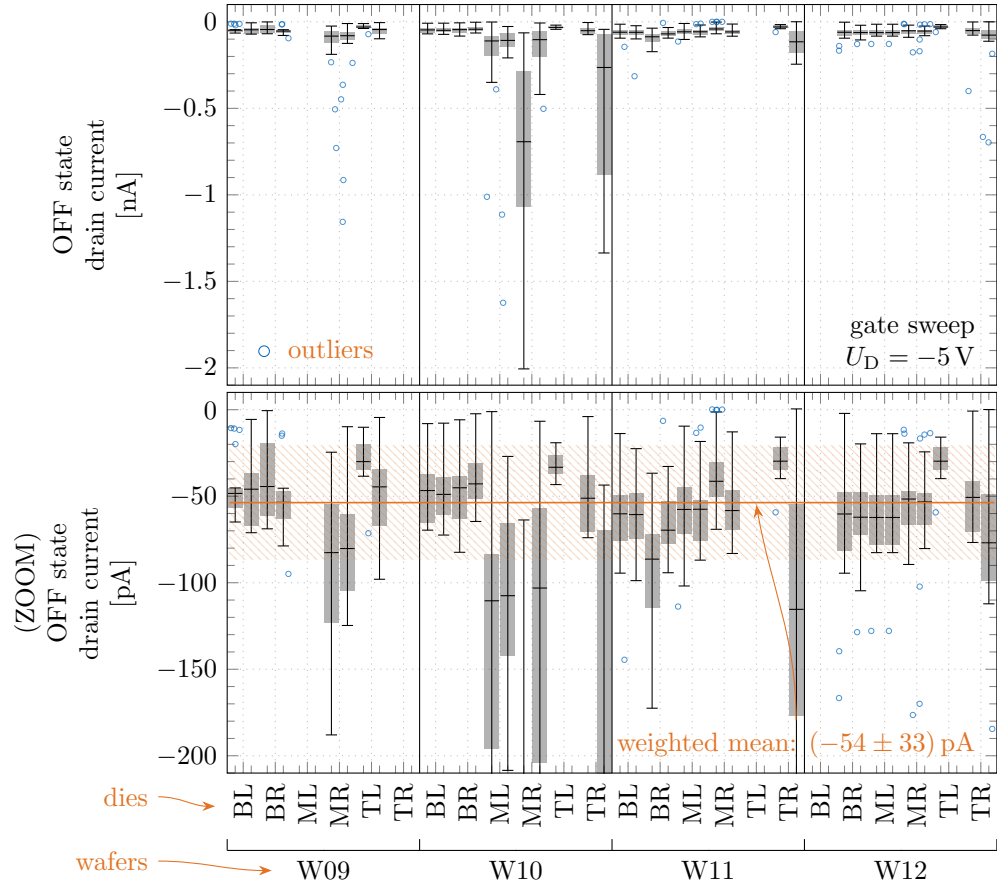


Figure 5.19: Results for the OFF state drain currents from the 'gate sweep' measurements performed with the customPCMS on all available SPDs. The data from all three gate length groups located on a single SPD are grouped to a single box plot. The upper figure is showing the complete data range, whereas the lower one is a close-up to the range where vast majority of data points are located. The weighted mean value with ± 1 standard deviation for the complete measurement is presented with . It is inline with the median value also calculated at -54 pA.

All devices and pixels are exhibiting more or less uniform behaviour spread around the mean value of the (94 ± 7) mV/decade, with the median being 0.5 mV/decade below the mean. This is in line with the typical SVS values that are between $70 \sim 100$ mV/decade at room temperature [88].

The SVS is directly correlated with the number of trap states in the transistor channel, and the amount of trap states is correlated with radiation damage. Therefore, those results offer a view into an unirradiated performance of the devices.

Parasitic subthreshold voltage swing The SVS parameter can also be extracted for the parasitic channel. For this the 'clear gate sweep' measurements (Tab. 5.2) were used and the results are presented on the lower plot in Fig. 5.20. The pixels are again

showing a uniform behaviour over all gate length groups on all SPDs and wafers. The mean value with ± 1 standard deviation is located at (126 ± 16) mV/decade, with the median being 2 mV/decade below the mean. As this is not a proper transistor channel it is good that its switching behaviour is slower compared to the main channel. However, it is not playing any important role as the DePFETs should not be operated in a way where the parasitic channel exists.

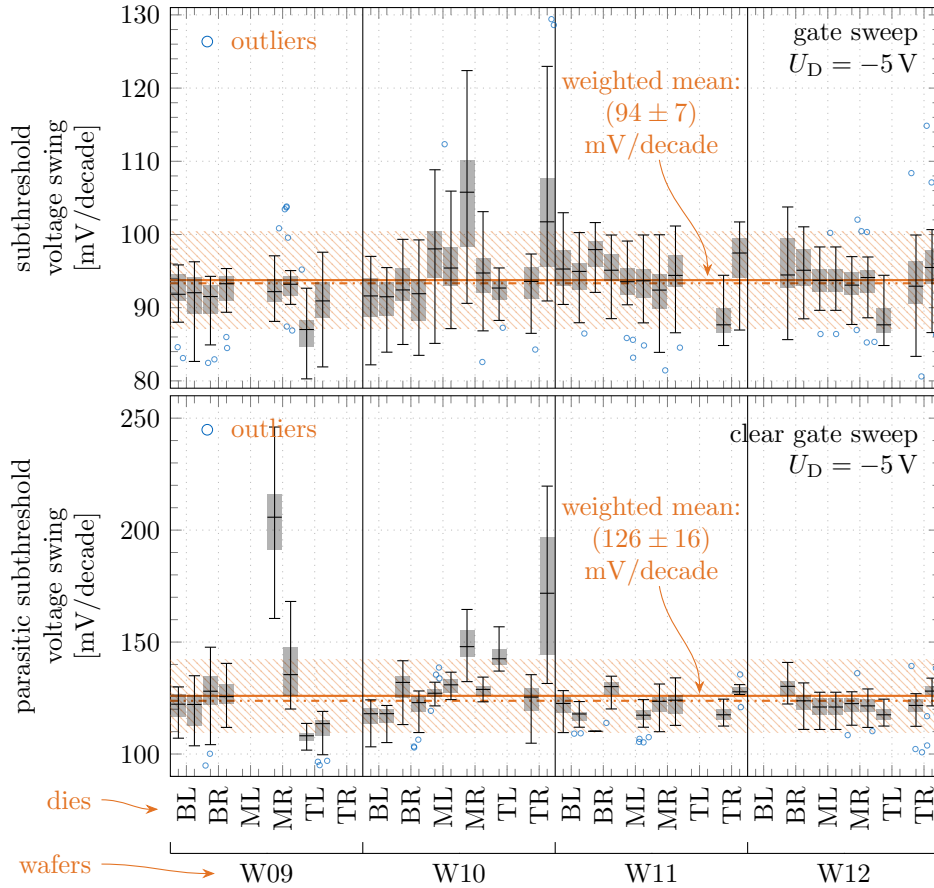


Figure 5.20: Results for the SVS from the 'gate sweep' (upper) and 'clear gate sweep' (lower) measurements performed with the customPCMS on all available SPDs. The data from all three groups of pixels located on a single SPD are grouped to a single box plot. The weighted mean value with ± 1 standard deviation for the complete measurement is presented with shaded orange . The W09 MR 80k1 and W10 TR 80k2 SPDs feature a deviating transition between the overall OFF state and the state where the parasitic transistor starts to conduct, as described in sec. 5.2.1.2. Consequence is that the parasitic subthreshold voltage swing is evaluated from not representative conditions.

5.2.1.4 Empty internal gate potential

The results for the empty internal gate (IG) potential (U_{IG}) are extremely useful for the cross-check of the simulated device behaviour. They are evaluated from the drain current vs. clear voltage (I_D vs. U_C) characteristics of the DePFET, obtained from the 'clear sweep' measurements (Tab. 5.2). In those measurements the following is necessary:

- The gate must be biased in the ON state. That way there exist a current path between source and drain implantations, and the IG potential is not influenced by the potential applied to the gate.
- The CG must be positively biased in order to weaken the potential barrier between charge storage regions and the clear implantation.
- The I_D must be measured while quasi-static sweeping the clear voltage from 0 V to 20 V.

Initially, the clear voltage (U_C) is not positive enough to remove the e^- from charge storage regions, and consequently they modulate the I_D (eq. 3.4). By making the U_C more and more positive the e^- are removed from the IG and I_D decreases until there are no e^- left in the IG. At this point the I_D reaches the constant value irregardless of the voltage applied to the clear.⁶ The I_D vs. U_C characteristic is shown with measurement points (\circ) on the left plot in Fig. 5.21.

Two different methods for the extraction of the U_{IG} were used and compared in the scope of this thesis. Both of them are presented in Fig. 5.21. A starting point was provided in D. Klose's master thesis [168]. In it he split the I_D vs. U_C characteristics in two parts: a linear part and a saturation part. In the former, the drain current is the sum of the DePFET's offset and signal currents. In the saturation part the drain current should, however, be at a constant offset current value. On both parts he performed a linear regression and defined the U_{IG} as a voltage at which the two lines intersect. This procedure is shown on the left plot in Fig. 5.21 and is named as ELR_C method, because of its similarities with the regular linear extrapolation method in the linear operation region (ELR) used for extraction of the U_T . However, for the EDET DH80k sensors that feature signal compression, this method wrongly evaluates the U_{IG} because the e^- collected in different charge storage regions feature different charge amplification factors. Consequently, a linear method is not sufficient to describe the response of drain current to the varying clear voltage. Therefore, a second method, called derivative method, was derived. It is shown on the right plot in Fig. 5.21. Here the derivative dI_D/dU_C is calculated and the U_{IG} is defined as the U_C where the derivative crosses the threshold line set at the 10 A/V. This value was selected as it is close enough to the flat part of the curve where the charge storage regions are empty, and yet far enough to avoid problems, arising from jitter in measured points, that would require manual changes in the otherwise automated procedure of the U_{IG} extraction. In order to minimize the errors this method utilizes a 5 point moving average (—) across all measurement points (\circ), and from the threshold level crossing of this line the U_C is interpolated.

⁶A small variation of the I_D is still allowed even after the IG is empty. This is because the clear potential can have a small influence on the effective transistor dimensions.

The ELR_C evaluates the U_{IG} potential through the extrapolation of behaviour in the region where the charge storage regions are completely empty and in the region where at least the IG is already filled to a certain degree. The derivative method, however, evaluates the U_{IG} on the transition point, i.e., based on the deviation of the DePFET response when the e^- start to arrive to the IG.

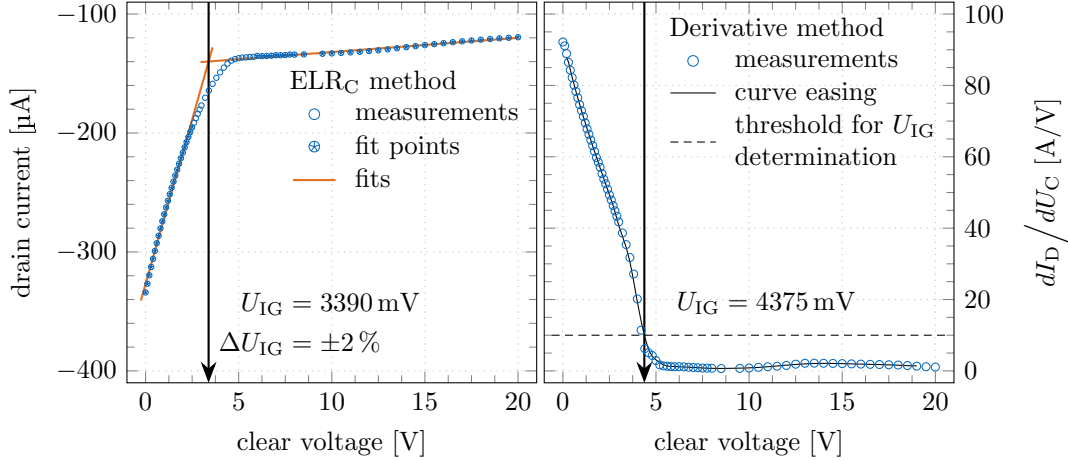


Figure 5.21: Two methods used for the extraction of the empty IG potential (U_{IG}). For the ELR (left) method an intersection of the two fitted lines is defined as the U_{IG} , whereas for the derivative method (right) the U_{IG} is defined as the point where the derivative of the drain current crosses the threshold line set at the 10 A/V . The data are taken from pixel 0 located on the W10 BR 80k2 SPD.

Results from both methods, for all SPDs tested with the customPCMS, are presented in Fig. 5.22. Pixels with different gate lengths are treated separately and the same is true for the SPDs from different wafers. Mean ($\overline{U_{IG}}$) and standard deviation (σ) values, obtained through the two methods, for all groups are numerically presented in Tab. 5.7. Both methods agree that the shorter the gate length the less positive is the U_{IG} . This is because both source implantations, i.e., the HDSP1 and HDSP2, that partially compensate the MDDN implantation, are implanted after the gate is structured (sec. 3.1). Now the smaller the gate length the bigger the fraction on the mask edges where ions can be implanted through the mask. The difference between the methods is that the ELR_C method reports $1100 \text{ mV} \pm 80 \text{ mV}$ lower empty IG potential than the derivative method. To put the numbers in context, the simulated empty IG potential is around $\sim 6 \text{ V}$ (Fig. 5.23). Consequently, both methods underestimate the empty IG potential. However, the derivative method is much closer to the expected value from simulations. The quality of the result with that method is directly correlated with the arbitrarily chosen threshold level used for determination of the empty IG potential. Setting this level too high evaluates in the underestimation of the empty IG potential, and setting it too low causes evaluation problems due to the jitter in measurement points. For the derivative method example presented in Fig. 5.21, the U_{IG} changes from 4390 mV to 5154 mV if the threshold is lowered to 2.5 A/V . This comes very close to

5 Characterization measurements

the simulated value, under consideration that the measured value is for the pixel with $3.8\ \mu\text{m}$ gate length and simulation is for one with $6\ \mu\text{m}$.

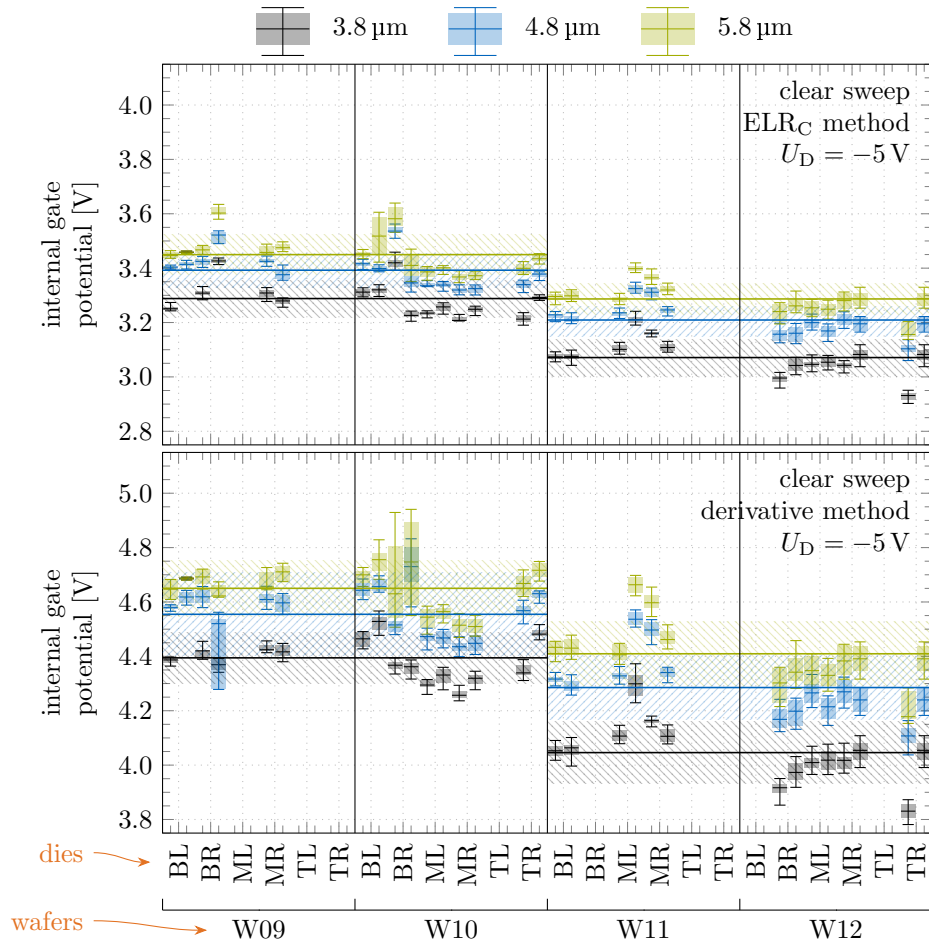


Figure 5.22: Results for the empty IG potential as obtained through both described methods; ELR_C method (top) and derivative method (bottom). The SOI and standard wafer types from the PXD10-1 production batch are treated separately. All voltages are given with respect to the source voltage.

Table 5.7: Mean ($\overline{U_{IG}}$) and standard deviation (σ) values for the measured empty IG potential values, compared over the two different wafer types for all groups of pixels with different gate lengths. Numerical collection of the results presented in Fig. 5.22.

	3.8 μm		4.8 μm		5.8 μm	
	$\overline{U_{IG}}$ [mV]	σ [mV]	$\overline{U_{IG}}$ [mV]	σ [mV]	$\overline{U_{IG}}$ [mV]	σ [mV]
ELR _C method						
SOI wafers	3290	(± 70)	3390	(± 60)	3450	(± 70)
standard wafers	3070	(± 70)	3210	(± 60)	3290	(± 60)
derivative method						
SOI wafers	4390	(± 90)	4550	(± 150)	4650	(± 100)
standard wafers	4050	(± 110)	4290	(± 120)	4410	(± 120)

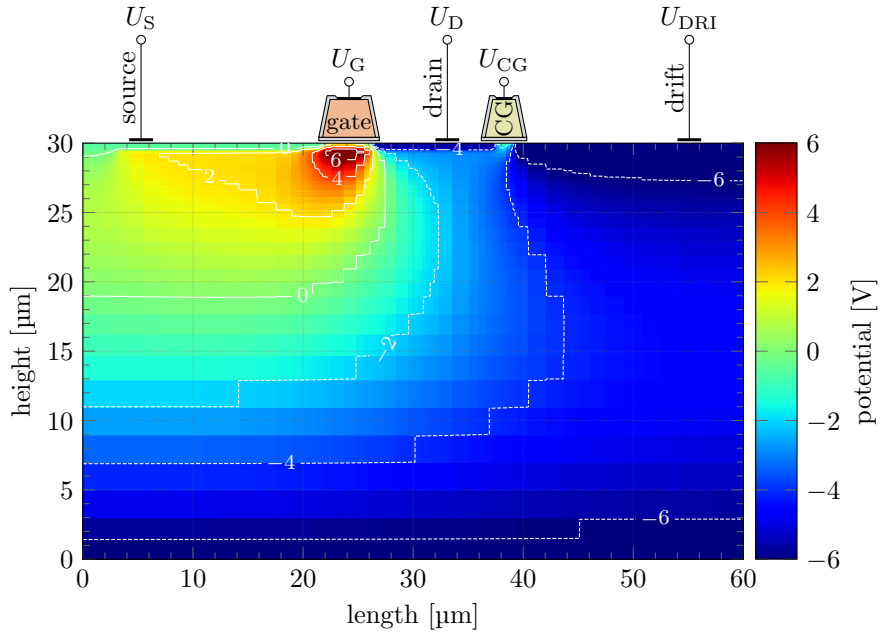


Figure 5.23: Simulated potential distribution inside the Si bulk from the central cut in the direction of the length of the transistor from the EDET DH80k devices. Simulated with the Oskar3 software [138] by R. Richter and K. Gärtner [138].

5.2.1.5 Pixel yield

Out of the 24 available SPD dies, 23 were tested with at least one pre-characterization system. With the generalPCMS 1104 pixel across 23 SPD dies were tested and 60 of them were non-functional. With the customPCMS 912 pixels were tested and 33 were non-functional. This results in a yield of 94.57% in the former, and 96.38% in the latter case. Despite the small relative difference, the absolute difference is almost doubled inside the 20% increase in the total pixel number. The complete results are presented in Fig. 5.24.

To compare the results, on the 912 pixels that were measured with both measurement systems, there were 33 labelled as non-functional with the customPCMS and 57 with the generalPCMS. Consequently, it is indicative that the measurements performed with the generalPCMS are less reliable. This is not due to the system itself, but rather because of the way the measurements were performed. The SPDs were tested on a gel-pak (sec. 5.2.1.3) which did not fix the vertical position of the SPD die. Consequently, the semi-automatic contact needle, used to contact the drains one by one, did not always make good electrical contact or it changed the contact properties of remaining four manual contact needles. The result is many bad measurement that get pixels labelled as non-functional.

For the final yield the two measurement sets are combined. The measurements performed with the customPCMS are more reliable. Therefore, the result from the generalPCMS are taken into consideration only where the measurements performed with the customPCMS are missing. The result of this is a final yield of 96.74%.

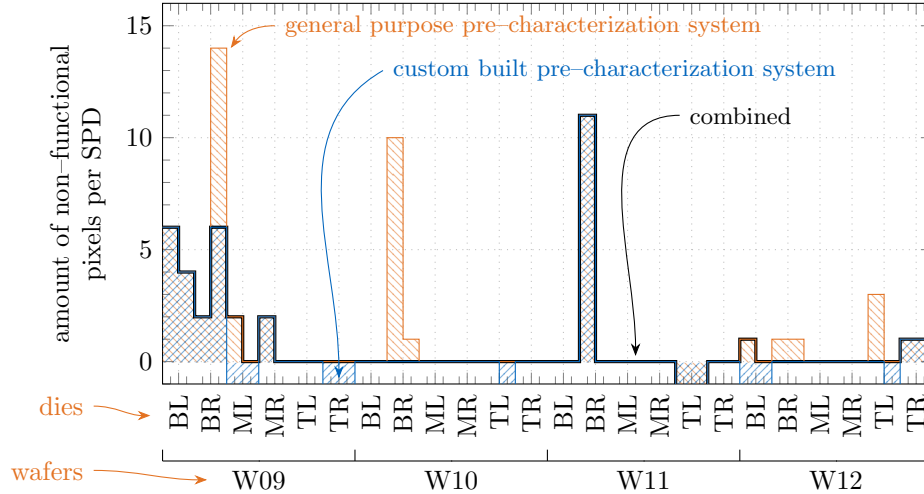


Figure 5.24: Amount of non-functional pixels as determined from the measurements with generalPCMS (orange hatched) and customPCMS (blue hatched). The combination of the two as the final amount of non-functional pixels per device is presented with the tick black line (—). All values that reach into the negative realm represent the missing measurements.

The defects that cause the pixels to not function properly are not covered in the scope of this thesis. They are, however, thoroughly described in refs. [168, 169].

5.2.2 Dynamic operation mode

In order to characterize the DePFET pixels in the same mode of operation as the final experiment, i.e., dynamic mode, two SPDs were tested with the single pixel measurement system (SPIX). The two SPDs were the W12 BL 80k1 and W09 ML 80k1. Topologically they are the same, however the former is from the standard wafer and the latter from the SOI wafer (chapter 4). The results presented in this section are chronological. Therefore, before performing the measurements for this section no shortcomings of the SPDs were known (sec. 4.3). Consequently, the measurements were performed as if there would be no problems with them. This means that the SPD was connected to the SPIX measurement system (sec. 5.1.2) and operated just as any new device would be. Initial starting points for biasing voltages were provided from simulations by R. Richter [113] and a 250 ns clear pulse (t_C) was repeated every 100 μ s, which gives the so-called exposure time (t_{EXP}). On the SPIX system one has a real time view of the DePFET's drain current, and the disturbance of the drain current level caused by the clear pulse can be seen as a heart beat (upper plot in Fig. 5.25).⁷ Once the clear pulse was properly applied, an ^{55}Fe radioactive source was placed above the SPD. At that point the clear gate (U_{CG}), clear OFF (U_C^{OFF}) and clear ON (U_C^{ON}) voltages were manually varied until the changes in drain current level during the exposure time were observed in the SPIX's live view (lower plot in Fig. 5.25). Those changes indicated the arrival of X-ray generated

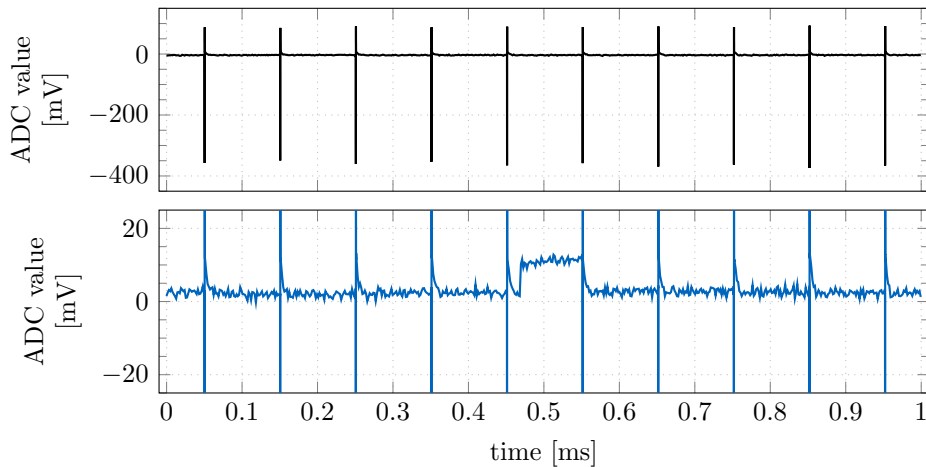


Figure 5.25: Live view of the DePFET's output characteristics as seen with the SPIX measurement system; DePFET operation in action where a clear pulse is repeated every 0.1 ms (top), and a response to a single X-ray event caused by the ^{55}Fe radioactive decay.

⁷The drain current is seen in the ADU or mV units after it's been converted and amplified by the discrete drain current readout board circuitry and digitized with the analogue-to-digital converter.

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signal charge in the pixel's IG, produced by the radioactive decays in ^{55}Fe radioactive source. At that time, those were the first events recorded with both the EDET DH80k device and the SPIX measurement system. Consequently, most of the initial work was invested to measure the performance of the SPIX measurement system, before turning towards the characterization and optimization of EDET DH80k devices. Therefore, the operational voltages for the first SPD were kept constant at their initial values (Tab. 5.8). After observing the ^{55}Fe X-ray events, a measurement was performed in order to obtain their energy spectrum. In this measurement, pixels 20 to 23 from the W12 BL 80k1 SPD, operated at the room temperature, were illuminated from the front side. As the equivalent noise charge (ENC) specifics of the SPIX system were not yet known, the measurement was performed in such a way that the full data stream of $\pm 8 \mu\text{s}$ around the clear pulse was recorded with the maximum ADC frequency of 62.5 MHz. From there the correlated double sampling (CDS) filtering (sec. 3.1.4) was performed with varying integration times. Fig. 5.26 shows two combined ^{55}Fe spectra of the four pixels at the integration time of $6.4 \mu\text{s}$. The first is obtained without common mode corrections (left) and the second with common mode corrections (right). In both cases ^{55}Fe K_α and K_β emission lines are easily observable and also the ^{55}Fe K_α Si escape peak is visible.⁸ From them the system's ENC noise, FWHM energy resolutions at ^{55}Fe K_α and K_β emission lines, and peak-to-valley ratio (PV)⁹ are obtained and collected in Tab. 5.9. Taking into account that EDET DH80k structures realized on the SPDs are not optimised for spectroscopy (e.g., small pixel size, only two rows of pixels) they still offer a very good

Table 5.8: Voltages used with the W12 BL 80k1 SPD.

U_S	U_D	U_G^{ON}	U_G^{OFF}	U_C^{ON}	U_C^{OFF}	U_{CG}	U_{CE}	U_{DRI}
[V]	[V]	[V]	[V]	[V]	[V]	[V]	[V]	[V]
0	-5	-2.865	10	18	3	1.5	5	-10

Table 5.9: FOMs from the ^{55}Fe spectra presented in Fig. 5.26.

	ENC	K_α FWHM	K_β FWHM	PV
	[e ⁻]	[eV]	[eV]	
without CMC	11.42 ± 0.02	171 ± 2	181 ± 5	21.9 ± 2.7
with CMC	5.10 ± 0.02	149 ± 3	157 ± 5	24.9 ± 2.6

⁸Primary radiation ionizes the Si atom which afterwards relaxes itself into the lower energy state. If this occurs through the secondary X-ray photon emission this photon can traverse outside of the detector's sensitive volume. That way the measured energy of the primary radiation is reduced by the secondary X-ray.

⁹Defined as the quotient between the emission line with the highest number of counts (peak) and mean level of the counts between the energies of 2 keV and 4 keV (valley).

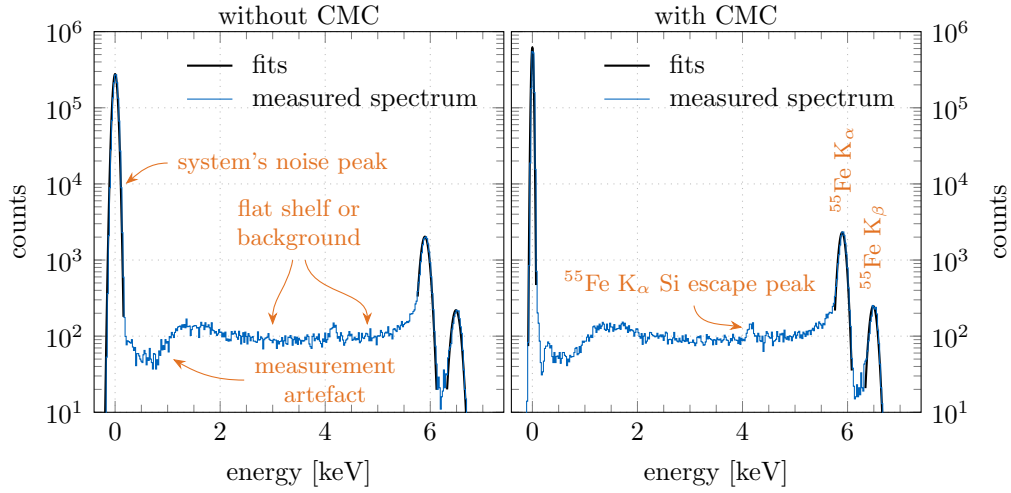


Figure 5.26: Combined ^{55}Fe spectrum as measured at the room temperature with pixels 20 to 23 from the W12 BL 80k1 SPD; without (left) and with (right) common mode corrections. For the measurement the full data stream of $\pm 8\ \mu\text{s}$ around the clear pulse was recorded. Afterwards the common mode correction filtering with varying integration times between $0.32\ \mu\text{s}$ and $6.88\ \mu\text{s}$ was performed (Fig. 5.27). The spectra shown above feature the CDS filtering with $6.4\ \mu\text{s}$ of integration time. A mean ENC of $11.4\ e^-$ ($5.1\ e^-$), a FWHM energy resolution of $171\ \text{eV}$ ($149\ \text{eV}$) at $^{55}\text{Fe}\ K_\alpha$ and $181\ \text{eV}$ ($157\ \text{eV}$) at $^{55}\text{Fe}\ K_\beta$ were obtained without (with) common mode corrections.

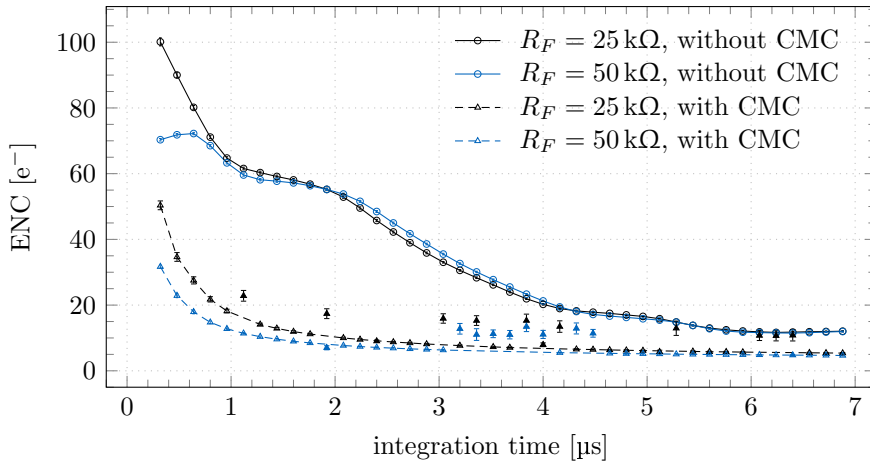


Figure 5.27: Measured ENC values as a function of the integration time. Measurements were made with two different gain settings controlled by the feedback resistor (R_F) on the DROB, and results were evaluated with and without the common mode correction filtering. The errors of evaluated ENC values are in general too small to be seen on the plot. However, in some cases the evaluation method fails to converge and yields the wrong result. Those points are presented with filled markers (\blacktriangle) so that they can be easily ignored. Lower ENC value means better performance.

performance. The relatively low PV ratio is a consequence of the signal e^- being split on the pixel borders. As only four pixels, arranged in two physical rows, were operated, the reconstruction of split events was not possible. Consequently, all those events are added to the flat shelf area. Main reasons for the flat shelf to exist is the incomplete charge collection from events that happen at the entrance window, highly doped regions that are not depleted, or on pixel borders. More detailed explanation is given in refs. [148, 170]. The dip between the system's noise peak and the flat shelf has no physical meaning, but is there due to the specifics with which the measurement was performed in order to optimize the data storage, hence the name – measurement artefact.

The second plot generated from the same measurement type is presented in Fig. 5.27. This plot shows how the ENC of the complete system varies with the integration time. The measurements were performed with two different gain settings, controlled with the feedback resistor (R_F) on the discrete drain current readout board (DROB), and their results were evaluated without and with common mode corrections. The first observation drawn from the plot is that the common mode noise is the biggest contributor to the overall ENC performance of the system. By applying the common mode correction the ENC is reduced by a minimum of 50 % (55 %) at integration times above 6 μs and a maximum of 81 % (86 %) at shorter integration times in case of 25 k Ω (50 k Ω) feedback resistor. However, the common mode corrections are only possible when majority of pixels do not detect any charge. Therefore, it can be used when events happen randomly, e.g., radioactive source, but not when they are pulsed and cover the complete array, e.g., flat field illumination with the pulsed linear high-speed LED. An integration time of 6.4 μs was selected for future measurements, as the minimum of the ENC is located at that value and the lower the ENC the better the system performance.

In order to verify that the ENC of the system is not dominated by the noise originating from the DROB, two different gain settings were tested. The main contributor on the DROB is the feedback resistor that determines the gain of first stage operational amplifier (OpAMP). It's current noise density is inversely proportional to the size of the feedback resistor

$$I_n \propto \frac{1}{\sqrt{R_F}} .$$

If the ENC would reduce for around 29 % after doubling the feedback resistor size, the main contributor to the ENC would be the feedback resistor. However, after the filtering out the common mode noise contribution the change at the integration time of 6.4 μs is only 13 %. This means that multiple noise contributions are on the same level, and the 50 k Ω feedback resistor is kept as it is the biggest that can join the output range of the EDET DH80k DePFET drain current and the input range of the used first stage OpAMP.

Once an energy calibration is available, the device inherent leakage current (I_L), described in sec. 3.2.2.2), can be used to determine the dynamic range of the devices. Under the condition of constant temperature, the mean level of leakage current is constant. In case the pixel only collects leakage current, the amount of e^- collected in charge storage regions is proportional to the exposure time t_{EXP} . By extending the t_{EXP} to the order

of seconds, enough e^- will be collected in the charge storage regions to determine the total dynamic range. Additionally, multiple readouts can be implemented isochronally during the t_{EXP} to record the complete response function. This yields the result that is presented in Fig. 5.28. Three different regions are observed on that figure; the internal gate region (IG), the overflow region (OF), and the region where the overflow to clear contact happens. The first two regions are parametrized by their respective charge amplification factors

$$g_q^i = \left. \frac{dI_D}{dQ} \right|_i \quad \text{where } i \in [\text{IG}, \text{OF}],$$

and between them is the transition area with the kink. As the IG gets closer to maximum capacity more e^- begin to be collected in the OF. As a consequence the first stage amplification factor is reduced from g_q^{IG} to g_q^{OF} . The kink denotes the point where the biggest change between the two appears, i.e., the point where the d^2I_D/dQ^2 is at the most negative value. The collection of e^- in the OF continues until it is completely filled. At that point e^- start to flow to the next most positive contact – the clear contact. When this happens, the pixel has reached its maximum fill level. This maximum fill level is denoted with the Q_{MAX} . All described parametrization factors, i.e., figures of merit (FOMs), and also the leakage current (I_L), are collected in Tab. 5.10.

In order to compare the response function and its extracted parameters to the simulated version (Fig. 3.14), one first has to correct for differences in pixel dimensions. This is a very rudimentary correction as also the biasing conditions are not equal. The

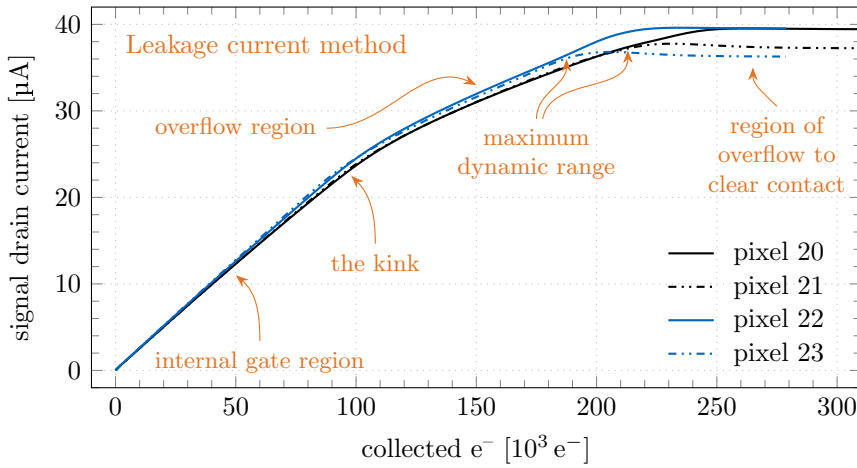


Figure 5.28: Response function of pixels 20 to 23 ($L = 5.8 \mu\text{m}$) from the W12 BL 80k1 SPD measured by the means of leakage current over their full dynamic range. Between two consecutive clears that were 2.56 s apart 715 readouts occurred isochronally every 4 ms. The parametrization of the above plot is collected in Tab. 5.10.

Table 5.10: FOMs from the response function presented in Fig. 5.28.

pixel	g_q^{IG} [pA/e ⁻]	g_q^{OF} [pA/e ⁻]	kink [10 ³ e ⁻]	transition [10 ³ e ⁻]	Q_{MAX} [10 ³ e ⁻]	I_L [e ⁻ /μs]
20	238 ± 9	109 ± 12	105	93 to 129	207	0.11
21	242 ± 6	117 ± 11	100	86 to 124	189	0.11
22	247 ± 6	125 ± 8	99	90 to 124	184	0.10
23	253 ± 3	129 ± 8	90	81 to 114	179	0.10
mean	243 ± 6	119 ± 9	99	89 to 123	190	0.105

measured mean charge amplification factors scale as

$$\frac{g_q^{\text{sim}}}{g_q^{\text{meas}}} = \sqrt{\frac{L_{\text{meas}}^3 W_{\text{meas}}}{L_{\text{sim}}^3 W_{\text{sim}}}}, \quad (5.4)$$

which yield a 255 pA/e⁻ (125 pA/e⁻) scaled charge amplification factor for the IG (OF) region.¹⁰ The simulated values are therefore roughly 18 % (44 %) smaller than the measured ones. For the 3D simulation performed with the Oskar3 software [138] a deviation of this order is to be expected, as it includes only a very limited set of physical models and one can define only a single value for a channel mobility, without any field and doping dependencies [113]. The average scaled kink of 107 ke⁻ is in good approximation of the simulated one at around 100 ke⁻, but the biggest discrepancy comes in a way of Q_{MAX} . Even after scaling (see appendix. A), the mean Q_{MAX} of 279 ke⁻ does not come close to the values allowed by the simulation ($> 10^6$ e⁻) or the minimum capacity needed by the EDET project (800 ke⁻).

In order to investigate the discrepancies, a manual scan of the response functions at different U_{CG} and U_C conditions was performed. Fig. 5.29 shows a subset of those scans. The result from this was a finding that the Q_{MAX} can be influenced by the operational voltages, yet the W12 BL 80k1 SPD has an extremely small window of operational voltages, where the response function behaves like in simulation. The expected behaviour appears only at $U_{\text{CG}} \sim 1.5$ V and $U_C \sim 3$ V. Making the clear voltage more positive reduces the Q_{MAX} , whereas making it more negative causes the response similar to that of the back-emission of e⁻ from the clear contact. An interesting thing, however, happens if the U_{CG} is made more negative. At that point an unexpected increase of the charge amplification factor is observed. An explanation of this phenomenon could be the existence of the potential pocket. The e⁻, generated in the Si bulk, drift to their closest potential minimum. If everything is as planned, the potential minimum is always one of the charge storage regions. But in case a potential pocket exists, some e⁻ end in it and some in the IG. This continues until the potential pocket is filled. From that point on,

¹⁰Under a rudimentary assumption that all other contributions are equal in both case.

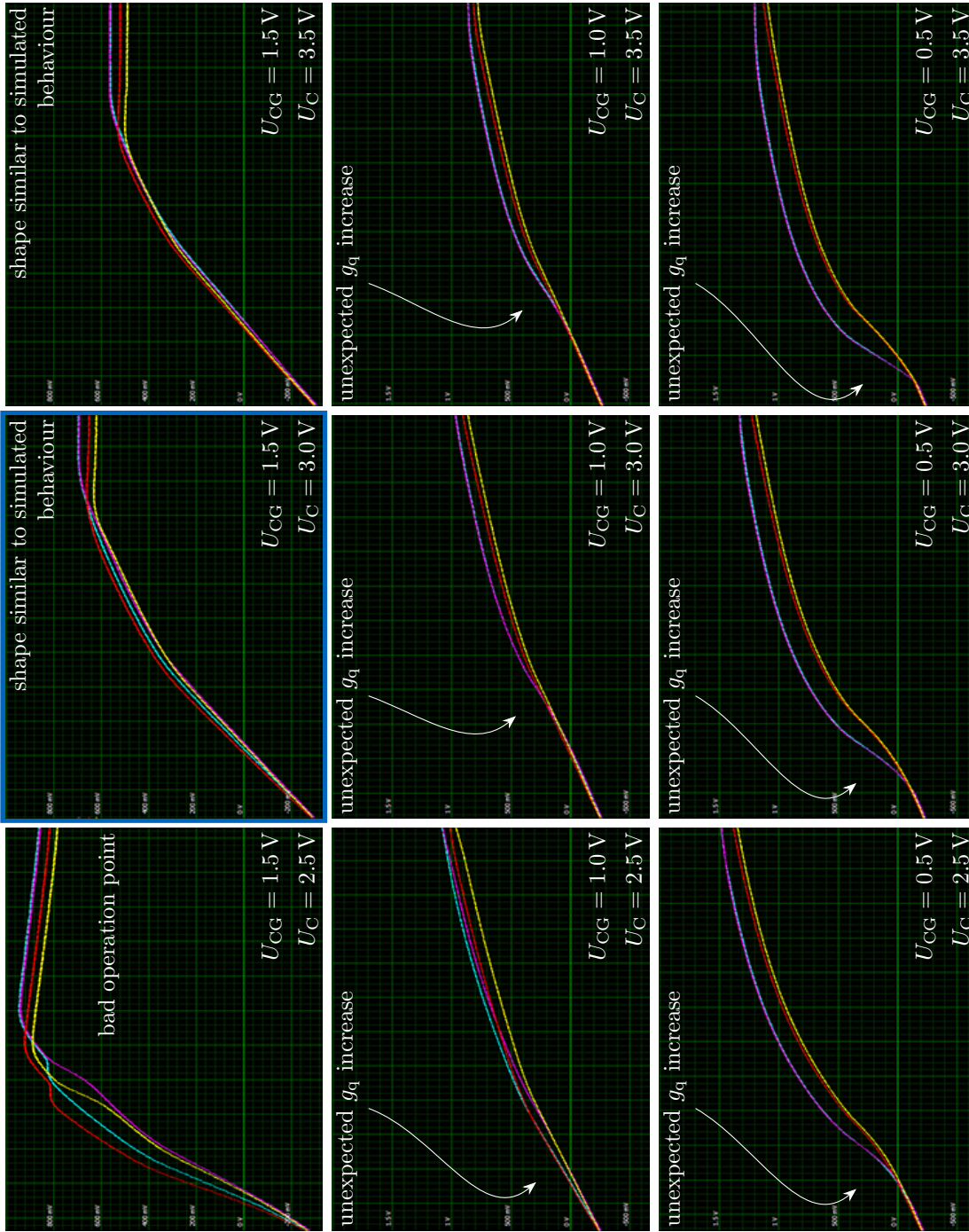


Figure 5.29: Response function of pixels 20 to 23 from the W12 BL 80k1 SPD measured at three different CG and clear conditions. A single 3s long sequence was recorded by the means of SPIX's live view. Plot with the blue border represents the same condition as presented previously.

all e^- begin to be collected by the IG. This presents itself as an increase in the charge amplification factor. In case of the SPDs, the potential pocket is a consequence of the design layout error (sec. 4.3). Due to the mistake, the aluminium connection between the drift implantation and contact pad is missing, and the whole region is left floating. Because this region is of the p^+ -type, it is attractive to the h^+ and it becomes positively biased. Now, in order for the e^- generated below drift to arrive to the charge storage regions they have to pass either below the drain or clear. The former is biased very negatively and presents too big of a barrier, therefore only the latter option is possible. This limits the window of operational voltages a lot. Clear voltage that is too positive means that the e^- passing below it end in it, and a too negative voltage creates a barrier and the e^- stay in the drift region.

In order to mitigate this problem, a punch-through biasing is useful. As the drift is floating, it is pulled to the potential of the surrounding p^+ -type contacts. Therefore, by negatively biasing the backside of the SPD die, the drift should become sufficiently negative for the potential pocket to disappear. To not complicate the SPIX system with a high voltage power supply unit (PSU), needed to deplete 450 μm of Si from standard wafers, the W12 BL 80k1 SPD was swapped for the W09 ML 80k1, which is a 50 μm thin SPD. That way the device can be depleted through punch-through mechanism by relatively low voltages.¹¹ Additionally, the biasing scheme was changed as well. As it is impossible to switch between the two rows of pixels on the SPD, it is not useful to have the global gate contact connected to the switcher ASIC. Consequently, the gate was statically biased through the PSU, and the vacant switcher channel was connected to the clear gate (CG) in order to help with clearing. This is helpful because the capacitive CG coupling of the clear to the CG, on the SPDs, is not sufficient to help in the clearing process.

Tab. 5.11 contains the biasing conditions that were used in order to perform the dynamic range measurements on 6 pixels from the W09 ML 80k1 SPD.

The measurements exactly like the ones performed on the W12 BL 80k1 SPD were performed also on the W09 ML 80k1 SPD. In addition, a second method of measur-

Table 5.11: Voltages used with the W09 ML 80k1 SPD.

U_S	U_D	U_G	U_C^{ON}	U_C^{OFF}	$U_{\text{CG}}^{\text{ON}}$	$U_{\text{CG}}^{\text{OFF}}$	U_{CE}	U_{PT}	U_{DRI}
[V]	[V]	[V]	[V]	[V]	[V]	[V]	[V]	[V]	[V]
0	-5	varied ^a	10	3	8	3.2	5	-35	NC

^a Different gate lengths on the SPDs require different gate voltages in order to achieve $I_{\text{OFFS}} \sim 100 \mu\text{A}$; -1.474 V was used for the 3.8 μm gate length group, -1.995 V for the 4.8 μm , and -2.370 V for the 5.8 μm .

¹¹Another layout error rendered the use of the punch-through contact on the SPDs impossible. Therefore, a smaller p^+ -type implantation was used. This implantation is located on a test structure on the half of the SPD die that was not described.

ing the dynamic range was added. This method employs the linear high-speed LED (sec. 5.1.2.3) through which the measurement speed can be increased by at least two orders of magnitude. Instead of waiting for the leakage current to generate enough e^- to fill the charge storage regions, an infrared LED was used to emit 16 ns short pulse every 10 μs . Thus, a well defined small average amount of e^-/h^+ pairs is generated inside the Si bulk on every LED pulse, and there is enough time between the light pulses to integrate and readout the collected e^- . Therefore, the response function can be measured very fast with high granularity. The top row of pixels collected in average $(1787 \pm 86) e^-$ and the bottom $(2463 \pm 191) e^-$. The difference between the two rows can be attributed to different collection areas due to the drift not being exactly defined. Results of those measurements are presented in Fig. 5.30, where the upper plot show the leakage current method and the lower plot the LED method. The extracted FOMs of those results are collected in Tab. 5.12.

The first thing to be done is the comparison of the two methods. In general, both methods offer similar results for everything but the Q_{MAX} and I_L . By employing the two methods over a plethora of pixels one would without a doubt arrive to the overlapping distributions for g_q^{IG} , g_q^{OF} and kink. However, this is not the intent of this thesis. The intent here is to perform the low noise measurements and extract as many FOMs as possible. And in order to obtain precise values for the Q_{MAX} and I_L both measurements are necessary. This is due to the fact that the leakage current method wrongly measure the Q_{MAX} and the LED method cannot be used to measure the I_L .

The Q_{MAX} heavily depends on the potential barriers around the clear region. The potential barrier around it is set by the CG. This one is fixed with the external voltage and does not change in time. However, the second potential barrier placed below the clear region, is set by the deep p implantation (sec. 3.1) which is not fixed by an external voltage. The level of this potential barrier depends on the dynamic operation of DePFETs, i.e. on the repetitive clear pulses. In addition to removing the e^- from the charge storage regions, those very positive clear pulses also deplete the deep p implantation, by pushing away the h^+ which accumulated in this region. This in turn leaves the negative stationary ions that on one hand generate a potential barrier for e^- , and on the other create a potential pocket for h^+ . In normal operation mode, where the time between two consecutive readouts is kept small, it never happens that enough h^+ would be collected by the deep p implantation to weaken the potential barrier. However, this is not the case with the leakage current method, where the times between the clear pulses are extremely long. The potential barrier below the clear, set by the deep p implantation, gets reduced with time and the probability for e^- to overcome it increases. Consequently, an ever increasing part of the e^- , generated in the Si bulk, do not arrive to charge storage regions, but are lost to the clear implantation.

First conclusions can be made at this point. The leakage current will not be influential in the scope of EDET DH80k camera sensor operation.¹² With the mean of $0.365 e^-/\mu\text{s}$

¹²In case of the SPDs, the collection area for thermally generated e^- , that are a source of I_L , is not exactly defined. Therefore, no scaling to different pixel sizes was performed.

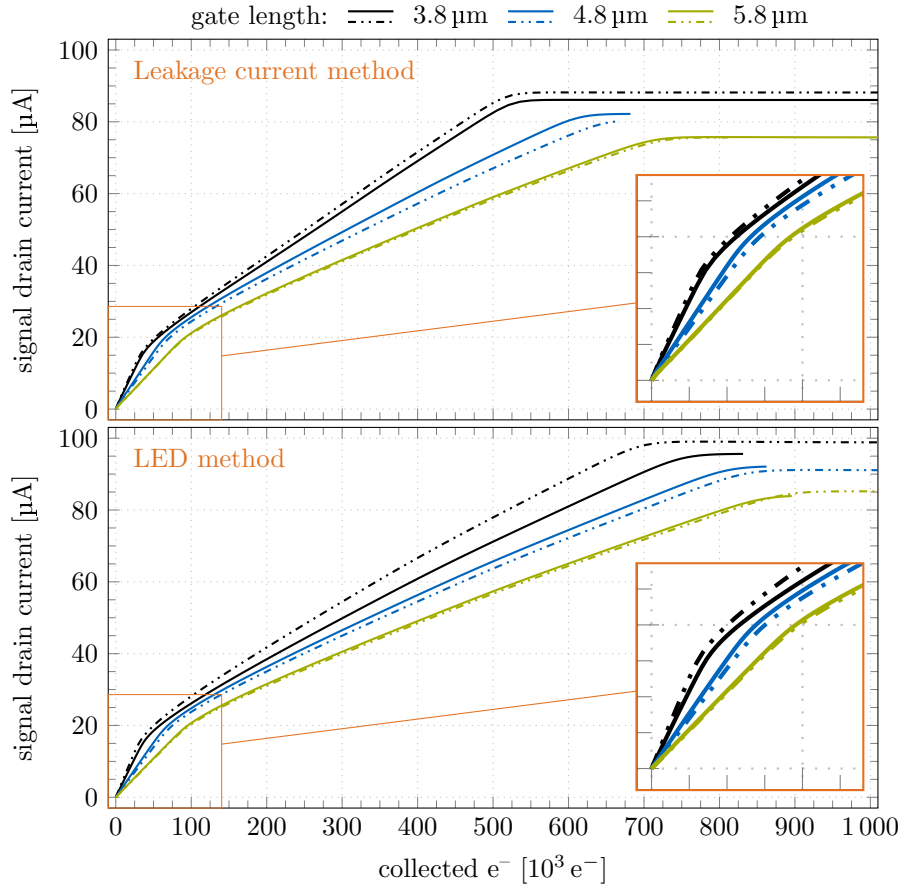


Figure 5.30: Response functions of six pixels from the W09 ML 80k1 SPD measured with two different methods; leakage current (upper) and LED (lower). Pixels differ between themselves only in the gate length. The full line style (—) represents even numbers and the dash dot dot style ($\text{-}\cdot\cdot\text{-}$) the odd ones. The parametrization of the above plot is collected in Tab. 5.12. Curves in both methods were sampled isochronally from 500 to 510 times, with the samples being apart 5 ms ($10\ \mu\text{s}$) in case of the leakage current (LED) method.

and $12.5\ \mu\text{s}$ between consecutive clear pulses, the collected e^- from this contribution are negligible in comparison to the signal e^- .

Other parameters measured through the LED method are in parallel with the expectations from the simulations [113]. Despite the measured numbers for Q_{MAX} barely satisfy the EDET project condition of $800\ \text{ke}^-$ storage capacity, they are well over this limit when the SPD pixel dimensions are scaled to the pixel dimensions of main devices – see appendix A. In that case the mean Q_{MAX} increases to $1225\ \text{ke}^-$, $1401\ \text{ke}^-$ and $1514\ \text{ke}^-$ for pixels from the $3.8\ \mu\text{m}$, $4.8\ \mu\text{m}$ and $5.8\ \mu\text{m}$ gate length group.

A manual scan of possible U_{CG} and U_{C} conditions, like the one presented in Fig. 5.28 for W12 BL 80k1 SPD, resulted in a bigger operation window, where pixels exhibit the

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Table 5.12: FOMs extracted from the measured dynamic range presented in Fig. 5.30. The data is for 6 pixels from the W09 ML 80k1 SPD.

pixel	L [μm]	g_q^{IG} [pA/e $^-$]	g_q^{OF} [pA/e $^-$]	kink [10^3 e $^-$]	transition [10^3 e $^-$]	Q_{MAX} [10^3 e $^-$]	I_L [e $^-$ / μs]
Leakage current method							
6	3.8	430 ± 1	141 ± 7	36	24 to 57	482	0.52
7	3.8	472 ± 1	147 ± 9	33	22 to 50	475	0.39
8	4.8	314 ± 4	112 ± 13	59	49 to 77	588	0.27
9	4.8	287 ± 4	104 ± 13	65	54 to 83	614	0.26
16	5.8	221 ± 2	89 ± 11	86	73 to 110	680	0.43
17	5.8	219 ± 6	88 ± 11	85	72 to 109	691	0.32
LED method							
6	3.8	428 ± 8	111 ± 15	37	28 to 52	707	NA ^a
7	3.8	507 ± 5	124 ± 17	32	21 to 47	646	NA ^a
8	4.8	304 ± 5	96 ± 13	62	52 to 83	771	NA ^a
9	4.8	278 ± 2	93 ± 12	69	55 to 91	788	NA ^a
16	5.8	215 ± 2	83 ± 11	88	75 to 113	829	NA ^a
17	5.8	212 ± 1	81 ± 10	92	73 to 119	852	NA ^a

^a Not available (NA) through the LED method.

expected response function, when compared with the W12 BL 80k1 SPD. However, the problem of a not well defined state of the drift implantation still remained. Therefore, the decision to modify the SPIX system to accommodate the prototyping matrices (PMATs) was made. The main bulk of characterization and optimization work was therefore performed on single pixel measurements from prototyping matrices.

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In this section the results from the dynamic measurements performed on the prototyping matrices (PMATs) will be shown. This includes both the optimization and characterization measurements. However, the approach at this point will be different to the one shown in the previous section (sec. 5.2.2). There, all presented measurements were more or less a proof of principle, i.e., showing that the EDET DH80k DePFET pixel can do what was previously only simulated. Now with PMATs, the results will follow a bottoms up approach. Consequently, the optimization of operational parameters will be done in advance of the measurements of the full response functions.

As described in sec. 4.2 three different PMATs from the PXD10–1 production batch will be tested – the main design 50 μm thick W09 F07, the main design 30 μm thick W10 F07 and the experimental design 50 μm thick W09 B07.

The maximum number of simultaneously read out pixels with the single pixel measurement system (SPIX) is limited to four. This coupled with the double pixel double row layout of the EDET DH80k devices makes it impossible to read out the sub-array of adjacent pixels bigger than 2×2 . Consequently, only a single electrical row for gate and clear voltages was connected to the switching circuitry. All remaining electrical rows were kept at fixed all gate (U_G^{ALL}) and all clear (U_C^{ALL}) voltages. The former was kept in the OFF state and the latter in the ON state. That way a well defined state of all pixels was achieved.

5.3.1 Optimization of operation parameters

The operational parameter space of a DePFET pixel comprises from the following voltages: clear OFF (U_C^{OFF}), clear ON (U_C^{ON}), clear gate (U_{CG}), drift (U_{DRI}) and punch-through (U_{PT}). By performing a very rough scan with only 20 measurement points on each parameter, the complete scan would take 370 days.¹³ Consequently, the measurements has to be split to multiple separate scans. Within each scan a maximum of two contacts have their applied voltage varied whereas the rest are kept constant.

5.3.1.1 Operation window scan

Two structures that are the closest to the DePFET’s transistor channel are the clear gate (CG) structure and the clear n^+ -type Si implantation. The U_{CG} and U_C^{OFF} , respectively applied to the CG and clear, define the so-called operation window of the DePFET pixel. Whereas the U_C^{ON} voltage, applied to the clear during the clear pulse, controls the clearing process which will be discussed in the next section (sec. 5.3.1.2).

Different biasing conditions can cause different problems. In general they were already discussed in sec. 3.1.2, here, however, they will be presented with actual measurements:

- Back-emission of e^- : e^- are emitted from the clear contact and collected in the charge storage regions.
- Parasitic channel: an unwanted current path between source and drain implantations under the CG that is not controlled by the U_G .
- Charge loss: e^- get collected by the clear contact instead of charge storage regions.

In order to evaluate all three effects the operation window scan was done with two separate scans. The first was performed without external illumination, i.e., a dark scan, whereas the second was performed so that the PMAT was illuminated from the backside with the linear high-speed LED, i.e., an illuminated scan. Biasing conditions were the same in both scans and are collected in Tab. 5.13. Missing in table are the U_C^{OFF} and U_{CG} as they were swept from -2 V to 5 V in 0.1 V steps.

¹³Under the generous assumption that a single measurement and its analysis takes only 10s.

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Table 5.13: Voltages used for the operation window scans with the W09 F07, W10 F07 and W09 B07 PMATs.

U_S	U_D	U_G^{ON}	U_G^{OFF}	U_G^{ALL}	U_C^{ON}	U_C^{ALL}	U_{CE}	U_{DRI}	U_{PT}
[V]	[V]	[V]	[V]	[V]	[V]	[V]	[V]	[V]	[V]
0	-5	varied ^a	5	5	15 ^b	10	10	-5	varied ^c

^a Voltage evaluated for every PMAT separately so that $I_{OFFS} \sim 100 \mu A$. The evaluation was done at the U_{CG} of 0 V and U_C^{OFF} of 1 V. For the PMATs W09 F07 and W10 F07 this resulted in -2.18 V, and for the W09 B07 in -1.86 V.

^b Measured with regards to the U_C^{OFF} voltage.

^c Depends on the thickness of the device; -35 V was applied to the $50 \mu m$ thick PMATs and -20 V to the $30 \mu m$ thick PMAT.

Dark scan A purpose of the dark scan is to determine the limitations of the operation window without any externally generated e^-/h^+ pairs. This is necessary as it is impossible to distinguish between different contributions to the drain current, i.e., e^- originating from the back-emission process modulate the drain current just as the signal e^- do, and the same is true for the parasitic current contribution. The dark scan was performed with $100 \mu s$ between the two consecutive clear pulses. At good operation points the charge storage regions should be empty apart from a few e^- collected due to the leakage current. Consequently, the drain current there should be more or less stable around the set I_{OFFS} . At bad operation points, however, the drain current can increase significantly due to e^- collected in charge storage regions because of the back-emission, or because of the parasitic channel. The measured quantity in case of this scan is, therefore, the level of the drain current measured shortly before the clear pulse. In order to compare the results across different PMATs, the drain currents need to be on the same level. Therefore, from the drain currents measured at different U_{CG} and U_C^{OFF} points ($I_D^{U_{CG}, U_C^{OFF}}$) an offset drain current from the reference point will be subtracted. For the reference point, a measurement at the U_{CG} of 0 V and U_C^{OFF} of 1 V was selected, as it was far away from all problematic regions of operation and was also used to tune the I_{OFFS} to $100 \mu A$. This is performed in the following way

$$\begin{aligned} \Delta I_D^{U_{CG}, U_C^{OFF}} &= I_D^{U_{CG}, U_C^{OFF}} - I_D^{U_{CG}, U_C^{OFF}} \Big|_{U_{CG}=0V, U_C^{OFF}=1V} \\ &\approx I_D^{U_{CG}, U_C^{OFF}} - 100 \mu A, \end{aligned} \quad (5.5)$$

The $\Delta I_D^{U_{CG}, U_C^{OFF}}$ is the value calculated for every measurement point of every measured DePFET pixel. The final FOMs, for comparison of different PMATs between themselves, are the mean and standard deviation values, calculated from the above quantity across all measured pixels from a single PMAT.

Fig. 5.31 shows the result of the described dark scan, performed on four pixels from the W09 F07 PMAT, with the mean $\Delta I_D^{U_{CG}, U_C^{OFF}}$ value being presented on the upper plot and its standard deviation value on the lower plot. For the mean value of $\Delta I_D^{U_{CG}, U_C^{OFF}}$, the colour scale is limited from $-8 \mu\text{A}$ to $8 \mu\text{A}$, as this is the extent in which the variations for good operation points are tolerated. It can be seen that above of the $U_{CG} \approx U_C^{OFF}$ line the $\Delta I_D^{U_{CG}, U_C^{OFF}}$ values start to exceed those limits. This is because of the back-emission of e^- from clear region to the charge storage regions. At the very top right corner of the back-emission region, the transition back to the bounds, set by the colour scale, occurs. This is because the clear implantation becomes more positive than the IG and, consequently, the back-emission is suppressed. In addition, the clear implantation at those voltages becomes a global minimum for e^- generated in the Si bulk. At the bottom of the plot the values start to slightly increase due to the onset of the parasitic channel. This happens a bit earlier in the dynamic measurements than it did in the quasi-static ones (sec. 5.2.1.2). Reason for this is that the parasitic channel also depends on the U_C . In static measurements the U_C was kept at 10 V, whereas here it is kept between -1 V and 5 V . Consequently, the potential below the CG is slightly less repellent for h^+ due to the lower U_C^{OFF} voltage.

The remaining area is the operation window of the measured pixels. Small changes of the drain current in it are expected as the U_{CG} and U_C^{OFF} influence the transistor channel (eq. 2.22). Positive voltages applied to those two contacts repel the h^+ from the edge of the channel, i.e., effectively making the channel narrower. As CG is closer to the channel than clear, it also has a bigger influence. This is seen through iso-current lines. They change more often when doing the cut at the constant U_C^{OFF} in comparison to the cut at the constant U_{CG} .

For standard deviation values, a small scale from $0 \mu\text{A}$ to $0.1 \mu\text{A}$ is selected to show where the behaviour of four pixels, from a single PMAT, diverges. At the reference point the standard deviation is $0 \mu\text{A}$, because all $\Delta I_D^{U_{CG}, U_C^{OFF}}$ values at that point are always $0 \mu\text{A}$. By changing the U_{CG} and U_C^{OFF} the standard deviation remains small if the responses of measured pixels are similar, and increases if they start to differ. As each of the pixels has its own drain connection one of the reasons for divergence can be the parasitic current. That is why the standard deviation increases at low U_{CG} .

The side-by-side comparison of three different PMATs is shown in Fig. 5.32; W09 F07 (left), W10 F07 (middle), and W09 B07 (right). The plots feature the same data structure as explained in the text above, with a small distinction – values that are outside of the set limits are masked away. Both of the PMATs featuring the main design, i.e., design C, are showing a very big operation window. The third PMAT with the experimental design, i.e., design D, however, is showing a more limited operation window. Even though the mean relative drain current of four pixels is exhibiting similar behaviour, the pixels diverge a lot with changing of the applied voltages. Fig. 5.33 is showing the overlap of good parts from all dark operation window scans performed on the three PMATs. In order for the operation point to be deemed good, the mean value

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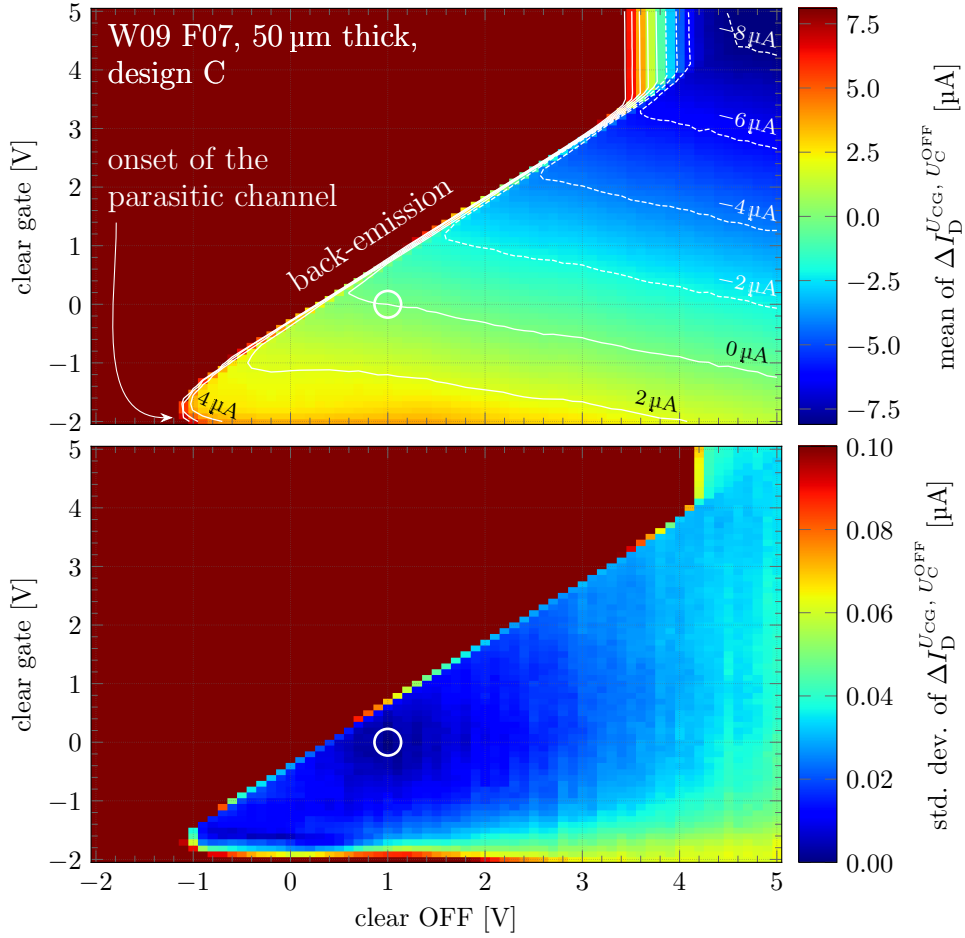


Figure 5.31: Explanatory plot for the two-dimensional operation window scan performed on four pixels from the W09 F07 PMAT. The main quantity, from which the plots are calculated, is the drain current from which the reference value (white circle) is subtracted (eq. 5.5). This quantity was measured for four pixels, and the plots show the mean (upper plot) and standard deviation (lower plot) values of those four pixels. The reference value is set at U_{CG} of 0 V and U_C^{OFF} of 1 V. The values on the two plots can extend beyond the limits set on the colour bars, however, the colours are capped to the levels at which changes are expected.

5 Characterization measurements

has to be within the open interval of plotted limits and the standard deviation value has to be smaller than the upper plotted limit.

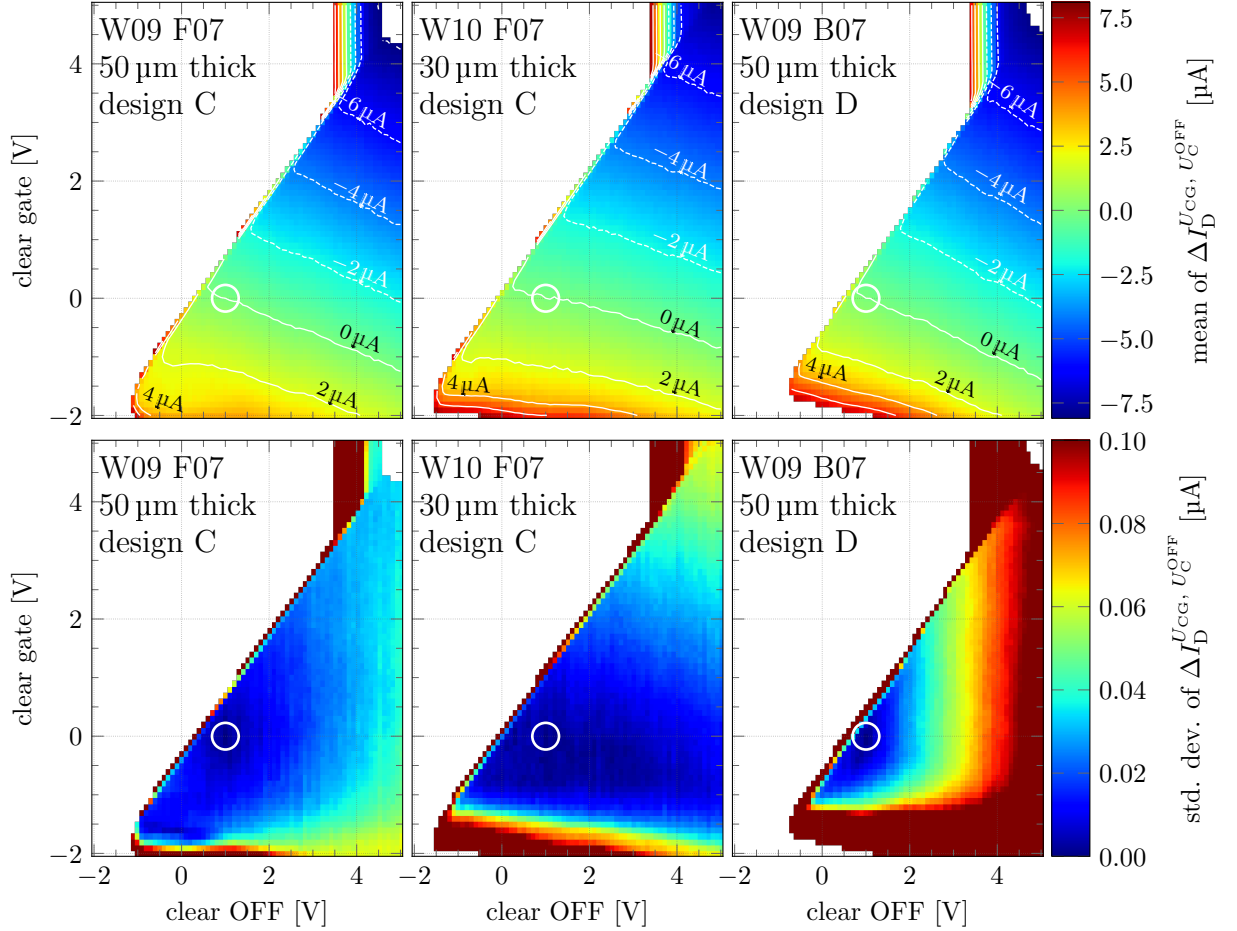


Figure 5.32: Comparison of the dark operation window scans performed on three different PMATs; the main design 50 μm thick W09 F07 (left), the main design 30 μm thick W10 F07 (middle), and the experimental design 50 μm thick W09 B07 (right). Four pixels were measured on each PMAT. The measurement points where the measured quantity of any pixel is beyond the limits, due to the e^- back-emission or parasitic channel, is masked away, i.e., shown in white colour. Apart from this the plot has the same structure as described in Fig. 5.31 caption. The mean values of four pixels are shown on the upper plot, and their standard deviations on the lower.

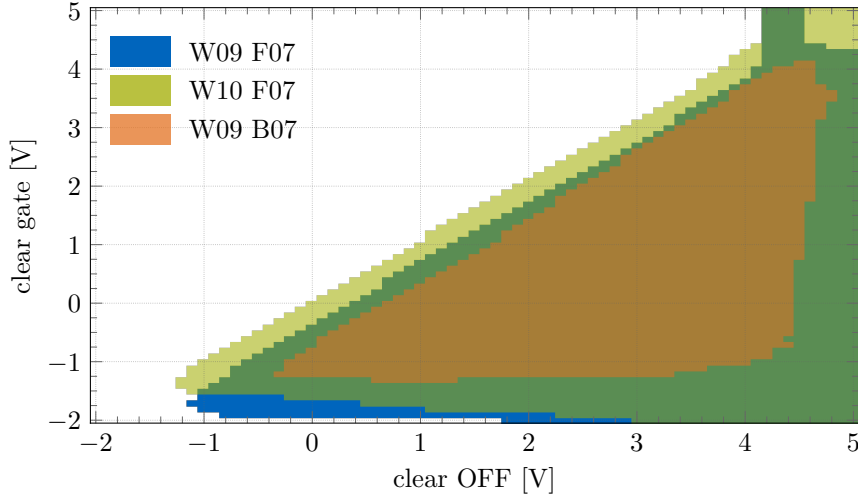


Figure 5.33: Direct comparison of the measured dark operation windows for the W09 F07, W10 F07 and W09 B07 PMATs.

Illuminated scan To investigate the effects of operation window parameters on the charge collection, an illuminated operation window scan was performed. In it, the consecutive clear pulses (t_{EXP}) were 1.885 ms apart, in order to have enough time between them for 257 LED illumination pulses with consequent integrations of the drain current. That way the response function of the sensor was measured with sufficient granularity. Because of the relatively long t_{EXP} the contribution of leakage current (I_L) could not be neglected. Therefore, the LED illumination pulses were provided only in every even repetition of the t_{EXP} . On every odd repetition of the t_{EXP} , the drain current was still integrated but there was no LED illumination. By subtracting the odd part of the repetition from the even one the leakage current contribution is effectively removed.

An approximation of the leakage current can be obtained from the sequence repetitions with no LED illumination pulses. Exact number cannot be provided because of the missing energy calibration.¹⁴ In order to extrapolate in which order of magnitude to look for the drain current arising from the leakage current contribution, the following calculations can be made. A 15 fA per $75 \mu\text{m} \times 75 \mu\text{m}$ pixel is a typical number [171] from the spectroscopic DePFET pixel for XEUS project [172]. For the EDET DH80k pixel this translates to $0.06 e^-/\mu\text{s}$. But the leakage current depends heavily on the poly-Si area. Consequently, it is expected that EDET DH80k devices will feature higher leakage current as they have much larger poly-Si area. A good area to search would be somewhere from $0.1 e^-/\mu\text{s}$ to $0.5 e^-/\mu\text{s}$. If the SPD pixels with gate length of $4.8 \mu\text{m}$ had the charge amplification factor of around $300 \text{ pA}/e^-$, the PMAT pixels with gate

¹⁴Energy calibration using the radioactive ^{55}Fe source would have to be recorded for every point in the operation window scan. In addition to the long duration of such measurement, since a sufficient statistics is needed in every measurement point, it would also cause radiation damage of the sensor. This is, however, unwanted before the full characterization is completed.

5 Characterization measurements

length of $5\ \mu\text{m}$ have it around $250\ \text{pA}/e^-$ (eq. 5.4). This yields the drain current region, originating from the leakage current contribution, from $50\ \text{nA}$ to $250\ \text{nA}$. Fig. 5.34 shows the mean and standard deviation values of the measured drain current, originating from leakage current contribution, for four pixels that were measured on each of the W09 F07, W10 F07 and W09 B07 PMATs. The two PMATs from the W09 are featuring more or less the same mean results in the vicinity of $150\ \text{nA}$, and the PMAT from W10 shows a slightly higher leakage current that corresponds to around $200\ \text{nA}$ of drain current. None, however, should pose any problems for the final EDET DH80k camera system. With the worst of the above two limiting numbers, an average additional accumulation of around $5e^-$ in the planned t_{EXP} of $12.8\ \mu\text{s}$ can be extrapolated. This is negligible when compared to the planned $800\ ke^-$ originating from tEM's e^- beam.

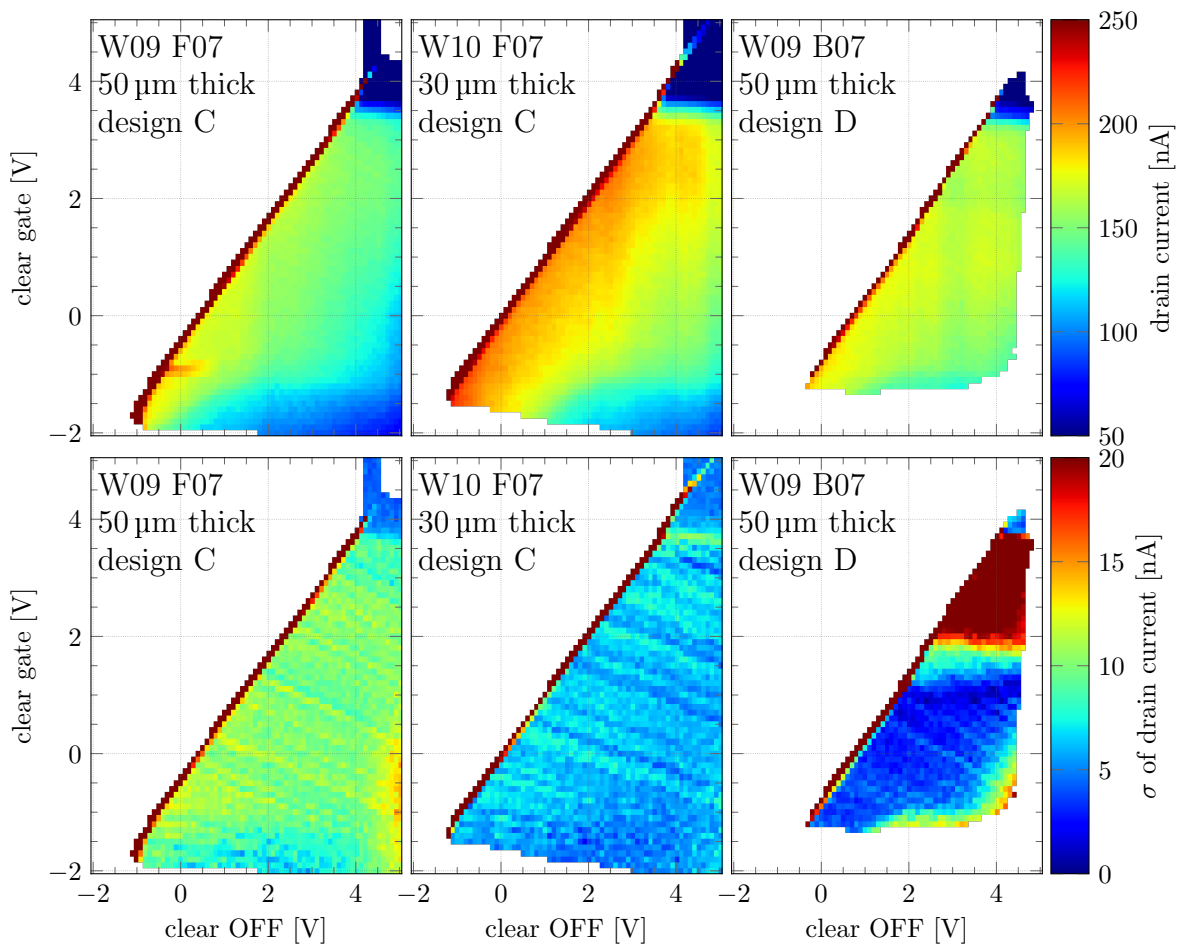


Figure 5.34: Drain current that is a consequence of the DePFET's leakage current measured for four pixels on the W09 F07, W10 F07 and W09 B07 protectPMATs; mean values (upper) and the standard deviation values (lower). Masked away are the measurements outside of the previously determined dark operation windows (Fig. 5.33).

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In regards to the differences between pixels. Both PMATs with the design C have uniform responses of all four pixels over the complete measured area. However, with the experimental design D the differences between pixels become much greater above the U_{CG} of 2 V. This limits the operation window of the design D even more.

Additionally, the diagonal limit from the measured dark operation window should be shifted for an additional quarter of a volt in order to avoid regions with increased leakage current. For the U_{CG} this means a shift towards more negative voltages and for the U_C^{OFF} towards more positive voltages.

Fig. 5.35 shows the heat maps consisting of the normalized charge amplitudes at different operation points in the illuminated operation window scan. From eq. 3.4 it follows that the signal current, corresponding to the collected charge, is

$$I_{SIG} = I_D - I_{OFFS} .$$

The I_D is the drain current measured after every charge injection, and the I_{OFFS} is the drain current before the first charge injection, i.e., the offset current. The heat maps are shown for three different levels of the injected charge that correspond with three different levels of signal drain currents. The top row is for the level that corresponds to 33 μ A, the middle row for approximately 66 μ A, and the bottom row for approximately 97 μ A. The columns again represent three different PMATs, i.e., the left column is showing the results from the W09 F07 PMAT, the middle from the W10 F07 PMAT, and the right from the W09 B07 PMAT. All signal currents are normalized to the signal current at the U_{CG} of 0 V and U_C^{OFF} of 1 V (marked with white circle on all plots)

$$\text{normalized charge} = \frac{I_{SIG}^{U_{CG}, U_C^{OFF}}}{I_{SIG}^{U_{CG}, U_C^{OFF}} \Big|_{U_{CG}=0\text{V}, U_C^{OFF}=1\text{V}}} \times 100 \% .$$

Because of the normalization, the result is invariant to the changes in the channel width that occur due to variable biasing conditions of the U_{CG} and U_C^{OFF} . This follows from eq. 3.7, where the channel width is represented twice in the $g_{q, \text{corr}}$ and is effectively cancelled out. Consequently, the plots are showing charge losses. Too positive biasing of the either of the two contacts leads to the reduction in collected charge. The limiting case for charge losses is set at 10 % of the charge collected in the normalization point.

From the plots it can be concluded that in order to maximize the collected charge the PMATs should be operated close to the bottom left tip of the operation window. However, the EDET DH80k devices will be irradiated with energetic e^- that cause oxide radiation damage (chapter 6). This damage causes a positive shift in potentials under the gate and CG structures (sec. 3.3). If the irradiation is homogeneous over the complete sensor, the shift can be easily corrected by changing the applied U_G and U_C^{OFF} values. However, if the irradiation is inhomogeneous some pixels can see higher potential shifts than other. In case of the operation where the collected charge is maximized, this can quickly lead to problems. As the window of good CG biasing conditions in that point is tiny, the pixels with more radiation damage can quickly end up in the back-emission

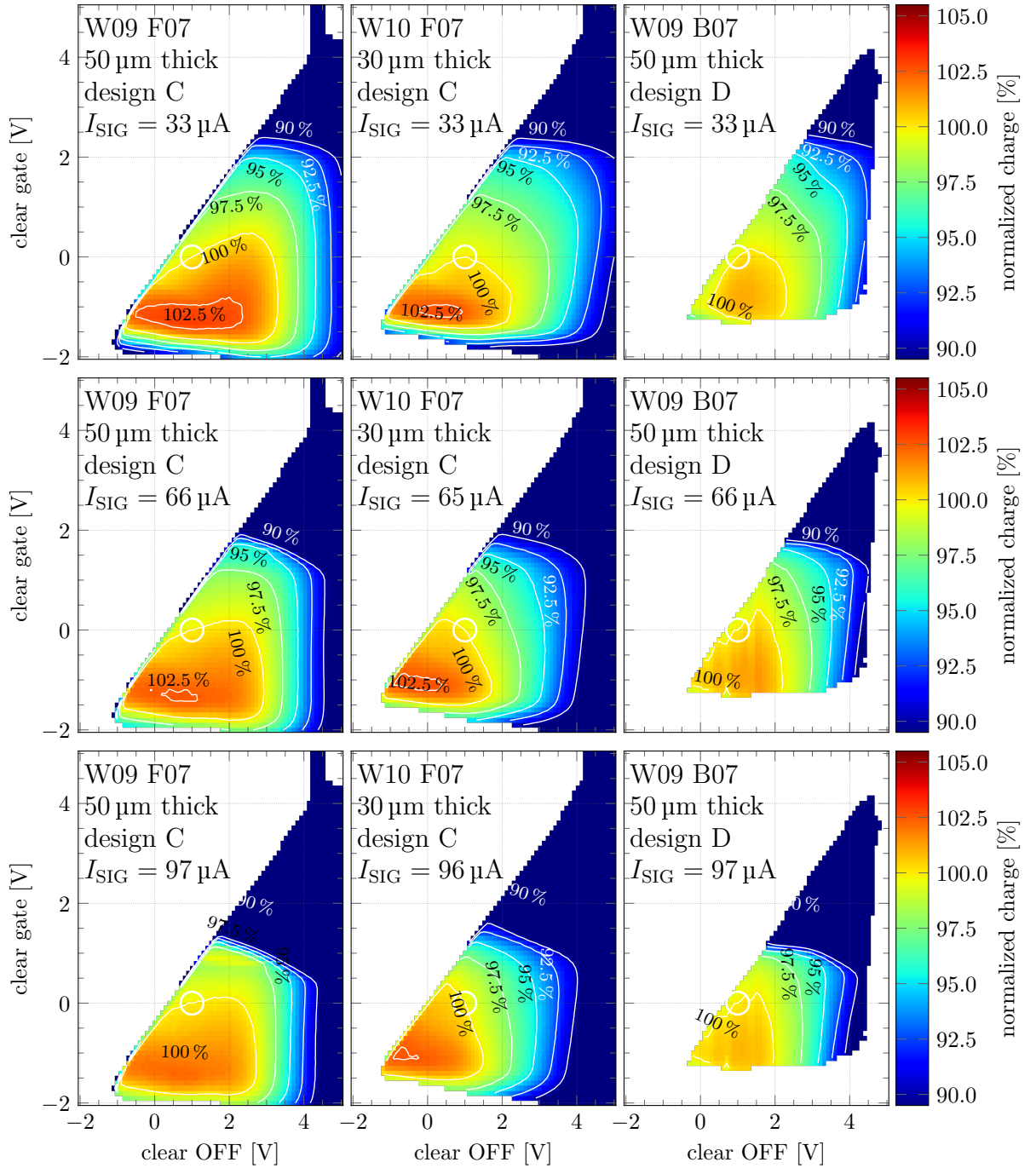


Figure 5.35: Heat maps for three PMATs depicting the charge losses in illuminated operation window scan; W09 F07 (left), W10 F07 (middle), and W09 B07 (right). Three rows represent different levels of injected charge represented with the levels of signal current; $33 \mu\text{A}$ (top row), approximately $66 \mu\text{A}$ (middle row), and approximately $97 \mu\text{A}$ (bottom row). Signal currents are normalized to the measured signal current at U_{CG} of 0 V and $U_{\text{C}}^{\text{OFF}}$ of 1 V – white circles.

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region. Therefore, it could be beneficial to operate the devices at more positive U_C^{OFF} voltages, as they offer a much bigger operation window on the CG structure.

Comparison of the operation windows for all three PMATs is presented in Fig. 5.36. On it the cuts from all above used limitations are joined together. This means that in addition to the cuts presented in Fig. 5.33, limitations were set also on the leakage current, charge loss and parasitic channel.

- The leakage current is limited with the maximum drain current of 250 nA in 1.885 μs long unilluminated sequence between two consecutive clear pulses. On top of that a maximum spread between four pixels is limited to the standard deviation of 20 nA.
- The allowed charge loss is limited to a maximum of 10 % at the signal current level of around 97 μA . This corresponds to around 1 Me^- collected in the charge storage regions.
- The parasitic channel limitation is set with a low limit on the CG voltage at -1.4 V .

The biggest operation window on the CG parameter is obtained with the W10 F07 PMAT. It yields a 3.1 V big opening on the U_{CG} at the U_C^{OFF} of 1.6 V. The W09 F07 PMAT features an opening of 2.9 V at the U_C^{OFF} of 1.8 V. The smallest operation window in all parameters is measured with the W09 B07 PMAT that features an experimental pixel design of the type D. It offers an opening of 2.4 V at the U_C^{OFF} of 2 V.

The consequence of possible inhomogeneous irradiation is shown in Fig. 5.37. Here the one-dimensional slices through the two-dimensional measurements shown in Fig. 5.35 are presented. The slices are made at the U_C^{OFF} where the operation window of the U_{CG} is maximized (Fig. 5.36). The charge shown is normalized to the point where U_{CG} is -1 V . At the start of the imaging with the EDET DH80k camera system all pixels can

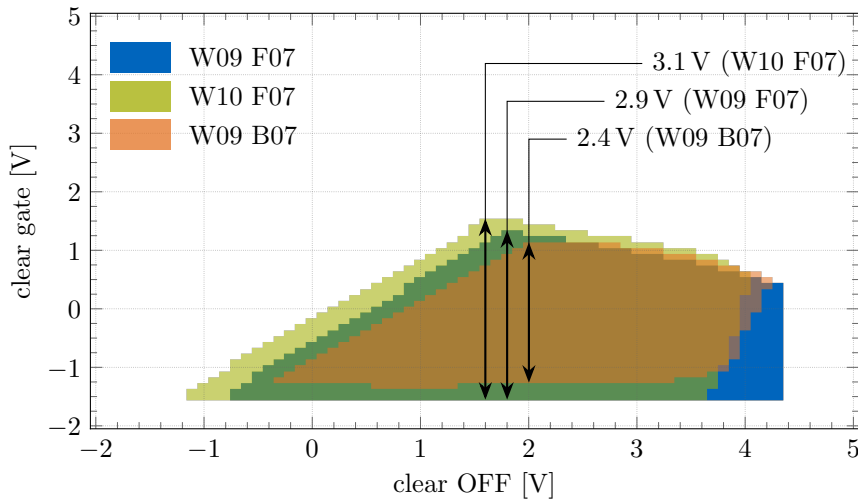


Figure 5.36: Direct comparison of the final operation windows for the W09 F07, W10 F07 and W09 B07 PMATs. Additionally, the maximum operation window on the CG parameter is explicitly shown for each PMAT separately.

be biased with the U_{CG} of -1 V, and all of them are collecting the same amount of charge. After some time of inhomogeneous irradiation, pixels with no radiation damage see the same potentials under the CG, whereas the potentials in ones that are damage shift to more positive voltages. With this they effectively start to loose charge storage capabilities. Both F07 PMATs show similar behaviour between themselves and also between the tested pixels. By accruing of 1 V to 1.5 V of the U_{CG} shift, the losses for all pixels are in the range of 2%. The behaviour of the B07 PMAT, however, is showing bigger differences between pixels that share the same source. This means that a small change in potential under the CG can lead to a significant difference in the response of neighbouring pixels. Consequently, it can be inferred that the omission of CG bridges, separating the clear and drift regions, is not beneficial. Why pixels from this device behave so differently is still unanswered.

One unknown effect that was unknown until this point is the so called source spillover. This is first shown on the left plot in Fig. 5.37, and further explained in Fig. 5.38. The weakest potential barrier between the charge storage regions of two adjacent pixels that

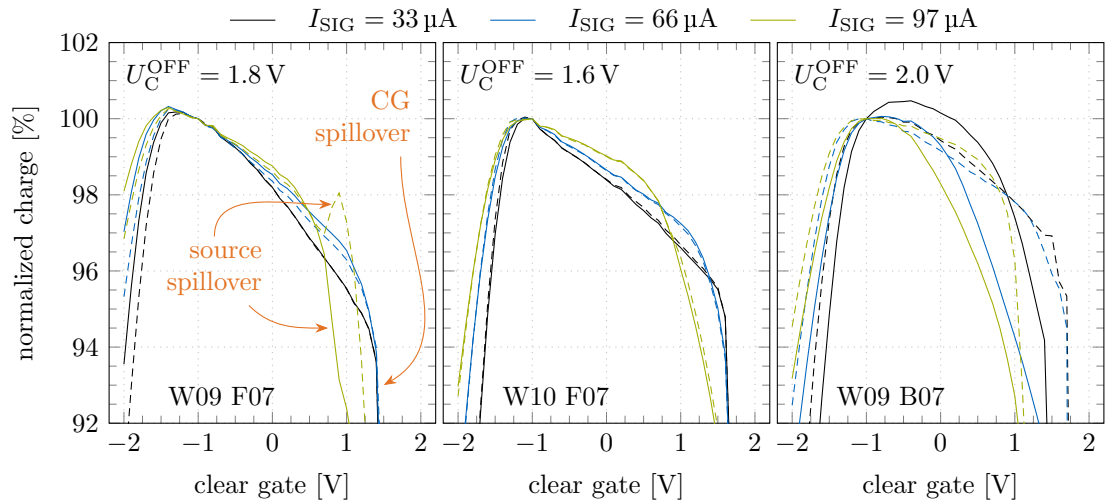


Figure 5.37: One-dimensional slices of the measurements presented in Fig. 5.35 through the U_C^{OFF} where the maximum operation window on the U_{CG} parameter is located (Fig. 5.36). Six lines are shown with two different line styles and three different colours, each of them is normalized to the charge measured at the U_{CG} of -2 V. Different line styles represent two pixels that share the source, and different colours represent different levels of injected charge through the signal drain current I_{SIG} . With orange colour two effects are denoted. The CG spillover happens when the barrier set by the CG is overcome and any additional e^- coming to the charge storage regions drift further to the clear region. The source spillover happens when the barrier set by the source is overcome. This barrier separates the charge storage regions of two neighbouring pixels that share the source. Now e^- that should be collected in one pixel, get collected in its neighbour. This leads to the increase of normalized charge amplitude in one and steep decrease in the other. Additional explanation of the source spillover is shown in Fig. 5.38.

share the source is not the barrier below the CG, but the barrier below source. When enough e^- are collected in charge storage regions of one pixel the barrier below source can be overcome. If the neighbouring pixel has less e^- in its charge storage regions, it will collect e^- from both pixels until it reaches the same level. When the same level is reached both pixels will continue to collect e^- until they reach the CG spillover point, and all further e^- start to overflow to the clear contact.

The level of collected e^- at which the source spillover effect happens cannot be determined from this measurement. In order to be able to do so pixels need to be calibrated. This will be done at a later point in the thesis where the response function of the pixels with optimized biasing parameters will be measured. As the e^- are not lost due to this effect it only influences the position resolution of the sensor.

The source spillover effect is not shown in any of the simulations performed by R. Richter and K. Gärtner. Reason for this is that the three-dimensional simulations included only one pixel. As the simulation tool uses symmetrical boundary conditions, e^- cannot overflow to the neighbouring pixel as it has the exact same fill. In order to simulate the effect, the simulations would have to be repeated by simulating a minimum of two pixels that share the same source.

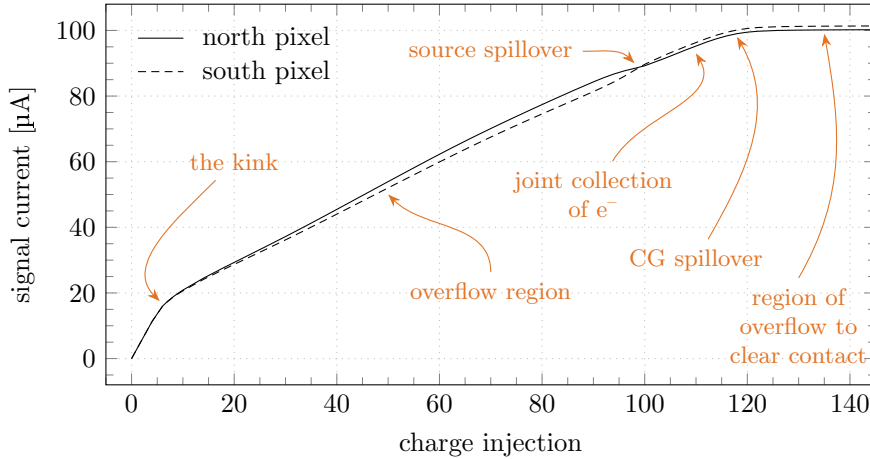


Figure 5.38: Response function of the two pixels from the W09 F07 PMAT that share the source. The U_C^{OFF} of 1.8 V and U_{CG} of -1 V were selected so that a source spillover effect is shown (left plot in Fig. 5.37).

5.3.1.2 Incomplete clear scan

The clearing process is essentially moving of the e^- from the old potential minimum, i.e., charge storage regions, to the new potential minimum, i.e., clear region during the clear pulse. When this process is complete the spread of the system's noise peak, i.e., ENC, is a consequence of the contributions described in sec. 3.2. However, if there exist a potential barrier that prevents the removal of a small fraction of most tightly bound e^- the system's noise peak broadens because of the variation in their number. This process

can be compared with the leakage current in a reverse biased diode [121]. Charge carriers there also have to overcome a potential barrier, and their average number is constant but Poisson distributed.¹⁵ Consequently, if there exist a small potential barrier that prevents the removal of most tightly bound e^- from the IG, their number (N) will in average be constant. However, as the e^- follow the Poisson distribution, their number will vary with the standard deviation of \sqrt{N} . Consequently, the width of the system's noise peak will broaden by this contribution.

The most tightly bound e^- in the internal gate (IG) are the hardest to remove. Therefore, there is no need to inject a lot of e^- to the pixels for this scan. The biasing conditions of PMATs were the same as in the operation window scan (Tab. 5.13), with the difference that the U_{CG} and U_C^{OFF} were respectively biased statically at 0 V and 1 V, and the U_C^{ON} was swept from 6 V to 19 V in 0.1 V steps, all with regards to the U_C^{OFF} . The operation sequence consisted of 100 μ s between the two consecutive clear pulses. A tiny amount¹⁶ of e^- , corresponding to the signal drain current of 1 μ A to 2 μ A, was injected in every second repetition with the linear high-speed LED. That way the amount amount of e^- collected was tracked and the system's noise as well.

Fig. 5.39 shows the results of such scans performed on three different PMATs. The upper plot tracks the spread of the system's noise peak and the lower one shows the normalized amount of collected charge. On each PMAT four pixels were measured and their mean value with ± 1 standard deviation is shown. In order to assert that the complete clear of the charge storage regions is achieved, two conditions must be met:

- the spread of the system's noise peak must be minimized, and
- the collected charge must be maximized.

This is achieved at the U_C^{ON} of 12.75 V for the W09 F07 PMAT, 13.5 V for the W10 F07 PMAT, and 15.5 V for the W09 B07 PMAT – depicted on the plot with dashed vertical lines in the colour of each PMAT. The assumption that the IG is completely empty at mentioned values was verified with additional measurements not presented in this thesis. There, multiple consecutive pulses were generated one after another and the sigma level of the noise peak did not change. The lower the U_C^{ON} value the better. Consequently, the two F07 PMATs featuring the main design type C offer better performance than the experimental design type D on the W09 B07 PMAT.

Although these scans were taken at reference levels only, the results can be used to adapt operation parameters for arbitrary operating conditions if one considers the dependencies of biasing the U_C^{OFF} and U_{CG} .

For Fig. 5.40, an incomplete clear scan was performed on W09 F07 PMAT at three different U_C^{OFF} conditions. For all three conditions the U_{CG} was kept at 0 V. The result shown in black colour is the same as the one shown with black colour in Fig. 5.39, and represents the U_C^{OFF} condition of 1 V. Two additional scans were performed, one with 0.5 V higher U_C^{OFF} and one with 0.5 V lower. As the results from all three scans overlap it is clear that the clearing capability depends on the difference between the U_C^{ON} and U_C^{OFF} , which in case of the W09 F07 PMAT needs to be higher than 12.75 V.

¹⁵Under the assumption of constant conditions.

¹⁶An exact number is not necessary for this scan, however, it was kept constant during the scan.

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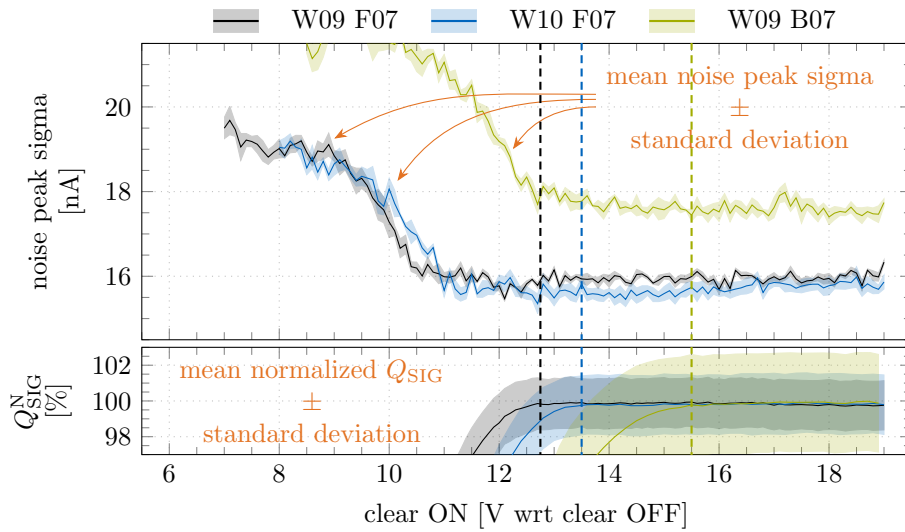


Figure 5.39: Changes of the spread of the noise peak and the normalized amount of the injected e^- (Q_{SIG}^N) in dependence of the U_C^{ON} for three PMATs. U_C^{ON} is measured with respect to the U_C^{OFF} voltage. The amount of injected e^- varied slightly across PMATs, but in general it was proportional to the I_{SIG} of roughly $1 \mu A$. Normalization was done to the highest measured I_{SIG} on each PMAT. Minimum U_C^{ON} voltage, where the spread of the noise peak is minimized and the Q_{SIG}^N is maximized, is at 12.75 V for the W09 F07, 13.5 V for the W10 F07, and 15.5 V for the W09 B07.

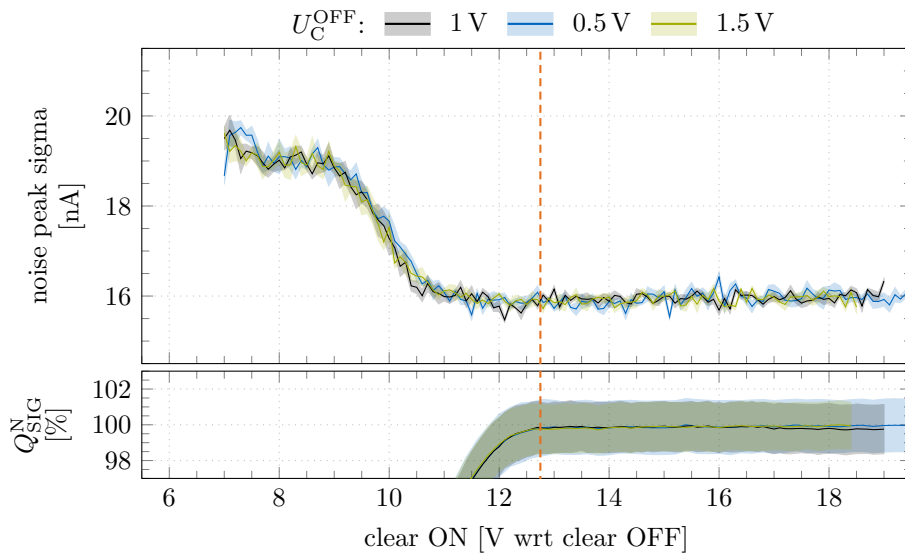


Figure 5.40: Influence of the applied U_C^{OFF} on the clearing capabilities. Data from the W09 F07 PMAT with the U_{CG} set to 0 V. Clearing capability depends on the difference between the U_C^{ON} and U_C^{OFF} . All three measurements show complete clear when the difference is higher than 12.75 V (dashed orange line).

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The second dependency – the U_{CG} dependency – is more crucial as it is setting the barrier potential between the charge storage regions and the clear region. Setting the U_{CG} very negative makes the barrier higher. However, the U_{CG} is capacitively coupled to the clear. This means that the CG pulse amplitude corresponds to the level of U_C^{ON} , measured with respect to the U_C^{OFF} , multiplied by the ratio of respective capacitances. Consequently, it is expected that if the U_{CG} is more negative the U_C^{ON} has to be higher in order to weaken the barrier. This is presented in Fig. 5.41, where an incomplete clear scan was performed on W09 F07 PMAT at three different U_{CG} conditions. For all conditions the U_C^{OFF} was kept at 1 V. The result shown in black colour is the same as the one shown with black colour in Fig. 5.39, and represents the U_{CG} condition of 0 V. Around that condition, two scans were performed with the U_{CG} set to -0.5 V and 0.5 V. The minimum U_C^{ON} needed for the complete clear changes in steps of 1.5 V for every half volt of a change of the U_{CG} .

In order to operate a new camera, that has not yet been damaged by irradiation, at the point optimized for the irradiation damage, i.e., at the U_C^{OFF} where the U_{CG} operation window is maximized and U_{CG} of -1 V, the minimum necessary difference between the U_C^{ON} and U_C^{OFF} has to be 3 V higher than the one measured in Fig. 5.39.

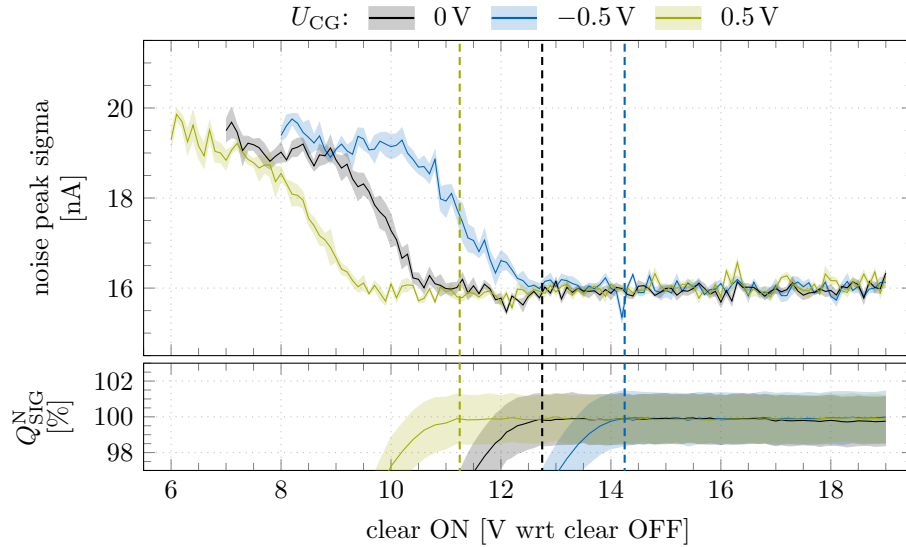


Figure 5.41: Influence of the applied U_{CG} on the clearing capabilities. Measurements were performed on the W09 F07 PMAT with the U_C^{OFF} set to 1 V. 0.5 V of a change on the U_{CG} causes a -1.5 V shift of the minimum necessary difference between the U_C^{ON} and U_C^{OFF} for the complete clear.

5.3.1.3 Charge collection scan

The last two parameters that have a significant influence over the DePFET's response to the incoming radiation are the punch-through (U_{PT}) and drift (U_{DRI}) voltages. In

this section, an investigation of the influence of those two operation parameters over the charge collection efficiency will be presented.

In general, the punch-through (PT) method (sec. 2.2.1) is used to deplete the Si bulk and also provide the vertical drift field for charge carriers. However, the U_{PT} applied to the PT contact also influences the charge amplification factors and charge losses. A more negative U_{PT} pushes the e^- in charge storage regions closer to the transistor channel. The closer they are the more mirror charges they induce in the channel, and the fractional value of the factor f in eq. 3.7 increases. On the other hand, the U_{PT} also affects the potential barrier below the clear set by the deep p implantation. The more negative the U_{PT} , the lower the potential barrier and consequently the more probable that signal e^- are permanently lost into the clear. However, in the current setup the two processes are indistinguishable between each other. Consequently, one cannot determine where the charge losses actually start, but can only determine where the response of the sensor is maximized. Beyond this point the sensor should not be operated, as the charge losses start to dominate and more and more of the original information about ionizing radiation is lost. For the science case of EDET DH80k project, the level of charge losses occurring at the point where the response is maximized will not be observable due to the coarse granularity of the DCD ASICs. As a future outlook, one could design a laser injection system that introduces e^-/h^+ pairs into the Si bulk over a tiny fraction of the pixel area. That way, under the fixed biasing conditions different regions could be determined, e.g., regions where charge losses dominate and regions where there is no charge losses or they are minimized. From there the two effects could be unravelled.

The U_{DRI} applied to the drift region influences the lateral drift fields in the Si bulk, and it creates a boundary between pixels from different double rows it separates. The undesirable effects of the U_{DRI} are the following. If biased too positively, it can generate a potential pocket if the barrier set by the clear gate is too high, whereas if biased too negatively it can cause a non-uniform response over the array. Non-uniform response is a consequence of the current flow through the drift implantation, which is caused by the parasitic h^+ paths between neighbouring p^+ -type implantations. As the resistivity of the drift implantation is very high, even a small current on it leads to a significant voltage drop over it.

The biasing conditions for the charge collection scans performed on three PMATs are gathered in Tab. 5.14. In addition to them the U_{DRI} and U_{PT} were swept. The former was swept between 0 V and -10 V, and the latter between -7 V and -41 V for the $50\ \mu\text{m}$ thick PMATs from PXD10-1 wafer W09 and between -5 V and -17 V for the $30\ \mu\text{m}$ thick PMAT from PXD10-1 wafer W10. The step for all sweeps was 0.25 V. There was always $100\ \mu\text{s}$ between the consecutive clear pulses and the charge was injected every second repetition in order to allow for tracking of the signal and noise levels.

One-dimensional slices An introduction to the complete charge collection scan is first explained on two one-dimensional voltage sweeps. This is presented in Fig. 5.42, where two one-dimensional slices from the overall charge collection scan are shown from a single pixel on the W09 F07 PMAT. On the left side there is a PT slice at a fixed U_{DRI} of

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Table 5.14: Voltages used for the charge collection scans with the W09 F07, W10 F07 and W09 B07 PMATs.

U_S	U_D	U_G^{ON}	U_G^{OFF}	U_G^{ALL}	U_C^{ON}	U_C^{OFF}	U_C^{ALL}	U_{CG}	U_{CE}
[V]	[V]	[V]	[V]	[V]	[V]	[V]	[V]	[V]	[V]
0	-5	varied ^a	5	5	varied ^b	1	10	0	10

^a Voltage evaluated for every PMAT separately so that $I_{OFFS} \sim 100 \mu A$. The evaluation was done at the PT of $-25 V$ ($-10 V$) for PMATs from the wafer W09 (W10), and drift of $-5 V$. For the F07 design this resulted in $-2.18 V$, and for the B07 in $-1.86 V$.

^b Measured with regards to the U_C^{OFF} voltage. For the PMATs with the F07 design $15 V$ was used, and for the B07 $17 V$.

$-5 V$, and on the right the drift slice at a fixed U_{PT} of $-25 V$. On both plots there are two curves of different colours that represent different amplitudes of injected charge. Black colour represents a small amount of signal charge that fills only a portion of the internal gate (IG), whereas the blue colour denotes a bigger amount of signal charge that completely fills the IG and also a part of the overflow region (OF).

The behaviour in the PT slice is as described above. From $-10 V$ to around $-23 V$ the increase in charge amplification factor dominates and afterwards the charge losses overtake. The fraction of the lost charge is much larger for smaller amounts of injected charge. In absolute terms the charge losses for the blue curve are 12 times the size of those at the black curve. However, an expected outcome would be that, relatively speaking, the same amount of charge is lost in both cases. Since if there exist a significant probability for e^- to overcome the potential barrier, this probability should not depend on the amount of e^- . Therefore, those differences will be a subject of further studies through both the simulations and measurements. By narrowing down the response to 1% around the maximized response level, the parameter window is $8 V$ ($14 V$) for a small (big) amount of injected charge.

Behaviour of the two curves in the drift slice differs significantly. At too positive drift voltages the lateral drift field is not sufficient to move the e^- from the drift contact into the internal gate. Through the normalized scale it looks much worse for small amounts of injected charge than for the big ones. However, small losses on small levels of injected charge can show themselves as high relative losses. At very negative drift voltages a parasitic current path between source and drift implantations can occur. The current path is enabled over the deep p implantation, which in turn reduces the formed potential barrier. However, barrier is still strong enough to prevent losses in case of small amounts of injected charge but not for large amounts. Therefore, in case of the former the collection efficiency increases towards the most negative voltages, whereas in the latter case there exist a maximum at around $-6 V$. With the same 1% limit as

before, the parameter window in case of small amount of injected charge is limited to 3.5 V, but for the big amounts of injected charge the complete shown range is available.

In order to completely understand the origin of the described effects detailed three-dimensional simulations of the EDET DH80k pixel design with the state-of-the-art simulation tools would be necessary. However, charge losses of the 1% range that originate from imperfectly biased U_{DRI} and U_{PT} will not cause problems for the EDET DH80k science case. This is because the intended use of the EDET DH80k sensors is for transmission electron microscopy (TEM). The number of primary electrons in TEM is following the Poisson distribution. By imaging with 100 e^- per pixel this yields a 10% error.

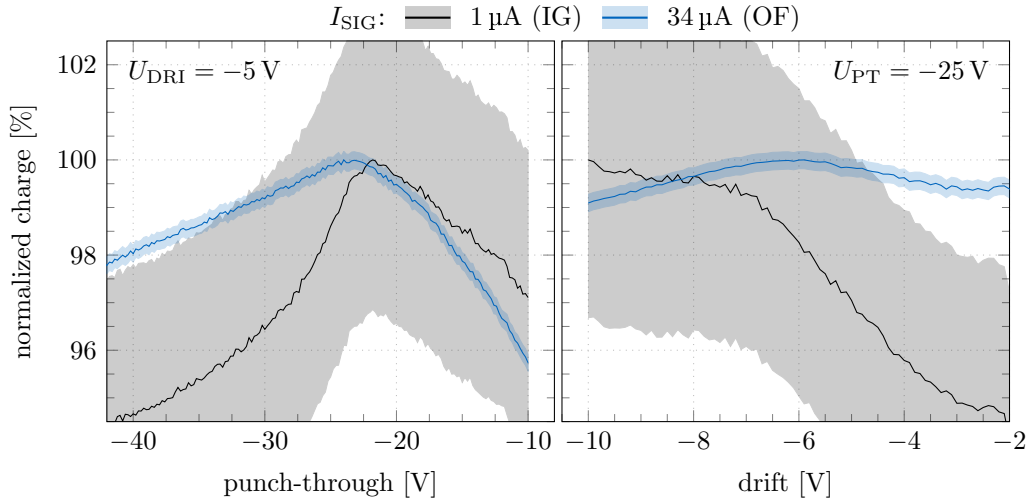


Figure 5.42: Two one-dimensional scans for the charge collection studies that were performed on the W09 F07 PMAT; PT (left) and drift (right). For the PT scan the U_{DRI} was fixed at -5 V , and for the drift scan the U_{PT} was constant at -25 V . Two different levels of charge were injected into the sensor for both scans. The black colour is for the low level of signal charge that is collected only in the IG and at a maximum corresponds to the I_{SIG} of $1 \mu\text{A}$. A higher amount of injected charge – equivalent to the maximum I_{SIG} of $34 \mu\text{A}$ – is shown in blue colour. That way the IG was completely filled and the charge was collected in OF as well. All curves feature the mean value of the normalized charge ± 1 standard deviation band.

Asymmetric boundaries Under this paragraph an explanation as to why the results from only a single pixel, out of four measured, are presented throughout this section. The target of the charge collection analysis is to evaluate the response under the same operating conditions as will be present in the final experiment. However, four connected pixels have different boundary conditions that influence their charge collection areas. Therefore, the pixels do not behave identically (Fig. 5.43). The SPIX’s discrete drain current readout board (DROB) is not suitable to cope with the high density, topologically optimized EDET DH80k DePFET readout. Single electrical row controls two double

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physical rows of pixels (sec. 3.4). In order to readout one minimum cell (Fig. 3.12), that gets repeated throughout the array, four readout channels are necessary. As only four channels are available on the DROB, it is not possible to read out multiple minimum cells from adjacent rows in the rolling shutter mode. Therefore, only one electrical row on the array is activated and dynamically controlled, whereas the rest is statically biased. This leads to different border conditions for charge collection areas. Statically biased pixels have a relatively positive all clear voltage (U_C^{ALL}) of around 10 V to assure that the charge generated in those pixels is cleared away after the charge storage regions are filled. However, the U_C^{ALL} influences the charge collection area and can lead to differences between the pixels connected to the DROB. Pixels on the north side have representative border conditions, as their northern neighbours have the exact same biasing conditions.¹⁷ This, however, is not the case for the south pixels. Their southern border depends on the applied U_C^{ALL} . Consequently, they can have significantly different responses to the injected charge when compared to the north pixels. Therefore, the conditions in south pixels are not representing the conditions in final experiment.

Evidence of the described differences is presented in Fig. 5.44. The left plot shows the response of the north pixel at two different U_C^{ALL} conditions from the drift slice of the charge collection scan. This pixel has the representative border conditions, and as the distance to the statically biased part of the array is big, it shows a minimal dependency on the U_C^{ALL} in both scans. The same is not true for the south pixel presented on the right plot. Here the difference between the two conditions is significant. As the target of

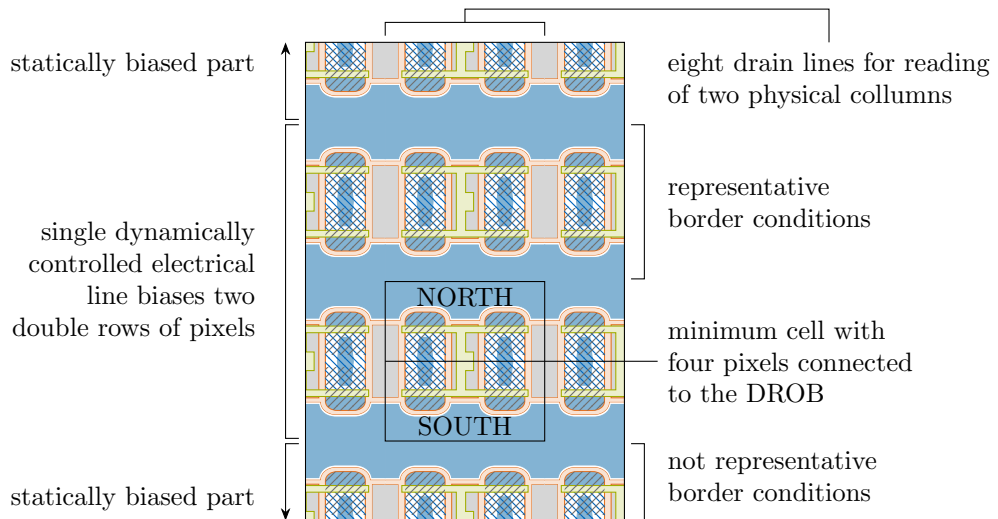


Figure 5.43: A single electrical row turns on two double rows of pixels but the SPIX measurement system can only control four pixels from a single double row. Consequently, the pixels to the north have different boundary conditions, for the charge collection areas, than the ones to the south.

¹⁷Representative towards the conditions in the final experiment.

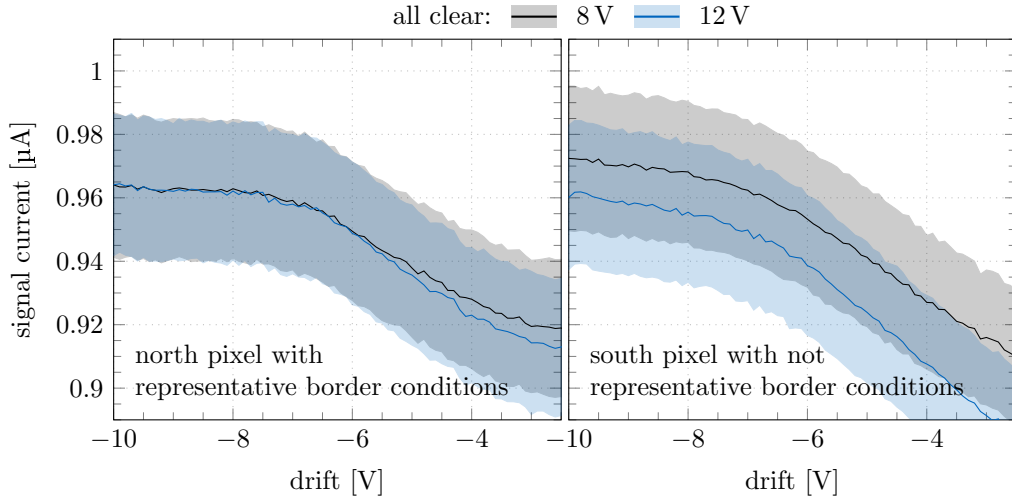


Figure 5.44: Different boundary conditions are a consequence of the intricate electrical design of EDET DH80k arrays and their incompatibility with the SPIX measurement system – described in Fig. 5.43. Consequence of this is that the upper two pixels (left plot, denoted with north pixel), and the bottom two pixels (right plot, denoted with south pixel) behave differently. The response of south pixels depends heavily on the conditions applied to the static part of the array. On both plots the response of a single pixel to a small amount of injected charge is shown at two different all clear voltages (U_C^{ALL}). With the north pixel the influence is minimal, whereas with the south pixel the difference is substantial.

the analysis is the evaluation of the array’s behaviour in operating conditions equivalent to the experiment, these pixels are not used for the analysis.

Complete charge collection scans To investigate the effect of U_{DRI} and U_{PT} parameters on the charge collection two-dimensional charge collection scans were performed. Fig. 5.45 is showing the results for complete charge collection scans that were previously presented and explained with one-dimensional slices. On it there is a comparison of three PMATs measured in the scope of this thesis. The left column has the data from the W09 F07 PMAT, the middle column from the W10 F07, and the right column from the W09 B07. The two rows represent different levels of the injected charge. The upper row is for the small amount of injected charge that only fills a fraction of the IG, and the lower row is for the bigger amount of injected charge that in addition to the IG fills also a part of the OF.

Both F07 PMATs that feature the main design C show very similar behaviour. In both cases the best U_{DRI} for the small amount of injected charge is very negative, whereas in a case of big amount of injected charge it shifts towards more positive values. The main difference between the two PMATs is that the U_{PT} scale of the 30 μm thin wafer W10 is much more compressed than the one from the 50 μm thin wafer W09. This is, however, to be expected from eq. 2.7 where the U_{PT} from 30 μm thin wafers are proportional to

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50 μm via the following scaling factor

$$\frac{U_{\text{PT}}^{50\ \mu\text{m}}}{U_{\text{PT}}^{30\ \mu\text{m}}} \propto \frac{(50\ \mu\text{m})^2}{(30\ \mu\text{m})^2} = 2.78.$$

By limiting the global current flows on the PT and drift contacts between $\pm 1\ \text{mA}$, presented in Fig. 5.46, a bit stricter cuts come into play. The small current range is applied in order to avoid unwanted voltage drops over the drift implantation. The limit on the PT current does not cause any nuisances as the regions with the highest values of normalized charge (Fig. 5.45) correspond with the regions of low PT current values (Fig. 5.46). The drift current limit, however, limits the lowest allowed U_{DRI} for both

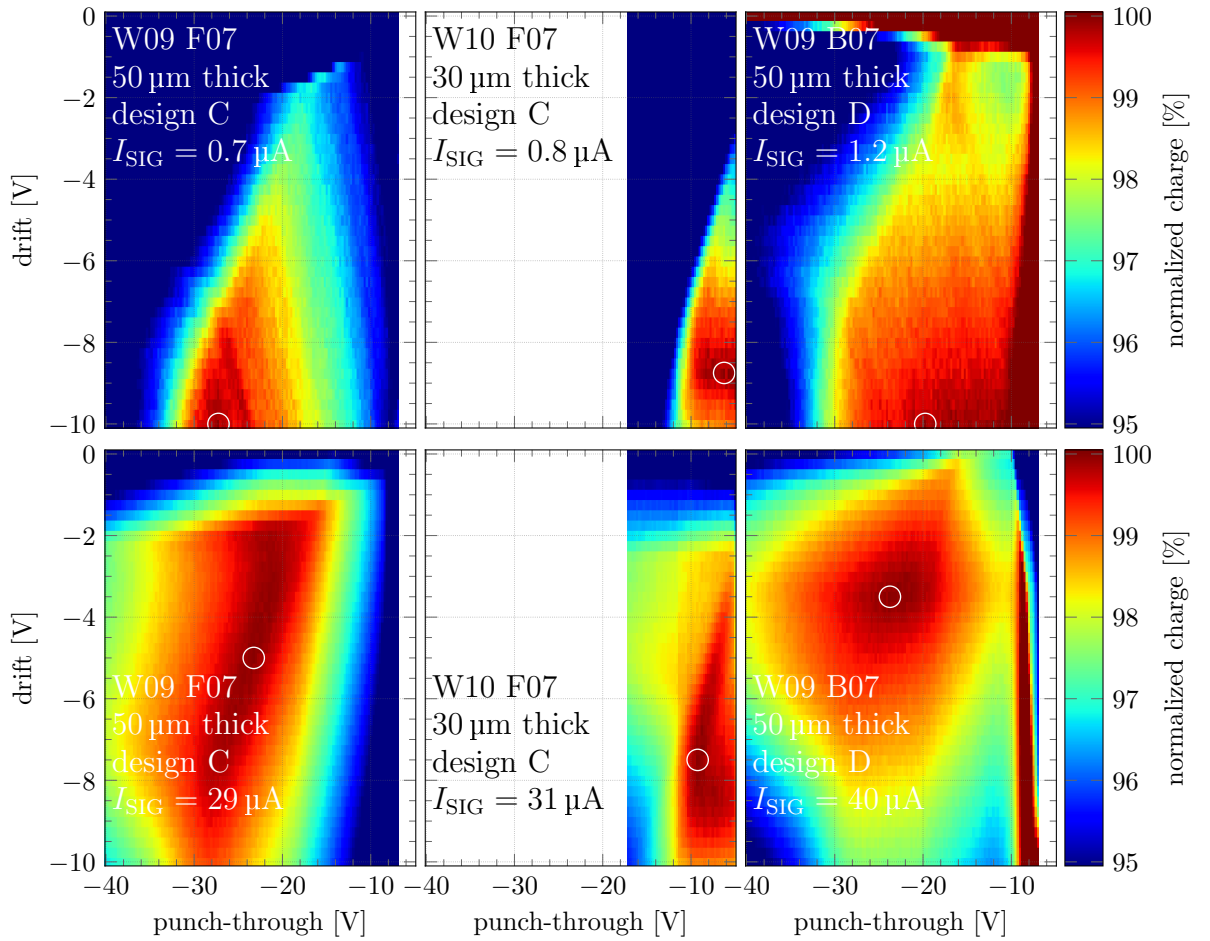


Figure 5.45: Complete charge collection scans for three different PMATs; W09 F07 (left), W10 F07 (middle), and W09 B07 (right). Two rows represent scans performed at different levels of injected charge. In scans from the top row only a fraction of the IG filled with e^- , whereas in the bottom row the IG is completely filled and e^- also overflow to the OF. Colour scale represents the normalized charge amplitude as described under one-dimensional slices in Fig. 5.42.

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F07 PMATs to around -6.5 V. This effectively means that the PMATs should not be operated at the point where the normalized charge amplitude is maximized in case of small amounts of injected charge. But focusing on the bright side, the purpose of the EDET DH80k sensors is bright field imaging which corresponds to big amounts of injected charges. For those cases, the 99% to 100% range of the normalized charge amplitude is still available. In case of the $50\ \mu\text{m}$ thick F07 PMAT the optimum follows the linear trend where

$$U_{\text{DRI}} = 0.8 \cdot U_{\text{PT}} + 14.4\ \text{V}$$

with an average U_{PT} window, limited to 1%, of 14 V around the trend line. For the $30\ \mu\text{m}$ thick F07 PMAT the linear trend is at

$$U_{\text{DRI}} = 0.34 \cdot U_{\text{PT}} - 4.8\ \text{V}$$

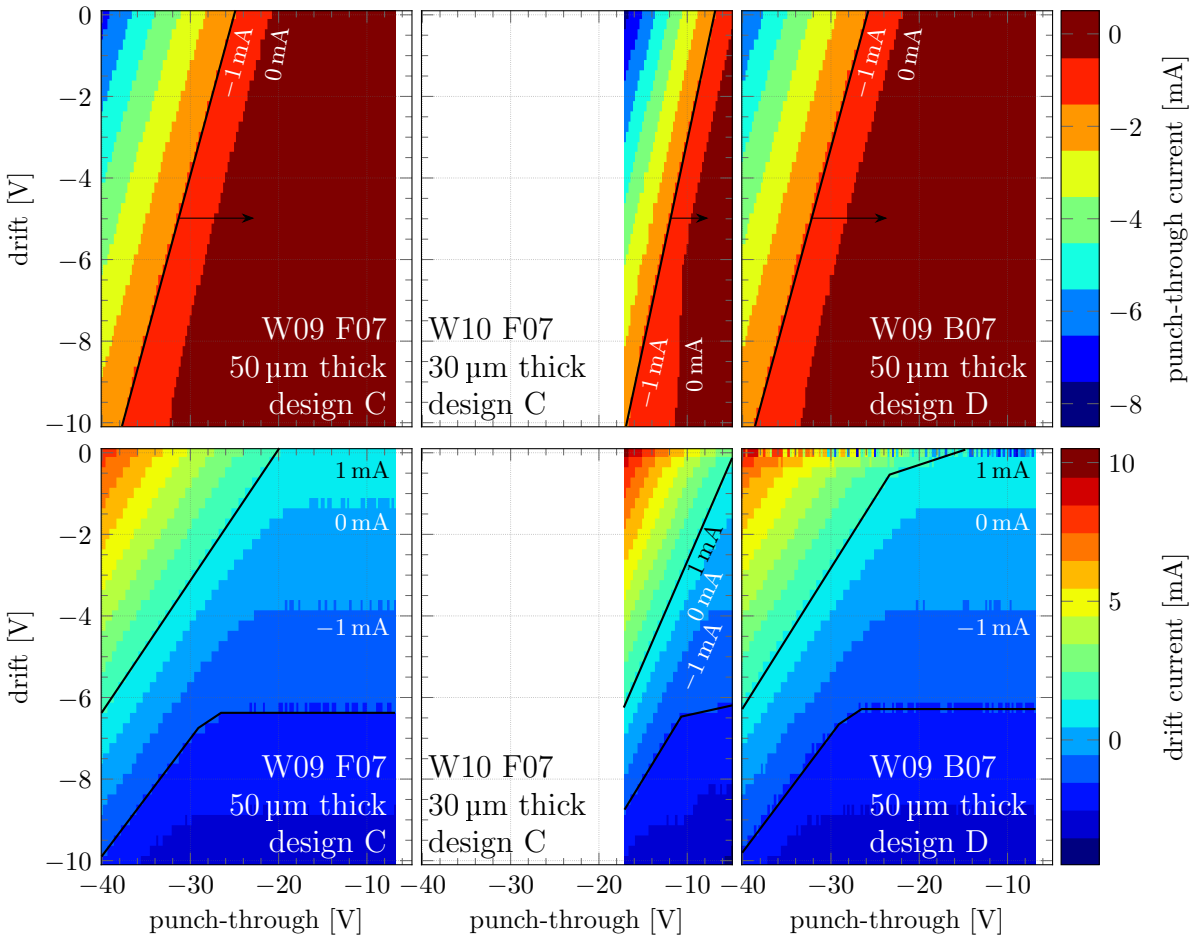


Figure 5.46: Global PMAT currents for the PT (top) and drift (bottom). Measured with the SPIX PSUs during the charge collection scans from Fig. 5.45; W09 F07 (left), W10 F07 (middle), and W09 B07 (right). Additional thick black lines show the limiting currents between -1 mA and 1 mA for the ease of visualization.

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with the average 1% U_{PT} window of 5 V. Comparison of the two observed average U_{PT} windows around the trend lines is also in agreement with the previously stated scaling factor due to thickness differences.

For the last remaining PMAT W09 B07, featuring an experimental design D which omits the clear gate (CG) bridges that separate the clear and drift regions, the charge collection scans are very different when compared with the ones from the F07 PMATs. In both small and big amounts of injected charge the U_{PT} region above -12 V and U_{DRI} region above -1 V have to be neglected. At those voltages the response of the DePFET pixels is different from the expected response function (sec. 3.1.1), and cannot be directly compared. From the perspective of PT and drift currents the W09 B07 behaves as W09 F07. The minimum limit for the U_{DRI} is therefore again set at -6 V. This sets the operation limits so, that the sensor should not be operated in the region where the normalized charge amplitude is maximized for the small amounts of injected charge. In case of the big amounts of injected charge, the W09 B07 PMAT does not show a trend line like the other two PMATs. However, it does show a circular shape around the (U_{PT}, U_{DRI}) point of $(-23.75$ V, -3.5 V) at which the normalized charge amplitude is maximized. From this point the normalized charge amplitude drops equally in all directions. In general, the charge collection window of the W09 B07 PMAT looks better in the PT dimension and worse in the drift dimension. The reason for the worse behaviour in drift could lay in the way the deep p region is implanted. Graphical representation of the following description is presented in Fig. 5.47. The deep p implantation is everywhere in the pixel apart from the source and drain regions, and it is implanted after the structuring of the first poly-Si layer, i.e., after the structuring of the CG, which acts as a mask. By omitting the CG bridges that encapsulate clear regions one omits the separation between the deep p region below the drift and the one below the clear. The h^+ from the source now have to overcome only one CG barrier in order to have an easy path to the drift

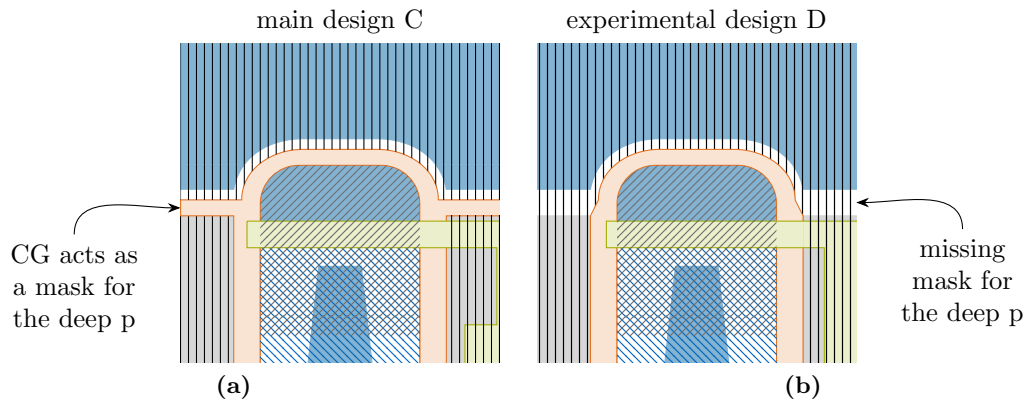


Figure 5.47: Two variations of the PMAT pixel design with added deep p implantation that is represented by vertical black lines; the main design C (a) and the experimental design D (b). All other parts are the same as in Fig. 4.3.

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regions over the deep p implantation. Consequently, the deep p barrier that prevents e^- losses to the clear contact can be weakened by the h^+ current from source to drift.

Additional investigations performed on the W09 F07 PMAT In order to observe the influence of radiation damage on the optima from charge collection scans, the W09 F07 was tested at different U_{CG} conditions with the U_C^{OFF} set to the value where the operation window on the U_{CG} is maximized. The U_C^{OFF} was therefore set in accordance with measurements presented in sec. 5.3.1.1 at 1.8 V. The charge collection scans were then performed at seven different U_{CG} values between -1.5 V and 1.5 V in 0.5 V steps, for both the small and big amounts of injected charge. With different U_{CG} settings one can simulate the behaviour of radiation damage that occurs due to the positive charge trapping in the SiO_2 on the SiO_2/Si interface below the CG structure (sec. 3.3). The remaining voltages were as described in the beginning of this section (Tab. 5.14).

Results from three out of seven measurement points are shown in Fig. 5.48 – on the left plot the U_{CG} is set to -1 V, on the middle one to 0 V, and on the right one to the 1 V. Two different colour maps stand for two levels of the injected charge. The red one stands for big amounts where the IG is completely filled and the e^- are overflowing to the OF, and the blue one is for the small amounts of injected charge where only a fraction of the IG capacity is filled. The limits in both cases are set to 1% of the maximum measured signal current (I_{SIG}) through which the normalization is performed. The maximum measured I_{SIG} is shown on plots with the white circle. From the shown plots it can be deduced that the CG influence on the charge collection efficiency is marginal at best. It only manages to shift the complete result by a bit to the left or right on the PT axis. However, the majority part of the normalized charge distributions from different charge collection scans always overlap.

A different view that takes into account all seven scans is presented in two ways in Fig. 5.49. On the left side all seven measured normalized charge distributions with the same level of injected charge are summed together and renormalized. This results in two normalized charge distributions where one belongs to the small amount of injected charge (blue colour map) and the other to the big (red colour map). The best (U_{PT} , U_{DRI}) operation point for the former is at $(-25.0$ V, -9.5 V) and at $(-19.0$ V, -2.5 V) for the latter. The best operation region for the combined small amount of injected charge is still out of the limits set by the PT and drift current (Fig. 5.46), and for the combined big amount the distribution follows the linear trend as

$$U_{DRI} = 0.8 \cdot U_{PT} + 12.4 \text{ V} ,$$

with the average 1% U_{PT} window of $9 \text{ V} \pm 1 \text{ V}$.

By summing and renormalizing the two combined distributions together one is left with the joined normalized charge distribution shown on the right side in Fig. 5.49. From this distribution the best (PT, drift) operation voltage for the overall performance can be determined. That point is at $(-24.5$ V, -7.25 V). As this is already outside the limits set by the PT and drift currents, it is best to operate the sensor at a 1 V more positive voltages on both the PT and drift.

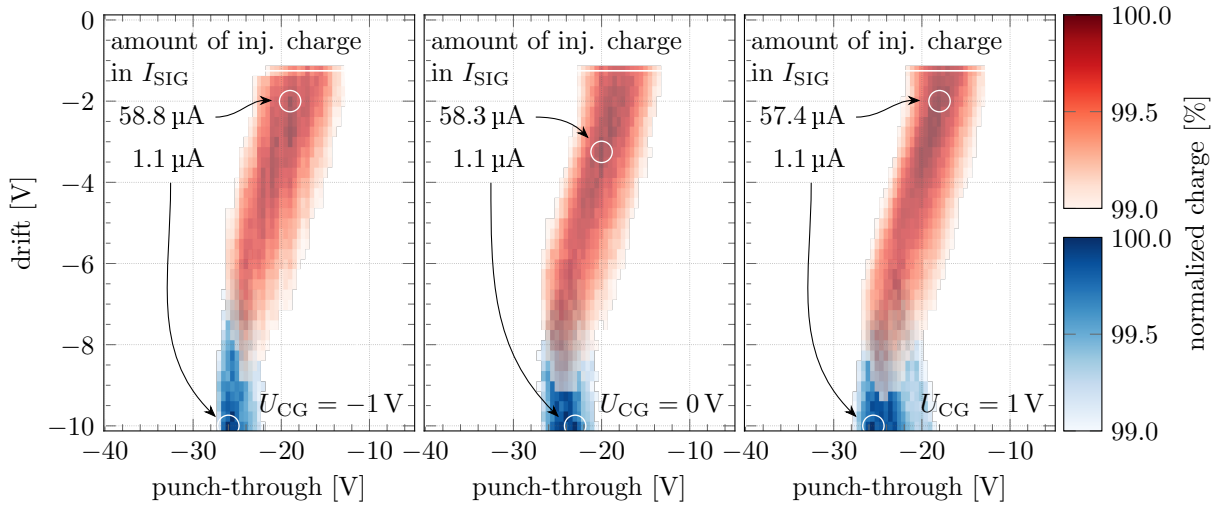


Figure 5.48: Examples of the charge collection scans for the W09 F07 PMAT at U_C^{OFF} of 1.8 V where the U_{CG} operation window is maximized; U_{CG} at -1 V (left), 0 V (middle), and 1 V (right). Different colour scales indicate two levels of the injected charge. Red is for the big amount of injected charge and blue for the small. Both scales are limited to 1% of the respective maximum charge. White circles represent the point where the maximum I_{SIG} is measured, and this point is used for normalization.

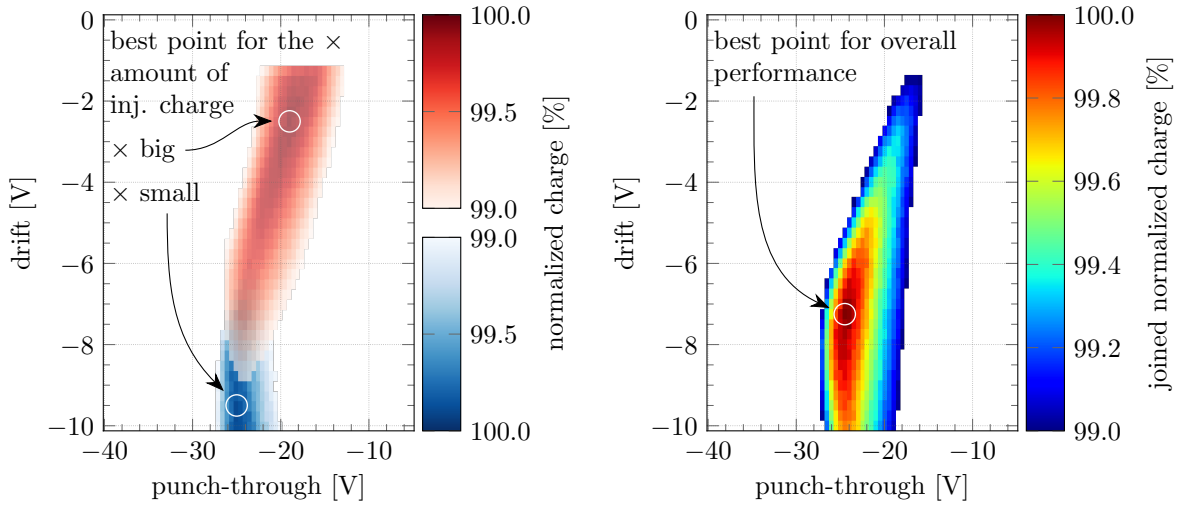


Figure 5.49: Two overall representations of seven charge collection scans from the W09 F07 PMAT at U_C^{OFF} of 1.8 V where the U_{CG} operation window is maximized. Scans with different amounts of the injected charge are treated separately (left) and together (right). The former case yields two optimal $(U_{\text{PT}}, U_{\text{DRI}})$ operation points at $(-25.0$ V, -9.5 V) for small amounts of injected charge and $(-19.0$ V, -2.5 V) for big. The best overall performance for the mixed scenario is evaluated from the latter plot at $(-24.5$ V, -7.25 V).

The three results from Fig. 5.48 give the best operation points for the case of small, big and overall amounts of injected charge. Only with the small amounts of injected charge exists a trade-off between the best possible charge collection and the problems that could arise on the array level due to the current flow to the drift contact. In order to investigate the actual influence of that current the complete array has to be tested with the setup that supports the full array operation. This is, however, not possible with the SPIX measurement system, but will be subject of further investigations.

5.3.2 Response function

Measurements described in the previous section yield multiple operation points that are best for different scenarios. In order to directly compare different scenarios between themselves, measurements in each of them have to be calibrated with a known radioactive source. This means that the radioactive spectra have to be recorded, and afterwards, for each scenario a calibrated response function over the complete dynamic range can be measured as well. A goal of this section is to compare the measurements from different scenarios in order to exactly determine the performance in each of the chosen scenarios. First the selected operation points for different scenarios will be presented, then the measurements and afterwards the comparison of results.

From the operation window scans (sec. 5.3.1.1) three such points are obtained from the (U_{CG}, U_C^{OFF}) domain of measurements. The first is located at the leftmost corner of the operation window (Fig. 5.36). This point is generally the best point for operation of DePFETs when radiation damage is not a concern [171, 173], and will henceforth be named as 'spectroscopy point'. The other two points are obtained from the same scan, at the U_C^{OFF} where the U_{CG} operation window is maximized (Fig. 5.36). One is located at the most negative U_{CG} , just before the onset of the parasitic channel, and the other at the most positive U_{CG} voltage, just before the back-emission probability becomes significant. The former will henceforth be named 'radiation point' as it allows for the most changes due to the radiation, and the latter will be named 'damaged point' as it simulates a positive charge build-up in the SiO_2 that shifts the potential towards more positive voltages (sec. 3.3). The damaged point should give insights to how the response of DePFETs will change with radiation damage. The U_{CG} and U_C^{OFF} pairs for the three described points from all evaluated PMATs are collected in Tab. 5.15.

From the charge collection scan (sec. 5.3.1.3) another two points in the (U_{PT}, U_{DRI}) domain are obtained for the W10 F07 and W09 B07 PMATs, and three points for the PMAT W09 F07. The two points common to all three PMATs are the so-called 'IG optimized point' and 'OF optimized point'. The former is located where the charge collection scans showed the best result for a small amount of injected charge, i.e. charge that only fills a fraction of the IG, and the latter for where they showed the best result for a big amount of injected charge, i.e., charge that completely fills the IG and also a part of the OF. As the additional measurements were performed on the PMAT W09 F07 an additional 'overall optimized point' exists for this device. At this point the charge collection is optimized for the cross-section of both scenarios – one with small amount

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of injected charge and the other with big amount of injected charge. The U_{PT} and U_{DRI} pairs for the described points of three PMATs are collected in Tab. 5.16.

For measurements performed in all described points, the difference between U_C^{ON} and U_C^{OFF} was selected in accordance with the criteria presented in sec. 5.3.1.2. The difference was calculated for the most negative applied U_{CG} . Consequently, the collected charges were completely removed also when simulating the radiation damage with more positive U_{CG} . For the W09 F07 PMAT, this resulted in the 17.75 V difference between U_C^{ON} and U_C^{OFF} , for the W10 F07 PMAT in 18.5 V and for the W09 B07 PMAT in 19.75 V.

The U_G^{ON} voltage was evaluated at the most negative applied U_{CG} , and re-evaluated at any change in the U_C^{OFF} , U_{PT} or U_{DRI} . Evaluation was done so that the $I_{OFFS} \sim 100 \mu A$. During the simulation of radiation damage, i.e., changes in U_{CG} , the U_G^{ON} remained constant as will be the case during the actual usage.

The remaining voltages were kept constant during the measurements, and were set as following: the difference between U_S and U_D was set to $-5 V$, the U_C^{OFF} was set to $5 V$, and U_C^{ALL} and U_{CE} were set to $10 V$.

Exact procedure for the measurements performed in this section is as following. After the voltages for desired the operation point were applied, the ^{55}Fe source was shortly

Table 5.15: Collection of the U_{CG} and U_C^{OFF} voltages for three different operation points. Values for the three PMATs were obtained from the operation window scans described in sec. 5.3.1.1.

	W09 F07		W10 F07		W09 B07	
	U_{CG}	U_C^{OFF}	U_{CG}	U_C^{OFF}	U_{CG}	U_C^{OFF}
	[V]	[V]	[V]	[V]	[V]	[V]
spectroscopy point	-1.25	-0.50	-1.25	-1.00	-1.00	0.00
radiation point	-1.25	1.80	-1.25	1.60	-1.00	2.00
damaged point	1.25	1.80	1.60	1.60	1.20	2.00

Table 5.16: Collection of the U_{PT} and U_{DRI} voltages for three different operation points. Values for the three PMATs were obtained from the charge collection scans described in sec. 5.3.1.3.

	W09 F07		W10 F07		W09 B07	
	U_{PT}	U_{DRI}	U_{PT}	U_{DRI}	U_{PT}	U_{DRI}
	[V]	[V]	[V]	[V]	[V]	[V]
IG optimized point	-27.50	-10.00	-6.25	-8.75	-19.75	-10.00
OF optimized point	-23.00	-5.00	-9.25	-7.50	-23.75	-3.50
overall optimized point	-24.50	-7.25				

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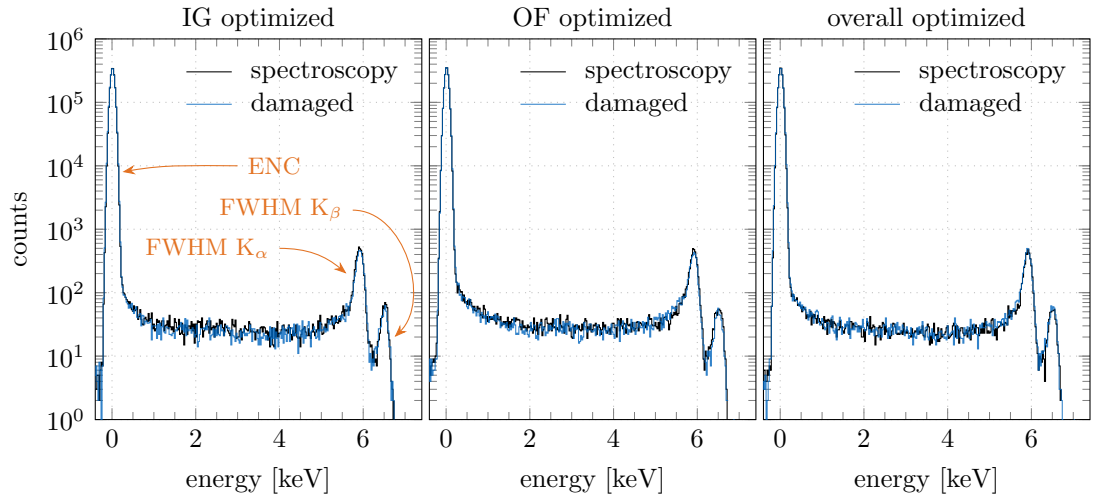
placed over the sensor and around $3 \cdot 10^5$ events outside the system's noise peak were recorded in order to obtain the energy spectrum. This spectrum was then used for the energy calibration and conversion of the recorded ADC's ADU values to the number of e^- . For the next two steps a pulsed linear high-speed LED was used in order to measure the complete response function. In one of them, the linear part was investigated with 201 light injections and subsequent digitizations, and in the other the complete response was investigated with 801 light injections.¹⁸ For the last step, the same measurement was repeated without the LED pulses in order to remove the contribution of leakage current.

A subset of six results from measurements performed over the union of all three optimization points in the (U_{PT}, U_{DRI}) domain and two points from the (U_{CG}, U_C^{OFF}) domain is presented in Fig. 5.50. From it, it can be deduced that the differences between the spectra recorded with each setting are miniscule. The same is true for the measurements inside the same point of operation in the (U_{CG}, U_C^{OFF}) domain, i.e., spectroscopy point, radiation point and damaged point. However, varying the U_{CG} can have a big impact on at least the maximum dynamic range. In order to compare different operation points a set of characterization parameters is extracted from the measurements and they are afterwards compared further. Parameters extracted from the ^{55}Fe energy spectrum are the equivalent noise charge (ENC), full width at half maximum (FWHM) energy resolution of the K_α and K_β peaks, and charge amplification factor of the IG region (g_q^{IG}). From the response function measurements a position of the kink, that denotes the middle point of transition between the IG and OF, is extracted, as well as the charge amplification factor of the e^- collected in the OF (g_q^{OF}), and the maximal dynamic range Q_{MAX} . On each PMAT those parameters were extracted for four pixels. For further analysis a weighted average and its standard deviation is used. Prior to the comparison of different PMATs a more thorough investigation was performed on the W09 F07 PMAT. In addition to the three operation points in the (U_{CG}, U_C^{OFF}) domain more points were added between the spectroscopy and radiation point, as well as between the radiation and damaged point. The results of the former are presented in Figs. 5.51 and 5.52, and the latter in Figs. 5.53 and 5.54.

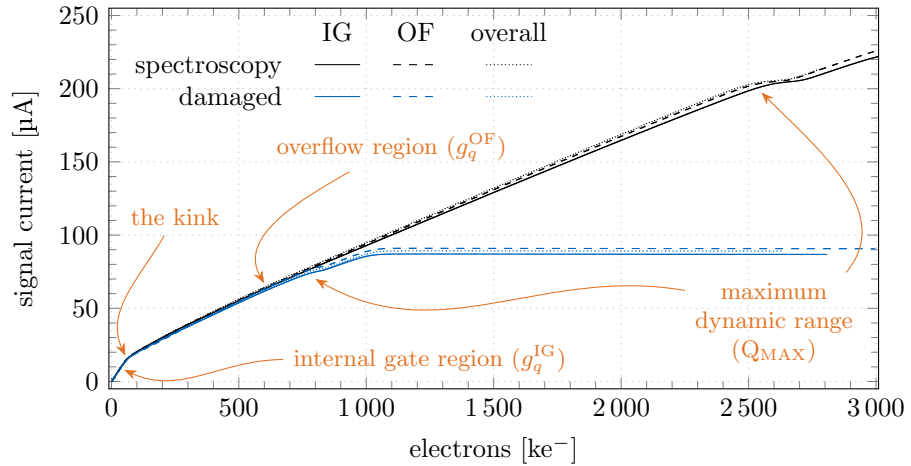
In Fig. 5.51 the extracted leakage current (upper left), ENC (upper right), and FWHM energy resolution of ^{55}Fe K_α (lower left) and K_β (lower right) peaks in dependence of the applied U_C^{OFF} are shown. The U_{CG} is set to -1.25 V , which is the most negative voltage allowed for the W09 F07 PMAT. The full orange line on all plots represents the spectroscopy optimization point, and the dashed orange line the radiation point.

The leakage current shows the lowering tendency with increasing of the U_C^{OFF} . This is explained in sec. 3.1.2. Lowering of the U_C^{OFF} increases the probability of e^- back-emission and vice versa. The biggest difference between the three curves shown on the leakage current plot is in the applied U_{DRI} . The higher the U_{DRI} the higher the noise. The leakage current varies between $0.25\text{ e}^-/\mu\text{s}/\text{pixel}$ and $0.5\text{ e}^-/\mu\text{s}/\text{pixel}$ and contributes a maximum average value of 2.5 e^- to the noise at the planned 80 kHz operation mode.

¹⁸The duration of each LED pulse was different for the two measurement steps.



(a)



(b)

Figure 5.50: An example of six measurements performed on the W09 F07 PMAT at different optimized operation points; ^{55}Fe spectra used for calibration (a), and calibrated response functions (b). The results from a single pixel out of the four measured are shown. Calibration and measurement errors are not shown as they are too small for the presented scales. In case of the response function optimized for the spectroscopy and OF condition, the x -axis standard deviation is around 9ke^- at 2Me^- of collected charge, and $0.6\mu\text{A}$ at $155\mu\text{A}$ for the y axis. They are, however, included in the analysis. Denoted with the orange colour are the parameters extracted from each measurement. They are further used in the comparison between different operation points. Those parameters are the charge amplification factors g_q^{IG} and g_q^{OF} , the position of the kink and the maximum dynamic range Q_{MAX} .

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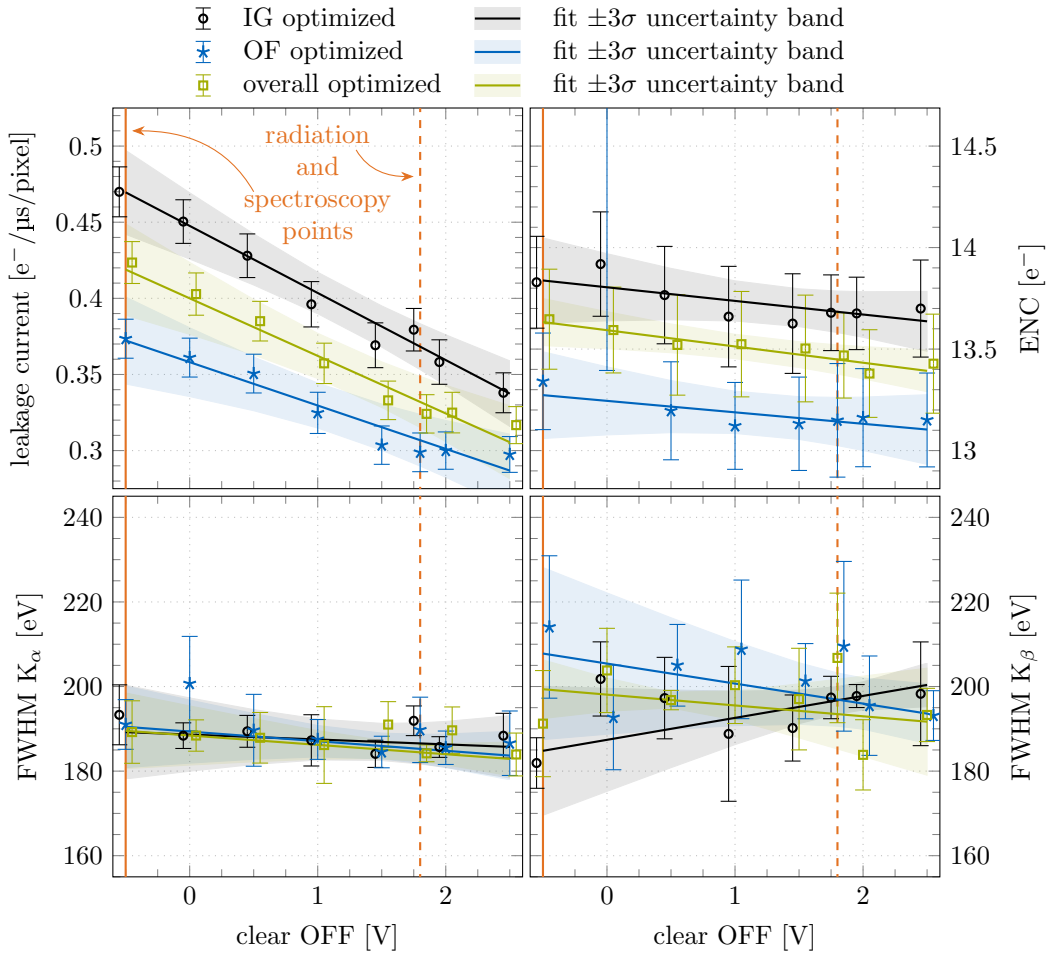


Figure 5.51: First set of extracted parameters from the W09 F07 PMAT for three optimized points of operation in the (U_{PT}, U_{DRI}) domain at multiple U_C^{OFF} values with the U_{CG} fixed to -1.25 V. The spectroscopy and radiation points are denoted with full and dashed orange lines respectively. For better visibility the 'IG optimized' markers are offset for -50 mV and the 'overall optimized' markers for 50 mV with regards to the 'OF optimized' markers. Each marker denotes the weighted mean value extracted from measurements performed on four pixels. The error bars are the ± 1 standard deviation of that distribution. Both are calculated according to ref. [33]. Additionally, a linear regression line with $\pm 3\sigma$ uncertainty band is plotted for each set of markers, with standard deviations to the power of -2 being used as weights.

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This value is much lower than the digitization noise caused by the DCD [84, 85], and can therefore be neglected.

The lowering of the leakage current is responsible for lowering of the ENC as well. However, as the leakage current is not the main source of the noise in the SPIX system the lowering is not as pronounced. The main sources of noise with those measurements are the common mode and thermal noise, both described in sec. 3.2.2. As the three curves are again well separated and the biggest change between them is in U_{DRI} , the drift has to be the reason for the offset.

The FWHM of both the K_α and K_β peaks of the ^{55}Fe radioactive source are very little influenced with the variation of the $U_{\text{C}}^{\text{OFF}}$. The former is in all cases evenly spread around (187 ± 3) eV and the latter around (196 ± 5) eV. Bigger error bars in case of the K_β peak are due to the smaller statistics and consequently poorer fits.

In Fig. 5.52 the extracted charge amplification factors of the IG (upper left) and OF (upper right) regions, the kink (lower left), and the Q_{MAX} (lower right) in dependence of the $U_{\text{C}}^{\text{OFF}}$ are shown. Everything else is the same as in Fig. 5.51.

The values of both charge amplification factors from different measurement sets correspond very well between themselves – all within measurement errors. Also they show little to no dependence on the $U_{\text{C}}^{\text{OFF}}$. The weighted mean value of the former is (284 ± 3) pA/e $^-$ and (84 ± 2) pA/e $^-$ of the latter.

The three sets of kink positions overlap more or less everywhere. The interesting part here is that the position of the kink moves to higher numbers of e $^-$ – overall the change between the lowest and highest $U_{\text{C}}^{\text{OFF}}$ setting is (3.6 ± 1.7) ke $^-$. Despite the effect is minimal, and will have no influence over the final performance, it is important to understand it. The potentials of both IG and OF regions are defined by the implantation profiles and the potentials applied to different contacts in their vicinity. The former is coupled the strongest to the potential of the channel and the latter to the source. The channel forms close to the surface while the source implantation extends several hundred nm into the device. This causes a larger in-coupling of the potentials of adjacent contacts into the IG potential than to the OF. A change of the $U_{\text{C}}^{\text{OFF}}$ hence has a stronger effect on the IG potential than on the potential of the OF, which leads to the observed behaviour.

In weighted average over all measurement sets, the Q_{MAX} changes from (2400 ± 41) ke $^-$ to (2224 ± 79) ke $^-$. This yields the overall decrease of capacity for (174 ± 89) ke $^-$, which is tiny. The reason for the decrease is that the potential of the OF region is reduced with the amount of e $^-$ stored in it. Therefore, the higher the amount of e $^-$ in it the lower the potential and the easier it is for the e $^-$ to overcome the boundaries of charge storage regions. The weakest barrier is first to the neighbouring pixel over the common source, and afterwards to the clear region over the barrier set by the U_{CG} . As all the values here are well beyond the EDET DH80k planned storage capacity of 800 ke $^-$ it will not cause any problems.

Overall, none of the measured parameters worsen over the range of measured $U_{\text{C}}^{\text{OFF}}$ values. Consequently, for the scope of the EDET DH80k the choice of the $U_{\text{C}}^{\text{OFF}}$ will not influence the overall performance of the sensor. Also in the $(U_{\text{PT}}, U_{\text{DRI}})$ domain the sensor is more or less invariant to the points selected in sec. 5.3.1.3. The biggest difference comes in the way of leakage current which is mostly influenced by the negative

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drift voltages. However, all levels of the leakage current are essentially negligible in the scope of EDET DH80k.

In Fig. 5.53 the extracted leakage current (upper left), ENC (upper right), and FWHM energy resolution of ^{55}Fe K_α (lower left) and K_β (lower right) peaks in dependence of the applied U_{CG} are shown. The $U_{\text{C}}^{\text{OFF}}$ is set to 1.8 V, which is the point where the biggest operation window on the U_{CG} for W09 F07 PMAT is located. The dashed orange line on all plots represents the radiation optimization point, and the dotted orange line the damaged point.

The effect on the leakage current and ENC is the same but opposite as in the previous case. Both of them are at their lowest values when the U_{CG} is the most negative and increase with increasing U_{CG} . They increase because the barrier separating the charge storage regions and clear regions weakens and the probability for back-emission of e^- from clear region increases.

In the FWHM energy resolution of ^{55}Fe K_α and K_β peaks there is also no statistical difference between any of optimization points from the $(U_{\text{PT}}, U_{\text{DRI}})$ domain, as well as no difference with varying of the U_{CG} . The former is spread around (190 ± 5) eV and the latter around (202 ± 7) eV. This points to the fact that there should be no difference in energy resolution between the pixels that will obtain more radiation and the ones that will obtain less.

Fig. 5.54 shows the extracted charge amplification factors of the IG (upper left) and OF (upper right) regions, the kink (lower left), and the Q_{MAX} (lower right), all as a function of the U_{CG} . Everything else is the same as in Fig. 5.53.

Varying of the U_{CG} also has no influence over the charge amplification factors, and neither does the varying of the optimization points in the $(U_{\text{PT}}, U_{\text{DRI}})$ domain. The former is evenly spread around (287 ± 2) pA/ e^- and the latter around (86 ± 2) pA/ e^- . Both values are within one standard deviation margin of values that were measured in the previous parametrization where the $U_{\text{C}}^{\text{OFF}}$ was varied and U_{CG} was fixed.

The interesting things happen with the last two parameters. In all cases, the position of the kink moves to lower values with increasing U_{CG} . The change is (-3.8 ± 1.8) ke $^-$ at a 2.5 V difference on the U_{CG} . This is in contradiction with the previous results where the $U_{\text{C}}^{\text{OFF}}$ was varied and the U_{CG} fixed. If the $U_{\text{C}}^{\text{OFF}}$ capacitively couples to the potential of the IG, the same should be true for the U_{CG} . Consequently, by making the U_{CG} more positive, the kink position should move to higher values. As it does not there has to be another effect that counteracts it. The counteracting part could be the h^+ current between source and drift regions (briefly described in sec. 5.3.1.3). Essentially, there is a transistor like characteristics with the CG acting as the gate that has source p-type implantations on one side and deep p and drift p-type implantations on the other side. Normally, the threshold voltage of such transistor is set very negative with the existence of the MDDN implantation that forms the charge storage regions. However, due to the double pixel design of the EDET DH80k DePFETs, this implantation is omitted in the central part of the adjacent pixels to separate their charge storage regions. Consequently, the unwanted current path through this part can be made at more positive U_{CG} . Now if the unwanted path for h^+ exists, more and more h^+ make their way to the deep p region below clear. That way the region becomes more positive and the result is similar

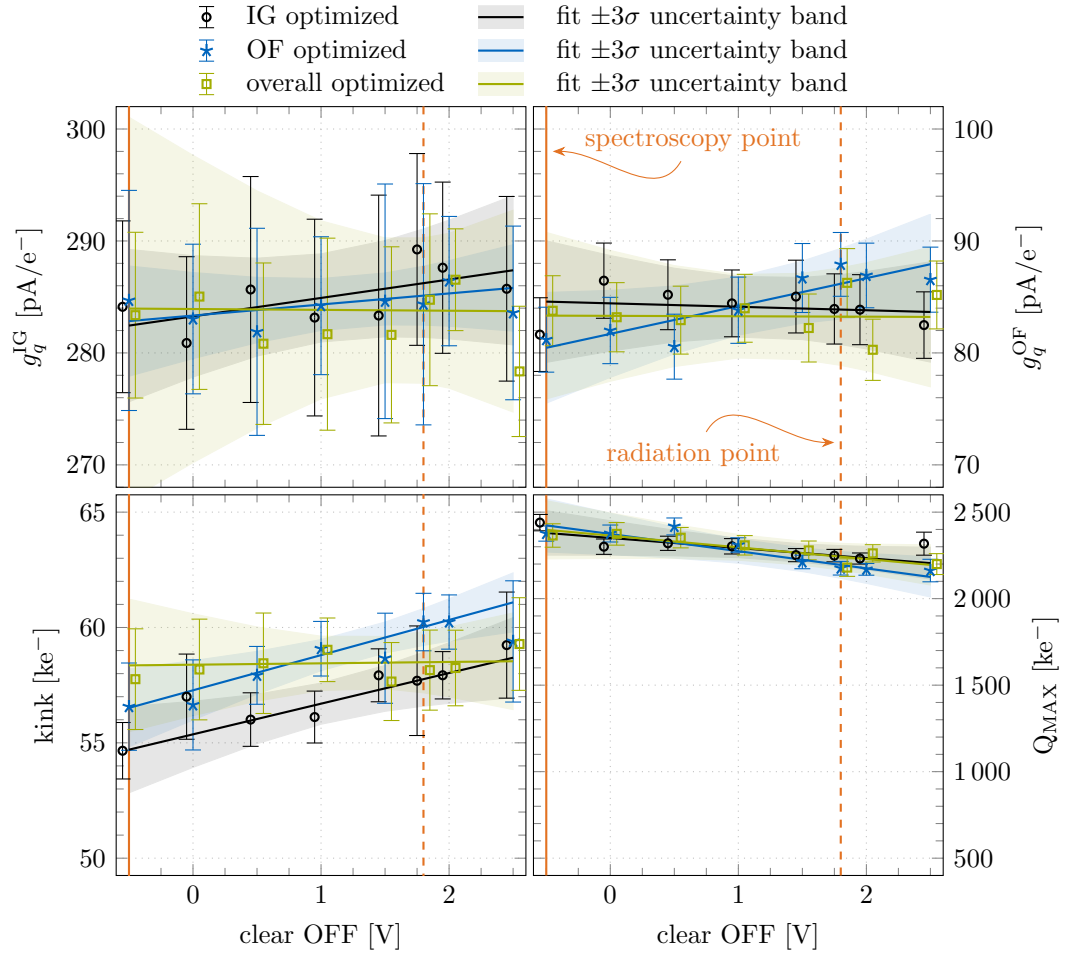


Figure 5.52: Second set of extracted parameters from the W09 F07 PMAT for three optimized points of operation in the $(U_{\text{PT}}, U_{\text{DRI}})$ domain at multiple $U_{\text{C}}^{\text{OFF}}$ values with the U_{CG} fixed to -1.25 V. The data has the same structure as described under the previous figure.

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to making the U_C^{OFF} more positive. By making the U_{CG} more positive the unwanted current path is reduced. This leads to the deep p region becoming more negative, and the effect is the same as by making the U_C^{OFF} more negative. In order to confirm or deny this hypothesis, a detailed simulation of the design would be required. However, just like with previous parametrization results, the change of the kink position is minimal and should have no influence over the final performance.

By far the biggest change of all parameters, from both parametrization results, comes in a way of Q_{MAX} changes. Through the variation of the U_{CG} the Q_{MAX} changes from $(2.21 \pm 0.04) \text{ Me}^-$ when operated at the radiation point, to $(720 \pm 10) \text{ ke}^-$ at the damaged point. This means that after an extensive inhomogeneous irradiation some

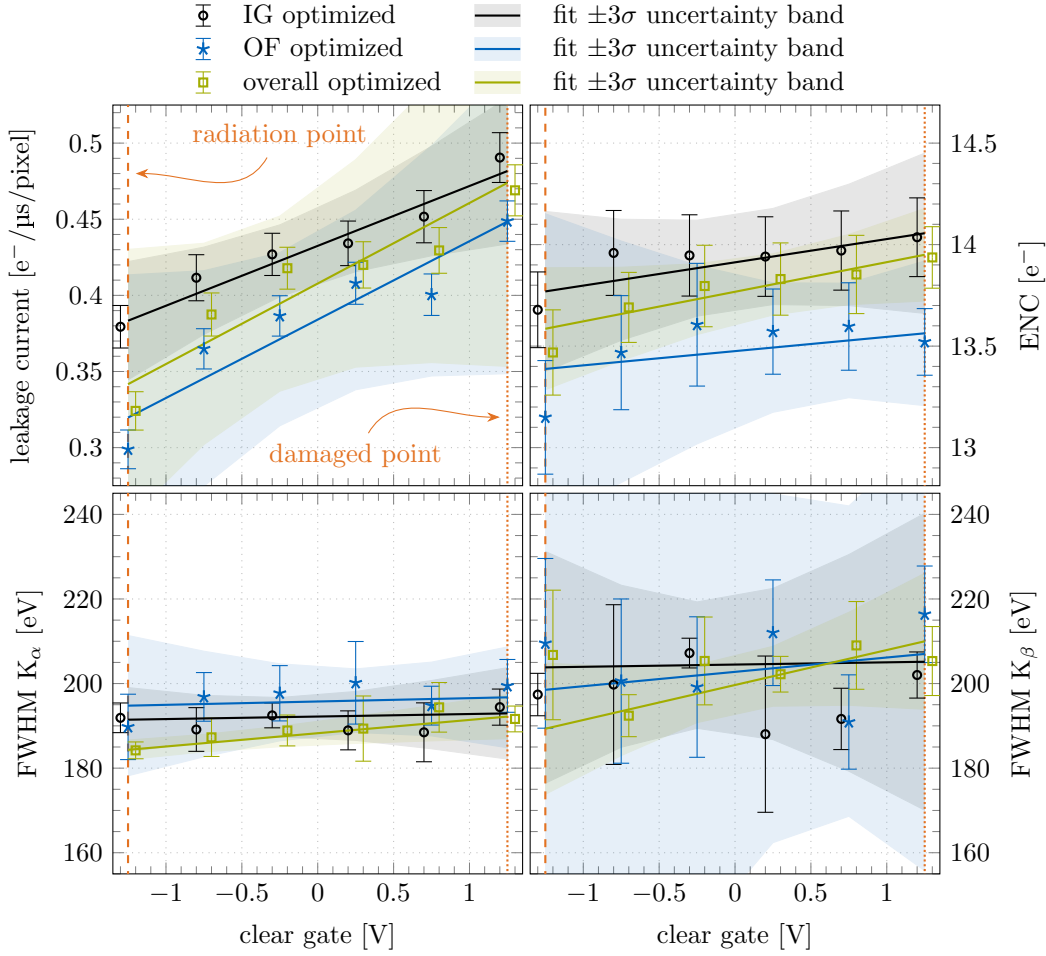


Figure 5.53: First set of extracted parameters from the W09 F07 PMAT for three optimized points of operation in the $(U_{\text{PT}}, U_{\text{DRI}})$ domain at multiple U_{CG} values with the U_C^{OFF} fixed to 1.8 V. The radiation and damaged points are denoted with dashed and dotted orange lines respectively. The remaining data has the same structure as described in Fig. 5.51.

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pixels would not satisfy the 800 ke^- dynamic range condition of the EDET DH80k project shortly before they would go completely out of the operation window due to the back-emission of e^- .

The parametrization results presented so far confirm that the biggest, if not the only, problem of DePFETs in the EDET DH80k project is the damage from inhomogeneous irradiation. The damage causes a positive charge build-up in the SiO_2 at the SiO_2/Si interface below the CG. This in turn diminishes the potential barrier between the charge storage regions and clear implantation, which effectively leads to the lowering of the Q_{MAX} .

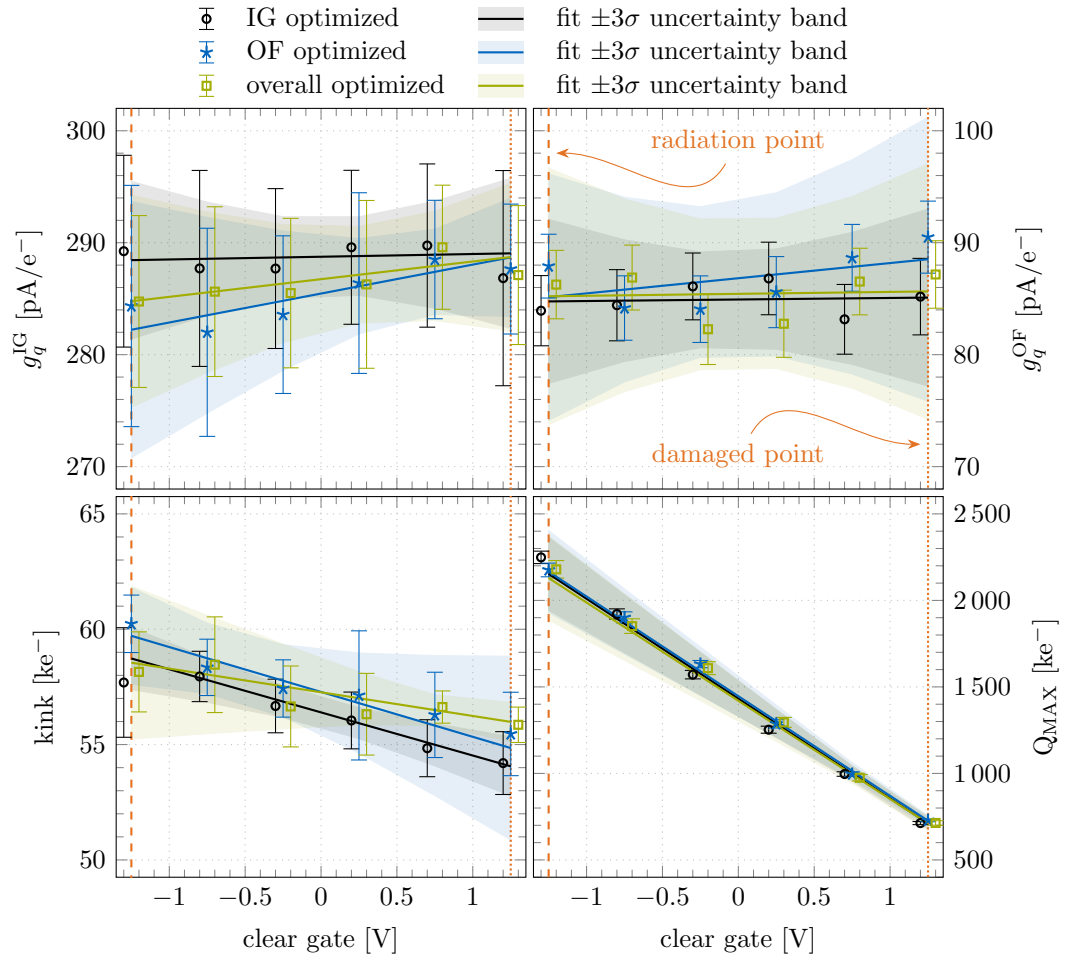


Figure 5.54: Second set of extracted parameters from the W09 F07 PMAT for three optimized points of operation in the $(U_{\text{PT}}, U_{\text{DRI}})$ domain at multiple U_{CG} values with the $U_{\text{C}}^{\text{OFF}}$ fixed to 1.8 V. The data has the same structure as described under the previous figure.

Comparison of the three prototyping matrices The previously described parameter sets obtained from measurements performed in the optimization points (Tabs. 5.15 and 5.16) were used for the comparison of W09 F07, W10 F07 and W09 B07 PMATs. They can be found in Figs. 5.55 and 5.56.

In regards to the leakage current (first row in Fig. 5.55), all three PMATs behave similarly. They exhibit the levels of leakage currents between $0.3 \text{ e}^-/\mu\text{s}/\text{px}$ and $0.6 \text{ e}^-/\mu\text{s}/\text{px}$. These levels will in no case influence the performance of the final EDET DH80k camera system as the noise originating from this contribution is much smaller than the one from fast digitization needed to achieve the 80 kHz [84, 85]. Interesting thing to note here is the homogeneity of the response of different pixels. This can be inferred from the size of the error bars. The best PMAT in this respect is the $30 \mu\text{m}$ thick W10 F07, followed by the $50 \mu\text{m}$ W09 F07 PMAT. Both of them feature the main design C that is implemented on the main devices for the EDET DH80k project. The worst behaviour is again obtained from the $50 \mu\text{m}$ W09 B07 PMAT that features the experimental design type D. This is especially clear when simulating the conditions of radiation damage in the damaged point of operation in the $(U_{\text{PT}}, U_{\text{DRI}})$ domain. In this case, two pixels are seeing a much higher level of the leakage current which leads to the enormous error bars. The reason for this could be in the asymmetric boundary conditions discussed in sec. 5.3.1.3.

The ENC behaviour (second row in Fig. 5.55) is very similar in both PMATs featuring the main design C – the F07 PMATs from both the W09 and W10 wafers. With the W09 B07 PMAT an additional noise hindering the performance coupled in especially when operating in the IG optimized point from the $(U_{\text{PT}}, U_{\text{DRI}})$ domain. In this point the drift is biased at a very negative voltage of -10 V . The reason for the problems most likely lays in the directly connected deep p implantation below clear and the drift regions.

The best FWHM energy resolution of both the ^{55}Fe K_α and K_β (third and fourth row in Fig. 5.55) between the three PMATs was achieved with the $50 \mu\text{m}$ thick PMAT of the standard design C, i.e., W09 F07 PMAT. The weighted mean and standard deviation were calculated for shown measurements resulted as it was previously shown that the biasing conditions have little influence over the results. The calculation yielded an energy resolution of $(189 \pm 5) \text{ eV}$ at ^{55}Fe K_α peak and $(198 \pm 11) \text{ eV}$ at ^{55}Fe K_β peak. The thinner PMAT W10 F07 performed slightly worse. The reason behind this is in the location of X-ray absorption events. If they happen on the edge of the depleted volume, i.e., very close to the backside p^+ -type doped entrance window, or the drift or source regions, part of the generated e^- cloud can be lost. This leads to the inferior performance and is described in more detail in refs. [148, 170]. The attenuation length from the Beer-Lamberts law (eq. 1.17) for the 5.9 keV X-rays in Si is about $29.1 \mu\text{m}$ [34]. Consequently, with $30 \mu\text{m}$ thick PMAT a bigger fraction of absorption events happens on the edges of the device. With the W10 F07 PMAT the FWHM energy resolutions are $(203 \pm 5) \text{ eV}$ and $(217 \pm 6) \text{ eV}$ for ^{55}Fe K_α and K_β respectively. Despite the thicker body, the W09 B07 PMAT behaved even worse than the previously described PMAT. The FWHM energy resolutions here are $(204 \pm 7) \text{ eV}$ and $(226 \pm 12) \text{ eV}$ for ^{55}Fe K_α and K_β respectively. The parameter points with enormous error bars have very little

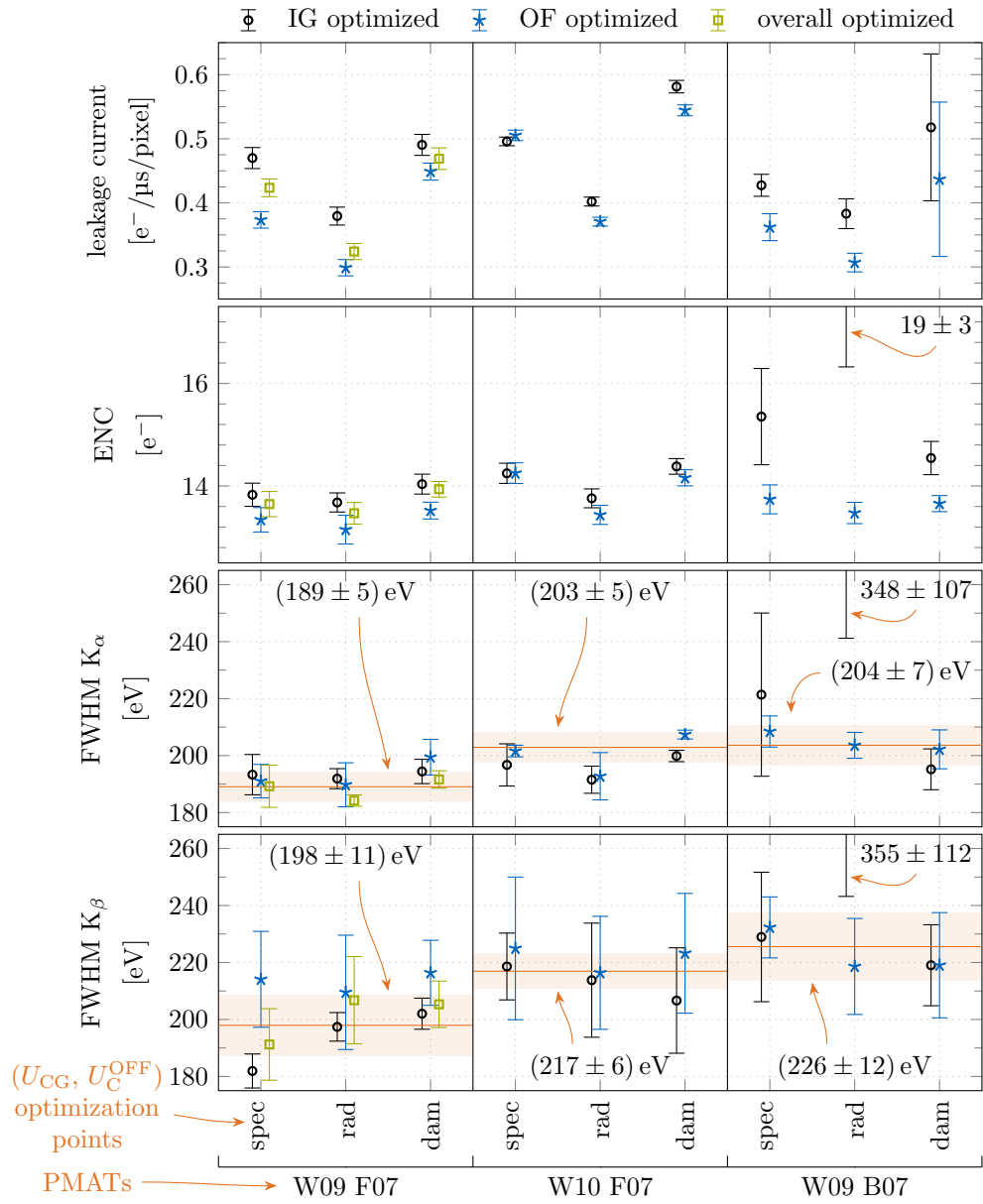


Figure 5.55: Comparison of the first set of extracted parameters for the W09 F07, W10 F07 and W09 B07 PMATs in all selected optimization points from both (U_{PT}, U_{DRI}) and (U_{CG}, U_C^{OFF}) domains. The naming convention of the (U_{CG}, U_C^{OFF}) domain is shortened so that the 'spec' represents the spectroscopy point, 'rad' the radiation point and 'dam' the damaged point of operation. The IG optimized and overall optimized datasets from the (U_{PT}, U_{DRI}) domain are respectively offset to the left and right side of the OF optimized dataset for better visibility. Orange line and its corresponding band (—) represent the weighted mean ± 1 standard deviation of all datasets for a given PMAT. This is added only where it was previously shown that there is no measurable difference between different operation points.

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influence over the weighted mean as they are evaluated with weights which are standard deviations of the points to the power of -2 . Consequently, the result is mostly based on the measurements from the OF optimized condition.

The charge amplification factors g_q^{IG} and g_q^{OF} (first and second row in Fig. 5.56) are important for the response function. All three PMATs have the g_q^{IG} in vicinity of the planned 300 pA/e^- . The biggest difference is in the homogeneity between the measurements. The W09 B07 PMAT exhibits a much larger spread than the other two PMATs. However, in all cases the measured parameter is stable throughout all different conditions. The same is true for the g_q^{OF} , where the value around 80 pA/e^- is achieved across all conditions in all three PMATs.

The previously observed and described variability of the kink position in W09 F07 PMAT is observed in the remaining two PMATs as well (third row in Fig. 5.56). The conclusion is the same. As the changes in the kink position are relatively small, they will not be observed when digitizing with the harsh granularity of the DCD. Additionally, the calibration of the full response function in the final camera will not be performed with the granularity of 801 measurements but with three points in the IG region and 5 points in the OF [137]. Afterwards the response will be interpolated with two linear functions. This will result in the interpolation errors for the transition region that will be much bigger than the offsets due to different potentials which are about 3 ke^- .

The last parameter compared over the three PMATs is the maximum dynamic range Q_{MAX} (fourth row in Fig. 5.56). The best performance is featured on the W10 F07 PMAT. On it the maximum charge handling capacity does not change when changing the operation point from the spectroscopy point to the radiation point. However, as the EDET DH80k devices need to be operated in the point where the operational window for the potential shifts due to the inhomogeneous radiation damage is bigger, this comparison is not of the utmost importance. The most important comparison is in charge handling capacity between the radiation and damaged points. Here all three PMATs behave similarly. Just before the onset of e^- back-emission the charge handling capacity of pixels drops to the level of 750 ke^- . The difference is that for the W10 F07 this happens after simulation of 2.85 V of the U_{CG} shift, whereas for the W09 F07 and W09 B07 the same happens after the respective shifts of 2.5 V and 2.2 V . Consequently, the thinnest device behaves the best and the one with the experimental design the worst.

In conclusion, the W09 F07 and W10 F07 PMATs behave very similarly and are both very suitable for the EDET project. When comparing themselves between each other they are both easy to operate, they fulfil the minimum charge handling capacity when simulating the radiation damage and the remaining parameters of the response function remain constant at different operation points. However, the thinner of the two PMATs exhibits a bigger operation window on the U_{CG} parameter. Additionally, it should also receive less radiation damage in the transmission electron microscope environment [82]. Therefore, if the thickness of $30 \mu\text{m}$ will not cause any structural problems with final EDET DH80k devices they should be the go-to option for this project.

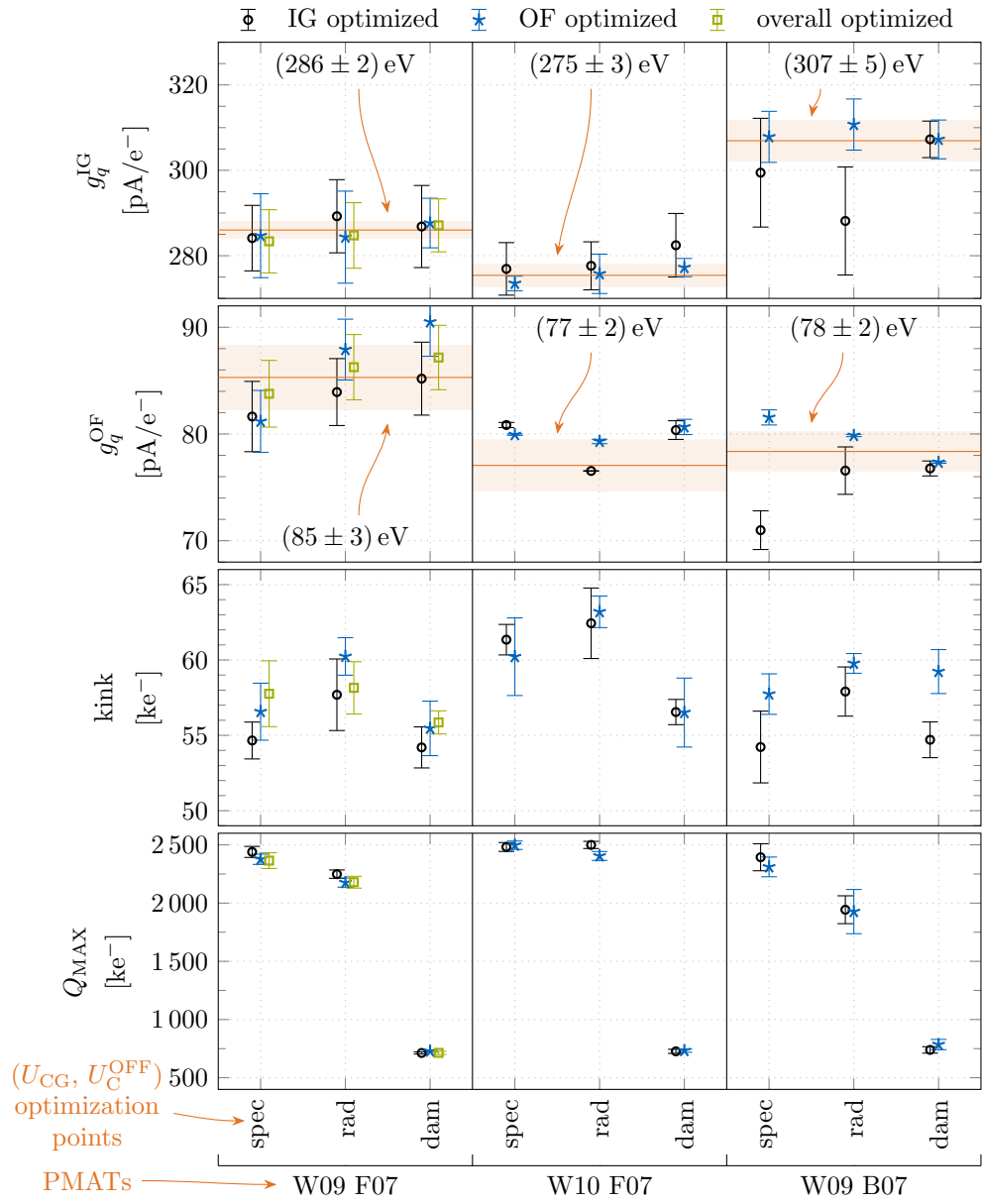


Figure 5.56: Comparison of the second set of extracted parameters for the W09 F07, W10 F07 and W09 B07 PMATs. The data has the exact same structure as explained in the caption of Fig. 5.55.

5.3 Characterization of single pixels on prototyping matrices

Despite the parametrization results of the 50 μm thick PMAT with the experimental design D, i.e., W09 B07, show similar behaviour, the design is actually inferior in all performed measurements. It features a smaller operation window, needs higher U_C^{ON} for the complete removal of collected e^- , and loses charge easier. However, the idea behind the design is valid. The CG bridges can cause potential pockets for e^- , especially after the device has sustained some radiation damage. Omitting them could therefore bridge this problem as the e^- would always have an easy way from the drift region to the charge storage regions below the clear. But before this can happen extensive simulations of the design are needed in order to investigate and pinpoint the root of the problems. As already discussed, one possible cause of the problems and a good start of the investigation could be the deep p implantation.

6 Radiation studies

Radiation studies were performed to predict how the high intensity e^- beam of a transmission electron microscope (tEM) will influence the behaviour of EDET DH80k devices in the final experiment. Three single pixel devices (SPDs), described in sec. 4.3, were irradiated with different amounts of 55 keV e^- :

- W09 TL 80k1 from the 50 μm thick silicon-on-insulator (SOI) wafer, and
- W11 TR 80k1 and W12 TL 80k1 from the 450 μm thick standard wafers.

The irradiation campaign was performed with the Egun300 system that is located at the Deutsches Elektronen-Synchrotron (DESY) research centre in Hamburg, and is a part of the MPSD institute. The campaign would not have been possible without the help of many MPSD colleagues that are a part of the EDET collaboration, and also some that are not. A modified version of the customPCMS, presented in sec. 5.1.1, was used for the control of DePFET pixels during their irradiation and measurements of their characteristics afterwards. Specifics of both systems will be presented in the following sec. 6.1.

The customPCMS is not designed to measure the current or the shape of the e^- beam impinging on the connected SPD. Therefore, this was done by the means of the faraday cup (FC) and CCD camera. Both instruments are a part of the the Egun300 system. The e^- beam had to be characterized in order to position the array into, or close to the centre of the e^- beam, and to determine the amount of e^- hitting the array. The exact procedure and extraction of the parameters will be presented in sec. 6.2. Those parameters were then combined with the Geant4 [174] simulations of the EDET DH80k DePFET pixel design in order to determine the total ionizing dose inflicted to the SiO_2 . The simulations results, performed and provided by I. Dourki [175], are presented in sec. 6.3.

The SPDs were irradiated in steps. Before each step and additionally after the last one

- the e^- beam current was measured, and
- the transfer characteristics of both the gate and clear gate (CG) structures were measured in the same way as described in sec. 5.2.1.

That way the changes due to the radiation damage were well tracked. During the irradiation the DePFETs were statically biased so that charge storage regions were always empty, and in addition so that there was no current between the source and drain regions. This meant that

- the gate structures were kept fixed at a voltage higher than the most positive threshold voltage (U_T) of the 24 pixels on the tested SPD, and

6 Radiation studies

- that the CG and clear structures were respectively kept at relatively positive voltages of 5 V and 15 V, in order to completely remove all e^- generated by the incident high energy e^- beam.

Conditions like this were chosen in order for the DePFET transistors to be as close as possible to the conditions that will be in effect in the final experiment. However, due to three groups of pixels implemented on the SPDs that have different gate lengths and consequently different U_T voltages, the exact OFF state conditions varied across the irradiated SPD. In general, 1 V was selected as a starting condition for the U_G^{OFF} and was afterwards reduced in order to compensate for the threshold voltage shifts. The same compensation was also performed for the CG structure. Fig. 6.1 is showing an example of such stepwise irradiation through the measured transfer curves where the gate voltage was swept and all other voltages were kept fixed. On it the measurements from a single pixel of the W09 TL 80k1 SPD are shown. The right most curve, labelled as 0 min, is the gate transfer curve before any irradiation, and the left most curve is the gate transfer curve after the cumulative irradiation period of 295 min. In this time radiation damage caused a 2.5 V shift of the transfer curve (sec 3.3). This means that the SiO_2 accumulated so much positive charge that a 2.5 V more negative gate voltage was needed to switch the transistor from OFF to ON state. In order to obtain the figure of merit (FOM), from which the shifts due to the radiation damage were calculated, the threshold voltage (U_T) and the parasitic threshold voltage ($U_{T, \text{CG}}$) were extracted from the transfer curves before each irradiation step, and additionally after the last one. They were calculated by the means of linear extrapolation method in the saturation operation region (ESR) method (sec. 5.2.1.1) from the respective 'gate sweep' and 'clear

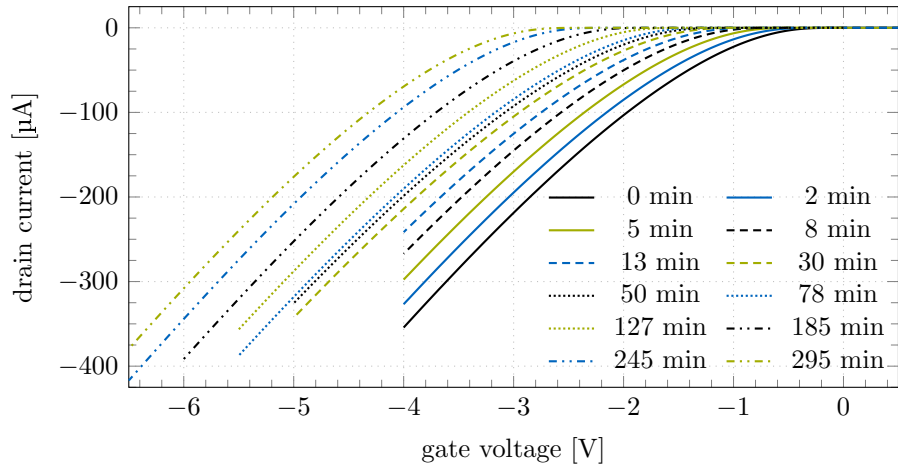


Figure 6.1: Transfer curves from the 'gate sweep' measurements performed before each and after the last irradiation step. Plotted data is from the pixel 1 on the W09 TL 80k1 SPD. It shows the build-up of positive charge in the SiO_2 as more and more negative gate voltages are needed in order to switch the DePFET transistor from OFF to ON state.

gate sweep' measurements. By subtracting all subsequent U_T and $U_{T, CG}$ voltages from the initial, unirradiated one, the U_T and $U_{T, CG}$ voltage shifts are obtained.

$$\Delta U_T \Big|_{0 \text{ min}}^{5 \text{ min}} = U_T^{5 \text{ min}} - U_T^{0 \text{ min}} = (-0.170 \pm 0.001) \text{ V}$$

$$\Delta U_T \Big|_{0 \text{ min}}^{127 \text{ min}} = U_T^{127 \text{ min}} - U_T^{0 \text{ min}} = (-1.427 \pm 0.002) \text{ V}$$

The remaining step now is to plot and examine the U_T and $U_{T, CG}$ voltage shifts with respect to the inflicted dose of radiation. This is done in sec. 6.4. From the same 'gate sweep' and 'clear gate sweep' measurements additional characterization parameters can be extracted from their subthreshold behaviour (sec. 5.2.1.3). This is done in sec. 6.5.

Electric field in the oxide In order to minimize the radiation damage the electric field in the SiO_2 should be minimized (sec. 3.3). Consequently, the voltages applied to the gate and CG structures should be around 0 V. However, as the threshold voltage of pixels with the shortest gate length on the SPD is around 0 V (sec. 5.2.1.1) this cannot be fully realized in order to have the transistor in the OFF state. Therefore, 1 V was applied to the gate structure prior to any irradiation. For the CG the applied voltage was set at 5 V in order to have the charge storage regions empty. As the thicknesses of insulator layers below both structures are very similar, it is inferred that the electric field below the CG structure will be stronger than the one below the gate structure. Consequently, it is to be expected that the CG structure, under those biasing conditions, will be more sensitive to the radiation damage.

As the goal is to always have the same field in the SiO_2 , the applied voltages to the gate and CG structures during the irradiation need to be adjusted. This was done between the measurements when the initial results of the characterization became available. However, the corrections were not applied often enough as it can be seen from Fig. 6.2. The orange curve on both plots is showing the applied voltage to the respective structure during the irradiation time. The three remaining curves show the separate mean ± 1 standard deviation values of the applied voltage with subtracted measured U_T ($U_{T, CG}$) for all three groups of pixels located on the SPD. Ideally, when the corrections of the applied voltages are performed, the three curves should be corrected to their initial values. For the gate structure the implemented corrections more or less worked¹ but should have been performed more frequent for optimal results. The three curves deviate between themselves more and more because different gate lengths have different sensitivities to the radiation damage. The same was already observed in ref. [163] and will be further discussed in sec. 6.4. In addition, due to the characteristics of the e^- beam generated by the electron gun, the e^- beam is not uniform over the complete SPD array but has a two-dimensional Gaussian shape with the standard deviation on the order of the complete length of the array. For the CG structure a mistake in programming prevented the corrections after most of the steps, and worsened the electric field conditions further.

¹With the exception of the 8th irradiation step where the gate voltage was accidentally corrected for 0.5 V in the wrong direction.

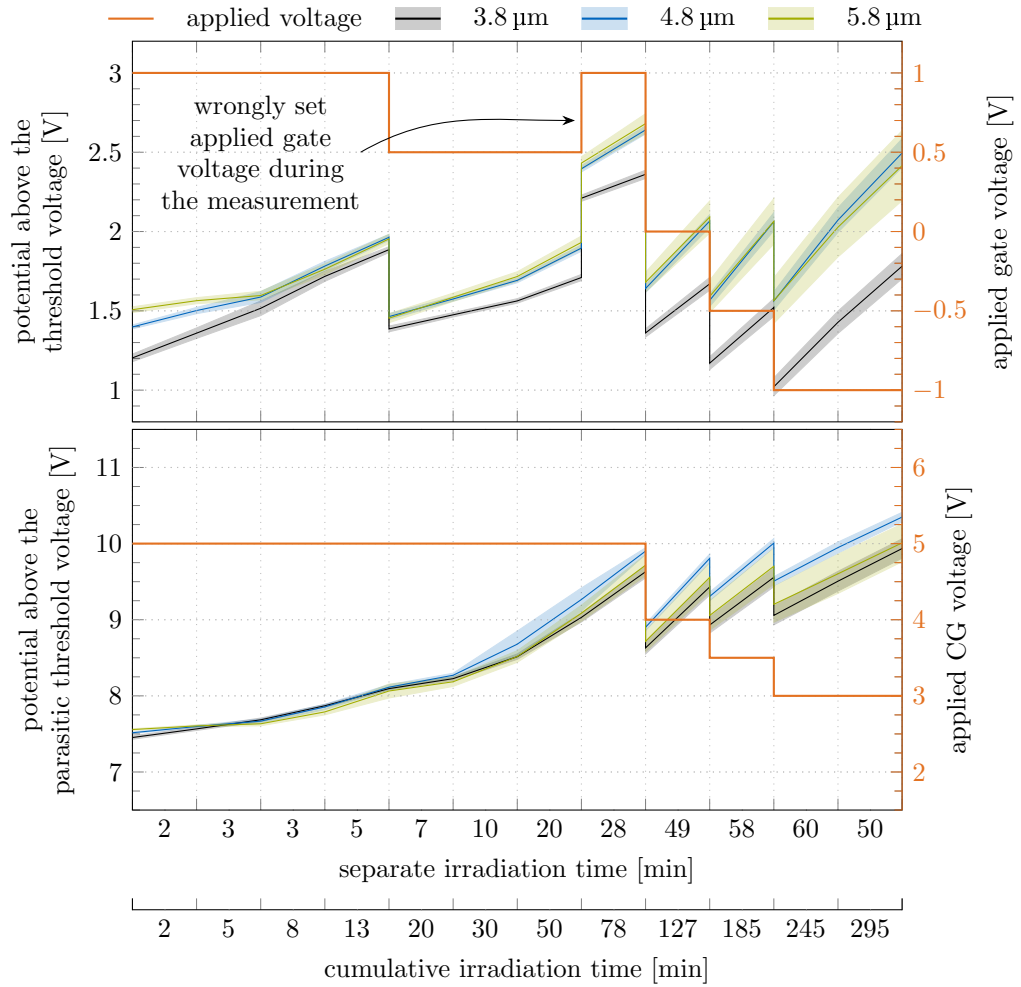


Figure 6.2: Corrections of the gate (upper) and CG (lower) voltages with respect to their threshold voltages for all irradiation steps performed on the W09 TL 80k1 SPD.

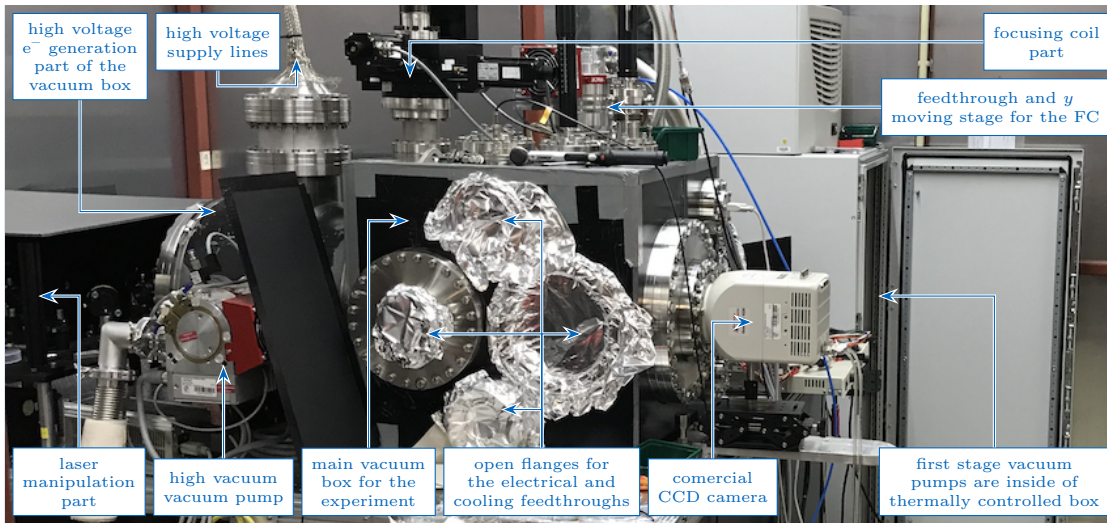
6.1 Electron gun and measurement setup

For the irradiation campaign the Egun300 system was used in combination with the modified version of the customPCMS, presented in sec. 5.1.1. Both of them together are presented in pictures and schematics on Figs. 6.3 and 6.4. The Egun300 system can be split into two parts: the e^- generation part, and the main part where the irradiations are performed. As the Egun300 system generates the high energy e^- through the means of high voltage acceleration, everything is placed in a well isolated room to which there is no access when the experiment is running.

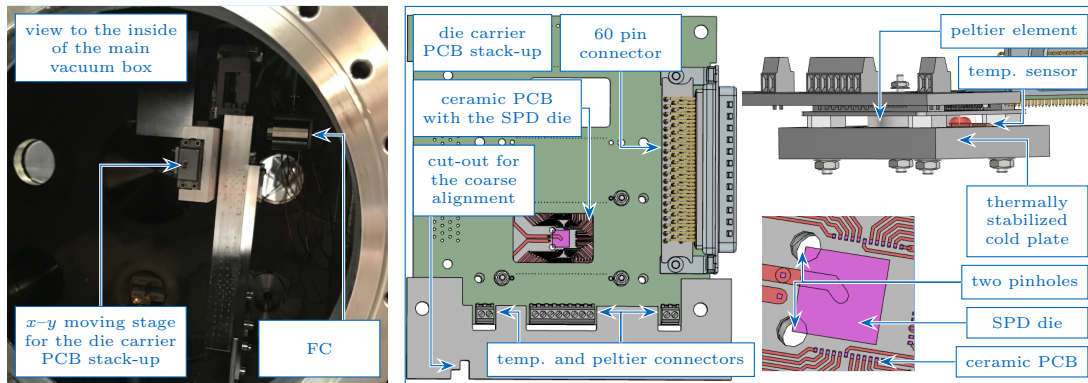
The e^- generation part comprises of a laser system, a smaller vacuum box with the photocathode for generation of e^- , a high voltage power supply module, and an e^- acceleration system. Laser system provides very short pulses of high intensity photon bursts

6.1 Electron gun and measurement setup

with a frequency of 1 kHz. Those laser pulses are then focused onto the photocathode in the vacuum box where they generate bursts of e^- with the same frequency. The e^- are afterwards accelerated with the high voltage acceleration part in the direction of the main part of the system. The limit of the acceleration depends on the breakdown voltage of this system, which in turn depends on the cleanliness of the components in both vacuum boxes and the achievable level of vacuum. During the campaign the highest, easily achievable voltage before the breakdowns occur was 55 kV, and was therefore used



(a)



(b)

(c)

Figure 6.3: Pictures of the Egun300 system that was used for irradiation campaign. The general overview of the Egun300 components as seen from the outside of the main vacuum box (a), and from the inside (b). The CAD drawings of the modifications of a customPCMS are presented on the (c).

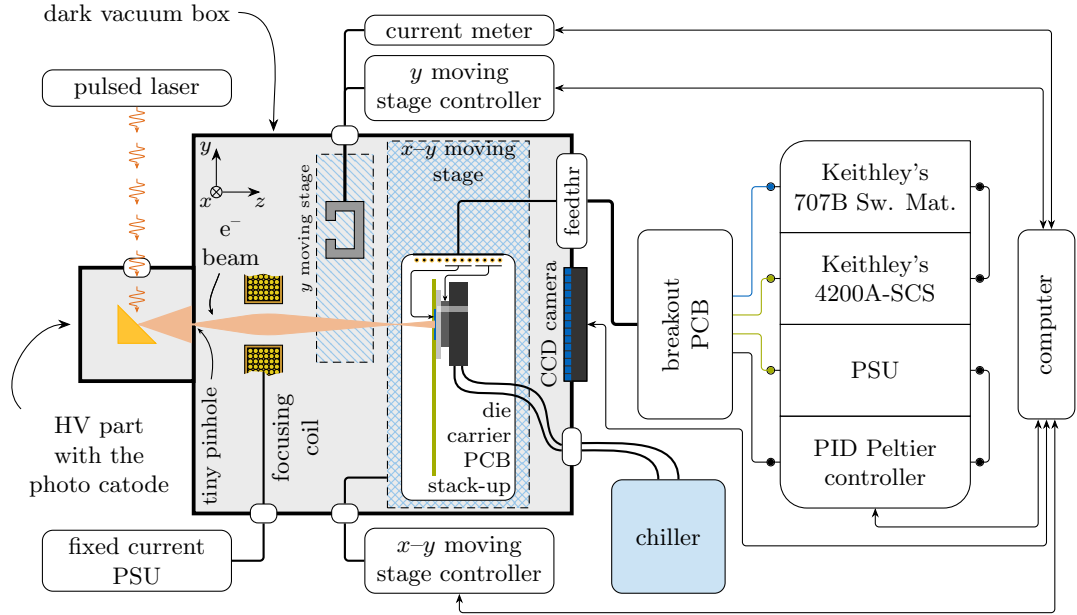


Figure 6.4: Schematic overview of the complete Egun300 system with the modified custom-PCMS, as it was used for the radiation campaign.

throughout the campaign². The e^- generation part is connected with the main part of the Egun300 system through a tiny round pinhole.

When the 55 keV e^- arrive to the main part they first pass through the focusing coil. The coil acts as a lens that adjusts the focusing point of the e^- beam in dependence of the current that is flowing through it. Consequently, it also adjusts the shape parameters of the e^- beam. Afterwards, the e^- continue their way towards the backside of the vacuum box. In their path a FC can be lowered by the means of the one-dimensional moving stage. Through it, it is possible to measure the current of the e^- beam. As the FC collects all e^- that hit it, it can only be used between irradiation procedures. The next thing that can be positioned in the path of the e^- beam is the die carrier PCB stack-up from the modified customPCMS. This one is located on the two-dimensional moving stage, so that the DePFET array can be placed directly into the e^- beam. The last thing that the e^- can hit is the CCD camera at the very back of the vacuum box. With it the exact shape of the e^- beam can be measured in the plane of the CCD camera.

The customPCMS was modified with:

- The special aluminium plate with an L shaped cut-out that is needed for the coarse alignment of the e^- beam, and also for the calculation of the widening of the e^- beam measured at different planes along the z axis.
- The ring shaped Peltier element from TE technology [176] that was placed below the ceramic PCB carrying the die. It was there for the thermal stabilization of the

²Breakdowns are an unwanted occurrence in the radiation study with the SPDs as they produce high amounts of e^- that cannot be measured with this system. Therefore, they should be avoided.

SPD die to 5 °C. The ring shape was necessary for precise positioning. In specific locations the e⁻ beam could pass through the die carrier PCB stack-up to the CCD camera behind it while being obstructed only by a tiny part of the SPD die corner.

- The water cooled aluminium cold plate that was placed below the Peltier element. It was connected with peek water pipes to the chiller on the outside of the vacuum box. The cold plate had two holes in it in order to allow the e⁻ beam pass through as well.
- Multiple PT1000 temperature sensors [177] for measurements of the temperature.
- The proportional–integral–derivative (PID) controller for the Peltier element from Meerstetter engineering [178] for an automatized temperature control.
- KERATHERM U90 silicone free U-Films [179] for improved heat conductivity on all thermal contacts.

Additionally, the die carrier PCB and the breakout PCB were not connected directly as in sec. 5.1.1. On the vacuum side a special vacuum compatible cable with peek connectors [180] was connecting the die carrier PCB to the electrical feed-through with the matching connector [180]. On the outside, the breakout PCB was mounted directly to the feed-through. The remaining connections were the same as in sec. 5.1.1.

6.2 Positioning and characterization of the e⁻ beam

A good knowledge of the shape and position of the e⁻ beam is mandatory in order to determine the dose received by the irradiated samples. The e⁻ beam generated by the Egun300 system has a two-dimensional Gaussian distribution. In the orthogonal (x, y) coordinate system it is parametrized as

$$G_{2D} = \frac{A}{2\pi\sigma_x\sigma_y} \exp\left(-\frac{(x-x_0)^2}{2\sigma_x^2} - \frac{(y-y_0)^2}{2\sigma_y^2}\right), \quad (6.1)$$

where the

- A is the volume of the distribution influenced by the current of the e⁻ beam, the
- (x_0, y_0) are the centre coordinates of the distribution, and the
- (σ_x, σ_y) are the standard deviations of the distribution, each in its own axis.

The last four parameters of the distribution are controlled by the focusing coil. If the current through the coil does not change, neither do those parameters. Consequently, it is necessary to measure them only once before the first irradiation and then keep the coil current constant. As the SPD array connected to the radiation studies measurement system cannot be used as a camera, the positioning and characterization of the e⁻ beam has to be performed with the FC and CCD camera from the Egun300 system.

In order to achieve the best results three methods were developed in order to determine the position and dimensions of the e⁻ beam in the plane of the SPD:

- the knife edge method,

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- the pinhole CCD method, and
- the array threshold voltage shift method.

With the FC measurements of the e^- beam current, the set of parameters is complete as everything needed to parametrize the distribution is obtained.

6.2.1 Knife edge method

The knife edge method is the simplest and yet the most important method. It is so important because it directly provides the x_0^{KE} , y_0^{KE} , σ_x^{KE} , σ_y^{KE} parameters in the plane of the SPD. The KE index stands for the characterization through the knife edge method.

In essence, this method works by blocking the e^- beam in incrementing steps and meanwhile recording the integrated values with the CCD camera. That way a one-dimensional cumulative distribution function is obtained

$$\text{CDF}_i = \text{offset} + \frac{A}{2} \left(1 + \text{erf} \left(\frac{i - i_0^{\text{KE}}}{\sqrt{2}\sigma_i^{\text{KE}}} \right) \right). \quad (6.2)$$

The offset is the integrated response from the CCD when the e^- beam is completely blocked, the erf is the error function, and the i is either x or y dimensions, depending on the direction of movement of the blocking material. In this specific use case, the L shaped cut-out was used as blocker in order to obtain its coordinate. Two such measurements are shown in Fig. 6.5. In both, multiple integrated CCD values were recorded for each position of the blocker in order to minimize the noise originating from the e^- beam and

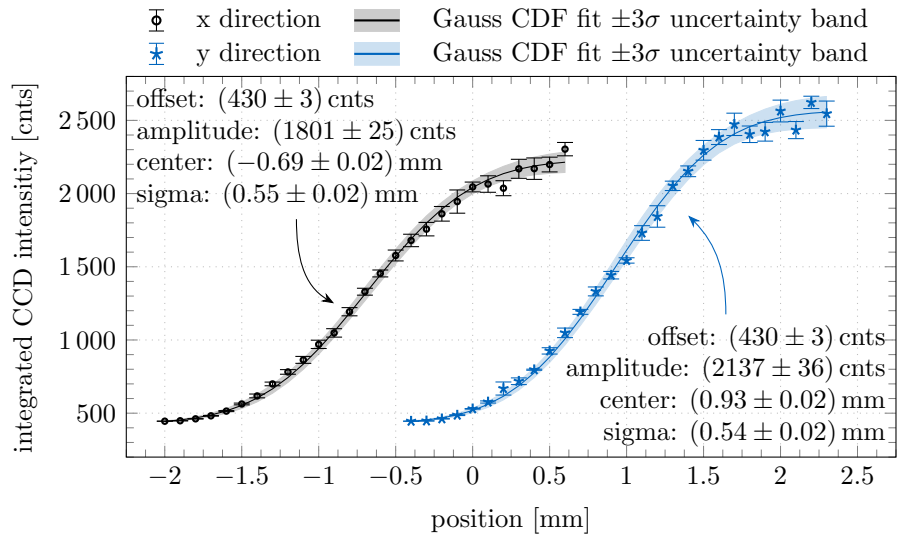


Figure 6.5: Cutting edge method of determining the e^- beam parameters with the aluminium plate for the coarse alignment. The data is from the irradiation of the W09 TL 80k1 SPD.

CCD itself. Those multiple values were then joined to mean values that were used for the fit, and their standard deviations that were used as weights in the fitting procedure.

By using the L shaped cut-out as blocker, its position $(x_0^{\text{KE}}, y_0^{\text{KE}})$ is known. From here, the position of the two pinholes, over which the SPD die is placed, can be roughly calculated from the CAD drawings of the system, and the die carrier PCB stack-up can be moved with the moving stages to the estimated position of one of the SPD die corners.

The emphasis on the word roughly is necessary due to the clearances used in the holes for mounting of the complete die carrier PCB stack-up. Those errors were estimated to a 0.5 mm, which is on the level of the standard deviation of the e^- beam and also on the level of the width of the array. By utilizing solely this method, the position of the array in regards to the centre of the e^- beam would be accompanied with big error margins. Those position error margins would consequently translate to big uncertainties in the determined dose levels for each irradiated pixel. Consequently, this was the reasoning for the inclusion of the two pinholes, through which the positions of the two SPD die corners can be obtained, and the position error margins can be reduced significantly.

As the SPD die corner was positioned roughly in the centre of the e^- beam, the miss-positioning was estimated by eye and added to the shift between the SPD die corner and the centre of the SPD array. This is the end of the method that was used for positioning of the array into the e^- beam. The remaining two methods were used for post-analysis in order to reduce the size of error-bars.

6.2.2 Pinhole CCD method

The pinhole CCD method was developed in order to improve the determination of the relative position between the centre of the SPD array and the centre of e^- beam. The complete procedure is presented in Fig. 6.6, and it will be further described here. Three CCD images are necessary for the method to work:

- an unobstructed image of the e^- beam (top red profile in Fig. 6.6a),
- an e^- beam imaged through the top pinhole (top blue profile in Fig. 6.6a), and
- an e^- beam imaged through the bottom pinhole (bottom blue profile in Fig. 6.6a).

Additionally, the exact length (L) of movement of the die carrier PCB stack-up between the latter two CCD images is needed, as the e^- beam parameters depend on the z position in which they are measured. This is because of the diverging/converging nature of the e^- beam, which is controlled by the setting of the focusing coil. As the CCD camera and the die carrier PCB stack-up are not in the same z plane, the movements in the die carrier PCB stack-up plane need to be scaled for the CCD plane, where they are recorded. The scaling is performed with the magnification factor (M) that will be calculated in the following paragraph. With the combination of the L and M Fig. 6.6a can be finalized, where the bottom red and blue profiles are offset from the top ones by the L/M .

The profile of the unobstructed CCD image is fitted with the two-dimensional Gaussian distribution (eq. 6.1), with the weights set to the square root of intensity – counting

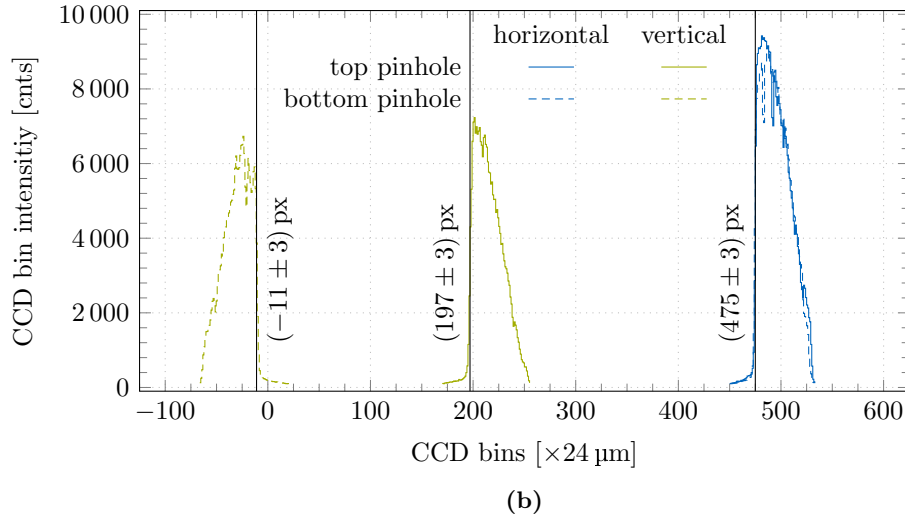
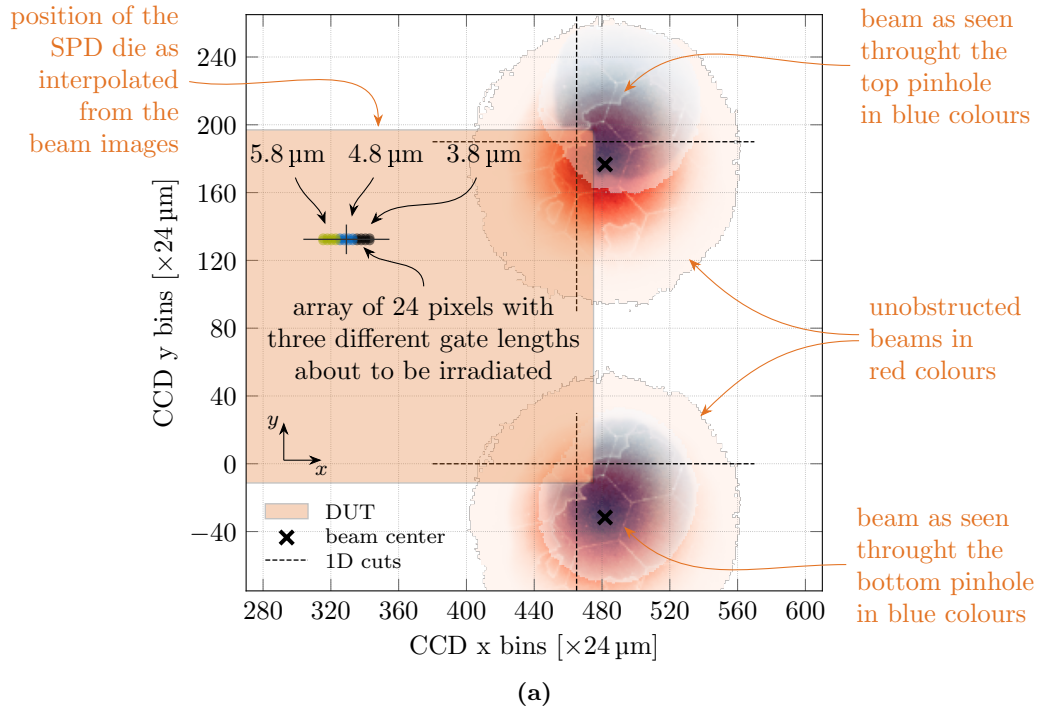


Figure 6.6: Precise method of determining the array position through the SPD die corner locations. For the method to succeed three CCD images are necessary. First CCD image is of the completely unobstructed e^- beam, and the remaining two are the images of the e^- beam that passed through the two pinholes in the die carrier PCB stack-up, where a part of the e^- beam was blocked by the SPD die corner placed over the pinhole. The method also includes a possible rotation of the stack-up against the eigenaxes. End result is shown on (a), whereas (b) shows four one-dimensional slices from which the corner points are evaluated. The data is from the irradiation of the W09 TL 80k1 SPD.

statistics. From there the following parameters are obtained: A^{CCD} , x_0^{CCD} , y_0^{CCD} , σ_x^{CCD} and σ_y^{CCD} , and the magnification factor is calculated as

$$M = \frac{\sigma^{\text{KE}}}{\sigma^{\text{CCD}}} \pm \sqrt{\left(\frac{1}{\sigma^{\text{CCD}} \sigma_{\text{err}}^{\text{KE}}}\right)^2 + \left(\frac{\sigma^{\text{KE}}}{(\sigma^{\text{CCD}})^2 \sigma_{\text{err}}^{\text{CCD}}}\right)^2} \quad (6.3)$$

$$= 0.84 \pm 0.01 \Big|_{\text{W09 TL 80k1}}.$$

The σ^{KE} is measured in the plane of the die carrier PCB stack-up through the knife edge method, and the σ^{CCD} is measured in the CCD plane. A magnification factor smaller than 1 means that the e^- beam is diverging, and is consequently broader in the CCD plane than in the plane of the die carrier PCB stack-up. The e^- beam showed nearly no asymmetry in x and y direction. Thus, a joint value of σ_x and σ_y was used for the calculation of the magnification factor.

Afterwards, the CCD image of the e^- beam obstructed with the top SPD die corner is plotted in the same coordinate system. The image of the bottom SPD die corner is plotted with the L/M shift in the y direction. From here four one-dimensional slices are selected (dashed black lines in Fig. 6.6a), and the SPD die edges are evaluated at the middle of the sharp intensity swing between 20 % and 80 %. To the evaluated values a systematic error of $72 \mu\text{m}$ is assigned, which corresponds with 3 CCD pixels. This is shown in Fig. 6.6b.

The SPD die and the SPD array, about to be irradiated, can now be plotted in the same coordinate system. Consequently, a more precise offset between the centre of the array and centre of the e^- beam can be determined. Without this method it would have to be assumed that the centres of the e^- beam and the array are perfectly aligned. With it, however, it can be evaluated that for the W09 TL 80k1 SPD they were offset by $(136 \pm 60) \mu\text{m}$ in x direction and $(-409 \pm 61) \mu\text{m}$ in y .

6.2.3 Array threshold voltage shift

The third method is meant for the offline analysis with the goal to further improve the precision of the x dimension of e^- beam position. The method does not require any input from the FC or the CCD camera, but is purely based on the differences in threshold voltage shifts measured from the pixels themselves. The method employs the following facts:

- The e^- beam has a Gaussian shape with the (σ_x, σ_y) on the order of the SPD array width.
- Pixels acquire different dose depending on their position, however, the position dependent amount of dose follows the same distribution as found in the e^- beam.
- Pixels with different gate lengths exhibit different threshold voltage shifts.
- By scaling the threshold voltage shifts and fitting their values it is possible to improve the position of x dimension.

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The σ_x from Gaussian profile of the e^- beam is comparable with the width of the SPD array (720 μm). Consequently, the shape of the e^- beam has to be imparted to the array. This is done through the threshold voltage shifts that are very position dependent. The method would have been very straightforward if all pixels would have had identical gate lengths. However, as this was not the case, pixels with different gate lengths reacted to the radiation damage differently (sec. 3.3). Consequently, a more abstract method had to be implemented.

Three steps of the complete procedure are graphically presented in Fig. 6.7, and will be further described in text. The upper plot shows the threshold voltage shifts (ΔU_T) from the last three irradiation steps of the W09 TL 80k1. As expected, different groups of pixels reacted differently, even though some pixels with different gate lengths are neighbours, i.e., pixels on different sides of vertical black lines. The next observation is that pixels from the two different rows reacted similarly and no additional data can be extracted from the tiny differences. Consequently they are joined together through the weighted mean on the middle plot. From here each group of pixels with unique gate length is treated separately. In every group the normalization happens as

$$\text{norm. } \Delta U_{Ti} = \Delta U_{Ti} / \min(\Delta U_{Ti}),$$

where the ΔU_T denotes the pixel's threshold voltage shifts, \min is the minimum value selector, and i is the unique group of pixels with the gate lengths of either 3.8 μm , 4.8 μm or 5.8 μm . This essentially changes the ΔU_T values to the interval from 0 to 1. The most negative ΔU_T is assigned the value 1 and the rest are scaled to it.

For the bordering pixels between the groups the algorithm is as follows. It takes the last two pixels of one group and calculates the norm. ΔU_T difference between them. This step gets repeated on the first two pixels from the consequent group. From those two values it then calculates a single mean value, and it uses it to correct all norm. ΔU_T values from the latter group of pixels. Additionally, it also assigns the systematic uncertainty of the procedure on the order of 5%. Because of the scaling the values can now be also greater than 1. The algorithm for correction of the border values is first applied to the 3.8 μm and 4.8 μm groups of pixels, and afterwards also to the 4.8 μm and 5.8 μm groups. The uncertainties are scaled through the Gaussian propagation.

The last remaining step is to fit the one-dimensional Gauss function

$$G = \frac{A}{\sqrt{2\pi}\sigma_x} \exp\left(-\frac{(x-x_0)^2}{2\sigma_x^2}\right)$$

over the data points from matching irradiation steps. Parameter names are the same as for the two-dimensional Gaussian distribution (eq. 6.1). Center and standard deviation parameters from the fits are gathered in Tab. 6.1. The combined centre position of $(128 \pm 25) \mu\text{m}$ is well in line with the result from the pinhole CCD method, but with a significantly smaller error. The combined standard deviation of $(492 \pm 39) \mu\text{m}$ is also inline with the initial values from the knife edge method. However, the initial method yields the result in fewer steps and has consequently smaller error.

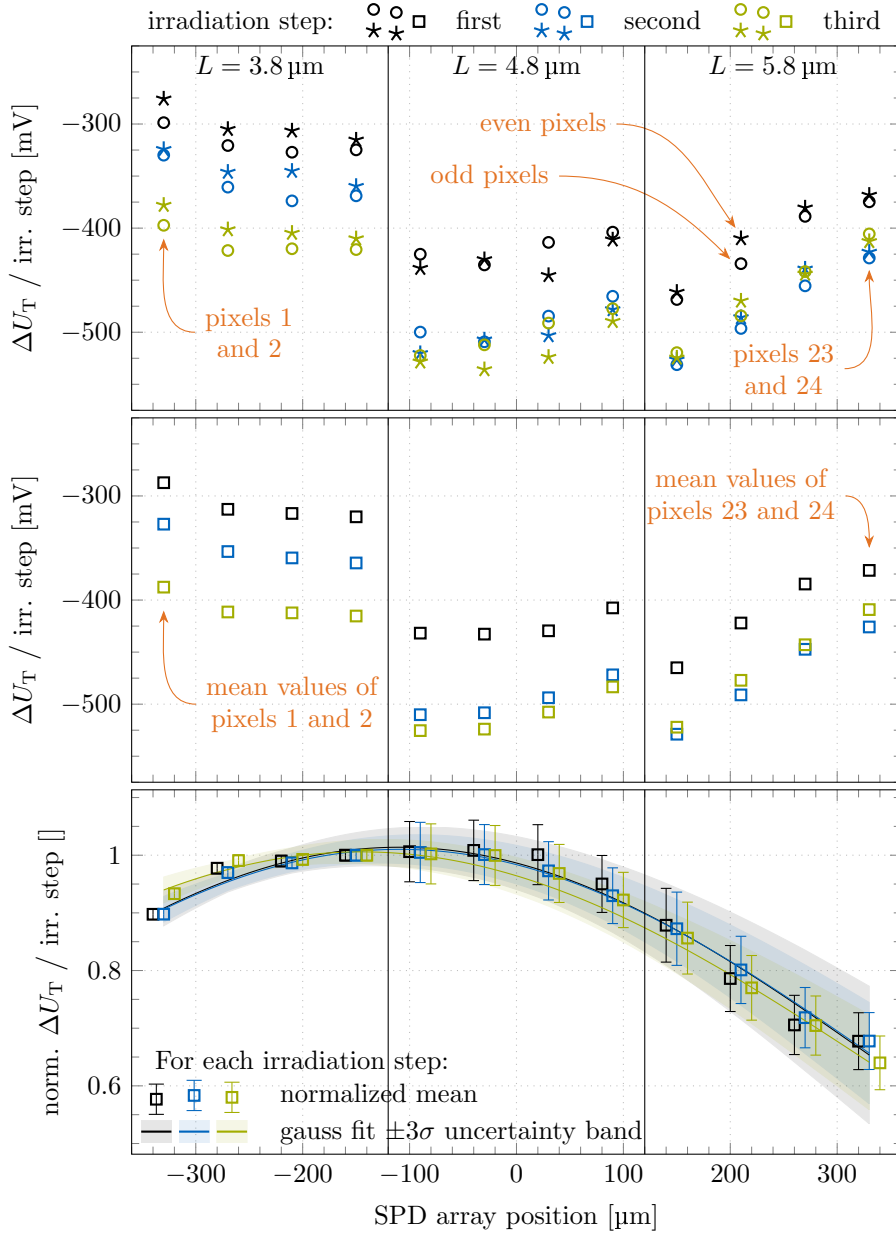


Figure 6.7: An abstract method of determining of the e^- beam x position maxima from the threshold voltage shifts. The method uses the fact that the shape of the e^- beam is Gaussian. From there it corrects the results through normalization and offset corrections, and afterwards fits the shape with a Gaussian profile. Different points have different weights that depend on the amount of corrections. On the lower plot, data points from different irradiation steps are offset for $\pm 10 \mu\text{m}$ with regards to the blue dataset. The data is from the last three irradiation steps performed on the W09 TL 80k1 SPD. The first step denotes the irradiation from 127 min to 185 min, the second from 185 min to 245 min, and the third from 245 min to 295 min. The fit parameters are presented in Tab. 6.1.

6 Radiation studies

Table 6.1: Center and standard deviation parameters of the Gauss distribution fits presented in Fig. 6.7.

	x_0 [μm]	σ_x [μm]
127 min to 185 min	109 ± 8	473 ± 16
185 min to 245 min	145 ± 8	501 ± 18
245 min to 295 min	155 ± 19	596 ± 48
w. mean	128 ± 25	492 ± 39

6.2.4 Electron beam current

Current of the e^- beam was precisely measured by the means of the FC that was connected to the current meter. Before each irradiation step, and additionally after the last one, the FC was placed into the e^- beam path so that all e^- from the e^- beam were collected in it. The current (I_{ON}) was afterwards measured for 2 min to 5 min with one measurement point every 3 s. Afterwards, the e^- beam was turned off by blocking the laser beam, and the measurement of the vacuum level (I_{OFF}) was performed in the same duration. Multiple measurements were necessary in order to reduce the noise level. The amount of e^- (N_{e^-}) inside each e^- bunch follows the

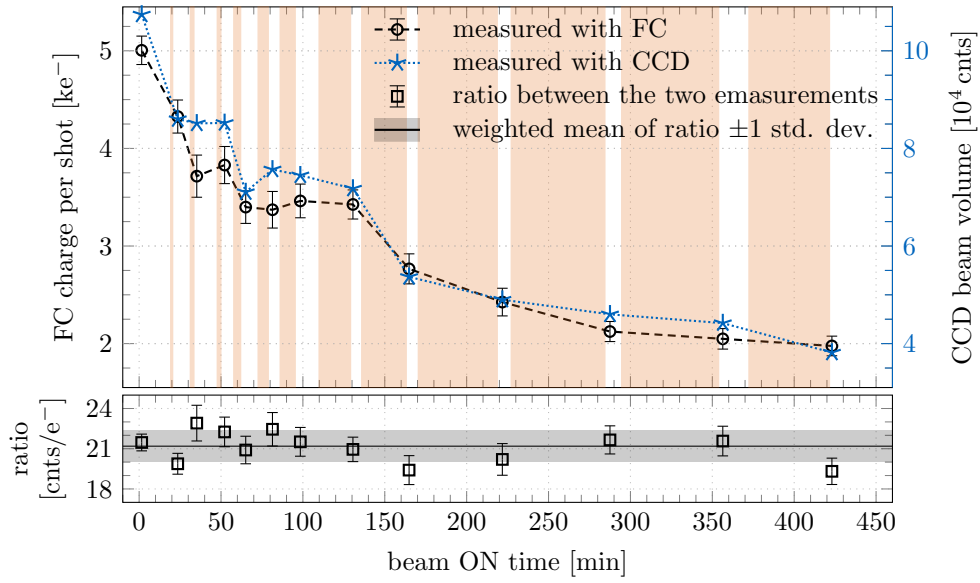
$$N_{e^-} = \frac{I_{\text{ON}} - I_{\text{OFF}}}{e\nu},$$

where e is the elementary charge constant of $1.602 \cdot 10^{-19}$ C [11], and ν is the frequency of laser pulses (1 kHz). Those measurements, with regards to the total time when the e^- beam was turned on, are plotted in Fig. 6.8a. As it can be observed, the current of the e^- beam changed drastically throughout the complete irradiation procedure of a single SPD. This was against the expectations and prolonged the complete campaign.

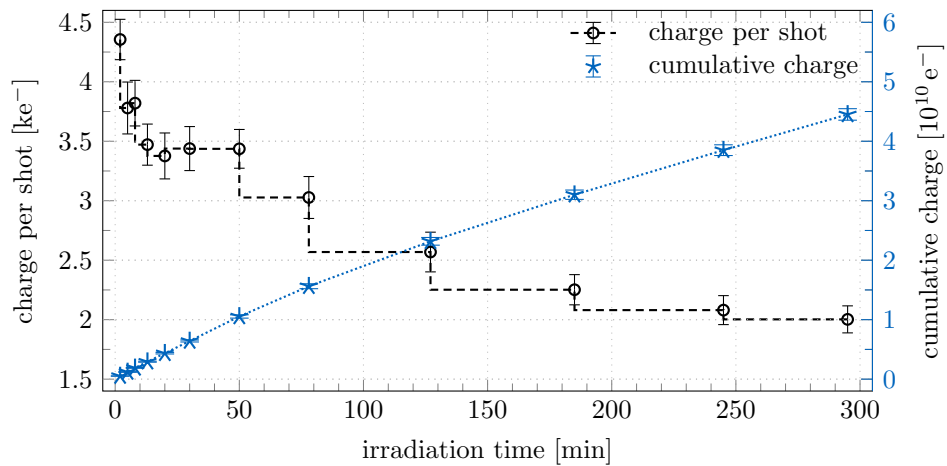
Linear interpolation was used to calculate the average amount of e^- hitting the SPD during each irradiation step. Irradiation times were placed on the total e^- beam ON time scale according to the data logs, and the mean value of e^- in that period was kept for the dose tracking. This is shown in Fig. 6.8b, where charge per shot and cumulative charge are shown with respect to the irradiation time.

In addition to the charge per shot measured with the FC, Fig. 6.8a also shows the e^- beam volume as obtained from the CCD images of the unobstructed e^- beam. As the latter is directly proportional to the former, an additional fail-safe is in place to observe the e^- beam parameters. Between them the conversion ratio of (21.2 ± 1.2) cnts/ e^- is measured. However, as the FC results are integrated over a larger period of time, their values are preferred. The CCD results are there just as a backup in case of corrupt file problems with the FC method.

6.2 Positioning and characterization of the electron beam



(a)



(b)

Figure 6.8: (a) Number of e^- in the bunch as obtained from the FC, volume of the unobstructed e^- beam as obtained with the CCD camera, and the conversion factor between the two. Orange stripes represent the irradiation times, i.e., when the e^- were hitting the SPD. (b). Average number of e^- in the bunch during the irradiation of the sensor and their cumulative number.

6.3 Determination of the total ionizing dose

Geant4 simulations [174] in combination with all parameters obtained in previous sections were used to assign the total ionizing dose inflicted to the SiO_2 of each pixel. The simulations were performed by I. Dourki. The exact stack-up of layers (e.g., SiO_2 , poly-Si, aluminium) used in the SPD DePFETs is simulated in combination with multitude of impinging high energy e^- . From there, the average dose imparted to each layer can be obtained. The results of such simulations are shown in Fig. 6.9. The left plot shows the imparted dose to the stack-up around the DePFET's channel, and the one on the right to the stack-up around the parasitic channel. Three different energies of impinging e^- were simulated. The dose is calculated as the energy that the impinging e^- imparted to the specific layer (E_{imp}^i) divided with the mass of that layer (m^i)

$$\text{total dose}^i = \frac{E_{\text{imp}}^i}{m^i},$$

where i denotes the layer [181]. More on the specifics of described simulations can be found in the PhD thesis of I. Dourki [82].

Fig. 6.10 shows the obtained results after 6 irradiation steps performed on the W09 TL 80k1 SPD. To obtain the dose imparted to each pixel in the SPD array the data from all previous methods is joined together. The e^- beam dose profile in each irradiation step is obtained by the combination of:

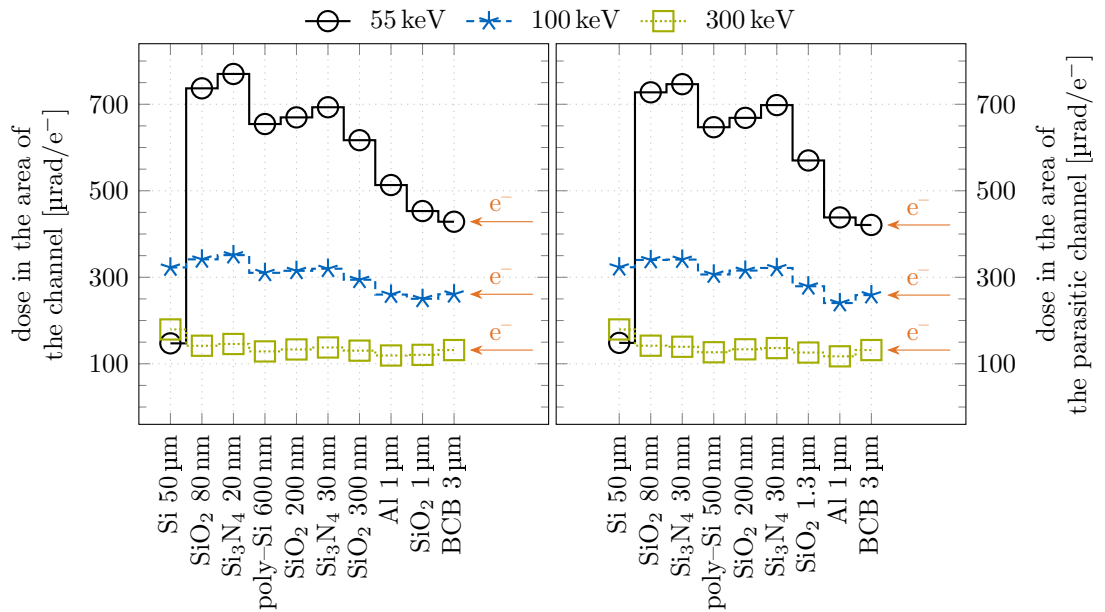


Figure 6.9: Simulations for the dose per layer in the EDET DH80k DePFET layout, caused by a single e^- . In addition to the shown layers, there is also a $400 \mu\text{m}$ thick layer of Si on the left side. Simulations were performed with the Geant4 simulation tool [174] by I. Dourki [175].

6.3 Determination of the total ionizing dose

- the parametrization of the unobstructed e^- beam through the CCD image in order to obtain the e^- beam centre and standard deviation,
- the measurements of the e^- beam current in order to obtain the amount of e^- in each shot, and
- the conversion from the number of e^- to the dose through simulations.

Through the position of each pixel in the e^- beam dose profile, obtained by methods described in sec. 6.2, a dose value after each irradiation step is obtained. In the first irradiation step (top left plot in Fig. 6.10) the e^- beam centre was missing the SPD array for almost 1 mm due to the wrong settings on the focusing coil. This was realised and corrected before the second irradiation step (top centre plot in Fig. 6.10). Because of the changes, the e^- beam shape and position changed with regards to the SPD array. Con-

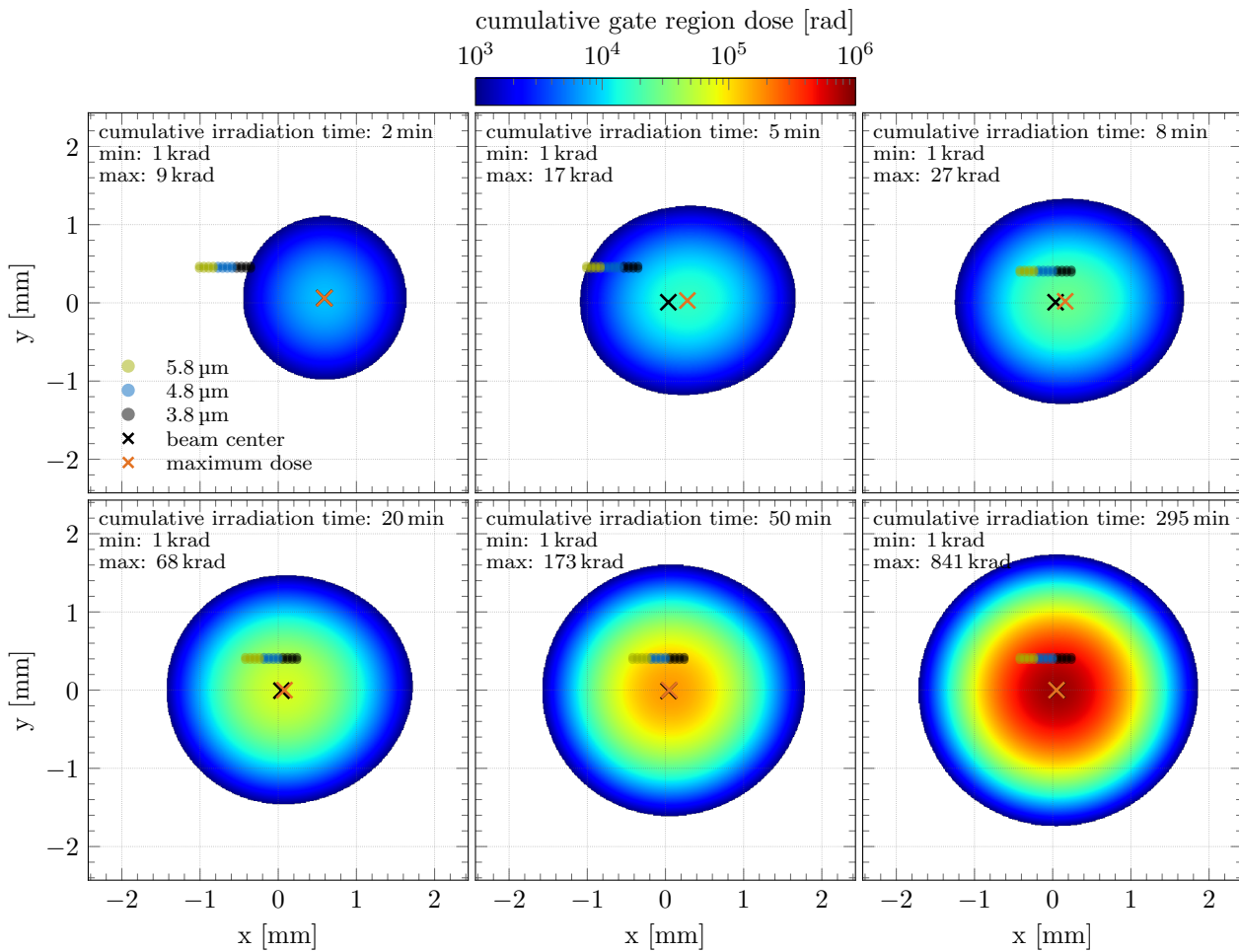


Figure 6.10: Final combination of pixel positions and e^- beam parameters in order to obtain the most precise dose estimation for each pixel. Data is taken from the irradiations of the W09 TL 80k1 SPD.

sequently, the centre of the e^- beam is misaligned with the point where the cumulative dose is at its maxima. As the threshold voltage shifts obtained in this configuration were still small in comparison to what they should be, the repositioning of the SPD array was performed through the visual pinhole CCD method. This is seen in the third irradiation step (top right plot in Fig. 6.10). At that point the SPD array was as close to the centre of the dose profile as it could have been determined with the data available at that time. The following three irradiation steps, shown in the bottom row in Fig. 6.10, feature no other changes but the changes in the maximum dose. As the amount of e^- shot in the first irradiation steps is almost negligible when compared to all other steps, the centre of the e^- beam and position of the dose maxima coincide more and more towards the end of the irradiations.

6.4 Threshold voltage shifts

Threshold voltage shifts in dependence of the dose inflicted to the SiO_2 layer below the gate structure are shown in Fig. 6.11. All three irradiated SPDs are included and are segregated according to the gate length groups. The response curves look similar to the ones already found in literature on the topic of DePFET radiation damage [163, 182, 183]. However, none of them performed the studies with e^- in the transmission electron microscopy energy range. Even though the mechanisms for oxide damage are the same, the examination of how the EDET DH80k structures will cope with radiation effects is warranted. To build on the existing literature, the curves could be described as

$$\Delta U_T(\text{dose}) = \begin{cases} A - B \cdot \ln(\text{dose}) & ; \text{dose} \leq \text{dose}_0 \\ C - D \cdot \text{dose} & ; \text{dose} > \text{dose}_0 \end{cases},$$

where the ΔU_T is the threshold voltage shift, and the A , B , C and D are the coefficients. Meaning that initially the radiation damage has a logarithmic response to the point dose_0 , and from then on it behaves linearly. In the initial logarithmic part all SPDs behave extremely similar³, and additionally this region of operation will quickly be surpassed in the real life operation of the EDET DH80k DePFET's.

Therefore, it makes more sense to focus only on the linear part, as it will be in this part where the SPDs will live the majority of their lifespan. The measurement points beyond the 150krad of total ionizing dose were therefore linearly interpolated. The interesting result of the linear interpolation is its slope, as it tells how the threshold voltage shift is changing with the respect to radiation damage. Under the condition that the linear regime continues beyond the measured point, one can extrapolate and predict the future behaviour. The slopes are gathered in Tab. 6.2.

In the linear regime, two SPDs always overlap within one standard deviation error bands, and the third one always differs. The two SPDs behaving similarly are built on standard wafers, whereas the third SPD, W09 TL 80k1, was built on the silicon-on-insulator (SOI) wafer. The latter SPD always shows worse performance in comparison

³Within the scope of groups of pixels with identical gate lengths.

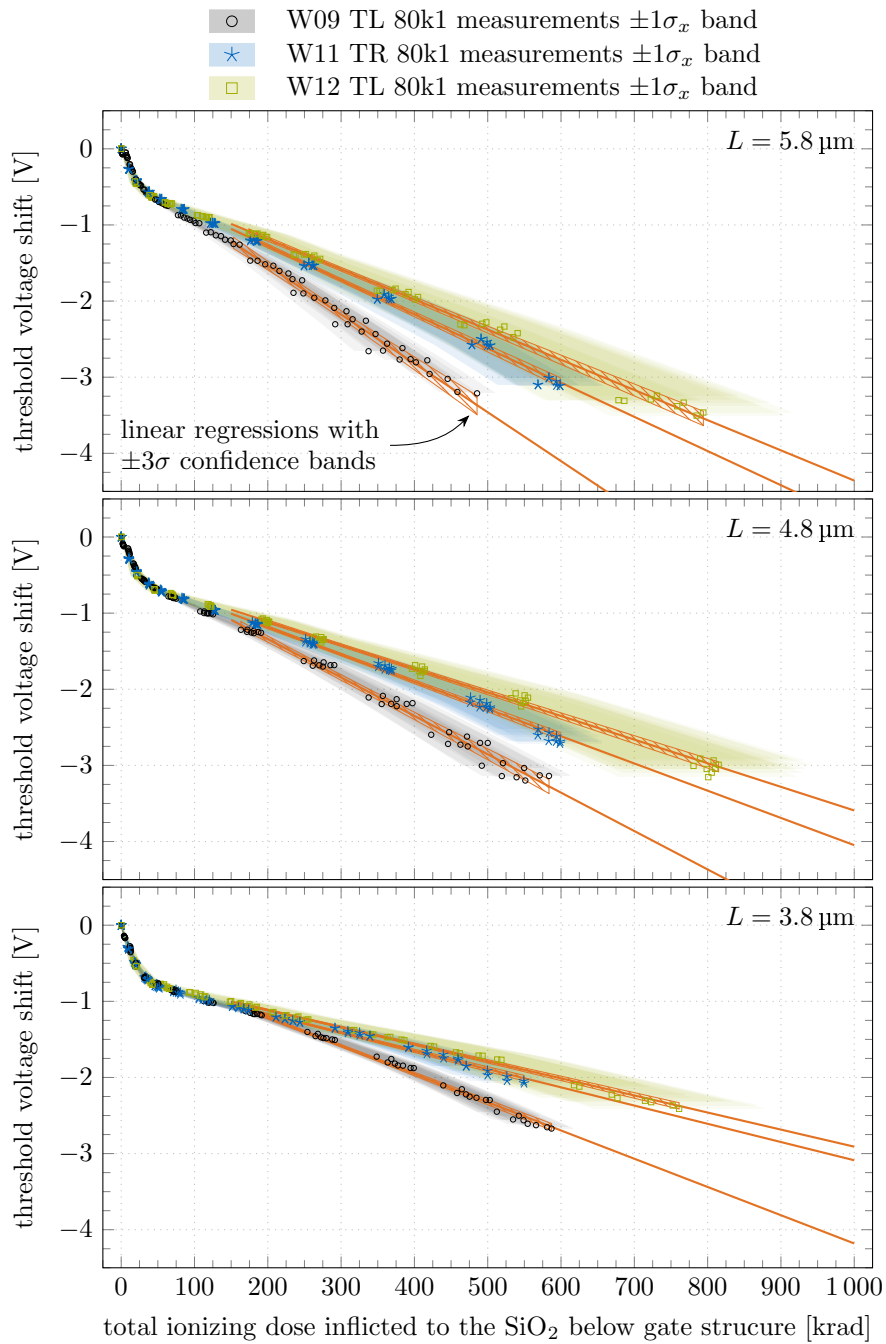


Figure 6.11: Threshold voltage shifts for the DePFET channel. Results from the irradiation studies performed on the W09 TL 80k1, W11 TR 80k1 and W12 TL 80k1 SPDs. Pixels are segregated by their gate length groups. Numerical values for linear extrapolations are presented in Tab. 6.2.

6 Radiation studies

Table 6.2: Rate of the gate damage extracted from the linear part of the threshold voltage shift versus the total ionizing dose curve for measurements performed on the W09 TL 80k1, W11 TR 80k1 and W12 TL 80k SPDs. Numerical collection of results presented in Fig. 6.11.

	rate of damage [V/Mrad]		
	3.8 μm	4.8 μm	5.8 μm
W09 TL 80k1	-3.7 ± 0.1	-5.0 ± 0.1	-6.4 ± 0.2
W11 TR 80k1	-2.4 ± 0.1	-3.6 ± 0.1	-4.5 ± 0.2
W12 TL 80k1	-2.2 ± 0.1	-3.1 ± 0.2	-4.0 ± 0.2

to the former two. Due to a statistic sample of only 3 SPDs, the real reason behind the discrepancy cannot be explained with confidence. As there were no differences on the frontside manufacturing of DePFETs in PXD10–1 production batch at HLL MPG (chapter 4), only two plausible reasons for the differences to occur come to mind:

- First is a different polishing of the surface between the SOI and standard wafers, which is a consequence of additional steps needed at external contractors in order to produce SOI wafers, and the different surface quality can influence the rate of radiation damage [113].
- The other reason can simply be because of the unnoticed mistake that occurred while the W09 TL 80k1 SPD was irradiated, e.g., wrongly applied biasing conditions or wrongly measured e^- beam current.

In order to investigate the difference, additional irradiation campaigns are necessary. In those future campaigns, multiple SPDs of both types will be the subject of investigations in order to determine which response curve is the most likely one.

The only other measurements, on which the EDET estimations for threshold voltage shifts under e^- irradiation were based, were performed in M. Hensel’s master thesis [184]. He irradiated two DePFET like structures from the PXD9 production run. The gate dimensions were 20 μm in length and 120 μm in width. He irradiated them with the same Egun300 system as described in sec. 6.1, albeit with different e^- beam specifications. For them he measured a maximum threshold voltage shift of about -2.5 V at the estimated dose of 1.5 Mrad. In comparison with measurement performed in this work, his results show much slower rate of the threshold voltage shifts. However, it should be noted that for his measurements the e^- beam current was believed to be constant and was not measured throughout the course of irradiation. As shown in sec. 6.2.4, the current is all but constant. Consequently, the estimated dose in ref. [184] can be greatly overestimated.

To return to the measurements performed in this work. The rates of the threshold voltage shifts are shown in Fig. 6.12, where all results from Fig. 6.11 are gathered on a single plot. In addition to measured points, a linear interpolation is performed on the two dataset. The first set is with the points from the measurements performed on the

SPD built on a SOI wafer, and the other from the SPDs built on standard wafers. In case of the former, the reduction in the rate of damage is $(21.0 \pm 1.5) \%$ when the gate length decreases from $5.8 \mu\text{m}$ to $4.8 \mu\text{m}$, and an additional $(26.5 \pm 1.9) \%$ when it goes from $4.8 \mu\text{m}$ to $3.8 \mu\text{m}$ – this is denoted with orange arrows in Fig. 6.12. For the SPDs built on the standard wafer the reduction is $(23 \pm 9) \%$ in the former change, and an additional $(30 \pm 10) \%$ in the latter. In all cases, the shorter the gate length the less pronounced are the effects of radiation damage. This is in line with the observations made in the PhD thesis from A. Ritter [163]. Therefore, it can be ruled out, with a high degree of certainty, that this is a consequence of a measurement artefact or a mistake in the data analysis. However, mechanism behind the gate length dependency of radiation damage rates is unknown. The radiation hardness comparison of commercial MOSFET devices is done for transistors with different gate lengths, but those transistors always come from different technologies where there are additional variables, e.g., width of the transistor, dielectric thicknesses. Consequently, no specific reason as to why the shorter gate lengths perform better can be given. In order to uncover this effect, the simulations and additional radiation studies are needed. The former are essential for determination of the exact electric fields in the SiO_2 below the poly-Si structures, and the latter can show the influence of different biasing conditions on the rate of radiation damage, e.g., how the rate of damage, in dependence of the gate length, changes if source and drain are kept at the same potential.

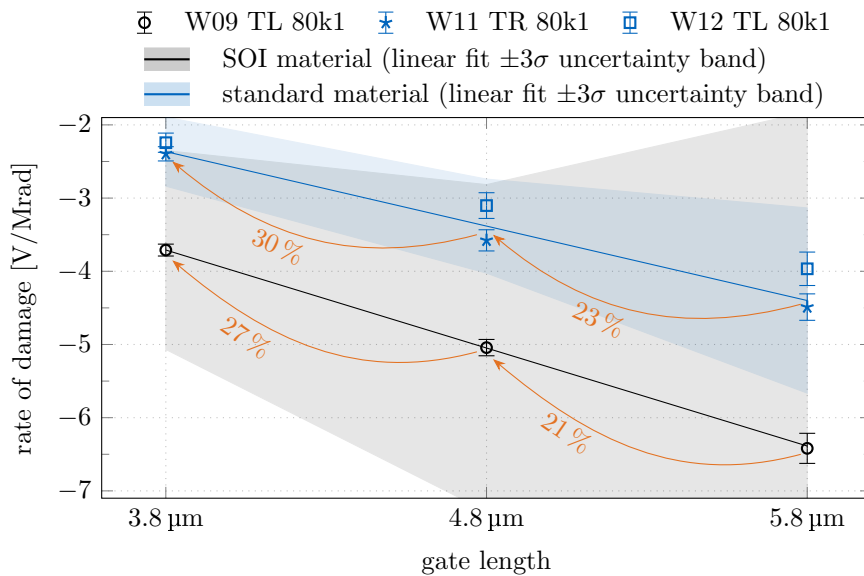


Figure 6.12: Rate of the threshold voltage shifts in dependence of the gate length as extracted from Fig. 6.11. The SPDs built on the same type of material (SOI or standard) are evaluated together. The improvements between different gate lengths are shown with the orange colour.

The question now is what happens with the operation of DePFETs that have sustained radiation damage. The results presented so far suggest that shorter gate lengths should cope better with the radiation, as the rate of damage is slower with them. However, an impact of the gate length variations (discussed in sec. 5.2.1.1 under the paragraph of measurement errors) on the threshold voltage shifts needs to be taken into account as well. In order to include it, a simulation was performed with the goal of predicting the changes in the DePFET array operation, that are caused because of gate dimension variations and radiation effects.

Simulation of radiation damage For the simulations presented here, 8192 pixels arranged in the same shape as in the prototyping matrices (PMATs) were simulated. A simulation is performed through the response of an empty DePFETs. For this the offset drain current is modelled with eq. 3.7 as

$$I_{\text{OFFS}} = \begin{cases} \frac{W}{L} U_G^2 \cdot K & ; U_G < U_T \\ 0 & ; U_G \geq U_T \end{cases}, \quad (6.4)$$

where:

- W and L are the respective gate width and length distributions generated with the standard deviation of 40 nm [162] around their mean values W_0 and L_0 . The L_0 values used with this simulations are the 5.8 μm , 4.8 μm and 3.8 μm , and the W_0 value is 27.8 μm .
- The U_G and U_T are respectively the applied gate voltage and threshold voltage. Both of them are dimensionally dependent and were derived from the measurements presented in sec. 5.2.1.1. The condition for the U_G derivation was so that the drain current was 100 μA in the actual measurements. This resulted in the U_G (U_T) of -2.4 V (-0.5 V) for the DePFET pixels with the gate length of 5.8 μm , -2.0 V (-0.4 V) for the DePFET pixels with the gate length of 4.8 μm , and -1.6 V (-0.15 V) for the DePFET pixels with the gate length of 3.8 μm .
- The K wraps the remaining constant of eq. 3.7, however, in the simulation it is calculated as

$$K = 100\ \mu\text{A} \Big/ \frac{W}{L} U_G^2,$$

in order to have the mean of the generated distribution of drain currents positioned nicely at 100 μA .

At this point the initial offset drain current distribution is obtained and the effects of radiation have to be included. For this, three different scenarios were simulated. In the first, the dose profile is completely uniform over the complete PMAT area, whereas in the second and third scenario there exists a linear gradient over the simulated PMAT columns, while still being constant along the simulated PMAT rows. For the second

scenario the total gradient is 5 %, from -2.5% on the first column to 2.5% on the last one. The total gradient for the third scenario is 10 %, and it is distributed over the PMAT in the same way as in the previous scenario. In both cases, pixels to the right of the centre column receive more radiation damage, and pixels to the left receive less.

In order to convert the dose value to the threshold voltage shift value that is actually hurting the performance the linear interpolations shown in Fig. 6.12 were used. Consequently, even the small deviations from the L_0 value will evaluate to the different threshold voltage shifts. This essentially means that the U_G becomes

$$U_G \rightarrow U_{G,0} + \Delta U_T - \text{mean}(\Delta U_T) ,$$

where $U_{G,0}$, ΔU_T and $\text{mean}(\Delta U_T)$ are as following:

- The $U_{G,0}$ is the applied gate voltage from previous eq. 6.4.
- The ΔU_T is a function of the gate length L as

$$\Delta U_T = (kL + n) \cdot \text{dose profile} ,$$

where k and n are the linear interpolation parameters from Fig. 6.12, and the dose profile is as described in the above paragraph.

- The $\text{mean}(\Delta U_T)$ is the mean value of the threshold voltage shift for which the applied gate voltage is corrected in order to have the mean of the distribution again at $100\ \mu\text{A}$.

All building blocks of the simulation are now know, and the result of one such simulation is presented in Fig. 6.13. On it the offset current distributions are shown for the three different gate lengths ($5.8\ \mu\text{m}$, $4.8\ \mu\text{m}$ and $3.8\ \mu\text{m}$) and three different levels of inflicted radiation damage (initial distribution⁴ and after 1 Mrad and 2 Mrad of uniformly inflicted dose). The distributions quickly widen solely from the gate length variance. The next thing that can be seen is that the initial distribution is wider when the mean gate length is smaller. This also propagates further under uniform irradiation. Consequently, after some radiation damage the offset current distribution of pixels with shorter gate lengths is wider than that of the pixels with larger gate lengths.

Parametrization of the offset current distribution through its standard deviation is shown in Fig. 6.14. In addition to the uniform dose profile scenario, results from the other two scenarios with 5 % and 10 % gradients in the dose profile are shown as well. In each colour group of curves belonging to the left hand side axis the lowest line represents the best behaviour. For the first two scenarios, pixels with longer gate lengths perform the best. However, at 10 % gradient in the dose profile, pixels with shorter gate length show better performance. The improvement happens inside 0.5 Mrad of inflicted dose, where an initially wider distribution of the pixels with shorter gate lengths improves

⁴The initial distribution in this case is not the one of the unirradiated sensor but of the slightly irradiated sensor. Slight irradiation means that the threshold voltage shift behaviour is just out of the logarithmic region at the beginning of the linear region. For all measured pixels with three different gate lengths this happens around 50 krad.

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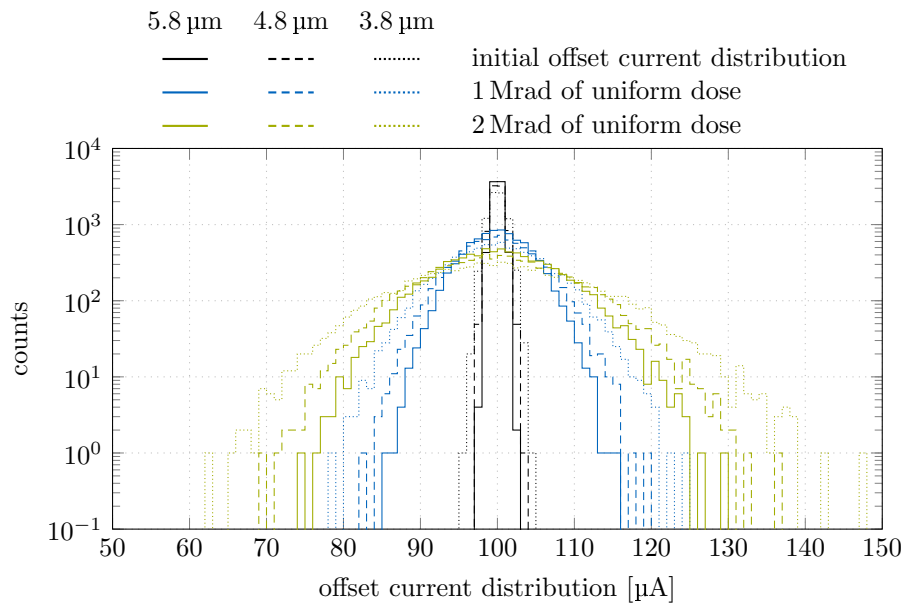


Figure 6.13: Changes in the offset current distributions under the uniform irradiation over the complete array area. Changes originate solely from the variance of the gate lengths.

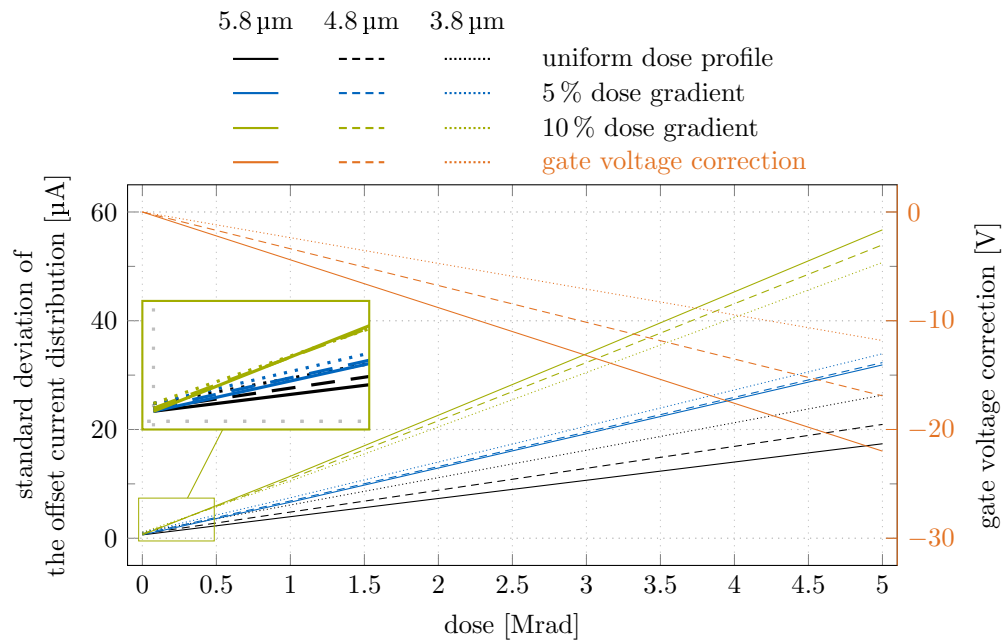


Figure 6.14: Spread of the offset current distributions in dependence of the dose for the three different dose profile scenarios. The right axis is showing the necessary correction of the gate voltage in order to have the offset current distribution centred around 100 μA .

beyond that of the pixels with longer gate lengths. Consequently, the choice of the gate length should be based on the homogeneity of the radiation. If the radiation is really homogenous, then longer gate lengths are preferred. However, if there exist an in-built inhomogeneity of radiation, shorter gate lengths are beneficial.

On top of the shown standard deviations, the right hand side axis in Fig. 6.14 shows also the gate voltage corrections necessary to keep the centre of offset current distribution at 100 μA . Here, the shorter gate lengths are preferred due to the smaller rate of damage. Those overall shifts are important as the switcher ASICs (sec. 5.1.2.1) are capable of operating only in a specified voltage range. Consequently, if the corrections become too negative it could be that the gate voltage goes out of the operation window of the switcher ASICs. Additionally, different aluminium lines on the DePFET front side cross each other with dielectrics between them. Normally, the breakdown voltage between two aluminium layers is above 100 V. However, there exist artefacts, i.e., aluminium hillocks [185], that occur during the production and cause weaknesses in the dielectrics. Because of those artefacts the breakdown voltage can be greatly reduced, and in case of the big potential difference between two aluminium lines a breakdown can occur between them. This in turn essentially renders a part of the array useless.

Consequence of the offset current distribution widening The offset current plays a role in the intrinsic amplification factor of the DePFET's. This is seen from eq. 3.7, where the signal drain current in the saturation mode of operation follows the

$$I_{\text{SIG}} = g_{\text{q}} Q_{\text{SIG}} = K I_{\text{OFFS}}^{0.5} Q_{\text{SIG}} ,$$

and K denotes the constants from the mentioned equation. The radiation will, therefore, not only change the offset current distribution, but also the charge amplification (g_{q}). Consequently, the EDET DH80k sensor will have to be calibrated many-a-time during its lifespan in order to ensure equal responses from all pixels.

6.4.1 Parasitic threshold voltage shifts

The conditions in the parasitic channel during this radiation campaign did not represent the realistic conditions for the EDET DH80k sensors. In order to keep the charge storage regions empty, the clear gate (CG) was biased with a very positive voltage. This in turn caused strong electric fields in the SiO_2 below CG structure, and due to this the yield of h^+ that escape initial recombination is higher than it should be (sec. 3.3). Consequently, the amount of h^+ that get trapped in the SiO_2 is higher as well. This leads to the significantly higher parasitic threshold voltage shifts. In dynamically operated EDET DH80k DePFET arrays, the CG is kept around 0 V. Consequently, the parasitic threshold voltage shifts should be smaller under the same dose.

Measurements of the parasitic threshold voltage shifts are presented in Fig. 6.15. It can be seen that even after 700 krad of dose the response is still not in the linear regime. However, in order to do the worst case estimations, the linear interpolation was performed on all data points beyond the dose of 200 krad. That way, an extrapolation

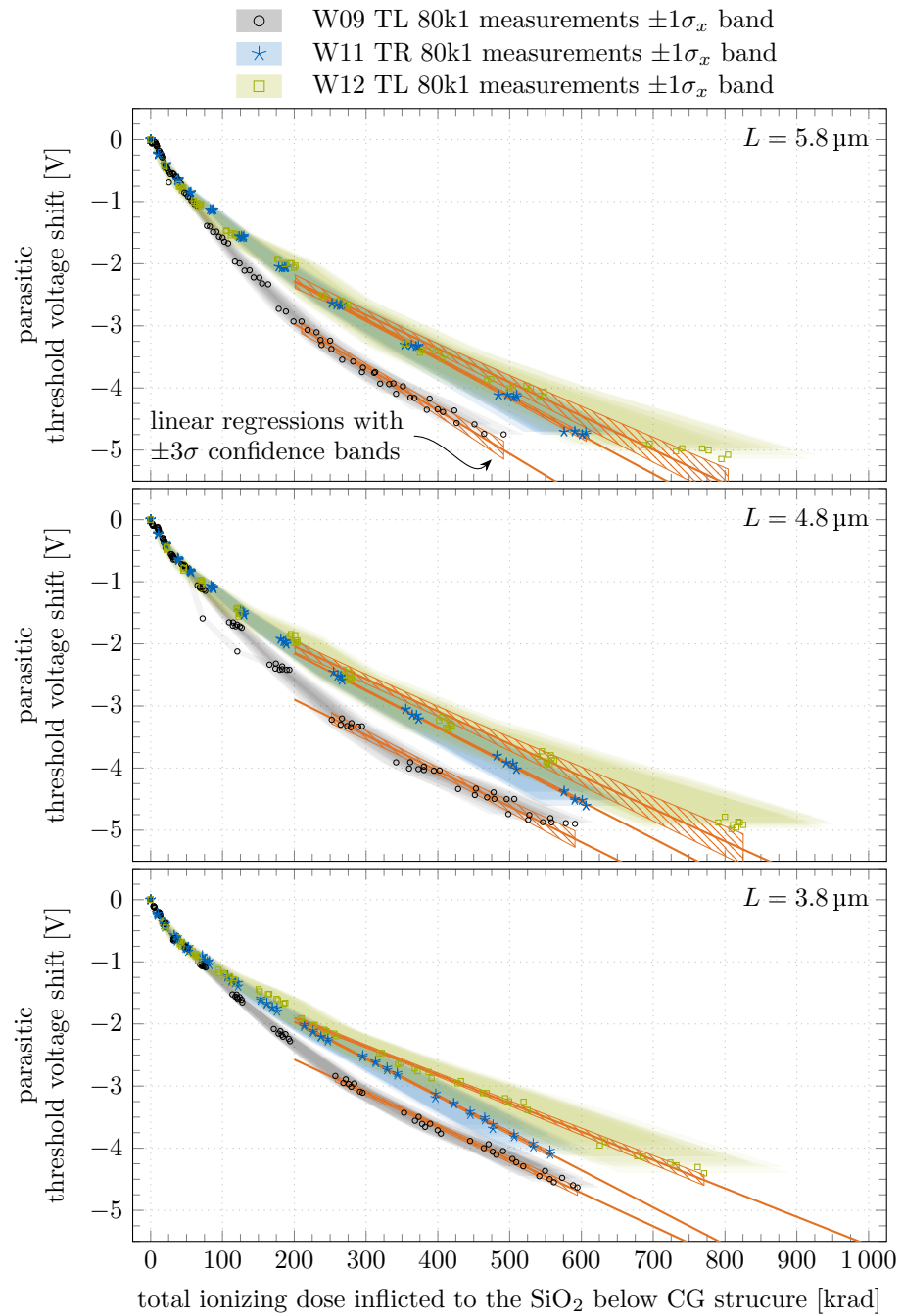


Figure 6.15: Threshold voltage shifts for the parasitic DePFET channel. Results from the irradiation studies performed on the W09 TL 80k1, W11 TR 80k1 and W12 TL 80k1 SPDs. Pixels are segregated by their gate length groups. Numerical values for linear extrapolations are presented in Tab. 6.3.

can be made to the minimal longevity⁵ of DePFET structures inside the CG operation window. The numerical values of linear interpolations are gathered in Tab. 6.3. As the values from different SPDs are representing the worst case scenarios nothing is lost if the weighted mean is calculated, and joined values are taken further.

Assuming a 2.5 V of the CG operation window (sec. 5.3.1.1) different scenarios can be thought of. In the ideal case of a completely homogeneous dose profile and a well defined parasitic channel dimensions, the CG voltage would never come out of its operation window, but would only need to be adjusted for the shifts. However, in case of the 10% gradient in the dose profile the 3.8 μm structures would spread over the complete operation window before (4.72 ± 0.20) Mrad. The 4.8 μm structures would do the same in (4.38 ± 0.18) Mrad, and 5.8 μm ones in (3.97 ± 0.15) Mrad. The emphasis has to be on the word 'before'. This is due to the fact that the length and width of the parasitic channel are not trivially defined. Consequently, it cannot be simply simulated what the variations cause. It can only be hoped, that the negligence of those variations will not cause bigger problems, than the correct biasing will bring improvements. Therefore, those values could be a realistic and not worst case estimation.

Table 6.3: Rate of the damage extracted from the parasitic threshold voltage shift versus the total ionizing dose curve for measurements performed on the W09 TL 80k1, W11 TR 80k1 and W12 TL 80k SPDs. Numerical collection of results presented in Fig. 6.15.

	rate of damage [V/Mrad]		
	3.8 μm	4.8 μm	5.8 μm
W09 TL 80k1	-5.4 ± 0.2	-5.7 ± 0.2	-7.0 ± 0.3
W11 TR 80k1	-6.0 ± 0.3	-6.0 ± 0.3	-6.2 ± 0.4
W11 TR 80k1	-4.6 ± 0.3	-5.2 ± 0.3	-5.4 ± 0.4
w. mean	-5.3 ± 0.6	-5.7 ± 0.3	-6.3 ± 0.8

6.5 Subthreshold behaviour

The subthreshold behaviour can be evaluated after each irradiation step in the same manner as it was described in sec. 5.2.1.3. However, here the values that tell how quickly the transistors turn ON (Fig. 6.16) yield an additional piece of information about the interface traps. From the subthreshold voltage swing (SVS) definition (eq. 5.3) the following relation is obtained for the perfect MOSFET without interface traps in weak inversion [90]

$$\text{SVS}_{\text{IDEAL}} = \ln 10 \frac{k_{\text{B}}T}{e} \frac{C_{\text{OX}} + C_{\text{D}}}{C_{\text{OX}}}, \quad (6.5)$$

⁵As the curve should become less steep in the linear region, the presented case really serves as the worst case scenario and actual longevity will be increased. Additionally, biasing of the CG around 0 V also works in the direction of increasing the longevity.

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where C_D is the capacitance of the semiconductor depletion layer per unit area. However, in case there exists a significant density of interface traps⁶ ($D_{IT} = C_{IT}/e^2$), the above capacitive voltage divider has to include the capacity contribution of interface traps (C_{IT}) as well. The numerator, therefore, gets an additional contribution in form of C_{IT} and eq. 6.5 can be rewritten in form of density of interface traps.

$$\begin{aligned}
 SVS &= \ln 10 \frac{k_B T}{e} \frac{C_{OX} + C_D + C_{IT}}{C_{OX}} \\
 &= SVS_{IDEAL} + \ln 10 \frac{k_B T}{e} \frac{C_{IT}}{C_{OX}} \\
 &= SVS_{IDEAL} + \ln 10 k_B T e \frac{D_{IT}}{C_{OX}} \\
 D_{IT} &= \frac{C_{OX}}{\ln 10 k_B T e} \left(SVS - SVS_{IDEAL} \right)
 \end{aligned} \tag{6.6}$$

As it is difficult to determine the depletion layer capacitance, the usual approach for radiation studies is to evaluate the change in the density of interface traps with regards to the unirradiated state. This is done by subtraction of eq. 6.6 from itself after different irradiation steps

$$\Delta D_{IT} = D_{IT}^i - D_{IT}^0 = \underbrace{\frac{C_{OX}}{\ln 10 k_B T e}}_k \left(\underbrace{SVS^i - SVS^0}_{\Delta SVS} \right) = k \cdot \Delta SVS. \tag{6.7}$$

Index i represents the state after the i^{th} irradiation state, and 0 the unirradiated state. Now, only the sheet capacitance of the SiO_2 layer remains. The conversion factor k , between the density of interface traps and the subthreshold voltage swing, is evaluated at $4.88 \cdot 10^{12} \text{ V}^{-1} \text{ eV}^{-1} \text{ cm}^{-2}$.

In Fig. 6.16 all measured subthreshold voltage swing results for gate and CG structures are presented. The data is collected from radiation studies performed on the W09 TL 80k1, W11 TR 80k1 and W12 TL 80k1 SPDs. As shown in sec. 5.2.1.3, gate length does not play a major role in the response. Consequently, all pixels from a single SPD are evaluated together. The evaluation is done through the means of linear interpolation. Numerical results of the interpolation are gathered in Tab. 6.4. Additionally, all data points were interpolated together as well. This common interpolation is used as a basis for the right hand side axis in Fig. 6.16. The intercept value of the interpolation is the basis for the zeroth value of the new axis. In average for the three SPDs, the density of interface traps in the gate region increases by $(1.43 \pm 0.01) \cdot 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ for every 1 Mrad of dose. For the CG structure the average increase in density of interface trap states is $(5.5 \pm 1.3) \%$ higher than that of the gate structure.

⁶Defined per unit area.

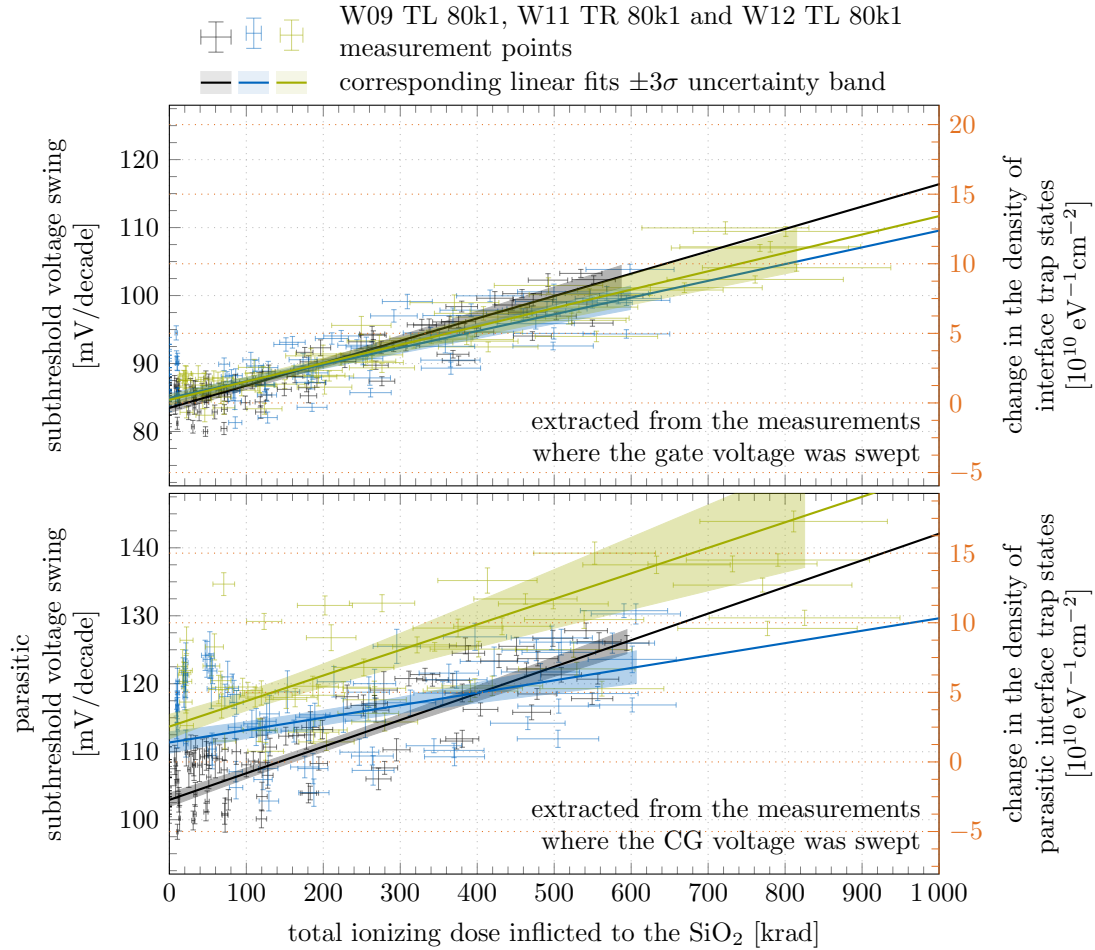


Figure 6.16: Measured subthreshold voltage swings in dependence of the total ionizing dose inflicted to the SiO_2 of both the gate and CG structures. Datasets from three irradiated SPDs with corresponding linear interpolations and uncertainty bands are plotted. Numerical results of those interpolations are gathered in Tab. 6.4. Additionally, the right hand side axis is showing the change in density of interface trap states caused by the incoming radiation. The zero of this scale is matched with the overall linear interpolation of all SPD together.

Table 6.4: Numerical collection of results presented in Fig. 6.16.

	gate sweeps		clear gate sweeps	
	intercept	slope	intercept	slope
	$\left[\frac{\text{mV}}{\text{dec}}\right]$	$\left[\frac{\text{mV/dec}}{\text{Mrad}}\right]$	$\left[\frac{\text{mV}}{\text{dec}}\right]$	$\left[\frac{\text{mV/dec}}{\text{Mrad}}\right]$
W09 TL 80k1	83.5 ± 0.2	33 ± 1	103.0 ± 0.3	39 ± 1
W11 TR 80k1	85.0 ± 0.3	25 ± 1	111.4 ± 0.5	18 ± 2
W12 TL 80k1	84.6 ± 0.3	27 ± 1	113.7 ± 0.6	38 ± 3
all together	84.2 ± 0.5	29.3 ± 0.2	108.5 ± 0.1	30.9 ± 0.3

6.6 Increase of the lifetime

Even after the threshold voltage shifts become too large to operate the sensor with sufficient quality, it is possible to repair it to a certain degree. Initial studies on this point were performed in refs. [163, 184]. It was shown that the efficient removal of SiO₂/Si interface trapped holes is possible with heating of the sensor to the temperatures higher than 250 °C. However, in case of the EDET DH80k DePFETs this is not possible, as those temperatures would cause problems with soldered components on the edges of the main devices. Nonetheless, the EDET collaboration is working on the focused high power laser annealing. That way, a high temperature is achieved on a small localized part of the sensor, while the remaining part of the sensor is thermally stable at low temperatures. The process is then repeated in scanning fashion over the complete sensitive area.

The system is still in developmental stages and was consequently not included in this work. It will, however, be investigated and developed further afterwards. The plan is to have the complete system included in the transmission electron microscope (tEM) chamber behind the sensor. That way, the sensor can be annealed on a regular over-the-night basis, when the experiment is not running. This should lead to significant simplifications in the operation, as the vacuum of the tEM will not have to be broken on a regular basis for the exchange and annealing of the sensors.

7 Summary

The EDET collaboration is developing a novel DePFET based camera system to achieve real-time real-space imaging of fast dynamic processes with transmission electron microscopy (TEM). The camera system uses a combination of technologies that were never before used all together. Some of the most remarkable achievements are:

- The ability to record movies with a 1 Mpixel array at a peak full-frame readout frequency of 80 kHz.
- The ability to detect incident high-energy electrons over the sensitive area of $3\text{ cm} \times 3\text{ cm}$ which is back-thinned to only $30\text{ }\mu\text{m}$ and integrated together with the frontend electronics on a single all silicon module.
- The ability to store the generated signal charges of a minimum of 100 incident electrons hitting each pixel with the energy of 300 keV. This is necessary in order to have the capability to image biological samples that are inherently of low contrast due to their low atomic number composition.
- The ability to compress the response signal in order to have a higher charge amplification for up to the first 10^5 stored signal charges, and a lower charge amplification for any further stored signal charges.

In order to fully understand how this novel combination of technologies, joined on a DePFET pixel level, functions, it is necessary to gain an in-depth understanding of the sensor's behaviour. This is done through multiple sets of characterization measurements.

The sensitivity to radiation damage is one of the most important predicaments of silicon sensors operating in the TEM environment. The radiation damage presents itself in the form of trapped positive charges that accumulate in the silicon oxide (SiO_2) layers close to the surface of silicon. When the charges are trapped in the SiO_2 below the DePFET's polycrystalline-silicon (poly-Si) structures, they modify the potential distribution in their vicinity and effectively alter the transistor transfer characteristics and operational parameter space. One way to minimize the accumulation of trapped charges is through the minimization of the electric field in the SiO_2 layers. The lower the electric field, the higher the probability for recombination of generated electron/hole pairs before they get separated and trapped. For a vast majority of time during the electron irradiation, both DePFET's poly-Si structures are biased in their OFF states, i.e., at voltages slightly higher than the threshold voltages. If the applied voltages are close to the source voltage, the electric field is minimized. A set of quasi-static characterization measurements elucidates that the threshold voltages of EDET DH80k DePFET transistors are, depending on the gate length, a few hundred mV below the source potential. This result illustrates a successful conclusion of the device simulations,

that were performed prior to the beginning of the manufacturing process, which should in turn offer an optimized response to radiation damage.

Sensors intended for TEM need to be thin to minimize the problem of electron multiple scattering. However, this in turn elevates the risk of thermo–mechanical stress which can in turn cause irreparable damage to sensors. Therefore, in the scope of EDET DH80k project special care has to be taken for devices built on silicon-on-insulator (SOI) wafers, that are thinned to a minimum thickness of 30 μm . This is especially critical for the main devices intended for the final EDET DH80k camera system that feature a 3 cm \times 3 cm big thinned area. Thermo–mechanical stress can be caused by the DePFET’s parasitic current path and its global current draw in the transistor OFF state. Through the measurements it was shown that the parasitic current path is suppressed if the clear gate structure is biased above -1 V. The current draw of a single pixel in the OFF state was measured to be of the order of 50 pA. This yields only 0.26 mW for the complete EDET DH80k camera system when in OFF state, i.e., collection mode, and confirms the DePFET to be a low power device. Therefore, through proper biasing the EDET DH80k devices should allow smooth operation.

Prior to production, the EDET DH80k DePFET pixel design and its implantation parameters were extensively simulated. The quasi–static characterization measurements performed on single pixel devices revealed a good match between measured and simulated values, e.g., the empty internal gate potential was measured at the level of 5 V which is very close to the simulated 6 V. However, the measurements also revealed a small discrepancy between devices from standard and SOI wafers. In order to manufacture devices on SOI wafers, as opposed to the standard ones, additional steps at external contractors are necessary. Consequently, a comparison between the two is called for. The SOI devices exhibited spreads in the measured threshold voltage distribution almost twice the size of those from standard wafers. Additionally, they indicated a potential position dependent variation in the threshold voltage, more pixels, with regards to pixels from standard wafers, featured earlier onsets of the parasitic current paths, and a higher number of pixels was in general non–functional. Consequently, additional future investigations of DePFET pixels from SOI wafer are needed in order to optimize the manufacturing process.

Quasi–static characterization measurements are essential to learn about the fundamental DePFET transistor parameters and for insights about the uniformity of production process. However, in the final experiment the EDET DH80k camera system will be operated in the dynamic mode. Therefore, the next important step is understanding the DePFET behaviour in this mode of operation. The final system is highly specialized to record extremely fast bursts of images from big arrays of pixels. However, the goal of this work is to have a detailed look into the response of single pixels under different operating conditions. For this reason, a single pixel measurement system, which features extreme modularity and offers a high degree of precision, was developed in the scope of this work. With it multiple pixels from three different prototyping matrices (PMATs) from SOI wafers were tested and evaluated. Those PMATs feature two different pixel designs and two different thicknesses, i.e., 30 μm and 50 μm . The results show that the design implemented on the main devices, meant for the final EDET DH80k camera sys-

tem, exhibits superior performance across the two designs, and that the thickness has virtually no impact on the DePFET's operational parameter space and response. The evaluation was based on the variation of different DePFET operational parameters. The most important operational parameters are the voltages applied to the DePFET's clear gate structure (U_{CG}), clear implantation (U_C^{OFF})¹, punch-through implantation (U_{PT}) and drift implantation (U_{DRI}). As the four-dimensional operation parameter space is too vast to be fully evaluated in a single measurement scan, it was split in two separate scans where only two operational parameters were varied and the rest were kept constant. The (U_{CG} , U_C^{OFF}) domain of operational parameters controls the response of a DePFET transistor the most, as their corresponding structures are the closest to the channel and charge collection areas. Together they define a so-called DePFET operation window. The (U_{PT} , U_{DRI}) domain of operational parameters has the most influence over the potential distribution in the silicon bulk. Through it they control the charge collection efficiency of the charges generated in the silicon bulk. From the two measurement scans, performed in both operational parameter domains, three operational points per scan were determined as candidates for the optimal point of operation. In a union of those nine operation points a final evaluation of the performance was carried out. The comparison of the performance was conducted through the parametrization of the recorded spectra of the radioactive isotope iron-55 (^{55}Fe) and through the parametrization of the response function, measured over the complete dynamic range of the charge storage regions. The parameters that were compared, i.e., response parameters, are the equivalent noise charge values, ^{55}Fe K_α and K_β full width half maximum values, leakage current values, charge amplification factors of both storage regions, kink position values, and the maximum charge handling capacity values. The result was that in all compared optimal points, only the U_{CG} could potentially hinder the performance of sensors in the scope of the EDET DH80k project. The remaining operational parameters cause no significant differences between compared response parameters measured in the optimal points. The U_{CG} controls the potential below the clear gate structure. Two effects depend on this potential and consequently limit the U_{CG} parameter space. In the negative direction the U_{CG} is limited with the onset of DePFET's parasitic current paths between source and drain implantations. In the positive it first increases the probability for electrons in charge storage regions to overcome the clear gate potential barrier and move to clear implantation, until it eventually becomes so positive that it causes the back-emission of electrons from the clear implantation to the charge storage regions. The distance between the limiting values for those two effects defines the clear gate operation window. Its size is directly correlated with the amount of radiation damage the DePFETs can sustain, as the accumulation of positive charges in the SiO_2 layers below the clear gate structure essentially change the potential below it. The maximum size of the clear gate operation window was evaluated to be on the level of 3 V for the PMATs featuring the design C. The maximum charge handling capacity of a DePFET depends heavily on the U_{CG} . At the most negative U_{CG} it is higher than 2Me^- , without regards

¹There also exists a U_C^{ON} voltage which is applied to the clear implantation for the on-demand removal of charges collected in charge storage regions.

7 Summary

to other three voltages inside the scope of optimized points. However, by increasing the U_{CG} the maximum charge handling capacity can drop significantly. Shortly before entering the back-emission region, at the operational parameter settings where the clear gate operation window is maximized, it can even drop below the EDET DH80k limiting case of 800 ke^- . This leads to the conclusion that the radiation damage will influence conditions in each pixel, as the variation of U_{CG} essentially simulates radiation damage.

The other significant response parameters for the EDET DH80k project are the charge gain factors of both charge storage regions. They were measured to be stable over all nine optimal points and of the order of 280 pA/e^- for the internal gate charge amplification factor and 80 pA/e^- for the overflow charge amplification factor. This yields a 70 % signal compression between amplification of charges collected in the two charge storage regions.

Energetic electrons cause radiation damage to DePFET sensors. The accumulation of charges in SiO_2 layers below poly-Si structures causes shifts of the threshold voltages to more positive values. If the threshold voltage shifts (ΔU_T) are homogeneous over all pixels, their contribution can be compensated by correcting the voltages applied to the poly-Si structures. However, the problems arise from two causes. The first is the intrinsic variation in dimensions of poly-Si structures, and the second is the inhomogeneous radiation. Both cause inhomogeneous ΔU_T across DePFET pixels. To investigate the direct impact of radiation damage, a radiation campaign with 55 keV electrons was carried out in the scope of this work. Three single pixel devices from both wafer types were irradiated to the dose of almost 1 Mrad . The results are the ΔU_T rates in the range of 2 V/Mrad to 7 V/Mrad , depending on the gate length, wafer type and poly-Si structure. In general, longer gate lengths always accumulated bigger ΔU_T , and the single pixel device built on a SOI wafer also exhibited bigger ΔU_T as opposed to the two single pixel devices from standard wafers. A simulation of the changes in DePFET offset currents was performed with obtained results of the ΔU_T rates. It showed that the longer gate lengths are preferred, as long as radiation is homogeneous over all pixels. This is because the one standard deviation of the intrinsic variation in dimensions of poly-Si structures is measured to be 40 nm , regardless of the mean value. Consequently, the initial offset current distribution is narrower and it also widens more slowly, despite bigger ΔU_T rates. However, the same simulation showed that the shorter gate lengths would be favourable in case of inhomogeneous radiation with at least 5 % gradient. Operating under the condition that the TEM imaging of dynamic processes should, on average, cause homogeneous radiation damage to the sensors, the final experiment will include EDET DH80k devices with $6 \mu\text{m}$ long gate lengths, i.e., longer gate lengths. The extrapolation of observed and simulated behaviours of radiation damage effects leads to the conclusion, that the EDET DH80k devices should perform sufficiently well to the total ionizing dose of at least 5 Mrad . However, this life expectancy should be prolonged through the means of laser annealing. The laser annealing system is already under development and should eventually be integrated under the EDET DH80k camera system. That way, the annealing could be performed whenever the system will not be in use. Additionally, the following EDET production run features different thicknesses of dielectric layers, which should in turn decrease the ΔU_T and prolong a life expectancy.

Both the laser annealing system and the optimized dielectric layers will be the subject of future studies.

8 Conclusion

In the scope of this work comprehensive quasi-static characterizations were conducted on the EDET DH80k single pixel DePFET structures. Those characterizations offer insights into fundamental DePFET parameters, such as threshold voltage and empty internal gate potential, and are therefore a key tool to determine the sensor quality for a given application. The main results confirmed the success of the production as the evaluated values matched those that were previously only simulated in specialized software. However, they also indicated a possible positional dependency of parameters on silicon-on-insulator (SOI) wafers. Consequently, the devices built on SOI wafers should be studied further since such variances have a direct influence over the response homogeneity of big area devices with several thousands of interconnected pixels.

An in-depth understanding of the DePFET's response in a dynamic mode of operation is necessary to ensure optimal behaviour within the scope of a given project. However, the final EDET DH80k camera system is highly specialized to record extremely fast bursts of images from big arrays of pixels and is consequently not suitable for this task. Therefore, in the frame of this work a highly modular single pixel measurement system was developed and used to extensively study different designs of the EDET DH80k DePFET pixels. The studies were performed in a multi-parameter space where the DePFET's response was carefully tracked in order to identify an optimal operation window. Five biasing voltages were identified to have the most impact over the response. Inside the optimal operation window the DePFET's response is as expected from software simulations, whereas outside of it different processes hinder the performance, i.e., e^- back-emission to the silicon bulk, parasitic transistor channel under the clear gate structure and signal charge losses to the clear implantation. It was concluded that the operation window is large enough to operate the big area devices and that the design which is implemented on them is in fact the best available at this point. Additionally, the most critical parameter was found to be the biasing voltage applied to the DePFET's clear gate structure. It is the only one that severely impacts the DePFET's properties, i.e., charge storage capacity, by changes inside the optimal operation window. Over the complete clear gate operation window the EDET DH80k DePFET's charge storage capacity changes from more than 2.3 Me^- on one end, to slightly below 800 ke^- on the other. In the final experiment it will therefore be imperative to avoid injecting more signal charges into the sensor than the worst DePFET pixel will be able to store at a given set of parameters. The optimal biasing conditions provided in this work will serve as starting operation points for the final EDET DH80k camera system. From them a cross-section of operation windows for all interconnected pixels from big area devices will have to be derived.

8 Conclusion

For a complete characterization it is also necessary to address the radiation damage that energetic electrons cause in DePFETs. The damage expresses itself in a form of a positive charge build-up in the silicon oxide layers below the DePFET's polycrystalline-silicon structures, i.e., gate and clear gate structures. Essentially this shifts the corresponding transistor threshold voltages to more positive values. Therefore, it would be beneficial to operate the EDET DH80k camera system at a point where the operation window is maximized. By combining the findings presented in this thesis it was possible to conclude that since only the clear gate biasing voltage significantly impacts the DePFET's behaviour, the remaining parameters can be adjusted so that the clear gate operation window is maximized. Operating the final EDET DH80k camera system at that point should extend its lifetime in the final experiment.

To further assess the impact of radiation damage a radiation campaign was performed within the scope of this work. The EDET DH80k single pixel DePFET structures, featuring three different design gate lengths, were irradiated with 55 keV e^- to a maximum of 1 Mrad of the total ionizing dose. The results showed that the rate of the radiation damage depends on the gate length and that the shorter gate lengths generally incur damage at slower rates. Those results were used in a simulation study to evaluate and extrapolate the levels of radiation damage that the EDET DH80k devices could sustain in the final experiment. The simulation study was based on the changes that the radiation damage causes to the DePFET's offset current, which directly impacts the DePFET's signal charge amplification. It included the inherent manufacturing variations of the produced DePFET gate lengths and also the different distributions of dose profiles. The outcome highlighted that the DePFETs with longer design gate lengths are to be preferred in case of a homogeneous dose profile, despite incurring higher threshold voltage shifts. This is because the offset current distribution of multi-thousand pixels with longer design gate lengths changes more homogeneously than that of the ones with shorter design gate lengths. The more homogeneous the change, the easier it is to correct it with global biasing voltages applied to the affected structures. As the homogeneous e^- irradiation is expected in the dynamic transmission electron microscopy, the big area devices feature DePFETs with longer design gate lengths. They should be able to sustain a minimum of 5 Mrad of radiation damage.

The radiation campaign and a corresponding simulation study showed two additional important results. First, because of the offset current distribution changes that arise from radiation damage, calibrations of the DePFET response curves will be necessary on a regular basis. Secondly, the measured rates of radiation damage are worse than those anticipated from the preliminary studies performed in the scope of M. Hensel's master thesis [184]. This illustrates the importance of additional components in the final EDET DH80k camera system that have to be implemented in the transmission electron microscope's vacuum chamber. On one hand, a system for non-damaging response curve calibration is necessary, and on the other the inclusion of a laser annealing system would be beneficial to mitigate part of the radiation damage problem and also to prolong the camera's life span. Both such systems are currently under development.

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A Rudimentary scaling

In order to do a rudimentary comparison of pixel storage capacities between different designs one has to correct for different dimensions. The Fig. A.1 shows and explains all the relevant parameters that will be used for scaling. By keeping the DePFET biasing conditions equal over different devices the most relevant scaling factors in terms of pixel storage capacities are the areas covered by the IG region and overflow region.

In order to calculate those the first thing that needs to be performed is the translation from the design values (L, W, L_{OF}) to the produced values (L', W', L'_{OF}). The difference between those values arises from the etching of poly-Si structures. In case of the PXD-10 production run all wafers were plasma etched [166] which results in the mean difference (δ) of $0.6 \mu\text{m}$ [113, 162]. The translation for the three design parameters is therefore as following:

$$\begin{aligned} L' &= L - \delta, \\ W' &= W + \delta, \\ L'_{OF} &= L_{OF} + \delta/2. \end{aligned}$$

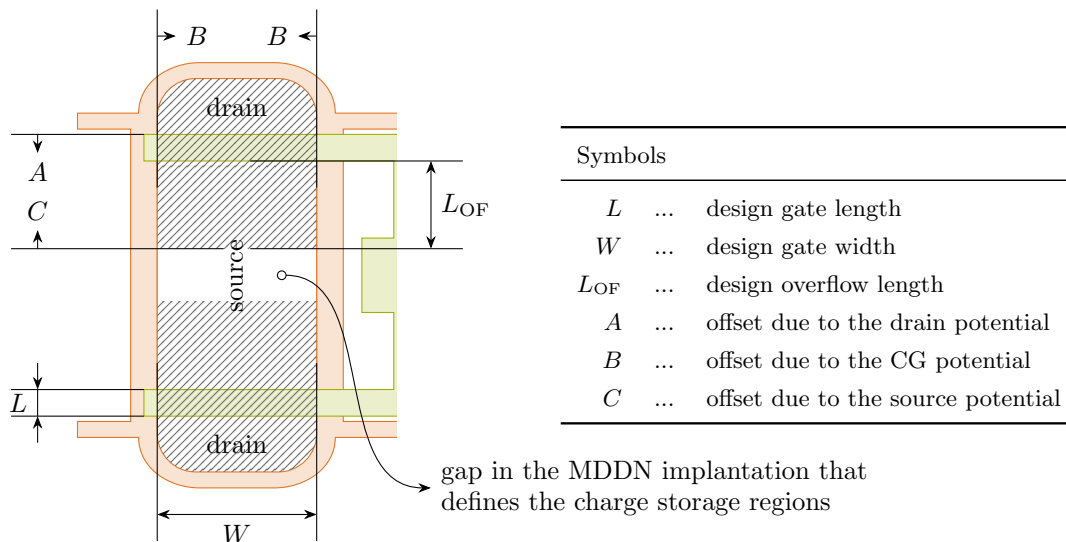


Figure A.1: The EDET DH80k pixel design with added symbols that are necessary to perform the rudimentary scaling procedure between different dimensions. Tilted stripes denote the MDDN implantations that define the charge storage regions.

A Rudimentary scaling

The design gate length decreases due to the second layer poly-Si etching, and the design gate width increases due to the first layer poly-Si etching. The second layer poly-Si etching also influences the design overflow length, but only on one relevant side.

The second thing is to correct the scaling due to the repelling potentials¹ for e^- from the neighbouring regions; the drain (A), the CG (B) and the source (C). The drain and source regions are formed from the p^+ -type implantations which are repelling e^- in the depleted volumes on their borders. In addition, one must also include the applied voltages. Consequently, the drain region is pushing e^- further away than the source region. The repelling from the CG side is because the potential caused by the voltage applied to the CG is more negative than the potential in the charge storage regions. The estimated values from the A , B and C parameters are respectively $2\ \mu\text{m}$, $1\ \mu\text{m}$ and $0.5\ \mu\text{m}$ [113].

The IG area (A_{IG}) and overflow area (A_{OF}) can now be calculated as

$$\begin{aligned} A_{\text{IG}} &= (L' - A)(W' - 2B) \quad \text{and} \\ A_{\text{OF}} &= (L'_{\text{OF}} - C)(W' - 2B) . \end{aligned}$$

From here the scaling factors between two different designs, e.g., SPD and dimensions used in the simulations, are

$$\begin{aligned} f_{\text{IG}} &= A_{\text{IG}}^{\text{SIMUL}} / A_{\text{IG}}^{\text{SPD}} \quad \text{and} \\ f_{\text{OF}} &= A_{\text{OF}}^{\text{SIMUL}} / A_{\text{OF}}^{\text{SPD}} , \end{aligned}$$

which are used to calculate the scaled storage capacities as

$$\begin{aligned} Q_{\text{IG}}^{\text{SPD, scaled}} &= f_{\text{IG}} Q_{\text{IG}}^{\text{SPD}} \quad \text{and} \\ Q_{\text{OF}}^{\text{SPD, scaled}} &= f_{\text{OF}} Q_{\text{OF}}^{\text{SPD}} . \end{aligned}$$

The maximum scaled storage capacity is then

$$Q_{\text{MAX}}^{\text{SPD, scaled}} = Q_{\text{IG}}^{\text{SPD, scaled}} + Q_{\text{OF}}^{\text{SPD, scaled}} .$$

¹In this case the comparison is done to the potential of the charge storage regions.

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Acronyms

4200-SMU	Keithley's 4200 Source-Measure Unit
4200A-SCS	Keithley's 4200A-SCS Parameter Analyzer
707B	Keithley's 707B 6 slot switching matrix mainframe
7174A	Keithley's 7174A switching matrix card
ADC	analogue-to-digital converter
ASIC	application-specific integrated circuit
ASM	all silicon module
CCD	charge coupled device
CDF	cumulative distribution function
CDS	correlated double sampling
CE	cutting edge
CG	clear gate
CMC	common mode correction algorithm
CMOS	complementary metal-oxide-semiconductor
cPCIe	CompactPCI Express connector
customPCMS	custom built pre-characterization measurement system
DCD	drain current digitizer
DePFET	depleted p-channel field effect transistor
DMC	DePFET movie chip
DR	depleted region
DROB	discrete drain current readout board
e^-	electron
e^-/h^+ pair	electron/hole pair
cryo-EM	electron cryo-microscopy
ELR	linear extrapolation method in the linear operation region
EM	electron microscope
ENC	equivalent noise charge
ESA	European Space Agency
ESR	linear extrapolation method in the saturation operation region

Acronyms

FC	faraday cup
⁵⁵ Fe	radioactive isotope iron-55
film	photographic emulsion
FOM	figure of merit
FPGA	field programmable gate array
FWHM	full width at half maximum
generalPCMS	general purpose pre-characterization measurement system
h ⁺	hole
HDSN	high-dose shallow n implantation
HDSP1	high-dose shallow p implantation
HDSP2	high-dose shallow p implantation
HLL MPG	Semiconductor Laboratory of the Max Planck Society
IG	internal gate
IML	inter module link
IP	imaging plate
IQR	interquartile range
LDSP	low-dose shallow p implantation
LED	light-emitting diode
⁵⁵ Mn	stable isotope manganese-55
MDDN	medium-dose deep n implantation
MIC	module interface circuitry
MOSFET	metal-oxide-semiconductor field effect transistor
MPSD	Max Planck Institute for the Structure and Dynamics of Matter
OF	overflow region
OF1	overflow 1
OF2	overflow 2
OpAMP	operational amplifier
PA200N	SÜSS's PA200N semiautomatic probe station
PCB	printed circuit board
PMAT	prototyping matrix
poly-Si	polycrystalline-silicon
PSU	power supply unit

PT	punch-through
QN	quantum number
Si	silicon
Si ₃ N ₄	silicon nitride
SiO ₂	silicon oxide
SOI	silicon-on-insulator
SPD	single pixel device
SPIX	single pixel measurement system
SS	single sampling
SVS	subthreshold voltage swing
TEM	transmission electron microscopy
tEM	transmission electron microscope

Symbols

$1/f$	low-frequency voltage noise
A	atomic mass number
$\langle -dE/dx \rangle$	average energy loss per unit path
$d\sigma_{el}/d\Omega$	differential cross-section for elastic electron-nucleus scattering
$d\sigma_r/d\Omega$	Rutherford differential cross-section for elastic electron-nucleus scattering
$d\sigma_{in}/d\Omega$	differential cross-section for inelastic scattering
I_D	drain current
I_L	leakage current
I_{OFFS}	offset current is a DePFET drain current when the charge storage regions are completely empty
I_{SIG}	signal current is a DePFET drain current from which the I_{OFFS} is subtracted
NA	numerical aperture is the property of the microscope's lens
PV	peak-to-valley ratio
Q_{MAX}	maximum charge that can be stored in the charge storage regions of the DePFET pixel
Q_{SIG}	signal charge that is stored in the charge storage regions of the DePFET pixel
U_B	bulk voltage, measured with respect to the U_S , that is applied to the Si bulk
U_{CG}	clear gate voltage measured with respect to the U_S
U_{CG}^{ON}	clear gate voltage, measured with respect to the U_S , that is applied during the clear process in order to reduce the potential barrier between the charge storage regions and the clear implantation

Symbols

U_{CG}^{OFF}	clear gate voltage, measured with respect to the U_S , that is applied between clearing processes
U_C	clear voltage measured with respect to the U_S
U_C^{ON}	clear voltage, measured with respect to the U_S , that is applied during the clear process
U_C^{OFF}	clear voltage, measured with respect to the U_S , that is applied between clearing processes
U_C^{ALL}	clear voltage, measured with respect to the U_S , that is applied to the statically biased part of the array
U_{CE}	cutting edge voltage, measured with respect to the U_S , applied to prevent collection of electrons generated beyond the edges of the radiation sensitive array
U_D	drain voltage measured with respect to the U_S
U_{DRI}	drift voltage, measured with respect to the U_S , that generates a lateral drift field which pushes electrons towards the charge storage regions
U_{FB}	flat-band potential is a potential at which there is no bending of energy bands at the Si/SiO ₂ transition
U_G	gate voltage measured with respect to the U_S
U_G^{ON}	gate voltage, measured with respect to the U_S , at which the transistor channel conducts the current
U_G^{OFF}	gate voltage, measured with respect to the U_S , at which the transistor channel does not conduct the current
U_G^{ALL}	gate voltage, measured with respect to the U_S , that is applied to the statically biased part of the array
U_{IG}	potential of the IG region in the DePFET pixel
$U_{T, CG}$	parasitic threshold voltage, measured with respect to the U_S , is a voltage at which the surface of Si below the CG structure changes between depletion and inversion modes
U_{PT}	punch-through voltage, measured with respect to the U_S , that is applied to deplete the Si bulk through the punch-through mechanism
U_S	source voltage
U_{SUB}	subtraction voltage is used for the subtraction of the DePFET offset current
U_T	threshold voltage, measured with respect to the U_S , is a voltage at which the surface of Si below the gate structure changes between depletion and inversion modes
ΔU_T	change of the U_T due to the positive charge build-up in the SiO ₂

Z atomic number

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