Technische Universität München

Fakultät für Maschinenwesen

Lehrstuhl für Fahrzeugtechnik

Improving the Partial Load Efficiency of Electric Powertrains by Silicon MOSFET Multilevel Inverters

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Vollständiger Abdruck der von der Fakultät für Maschinenwesen der Technischen Universität München zur Erlangung des akademischen Grades eines

Doktor-Ingenieurs

genehmigten Dissertation.

Vorsitzender:	Prof. Dr.-Ing. Nikolaus A. Adams
Prüfer der Dissertation:	1. Prof. Dr.-Ing. Markus Lienkamp
	2. Prof. Dr.-Ing. Dieter Gerling

Die Dissertation wurde am 30.07.2019 bei der Technischen Universität München eingereicht und durch die Fakultät für Maschinenwesen am 27.11.2019 angenommen

We will make electricity so cheap that only the rich will burn candles.

There is no substitute for hard work.

Thomas A. Edison

Acknowledgement

This dissertation and relevant studies were conducted during my time as a research associate in TUMCREATE, Singapore, and a Ph.D. candidate in the Institute of Automotive Technology (FTM), Technical University of Munich (TUM), Germany. This dissertation is funded by the National Research Foundation (NRF) of Singapore, under its Campus for Research Excellence And Technological Enterprise (CREATE) program. Therefore, first, I would like to show my gratitude to the organizations above. Without the support of these organizations, the studies in this dissertation could not be conducted.

Besides, I would also like to acknowledge the supports I received from the individuals. These supports have guided me through the difficulties I encountered during my research.

First, I am indeed grateful for the supervision and the trust I received from Prof. Dr.-Ing. Markus Lienkamp. In the beginning of 2015, although I could not speak a single word of German and had little knowledge about what to expect in a German university, Prof. Lienkamp still trusted me and gave me a chance of interview. Since then, my dream career toward electric and smart vehicles was finally started. During the doctoral research, Prof. Lienkamp has given me the freedom to search for my own topic, and always stayed supportive. In meetings, his feedbacks have always been sharp and constructive. I am particularly thankful that Prof. Lienkamp has also taken patience to polish my logic reasoning and presentation skills. Before these direct and indirect trainings, I would not be confident to handle the tasks I will encounter in the future.

Second, I would like to express my gratitude to the colleagues I met in Singapore and in Munich. The teams were one of the highlights during my Ph.D. period. Particularly, I would like to thank Mr. Felix Roemer, who is working on the same circuit and has supported me through the difficulties I encountered in the research. I have learned much from his maturity of handling tasks and his hands-on skills.

I would like to thank Mr. Aditya Pathak and Mr. Olaf Teichert as well, for their support during research, the effort to review my dissertation and the valuable feedbacks. Many thanks to Dr. Olga Ilina and Dr. Leon Voss from ANSYS, who have helped to validate all my results. Sincere thanks also go to Dr. Philip Wacker, Dr. Matthias Kerler and Mr. Jörn Adermann, who helped me to kick-start my topic, offered great help during the research, and later provided valuable suggestions regarding my career.

In addition, I wish to acknowledge the great help I received from Dr. Aybike Ongel, my direct supervisor in Singapore, for trusting me and supporting me in my research and projects. I also wish to acknowledge the help I received from Mr. Raymond Khoo, Mr. Ganesh Sethuraman, Mr. Manfred Kloeppel, Mr. Benedikt Jaeger and Mr. Alexander Koch. It has been a major pleasure to work together with you designing the next generation of public transport for Singapore.

In terms of personal life, I would like to thank my girlfriend Ms. Jiajie Cheng for supporting my decision pursuing a Ph.D. and helping me emotionally when I was struggling. We have been in

distant relationship for more than five years, because of our career endeavors. I hope the completion of my Ph.D. could bring this difficult time to an end.

I also wish to acknowledge that the friendship with Mr. Jiangyuan Li and Mr. Xuesong Li has always helped me and encouraged me to go further in this path full of challenges. It is so lucky that we knew each other in our early age, encountered a similar life, and supported each other like a family.

I would sincerely thank my parents for loving me and supporting me in all the aspects. You have given me the best help you could, and supported all the decisions I have made in terms of career and personal life.

Finally, I would like to express my gratitude to all the individuals and organizations, whom I have failed to cover in this short acknowledgement.

Singapore, May 2019

Fengqi Chang

Table of Contents

Abbreviations

AC	Alternating Current
ASM	Asynchronous Motor
BEV	Battery Electric Vehicle
CC-CV	Constant Current - Constant Voltage
CHB	Cascaded H-Bridges
CPLD	Complex Programmable Logic Device
CTE	Coefficient of Thermal Expansion
DAC	Digital Analog Converter
DC	Direct Current
DOD	Depth of Discharge
ECM	Equivalent Circuit Model
EDLC	Equivalent Double Layer Capacitor
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EV	Electric Vehicle
HVAC	Heating, Ventilation and Air Conditioning
IC	Integrated Circuit
ICEV	Internal Combustion Engine Vehicle
IGBT	Insulated Gate Bipolar Transistor
IPM	Interior Permanent Magnet
MCU	Micro Control Unit
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MTBF	Mean Time Between Failures
NMC	Nickel Manganese Cobalt
NPC	Neutral Point Clamped
OCV	Open Circuit Voltage
OEM	Original Equipment Manufacturer
opamp	Operational Amplifier
PCB	Printed Circuit Board

PHEV	Plug-in Hybrid Electric Vehicle
PSC-PWM	Phase Shifted Carrier PWM
PSM	Permanent-magnet Synchronous Motor
PWM	Pulse Width Modulation
RMS	Root Mean Square
Si	Silicon
SiC	Silicon Carbide
SOC	State of Charge
SRM	Switched Reluctance Motor
THD	Total Harmonic Distortion
TI	Texas Instrument
USD	United States Dollar
WBG	Wide Band Gap

Symbols

Symbol	Unit	Description
α	-	Coefficient of the die attachment reliability model
α_{cap}	USD	Fixed cost of the DC-link capacitor
α_{Ccap}	USD/F	Unit cost of the DC-link capacitor per farad
α_{copper}	1/K	The coefficient of thermal expansion of copper
α_{solder}	1/K	The coefficient of thermal expansion of solder
α_{T}	-	The temperature coefficient of capacitor reliability model
α_{V}	-	The voltage coefficient of capacitor reliability model
α_{Vcap}	USD/V	Unit cost of the DC-link capacitor per voltage
β_1,β_2,β_3	-	Regressed coefficients to calculate the iron loss
$\Delta\gamma$	-	Relative deformation of a solder joint due to temperature
θ	rad	The phase lag of the AC current
$\Delta\eta$	%	Inverter efficiency improvement compared to the benchmark
$\Delta\eta_{\mathrm{sys}}$	%	System efficiency improvement compared to the benchmark
$\Delta\eta_{\mathrm{BM}}$	%	Combined efficiency change of the motor and batteries
$\eta_{\mathrm{inv\_ave}}$	%	Average efficiency of the inverter
ρ_{L}	kg/m^3	Density of the air
a	m/s^2	Vehicle acceleration
$a_{\mathrm{Vibration}}$	m/s^2	Acceleration of the mechanical vibration
A_{A}	m^2	Cross section area of the vehicle
A_{Die}	mm^2	Size of the die in the switch
A_1,A_2	-	Coefficients of the die attachment reliability model
a_{Diode}	-	Coefficient to calculate the diode switching loss
a_{IGBT}	-	Coefficient to calculate the IGBT switching loss
a_{SiC}	-	Coefficient to calculate the SiC MOSFET switching loss
b_{Diode}	-	Coefficient to calculate the diode switching loss

b_{IGBT}	-	Coefficient to calculate the IGBT switching loss
b_{SiC}	-	Coefficient to calculate the SiC MOSFET switching loss
$b_{100\mathrm{km.el}}$	kWh/100 km	Energy consumption of the vehicle per 100 km
$\cos\theta$	-	Power factor of the inverter
c	-	Index to calculate the cycle life of a PCB solder joint
c_{bat}	USD/kWh	Unit price of the batter per capacity
c_{CPLD}	USD	Unit cost of the CPLD
$c_{\mathrm{concactor}}$	USD	Unit cost of the contactor
c_{Die}	USD/mm^2	Unit cost of the die
c_{FBR}	USD	Unit cost of one set of fiber optic communication
$c_{\mathrm{fix\_HS}}$	USD	Fixed cost of the heatsink
$c_{\mathrm{V\_HS}}$	USD/m^3	Unit cost of the heatsink per volume
c_{W}	-	Air drag coefficient of the vehicle
C_{DC}	F	Rated capacitance of the DC-link capacitor
$C_{\mathrm{Dth(j-c)}}$	K/J	Thermal capacitance between diode junction and casing
$C_{\mathrm{Tth(j-c)}}$	K/J	Thermal capacitance between transistor junction and casing
C_{cap}	USD	Total cost of one DC-link capacitor
C_{CMCU}	USD	Cost of the central micro control unit of inverters
C_{HS}	USD	Total cost of the heatsinks
C_{IC}	USD	Total cost of the ICs
C_{inv}	USD	Total capital cost of the inverter
C_{Package}	USD	Cost of the switch package
C_{Switch}	USD	Total cost of one switch
C_{sys}	USD	System cost of the inverter solution
ΔC_{sys}	USD	Change of the system cost compared to benchmark
D_{Bond}	m	Diameter of the bond wire
D_{PCB}	m	Deformation of the PCB in vibration
ΔE	kWh/100 km	Energy consumption reduction per 100 km
E_{cycle}	Wh	Energy consumption in one driving cycle
f_{cycle}	Hz	The frequency of the stress cycle for reliability simulation
f_{nPCB}	Hz	Natural mechanical resonance frequency of the PCB board
f_{R}	-	Rolling resistance coefficient

f_{s}	Hz	Switching frequency
f_{SO}	Hz	Overall switching frequency at the output of the CHB
g	m/s^2	Gravitational acceleration
G_{F}	-	Open-loop amplification ratio of the feedback operational amplifier network
G_{P}	-	Open-loop amplification ratio of the power operational amplifiers
h	mm	The height of the PCB solder joint
l	mm	The length of the PCB solder joint
i_{g}	-	Transmission ratio of the vehicle
$I_{\mathrm{bat\_ave}}$	A	Average current of the battery
$I_{\mathrm{bat\_RMS}}$	A	RMS value of the battery current
$I_{\mathrm{bat\_S\_RMS}}$	A	RMS value of switching frequency ripples in battery current
$I_{\mathrm{bat\_AC\_RMS}}$	A	RMS value of AC frequency ripples in battery current
I_{Bond}	A	Average current conducted per bond wire in a stress cycle
I_{cell}	A	Current of one battery cell
I_{dev}	A	Error of the current generated by the testing circuit
$I_{\mathrm{P\_RMS}}$	A	RMS value of the phase current
$I_{\mathrm{Q\_Mcycle}}$	C/s	Charge rate caused by the micro cycles
$I_{\mathrm{Ripple\_RMS}}$	A	RMS value of all the ripples inside battery current
K_{AMP}	-	Closed-loop amplification ratio of the battery testing circuit
K_{P}	-	Parameter for the SOC balancing control
m_{a}	-	Modulation index of inverters
M	kg	Mass of the vehicle
n	1/min	Rotation speed of the motor
n_{p}	-	Number of paralleled switches
n_{Bond}	-	Total number of bond wire joints in the inverter system
n_{C}	-	Total number of DC-link capacitors in the inverter system
n_{Die}	-	Total number of semiconductor dies in the inverter system
n_{Solder}	-	Total number of PCB solder joints in the inverter system
$N_{\mathrm{contactor}}$	-	Number of contactors in the powertrain system
N	-	The number of submodules in the CHB
N_{HS}	-	Number of the heatsinks

N_{fBond}	-	Cycle life of one bond wire joint
N_{fC}	-	Cycle life of the DC-link capacitor
N_{fDie}	-	Cycle life of one die attachment
N_{finv}	-	Cycle life of one inverter
N_{fMSolder}	-	Cycle life of one PCB solder joint in thermal stress
N_{fTSolder}	-	Cycle life of one PCB solder joint in mechanical stress
$P_{\mathrm{bat\_ohmic}}$	W	Total ohmic loss of the batteries
P_{battery}	W	Terminal power of the battery pack
$P_{\mathrm{IGBT\_Loss}}$	W	Total loss of the IGBT inverter
$P_{\mathrm{C\_Diode}}$	W	Conduction loss of one anti-paralleled diode
$P_{\mathrm{C\_IGBT}}$	W	Conduction loss of one IGBT
P_{S}	W	Total switching loss of one IGBT and one diode
$P_{\mathrm{CHB\_Loss}}$	W	Total loss of the CHB
$P_{\mathrm{C\_CHB}}$	W	Total conduction loss of the CHB
$P_{\mathrm{C\_MOSFET}}$	W	Conduction loss of one MOSFET
$P_{\mathrm{S\_CHB}}$	W	Total switching loss of the CHB
$P_{\mathrm{S\_MOS}}$	W	Switching loss of one MOSFET
$P_{\mathrm{S\_Diode}}$	W	Switching loss of one diode
$P_{\mathrm{SiC\_Loss}}$	W	Total loss of the SiC MOSFET inverter
$P_{\mathrm{C\_Total}}$	W	Total conduction loss of the SiC MOSFET inverter
$P_{\mathrm{C\_SiC}}$	W	Conduction loss of one SiC MOSFET
$P_{\mathrm{S\_Total}}$	W	Total switching loss of the SiC MOSFET inverter
$P_{\mathrm{Transistor}}$	W	Total loss of one transistor
P_{Diode}	W	Total loss of one diode
P_{Copper}	W	Copper loss of the motor
$P_{\mathrm{Iron\_Loss}}$	W	Iron loss of the motor
$P_{\mathrm{M\_Loss}}$	W	Total loss of the motor
$P_{\mathrm{Loss\_Max}}$	W	Maximum loss dissipated via one heatsink
Q_{rr}	C	Recovery charge of the diode
r_{ppIGBT}	%	Ripple index of the DC voltage caused by the IGBT
R	m	Radius of the tyre
$R_{\mathrm{bat\_AC}}$	Ω	Resistance of batteries for AC frequency ripples

$R_{\mathrm{bat\_DC}}$	Ω	DC resistance of batteries
$R_{\mathrm{bat\_fs}}$	Ω	Resistance of batteries for switching frequency ripples
R_{C}	Ω	Conduction dynamic resistance of the IGBT
R_{D}	Ω	Conduction dynamic resistance of the anti-paralleled diode
R_{S}	Ω	The stator winding resistance of the motor
R_{Sample}	Ω	Sampling resistance used in the battery testing circuit
R_{on}	Ω	On-state resistance of MOSFETs
$R_{\mathrm{Dth(j-c)}}$	K/W	Thermal resistance between diode junction and casing
$R_{\mathrm{Tth(j-c)}}$	K/W	Thermal resistance between transistor junction and casing
$R_{\mathrm{th(c-s)}}$	K/W	Thermal resistance between the heatsink and casing
R_{veh}	km	Nominal range of the electric vehicle
SOC_{ave}	%	The average SOC of all the submodules in the CHB
SOC_{i}	%	The SOC of the *i*th submodule in the CHB
t_{cycle}	s	Duration of the driving cycle
t_{fC}	s	The life time of a DC-link capacitor
t_{FI}	s	Falling time of the current
t_{FU}	s	Falling time of the voltage
t_{nominal}	s	The life time of a DC-link capacitor in nominal condition
$t_{\mathrm{trans\_CHB}}$	s	The length of one switching transient of the CHB
$t_{\mathrm{trans\_IGBT}}$	s	The length of one switching transient of the IGBT
T_{j}	°C	Junction temperature of switches
ΔT_{j}	°C	Swing of the junction temperature in a thermal stress cycle
T_{max}	°C	Maximum temperature of a PCB solder joint in one cycle
T_{min}	°C	Minimum temperature of a PCB solder joint in one cycle
T_{Mean}	°C	Average temperature in a thermal stress cycle
T_{n}	°C	The nominal temperature of the DC-link capacitor
T_{test}	°C	The temperature of the DC-link capacitor in the reliability test
t_{on}	s	The on-state time of the switch in one stress cycle
t_{RI}	s	Rising time of the current
t_{RU}	s	Rising time of the voltage
T	N M	Torque of the motor
T_{AC}	s	Period of the AC current

u_{AC}	V	AC output voltage of one H-bridge
u_{CE0}	V	Zero current voltage drop of the IGBT
u_{F0}	V	Zero current voltage drop of the anti-paralleled diode
u_{DC}	V	DC voltage of the battery pack or battery module
$u_{\mathrm{DC\_IGBT}}$	V	DC voltage switched by the MOSFETs in the CHB
$u_{\mathrm{DC\_IGBT}}$	V	DC voltage switched by the IGBTs
u_{N}	V	Output voltage of the negative side half-bridge
u_{P}	V	Output voltage of the positive side half-bridge
u_{ref}	V	Reference voltage of the inverter
$u_{\mathrm{ref\_i}}$	V	Reference voltage of the *i*th submodule in the CHB
U_{cap}	V	Rated voltage of the DC-link capacitor
U_{P}	V	Peak value of the AC voltage
v	m/s	Speed of the vehicle
dv/dt	kV/us	Speed of the voltage change, for EMI evaluation
Δv_{pp}	V	Peak value of the voltage ripples on the DC link
V	V	Rated voltage of the switch for reliability simulation
V_{bat}	V	Voltage of one battery cell
V_{IN}	V	Input voltage given by the DAC to control current waveform
V_{HS}	m^3	Volume of the heatsink
V_{N}	V	The absolute voltage of the battery anode in testing circuits
V_{P}	V	The absolute voltage of the battery cathode in testing circuits
V_{n}	V	The nominal voltage of the DC-link capacitor
V_{test}	V	The voltage of the DC-link capacitor in the reliability test
V_{REF}	V	Reference voltage for the DAC and the power operational amplifier circuit

1 Introduction

Climate change is one of the major challenges that humanity has to deal with in the near future, which is potentially caused by the growing greenhouse gas emissions [1], [2]. Among the total greenhouse gas emissions worldwide in 2016, 20 % is attributed to road vehicles consuming fossil fuels [3]. The usage of fossil fuels in the transport sector is also one of the main reasons for heavy urban air pollutions that are commonly observed in urbanized areas [4], [5]. Therefore, to mitigate the problems associated with fossil fuels, electric vehicles (EV), particularly battery electric vehicles (BEV), have been more insistently confirmed by governments and industries to be an inevitable choice [6]–[9].

Several countries declared a road map to completely phase out internal combustion vehicles in 2030-2040 [10], [11]. Some cities have already forbidden certain internal combustion engine vehicles (ICEVs) to enter certain areas, in order to reduce local pollution [12], [13]. Tax incentives or specific license plate quota were also provided to BEV buyers, and significantly contributed to the rapid growth of the BEV market in recent years [14], [15]. In industries, a growing amount of funding is invested in relevant technologies to accelerate this transition. In 2017, more than 90 billion US dollars were invested by major original equipment manufacturers (OEM) worldwide in research and development of EVs [16]. Volkswagen even announced to completely electrify its fleet before 2030 [17].

1.1 Motivation and Goals

Despite the rapid growth of BEV sales, BEVs still only account for a rather small portion of the total annual sales of vehicles [18]. In 2017, 90 million vehicles were sold worldwide [19], while only 0.7 million of them, i.e., 0.78 %, were BEVs (plug-in hybrid electric vehicles, PHEV, not included in the value) [18]. Moreover, the currently observed rapid growth is mainly a result of short-term policies and thus might not be sustainable [20]. In China, the largest market of BEVs [18], the decrease in subsidies to electric vehicle buyers is expected to reduce the sales of BEVs by 42 % [21].

The main factors hindering the acceptance of BEVs include their high retail price and limited range, which are majorly caused by the high cost of batteries [22]–[24]. The price of an economic BEV with a rated range of 300 km or longer is still generally higher than 30,000 United States dollars (USD) [25], even though the progress in battery technology and economies of scale have reduced the battery price significantly in recent years [26].

In order to accelerate the public acceptance of BEVs, besides waiting for the battery price to decrease even further, an alternative solution is to improve the efficiency of the powertrain. On the one hand, a higher efficiency can be used to prolong the driving range with a given battery pack capacity. On the other hand, a higher efficiency can also reduce the purchasing cost of a BEV, via a reduced requirement of battery pack capacity for the same range. Therefore,

motivated by the challenges and the benefits of efficiency improvement, with the focus on the design of the inverter (a determining component for the powertrain efficiency, defined and introduced in detail in chapter 2), the goals of the dissertation are formulated as follows:

- Benchmarking of an state-of-the-art automotive inverter and identifying potentials to improve efficiency
- Developing a general concept to improve the efficiency of automotive inverters
- Evaluating the inverter design systematically, besides the efficiency improvement

1.2 Scope

As this dissertation is primarily searching for an efficient inverter design and investigating the improvements, it is essential to define the criteria to evaluate inverter designs. Considering the relevance to automotive applications, this dissertation conducts dedicated investigations in four aspects, efficiency, cost, influence on battery aging and reliability.

First, the efficiency is the most important aspect to consider, as it is the fundamental motivation of the research. The efficiency values used for evaluation are the average inverter efficiency over one driving cycle or driving test, rather than the peak efficiency, because the range and the energy consumption of BEVs are only influenced by the average efficiency.

Second, the powertrain system cost is calculated, in order to determine if the benefit of a higher efficiency can pay off the cost. As explained in section 1.1, an increase in efficiency can reduce the cost of the battery. Nonetheless, if the cost of an efficient inverter is rather high and cannot be compensated by the reduced battery cost, the system cost will increase. Such an inverter would not be worth implementing anymore. To determine whether a novel inverter design should be implemented in a certain vehicle, the system cost should be modelled. Cost analysis should be conducted in different scenarios to identify the appropriate scenarios to implement the proposed inverter design.

Third, the influence of the inverter on the aging of batteries should be considered as well, because the aging behavior of batteries could be affected by the inverter design, due to the change of current waveforms, particularly the ripples in the current waveforms. If an inverter concept is identified to be harmful to batteries, it should not be considered for any BEV, regardless of its efficiency improvement.

In the end, a quantitative reliability assessment of an inverter design is also necessary, as the differences in terms of circuits and thermal behaviors may significantly change the reliability of an inverter system. Especially for automotive applications, where the reliability is of high importance, the reliability assessment cannot be neglected, in case that a more efficient inverter concept deteriorates the reliability significantly.

After introducing the targets and the scope, the next chapter benchmarks a state-of-the-art automotive inverter, in order to identify the potential problems in terms of efficiency. The specific research question of the dissertation is then formulated based on extensive analysis and discussions of the problems identified.

2 Problem Identification

In previous studies, the efficiency of inverters has attracted little attention, because current automotive inverters in BEVs directly adopt the designs of industrial inverters, and the average efficiency of such inverter designs is higher than 97 % in industrial applications [27]–[29]. In industrial applications, inverters mostly operate continuously in the nominal power range [30], [31]. The efficiency is hence close to the high nominal efficiency documented in the datasheets, often in the range of 97-99 % [28], [32].

However, in contrast, the power profile of an automotive inverter varies in a much broader range, because the speed and acceleration of a vehicle can change significantly over a realistic driving profile [33]–[35]. Nonetheless, the average efficiency of an automotive inverter in realistic driving scenarios is not yet available in the literature. Therefore, in order to identify the problems and potentials of improvement, the efficiency of currently used inverter designs should first be benchmarked with driving cycle tests.

The BMW i3 (94 Ah version) is selected as the reference vehicle for benchmarking, and will be hereafter referred to as the “reference vehicle”, and its inverter as the “benchmarked IGBT inverter”. Although the reference vehicle was first released to the market in 2013, it is still selected as the benchmark. The reason is that it is still one of the most efficient BEVs in terms of energy consumption per 100 km, even compared to the BEVs released recently [36], due its powertrain design and light-weight structure. The benchmarked IGBT inverter can still demonstrate the state-of-the-art performance of current automotive inverter designs, according to a benchmarking research conducted by Oak Ridge National Laboratory in late 2016 [37].

2.1 Inverter Efficiency of the Reference Vehicle

In this section, the conventional powertrain architecture is introduced first to clarify some basic definitions. Then the powertrain losses of the reference vehicle are modelled, to benchmark the inverter efficiency with driving cycle simulations. The simulation results are analyzed and verified by experiments. Based on the results, the problems of the inverter design are identified. The research question of the dissertation is then formulated.

2.1.1 Powertrain Architecture and Components

Most BEVs, including the reference vehicle, adopt the electric powertrain architecture in Figure 2.1. It is primarily composed of three components, a battery pack to store the energy for the vehicle, an electric motor to drive the vehicle, and an inverter to convert the direct current (DC) voltage of the battery pack to alternating current (AC) voltage to control the motor.

The number of motors and inverters is not necessarily one. BEV concepts that are developed for better drivability, off-road or lateral performance can have multiple sets of motors and

inverters. In this section, the fundamental definitions associated with each component in the conventional architecture are introduced, along with the specifications of the reference vehicle.

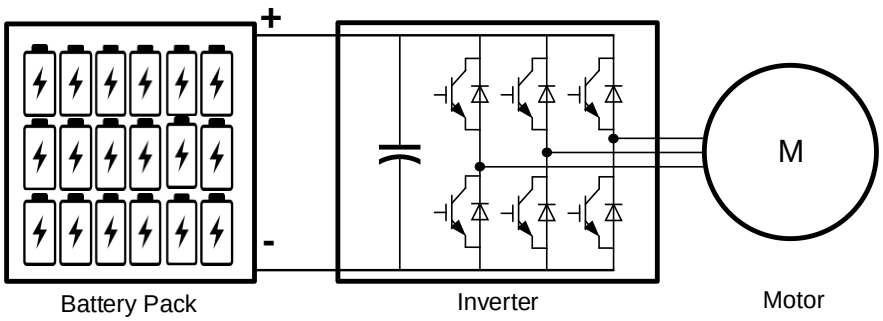


Figure 2.1: Conventional architecture of an electric powertrain

Battery Pack

A battery pack is composed of battery cells that are connected in series and parallel. The number of cells connected in parallel is determined by the desired capacity of the battery pack, while the DC nominal voltage defines the number of cells connected in series. The battery pack voltage of most BEVs is in 400 V level, and each lithium cell has a nominal voltage of 3.3 V or 3.7 V, depending on the battery chemistry [38]. Hence, the number of cells connected in series is often in the range of 90-120 [39, p. 11]. Specifically for the reference vehicle, 96 battery cells are connected in series to provide a nominal voltage of 360 V [37].

However, a large number of battery cells connected in series can cause a problem that the state of charge (SOC) of cells could be imbalanced [40]. As a result, the capacity of the battery pack cannot be fully utilized. Moreover, since the imbalance of batteries tends to grow during the usage of a BEV [40], the usable capacity of the battery pack decreases continuously. To maintain the usable capacity of the battery pack, the SOC of the series-connected cells must be balanced.

This function is often integrated within the battery management system (BMS), which monitors the voltage and temperatures of cells to ensure safety. A typical BMS consists of several slave BMSs and a master BMS. Each slave BMS is connected to a battery module, which is a submodule of the pack and typically composed of 12-16 cells in series. The slave BMSs conduct measurements and SOC balancing. The master BMS works as a central controller for the slave BMSs.

Inverter

As the battery pack only provides a DC voltage output, while a controllable AC voltage is required to drive the motor, an inverter is required for the voltage conversion. The most common inverter used by BEVs is shown in Figure 2.1. It is primarily composed of a DC-link capacitor (working as a filter for the DC voltage) and six switches, more specifically, six insulated insulated-gate bipolar transistors (IGBTs). This structure is thus called the six-pack topology [41].

In this structure, every two IGBTs form a bridge structure, called a half-bridge [42]. The two IGBTs in one half-bridge are switched on and off complementarily, so that the voltage at the output is switched between zero and the battery pack voltage. By defining an appropriate switching sequence, the inverter generates an equivalent sinusoidal AC voltage output. The most common approach to determine the switching sequence of one half-bridge is the pulse width modulation (PWM). The switching-on sequence of the upper IGBT can be obtained by comparing the desired sinusoidal AC voltage waveform, the reference voltage, to the triangular

carrier waveform. The generated switching-on sequence is recorded in the PWM signal. The PWM signal of the lower IGBT is determined complementarily. The PWM signals of all six IGBTs can be obtained by comparing the reference voltage of three phases with the carrier waves.

Nonetheless, a digital signal at the output of a controller is not sufficient to drive an IGBT. The switching-on and switching-off of an IGBT must be conducted by a gate driving circuit, or a driver, as demonstrated in Figure 2.2. A driving circuit for automotive inverters is primarily composed of an isolated dual-channel DC source to provide the isolated gate voltage (usually ±15 V), a push-pull circuit or other amplifying circuits to select the output voltage, and a resistor to limit the gate current and the switching speed [42]. Applying the PWM signal (usually isolated for reliability) at the gate driver, the gate voltage of the switch alternates accordingly between 15 V and -15 V. The switch is thus turned on or off following the desired switching sequence. There are indeed more sophisticated driving circuit designs, and the design of gate drivers is one of the main topics in power electronics field. Limited by the scope of the research, these advanced designs are not discussed in this dissertation.

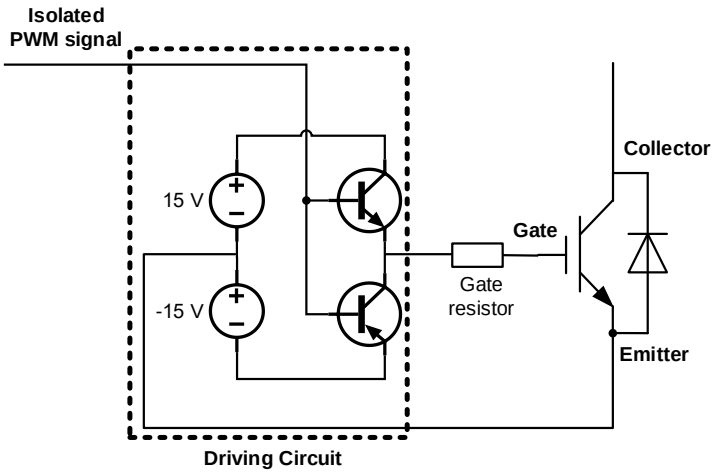


Figure 2.2: The driving circuit for an IGBT

The six-pack IGBT inverter design is the most common solution for 400 V level industrial applications. The products have been available on the market for more than 20 years [43]. Due to the availability of six-pack IGBT inverters in the voltage level of BEVs, they are widely used in the BEVs nowadays. In the reference vehicle, the benchmarked inverter uses the six-pack IGBT module FS800R07A2E3 from Infineon [37, p. 67].

Electric Motor

Electric motors provide the driving force to the vehicle drivetrain under the control of inverters. For BEVs, there are different types of appropriate electric motors. They differentiate from each other in terms of the windings structure, rotor structure and the placement of permanent magnet materials, etc. Introductions and comparisons of different electric motors can be found in [44]–[46]. Among all the options, permanent magnet synchronous motors (PSM) and asynchronous motors (ASM) are most frequently used in BEVs [44]. The motor of the reference vehicle is a PSM. However, the inner magnetic circuit of this motor is optimized by implementing the features of switched reluctance motors (SRM) and interior permanent magnet motors (IPM), so that the efficiency and torque density could be higher than a common PSM [37].

After the introductions in this section, the following section models the losses on each component of the powertrain. The performance of the powertrain is subsequently evaluated with the developed models in different driving cycles.

2.1.2 Powertrain Loss Modelling of the Reference Vehicle

In order to obtain the efficiency of the inverter and the powertrain in driving cycle simulations, the losses of the three components are modelled. Furthermore, to use the powertrain models in driving cycle simulations, the longitudinal model of the vehicle is also developed.

First, the loss of the battery pack is ignored. At most operational points during a driving cycle, due to the limited power demand, the discharge C-rate of the battery pack is rather low. Hence, in driving cycle simulations, compared to the losses caused by the motor and the inverter, the losses in battery cells are rather insignificant[47], and thus neglected in the loss modelling. The losses in battery cells are more significant during a high C-rate charge [38].

Second, the loss of the six-pack IGBT inverter in the reference vehicle is modelled. The inverter loss is composed of conduction loss and switching loss. The conduction loss is the loss on the semiconductor switch while conducting current. The switching loss is the loss caused by the transient voltage and current during switching-on or switching-off of the switch. As each IGBT has an anti-paralleled diode next to it, the conduction loss and switching loss (reverse recovery loss) of the anti-paralleled diodes are also considered.

These losses are modelled in eq. (2.1). The conduction loss of one IGBT, $P_{\mathrm{C\_IGBT}}$, and the conduction loss of one diode, $P_{\mathrm{C\_Diode}}$, are calculated based on the models proposed and verified by [48]. $P_{\mathrm{C\_IGBT}}$ is mainly influenced by two parameters, u_{CE0}, the zero-current forward voltage of the IGBT, and R_{C}, the dynamic resistance when the current changes. $P_{\mathrm{C\_Diode}}$ is determined by u_{F0} and R_{D}, which are defined similarly as u_{CE0} and R_{C}. Besides the switch parameters, the switching loss also varies with the electrical operational points, which are defined by $I_{\mathrm{P\_RMS}}$, m_{a} and $\cos\theta$. $I_{\mathrm{P\_RMS}}$ is the RMS value of the phase AC current. m_{a} is the modulation index, calculated by the dividing the peak to peak AC voltage with the battery pack voltage, u_{DC}. The power factor is $\cos\theta$, the cosine value of the phase lag between the AC current and voltage.

$$\begin{cases} P_{\mathrm{C\_IGBT}} = u_{\mathrm{CE0}}\sqrt{2}I_{\mathrm{P\_RMS}}\left(\frac{1}{2\pi}+\frac{m_{\mathrm{a}}\cos\theta}{8}\right)+2R_{\mathrm{C}}I_{\mathrm{P\_RMS}}^{2}\left(\frac{1}{8}+\frac{m_{\mathrm{a}}\cos\theta}{3\pi}\right) \\ P_{\mathrm{C\_Diode}} = u_{\mathrm{F0}}\sqrt{2}I_{\mathrm{P\_RMS}}\left(\frac{1}{2\pi}-\frac{m_{\mathrm{a}}\cos\theta}{8}\right)+2R_{\mathrm{D}}I_{\mathrm{P\_RMS}}^{2}\left(\frac{1}{8}-\frac{m_{\mathrm{a}}\cos\theta}{3\pi}\right) \\ P_{\mathrm{S}} = f_{\mathrm{s}}u_{DC}\left(a_{\mathrm{IGBT}}+2\sqrt{2}b_{\mathrm{IGBT}}I_{\mathrm{P\_RMS}}/\pi\right)+f_{\mathrm{s}}u_{DC}\left(a_{\mathrm{Diode}}+2\sqrt{2}b_{\mathrm{Diode}}I_{\mathrm{P\_RMS}}/\pi\right) \\ P_{\mathrm{IGBT\_Loss}} = 6\left(P_{\mathrm{C\_IGTB}}+P_{\mathrm{C\_Diode}}+P_{\mathrm{S}}\right) \end{cases} \tag{2.1}$$

The total switching loss of one IGBT and one diode, P_{S}, is deduced based on datasheet values [49]. By linearizing the datasheet values with regard to $I_{\mathrm{P\_RMS}}$ and u_{DC}, the formula of P_{S} can be derived. a_{IGBT}, b_{IGBT}, a_{Diode} and b_{Diode} are four coefficients obtained in the linearization. f_{s} is the switching frequency. In the end, multiplying the total loss of one IGBT and one diode by six, the total loss of the IGBT inverter $P_{\mathrm{IGBT\_Loss}}$ can be obtained.

In addition, as the parameters of the loss model in eq. (2.1) are thermal-dependent, a thermal model of the IGBT is constructed, in order to improve the accuracy, Figure 2.3 [50]. The thermal model is a typical equivalent circuit model based on the heat resistance and capacitance values.

The input to the model is the total loss of one diode, P_{Diode} and one transistor, $P_{\mathrm{Transistor}}$. The output of the model is the junction temperature, T_{j}. At the beginning of each time step of the simulation, T_{j} is updated according to the component losses. Then the parameters in eq. (2.1) are updated according to the datasheet of the IGBT module [49].

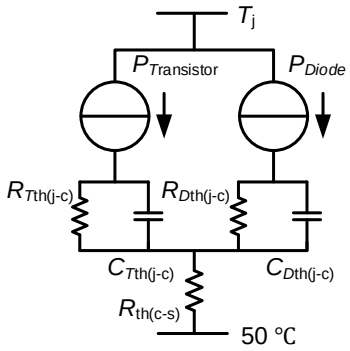


Figure 2.3: Thermal model the IGBT to calculate the junction temperature [50]

To obtain the inputs of the inverter loss model in eq. (2.1), the PSM model in [51] is selected, and parametrized according to the PSM in the reference vehicle [52]. This model converts the mechanical operation points (in rotation speed and torque coordinate) to electrical operation points, (in voltage, current and power factor coordinate). The obtained electrical operation points can be directly used in eq. (2.1) as inputs.

Besides the conversion, the PSM model in [51] can also be used to calculate the copper loss on the three phases, $P_{\mathrm{Copper\_Loss}}$, based on the resistance R_{S} and current values, eq. (2.2). The iron loss of the motor, $P_{\mathrm{Iron\_Loss}}$ is modelled by eq. (2.2), a simplified version of the iron loss model in [53]. T is the motor torque and n is the rotation speed of the motor. The coefficients in eq. (2.2), β_1 to β_3 are obtained via a nonlinear regression, using the measurement results provided in the datasheet of the motor in the reference vehicle [52, p. 49]. Hence, the highest accuracy can be ensured. Summing up the two types of losses, the total loss of the motor, $P_{\mathrm{M\_Loss}}$ can be obtained.

$$\begin{cases} P_{\mathrm{Copper\_Loss}} = 3R_{\mathrm{S}}I_{\mathrm{P\_RMS}}^2 \\ P_{\mathrm{Iron\_Loss}} = (\beta_1 n + \beta_2 n^2)T^{\beta 3} \\ P_{\mathrm{M\_Loss}} = P_{\mathrm{Copper\_Loss}} + P_{\mathrm{Iron\_Loss}} \end{cases} \tag{2.2}$$

With the models in eq. (2.1) and (2.2), the efficiency maps of the inverter and motor can be obtained. Nonetheless, to test the performance of the powertrain in driving cycle simulations, a longitudinal model of the reference vehicle is still necessary, eq. (2.3) [50]. The inputs of the longitudinal model are the profile of speed, v, and the profile of acceleration, a, which is derived based on the speed profile. The output is the mechanical operation point of the motor, T and n, in each time step of the simulation.

$$\begin{cases} T = (0.5\rho_{\mathrm{L}}c_{\mathrm{w}}A_{\mathrm{A}}v^2 + f_{\mathrm{R}}Mg + Ma)R / i_{\mathrm{g}} \\ n = \dfrac{30vi_g}{R\pi} \end{cases} \tag{2.3}$$

The symbols of the vehicle parameters in eq. (2.3) are designated following the nomenclature standard of the research institute. The detailed definitions are in the list of symbols, at the beginning of the dissertation. The parameter values of the experimental configuration in [54] are used in this dissertation, so that the accuracy of the models can be conveniently verified. These values are slightly different from the public information of the reference vehicle. The parameters of all the models developed in this section are provided in Appendix A1.

The driving cycle simulation model is developed by combining the powertrain loss models and the longitudinal vehicle model, as demonstrated in Figure 2.4. The total energy consumption in a driving cycle, E_{Cycle}, is the integral of battery power, P_{battery}, over time. The average efficiency of the inverter, $\eta_{\mathrm{inv\_ave}}$, is defined by the energy throughput on the AC side of the inverter and the inverter loss, eq. (2.4).

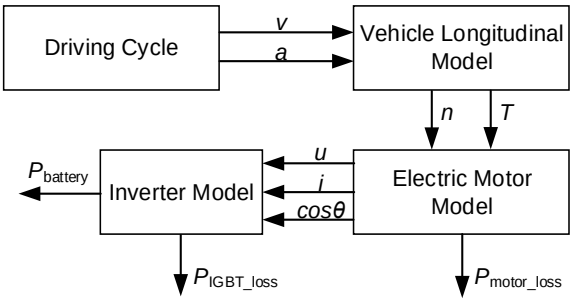


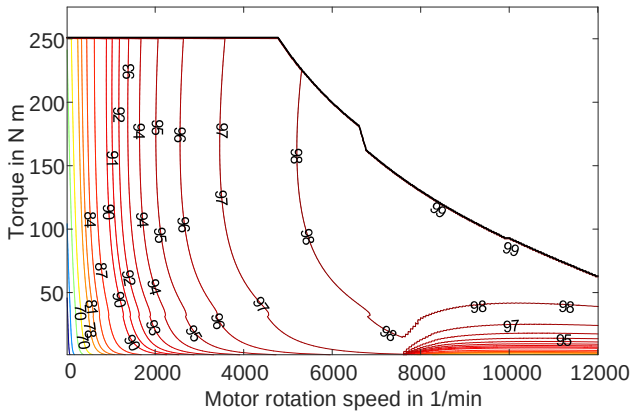
Figure 2.4: Block diagram of the driving cycle simulation to quantify the powertrain efficiency [50]

$$\begin{cases} E_{\mathrm{cycle}} = \int P_{\mathrm{battery}} \\ \eta_{\mathrm{inv\_ave}} = 1 - \dfrac{\int P_{\mathrm{IGBT\_loss}}}{\int |ui\cos\theta| + \int P_{\mathrm{IGBT\_loss}}} \end{cases} \tag{2.4}$$

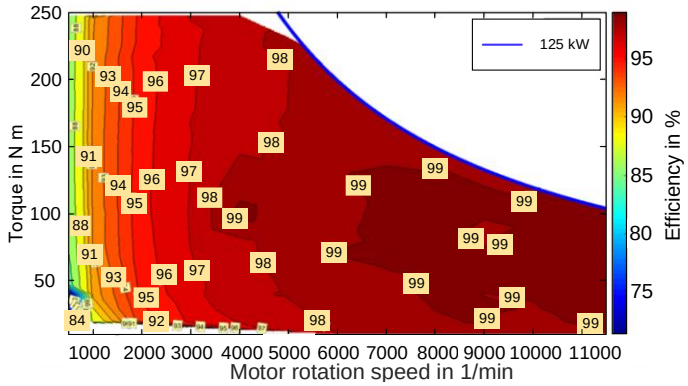
2.1.3 Model Verification and Simulation Results

Before collecting results from the driving cycle simulations, it is necessary to verify the accuracy of the models. Without verifications, the simulation results could contain significant errors and thus distort the analysis. The accuracy of the inverter model is verified first. The losses of the IGBT inverter calculated by eq. (2.1) are compared to the results simulated in ANSYS Simplorer, which provides an experimentally verified high accuracy, according to [55], [56]. The error of efficiency at all the operational points is within 1 %. A detailed comparison between the results of the two simulations is available in Appendix A2.

Besides the verification with accurate models, the accuracy of the inverter model is also verified by the experimental results in [37]. The simulated efficiency map of the IGBT inverter, Figure 2.5(a), is compared to the measured efficiency map, Figure 2.5(b) [37]. Comparing the efficiency contour at each speed value, it is observed that the efficiency error of the simulation is always within 1 %. The shapes of the contours are also rather similar. Therefore, based on the two verifications, the loss model of the IGBT inverter is proven to have a sufficiently high accuracy.



(a) Simulated efficiency map [50]



(b) Efficiency map obtained from experiment [37]

Figure 2.5: Simulated and measured efficiency maps of the IGBT inverter in the reference vehicle

Second, the vehicle model and the motor model also need verification. For this purpose, the driving cycle FTP72 is simulated using the model in Figure 2.4, and the results are compared to the experimental results in [54]. The current waveforms of the battery pack over the whole driving cycle are compared, Figure 2.6. The error is not directly visible, because the average absolute error is only 0.88 A. The simulated net output energy of the battery pack is 1264 W h, whilst the results from the experiment is 1248 Wh. The error of energy consumption is 1.42 %. Therefore, the accuracy of the vehicle model and the motor model can also be confirmed. As all the models used in Figure 2.4 are verified, the results of driving cycle simulations are reliable and can be used for further analysis.

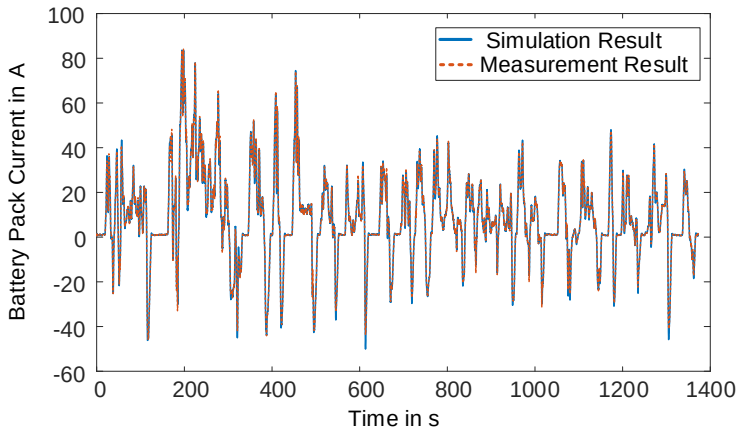


Figure 2.6: Comparison of the simulated battery current waveform and the measured waveform [50]

In order to analyze the efficiency of the inverter in urban, comprehensive and highway driving scenarios, the reference vehicle is simulated in the corresponding driving cycles. The results are listed in Table 2.1. All the values of energy are converted to kWh/100 km, to form a basis of comparison. It is first observed that the total energy consumption of the BEV increases, as the driving scenario changes from urban driving to highway driving. Nevertheless, as the total energy consumption increases, the total loss on the inverter decreases. That makes the efficiency in highway driving cycles rather close to the nominal value in the datasheet. The potential to improve the efficiency in highway driving is rather minimal.

On the contrary, although the BEV energy consumptions in urban and comprehensive driving cycles are comparatively low, the inverter losses turn to be significantly higher. The inverter efficiency in these driving cycles is thus much lower than the nominal values. Especially in urban cycles, the average efficiency is lower than 90 %. Hence, a problem of inverter efficiency in urban and comprehensive driving scenarios is identified. To understand the reasons for the problem, an analysis of the efficiency map, Figure 2.5, is necessary.

Table 2.1: Driving cycle simulation results of the IGBT inverter in the reference vehicle [50]

Driving cycles		BEV consumption per 100 km	Inverter loss	Inverter efficiency
Urban cycles	USA NECC	10.3 kWh	4.18 kWh	86.2 %
	Europe City	8.4 kWh	2.31 kWh	86.8 %
	USA City II	8.5 kWh	2.09 kWh	88.8 %
Comprehensive cycles	FTP72	9.7 kWh	1.72 kWh	90.8 %
	NEDC	11.1 kWh	1.39 kWh	91.9 %
	WLTP C3	12.8 kWh	1.20 kWh	93.7 %
Highway cycles	Artemis 130	18.1 kWh	0.72 kWh	96.5 %
	Artemis 150	19.1 kWh	0.85 kWh	96.6 %

In Figure 2.5, the inverter efficiency reaches the nominal efficiency, 97 %, only when the motor speed is higher than 4000 1/min (corresponding to a vehicle speed of 50 km/h). If the motor speed is higher than 8000 1/min, the torque is additionally required to be higher than 30 N m (corresponding to an acceleration of 0.23 m/s^2). That means the nominal efficiency of the inverter can only be reached when the speed is relatively high and the vehicle is still accelerating. In urban or sub-urban driving scenarios, this combination of speed and acceleration is uncommon, because vehicle drives mostly at low speed with mild accelerations. The operating points of the inverter mostly lie in the partial load area. Therefore, the main reason for the low efficiency in urban and comprehensive driving cycles is the low partial load efficiency of the inverter.

The root cause of the low partial load efficiency, especially the low efficiency in low speed area, can be further traced back to the formulas of inverter losses, eq. (2.1). First, the switching loss is only related to the DC link voltage and the AC current. The motor speed, which is linear to the output AC voltage of the inverter [51], does not affect the switching loss at all. When the vehicle speed decreases, the inverter power decreases accordingly, but the switching loss stays constant. Consequently, the inverter efficiency decreases with speed. Since the switching loss

accounts for more than 70 % of the total loss of an IGBT inverter [47], the pattern of the switching loss can be identified as the main reason for the low partial load efficiency problem.

Second, the conduction loss also partly contributes to the efficiency problem. In eq. (2.1), the conduction loss formula contains terms that are linear with the inverter current. The reason is that the IGBT is a bipolar switch and has a constant forward voltage drop of about 0.7 V regardless of the current [41]. Due to this diode-like feature, when the AC output voltage decreases with speed, the constant voltage drop becomes more significant in the output voltage and makes the conduction loss accounts for a larger part in the inverter power. As a result, the inverter efficiency in the low speed area is further deteriorated by the conduction loss.

To summarize, the root causes for the partial load efficiency problem are the features of the IGBTs. These characteristics are not problematic for industrial applications that mostly operate in the nominal power area. However, for a BEV driving in urban or comprehensive scenarios, the energy consumption can be further reduced by improving the partial load efficiency of the inverter. With the aim to improve the partial load efficiency, the research question of the dissertation is formulated based on the problems and the identified root causes.

2.1.4 Research Question

Motivated by the benefits resulting from the higher powertrain efficiency, this dissertation aims to improve the powertrain efficiency via an improved inverter design. Considering the fact that the main problem of the state-of-the-art inverter design is its low partial load efficiency, the research question is formulated as: *What is a general design of automotive inverter that can provide high efficiency in the partial load area and the nominal load area?*

Moreover, according to the analysis in the previous section, the targeted inverter design should primarily solve the problems associated with the features of the IGBT. Hence, the research question can be decomposed into two parts, each part targeting one loss item:

- Find an inverter design that reduces the switching loss in the whole operational range or makes the switching loss dependent on the speed of the motor.
- Find an inverter design that reduces the conduction loss in the whole operational range or eliminates the linear term in the conduction loss formula.

With the proposed research question, existing solutions to improve partial load efficiency of inverters are systematically reviewed and categorized in the next section. The features of each category are further summarized to identify the challenges and benefits of the solutions.

2.2 State of the Art Solutions

As stated at the beginning of the chapter, the partial load efficiency of automotive inverters has not been extensively studied, as the problem has not been widely recognized previously. In the research field of power electronics, most studies focus on general approaches to reduce the inverter loss in the nominal load area, e.g., soft switching technologies [57]–[59], or the optimization of circuit parameters [60]–[62]. However, these solutions are either inappropriate to implement in automotive inverters or contribute marginally for the partial load efficiency problem.

Improved motor control algorithms, e.g., the flux optimized vector control algorithm [51], are another general approach to reduce the losses of inverters, but these algorithms have been widely implemented for many years and do not fully solve the partial load efficiency problem of inverters. In fact, in the simulations of the reference vehicle in section 2.1, the flux optimized vector control is already implemented in the motor model [51], while the problem of low partial load efficiency is still significant in the results. Further improvement of the inverter efficiency via motor control algorithms is expected to be difficult and marginal.

Nonetheless, in recent years, there are indeed a few studies dedicatedly studying the partial load efficiency of inverters, as electrification has been confirmed to be the inevitable trend of the automotive industry. All of these studies approach the problem by improving the circuit design, which reveals the limitations of the general methods introduced above. Based on the primary ideas of the studies, the solutions proposed by these studies are classified into three categories and discussed respectively.

2.2.1 Shift DC Link Voltage

Among the few studies focusing on the partial load efficiency problem, the first category of studies investigate different methods to shift the DC link voltage of the inverter at different speeds, in order to correlate the switching loss and the motor speed. When the motor speed is low, i.e., the AC voltage is low, these methods reduce the DC link voltage of the inverter, in order to achieve a lower switching loss. The efficiency in the low speed area can thus be effectively improved.

Among this category of solutions, [63]–[67] use a bidirectional DC/DC converter between the inverter and the battery pack, so that the DC link voltage can be shifted continuously, Figure 2.7. When the motor is operating below the nominal speed, an optimal DC voltage is chosen to optimize the partial load efficiency. However, as these solutions require a DC/DC converter in the powertrain, the efficiency improvement can be significantly affected by the losses of the DC/DC converter. A DC/DC converter that is able to handle the maximum power of the powertrain is also expensive and can make these solutions not cost-effective. Bypassing the DC/DC converter at a high power can help to reduce the power rating of the DC/DC converter, but expensive high voltage mechanic contactors are required to conduct bypassing.

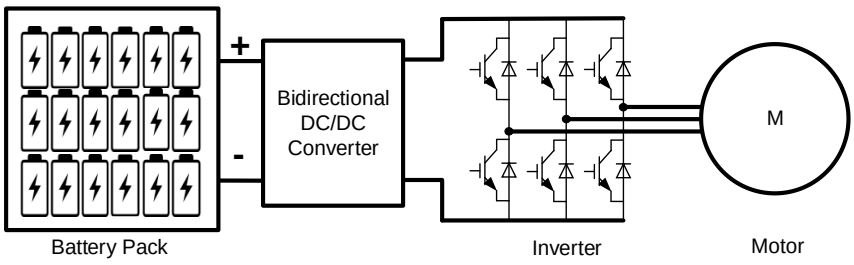


Figure 2.7: Using a DC/DC converter to improve the partial load efficiency for BEVs

[68]–[70] shift the DC link voltage using a Z-source inverter, Figure 2.8. The basic idea of the Z-source inverter is to integrate the DC/DC conversion components into the inverter. However, the passive components in the DC link, especially the high current inductors, can significantly increase the weight of the inverter, which is not appropriate for automotive applications. The passive components in the circuit also cause additional losses and limit the improvement of the efficiency.

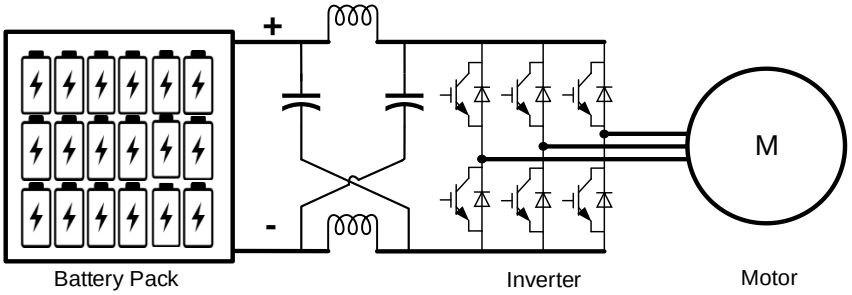


Figure 2.8: A Z-source inverter to improve the partial load efficiency for BEVs

[71], [72] propose to use an active battery pack to vary the DC link voltage when the motor speed changes. The active pack actively connects the battery modules in parallel or series, in order to shift the DC voltage. As this solution can only generate a DC voltage of specific values instead of a continuous voltage output, the passive components required by the voltage conversion can be eliminated. The switches required to realize the active connecting functions are silicon (Si) Metal Oxide Semiconductor Field Effect Transistors (MOSFET), Si MOSFETs, which have a rather low cost. Hence, the cost of such a system could be insignificant. However, as the DC voltage of such system shifts abruptly from one value to another, the pre-charge and pre-discharge of the DC-link capacitor in the six-pack inverter must be carefully managed. The corresponding control strategies are discussed in [73].

In summary, six-pack IGBT inverters are still used by this category of solutions. At low speed, the DC link voltage is shifted actively by different mechanisms. Therefore, this category of solutions only reduces the switching loss of IGBTs in the partial load area. The conduction loss stays unchanged. Moreover, all these solutions require additional components and an unaltered IGBT inverter, which tends to worsen the cost, weight, reliability and nominal load efficiency of the inverter.

2.2.2 SiC MOSFET with High Voltage DC Link

In contrast to the previous category that still adopts IGBTs in the inverter, many researchers propose to replace the IGBTs with MOSFETs made of wide band gap (WBG) materials, particularly silicon carbide (SiC) MOSFETs, in the conventional powertrain architecture [74]–[78]. They also deem this approach as the ultimate solution to the partial load efficiency problem.

As a MOSFET is a unipolar switch, its switching transient is intrinsically much shorter, compared to an IGBT [79, p. 12]. Due to the property of the SiC material, SiC diodes also have a much lower recovery loss, compared to Si diodes [80]. As a result, the switching loss of a SiC MOSFET inverter is 80 % lower than that of an IGBT inverter at full power [81]. The SiC material also has a higher thermal conductance compared to Si, and is possible to withstand high temperature up to 175 °C. The cooling design of inverters with SiC switches could be thus made easier.

The improvements of SiC MOSFETs in terms of efficiency and thermal management have been investigated experimentally in [80]–[84]. Nonetheless, specifically for automotive applications, it is still controversial whether or when the improvements of SiC MOSFETs are able to pay off their high cost, especially for light-duty private vehicles [81]–[88]. Although having been prototyped in laboratories worldwide for many years, the only commercialized vehicle reported to use a SiC MOSFET inverter is the newest Tesla Model 3 [89]. That partly reveals the concerns regarding the implementation of SiC MOSFET inverters. Besides, SiC MOSFETs also bring challenges to

the circuit design. If the parasitic parameters or the driving circuit are not properly designed, SiC MOSFETs can result in a much worse electromagnetic compatibility (EMC), due to their intrinsic high speed of switching [90]. The high EMI results in potential risks for other electronic devices in the vehicle, and may damage the insulation of the electric motor [91].

In order to mitigate the high price of SiC MOSFETs, [92]–[94] mix a SiC MOSFET inverter with an IGBT inverter. A SiC MOSFET with a low current rating is paralleled next to each IGBT in the six-pack structure. The SiC MOSFET is only used to absorb the switching transient of the IGBT, or handle a rather low current. Hence in these circuits, the IGBTs are operating under soft switching conditions [93], i.e., the switching of the IGBT only happens at zero current. Nonetheless, significant challenges regarding the switching transient control arise, because the SiC MOSFETs are used at the limit of the safe operation area [93]. The reliability of such a solution could be questionable.

As a summary, compared to the IGBT inverter, SiC MOSFET inverters can effectively reduce the switching loss in the whole range of operation. The conduction loss could be slightly higher at a higher load [95]. The main disadvantage of this solution is the high price of SiC MOSFETs, which makes the solution inappropriate for cost sensitive scenarios.

2.2.3 Si MOSFET with Low Voltage DC Link

As stated in the previous section, the benefits of SiC MOSFET inverters are mainly attributed to the unipolar properties of MOSFETs. To avoid the high cost of SiC semiconductors, a natural idea is to replace SiC MOSFETs with Si MOSFETs for the inverter design. Following this approach, the advantages of MOSFETs can still be utilized.

However, Si MOSFETs are not directly compatible with a high voltage DC link, because a low on-state resistance is only possible to realize in low voltage Si MOSFETs, which is caused by the limitations of the Si material [95]. To enable the usage of Si MOSFETs, [96] proposes to reduce the DC link voltage to 48 V, and to use a multiphase inverter composed of low voltage Si MOSFETs in a 300 kW powertrain, Figure 2.9 [97]. Such a multiphase inverter follows the same basic structure as in Figure 2.1, but it has 60 half bridges, corresponding to the 60 phases of the system [96]. Experiments prove that the switching loss and the conduction loss are both considerably lower than those of a conventional IGBT inverter in the partial load area. Because of the low price of 48 V Si MOSFETs, the system also has a low cost [97]. Nevertheless, challenges of high current (possibly up to higher than 2000 A) have to be carefully managed [96]. The circuit breakers and cables for such a high current might increase the system cost.

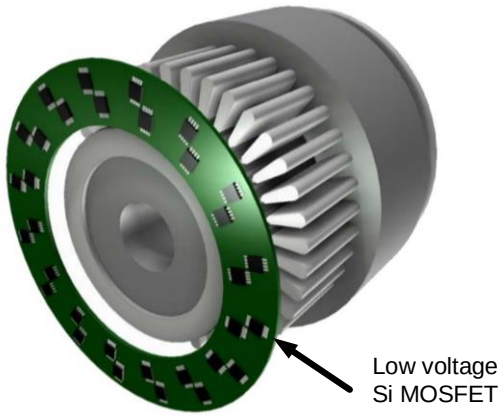


Figure 2.9: The 48V high power MOSFET inverter and the motor for BEVs [97]

There are also solutions that cannot be directly covered by the three categories above. [33]–[35] propose to parallel multiple discrete low current IGBTs to build the inverter and improve the efficiency via an improved control. However, the improvement is limited in terms of efficiency. According to the results in [33]–[35], for the benchmarked inverter, this solution is expected to reduce the inverter loss by 15 % and thus increase the efficiency by 1.2 % in NEDC driving cycle. Due to the high number of gate drivers, this solution might not be cost-effective as well. [59] integrates a resonance soft-switching circuit in an IGBT inverter, in order to reduce the switching loss. However, this solution is also not as effective as the three types of solutions discussed above. Therefore, these solutions are not extensively discussed any further.

2.2.4 Discussions and Criticisms

An overview of the existing solutions is presented in Table 2.2. Each category is marked with its corresponding loss reduction mechanisms. Compared to the IGBT inverters in the respective study, the expected efficiency improvement (in comprehensive driving cycles, .e.g., WLTP C3 and NEDC) and the main disadvantages of each solution are also summarized in the table.

Table 2.2: Summary of the existing solutions to the partial load efficiency problem

Solution Type	Losses reduced by the method		Efficiency improvement	Disadvantages
	Switching Loss	Conduction Loss		
DC voltage shifting	X		1-2 % [71], [72]	Limited effect, cost
SiC MOSFET	X	X	4-6 % [83], [92]	High cost, high EMI
Si MOSFET	X	X	4-6 % [97]	High current

As observed in Table 2.2, the first category of solutions, the DC voltage shifting approach, reduces the switching loss at partial load by varying the DC link voltage. Nonetheless, even with the solutions implemented, the switching loss of the IGBT inverter still contributes significantly to the total losses [66]. The conduction loss is not reduced at all. As a result, the overall improvement is limited.

Solutions based on Si or SiC MOSFETs reduce the switching loss in the whole range of power. The conduction loss in partial load is also reduced by Si or SiC MOSFETs.

The reduction of the switching loss is attributed to the shorter switching transients of unipolar switches. Unipolar switches conduct the current via a channel formed by the existing carriers, under the control of the gate voltage [98]. The formation and elimination of the channel can be completed rather rapidly [99]. In contrast, the switching-on or switching-off of an IGBT involves the generation or neutralization of new carriers, which can last up to 100 ns [49]. An experimental evidence of this difference is the tail current of the IGBT [100].

MOSFETs have a lower conduction loss in partial load, because MOSFETs conduct current like a resistor, and the conduction loss formula contains no term that is linear with the load current. Only quadratic terms are in the formula. Hence, the conduction of a MOSFET loss at a low current (corresponding to the low torque area) is lower than that of an IGBT.

Due to the decrease in the switching loss and the conduction loss, the efficiency improvement with Si or SiC MOSFETs is more significant in comparison to the DC voltage shifting methods. However, the additional challenges associated with the two types of MOSFETs need to be further

addressed. On the overall level, except for the three categories discussed above, most existing solutions only investigate the general approaches to improve the efficiency of an inverter. They do not dedicatedly identify the efficiency problem in the partial load area. The root causes for the low partial load efficiency are also not well analyzed.

In addition, although significant efficiency improvements are reported in existing studies, these improvements could be overestimated. First, the IGBT inverters used as benchmarks are sometimes not a state-of-the-art inverter, e.g., in [68], [85]. Their performance cannot represent a typical automotive inverter. Second, and also more commonly, the specifications of the benchmarked inverters and vehicles are unpractically matched, e.g., in [63]–[65], [67]. The specifications of the inverter, motor and vehicle are arbitrarily chosen instead of following an existing BEV. The IGBT inverter tends to be oversized and thus works more often in the low-efficiency area, resulting in a lower average efficiency in the tests. As the benchmark efficiency is potentially underrated, the efficiency improvements could be overestimated.

Moreover, the costs of the existing solutions are often not investigated at all, or just roughly discussed [83]. Hence, it is difficult to determine if the solutions are cost-effective or not. It is inappropriate to estimate the cost based on the large volume retail prices of the components, because these prices could still be considerably different from the purchasing price of OEMs, and may contain market noises. To decide if a solution is cost-effective, a cost model is still necessary. However, a cost model suitable for automotive applications is not yet available in previous studies.

2.3 Structure of the Dissertation

Due to the disadvantages of the existing solutions to the partial load efficiency problem, an improved concept is investigated. Holistic investigations on different aspects are conducted to assess the performance of the concept, instead of only focusing on the efficiency. Hence, the structure of the dissertation is formed and depicted in Figure 2.10.

First, in chapter 1, the background and the topic of the dissertation are introduced. Then the partial load efficiency problem of IGBT inverters is identified by simulating the reference vehicle in chapter 2. Existing solutions to the problem are summarized. Their disadvantages and common features are also discussed.

By summarizing the existing solutions, chapter 3 proposes an overall concept to solve the partial load efficiency problem. The functional mechanisms of the concept are briefly explained. The concept is compared to the benchmarked IGBT inverter in terms of efficiency, cost, influence on battery aging and reliability, respectively in chapter 4 to chapter 7.

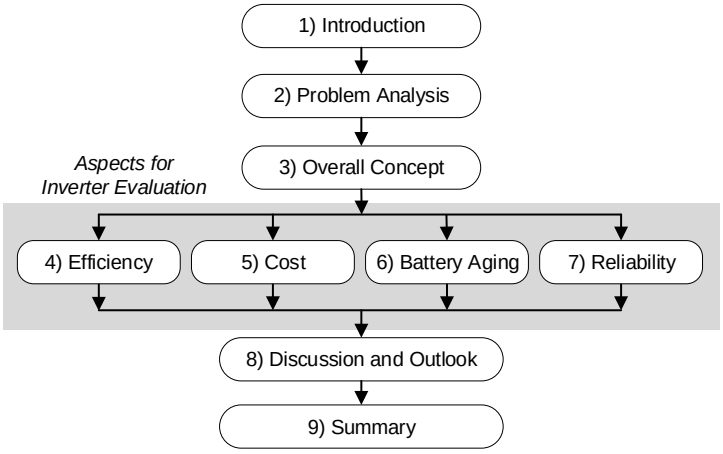


Figure 2.10: Structure of the dissertation

In chapter 4, the state-of-the-art studies regarding the efficiency modelling of the proposed concept are summarized. Then the efficiency of the proposed concept is modelled and verified. In chapter 5, a cost model for automotive inverters is constructed based on existing studies. The cost of the proposed concept is calculated and compared to the benchmarked IGBT inverter on the component level and the system level. A parameter sensitivity analysis is also conducted to investigate the cost reductions in different scenarios. Besides the comparisons to the benchmarked IGBT inverter, a state-of-the-art SiC MOSFET inverter is also added in the comparisons in chapter 4 and 5, as SiC MOSFETs are deemed by many researcher as the most promising solution to the efficiency problem.

Chapter 6 investigates the influence of the proposed concept on the battery aging behavior. Existing opinions on this topic are collected, but they cannot be directly used, due to their inconsistency and the lack of experimental verifications. Therefore, a battery testing circuit is designed for a dedicated aging test and the results are presented.

The reliability of the proposed concept is discussed in chapter 7. Since the proposed concept is fundamentally different from the conventional structure shown in Figure 2.1, it is necessary to evaluate the reliability quantitatively. For this purpose, existing component reliability models are summarized and combined to construct the reliability model for the inverter system.

The overall discussion and outlook are presented in chapter 8. Additional aspects to evaluate the concept are discussed generally. The most appropriate scenarios to implement the proposed concept are identified. In the end, the dissertation is summarized in chapter 9. The findings and the overall conclusion of the whole dissertation are stated.

3 Overall Concept

The previous chapter formulated the research question, reviewed and criticized the existing approaches for improving inverter efficiency. This chapter proposes the overall concept based on the analysis of the existing solutions and the trend towards high voltage powertrains. The operational mechanisms of the proposed concept are introduced. In the end, a CHB is parametrized identically as the benchmarked IGBT inverter for a fair comparison.

3.1 Proposal of the Cascaded H-Bridge

As observed in Table 2.2, the solutions that use unipolar switches, MOSFETs, are significantly more effective than the other approaches, such as the DC voltage shifting. The root causes of the partial load efficiency problem also indicate that IGBTs are not an optimal choice for automotive inverters. They are still used in most of BEVs, majorly because of their availability on the market and the path dependence on the 400 V level industrial inverter designs. Therefore, in order to improve the partial load efficiency effectively, the concept is required to use MOSFETs, particularly Si MOSFETs, to avoid the high cost of SiC switches.

However, Si MOSFETs with low on-state resistance are only available for low voltage applications. Using a low voltage DC link to solve that problem can be relatively challenging, as discussed in section 2.2.3. Moreover, low voltage DC links are not expected in all the BEVs in the future. To enable a higher charging power up to 350 kW, the trend of technology is to further increase the DC link voltage from 400 V level to 800 V level, Figure 3.1 [101], as demonstrated by Porsche. The high voltage is the key driving factor to make the charging time of BEVs comparable to the refueling time of an ICEV [101]. A higher DC link voltage is also able to reduce the ohmic losses during charging and driving. Hence, another requirement of the solution is that the proposed concept should be compatible with a high voltage of 400 V or 800 V.

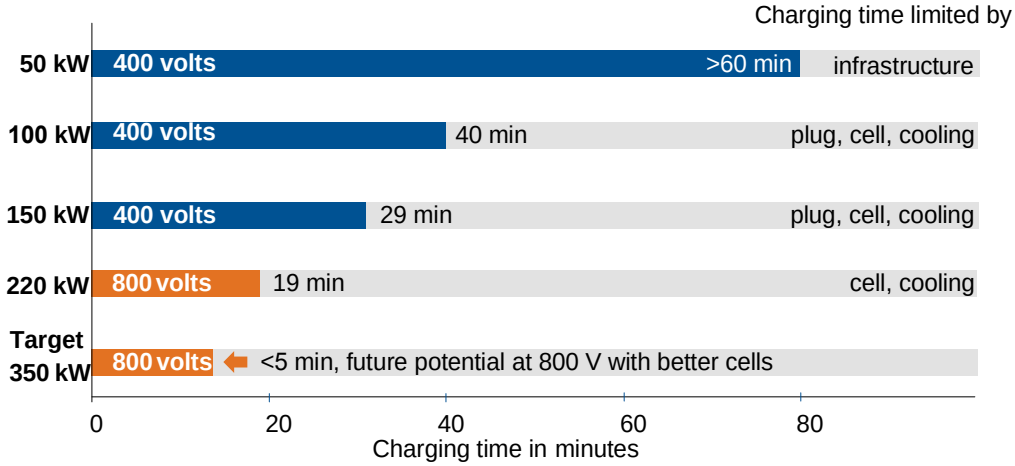


Figure 3.1: Fast charging possibilities enabled by the 800 V DC link [101]

Based on the two requirements, i.e., the usage of Si MOSFETs and the compatibility with high voltage, it is observed that the concept is essentially required to use the low voltage Si MOSFETs in high voltage applications. To reach a high voltage level that cannot be handled by individual switches, there is a standard solution, the multilevel circuit, or multilevel topology [102]. Therefore, to improve the partial load efficiency, this dissertation proposes to design automotive inverters using Si MOSFETs multilevel circuits.

This type of circuits is never used commercially in BEVs, but has been used for almost 40 years [103] in industrial applications with a voltage of 10 kV or higher, e.g., power grid [104], [105] and the traction of trains [106], [107]. There are also different types of multilevel circuits with different advantages and disadvantages. In order to determine an appropriate choice for BEVs, all the categories of multilevel circuits are explored.

The first type of multilevel circuit is called neutral point clamped (NPC) topology, Figure 3.2 [102]. It requires connections from the neutral point(s) of the DC link to the switches to clamp the DC voltage of the switches. The DC link voltage, u_{DC}, is hence distributed evenly on multiple switches. In this way, the phase output voltage has three levels, and the line-to-line voltage has five levels. In contrast, the phase output voltage of a six-pack inverter only has two levels, and the line-to-line voltage has three levels. However, for a switch rated at a given voltage, the number of required switches grows polynomially (quadratic) with the DC link voltage [108]. In this dissertation, as the target is to use MOSFETs rated at 100 V or lower (for a lower on-state resistance) in 400 V level, more than 30 switches are necessary per phase. Multiplying the number of paralleled switches, this number is even higher. Therefore, this category of circuits tends to be over complicated for the application of this dissertation. Considering that the DC link voltage will increase to 800 V in the future, this category of circuits becomes even less preferred.

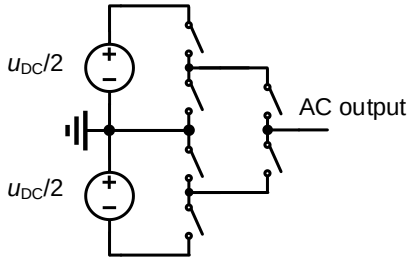


Figure 3.2: Three level neutral point clamped (NPC) circuit, one phase, output $+u_{\mathrm{DC}}/2$, 0, and $-u_{\mathrm{DC}}/2$

Another type of multilevel inverters uses flying capacitors to restrict the DC voltage blocked by each switch [109]. A typical example is shown in Figure 3.3 [108]. By controlling the voltage of the flying capacitor strictly to $u_{\mathrm{DC}}/2$, a stable operation can be realized. This type of circuits uses a smaller number of components to reach the same voltage level, compared to the NPC type. The number of switches and capacitors grows linearly with the DC link voltage.

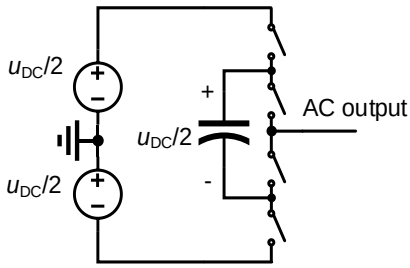


Figure 3.3: Three level flying capacitor circuit, one phase, output $+u_{\mathrm{DC}}/2$, 0 and $-u_{\mathrm{DC}}/2$

However, as the flying capacitor is working as a filter in a single phase system, the stabilization of the capacitor voltage becomes challenging when the frequency of the AC side is low [108]. Besides, as capacitors are one of the main bottle necks of the system reliability [110], solutions using an excessive amount of capacitors are generally not preferred in automotive applications. The usage of a high number of capacitors, therefore, forms another disadvantage of this type of circuits. Hence, this category of circuits is also not an appropriate choice for BEVs.

The last category of multilevel circuits cascades low voltage submodules to reach high voltage. A typical example is the Cascaded H-Bridge (CHB), Figure 3.4. Different from the previous two types of circuits, the cascaded circuit does not have a DC link. Instead, each submodule consists of a small inverter and an isolated low voltage DC source. The AC output voltage of each submodule can thus be cascaded to form a higher AC voltage.

The CHB does not have the problems of high complexity or low frequency operation, but it is not a popular solution for industrial applications, because an isolated DC source is needed per submodule, which could be rather expensive and bulky [111]. In most industrial applications, only one high power AC or DC source works as the main power supply. Hence, the high power multi-winding transformers are often used to create the required isolated DC sources [111]. These transformers are heavy and expensive, and can thus significantly increase the cost and weight of the system.

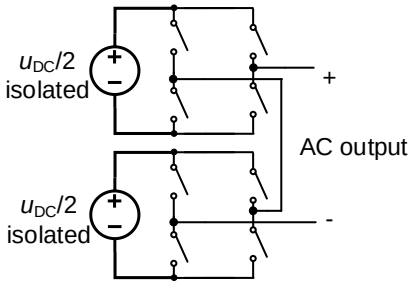


Figure 3.4: Five level cascaded H-bridge circuit, one phase, output $\pm u_{DC}$, $\pm u_{DC}/2$, and 0

However, for automotive applications, this problem does not exist, because battery modules can be directly used as isolated DC sources. The modularity of the cascaded circuits is also highly preferable for electric powertrains [112]. Therefore, this dissertation adopts the Si MOSFET CHB as the overall concept to solve the partial load efficiency problem. A general three-phase configuration of the CHB for BEVs is demonstrated in Figure 3.5.

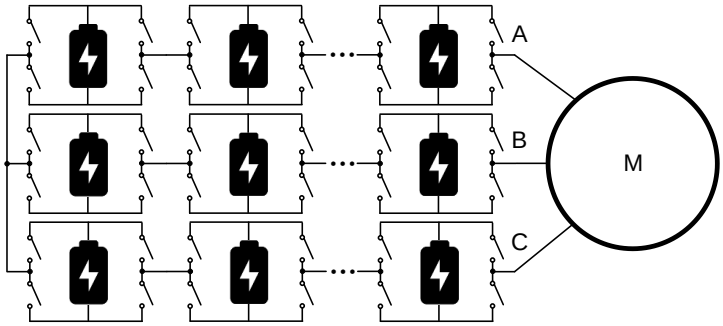


Figure 3.5: General three phase configuration of a CHB powered by battery modules

There are indeed other cascaded multilevel circuits besides the CHB, such as the modular multilevel converter (MMC), with a battery module in each half-bridge [113]. The circuit of submodules can also be changed for different purposes. In this research, the CHB is chosen as

an example of cascaded multilevel inverters, due to its simplicity, modularity and the elimination of passive components. Investigations are conducted for the CHB, in order to quantitatively confirm, whether the proposed solution is generally more efficient than the conventional IGBT inverter, and whether the solution is promising in terms of cost and other aspects.

It is worth noting that using CHB or other cascaded multilevel inverters in BEVs is not an entirely new idea. Although uncommon, some previous studies [114]–[117] also proposed to use cascaded multilevel converters in BEVs. However, their focus is on SOC balancing, which will be explained in the next section. Hence, each submodule contains only one battery cell, instead of a module. The usage of Si MOSFETs is not necessarily specified. The efficiency assessment is also not within their scope. Therefore, the research of this dissertation is fundamentally different from those in [114]–[117].

3.2 Operational Mechanism of the CHB

Before further modelling and assessments, the operational mechanisms of the CHB are introduced in this section, in order to make the dissertation easier to understand. First, a PWM algorithm of the CHB is introduced to demonstrate how the AC voltage waveform is generated. The SOC balancing of battery modules is then briefly explained.

3.2.1 Voltage Generation using PWM

As introduced in 2.1.1, for a conventional six-pack IGBT inverter, the PWM process is rather straight forward and has been introduced in [79] in detail. However, for the CHB, since the number of switches is significantly higher, it is necessary to explain how the PWM works to generate the desired AC voltage.

The explanation starts at the PWM process of one H-bridge, Figure 3.6. Taking the anode of the battery module as the reference ground for all voltage values, all feasible switch states and the corresponding outputs are enumerated in Table 3.1. The output voltage of an H-bridge u_{AC} is obtained by deducting the positive terminal voltage, u_{P}, with the negative terminal voltage, u_{N}. The PWM process of one H-bridge is to define a sequence to shift among the four statuses in Table 3.1. However, as four switches are involved simultaneously, the switching sequence cannot be directly determined by comparing the reference voltage with one carrier wave.

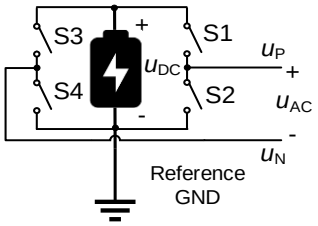


Figure 3.6: Circuit of one H-bridge

In order to still use the waveform comparison approach, a straightforward idea is to control the two half bridges individually and let each half bridge generate half of the reference voltage, $u_{\mathrm{ref}}/2$. In this way, the PWM of one H-bridge is similar to that of a conventional inverter with 2 phases. $u_{\mathrm{ref}}/2$ and $-u_{\mathrm{ref}}/2$ are given respectively to the two phases as the reference voltage. As the two references are the additive inverse of each other, such a process is also equivalent to comparing

one reference, $u_{\mathrm{ref}}/2$, with two phase-inverted triangular carrier waves, as demonstrated in Figure 3.7. For the PWM of one H-bridge, the illustration in Figure 3.7 is also more common than using two references and one carrier, because only one reference value is actually given to the whole circuit. The two carriers also manifest the degrees of freedom of the circuit: carrier 1 stands for S1 and S2 in Figure 3.6, while carrier 2 stands for S3 and S4.

Table 3.1: Switch state of the H-Bridge and corresponding voltage values

Switch state				Voltage values		
S1	S2	S3	S4	u_{P}	u_{N}	u_{AC}
on	off	off	on	u_{DC}	0	u_{DC}
on	off	on	off	u_{DC}	u_{DC}	*0*
off	on	on	off	0	u_{DC}	$-u_{\mathrm{DC}}$
off	on	off	on	0	0	*0*

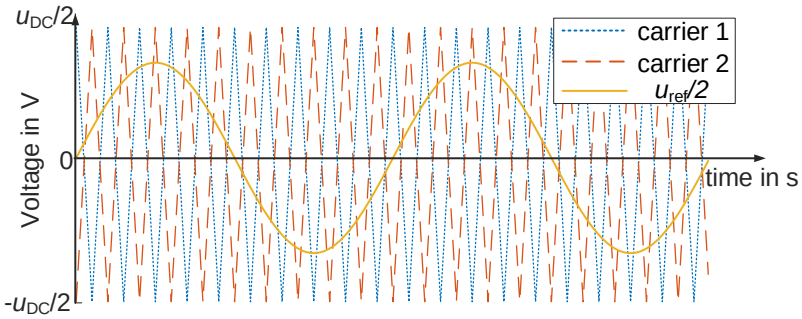


Figure 3.7: PWM process of one H-bridge

By simply duplicating the PWM process of one H-bridge, the PWM of the CHB can be conducted as well, because each H-bridge in the CHB can be controlled individually. For a CHB with N submodules per phase, to generate the desired AC voltage of one phase, u_{ref}, a naive approach is to use u_{ref}/N as the reference voltage to each module, and then repeat the procedure in Figure 3.7. Following this naive approach, all the N submodules change their output voltage simultaneously. The output voltage hence shifts among Nu_{DC}, 0 and $-Nu_{\mathrm{DC}}$, Figure 3.8.

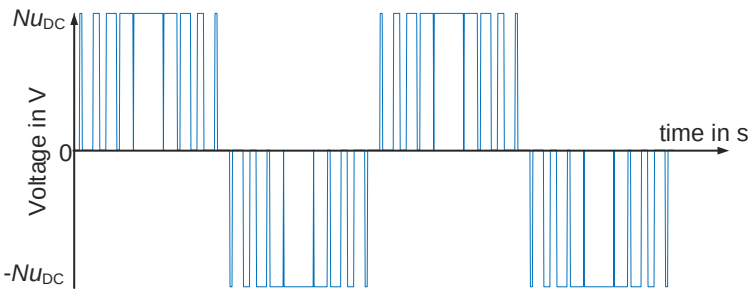


Figure 3.8: AC output voltage of one phase in the CHB following the naive PWM approach

This voltage waveform is indeed able to drive the electric motor, but the total harmonics distortion (THD) is as high as an IGBT inverter, which also affects the motor efficiency. To reduce the THD, a common modification is to sequentially shift the phase of the two carrier waves of each H-bridge by a phase angle of $2\pi/N$, [118]. N is the number of submodules in one phase. This

process is visualized in Figure 3.9. For clarity, only the carrier waves of the positive side half bridges are plotted in dotted lines (the carrier 1 in Figure 3.7). The negative side carriers can be obtained by simply inverting the plotted carriers. The reference sinewave is $u_{\mathrm{ref}}/2N$, applied to all the half bridges in the submodules. The period of the carriers is enlarged to demonstrate their phase difference clearly.

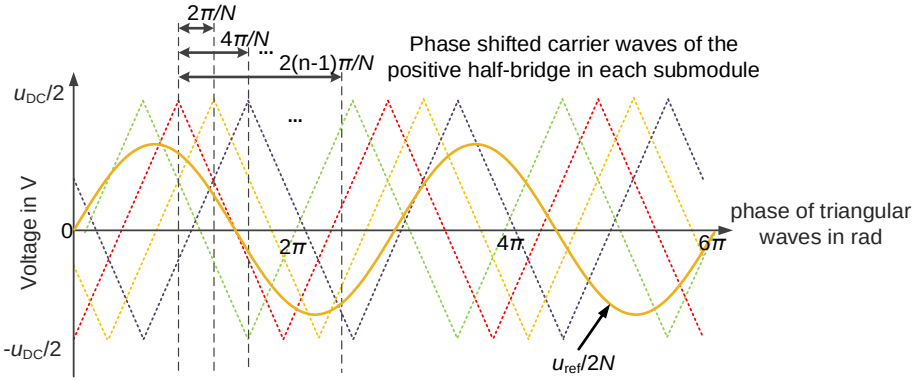


Figure 3.9: Phase-shifted carrier PWM of one phase in CHB

Due to the phase shift of the carrier waves, the carriers never cross the reference simultaneously. Hence, the outputs of any two submodules also never change at the same time. As a result, the waveform of the output voltage is changed from the waveform in Figure 3.8 to the waveform in Figure 3.10, which only changes by u_{DC} each time.

Since this waveform better approximates a sinewave compared to Figure 3.8, the THD is reduced and the motor efficiency could be slightly improved. Due to the carrier phase shifting feature of the PWM algorithm, it is often referred to as phase-shifted carrier PWM (PSC-PWM) [118]. There are also other PWM algorithms for the CHB, with considerations in different aspects [119]–[121]. However, as PWM algorithms differ little from each other in terms of the inverter efficiency, only the PSC-PWM algorithm is introduced and implemented for further simulations.

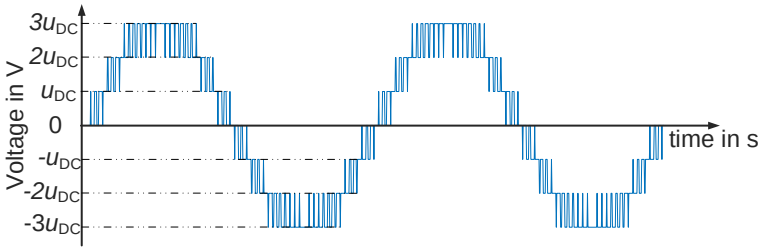


Figure 3.10: AC output voltage of one phase in the CHB following Phase-shifted carrier PWM

The descriptions above mainly focus on the discharging scenario, i.e., the energy of the batteries is converted to drive the motor. For the charging of the circuit, there are two feasible approaches. First, the CHB concept is still compatible with conventional DC charging. By making all H-bridges generate $+u_{\mathrm{DC}}$ (the status in the first row of Table 3.1), the battery modules are connected in series via MOSFETs, and hence form a conventional high voltage battery pack. In this case, at the output of each phase, a DC-charger can be applied following the conventional constant current constant voltage (CC-CV) scheme. The output terminals of the three phases can also be combined during charging, so that all modules can be charged simultaneously by one charger.

Second, the CHB can also be directly charged by the 400 V three-phase power grid, without using any energy conversion devices. A grid-connection control algorithm is necessary to control

the charging power and calculate the reference voltage [122]. The reference voltage is then generated following the PWM algorithm introduced above. However, as this topic is not within the scope of the research, the AC charging mechanism is not explained in detail.

3.2.2 SOC Balancing of Battery Modules

As stated in section 2.1.1, for a conventional powertrain using a six-pack inverter, a master BMS and a slave BMS per battery module are needed to balance all the series connected battery cells. The energy of the cells or modules with a higher voltage is actively dissipated on resistors of the BMS, until the voltage values converge. For the CHB, however, only a slave BMS is required in each module to realize the local SOC balance within the module. The SOC of submodules can be balanced by the PWM algorithms.

To enable SOC balancing, the PWM algorithm introduced in section 3.2.1 needs slight modification. Otherwise, due to the identical reference voltage and the identical AC current, each module generates the same power, which is not able to make the imbalanced SOC converge. To balance the SOC, the power of the modules should be adjusted according to their SOC values.

This can be realized by correlating the reference voltage to the SOC of the module, eq. (3.1). Compared to the algorithm in section 3.2.1, the reference voltage of each submodule contains an item proportional to the difference between its SOC, SOC_{i}, and the average SOC of the all modules, SOC_{ave}. K_{p} is a parameter to determine the balancing speed. Its value is positive during discharge, and turns to negative during charge or regeneration. As the current of each submodule is identical, the power of the submodules is also shifted proportionally according to their SOC deviations. Hence, the SOC of all submodules tends to converge back to SOC_{ave}, once there is an identifiable deviation. The SOC balancing is thus realized by applying eq. (3.1).

$$\begin{cases} u_{\mathrm{ref}\_i} = u_{\mathrm{ref}} / 2N + (SOC_i - SOC_{\mathrm{ave}})K_{\mathrm{p}} \\ i = 1, 2, ..., N \end{cases} \tag{3.1}$$

In general, a master BMS can also be used for module SOC balancing in the CHB, but the SOC balancing based on PWM algorithms is more advantageous. First, the hardware cost of the master BMS can be saved. Second, the imbalanced energy of the battery modules is also used to drive the vehicle, instead of being dissipated by the BMS. In the end, in most cases, the speed of balancing using eq. (3.1) is faster than a master BMS [120], because the balancing power is a portion of the system power, instead of being restricted by a dissipation resistor.

It is worth noting that the SOC balancing approach is applicable regardless of the waveform of u_{ref}. That means this approach is usable in all scenarios, including discharging, DC charging, and AC charging. Nonetheless, as the introduction of SOC balancing only aims to explain the operational mechanism of the CHB, the discussion is not extended further. Different balancing algorithms are available in the dedicated studies [114]–[117]. SOC balancing is also a main subtopic in the dissertation of a researcher from the same research institute, Mr. Felix Roemer.

3.3 Specifications of the CHB for Further Analysis

In the previous two sections, the CHB is first proposed as the overall concept to solve the partial load efficiency problem. Then the general operational mechanisms of the CHB are introduced,

including the PWM algorithm and module SOC balancing approach. In order to conduct quantitative comparisons to the benchmarked IGBT inverter, the general concept should be specified in the following parts of the dissertation. Therefore, this section specifies the configurations of the CHB for further discussions. The CHB is configured to match the specifications of the benchmarked IGBT inverter. This CHB will be used thereafter in the dissertation for all the quantitative investigations.

The CHB is shown in Figure 3.11. It contains three submodules per phase, and nine submodules in total. In order to match the electrical performance, the specifications must be identical to the benchmarked inverter. Therefore, in order to match the maximum continuous current of the benchmarked IGBT inverter, 600 A, six Si MOSFETs IPP100N10S3-05 are paralleled at each switch position in the CHB. The nominal voltage of each battery module is set to be 60 V, so that the maximum swing of the output AC voltage is also 360 V (-180 V to 180 V). The voltage redundancies of the two inverters are also well matched, 44.6 % for the benchmark IGBT inverter, 40 % for the CHB. The voltage redundancy is defined by the maximum voltage of the selected switch and the actual DC voltage it is blocking [98]. The match of this value manifests that the voltage of the switches selected for the CHB is not overrated or underrated. For the components outside the inverter circuit, two inverters are identical. Therefore, to simulate the CHB in driving cycles, the vehicle model and the motor model in section 2.1.2 can still be used and kept unchanged.

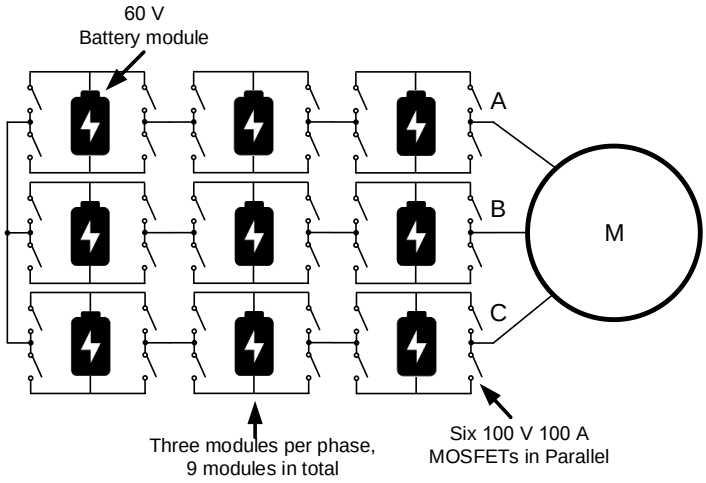


Figure 3.11: The configuration of the CHB to be used for further analysis

It is worth mentioning that the Si MOSFET and the configurations of the instance are not specifically chosen or optimized. The MOSFET IPP100N10S3-05 is arbitrarily selected from the automotive MOSFETs family of Infineon. The 60 V nominal voltage of battery modules is also configured to match the maximum AC output voltage of the benchmarked inverter. There are many other possible configurations using different automotive MOSFETs [50]. Additionally, only because of the availability of their parameters, discrete components are used for the CHB. This is not a recommendation to use discrete components in practical implementations. Switch modules could be a better choice for practical applications [50].

The intention of comparing an arbitrarily configured CHB with the benchmarked IGBT inverter is to prove the general effectiveness of the concept. Once the improvements of the arbitrarily configured CHB are confirmed, the overall concept of the CHB can be proven to be generally advantageous as well.

Additionally, as SiC MOSFET inverters are also promising to solve the partial load efficiency problem, a SiC MOSFET inverter is added to the efficiency comparison and the cost comparison, in order to obtain an overview of the performance of different solutions. For the SiC MOSFET inverter, the switch C2M0025120D from Cree is selected, because this switch represents the state-of-art performance of SiC MOSFETs. The on-state resistance of this switch is the lowest among all the discrete SiC MOSFETs available on the market (bare dies and modules are excluded). To match the continuous operation current of the benchmarked IGBT inverter, six SiC MOSFETs are paralleled at each switch position. However, as most SiC MOSFETs are rated at either 1200 V or 900 V, the voltage redundancy is inevitably higher than that of the CHB and the benchmarked IGBT inverter.

The specifications of the three inverters to be compared are listed in Table 3.2. Besides the specifications explained above, the values of the gate resistance and the switching frequency are also provided. The value of the gate resistance influences the switching loss significantly. In order to prove that the comparison is fair for the three inverters, the values of the gate resistance are set to be the same, as shown in Table 3.2. For the switching frequency, the switching frequencies of the two MOSFET inverters are 20 kHz, in order to demonstrate the high frequency capability of MOSFETs. The switching frequency of the benchmarked IGBT inverter remains 8 kHz to demonstrate the realistic performance of a state-of-the-art inverter.

Table 3.2: Specifications of the three inverters to be compared

Specifications	Si IGBT (Benchmark)	SiC MOSFET	CHB
Output voltage (phase peak value)	180 V	180 V	180 V
Rated current (75 °C RMS value)	600 A	600 A	600 A
DC voltage	360 V	360 V	60 V per module
Selected switch	FS800R07A2E3	C2M0025120D	IPP100N10S3-05
Maximum voltage of the switch	650 V	1200 V	100 V
Voltage redundancy of switch	44.6 %	70 %	40 %
Gate resistance	2.2 Ω	2.2 Ω	2.2 Ω
Number of submodules	1	1	9
Number of parallel	1	6	6
Total number of switches	6 (in one module)	36	216
Output switching frequency	8 kHz	20 kHz	20 kHz

Table 3.2 only contains the most important specification values of the three inverters. To avoid a large amount of details in the main text, more parameter values are provided in Appendix A1. With the configurations of the CHB and the SiC MOSFET inverter specified, the next chapter compares the efficiency of the three inverters quantitatively.

4 Efficiency

This chapter first reviews previous studies on the efficiency modelling of the CHB or other multilevel inverters using Si MOSFETs. Then based on the research gap, the loss model of the CHB is constructed. The loss of the SiC MOSFET inverter is modelled by modifying an existing model for six-pack Si MOSFET inverters. The two loss models are verified and put into the powertrain simulation model in Figure 2.4, in order to verify the efficiency improvements of the two inverters in driving cycles. In the end, the results of the CHB in terms of efficiency are discussed in detail and compared to the existing approaches discussed in chapter 2.

4.1 State of the Art Studies on the Efficiency of CHB

As stated in the previous chapter, although several studies also propose to use the CHB or similar circuits for BEVs, their motivations are to realize the SOC balancing via PWM algorithms, instead of the efficiency improvement. Therefore, few studies have conducted efficiency modelling or comparisons for the CHB or other cascaded multilevel inverters in BEVs.

[114]–[117] and [123], [124] propose to use cascaded multilevel inverters in BEVs to balance the SOC of each individual battery cell via PWM algorithms. Each submodule thus has only one battery cell. The energy conversion efficiency is not within the scope of their research, and is not discussed at all. Nonetheless, as a considerable amount of switches are involved to balance each individual cell, the efficiency of the circuits in [114]–[117], [123], [124] is expected to be lower than that of the benchmarked IGBT inverter.

The efficiency deterioration is also supported by the discussions in [125]. In [125], a cascaded multilevel inverter with only one battery cell per module is proposed for BEVs. The loss of the proposed inverter is modelled. The loss model is not parametrized for a quantitative assessment, but [125] still generally indicates that the efficiency of the proposed inverter is rather limited, due to the significantly increased conduction loss caused by the high number of switches.

Different from [114]–[117], [123], [124], the Si MOSFET multilevel inverters in [126]–[128] adopt battery modules instead of battery cells. Quantitative efficiency assessments are also conducted. Nonetheless, their efficiency assessments are not based on driving cycles.

[126] models the efficiency of a Si MOSFET multilevel inverter, and concludes its efficiency is comparable to a SiC MOSFET inverter at nominal load. The efficiency in the partial load area is still missing. No comparison to the IGBT inverter is conducted, either.

[127], [128] compare the efficiency of a conventional IGBT inverter and a Si MOSFET multilevel inverter. The efficiency of inverters is simulated by sweeping the power from 0 to 100 % of the maximum power, and the improvements in partial load are visible. However, such a result cannot be further converted to the efficiency in driving cycles, as a driving cycle simulation requires efficiency maps, instead of an efficiency curve. The efficiency improvement reported in [128] is

also not a good representative for the performance of the CHB, as the inverter in [128] almost always engages diodes while conducting current, and its conduction loss model thus still contains linear terms. Therefore, using the results in [128], the efficiency of the CHB tends to be underestimated.

The efficiency comparisons in driving cycles are conducted in [129], [130]. Models of vehicle and motors are developed by the two studies, in order to compare the efficiency of an IGBT inverter and a Si MOSFET multilevel inverter quantitatively in driving cycle simulations.

[129] simulates the two inverters in a compact car with driving cycles and compares their total losses. A significant loss reduction is observed in urban driving cycles. However, the 135 kW power of the motor and the two inverters tends to be oversized for the simulated vehicle with a weight of 1100 kg. The oversizing makes the inverters operate more often in the partial load area. The IGBT used for the comparison in the study is also not a state of the art model, because its zero-current forward voltage is 0.92 V. As a reference, the zero-current forward voltage of the IGBT in the reference vehicle is only 0.7 V [49]. Hence, the results could be inaccurate and biased toward the Si MOSFET multilevel inverter. Moreover, the improvement in partial load and the necessity to use Si MOSFETs are not specified in [129].

[130] compares the efficiency of two inverters in a Nissan Leaf ZE0. Driving cycle simulations are performed for the comparison as well. The efficiency improvement of cascaded multilevel inverter in the partial load area is also briefly described by [130]. Nonetheless, the configurations of the simulation in [130] are not able to accurately simulate the electric powertrain of a Nissan Leaf ZE0. First, the IGBT used for the comparison in the study is also not a state-of-the-art model. Second, the switching frequency of the IGBT is 20 kHz, much higher than the common values of automotive inverters, 5-10 kHz [131], which tends to underestimate the efficiency of the IGBT inverter. Furthermore, it is also observed that the motor used in the simulation is not an automotive motor, but an industrial motor. That can be proven by the nominal frequency of the selected motor, which is only 50 Hz. In comparison, an automotive motor is usually rated at a much higher frequency and in general more efficient [52], [132], [133]. The usage of the industrial motor model further distorts the results of the comparison.

As the energy consumption results are highly likely to be distorted, the efficiency improvement of the CHB cannot be directly confirmed by the simulation results in [129], [130]. The results in [129], [130] indicate a positive direction, but estimating the cost reduction of the CHB is not possible, because no accurate results of the energy savings can be provided. Therefore, based on the results of [129], [130], it is not possible to decide if the CHB concept is worth implementing.

Studies regarding the efficiency of Si MOSFET multilevel inverters are summarized in Table 4.1. As observed, a quantitative and accurate efficiency assessment of the CHB or similar inverters has not been conducted in a well-configured BEV powertrain model. The targets of implementing Si MOSFET multilevel inverters are also mostly not to improve the powertrain efficiency, but to use the SOC balancing capability. Hence, in previous studies, the efficiency of the inverters is only generally analyzed to prove that the efficiency is not a disadvantage. Discussions and analysis regarding the efficiency in driving cycles are limited.

To verify if the CHB is able to outperform the benchmarked IGBT inverter, a loss model of the CHB is developed in the next section. The state-of-the-art SiC inverter introduced in chapter 3 is also modelled and compared, in order to obtain an additional reference for the performance of the CHB. The accuracy of the two models is verified first. Then the two models are plugged into the powertrain model in Figure 2.4 for driving cycle simulations.

Table 4.1: Summary of the studies on the efficiency Si MOSFET multilevel inverters

Literature	Aspects of efficiency research in literature		
	Quantitative efficiency analysis	Driving cycle simulation	Powertrain model quality
[114]–[116], [123], [124]	Not conducted	Not conducted	No powertrain model
[125]	Yes	Not conducted	No powertrain model
[126]–[128]	Yes	Not conducted	No powertrain model
[129][130]	Yes	Yes	Not well configured

4.2 Approach

As there is no model directly available to evaluate the efficiency of the CHB, this section first develops the loss model for the CHB. The losses of the SiC MOSFET inverter are also modelled, following the modelling approach of a six-pack Si MOSFET inverter in [134]. The two models have the same inputs and outputs as the IGBT loss model in eq. (2.1), so that they can be easily incorporated in the powertrain simulation model in Figure 2.4 to obtain the average efficiency in driving cycles. Besides the development of the two models, their accuracy is also verified in this section.

4.2.1 Loss Model of the CHB

To simplify the loss modelling, following assumptions are made. First, the CHB is assumed to use the PSC-PWM algorithm introduced in section 3.2.1. All the battery modules are assumed to be perfectly balanced, so that the DC voltage, u_{DC}, of each H-bridge is identical. Combining the two assumptions together, all the MOSFETs in the CHB can be deemed working identically. Hence, each MOSFET in the CHB also has exactly the same switching loss and conduction loss. Due to the identical losses on each MOSFET, the modelling of the whole CHB can be simplified to the modelling of one MOSFET.

The conduction loss of one MOSFET is modelled first. As the MOSFET is a unipolar switch, in the turned-on state, the current can be conducted in both directions like in a resistor, either from the source node to the drain node, or in the opposite direction [129]. When the current is not high enough to turn on the anti-paralleled diode, i.e., only the MOSFET channel is conducting the current, the conduction loss on the MOSFET is the same as that on a resistor. Such a situation happens, when the voltage drop on the MOSFET channel is constantly lower than the zero current forward voltage of the anti-paralleled diode, u_{F0}, as described by the condition in eq. (4.1). R_{on} is the on-state resistance of the MOSFET. $I_{\mathrm{P\_RMS}}$ is the RMS value of the phase AC current. n_{p} is the number of paralleled MOSFETs.

$$\sqrt{2} I_{\mathrm{P\_RMS}} R_{\mathrm{on}} / n_{\mathrm{p}} <= u_{\mathrm{F0}} \tag{4.1}$$

Once eq. (4.1) holds, for a CHB composed of *N* submodules in each phase, as the AC current flows through 2*N* MOSFET channels in one phase, the conduction loss of one phase is the total loss on the 2*N* on-state resistors. Accordingly, the total conduction loss of three phases in a CHB,

$P_{\mathrm{C\_CHB}}$, is the loss on 6*N* on-state resistors. Considering the number of paralleled switches, the total conduction loss of the CHB can be calculated using eq. (4.2).

$$P_{\mathrm{C\_CHB}} = 6NI_{\mathrm{P\_RMS}}^2 R_{\mathrm{on}} / n_{\mathrm{p}} \quad \text{if } (\sqrt{2} I_{\mathrm{P\_RMS}} R_{\mathrm{on}} / n_{\mathrm{p}} \le u_{\mathrm{F0}}) \tag{4.2}$$

Nonetheless, if condition eq. (4.1) does not hold anymore, the modelling of the conduction loss will be more complicated. The modelling needs to start from the conduction loss of a single MOSFET within one switching period, T_{S}. As T_{S} is in general much shorter than the period of the output AC voltage, T_{AC}, the reference voltage and the AC current can be deemed as constants in each T_{S}. Hence, the conduction loss of one MOSFET and one anti-paralleled diode can be calculated in each T_{S}. Summing the conduction losses over one AC period, T_{AC}, the average power of the conduction loss on one MOSFET, $P_{\mathrm{C\_MOS}}$, and on one diode, $P_{\mathrm{C\_Diode}}$, can be obtained. The analytical solutions are given in eq. (4.3). As the whole CHB contains $12Nn_{\mathrm{p}}$ switches in total, the total conduction loss, $P_{\mathrm{C\_CHB}}$, is obtained by multiplying the results of one switch with $12Nn_{\mathrm{p}}$.

$$\begin{cases} P_{\mathrm{C\_MOS}} = 2R_{\mathrm{on}} I_{\mathrm{P\_RMS}}^2 \left(\frac{1}{8} + \frac{m_a \cos\theta}{3\pi}\right) / n_{\mathrm{p}}^2 \\ P_{\mathrm{C\_Diode}} = \sqrt{2} u_{\mathrm{F0}} I_{\mathrm{P\_RMS}} \left(\frac{1}{2\pi} - \frac{m_a \cos\theta}{8}\right) / n_{\mathrm{p}} + 2R_{\mathrm{d}} I_{\mathrm{P\_RMS}}^2 \left(\frac{1}{8} - \frac{m_a \cos\theta}{3\pi}\right) / n_{\mathrm{p}}^2 \\ P_{\mathrm{C\_CHB}} = 12Nn_{\mathrm{p}} \left(P_{\mathrm{C\_MOS}} + P_{\mathrm{C\_Diode}}\right) \end{cases} \tag{4.3}$$

$$\text{if } (\sqrt{2} i_{\mathrm{P\_RMS}} R_{\mathrm{on}} / n_{\mathrm{p}} > u_{\mathrm{F0}})$$

$$m_a = \frac{U_{\mathrm{P}}}{N u_{\mathrm{DC}}} \tag{4.4}$$

In eq. (4.3), $\cos\theta$ is the power factor, following the same definition as in the model of the benchmarked IGBT inverter, eq. (2.1). Nonetheless, the definition of the modulation index, m_{a} is slightly different from that of eq. (2.1). For the CHB, m_{a} is defined by dividing the peak phase voltage, U_{P}, with the summed battery module voltage in one phase, Nu_{DC}, eq. (4.4). Besides, it is also worth noting that the derivation of eq. (4.3) is not trivial. The detailed derivation process is provided in a publication [50].

After obtaining the conduction loss model in two different situations, the switching loss is further modelled. For the MOSFETs, only the worst-case switching loss is modelled for simplification. During a switching-on transient of MOSFETs, in the worst case, the voltage only starts to fall when the current reaches the load current, and vice versa for a worst-case switching-off transient. Hence, in one cycle of turning-on and -off, the worst-case energy loss of one MOSFET can be calculated based on the falling/rising time of the current and voltage. For the diode, in the worst case, all the recovery charge, Q_{rr}, is assumed to be transferred from u_{DC} to 0 V. Such an assumption results in an energy loss of $Q_{\mathrm{rr}} u_{\mathrm{DC}}$ in each recovery of the diode.

Multiplying the energy loss values with f_{s}, the worst case switching-loss of one MOSFET, $P_{\mathrm{S\_MOS}}$ and its anti-paralleled diode $P_{\mathrm{S\_Diode}}$ can be obtained as in eq. (4.5). The total switching loss of CHB, $P_{\mathrm{S\_CHB}}$, is obtained by multiplying the switching loss of one MOSFET with the number of switches, $12Nn_{\mathrm{p}}$. In eq. (4.5), t_{RI}, t_{FU}, t_{FI} and t_{RU} are respectively the rising time of current, falling time of voltage, falling time of current, and the rising time of voltage.

Combining eq. (4.2), (4.3), and (4.5), the total loss of the CHB can be calculated, eq. (4.6). f_{SO} is the overall switching frequency observed at the AC output. For the PSC-PWM algorithm, f_{SO}

is $2N$ times f_s [128]. To improve the accuracy of the model, a thermal model is also implemented, following the same approach as the IGBT thermal model, Figure 2.3. All the required parameters are given in Appendix A1.

$$\begin{cases} P_{\text{S\_MOS}} = \dfrac{\sqrt{2} f_{\text{S}} u_{\text{DC}} I_{\text{P\_RMS}}}{2\pi n_{\text{p}}} (t_{\text{RI}} + t_{\text{FU}} + t_{\text{FI}} + t_{\text{RU}}) \\ P_{\text{S\_Diode}} = f_{\text{S}} Q_{\text{rr}} u_{\text{DC}} \\ P_{\text{S\_CHB}} = 12 N n_{\text{p}} (P_{\text{S\_MOS}} + P_{\text{S\_Diode}}) \end{cases} \tag{4.5}$$

$$P_{\text{CHB\_Loss}} = P_{\text{C\_CHB}} + \frac{6\sqrt{2} f_{\text{SO}} u_{\text{DC}} I_{\text{P\_RMS}}}{\pi} (t_{\text{RI}} + t_{\text{FU}} + t_{\text{FI}} + t_{\text{RU}}) + 6 n_{\text{p}} f_{\text{SO}} Q_{\text{rr}} u_{\text{DC}} \tag{4.6}$$

The loss model of the CHB is derived based on the PSC-PWM algorithm, but this model is also generally applicable for other PWM algorithms without significant errors. That is because the switching loss and the conduction loss are independent of the PWM algorithm. For the switching loss, as long as the required f_{SO} of the output AC voltage is given, the total times of switch-on and switch-off per second of the whole inverter are defined. The switching loss is only determined by f_{SO}, regardless of the choice of the PWM algorithm. For the conduction loss, no matter which PWM algorithm is used, the load current still flows through the same number of switches (either diodes or MOSFETs). Hence, the total conduction loss always follows the pattern described in eq. (4.2) and (4.3). The conduction loss is not directly influenced by the PWM algorithm, either. In fact, even without the assumption of PSC-PWM, the final analytical solution still stays the same. The change of the PWM algorithm only influences the derivation process of the total loss.

The main influence of the PWM algorithm is on the heat distribution among switches. When the PSC-PWM is used, the total loss is strictly equally distributed on each switch. All the switches are thus expected to have the same junction temperature and the same parameters for the loss model. If another PWM algorithm is chosen, the switch junctions cannot have an identical temperature anymore. The thermal model implemented for PSC-PWM will inevitably cause some errors, which further leads to the errors of the parameters and the total loss. Therefore, the developed loss model in eq. (4.6) is still expected to cause insignificant errors for other PWM algorithms, although the formula is formally correct.

4.2.2 Loss Model of the SiC MOSFET Inverter

In addition to the loss model of the CHB, this section also models the total loss of the state-of-the-art SiC MOSFET inverter, to provide a better overview regarding the efficiency of different inverters. For a six-pack SiC MOSFET inverter, the pattern of the conduction loss is similar to that of the CHB. When the current is low and not able to turn on the anti-paralleled diodes, the MOSFET channels are conducting the current all the time. Thus the conduction loss of one SiC MOSFET, $P_{\text{C\_SiC}}$, and one diode, $P_{\text{C\_Doide}}$, can be calculated by eq. (4.7).

$$\begin{cases} P_{\text{C\_SiC}} = 3 R_{\text{on}} I_{\text{P\_RMS}}^2 / n_{\text{p}}^2 \\ P_{\text{C\_Diode}} = 0 \\ \text{if } \sqrt{2} R_{\text{on}} I_{\text{P\_RMS}} / n_{\text{p}} \le u_{\text{F0}} \end{cases} \tag{4.7}$$

When the current is high enough to trigger the conduction of the anti-paralleled diodes, the formula in [134] for a six-pack Si MOSFET inverter can be used instead, eq. (4.8). As the SiC

MOSFET inverter also has the six-pack structure, the definition of the modulation index, m_{a}, in eq. (4.8) is the same as that in the IGBT inverter loss model, eq. (2.1).

$$\begin{cases} P_{\mathrm{C\_SiC}} = 2R_{\mathrm{on}} I_{\mathrm{P\_RMS}}^2 \left(\frac{1}{8} + \frac{m_a \cos\theta}{3\pi}\right) / n_{\mathrm{p}}^2 \\ P_{\mathrm{C\_Diode}} = u_{\mathrm{F0}} \sqrt{2} I_{\mathrm{P\_RMS}} \left(\frac{1}{2\pi} - \frac{m_{\mathrm{a}} \cos\theta}{8}\right) / n_{\mathrm{p}} + 2R_{\mathrm{D}} I_{\mathrm{P\_RMS}}^2 \left(\frac{1}{8} - \frac{m_{\mathrm{a}} \cos\theta}{3\pi}\right) / n_{\mathrm{p}}^2 \\ \text{if } \sqrt{2} R_{\mathrm{on}} I_{\mathrm{P\_RMS}} / n_{\mathrm{p}} > u_{\mathrm{F0}} \end{cases} \tag{4.8}$$

The total switching loss of the SiC MOSFET inverter, $P_{\mathrm{S\_Total}}$ is modelled differently from that of a Si MOSFET inverter, eq. (4.9). First, the recovery loss of the SiC diode is zero in the model, because the recovery loss of the SiC diode is negligible, compared to the recovery loss of Si diodes [78]. Second, the switching loss of the SiC MOSFET is not modelled directly with the rising/falling time values, because this worst-case approximation tends to over-estimate the switching loss of a SiC MOSFET significantly. Instead, a linear model is used for the switching loss, eq. (4.9), due to the linear dependence of the switching loss on current and voltage [135].

$$\begin{cases} P_{\mathrm{C\_Total}} = 6n_{\mathrm{p}} \left(P_{\mathrm{C\_SiC}} + P_{\mathrm{C\_Diode}}\right) \\ P_{\mathrm{S\_Total}} = 6n_{\mathrm{p}} f_{\mathrm{s}} u_{\mathrm{DC}} \left(a_{\mathrm{SiC}} + b_{\mathrm{SiC}} \frac{2\sqrt{2} I_{\mathrm{P\_RMS}}}{\pi}\right) \\ P_{\mathrm{SiC\_Loss}} = \left(P_{\mathrm{C\_Total}} + P_{\mathrm{S\_Total}}\right) \end{cases} \tag{4.9}$$

The parameters of the linear model, a_{SiC} and b_{SiC} can be obtained via a linear regression of the switching loss data in the datasheet. Adding the total conduction loss to the switching loss, the total loss of the SiC MOSFET inverter, $P_{\mathrm{SiC\_Loss}}$, can be obtained, eq. (4.9). All the parameter values of the SiC MOSFET inverter are given in Appendix A1.

As the SiC MOSFET inverter and the CHB are not standard products, like the IGBT inverter, datasheet values of on-shelf products are not available to verify the accuracy of the models. Therefore, the accuracy of the models is still verified by ANSYS Simplorer. The models in ANSYS Simplorer are experimentally proven to have a high accuracy [55], [56]. Because the ANSYS models simulate detailed behaviors of semiconductors, and requires a simulation time step in microsecond level, these models are too slow for driving cycle simulations. Therefore, ANSYS Simplorer is only used for verifications, instead of being directly used in driving cycle simulations. Comparing the modelled efficiency to the results of ANSYS Simplorer, the errors of the two models are proven to be within ±1 % at the operational points commonly used by BEVs.

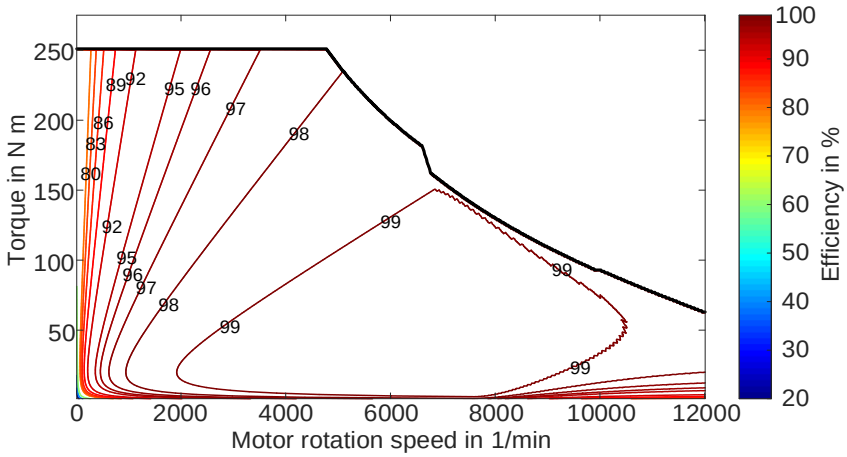
Besides the verification with the accurate simulations, the accuracy of the CHB loss model is also verified experimentally on the module level. The experimental results indicate that the error of the CHB loss model is within ±1 % at the operational points commonly used by BEVs. The verifications confirmed the loss models in this section are accurate. Hence, the modes can be used to generate accurate results in driving cycle simulations. To avoid listing a large amount of verification data in the main text, the details of verifications are provided in Appendix A2.

4.3 Results

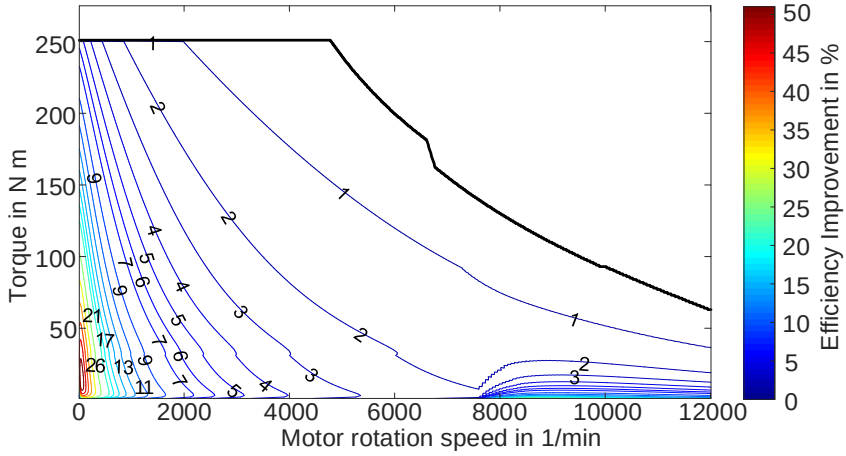
Using the loss models constructed in the previous section and the powertrain model in Figure 2.4, the efficiency maps and driving cycle performance of the two inverters can be obtained. The

average efficiency of the two inverters is also defined by the energy throughput observed on the AC side of inverters, following eq. (2.4). The efficiency maps of the CHB and the SiC MOSFET are depicted in Figure 4.1 and Figure 4.2 respectively. Using the benchmarked IGBT as the reference, the maps of the efficiency improvement are also plotted.

First, according to Figure 4.1(a), a rather high efficiency in the whole range of speed is achieved by the CHB. When the motor speed is higher than 4000 1/min, compared to the benchmarked inverter, the efficiency is improved by 2-3 %, Figure 4.1(b). In the area of lower speed, the improvement is more significant. As observed in Figure 4.1(b), the efficiency improvement in comparison to the benchmarked IGBT inverter is in the range of 4-10 %, when the speed is lower than 4000 1/min, corresponding to a vehicle speed of 50 km/h. Such a range of speed is sufficient to cover most urban driving scenarios.



(a) Efficiency map of the CHB [50]

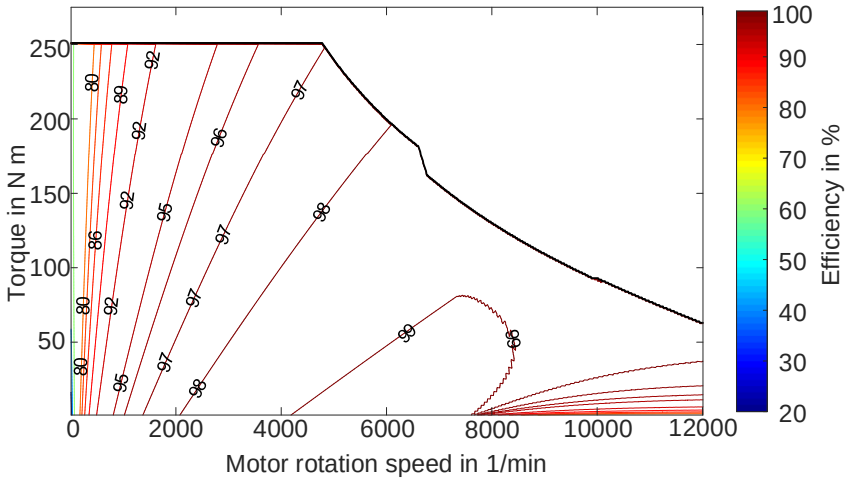


(b) Map of efficiency improvement compared to the IGBT

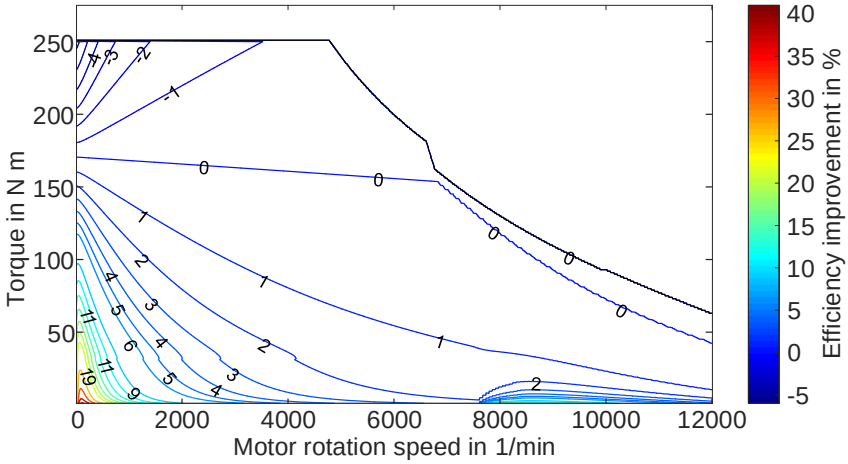
Figure 4.1: Efficiency map and the map of efficiency improvement of the CHB

Second, the SiC MOSFET inverter also enlarges the high efficiency area compared to the benchmarked IGBT inverter, Figure 4.2(a). The threshold motor speed to reach 97 % efficiency is reduced from 4000 1/min (for the IGBT inverter) to lower than 2000 1/min. However, the SiC MOSFET inverter is not able to realize an efficiency improvement in the whole map, as observed in Figure 4.2(b). When the torque is higher than 170 N m, the efficiency improvement becomes negative. Nonetheless, a motor torque of 170 N m corresponds to an acceleration of 4.68 m/s^2 for the reference vehicle. Even for sporty drivers, the operation points in this area are also not

frequently used [136]. Hence, in driving cycle simulations or realistic driving tests, the average efficiency can still be improved.



(a) Efficiency map of the SiC MOSFET inverter [50]



(b) Map of efficiency improvement compared to the IGBT

Figure 4.2: Efficiency map and the map of efficiency improvement of the SiC MOSFET inverter

With the improvements observed in the efficiency maps, a significant efficiency improvement can also be expected in the driving cycle simulations. The driving cycle simulation results of the SiC MOSFET inverter and CHB are respectively listed in Table 4.2 and Table 4.3. All the energy values are converted to kWh/100 km for the convenience of comparison. Their efficiency improvements and loss reductions compared to the benchmarked IGBT inverter are also included in the tables.

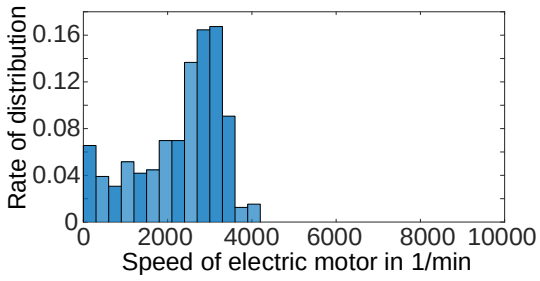
As expected, the efficiency of the two inverters is higher than that of the IGBT inverter in all the driving cycles. Nonetheless, the extent of the improvement is determined by the driving scenarios. The efficiency improvements of the two inverters are most significant in urban driving cycles, around 10 %, because the motor speed is almost constantly lower than 4000 1/min, Figure 4.3(a). In comprehensive driving cycles, because the vehicle only drives about 50 % of the time below 4000 1/min, Figure 4.3 (b), the efficiency improvements are comparatively lower, but still in the range of 5-8 %. However, in highway driving cycles, the improvement is limited to 2-3 %. This can be explained by the fact that the motor speed is mostly above 6000 1/min in a highway driving scenarios, Figure 4.3(c). The efficiency improvements of the two inverters are less significant in the area with a higher speed.

Table 4.2: Driving cycle simulation results and efficiency improvements of the CHB

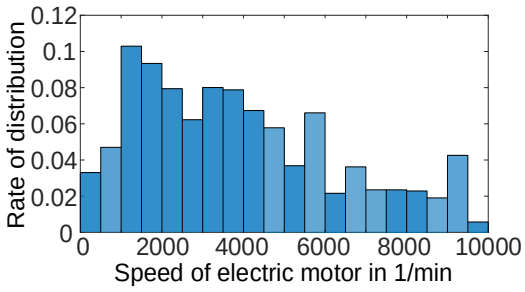
Driving cycles		BEV energy consumption	Inverter loss	Inverter efficiency	Efficiency improvement	Loss reduction
Urban cycles	USA NECC	6.9 kWh	0.76 kWh	97.2 %	11.0 %	3.4 kWh
	Europe City	6.4 kWh	0.30 kWh	98.1 %	11.3 %	2.0 kWh
	USA City II	6.8 kWh	0.32 kWh	98.1 %	9.3 %	1.7 kWh
Compre-hensive cycles	FTP72	8.2 kWh	0.27 kWh	98.4 %	7.6 %	1.5 kWh
	NEDC	9.9 kWh	0.17 kWh	98.9 %	7.0 %	1.2 kWh
	WLTP C3	11.8 kWh	0.17 kWh	99.1 %	5.4 %	1.0 kWh
Highway cycles	Artemis 130	17.5 kWh	0.11 kWh	99.4 %	2.8 %	0.6 kWh
	Artemis 150	18.5 kWh	0.13 kWh	99.4 %	2.9 %	0.6 kWh

Table 4.3: Driving cycle simulation results and efficiency improvement of the SiC MOSFET inverter

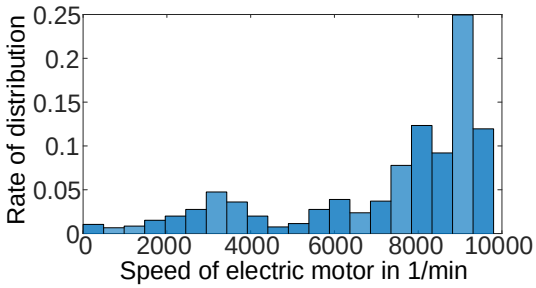
Driving cycles		BEV energy consumption	Inverter loss	Inverter efficiency	Efficiency improvement	Loss reduction
Urban cycles	USA NECC	7.5 kWh	1.36 kWh	95.0 %	8.8 %	2.8 kWh
	Europe City	6.6 kWh	0.54 kWh	96.5 %	9.7 %	1.8 kWh
	USA City II	7.0 kWh	0.58 kWh	96.6 %	7.8 %	1.5 kWh
Compreh ensive cycles	FTP72	8.4 kWh	0.49 kWh	97.2 %	6.4 %	1.3 kWh
	NEDC	10.0 kWh	0.31 kWh	98.1 %	6.2 %	1.1 kWh
	WLTP C3	11.9 kWh	0.31 kWh	98.3 %	4.6 %	0.9 kWh
Highway cycles	Artemis 130	17.6 kWh	0.22 kWh	98.8 %	2.2 %	0.5 kWh
	Artemis 150	18.6 kWh	0.25 kWh	98.9 %	2.4 %	0.5 kWh



(a) USA City II driving cycle speed distribution



(b) WLTP C3 driving cycle speed distribution



(c) Artemis 130 driving cycle speed distribution

Figure 4.3: Motor speed distribution of different driving cycles [50]

Based on the simulation results and the verifications, it can be confirmed that the average efficiency of the CHB is generally higher than that of the benchmarked IGBT inverter, due to the significant efficiency improvement in the partial load area. Hence, one objective of the design, to improve the inverter efficiency, is successfully achieved by the CHB.

Another finding of the simulation is that the CHB also slightly outperforms the SiC MOSFET inverter in driving cycle simulations. To understand the results better, the CHB and the SiC MOSFET inverter are further discussed in the next section. Besides, the CHB is also compared to the other existing approaches summarized in chapter 2, in terms of the efficiency improvement.

4.4 Discussion

With the improvement of the CHB confirmed in the previous section, this section further compares the CHB to the existing solutions to the partial load efficiency problems. The comparison covers all three categories of methods discussed in chapter 2. The influences of the CHB on the efficiency of the battery and the motor are also discussed.

4.4.1 Comparison of SiC MOSFET Inverter and CHB

The SiC MOSFET inverter and the CHB are both able to outperform the IGBT inverter in terms of efficiency. Nonetheless, as shown in Table 4.3 and Table 4.2, the efficiency improvement of the SiC MOSFET inverter is relatively lower than that of the CHB. To explain the reason, the total switching losses and conduction losses of the two inverters per 100 km in different driving cycles are listed in Table 4.4 and analyzed.

In Table 4.4, it is first observed that the total conduction losses of the two inverters are similar in all the driving cycles. The difference in the efficiency cannot be explained by the conduction loss. The reason is that the equivalent on-state resistance values of the two inverters are rather close. Following the configurations in Appendix A1, the total on-state resistance in one phase of the CHB is 4 mΩ, while the resistance per phase of the SiC MOSFET inverter is 4.17 mΩ. Moreover, due to the high efficiency of the two inverters, their junction temperatures should be close to the ambient temperature. Hence, the on-state resistance values of the two inverters do not diverge much, even when considering the influence of the junction temperatures.

The difference in average efficiency is mainly attributed to the difference in switching losses between the two inverters. According to Table 4.4, although the switching loss of the SiC

MOSFET inverter is 75-80 % lower than that of the IGBT inverter in all the driving cycles, it is still significantly higher than the switching loss of the CHB, by a factor of 3-4.

That is because the SiC MOSFETs switch the whole DC link voltage, 360 V, while the Si MOSFETs in the CHB only turn on or off at the module DC voltage, 60 V. In addition, to reach the same switching frequency in the output AC voltage, the total times of switching of the two inverters are identical. That means each H-bridge switches much less frequently compared to the SiC MOSFET inverter, but the observed switching frequency in the output voltage waveform stays the same, because the switching of each H-bridge is aggregated in the AC output [118]. Therefore, theoretically, the switching loss of the SiC MOSFET inverter is 6 times the switching loss of the CHB. Nonetheless, as the SiC material lowers the energy loss per switching cycle, this factor is reduced from 6 to around 3-4, as observed in Table 4.4.

Based on the detailed analysis, the reduced switching loss is identified as the main reason for the higher efficiency of the CHB. Although the SiC MOSFET inverter uses more advanced semiconductor materials, the CHB still prevails due to the advanced circuit design. Hence, the effect of improving circuit design could be more significant than the effect of only using advanced switches.

Table 4.4: Switching and conduction losses of the three inverters in different driving cycles

Driving cycles	IGBT Inverter losses		SiC MOSFET inverter losses		CHB inverter losses	
	Conduction	Switching	Conduction	Switching	Conduction	Switching
USA NECC	0.72 kWh	3.45 kWh	0.53 kWh	0.84 kWh	0.50 kWh	0.26 kWh
Europe City	0.33 kWh	1.98 kWh	0.15 kWh	0.40 kWh	0.15 kWh	0.15 kWh
USA City II	0.32 kWh	1.76 kWh	0.19 kWh	0.38 kWh	0.19 kWh	0.13 kWh
FTP72	0.27 kWh	1.45 kWh	0.17 kWh	0.32 kWh	0.16 kWh	0.11 kWh
NEDC	0.19 kWh	1.20 kWh	0.08 kWh	0.23 kWh	0.08 kWh	0.09 kWh
WLTP C3	0.18 kWh	1.02 kWh	0.09 kWh	0.22 kWh	0.09 kWh	0.08 kWh
Artemis 130	0.12 kWh	0.61 kWh	0.07 kWh	0.16 kWh	0.07 kWh	0.04 kWh
Artemis 150	0.14 kWh	0.61 kWh	0.09 kWh	0.15 kWh	0.08 kWh	0.04 kWh

4.4.2 Comparison to DC Voltage Shifting Approaches

After the comparison with the SiC MOSFET inverter, the CHB is also compared to the DC voltage shifting approaches [63]–[72] in the reference vehicle. As these approaches aim to reduce the IGBT switching loss by shifting the DC link voltage, their improvements can be calculated based on the switching loss profiles and the AC voltage profiles of the benchmarked inverter, which are already obtained in driving cycle simulations.

Additionally, for the approaches capable of adjusting voltage continuously [63]–[70], the efficiency of DC/DC conversion is assumed to be a constant, 98 %, which is rather optimistic but achievable with the state-of-the-art design [67]. For the approach shifting DC voltage by actively reconfiguring the battery pack [71], [72] (battery pack switching), the battery pack is assumed to

be able to provide full DC link voltage u_{DC} and half DC link voltage $u_{\mathrm{DC}}/2$. The losses on the switches in the battery pack are negligible, according to the results in [71].

Applying the calculation method and the assumptions, the efficiency improvement, $\Delta\eta$, and the energy consumption reduction, ΔE, of each DC voltage shifting approach are obtained and summarized in Table 4.5. The reference of the comparison is still the benchmarked IGBT inverter in the reference vehicle. The reduced energy consumptions are converted to kWh/100 km. Negative values mean deterioration of the efficiency and energy consumptions. Due to the optimistic assumptions implemented, the improvements of the two voltage shifting approaches should be able to represent their best-case results. The efficiency improvements and energy consumption reductions of the CHB are also included in Table 4.5, for the convenience of comparison.

As visible in Table 4.5, the efficiency improvement of the CHB is more significant than that of the DC voltage shifting approaches in [63]–[72]. In urban and comprehensive driving cycles, the efficiency improvement of the CHB is approximately 100 % higher than the improvements of the other two approaches. Correspondingly, the reduction of the energy consumption is also much more significant. In highway driving cycles, the advantage of the CHB concept is more obvious. The improvements of the DC voltage shifting approaches are negligible or even negative, while the CHB can still realize a significant improvement.

The reason for the outperformance of the CHB is that the DC voltage shifting approaches only reduce the switching loss of IGBTs in low speed scenarios. The switching loss stays unchanged when the vehicle is driving at a high speed, because the inverter requires a full DC link voltage in this case. Another reason is that the conduction loss of the IGBT inverter is not reduced at all by the DC voltage shifting approaches. In fact, according to the simulation results in Table 4.4, the conduction loss of the IGBT inverter is already higher than the total loss of the CHB in all driving cycles. Therefore, even if the DC voltage shifting approaches could eliminate the switching loss of the IGBTs, the achieved efficiency improvements would still be lower than that of the CHB.

Table 4.5: Improvements of DC voltage shifting solutions and the CHB, compared to the IGBT inverter

Driving cycles	Continuous voltage shifting		Battery pack switching		CHB	
	$\Delta\eta$	ΔE	$\Delta\eta$	ΔE	$\Delta\eta$	ΔE
USA NECC	7.2 %	2.35 kWh	5.4 %	1.79 kWh	11.0 %	3.4 kWh
Europe City	6.4 %	1.21 kWh	5.4 %	1.04 kWh	11.3 %	2.0 kWh
USA City II	4.7 %	0.90 kWh	4.4 %	0.86 kWh	9.3 %	1.7 kWh
FTP72	3.1 %	0.65 kWh	3.2 %	0.68 kWh	7.6 %	1.5 kWh
NEDC	2.2 %	0.44 kWh	2.5 %	0.49 kWh	7.0 %	1.2 kWh
WLTP C3	0.8 %	0.16 kWh	1.5 %	0.30 kWh	5.4 %	1.0 kWh
Artemis 130	-1.2 %	-0.29 kWh	0.3 %	0.08 kWh	2.8 %	0.6 kWh
Artemis 150	-1.4 %	-0.31 kWh	0.4 %	0.08 kWh	2.9 %	0.6 kWh

Additionally, the two types of DC voltage shifting approaches are also compared with each other. In urban driving cycles, the battery pack switching approach is less effective than the continuous shifting approaches. The reason is that the battery pack switching approach is not able to generate a DC voltage lower than $u_{\mathrm{DC}}/2$. The DC voltage cannot perfectly adapt to the low speed in urban driving scenarios.

In comprehensive driving cycles, the efficiency improvements of the two DC voltage shifting approaches are similar, in the range of 1-3 %. That is because high-speed scenarios and low-speed scenarios are approximately equally encountered in these driving cycles, and the features of the two approaches are not well manifested.

In highway driving scenarios, the efficiency improvement of continuous voltage shifting approaches turns to be negative, because the additional loss on the DC/DC conversion components becomes more significant and deteriorates the system efficiency. The improvements of the battery pack switching approach are still positive, but close to zero, due to the sparsity of the opportunity to reduce the DC voltage. Therefore, these two types of approaches are more appropriate for vehicles designed for urban and comprehensive driving scenarios, while they are not preferred in highway driving scenarios.

To summarize, in all driving scenarios, the efficiency improvement of the CHB is higher than the best-case improvements of the DC voltage shifting approaches. Moreover, the CHB is generally more advantageous, while the applicability of the DC voltage shifting approaches is restricted to urban or comprehensive driving scenarios. Specifically, according to the analysis, the continuous voltage shifting approaches are more suitable for low speed urban driving, while the battery pack switching approach is more appropriate for the comprehensive driving cycle with a mid-level speed.

4.4.3 Comparison to the Low Voltage Si MOSFET Inverter

Compared to the multiphase Si MOSFET inverter with a low voltage DC link [96], [97], the efficiency of the CHB is expected to be similar. That is because both concepts use low voltage Si MOSFETs, and the power handled by each submodule in the two concepts is similar. A detailed explanation is provided below.

First, the submodules in the two inverters are expected to perform similarly in terms of efficiency, as the basic submodules in both inverters are half bridges composed of low voltage Si MOSFETs. The submodule efficiency is mainly defined by the switch characteristics. Second, on the system level, in most cases, the system efficiency of the two concepts is the same as their submodule efficiency. That is because the whole system power is uniformly distributed to each half bridge in both inverters, unless specific control algorithms are implemented to change the power distribution significantly.

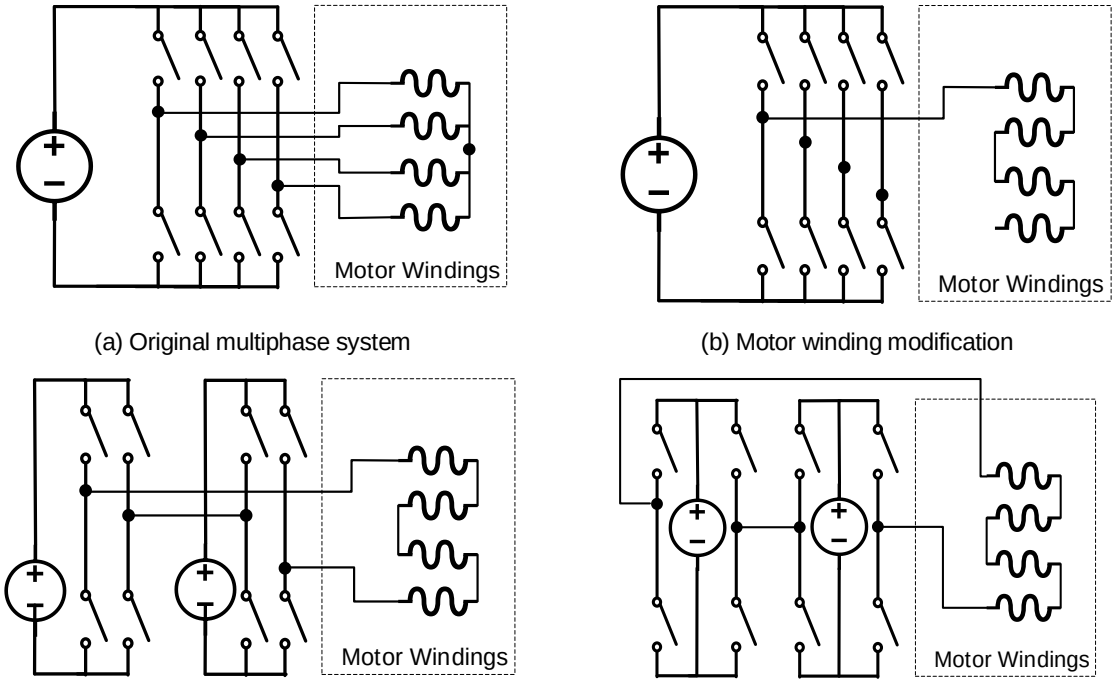
The uniform power distribution of the CHB is explained in section 3.2, while the control of the multiphase inverter is introduced in [96]. Therefore, combining the two factors, the two inverters are expected to have a similar system efficiency, when they are controlled by common algorithms. If improved algorithms are implemented to enhance the efficiency of the two inverters, the efficiency difference between the two inverters can slightly increase. Nonetheless, as the efficiency of both inverters is already rather close to 99 %, the expected deviation is limited.

Besides the similarity of the load distribution and submodule performance, the two concepts are also linked in terms of the circuit design. In fact, the concept of multiphase low voltage inverter

can be also deemed as a flattened version of the CHB. By rewiring the motor, inverter and the battery pack, a multiphase system can actually be converted to a CHB system, while the current and voltage of each MOSFET or motor winding are not changed at all.

An example of the rewiring is demonstrated in Figure 4.4. After the rewiring, four phases of a multiphase system are converted into a single-phase CHB system, which has two modules in cascade. The first step is to disconnect the motor and the inverter, and reconnect the star-shape connected windings in series, from Figure 4.4 (a) to (b). The second step is to split the DC link and form two H-bridges with the four half-bridge modules, from Figure 4.4 (b) to (c). The two H-bridges are also connected in series. The last step rearranges the layout of the circuit and obtains the common drawing of one phase of the CHB concept. No rewiring is conducted in this step.

After this rewiring process, at a certain operation point of the motor, each motor winding and each MOSFET still have the same voltage and current in terms of RMS value. Therefore, the two systems theoretically have exactly the same efficiency at all the operational points. The phase angle of the current is inevitably changed by the rewiring process, as the connection of the motor windings is changed from star-shape connection to series connection. Nonetheless, as long as the RMS values are kept the same, the efficiency of the system is expected to be unchanged.



(a) Original multiphase system

(b) Motor winding modification

(c) Forming and cascading H-bridges

(d) Stretch the CHB to the common shape

Figure 4.4: Converting a multiphase inverter to a single-phase CHB by rewiring

The differences between the two designs are in terms of their ohmic losses on the DC side and their control strategies. On the one hand, due to the low voltage DC link, the low voltage multiphase solution inevitably has higher ohmic losses on the cables and connectors on the DC side. On the other hand, the multiphase design has more degrees of freedom to control the motor, which can further optimize the efficiency [97]. However, as the two effects counter balance each other, on system level, the two solutions are still expected to have a similar performance in terms of efficiency.

To summarize, a multiphase Si MOSFET inverter with a low voltage DC link should have a rather similar efficiency map, compared to the CHB using the same number of MOSFETs. To conclude which solution is more appropriate for a specific scenario, aspects other than the efficiency need to be considered. As this chapter focuses on the efficiency, the discussion is not extended further.

4.4.4 Influence on Battery Loss and Motor Loss

The previous modelling and discussions focus purely on the efficiency of the inverter. In fact, the change of the inverter design can also slightly influence the losses on the batteries and the motor. As the CHB does not have a DC link and creates ripples in the battery current, the ohmic losses of the batteries could be increased. For the motor, because the CHB results in a lower THD compared to six-pack inverters, the copper loss of the motor caused by the harmonic current tends to be reduced. Therefore, this section investigates the battery loss and motor loss before and after implementing the CHB, in order to understand its impact on the system level efficiency.

First, for a high simulation speed, the ohmic losses of the batteries are not directly simulated in a circuit simulation software. Instead, the ohmic losses are calculated based on the equivalent circuit model (ECM) of battery cells, and the ripple current models of the CHB and the IGBT inverter. The cell ECM is parameterized according to the impedance spectrum of a 35 Ah lithium nickel manganese cobalt oxide (NMC) cell [137], which could better approximate the performance of the large NMC cells used in the reference vehicle. With the ECM, the resistance of the battery cells for current at different frequencies can be obtained.

The current ripples caused by the CHB are assumed not filtered at all. The RMS values of the ripples can be calculated by eq. (4.10), based on the average current of the batteries, $I_{\mathrm{bat\_ave}}$. It mainly contains ripple components at two frequencies, the switching frequency and the AC frequency. Combining the ripple components with the corresponding battery resistance, the total ohmic losses of the batteries in the CHB are obtained. The switching frequency ripple model is developed by [138]. $I_{\mathrm{bat\_S\_RMS}}$ and $I_{\mathrm{bat\_AC\_RMS}}$ are respectively the RMS values of the switching frequency ripples and AC frequency ripples. $R_{\mathrm{bat\_DC}}$, $R_{\mathrm{bat\_fs}}$ and $R_{\mathrm{bat\_AC}}$ are respectively the resistance of the batteries for the DC current, the switching frequency ripples, and the AC frequency ripples. To avoid the derivation details, the derivation of the low frequency ripples is given in Appendix A3.

$$\begin{cases} I_{\mathrm{bat\_RMS}} = \dfrac{2I_{\mathrm{bat\_ave}}}{\cos\theta}\sqrt{\dfrac{1+(1/3)\cos 2\theta}{\pi m_{\mathrm{a}}}} \\ I_{\mathrm{bat\_S\_RMS}} = \dfrac{2I_{\mathrm{bat\_ave}}}{\cos\theta}\sqrt{\dfrac{24-6\pi m_{\mathrm{a}}+(8-3\pi m_{\mathrm{a}})\cos 2\theta}{24\pi m_{\mathrm{a}}}} \\ I_{\mathrm{bat\_AC\_RMS}} = \sqrt{I^2_{\mathrm{bat\_RMS}} - I^2_{\mathrm{bat\_ave}} - I^2_{\mathrm{bat\_s\_RMS}}} \\ P_{\mathrm{bat\_ohmic}} = R_{\mathrm{bat\_DC}} I^2_{\mathrm{bat\_ave}} + R_{\mathrm{bat\_fs}} I^2_{\mathrm{bat\_s\_RMS}} + R_{\mathrm{bat\_AC}} I^2_{\mathrm{bat\_AC\_RMS}} \end{cases} \tag{4.10}$$

For the IGBT inverter, only the switching frequency ripples need to be considered. To obtain the RMS value of the ripple current, $I_{\mathrm{bat\_S\_RMS}}$, the model in [139] is used to calculate the RMS value of the envelope of voltage ripples, Δv_{pp}, on the DC-link capacitance, C_{DC} (475 µF for the benchmarked inverter). r_{ppIGBT} is a factor to determine the envelope of the ripples. For simplification, assuming the ripple current is triangle wave, the RMS value of the ripple current triggered by the ripple voltage can also be obtained eq. (4.11). Together with the corresponding

resistance values of the cells, the formula for the battery pack ohmic loss can be obtained. The details of the derivation are also in Appendix A3. Inserting the two models developed above into the driving cycle simulation framework, the ohmic losses of the batteries can be obtained. The results are in Table 4.6. All the energy values are still converted to kWh/100 km values for the convenience of comparison.

$$\begin{cases} r_{\mathrm{ppIGBT}} = -1.09 m_{\mathrm{a}}^2 + 0.74 m_{\mathrm{a}} \\ \Delta v_{\mathrm{pp}} = \dfrac{\sqrt{2} I_{\mathrm{AC\_RMS}} r_{\mathrm{ppIGBT}}}{3 C_{\mathrm{DC}} f_{\mathrm{S}}} \\ I_{\mathrm{bat\_S\_RMS}} = \Delta v_{\mathrm{pp}} / R_{\mathrm{bat\_fs}} / 3 \\ P_{\mathrm{bat\_ohmic}} = R_{\mathrm{bat\_DC}} I_{\mathrm{bat\_ave}}^2 + R_{\mathrm{bat\_fs}} I_{\mathrm{bat\_s\_RMS}}^2 \end{cases} \tag{4.11}$$

Second, the copper loss of the motor caused by the harmonic current is also simulated. The harmonic components in the AC current of the two inverters are calculated using the double Fourier analysis approach in [140] and [141]. The results in different driving cycles are provided in Table 4.6 as well. The harmonic current can indeed deteriorate other losses in the motor as well. Nonetheless, due to the limit of the research scope, only the copper loss on the stator windings is calculated in the discussion.

In the end, adding the ohmic loss of batteries and the harmonic loss of the motor into the overall loss of the inverters, the efficiency improvement of the CHB on system level, $\Delta\eta_{\mathrm{sys}}$, can be obtained. The combined influence of batteries and the motor on the system efficiency, $\Delta\eta_{\mathrm{BM}}$, is also calculated. The results are collected in Table 4.6. It is first observed that the efficiency improvement on the inverter level is similar to that on the system level. Except for the USA NECC driving cycle, where the efficiency improvement is decreased by 2.10 %, all the other driving cycles only lead to a difference below 0.3 %. That means the CHB has rather little influence on the total loss of the batteries and the motor. Nonetheless, the insignificance is only on the system level, because the changes of the two types of losses counterbalance each other. When checking each individual type of loss, the influence of the CHB is remarkable.

Table 4.6: Simulated battery losses and the corresponding influence on efficiency improvements

	IGBT		CHB			
Driving cycles	Battery ohmic loss	Harmonic copper loss	Battery ohmic loss	Harmonic copper loss	$\Delta\eta_{\mathrm{BM}}$	$\Delta\eta_{\mathrm{sys}}$
USA NECC	0.20 kWh	0.13 kWh	0.46 kWh	0.03 kWh	-2.10 %	8.9 %
Europe City	0.07 kWh	0.12 kWh	0.15 kWh	0.03 kWh	0.24 %	11.5 %
USA City II	0.09 kWh	0.12 kWh	0.20 kWh	0.03 kWh	-0.16 %	9.1 %
FTP72	0.11 kWh	0.11 kWh	0.23 kWh	0.02 kWh	-0.25 %	7.4 %
NEDC	0.11 kWh	0.10 kWh	0.17 kWh	0.02 kWh	0.27 %	7.3 %
WLTP C3	0.18 kWh	0.09 kWh	0.26 kWh	0.02 kWh	-0.02 %	5.4 %
Artemis 130	0.41 kWh	0.07 kWh	0.46 kWh	0.00 kWh	0.07 %	2.9 %
Artemis 150	0.35 kWh	0.07 kWh	0.39 kWh	0.00 kWh	0.08 %	3.0 %

Compared to the IGBT inverter, the CHB almost doubles the battery ohmic losses in all the urban and comprehensive driving cycles. In highway driving cycles, the difference is less significant. The higher ohmic losses in urban driving cycles are caused by the higher amplitude of the current ripples at a low speed. According to ripple formulas in eq. (4.10), the amplitude of the ripple is inversely proportional to the square root of m_{a}. Hence, the amplitude of the ripples increases as the speed is lower, which results in a higher battery ohmic loss in low speed driving cycles.

In terms of the copper loss caused by the harmonic current, the CHB outperforms the IGBT inverter, due to the much lower THD of the multilevel voltage waveforms. In all the driving cycle simulations, the harmonic copper loss caused by the IGBT inverter is around 0.1 kWh/100 km, while the CHB can decrease this loss by 0.07 kWh. Such a reduction of the harmonic copper loss corresponds to an efficiency improvement of around 0.5 %.

Based on the simulation results, the CHB is confirmed to have a positive influence on the motor efficiency and a negative influence on the battery efficiency. Nonetheless, as the two effects are not significant and they can cancel each other, the efficiency improvement of the CHB on the system level is approximately the same as the improvement on the inverter level.

However, in practical implementations, the system level improvement of the CHB is expected to be higher. On the one hand, for a lower battery ohmic losses, the high frequency ripples in the CHB can be easily reduced, either via hardware filtering at a low cost, or via control algorithms to suppress ripples [142], [143]. The battery ohmic losses in the simulation rather demonstrate the worst case of the CHB. On the other hand, the loss reduction in the motor caused by the CHB is underestimated in the simulations, because the simulations only consider the copper loss caused by the harmonics. According to the experiments in [144], the iron loss caused by the harmonics is similar to the harmonic copper loss, and it is even more sensitive to the THD [145]. Hence, the simulations roughly underestimate the reduction of the harmonic losses by about 40-50 %. Combining the two factors discussed above, $\Delta\eta_{\mathrm{sys}}$ of the CHB in pratical implementations is expected to be 0.5-1 % higher than the results in Table 4.6.

To summarize the discussions, the inverter designs using MOSFETs are generally more efficient than the DC voltage shifting approaches, which still use IGBTs. Compared to the SiC MOSFET inverter, the CHB still prevails at a switching frequency of 20 kHz, due to the low DC voltage of the submodules. Compared to the low voltage Si MOSFET multiphase inverter proposed by [96], the CHB is expected to have a similar performance, because of their similarities in terms of the circuit design.

On the system level, the CHB is expected to influence the efficiency of the motor and the batteries slightly. Nonetheless, the summed influence is rather insignificant and could be positive in practical implementations. Therefore, even considering the whole powertrain system, the CHB still outperform most of the existing approaches in terms of efficiency.

However, this chapter only discusses the efficiency of different solutions. To decide if a solution is worth implementing or not, the cost of the solution should also be assessed, as the primary goal of improving the partial load efficiency is to reduce the cost of BEVs. Therefore, the next chapter conducts an investigation on the cost of inverters and powertrain systems.

5 Cost

As the fundamental motivation of the research is to reduce the cost of BEVs by improving the inverter efficiency, the costs of the benchmarked IGBT inverter and the CHB are modelled in this chapter. The SiC MOSFET inverter simulated in chapter 4 is also added to the cost comparison to provide a complete analysis. In addition to the costs of the inverters, the influence of the inverters on the system cost is discussed as well, which is the determining factor in this dissertation to decide if a novel inverter concept should be implemented.

For the purposes stated above, this chapter first summarizes previous studies regarding the costs of power electronic systems. Then the model for the cost assessment of BEV inverters is developed based on the existing studies. The costs of the three inverters are obtained based on the models of different components. In the end, the performances of the three inverters in different scenarios are discussed. In this chapter, only the capital costs or purchasing costs of the inverters and BEVs are discussed. The operational costs and the total cost of ownership are not within the scope of the research.

5.1 State of the Art

A number of studies discussed in chapter 2 also pointed out a higher efficiency is capable of reducing the system cost of BEVs. However, a detailed cost assessment to verify the claims is only sparsely visible in a few studies.

Among the DC voltage shifting approaches, only the cost of the solution proposed in [71], [72] is calculated. As a continuation of [71], [72], which propose to discontinuously shift the DC voltage by actively switching the battery pack configuration, [146, p. 87] estimates the cost of the proposed approach based on the cost of the prototyping. Besides, a mass-production cost of the solution is also estimated by extrapolating the retail prices on electronic components distribution websites.

The cost of the low voltage Si MOSFET multiphase inverter (proposed by [96]) is discussed in [147]. The costs of connectors, cables and insulations are considered in the assessment. The system cost of the solution is compared to that of a Tesla Model S.

The cost of the SiC MOSFET inverters is investigated by more studies. [78], [83], [148] qualitatively compare the system costs of a SiC MOSFET inverter and an IGBT inverter, without giving specific values of cost. [85] conducts a quantitative comparison, but the comparison only considers the costs of the switches. The retail prices of the switches are also used by the comparison, which tends to overestimate the price difference between a Si IGBT and a SiC MOSFET.

On the system level, [149] models the life cycle costs of a SiC MOSFET circuit, based on a crudely estimated price of switches. The comparison is biased toward the cost of switches. The

possibilities to reduce the costs of cooling and to downsize passive components are neglected. A cost estimation of a SiC MOSFET DC/DC converter is provided in [80], in which the influences on the cooling system and passive components are incorporated. Nonetheless, the cost values are not directly used for the cost assessment. Instead, [80] uses the amount of required materials as a cost indicator, in order to compare a Si IGBT converter and a SiC MOSFET converter.

In the studies discussed above, it is observed that the prices of the components, especially the cost of the semiconductor switches, are obtained via individual surveys and approximations. These values could be still considerably different from the OEM purchasing prices. Moreover, because the individual surveys are possible to include the fluctuations of the market status or the marketing strategies of component distributors, the obtained results could also lack in generality and are only applicable for a certain specification. If the specifications of the solution change, the surveys should be conducted again to verify if the solution is worth implementing.

Therefore, the existing approaches based on individual surveys are not appropriate to calculate the cost of the CHB, as the CHB is proposed as a general concept and could be configured differently in different vehicles. To better simulate the OEM purchasing prices and to develop a general approach to assess the cost of the CHB concept, the cost values should be obtained from cost models.

Fortunately, as cost modelling itself is an active topic, there are a few existing studies focusing on the cost modelling of power electronic systems and components. [150] proposes to model the price of high voltage (650-1200 V) semiconductor switches based on the die size, material type and the packaging type, which well manifests the production procedure of the switches. As a continuation of [150], the costs of passive components and cooling devices of power electronic systems are further modelled by [151]. The cost models are proposed based on the production procedure of each component and verified by the real data. The models developed by [151] are implemented in [135], in order to compare the costs of different photovoltaic converters. Furthermore, based on the component cost models in [150], [151], an approach to holistically model the cost of a high voltage inverter is proposed by [152]. This system cost model takes the costs of casing and assembly into consideration as well. Cost models for low voltage components can be found in [153], but the validation and the economic background of the models are not discussed.

According to [150]–[153], the components that have a significant influence on the inverter cost are given in Table 5.1. The item L/C refers to the passive components in the main circuit, i.e., inductors and capacitors. The item ICs (integrated circuits) refers to the sensors, communication chips and microcontrollers required by the controlling mechanism of the inverter, besides the gate drivers. The coverage of the cost models in the literature is also marked in Table 5.1.

Table 5.1: Inverter cost models and their coverage of main cost items

Cost models in literature	Main cost items of an automotive inverter					
	Switch	Driver	L/C	ICs	Cooling	Manufacturing
[150]	X					
[151]	X		X	X	X	X
[152]	X	X	X	X		X
[153]	X		X			

The available cost models in [150]–[153] are able to calculate the cost of any IGBT automotive inverters. For the SiC MOSFET inverter, the model is still usable, but some parameters need to be updated. However, for the CHB, the cost models are not directly applicable anymore. That is because the CHB follows a distributed layout, while the inverter systems assessed in the previous studies all follow a concentrated layout, i.e., the whole system is assembled together in a single casing. The costs of the components in the CHB, e.g., ICs, heatsinks and passive components, should be calculated differently. Hence, a cost model for the CHB should be re-constructed from the component level.

Moreover, it is also worth noting that modelling the cost of the CHB is not simply combining the existing component cost models. The corresponding component models should first be parametrized appropriately according to the performance and specifications of the CHB, before using the component cost models to evaluate the system costs

As a summary, for the cost assessment of the CHB, the studies regarding the efficiency improvement have not provided an approach to generate accurate and generally valid results. The existing cost models are also not directly applicable, due to the structural change of the CHB concept. To obtain the cost of the CHB and assess its influence on the system cost of BEVs, additional modelling efforts are still necessary. The existing cost models and component configuration approaches should be adapted to calculate the cost of the CHB. Such an adapted approach will be explained in the next section.

5.2 Approach

In order to compare the costs of the benchmarked IGBT inverter, the SiC MOSFET inverter and the CHB, a cost model for automotive inverters is developed in this section, based on the component models in [150]–[153]. As stated in the previous section, the models [150]–[153] can directly calculate the cost of six-pack IGBT inverters. The purpose of developing a new model is mainly to adapt the cost models to the CHB concept, and update the necessary parameters for the SiC MOSFET inverter. The construction of the cost model mainly consists of two steps. First, the cost models of the components are adapted, i.e., adapting the models of the six main cost items in Table 5.1 for the CHB and SiC inverter. Second, the adapted component models are combined to calculate the system costs.

5.2.1 Component Cost

First, for the switch cost, C_{switch}, the model in [151] is generally applicable for all types of high voltage switches, eq. (5.1). C_{package} is the package cost, c_{Die} is the unit cost of the die, and A_{Die} is the size of the die inside the switch. For SiC MOSFETs, the model can be directly used, as all the necessary parameters are already given in [151].

$$C_{\mathrm{switch}} = C_{\mathrm{package}} + c_{\mathrm{Die}} A_{\mathrm{Die}} \tag{5.1}$$

For low voltage Si MOSFETs in the CHB, the model is still reasonable to use, as it is developed based on the production procedure of switches. Nonetheless, the unit price of the dies and the price of packages should be re-parametrized for low voltage Si MOSFETs. Due to the planar structure of low voltage Si MOSFETs and the similarity of price [98], this dissertation uses the unit price of PiN diode dies given in [151] for the Si MOSFET dies. The package cost is

determined mainly by the size of the package [151]. By the regression analysis and extrapolation of the costs of different packages given in [151], the cost of different switches can be obtained using the package sizes given in the datasheets. The Si MOSFET cost model developed by [153] is not adopted in this dissertation, because the verification and the economic background of this model are not as clear as those in [151]. The parameters to use the model are also not provided.

Second, the cost of gate drivers, C_{GD}, should also be modelled differently for different inverter concepts. The driving circuit of the CHB and the IGBT inverter can be cheaper than that of the SiC MOSFET inverter. That is because Si switches (IGBTs and MOSFETs) usually only require a common supply of ±15 V to turn on and off [154], while SiC MOSFETs require a gate voltage set of +20 V/-5 V [155], [156] for a safe switch on and off. An isolated ±15 V DC source is rather standard and cheap due to the effect of economies of scale. The DC sources with unsymmetrical outputs, however, are mostly only customized for gate driving purposes, and are more expensive, as observed on the website of corresponding manufacturers [157], [158]. The drivers of SiC MOSFETs also require dedicated designs to suppress the EMI. Therefore, in the cost assessment, instead of giving a constant unit price as the output, the cost model of drivers should take the material of the switches as input and alter the unit price of the driver accordingly. Additionally, it is worth noting that the IGBTs work the best with +15 V/-10 V gate voltage [159]–[161], which is also the configuration in most inverters on the market. However, in this dissertation, it is assumed that the IGBTs use the same drivers as the Si MOSFETs do, to form a worst-case scenario for the CHB and examine if the CHB is still advantageous.

The adaption of the capacitor cost model is relatively simple. The SiC MOSFET inverter is assumed to have the same DC-link capacitor as the benchmarked IGBT inverter, a 475 µF, 450 V film capacitor, because this capacitance value is already rather low even for the SiC MOSFET inverters and should not be further reduced [37]. Subsequently, using the linear cost model developed by [151], the capacitor cost, C_{cap}, can be calculated by eq. (5.2). U_{cap} is the rated voltage of the capacitor. C_{DC} is the capacitance. The three coefficient, α_{cap}, α_{Vcap} and α_{Ccap} are given in [151], based on a linear regression.

For the CHB, the cost of the capacitor is zero, as indicated in eq. (5.2), since each H-bridge in the CHB is closely coupled to the battery module and does not need a large DC-link capacitor for voltage stabilization, Figure 3.11. Even considering the filtering capacitors for the current ripples, the cost of capacitors in the CHB is still negligible. As it is impractical to filter the low frequency current ripples [50], the filtering capacitors should only target the switching frequency ripples, and thus have a rather small capacitance. Due to the limited module voltage, the voltage rating of these capacitors is also low. Therefore, compared to the six-pack inverters, the capacitor cost of the CHB is negligible, even considering the filters for switching frequency ripples.

$$C_{\mathrm{cap}} = \begin{cases} \alpha_{\mathrm{cap}} + \alpha_{\mathrm{Vcap}} U_{\mathrm{cap}} + \alpha_{\mathrm{Ccap}} C_{\mathrm{DC}} & \text{if not CHB} \\ 0 & \text{if CHB} \end{cases} \tag{5.2}$$

Fourth, the cost model of ICs is also adapted. For the SiC MOSFET inverter, the cost of the ICs for circuit control is approximately the same as that of an IGBT inverter, because they both use the six-pack structure. However, for the CHB, the cost of ICs should be recalculated. In addition to the central controller, each H-bridge module also needs an additional controller (usually CPLD, complex programmable logic device) to process the commands from the central controller. Additionally, as the CHB follows a distributed layout, communications via wires could bring large interferences to the control circuit. Hence, a cascaded multilevel inverter like the CHB often uses fiber optic communication for the control of switches and transmission of sensor information.

Considering the factors discussed above, the cost of ICs, C_{IC}, can be calculated by eq. (5.3). C_{CMCU} is the cost of the central controller. c_{CPLD} and c_{FBR} are respectively the unit cost of the CPLD and the fiber optic communication set. N is the number of H-bridge submodules. For six-pack inverters, N is zero. The IC costs of the three inverters can be obtained by eq. (5.3).

$$C_{\mathrm{IC}} = C_{\mathrm{CMCU}} + N(c_{\mathrm{CPLD}} + c_{\mathrm{FBR}}) \tag{5.3}$$

For the cost of cooling devices, C_{HS}, only the heatsinks are considered, as automotive inverters are liquid cooled and do not require fans. For the SiC MOSFET inverter, after resizing the heatsink using the model in [162], the heatsink cost model in [151] is directly applicable, as the SiC MOSFET inverter also follows the six-pack structure. For the CHB, because each H-bridge module requires an individual heatsink, the cost model in [151] needs further adaption. First, using the maximum loss per module, $P_{\mathrm{loss\_max}}$, and the models developed in [162], the required volume of the heatsink of each module, V_{HS}, can be obtained. Then based on V_{HS}, the cost model in [151] can provide the cost of cooling devices in each module. Multiplying the number of modules with the cooling cost per module, the overall cost of cooling devices in the CHB system can be obtained.

The cooling costs of the three inverters can be calculated by eq. (5.4). N_{HS} is the number of heatsinks in the inverter. For six-pack inverters, N_{HS} is always one. For the CHB, N_{HS} equals the number of submodules, N. $P_{\mathrm{loss\_max}}$ is the maximum power dissipated via each heatsink. The coefficients of the cost model, $c_{\mathrm{fix\_HS}}$ and $c_{\mathrm{V\_HS}}$, are obtained by [151] via a linear regression.

$$\begin{cases} C_{\mathrm{HS}} = N_{\mathrm{HS}}(c_{\mathrm{fix\_HS}} + c_{\mathrm{V\_HS}} V_{\mathrm{HS}}) \\ V_{\mathrm{HS}} = f(P_{\mathrm{loss\_max}}) \end{cases} \tag{5.4}$$

In the end, the manufacturing cost is also considered. In this dissertation, the modular structure of the CHB is assumed not to influence the manufacturing cost, because modular designs have been widely adopted by the current inverters as well. Instead of directly using one high-power switch, the IGBT inverters usually connect several small six-pack inverters in parallel to reach a higher power. An example, Figure 5.1, shows a 100 kW state-of-the-art automotive inverter with two 50 kW modules in parallel, produced by Brusa Elektronik [49]. By changing the number of submodules, products with different power ratings are made available [49].

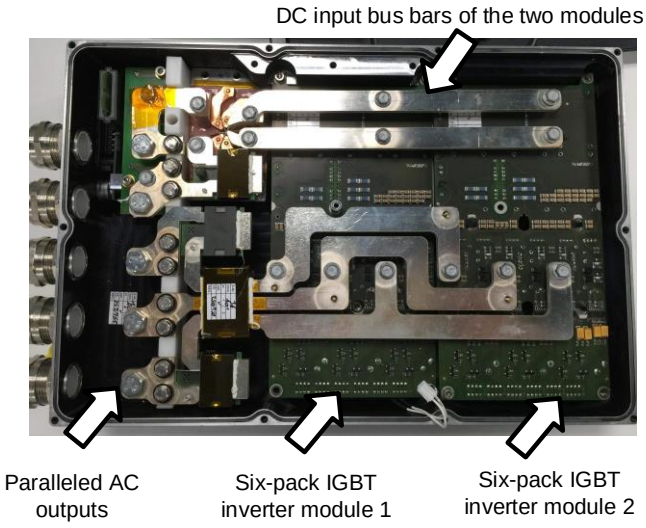


Figure 5.1: Internal structure of a modularized 100 kW state-of-the-art IGBT inverter

Therefore, it is reasonable to use the overhead factor 1.25 of IGBT inverters [152] to estimate the manufacturing cost of the CHB as well. For the SiC MOSFET inverter, [152] suggests using 1.1 as the overhead factor to incorporate the manufacturing cost. This overhead not only includes the cost of manufacturing, but also includes the cost of other comparatively cheaper components, e.g., connectors, printed circuit boards (PCB) and housing.

5.2.2 Inverter Cost and System Cost

Summing up the costs of all the components and multiplying the result with the manufacturing overhead factor, the capital cost of the inverter, C_{inv}, can be obtained, Figure 5.2. Due to the adaptions of the component cost models, the model in Figure 5.2 is applicable for all the three inverters to be compared in this chapter. The parameters of the three inverters are given in Appendix B. For a differently configured CHB or the other two types of inverters, the model in Figure 5.2 is still generally applicable, as long as the selected switch is known and simulated. Therefore, the cost model Figure 5.2 does not rely on individual investigations to calculate the cost of different inverters.

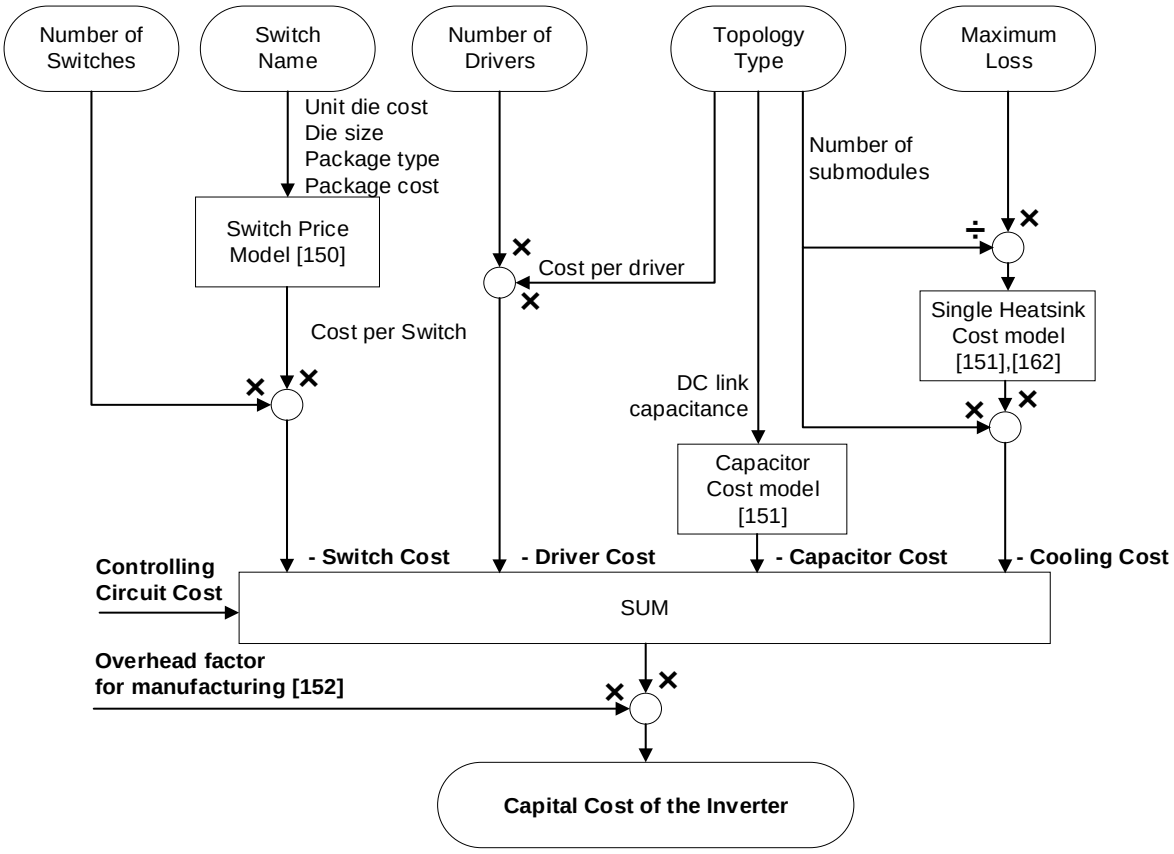


Figure 5.2: Block diagram of the cost model for the SiC MOSFET, CHB and IGBT inverter

Besides the capital cost of the inverter, the system cost is also modelled, to evaluate the influence on the cost of the vehicle. As it is impractical and unnecessary to analyze the cost of each component in the reference vehicle, only the parts that could be influenced by the inverter selection are identified and analyzed.

First, the inverter selection influences the cost of batteries. To reach the nominal range of the reference vehicle (300 km rated by the WLTP C3 driving cycle [163]), a more efficient inverter requires less battery capacity, due to the reduced energy consumption. The battery cost using a

certain inverter can be obtained by multiplying the corresponding energy consumptions for the 300 km range with the battery cost.

Second, the cost of contactors is also influenced by the inverter design. For a six-pack inverter, two high voltage high current contactors are usually necessary, one on the positive side and another on the negative side of the DC link respectively [164]. That is because the battery pack of the six-pack inverter has an always-on high voltage. For safety, the battery pack should be disconnected from other components when the vehicle is deactivated [147]. The necessity of disconnection is regulated in the norm ECE R100 [165].

For the CHB, however, contactors are not certainly necessary, as there is no presence of an always-on high voltage in the system. Even if it is still desired to completely disconnect the battery modules from the H-bridges during idling time, cheap Si MOSFET relays can be used to replace the expensive mechanical contactors, because of the low voltage. Therefore, in general, the cost of contactors in the CHB can be neglected. Nonetheless, to calculate the worst-case cost of the CHB, it is still assumed that each H-bridge is equipped with a low voltage mechanical contactor at the positive output of the battery module. More specifically, nine contactors in total are required for the CHB discussed in this dissertation.

In the end, the cost of the cables or bus bars could also be different for the CHB and the six-pack inverters, due to the structural difference. However, as the difference is not easily quantifiable and the prices of cables and bus bars are comparatively low, this part of the cost is not counted in the system cost. The other components in the powertrain system are assumed not to be influenced by the inverter design.

Based on the former analysis, the system cost used to compare inverter designs, C_{sys}, can be calculated by eq. (5.5). c_{bat} is the unit price of batteries on the pack level in USD/kWh. R_{veh} is the nominal range of the vehicle in kilometer. $b_{100\mathrm{km,el}}$ is the energy consumption per 100 km in the WLTP C3 driving cycle. $c_{\mathrm{contactor}}$ and $N_{\mathrm{contactor}}$ are respectively the unit price and the number of contactors required by the selected inverter design.

$$C_{\mathrm{sys}} = c_{\mathrm{bat}} R_{\mathrm{veh}} b_{100\mathrm{km,el}} / 100 + c_{\mathrm{contactor}} N_{\mathrm{contactor}} + C_{\mathrm{inv}} \tag{5.5}$$

It should be noted that the C_{sys} obtained in eq. (5.5) is not the overall powertrain system cost or the vehicle cost. C_{sys} is only the total cost of the parts that can be considerably influenced by the choice of inverters. The absolute value of C_{sys} is not relevant for the cost assessment. The main purpose of C_{sys} is to compare the C_{sys} values of different inverters and thus quantitatively determine whether a solution for efficiency improvement is cost-effective. The cost reduction or increase caused by a certain solution can also be determined based on C_{sys} values.

5.3 Results

Substituting the parameter values in Appendix B into the cost model in Figure 5.2, the capital costs of the three inverters are obtained in Table 5.2. The component costs of the inverters are also included to make the cost analysis more transparent. U/P means the unit price and Qty refers to the quantity of the components used in each inverter. All the currency values are in USD. This result has already been released in a publication [50].

In Table 5.2, it is observed that the higher efficiency of the CHB and SiC MOSFET inverter is also associated with a higher capital cost. Compared to the cost of the IGBT inverter, the CHB is almost 50 % more expensive, while the SiC MOSFET inverter costs more than double. The high price of the SiC MOSFET inverter can be explained by the high cost of the switches, which is two times higher than the cost of the IGBT, four times higher than the cost of the Si MOSFET. The per-current cost of the SiC MOSFET used in Table 5.2 is 0.28 USD/A. This value is already an optimistic estimation of the current price in large quantities, according to a prediction published by Cree [166, p. 24], one of the main SiC MOSFET manufacturers.

The CHB also has a higher cost compared to the IGBT inverter, but the higher cost is not caused by the switches. Although much more switches are used by the CHB, due to the extremely low unit price of the Si MOSFET, the switch cost of the CHB is actually lower than that of the IGBT inverter. The cost of the CHB is mainly increased by the cost of gate drivers and ICs. The unit costs of the gate drivers in the CHB and the IGBT are the same, but the CHB needs much more gate drivers, as the number of individually controllable switches is higher. Hence, the total driver cost of the CHB is six times that of the IGBT inverter. Furthermore, due to the implementation of the fiber optic communication system and CPLDs, the cost of ICs in the CHB is also much higher. A detailed cost break down of the ICs and gate drivers can be found in [50] to jusify the cost values in Table 5.2.

Table 5.2: Capital cost of the IGBT inverter, the SiC MOSFET inverter and the CHB [50]

Costs	IGBT			SiC MOSFET			CHB		
	U/P	Qty	Sum	U/P	Qty	Sum	U/P	Qty	Sum
Switch cost	296.6	1	296	28.1	36	1011.6	0.94	216	203.4
Driver cost	6.5	6	39	11	6	66	6.5	36	234
Capacitor cost	30.3	1	30.3	30.3	1	30.3	-	0	0
Heatsink cost	17.3	1	17.3	14.9	1	14.9	1.8	9	16.2
IC cost	150	1	150	150	1	150	300	1	300
Overhead cost			133.3			127.3			188.6
Inverter total sum			666			1400			942

Due to the higher cost of the CHB and the SiC MOSFET inverter, it cannot be directly decided whether the CHB or the SiC MOSFET inverter is cost-effective. To make the decision, the system cost of the two inverters should also be assessed. Using eq. (5.5), the system cost of the three inverters are calculated and provided in Table 5.3. The cost breakdown of each inverter is also listed in Table 5.3. All the cost values are still in USD. The quantity of the battery is defined by the energy consumption to drive 300 km following the WLTP C3 driving cycle. The value of unit battery cost used in this dissertation is 165 USD/kWh, which is the pack level cost for smaller cells in 2017, estimated by [26]. More scenarios of battery cost are covered in the discussion. The unit cost values of the contactors are the distributor quotation values in large quantities [50].

As already mentioned in the previous section, C_{sys} is not an indicator of the overall powertrain cost, because it only considers the cost terms that could be influenced by the choice of the inverter. Nonetheless, once the choice of the inverter is changed from the IGBT inverter to

another solution, the change of the C_{sys} value, ΔC_{sys}, is a good indicator for the reduction or increase in the BEV cost. If the BEV cost is reduced, ΔC_{sys} will be a positive value, vice versa.

Compared to the benchmarked IGBT inverter, the cost reduction, ΔC_{sys}, of the SiC MOSFET inverter is negative, -288 USD. That means implementing the SiC MOSFET inverter in the reference vehicle increases the overall cost by 288 USD. Hence, as of now, the SiC MOSFET inverter is not a cost-effective solution. Although the battery cost is reduced by 507 USD, it is still insufficient to pay off the high price of SiC MOSFETs. To break even with the IGBT inverter in the reference vehicle, the cost per SiC MOSFET needs to decline by 29 %, to 20.1 USD, corresponding to a per-current price of 0.20 USD/A. Such a cost could be achieved in the future, if the 6-inch or even larger wafers are used in mass productions [167, p. 30].

Table 5.3: System cost of the three inverters for comparison

Results generated based on WLTP C3 cycle	IGBT			SiC MOSFET			CHB		
	U/P	Qty	Sum	U/P	Qty	Sum	U/P	Qty	Sum
Inverter cost	666	1	666	1400	1	1400	942	1	942
Battery cost	165	38.4	6336	165	35.7	5890	165	35.4	5841
Contactor cost	37	2	74	37	2	74	20	9	180
C_{sys}			7076			7364			6936
ΔC_{sys}			0			-288			113

A positive cost reduction is achieved by the CHB. According to the ΔC_{sys}, the implementation of the CHB in the reference vehicle could result in a cost reduction of 113 USD. That is because the decrease in the battery cost is similar to that of the SiC MOSFET inverter, while the capital cost of the CHB is much lower.

It is worth noting that the CHB inverter also reduce the weight of the vehicle due to the reduced battery capacity, which can further reduce the energy consumption of the vehicle and thus the system cost. Using the energy density of the battery in the reference vehicle, 175 Wh/kg [168], the CHB reduces the weight of the vehicle by 17 kg. Consequently, the required battery capacity to reach the nominal range of 300 km can be further reduced to 35.1 kWh. Hence, the final cost reduction realized by the CHB is 162.5 USD, 49.5 USD higher than that in Table 5.3. The additional cost reduction due to the weight reduction effect is not incorporated in Table 5.3, in order to demonstrate the improvement of the CHB in the worst case,

Another worst-case assumption for the CHB implemented in Table 5.3 is that each H-bridge submodule is equipped with an expensive mechanical contactor. In practical implementations, the contactor is not necessarily required for the low voltage modules [147]. Additionally, the cost of the IGBT inverter is also estimated rather conservatively. Therefore, when implementing the CHB concept in BEVs, the cost reduction is expected to be even higher.

In this section, the costs of the three inverters are compared in the reference vehicle with a specific battery price. The results can thus only determine that the CHB is worth implementing in this specific scenario. To enhance the generality of the CHB concept and investigate its applicability in more scenarios, a parameter sensitivity analysis is necessary. Another concern regarding the cost values in this section is the accuracy of the efficiency. As observed in Table

5.3, the system cost of the three inverters is highly influenced by the battery cost, which is rather sensitive to the efficiency of the inverters. Hence, it is questionable if the CHB is still able to pay off its capital cost, considering the ±1 % error of simulations. The two concerns will be discussed in the next section.

5.4 Discussion

To holistically investigate the cost reduction associated with the CHB concept, this section first considers the influence of the possible errors arising from the driving cycle simulations and calculates the cost reduction in an extreme worst-case scenario. This calculation is followed by a parameter sensitivity analysis to evaluate the scenarios with a different battery cost, nominal range, and driving cycles, as these factors highly influence the system costs.

5.4.1 Cost Reductions Considering Efficiency Accuracy

As the cost calculations in Table 5.3 are sensitive to the energy consumption, the accuracy of the efficiency can significantly influence the system cost. Therefore, before choosing the inverter solution based on the ΔC_{sys} values in Table 5.3, it is still necessary to consider the possible errors of the efficiency in the simulations.

The efficiency in this dissertation is defined based on the energy throughput of the inverter, as in eq. (2.4). Hence, in driving cycle simulations, the percentage error of the efficiency is the same as the percentage error of the total energy consumption of the BEV. As the error of the simulated efficiency is verified to be within ±1 % (in Appendix A2), the maximum and the minimum energy consumptions of each inverter can be obtained by multiplying 1.01 and 0.99 with the corresponding values in Table 5.3. Accordingly, for each inverter, the maximum and the minimum of the system cost can also be determined. The results are provided in Table 5.4.

Table 5.4: The maximum and minimum of the system costs for the three inverters in USD

Results generated based on WLTP C3 cycle	IGBT		SiC MOSFET		CHB	
	min	max	min	max	max	min
Inverter cost	666	666	1400	1400	942	942
Battery cost	6273	6399	5831	5949	5782	5896
Contactor cost	74	74	74	74	180	180
C_{sys}	7013	7139	7305	7423	6904	7018

According to the results in Table 5.4, even the minimum cost of the SiC MOSFET system cost is still higher than the maximum of the CHB the IGBT system costs. The SiC MOSFET inverter is thus confirmed surely not a cost-effective choice for the reference, given the current price of SiC MOSFETs. To make the minimum of the SiC MOSFET inverter break even with the supremum of the IGBT inverter, the cost per SiC MOSFET still needs to decrease by 16.5 %, to 23.5 USD. This switch cost corresponds to a per-current price of 0.235 A/USD, which is possible to realize rather recently by choosing the SiC MOSFETs with a lower voltage rating [166] (the implementations of 6-inch wafers would still take some time [167, p. 30]). Therefore, with an

optimal design, the SiC MOSFET inverter might be able to break even with the IGBT inverter in the near future.

As for the CHB, comparing the maximum of the CHB cost and the minimum of the IGBT inverter cost, the CHB system is only 5 USD more expensive than the IGBT inverter system. That means the worst-case CHB is still close to break even with the IGBT inverter, when considering the worst-case errors of the efficiency. Hence, it can be confirmed that the cost reduction of the CHB is not a result of simulation errors.

Additionally, the results in Table 5.4 also indicate that the accuracy is rather important for the studies on efficiency improvement. An efficiency error of 1 % could already considerably change the system cost of the proposed solution, and thus influence the choice of the solution. If the error of efficiency further grows, the system cost intervals of different solutions will increasingly overlap. Consequently, the system costs of different solutions cannot be differentiated anymore, and it will be even more difficult to decide which solution is the most cost-effective.

5.4.2 Parameter Sensitivity Analysis

In the comparisons above, the specifications of the reference vehicle are strictly taken and the CHB is proven to be cost-effective for the specific scenario. However, as shown in Table 5.3, the cost is sensitive to the total cost of batteries, which could be influenced by the nominal range, the battery price and the selected driving cycle for range rating. Therefore, a sensitivity analysis regarding each parameter is necessary, so that the applicability of the CHB can be generally examined in different vehicle concepts and at different battery costs. In the sensitivity analysis, the worst-case assumption of the contactor cost is loosened, to demonstrate a common scenario. The contactors of the three inverters are not included in the system costs in this section.

First, the sensitivity of the system costs to the battery price is analyzed for the three inverters. In Table 5.3, the unit price of the battery is the current cost of small cells on the pack level [26]. As the cost of the battery has been continuously declining, it is reasonable to assume that the price of the battery will be even lower in the future. Moreover, using larger cells in the future can also reduce the battery cost on the pack level [26]. According to the results in [26], by using 60 Ah cells, the battery cost on pack level is expected to reduce to 105 USD/kWh in 2030. Therefore, to simulate the possible changes of the battery cost, the system costs of the three inverters are recalculated by sweeping the battery price value in an even larger interval, from 70 USD/kWh to 220 USD/kWh. The C_{sys} curves of the three inverters are plotted in Figure 5.3.

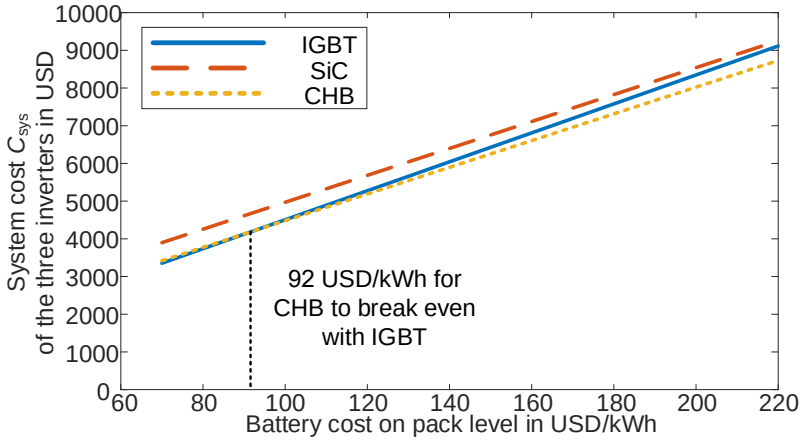


Figure 5.3: The system costs of the three inverters when battery unit cost varies

For the reference vehicle, due to the high price of the SiC switches, the SiC MOSFET inverter is constantly more expensive than the benchmarked IGBT inverter, even when the battery price reaches 220 USD/kWh. Therefore, in the future, SiC MOSFETs will be even less preferred in terms of cost, if the SiC MOSFETs cannot become cheaper rapidly.

For the CHB, as long as the battery price is higher than 92 USD/kWh on the pack level, the CHB is a better choice than the benchmarked IGBT inverter for the reference vehicle. If the battery price drops further down in the future, the CHB will not be able to reduce the cost for the reference vehicle anymore. Nonetheless, according to the survey in [26], since the pack-level cost of batteries is not going to reach 92 USD/kWh in the near future, the applicability of the CHB for the reference vehicle will be valid for a rather long time.

In addition, if the cost of batteries declines further in the future, another trend can be foreseen is that the nominal range of the BEVs will increase, instead of being restricted to 300 km. Such a trend will also be in favor of solutions with a higher efficiency. Hence, the sensitivity of the system costs to the nominal range is also worth exploring. The sensitivity analysis regarding the nominal range is conducted by sweeping the nominal range from 100 km to 800 km, rated by WLPT C3 driving cycle. 800 km may seem to be an unnecessarily high value, but it might be preferred in the future, since the range rated by driving cycles is lower than the real range, especially in winter or summer periods with a heavy usage of the HVAC (heating, ventilation, and air conditioning) system [169]–[171]. The result of the range sweep is presented in Figure 5.4. The battery price is kept constant at 165 USD/kWh.

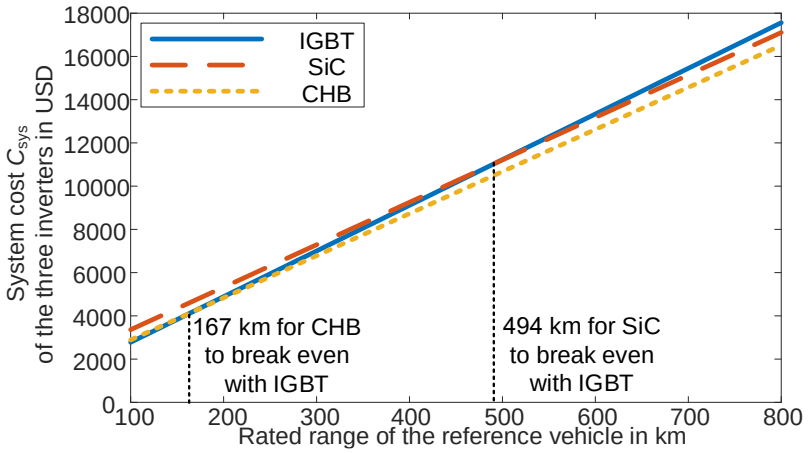


Figure 5.4: The system costs of the three inverters when the rated range varies

As the nominal range increases, the inverters with a high efficiency become more and more preferable, because the reduced battery capacity requirement becomes more significant. For the CHB, as long as the rated range is higher than 167 km, it can break even with the benchmarked IGBT inverter. Hence, the CHB is generally recommendable for different BEVs, because many BEVs nowadays have a nominal range above 200 km. As the nominal range further increases in the future, the improvement of the CHB will become more significant.

For the SiC MOSFET inverter, the threshold range to break even is 494 km. Therefore, given the current price of SiC MOSFETs, the SiC MOSFET inverter should only be used in high-end BEVs with a rather long nominal range. As the SiC material gradually becomes cheaper in the future, the SiC MOSFETs will be applicable for more vehicle concepts.

To better illustrate the results, Figure 5.3 and Figure 5.4 are merged into a map and illustrated in Figure 5.5. In the coordinate of the rated range and the battery cost, each point is marked by

the inverter design that can achieve the lowest system cost. With this map, once the nominal range and the battery cost are given, the most preferable inverter (in terms of the system cost) can be rapidly decided.

In Figure 5.5, the SiC MOSFET inverter does not outperform the other two inverters at any point, due to the currently high price of SiC switches. The benchmarked IGBT inverter can achieve a lower system cost when the WLTP range is lower than 400 km and the cost of the battery is sufficiently low. The CHB prevails in most of area of Figure 5.5. As long as the nominal range is higher than 400 km, in the evaluated range of the battery cost, the CHB is surely able to reduce the cost of the reference vehicle.

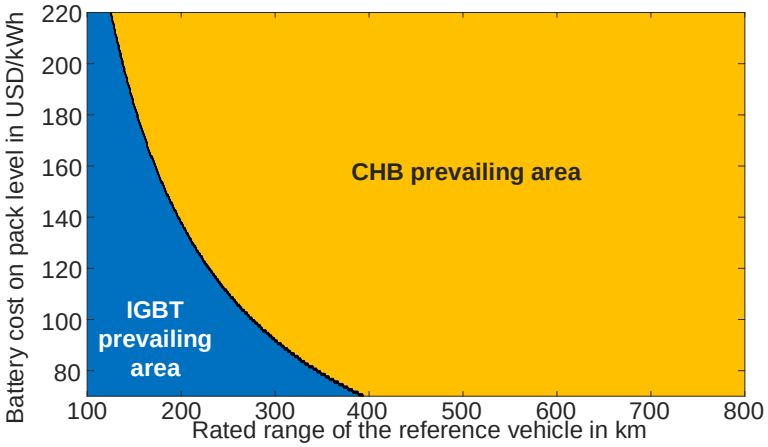


Figure 5.5: The prevailing scenarios of IGBT and CHB, SiC not preferred in the whole range

Furthermore, the prevailing area of the CHB also covers almost all the possible scenarios in the future. On the one hand, a nominal range above 400 km could be rather common for BEVs in the future. Even nowadays, the nominal range of many BEV models has already surpassed this value. On the other hand, the cost of the battery on the pack level is unlikely to become lower than 70 USD/kWh in the nearby decades [26]. Due to the increasing costs of the raw materials, even optimistic predictions are not foreseeing a battery cost lower than 70 USD/kWh costs. Therefore, the CHB is expected to be generally preferable in the future.

Another factor worth discussing is the driving cycle to rate the nominal range. In the discussions above, all the nominal range values are rated by the WLTP C3 driving cycle, which is the standard driving cycle to quantify the nominal range of BEVs [163]. Nonetheless, it is still possible that different vehicle concepts rate the nominal range with other driving cycles. Therefore, as the last part of the sensitivity analysis, the influence of driving cycles is also discussed. The system costs of the three inverters are recalculated based on the 300 km energy consumption in different driving cycles, following the same approach as used for the WLTP driving cycle in Table 5.3. The cost of the battery is still kept at 165 USD/kWh. The obtained system costs are plotted in a bar chart, Figure 5.6.

When using the four driving cycles with a lower average speed, i.e., from USA NECC cycle to FTP 72 cycle on left side of Figure 5.6, to rate the range, the SiC MOSFET inverter and the CHB are both able to reduce the overall cost, because more partial load operations are involved in these driving cycles. In the other four driving cycles with a higher speed, the SiC MOSFET inverter cannot achieve cost reductions anymore.

In comparison, the system cost reductions of the CHB inverter are visible in all driving cycles, due to the low capital cost and the high efficiency improvement. Even when rating the range with

the two highway driving cycles, the CHB is still able to reduce the cost for the reference vehicle. One reason is the considerable efficiency improvement of the CHB in highway driving cycles. The relatively high battery price used to obtain Figure 5.6 also partly contributes to the cost reductions in highway driving cycles. Considering the lower battery price in the future, the CHB might not be able to reduce the cost for vehicle concepts that rate their ranges with high-speed driving cycles. However, as discussed in [172], the majority of vehicles in the future will still be driving in urban environments. It is highly unlikely that the highway driving cycles will be widely implemented to rate the range of BEVs.

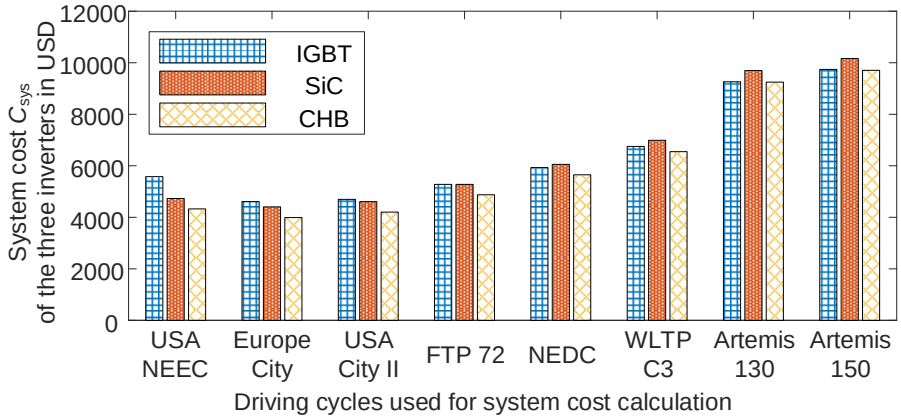


Figure 5.6: System costs for the three inverters using the energy consumption of different cycles [50]

To summarize this section, considering the analysis of the simulation error and the parameter sensitivity, the general applicability of the CHB is proven. Even in the worst case, by improving the efficiency, the CHB is still able to reduce the system cost for a variety of vehicle concepts.

Moreover, it is worth noting that the configuration of the CHB used in this chapter is not optimal. In practical implementations, it is necessary to search for the optimal configuration for the targeted vehicle concept, e.g., the optimal number of modules and the optimal choice of MOSFETs, in order to achieve the highest cost reduction for the system. Besides, the cost assessment in this chapter does not consider the reduced energy cost as well, which could be more significant than the reduced battery cost in the long run. The optimization of the circuit parameters and the operation cost are not within the scope of this research. Nonetheless, they are main subtopics in the dissertation of Mr. Felix Roemer, a Ph.D. candidate from the same institute. The optimally configured CHB for the reference vehicle and its influence on the total cost of ownership can be found in this dissertation.

After the investigations in chapter 4 and 5, it can be concluded that the main goals of the research, i.e., improving the partial load efficiency and reducing the cost of BEVs, are achieved by the CHB concept. However, before practical implementations, there are still several concerns regarding the CHB concept. First, as mentioned in the discussion of chapter 4, the battery current in the CHB contains large ripples, because of the change in the circuit structure. Besides the slightly increased ohmic losses, it is unknown whether the current ripples could accelerate the aging of the batteries. Second, the reliability of the CHB could also be questionable, as a much higher number of components, especially switches, are used in the CHB. These two concerns will be investigated in detail in the next two chapters.

6 Influence on Battery Aging

A typical current waveform of one battery cell in the CHB is depicted in Figure 6.1, where positive current implies the discharge of the battery cell. The current of the batteries contains low frequency ripples and switching frequency ripples, as mentioned in the discussion of chapter 4. The reason for the low frequency ripples is that the battery modules in the CHB are only providing power for a single phase [173], [174]. The switching frequency ripples in the current are generated by the PWM process, because the batteries are directly connected to the switches. Both types of ripples might be able to accelerate the aging of lithium batteries.

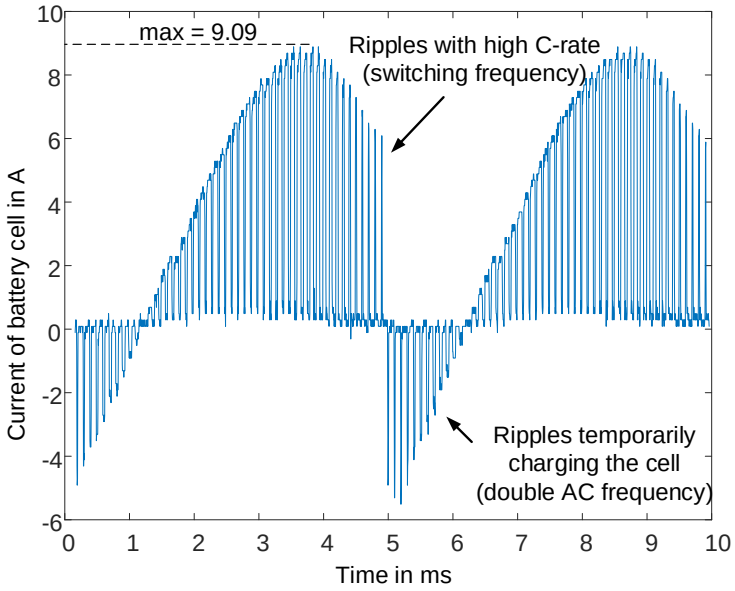


Figure 6.1: Measured current waveform of one cell in the CHB when the power factor is 0.8

First, from a conventional point of view, the switching frequency ripples might be able to accelerate the aging, because of their high C-rate, which is identified as one of the driving factors for battery aging in multiple studies [173], [174]. In Figure 6.1, the average discharge current is only 2.4 A, but the peak value of the switching frequency ripples is 9.09 A. Such a peak value is only instantaneous. However, it is not certain if the repetitive high C-rate of the switching frequency ripples is harmful to battery cells.

Second, if the power factor is not strictly 1.0, due to the phase lag of the AC current, the battery cells in the CHB will be temporarily charged while the CHB is driving the motor. As the temporary charge happens twice in each AC period, they are referred to as double-frequency ripples [173]. Compared to the cells discharged by DC current, the double-frequency ripples create micro charge and discharge cycles, and thus increase the charge throughput of cells. As the total charge throughput is proven to be one of the most significant driving factors for the aging of batteries, the double-frequency ripples are also suspected to be harmful to batteries. The cycle

life of battery cells might be consumed much faster in the CHB, due to the existence of the double-frequency ripples.

Due to the concerns over the two types of current ripples, it is necessary to investigate whether the current waveform of the CHB really accelerates the aging of lithium batteries. If identified to be significantly harmful to lithium batteries, the CHB concept should be reconsidered, as the batteries have the highest cost among all the components in a BEV.

6.1 State of the Art

In previous studies, the switching frequency ripples and the double-frequency ripples are mostly deemed as harmful to the battery cells. This can be proven by the availability of literature focusing on the suppression of the current ripples in single-phase power supply systems, e.g., on-board chargers [175]–[184]. In a single-phase system, if not filtered at all, the current waveform of batteries will be the same as in Figure 6.1. The studies regarding the ripple suppression have not experimentally verified that the ripples can damage batteries. Instead, the damages of ripples are mostly only claimed in the introduction part, by quoting the assertions in other studies.

However, after extensive investigations on the directly cited studies in [175]–[184], it is found out that most supporting studies are not supported by experimental investigations, either. Even tracing back to the most original sources quoted in these studies, only [185]–[187] are found to have conducted experiments with ripple current. Nonetheless, in [185], [186], the ripple current was implemented on lead-acid batteries or fuel cells. Hence, the obtained results are not applicable for the CHB to be used in BEVs, which adopts lithium-ion batteries.

Among the original sources, [187] is found to have tested lithium battery cells with ripple current. In [187], the experiment measures the electrochemical efficiency and the temperature of the cells, when the cells are tested by current ripples. The results indicate that the differences caused by ripples is rather minimal. No long-term test is conducted to investigate the influences of the ripples on the battery aging. Therefore, the damages of the ripple current to lithium batteries claimed in [175]–[184] are not concretely supported by experimental results.

If not restricting the shape of the current ripples to be exactly the same as Figure 6.1, a few more studies are found to have generally investigated the influence of ripple current in long-term battery aging experiments [188]–[193]. The ripple current waveforms in these studies are formed by superimposing a ripple current to a constant DC current.

[188] tests 2 Ah lithium cobalt oxide (LiCoO2) cells with square wave current in float charging state. The square waves have an amplitude of ±1 A and the frequencies of the waveforms vary from 1 Hz to 10 kHz. In the experiment that lasted 147 days, if the frequency of the current waveform is 100 Hz or higher, the ripples show no impact on the battery aging. For cells tested by ripple with a frequency of 10 Hz or even lower, an additional capacity loss of about 7 % is observed. Therefore, [188] concludes that ripples are not harmful to the batteries, as long as the frequency is higher than a corner value. In the case of [188], the corner frequency is 10 Hz.

[189] investigates the influence of 120 Hz half sinewave ripples [189]. In each cycle, the tested cells are charged by the ripple current until the SOC is 80 %, and discharged by constant DC current until the SOC equals 30 %. After 250 test cycles, compared to the cells only tested by the constant DC current, the capacity losses of the cells charged by ripple current are on average

0.55 % higher. However, as the difference is low, the study does not confirm any concrete impact of the current ripples.

An aging test is conducted in [190] using the same ripple current waveform as in [189]. In each cycle, lithium battery cells are charged by ripple current, and then discharged on a resistor until 2.8 V. After 2000 cycles, the capacity losses of the DC-charged cell and the ripple-charged cell are respectively 15.1 % and 16.3 %. An additional capacity loss of 1.2 % is attributed to the ripple current. However, [190] deems this additional capacity loss as acceptable. As only two cells are tested, the generality of the conclusion could also be limited.

[191] tests the influence of switching frequency ripples in a DC/DC converter [191]. Using two filter configurations, two 8 kHz ripple waveforms with different amplitudes, 37.5 A and 1 A respectively, are generated. The two current waveforms are applied on two 40 Ah battery packs. A slightly higher capacity loss is observed on the pack tested by the higher ripples. Nonetheless, [191] concludes the difference is not directly caused by the ripples, but by the increased cell temperature, which could have been eliminated with an improved cooling. [191] explains the finding with the intrinsic equivalent double-layer capacitors (EDLC) of the batteries, which can effectively filter the switching frequency ripples.

[192] superimposes sinusoidal ripples at different frequencies onto a constant DC current to test the influence on the battery aging. The frequencies of the ripples are respectively 10 Hz, 55 Hz, 254 Hz and 14.8 kHz. Their amplitudes are fixed at 0.6 C. Based on the experimental results, [192] concludes that the capacity fade and the impedance increase become more significant, as the frequency of the ripples grows.

The most recent result regarding the influence of ripples is published by Brand et al. in late 2018 [193]. NMC cells are tested, and the waveforms of the ripple current are generated by superimposing a sinusoidal current of ±0.2 C onto a 0.225 C DC current. In the experiment, an additional capacity loss is observed on the ripple-tested cells. However, the difference is within 1 %. The difference starts to appear after the first 50 cycles, and does not increase further as the test goes on. Therefore, Brand et al. suggests that battery cells can tolerate the current ripples.

Besides the direct experimental investigations, [193] also systematically summarizes and compares the results in previous studies, especially the experimental results in [188]. [193] reveals that the battery aging is not significantly influenced by ripples, as long as the temperature is kept the same as that of the cells tested by DC current. The contradictions with [188] are mainly explained by the difference in the method of cell capacity measurement.

The configurations and conclusions of experiments in [188]–[193] are summarized in Table 6.1. In the column of conclusions, neutral means no influence identified, while negative means negative influences of the ripple current are concluded. The features of the current waveform in Figure 6.1 are also added to the last row for comparison. It is observed that the test configurations and the conclusions of existing studies are rather inconsistent. [193] indicates that the inconsistency of conclusions is caused by the thermal management and measurement methods in different experiments, and that current ripples are generally not harmful to batteries.

Nonetheless, due to the differences between the ripple waveform in [193] and the ripple waveform in the CHB, the conclusions in [193] are not directly applicable for the batteries in the CHB, although its analysis is detailed and convincing. First, compared to the sinusoidal ripples with a single frequency in [193], the ripple current in the CHB is a compound of multiple frequencies, as visible in Figure 6.1. An additional compound effect of different frequencies is still possible.

Second, the peak value of the ripples in the CHB is much higher than those in [188]–[193]. It is not easy to confirm if the conclusion in [193] still holds, when the amplitude of the ripples becomes higher.

Third, the most significant difference is that the battery current in the CHB crosses zero frequently, and hence forms a large amount of micro cycles. Similar micro cycles do not exist in the waveforms of the previous studies, except for [188], as visible in Table 6.1. That means the ripples in [189]–[193] do change the charge throughput, which is one of the most important driving factors of the battery aging. In the analysis of [193], however, this factor is only briefly mentioned when explaining the contradictions with [188].

Hence, due to the difference in ripple waveforms, the findings in [193] cannot be directly applied for the batteries in the CHB. As a concrete conclusion cannot be drawn based on previous experimental studies, a specific investigation for the ripple current in the CHB is still necessary.

Table 6.1: The configurations of experiments in previous studies regarding the influence of ripples

Experiments	Configurations of experiments					
	Shape	Micro cycles	Frequency	Maximum ripple amplitude C-rate	Waveform mean C-rate	Conclusion
[188]	square	X	1 Hz-10 kHz	0.5	0	negative
[189]	half sine		120 Hz	0.25	0.3	neutral
[190]	half sine		120 Hz	0.52	0.67	neutral
[191]	triangle		8 kHz	1	0.75	neutral
[192]	sine		10 Hz-14.8 kHz	0.6	0.8	negative
[193]	sine		1 Hz-30 kHz	0.2	0.225	neutral
Figure 6.1	compound	X	200 Hz&10 kHz	2.5	0.8	-

Additionally, for the investigation on the ripple current in the CHB, the existing battery aging models [194]–[197] are not capable of generating a concrete conclusion, due to the limit of the time resolution and modelling approach. Existing battery aging models in [194]–[197] are parametrized by regressing the measured capacity and impedance in aging tests. The time resolution is limited to the cycle level. The obtained models are not able to incorporate the influence of high frequency ripples. Furthermore, in an aging simulation, the conventional ECM [47] is often used to provide inputs to the cell aging models. However, according to the experimental results in [193], the ECM tends to neglect the filtering effect of the battery cells and significantly overestimate the aging.

As a dedicated investigation is not possible to be conducted via simulations, an experimental investigation for the CHB is necessary, so that the long-term influences of the current waveform in the CHB can be monitored. In the next section, the configurations of such a long-term experiment of battery cells will be introduced, including the design of the testing hardware and the parameters of the waveforms.

6.2 Approach

To enable the experimental investigation, a test rig is designed, due to the lack of commercial testing equipment to generate the desired high frequency current waveforms. After introducing the design of the testing hardware, the configurations of the aging experiment are specified. The purposes of the experimental configurations are further explained.

6.2.1 Design of the Testing Hardware

To test the aging behavior of the batteries in the CHB, there are three important requirements for the testing hardware. First, the hardware must be able to change the current rapidly according to the command, so that an undistorted high frequency current waveform can be generated to resemble the waveform in Figure 6.1. Second, the generated waveform must be accurate. Otherwise, the results might be influenced by the inaccuracy of the current waveform. Third, the hardware must be able to do the cycling test automatically and stay thermally stable. As the experiment is expected to last several months, manual interference in every cycle must be avoided.

However, after a thorough search, no commercial equipment is able to meet the requirements, particularly the requirement of high frequency compatibility. The high frequency current generator only supports sinewaves with a low amperage [198, p. 173], which is specifically designed for the impedance tests instead of aging tests. Furthermore, the commercial equipment cannot generate the micro cycles in the current waveform, due to the lack of bidirectional output capability. Hence, the high frequency current waveform in Figure 6.1 cannot be generated by commercial equipment. A set of specifically designed hardware is thus required.

Nonetheless, to design a dedicated test rig, it is not wise to put cells directly in H-bridges and discharge to a load resistor. On the one hand, since the accuracy of the current is determined by the accuracy of the load resistor, it is difficult to meet the requirement of accuracy. On the other hand, as this configuration needs additional power sources to charge the tested cell, test automation is also difficult to realize. Therefore, in this dissertation, a set of testing hardware is designed using power analog circuit. A simplified schematic of the design is in Figure 6.2, the detailed schematic is provided in Appendix C.

The circuit is mainly composed of three parts, a digital to analog conversion (DAC) circuit, a main circuit composed of two power operational amplifiers (opamp), and a feedback analog circuit. The directions of signals are also marked in Figure 6.2.

The DAC circuit is composed of a DAC chip and a reference voltage generator (REF0525 from Texas Instrument, TI) to generate an accurate 2.5 V reference voltage, V_{REF}, for the DAC chip and the power opamp circuit. The DAC circuit receives commands from the micro-controller unit (MCU) and generates the input voltage, V_{IN}, for the power opamp circuit.

Once V_{IN} is shifted away from V_{REF}, a current can be generated for the tested cell. Via a 0.1 Ω sampling resistor, R_{Sample}, the value of the current is sent to the feedback analog circuit to generate an appropriate feedback signal. This feedback signal is then sent to the power opamp circuit to form a negative feedback loop. In this way, the current of the tested cell can be stabilized. Hence, the command given by the MCU can be converted to the desired current value, I_{cell}, for the tested battery cell. There is no feedback signal sent to the MCU. The closed-loop control of the current is only realized by the analog components in the circuit.

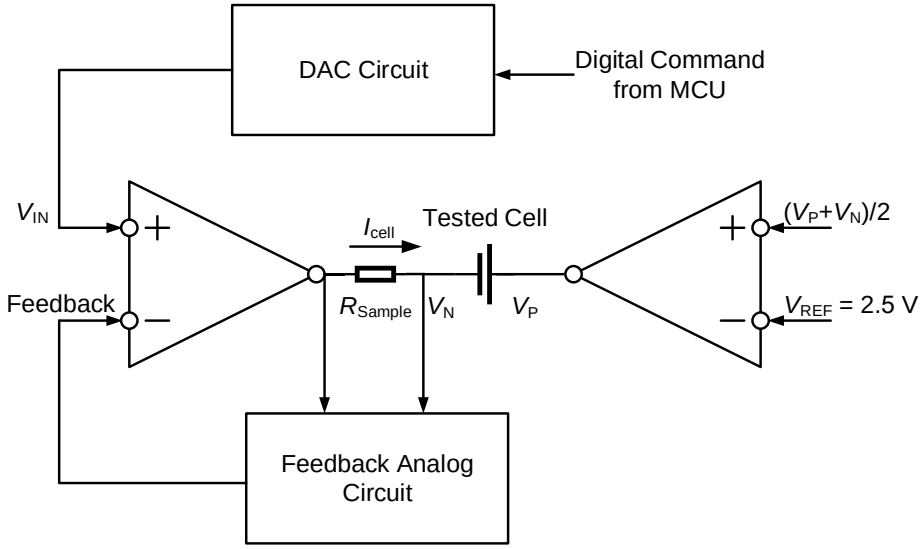


Figure 6.2: Simplified schematic of the testing hardware to generate high frequency current

Assuming all the opamps are ideal, i.e., their open-loop gains are infinite, the conversion from V_{IN} to I_{cell} can be calculated by eq. (6.1). K_{AMP} is the amplification ratio determined by the design of the feedback analog circuit. K_{AMP} is set to be 4. V_{IN} can be shifted in two directions to change the direction of I_{cell}.

$$\begin{cases} I_{\mathrm{cell}} = K_{\mathrm{AMP}}(V_{\mathrm{IN}} - V_{\mathrm{REF}}) \\ V_{\mathrm{cell}} = (V_{\mathrm{P}} - V_{\mathrm{N}}) \\ V_{\mathrm{REF}} = (V_{\mathrm{P}} + V_{\mathrm{N}})/2 \end{cases} \tag{6.1}$$

In eq. (6.1) and Figure 6.2, V_{P} and V_{N} are respectively the cathode voltage and anode voltage of the tested cell, referencing to the ground of the analog circuit. Connecting the average value of V_{P} and V_{N} back to the power opamp network, due to the virtual short circuit property of ideal opamps, the average value of V_{P} and V_{N} is forced to equal V_{REF}, i.e., 2.5 V. Hence, the output voltage swing of the two opamps can be limited in a safe range. Using V_{cell} to represent the voltage of the tested cell, the values of V_{P} and V_{N} can be obtained by solving the two equations in eq. (6.1). Hence, it is confirmed that the circuit can safely generate the desired current. The basic functionality for the test is realized.

To meet the three requirements, the components in the circuit should be carefully selected. A high-speed DAC chip must be used, in order to meet the requirement of high frequency. Hence, the DAC TLV5616 from TI is selected.

To meet the requirement of high accuracy and avoid waveform distortions during transients, the opamps in the circuit are required to have high open-loop gains in a wide range of frequency. Considering the non-ideal open-loop gains of opamps, i.e. the gain is not infinite, the error of the current, I_{dev}, with regard to the desired value is calculated in eq. (6.2).

$$I_{\mathrm{dev}} = \frac{K_{\mathrm{AMP}} V_{IN}}{(G_{\mathrm{F}}+1)R_{\mathrm{Sample}}} - \frac{K_{\mathrm{AMP}} V_{\mathrm{REF}}}{G_{\mathrm{P}} + R_{\mathrm{S}} K_{\mathrm{AMP}}} + \frac{K_{\mathrm{AMP}} V_{\mathrm{BAT}}}{2(G_{\mathrm{P}} + R_{\mathrm{Sample}} K_{\mathrm{AMP}})} \tag{6.2}$$

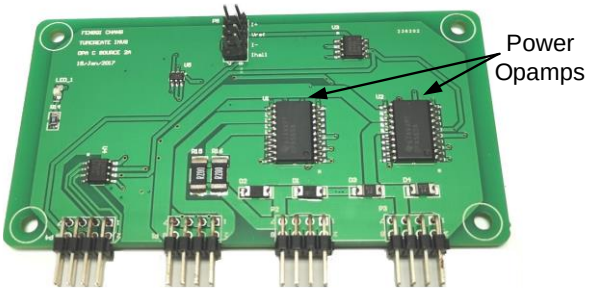
G_{F} is the open-loop gain of the feedback analog circuit. G_{P} is the open-loop gain of the power opamp circuit. Substituting the sampling resistance value of 0.1 Ω, to limit the error of current within 0.01 A in all possible situations, G_{F} must be higher than 3000 at the desired high frequency. G_{P} should be higher than 200. To meet this requirement, the power opamp OPA569 is selected

for the power opamp circuit, and the opamp OPA890 is selected for the feedback circuit. The two opamps are both from TI. Even at 100 kHz, which is ten times the maximum frequency of the ripples to be tested, their open-loop gains are still higher than the minimum requirement [199], [200]. Therefore, the accuracy of the current is ensured.

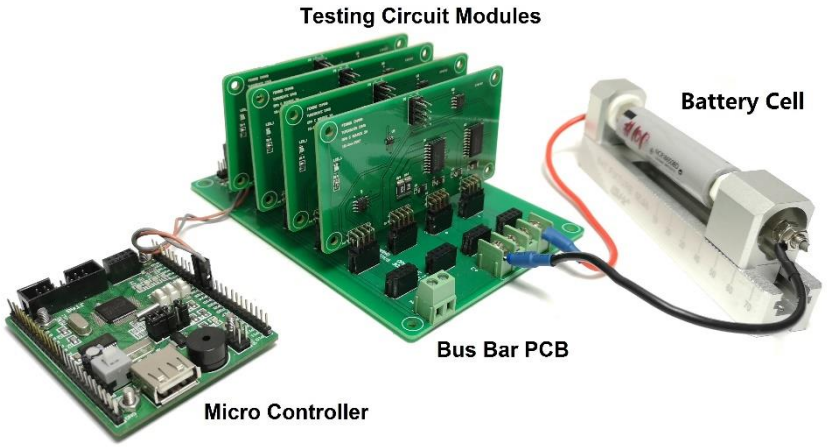
The last requirement, the automation of the cycling test, is relatively simple to meet, as the circuit has the bidirectional output capability. By programming the MCU appropriately, this function can be realized. Hence, the hardware design is able to meet the three requirements.

The picture of the hardware implementation is shown in Figure 6.3(a). Its maximum current is ±2 A, limited by the maximum current of the power opamp OPA569. To generate a higher current in the test, multiple modules should be paralleled to form a test rig. The digital signal interfaces of the modules are paralleled as well, so that all the modules receive identical commands from the same micro controller and behave identically. As a result, after the parallelization, the three requirements can still be met by the test rig.

An example of the assembled testing rig for one cell is in Figure 6.3(b). The wiring details are excluded. Four modules are vertically inserted in a larger PCB. The larger PCB at the bottom is only serving as a bus bar board paralleling the digital and power interfaces of the modules. The bus bar PCB can parallel up to six modules in total and generate a maximum current of ±12 A to test one cell.



(a) One module of the designed circuit



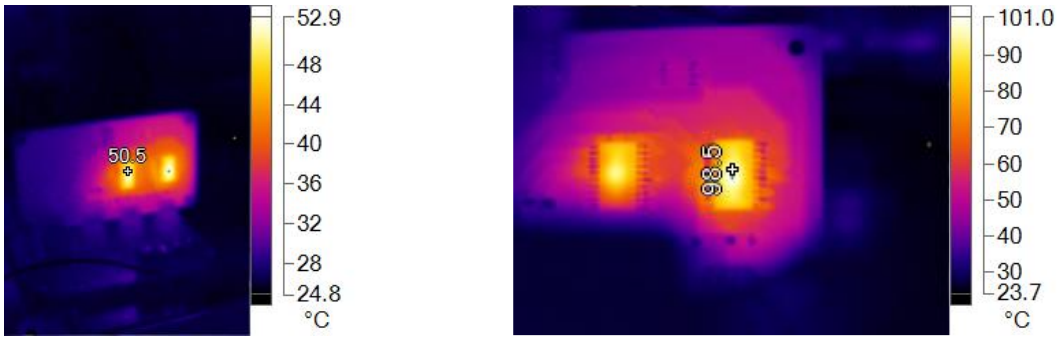
(b) Assembled test rig for one battery cell

Figure 6.3: Pictures of the designed hardware

Additionally, before the experiment, it is also necessary to ensure the thermal stability of the hardware in long-term experiments, because the discharging process involves energy dissipation and could create potential problems. Specifically for the circuit design in Figure 6.2,

the energy of the battery is dissipated on the power opamps. Hence, it is necessary to verify if the opamps are able to endure the possible high temperature during discharge.

The thermal images of one module during maximum current charge and discharge are respectively depicted in Figure 6.4(a) and (b). The images are taken after the circuit has been continuously operating at the maximum current, 2 A, for more than 15 min. The ambient temperature is 25 °C and the circuit does not have active cooling. Hence, the measurements in Figure 6.4 are conducted in the thermal steady state. The maximum and minimum temperatures are marked by the temperature scale of the images. Due to the automatic calibration of the thermal camera, the color scale in the two thermal images is different.



(a) Thermal image during charge (b) Thermal image during discharge

Figure 6.4: Thermal stability tests in charge and discharge process

In Figure 6.4(a) and (b), the two bright rectangles correspond to the two power opamps in Figure 6.3(c). In the maximum current charge test, Figure 6.4(a), the measured temperature of the opamp is 50.5 °C, which is a safe temperature for semiconductors. The temperatures of the two opamps are also similar. Hence, the thermal stability during maximum current charge is verified.

In the maximum current discharge test, Figure 6.4(b), as the energy of the battery is only dissipated on the opamp on the right side, its temperature is significantly higher than that on the left side. That is visible via the brightness and the size of the bright area. The measured temperature of the right opamp is 98.5 °C, much higher than the temperature in the charge test, but there is still a safety margin of 26.5 °C to reach the maximum operation temperature, 125 °C. Therefore, in the experiment, by applying forced-air cooling to the opamps, the thermal stability of the circuit can be well ensured.

As a summary of this section, the proposed hardware design can safely and automatically cycle the battery cells with the desired ripple current waveform in Figure 6.1. Following the introduction of the hardware, the configurations of the experiment are explained in the next section.

6.2.2 Configurations of the Experiment

The configurations of the experiment are introduced in three steps. First, the battery cells used in the experiment are introduced. Then the parameter settings of the ripple current waveform for each cell are explained. In the end, the procedures of the experiment are also stated.

For the aging experiment, Panasonic NCR18650BD cells are used. The cathode material of these cells is NMC and the gravimetric energy density is 217 Wh/kg. The NCR18650BD cell has been released to the market for more than four years and is not a state-of-the-art model. Nonetheless, due to its limited cycle life, the total time of the experiment can be significantly reduced. According to the datasheet [201], the full cycle life of the cell is only 500. After 500

charge/discharge cycles, with a cycle depth of 100 % (corresponding to cycling between 4.15 V and 2.5 V), the cells are expected to lose 20 % of their original capacity.

It is also worth noting that the NCR18650BD cells used in the experiment were obtained in 2014, came from an official distributor in a large quantity. The authenticity of the cells can be ensured. Since the acquisition, these cells were kept untouched for three years. The storage environment had a constant temperature of 25 °C. Before the aging experiment in the fourth quarter of 2017, the cells were taken out for initial characterization. Nonetheless, compared to the typical values of brand new cells in the datasheet [201], no significant calendar aging was identified in the measurements. Therefore, these cells were considered as new cells for the aging experiment.

A possible explanation for the limited calendar aging during such a long time is that the cells are kept at an ideal SOC and temperature. According to the aging model in [197], keeping the cells at 25 °C and 3.3 V (the open circuit voltage of the cells when taken out for initial characterization, corresponding to around 15 % SOC), the calendar aging for three years is only expected to cause a capacity reduction less than 2 %. The expected impedance increase is limited to 4 %. Hence, even after a long-time storage, the degradation is still not significant. Furthermore, according to the aging model in [197], the expected calendar aging is only equivalent to the effect of four to five full cycles. Hence, the conditions of the cells are still acceptable for the experiment to last 500 full cycles.

After verifying the feasibility of the cells, in total eight cells are taken for the aging experiment. Each cell is numbered and tested in one test rig shown in Figure 6.3. The parameters of the current waveforms are listed in Table 6.2. These current waveforms are only used for discharging the cells. The charging is still conducted by the DC current.

Table 6.2: The parameters of the current waveforms used for cell aging test

Cell Number	Parameters of the current waveform				
	DC or ripple	Switching frequency	Power factor	AC frequency	Average C-rate
Cell 1	DC	-	-	-	0.8 C
Cell 2	DC	-	-	-	0.8 C
Cell 3	Ripple	2 kHz	0.8	100 Hz	0.8 C
Cell 4	Ripple	5 kHz	0.8	100 Hz	0.8 C
Cell 5	Ripple	10 kHz	0.8	100 Hz	0.8 C
Cell 6	Ripple	10 kHz	0.8	100 Hz	0.8 C
Cell 7	Ripple	10 kHz	0.9	100 Hz	0.8 C
Cell 8	Ripple	10 kHz	0.7	100 Hz	0.8 C

First, all the current waveforms have the same discharge C-rate, 0.8 C, in case that the difference in the average C-rate could potentially distort the results. To ensure the evenness of the average C-rate, before the experiment, the output current waveforms of all the test rigs are measured by the current probe Rohde & Schwarz HZO51 and the oscilloscope HMO724. The average values of all the output current waveforms are within 2.4±0.02 A, i.e., the error is within 1 %. Hence, the experiment cannot be distorted by the inaccuracy of the average C-rate.

The current waveforms are differentiated from each other by four other parameters. The first parameter is whether the current is DC or contains ripple. Cell 1 and cell 2 are tested by the DC current to form the control group. The other six cells are tested by different ripple current waveforms in the aging test, and they form the experimental group.

The second parameter is the switching frequency. The frequency of the switching frequency ripples is varied, but the amplitude of the ripples and the micro cycles stay constant. Hence, comparing the aging results of cell 3 to cell 6, the influence of high frequency ripples can be identified, as the current waveforms only differentiate from each other by the switching frequency. The experiments on cell 3 to cell 6 are similar to the experiments in [188]–[193], where the influence of frequency is the focus.

Another parameter is the power factor, $\cos\theta$. As demonstrated in Figure 6.1, when $\cos\theta$ is not 1.0, the battery current contains double-frequency ripples. If $\cos\theta$ decreases (phase lag increases), the negative part of the waveform will expand, because the zero cross point of the AC voltage moves further to the left and the current is flipped to negative earlier. As a result, the depth of the micro cycles increases. At a given average C-rate, to compensate for the increased negative current, the peak value of the current should also be increased. Therefore, as $\cos\theta$ decreases, the peak value of the current and the depth of micro cycles increase accordingly, which could deteriorate the battery aging. The experimental group for $\cos\theta$ is composed of cell 5 to cell 8. The power factor is shifted from 0.8 to 0.7 and 0.9. The other parameters are not changed.

The influence of AC frequency is not tested in this experiment, because its potential influences could be partially observed in the experimental group for the power factor. When the AC frequency changes, the maximum C-rate and switching ripples all stay the same. The depth of one micro cycle changes with the AC frequency, due to the change of the micro cycle duration.

After introducing the discharging current waveforms, the test profile of one test cycle is demonstrated in Figure 6.5. The profile is applicable for all the cells, regardless of the discharge waveform settings.

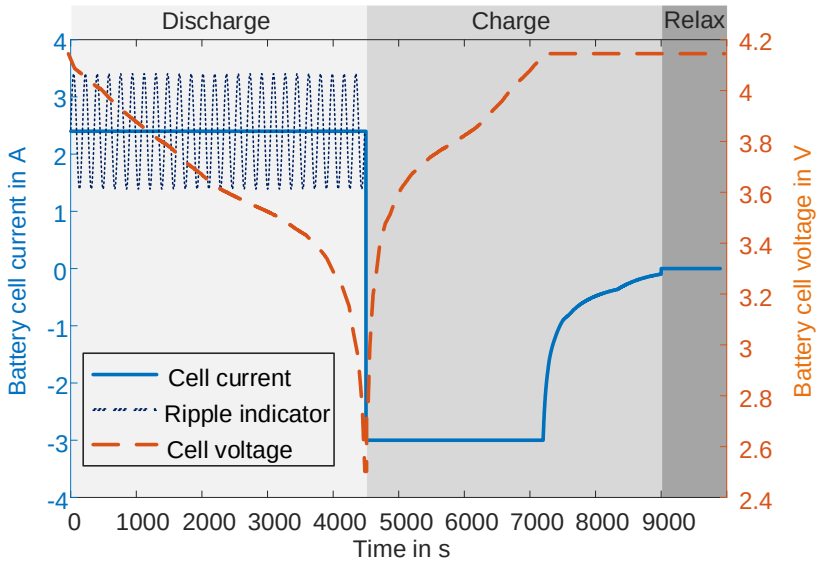


Figure 6.5: Test profile of the aging experiment

As visible in the voltage curve (the dotted curve, corresponding to the right Y-axis), every test cycle starts from a cell voltage of 4.15 V. In each cycle, the cells are first discharged by the

corresponding 0.8 C current waveforms in Table 6.2, illustrated by the ripple indicator and the current curve (solid curve, corresponding to the left Y-axis). A positive current value refers to discharge. The discharge continues, until the terminal voltage of the battery decreases to 2.5 V, and the charge immediately starts.

The charge of all the battery cells follows the common CC-CV scheme. No ripple is injected during the charging for all the cells. The scheme starts with 3 A CC charging (1 C charging) and switches to CV charging, once the terminal voltage reaches 4.15 V. When the charge current is lower than 100 mA, the charging process stops.

In the end, after the cells are fully charged, a relaxation time of 15 min is provided to the cells, before entering the next testing cycle. The cycle depth of this testing profile is thus 100 %. One cycle for a brand new cell takes almost three hours.

After every 50 cycles, the cells are taken out from the testing rigs to measure their capacity (1 C discharge capacity) and inner resistance (200 ms DC resistance at 80 % SOC) manually. Due to the inaccessibility of the commercial testing equipment, the cells are manually measured by a device built in-house [202], and an electronic load Agilent N3300A. Nonetheless, the accuracy of the measurement can still be ensured, because the accuracy of the electronic load is 0.1 %, according to the datasheet [203]. As the setup only has one channel, the measurement of eight cells takes up to several days. Hence, including the measurements, the aging experiment in total lasted more than three months. The results of the aging experiment are discussed in the next section.

It is worth noting that the results will also contain calendar aging, because of the long time of the experiment. Nonetheless, as the primary goal of the experiment is only to answer if the CHB accelerates the degradation of batteries or not, and the cyclic aging is much more significant, the two types of aging mechanisms are not explicitly differentiated in the analysis in the following sections.

6.3 Result

First, the capacity reductions of the eight cells are discussed. The measured capacity reductions of the cells are in Table 6.3. The results are not plotted together in one figure, because the reduction curves will intertwine significantly in the figure, which could cause difficulties for the comparison. Therefore, in this section, necessary curves are only plotted in individual figures for each analysis.

In the results, it is first observed that the capacity reduction curves of cell 4, cell 6 and cell 8 are abnormal. The corresponding three columns are also marked in Table 6.3. After 500 cycles of aging test, their residual capacity is still around 85 % of their initial capacity. This value is much higher than the expected value, 80 %, in the datasheet [201]. From the 200th cycle to the end of the experiment, the three abnormal cells only loose about 5 % of their capacity, while the capacity reduction of the other five cells is around 10 %.

The capacity reductions of the three abnormal cells are lower than the cells tested by DC current, so a negative conclusion for the CHB cannot be formed based on them. However, as these three capacity reduction curves are significantly in favor of the CHB, in order to evaluate the CHB concept more critically, the three curves are excluded from the analysis below.

Moreover, because the aim of this chapter is only to determine whether the ripples in the CHB is harmful to lithium batteries or not, and the three curves are in favor of the CHB, the three abnormal curves do not influence the generality of the obtained conclusion. The possible reasons for the three abnormal capacity reduction curves are briefly discussed in the next section.

Table 6.3: The capacity of the cells measured over the whole aging experiment

Number of finished cycles	The capacity normalized to the initial capacity of each cell							
	Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8
0	100 %	100 %	100 %	100 %	100 %	100 %	100 %	100 %
50	92.7 %	92.6 %	92.4 %	93.9 %	92.2 %	92.9 %	92.5 %	93.3 %
100	89.7 %	89.5 %	89.2 %	91.4 %	88.9 %	89.9 %	89.4 %	90.6 %
200	88.3 %	87.4 %	88.3 %	90.4 %	85.4 %	91.8 %	86.8 %	89.8 %
250	86.2 %	85.9 %	86.3 %	89.1 %	82.8 %	91.5 %	85.0 %	89.5 %
300	84.4 %	84.8 %	86.3 %	87.2 %	81.8 %	90.4 %	84.4 %	87.8 %
350	85.1 %	82.7 %	83.7 %	88.6 %	80.4 %	89.9 %	83.2 %	89.9 %
400	82.9 %	81.9 %	82.4 %	87.9 %	80.6 %	87.3 %	81.7 %	89.2 %
450	82.5 %	82.6 %	81.6 %	86.7 %	78.9 %	86.3 %	80.2 %	86.5 %
500	79.8 %	80.2 %	78.6 %	85.1 %	77.5 %	85.1 %	77.6 %	86.2 %

Excluding the three abnormal curves, the average capacity reductions of the cells with and without current ripples are compared, Figure 6.6. The solid curve depicts the average capacity reduction of the two cells tested by the DC current, i.e., cell 1 and 2. The dotted curve depicts the average capacity reduction of cell 3, cell 5, and cell 7, which are tested by different current ripples.

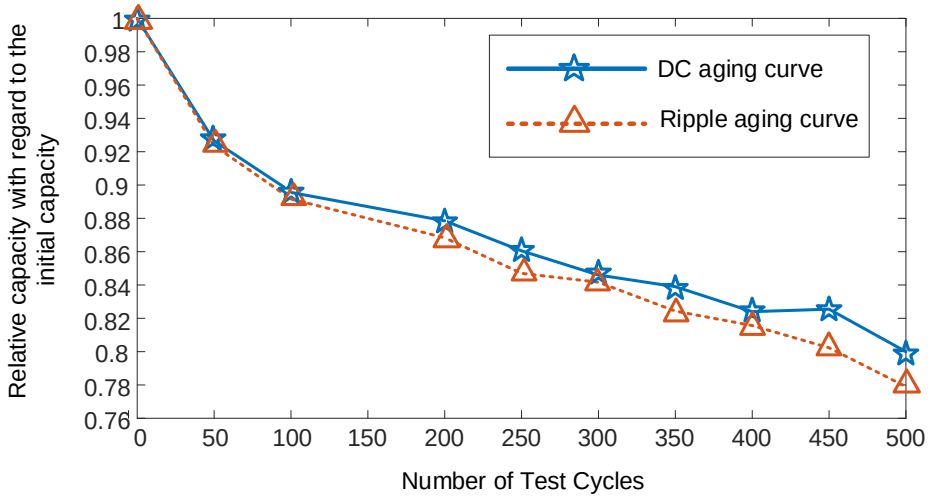


Figure 6.6: Average capacity reduction curves of the cells tested by DC and ripple current

As illustrated in Figure 6.6, in the first 100 cycles, there is no visible difference between the cells tested by DC current and ripple current. Nonetheless, after the 200th cycle, a small difference

around 2 % is established. From then on, the average capacity loss of the ripple-tested cells is constantly around 2 % higher than that of the DC-tested cells. At the end of the experiment, the DC-tested cells still have a capacity of 80.0 % on average, while the average residual capacity of the ripple-tested cells is 77.9 %.

In the experiment, the ripple current is identified to cause an additional capacity loss of 2.1 % on average. However, this additional loss is small, and it could be overestimated, due to the randomness of the aging behavior and the limited number of samples. Besides, the additional capacity loss appears after 100-200 full cycles, and does not develop further, corresponding well to the result in [193], which only measured an additional capacity loss lower than 1 %. As an increase in the aging speed is not observed, and the additional capacity loss is small and could be overestimated, the CHB remains a valid concept.

Moreover, the small additional capacity loss does not influence the validity of the cost assessments in chapter 5. First, the small additional capacity loss only appears when the battery is cycled by 100-200 full cycles. Hence, it does not influence the calculation of the initial purchasing cost. Second, since the CHB has the capability to actively balance the capacity of modules, especially for aged and thus nonhomogeneous batteries, the small additional capacity reduction could be compensated by the increased usable capacity on the pack level [114]–[117]. Consequently, the CHB does not require additional battery capacity to counterbalance the possible additional capacity loss, and hence does not cause a higher cost even in the long term.

Besides the comparison on the average level, to investigate the influence of the power factor and the switching frequency, the aging curves of cell 3, 5 and 7 are also compared to each other in Figure 6.7. In the first 100 cycles, almost no difference can be identified between the three curves. The difference starts to appear from the 200th cycle. From the 200th cycle, the residual capacities of cell 3 and cell 7 are constantly higher than that of cell 5. However, from the 400th cycle until the end, the difference of the three curves converges. Cell 3, cell 5 and cell 7 even have almost the same residual capacity in the end. After 500 full cycles of tests, no significant difference is caused by the different switching frequencies or the different power factors.

A divergence of the capacity reduction is observed from the 200th cycle to the 400th cycle. However, due to the limited number of samples and the convergence at the end of the experiment, it is difficult to attribute the divergence to the difference in switching frequencies or power factors. It is more likely that the divergence is a result of the stochastic property of the battery aging behaviors, which were reported in previous studies as well [204]–[207].

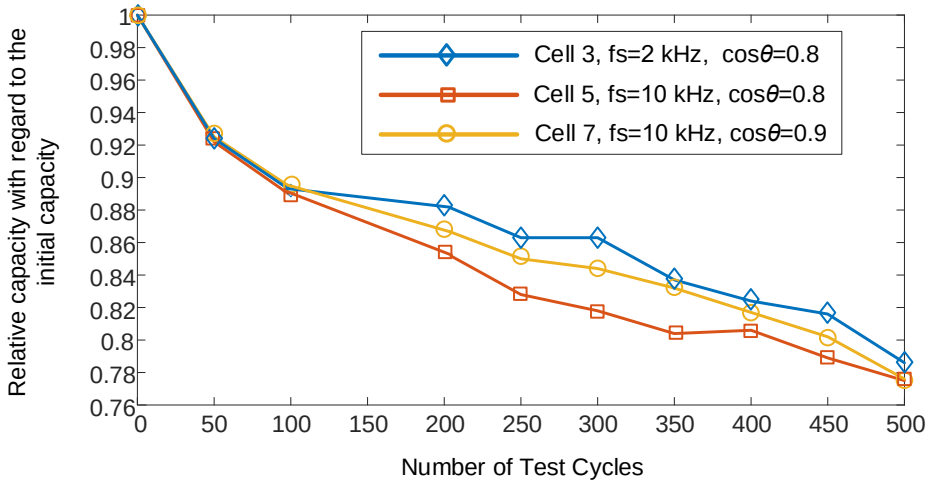


Figure 6.7: Three normal aging curve of the cells tested by different ripple current waveforms

Besides the capacity reduction curves, the records of the inner resistance are also analyzed. The aging curves of the 200 ms DC resistance of the cells are plotted in Figure 6.8. The assertions based on the capacity reductions curves are further supported by the aging curves of the inner resistance.

It is observed that the ripples do not influence the battery aging in terms of the inner resistance. Except for cell 6, which constantly has the lowest resistance, the resistance values of the other seven cells are rather close to each other over the whole experiment. Excluding cell 6, it is also observed that the spread of the resistance values is only doubled (from 10 mΩ to 20 mΩ) after 500 cycles of test. This extent of inhomogeneity growth is also observable in the aging tests that use identical DC current to test all the cells [194]–[197], [204]. Therefore, except for cell 6, the other cells cannot be differentiated from each other by the difference in resistance growth. Hence, the resistance curves further prove that the ripple current in the CHB does not significantly influence the aging of NMC batteries, regardless of the ripple parameters.

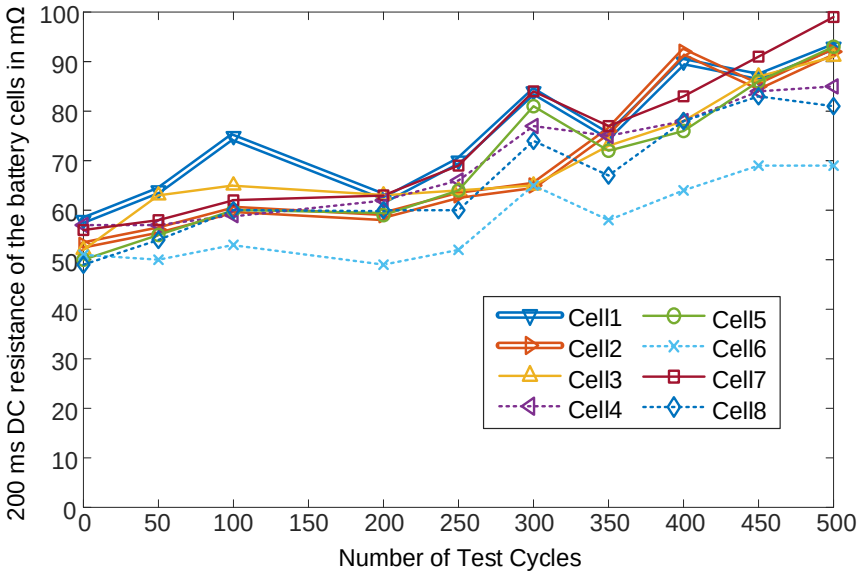


Figure 6.8: 200 ms DC resistance of the cells over the aging test

In addition, the resistance curves of the cells are more consistent than the capacity curves. The three abnormal cells (cell 4, 6 and 8, marked by dotted lines) still have the lowest inner resistance at the end of test, but they are not as recognizable as they are in the data of capacity reductions. Hence, the resistance curves can form a stronger proof for the harmlessness of the ripple current in the CHB.

Based on the experimental results and the analysis above, a conclusion can be drawn that the CHB does not significantly influence the aging of NMC battery cells. In the tested range, the switching frequency and the power factor are also confirmed not to be influential for the aging behaviors. The CHB might be able to cause an additional capacity loss of 1-2 % at the end of life of batteries, but the additional capacity loss is small and could be counterbalanced by the pack level balancing capability of the CHB. The effect of the balancing capability will be quantitatively calculated in the dissertation of Mr. Felix Roemer, considering different types of cells and different extent of aging. Therefore, even considering the possible additional capacity loss caused by the CHB, this concept remains preferable. The conclusion is supported by the records of the capacity and the inner resistance.

The validity of the conclusion is not restricted to the CHB, but can be generalized to all the single-phase power supply systems using lithium batteries, where the current ripples have exactly the same patterns as the ripples in the CHB. Besides the cascaded multilevel automotive inverters [114]–[117], this type of systems includes onboard chargers and household energy storage systems. Therefore, in these systems, the efforts and costs to suppress battery current ripples could be reduced for future designs. A possible explanation to that phenomenon is that the equivalent double layer capacitor of the cell could filter the current ripples significantly [188].

In the next section, the experimental results are further analyzed. By comparing the results in this section to those in the previous studies, an overview of the potential influences of the ripple current can be formed. Based on the overview, the conclusion of the experiment can be generalized accordingly.

6.4 Discussion

In this section, first, the possible reasons for the three abnormal capacity reduction curves are briefly discussed. Second, the conclusion obtained from the experiment is compared to the conclusions of the previous studies. The similarities and the contradictions are explained. In the end, based on the explanations, the influence of the CHB on the battery aging is confirmed to be generally insignificant in practical implementations.

6.4.1 Possible Explanations of the Unexpected Curves

The first section of discussion aims to provide brief explanations for the three unexpected capacity reduction curves. The three capacity reduction curves are illustrated in Figure 6.9. The average capacity reduction of the three normal ripple-tested cells (the ripple-tested curve in Figure 6.6) is also added to Figure 6.9 as a reference.

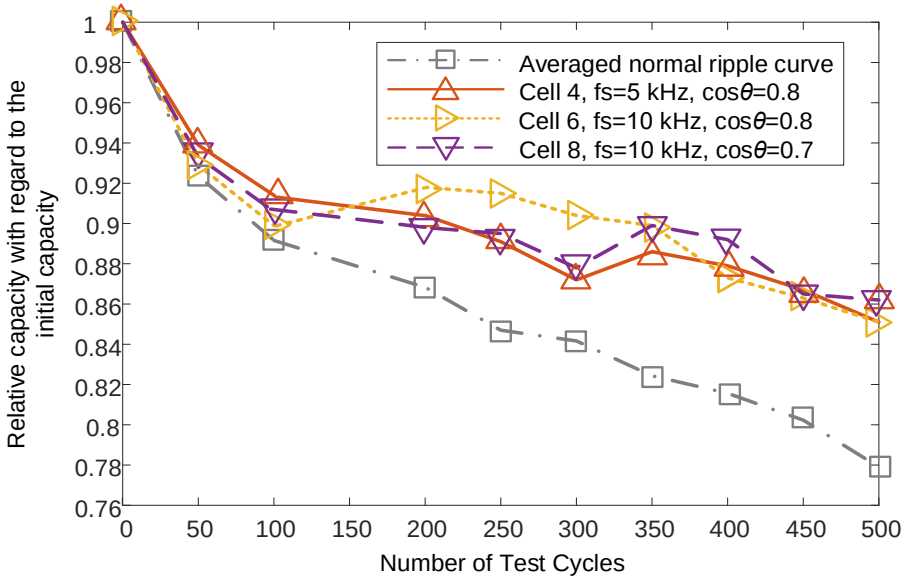


Figure 6.9: Capacity reduction curves of the three abnormal cells

The three unexpected curves diverge from the normal curve since the 50th cycle, the first measurement after the experiment starts. Therefore, the first possible explanation is that these

three cells are not cycled by a depth of discharge (DOD) of 100 %, so that the aging of the three cells is much slower than the other five cells. The error of DOD could be mainly caused by occasional faults of the cell voltage measurement, which are not identified or eliminated during the verifications of the test rigs.

Besides the problem of the program, another explanation is that these three cells are not well isolated from the forced-air cooling of the test rigs. As the three cells could have been actively cooled during the test and have a lower temperature, the speed of aging could naturally be decreased.

It is also possible that the three unexpected curves are caused by a deterministic mechanism that is not considered in the experiment design, e.g., the capacity recovery effect reported in [208]–[211], which could be triggered by the longer relaxation period provided to the three cells in each manual measurement operation. To investigate and confirm the real reason for the three abnormal curves, a dedicated long-term experiment would still be required.

However, as the aim of this chapter is only to determine whether the CHB is harmful to lithium batteries, and the three abnormal curves in favor of the CHB do not influence the conclusion obtained in the last section, such an experiment is not within the scope of the research. Because of the same reason, the possible explanations for the three unexpected curves are also only briefly discussed without further analysis.

6.4.2 Explanation of Similarities and Contradictions

In this chapter, the ripples in the CHB are experimentally proven to have a negligible influence on the aging of lithium batteries, which is similar to the conclusions in [189]–[191], [193], although the ripples in the CHB have much higher peak values and contain micro cycles of charge and discharge. However, the conclusion of this chapter is contradicting the conclusion of [188], which also implemented micro cycles in the aging test of lithium batteries. Therefore, in the second part of the discussion, the similarities and the contradictions among different studies are explained based on a detailed analysis of the waveforms, in order to establish an aligned perception of the influence of ripple current.

First, this section explains why the results of the experiment in this chapter are similar to those in [189]–[191], [193]. The similarities within [189]–[191], [193] are noticed and summarized by [193], with electrochemical explanations provided. Based on the explanation, [193] further indicates that the current ripples influence the aging via its influence on two stress factors, the temperature increase and the total charge throughput. As long as these two factors are kept unchanged, the ripples are not supposed to cause any influence on the aging. Therefore, to explain the similarity between the experiment in this dissertation and the experiments in [189]–[191], [193], the temperature increase and the charge throughput of the cells in the CHB need to be quantitatively assessed.

The temperature increase is estimated by the RMS value of the battery current, because it is linked directly to the heat generation in the cells. Without filtering, the RMS value of the battery current, $I_{\mathrm{bat\_RMS}}$, in the CHB can be calculated using eq. (6.3).

In eq. (6.3), $I_{\mathrm{bat\_RMS}}$ is determined by the average current, $I_{\mathrm{bat\_ave}}$, the power factor $\cos\theta$, and the modulation index m_{a}. Once $I_{\mathrm{bat\_RMS}}$ is obtained, the RMS value of ripples $I_{\mathrm{ripple\_RMS}}$ can be calculated accordingly by the second equation of eq. (6.3). Using the typical experimental settings in eq. (6.3), i.e., $\cos\theta$ and m_{a} are both 0.8, the value of $I_{\mathrm{ripple\_RMS}}$ equals $0.31 I_{\mathrm{bat\_ave}}$.

That means the RMS value of the ripples is only 31 % of the DC current. Changing $\cos\theta$ to 0.7 or 0.9, the percentage value becomes respectively 48 % and 16 %.

$$\begin{cases} I_{\text{bat\_RMS}} = \dfrac{2I_{\text{bat\_ave}}}{\cos\theta}\sqrt{\dfrac{(1+\frac{1}{3}\cos 2\theta)}{\pi m_{\text{a}}}} \\ I_{\text{ripple\_RMS}} = \sqrt{I_{\text{bat\_RMS}}^2 - I_{\text{bat\_ave}}^2} \end{cases} \tag{6.3}$$

According to the features of the ripples summarized in Table 6.1, the RMS values of the ripples in the CHB are, in fact, comparable to the RMS values of the ripples in [189]–[193]. Hence, the battery cells in the CHB are expected to have a similar temperature increase, compared to the battery cells tested in the previous studies. Therefore, the aging effect of the ripples in the CHB is not much different from the ripples in the previous studies. The peak value of the ripples in the CHB is indeed much higher, due to the switching frequency pulses. However, as the pulses at switching frequency only last a short time, the corresponding RMS values are significantly lower than the peak values.

Besides the RMS value of the current, the charge throughput of the batteries in the CHB is also assessed. In [189]–[191], [193], as the battery current never crosses zero, the charge throughput of the ripple-tested cells is expected to be the same as the throughput of DC-tested cells. However, for the CHB, due to the micro cycles in the current waveform, the charge throughput of the cells is increased. The rate of the additional charge throughput caused by micro cycles, $I_{\text{Q\_Mcycle}}$, is defined in eq. (6.4). The unit of $I_{\text{Q\_Mcycle}}$ is Coulomb per second, instead of directly Ampere, as this value does not describe a real current in the circuit. An analytical solution of $I_{\text{Q\_Mcycle}}$ is provided in eq. (6.4).

$$I_{\text{Q\_Mcycle}} = \frac{\int_0^{T_{\text{AC}}} |\, i_{\text{bat}} \,|}{T_{\text{AC}}} - I_{\text{bat\_ave}} = \frac{2I_{\text{bat\_ave}}}{\pi}(\tan\theta - \theta) \tag{6.4}$$

When $\cos\theta$ is 0.8 or 0.9, $I_{\text{Q\_Mcycle}}$ equals respectively $0.069I_{\text{bat\_ave}}$ or $0.021I_{\text{bat\_ave}}$. That means the micro cycles can only increase the charge throughput by 6.9 % or 2.1 %, on top of the necessary charge throughput. This extent of increase is rather insignificant. According to the aging model in [197], after 500 full cycles, the additional capacity loss caused by the 6.9 % additional charge throughput is estimated to be less than 2 %.

When $\cos\theta$ is 0.7, the charge throughput is correspondingly increased by 14.3 %. If all the increased charge throughput would have an influence on the aging, the expected additional capacity loss would be 6 % at the end of the experiment [197]. Nonetheless, such a significant deterioration is not observed. The only explanation is that the real additional charge throughput seen by the cells is not as high as predicted, due to the filtering effect of the EDLC in the battery cells.

The filtering effect is proven in [188], [193], and a corner frequency of 10 Hz is identified. As the micro cycles of the experiment in this chapter have a frequency of 200 Hz, the effective additional charge throughput of the cells is much less than the value predicted by eq. (6.4). Therefore, the effective charge throughput of the cells in the CHB is not much different from those in [189]–[191], [193], although the CHB triggers micro cycles in the current waveforms. Due to the similarities in terms of the temperature increase and the charge throughput, the similarities of the results in this chapter and in [189]–[191], [193] can be naturally understood.

Second, after explaining the similarity, the contradiction with the conclusion in [188] is also discussed. In [188], all the cells are working in float charging status and tested by ripples at different frequencies. The results are shown in Figure 6.10.

The residual capacities of the cells tested by different frequencies are recorded in Figure 6.10. The three curves are obtained respectively after 50 days, 80 days and 147 days of continuous tests. At the end of the experiment, the cells that are tested by low frequency ripples experience an additional capacity loss of 7 %, while the capacity loss of the cells tested by high frequency ripples shows no difference, compared to the DC-tested cells. Such a significantly accelerated aging caused by the low frequency ripples is not visible in other studies or in this chapter. [193] suggested this contradiction is mainly due to the method of capacity measurement. However, after analyzing the test configurations of [188], the significant difference can be better explained by the charge throughput caused by the ripples.

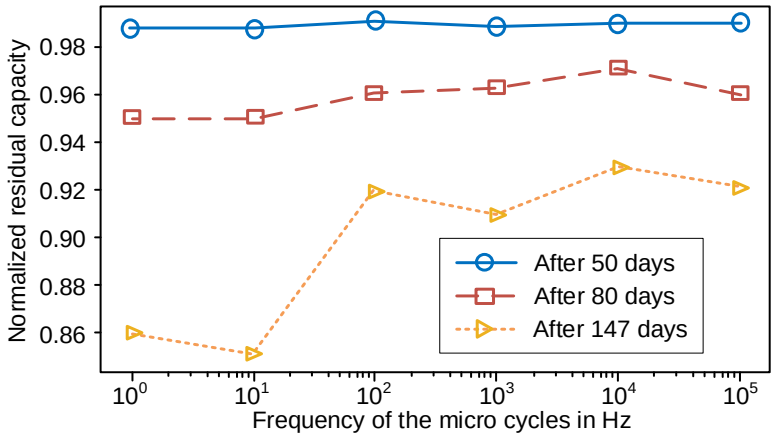


Figure 6.10: The capacity reductions in the aging experiment of [188]

In the experiment of [188], the cells are working in float charging status. The current waveforms injected to the cells only contain micro cycles (±1 A square waves). Average values of the current waveforms are zero, and the cells are not cycled by any load. Hence, in the experiment of [188], the charge throughput caused by the micro cycles is the only determining factor for the aging.

Moreover, as the ±1 A square waves are continuously injected to the 2 Ah NMC cells during the test, at the terminal of each battery cell, the accumulated charge throughput is significant. After 147 days of test, the accumulated charge throughput of each cell is equivalent to 882 full cycles. In comparison, for the CHB, even if the power factor is 0.7, after 500 cycles of test, the charge throughput caused by micro cycles is only equivalent to 35 full cycles, because the throughput is increased by 14.3%, only in discharge process. The charge throughput caused by the micro cycles in [188] is 24 times higher than that in the CHB. Hence, even a small difference in the filtering effect can cause a rather large impact on the aging of the cells in [188].

For micro cycles at higher frequencies, because the large amount of additional charge throughput can be removed completely, no extra aging is observed on the cells. That explains the consistent aging behaviors of the cells tested by the ripples at 100 Hz or a higher frequency. For the micro cycles at lower frequencies, because the throughput can only be partially filtered, a significant impact on the aging can be expected, which explains the 7 % extra capacity loss.

In fact, according to the aging model in [197], the 7 % extra capacity loss corresponds to 180 effective full cycles. That means around 80 % of the additional throughput at the terminal is removed by the filtering effect. However, the remaining effective charge throughput is still sufficient to cause a significant extra capacity loss.

Therefore, the conclusion in [188] is also reasonable. The contradiction is mainly attributed to the amplified impact of the micro cycles, which is caused by the configuration of float charging in the experiment and the continuous exposure to micro cycles. In [189]–[191], [193] and the experiment of this chapter, however, the impact of micro cycles is rather restricted.

In the end, after confirming the negative conclusion in [188] regarding the ripples is also reasonable, two preconditions for a ripple current waveform to be harmful can be summarized. First, the ripples should contain micro cycles, i.e., the charge throughput must be increased. Otherwise, as long as a sufficient cooling is provided, the ripples have no impact on the aging. Second, the micro cycles must have a frequency lower than 10 Hz and contribute a large amount of charge throughput, so that the extra charge throughput caused by the micro cycles can effectively cause extra degradations.

By checking the two preconditions, it can be generally confirmed if the current ripples in a certain system are harmful to batteries. Therefore, to generalize the conclusion regarding the CHB in this chapter, instead of restricting to the configurations of the experiment, the two preconditions are examined in the next section.

6.4.3 Generalization of the Conclusion

In the CHB, when the double AC frequency is lower than 10 Hz, the two preconditions obtained in the last section are indeed possible to be met. However, the possibility to meet the two preconditions is extremely low. The associated additional charge throughput is rather limited.

First, to make the frequency of micro cycles below 10 Hz, the AC frequency must be lower than 5 Hz. However, as this frequency corresponds to an extremely low speed (0.8 km/h for the reference vehicle), it is rarely encountered. Even in rather mild urban driving cycles, such a low speed is still invisible with a time resolution of one second.

Second, the increased charge throughput in the CHB is limited, because the power factor of the motor in BEVs is often high and only results in small micro cycles. For the reference vehicle, which uses a PSM, the power factor is almost constantly close to 1.0. In a WLTP C3 driving cycle simulation, the power factor is usually higher than 0.95, Figure 6.11. According to eq. (6.4), with such a high power factor, the charge throughput can only be increased by 0.71 % at the terminals of cells. Considering the filtering effect of batteries, the effective charge throughput caused by micro cycles is negligible.

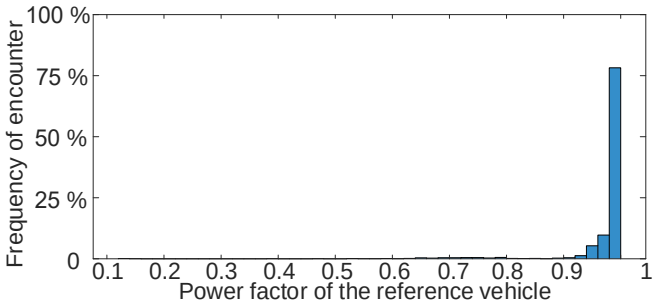


Figure 6.11: The histogram of power factor values in the reference vehicle (tested by WLTP C3 cycle)

For an ASM, the power factor is relatively lower, but still stays constantly above 0.65 in BEVs [52], [212]. The corresponding increase in the charge throughput at the terminals of cells is thus limited to 20 % in the worst case, according to eq. (6.4). Additionally, according to the results of [188], for micro cycles at 10 Hz or lower frequencies, the filter effect is still able to remove 80 %

of the additional charge throughput. Therefore, even if the ASM would be constantly operating at a power factor of 0.65 and a frequency under 5 Hz, the effective increase in the charge throughput would still be limited to 4 %, which is expected to cause an additional capacity loss below 2 % after 500 full cycles, using the aging model in [197]. Therefore, realistically, even when driving an ASM, the influence of the CHB on the battery aging is still negligible.

As a summary, although the two predictions are possible to occur in the CHB, the additional aging caused by the ripples is still expected to be negligible, due to the low possibility to encounter low frequencies and the limited effective charge throughput caused by the micro cycles. Therefore, the CHB can be concluded to be generally unharmful to lithium batteries in BEVs.

Via the experimental investigation and the discussions, this chapter resolves the concern that the CHB could accelerate the aging of the batteries. In the next chapter, the reliability of the CHB is modelled and quantitatively assessed by simulations, in order to resolve the other concern that the CHB could be unreliable due to the high number of components.

7 Reliability

Another concern regarding the CHB is its reliability. Because of the adoption of low power semiconductor switches, the CHB inevitably has a higher number of switches and driving circuits, compared to the benchmarked IGBT inverter. Moreover, due to the distributed structure, the CHB also has a large number of components for control and communications. Based on the much higher number of components in the CHB, the concern regarding its reliability naturally arises. Especially for automotive applications, where the reliability of components is crucial, the reliability of a new technology must be assessed before any practical implementation.

In this chapter, the reliability of the CHB for the reference vehicle is modelled and evaluated in a fatigue analysis. The simulation uses models developed by previous studies. The results are compared to the results of the benchmarked IGBT inverter, in order to identify if the reliability is deteriorated. However, as it is financially and physically impractical for this dissertation to verify the results of the fatigue simulation experimentally, the conclusions obtained in this chapter should be rather taken as a reference, instead of a strict quantitative prediction of the reliability.

7.1 State of the Art

In this section, the state-of-the-art studies regarding the reliability of power electronic systems are discussed. First, the overall approaches to assess the reliabilities are compared. With the overall approach selected, the studies following this approach are then summarized. It is identified that a study investigating the system reliability of the CHB or similar circuits is not yet available. Hence, a reliability model still needs to be constructed for the reliability assessment.

7.1.1 Approaches for Reliability Assessment

The previous studies on the reliability of power electronic mainly use three different approaches for the assessment [213]–[216]. The first possible approach calculates the mean time between failures (MTBF) of the system, using the failure rate values of different components in handbooks, e.g., the Military Handbook [217]. This approach is easy to understand and implement for different systems. However, as most handbooks were published decades ago, technology advancements have made the failure rates in these documents outdated. Additionally, even with up-to-date failure rate values, the approach is still not able to predict the MTBF accurately, because the influence of mission profiles on the system cannot be considered in this approach. Therefore, nowadays researchers have suggested to abandon this approach for reliability assessments [218], [219].

The second possible approach is to assess the reliability in experiments. [220]–[224] assess the lifetime of different components by testing them with practical thermal or mechanical stress profiles. To reduce the duration of the experiment, [225]–[227] develop methods to accelerate

the test. As the targeted systems or components are directly tested in the expected environments, the experimental assessment is able to accurately predict the lifetime of the system and reveal the flaws of the design. Such an experiment is also generally mandatorily required as a final step to verify the reliability of products [228], [229].

However, the time and the cost of these experiments could be rather high. To create the desired environments or stresses, the required testing equipment could be expensive, e.g., shakers and climate chambers. It is also often the case that a reliability experiment tests multiple samples of the targeted system simultaneously, in order to identify the reliability in different environments [222], [227]. Hence, multiple sets of the expensive equipment are required. In addition, even though a number of studies have proposed methods to reduce the testing duration, a reliability experiment can still easily last for months. Therefore, despite the advantages of experimental assessments, it is not feasible for the reliability assessment of this dissertation. Even for industrial projects, due to the high cost in terms of time and funding, such an experiment is also unacceptable in the early phase of the development, as a quick and rough validation of concepts is sufficient [172].

The third possible approach is the fatigue analysis, which has been widely implemented for different power electronic systems and components [230]–[232]. Similar to the first approach, this approach is based on the failure rates of components. Hence, it is simple to understand and implement. Nonetheless, as this approach calculates the failure rates based on the simulated stress profiles and fatigue models, instead of relying on fixed values in handbooks, the influence of mission profiles can be well incorporated. As the fatigue analysis is a good compromise between convenience and accuracy, this approach is the most appropriate to assess the reliability of the CHB concept.

7.1.2 Fatigue Analysis of Power Electronic Components & Systems

Fatigue analysis is not a novel approach for reliability analysis. It has been used to calculate the MTBF of different systems in previous studies. The main challenge of implementing this approach is to establish the failure rate models. Furthermore, as it is not practical to model every detail of the targeted system, the fragile components and influencing stress factors in the system should be identified first.

Specifically for power electronic systems, according to the field surveys in [233]–[235], more than 90 % of the system failures of industrial inverters can be attributed to semiconductor switches, DC-link capacitors and the solder joints on PCBs [233], and their contributions to the failures of industrial power electronic systems are visualized in Figure 7.1. The failure of the PCB means failure of the PCB solder joints. The failure of switches means the failure of bond wire joints or the failure of solder joints connecting the die and the substrate. Therefore, this section starts with a review of the reliability models of these components, to select applicable models for the reliability assessment. Then the existing models for the system reliability are also discussed.

First, the switch reliability has been extensively modelled in different studies. [230], [231] determine the reliability of IGBT modules based on the simulated profiles of the junction temperature. In a switch, the failure of the semiconductor itself is sparse to encounter, the main reason of the switch failure is the lift-off of bond wires [230]. Bond wire lift-off means the weld joint on the die fails, which is caused by the temperature swing and thermal expansion mismatch of different materials. The bond wire lift-off is also related to the operational current and voltage

of the switch. [236] develops and parametrizes a reliability model for bond wire joints in IGBT modules based on experimental data.

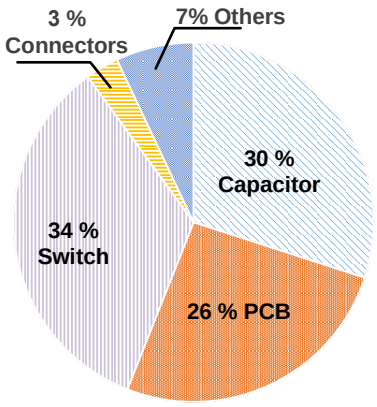


Figure 7.1: Fragile components and their contributions to failures in industrial applications [233]

In addition to the lift-off of the bond wire, the second most significant failure mechanism of switches is the failure of the die attachment [232], [237]–[240]. Die attachment is the solder joint connecting the die and the substrate. If the die attachment fails, the die will be not attached to substrate of the switch anymore. The die is thus expected to fail rapidly due to thermal run away [238]. The reliability models of the die attachment can be found in [232], [241], [242].

To better incorporate the influence of mission profiles in the model, [243]–[246] implement more detailed thermal models. The rain flow counting algorithm is also implemented to convert the simulated temperature profile into thermal stress cycles, which are the inputs of the reliability models. In this way, the cycle life of the components can be more accurately estimated. Rain flow counting is an algorithm used in fatigue analysis to count stress cycles in a stress profile obtained in experiments or simulations. The swing, mean value and the duration of each identified stress cycle are calculated by the algorithm simultaneously. A detailed introduction of the rain flow counting algorithm is provided in [247].

Besides the switches, the DC-link capacitors also significantly contribute to the system failure. Hence, the reliability models for capacitors are available as well. A capacitor reliability model is introduced in [248], taking the voltage and temperature of the capacitor into consideration. [110] further considers the influence of the humidity. [249] uses the model developed by [110] in simulations and introduced the approach to obtain the required stress factors.

The last significant factor for system failures is the failure of PCB solder joints. As most products are required by law to use the lead-free solder in the production, the reliability of PCB solder joints becomes one of the major concerns for electronic industry [250]. [250], [251] mainly model the reliability of PCB solder joints in mechanical vibrations. The developed models are validated by experimental data. [252]–[255] investigate the influence of thermal stress on the reliability of solder joints. The thermal stress is generated by altering the current flowing through the solder joints. [252]–[254] construct the models empirically based on the experimental data, while the model in [255] is obtained via a detailed analysis of the thermal expansion of different materials. Therefore, the model in [255] is more universally applicable. [256] further studied the effect of concurrent power and vibration loads. The results indicate that two concurrent factors can influence the reliability more significantly than each individual factor. A model is also constructed by [256] to describe joint effect.

In addition to the models of component reliability, the system reliability is investigated in different studies. [257] models the reliability of a DC/DC converter, considering the fatigue of switches

and capacitors in power cycles. [258] compares the reliability of different inverter designs for BEVs. However, the model used in [258] only considers the thermal reliability of the switches. Other factors are neglected. [259] evaluates the reliability of a high voltage single-phase inverter using the H-bridge circuit. The reliability of capacitors and switches is included in the model, but the reliability of PCB solder joints is not considered. [260], [261] calculate the system reliability with a broader coverage of components. However, as the calculations in [260], [261] use fixed reliability values instead of fatigue models, they are not possible to assess the system reliability in different mission profiles.

A more holistic approach is introduced in [262]. In order to obtain a well-rounded model for the system reliability, [262] pointed out the necessity to consider PCBs, capacitors and switches simultaneously. However, as [262] is a literature review, a system reliability model is not constructed. The approach to obtain the necessary inputs is also not provided. Furthermore, the reliability model for the PCB solder joints suggested by [262] only considers the vibrations. The influence of thermal stress is not included, which is also of importance. The reliability of PCB solder joints could be overestimated.

In the literature review above, it is observed that the component reliability models are available, but the studies on the system reliability are mostly biased toward switches and capacitors. The reliability of the PCB solder joints is often neglected. The existing studies on system reliability are also biased toward the influence of electrical and thermal stress factors. The influence of mechanical vibrations is often not considered at all. For stationary power electronic systems, excluding the influence of vibrations is still reasonable. For the two automotive inverters to be assessed in this chapter, the influence of mechanical vibrations could be significant.

Therefore, the existing models on the system level are not appropriate for the reliability assessment in this dissertation. To conduct a more holistic assessment for the CHB and the benchmarked IGBT, in the next section, a system reliability model is constructed based on the reliability models of different components introduced in this section.

7.2 Approach

For automotive inverters, an approach to calculate the system reliability is not directly available, but existing studies have proposed different models to calculate the reliability of each fragile point in the inverter. Based on the discussion in the previous chapter, four types of fragile points, die attachments, bond wire joints, PCB solder joints and DC-link capacitors can be identified. The corresponding stress factors are also summarized and demonstrated in Figure 7.2.

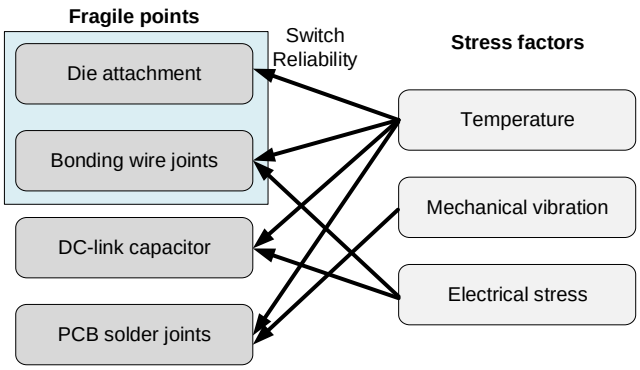


Figure 7.2: Weak points and corresponding stress factors in an automotive inverter

The reliability of the die attachment is mainly influenced by junction temperature [237]–[242]. The reliability of the bond wire joints depends on the temperature swing, the working current and the working voltage of the switch [232], [236]. The joints of bond wires are assumed not influenced by mechanical vibrations, due to its limited significance compared to the temperature swing. Moreover, as the bond wires in a switch module are emerged in the silica gel, the influence of mechanical vibrations can be damped [230]. The lifetime of DC-link capacitors is determined by the voltage stress and the temperature [110]. For automotive inverters, the humidity is not necessary to consider, because the casings of all automotive inverters are required to be moisture-resistant [263]. In the end, the stress factors for the solder joints on PCBs are the temperature swing and mechanical vibrations.

With the stress factors of each fragile point obtained, by combining the corresponding reliability models, an approach to calculate the system reliability can be obtained, Figure 7.3. The approach is mainly composed of four steps.

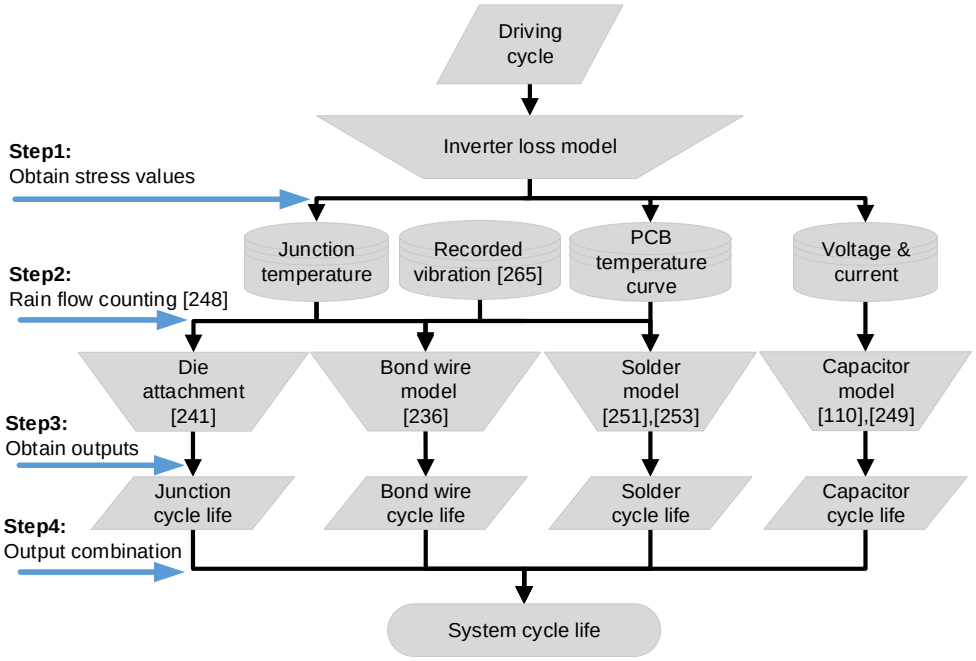


Figure 7.3: Structure of the inverter reliability model

The first step is to calculate the stress profiles required by the component reliability models. The temperature profile of the semiconductor junction can be obtained in the driving cycle simulations introduced in chapter 2 and 4. The simulation still uses the assumption that the heatsink temperature is constantly 30 °C. After obtaining the temperature profile of the junction, the temperature of the PCB solder joints is estimated using the assumed thermal resistance between the PCB and the semiconductor junctions.

For the CHB, since the aluminum base PCBs are often used for MOSFET inverters [264], the thermal resistance between the MOSFET junctions and the solder joints is assumed to be 1.5 K/W. This value is estimated by summing the thermal resistance from the MOSFET junctions to the aluminum base and the thermal resistance from the aluminum base to PCB solder joints [265]. For the IGBT inverter, the thermal resistance between the IGBT junctions and PCB solder joints is much higher, because the PCB only contacts the IGBT module via its ceramic casing. Hence, the thermal resistance between the junctions and the PCB solder joints is assumed 30 K/W for the IGBT inverter.

The thermal resistance values in this chapter only describe the thermal connectivity between the PCB solder joints and the switches. They are assumed not to dissipate any heat for the switches, and hence these thermal resistance values do not influence the junction temperature. In the simulation, the junction temperature is only determined by the total loss of the inverter and the junction to heatsink thermal resistance, which is obtained in the corresponding datasheet of the switch [49], [99], as demonstrated in Figure 2.3.

The electrical stress profiles, the AC voltage profile and the AC current profile, can also be obtained in driving cycle simulations. For the DC-link capacitor, the current and voltage profile is further converted to the ripple current profile using the approach in [249]. Then the ripple current profile can be converted to temperature profile of the DC-link capacitor following the approach introduced in [110].

To incorporate the influence of the mechanical stress on the reliability of PCB solder joints, the worst-case value recorded in [266] is used. That is because the driving cycle simulations in this dissertation are not capable of generating mechanical stress profiles.

After obtaining all the stress profiles, in the second step, the temperature profile and the electrical stress profiles are converted to stress cycles by applying the rain flow counting algorithm [247]. In this way, the influence of the stress profiles can be accurately incorporated by the fatigue models of the fragile points.

In the third step, using the inputs generated by the previous step, the reliability models are used to calculate the failure rate of different fragile points. The model in [241] is used to calculate the cycle life of one die attachment, N_{fDie}, in the IGBT inverter and the CHB, eq. (7.1). ΔT_{J} is the swing of the temperature junction in a thermal cycle. T_{Mean} is the average temperature of the junction in the thermal cycle. The thermal cycles are obtained by the rain flow counting algorithm in the previous step. A_1, A_2 and α are coefficients provided in [241].

$$N_{\mathrm{fDie}} = A_1 \Delta T_{\mathrm{J}}^{\alpha} e^{A_2/T_{\mathrm{Mean}}} \tag{7.1}$$

For the bond wire joints in the IGBTs and MOSFETs, the empirical model developed by [236] is selected, eq. (7.2). The model is obtained via a large number of experiments, but it can also take the stress cycles as inputs. Therefore, this empirical model is selected to estimate the reliability of automotive inverters. In eq. (7.2), t_{on} is the on time of the switch. D_{Bond} is the diameter of the bond wire. I_{Bond} is the current per bond wire. V is the voltage rating of the switch. K is a constant value provided in [236].

$$N_{\mathrm{fBond}} = K \Delta T_{\mathrm{J}}^{-4.416} e^{1285/T_{\mathrm{Mean}}} t_{\mathrm{on}}^{-0.463} I_{\mathrm{Bond}}^{-0.716} V^{-0.761} D_{\mathrm{Bond}}^{-0.5} \tag{7.2}$$

The cycle life of one PCB solder joint can be influenced by thermal stress and mechanical stress. In a certain thermal cycle, for the thermal cycle life of the PCB solder joint, N_{fTSolder}, the model in [253] is used, eq. (7.3). α_{Copper} and α_{Solder} are the coefficients of thermal expansion (CTE) of the two materials connected by the solder joint, copper and solder. Together with the maximum and the minimum temperatures of the thermal cycle, $T_{\max}$ and $T_{\min}$, the ratio of mismatch, $\Delta\gamma$, at one joint can be calculated. l is the length of the solder joint, and h is the height of the joint [253]. After $\Delta\gamma$ is obtained, based on the mean temperature and the frequency of the thermal cycle, T_{mean} and f_{cycle}, N_{fTsolder} can be calculated. The constant coefficients in eq. (7.3) are also obtained in [253]. The model in eq. (7.3) is an empirical model and its constant values could be a bit outdated. However, as the model manifests the fact that the failure is triggered by the mismatch of thermal expansions, it is still selected for the reliability simulation.

$$\begin{cases} \Delta\gamma = \dfrac{l}{\sqrt{2}h}(\alpha_{\text{Copper}} - \alpha_{\text{Solder}})(T_{\max} - T_{\min}); \\ c = -0.442 - 0.0006T_{\text{Mean}} + 0.174log(1 + f_{\text{cycle}}) \\ N_{\text{fTSolder}} = 0.5(\Delta\gamma / 7)^{(\frac{1}{c})} \end{cases} \tag{7.3}$$

The cycle life of one PCB solder joint under mechanical stress, N_{fMSolder}, is calculated using the model in [251], eq. (7.4). Using the worst-case acceleration of the vibration, $a_{\text{Vibration}}$, provided in [266], and the natural resonance frequency of the PCB board, f_{nPCB}, the deformation of the board, D_{PCB}, can be calculated. With D_{PCB} obtained, using the logarithmic linear model developed by [266], eq. (7.4), N_{fMSolder} can be obtained.

$$\begin{cases} D_{\text{PCB}} = \dfrac{a_{\text{Vibration}}}{4\pi^2 f_{\text{nPCB}}} \\ N_{\text{fMSolder}} = e^{\frac{0.812 - D}{0.0215}} \end{cases} \tag{7.4}$$

The reliability of the DC-link capacitor is calculated by the model in [110], which has been verified and used in different studies, eq. (7.5). t_{nominal}, T_{n} and V_{n} are respectively the nominal lifetime, nominal temperature and nominal voltage of the capacitor. T_{test} and V_{test} are the temperature and the voltage seen by the capacitor in the reliability test. α_{T} and α_{V} are two constants provided in [110]. With these values, the lifetime of the capacitor, t_{fC} can be calculated by eq. (7.5). Furthermore, using the duration of the driving cycle, t_{cycle}, t_{fC} can also be converted to cycle life, N_{fC}, with regard to the driving cycle. This model is only used for the IGBT inverter, because the CHB does not require a DC-link capacitor.

$$\begin{cases} t_{\text{fC}} = t_{\text{nominal}} e^{-\alpha_{\text{T}}(1/T_{\text{test}} - 1/T_{\text{n}})} e^{-\alpha_{\text{V}}(V_{\text{test}} - V_{\text{n}})/V_{\text{n}}} \\ N_{\text{fC}} = t_{\text{fC}} / t_{\text{cycle}} \end{cases} \tag{7.5}$$

The last step of the approach is to calculate the cycle life of the whole inverter system. As it is often assumed that the failure of the fragile points follows the Poisson process, the cycle life of the whole inverter system, N_{finv}, can be calculated by eq. (7.6). The cycle life values of different fragile points are combined to form the cycle life of the inverter system, according to the number of each fragile points. n_{Die}, n_{Bond}. n_{Solder} and n_{C} are respectively the number of dies, the number of bond wire joints, the number of PCB joints and the number of capacitors. Multiplying N_{finv} with the distance of the driving cycle, the mileage life of the inverter can be obtained as well. All the necessary parameters of the formulas discussed above are provided in Appendix D.

$$N_{\text{finv}} = \frac{1}{n_{\text{Die}} / N_{\text{fDie}} + n_{\text{Bond}} / N_{\text{fBond}} + n_{\text{Solder}}(1 / N_{\text{fTSolder}} + 1 / N_{\text{fMSolder}}) + n_{\text{C}} / N_{\text{fC}}} \tag{7.6}$$

Before introducing the results, several assumptions implied in the model should be noted. First, due to availability reasons, the parameters used by the models are mostly obtained from studies focusing on industrial applications. Hence, the parameters manifest the performance of industrial grade components, instead of automotive grade components with a higher reliability. The cycle life of the system could be underestimated for the CHB that uses automotive grade components. Second, the ambient temperature of the simulation is set constantly 30 °C, which could be mild compared to realistic environments a BEV could encounter. This assumption tends to overestimate the reliability of the inverters.

The failure predicted by the model is defined by the situation when any fragile point fails, regardless if the failed point causes a system breakdown. This definition of failure is implied when combining the expected cycle life of all fragile points in eq. (7.6). Additionally, due to the adoption of multiple empirical models and assumptions, the results generated by the model might not be an accurate estimation of the reliability of the two inverters. Nonetheless, by comparing the results of the two inverters, it is sufficient to identify if the reliability of the CHB is significantly lower than that of the IGBT inverter.

7.3 Results

The three comprehensive driving cycles, i.e., FTP72, NEDC and WLTP C3, are used for the reliability simulations, in order to compare the reliability of the CHB and the benchmarked IGBT. The obtained values of the mileage life of the two inverters are illustrated in Figure 7.4.

First, in all the comprehensive driving cycles, the mileage life of the CHB is longer than that of the benchmarked IGBT inverter. However, the mileage life values of the two inverters are in the same order of magnitude. For a reliability assessment based on fatigue analysis, such a difference is not significant enough to make a concrete judgment which design is more reliable, because empirical formulas are used in the model.

Second, according to the simulation results, both inverters have a mileage life in the level of million kilometers in all three driving cycles. Such a mileage life is much higher than the mileage life of the mechanic components in other subsystems, e.g., HVAC system, transmission etc. According to the data collected by [267], the mileage per replacement of these components is around 100,000 to 150,000 kilometers. Hence, in general the inverter does not form a bottleneck for the reliability of BEVs. Even if the CHB would have a slightly shorter mileage life, the reliability of the BEV or powertrain system would not be deteriorated. Therefore, the simulation results resolve the concern regarding the reliability of the CHB.

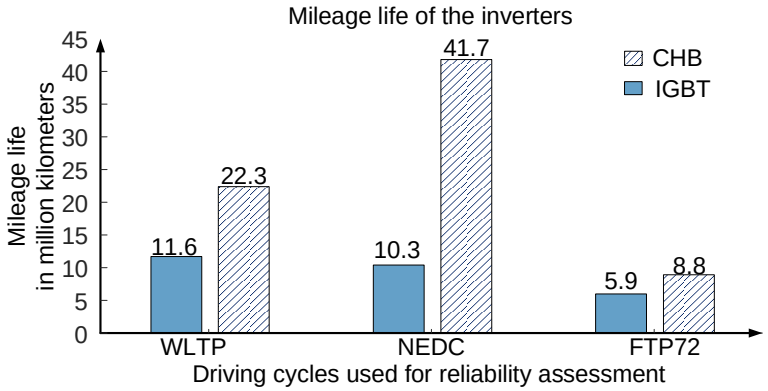


Figure 7.4: Mileage life of the two inverters in different synthetic driving cycles

Comparing the mileage life values across different driving cycles, another observation is that the driving cycle has a significant influence on the predicted mileage life. For both inverters, the mileage life values in FTP72 cycle are significantly lower. Additionally, for the CHB inverter, the mileage life in NEDC cycle is much higher. The decrease in mileage life observed in the FTP72 cycle is explained by the temperature curves. Figure 7.5 compares the junction temperature curves of the IGBT in different driving cycles. Compared to the other two driving cycles, because FTP72 cycle contains more starts and stops in the same distance, large temperature swings are

observed more often. As a result, all the fragile points influenced by the temperature swings have a lower cycle life, which eventually causes a shorter mileage life for the inverter.

The shorter mileage life of the CHB in FTP72 cycle can be explained similarly, because the temperature curves of the CHB in different driving cycles have the same difference, as shown in Figure 7.6. Since the CHB has a much higher efficiency in the partial load area, the maximum junction temperature of the MOSFETs in the CHB is significantly lower. However, a higher number of large temperature swings cycle can still be clearly seen in FTP27 cycle.

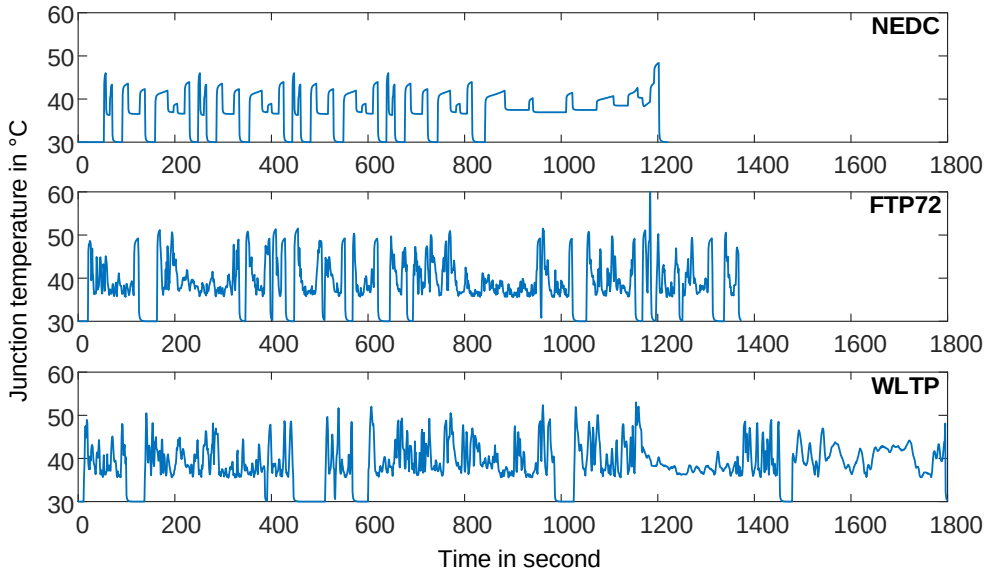


Figure 7.5: Junction temperature curves of the IGBT

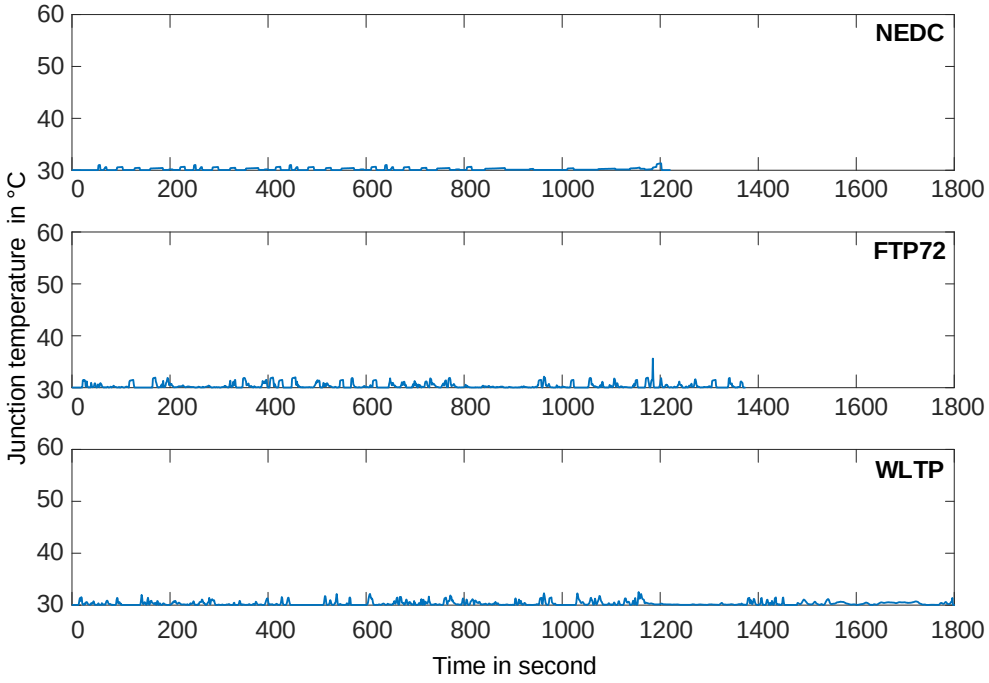


Figure 7.6: Junction temperature curves of the MOSFETs in the CHB

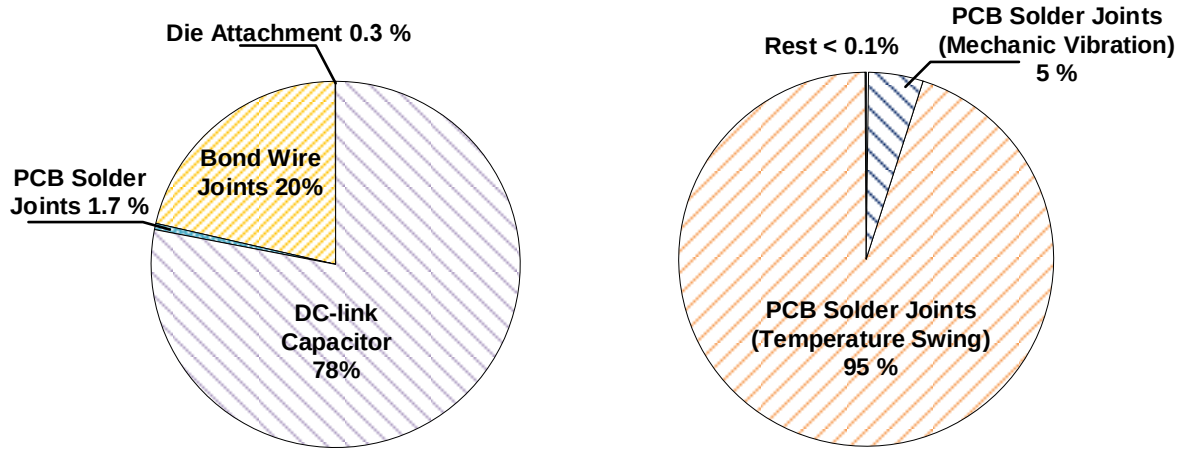
The much longer mileage life of the CHB in NEDC cycle can be explained by the driving behavior as well. Compared to the other two driving cycles, the NEDC cycle has a more smooth speed curve. Therefore, the NEDC cycle results in a smooth temperature curve, while the temperature

curves of the other two driving cycles have a large amount of ripples. In the fatigue analysis, these ripples are deemed as temperature swings. Although the amplitude of these swings is low, due to their large amount, the influence is significant. As the NEDC cycle does not trigger these small swings, the corresponding mileage life is naturally much higher.

However, for the IGBT inverter, a longer mileage life is not observed in the NEDC cycle. That is because the mileage life of the IGBT is bottlenecked by the life of the DC-link capacitor. The influence of the switch temperature is not visible anymore. Moreover, as the NEDC cycle triggers higher current ripples on the DC-link capacitor due to its lower speed [268], the DC-link capacitor is expected to have a higher temperature and thus a shorter mileage life. Therefore, compared to WLTP C3 cycle, the IGBT inverter even turns out to have a shorter mileage life in the NEDC cycle.

To make the explanations above clearer, the contributions of each failure mechanism in both inverters are illustrated in the pie charts in Figure 7.7, when the inverters are tested by WLTP C3 cycle. For the failure of the PCB solder joints in the CHB, the contributions of mechanical vibrations and temperature swings are differentiated. For the IGBT inverter, the DC-link capacitor is the dominating failure mechanism in WLTP C3 cycle, while the influence of temperature explains only about 20 % of the failure. The DC-link capacitor forms the bottleneck of the reliability. Therefore, when shifting to NEDC cycle, the deterioration of the capacitor reliability overrides the reliability improvements caused by less temperature swings. The distribution is significantly different from that of industrial inverters in Figure 7.1, which could be explained by the difference in application scenarios and the possible errors in the fatigue analysis models.

For the CHB, the dominant failure mechanism is the thermal failure of PCB solder joints. When the test cycle shifts from WLTP C3 to NEDC, the mileage life increases, due to the reduced temperature swings.



(a) Benchmarked IGBT inverter (b) CHB

Figure 7.7: The contribution of each failure mechanism in the two inverters

In addition to the assessment with common comprehensive driving cycles, the two inverter are also assessed in a maximum acceleration simulation, in order to investigate the reliability in the extreme case. The test starts with a full-pedal acceleration for 10 s. According to the datasheets [49], [99], this short period is sufficient for the junction temperature to reach steady state. Then the inverter is immediately idled for another 10 s, so that the junction temperature converges back to the ambient temperature (heatsink temperature). The convergence in 10 s is possible, because the thermal capacitance of switches is limited. The thermal time constant of the switch

is about 2 s [49]. Therefore, when the switch is actively cooled, the junction temperature is almost only determined by the total loss of the switch, with a limited time delay.

Such a test profile generates the maximum temperature swing that is possible to encounter in the reference vehicle, and thus is one of the most challenging scenarios for the reliability of switches. However, as the test only lasts 20 s, components outside the switches, e.g., PCB solder joints and the DC-link capacitor, do not experience the swing. The simulated results of the test are listed in Table 7.1. The expected cycle life is given without converting to the mileage values, because the mileage is not an appropriate metric for the reliability in extreme scenarios.

Table 7.1: Reliability of the two inverters in maximum acceleration test

Inverter Type	Temperature swing	Maximum junction temperature	Expected cycle life
IGBT	75 °C	105 °C	85,161 cycles
CHB	26 °C	56 °C	133,817 cycles

According to the results in Table 7.1, the IGBT is expected to last about 85,000 before the first fragile point fails. The cycle life of the CHB is higher, more than about 133,000 cycles. That is because the temperature swing of the MOSFETs in the CHB is much lower during the maximum acceleration test, due to the higher efficiency of the CHB. Nonetheless, as the cycle life values of the two inverters are still in the same order of magnitude, it cannot be concretely judged if one inverter in more reliable. Moreover, the result of the IGBT in Table 7.1 roughly matches the power cycling test result of state-of-the-art automotive inverters [269]. According to [269], with a temperature swing of 75 °C, a state-of-the-art automotive inverter is supposed to survive around 100,000 temperature cycles before breakdown. Hence, the result of the IGBT inverter generated by the reliability model is reasonable. Other results generated by the model are thus expected to be in a reasonable range as well.

Based on the simulation results and the analysis, it is observed that the reliability of the CHB is not a problem, although the CHB has more components. The reliability of the CHB is in fact similar to that of the IGBT inverter. In the next section, the results are further explained and discussed.

7.4 Discussion

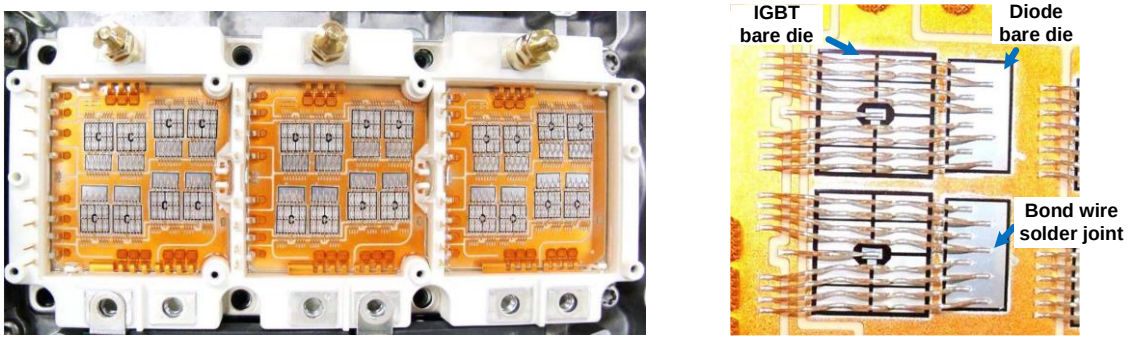
This section first aims to explain why the expected lower reliability of the CHB is not observed. Then mileage until breakdown of the two inverters is discussed based on the results in the previous section. The fault tolerance operation of the CHB is also briefly introduced.

7.4.1 Explanation of the Results

Although the CHB has more components, especially more switches in the system, its reliability is in the same order of magnitude as an IGBT inverter. The similarity of the reliability can be explained in two aspects. First, because of the high efficiency, the thermal stress of the MOSFETs in the CHB is much lower than that of the IGBT. That is obvious by comparing the junction temperature curves in Figure 7.5 and the curves in Figure 7.6.

Second, the six-pack IGBT module of the benchmarked inverter is also composed of multiple smaller switches. Opening up the module, Figure 7.8(a), 24 IGBT dies and 24 diode dies can be found [37]. Compared to the 216 MOSFET dies used in the CHB, 48 is not a significantly lower value to change the reliability fundamentally. The difference in the number of bond wire joints is even smaller. In the CHB, there are five bond wire joints per MOSFET [270], and in total 1080 joints. In the IGBT module, only counting the joints on the dies, excluding those connected to copper bars (due to weak thermal connectivity to the dies), there are 17 joints on each die of IGBT and 8 joints on each die of diode, according to Figure 7.8(b). In total, the IGBT module has 600 bond wire joints on the dies. The number of fragile points in the IGBT module is not significantly lower than that in the MOSFETs of the CHB. The IGBT module is only much more integrated.

Moreover, due to the reduced stress, the dominating failure mechanism of the CHB is actually not the failures inside MOSFETs. The contribution of switch related failures is negligible, according to the percentage contribution of each failure mechanism illustrated in Figure 7.7. The dominating driving factor for the failure of the CHB is the failure of PCB solder joints. That phenomenon is caused by two reasons. First, the CHB is assumed to have a much higher number of PCB solder joints. In the simulation, the CHB is estimated to have 500 solder joints on each PCB, and 4500 solder joints in total in the system. This estimation includes solder joints of switches, drivers, controllers, small passive components and redundant joints etc. Second, all the PCB solder joints are assumed closely coupled to the junctions of the MOSFETs, via a thermal resistance of 1.5 K/W. As a result, all the PCB solder joints are exposed to the temperature swings of the semiconductors. The two factors together make the failure of PCB solder joints the most dominating reason for the system failure of the CHB.



(a) the overview of the opened-up IGBT module (b) the detailed structure of one switch

Figure 7.8: The internal structure of the IGBT module used for the reference vehicle [37]

7.4.2 Realistic Mileage Life of the Two Inverters

In the previous sections, comparisons are conducted based on the mileage until one fragile point fails, regardless if the failure of this point could cause a breakdown of the inverter or not. Therefore, based on the results obtained in previous sections, the realistic mileage life of the two inverters is discussed. The realistic mileage life means the mileage an inverter can operate continuously without compromising its functionality. The value of the realistic mileage life could manifest the reliability from the perspective of the users.

For the CHB, the failure predicted by the model does not certainly lead to a fatal error of the system, because the predicted failure is most probably the failure of a PCB solder joint, and many solder joints on the PCB have no significant influence on the operation of the system.

These solder joints include the solder joints of redundant decoupling capacitors, redundant connectors, and unused pins of ICs. Therefore, the realistic mileage life of the CHB should be longer than the prediction generated by the model.

In contrast, the main failure mechanisms of the IGBT inverter are the failure of DC-link capacitor and the failure of bond wire joints, Figure 7.7. These failures usually lead to the breakdown of the inverter. If a bond wire joint fails, the current rating of the switch will be reduced. In this case, once a high current is demanded, the still functional joints will also fail due to overcurrent. For IGBT modules with multiple dies in parallel, the failure of a bond wire joint is possible to cause current imbalance and eventually break the switch due to thermal runaway [271]. If the DC-link capacitor fails, regardless if it enters open circuit or short circuit state, the inverter cannot operate normally anymore. Hence, the realistic mileage life of the benchmarked IGBT inverter should be consistent with the value predicted by the model.

In addition to the failure mechanism, the predicted mileage life of the CHB is also significantly influenced by the assumption that all the PCB solder joints are thermally coupled to MOSFET junctions, with a thermal resistance of 1.5 K/W. This assumption is only a worst-case assumption. On the one hand, in a realistic scenario, not every solder joint on a PCB board can be so closely coupled to the MOSFET junctions. On the other hand, there are different approaches to make most of the PCB solder joints thermally isolated from the MOSFETs and significantly improve the reliability. The approaches will be introduced in the next chapter. Therefore, the reliability of the CHB tends to be underestimated in the simulations of this chapter.

Combining the discussions regarding the failure mechanism and the assumptions, the realistic mileage life of the CHB is expected to be longer than the predicted value, while the realistic mileage life of the IGBT inverter should be consistent with the prediction. Therefore, the CHB is further confirmed not to have any disadvantages in terms of reliability. Realistically, the CHB is even more reliable than the IGBT inverter.

Moreover, the CHB and other multilevel inverters also have the capability to operate continuously, even if one or several submodules completely break down. Such a fault-tolerance operation can be realized by bypassing the fault modules with the switches [124], [272]–[276]. In this case, the maximum power of the CHB is reduced [124], but the vehicle is still drivable. When one module in the CHB breaks down, the BEV does not necessarily require an immediate repair. The expected available time (availability) of the BEV using the CHB is much longer than that using the IGBT inverter.

According to an estimation in [124], a multilevel inverter is supposed to have the same availability as the IGBT inverter, if the two inverters should provide at least 93 % of their maximum power. If the power requirement is reduced to 90 % of the maximum power, the availability of the multilevel inverter will become more than ten times higher than that of the IGBT inverter [124]. Therefore, considering the continuous operation at a lower power, the CHB tends to be significantly more reliable than the benchmarked IGBT inverter. Different control algorithms to conduct fault-tolerance operations are extensively explained in [124], [272]–[276]. Hence, the details of the algorithms will not be discussed in this section.

To summarize this chapter, the simulations prove that reliability of the CHB and the benchmarked IGBT inverter is in the same level. The reliability of the CHB concept is generally not a problem, although a higher number of components are used. The reliability of inverters generally does not form a bottleneck for the reliability of BEVs. Due to the assumptions and the failure mechanisms of the two inverters, the realistic mileage until breakdown of the CHB could be even higher than that of the IGBT inverter. Furthermore, because of the fault-tolerance capability of the CHB, in

comparison to the benchmarked IGBT inverter, the CHB is expected to result in a longer available time in practical implementations. Therefore, even considering reliability, the CHB concept is still a preferable concept for BEVs.

After resolving the concerns over the CHB concept, the next chapter discusses several aspects that are not covered by dedicated investigations. Some guidelines for practical implementations are provided. In the end, the limitations of the concept and the overall research of the dissertation are also discussed.

8 Discussion and Outlook

In the previous four chapters, the proposed CHB concept is investigated in terms of efficiency, cost, battery aging and reliability. The assessments of efficiency and cost confirm that the targets of design are successfully met. The latter two chapters resolve the two concerns regarding the CHB concept. Hence, the CHB concept is proven to be a generally appropriate concept to improve the performance of electric powertrains.

However, as the CHB concept is proposed for BEVs, its weight, volume and EMI should also be discussed. On the system level, due to the structural change, there are also several challenges associated with the CHB concept. Therefore, this chapter first covers these considerations via a discussion. Then based on results and discussions in previous chapters, the most appropriate vehicle concepts to implement the CHB are identified.

In addition to the conceptual discussions, this chapter also introduces the technical guidelines to realize the predicted improvements in practical implementations. The guidelines are summarized based on the prototyping experience and the analysis in the previous chapters. In the end, the limit and the outlook of the research are discussed. Further possible improvements of the CHB concept are enumerated as possible topics for future studies.

8.1 Additional Considerations

For automotive applications, besides the four investigations, there are still several additional aspects to be considered. First, on the component level, the weight, volume and EMI are also important criteria. Second, due to the elimination of the DC link, the challenges associated with the CHB concept are also discussed.

8.1.1 Weight, Volume and EMI of the CHB Concept

First, compared to IGBT inverters using six-pack topology, the CHB inevitably has a higher weight, as more components are used. However, as the additional components are limited to ICs, switches or driving circuits, the added weight is limited within several kilograms. Besides, since the CHB reduces the required battery capacity, the reduced weight of the batteries could counterbalance the increased weight of the inverter. Therefore, the CHB is not expected to increase the weight of BEV. For BEVs with a longer nominal range, as the weight reduction of batteries is more significant, the CHB can even help to reduce the curb weight of the vehicle.

Second, the CHB may bring challenges to the volume of the battery pack. Since the CHB is electrically connected to batteries, to avoid a complicated wiring process, the optimal method is to integrate the H-Bridges horizontally within the battery modules. However, via an optimized packaging and board design, the volume of the battery pack does not necessarily increase after

the integration of the CHB. Even in the worst case, only the height of the battery pack casing is expected to increase by 1-2 cm, due to the integration of the CHB.

As most high power MOSFETs have a planar package, the height of the H-bridge modules can be restricted within 1-2 cm, determined by the height of the connectors, which is usually the tallest component on a MOSFET board. Such a height is close to the height of a slave BMS board. Therefore, by optimizing the size and the shape of the H-bridge modules, or even integrating the slave BMS boards into the H-bridge modules, the modules can be inserted into the packaging space reserved for the slave BMS boards, which is necessary as well for the conventional powertrain architecture. Such an optimization of the H-bridge module is often feasible, due to the limited maximum power and the limited heat dissipation of a single module. In this case, the CHB does not change the size of the battery pack casing at all, and hence has no influence on the vehicle packaging. Moreover, due to the integration, the packaging space reserved for the IGBT inverter is made available. The packaging of the vehicle could be even simplified.

Nonetheless, the situation in the previous chapter may not be always feasible. In the worst case, when the optimally designed H-bridge modules still cannot fit in the packaging space of slave BMS boards, the alternative solution is to attach the H-bridge modules horizontally on top of the battery modules. The height of the battery pack casing will be increased by 1-2 cm. Because battery packs are often installed either under the floor/seats for passenger vehicle [277] or on the roof for buses [278, p. 21], and considering the saved space originally occupied by the IGBT inverter, such an increase in height is not expected to significantly influence the packaging design, the weight or the air resistance coefficient of the vehicle. Therefore, even in the worst case, following the planar design approach, the CHB is still not expected to cause a significantly problem in terms of packaging.

Third, the EMI level is also an important criterion to evaluate inverters. To estimate the EMI of an inverter, a straightforward approach is to calculate the speed of voltage shifting during the turn-on or turn-off transient of the switch, usually marked as $\mathrm{d}v/\mathrm{d}t$ [90], for which the duration of the switching transient and the DC voltage blocked by the switches are necessary.

The switching transient time of an IGBT, $t_{\mathrm{trans\_IGBT}}$, is usually around 5 times that of a MOSFET in the CHB, $t_{\mathrm{trans\_CHB}}$, [79, p. 12]. However, in a CHB, the DC voltage switched by the MOSFETs is much lower. For a CHB with *N* modules per phase and an IGBT inverter with the same voltage output capability, the voltage blocked by MOSFETs, $u_{\mathrm{DC\_CHB}}$ is only 1/2*N* of the voltage blocked by the IGBT, $u_{\mathrm{DC\_IGBT}}$. Hence, the $\mathrm{d}v/\mathrm{d}t$ of the CHB and that of the IGBT have a relationship in eq. (8.1). When *N*≥3, the case in most studies [116], [125]–[130], the $\mathrm{d}v/\mathrm{d}t$ of the CHB is lower. Therefore, the CHB concept is expected not to have severe problems in terms of EMI.

$$\frac{(dv/dt)_{\mathrm{CHB}}}{(dv/dt)_{\mathrm{IGBT}}} = \frac{u_{\mathrm{DC\_CHB}}}{u_{\mathrm{DC\_IGBT}}} \cdot \frac{t_{\mathrm{trans\_IGBT}}}{t_{\mathrm{trans\_CHB}}} = \frac{5}{2N} \tag{8.1}$$

Based on the discussions above, it observed that the CHB concept does not have significant problems in terms of weight, volume or EMI. Therefore, the CHB remains a valid concept, even when broadening the aspects of considerations.

8.1.2 Challenges on System

The previous section further proves that the CHB concept does not have problems on the component level. However, it does not indicate that the CHB concept is perfect. In fact, the main

challenge associated with the CHB is the influence on the overall system design. In this section, the two problems introduced by the CHB concept, i.e., the power supply for auxiliaries and the compatibility with multiple motors, are discussed. However, due to their solvability, the two problems do not affect the plausibility of the CHB concept. They are only deemed as challenges associated with the concept.

Auxiliaries Power Supply

The first challenge associated with the CHB is the power supply of the auxiliaries, which is usually a low DC voltage (e.g., 12 V or 24 V) required by the auxiliary loads in BEVs. In a conventional electric powertrain structure, the power of auxiliaries is supplied by a DC/DC converter, which converts the varying high voltage of the DC link to a stable low voltage. However, for the CHB, due to the elimination of the high voltage DC link, the conventional solution is not feasible anymore. In this case, to generate the low voltage for the auxiliaries, a straightforward solution is to integrate a small DC/DC converter in each H-bridge module. The converters are then paralleled, so that enough power is provided to supply the auxiliary load.

Another possible solution is to equip only one or several modules with a DC/DC converter, in order to reduce the total number of converters. This solution is also proposed by [279]. Such a solution could have a lower cost. However, it also causes the imbalance of the load distributions among different submodules, which brings additional challenges to the SOC balancing. The SOC balancing algorithms are shortly introduced in section 3.2.2, but it is still necessary to verify if the balancing capability of the standard algorithms is sufficient to correct the unevenly distributed auxiliary load.

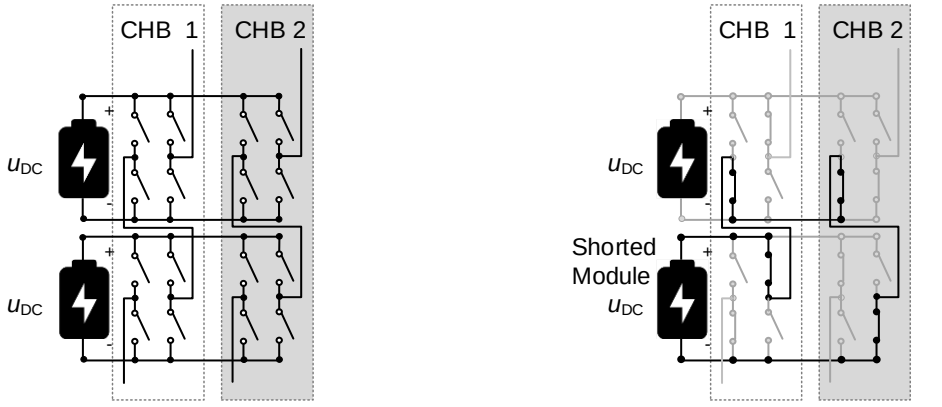
For the CHB concept, the power of auxiliaries can be supplied by different approaches. The two possible approaches discussed above are only two examples. To come up with the optimal solution for a certain scenario, dedicated investigations are still necessary. Limited by the scope of research, these investigations are not conducted in this dissertation.

Multi-Motor Compatibility

Another problem of the CHB concept is its compatibility with the powertrains with multiple motors. In order to achieve high performance and further improve the motor efficiency, high-end BEVs are often equipped with two [280]–[282] or even more motors [283], [284]. In the conventional powertrain system, the high voltage DC link serves as a central power supply, so that multiple inverters can be connected to control multiple motors. In contrast, in the CHB, as the inverter and the batteries are integrated, the central power supply does not exist anymore. Driving multiple motors becomes a more difficult task.

A possible solution is to install multiple sets of isolated CHB systems in the vehicles, and each CHB system is powered by an individual set of batteries. In this case, every motor can be controlled by an individual CHB. However, it is challenging to charge or balance the batteries in several sets of batteries. As the number of motor further increases, the challenge of having multiple sets of batteries becomes even more severe. Therefore, this solution is generally not appropriate.

A possible alternative is demonstrated in Figure 8.1(a). Instead of adding another set of batteries into the vehicle, this solution connects two or more H-bridges to a single battery module, and then cascade the H-bridges to form multiple sets of CHBs using one set of batteries. Following this approach, the multiple CHB systems can be powered by the same batteries, Figure 8.1(a). Then each CHB can be used to control one motor.



(a) one battery module with two H-bridges (b) a short circuit status

Figure 8.1: A possible solution to control multiple motors with the CHB concept

However, in this case, for the second set of H-bridges, the power supplies of the modules are not isolated anymore, because the first set already establishes certain electrical connections among the batteries. Therefore, the control strategy and the PWM algorithms of the two CHBs should be carefully designed and well synchronized. Otherwise, it is possible to short the battery modules in certain switch statuses.

One example is demonstrated in Figure 8.1(b). The two CHB systems are seemingly normal individually. The CHB1 is generating $2u_{\mathrm{DC}}$ as the output, while the CHB2 is supplying $-u_{\mathrm{DC}}$ to the load. However, in this case, a route to short circuit the lower battery module is created between the two systems, as highlighted in Figure 8.1(b). Therefore, to implement this solution to drive a BEV with multiple motors, the appropriate PWM algorithms should be specifically investigated.

As a summary, it is possible to make the proposed CHB concept compatible with multi-motor powertrain architectures. However, the control algorithms to control multiple motors still requires further research.

8.2 Most Appropriate Scenarios for the CHB

Based on the results in previous chapters and the additional considerations, it is observed that the CHB concept is generally more preferable than a conventional IGBT inverter for different vehicle concepts. Nonetheless, in several scenarios, the advantages of the CHB can be maximized. To identify the most appropriate scenarios to implement the CHB concept, the features making the CHB concept more competitive are summarized first. Then the most appropriate scenarios for the CHB are identified accordingly.

First, to fully utilize the high efficiency of the CHB, vehicle concepts should be more toward urban driving scenarios. That is because the efficiency improvement of the concept is more significant in the partial load area, according to the efficiency analysis in chapter 4. The corresponding cost reduction effect is also more significant.

Second, according to the cost assessment in chapter 5, to maximize the cost reduction effect of the CHB, the rated capacity of the battery pack should be high enough. A high capacity of the battery pack is a result of either a high nominal range, or a high weight of the vehicle (leading to

a high consumption). Hence, in terms of the cost reduction, the CHB concept should be implemented in BEVs with a long range or high weight.

The results in chapter 6 do not provide suggestions for vehicle concept selection. The results of the reliability assessment in chapter 7 indicate that the CHB has a longer mileage until breakdown. The CHB also has the possibility to conduct fault-tolerance operations by limiting the maximum power. Therefore, if BEVs are required to be continuously available, regardless of the driving performance, the CHB is also more preferable.

In the end, the main challenge associated with the CHB concept is the difficulty to control multiple motors. The CHB concept is more straightforward to implement in vehicle concepts that use one or two motors in the powertrain system. Therefore, for BEVs pursuing extreme driving performance by equipping more than two motors, the CHB concept is not recommended. The CHB concept is more suitable when the high driving performance is not a crucial factor.

Summarizing the features discussed above, the most appropriate scenarios for the CHB concept can be obtained. Several examples are enumerated below.

First, urban electric buses and electric taxis are appropriate to implement the CHB concept, because the two types of vehicles exclusively drive in urban scenarios, where the cost reduction effect of the CHB is more significant. As the two types of vehicles are used in cost-sensitive scenarios, the cost reduction effect of the CHB is also more beneficial. Furthermore, as the two types of vehicles are used for public services, the fault-tolerance capability of the CHB can significantly improve the service quality. The disadvantage of the CHB can be avoided, because an extreme driving performance is not the key requirement of these vehicles, and one or two electric motors are usually sufficient to drive the vehicle. Nonetheless, as these two scenarios do not necessarily need dedicated inverter design, they may not be an ideal market entrance for the CHB concept.

Second, for entry-level personal BEVs, e.g., the reference vehicle, the CHB concept is also preferred. On the one hand, the entry-level BEVs are cost-sensitive. The cost reduction effect of the CHB is rather important for these vehicles. On the other hand, such a BEV also does not require an extreme acceleration, so that the CHB only needs to drive one motor. The challenge of multi-motor compatibility does not exist. Additionally, due to potentially large market size, entry-level personal BEV might be an ideal scenario for the CHB to enter the market.

It is worth noting that the CHB concept is generally more advanced than the conventional IGBT inverter, as proven in the previous chapters. The examples in this section only indicate several scenarios where the benefits of the CHB concept can be maximized. The feasibility of the CHB concept is not restricted within the scenarios enumerated above. An example is that the CHB can also be used in high-performance vehicles for efficiency improvement, but the performance is not achieved by increasing the number of motors. To reach a high driving performance with the CHB concept, a more feasible approach is to use motors with higher voltage. That is because the CHB can easily reach higher voltage by cascading more modules. In addition, different from six-pack inverters, the partial load efficiency of the CHB does not decrease with the increasing system voltage, as its switching loss is only related to the module voltage. Hence, even for a high voltage CHB, the efficiency is still expected to be much higher than that of a 400 V IGBT inverter. As a result, the CHB can also be used in sporty BEVs to improve the efficiency.

8.3 Guidelines for Practical Implementations

In the previous discussions, it is observed that the CHB is capable of reducing the system cost in a number of scenarios, due to its improved efficiency. To realize the predicted efficiency improvement and cost reduction, this section provides the technical guidelines for the practical implementations of the CHB. The guidelines are obtained from the experience of constructing a functional prototype. The prototype is built to demonstrate the functions and the advantages of the CHB, when the CHB is implemented in an electric bus concept. The electric bus concept is designed for the future public transport system in Singapore [285].

Different from the switch selection introduced in chapter 3, the prototype of the CHB uses five IPT015N10N5 (maximum current 300 A [286]) MOSFETs in parallel at each switch position. With forced-air cooling, the prototype can handle a maximum current of 500 A and provide ±150 V AC voltage output, which is sufficient to drive a minibus. However, as the battery modules in the prototype are recycled from another project and significantly aged, the maximum charge and discharge current of the modules is limited to 15 A, less than 0.3 C for the 48 Ah battery modules. Therefore, for the safety, the CHB prototype is only tested by discharging to load resistors at a low current. Based on the considerations of the design, the problems identified in tests and the possible approaches for further improvements, the guidelines for practical implementations are obtained. The guidelines are mainly about the selection of the MOSFETs and the cooling design.

8.3.1 MOSFET Selection

When selecting a MOSFET for the CHB, the on-state resistance should not be the only criterion. The parasite capacitance should also be checked carefully [287, p. 73]. That is because the MOSFETs with an extremely low resistance tend to have a high parasitic capacitance. When the parasitic capacitance of MOSFET is high, voltage oscillations could happen during the switching-off of the MOSFET.

In the prototype, each of selected MOSFET IPT015N10N5 has an on-state resistance of 1.5 mΩ, but meanwhile a high parasitic capacitance (1800 pF according to datasheet [286]). As a result, an intense oscillation of the voltage is observed, Figure 8.2. Such a high oscillation not only forms a high EMI for other electronic components in the system (due to the much higher $\mathrm{d}v/\mathrm{d}t$), but also has the potential to break down the MOSFETs, due to the overshoot of the voltage (60 % overshoot in Figure 8.2). Therefore, snubber circuits must be used to damp the oscillations.

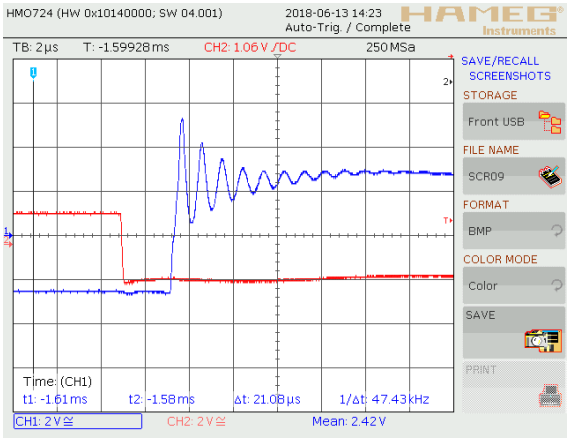


Figure 8.2: Voltage oscillation measured during the turning-off of a MOSFET

However, if the parasitic capacitance of the selected MOSFET is too high, the additional switching loss caused by the snubber circuit will significant. For the prototype, to damp the oscillations in Figure 8.2, the resistor-capacitor snubber circuits can theoretically increase the average switching loss by about 120 % in a WLTP C3 driving cycle. According to the efficiency analysis in Table 4.4, such an increase in the switching loss corresponds to an efficiency decrease of 1 %. Therefore, to realize the predicted improvement of the efficiency, besides optimizing the parasitic parameters of the circuit, it is also important to reduce the intrinsic oscillation by selecting appropriate MOSFETs for the CHB.

To reduce the total parasite capacitance of switches, sometimes it is more recommendable to parallel multiple smaller MOSFETs, instead of using a single MOSFET rated at a much higher current. That is because an extremely low on-state resistance could be associated with a rather high parasite capacitance. For example, for the prototype, by replacing the five paralleled IPT015N10N5 MOSFETs with ten paralleled IRF100B201 MOSFETs, the overall on-state resistance of the CHB is not changed, but the parasitic capacitance can be reduced by 30 % [286], [288]. Accordingly, the additional switching loss caused by the snubber circuits can also be reduced approximately by 30 % [289].

In addition, for an optimal efficiency of the CHB, the switch modules could be more preferable than the discrete MOSFETs, as the parasite parameters of the switch modules have mostly been optimized. Although the whole dissertation analyzes the CHB that is composed of discrete components, it does not form a recommendation to use discrete components in practical implementations. The purpose of using discrete components is only to simplify the modelling of the efficiency and the cost. For practical implementations, switch modules and driving circuit modules could be better choices in terms of the efficiency.

8.3.2 Cooling Design

In the cost analysis, the cost of heatsinks is included in order to demonstrate the worst-case scenario of the CHB. However, for practical implementations, the dedicated heatsinks are not certainly necessary. Since the heat generated by the Si MOSFETs is much lower than the cooling power required by the fast charging of batteries, without causing any problem, the H-bridge modules can share the heatsinks of the batteries, which is required and generally rather efficient in terms of cooling.

Moreover, as H-bridge modules using Si MOSFETs are usually built on aluminum base PCBs, the integration of the heatsinks is also generally feasible in terms of packaging. The aluminum base of the PCBs can be conveniently attached to the heatsinks of the battery modules, so that the switches are also cooled by the same heatsinks. Such a layout is also planned in the prototype, Figure 8.3 (only to demonstrate the layout, the heatsink is not yet connected to the H-bridge module in the figure). The heatsink of the battery module is horizontally installed on the battery cells. By simply attaching the H-bridge PCB horizontally on top, the heat of the MOSFETs can be dissipated via the same heatsink. The heatsink cost of the CHB can thus be eliminated.

The cooling design also has an influence on the reliability of the CHB, and thus influences the total cost of the ownership of the BEV. Therefore, the cooling design should also consider the reliability. According to the analysis in chapter 7, to improve the reliability of the CHB, the MOSFETs should be thermally decoupled from other components. Hence, in practical implementations, it is not wise to put all the components of the submodule on one aluminum base PCB, like in the prototype in Figure 8.3. Instead, it is recommendable to put the power

components (MOSFETs, drivers) on the aluminum base PCB, and the other components on a separate common PCB. According to the model in chapter 7, such a thermal isolation is expected to improve the mileage life of the CHB by factor 5-10.

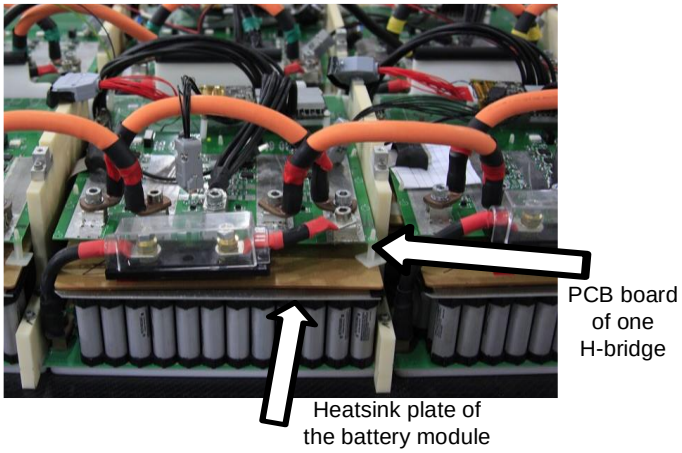


Figure 8.3: One H-bridge and its battery module in the CHB prototype

Such a thermal isolation design has already been commonly implemented in automotive products, including low voltage six-pack MOSFET inverters [290], and BMSs with MOSFET relays [264]. Even in the IGBT inverter in Figure 5.1 and in the benchmarked inverter, the control boards and the power modules are also thermally decoupled [37], [49] This approach of design not only has the potential to improve the reliability, but also slightly reduces the cost, as the material cost of aluminum base PCBs is higher.

In the end of this section, it is worth noting that the prototype in Figure 8.3 does not correctly demonstrate the height of the CHB in practical implementations. Since the fast prototyping was adopted, the modules are connected by stiff cables recycled from previous projects. The slave BMSs are also not well integrated in the modules. In practical implementation, even following the prototype layout, the height of the CHB can be restricted around 1 cm, by using customized flat bus bars and optimizing the integration of the slave BMS boards.

8.4 Limitations of the Research & Outlook

This dissertation proposed and verified the CHB concept. Nonetheless, the research still has a few restrictions. Moreover, as the scope of the research is limited to proposal and verifications of the concept, the potentials of the CHB concept are not fully exploited. These potentials will be introduced as the outlook of this research.

8.4.1 Limitations of the Research

As this dissertation mainly conducts four investigations for the CHB concept, the limitations of the research are also summarized accordingly. In each aspect, the limitations in terms of the methodology and the research scope are discussed.

Efficiency

In the efficiency assessment, all the other models are verified by full-scale experimental results, except for models of the CHB and the SiC MOSFET inverter. For the CHB, a full power prototype

is constructed, but its efficiency is not directly tested, because the battery modules of the prototype are recycled from a previous project, and are unsafe to run at high power. The efficiency model of the SiC MOSFET inverter is also only verified by ANSYS Simplorer, as it is impractical to build up a full power SiC MOSFET.

Another limitation is that only the reference vehicle is modelled. The improvements in other vehicles are not simulated. The reason is that the research of efficiency requires a high accuracy, and the motor parameters of other vehicles are not available. The detailed motor parameters of the reference vehicle is obtained, because the institute in Singapore coincidentally possesses a motor from the same series.

In the end, this dissertation does not compare the CHB with possible solutions that mix IGBTs and SiC MOSFET. A publication of the author [41] proves that mixing SiC MOSFETs and IGBTs in a single inverter is not cost effective. However, for a dual-motor BEV, using a SiC MOSFET inverter to control a small PSM, and an IGBT inverter to control a high-power ASM, a higher efficiency could be achieved at an acceptable cost. Due to the limit of the scope of the research, these solutions are not further modelled or discussed in this dissertation.

Cost

The system costs of the three inverters are estimated based on their energy consumptions and the capital costs. The capital cost is further obtained via a cost model. This model is generally better than using the large-bundle retail prices online, but the results are still rather difficult to verify. On the one hand, the OEM purchasing prices of different inverters and components are not available. On the other hand, the model still implements a few empirical factors, e.g., the manufacturing overhead, which could considerably vary case by case. Hence, the predicted cost reductions could still be inaccurate.

Regarding the scope of the research, another limitation of the cost assessment is that the cost associated with the system challenges (discussed in section 8.1.2) are not incorporated. For the reference vehicle, as only one motor is used, this is not a major problem. For vehicle concepts with multiple motors, the scope of the cost comparison needs to be broadened.

Influence on Battery Aging

First, the main limit of this part of research is that the number of the testing channels is limited to eight. The number of channels further limits the sample size of the test cells, which makes the experiment results potentially influenced by the randomness in the aging process. No more channels are constructed for the experiment, because all the test rigs are soldered and constructed in-house, which is a rather time-consuming process.

Second, the three unexpected aging curves form another limit of the research. The three curves do not change the conclusion of the research, but they are still worth further investigations. Due to the limit of the scope of research, only several possible explanations are provided in the dissertation. To determine the real reason, dedicated investigations are still necessary.

Reliability

As already mentioned in chapter 7, it is physically not feasible for this research to verify the results of reliability on the system level. The reliability model is only indirectly verified via literature research. For implementations in BEVs, a long-term test with multiple full-scale prototypes is still necessary to investigate the realistic reliability of the concept. The reliability research in this dissertation only indicates directionally that the CHB is not expected to deteriorate the reliability of BEVs.

8.4.2 Outlook for Further Improvements

As this research is limited to the proposal and verification of the concept, the potentials of the CHB concept are not fully exploited. In fact, via circuit optimization and improved control algorithms, the efficiency of the CHB could be further improved. These two topics are not covered in dissertation, but they are dedicatedly investigated in the dissertation of Mr. Felix Roemer, a Ph.D. candidate from the same institute. Besides the efficiency and cost, on system level, the concepts also have other advantages that could be further explored in the future.

Optimization

In this dissertation, the CHB is arbitrarily configured to match the specification of the benchmarked IGBT inverter. However, for an optimal efficiency or cost, the parameters of the circuit can still be optimized. These parameters include the number of submodules per phase, the nominal DC voltage of each submodule and the selection of MOSFETs. Besides the optimization of the parameters, it is also worth investigating whether the H-bridge is the optimal submodule. In fact, for modular multilevel inverters aiming at other applications, the optimal submodule circuit is an active topic of research [104], [113]. The developed methods could also be feasible for automotive inverters.

Control Algorithms

Through an improved control algorithm, the efficiency of the CHB can also be further enhanced. First, via an improved SOC balancing algorithm, more energy in the batteries could be used to drive the BEV, instead of being dissipated on the BMSs. Second, according to eq. (6.3), the RMS value of the ripples is related to the AC voltage of each submodule. Therefore, by carefully controlling the reference voltage of each submodule, the battery ohmic losses caused by the ripple current can also be reduced. In the end, due to the multilevel feature of the AC voltage waveforms, it is questionable whether the CHB still needs a rather high switching frequency to realize a low THD. To further reduce the switching loss, which accounts for approximately 50 % in the total loss of the inverter, the optimal switching frequency at each operational point should be searched for.

System Level Advantages

First, due to the balancing capability of the concept, new battery modules and aged battery modules could be mixed in the system. Therefore, when some battery modules reach end of life or break down, it is not necessary to replace the whole battery pack. The operation cost of the BEVs could thus be further reduced.

Second, the aged modules are more convenient for second life usage. Since each battery module has an integrated H-bridge on it, by cascading the aged modules, they can be directly connected to the AC power grid. Due to the balancing capability of these modules, the measurement and re-matching of the aged modules are not necessary either. Nonetheless, to realize the potential advantage, more studies should be conducted.

In the end, due to the AC interface of the CHB, no charging station is required anymore for high power charging of the batteries. The CHB can be directly charged by the three-phase 400 V AC power grid. Hence, the cost of infrastructures for a number of applications can be reduced. To realize the AC charging, further investigations regarding the control strategies and the system designs should be conducted.

9 Summary

Motivated by the possibility to reduce the cost of BEVs via a higher efficiency, this dissertation starts with driving cycle simulations to identify the efficiency of a benchmarked IGBT inverter. In the simulation, it is noticed that the benchmarked IGBT inverter has a rather low efficiency in the partial load area, which is mainly attributed to the intrinsic characteristics of IGBTs. As BEVs are not always driving at high speed, the low partial load efficiency of the IGBT inverters significantly deteriorates the average efficiency of electric powertrains.

Therefore, with the aim to improve the partial load efficiency, the dissertation conducts a literature research and categorizes the existing methods into three types, i.e., active DC link voltage control, SiC MOSFET inverter, and low voltage Si MOSFET inverter. By summarizing the existing studies, the dissertation identifies two key factors to solve the partial load problem at an acceptable cost. First, the switches of the inverter should work at a lower voltage, to reduce the switching loss at low speed. Second, Si MOSFETs should be used, so that the high losses of IGBTs and the high cost of SiC MOSFETs can be avoided.

Combining the two key factors, while considering the high voltage requirement associated with fast charging, this dissertation proposes to use the CHB as the general concept to solve the partial load efficiency problem. Such a circuit has been used for decades in industrial applications, but for automotive applications, its potential for efficiency improvement has not been evaluated yet. To verify the advantages of the concept, the efficiency and the cost of a specific CHB are examined, using a reference vehicle as an evaluation platform.

First, based on verified efficiency models, the CHB is proven to be capable of improving the efficiency significantly in all driving scenarios. In comprehensive driving cycles, the efficiency improvement is around 6 %. The improvement of efficiency is also proven to be more significant than that of the existing approaches, even when considering the influence of the CHB on the batteries and the motor.

Second, the system cost of the CHB is evaluated. The CHB indeed has a higher capital cost in the worst case, but the system cost can be effectively reduced, due to the reduced requirement of the battery capacity. Even in the worst-case scenario, CHB is still capable of reducing the system cost by 113 USD, which could be a significant cost reduction for mass-produced vehicles. A parameter sensitivity analysis further proves that the CHB concept is generally cost-effective for different BEVs.

The two verifications confirm that the proposed concept successfully meets the target of design, i.e., to reduce the cost via a higher efficiency. Compared to the existing approaches, especially the SiC MOSFET inverter, the CHB concept is also proven to be more effective.

Nonetheless, before practical implementations, there are still two concerns regarding the CHB concept. First, because of the ripples in the current waveform, the CHB is suspected to be harmful to lithium batteries. Second, since a much higher number of components are used in the

CHB, the reliability could also be questionable. To resolve the two concerns, dedicated investigations are conducted in the second half of the dissertation.

In order to investigate the influence of the current ripples on the battery aging, an aging experiment with eight battery cells is conducted, with a set of specifically designed hardware. According to the experimental results, the ripples in the CHB are harmless for lithium batteries, although three cells generate low capacity losses. An extensive discussion on previous studies further identifies two pre-conditions for the current ripples to become harmful. Nonetheless, the two conditions can be rather rarely met in the CHB. Therefore, the concern regarding the batteries is resolved.

To resolve the concern of reliability, the reliability of the CHB and the benchmarked IGBT inverter is modelled. The model is a combination of the fatigue models of the identified fragile points. The results indicate that the CHB should be at least as reliable as the IGBT inverter. Considering the dominant failure mechanism and the capability of the CHB to work during a fault, the CHB could be even more reliable than predicted.

According to the results obtained from the four investigations, the CHB concept is confirmed to be capable of outperforming the IGBT inverters. The advantages and disadvantages in other aspects are roughly discussed in the end. Several scenarios recommended for the CHB are also enumerated. Based on the experience gained from a prototype, the dissertation further provides suggestions for practical implementations.

As an overall conclusion, the CHB concept is proven to be generally promising for BEVs, in terms of efficiency and cost. This conclusion holds particularly before SiC MOSFETs become much cheaper.

However, to implement the CHB concept in BEVs, it is still necessary to search for the optimal solution to supply the power for auxiliaries, and the optimal solution to drive multiple motors in the powertrain. Moreover, to exploit the advantages of the CHB, an optimization of the concept is still recommended. Higher improvements are still possible by improving controlling algorithms and optimizing the specifications of the circuit. Additionally, further investigations should also be conducted to evaluate the efficiency improvement realized by mixing Si IGBTs and SiC MOSFETs. Especially for two-motor-driven BEVs, this solution could also improve the powertrain efficiency significantly. Nonetheless, whether this solution is cost-effective or not still requires further research.

List of Figures

List of Tables

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Appendix

Appendix A Efficiency Information

1. Parameters of the Models

In this appendix, all the detailed information regarding the efficiency analysis is provided. First, in Table A.1, the parameters of the reference vehicle and the motor can be found. Table A.2 contains all the necessary parameters of the efficiency models.

It is seen that the specifications of the three inverters match well with each other. The detailed parameters for the switches can be found in the datasheets of the corresponding switches. For the CHB and the SiC inverter, as they use discrete switches, the thermal circuit is simplified. Only one thermal resistor is assumed to be between the heatsink and the junction of the switch. Therefore, for these two inverters, only one thermal resistance value is give.

Table A.1: The parameters of the reference vehicle

Vehicle Parameters					
Parameter	**Symbol**	**Value**	**Parameter**	**Symbol**	**Value**
Mass	M	1443.3 kg	Gear ratio	i_{G}	9.7
Rolling resistance	f_{R}	0.0075	Transmission efficiency	η	98 %
Air resistance	c_{w}	0.33	Radius of tyre	r	0.350 m
Cross section	A_{A}	2.04 m^2	Rotation mass coefficient	∂	1.0696
Electrical Parameters					
IGBT module	Infineon HybridPACK™2		Nominal voltage of battery pack	360 V	
Rated current	400 A		Maximum current	600 A	
Electric machine	PSM		Number of pole pairs	6	
Coefficient $\boldsymbol{\beta_1}$	-2.5115×10^{-4}		Coefficient β_2	1.1425×10^{-6}	
Coefficient $\boldsymbol{\beta_3}$	0.945		Stator resistance R_{S}	9 mΩ	

Table A.2: The efficiency model parameters of the three inverters

Benchmarked IGBT Inverter					
Parameter	**Symbol**	**Value**	**Parameter**	**Symbol**	**Value**
IGBT forward voltage	u_{CE0}	0.7 V	IGBT dynamic resistance	R_{C}	0.75 mΩ
Diode forward voltage	u_{F0}	0.8 V	Diode dynamic resistance	R_{D}	1.1 mΩ
IGBT loss coefficient	a_{IGBT}	0.038	IGBT loss coefficient	b_{IGBT}	5.9×10^{-5}
Diode loss coefficient	a_{Diode}	9.3×10^{-3}	Diode loss coefficient	b_{Diode}	1.5×10^{-5}

IGBT thermal resistance	$R_{\mathrm{Tth(j-c)}}$	0.1 K/W	IGBT thermal capacitance	$C_{\mathrm{Tth(j-c)}}$	235 s·K/W
Diode thermal resistance	$R_{\mathrm{Dth(j-c)}}$	0.1 K/W	Diode thermal capacitance	$C_{\mathrm{Dth(j-c)}}$	250 s·K/W
Case thermal resistance	$R_{\mathrm{Dth(c-s)}}$	0.03 K/W	DC link voltage	u_{DC}	360V
Switching frequency	f_{s}	8 kHz	Gate resistance	R_{G}	2.2 Ω

SiC MOSFET Inverter

Parameter	**Symbol**	**Value**	**Parameter**	**Symbol**	**Value**
SiC on-state resistance	R_{on}	25 mΩ	DC link voltage	u_{DC}	360V
Number of parallel	n_{P}	6	Gate resistance	R_{G}	2.2 Ω
Diode forward voltage	u_{F0}	2.7 V	Diode dynamic resistance	R_{D}	15 mΩ
SiC loss coefficient	a_{SiC}	0	SiC loss coefficient	b_{SiC}	6.25×10^{-8}
SiC thermal resistance	$R_{\mathrm{Tth(j-c)}}$	0.25 K/W	Switching frequency	f_{s}	20 kHz

CHB

Parameter	**Symbol**	**Value**	**Parameter**	**Symbol**	**Value**
MOSFET resistance	R_{on}	4 mΩ	Diode recovery charge	Q_{rr}	380 nC
Number of parallel	n_{P}	6	Gate resistance	R_{G}	2.2 Ω
Diode forward voltage	u_{F0}	0.71 V	Diode dynamic resistance	R_{D}	1.85 mΩ
Voltage rising time	t_{ru}	9 ns	Voltage falling time	t_{fu}	21 ns
Current rising time	t_{ri}	17 ns	Current falling time	t_{fi}	20 ns
MOS thermal resistance	$R_{\mathrm{Tth(j-c)}}$	0.5 K/W	Case thermal resistance	$R_{\mathrm{Dth(c-s)}}$	0.5 K/W
Module DC voltage	u_{DC}	60 V	Switching frequency	f_{s}	20 kHz

2. Verifications of the Efficiency Models

Second, in Table A.3, Table A.4 and Table A.5, the results of accuracy verification are provided. Compared to the efficiency of ANSYS Simplorer, the errors of the proposed models are calculated. The error is defined by deducting the model predicted efficiency from the ANSYS efficiency.

It is seen that an error of 1 % is realized at most operational points. Only some points with an extremely low power could have an error of 2 %. Therefore, the proposed efficiency models can be deemed as rather accurate. Besides, it is seen that the proposed models tend to underestimate the efficiency of the three inverters slightly.

Table A.3: Verification of the IGBT efficiency model

U/I	50 V	100 V	150 V	160 V	cosθ
50 A	1.64 %	0.90 %	0.61 %	0.57 %	
100 A	2.45 %	1.34 %	0.90 %	0.84 %	
150 A	2.24 %	1.19 %	0.80 %	0.75 %	0.6
200 A	2.04 %	1.07 %	0.71 %	0.66 %	
250 A	1.90 %	0.99 %	0.65 %	0.60 %	
50 A	1.30 %	0.69 %	0.45 %	0.42 %	
100 A	1.92 %	1.01 %	0.67 %	0.62 %	
150 A	1.74 %	0.89 %	0.58 %	0.54 %	0.8
200 A	1.57 %	0.80 %	0.51 %	0.48 %	
250 A	1.47 %	0.73 %	0.47 %	0.43 %	
50 A	1.07 %	0.55 %	0.35 %	0.33 %	
100 A	1.57 %	0.80 %	0.52 %	0.48 %	
150 A	1.42 %	0.71 %	0.45 %	0.42 %	1.0
200 A	1.28 %	0.63 %	0.39 %	0.36 %	
250 A	1.18 %	0.57 %	0.35 %	0.33 %	

Table A.4: Verification of the SiC efficiency model

U/I	50 V	100 V	150 V	160 V	cosθ
50 A	1.19 %	0.65 %	0.44 %	0.41 %	
100 A	0.77 %	0.44 %	0.30 %	0.29 %	
150 A	0.36 %	0.28 %	0.17 %	0.19 %	0.6
200 A	0.16 %	0.13 %	0.01 %	0.09 %	
250 A	-0.09 %	-0.01 %	0.01 %	0.01 %	
50 A	1.13 %	0.61 %	0.41 %	0.39 %	
100 A	0.81 %	0.45 %	0.31 %	0.29 %	
150 A	0.54 %	0.32 %	0.22 %	0.21 %	0.8
200 A	0.31 %	0.20 %	0.14 %	0.14 %	
250 A	0.09 %	0.09 %	0.07 %	0.07 %	

50 A	1.13 %	0.61 %	0.40 %	0.38 %	
100 A	0.86 %	0.47 %	0.32 %	0.31 %	
150 A	0.63 %	0.36 %	0.25 %	0.24 %	1.0
200 A	0.43 %	0.26 %	0.18 %	0.17 %	
250 A	0.24 %	0.16 %	0.11 %	0.11 %	

Table A.5: Verification of the CHB efficiency model

U/I	50 V	100 V	150 V	160 V	cosθ
50 A	0.98 %	0.68 %	0.49 %	0.46 %	
100 A	0.87 %	0.55 %	0.39 %	0.37 %	
150 A	0.23 %	0.21 %	0.19 %	0.18 %	0.6
200 A	-0.03 %	0.08 %	0.11 %	0.11 %	
250 A	-0.16 %	0.01 %	0.07 %	0.07 %	
50 A	0.89 %	0.56 %	0.42 %	0.40 %	
100 A	0.45 %	0.34 %	0.29 %	0.28 %	
150 A	0.30 %	0.27 %	0.25 %	0.25 %	0.8
200 A	0.23 %	0.24 %	0.24 %	0.23 %	
250 A	0.21 %	0.04 %	0.23 %	0.23 %	
50 A	0.80 %	0.54 %	0.42 %	0.41 %	
100 A	0.47 %	0.38 %	0.33 %	0.32 %	
150 A	0.37 %	0.33 %	0.31 %	0.30 %	1.0
200 A	0.33 %	0.31 %	0.30 %	0.30 %	
250 A	-0.32 %	0.31%	0.31 %	0.31 %	

Besides the simulation verifications, for the CHB, the efficiency model is also experimentally on a motor test bench. However, the verification is only on the module level, because the batteries of the prototype are significantly aged and they are not safe anymore to operate at a high power. The test bench supports a maximum speed of 12000 1/min and maximum torque of 110 N m. The voltage and current sensors of the test bench are SP381501X, with a power measurement accuracy of 0.1 %.

The errors of the efficiency model compared to the experimental results are illustrated in the error map in Figure A.1. The definition of the errors is the same as in Table A.3, Table A.4 and Table A.5. According to the error map, the errors of the efficiency model are mostly within 1 %. Only in a small area, where the speed is low than 10 % of the maximum speed and the torque is

lower than 20 % of the maximum continuous torque, the errors reach 2-3 % level. Therefore, the efficiency model of the CHB is confirmed to have a high accuracy, at least on the module level. Besides, it is also seen that the efficiency model of the CHB tends to underestimate the efficiency in a large area, which agrees with the verifications in Table A.5. Therefore, the accuracy of the ANSYS models is also confirmed again by the experiment.

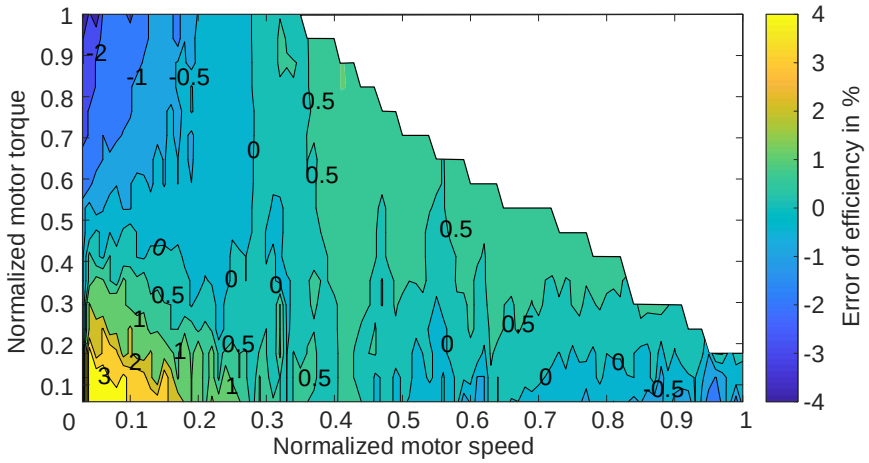

Figure A.1: The error of the CHB efficiency model (one module) compared to experimental results

In all the verifications, the errors are mainly caused by the oversimplified diode model. For the IGBT inverter, the conduction loss of the diode is obtained based on the simplification that the diode has a piecewise linear output character. For the CHB, the worst-case recovery loss is constantly assumed regardless of the operational points. Therefore, in the area with an extremely low power, the errors could be higher than 1 %. However, as this area is also sparsely used by BEVs, a slightly higher error in this area will not cause problems for the driving cycle simulations.

3. Deduction of the Ripple Current Models

In the end of this Appendix, the RMS values of the ripples are derived. These values are used in chapter 4 for the evaluation of the ohmic losses in batteries. First, the overall RMS value of the battery current in the CHB is calculated. Following the definition of the RMS value, in one AC period, the RMS value of the battery is calculated following eq. (10.1). Assuming the switching frequency approaches toward infinite, i.e., T_S approaches zero, the sum in the formula can be converted to an integral. In the end, converting the AC side values to the DC side values, eq. (4.10) and (6.3) can be obtained.

$$I_{\text{bat\_RMS}} = \sqrt{\frac{\sum I_{\text{AC\_peak}}^2 \sin^2(\omega k T_S - \theta) m_a \sin(\omega k T_S) T_S}{T_{\text{AC}}}} = \sqrt{\frac{\int_0^{\pi} I_{\text{AC\_peak}}^2 \sin^2(\omega t - \theta) m_a \sin(\omega t) d\omega t}{\pi}} \tag{10.1}$$

The current waveform of the battery contains mainly three components, the DC component, $I_{\text{bat\_ave}}$, the AC frequency component, $I_{\text{bat\_AC\_RMS}}$ and the switching component, $I_{\text{bat\_S\_RMS}}$. The DC component is the average current, which can be calculated by the average power. The switching frequency component, $I_{\text{bat\_S\_RMS}}$, is calculated by eq. (4.10), which is developed by [138]. Using the definition of the RMS value, and assuming that the remaining components of

$I_{\mathrm{bat\_RMS}}$ can all be allocated to the AC frequency ripples, the RMS value of the AC frequency ripples is obtained as in eq. (4.10) and (10.2).

$$I_{\mathrm{bat\_AC\_RMS}}=\sqrt{I_{\mathrm{bat\_RMS}}^2-I_{\mathrm{bat\_ave}}^2-I_{\mathrm{bat\_S\_RMS}}^2} \tag{10.2}$$

For the IGBT inverter, the ripple current is estimated based on the voltage ripples of the DC-link capacitor. Once the voltage ripple is obtained, the current ripples can be calculated accordingly. First, according to the research in [139], the ripple index, r_{ppIGBT}, is calculated. With the ripple index, the switching frequency, the AC current, and the DC-link capacitance, according to [139], the peak-to-peak value of the envelope of the ripples, Δv_{pp} is obtained.

$$\begin{cases} r_{\mathrm{ppIGBT}} = -1.09m_{\mathrm{a}}^2 + 0.74m_{\mathrm{a}} \\ \Delta v_{\mathrm{pp}} = \dfrac{\sqrt{2}I_{\mathrm{AC\_RMS}}r_{\mathrm{ppIGBT}}}{3C_{\mathrm{DC}}f_{\mathrm{S}}} \\ I_{\mathrm{bat\_S\_RMS}} = \Delta v_{\mathrm{pp}} / R_{\mathrm{bat\_fs}} / 3 \\ P_{\mathrm{bat\_ohmic}} = R_{\mathrm{bat\_DC}}I_{\mathrm{bat\_ave}}^2 + R_{\mathrm{bat\_fs}}I_{\mathrm{bat\_s\_RMS}}^2 \end{cases} \tag{10.3}$$

Assuming the ripples are triangle waves, the RMS value of the corresponding ripple current, $I_{\mathrm{bat\_S\_RMS}}$, can be calculated by dividing Δv_{pp} with the battery resistance at this frequency. The factor 3 is implemented when converting the peak-to-peak value of the triangle wave to the RMS value of the triangle wave.

In the end, multiplying the square of the current with the corresponding resistance, the total ohmic loss can be obtained. The description above explains how all the formulas in eq. (4.11) can be used. Eq. (4.11) is copied in eq. (10.3), for the convenience of explanation. The resistance values of the battery at different frequency are obtained in the impedance spectrum in [137]. Only the real part needs to be taken, because the imaginary part does not cause any losses.

Appendix B Cost Parameters

In Table B.1, the cost parameters of the three inverters are provided for verification. The currency values are in USD. All the three inverters are assumed to be controlled by a DSP (Digital Signal Processor) board as the central contreoller. This module is expected to cost 150 USD, according to the large volume prices of relevant components on online purchasing platforms. The cost of the ICs of the two six-pack inverters is thus 150 USD.

Table B.1: The parameters for the cost model

Parameters		IGBT		CHB	SiC
Switch cost parameters	No. of switches	1		216	36
	c_{Die} per mm^2	0.0613 (IGBT)	0.0273 (Diode)	0.0273	1.057
	A_{Die} in mm^2	98.88	49.41	17.28	26.018
	Number of dies per package	24	24	1	1
	$C_{package}$	118.82		0.46	0.6105
	$C_{switch} = c_{Die}A_{Die}+C_{package}$	296.61		0.93	28.1
Driver cost	No. of drivers	6		36	6
	Unit driver cost	6.5		6.5	11
Capacitor cost	DC-link capacitance	475 µF		-	475 µF
	Capacitor voltage	450 V		-	450 V
Heatsink cost	Number of modules	1		9	1
IC cost	Central Controller	150		150	150
	CPLDs and Communications	0		150	0
Manufacturing overhead		1.25		1.25	1.15

For the CHB, on top of the DSP module, each submodule additionally needs one CPLD EPM7064AETC44 (5.25 USD) chip and one set of fiber optic receiver/transceiver HFBR-2522/1521Z (respectively 5.72 USD and 5.24 USD for the receiver and transceiver) for a rapid communication and control. Therefore, an additional 9×(5.25 + 5.72 + 5.24) = 150 USD is assumed to for the cost of ICs in the CHB, which results in a total cost of 300 USD for the ICs of the CHB.

For the IGBT and Si MOSFET, the driving circuit is assumed to have one isolated ±15 V DC power supply MEA1D0515DC and one isolated circuit driver 1ED020I12-F2. The costs of other

components are negligible. The unit price of the driving circuit of the IGBT and Si MOSFET is thus estimated to be USD 6.5, based on the large bundle prices of the two components.

The driving circuit of the SiC is special, because the output gate voltage output is required to be +20/-5 V. According to the reference design CGD15FB45P1 provided by Wolfspeed, the cheapest solution results in a cost of USD 11, using the large volume prices of the relevant components.

Appendix C Aging Test Circuit

Schematic

The detailed schematic of the testing circuit is given in Figure C.1.

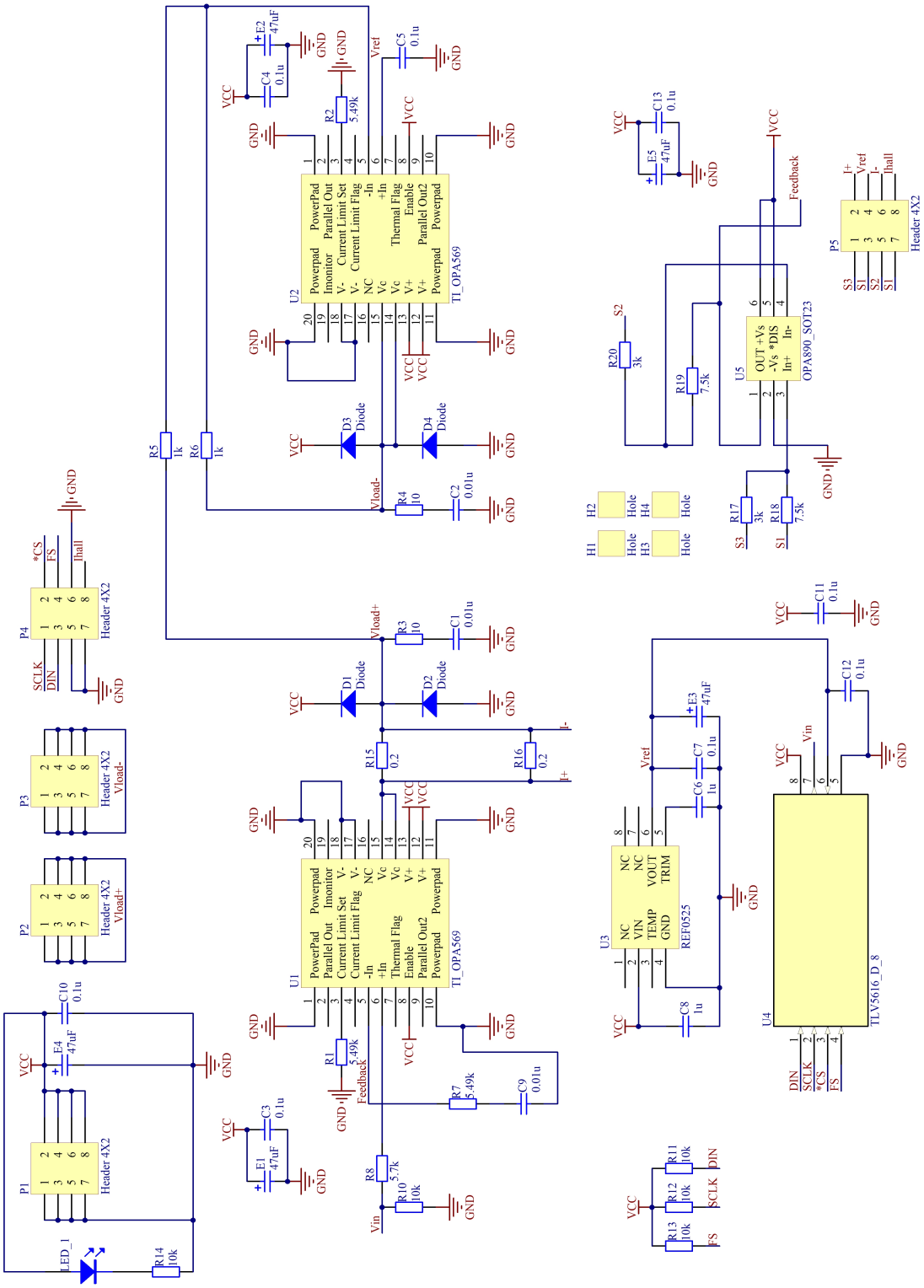

Figure C.1: Schematic of the testing circuit module board

The power opamp OPA569 from Texas Instrument is selected. The feedback network uses OPA890, due to its high gain at high frequency. The DAC is TLV5616. The selection of the ICs realizes the requirement of high frequency and high accuracy.

The design of the base board is relatively simply, as it only serves as a busbar for the power opamp modules. Therefore, its scehmatic is not given in the appendix. The digital interfaces of the modules are also paralleled by the base board and are controlled by the same micro controller, so that the multiple module boards do not require synchronization after the parallelization. Their behaviors are identical.

Appendix D Reliability Parameters

All the parameters required by the reliability models are provided in Table D.1 and Table D.2.

Table D.1: Parameters to model the reliability of the benchmarked IGBT inverter

The benchmared IGBT Inverter					
Die attachment reliability					
A_1	3.71×10^{13}	A_2	9455.52	α	-10.122
Bond wire reliability					
α_{Copper}	$25\ 10^{-6}\ K^{-1}$	α_{Solder}	$16\ 10^{-6}\ K^{-1}$	n_{Bond}	600
D_{Bond}	300 µm				
PCB reliability					
l	1.4 mm	h	0.47 mm	n_{PCB}	1
α_{copper}	$16\ 10^{-6}\ K^{-1}$	α_{Solder}	$23\ 10^{-6}\ K^{-1}$	n_{Solder}	100
$a_{Vibration}$	$0.9\ m/s^2$	f_n	0.86 Hz		
Capacitor reliability					
T_n	50 °C	T_{test}	61.3 °C	$t_{nominal}$	2.01×10^6 h
V_n	450 V	V_{test}	360 V		

Table D.2: Parameters to model the reliability of the CHB

The CHB					
Die attachment reliability					
k_b	$1.38\times10^{-23}\ J\ K^{-1}$	n_J	144		
Bond wire reliability model					
α_{Al}	$25\ 10^{-6}\ K^{-1}$	α_{Solder}	$16\ 10^{-6}\ K^{-1}$	n_{Bond}	1080
D_{Bond}	300 µm				
PCB reliability					
l_{PCB}	1.4 mm	h_{PCB}	0.47 mm	n_{PCB}	9
α_{PCB}	$18\ 10^{-6}\ K^{-1}$	$\alpha_{Ceramic}$	$10\ 10^{-6}\ K^{-1}$	n_{Solder}	500
$a_{Vibration}$	$0.9\ m/s^2$	f_n	2.53 Hz		

Nonetheless, the input of the values, i.e., the stress profiles, are not provided in the appendix, because the amount of data is too large to be directly listed here. For more details, the reader is referred to the MATLAB code and the data of the reliability simulation. The necessary comments can be found in the code.

Appendix E Electronic Attachments

In the end of the appendix, the folder structure of the electronic attachments is explained, in order to make the search and further usage of the work more convenient.

Powertrain models and component models:

Electronic Attachments\01 Efficiency Simulation Models\01 Models

Efficiency map calculation files:

Electronic Attachments\01 Efficiency Simulation Models\02 Efficiency Maps

All the verification calculations and results:

Electronic Attachments\01 Efficiency Simulation Models\03 Verifications

Detailed cost calculation of the three inverters:

Electronic Attachments\02 Cost Calculation

Design documents of the battery testing hardware:

Electronic Attachments\03 Battery Test Hardware Design

Simulation models for reliability, IGBT and CHB integrated:

Electronic Attachments\04 Reliability Simulation Models

Design documents of the CHB prototype:

Electronic Attachments\05 CHB Prototype Design

A rapid simulation model for battery packs:

Electronic Attachments\06 Battery Models