Closed Loop Current Control of a Grid Connected Transformerless Flying Capacitor Inverter

Master Thesis

to gain the academic degree

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Department of Electrical and Computer Engineering,
Institute for Electrical Drive Systems and Power Electronics.

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Abstract

Renewable sources of energy such as solar and wind energy are being increasingly used as alternatives to conventional energy resources. The primary energy of these sources varies widely in its nature due to various factors like weather conditions, irradiance level, wind speed, etc. Therefore, high efficiency power electronic converters are required to interface these sources with the grid. Specifically for solar power, there has been an increasing trend to use transformerless converters with multilevel output. The advantage of using such converters lies in the removal of the bulky transformers, implying smaller converters and better efficiencies. Moreover, control algorithms play a crucial role in the operation of grid-connected converters. Therefore, this thesis aims to examine linear and non-linear control techniques for a recently proposed transformerless inverter namely Siwakoti-H inverter, equipped with a LCL filter.

The linear controller is designed using pole placement to directly set the dominant dynamics of the controller and actively damp the resonant frequency of the filter. In addition, a major portion of this work deals with the application of model predictive control (MPC) for the control of Siwakoti-H inverter. MPC is an advanced control technique that has seen a lot of application in the past decade. Firstly, the direct MPC is introduced as a current controller. As a next step, MPC is used with a modulator to facilitate the use of long prediction horizons and reduce the computational effort. Finally, a non-linear model of the converter is proposed and its accuracy is verified using direct MPC scheme. The working of the proposed control algorithms is verified in simulations. Additionally, some experimental results are presented to prove that this topology can be controlled in the grid-connected mode.

Statement

The work in this thesis is based on the research jointly carried out at the the Department of Power Converter Systems (PCS), Fraunhofer Institute for Solar Energy Systems ISE, Freiburg and the Institute for Electrical Drive Systems and Power Electronics, Technische Universität München (TUM). No sections of this thesis were submitted or used to gain another academic degree. Hereby I state, that this thesis was written alone by myself, except of explicitly marked passages.

Munich, November 28, 2018
Mirza Abdul Waris Begh

Acknowledgments

I find it hard to express my gratefulness to the Creator of the heavens and the earth, for bestowing upon me His deepest blessings and for the warmth and kindness He has showered upon me.

This Master's thesis is based on my research jointly carried out at the Department of Power Converter Systems (PCS), Fraunhofer Institute for Solar Energy Systems ISE, Freiburg, and the Institute for Electrical Drive Systems and Power Electronics, Technical University of Munich (TUM).

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Words are inadequate to express my heartfelt gratitude to my parents and my siblings for the moral support and the trust they have in me. Without them, I could hardly finish this work.

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Mirza Abdul Waris Begh

Contents

Nomenclature

Symbol	Meaning
$\mathbb{N}$	$:= \{0, 1, 2, 3, \dots\}$, set of natural numbers
$\mathbb{N}_{>0}$	$:= \{1, 2, 3, \dots\}$, set of positive natural numbers
$\mathbb{R}$	$:= (-\infty, \infty)$, set of real numbers
$\mathbb{R}_{>0}$	$:= (0, \infty)$, set of positive real numbers
$\mathbb{R}_{\geq 0}$	$:= [0, \infty)$, set of positive real numbers including 0
$\mathbb{C}$	$:= [-\infty, \infty)$, set of complex numbers
In the following let $n, m \in \mathbb{N}_{>0}$.	
$\boldsymbol{x}$	$:= [x_1 \ x_2 \ \dots \ x_n]^\top \in \mathbb{R}^n$ (column) vector with $x_i \in \mathbb{R}$ $\forall i \in \{1, 2, \dots, n\}$, **all vectors are bold**
x	$\in \mathbb{R}$, scalar, **all scalars are non-bold**
$\mathbf{X}$	$:= \begin{bmatrix} x_{11} & \dots & x_{1m} \\ \vdots & \ddots & \vdots \\ x_{n1} & \dots & x_{nm} \end{bmatrix} \in \mathbb{R}^{n \times m}$, matrix with coefficients x_{ij} $\forall i \in \{1, 2, \dots, n\}$ $\forall j \in \{1, 2, \dots, m\}$, **all matrices are upper case and bold**
x	$\in \mathbb{R}$, constant scalar, **all constants are non-italic**
$\dot{x}$	$:= \frac{\mathrm{d}x}{\mathrm{d}t} \in \mathbb{R}$, first time derivative of $x \in \mathbb{R}$
α, β	orthogonal axes of the stationary reference frame
d, q	orthogonal axes of the rotating reference frame
$\mathfrak{Re}\{x\}$	real part of the complex variable x
$\mathfrak{Im}\{x\}$	imaginary part of the complex variable x
$\|x\|_\infty$	infinity-norm of the vector x (largest absolute value)

Chapter 1

Introduction

1.1 Background

Due to the uncertainty in the future supply of crude oil and the associated problems of environmental pollution, renewable energy sector has seen an increasing trend over the past decade, especially the solar and wind energy. The continuous growth of the renewable energy market is driven by its low carbon footprint, because carbon emissions are the major cause of global climate change. The global consumption of renewable energy is predicted to increase by an average of 2.6% (per year) till 2040 [1]. The integration of renewable energy resources to the grid requires an interfacing converter. Power electronic converters are considered as the backbone for energy conversion. For example, in solar power generation they convert the direct current (dc) from the photovoltaic (PV) system to alternating current (ac) which is then supplied to the grid [2]. Notable advances in semiconductor technology has enabled better and efficient power conversion. In order to increase the power quality and utilization of the PV system, new inverter topologies with better control algorithms are required to be proposed. This thesis aims to investigate some of these control techniques for a recently proposed transformerless inverter based on the principle of flying capacitor (FC).

In recent years, grid-tied inverters for PV systems have seen a rapid growth for both the utility-scale and distributed generation applications owing to government incentives, declining prices of PV panels and advancement in power electronics technology [3, 4]. The growth of PV has been exponential between 1992-2017. During this period, solar PV evolved from a niche market of small scale applications to a mainstream electricity source. There has been a huge growth from approximately 1.2 GW in 1992 to 401.5 GW in 2017. For example, see Figure 1.1 which shows the annual installed solar capacity for various regions of the world. Although, the European countries collectively have the highest amount of solar installations, China appears to take the lead in terms of the growth in solar installations. The European Photovoltaic Industry Association claims that by 2050 solar power will become the world's largest source of electricity [5]. In Germany it has become common to see PV systems installed on rooftops or PV farms of varied capacities next to the roads in the countryside.

A major part of the generated electricity from solar PVs is consumed immediately, since storage is comparatively expensive. Hence almost 99% of the installed PV capacity corresponds to grid-connected systems [4]. In grid-connected PV systems, storage is not necessary since all of the generated power is directly supplied to the utility grid. In this fashion traditional energy sources, like hydro or fossil fuels, can adapt to the power demand and behave as virtual storage devices to serve the purpose of power regulation and backup. However, solar power is inherently variable and intermittent in nature due to the day/night cycles and weather conditions. Moreover, due to its availability only during the day, storage of solar energy is potentially an important issue particularly in off-grid systems, to have continuous availability of electricity [5].

A typical configuration of a grid-connected PV system is presented in Figure 1.2. The PV

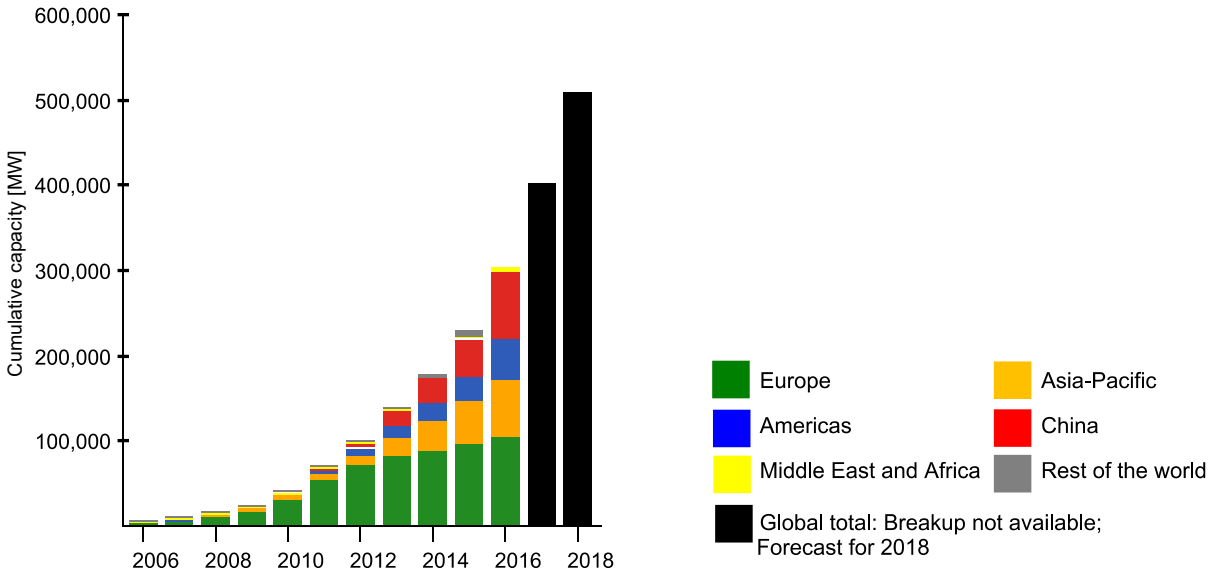


Figure 1.1: Yearly installed solar capacity [5].

panels generate a *dc* current that varies according to solar irradiance, temperature, and the terminal voltage [4]. The generated *dc* power must be converted and supplied to the grid as *ac* power. Additional components used include a grid connection filter, a transformer and a typical grid angle tracking system, e.g., a phase-locked-loop (PLL). An optional *dc/dc* conversion stage can be used between the PV panels and the inverter. A *dc/dc* converter is normally used to decouple the PV system operating point from the inverter and allow maximum power point tracking (MPPT) control. Additionally, the *dc/dc* stage can be used to boost the PV output voltage [4].

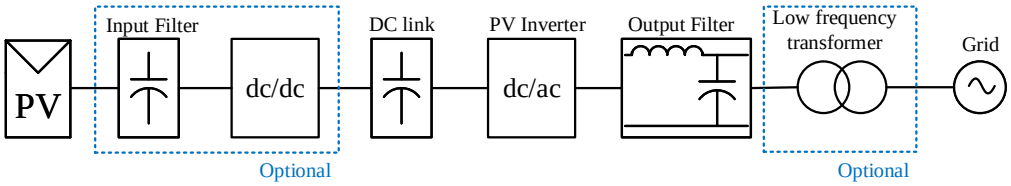


Figure 1.2: A generic structure of a grid connected PV system [4].

In PV applications, a transformer is often used for galvanic isolation and voltage transformations [3]. However, transformers are quite bulky and thus increase the size/weight of the inverter while reducing efficiency and power density. Due to the massive development of grid-connected PV systems, there has been an increasing trend to avoid the use of interfacing transformers and replace them by using transformerless inverter topologies. Although, transformerless topologies offer better efficiencies, less weight/volume ratio, and hence lower costs; removing the transformer gives rise to common-mode currents or leakage currents, due to the presence of parasitic capacitance between the PV panel and its frame [3]. Hence, additional measures have to be undertaken to eliminate the leakage currents and prevent any safety hazards. Consequently, grid-connected transformerless PV inverters must comply with strict safety standards [4]. Various research works have proposed different techniques to mitigate the common-mode currents, e.g., decoupling the *dc* from *ac* side and/or clamping the common-mode voltage (CMV) during the freewheeling period, or using common ground configurations [3]. Common-ground-type PV inverter has attracted a lot of interest from both industry and academia as it can effectively reduce the leakage current of the PV system. Many common ground transformerless inverters have been proposed, for e.g. in [6–12], but they either use more switches or more passive components. In [13] a new common-ground-type transformerless

inverter was proposed, consisting of only four switches and works on the principle of a flying capacitor. The new inverter allows direct connection between the grid-neutral and the negative-pole of the PV system in order to eliminate the leakage currents. In [3] a detailed design and analysis of the working of a family of transformerless inverters was presented.

1.2 Motivation

Power electronic converters are enabling technologies for control and conversion of electric power by virtue of a certain pattern of switching operations applied to semiconductor switches. In grid-connected power electronic systems quality of the current injected into the grid is a priority, whereas for renewable energy conversion efficiency of the converter is very important. These two objectives have been the main drivers behind the progress in the PV converter market and hence more and more PV systems are connected to the electrical grid via power electronics. The use of grid-connected converters allows independent control of active and reactive power exchanged with the grid. However, grid-connected converters generate harmonics which might be harmful for other devices connected to the same grid. In order to meet the grid-code requirement of injecting a clean current, with less total harmonic distortion (THD), it is crucial to use a filter (L or LCL filter) between the converter bridge and the grid [14]. Compared to the L filter, the LCL filter provides much higher attenuation of switching harmonics, and uses smaller components that reduce the volume and weight while increasing power density [15]. However, control of the LCL filters is complicated due to the presence of a resonant peak in its response. The resonant behavior of the LCL filter amplifies any harmonic components in its vicinity, thereby deteriorating the performance of the converter [16]. This behavior can either be damped by using passive methods which cause additional power losses or by using active damping methods [17].

Conventionally, the control of grid-connected inverters is carried out by employing voltage oriented control (VOC) [18, 19]. VOC uses linear controllers based on a simple proportional-integral (PI) controller, designed in the synchronous reference frame. Although these controllers are simple and can ensure a moderate quality of the injected grid current, the design of controller gains is often based on the linear model and hence does not include any non-linearity present in the system. Additionally, this controller suffers from the problem of integral-windup which necessitates the uses of anti-windup methods, hence the dynamic response of this scheme is slow.

Among other approaches, a proportional-resonant (PR) controller [20], state-feedback controller [21–24] and a predictive controller [25] have been proposed in literature. The PR controllers have been widely used for the control of grid-connected inverters due to their property to introduce infinite gain at selected frequencies, thereby mitigating the resonant behavior of LCL filters. In [21–23] a pole-placement based control strategy has been proposed that has inherent resonance damping and does not require any additional damping solutions. While [21] deals with the control design in continuous-time, [22,23] have proposed a controller in the discrete-time domain. Since pole-placement is generally not based on a systematic design procedure, [24] presents a controller design based on linear quadratic regulator (LQR), where a cost-function is minimized to place the poles in an optimal way.

Predictive Controllers are an alternative to linear controllers as they allow control of the system constraints, non-linearities and other requirements by using a single cost function. Model predictive control (MPC) uses a model of the system, called prediction model, to calculate (or predict) the future behavior of the controlled variables and then solve for the best possible prediction according to an optimization criterion [72]. Calculation of the predicted behavior and simultaneous optimization imposes an enormous calculation burden on the controller. However, due to continuous development in the semiconductor technology modern microprocessors have very high calculation power and are well suited for MPC applications.

MPC can handle multiple objectives simultaneously by incorporating them into a single cost

function. Moreover, MPC can successfully handle system and operational constraints that can be imposed on the variables of concern and thus allows the system to operate at its limits. Thanks to these characteristics, MPC is particularly effective for systems with complex dynamics, such as many power electronic systems [27]. MPC applied to power converters can be generally classified into two main approaches, continuous control set MPC (CCS-MPC) and finite control set MPC (FCS-MPC) [28]. While CCS-MPC generates a duty cycle and uses a modulator for generation of gating signals, FCS-MPC takes the advantage of the discrete nature of the power converter and hence the switches of the converter are directly manipulated without the need of a modulator [27, 29–31].

Motivated by the increasing trend in the use of transformerless topologies for grid-connected PV systems, the focus of this thesis is the design and implementation of various control strategies for a recently proposed Type-III, Siwakoti-H flying capacitor inverter (sFCI), see [3, Sec. II B], to enable subsequent connection to the grid.

1.3 Thesis objectives

Unlike the conventional three-level inverter topologies like neutral point clamped (NPC) and H-bridge, the sFCI topology has not been extensively analyzed for the design of a control algorithm. This thesis aims to design and implement different control techniques that can enable reference current tracking and voltage ripple control on the flying capacitor. This thesis aims to fulfill the following objectives:

- A thorough analysis of the operating states in order to understand the working of the sFCI and derivation of a mathematical model that describes the behavior of the linearized system.
- Realization and experimental evaluation of state-feedback controller and observer, using the pole placement approach for feedback gain calculation.
- Design and simulation of enumeration based FCS-MPC scheme using a linear model of the grid-connected three-phase sFCI.
- Design and simulation of a controller based on the CCS-MPC approach using the linear converter model.
- Derivation of a non-linear model of the grid-connected sFCI by incorporating the dynamics of the flying capacitor into the converter model, and validation of the derived non-linear model using direct MPC scheme.

1.4 Thesis organization

The upcoming chapters of this thesis are organized as follows:

Chapter 2 presents a literature review regarding the research problem. Firstly, it addresses the different multi-level inverter topologies which are widely used. Then, the sFCI is introduced as an interesting alternative to the conventional topologies. In addition, the basics of state-feedback control and MPC techniques are also discussed.

Chapter 3 discusses the sFCI topology in detail. The design, working of the sFCI and the open loop response for a resistive load is discussed. Further, a detailed analysis of the additional non-linearities of the sFCI is presented and a comparison is drawn with a conventional NPC converter. Finally, in chapter 3 a three-phase sFCI with LCL filter is presented and a linear system model is derived.

Chapter 4 proposes the design, simulation and analysis of a state-feedback controller and observer, in discrete time, for a single-phase sFCI. Further, the state-feedback controller is extended to the

three-phase sFCI. Firstly the issues related to the three phase system control are discussed and then a controller, designed in the (d, q)-reference frame, is presented. Performance of the controller for grid current control is verified by simulations.

Chapter 5 uses the linearized converter model and is further divided mainly into two parts, where the first part deals with the design of a controller using FCS-MPC scheme, and the second part deals with a controller using the CCS-MPC scheme. Mathematical modeling, design and working are presented for both the schemes and each part concludes with the simulation results.

Chapter 6 discusses the problems associated with the new topology and proposes solutions. In particular, a non-linear model is derived and a control scheme based on this model is presented. Finally, the operation is verified using Matlab simulations.

Chapter 7 briefly discusses the hardware implementation of the state-feedback control on a single-phase testbench. The various modules used and methodology adopted is presented. Experimental results are included which affirm the working of the controller and the fact that this new inverter can be controlled in the grid-connected mode. Chapter 8 concludes this thesis.

Chapter 2

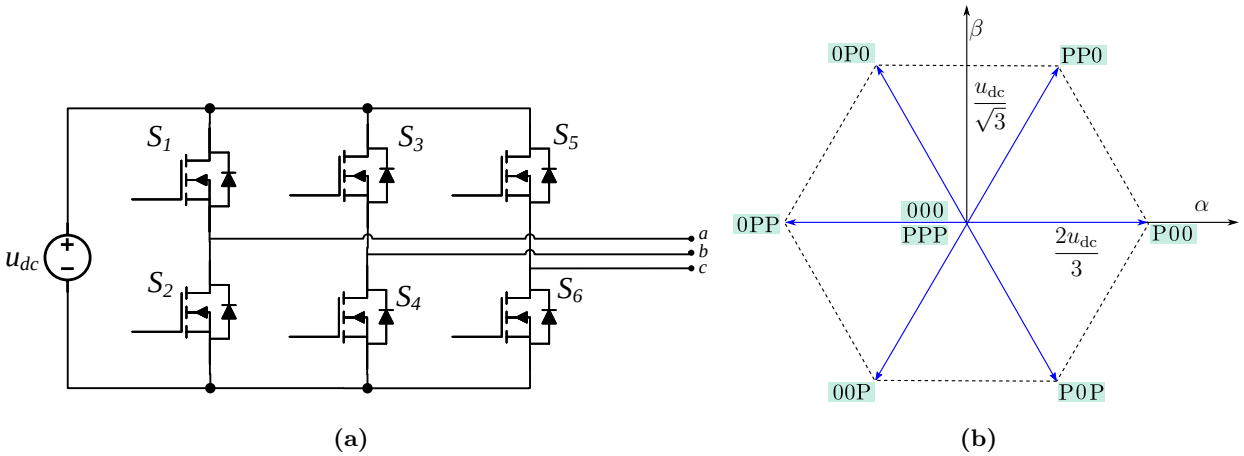
Theoretical Background

This chapter introduces the three-level inverter as an attractive alternative to the conventional two level voltage source inverter (VSI). First the different converter topologies used for grid-connected systems will be presented and later the sFCI will be introduced briefly. Finally, the conventional control and advanced control strategies for the multi-level inverters will be highlighted. This chapter is concluded by deriving a model for the system consisting of sFCI and LCL filter.

2.1 VSI Topologies

2.1.1 Two-level inverter

The most commonly used topology for a three-phase VSI with bi-directional energy flow capability is the two-level inverter (2LI), which can produce an output voltage having two levels [33]. This topology has a simple construction as there are only 6 switches with anti-parallel diodes, as depicted in Fig 2.1(a). The switches can be typically controlled with simple sine-wave pulse-width-modulation (PWM) signals. Since the semiconductor switches are switched at a very fast rate, the output current contains a lot of harmonics and specific filters have to be employed. Each phase in the 2LI has two states, namely 'P' and '0'. If the upper switch is turned *on*, the state is termed as 'P'. On the contrary, when the lower switch is *on* the state is termed as '0'. In general an n-level inverter can have a total of n^3 switching states. In case of 2LI there are 8 possible switching states, which give rise to 8 different voltage vectors, depicted in Fig. 2.1(b), with discrete voltage values $\in \{0, \pm\frac{1}{2}u_{dc}, \pm\frac{2}{3}u_{dc}\}$.



(a) **(b)**

Figure 2.1: (a) Schematic diagram of the two level inverter. (b) Switching vectors of the 2LI.

However, the two-level inverters have several drawbacks including higher THD, high electromagnetic interference (EMI) and higher dv/dt stress. To overcome these drawbacks multi-level inverters are preferred as they offer more output voltages, improved current THD and hence better performance.

2.1.2 Multilevel inverters

Multilevel Inverters (MLIs) have received a lot of attention in the industry during the last decade because of their increased power rating, less EMI and lower switching losses owing to their ability to work at lesser switching frequencies. The term MLI was coined with the advent of the three-level inverters which have a staircase voltage output [32]. Over the last two decades a number of multilevel topologies have emerged, even with more than three voltage levels. The elementary concept of a multilevel converter is to achieve higher power by synthesizing a staircase voltage waveform by employing several lower voltage *dc* sources. Capacitors, batteries, and renewable energy sources can be used as the *dc* voltage sources [33].

A MLI has several advantages over a conventional two-level inverter including reduced dv/dt stress of the switches, less electromagnetic compatibility (EMC) problems, lower current distortion and ability to operate for a wide range of switching frequencies. However, the main drawback of MLIs is the usage of more semiconductor switches, which increases the gate driver requirement and possibly the conduction losses. Traditionally, the MLIs are categorized into three main topologies: 1) Neutral Point Clamped (NPC), 2) Cascaded H-Bridge (CHB) and 3) Flying Capacitor (FC).

2.1.2.1 Neutral point clamped inverter

Fig 2.2(a) shows the schematic of a diode-clamped inverter also known as neutral point clamped (NPC) inverter. It is the most widely used topology and was introduced by Nabae, et al., in 1981 [32]. NPC has been widely implemented in medium voltage applications as it exhibits a relatively high efficiency [34]. It consists of four switches and two diodes connected in a fashion as shown in Fig. 2.2(a). The NPC utilizes a single *dc*-link that is subdivided into a number of voltage levels by a string of series capacitors. For a three-level NPC (3L-NPC), the *dc*-link uses two capacitors with the mid-point termed as the neutral point. A diode is connected between the neutral point and the mid-point of the upper and lower legs. Considering the neutral point to be at zero potential the output bridge voltage of the NPC has three values ($-\frac{1}{2}u_{dc}$, 0, $+\frac{1}{2}u_{dc}$). Unlike a 2LI, each phase of the 3L-NPC has three switching states, denoted as $\{N, 0, P\}$ and summarized in Table 2.1.

Switching state	**Notation**	S_1	S_2	S_3	S_4	**Bridge Voltage**
Positive	P	1	1	0	0	$+\frac{1}{2}u_{dc}$
Zero	0	0	1	1	0	0
Negative	N	0	0	1	1	$-\frac{1}{2}u_{dc}$

Table 2.1: Switching states of 3L-NPC inverter.

In total the 3L-NPC can produce as total of $3^3 = 27$ different voltage vectors, see Figure 2.2(b). The voltage vectors can take discrete voltage values as

$$u \in \left\{0, \pm\frac{u_{dc}}{6}, \pm\frac{u_{dc}}{3}, \pm\frac{u_{dc}}{2}, \pm\frac{2u_{dc}}{3}\right\}$$

Out of these 27 vectors, only a subset of 19 vectors are unique and rest of them can be considered as redundant. These redundant vectors serve the purpose of voltage balancing in control applications. Although higher levels for a NPC can be obtained by increasing the number of switches and passive devices, balancing of voltages on the input capacitors becomes quite tricky and therefore, NPC is

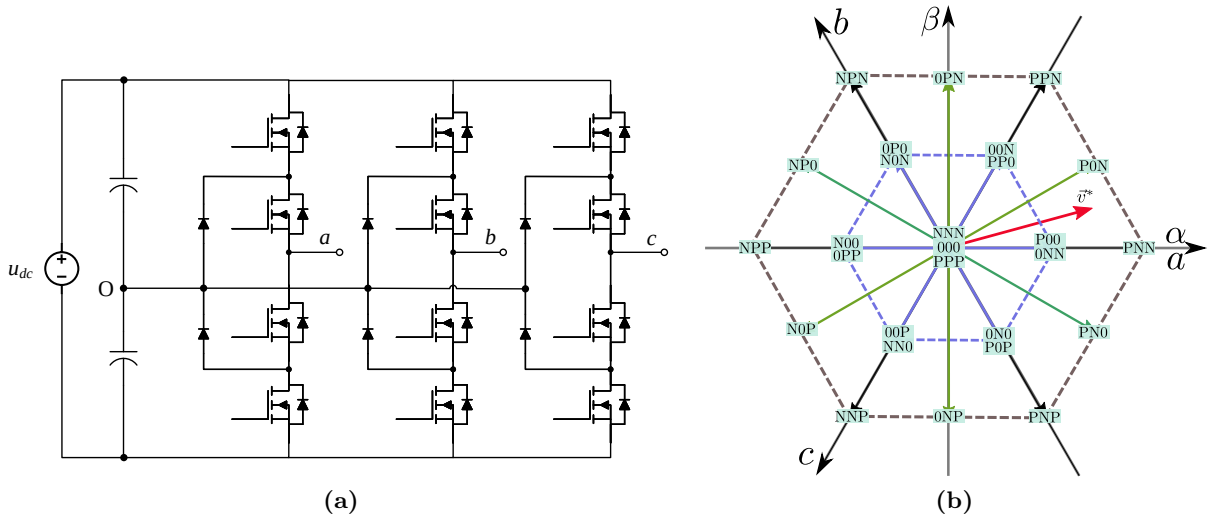


Figure 2.2: (a) Schematic diagram of the three level NPC inverter [32]. (b) Switching vectors of the 3L-NPC [35].

limited to three levels. Its applications include Static VAR Compensator, variable speed drives and high power interconnections [34].

2.1.2.2 Flying capacitor inverter

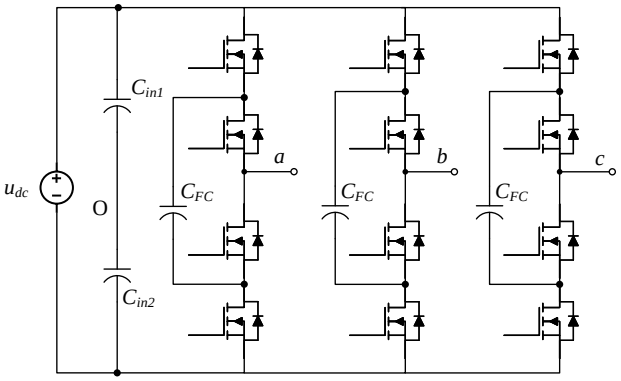


Figure 2.3: Schematic diagram of three-level flying capacitor multilevel inverter [36].

Flying Capacitor multilevel inverter (FC-MLI) was introduced by Meynard et al., in 1992 [36]. The structure of the FC-MLI is similar to the NPC except the clamping diodes are now replaced by the clamping capacitors, as depicted in Fig. 2.3. This inverter topology provides more flexibility in waveform synthesis and voltage balancing, although control algorithms are more complex. This topology has a ladder structure of *dc* side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform [33].

One advantage of the flying-capacitor based inverter is that it has redundancies for inner voltage levels; in other words, two or more valid switch combinations can synthesize an output voltage. Unlike the diode-clamped inverter, the flying-capacitor inverter does not require all of the switches that are conducting, to be in a consecutive series. Moreover, the redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels [33].

2.1.2.3 H-Bridge inverter

Figure 2.4 shows a schematic construction of a single phase H-bridge converter. These inverters have attracted a lot of interest due to their ability to scale up to higher voltages by simply cascading several units. Thus to construct a multilevel phase-leg, series of single-phase full-bridge inverters will be used, with separate *dc* sources [37]. The bridge output voltage of the each unit has three values ($-\frac{1}{2}u_{dc}$, 0, $+\frac{1}{2}u_{dc}$), resulting in a staircase waveform.

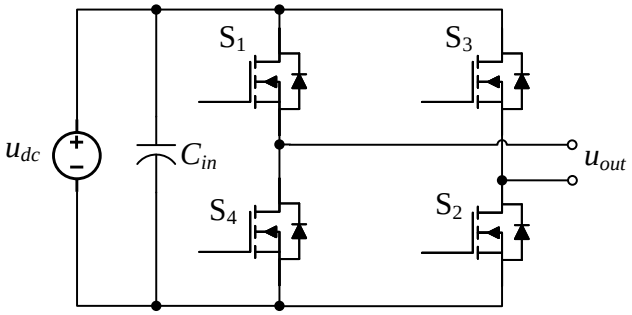


Figure 2.4: Phase-leg of the cascaded H-bridge (CHB) inverter.

Output is obtained by sequential control of the four switches S_1, S_2, S_3 and S_4. When S_1 and S_2 are switched *on*, the output is $+u_{dc}$; when S_3 and S_4 are switched *on*, the output is $-u_{dc}$; when either pair S_1, S_3 or S_2, S_4 are *on*, the output is 0. Addition of identical units in series would increase the output voltage levels. Although cascaded H-bridge inverter uses the least number of semiconductor devices when compared to other multi-level topologies, each unit requires a separate *dc* source and hence a large isolating transformer is required.

2.1.3 Siwakoti-H flying capacitor inverter (sFCI)

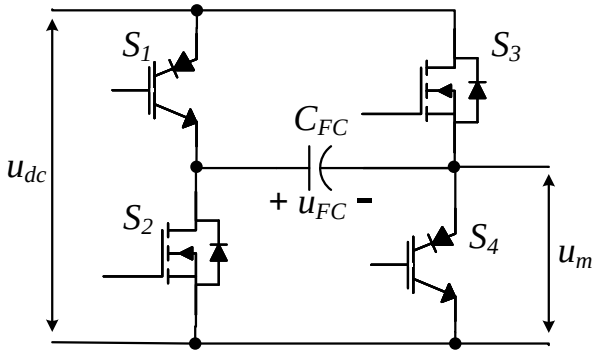


Figure 2.5: Phase leg of the Siwakoti-H inverter.

The sFCI is based on the topology proposed in [3, 13]. It is a common-ground-type transformerless inverter that works on the principle of a flying capacitor and has only four active switching elements, shown in Figure 2.5. The uniqueness of this topology is that, the negative voltage bus, required for the negative cycle, is fulfilled by using only a single input *dc* supply. This is achieved by the cyclic charging and discharging of the flying capacitor thus creating a virtual negative *dc*-link, as illustrated in Figure 2.6. Since the neutral of the grid can be directly connected to the negative pole of the *dc*-link, leakage current is automatically eliminated [37]. Phase leg of the three-level sFCI includes four power switches and one capacitor, as depicted in the Figure 2.5. Among the four switches, S_1 and S_4 are devices with bipolar voltage blocking capability whereas switches S_2 and S_3 are unipolar voltage devices. Therefore, the switches S_2 and S_3 are realized using a MOSFET while S_1 and S_4 are realized using a reverse blocking IGBT (RB-IGBT).

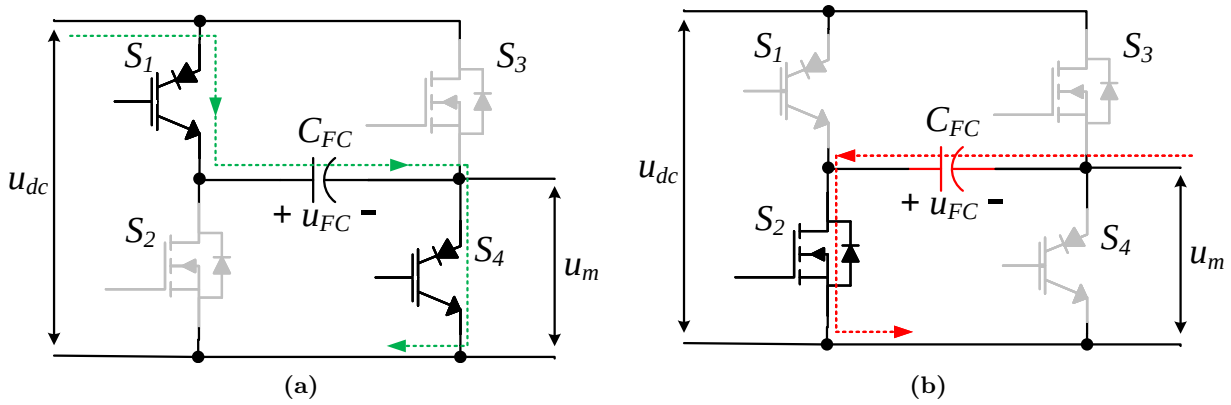


Figure 2.6: (a) Charging cycle of the flying capacitor, (b) discharging cycle of the flying capacitor where it acts as a virtual *dc*-link.

2.2 Control schemes

Figure 2.7 presents a classification of the control strategies used in grid-connected power electronic systems. As can be observed, the control of converters can be broadly classified into conventional and advanced strategies.

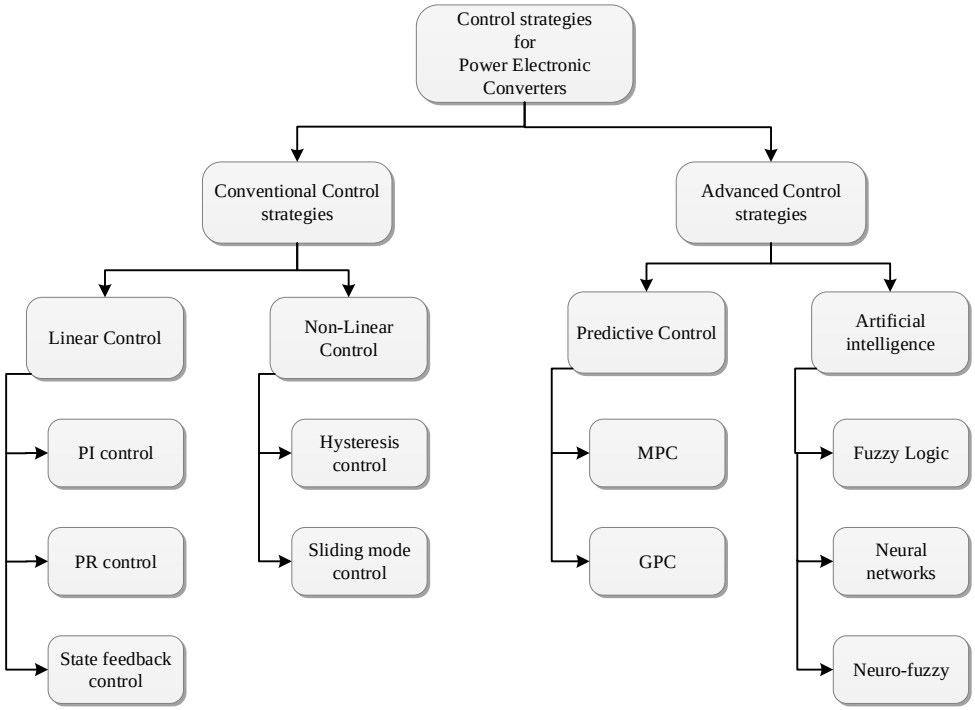


Figure 2.7: Control methods for grid-connected converters [38].

Among the linear control techniques, PI based Voltage Oriented Control (VOC) is very common as its implementation is simple and gives satisfactory steady-state performance. The non-linear behavior of the power converter is approximated to be linear for small time instants and hence a modulator can be employed for PWM generation [39]. A PWM modulator compares a sinusoidal reference signal to a triangular carrier signal, generating a pulsed waveform for switching the devices. In this fashion the inverter can operate between different states and hence generate voltages as desired.

Since the dynamic performance of the VOC is quite slow, it is not preferred in practical systems. On the contrary, state feedback control (SFC) has attracted a lot of attention and has many applications in grid connected systems [21–24]. It has superior dynamic performance compared to PI control and better steady state performance. However, the drawback of applying linear schemes to control non-linear systems is that they can produce uneven performance throughout the dynamic range. With linear controller design, the various system constraints and requirements (like the maximum current and switching frequency or total harmonic distortion) cannot be directly incorporated [39].

Non-linear techniques have several advantages over their linear counterparts. In particular, Model Predictive Control is a technique which can control multiple conflicting objectives and allows to incorporate system constraints as well. With predictive control the cascaded structure, found in linear schemes, can be avoided so as to produce very fast transient responses [39].

2.3 State feedback control

Grid-connected converters offer uni/bi-directional power transfer with low current distortion. Grid codes set stringent limits on the grid current THD, which can be divided into two parts. The first issue is related to low frequency harmonics due to grid voltage background distortion. This is connected to the disturbance rejection capability of the current controller [23, 40]. High control bandwidth is required for good harmonic rejection. The second issue of grid current harmonic distortion is related to harmonics at the switching frequency of the converter. LCL filters are increasingly used for mitigation of switching harmonics due to the superior filtering characteristic above their resonant frequency [23].

For damping the resonant behavior of the LCL filter, active damping is usually preferred as it is more flexible and efficient compared to passive damping. However, as the LCL resonance dynamics get closer to the desired control bandwidth, it becomes difficult to simultaneously achieve resonance damping and high bandwidth with reasonable robustness [22]. State Feedback Control[1] (SFC) [21–24, 41–43] enables high dynamic performance of a converter, connected to the grid via an LCL filter. With SFC, the dominant and resonant dynamics can be simultaneously set according to desired specifications and provide a convenient way for resonance damping [21].

In State Feedback Control, the closed loop poles can be placed using different approaches : 1) dead-beat control; 2) using Bessel Functions; 3) optimizing a cost function as in linear quadratic (LQ) control; 4) selecting the desired pole locations directly [21]. LQ control is very attractive for design of a controller when dealing with very complex systems, because it provides an indirect method for optimal pole placement. However, solution of the Riccati equation and selection of the cost-function weights is a tedious process [21]. A simpler alternative to LQ control is direct pole placement (see [21–23]) where the controller gains can be expressed using the parameters of the system and dynamic performance specifications (i.e., the bandwidth of current controller and the resonance damping of the LCL filter) [21].

The idea of pole placement is to specify the closed-loop performance in terms of pole and zero locations. The control parameters can be tuned to achieve the specified locations. Although parameter calculation is straightforward, proper specification of closed-loop poles and zeros is necessary [22]. In the following section a general solution for state-space system is derived and the criteria for controllability is deduced.

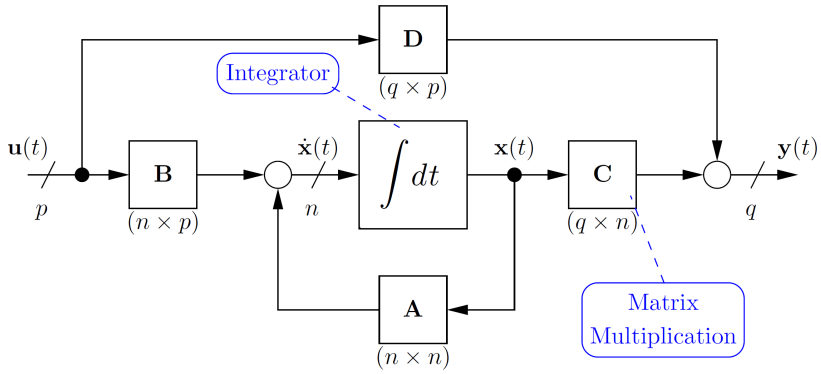
[1] In literature it is also called State Space Control.

2.3.1 Solution of the state space system

The dynamics of a linear time invariant (LTI) system can be represented using ordinary differential equations (ODE). A general LTI system in state space can be written as

$$\dot{\boldsymbol{x}}(t) = \mathbf{A}\boldsymbol{x}(t) + \mathbf{B}\boldsymbol{u}(t) \tag{2.1a}$$
$$\boldsymbol{y}(t) = \mathbf{C}\boldsymbol{x}(t) + \mathbf{D}\boldsymbol{u}(t) \tag{2.1b}$$

For the given LTI system, the state vector $\boldsymbol{x} \in \mathbb{R}^n$ has dimension n, the input vector $\boldsymbol{u} \in \mathbb{R}^p$ has dimension p and the output vector $\boldsymbol{y} \in \mathbb{R}^q$ has dimension q. Therefore, the state space matrices have dimension: $\mathbf{A} \in \mathbb{R}^{n\times n}$, $\mathbf{B} \in \mathbb{R}^{n\times p}$, $\mathbf{C} \in \mathbb{R}^{q\times n}$ and $\mathbf{D} \in \mathbb{R}^{q\times p}$. This set of equations including the dimensions of vectors and matrices is drawn in the following block diagram [44].



Let us consider the complete response of a linear system of first-order to an input $\boldsymbol{u}(t)$. The state equation $\dot{x} = ax + bu$ can be written in the form [45]

$$\dot{x}(t) - ax(t) = bu(t). \tag{2.2}$$

If both sides are multiplied by an integrating factor e^{-at}, the left-hand side becomes a perfect differential

$$e^{-at}\dot{x} - e^{-at}ax = \frac{d}{dt}\left(e^{-at}x(t)\right) = e^{-at}bu \tag{2.3}$$

which can be integrated directly to give

$$\int_0^t \frac{d}{d\tau}\left(e^{-a\tau}x(\tau)\right)d\tau = e^{-at}x(t) - x(0) = \int_0^t e^{-a\tau}bu(\tau)d\tau \tag{2.4}$$

and rearranged to give the state variable response explicitly:

$$x(t) = e^{at}x(0) + \int_0^t e^{-a(t-\tau)}bu(\tau)d\tau \tag{2.5}$$

The development of the expression for the response of higher order systems may be performed in a similar manner using the matrix exponential $e^{-\mathbf{A}t}$ as an integrating factor [45]. Matrix differentiation and integration are defined to be element by element operations, therefore if the state equation $\dot{\boldsymbol{x}}(t) = \mathbf{A}\boldsymbol{x}(t) + \mathbf{B}\boldsymbol{u}(t)$ is rearranged, and all terms pre-multiplied by the square matrix $e^{-\mathbf{A}t}$, we get:

$$e^{-\mathbf{A}t}\dot{\boldsymbol{x}}(t) - e^{-\mathbf{A}t}\mathbf{A}\boldsymbol{x}(t) = \frac{d}{dt}\left(e^{-\mathbf{A}t}\boldsymbol{x}(t)\right) = e^{-\mathbf{A}t}\mathbf{B}\boldsymbol{u}(t). \tag{2.6}$$

Integration of (2.6) gives

$$\int_0^t \frac{d}{d\tau}\left(e^{-\mathbf{A}\tau}\boldsymbol{x}(\tau)\right)d\tau = e^{-\mathbf{A}t}\boldsymbol{x}(t) - e^{-\mathbf{A}0}\boldsymbol{x}(0) = \int_0^t e^{-\mathbf{A}\tau}\mathbf{B}\boldsymbol{u}(\tau)d\tau, \tag{2.7}$$

and because $e^{-\mathbf{A}0} = \mathbf{I}$ and $\left[e^{-\mathbf{A}t}\right]^{-1} = e^{\mathbf{A}t}$ the complete state space response may be written as

$$\boldsymbol{x}(t) = e^{-\mathbf{A}t}\boldsymbol{x}(0) + \int_0^t e^{\mathbf{A}(t-\tau)}\mathbf{B}\boldsymbol{u}(\tau)d\tau. \tag{2.8}$$

To design a controller for the LTI system, linearization of the ODE is carried out in order to consider the behavior of the system around a reference or steady-state point. Additionally, controllability of the system has to be checked to verify that a controller can actually be designed.

2.3.2 Controllability

A system is controllable, if in finite time t_f any initial state $\boldsymbol{x}(0)$ can be driven to any given final state $\boldsymbol{x}(t_f)$ by appropriate choice of the control signal $\boldsymbol{u}(t)$ for $0 \leq t \leq t_f$, depicted in Figure 2.8. Considering the solution (2.8) of the state space system (2.1), for $0 \leq t \leq t_f$ we get

$$\underbrace{\boldsymbol{x}(t_f) - e^{-\mathbf{A}t_f}\boldsymbol{x}(0)}_{:=-e^{-\mathbf{A}t_f}\boldsymbol{x}_i} = \int_0^{t_f} e^{\mathbf{A}(t_f-\tau)}\mathbf{B}\boldsymbol{u}(\tau)d\tau. \tag{2.9}$$

The value $\boldsymbol{x}_i$ is defined by setting the LHS equal to $-e^{-\mathbf{A}t_f}\boldsymbol{x}_i$. As the equation has to be valid for any $\boldsymbol{x}(t_f)$ and any $\boldsymbol{x}(0)$, the following equation has to hold for all $\boldsymbol{x}_i \in \mathbb{R}^n$ [44].

$$-e^{-\mathbf{A}t_f}\boldsymbol{x}_i = \int_0^{t_f} e^{\mathbf{A}(t_f-\tau)}\mathbf{B}\boldsymbol{u}(\tau)d\tau. \tag{2.10}$$

The system is controllable, if for any $\boldsymbol{x}_i \in \mathbb{R}^n$, a finite t_f and a control input $\boldsymbol{u}(t)$ for $0 \leq t \leq t_f$ can be found, such that (2.10) holds. In other words: by appropriate choice of $\boldsymbol{u}(t)$, the system can be driven from any initial state $\boldsymbol{x}_i$ to the zero state in finite time t_f [44].

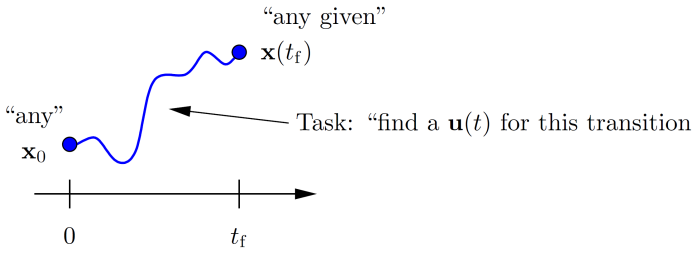


Figure 2.8: Driving a state $\boldsymbol{x}(0)$ to $\boldsymbol{x}(t_f)$ [44].

2.3.3 Kalman's controllability criterion

Consider (2.10) for a single-input single-output (SISO) system

$$-e^{-\mathbf{A}t_f}\boldsymbol{x}_i = \int_0^{t_f} e^{\mathbf{A}(t_f-\tau)}\mathbf{b}u(\tau)d\tau. \tag{2.11}$$

Using the definition of the matrix exponential we can write

$$\begin{aligned} -\boldsymbol{x}_i &= \int_0^{t_f} e^{\mathbf{A}(\tau)}\mathbf{b}u(\tau)d\tau = \int_0^{t_f} \left(\sum_{\nu=0}^{\infty} \frac{(-\mathbf{A})^\nu \tau^\nu}{\nu!}\right)\mathbf{b}u(\tau)d\tau \\ &= \sum_{\nu=0}^{\infty} \mathbf{A}^\nu \mathbf{b} \underbrace{\int_0^{t_f} \frac{(-1)^\nu \tau^\nu}{\nu!}u(\tau)d\tau}_{:=u_\nu} \end{aligned} \tag{2.12}$$

Thus we get for $\boldsymbol{x}_i$

$$\boldsymbol{x}_i = -\sum_{\nu=0}^{\infty} \mathbf{A}^{\nu}\mathbf{b}u_{\nu} \tag{2.13}$$

Hence for controllability, an arbitrary value $\boldsymbol{x}_i$ should be representable as a linear combination of the column vectors

$$\mathbf{b}, \mathbf{Ab}, \mathbf{A}^2\mathbf{b}, \ldots$$

As a consequence, the matrix composed of these n column vectors is called the controllability matrix $\mathbf{M}_c$ and it must have a rank $= n$ [45].

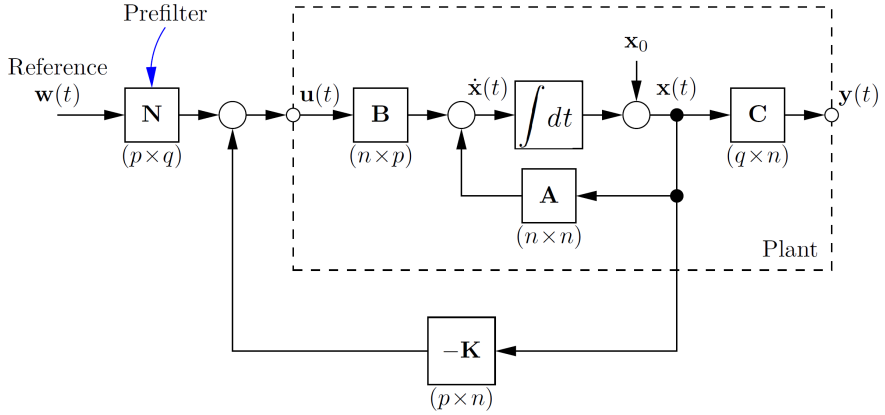
$$\mathbf{M}_c = \left[\mathbf{b}, \mathbf{Ab}, \mathbf{A}^2\mathbf{b}, \ldots, \mathbf{A}^{n-1}\mathbf{b}\right] \tag{2.14}$$

For MIMO systems the Kalman Controllability Criteria states: The LTI system $(\mathbf{A};\mathbf{B};\mathbf{C})$ is controllable if and only if the controllability matrix $\mathbf{M}_c$ has full rank $= n$, where

$$\mathbf{M}_c = \left[\mathbf{B}, \mathbf{AB}, \mathbf{A}^2\mathbf{B}, \ldots, \mathbf{A}^{n-1}\mathbf{B}\right] \tag{2.15}$$

2.3.4 State feedback

Once it is determined that the system (2.1) is controllable, assuming $\mathbf{D} = 0$, a feedback can be added to the system as shown below,



The state feedback controller is defined by

$$\boldsymbol{u}(t) = -\mathbf{K}\boldsymbol{x}(t) \tag{2.16}$$

Substituting (2.16) into the state ODE $\dot{\boldsymbol{x}}(t) = \mathbf{A}\boldsymbol{x}(t) + \mathbf{B}\boldsymbol{u}(t)$ yields the feedback system

$$\dot{\boldsymbol{x}}(t) = (\mathbf{A} - \mathbf{BK})\boldsymbol{x}(t) \tag{2.17}$$

The control design has two objectives:

- Design $\mathbf{K}$ such that the state space control loop is stable.
  $\Updownarrow$
  $(\mathbf{A} - \mathbf{BK})$ is stable, i.e., all its eigenvalues have negative real parts.
- Design a prefilter $\mathbf{N}$ such that for a reference input $\boldsymbol{w}$, the output vector $\boldsymbol{y}(t) \to \boldsymbol{w}$ for $t \to \infty$.
  $\Updownarrow$
  The control law becomes $\boldsymbol{u}(t) = -\mathbf{K}\boldsymbol{x}(t) + \mathbf{N}\boldsymbol{w}$

2.4 Model predictive control

Power electronic converters are inherently non-linear due to the switching nature of the semiconductor devices. Moreover, a converter system has operational restrictions such as limits on the voltage and current stress of the switches, and protective operation limits of associated components. Thus linear control techniques cannot capture all the associated dynamics of these non-linear systems. Since linearization of the system is carried out around a specific operating point for linear control design, the system behavior might deviate at a different operating point. In order to improve the performance of the controlled system and achieve higher efficiencies, the true nature of the power converter and its characteristics must be taken into consideration. Additionally, the discrete nature of the semiconductor switches must also be considered.

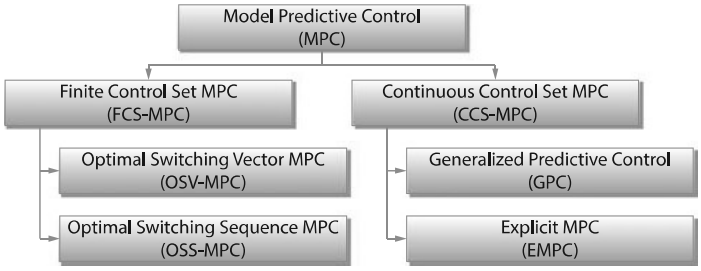


Figure 2.9: Classification of MPC strategies applied to power electronics and drives [28].

Among the control strategies adopted in power electronics, model predictive control (MPC) has gained a lot of popularity due to its various advantages including the ability to easily handle system constraints and non-linearities. MPC has been shown to outperform traditional control methods because of its easy handling of system constraints that are imposed by defining the control problem as a constrained optimization problem [46]. With the advancement in microprocessors, the computational abilities of control platforms has seen a steep improvement over the years, making it possible to implement computationally demanding algorithms like MPC [39]. MPC is an advanced control method that relies on the system model to predict its future behavior. Using the future predictions, the controller decides a sequence of appropriate control actions based on a predefined optimization criteria [27]. For example, optimization criterion for hysteresis-based predictive control requires the actuation to maintain the controlled variable within the defined hysteresis bounds around the reference signal [47]. On the contrary MPC can incorporate flexible criteria as all the control objectives can be tackled in a single performance criterion, i.e., the cost function [28]. The easy handling of system constraints and non-linearities eliminates the need for linearization, and therefore the system does not have any restrictions w.r.t operation points.

Figure 2.9 shows the most common MPC techniques used for power converters and drives. Table 2.2 summarizes the main features of the different MPC techniques.

2.4.1 MPC: Operating principle

The prerequisite for designing a predictive controller is the model of the system to be controlled. MPC uses this model to predict the future behavior of the state variables of the system. Based on the predicted states and other system constraints, minimization of a cost function is carried out that describes the desired system behavior [39]. In general, the cost function is based on the error between the predicted output with the reference values. The MPC controller computes a set of optimal switching sequences based on the minimal cost and these sequences act as the firing signals for the semiconductor switches. Although, for each sampling period, a set of switching sequences that minimizes the cost function is calculated, only the first element of the switching sequence is

Parameter	GPC	EMPC	OSV-MPC	OSS-MPC
Modulator	PWM	PWM	Not required	Not required
Fixed switching frequency	Yes	Yes	No	Yes
Optimization	Online	Offline	Online	Online
Constraints	Can be included but increases the computational cost	Yes	Yes	Yes
Long prediction horizon	Yes	Yes	Can be used	Can be used
Formulation	Complex	Complex	Very intuitive	Intuitive

Table 2.2: MPC techniques used in power electronics [28].

applied. Moreover, MPC controllers solve an open-loop optimal control problem where the MPC algorithm is repeated in a receding horizon fashion at every sampling instant, thus providing a feedback loop and potential robustness to system uncertainties [28]. Figure 2.10 shows a basic block diagram of the MPC strategy, where i^* denotes the reference current and $\hat{i}$ denotes the predicted current. Note that i^*, $\hat{i}$ at the time step $k+2$ are used instead of the time step k to compensate for the digital implementation delay [28, 48]. For detailed operation of this technique see [28, Sec. II].

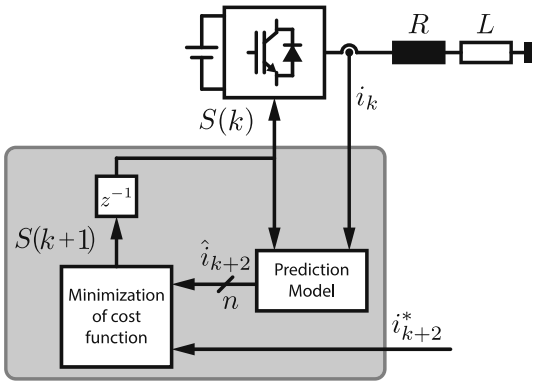


Figure 2.10: Block diagram of a basic MPC strategy applied for the current control in a VSI with output RL load [28].

As shown in Figure 2.9, MPC is broadly classified into two methods depending on the kind of optimization problem. Out of these methods, Continuous Control Set MPC (CCS-MPC) calculates a continuous control signal and employs a modulator to generate the desired switching signals. The main advantage of CCS-MPC is that it produces a fixed switching frequency [28].

Finite Control Set MPC (FCS-MPC) does not need a modulator as it utilizes the discrete nature of the power converter to formulate the MPC algorithm, and hence generates the switching signals directly. It uses a control set of output voltage vectors to calculate predictions, reducing the optimal problem to an enumerated search algorithm [28]. The main disadvantage is that FCS-MPC generates a variable switching frequency [39].

In general, MPC algorithms require a significant number of computations. CCS-MPC usually has a lower computational cost than FCS-MPC because it computes part or all of the optimization problem offline. For this reason, CCS-MPC can address long prediction horizon problems. On the contrary, FCS-MPC requires that the optimization problem to be solved online. Since FCS-MPC involves a lot of calculations, it is usually limited to short prediction horizons in power electronic applications [28].

2.4.2 Prediction model

The dynamic evolution of a system can be described in the continuous time domain using a state-space model, described in section 2.3. Generally, the switching behavior of the power converter can be neglected and the mathematical model of the filter/grid system is sufficiently accurate for prediction purposes. Moreover, control algorithms like MPC are usually implemented using digital hardware platforms like FPGAs or DSPs. Hence the continuous time model of the system has to be discretized. For linear systems discretization can be carried by using the Forward Euler method or the Zero-Order-Hold method, although non-linear systems usually require a more complex approach (see for example [52, 53]). For a sampling time of T_s the discrete-time state space representation of the continuous time model (2.1) becomes

$$\boldsymbol{x}(k+1) = \mathbf{A}\boldsymbol{x}(k) + \mathbf{B}\boldsymbol{u}(k) \tag{2.18a}$$

$$\boldsymbol{y}(k) = \mathbf{C}\boldsymbol{x}(k) + \mathbf{D}\boldsymbol{u}(k) \tag{2.18b}$$

2.4.3 Constraints

Using semiconductor switches imposes certain restrictions or constraints on the controller and therefore, only a finite set of actuation options are allowed. In literature these restrictions are referred as *switching constraints*.

The control scheme CCS-MPC requires a modulator. The controller in this case generates the voltage reference for the modulator, which is restricted to a bounded continuous set, such as $\mathcal{S} = [-1, 1] \in \mathbb{R}$. On the contrary, the control scheme FCS-MPC directly generates the required switch positions of the converter, which is constrained to a finite set of integers. For example, a two-level converter (section 2.1.1) can synthesize two voltage levels per phase. This characteristic can be captured by the input constraint $\mathcal{S} = \{0, P\} \approx \{0, 1\}$. Similarly, for a three level converter (section 2.1.2) the input constraint can be captured by the discrete set $\mathcal{S} = \{N, 0, P\} \approx \{-1, 0, 1\}$. This kind of restrictions are known as "*hard*" constraints, as they cannot be relaxed [55].

In addition to this, restrictions can be imposed on the system states to prevent operation beyond the safe limits. For example, the upper constraint on the value of currents can be set to a value which is slightly less than the maximum allowed limit, in order to prevent damages due to over currents. This kind of restrictions are known as "*soft*" constraints [55].

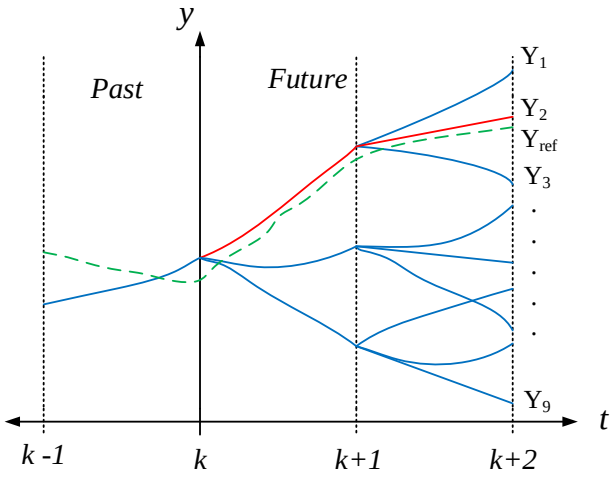
2.4.4 Prediction horizon

Based on the prediction model the controller makes predictions for a defined length of N_p time-steps, known as the prediction horizon. This generates a sequence of outputs $\mathbf{Y} = [\boldsymbol{y}^\top(k+1),\ \boldsymbol{y}^\top(k+2), \ldots,\ \boldsymbol{y}^\top(k+N_p))]^\top$. The controller is tasked to drive the system in such a manner that it follows a reference trajectory (denoted as $\mathbf{Y}_{\text{ref}}$) over the prediction horizon. In order to minimize the deviations from the reference trajectory an optimization criterion is evaluated at each time step, for all possible switching states (which fulfill the system constraints). This is accomplished using a cost function.

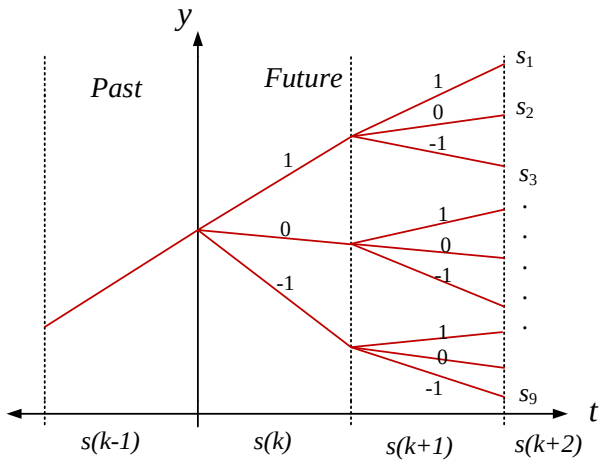
2.4.5 Cost function

The cost function in MPC is a measure to define the behavior of the system. The control objectives can be fulfilled using the cost function, which can incorporate the different system states, outputs, and constraints into a scalar cost. It can be complex depending on which variables and control objectives are considered. The cost function facilitates a comparison between the predicted and the reference values [55]. A general definition of the cost function is

$$J = \sum_{l=k}^{k+N_p-1} (\boldsymbol{y}(l) - \boldsymbol{y}_{\text{ref}}(l))^\top \mathbf{Q} (\boldsymbol{y}(l) - \boldsymbol{y}_{\text{ref}}(l)) + \sum_{r=k}^{k+N_c-1} (\boldsymbol{s}(r))^\top \mathbf{R}\, \boldsymbol{s}(r) \tag{2.19}$$



(a) Trajectories of predicted current $\mathbf{Y}$, the reference trajectory $\mathbf{Y}_{\text{ref}}$ (green dotted), and minimum cost trajectory (red).



(b) Corresponding candidate switching sequences.

Figure 2.11: Typical operation of FCS-MPC for a three level inverter.

where $\boldsymbol{y}(l)$ is a vector containing the predicted outputs, and $\boldsymbol{y}_{\text{ref}}(l)$ is a vector containing the reference values at the instant l, $\boldsymbol{s}(r)$ is the input vector at the instant r, N_p and N_c are the prediction and control horizons, respectively [28,56]. $\mathbf{Q}$ and $\mathbf{R}$ are matrices containing the weighting factors. Choice of the weighting factors and the states that are controlled impact the system's performance and stability. Therefore, it is a matter of tuning and requires some trial and error. To summarize, the cost function uses the difference vector $\Delta\boldsymbol{y}(l) = (\boldsymbol{y}(l) - \boldsymbol{y}_{\text{ref}}(l))$ and the sequence of manipulated variables (switching states that fulfill the system constraints)[2]

$$\mathbf{S}(k) = [\boldsymbol{s}^\top(k),\ \boldsymbol{s}^\top(k+1), \ldots,\ \boldsymbol{s}^\top(k+N_c-1)]^\top \tag{2.20}$$

as arguments. Based on these two arguments, the future states and controlled variables can be predicted over the prediction horizon using the prediction model [55].

A typical example of a cost function where the matrices $\mathbf{Q}$ and $\mathbf{R}$ are diagonal, can be written as

$$J = \sum_{l=k}^{k+N_p-1} (\lambda_e J_e(l) + \lambda_s J_s(l)) \tag{2.21}$$

For FCS-MPC, the controller does not need an external modulator and can therefore directly generate the set of optimal switching positions to be applied at the time instant $k+1$. The cost function J is evaluated for all the candidate switching sequences $\mathbf{S}(k)$ over the prediction horizon N_p, and the set that corresponds to minimum cost is selected as the optimal switching sequence $\boldsymbol{s}_{opt}(k)$. The first term J_e corresponds to minimization of the reference tracking error, penalized by the weighting factor λ_e. The second term is J_s with a weighting factor λ_s, is related to penalization of the switchings for the power converter, which indirectly corresponds to reduction of switching frequency [47]. Considering a three level inverter where the controller has to decide between three discrete possibilities $\{-1, 0, 1\}$, evolution of predicted trajectories and corresponding switching sequences is presented in Figure 2.11.

[2] In literature these are also known as candidate switching sequences.

2.4.6 Receding horizon policy

The solution to the optimization problem at time step k, generates a sequence of manipulated variables $\mathbf{S}_{opt}$ from time step k to $k + N_p - 1$. To provide feedback, only the first element of this sequence, namely $\boldsymbol{s}_{opt}(k)$, is applied to the system. At the next time step $k+1$, a new state estimate is obtained and the optimization problem is solved again over the shifted horizon from $k + 1$ to $k + N_p$. This policy is known as receding horizon control [55].

2.5 Summary

In this chapter, different VSI topologies were discussed. Additionally, sFCI was introduced as an attractive alternative to conventional topologies, for PV applications. sFCI has a lot of potential for application in the PV field because it uses less number of switches and smaller additional components. Further, the basics and working principles of famous control techniques SFC and MPC were discussed. SFC and MPC are quite popular for grid connected applications. SFC, with its straightforward design can be used for control of linearized systems. On the other hand, MPC has a lot of potential to control non-linear and constrained systems. In this thesis an attempt is made to analyse the sFCI topology and design a closed loop for grid connected operation.

Chapter 3

Siwakoti-H Topology: Analysis and System Modeling

This chapter discusses the working of Siwakoti-H Flying Capacitor Inverter (sFCI). The design of the three level sFCI topology, it's working in different modes, various switching states will be discussed and the additional non-linearities present in the topology will be analysed. Furthermore, open-loop behavior of the sFCI in conjunction with an LCL filter will be presented. Finally, a continuous-time model of the inverter will be derived.

3.1 Novel flying capacitor topology

The sFCI was presented briefly in section 2.1.3, and is based on the topology proposed in [3,13]. Due to its novel nature, the Siwakoti-H flying capacitor inverter (sFCI) presents an interesting problem for analysis and system modeling. In particular, the behavior of the flying capacitor and its interaction with the LCL filter adds to the problem at hand. This topology is similar to a conventional T-type (3 level NPC) inverter, where it only uses four active switches; two of them with unipolar voltage blocking capability and two with bipolar voltage blocking capability [3]. However, the *dc*-link voltage requirement of this topology is only half of that required in NPC converter [32], or ANPC [57]. This reduces the front-end voltage boost requirement and associated circuitry, which helps in improving the efficiency and size of the system. In addition, it also reduces the size and number of passive component (capacitor) requirements.

Figure 3.1 illustrates a single phase sFCI with an LCL filter connected to a resistive load. It

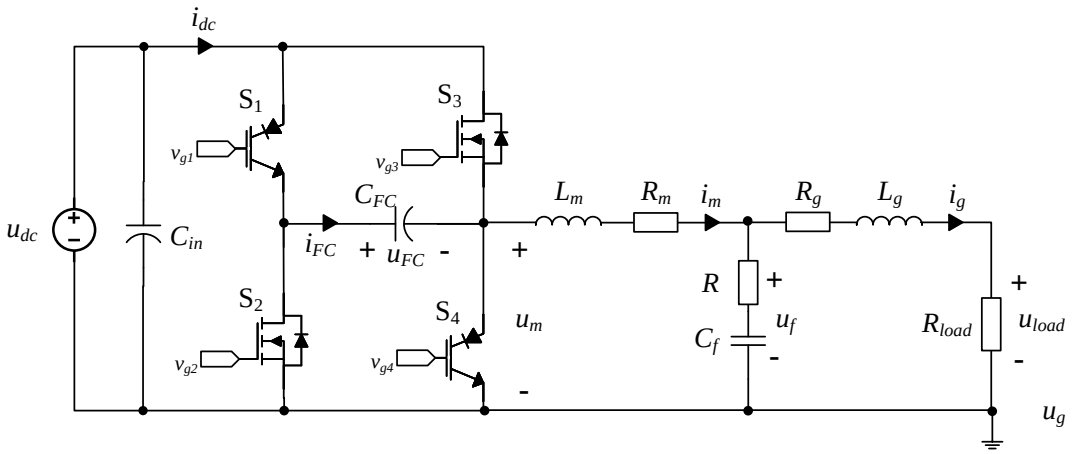


Figure 3.1: Single-phase sFCI with LCL filter, resistive load and various measurements.

Parameter	Symbol	Value
Nominal power (base power)	P_n	5 kVA
Converter side inductance	L_m	400 µH
Converter side resistance	R_m	50 mΩ
Grid side inductance	L_g	56 µH
Grid side resistance	R_g	30 mΩ
Filter Capacitance	C_f	5 µF
ESR of filter capacitor	R	7.4 mΩ
Flying Capacitor	C_{FC}	680 µF
DC link voltage	u_{dc}	400 V
Load Resistor	R_{load}	31.7 Ω

Table 3.1: System parameters from hardware test bench.

consists of a *dc*-link with a constant voltage $u_{dc} > 0$ which can be supplied from a renewable energy resource like PV. The LCL-filter consists of main inductor[1] and grid-side inductor, L_m and L_g, with internal resistances R_m and R_g respectively, and the filter capacitance C_f with electrostatic resistance (ESR) R. The hardware test-bench design of the converter and associated components was carried out in [37]. The various system parameters of the hardware test-bench are detailed in Table 3.1. For further analysis and simulations the same parameters will be utilized.

3.1.1 Description of the Siwakoti-H topology

The single phase of the sFCI, see Figure 3.1, consists of four active switching elements, $S_1 - S_4$, and a flying capacitor C_{FC}. Among the four switches, S_1 and S_4 are devices with bipolar voltage blocking capability whereas switches S_2 and S_3 are unipolar voltage devices. Hence, the switches S_2 and S_3 are realized using a MOSFET while S_1 and S_4 are realized using a reverse blocking IGBT (RB-IGBT). A RB-IGBT is a series combination of a normal IGBT and a power diode, depicted in Figure 3.2(a). It only conducts in the forward direction when the gating signal is supplied and the series diode is forward biased. Moreover, due to the presence of the series diode, RB-IGBT offers bidirectional voltage blocking capability.

In this topology, only one switch carries the load current during the positive or the negative cycle. Switch S_3 conducts the load current during the positive cycle and creates a positive operation state. Switch S_2 conducts the load current during the negative cycle and creates a negative operation state. When switches S_1 and S_4 are turned *on*, charging of the flying capacitor C_{FC} takes place, giving rise to the zero state. C_{FC} is continuously charged in both the positive and negative cycles. The inverter is modulated using a standard unipolar sinusoidal PWM (SPWM), where S_1 and S_4 experience high frequency switching in both positive and negative cycles for charging C_{FC}. The reduction in the number of active and passive components and a simple modulation technique makes this topology very versatile and useful for applications which require common bus bar configurations (positive or negative) [3].

3.1.2 Operating principle of the Siwakoti-H topology

The sFCI is a common ground type transformerless inverter that works on the principle of a flying capacitor. Figure 3.2(b) illustrates the the charging and discharging process of the flying capacitor to create a negative supply voltage for the inverter, during the negative cycle. When the switches are in position 1, the flying capacitor C_{FC} connects to the input voltage and charges up to the input voltage. However, when the switches turn to position 2, a negative voltage, with magnitude approximately

[1] also referred as converter-side inductor.

equal to input voltage, appear at the output side. The process is continuously repeated at a high switching frequency to maintain a desired voltage across the output port [3].

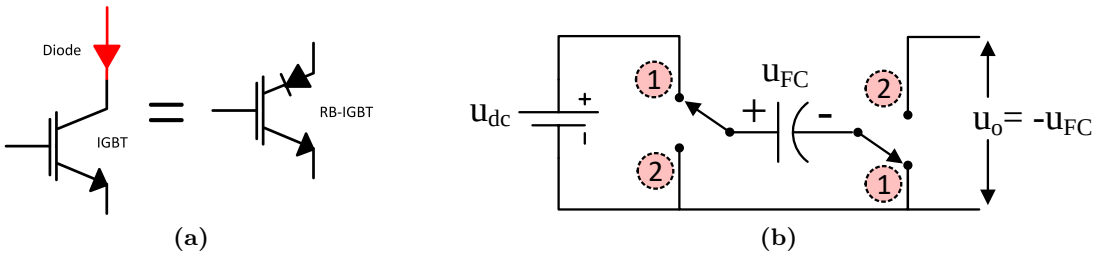


Figure 3.2: (a) Realization of a reverse blocking IGBT (RB-IGBT). (b) Illustration of the charging and discharging of the flying capacitor (C_{FC}) to create a negative bus voltage in the inverter during the negative cycle [3].

3.1.3 Operating modes (states) of the Siwakoti-H topology

This topology has three modes of operation, i.e., positive active (P), negative active (N) and zero state (O). The zero state is common in both positive and negative cycles, e.g., in positive cycle, the switching sequence is POPO and in negative cycle, the switching sequence is NONO [3]. Figure 3.3 shows the different switching states of the topology and paths of current flow (red-dotted line represents the active current path, blue-dotted line represents the reactive current path, and green-dotted line represents the charging current path for C_{FC}). Switching table of the single phase sFCI is shown in Table 3.2.

States	**Notation**	S_1	S_2	S_3	S_4	**Bridge Output**
Positive state	P	0	0	1	0	$+u_{dc}$
Negative state	N	0	1	0	0	$-u_{FC}$
Zero state	O	1	0	0	1	0

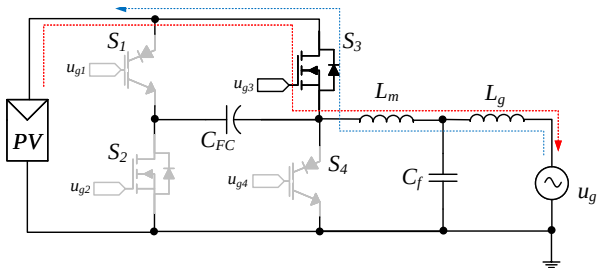
Table 3.2: Switching table of the sFCI.

3.1.3.1 Positive state (active)

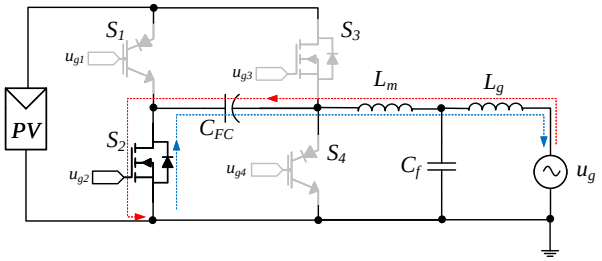
During this state the positive modulating signal is compared with a triangular carrier wave to create switching pulses for the switch S_3, which creates a unipolar positive voltage u_m at the output of the converter bridge. Switches S_1 and S_4 are *off* during this state, while the switch S_2 is *off* for the complete positive cycle. Since a MOSFET is used for the switch S_3, the circuit has capability to conduct reactive current via the reverse diode, thus offering reactive power support. It should be noted that power in this state is completely supplied from the input *dc* supply. Figure 3.3(a) gives a clear picture of the positive state.

3.1.3.2 Negative state (active)

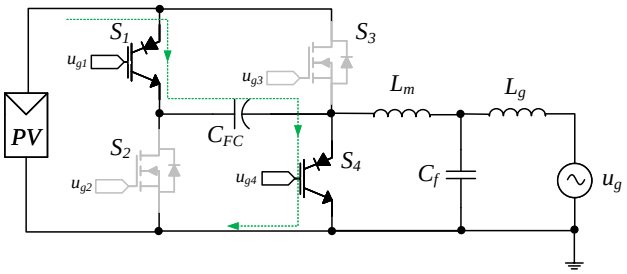
During this state the negative modulating signal is compared with a triangular carrier wave to create switching pulses for the switch S_2. The Flying Capacitor acts as a virtual *dc*-link for the inverter during this operation state, and creates a negative unipolar voltage u_m at the output of the converter bridge. Switches S_1 and S_4 are *off* during this state, while the switch S_3 is *off* for the



(a) Positive State.



(b) Negative State.



(c) Zero State.

Figure 3.3: Schematic overview of the three operation states and with respective paths for the current flows (red: active current path, blue: reactive current path, green: C_{FC} charging current path).

complete negative cycle. This state can also allow reactive power flow via the reverse diode of S_2. Figure 3.3(b) gives a clear picture of the negative state.

3.1.3.3 Zero state

This state exists in both the positive and negative cycles. The main purpose of this state is to continuously charge the flying capacitor C_{FC} and maintain the voltage across C_{FC} around the input *dc*-link voltage ($\approx 400\,\mathrm{V}$). The flying capacitor is designed to sustain a ripple voltage ($\delta_{FC} = max(u_{FC}) - min(u_{FC})$), where the voltage u_{FC} is restricted by a maximum limit of 450 V. Zero state follows the active states, where both the switches S_1 and S_4 are turned *on*. Charging of the capacitor in both positive and negative cycles helps in reducing the size of the capacitor with the switching frequency, see Figure 3.3(c).

3.2 Analysis of sFCI behavior in open-loop

In order to design the closed loop controller, a model of the system under consideration must be derived. Conventional topologies like NPC, ML-FCI and H-bridge have been extensively studied in literature and mathematical models are readily available [32–34, 36]. However, sFCI is a novel topology and has been recently designed [3, 13, 37]. Hence, a detailed analysis of the working modes and system responses is necessary to understand the behavior. In the following discussion, analysis of the open-loop response of three-level sFCI (3L-sFCI) is undertaken and comparison to a three-level NPC (3L-NPC) converter is carried out to highlight the differences and additional non-linearities.

3.2.1 Open-loop response

Using the parameters give in Table 3.1 the open-loop system is simulated, in standalone version of PLECS ®, for a resistive load R_{load}. A unipolar sinusoidal PWM (SPWM) with a carrier frequency of 40kHz is employed to generate the switching signals for the four switches, see Figure 3.4.

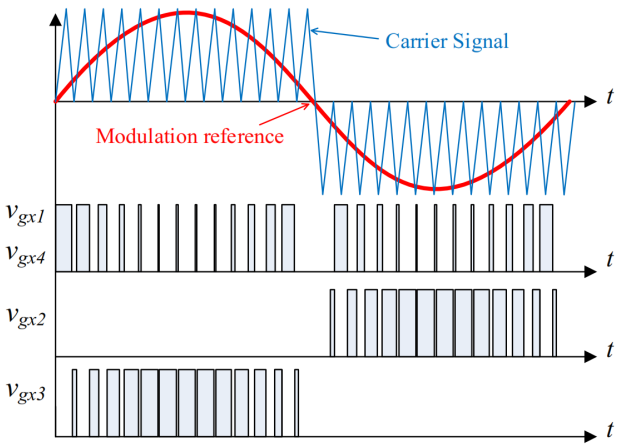
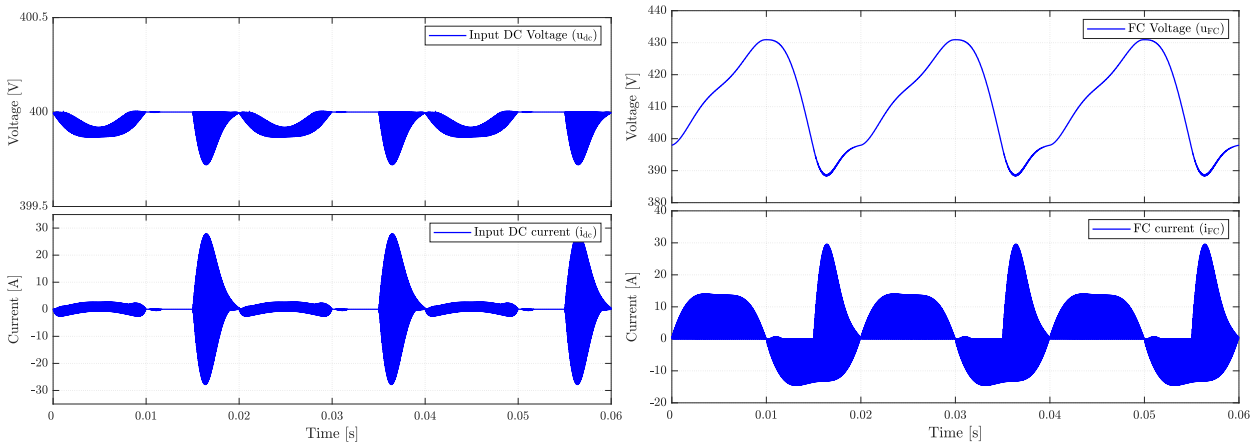


Figure 3.4: SPWM strategy for generation of gating signals [37].

Figures 3.5 and 3.6 show the response of the sFCI equipped with an LCL filter and connected to a resistive load of 31.7 Ω. Figure 3.5 shows a comparison between the voltage and current waveforms of the two *dc*-links (u_{dc} and u_{FC}). Unlike a three-level NPC converter where the two input capacitors are coupled and dependent on each other, it can be concluded that the input capacitor C_{in} and the flying capacitor C_{FC} do not have any specific coupling, although C_{FC} is charged by the energy supplied by C_{in}. Figure 3.6(a) shows the bridge voltage at the output of the converter and the filtered voltage across the load. Figure 3.6(b) shows the three states of the LCL filter. Comparing the main inductor current (red) and grid side current (blue) we can conclude that the LCL filter offers very good attenuation of switching frequency harmonics and filters out the current ripple.

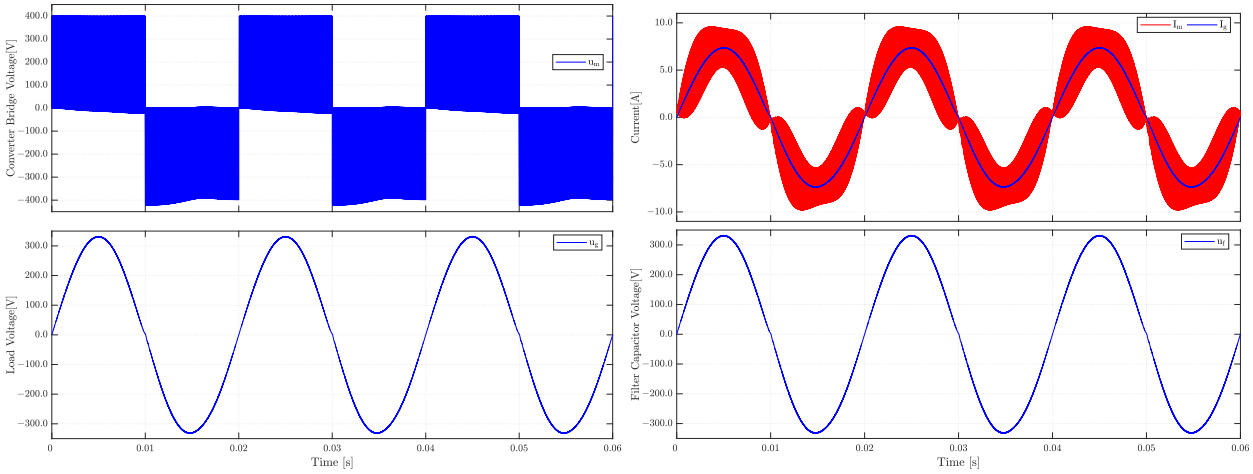


(a) Input DC link. **(b)** Flying Capacitor.

Figure 3.5: Voltage and current waveforms of (a) the input *dc* supply and (b) the flying capacitor.

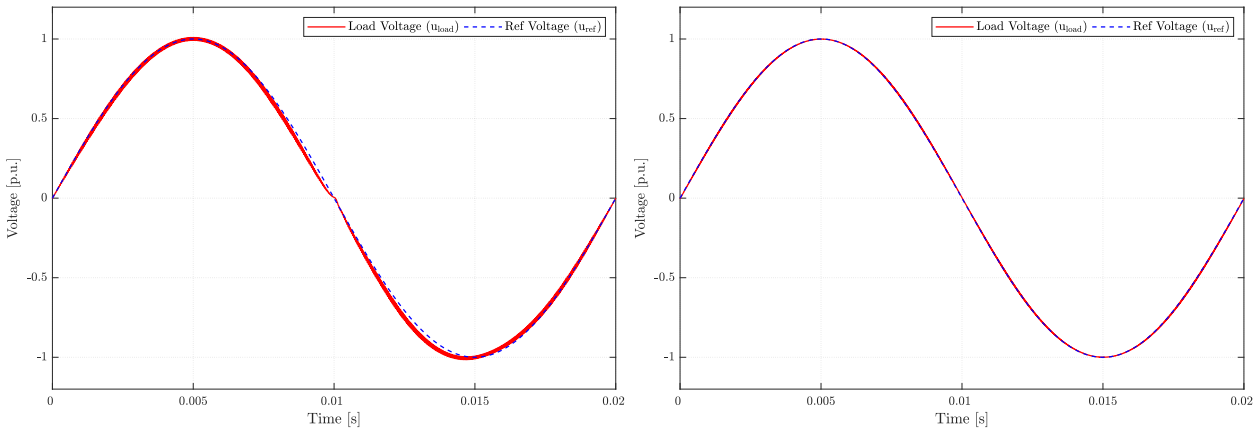
3.2.2 Open-loop voltage comparison

Figure 3.7 shows the voltage comparison in per unit (p.u.) form. Each plot consists of the load voltage u_{load} (red color) and the sinusoidal PWM reference u_{ref} (blue color). Compared to the NPC which has a sinusoidal response for the load current, sFCI does not appear to give a purely sinusoidal response as there is quite visible deviation compared to the reference voltage. Particularly, the deviation is prominent in the negative half cycle. To understand this behavior further, investigation of the converter bridge voltage provides more insight.



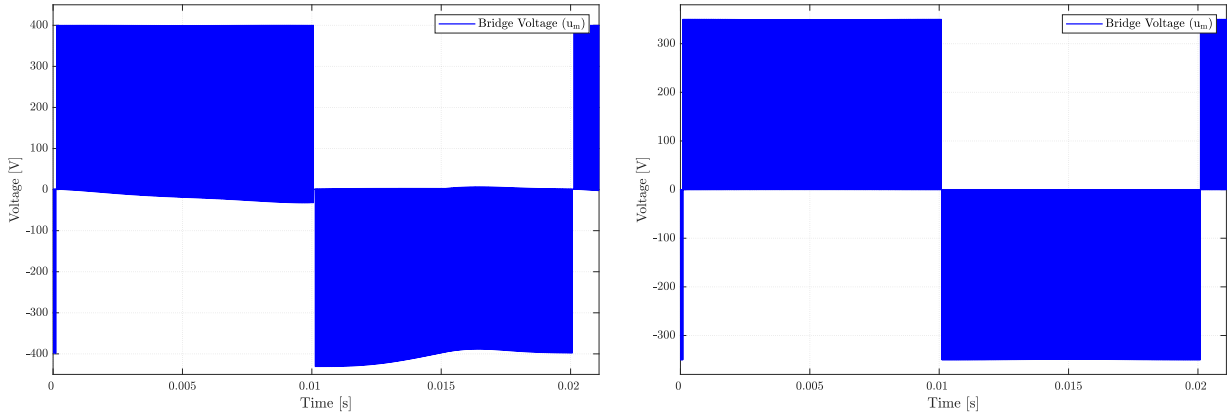
(a) **(b)**

Figure 3.6: (a) Voltage across the converter bridge and the load and (b) measurements of the states of the LCL filter.



(a) 3L-sFCI. **(b)** 3L-NPC converter.

Figure 3.7: Comparison of load voltages during open-loop operation



(a) 3L-sFCI. **(b)** 3L-NPC converter.

Figure 3.8: Comparison of the output voltage u_m of the converter bridge.

Figure 3.8 shows a comparison between the bridge voltages u_m of the sFCI and NPC converter. During the positive cycle, the sFCI has an input *dc* voltage of 400 V and hence the voltage across the bridge is $\approx u_{dc}$. However, for the negative cycle flying capacitor acts as the *dc* supply and supplies the load. In Figure 3.5(b) it was observed that the flying capacitor has a voltage ripple $\delta_{FC} \approx 40$ V, and it discharges continuously during the negative state. This slow decrease in the voltage of the flying capacitor is visible at the bridge output and hence responsible for distorted voltage output. On the contrary, the bridge voltage output of the NPC is sinusoidal and has minimal distortions, because the input *dc* supply is reasonably constant.

3.2.3 Bridge voltage analysis

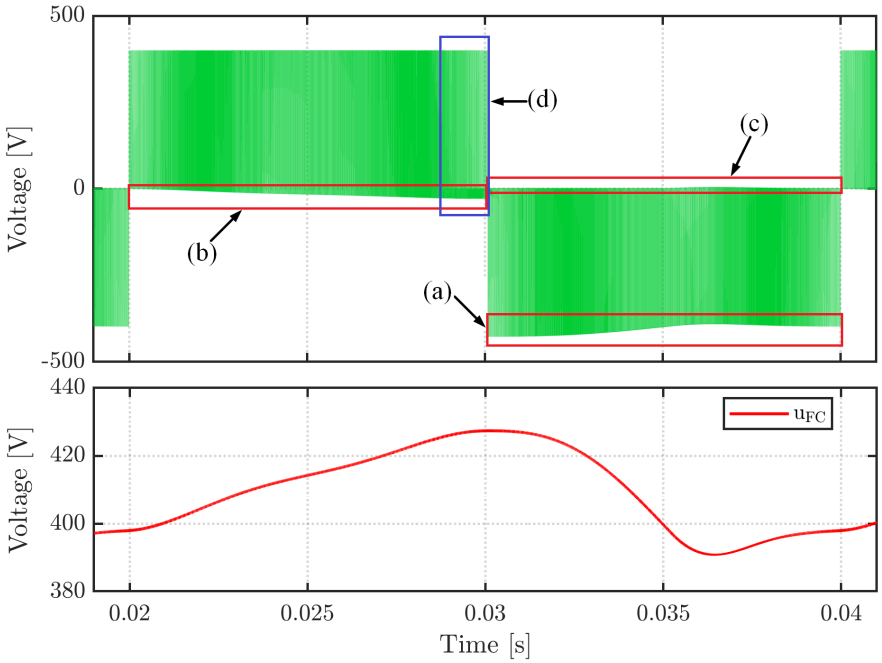


Figure 3.9: Bridge output voltage with distortion regions marked with red/blue, and flying capacitor voltage.

Figure 3.9 shows the converter bridge voltage and flying capacitor voltage for a single cycle with regions marked in red/blue specifying the distorted regions. Figure 3.10 presents a zoomed view of three specific regions. A detailed explanation is as follows:

(a) The peak bridge output voltage follows the slow decrease in the C_{FC} voltage. As can be seen, peak output voltage u_m varies between -430 V and -390 V due to the voltage ripple of the flying capacitor (δ_{FC}). From 0.03 s to 0.036 s the flying capacitor discharges without charging during the zero state, whereas 0.036 s onwards the flying capacitor discharges and subsequently charges during the zero state, hence a slight increase is observed.

(b) It shows the bridge voltage u_m during the positive cycle when zero state is active. Unlike the NPC converter, where bridge voltage during the zero state = 0, sFCI does not show similar behavior. The main reason for this is that the voltage of the C_{FC} is higher than the input *dc*-link. Due to this a negative voltage drop appears across the switch S_4, i.e., $u_{S_4} = (u_{dc} - u_{FC}) < 0$, and subsequently the series diode of the RB-IGBT is reverse biased. Hence, S_4 does not conduct any current for most of the positive cycle (S_4 conducts during the region (d), discussed later), even though it is supplied with switching signals. This negative voltage drop u_{S_4} appears at the output and keeps increasing as the FC is charging continuously (only during zero state).

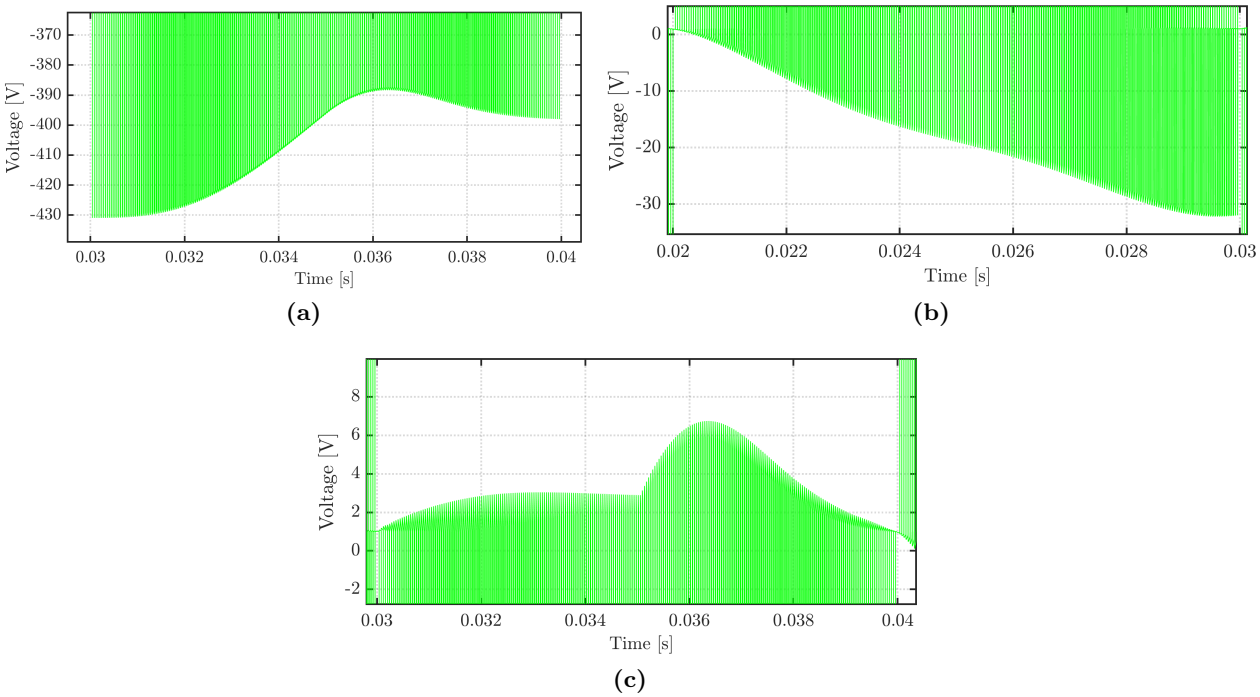


Figure 3.10: Open-loop converter bridge voltage u_m: zoom-in view (a) distortion during negative state, (b) distortion during zero-state of positive half cycle, (c) distortion during zero-state of negative half cycle.

(c) It shows the bridge voltage u_m during the negative cycle when zero state is active. Again, this is in contrast to the behavior of conventional topologies like NPC, where voltage at the bridge is essentially zero. In this case, from 0.03 s to 0.035 s a small voltage drop appears across the output because switch S_4 conducts the main inductor current, while no charging currents flow as ($u_{dc} < u_{FC}$). Beyond 0.035 s ($u_{dc} > u_{FC}$), hence charging currents flow and switch S_4 conducts both the main inductor current i_m and C_{FC} charging current i_{FC}. Therefore, increase in voltage drop across the switch S_4 is observed.

3.2.4 Three-step voltage behavior

In addition to the distorted regions (a,b,c) discussed above, the bridge voltage u_m, see Figure 3.9, has an additional region marked in blue. A zoomed-in view of this region is presented in Figure 3.11. In general, the conventional topologies like NPC can only generate two voltage values during one switching period, i.e., either positive and zero or negative and zero. However, from Figure 3.11 it is observed that the Siwakoti-H inverter generates three different voltage values in a single switching period. This behavior is primarily due to the ripple of the flying capacitor. As discussed earlier, switch S_4 does not conduct for most part of the positive cycle. But, near the transition from positive to negative cycle the main inductor current i_m goes negative due to the current ripple. It is clear from Figure 3.6(b) that the main inductor current i_m has a current ripple ≈ 5 A. In this situation, series diode of the switch S_4 becomes forward biased due to high di/dt and hence S_4 conducts for a part of the switching period. Whenever S_4 conducts, the output voltage changes from a negative value (u_{S_4}) to a voltage ≈ 0. Hence, instead of a normal two voltage level behavior, three stepped voltages are observed in the sFCI.

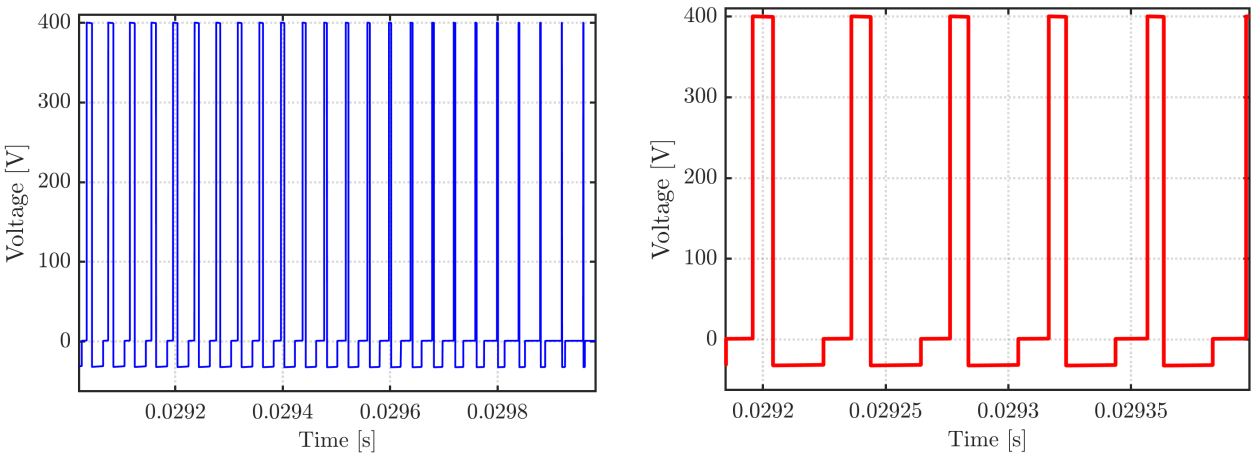


Figure 3.11: Open-loop converter bridge voltage: three-step behavior.

3.2.5 Operating cases of zero-state

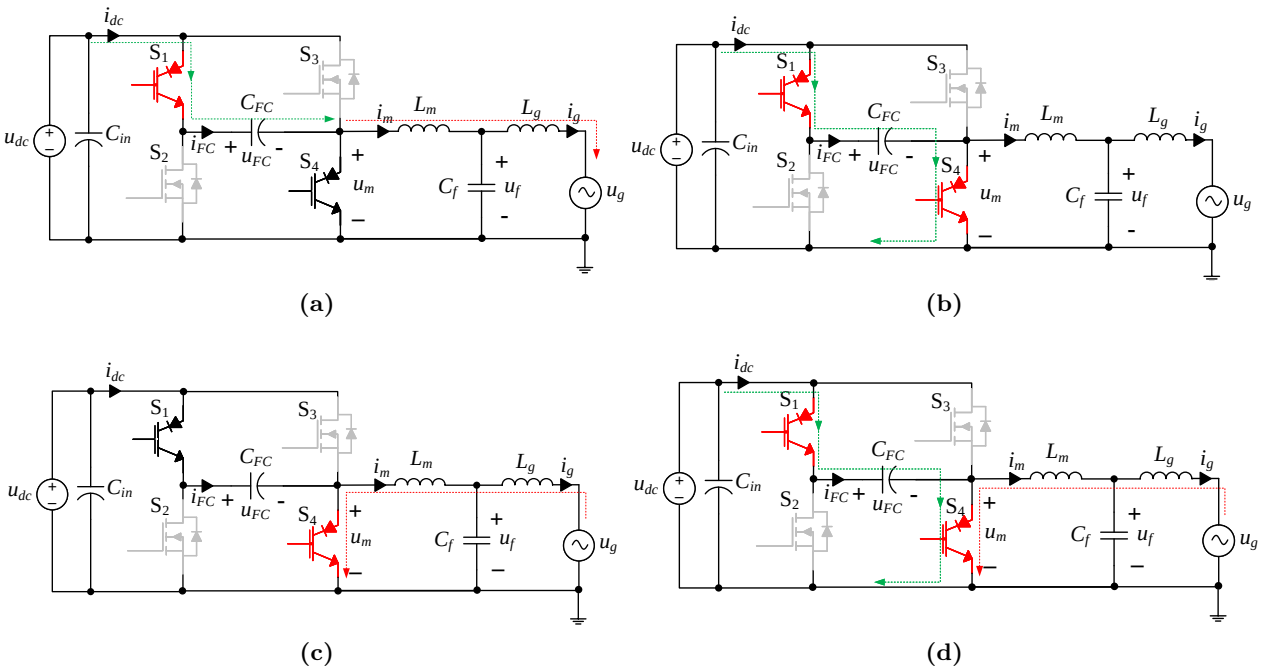


Figure 3.12: Zero-state: four different operating modes.

In [3,13] only three working states of the sFCI were proposed, and described in section 3.1.3. However, from the previous discussion we can conclude that *zero state* does not actually generate zero voltage at the output of the converter. Rather the zero state can be divided into four cases based on the cycle of operation and other conditions. The proposed operating modes of the zero state are illustrated in Figure 3.12. In all the four cases, switches S_1 and S_4 are supplied with gating signals. Explanation of the four cases is as follows:

(a) This case exists during the positive cycle. When the main inductor current $i_m > 0$, the voltage across switch S_4 is negative due to the voltage ripple δ_{FC} and therefore S_4 does not conduct. Moreover, the charging current i_{FC} flows via $S_1 \rightarrow C_{FC} \rightarrow L_m$.

(b) This case also exists during the positive cycle. When the main inductor current i_m becomes negative due to its ripple, the series diode of S_4 is forward biased [for details see section 3.2.5]. Hence charging current i_{FC} flows via $S_1 \rightarrow C_{FC} \rightarrow S_4$.

(c) This case is existent during the negative cycle when $(u_{dc} < u_{FC})$. In this case charging current i_{FC} does not flow as the voltage u_{FC} is more than the input *dc*-link. The main inductor current i_m is negative and flows through S_4, as the switch S_2 is turned OFF.

(d) This case also occurs during the negative cycle. When $(u_{dc} > u_{FC})$, charging current i_{FC} flows via $S_1 \rightarrow C_{FC} \rightarrow S_4$. Additionally, i_m also flows through S_4 as the switch S_2 is OFF. Hence, the current stress on S_4 is maximum in this case.

3.3 Mathematical basics for system modeling

In this section, the utilized nomenclature for three-phase electrical systems is introduced. In contrast to the general complex representation/notation, the space vectors are introduced in the *vector-/matrix* representation.

3.3.1 Three-phase electrical systems

Three phase systems are described using vector variables. In general, the following vector

$$\boldsymbol{x}^{abc}(t) := \begin{bmatrix} x_a(t) \\ x_b(t) \\ x_c(t) \end{bmatrix} := \begin{bmatrix} \tilde{x}_a(t)\cos(\phi_a(t)) \\ \tilde{x}_b(t)\cos(\phi_b(t)) \\ \tilde{x}_c(t)\cos(\phi_c(t)) \end{bmatrix}, \qquad \boldsymbol{x}^{abc} \in \mathbb{R}^3 \tag{3.1}$$

with sinusoidal components is defined, see [58, Sec. 2]. The phase quantities $x_a(t), x_b(t), x_c(t)$ have amplitudes $\tilde{x}_a(t), \tilde{x}_b(t), \tilde{x}_c(t)$ and phase angles $\phi_a(t), \phi_b(t), \phi_c(t) \in \mathbb{R}$(in rad), respectively. The variable $\boldsymbol{x}$ corresponds to the phase voltage vector $\boldsymbol{u}$ (in V)[3] or the phase current vector $\boldsymbol{i}$ (in A)[3].

In this thesis, mainly *balanced* three phase electrical grid is considered. Hence, the following assumptions can be imposed on the phase quantities:

Assumption (A.1): *All phases have same amplitude, i.e.*

$$\forall t \geq 0\,\mathrm{s}: \qquad \tilde{x}(t) := \tilde{x}_a(t) = \tilde{x}_b(t) = \tilde{x}_c(t). \tag{3.2}$$

Assumption (A.2): *Each phase is shifted from one another by an angle of* $\frac{2}{3}\pi$*, i.e.*

$$\forall t \geq 0\,\mathrm{s}: \qquad \phi(t) := \phi_a(t) = \phi_b(t) + \frac{2}{3}\pi = \phi_c(t) + \frac{4}{3}\pi. \tag{3.3}$$

3.3.2 Space vectors and transforms

The use of space vectors to represent the three-phase systems is well established in practice [58]. The three phases of the an electrical grid are *spatially* displaced from each other by $120° = \frac{2}{3}\pi$. The three phases *a, b, c* are plotted as vectors in Figure 3.13, where all the electrical quantities can be described along the three axes. In order to simplify the calculations and reduce the number of the manipulated variables, orthogonal coordinate system is generally used, where the three phase quantities can be transformed to a two phase vector space. In Figure 3.13, two orthogonal coordinate systems are shown:

1. The stationary $s = (\alpha, \beta)$-reference frame with the axes α, β and the vector $\boldsymbol{x}^s = (x^\alpha, x^\beta)^\top$. The α-axis of the s-reference frame/coordinate system is aligned with the a-axis of the general (a, b, c) coordinate system.

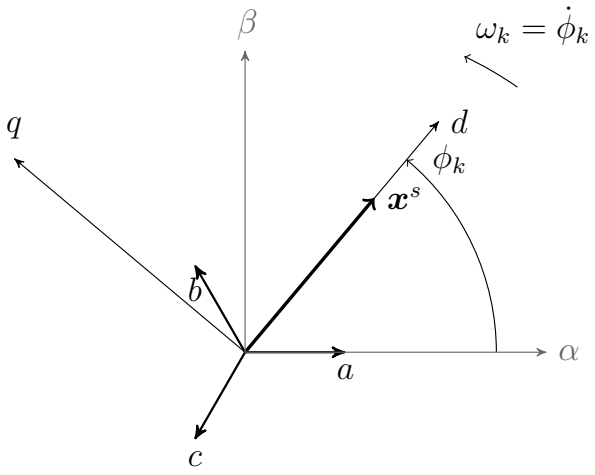


Figure 3.13: Various reference frames (or coordinate systems): general (a, b, c)-reference frame, stationary $s = (\alpha, \beta)$-reference frame, and rotating $k = (d, q)$-reference frame. The vector $\boldsymbol{x}^s = (x^\alpha, x^\beta)^\top$ has a length $\| \boldsymbol{x}^s \| = \sqrt{(x^\alpha)^2 + (x^\beta)^2}$ [58].

2. The rotating $k = (d, q)$-reference frame with the axes d, q and the vector $\boldsymbol{x}^k = (x^d, x^q)^\top$. The d-axis of the k-reference frame/coordinate system is displaced by an angle ϕ_k from the a-axis of the general (a, b, c) coordinate system.

3.3.2.1 Clarke transformation $(a, b, c) \leftrightarrow (\alpha, \beta)$

The mathematical conversion of the three phase quantities $\boldsymbol{x}^{abc}(t)$ to the stationary s-reference frame is known as the *Clarke Transformation*. The space vector $\boldsymbol{x}^s$ can be described in the Cartesian (α, β)-coordinate system as shown in Figure 3.13, since three linearly dependent quantities can be expressed by two linearly independent variables. The space vector $\boldsymbol{x}^s$ can be summarized as a complex number:

$$\begin{aligned} \boldsymbol{x}^s &= \frac{2}{3}(x_a + x_b e^{j\cdot\frac{2}{3}\pi} + x_c e^{j\cdot\frac{4}{3}\pi}) \\ &= \frac{2}{3}\left[x_a - \frac{1}{2}x_b - \frac{1}{2}x_c + j\left(\frac{\sqrt{3}}{2}x_b - \frac{\sqrt{3}}{2}x_c\right)\right] \end{aligned} \tag{3.4}$$

The transformation from phase-values to space vector can also be expressed in the matrix notation:

$$\boldsymbol{x}^{\alpha\beta}(t) = \begin{bmatrix} x^\alpha \\ x^\beta \end{bmatrix} = \frac{2}{3} \cdot \underbrace{\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}}_{=:\mathbf{T}_c \in \mathbb{R}^{2\times 3}} \cdot \boldsymbol{x}^{abc}(t) \tag{3.5}$$

Here the factor $\frac{2}{3}$ is use to scale the length of the space vector to the amplitude of the phase values, and hence yields an amplitude correct transformation. Also, the inverse Clarke transformation $(\alpha, \beta) \leftrightarrow (a, b, c)$ can be written as

$$\boldsymbol{x}^{abc}(t) = \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}}_{=:\mathbf{T}_c^{-1} \in \mathbb{R}^{3\times 2}} \cdot \boldsymbol{x}^{\alpha\beta}(t). \tag{3.6}$$

3.3.2.2 Park transformation $(\alpha, \beta) \leftrightarrow (d, q)$

The previous section discussed the stationary coordinate system (α, β). If any space vector is rotated counterclockwise by an angle ϕ_k, the rotation can be described by the matrix:

$$\mathbf{T}_\mathrm{p}(\phi_\mathrm{k}) = \begin{bmatrix} \cos(\phi_\mathrm{k}) & -\sin(\phi_\mathrm{k}) \\ \sin(\phi_\mathrm{k}) & \cos(\phi_\mathrm{k}) \end{bmatrix} \tag{3.7}$$

For three-phase electrical systems this transformation is famous as *Park Transformation* [59]. Figure 3.13 illustrates the definition of the angle ϕ_k. By using the *Park transformation* stationary quantities $\boldsymbol{x}^s = (x^\alpha, x^\beta)^\top$ can be represented in the rotating $k = (d, q)$-reference frame. The conversion between the stationary quantities and quantities in the k-reference frame is given by

$$\boldsymbol{x}^{dq}(t) = \begin{bmatrix} x^d \\ x^q \end{bmatrix} = \underbrace{\begin{bmatrix} \cos(\phi_\mathrm{k}) & \sin(\phi_\mathrm{k}) \\ -\sin(\phi_\mathrm{k}) & \cos(\phi_\mathrm{k}) \end{bmatrix}}_{=:\mathbf{T}_\mathrm{p}^{-1}(\phi_\mathrm{k}) \in \mathbb{R}^{2\times 2}} \cdot \boldsymbol{x}^{\alpha\beta}(t) \quad \Leftrightarrow \quad \boldsymbol{x}^{\alpha\beta}(t) = \underbrace{\begin{bmatrix} \cos(\phi_\mathrm{k}) & -\sin(\phi_\mathrm{k}) \\ \sin(\phi_\mathrm{k}) & \cos(\phi_\mathrm{k}) \end{bmatrix}}_{=:\mathbf{T}_\mathrm{p}(\phi_\mathrm{k}) \in \mathbb{R}^{2\times 2}} \cdot \boldsymbol{x}^{dq}(t) \tag{3.8}$$

Here, $\mathbf{T}_\mathrm{p}(\phi_\mathrm{k})$ is the Park transformation matrix and $\mathbf{T}_\mathrm{p}(\phi_\mathrm{k})^{-1}$ is the inverse Park transformation matrix. Table 3.3 presents an overview of the different coordinate systems relevant for our application.

Reference Frame	Abbrev.	Angle	Notation	Transform
General	(a, b, c)	-	$\boldsymbol{x}^{abc}$	-
Stationary	(α, β)	-	$\boldsymbol{x}^{\alpha\beta}$	Clarke
Rotating	(d, q)	ϕ_k	$\boldsymbol{x}^{dq}$	Clarke & Park

Table 3.3: Useful frames of reference.

3.4 LCL filters for grid connection

3.4.1 Transfer function of LCL filter

A single phase LCL filter, depicted in Figure 3.14, is considered for the derivation of the transfer function. Considering the LCL filter and invoking Kirchhoff's laws, the differential equations that define the dynamics of the filter can be summarized as:

$$0 = u_m - L_m \frac{\mathrm{d}i_m}{\mathrm{d}t} - R_m i_m - u_f \tag{3.9a}$$

$$0 = u_f - R_g i_g - L_g \frac{\mathrm{d}i_g}{\mathrm{d}t} - u_g \tag{3.9b}$$

$$0 = i_m - i_f - i_g \tag{3.9c}$$

$$0 = i_f - C_f \frac{\mathrm{d}}{\mathrm{d}t}(u_f - R i_f) \tag{3.9d}$$

Using Laplace transform and rearranging, the set of equations (3.9) can be written as:

$$i_m = i_f + i_g \tag{3.10}$$

$$u_m - u_f = i_m(sL_m + R_m) \tag{3.11}$$

$$u_f - u_g = i_g(sL_g + R_g) \tag{3.12}$$

$$u_f = i_f \left(\frac{1}{sC_f} + R \right) \tag{3.13}$$

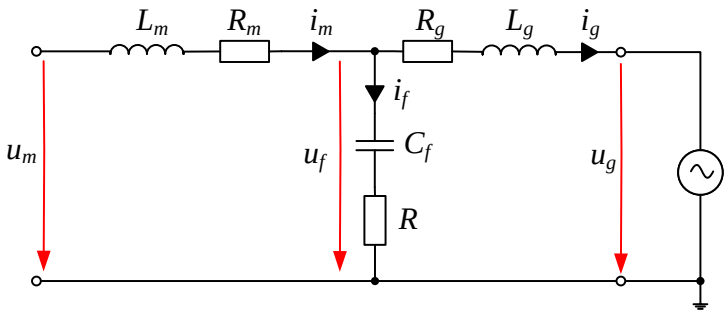


Figure 3.14: Single-phase schematic of LCL filter.

The notations used in the LCL filter are as follows:

- u_m: Converter Bridge output voltage.
- L_m: Main inductor.
- R_m: Internal resistance of main inductor.
- i_m: Main inductor current.
- u_f: Voltage drop across filter capacitor.
- i_f: Filter capacitor current.
- C_f: Filter capacitance.
- R: Parasitic resistance of filter capacitor.
- L_g: Grid side inductor.
- R_g: Internal resistance of grid side inductor.
- i_g: Grid current.
- u_g: Grid voltage

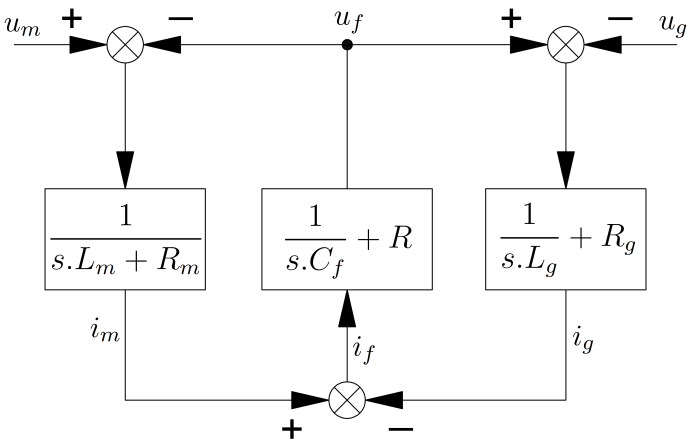


Figure 3.15: Block diagram of the LCL filter [60].

The block diagram of the filter is shown in Figure 3.15. From (3.12) and (3.13), we can write

$$i_f \left(\frac{1}{sC_f} + R \right) = i_g(sL_g + R_g) \tag{3.14a}$$

$$\Rightarrow \qquad i_f \qquad = i_g \frac{s^2 C_f L_g + sC_f R_g}{sC_f R + 1} \tag{3.14b}$$

Substituting (3.10), (3.12) and (3.14b) into (3.11) and rearranging the terms, the bridge voltage can

be expressed as:

$$\begin{aligned} u_m &= i_g(sL_g + R_g) + (i_g + i_f)(sL_m + R_m) \\ &= i_g(sL_g + R_g) + \left(i_g + i_g \frac{s^2 C_f L_g + sC_f R_g}{sC_f R + 1}\right)(sL_m + R_m) \end{aligned} \tag{3.15}$$

$$\Rightarrow \quad u_m = i_g \left(sL_g + R_g + sL_m + R_m + \frac{(sL_m + R_m)(s^2 C_f L_g + sC_f R_g)}{sC_f R + 1}\right) \tag{3.16}$$

Hence, the output-to-input transfer function $i_g(s)/u_m(s)$ of the LCL filter can be written as

$$\boldsymbol{H}(s) = \frac{sC_f R + 1}{s^3 L_g L_m C_f + s^2 C_f (L_g(R + R_m) + L_m(R + R_g)) + s(L_g + L_m + C_f(RR_g + RR_m + R_m R_g)) + R_g + R_i} \tag{3.17}$$

Using the system parameters from Table 3.1, the resonant frequency of the LCL filter can be calculated as

$$\omega_r = \sqrt{\frac{L_m + L_g}{L_m L_g C_f}} = 63.808 \cdot 10^3 \text{rad/s} \qquad \Rightarrow f_r = 10.155\text{kHz} \tag{3.18}$$

Figure 3.16 shows the bode plot considering a loss-less filter. The resonant peak is near 10kHz.

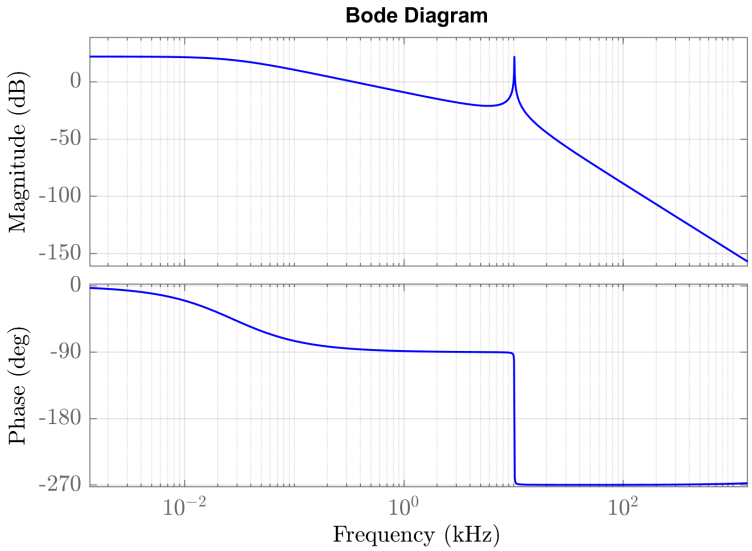


Figure 3.16: Bode plot of the LCL filter.

3.4.2 LCL filter resonance damping

Figure 3.16 shows the bode plot of the uncompensated and undamped LCL filter. The resonant peak is clearly visible and poses a challenge for the design of a controller. This resonant behavior of the LCL filter must be damped adequately using either a passive damping component(s) or an active damping (AD) strategy. If the resonant frequency is not adequately damped, the introduction of an LCL filter may worsen the performance of the system due to increased grid current distortion [25].

3.4.2.1 Passive Damping

Passive damping is achieved by adding a resistance in series or in parallel with the capacitance C_f or inductance L_m of the filter. Two possible solutions in which a series resistance is added are shown in Fig. 3.17.

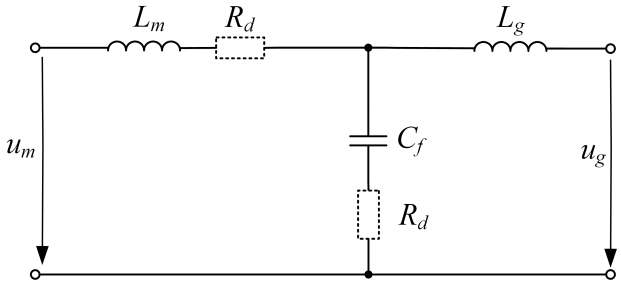
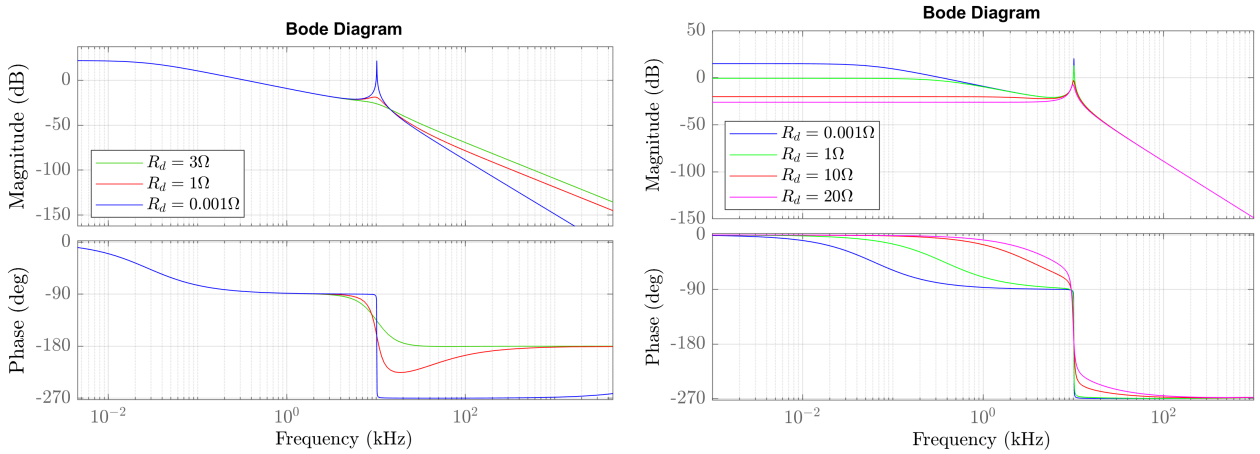


Figure 3.17: Possible positions for adding a damping resistance.

Addition of damping resistance R_d should adequately damp the resonant behavior of the LCL filter, although it is accompanied with increased power losses. Figure 3.18 shows the bode plots of two cases. It is clear that addition of damping resistance in series with the filter capacitor C_f provides good damping with less losses, compared to a series resistance for the inductor L_m.



(a) Damping resistance in series with filter capacitor C_f. **(b)** Damping resistance in series with main inductor L_m.

Figure 3.18: Bode plots of LCL filter with passive damping.

In Figure 3.18(a), adding a damping resistance of $R_d = 1\,\Omega$ provides good damping with a phase margin $> 90°$. On the contrary, adding a damping resistance $R_d = 20\,\Omega$ in series with L_m provides very less damping with significant increase in power losses.

3.4.2.2 Active Damping

Although passive damping is a simple solution it leads to a decrease in the system efficiency. Other approaches that can be employed for resonance damping include 1) virtual resistance method, 2) addition of a lag-lead compensator, and 3) using a Notch-filter. Virtual resistance method has been extensively use in literature [60–62] as it offers a workaround for resistance damping method. Instead of adding a real resistor, behavior of the resistor is emulated in the controller by using feedback signals and proportional terms. If tuned properly, virtual resistance method offers similar performance like passive damping without additional power losses.

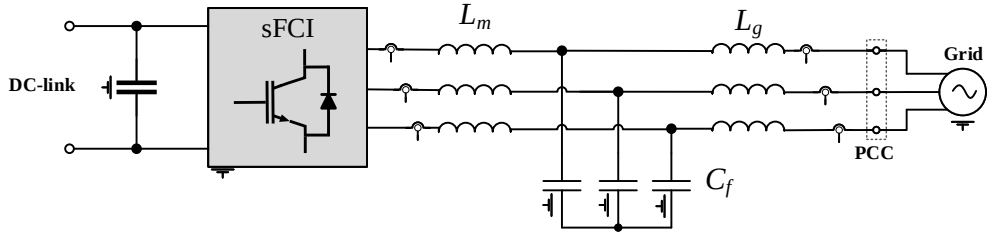


Figure 3.19: Three-phase sFCI with LCL filter, point of common coupling (PCC) and the grid.

3.5 System modeling of grid-connected sFCI equipped with LCL filter

Figure 3.19 shows a grid connected sFCI with an LCL filter. The converter has a common *dc*-link u_{dc} for all the three phases, employing a single *dc*-link capacitor C_{in} and separate flying capacitors (C_{FC}) for each phase. The LCL-filter consists of main inductor L_m and grid-side inductor L_g, with internal resistances R_m and R_g respectively. The filter capacitors C_f with parasitic resistance R are connected in a star configuration. The LCL-filter offers attenuation to the harmonics generated by the converter, before it is connected to the grid. It is assumed that the amplitude and phase of the grid voltage remains constant for the model and the direction of current flow is from converter to grid. Modeling of the system is based on the assumption that the converter is fed from an ideal energy source, meaning that the *dc*-link voltage u_{dc}/u_{FC} is constant. Modeling is carried out in the general (a, b, c)-reference frame.

For modeling we impose the following assumptions :

Assumption (A.3): *The grid has a positive magnitude, a constant angular frequency $\omega_g > 0$, and is symmetric, i.e., $u_g^a(t) + u_g^b(t) + u_g^c(t) = 0$.*

Assumption (A.4): *The grid voltage $u_g^{abc}(t) = [u_g^a(t)\ \ u_g^b(t)\ \ u_g^c(t)]^\top$ is considered as a disturbance input and is available for feedback for $t \geq 0$.*

Assumption (A.5): *The switching behavior of the converter bridge is neglected i.e. the non-linear behavior of the flying capacitor due to its interaction with the switches is not considered for modeling.*

Based on the assumption (A.5) the sFCI converter bridge can be neglected and the system model can be derived for the filter/grid system. Invoking assumption (A.4) and the Kirchoff's current and voltage laws yields the dynamics of the filter/grid system (see Figure 3.14) in the (a, b, c)-reference frame as follows

$$0 = -\boldsymbol{u}_m^{abc}(t) + R_m \boldsymbol{i}_m^{abc}(t) + L_m \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_m^{abc}(t) + R(\boldsymbol{i}_m^{abc}(t) - \boldsymbol{i}_g^{abc}(t)) + \boldsymbol{u}_f^{abc}(t) \tag{3.19a}$$

$$0 = \boldsymbol{i}_m^{abc}(t) - \boldsymbol{i}_g^{abc}(t) - C_f \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{u}_f^{abc}(t) \tag{3.19b}$$

$$0 = R(\boldsymbol{i}_m^{abc}(t) - \boldsymbol{i}_g^{abc}(t)) + \boldsymbol{u}_f^{abc}(t) - \boldsymbol{u}_g^{abc}(t) - R_g \boldsymbol{i}_g^{abc}(t) + -L_g \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_g^{abc}(t) \tag{3.19c}$$

Rearranging the terms to derive a state-space model of the system, we can write:

$$\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_m^{abc}(t) = \frac{1}{L_m}\boldsymbol{u}_m^{abc}(t) - \frac{R_m + R}{L_m}\boldsymbol{i}_m^{abc}(t) - \frac{1}{L_m}\boldsymbol{u}_f^{abc}(t) - \frac{R}{L_m}\boldsymbol{i}_g^{abc}(t) \tag{3.20a}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{u}_f^{abc}(t) = \frac{1}{C_f}\boldsymbol{i}_m^{abc}(t) - \frac{1}{C_f}\boldsymbol{i}_g^{abc}(t) \tag{3.20b}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_g^{abc}(t) = \frac{R}{L_g}\boldsymbol{i}_m^{abc}(t) + \frac{1}{L_g}\boldsymbol{u}_f^{abc}(t) - \frac{R + R_g}{L_g}\boldsymbol{i}_g^{abc}(t) - \frac{1}{L_g}\boldsymbol{u}_g^{abc}(t) \tag{3.20c}$$

For the model of the inverter, we denote the state, control input, and disturbance as

$$\begin{aligned} \boldsymbol{x} &:= \begin{bmatrix} \boldsymbol{i}_m^{abc} & \boldsymbol{u}_f^{abc} & \boldsymbol{i}_g^{abc} \end{bmatrix}^\top \\ \boldsymbol{u} &:= \boldsymbol{u}_m^{abc} \\ \boldsymbol{d} &:= \boldsymbol{u}_g^{abc} \end{aligned} \tag{3.21}$$

Hence the continuous-time state-space model of the system can be written as

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \mathbf{F}\boldsymbol{x}(t) + \mathbf{G}\boldsymbol{u}(t) + \mathbf{T}\boldsymbol{d}(t) \tag{3.22a}$$

$$\boldsymbol{y} = \mathbf{C}\boldsymbol{x}(t) \tag{3.22b}$$

where the system matrices are

$$\mathbf{F} = \begin{bmatrix} -\frac{R_m+R}{L_m} & -\frac{1}{L_m} & \frac{R}{L_m} \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} \\ \frac{R}{L_g} & \frac{1}{L_g} & \frac{R+R_g}{L_m} \end{bmatrix}; \mathbf{G} = \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \end{bmatrix}; \mathbf{T} = \begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L_g} \end{bmatrix}; \mathbf{C} = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix}. \tag{3.23}$$

3.6 Summary

In this chapter the design and working of the sFCI was discussed. The operation of the topology was analyzed in detail and preliminaries for system modeling were presented. As can be inferred, the sFCI has a simple construction but its response is not essentially linear, and exhibits a different behavior compared to the conventional inverter topologies due to additional non-linearities. Finally, the non-linear nature of the converter is neglected and behavior of the LCL filter/grid is modeled using mathematical equations.

Chapter 4

State-Feedback Current Control

This chapter proposes the design and digital implementation of a State Feedback Current Controller (SFCC) for the single phase and three phase sFCI converter. The objective of the controller is grid current reference ($i_{g,\text{ref}}$) tracking, maintaining the voltage ripple (δ_{FC}) of the flying capacitors below the maximum allowed value, and minimizing the THD of the grid side current. The design of the control structure for single-phase (phase leg) and three phase system are covered separately. The chapter is concluded by simulation results.

4.1 Controller design for a single-phase sFCI

Due to the novel nature of this inverter and lack of previous literature that deals with its control problem, separate approach was followed for the design of control loop for single-phase and three-phase sFCI. As a general notion, a single-phase controller can be extended to the three-phase system, at a later stage, without much effort. Hence, the following sections deal with the controller design for the single-phase sFCI.

A single phase grid-connected sFCI converter is shown in Figure 4.1. The current controller is implemented in the general (a, b, c)-reference frame. In the following sections, the continuous time and discrete time models of the system, are introduced. The losses in the filter components are neglected for the reasons: 1) internal resistances offer additional damping and can be neglected to consider the worst-case scenario for the LCL filter resonance [22]; and 2) the complexity of the discrete-time model and the control algorithm reduces.

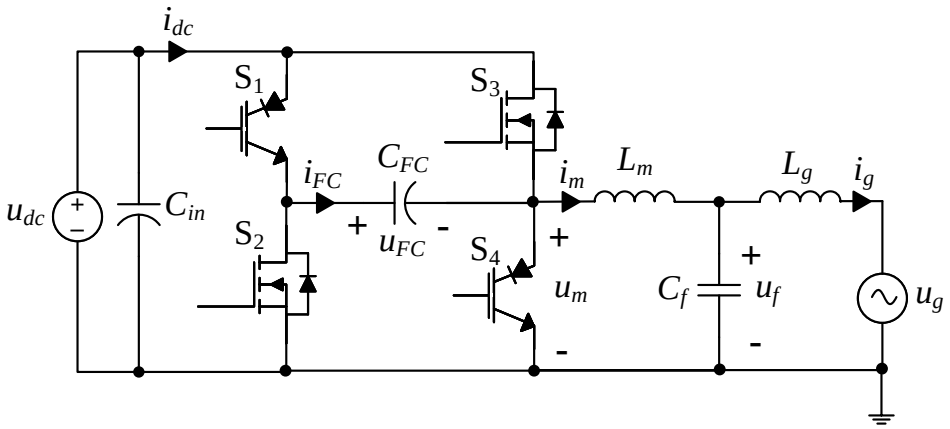


Figure 4.1: Single-phase grid-connected sFCI.

Assumption (A.6): *The losses in the filter components are neglected i.e. internal resistances R_m, R_g, and R are considered zero, and therefore not shown in Figure 4.1.*

Assumption (A.7): *The bridge voltage $u_m(t)$ is assumed to be constant during $kT_s < t < (k+1)T_s$, where T_s is the sampling time [22].*

Assumption (A.8): *The sampling frequency f_s and the switching frequency f_{sw} are equal.*

4.1.1 Continuous-time model

Invoking the assumption (A.5) the dynamics of the flying capacitor are neglected, and hence the system to be controlled reduces to an LCL filter. Based on the Assumption (A.6) the continuous time dynamics of the LCL filter described by the system of equations (3.22), (3.23) can be rewritten for the single phase system as:

$$\begin{aligned}\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} &= \underbrace{\begin{bmatrix} 0 & -\frac{1}{L_m} & 0 \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} \\ 0 & \frac{1}{L_g} & 0 \end{bmatrix}}_{\mathbf{F}} \boldsymbol{x}(t) + \underbrace{\begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{G}} u_m(t) + \underbrace{\begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L_g} \end{bmatrix}}_{\mathbf{T}} u_g(t) \\ y(t) &= \underbrace{\begin{bmatrix} 0 & 0 & 1 \end{bmatrix}}_{\mathbf{C}} \boldsymbol{x}(t)\end{aligned} \tag{4.1}$$

where $\boldsymbol{x} = [i_m \;\; u_f \;\; i_g]^\top$ is the state vector, y is the output i.e., grid current i_g, and input disturbance matrix $\mathbf{D}$ is assumed to be zero. Essentially the model of (4.1) can be summarized as:

$$\dot{\boldsymbol{x}}(t) = \mathbf{F}\boldsymbol{x}(t) + \mathbf{G}u_m(t) + \mathbf{T}u_g(t) \tag{4.2a}$$
$$y(t) = \mathbf{C}\boldsymbol{x}(t) \tag{4.2b}$$

The transfer function of the LCL filter from the bridge voltage to the converter current is given as

$$Y(s) = \mathbf{C}(s\mathbf{I} - \mathbf{F})^{-1}\mathbf{G} = \frac{1}{L_m}\frac{s^2 + \omega_z^2}{s(s^2 + \omega_r^2)} \tag{4.3}$$

$$\text{where} \qquad \omega_r = \sqrt{\frac{L_m + L_g}{L_m L_g C_f}} \quad \text{and} \quad \omega_z = \sqrt{\frac{1}{L_g C_f}} \tag{4.4}$$

are the resonance and anti-resonance frequencies of the LCL filter, respectively.

4.1.2 Discrete-time model

In general, a control algorithm has to be implemented on a DSP or an FPGA. One method is to design the controller in continuous time and then use discrete time equivalent for implementation, see [21, 23]. A better way is to discretize the system model and design the controller in discrete time. Therefore, this section discusses the derivation of a Zero-Order-Hold equivalent discrete-time model for the LCL filter/grid system. Based on the assumption (A.8) sampling frequency and switching frequency are equal. Under the assumptions (A.5), (A.6), (A.7), (A.8) and considering that the bridge voltage is averaged over the switching-cycle, the discrete time model of (4.1) becomes

$$\boldsymbol{x}(k+1) = \mathbf{A}\boldsymbol{x}(k) + \mathbf{B}u_m(k) + \mathbf{E}u_g(k) \tag{4.5a}$$
$$y(k) = \mathbf{C}\boldsymbol{x}(k) \tag{4.5b}$$

where the discretized system matrices are

$$\mathbf{A} = e^{\mathbf{F}T_s} = \begin{bmatrix} \frac{L_m + L_g\cos(\omega_r T_s)}{L_t} & -\frac{\sin(\omega_r T_s)}{\omega_r L_m} & \frac{L_g[1-\cos(\omega_r T_s)]}{L_t} \\ \frac{\sin(\omega_r T_s)}{\omega_r C_f} & \cos(\omega_r T_s) & -\frac{\sin(\omega_r T_s)}{\omega_r C_f} \\ \frac{L_m[1-\cos(\omega_r T_s)]}{L_t} & \frac{\sin(\omega_r T_s)}{\omega_r L_g} & \frac{L_g + L_m\cos(\omega_r T_s)}{L_t} \end{bmatrix}$$

$$\mathbf{B} = \left(\int_0^{T_s} e^{\mathbf{F}\tau}\cdot e^{\mathrm{j}\omega_g\tau} d\tau\right)\mathbf{G} = \begin{bmatrix} \frac{T_s}{L_t} + \frac{L_g\sin(\omega_r T_s)}{\omega_r L_m L_t} \\ \frac{L_g[1-\cos(\omega_r T_s)]}{L_t} \\ \frac{T_s}{L_t} + \frac{\sin(\omega_r T_s)}{\omega_r L_t} \end{bmatrix} \tag{4.6}$$

$$\mathbf{E} = \left(\int_0^{T_s} e^{\mathbf{F}\tau}\cdot e^{\mathrm{j}\omega_g\tau} d\tau\right)\mathbf{T} = \begin{bmatrix} -\frac{T_s}{L_t} + \frac{\sin(\omega_r T_s)}{\omega_r L_t} \\ \frac{L_m[1-\cos(\omega_r T_s)]}{L_t} \\ -\frac{T_s}{L_t} + \frac{L_m\sin(\omega_r T_s)}{\omega_r L_g L_t} \end{bmatrix}$$

Due to the finite computation time, there exists a computational delay between the calculation of the reference voltage $u_{m,\mathrm{ref}}$ and its application to the converter bridge u_m [63]. This delay can modeled as $u_m(k) = u_{m,\mathrm{ref}}(k-1)$ [22]. Taking the computational delay into account, the discrete-time model is written as

$$\begin{aligned} \boldsymbol{x}_d(k+1) &= \underbrace{\begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{0} & 0 \end{bmatrix}}_{\mathbf{A}_\mathrm{d}} \boldsymbol{x}_d(k) + \underbrace{\begin{bmatrix} 0 \\ 1 \end{bmatrix}}_{\mathbf{B}_\mathrm{d}} u_{m,\mathrm{ref}}(k) + \underbrace{\begin{bmatrix} \mathbf{E} \\ 0 \end{bmatrix}}_{\mathbf{E}_\mathrm{d}} u_g(k) \\ \boldsymbol{y}(k) &= \underbrace{\begin{bmatrix} \mathbf{C} & 0 \end{bmatrix}}_{\mathbf{C}_\mathrm{d}} \boldsymbol{x}_d(k) \end{aligned} \tag{4.7}$$

where the modified state vector is $\boldsymbol{x}_d = [\boldsymbol{x}^\top \;\; u_m]^\top$.

4.1.3 Controllability

For the design of the state-feedback controller, it must be assured that the system (3.22) is controllable. According to the Kalman Controllability criterion (see section 2.3.3), system (3.22) is controllable if

$$\operatorname{rank} \underbrace{\begin{bmatrix} \mathbf{G} & \mathbf{FG} & \mathbf{F}^2\mathbf{G} \end{bmatrix}}_{=:\mathbf{M}_\mathrm{c}} = 3. \tag{4.8}$$

Solving for $\mathbf{M}_\mathrm{c}$ we get

$$\mathbf{M}_\mathrm{c} = \frac{1}{L_m}\begin{bmatrix} 1 & 0 & -\frac{1}{L_m C_f} \\ 0 & \frac{1}{C_f} & 0 \\ 0 & 0 & \frac{1}{C_f L_g} \end{bmatrix} \tag{4.9}$$

Rank of $\mathbf{M}_\mathrm{c} = 3$ if, and only if, $L_m > 0$, $C_f > 0$, and $L_g > 0$. Since all these parameters are > 0, see Table 3.1, controllability matrix has a full rank and hence the system (3.22) is controllable.

4.2 Design of the current controller

The scheme of the current controller based on state-feedback is shown in Figure 4.2. For improved disturbance rejection the controller is extended using an integral-state, by introducing an integrator into the control loop. The integral state is defined as

$$x_I(k+1) = x_I(k) + i_{g,\mathrm{ref}}(k) - i_g(k) \tag{4.10}$$

where $i_{g,\mathrm{ref}}$ is the grid current reference. The state-space control law becomes

$$u_{m,\mathrm{ref}}(k) = k_I x_I(k) + k_f\, i_{g,\mathrm{ref}}(k) - \mathbf{K}\boldsymbol{x}_d(k) \tag{4.11}$$

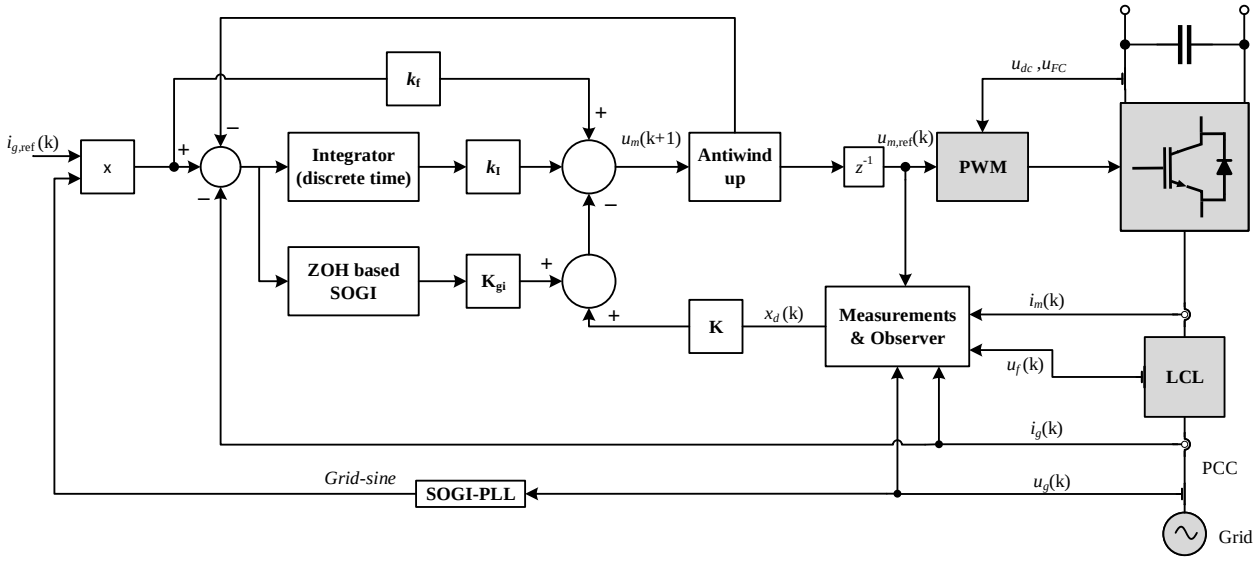


Figure 4.2: Closed loop control structure for the single-phase sFCI.

where k_I is the gain of the integral state, k_f is the feedforward gain, $\mathbf{K} = [k_1 \;\; k_2 \;\; k_3 \;\; k_4]$ is the state-feedback gain, and $\boldsymbol{x}_d = [\boldsymbol{x}^\top \;\; u_m]^\top$ is the state matrix augmented with the delayed voltage reference. The state feedback controller with the integral action included, can be designed to have good damping of the LCL filter resonance and disturbance rejection. The feedforward term is an additional degree of freedom for the design of reference-tracking based controllers [22].

4.2.1 Generalized integrators (GI)

Second order generalized integrators (SOGI) are used for obtaining zero steady state error when using stationary reference frames in grid-connected inverters, rectifiers, active filters and power supplies. These integrators have also been used in algorithms for grid synchronization, detection of sequences and harmonic compensation [64]. A common approach for control design of a single-phase grid-connected inverter is to use stationary frame controllers. Since the control variables are sinusoidal and time varying, proportional resonant (PR) controllers based on a proportional gain and SOGI are employed, due to their ability to eliminate steady state error for sinusoidal references. However, in state-feedback based control approaches, SOGIs can be employed to enable grid phase detection and/or variation in the grid parameters and subsequently minimize or eliminate the generated phase delay [65]. The SOGI can also be employed to generate quadrature-signals, which are very useful in single-phase PLLs (phase-locked-loop). Again, implementation of these algorithms is done using microcontrollers, hence design in discrete time is a necessity.

According to [66], the transfer function of a second order generalized integrator for a single sinusoidal signal is

$$G(s) = \frac{2s}{s^2 + \omega_o^2}. \tag{4.12}$$

Discrete time implementation consists of discretization of the continuous-time transfer function and calculation of difference equations. For the SOGI better results are obtained using zero-order-hold (ZOH) technique [64]. The following transfer function shows the implementation of the SOGI using ZOH discretization.

$$H_{zoh}(z) = \frac{\sin(\omega_o T_s)(z-1)}{z^2 - 2\cos(\omega_o T_s)z + 1} \tag{4.13}$$

Figure 4.3 shows the bode plot of (4.13). It shows that the SOGI has a high gain at 50 Hz. Generally,

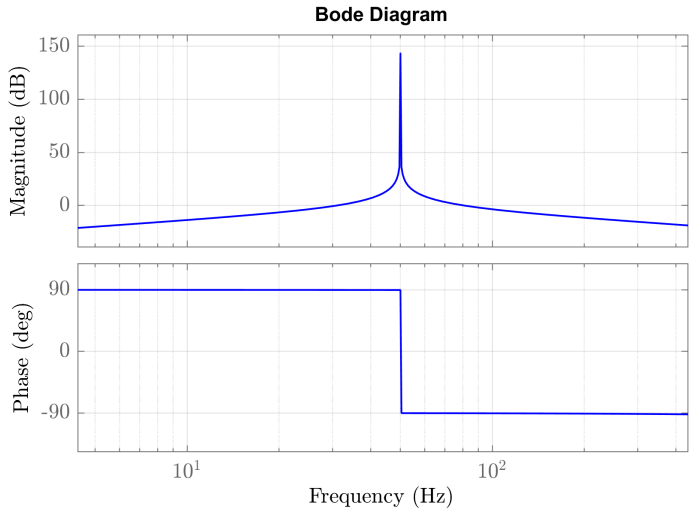


Figure 4.3: Bode plot of ZOH discretization based SOGI.

the basic functionality of the integrator in the controller is to introduce an infinite gain at the selected frequency, for eliminating steady state error at that particular frequency. A disadvantage of the ZOH based approach is that the difference equations have to be calculated off-line as opposed to the Euler approach. However, the discretized system model (4.1) is also based on the ZOH-equivalent model. Hence it makes sense to use ZOH implementation of the SOGI. Figure 4.4 depicts the structure of the SOGI where the sine and cosine gains are related to the tuning frequency of the SOGI, i.e., 50Hz in our case.

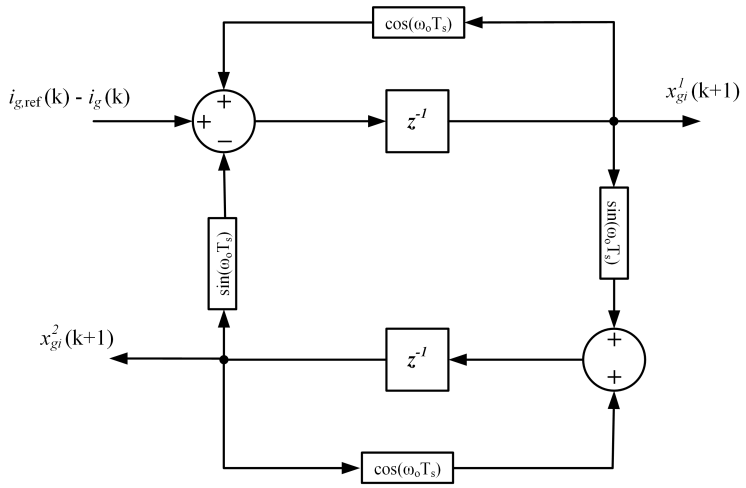


Figure 4.4: SOGI based on ZOH method.

The (discrete time) difference equations for the SOGI can be written as

$$\begin{aligned} x_{gi_1}(k+1) &= \cos(\omega_g T_s) x_{gi_1}(k) - \sin(\omega_g T_s) x_{gi_2}(k) - i_g(k) + i_{g,\text{ref}}(k) \\ x_{gi_2}(k+1) &= \sin(\omega_g T_s) x_{gi_1}(k) + \cos(\omega_g T_s) x_{gi_2}(k) \end{aligned} \tag{4.14}$$

Hence the generalized integrator model becomes

$$\underbrace{\begin{bmatrix} x_{gi_1}(k+1) \\ x_{gi_2}(k+1) \end{bmatrix}}_{\boldsymbol{x}_{gi}(k+1)} = \underbrace{\begin{bmatrix} \cos(\omega_g T_s) & -\sin(\omega_g T_s) \\ \sin(\omega_g T_s) & \cos(\omega_g T_s) \end{bmatrix}}_{\boldsymbol{\Gamma}_{\text{gi}}} \underbrace{\begin{bmatrix} x_{gi_1}(k) \\ x_{gi_2}(k) \end{bmatrix}}_{\boldsymbol{x}_{gi}(k)} + (i_{g,\text{ref}}(k) - i_g(k)) \tag{4.15}$$

$$\text{or} \qquad \boldsymbol{x}_{gi}(k+1) = \boldsymbol{\Gamma}_{\text{gi}} \boldsymbol{x}_{gi}(k) + (i_{g,\text{ref}}(k) - i_g(k))$$

4.2.2 Augmented system for pole placement design

For pole-placement, the system model of (4.7) is augmented with the integral state (4.10) and the generalized integrator (4.15), resulting in

$$\boldsymbol{x}_a(k+1) = \mathbf{A}_\mathrm{a}\boldsymbol{x}_a(k) + \mathbf{B}_\mathrm{a}u_{m,\mathrm{ref}}(k) + \mathbf{E}_\mathrm{a}u_g(k) + \mathbf{P}_\mathrm{a}i_{g,\mathrm{ref}}(k) \tag{4.16}$$

where $\boldsymbol{x}_a = [\boldsymbol{x}_d^\top \;\; x_I \;\; \boldsymbol{x}_{gi}^\top]^\top$ is the augmented state vector, and

$$\begin{aligned}
\mathbf{A}_\mathrm{a} &= \begin{bmatrix} \mathbf{A}_\mathrm{d} & \mathbf{0}_{4\mathrm{x}1} & \mathbf{0}_{4\mathrm{x}2} \\ -\mathbf{C}_\mathrm{d} & 1 & \mathbf{0}_{1\mathrm{x}2} \\ -\boldsymbol{\Gamma}_\mathrm{a} & \mathbf{0}_{2\mathrm{x}1} & \boldsymbol{\Gamma}_\mathrm{gi} \end{bmatrix}_{\mathbb{R}\in 7\mathrm{x}7}; \mathbf{B}_\mathrm{a} = \begin{bmatrix} \mathbf{B}_\mathrm{d} \\ 0 \\ \mathbf{0}_{2\mathrm{x}1} \end{bmatrix}_{\mathbb{R}\in 7\mathrm{x}1}; \mathbf{E}_\mathrm{a} = \begin{bmatrix} \mathbf{E}_\mathrm{d} \\ 0 \\ \mathbf{0}_{2\mathrm{x}1} \end{bmatrix}_{\mathbb{R}\in 7\mathrm{x}1}; \\
\boldsymbol{\Gamma}_\mathrm{a} &= \begin{bmatrix} \mathbf{C}_\mathrm{d} & 0 \\ \mathbf{0}_{1\mathrm{x}4} & 0 \end{bmatrix}_{\mathbb{R}\in 2\mathrm{x}5}; \mathbf{C}_\mathrm{d} = \begin{bmatrix} \mathbf{C} & 0 \end{bmatrix}_{\mathbb{R}\in 1\mathrm{x}4}; \mathbf{P}_\mathrm{a} = \begin{bmatrix} \mathbf{0}_{1\mathrm{x}4} & 1 & 1 & 0 \end{bmatrix}^\top_{\mathbb{R}\in 7\mathrm{x}1}
\end{aligned} \tag{4.17}$$

are the augmented system matrices. Hence, the current control loop is based on a multi-variable pole placement approach, which combines a state-feedback regulator with an integral block and an SOGI to achieve null tracking error. From (4.10), (4.15) and (4.16) the closed loop dynamics become

$$\begin{aligned}
\boldsymbol{x}_a(k+1) &= (\mathbf{A}_\mathrm{a} - \mathbf{B}_\mathrm{a}\mathbf{K}_\mathrm{a})\boldsymbol{x}_a(k) + (\mathbf{B}_\mathrm{a}k_t + \mathbf{P}_\mathrm{a})i_{g,\mathrm{ref}}(k) + \mathbf{E}_\mathrm{a}u_g(k) \\
\boldsymbol{y}(k) &= \mathbf{C}_\mathrm{a}\boldsymbol{x}_a(k)
\end{aligned} \tag{4.18}$$

The augmented state-feedback gain vector $\mathbf{K}_\mathrm{a} = [\mathbf{K} \;\; -k_I \;\; k_6 \;\; k_7]$ where the gains k_6, k_7 are related to the GI. Also the output vector $\mathbf{C}_\mathrm{a} = [0, 0, 1, 0, 0, 0, 0]$. The transfer function from the reference current $i_{g,\mathrm{ref}}(z)$ to the grid side current $i_g(z)$ is written as

$$H_{CL}(z) = \frac{\boldsymbol{n}(z)}{\boldsymbol{d}(z)} = \mathbf{C}_\mathrm{a}(z\mathbf{I} - \mathbf{A}_\mathrm{a} + \mathbf{B}_\mathrm{a}\mathbf{K}_\mathrm{a})^{-1}(\mathbf{B}_\mathrm{a}k_f + \mathbf{P}_\mathrm{a}). \tag{4.19}$$

The denominator polynomial (i.e. the characteristic polynomial) written as

$$\boldsymbol{d}(z) = \det(z\mathbf{I} - \mathbf{A}_\mathrm{a} + \mathbf{B}_\mathrm{a}\mathbf{K}_\mathrm{a}) \tag{4.20}$$

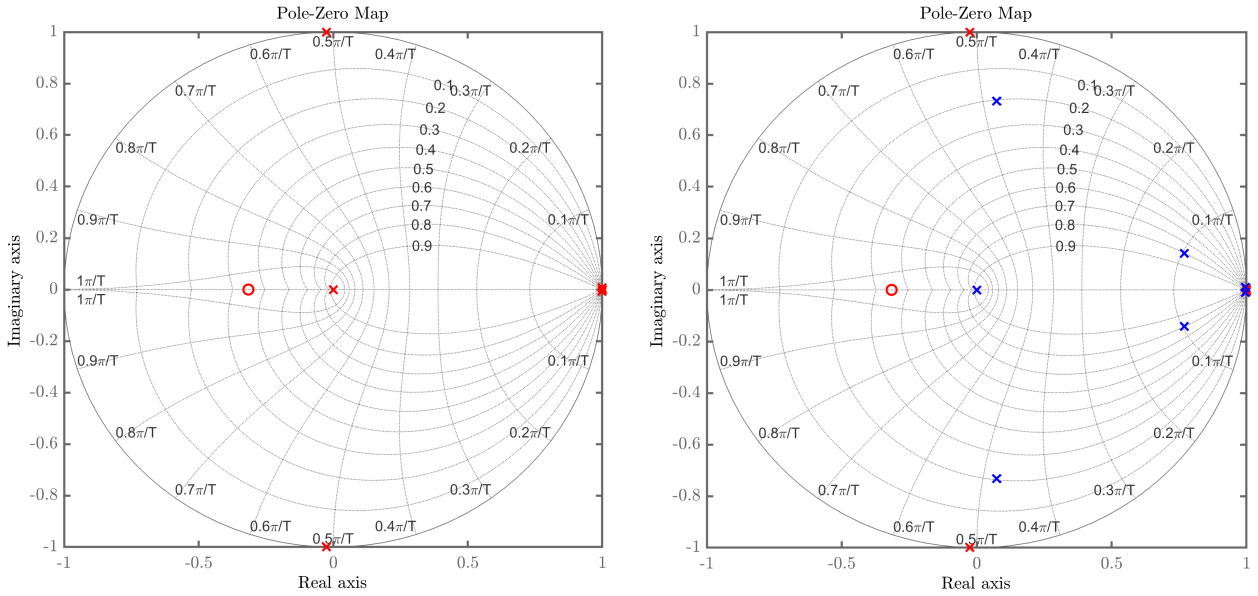
has seven poles, where one pole is originating from the ZOH property of the system, four poles depend on the dynamics of the LCL filter and the remaining two poles depend on the SOGI. The gain vector $\mathbf{K}_\mathrm{a}$ required to calculate the characteristic polynomial can either be solved using numerical tools like MATLAB or using analytical expressions. The former approach was used in this thesis.

4.2.3 Pole placement

A fully controllable system can be controlled by designing the feedback gain matrix using direct pole placement. Selection of the pole locations depends on a compromise between robustness and dynamic response [22, 23]. Figure 4.5(a) shows the poles and zeros of the open-loop transfer function from $u_{m,\mathrm{ref}}(z)$ to $i_g(z)$, obtained from (4.7). Poles and zeros are discrete counterparts of those in (4.2). Furthermore, there is a pole at the origin due to the ZOH property. Let the desired characteristic polynomial be

$$\boldsymbol{d}^*(z) = z(z - \boldsymbol{\alpha}_1)(z - \boldsymbol{\alpha}_2)(z - \boldsymbol{\alpha}_3)(z - \boldsymbol{\alpha}_4)(z - \boldsymbol{\alpha}_5)(z - \boldsymbol{\alpha}_6). \tag{4.21}$$

The poles of the closed-loop system can be arbitrarily placed at desired locations, and the system would respond accordingly. Although, root locus analysis would suggest that the closed-loop poles be placed near the open-loop poles in order to avoid aggressive inputs and/or compromise loop stability. Nevertheless, *near* or *close* is quite ill defined when the number of poles to be placed is significant. It implies, placing n poles explicitly rather than just a nominal area for dominant poles,



(a) (b)

Figure 4.5: Pole-zero plots. (a) Poles and zeros of the open-loop transfer function (red). (b) Closed loop poles set to desired positions (blue).

results in an overly specified design [67]. In practice, poles are placed such that the controller has sufficient bandwidth and the closed-loop offers sufficient damping to the LCL filter resonance.

In the desired characteristic polynomial (4.21), the two complex poles $\boldsymbol{\alpha}_{1,2}$ are placed to determine the dominant behavior (i.e., bandwidth of the controller) and two poles $\boldsymbol{\alpha}_{3,4}$ are placed to determine the resonant behavior (i.e., the resonance damping). To simplify the procedure, poles are specified in the continuous-time domain and them mapped to the discrete domain [22]. The dominant and the resonant behavior can be specified by two second order polynomials as

$$\underbrace{\left(s^2 + 2\zeta_1\omega_1 s + \omega_1^2\right)}_{\text{Dominant behavior}} \underbrace{\left(s^2 + 2\zeta_2\omega_2 s + \omega_2^2\right)}_{\text{Resonant behavior}}. \tag{4.22}$$

Let us first consider the poles related to dominant behavior. The frequency ω_1 specifies the desired bandwidth, selected as $1/20^{th}$ of the switching frequency. The damping ratio ζ_1 is set to a large value to prevent large overshoots. The corresponding discrete poles are

$$\boldsymbol{\alpha}_{1,2} = \exp\left[\left(-\zeta_1 \pm \mathrm{j}\sqrt{1-\zeta_1^2}\right)\omega_1 T_s\right]. \tag{4.23}$$

For damping of the resonant behavior, frequency ω_2 is kept near the natural frequency of the LCL filter ω_r, whereas the damping ratio ζ_2 is chosen to be small. Selecting higher values for ζ_2 is not recommended due to increased control effort [68]. The discrete poles for the resonance damping are

$$\boldsymbol{\alpha}_{3,4} = \exp\left[\left(-\zeta_2 \pm \mathrm{j}\sqrt{1-\zeta_2^2}\right)\omega_2 T_s\right]. \tag{4.24}$$

Furthermore, the pole at the origin due to the ZOH discretization, is not moved. The SOGI introduces a complex-conjugate pair of poles corresponding to its tuning frequency $\omega_g = 2\pi \cdot 50$ rad/s. Since the main aim of using an SOGI is to eliminate the phase-shift, it is sufficient to provide a slight damping to its poles (ζ_d), in order to keep them in the vicinity of the open loop poles and avoid aggressive control inputs which might compromise the loop stability. It should be noted that state-feedback control does not affect the location of zeros. The discrete poles for the SOGI are

$$\boldsymbol{\alpha}_{5,6} = \zeta_d \cdot \exp\left[\omega_g T_s\right]. \tag{4.25}$$

Note that in Figure 4.5 there exists a zero at $z = -3.14$ which is not shown for clarity. Table 4.1 gives an overview of the tuning parameters chosen for pole placement.

Parameter	Value
ζ_1	0.8
ω_1	$2\pi \cdot 1950\,\mathrm{rad\,s^{-1}}$
ζ_2	0.204
ω_2	$2\pi \cdot 10.155\,\mathrm{rad\,s^{-1}}$
ζ_d	0.1

Table 4.1: Tuning parameters for pole placement controller design.

4.2.4 DC voltage feedforward compensation (DVFC)

The input supply of the three-level sFCI is essentially composed of two separate capacitors, i.e., the input *dc*-link capacitor C_{in} and the flying capacitor C_{FC}, that are independently responsible for supplying power in the positive and negative cycles, respectively. Although the input capacitor C_{in} has a constant voltage across it, the flying capacitor has a voltage ripple equal to δ_{FC} across it, see Figure 4.7(b). This variation in the supply voltage has a prominent effect on the output of the converter bridge, discussed previously in the section 3.2. Moreover, the system model (3.22) was derived by neglecting the switching behavior of the converter bridge and the variation in the supply voltage. Therefore, for tackling this abrupt variation of supply voltage a feedforward approach is proposed, depicted in Figure 4.6.

As a general practice, the output of the state-feedback controller $u_{m,\mathrm{ref}}(k)$ [see Figure 4.2], which is fed to the PWM block, is normalized with the input *dc*-link voltage measurement. However, in the present scenario the normalization should be carried out separately for the positive and negative cycles using the voltage measurements across C_{in} and C_{FC}, respectively. In this way the effect of the voltage ripple δ_{FC} and the variation in the supply voltage can be incorporated into the control structure. This approach is termed as DC voltage feedforward compensation (DVFC). DVFC ensures that the controller indirectly maintains the voltage ripple of the flying capacitor below the maximum allowable limit.

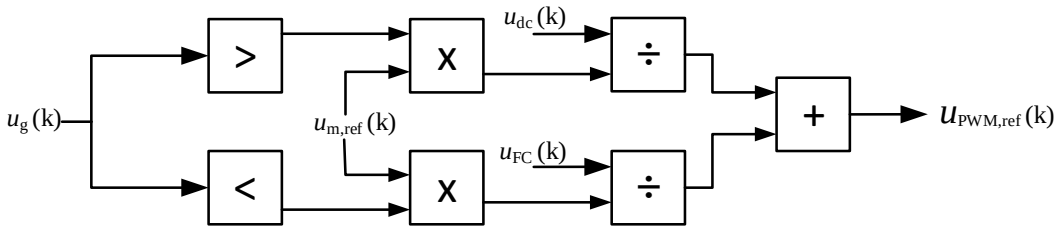


Figure 4.6: Illustration of dc voltage feedforward compensation (DVFC).

4.3 Performance evaluation of state-feedback control for single-phase sFCI

To investigate the performance of the proposed state-feedback current control (SFCC) strategy for the sFCI, several simulations using Matlab/Simulink and PLECS blockset have been conducted. The system parameters for the hardware test-bench are given in Table 3.1 and additional parameters used in the simulations are listed in Table 4.2. The system under consideration is a single-phase sFCI rated for 1.67 kW. Since the resonant frequency of the LCL filter is 10.155 kHz, the switching frequency is set to 40 kHz, i.e., almost 4 times the resonant frequency, in order to avoid any excitation of the filter modes and provide sufficient bandwidth to the control loop. Additionally, a level shifted sinusoidal PWM (SPWM) (see Figure 3.4) with a carrier frequency of 40 kHz is employed to generate the switching signals for the four switches.

Parameter	**Symbol**	**Value**
Switching frequency	f_{sw}	40 kHz
Resonant frequency	ω_r	$2\pi \cdot 10.155\,\mathrm{rad\,s^{-1}}$
Sampling time	T_s	25 µs
Dead time	T_d	300 ns
Nominal grid voltage	u_g	230 V(rms)
Grid Inductance	L_{grid}	0.01 mH
Grid Resistance	R_{grid}	0.1 Ω

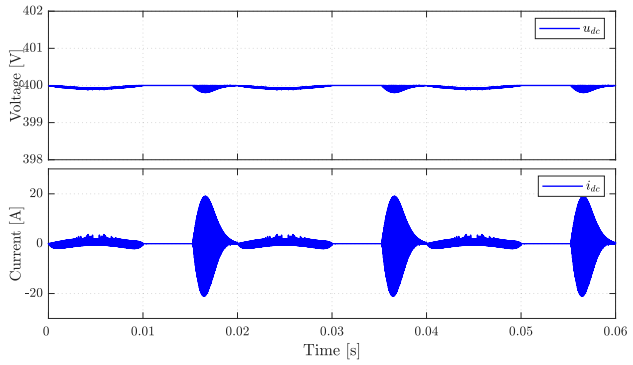
Table 4.2: Additional parameters for simulations.

4.3.1 Steady-state performance

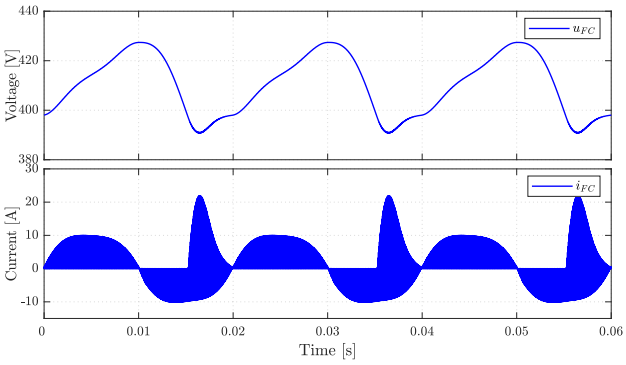
Based on the desired active power of 1.31 kW, the grid current reference (peak) is set to 8 A. Note that the reactive power demand is set to zero. Figure 4.7 shows the steady-state performance of the closed loop system. Figures 4.7(a) and (b) show the voltage and current waveforms of the two *dc* sources of the sFCI. Unlike the conventional NPC converter, where the two *dc*-link capacitors are coupled and make voltage balancing a possibility, the two input *dc* capacitors of the sFCI do not exhibit any coupling between each other, although the flying capacitor is charged using the input capacitor. While the input capacitor C_{in} has a constant voltage across it, the flying capacitor exhibits a voltage ripple $\delta_{FC} \approx 30 - 40$ V . Note that the maximum allowable voltage on the flying capacitor is restricted to 450 V, and therefore the ripple should not exceed this limit. From Figure 4.7(b) we conclude that the proposed SFCC can indirectly control the voltage ripple of the flying capacitor and thus achieves voltage balancing for the flying capacitor.

Figure 4.7(c) shows the output waveform of the converter bridge and compares it to the grid voltage. As can be observed, the controller is able to track the grid voltage properly and generates a voltage pattern that corresponds to the grid voltage in magnitude (average) and phase. From Figure 4.7(d) it is clear that the proposed SFCC achieves reference tracking, with a slight deviation at the zero crossing. This behavior is primarily due to the additional non-linearities, discussed in section 3.2. Moreover, due to the inability of the integral-state to respond quickly to a change in the *dc* source, i.e., from input capacitor to the flying capacitor, the grid current deviates from the reference current.

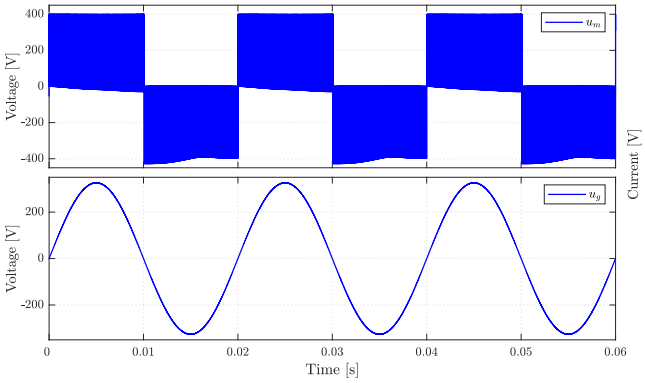
The total harmonic distortion (THD) of the grid current in Figure 4.7(d) is 2.02% (dead-time is 0 ns). However, for a dead-time of 300 ns, see Figure 4.8, the THD of the grid current increases to 3.7%, which also conforms with the standard limit of 5% set for the grid-connected PV inverters [69].



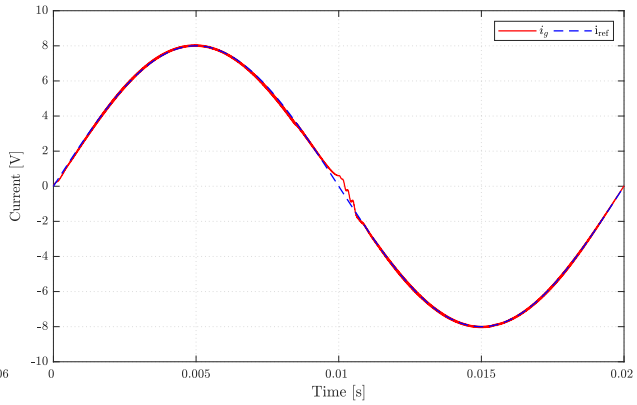
(a) Voltage and current waveforms for the input capacitor.



(b) Voltage and current waveforms for the flying capacitor.



(c) Converter Bridge voltage and the grid voltage.



(d) Comparison of reference current and the grid current.

Figure 4.7: Steady-state performance of the closed loop system using state-feedback control.

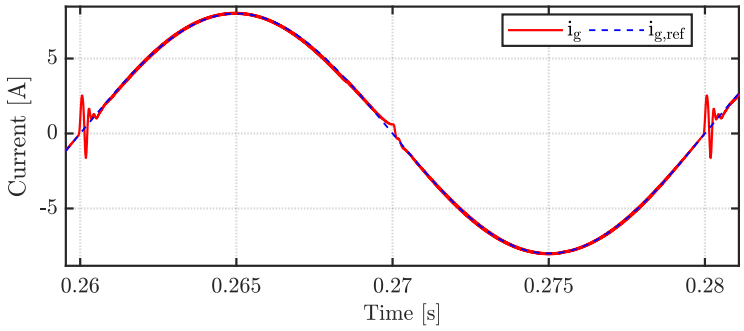
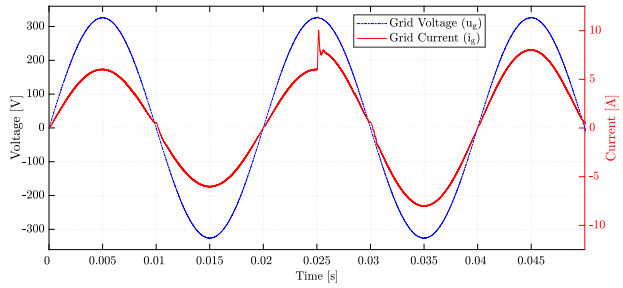


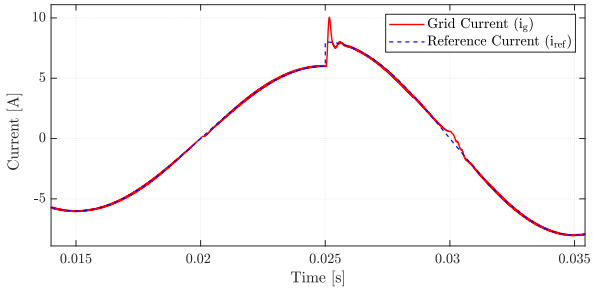
Figure 4.8: Comparison of reference current and the grid current when dead-time = 300 ns.

4.3.2 Dynamic performance

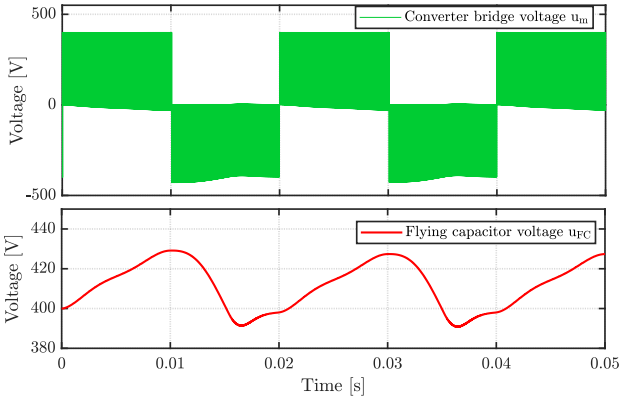
Figures 4.9(a)-(c) shows the dynamic response of the closed loop system for an initial current reference of 6 A ≈ 0.98 kW with a step at 0.025 s to 8 A. Figure 4.9(a) shows a comparison between the grid voltage and the grid current. Since the reactive power demand is set to zero, the grid current follows the grid voltage, i.e., it is in-phase with the grid, implying that the controller achieves grid synchronization. The dynamic response of the SFCC is apparent from Figure 4.9(b) which shows a zoomed view of the comparison between the reference current and the grid current. At 0.025 s the current reference is increased from 6 A to 8 A and it is observed that the controller settles within 2 ms after a small overshoot. From Figure 4.9(c) it is observed that the converter output voltage and the flying capacitor have the same behavior as in steady-state, with an increase in the voltage ripple



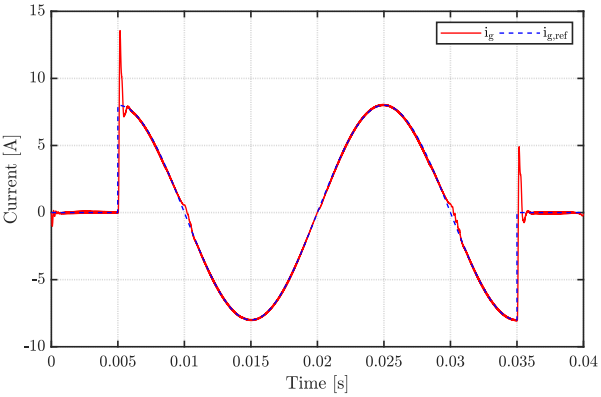
(a) Comparison of grid voltage and current.



(b) Comparison of reference and grid current.



(c) Converter Bridge voltage and C_{FC} voltage.



(d) Transient response of grid current for current variation from 0 A to 8 A to 0 A.

Figure 4.9: Dynamic performance of the closed loop system.

δ_{FC} due to increased current reference. Furthermore, Figure 4.9(d) shows the response of the grid current when the reference current is stepped from 0 A to 8 A and then again to 0 A. Compared to conventional control schemes based on PI approach, the pole placement based SFC offers improved dynamic response and less settling time.

4.3.3 Comparison of bode plots

Figure 4.10 presents the frequency response of the open-loop and closed-loop transfer functions for the single-phase grid-connected sFCI. As can be seen, the closed loop system offers a negative peak at the resonant frequency of the LCL filter. Hence, the state-feedback controller provides inherent resonance damping and does not require any additional damping methods.

4.4 Observer design

For hardware implementation an observer is designed, using the Luenberger Observer concept [70], to estimate the unmeasured states u_f and i_g. The observer dynamics, in discrete-time, with estimated state vector $\widehat{\boldsymbol{x}} = [\,\widehat{i}_m, \widehat{u}_f, \widehat{i}_g\,]^\top$ are given by

$$\begin{aligned} \widehat{\boldsymbol{x}}(k+1) &= \mathbf{A}\widehat{\boldsymbol{x}}(k) + \mathbf{B}\widehat{u}_m(k) + \mathbf{E}\widehat{u}_g(k) + \widehat{u}_{obs} \\ \widehat{y}(k) &= \mathbf{C}\widehat{\boldsymbol{x}}(k) \end{aligned} \tag{4.26}$$

with the observer feedback defined as

$$\widehat{u}_{obs} = \mathbf{L}(y(k) - \widehat{y}(k)) = \mathbf{LC}(\boldsymbol{x}(k) - \widehat{\boldsymbol{x}}(k)) \tag{4.27}$$

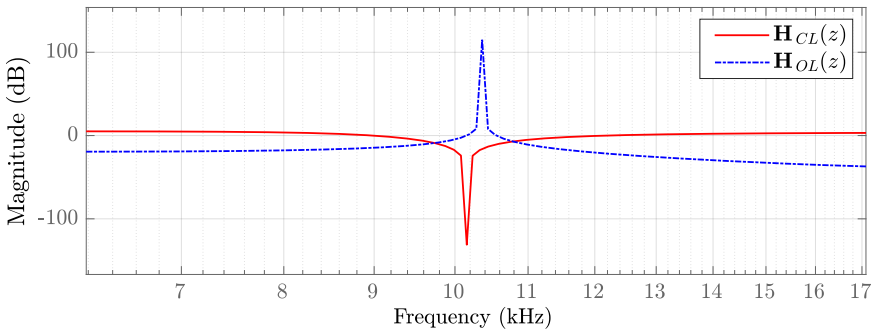


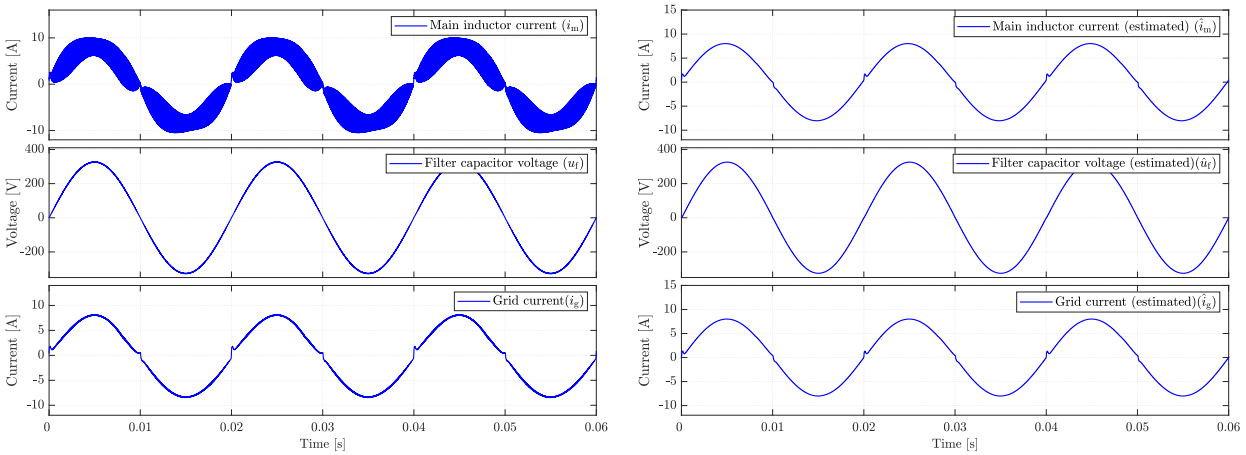
Figure 4.10: Frequency response of the closed-loop transfer function (4.19) (H_{CL}) from the reference current $i_{g,\text{ref}}(z)$ to the grid side current $i_g(z)$. The open-loop transfer function is obtained from (4.5) as $H_{OL} = \mathbf{C}(z\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}$.

where $\mathbf{L}$ is the observer gain vector, and has to be chosen such that the eigenvalues of $[\mathbf{A} - \mathbf{LC}]$ lie within the unit circle. Sensitivity to measurement noise and dynamic response of the observer play a vital role while selecting the pole locations. A rule of thumb to select the observer poles is to set them at least twice as fast as the controller dynamics [22, 68]. The characteristic equation for the estimation-error dynamics is

$$\boldsymbol{\alpha}_o(z) = \det(z\mathbf{I} - \mathbf{A} + \mathbf{LC}) \tag{4.28}$$

The poles of $\boldsymbol{\alpha}_o(z)$ can be mapped via continuous-time placement to independently set the dominant dynamics and the complex-conjugate parts. However, since the system is completely observable, pole locations can be chosen arbitrarily inside the unit circle. The latter approach was preferred in this thesis and the observer poles were placed in the vicinity of the origin, as per the dead-beat approach. Due to its inherent filtering property, this approach allows the observer to have higher dynamic performance.

Figure 4.11 shows the response of the observer where (a) depicts the original state measurements and (b) depicts the estimated states from the observer. It is apparent that the estimated states from the observer correspond to the actual state measurements.



(a) Measured states of the LCL filter.

(b) Estimated states of the LCL filter.

Figure 4.11: Steady-state performance of the observer.

4.5 Controller design for a three-phase sFCI

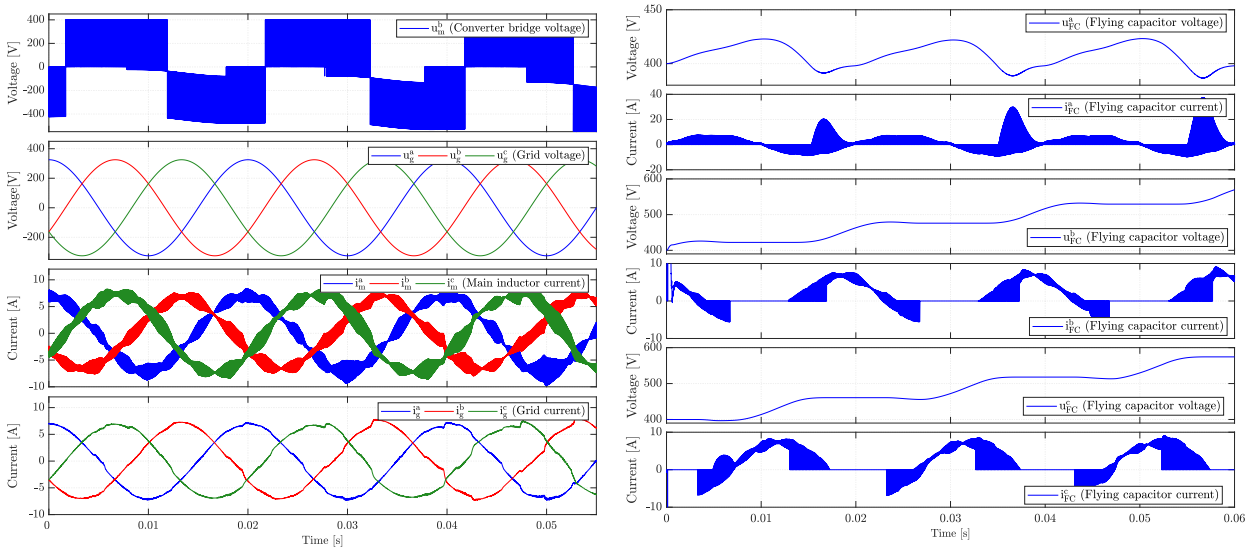
4.5.1 Motivation

The design of state-feedback controller for the single-phase sFCI was discussed in the previous sections. Generally, a controller designed in the (a, b, c)-reference frame for a single-phase inverter can be extended to a three-phase inverter by creating separate controllers for each phase. In this manner no extra transformations are required, and the control design is simple.

Figure 4.12 shows the response of the three-phase sFCI for a controller designed in (a, b, c)-reference frame, as indicated above. For the few initial cycles, the controller synchronizes with the grid and achieves reference tracking for the grid current. However, balancing of the voltage ripple on the flying capacitors only works for one of the phases while for the other two phases the voltage on the flying capacitors increases beyond the allowed limit, i.e., 450 V (termed as voltage fly-away) after a few cycles of operation, see Figure 4.12(b). Hence, a controller designed in (a, b, c)-reference frame does not fulfill all the control objectives.

Furthermore, design of the controller in the stationary (α, β)-reference frame and the rotating (d, q)-reference frame was investigated. The stationary (α, β)-reference frame controller gives a response similar to the (a, b, c)-reference frame controller, with the flying capacitor voltage exceeding the allowed limit (450 V) in phases b and c. However, the (d, q)-reference frame controller shows promising performance and is able to achieve both reference tracking and flying capacitor voltage control. Hence, it can be concluded that the three phases of the sFCI possess some inherent coupling due to the presence of flying capacitors.

In the following sections, design of the controller for three-phase sFCI in the rotating (d, q)-reference frame is discussed.



(a) Converter bridge voltage and states of LCL filter.

(b) Behavior of the three flying capacitors.

Figure 4.12: Closed loop results for three phase sFCI using controller designed in (a, b, c)-reference frame.

4.5.2 Mathematical model of the converter

The rotating (d,q)-reference frame is aligned with the grid voltage[1] (voltage orientation), i.e.,

$$\boldsymbol{u}_g^k(t) = u_g^d(t) + \mathrm{j}u_g^q(t) = \hat{u}_g(t) + \mathrm{j}0. \tag{4.29}$$

Using the Clarke transformation (3.5) and Park transformation (3.8) in (3.22) yields the system model in the (d,q)-reference frame. The continuous time model in the (d,q) frame can be written as

$$\frac{\mathrm{d}\boldsymbol{x}^{dq}(t)}{\mathrm{d}t} = \mathbf{F}\boldsymbol{x}^{dq}(t) + \mathbf{G}\boldsymbol{u}_m^{dq}(t) + \mathbf{T}\boldsymbol{u}_g^{dq}(t) \tag{4.30a}$$

$$\boldsymbol{y}(t) = \mathbf{C}\boldsymbol{x}^{dq}(t) \tag{4.30b}$$

where the state vector is $\boldsymbol{x}^{dq} = [i_m^d \;\; i_m^q \;\; u_f^d \;\; u_f^q \;\; i_g^d \;\; i_g^q]^\top$ and the system matrices are

$$\mathbf{F} = \begin{bmatrix} -\frac{R+R_m}{L_m} & \omega_g & -\frac{1}{L_m} & 0 & \frac{R}{L_m} & 0 \\ -\omega_g & -\frac{R+R_m}{L_m} & 0 & -\frac{1}{L_m} & 0 & \frac{R}{L_m} \\ \frac{1}{C_f} & 0 & 0 & \omega_g & -\frac{1}{C_f} & 0 \\ 0 & \frac{1}{C_f} & -\omega_g & 0 & 0 & -\frac{1}{C_f} \\ \frac{R}{L_g} & 0 & \frac{1}{L_g} & 0 & -\frac{R+R_g}{L_g} & \omega_g \\ 0 & \frac{R}{L_g} & 0 & \frac{1}{L_g} & -\omega_g & -\frac{R+R_g}{L_g} \end{bmatrix}; \mathbf{G} = \begin{bmatrix} \frac{1}{L_f} & 0 \\ 0 & \frac{1}{L_f} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}; \mathbf{T} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ -\frac{1}{L_g} & 0 \\ 0 & -\frac{1}{L_g} \end{bmatrix}. \tag{4.31}$$

Since the q-axis is 90° ahead of the d-axis, i.e., $\xi^q = \mathrm{j}\cdot\xi^d$ or $\xi^d = -\mathrm{j}\cdot\xi^q$, complex valued space vectors (e.g., the main inductor current $\boldsymbol{i}_m = i_m^d + \mathrm{j}\, i_m^q$) can be used to represent the system (4.30), (4.31) as follows

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \underbrace{\begin{bmatrix} -\frac{R+R_m}{L_m} - \mathrm{j}\omega_g & -\frac{1}{L_m} & \frac{R}{L_m} \\ \frac{1}{C_f} & -\mathrm{j}\omega_g & -\frac{1}{C_f} \\ \frac{R}{L_g} & \frac{1}{L_g} & -\frac{R+R_g}{L_g} - \mathrm{j}\omega_g \end{bmatrix}}_{\mathbf{F}} \boldsymbol{x}(t) + \underbrace{\begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{G}} \boldsymbol{u}_m(t) + \underbrace{\begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L_g} \end{bmatrix}}_{\mathbf{T}} \boldsymbol{u}_g(t) \tag{4.32a}$$

$$\boldsymbol{y}(t) = \underbrace{\begin{bmatrix} 0 & 0 & 1 \end{bmatrix}}_{\mathbf{C}} \boldsymbol{x}(t) \tag{4.32b}$$

The input matrices remain unchanged as there are no coupling terms. Since the imaginary part signifies the coupling between respective components, a complex-valued gain vector $\mathbf{K} \in \mathbb{R}^n$ can be back-transformed to the (d,q) frame using:

$$\begin{bmatrix} \mathbf{K}^d \\ \mathbf{K}^q \end{bmatrix} = \begin{bmatrix} \mathfrak{Re}(K_0) & \mathfrak{Im}(K_0) & \mathfrak{Re}(K_1) & \mathfrak{Im}(K_1) & \dots & \mathfrak{Re}(K_{n-1}) & \mathfrak{Im}(K_{n-1}) \\ -\mathfrak{Im}(K_0) & \mathfrak{Re}(K_0) & -\mathfrak{Im}(K_1) & \mathfrak{Re}(K_1) & \dots & -\mathfrak{Im}(K_{n-1}) & \mathfrak{Re}(K_{n-1}) \end{bmatrix} \tag{4.33}$$

4.5.3 Grid synchronization in power converters

Grid synchronization implies, the accurate detection of the phase angle and other attributes of the grid voltage, in order to tune an internal oscillator of the power converter to the oscillatory dynamics imposed by the grid. Usually the main attributes to enable grid connection, via power converters, are the phase angle and the amplitude of the fundamental frequency component of the grid voltage [71]. Grid synchronization techniques can be classified into two groups, namely the time-domain and the frequency-domain methods.

The time-domain detection methods are based on some kind of adaptive loop that tracks the specific component of input signal. The most commonly employed synchronization method is based

[1] Note: $\boldsymbol{u}_g^k(t) = \mathbf{T}_\mathrm{p}(\phi_g)^{-1}\mathbf{T}_\mathrm{c}\boldsymbol{u}_g^{abc}(t)$, where the angle $\phi_g(t) = \omega_g t$.

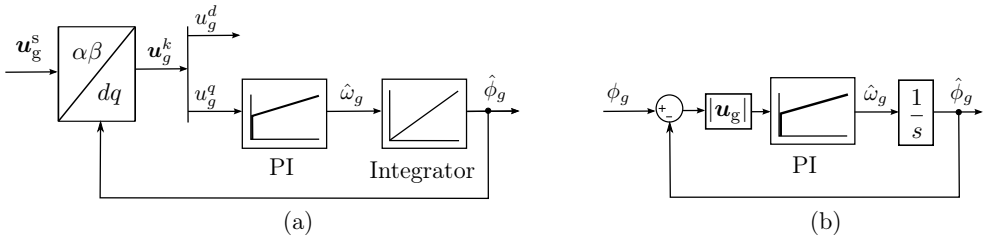


Figure 4.13: (a) Phase-locked-loop (PLL) for grid synchronization, and (b) block diagram of a PLL.

on a phase-locked-loop (PLL). A PLL is a closed loop system in which an oscillator is used to track the fundamental component of the grid voltage and calculate its phase-angle and amplitude. The structure of a PLL used for grid synchronization is shown in Figure 4.13(a). The aim of the PLL is to drive the quadrature q-component of the grid voltage to zero i.e., $\boldsymbol{u}_g = u_g^d + \mathrm{j}0$. From Figure 4.13(a) the q-component of the grid voltage can be written as

$$\begin{aligned} u_g^q &= -u_g^\alpha \sin(\hat{\phi}_g) + u_g^\beta \cos(\hat{\phi}_g) \\ &= -u_g \cos(\phi_g)\sin(\hat{\phi}_g) + u_g \sin(\phi_g)\cos(\hat{\phi}_g) \\ &= u_g \sin(\phi_g - \hat{\phi}_g) \approx u_g(\phi_g - \hat{\phi}_g) \end{aligned} \tag{4.34}$$

where u_g^α and u_g^β are the components of the grid voltage $\boldsymbol{u}_g^s$ in stationary reference frame, and $\hat{\phi}_g$ is the angle estimated by the PLL. Similarly, the d-component of the grid voltage can be written as

$$\begin{aligned} u_g^d &= u_g^\alpha \cos(\hat{\phi}_g) - u_g^\beta \sin(\hat{\phi}_g) \\ &= u_g \cos(\phi_g)\cos(\hat{\phi}_g) - u_g \sin(\phi_g)\sin(\hat{\phi}_g) \\ &= u_g \cos(\phi_g - \hat{\phi}_g) \end{aligned} \tag{4.35}$$

If the estimated angle of the PLL ($\hat{\phi}_g$) and the grid phase-angle (ϕ_g) are equal, i.e., $\hat{\phi}_g = \phi_g$, the q-component u_g^q will become negligible, and the d-component u_g^d will be equal to the amplitude of the grid voltage $\boldsymbol{u}_g^s$. A linearized block diagram of the PLL, considering (4.34), is shown in Fig. 4.13(b). The transfer function from (ϕ_g) to ($\hat{\phi}_g$) is written as

$$\boldsymbol{H}_{PLL}(s) = \frac{u_g(k_p s + k_i)}{s^2 + u_g k_p s + u_g k_i} \tag{4.36}$$

A comparison between the coefficients of the denominator polynomial of $\boldsymbol{H}_{PLL}(s)$ and a second-order polynomial $s^2 + 2\zeta_n\omega_n s + \omega_n^2$ yields the PI controller gains k_p and k_i of the PLL as

$$k_p = \frac{2\zeta_n\omega_n}{u_g}; \qquad k_i = \frac{\omega_n^2}{u_g}. \tag{4.37}$$

where k_p is the proportional gain, k_i is the integral gain, ω_n is the undamped natural frequency, and ζ_n is the damping factor. Figure 4.14 shows the output of the PLL block w.r.t the voltage of the phase-a.

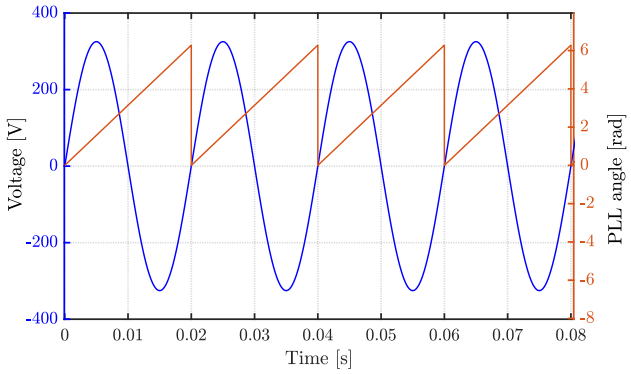


Figure 4.14: Output of the phase-locked-loop (PLL).

4.5.4 Controller design

Invoking the assumptions (A.4), (A.5) and (A.6), model of the LCL filter/grid with complex valued terms (4.32) is re-written as

$$\frac{d\boldsymbol{x}(t)}{dt} = \underbrace{\begin{bmatrix} -\mathrm{j}\omega_g & -\frac{1}{L_m} & 0 \\ \frac{1}{C_f} & -\mathrm{j}\omega_g & -\frac{1}{C_f} \\ 0 & \frac{1}{L_g} & -\mathrm{j}\omega_g \end{bmatrix}}_{\mathbf{F}} \boldsymbol{x}(t) + \underbrace{\begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{G}} \boldsymbol{u}_m(t) + \underbrace{\begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L_g} \end{bmatrix}}_{\mathbf{T}} \boldsymbol{u}_g(t) \tag{4.38a}$$

$$\boldsymbol{y}(t) = \underbrace{\begin{bmatrix} 0 & 0 & 1 \end{bmatrix}}_{\mathbf{C}} \boldsymbol{x}(t) \tag{4.38b}$$

The current control structure for the three-phase sFCI is shown in Figure 4.15. The model (4.38) is discretized and extended with an integral state, following the steps described in the sections 4.1 and 4.2. For pole placement, the augmented system matrix for the three-phase sFCI has five poles that are to be placed to set the dominant and resonant dynamics of the current controller. The pole placement procedure is similar to the method described in section 4.2.3. However, the calculated gain vector $\mathbf{K}$ is complex valued and must be back-transformed to the (d, q)-frame using (4.33). Note that the grid synchronization is carried using the PLL output, therefore poles related to the SOGI are not used in the three-phase approach.

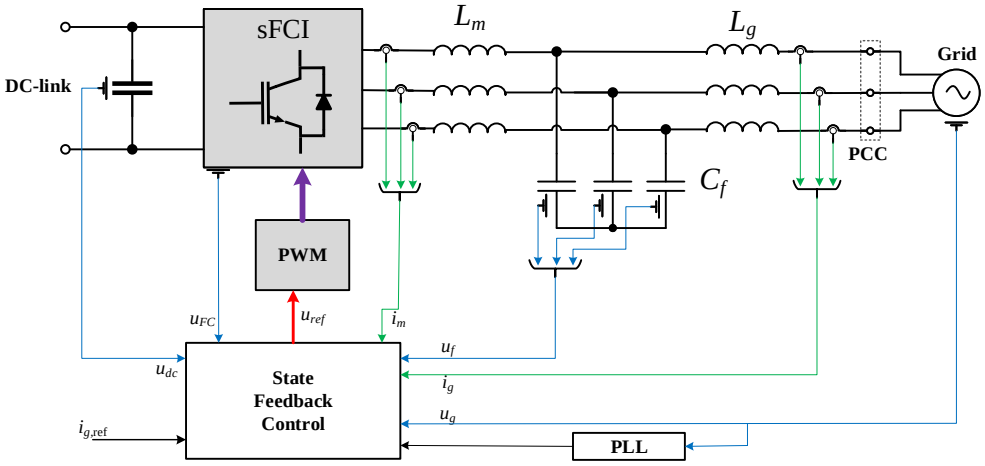
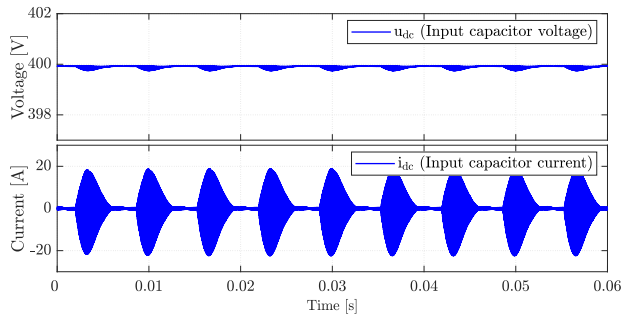


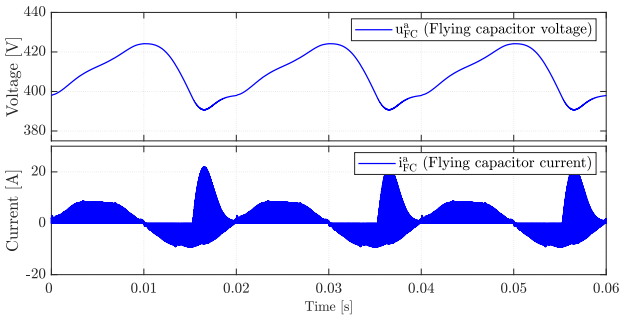
Figure 4.15: Closed loop control structure for three-phase sFCI.

4.6 Performance evaluation of state-feedback control for three-phase sFCI

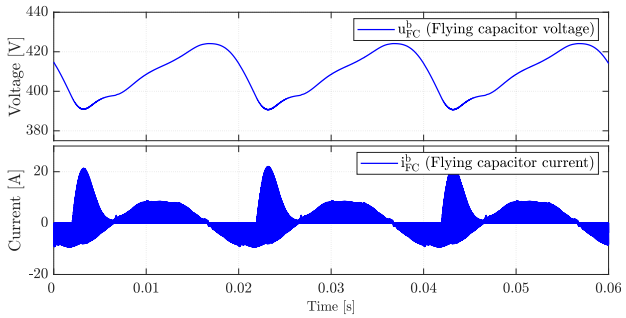
To investigate the performance of the proposed state-feedback current control (SFCC) scheme for the three-phase sFCI, several simulations using Matlab/Simulink and PLECS blockset have been conducted. The system parameters for the hardware test-bench are given in Table 3.1 and Table 4.2. The system under consideration is a three-phase sFCI rated for 5 kW. Please note that a dead-time of 300 ns is valid for all the simulations in this section.



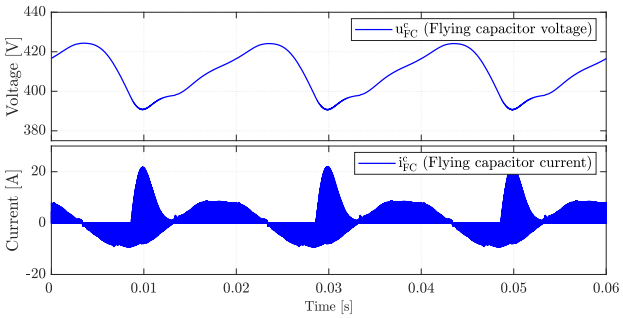
(a) Input capacitor waveforms.



(b) Flying capacitor of the phase-a.



(c) Flying capacitor of the phase-b.

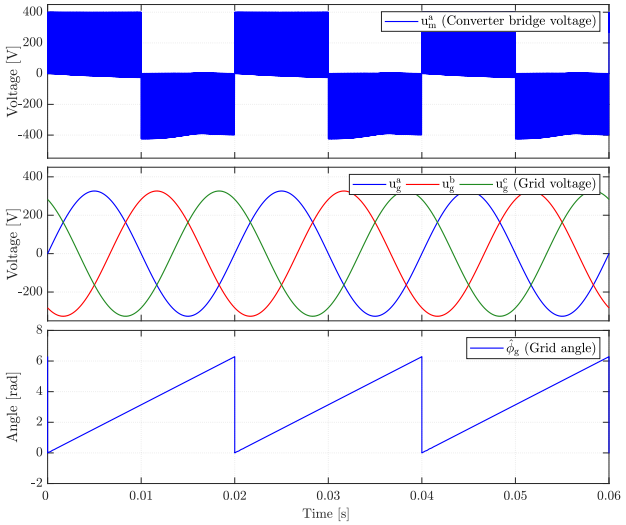


(d) Flying capacitor of the phase-c.

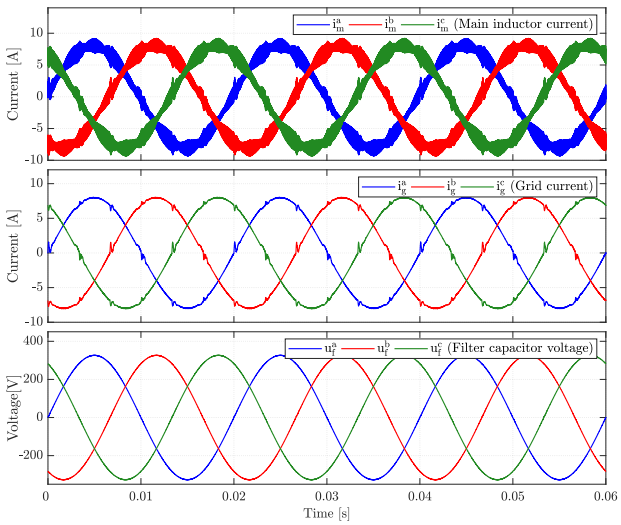
Figure 4.16: Steady-state simulation results for three-phase sFCI using controller designed in (d, q)-reference frame.

4.6.1 Steady-state performance

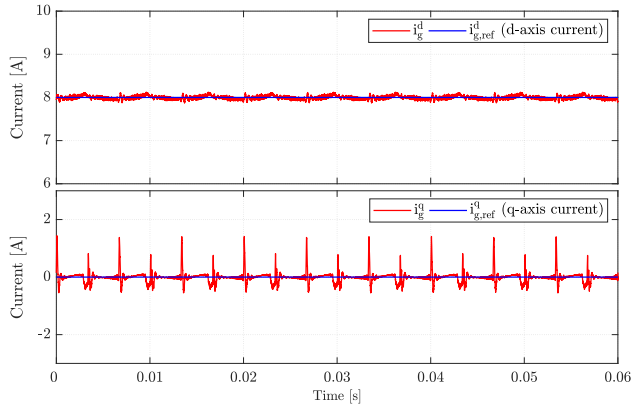
Based on the desired active power of 3.9 kW, the grid current reference is set to 8 A for each phase. The reactive power demand is set to zero. Figures 4.16 and 4.17 shows the steady-state performance of the three-phase sFCI. From Figure 4.16, which shows the voltage and current waveforms for the input dc-link and the three flying capacitors, we can infer that the controller achieves voltage control of all the three flying capacitors. Figure 4.17(a) shows the output of the converter phase-a and the grid voltage of the three phases. It also shows the output angle of the PLL as it tracks the phase-a and makes grid synchronization possible. Figure 4.17(b) shows the waveforms of the three states of the LCL filter. Compared to the main inductor current, the grid current has negligible current-ripple and thus lower harmonic content, implying that the LCL filter offers excellent attenuation of the switching frequency harmonics. Figure 4.17(c), which shows the steady-state performance of the d and q axis currents, highlights the reference tracking of the SFCC.



(a) Voltage waveforms and grid angle from the PLL.



(b) Waveforms for the states of the LCL filter.



(c) Steady-state performance of i_d and i_q w.r.t. their reference values.

Figure 4.17: Steady-state performance of the three-phase sFCI using state-feedback control.

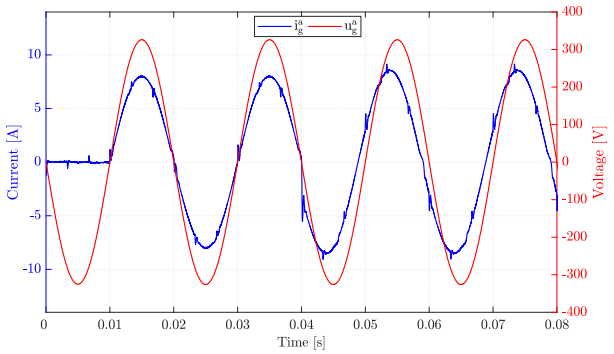
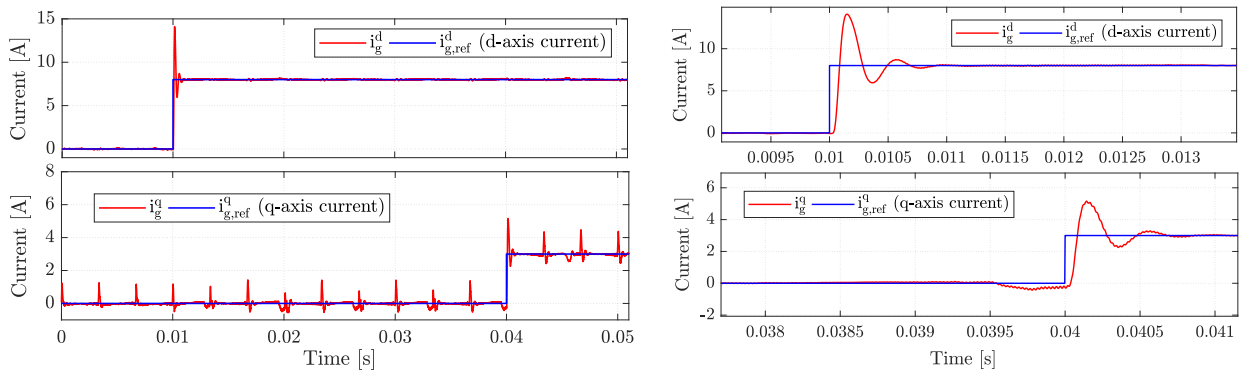


Figure 4.18: Dynamic performance of SFC: comparison of grid current and grid voltage of the phase-a.

4.6.2 Dynamic performance

Figures 4.18, 4.19 and 4.20 illustrate the dynamic performance of the SFCC. At 0.01 s the desired active power is set to 3.9 kW $\approx i_d = 8$ A (per phase), and at 0.04 s the reactive power demand is set



(a) Dynamic performance of i_d and i_q w.r.t. their reference values.

(b) Dynamic performance of the controller (zoomed view).

Figure 4.19: Closed loop simulation results for three-phase sFCI.

to 1.5 kVAr $\approx i_q = 3$ A (per phase). From Figure 4.18 it is observed that the grid current follows the grid voltage when there is no reactive power demand, and has a phase-shift w.r.t the grid voltage when the reactive power demand is set to 1.5 kVAr. From Figures 4.19(a) and (b) it is concluded that the SFCC offers excellent dynamic performance and has a settling time of less than 10 ms.

Figure 4.20, which presents a comparison between the actual grid current and its reference values, signifies the reference tracking of the proposed state-feedback current controller. In Figure 4.20, the sharp peaks in the grid current response arise due to two reasons: 1) due to the introduction of dead-time into the PWM block, and 2) due to the inherent coupling between the three flying capacitors. From this figure we can also observe that whenever any one of the phases undergoes transition from positive to negative cycle, the deviation in grid current affects all the other phases, thereby confirming that there exists some inherent coupling. This behavior requires a deeper study of this topology and is out of the scope of this thesis. Nevertheless, the grid current with all these distortions is observed to have an average THD of 2.25 %.

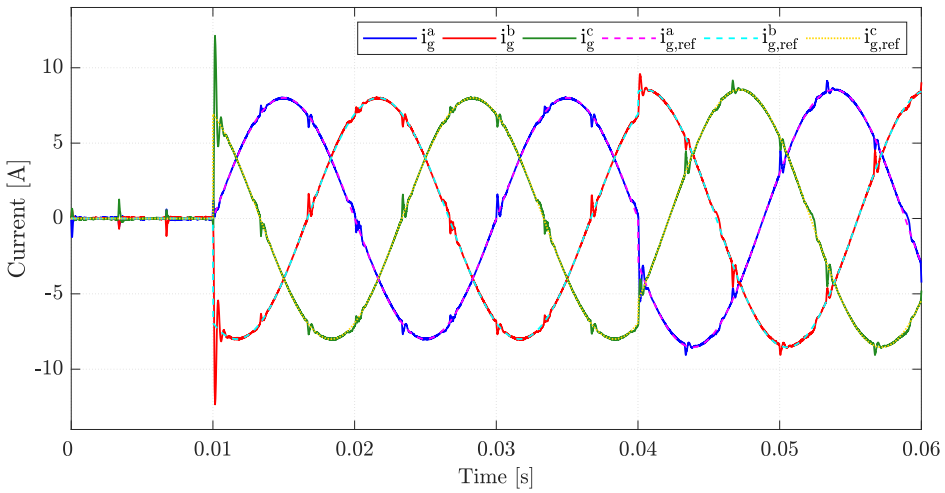


Figure 4.20: Dynamic performance of the (d, q)-reference frame controller: comparison of grid currents and their references.

4.7 Summary

This chapter proposed a state-feedback based current control scheme for the single-phase and three-phase sFCI, connected to the grid via an LCL filter. To achieve an improved dynamic and steady-state performance, a pole-placement based control design approach was discussed. The simulation results show that higher dynamic performance and better resonance damping can be achieved with the proposed controller in comparison with conventional linear control techniques. The results also show that the resonance of the LCL filter is well damped, and the dynamic performance specified by direct pole placement is obtained for the reference tracking, grid voltage disturbance rejection, and balancing of flying capacitor voltages.

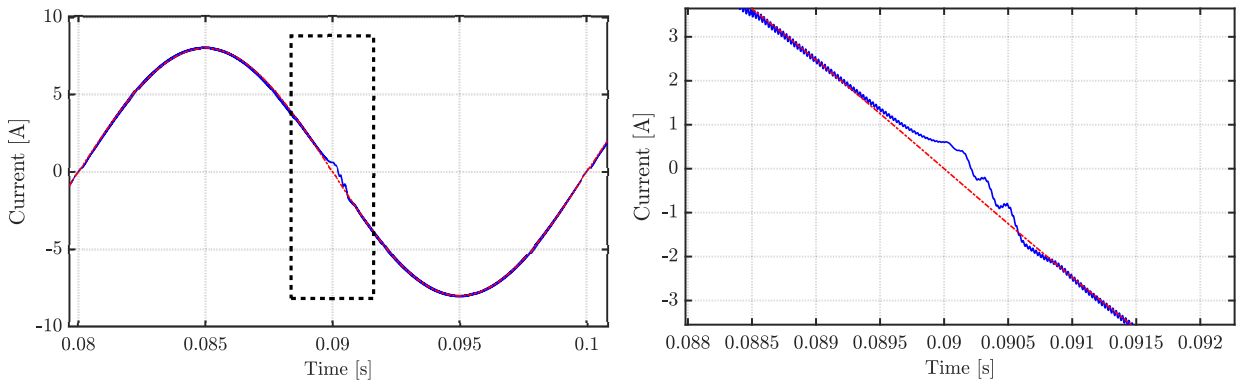
Chapter 5

Model Predictive Control using a Linearized Converter Model

This chapter begins with the motivation for using model predictive control (MPC) to control a three-phase sFCI. The first part of this chapter presents a finite-control-set MPC scheme with a prediction horizon of three. The second part of this chapter discusses the drawbacks of finite-control-set MPC and presents a model predictive control scheme using a continuous-control-set, where a modulator is required for generation of firing signals.

5.1 Motivation

Considering the additional non-linearities present in the sFCI topology, particularly the deviation of the grid current from its reference when the inverter operation changes from the positive cycle to the negative cycle, see Figure 5.1, it can be reasoned that a linear control technique like state-feedback control does not provide sufficient dynamic performance. Figure 5.1(b) shows a zoomed view of the grid current at the zero crossing where the inverter operation changes scheme. At this moment,



(a) (b)

Figure 5.1: Comparison of the grid current and its reference to highlight the deviation at zero crossing. (a) comparison for a single cycle, (b) zoomed view around zero crossing when the inverter supply changes from input *dc*-link to flying capacitor.

the flying capacitor starts discharging (negative state) and supplies power to the load, instead of the input *dc*-link. This changeover of input sources was tackled using a feed-forward approach known as DVFC, see section 4.2. However, the state-feedback controller is unable to react abruptly to this behavior and hence the output current deviates from its reference. From Figure 5.1 it is

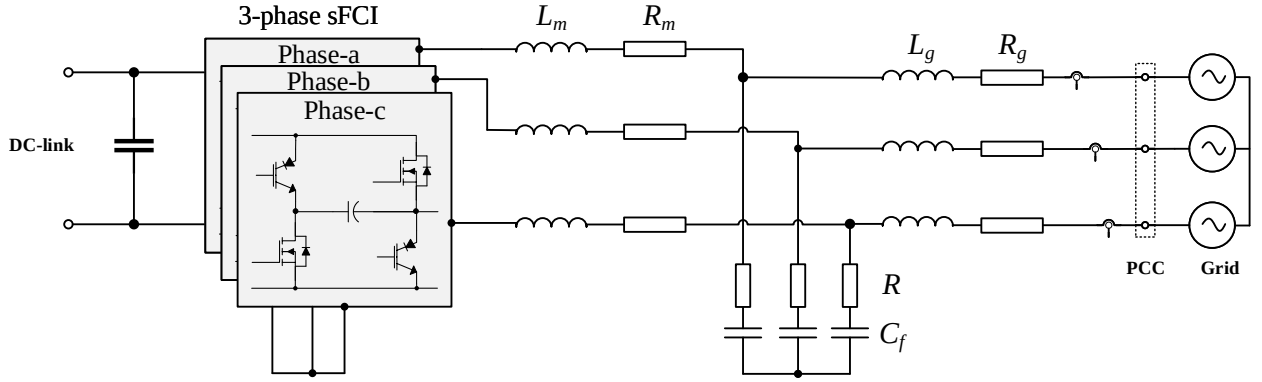


Figure 5.2: Three-phase Siwakoti-H flying capacitor inverter connected to the grid using LCL filter.

observed that the initial overshoot is followed by an oscillatory response due to the SOGI and the later undershoot is when the integral state reacts to this deviation and tries to minimize the error.

Unlike state-feedback control, predictive control techniques offer faster dynamic response, lower settling time and a provision to handle various non-linearities including system constraints. In the following sections a model predictive control (MPC) based scheme is designed to simultaneously control the main-inductor current, the filter capacitor voltage and the grid-side current by means of reference tracking.

5.2 Finite-control-set model predictive control (FCS-MPC)

In this section a FCS-MPC based strategy is introduced to control the sFCI. FCS-MPC departs from the concept of using a modulator as switching signals are generated directly from the controller stage. The objectives of the controller are to minimize tracking error and maintain the ripple voltage of the flying capacitor within the allowed limits. To achieve these control goals, a model of the system is derived that accurately predicts its behavior over the whole operating regime.

5.2.1 Continuous-time mathematical model

Figure 5.2 shows the configuration of a three-phase sFCI connected to the grid using an LCL filter. The LCL filter with main inductor L_m, grid-side inductor L_g and filter capacitor C_f provides sufficient attenuation to the switching frequency harmonics present in the main inductor current i_m. To simplify the modeling and ease the control design, the variables are expressed in the stationary (α, β)-reference frame instead of the three-phase system (a, b, c). A variable $\boldsymbol{\xi}^{abc} := [\xi_a \;\; \xi_b \;\; \xi_c]^\top$ can be transformed to a variable $\boldsymbol{\xi}^{\alpha\beta} := [\xi^\alpha \;\; \xi^\beta]^\top$ in the (α, β) system through $\boldsymbol{\xi}^{\alpha\beta} = \mathbf{T}_\mathrm{c}\, \boldsymbol{\xi}^{abc}$, where $\mathbf{T}_\mathrm{c}$ is the Clarke transformation matrix defined in section 3.3.

The system states include the main inductor currents, the grid currents and filter capacitor voltages. Thus, the state vector is $\boldsymbol{x} = [i_m^\alpha \;\; i_m^\beta \;\; u_f^\alpha \;\; u_f^\beta \;\; i_g^\alpha \;\; i_g^\beta]^\top \in \mathbb{R}^6$. The three-phase switch position $\boldsymbol{s}^{abc} \in \mathcal{S}^3$ is considered as the input to the system, with $\boldsymbol{s}^{abc} = [s_a \;\; s_b \;\; s_c]^\top$ and $\mathcal{S}^3 = \{-1, 0, 1\}$. Moreover, the grid voltage is considered as a disturbance to the system. A continuous-time model of the three-phase LCL filter/grid system, in the rotating (d, q)-reference frame was derived in section 4.5. Neglecting the coupling terms between the various axes transforms the model to the (α, β) system. The system model in the (α, β)-frame is thus written as

$$\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{x}^{\alpha\beta}(t) = \mathbf{F}\boldsymbol{x}^{\alpha\beta}(t) + \mathbf{G}\boldsymbol{u}_m^{\alpha\beta}(t) + \mathbf{T}\boldsymbol{u}_g^{\alpha\beta}(t) \tag{5.1a}$$

$$\boldsymbol{y} = \mathbf{C}\boldsymbol{x}^{\alpha\beta}(t) \tag{5.1b}$$

where the system matrices are

$$\mathbf{F} = \begin{bmatrix} -\frac{R+R_m}{L_m} & 0 & -\frac{1}{L_m} & 0 & \frac{R}{L_m} & 0 \\ 0 & -\frac{R+R_m}{L_m} & 0 & -\frac{1}{L_m} & 0 & \frac{R}{L_m} \\ \frac{1}{C_f} & 0 & 0 & 0 & -\frac{1}{C_f} & 0 \\ 0 & \frac{1}{C_f} & 0 & 0 & 0 & -\frac{1}{C_f} \\ \frac{R}{L_g} & 0 & \frac{1}{L_g} & 0 & -\frac{R+R_g}{L_g} & 0 \\ 0 & \frac{R}{L_g} & 0 & \frac{1}{L_g} & 0 & -\frac{R+R_g}{L_g} \end{bmatrix}, \mathbf{G} = \begin{bmatrix} \frac{1}{L_f} & 0 \\ 0 & \frac{1}{L_f} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \mathbf{T} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ -\frac{1}{L_g} & 0 \\ 0 & -\frac{1}{L_g} \end{bmatrix},$$

$$\mathbf{C} = \mathbf{I}_{6\times 6}, \text{ and } \boldsymbol{\xi}^{\alpha\beta} = \mathbf{T}_{\mathrm{c}}\, \boldsymbol{\xi}^{abc}. \tag{5.2}$$

In the mathematical model, all the states and inputs for the three-phase sFCI are transformed to the stationary frame. The output matrix $\mathbf{C}$ is an identity matrix of $\mathbb{R}^{6\times 6}$, as all the three states of the LCL filter will be controlled simultaneously by the predictive controller. Control of all the three states improves the transient response and provides stable control even with short horizons.

5.2.2 Converter bridge voltage: Space vectors

For a three-level inverter, each phase can have three discrete states, i.e., $\mathcal{S} = \{-1, 0, 1\} \approx \{\mathrm{N}, 0, \mathrm{P}\}$. Based on the switch positions of the three phases[1] $\boldsymbol{s}_{abc}$, the converter generates a set of discrete voltages at the output of the bridge. These can be expressed using space vectors, as defined in section 3.3. Considering the negative port of the dc-link as the reference, the space vector of the converter bridge voltage is defined as

$$\boldsymbol{u}_m^{abc} = \frac{2}{3}(u_a + e^{j2\pi/3}u_b + e^{j4\pi/3}u_c) \tag{5.3}$$

where u_a, u_b and u_c are the phase-to-neutral voltages of the three phases. The phase-to-neutral voltages are defined in terms of the input supply voltage u_{in} and the switch positions $\boldsymbol{s}_{abc} = [s_a \;\; s_b \;\; s_c]^\top$ as

$$\begin{aligned} u_a &= s_a u_{in} \\ u_b &= s_b u_{in} \\ u_c &= s_c u_{in} \end{aligned} \tag{5.4}$$

where $u_{in} = S^+ u_{dc} + (1 - S^+)u_{FC}$, and S^+ is a binary variable which is true for positive half cycle, i.e.,

$$S^+ = \begin{cases} 1 & \text{for} \quad \text{positive half cycle} \\ 0 & \text{for} \quad \text{negative half cycle.} \end{cases} \tag{5.5}$$

S^+ is used to distinguish between the two half-cycles of operation, as input dc-link supplies during the positive cycle and flying capacitor supplies during the negative cycle.

Using Clarke transformation to convert the space vectors to (α, β)-reference frame gives a total of $3^3 = 27$ voltage vectors (see Figure 2.2(b)). Neglecting the ripple on the flying capacitor and assuming $u_{in} \approx u_{dc} \approx u_{FC}$, the voltage vectors generated by the three-phase sFCI can be represented in the (α, β)-reference frame as follows

$$\boldsymbol{u}_m^{\alpha\beta} = \begin{cases} \frac{4}{3} \cdot u_{dc} \cdot e^{\mathrm{j}((n-21)\pi/3)} & \text{for} \quad n = \{21, 22, \ldots, 26\} \quad \text{6 long vectors} \\ \frac{2}{\sqrt{3}} \cdot u_{dc} \cdot e^{\mathrm{j}((n-15)\pi/3+\pi/6)} & \text{for} \quad n = \{15, 16, \ldots, 20\} \quad \text{6 intermediate vectors} \\ \frac{2}{3} \cdot u_{dc} \cdot e^{\mathrm{j}((n-3)\pi/3)} & \text{for} \quad n = \{3, 4, \ldots, 14\} \quad \text{12 short vectors} \\ 0 & \text{for} \quad n = \{0, 1, 2\} \quad \text{zero vectors} \end{cases} \tag{5.6}$$

[1]Note: A switching combination $s_{abc} = \{PN0\}$ denotes that the positive, negative and zero states are active in the phases a, b and c, respectively. For details of operating states see section 3.1.

Out of these 27 voltage vectors, a set of 19 vectors is active and the rest of the vectors are redundant. The active vectors in combination with the zero vectors can be used to generate the required bridge voltage.

5.2.3 Discrete-time model

Generally, a continuous-time state space model can be discretized using the Euler method or Tustin's equivalent. The Forward Euler method is adequately precise when the sampling interval is of the order of tens of microseconds. However, the performance of the controller degrades if the sampling frequency is decreased. Therefore, exact discretization is required to improve the controller performance.

Assumption (A.9): *The filter parameters $L_m, R_m, L_g, R_g, C_f, R$ are considered to be constant between two successive sampling instants.*

Considering the converter bridge output $u_m(t)$ to be piecewise constant during each sampling instant and invoking assumptions (A.4), (A.5) and (A.9), the continuous-time model (5.1), (5.2) can be discretized using zero-order-hold method. The exact discrete-time model is written as

$$\boldsymbol{x}^{\alpha\beta}(k+1) = \mathbf{A}\boldsymbol{x}^{\alpha\beta}(k) + \mathbf{B}\boldsymbol{u}_m^{\alpha\beta}(k) + \mathbf{E}\boldsymbol{u}_g^{\alpha\beta}(k) \tag{5.7a}$$

$$\boldsymbol{y}(k) = \mathbf{C}\boldsymbol{x}^{\alpha\beta}(k) \tag{5.7b}$$

where k is the discrete-time index, T_s is the sampling interval, and the discretized system matrices are

$$\mathbf{A} = e^{\mathbf{F}T_s},\ \ \mathbf{B} = \left(\int_0^{T_s} e^{\mathbf{F}\tau}\cdot e^{\mathrm{j}\omega_g\tau}d\tau\right)\mathbf{G},\ \ \mathbf{E} = \left(\int_0^{T_s} e^{\mathbf{F}\tau}\cdot e^{\mathrm{j}\omega_g\tau}d\tau\right)\mathbf{T}. \tag{5.8}$$

5.2.4 Control objectives

For the sFCI, the control objective is twofold. First, the grid current $\boldsymbol{i}_g$ should accurately track the reference current $\boldsymbol{i}_{g,\mathrm{ref}}$. In addition, the main inductor current $\boldsymbol{i}_m$ and the filter capacitor voltage $\boldsymbol{u}_f$ should be regulated along their reference trajectories $\boldsymbol{i}_{m,\mathrm{ref}}$ and $\boldsymbol{u}_{f,\mathrm{ref}}$, derived from a separate reference calculation block. Moreover, the switching losses are to be kept relatively low, which can be achieved indirectly by controlling the switching frequency. Finally, during transients, the above-mentioned controlled variables should quickly reach their desired values and with as little overshoot as possible.

5.2.5 Controller block diagram

The scheme of the proposed predictive controller with grid current reference tracking is illustrated in Figure 5.3. As can be seen, the desired system performance is achieved by directly manipulating the inverter switches, without the presence of a modulator. The proposed MPC algorithm first computes the evolution of the plant over the prediction horizon (i.e. the trajectories of the variables of concern) based on the measurements of the grid current, main inductor current, filter capacitor voltage, and grid voltage. Following this, the optimal control action (i.e. the switching signals) is chosen by minimizing a performance criterion in real time.

5.2.6 Control problem

The discrete-time model (5.7), (5.8) is used to predict the output $\boldsymbol{y}(t)$ of the system. At time-step k, the cost function that penalizes the error of the output variables and the switching effort over the finite prediction horizon of N_p time steps is written as

$$J(k) = \sum_{l=k}^{k+N_p-1} \|\boldsymbol{y}_{\mathrm{ref}}(l+1) - \boldsymbol{y}(l+1)\|_{\boldsymbol{Q}}^2 + \|\Delta\boldsymbol{s}_{abc}(l)\|_{\boldsymbol{R}}^2\,. \tag{5.9}$$

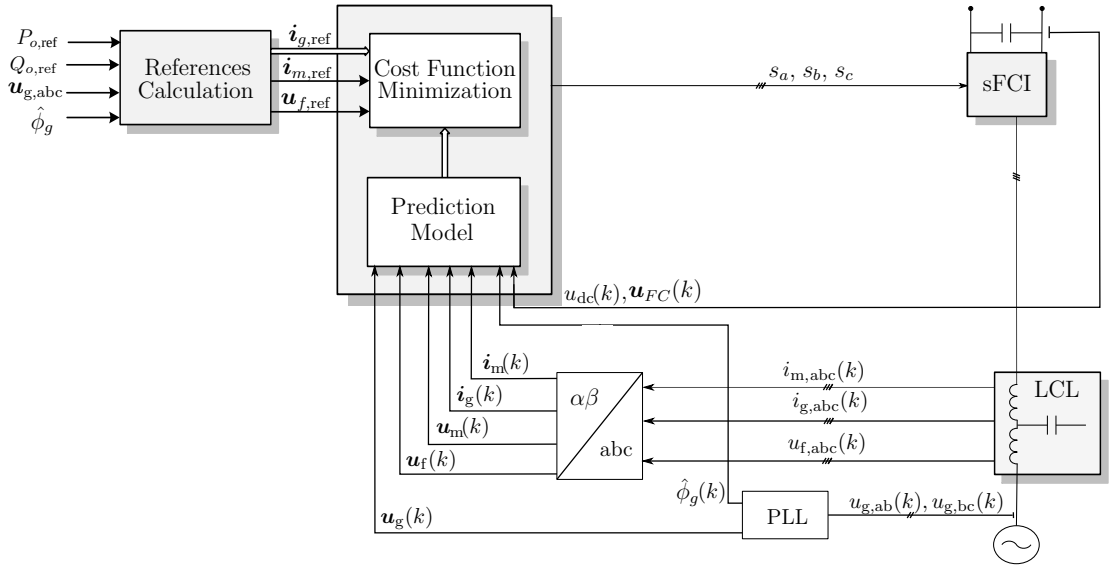


Figure 5.3: Finite-control-set model predictive control with reference tracking for the three-phase sFCI.

In (5.9) $\boldsymbol{y}_{\text{ref}} \in \mathbb{R}^6$ is a vector encompassing the reference values of the controlled variables (main inductor current, filter capacitor voltage and the grid current), i.e.

$$\boldsymbol{y}_{\text{ref}} = [i^{\alpha}_{m,\text{ref}} \;\; i^{\beta}_{m,\text{ref}} \;\; u^{\alpha}_{f,\text{ref}} \;\; u^{\beta}_{f,\text{ref}} \;\; i^{\alpha}_{g,\text{ref}} \;\; i^{\beta}_{g,\text{ref}}]^{\top}. \tag{5.10}$$

Moreover, the term $\Delta \boldsymbol{s}_{abc}(k) = \boldsymbol{s}_{abc}(k) - \boldsymbol{s}_{abc}(k-1)$ is added to control the inverter switching frequency by penalizing the switching transitions. The diagonal matrices $\boldsymbol{Q}$ and $\boldsymbol{R} \in \mathbb{R}^{6\times 6}$ are the weighting matrices[2] that set the trade-off between the overall tracking accuracy and the switching frequency. Note that $\boldsymbol{Q}$ and $\boldsymbol{R}$ are positive semidefinite, and the diagonal entries of $\boldsymbol{Q}$ are chosen in a way that the tracking accuracy among the three controlled variables is prioritized. More specifically, priority is given to the grid current by penalizing the corresponding error more heavily. This is achieved by choosing larger values for the corresponding diagonal entries in $\boldsymbol{Q}$. It implies that when more weight is put into the tracking of the grid current reference $\boldsymbol{i}_{g,\text{ref}}$, the trade-off between the tracking accuracy and the switching frequency is simplified to the trade-off between the grid current THD and the switching frequency of the converter. The switching frequency can be calculated by averaging the total number of *on* transitions, for each phase of the sFCI, over a time interval (MT_s) as

$$f_{sw,\text{avg}} = \lim_{M\to\infty} \frac{1}{MT_s} \cdot \frac{1}{12} \sum_{l=0}^{M-1} \left\| \boldsymbol{s}_{abc}(l) - \boldsymbol{s}_{abc}(l-1) \right\|. \tag{5.11}$$

Here, the *average switching frequency* is obtained by dividing the total number of transitions by 12, i.e., the total number of the controllable switches of the three-phase converter.

The optimal sequence of control actions is then computed by minimizing the cost function (5.9) over the optimization variable, i.e., the switching sequences

$$\mathbf{S}(k) = \left[\boldsymbol{s}^{\top}_{abc}(k),\;\; \boldsymbol{s}^{\top}_{abc}(k+1), \ldots,\;\; \boldsymbol{s}^{\top}_{abc}(k+N_p-1)\right]^{\top}$$

[2]The squared norm weighted with the positive (semi)definite matrix $\boldsymbol{W}$ is given by $\|\boldsymbol{\xi}\|^2_{\boldsymbol{W}} = \boldsymbol{\xi}^{\top}\boldsymbol{W}\boldsymbol{\xi}$

for a prediction horizon N_p. The optimization problem can be summarized as

$$\mathbf{S}_{opt}(k) = \arg \underset{\boldsymbol{S}(k)}{\text{minimize}} \quad J(k) \tag{5.12a}$$

$$\text{subject to} \quad \text{eq. (5.7)} \tag{5.12b}$$

$$\mathbf{S}(k) \in \mathbb{S} \tag{5.12c}$$

where $\mathbb{S} = \mathcal{S}^{3N_p}$. The output of the optimization problem is a set of optimal switching sequences $\mathbf{S}_{opt}(k)$, out of which only the first element $\boldsymbol{s}_{abc,opt}(k)$ is applied to the sFCI, whereas the rest of the elements are discarded. At the next time step $k+1$, the complete procedure is repeated for the updated measurements over a one-step shifted horizon, according to the receding horizon policy [27]. Figure 5.4 presents a typical flowchart of the FCS-MPC approach.

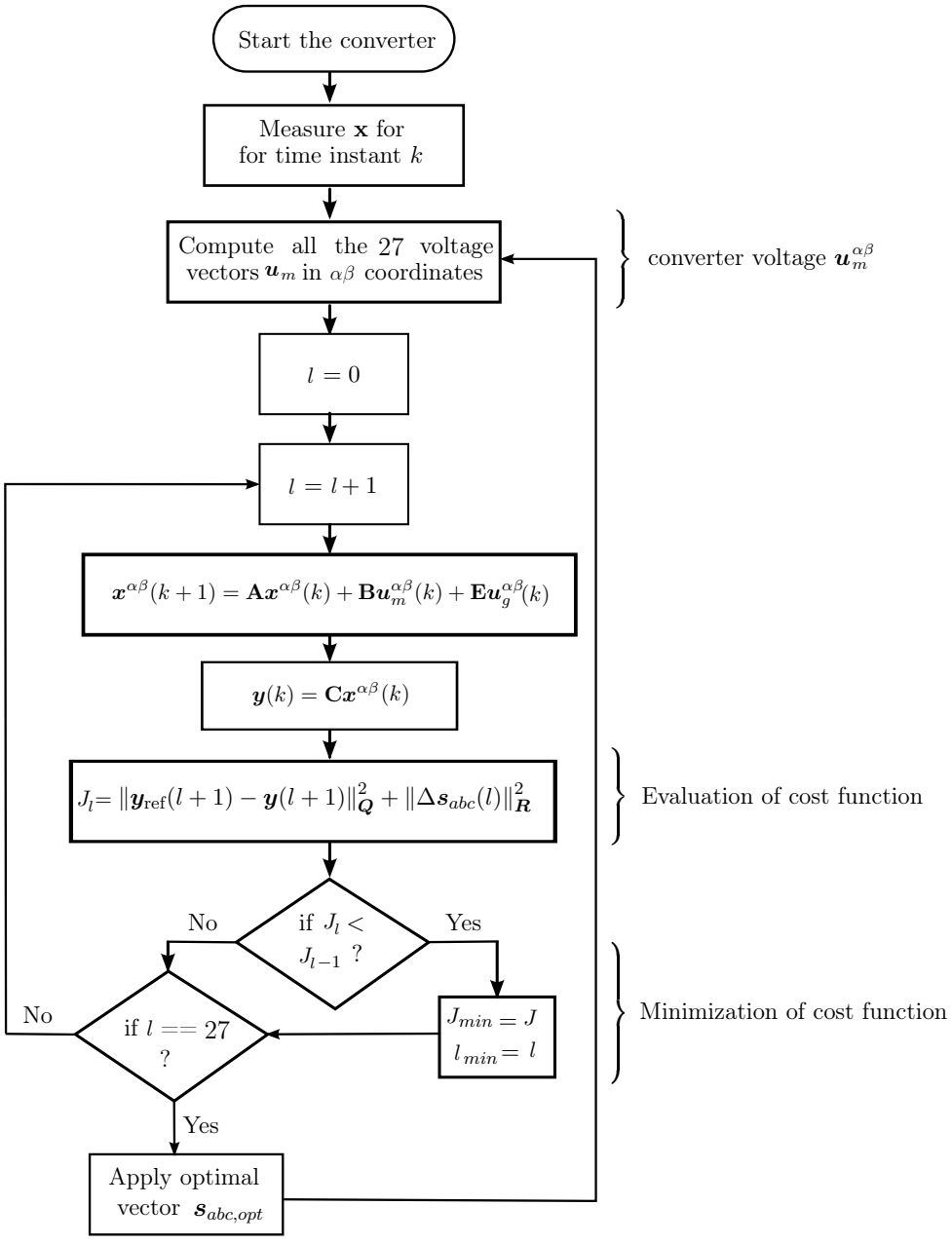


Figure 5.4: Flowchart of the FCS-MPC strategy applied to a three-phase sFCI.

5.2.7 Reference generation

The proposed FCS-MPC controller is based on the idea of reference tracking, which requires the generation of reference signals for all the three controlled variables. In Figure 5.3 a separate block is used for reference calculation, where the input power references $P_{o,\mathrm{ref}}$, $Q_{o,\mathrm{ref}}$ are used to calculate the reference signals for the grid-side current $\boldsymbol{i}^{\alpha\beta}_{g,\mathrm{ref}}$. First the reference currents in the (d,q)-coordinates are calculated as

$$i^{d}_{g,\mathrm{ref}} = \frac{P_{o,\mathrm{ref}}}{1.5\, u^{d}_{g}}, \qquad i^{q}_{g,\mathrm{ref}} = \frac{Q_{o,\mathrm{ref}}}{1.5\, u^{d}_{g}} \tag{5.13}$$

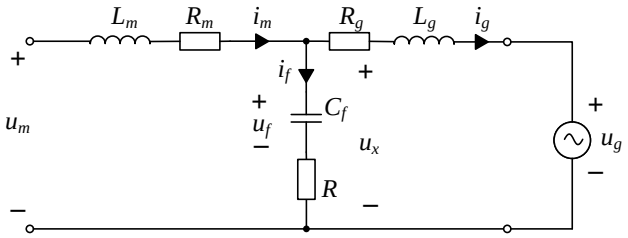


Figure 5.5: Per-phase model of the LCL filter.

where the q-axis components of the grid $u^{q}_{g} \approx 0$. Further the currents $\boldsymbol{i}^{dq}_{g,\mathrm{ref}}$ are transformed to $\boldsymbol{i}^{\alpha\beta}_{g,\mathrm{ref}}$ using Clarke transformation. Figure 5.5 shows a per phase model of the LCL filter which is referred to calculate the reference signals for the other controlled variables using the grid-current reference. From Figure 5.5 we can write

$$\begin{aligned} u_x &= u_g + i_{g,\mathrm{ref}}(R_g + s \cdot L_g) \\ u_{f,\mathrm{ref}} &= \frac{u_x}{1 + s \cdot RC_f} \\ i_{m,\mathrm{ref}} &= i_{g,\mathrm{ref}} + \frac{s \cdot u_x C_f}{1 + s \cdot RC_f} \end{aligned} \tag{5.14}$$

The system of equations (5.14) generates a set of signals, in the three-phase (a,b,c) system, which are transformed to the stationary $(\alpha\beta)$-reference frame. To summarize, the reference vector is

$$\begin{aligned} &\boldsymbol{y}_{\mathrm{ref}} = [(\boldsymbol{i}^{\alpha\beta}_{m,\mathrm{ref}})^{\top} \;\; (\boldsymbol{u}^{\alpha\beta}_{f,\mathrm{ref}})^{\top} \;\; (\boldsymbol{i}^{\alpha\beta}_{g,\mathrm{ref}})^{\top}]^{\top} \\ \text{where} \quad &\boldsymbol{i}^{\alpha\beta}_{g,\mathrm{ref}} = \mathbf{T}_{\mathrm{p}}\, \boldsymbol{i}^{dq}_{g,\mathrm{ref}}, \qquad \boldsymbol{u}^{\alpha\beta}_{f,\mathrm{ref}} = \mathbf{T}_{\mathrm{c}}\, \boldsymbol{u}^{abc}_{f,\mathrm{ref}}, \;\; \text{and} \qquad \boldsymbol{i}^{\alpha\beta}_{m,\mathrm{ref}} = \mathbf{T}_{\mathrm{c}}\, \boldsymbol{i}^{abc}_{m,\mathrm{ref}}. \end{aligned} \tag{5.15}$$

Figure 5.6 shows the generated reference signals for the controlled variables, where the power references are $P_{o,\mathrm{ref}} = 4.9\,\mathrm{kW}$, and $Q_{o,\mathrm{ref}} = 0$.

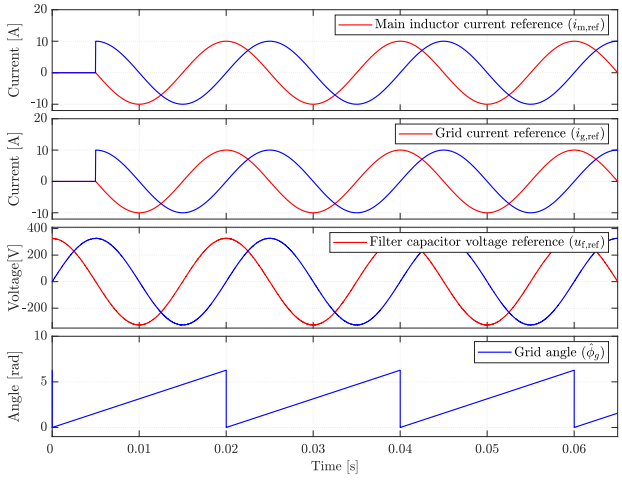


Figure 5.6: Reference signals for the main inductor current $\boldsymbol{i}_{m,\mathrm{ref}}$, grid current $\boldsymbol{i}_{g,\mathrm{ref}}$ and filter capacitor voltage $\boldsymbol{u}_{f,\mathrm{ref}}$ for an active power reference of 4.9 kW, which is enabled at 0.05 s.

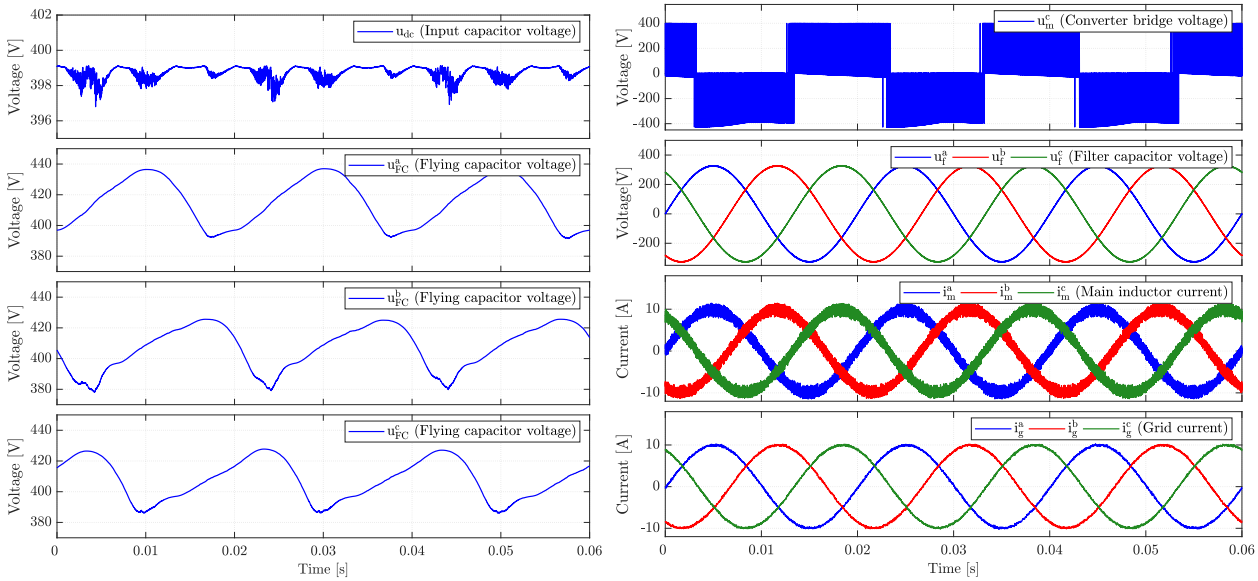
5.3 Performance evaluation of FCS-MPC

The performance of the proposed predictive controller was verified with simulations in Matlab/Simulink. The system under consideration is a three-phase sFCI rated for 5 kW. In addition to the system parameters, given is Table 3.1, Table 5.1 contains the implementation and controller data for the predictive controller. Generally the switching frequency of FCS predictive controller is variable and lesser compared to the conventional control techniques. This is due to the fact that only one output voltage vector is applied during the complete switching cycle. Furthermore, the same voltage vector might be used during subsequent switching periods, if any additional constraints are not specified, therefore the generated switching frequency is variable.

In order to compare the proposed controller with the previously designed SFCC, see section 4.2, the average switching frequency of the predictive controller must be comparable to the fixed switching frequency of the SFCC. Hence, the sampling time and controller step time have been reduced to 3.5 µs, and switching frequency penalization is minimal.

Parameter	**Symbol**	**Value**
Sampling time	T_s	3.5 µs
Controller step time	T_{ctl}	3.5 µs
Nominal grid voltage	u_g	230 V(rms)
Grid Inductance	L_{grid}	0.01 mH
Grid Resistance	R_{grid}	0.1 Ω
Damping Resistor	R_d	1.6733 Ω
Weighting factor matrices	$\boldsymbol{Q}$, $\boldsymbol{R}$	$\boldsymbol{Q} = \text{diag}(20, 20, 5, 5, 150, 150)$ $\boldsymbol{R} = \text{diag}(1, 1, 1, 1, 1, 1) \times 1e^{-4}$

Table 5.1: Implementation and controller data.



(a) Voltage waveforms for the *dc*-link capacitors. **(b)** Converter bridge voltage and states of the LCL filter.

Figure 5.7: Steady-state simulation results for the grid-connected three-phase sFCI with FCS-MPC.

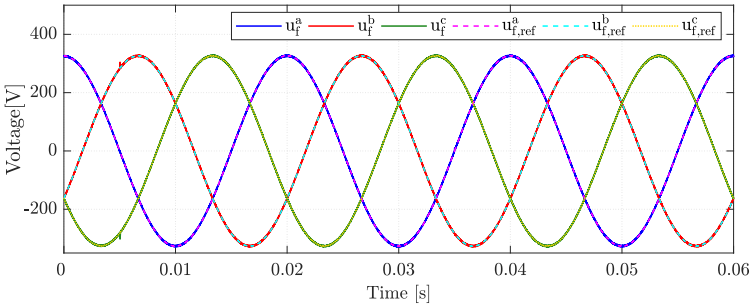
5.3.1 Steady-state performance

For an active-power reference of 4.9 kW and zero reactive power, the grid-current reference (peak) $i_{g,\text{ref}}$ is set to 10 A. The steady-state performance of the three-phase sFCI is shown in Figures 5.7(a) and (b). The flying capacitor voltages are maintained below the allowable limit of 450 V, as seen in the Figure 5.7(a).

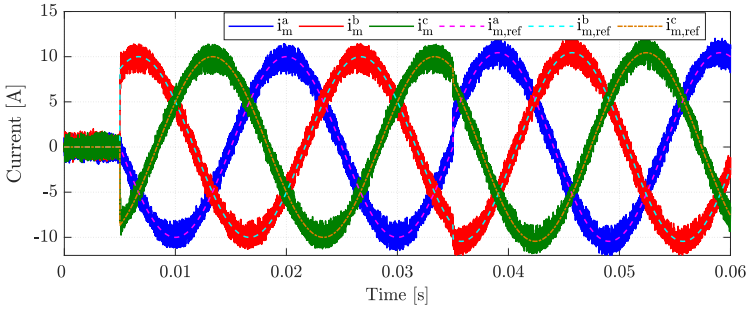
Despite the variation in the input *dc* supply, the grid current remains sinusoidal with a THD of 2% (see Figure 5.7(b)). Unlike the SFCC where the grid current deviates from the sinusoidal behavior due to an uneven bump around zero crossing (see Figure 4.8), the current response of the FCS-MPC is superior and has comparable THD.

5.3.2 Dynamic performance

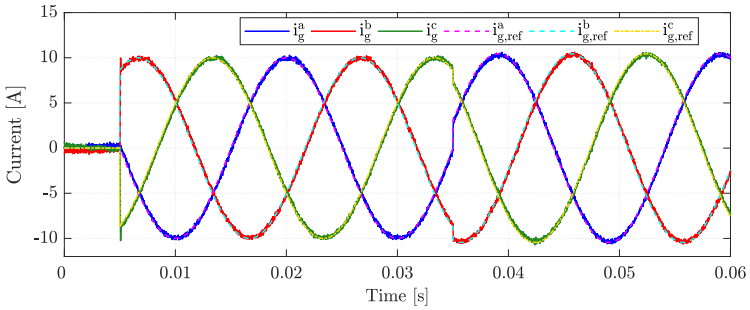
The dynamic response of the proposed MPC strategy is shown in Figures 5.8, 5.9, and 5.10. At 0.005 s the active power demand is stepped to 4.9 kW and at 0.035 s the reactive power demand is set to 1.5 kVAr (see Figure 5.10). Figure 5.8 compares the three controlled variables u_f, i_m, and i_g with their respective references. It is observed that the predictive controller has excellent transient



(a) Filter capacitor voltage and their references (dash-dotted lines).

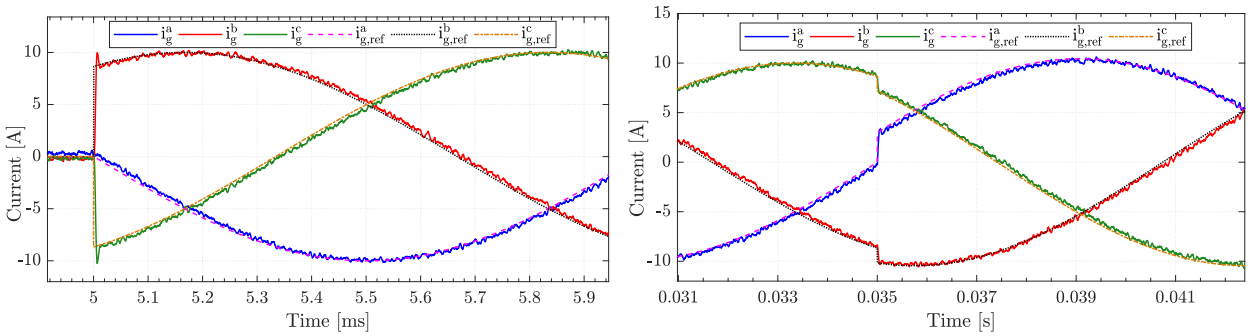


(b) Main inductor currents and their references (dash-dotted lines).



(c) Grid currents and their references (dash-dotted lines).

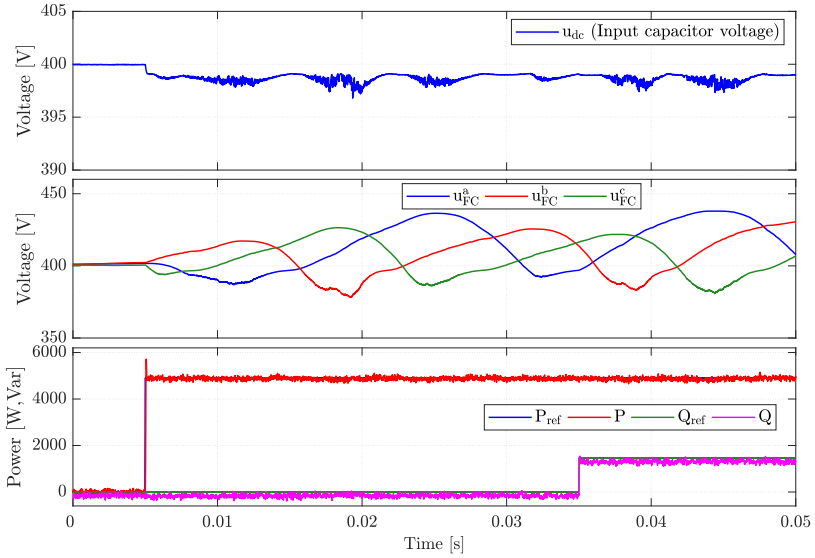
Figure 5.8: Dynamic response of the grid-connected three-phase sFCI with FCS-MPC for a prediction horizon of $N_p = 3$.



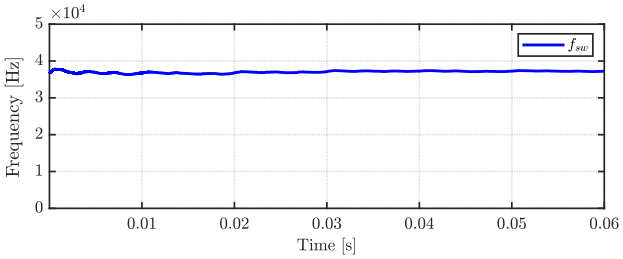
(a) Active power reference is set to 4.9 kW at 5 ms. **(b)** Reactive power reference is set to 1.5 kVar at 0.035 s.

Figure 5.9: Reference tracking of the grid currents.

response, compared to the SFCC, with less overshoot and settling time. In addition, all the variables follow their references implying superior reference tracking. The grid current tracking performance is shown in Figures 5.9(a) and (b). It can be observed that, as soon as the reference value changes the controller is able to follow with minimal overshoot. From Figures 5.9(a) and (b) we can conclude that the sFCI can deliver both active and reactive power, as and when the need arises.



(a) Capacitor voltages and output power response.



(b) Average switching frequency of the converter.

Figure 5.10: Closed-loop simulation results of the sFCI with FCS-MPC.

Figure 5.10(a) highlights the voltage control of flying capacitors during system transients. Additionally, it also depicts the reference tracking of the desired active and reactive power references. With an average switching frequency of 38 kHz (see Figure 5.10(b)) the performance of the proposed MPC is comparable and even better than the state-feedback controller.

5.4 Drawbacks of classical MPC

Finite-control-set model predictive control (FCS-MPC) has received a lot of attention (see e.g., [14, 16, 28, 31, 72]). It exploits the finite number of the switching states of a power converter and combines current control and modulation into one computational step. Simple concept, faster dynamics and flexibility in terms of the control target realization are the advantages. In the past decade, research on FCS-MPC has spread across various fields, e.g., renewable energy systems, multi-level converters, and electrical drives [35].

The concept of the classical FCS-MPC[3], has already been introduced in section 5.2. To ease the problem description, this concept is depicted in Figure 5.11, and denoted as classical MPC.

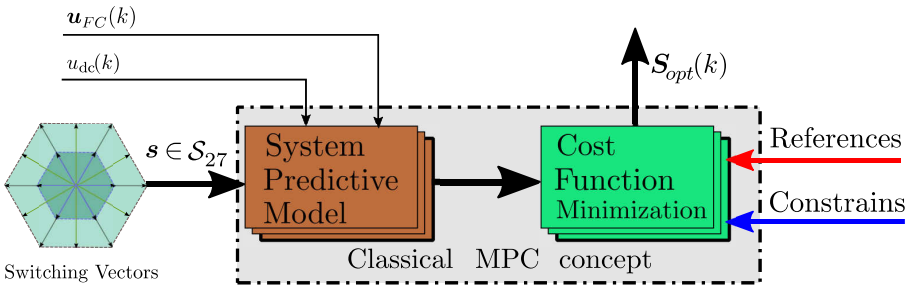


Figure 5.11: Classical MPC illustration [35].

FCS-MPC evaluates a given cost function for each element of an admissible (finite) set $\mathcal{S}$. The switching sequence which minimizes the cost function will be chosen and applied for a whole control interval. Typically, this technique *enumerates* all the admissible switching states to perform the state prediction and cost minimization, i.e., using "exhaustive search" manner to solve the optimization problem. This leads to extremely *heavy computational efforts*, in particular for multilevel power converters [31, 35].

5.4.1 Drawback 1: Heavy computational efforts due to enumeration

One of the major drawbacks of FCS-MPC for multi-level inverters is that: the computation time increases drastically as the number of switching states (e.g. 27 switching states for a 3L-sFCI) increases and therefore implying that real-time implementation may not be feasible [26, 35].

Recent literature, e.g., [31, 55], have already shown that long prediction horizons result in a drastically improved system performance: e.g., lower current THD is obtained. However, the computation time increases exponentially as the number of prediction steps increases, and hence real-time realization is not possible. This emphasizes the necessity to investigate alternate methods for the optimization problem. Therefore, many of the recent research works proposed new methods that reduce the the computational burden and enable real-time implementation. For example, [73, 74] proposed a sphere decoding method to control a 3L-NPC inverter-fed induction machine. It was proven to be effective in particular for multilevel and multiple prediction cases. In [75] three computationally efficient schemes, namely, move blocking, extrapolation, and event-based horizon MPC, have been discussed.

5.4.2 Drawback 2: Variable switching frequency

Another drawback of the FCS-MPC scheme is that it gives a variable switching frequency. Generally, in case of an LCL filter, the average switching frequency of the converter should be at least twice the resonant frequency, in order to avoid the excitation of resonant modes. This requires the system

[3] also known in literature as direct model predictive control (DMPC)

to sample at a very fast rate, e.g., the sampling time of FCS-MPC in the previous section was 3.5 µs, which makes the real-time implementation difficult. Additionally, the inherently variable switching frequency of the FCS-MPC approach gives rise to variable switching losses.

A possible solution to these drawbacks is to use a modulator with a fixed switching frequency, where the input duty-cycle of the modulator is generated from the predictive controller. In the following section, a control scheme known as continuous-control-set model predictive control, is proposed for a three-phase 3L-sFCI.

5.5 Continuous-control-set model predictive control (CCS-MPC)

This section presents a MPC scheme using the concept of unconstrained minimum, see [55, Section 5.2]. Also known as CCS-MPC, this scheme allows the use of long prediction horizon, i.e., $N_p > 3$ and simplifies real-time implementation, because most of the calculation can be done off-line. Moreover, when using long horizon approach for control of grid-connected inverters, use of additional resonance damping methods for the LCL filter is not necessary. First the prediction model is presented and then the control scheme is discussed in detail.

5.5.1 Continuous-time mathematical model

A continuous-time model of the LCL filter/grid, in the (α, β)-frame, has already been presented in section 5.2.1. Instead of treating the grid voltages as disturbance inputs, a simple oscillator can be used to model their sinusoidal nature [76]. Assuming the voltages u_g^α and u_g^β to be sinusoidal signals of fixed frequency $\omega_g = 2\pi f$, an oscillator can be modeled using a two-state linear system as

$$\begin{bmatrix} \dot{x}_{osc_1} \\ \dot{x}_{osc_2} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & \omega_g \\ -\omega_g & 0 \end{bmatrix}}_{\mathbf{T}_{osc}} \begin{bmatrix} x_{osc_1} \\ x_{osc_2} \end{bmatrix} \tag{5.16}$$

Combining the matrices $\mathbf{F}$, $\mathbf{T}$ from (5.1), (5.2) and $\mathbf{T}_{osc}$ from (5.16) gives an augmented system. The state vector becomes $\boldsymbol{x} = [i_m^\alpha \;\; i_m^\beta \;\; u_f^\alpha \;\; u_f^\beta \;\; i_g^\alpha \;\; i_g^\beta \;\; u_g^\alpha \;\; u_g^\beta]^\top \in \mathbb{R}^8$ and the system model can be written as

$$\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{x}^{\alpha\beta}(t) = \mathbf{F}_a \boldsymbol{x}^{\alpha\beta}(t) + \mathbf{G}_a \boldsymbol{u}_m^{\alpha\beta}(t) \tag{5.17a}$$

$$\boldsymbol{y} = \mathbf{C}_a \boldsymbol{x}^{\alpha\beta}(t) \tag{5.17b}$$

where the matrices of the augmented system are

$$\mathbf{F}_a = \begin{bmatrix} -\frac{R+R_m}{L_m} & 0 & -\frac{1}{L_m} & 0 & \frac{R}{L_m} & 0 & 0 & 0 \\ 0 & -\frac{R+R_m}{L_m} & 0 & -\frac{1}{L_m} & 0 & \frac{R}{L_m} & 0 & 0 \\ \frac{1}{C_f} & 0 & 0 & 0 & -\frac{1}{C_f} & 0 & 0 & 0 \\ 0 & \frac{1}{C_f} & 0 & 0 & 0 & -\frac{1}{C_f} & 0 & 0 \\ \frac{R}{L_g} & 0 & \frac{1}{L_g} & 0 & -\frac{R+R_g}{L_g} & 0 & -\frac{1}{L_g} & 0 \\ 0 & \frac{R}{L_g} & 0 & \frac{1}{L_g} & 0 & -\frac{R+R_g}{L_g} & 0 & -\frac{1}{L_g} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \omega_g \\ 0 & 0 & 0 & 0 & 0 & 0 & -\omega_g & 0 \end{bmatrix}, \; \mathbf{G}_a = \begin{bmatrix} \frac{1}{L_f} & 0 \\ 0 & \frac{1}{L_f} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

$$\mathbf{C}_a = \mathbf{I}_{8\times 8}, \;\; \text{and} \;\; \boldsymbol{\xi}^{\alpha\beta} = \mathbf{T}_c \, \boldsymbol{\xi}^{abc}. \tag{5.18}$$

5.5.2 Discrete-time model

Again, invoking assumptions (A.4), (A.5) and (A.9), the continuous-time model (5.17), (5.18) can be discretized using zero-order-hold method. The exact discrete-time model is written as

$$\boldsymbol{x}^{\alpha\beta}(k+1) = \mathbf{A}\boldsymbol{x}^{\alpha\beta}(k) + \mathbf{B}\boldsymbol{u}_m^{\alpha\beta}(k) \tag{5.19a}$$

$$\boldsymbol{y}(k) = \mathbf{C}\boldsymbol{x}^{\alpha\beta}(k) \tag{5.19b}$$

where k is the discrete-time index, T_s is the sampling interval, and the discretized system matrices are

$$\mathbf{A} = e^{\mathbf{F}_a T_s}, \;\; \mathbf{B} = \left(\int_0^{T_s} e^{\mathbf{F}_a \tau} \cdot e^{\mathrm{j}\omega_g \tau} d\tau \right) \mathbf{G}_a, \;\; \mathbf{C} = \mathbf{C}_a. \tag{5.20}$$

5.5.3 Control objectives

The main objective of the CCS-MPC is to regulate the grid current, main inductor current and filter capacitor voltage along their references. Additionally, the flying capacitor voltage must be maintained within the allowable limits. Moreover, the switching frequency of converter is constant because a modulator is used. To achieve the mentioned goals, the control algorithm calculates the optimal duty-cycle using the concept of unconstrained minimum, which is then applied to the PWM block for subsequent generation of gating signals.

5.5.4 Control and optimization problem

The control problem of MPC with reference tracking over a finite prediction horizon of length N_p was presented in (5.9), and is rewritten here as

$$J(k) = \sum_{l=k}^{k+N_p-1} \left\| \boldsymbol{y}_{\mathrm{ref}}(l+1) - \boldsymbol{y}(l+1) \right\|_{\boldsymbol{Q}}^2 + \lambda_s \left\| \Delta \boldsymbol{s}(l) \right\|_2^2 . \tag{5.21}$$

In (5.21) $\boldsymbol{y}_{\mathrm{ref}} \in \mathbb{R}^8$ encompasses the references for LCL filter states and the grid variables. The first term of the cost function implements the objective of reference tracking with $\boldsymbol{Q}$ as the weighting factor matrix. The second term implements the minimization of switching effort, where penalization is carried out using a non-negative weighting factor λ_s.

The dynamic evolution of the discrete-time prediction model (5.19) and (5.20) can be included in the cost function (5.21) using an optimization problem. Therefore, the remainder of this subsection closely follows the derivation of the optimization problem provided previously in [55, Section 5.2].

5.5.4.1 Derivation of optimization problem in vector form

By successively using the state equation (5.19a) (neglecting the superscripts) over the prediction horizon, we can write

$$\begin{aligned}
\boldsymbol{x}(k+1) &= \mathbf{A}\boldsymbol{x}(k) + \mathbf{B}\boldsymbol{u}_m(k) \\
\boldsymbol{x}(k+2) &= \mathbf{A}\boldsymbol{x}(k+1) + \mathbf{B}\boldsymbol{u}_m(k+1) \\
&= \mathbf{A}^2\boldsymbol{x}(k) + \mathbf{A}\mathbf{B}\boldsymbol{u}_m(k) + \mathbf{B}\boldsymbol{u}_m(k+1) \\
&\vdots
\end{aligned}$$

$$\boldsymbol{x}(k+N_p) = \mathbf{A}^{N_p}\boldsymbol{x}(k) + \mathbf{A}^{N_p-1}\mathbf{B}\boldsymbol{u}_m(k) + \cdots + \mathbf{A}^0\mathbf{B}\boldsymbol{u}_m(k+N_p-1) \tag{5.22}$$

The output trajectory vector for a prediction horizon of N_p was previously defined as

$$\mathbf{Y} = [\boldsymbol{y}^\top(k+1) \;\; \boldsymbol{y}^\top(k+2) \;\; \ldots \;\; \boldsymbol{y}^\top(k+N_p)]^\top. \tag{5.23}$$

Substituting (5.23) in (5.19b) yields

$$\mathbf{Y}(k) = \boldsymbol{\Gamma}\boldsymbol{x}(k) + \boldsymbol{\Upsilon}\mathbf{S}(k), \tag{5.24}$$

where the matrices $\boldsymbol{\Gamma}$ and $\boldsymbol{\Upsilon}$ are defined as

$$\boldsymbol{\Gamma} = \begin{bmatrix} \mathbf{CA} \\ \mathbf{CA}^2 \\ \vdots \\ \mathbf{CA}^{N_p} \end{bmatrix} \quad \text{and} \quad \boldsymbol{\Upsilon} = \begin{bmatrix} \mathbf{CB} & \mathbf{0}_{8\times2} & \dots & \mathbf{0}_{8\times2} \\ \mathbf{CAB} & \mathbf{CB} & \dots & \mathbf{0}_{8\times2} \\ \vdots & \vdots & & \vdots \\ \mathbf{CA}^{N_p-1}\mathbf{B} & \mathbf{CA}^{N_p-2}\mathbf{B} & \dots & \mathbf{CB} \end{bmatrix}. \tag{5.25}$$

If we define the output tracking error as $\Delta\boldsymbol{y} = \boldsymbol{y}_{\text{ref}} - \boldsymbol{y}$, the first term in the cost function can be written as

$$J_1 = \sum_{l=k}^{k+N_p-1} \|\Delta\boldsymbol{y}(l+1)\|_{\boldsymbol{Q}}^2 = \sum_{l=k}^{k+N_p-1} \Delta\boldsymbol{y}^\top(l+1)\,\boldsymbol{Q}\,\Delta\boldsymbol{y}(l+1) \tag{5.26a}$$

$$= [\Delta\boldsymbol{y}^\top(k+1) \;\; \dots \;\; \Delta\boldsymbol{y}^\top(k+N_p)]\,\boldsymbol{Q}_e\,[\Delta\boldsymbol{y}^\top(k+1) \;\; \dots \;\; \Delta\boldsymbol{y}^\top(k+N_p)]^\top \tag{5.26b}$$

$$= (\boldsymbol{\Xi}(k))^\top\,\boldsymbol{Q}_e\,(\boldsymbol{\Xi}(k)) = \|\boldsymbol{\Xi}(k)\|_{\boldsymbol{Q}_e}^2, \tag{5.26c}$$

where $\boldsymbol{Q}_e = \text{diag}(\boldsymbol{Q}, \dots, \boldsymbol{Q})$ is a diagonal matrix and $\boldsymbol{\Xi}(k)$ is the output error trajectory. Substituting (5.24) into $\boldsymbol{\Xi}(k) = \mathbf{Y}_{\text{ref}}(k) - \mathbf{Y}(k)$ in (5.26c), we get

$$J_1 = \|\mathbf{Y}_{\text{ref}}(k) - \boldsymbol{\Gamma}\boldsymbol{x}(k) - \boldsymbol{\Upsilon}\mathbf{S}(k)\|_{\boldsymbol{Q}_e}^2. \tag{5.27}$$

In a similar way the second term of the cost function (5.21) can be rewritten as

$$J_2 = \lambda_s \|\mathbf{W}\mathbf{S}(k) - \mathbf{Z}\boldsymbol{s}(k-1)\|_2^2 \tag{5.28}$$

with the matrices

$$\mathbf{W} = \begin{bmatrix} \mathbf{I}_2 & \mathbf{0}_{2\times2} & \dots & \mathbf{0}_{2\times2} \\ -\mathbf{I}_2 & \mathbf{I}_2 & \dots & \mathbf{0}_{2\times2} \\ \mathbf{0}_{2\times2} & -\mathbf{I}_{2\times2} & \dots & \mathbf{0}_{2\times2} \\ \vdots & \vdots & & \vdots \\ \mathbf{0}_{2\times2} & \mathbf{0}_{2\times2} & \dots & \mathbf{I}_2 \end{bmatrix} \quad \text{and} \quad \mathbf{Z} = \begin{bmatrix} \mathbf{I}_{2\times2} \\ \mathbf{0}_{2\times2} \\ \mathbf{0}_{2\times2} \\ \vdots \\ \mathbf{0}_{2\times2} \end{bmatrix}. \tag{5.29}$$

Combining (5.27) and (5.28) yields the cost function in vector form:

$$J = \|\mathbf{Y}_{\text{ref}}(k) - \boldsymbol{\Gamma}\boldsymbol{x}(k) - \boldsymbol{\Upsilon}\mathbf{S}(k)\|_{\boldsymbol{Q}_e}^2 + \lambda_s \|\mathbf{W}\mathbf{S}(k) - \mathbf{Z}\boldsymbol{s}(k-1)\|_2^2. \tag{5.30}$$

The first term in (5.30) penalizes the reference tracking error, while the second term penalizes the switching effort. After some further algebraic manipulations (see [55, Appendix 5.B]) the cost function can be written in a compact form

$$J = (\mathbf{S}(k))^\top\mathbf{H}\mathbf{S}(k) + 2(\boldsymbol{\Theta}(k))^\top\mathbf{S}(k) + \theta(k) \tag{5.31}$$

with

$$\mathbf{H} = \boldsymbol{\Upsilon}^\top\boldsymbol{Q}_e\boldsymbol{\Upsilon} + \lambda_s\mathbf{W}^\top\mathbf{W} \tag{5.32a}$$

$$(\boldsymbol{\Theta}(k))^\top = -(\mathbf{Y}_{\text{ref}}(k) - \boldsymbol{\Gamma}\boldsymbol{x}(k))^\top\boldsymbol{Q}_e\boldsymbol{\Upsilon} - \lambda_s(\mathbf{Z}\boldsymbol{s}(k-1))^\top\mathbf{W} \tag{5.32b}$$

$$\theta(k) = \|\mathbf{Y}_{\text{ref}}(k) - \boldsymbol{\Gamma}\boldsymbol{x}(k)\|_{\boldsymbol{Q}_e}^2 + \lambda_s \|\mathbf{Z}\boldsymbol{s}(k-1)\|_2^2. \tag{5.32c}$$

The cost function (5.31) consists of three terms. The first term is quadratic in the switching sequence $\mathbf{S}(k)$. The Hessian matrix $\mathbf{H}$ is time-invariant if the system parameters are time-invariant. Also, the

Hessian is symmetric and positive definite for $\lambda_s > 0$. The second term is linear in the switching sequence $\mathbf{S}(k)$. Here the time-varying vector $\mathbf{\Theta}(k)$ is a function of the state vector at time step k, the output references $\mathbf{Y}_{\text{ref}}(k)$, and the previously chosen switch position $\boldsymbol{s}(k-1)$. The third term is a time-varying scalar that has the same arguments as $\mathbf{\Theta}(k)$ [55].

By completing the squares, (5.31) can be rewritten as

$$J = (\mathbf{S}(k) + \mathbf{H}^{-1}\mathbf{\Theta}(k))^{\top}\mathbf{H}(\mathbf{S}(k) + \mathbf{H}^{-1}\mathbf{\Theta}(k)) + \text{const}(k). \tag{5.33}$$

The constant term in (5.33) is independent of $\mathbf{S}(k)$ and will not have any effect on the optimal solution. Omitting the constant term, we can reformulate the optimization problem as [55]

$$\mathbf{S}_{opt}(k) = \arg \underset{\boldsymbol{S}(k)}{\text{minimize}} \quad (\mathbf{S}(k) + \mathbf{H}^{-1}\mathbf{\Theta}(k))^{\top}\mathbf{H}(\mathbf{S}(k) + \mathbf{H}^{-1}\mathbf{\Theta}(k)) \tag{5.34a}$$

$$\text{subject to} \quad \mathbf{S}(k) \in [-1,\, 1]. \tag{5.34b}$$

5.5.4.2 Solution in terms of the unconstrained minimum

The optimization problem (5.34) is solved by minimization after neglecting all constraints, if any (hence termed as *unconstrained minimum*), and thus allowing $\mathbf{S}(k) \in [-1,\, 1]$. According to [55], the unconstrained minimum is the optimal solution of the problem (5.34), and can be calculated at every time step k as

$$\mathbf{S}_{unc}(k) = -\mathbf{H}^{-1}\mathbf{\Theta}(k). \tag{5.35}$$

$\mathbf{S}_{unc}(k) \in \mathbb{R}^{N_p \times 2}$ contains a sequence of values that signify the required duty cycle for operating the inverter at the next time step. In order to provide feedback and control the system, only first set of values from the generated solution $\mathbf{S}_{unc}(k)$ is used for further application to the modulator.

The optimal solution used for feedback $\mathbf{S}_{unc,opt}(k) \in \mathbb{R}^{1\times 2}$ contains only two values corresponding to the bridge voltage reference in (α, β)-frame. These values are transformed to the (abc)-reference frame using the inverse Clarke transformation and fed to the PWM block. The desired duty-cycle, which acts as the input to the PWM block, is defined as

$$\boldsymbol{u}_{abc,\text{ref}}(k) = \underbrace{\begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}}_{=:\mathbf{T}_c^{-1}\in\mathbb{R}^{3\times 2}} (\mathbf{S}_{unc,opt}(k))^{\top}\,. \tag{5.36}$$

5.5.5 Controller block diagram

The scheme of the proposed CCS-MPC is illustrated in Figure 5.12. As can be observed, the control block takes in all the measurements and predicts the future outcomes of all the controller variables, i.e., grid current, main inductor current, and the filter capacitor voltage. The reference signals are separately calculated (see section 5.2.4) and fed to the optimization stage where the optimal solution is generated using the optimization problem (5.34). Transforming the optimal solution $\mathbf{S}_{unc,opt}(k)$ to the (abc)-reference frame yields the required duty cycle $\boldsymbol{u}_{abc,\text{ref}}$, which is supplied to the modulator for generation of switching signals $\boldsymbol{s}_{abc}$. Additionally, the feed-forward compensation of dc-link voltages, defined previously in section 4.2.4, is used for scaling of the duty cycle inside the PWM block. The modulator generates the requisite gating signals and ensures desired system performance.

5.5.6 Discussion

From the above derivations we can observe that a MPC scheme based on this approach can be used to implement long horizons with less computational effort. Most of the matrices required for the calculation of the *unconstrained* solution can be calculated off-line. This removes the enormous

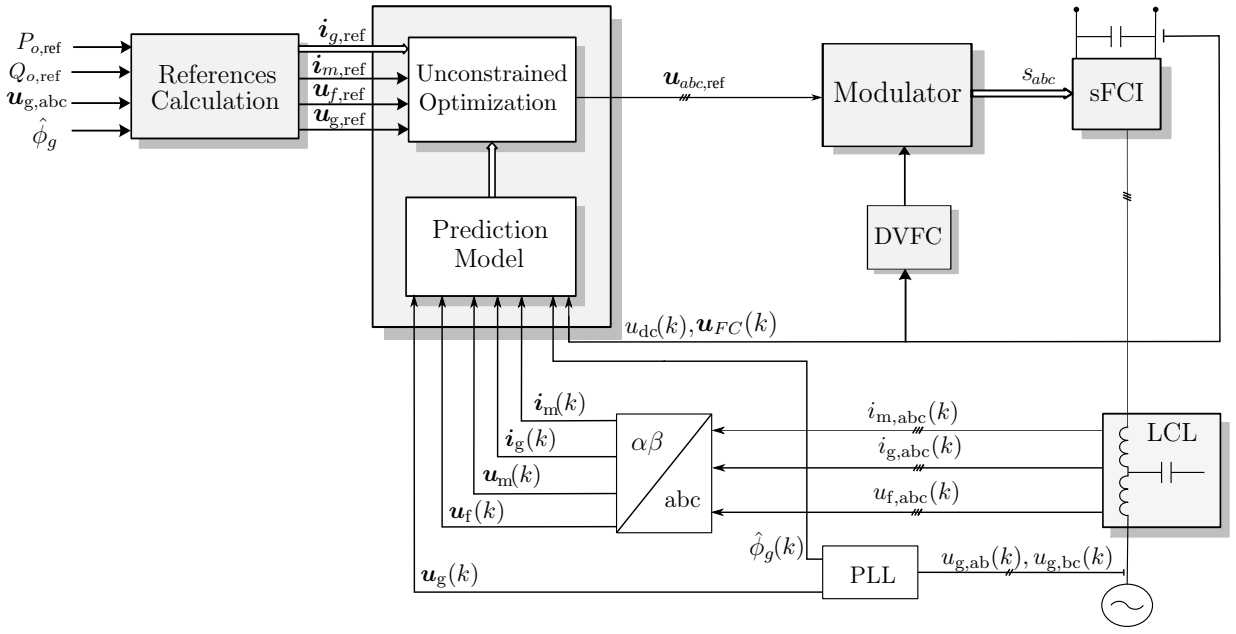


Figure 5.12: Continuous-control-set model predictive control with long prediction horizons for the three-phase sFCI using a modulator.

computational burden on the controller compared to the direct MPC approach. Also, the switching frequency of the system is fixed because of the modulator and hence the sampling frequency does not have to be very high. Both of these advantages make this control scheme feasible for real-time implementation.

5.6 Performance evaluation of CCS-MPC

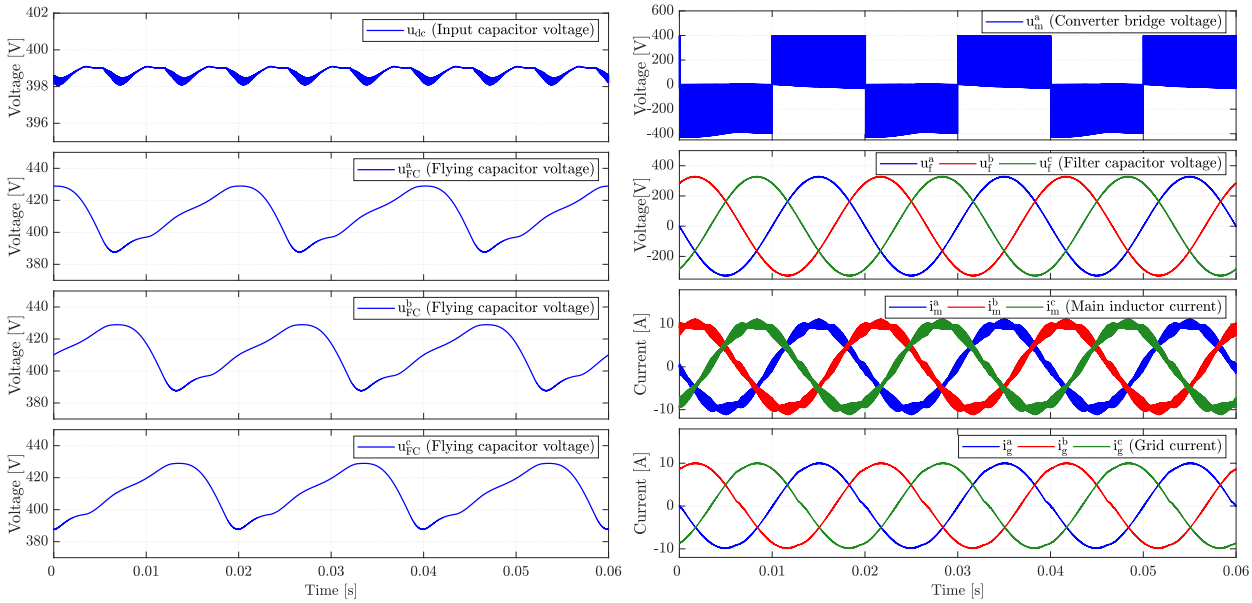
The performance of the proposed CCS-MPC scheme was verified with simulations in Matlab/Simulink and Plecs blockset. The system under consideration is a three-phase sFCI rated for 5 kW. In addition to the system parameters, given is Table 3.1, Table 5.2 contains the implementation and controller data for the CCS-MPC scheme. A level shifted sinusoidal PWM (SPWM) (see Figure 4.7) with a carrier frequency of 40kHz is employed to generate the switching signals.

Parameter	**Symbol**	**Value**
Switching frequency	f_{sw}	40 kHz
Resonant frequency	ω_r	$2\pi \cdot 10.155\,\text{rad}\,\text{s}^{-1}$
Sampling time	T_s	25 µs
Controller step time	T_{ctl}	25 µs
Nominal grid voltage	u_g	230 V(rms)
Grid Inductance	L_{grid}	0.01 mH
Grid Resistance	R_{grid}	0.1 Ω
Weighting factors	$\boldsymbol{Q}$, λ_s	$\boldsymbol{Q} = \text{diag}(10, 10, 1, 1, 90, 90, 1, 1)$
		$\lambda_s = 1e^{-4}$

Table 5.2: Implementation and controller data.

5.6.1 Steady-state performance

For an active-power reference of 4.9 kW and zero reactive power, the grid-current reference (peak) $i_{g,\text{ref}}$ is set to 10 A. The steady-state performance of the three-phase sFCI is shown in Figures 5.13(a) and (b). The voltage of all the flying capacitors is maintained below the allowable limit of 450 V, as seen in the Figure 5.13(a). Additionally, the flying capacitors discharge below the input *dc*-link voltage and hence the sFCI works as desired.



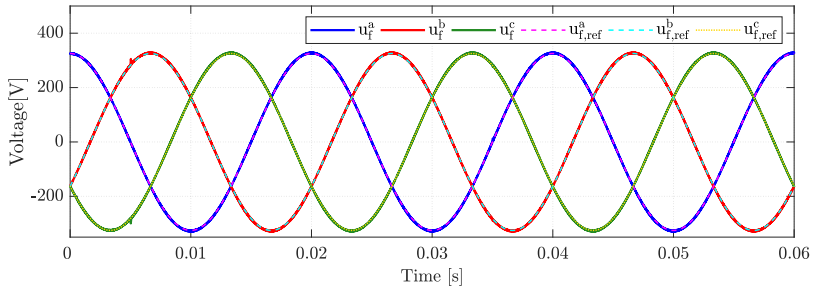
(a) Voltage waveforms for the *dc*-link capacitors. **(b)** Converter bridge voltage and states of the LCL filter.

Figure 5.13: Steady-state performance of the continuous-control-set model predictive control with prediction horizon $N_p = 15$ for a grid-connected three-phase sFCI.

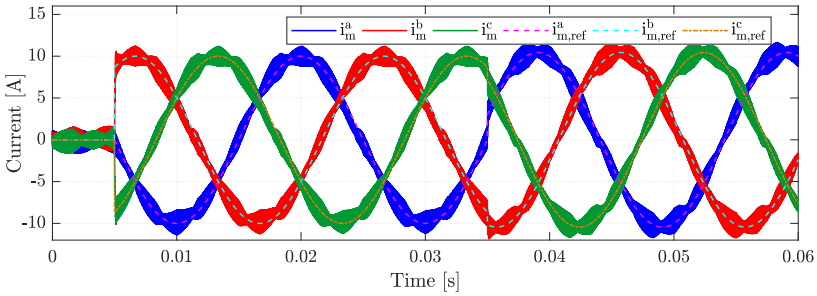
Despite the variation in the input *dc* supply, the grid current remains sinusoidal with an average THD of 2.3% (see Figure 5.13(b)). Unlike the SFCC where the grid current deviates form the sinusoidal behavior due to an uneven bump around zero crossing (see Figure 4.9), the current response of the CCS-MPC is superior and has comparable THD. Also, in comparison to the FCS-MPC scheme where the sampling time was set to 3.5 µs (see Section 5.2), the CCS-MPC scheme has a larger sampling time and thus makes it feasible for hardware implementation. Moreover, external methods for resonance damping are not required as this is taken care by the use of long-horizons.

5.6.2 Dynamic performance

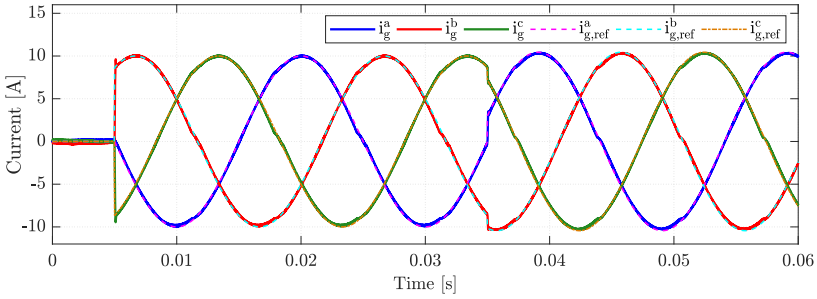
The dynamic performance of the CCS-MPC strategy is shown in Figures 5.14, 5.15, and 5.16. At 0.005 s the active power demand is stepped to 4.9 kW and at 0.035 s the reactive power demand is set to 1.5 kVAr (see Figure 5.16). Figure 5.14 compares the three controlled variables u_f, i_m, and i_g with their respective references. As can be seen, the CCS-MPC has excellent transient response with less overshoot and very less settling time, and the performance is comparable to that of FCS-MPC. In addition, all the variables follow their references implying superior reference tracking. The grid current tracking performance is shown in Figures 5.15(a) and (b). It can be observed that, as soon as the reference value changes the controller is able to follow with minimal overshoot. The capability of the sFCI to deliver both active and reactive power is clearly demonstrated in Figures 5.15(a) and (b).



(a) Filter capacitor voltage and their references (dash-dotted lines).

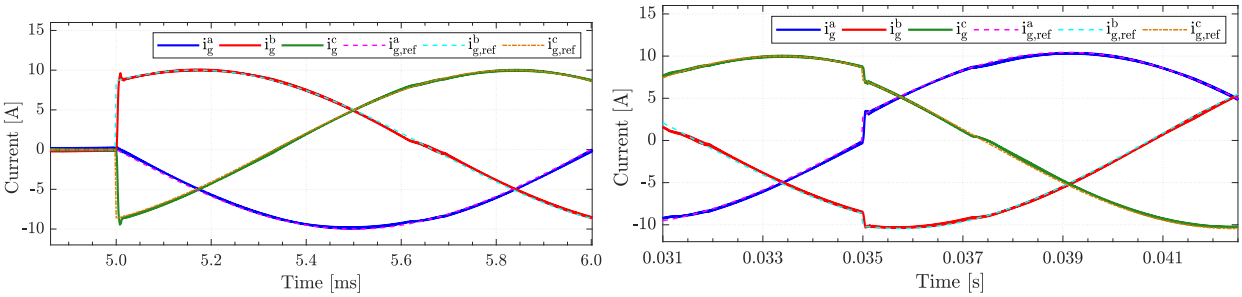


(b) Main inductor currents and their references (dash-dotted lines).



(c) Grid currents and their references (dash-dotted lines).

Figure 5.14: Dynamic response of the grid-connected three-phase sFCI with CCS-MPC for a prediction horizon of $N_p = 15$.



(a) Active power reference is set to 4.9 kW at 5 ms. **(b)** Reactive power reference is set to 1.5 kVar at 0.035 s.

Figure 5.15: Reference tracking of the grid currents.

Figure 5.16(a) highlights the voltage control of flying capacitors during system transients. Additionally, it also depicts the reference tracking of the desired active and reactive power references. Unlike FCS-MPC, both SFCC and CCS-MPC have a fixed switching frequency due to the use of a modulator. From the simulation results we can conclude that the performance of the proposed CCS-MPC is better than the state-feedback controller, although additional resources would be required for real-time implementation.

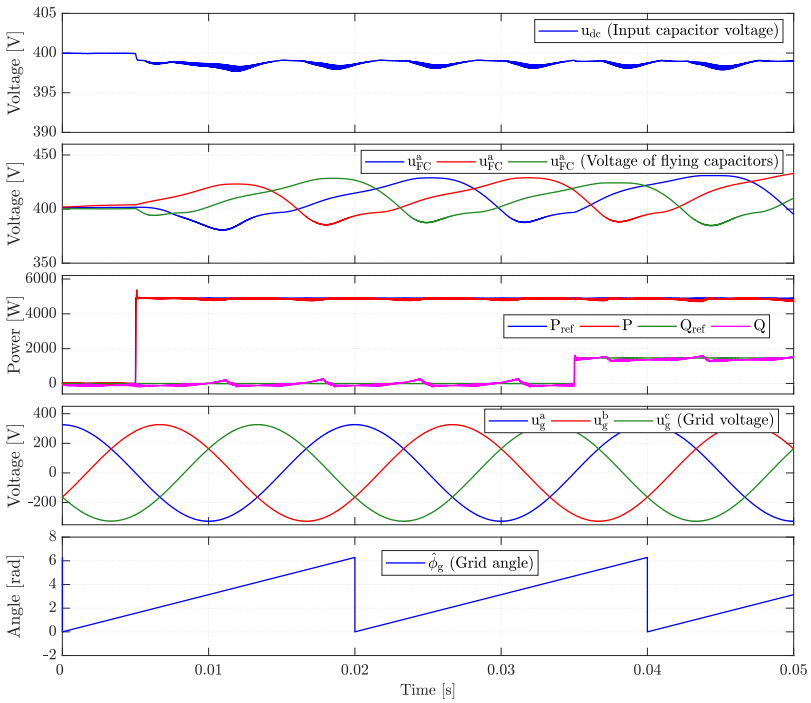


Figure 5.16: Closed-loop simulation results of the sFCI with FCS-MPC, showing capacitor voltages and output power response.

5.7 Summary

This chapter presented two control strategies based on model predictive control for the three-phase sFCI: 1) finite-control-set model predictive control (FCS-MPC) using exhaustive enumeration, and 2) continuous-control-set model predictive control (CCS-MPC) using long horizon approach. To achieve a better dynamic and steady-state performance, all the three states of the LCL filter are controlled using reference tracking.

The first control strategy is based on the conventional MPC where the cost function penalizes the errors between the measured values and the reference values. The simulation results highlight the superior performance of the FCS predictive controller compared to the state-feedback controller. The results also show that the controller is able to achieve resonance damping, for the LCL filter resonance, using a simple passive damping resistor R_d. However, real-time implementation of this method is not practically feasible as the sampling frequency is quite high, and the optimization procedure becomes computationally demanding for longer control horizons.

To overcome the limitations of FCS-MPC, a more sophisticated optimization procedure is derived using the concept of unconstrained minimum. Unlike the conventional scheme, long horizon control can be easily implemented using this method as most of the calculation can be done *off-line*. Moreover, the switching frequency is fixed and therefore the control step time and sampling time of the system can be set to a practically feasible values. Hence, this control scheme is feasible for real-time implementation.

Based on the presented results, it can be concluded that MPC schemes have a better dynamic performance compared to a linear controller (state-feedback control), shorter settling times, and also achieve superior reference tracking. Additionally, model predictive control also gives a better performance at the steady-state operating conditions.

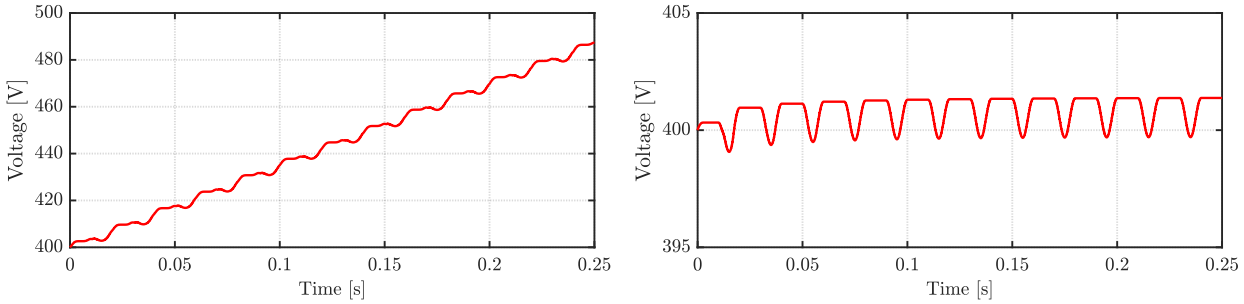
Chapter 6

Model Predictive Control using a Non-linear Converter Model

In the previous chapters the working of the sFCI was analyzed and control strategies based on state-feedback control and model predictive control were proposed. The control strategies were based on a linearized model of the filter/grid system, where the behavior of the flying capacitor and its interaction with the converter bridge was neglected. In order to capture the behavior of the flying capacitor, a non-linear converter model is derived in this chapter. To verify the correctness of the non-linear model, a direct model predictive control strategy is implemented for a single-phase sFCI.

6.1 Motivation

Although, using a flying capacitor in the sFCI allows to decrease the input *dc*-link requirement, additional problems arise due to the behavior of flying capacitor under no-load condition. One of the main drawbacks of the flying capacitor is that its voltage experiences a continuous increase when the load/grid is disconnected, see Figure 6.1(a). For the sFCI to work properly, the flying capacitor voltage has to be maintained below the maximum limit of 450 V. Moreover, the flying capacitor must discharge during the negative cycle to a voltage less than the input *dc*-link. When the load/grid is not present, the discharging path is open through the LCL filter and hence voltage on the flying capacitor does not decrease during the negative cycle. Therefore, a continuous increase in the flying capacitor voltage is observed (termed as voltage fly-away), which is detrimental to the operation of the inverter.



(a) u_{FC} without reverse switch S_5.

(b) u_{FC} with reverse switch S_5.

Figure 6.1: Voltage of the flying capacitor C_{FC} in no-load or grid-disconnected mode. (a) Voltage-flyaway condition for the flying capacitor, (b) voltage control when the reverse switch S_5 is used.

One of the solutions to this problem is to use an additional RB-IGBT (S_5) in an anti-parallel configuration with the switch S_4, see Figure 6.2. The gating signals for the switch S_5 are the same

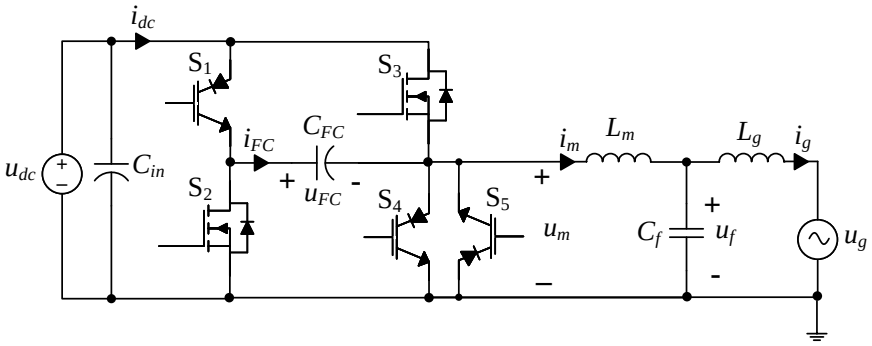


Figure 6.2: Phase leg of the three-level sFCI with an additional switch S_5.

as the switch S_4. In this manner the flying capacitor is allowed to discharge during the zero state of the negative cycle and hence the voltage can be maintained within the limits, see Figure 6.1(b). However, the reverse switch S_5 experiences high current stress and hence heats up very quickly.

Another solution is to model the behavior of the flying capacitor, in order to capture all possible dynamics of the system and design a control strategy where the voltage of the flying capacitor is controlled. In this method, the flying capacitor voltage can be defined as a state, and a direct MPC algorithm can be adopted to handle multiple control objectives, i.e., the regulation of the main inductor current, grid current and the capacitor voltage to their reference values, and control of the flying capacitor voltage under no-load condition.

In the following sections, a detailed analysis of the working states is presented and a non-linear model of the sFCI is derived, to capture the dynamics of the converter bridge, the flying capacitor and the LCL filter.

6.2 Analysis of the six working states of the sFCI

Unlike the three operating states proposed in [3, 13] and described in section 3.1.3, the inverter operation can be classified into six cases. Although the positive and negative states essentially remain the same, the zero state can be further classified into four cases, introduced in section 3.2.4. This classification is based on the cycle of operation and some additional conditions. In the following sections the inverter operation is analyzed in separate cases and mathematical equations that govern the respective case are derived.

6.2.1 Positive cycle

The following three cases exist during the positive cycle of the inverter operation. Switch S_2 remains *off* for the complete positive cycle. Note that the duty cycle from the controller is defined as

$$\mathrm{d(t)} = \begin{cases} 1 & \text{if switching state is P or N,} \\ 0 & \text{if switching state is O.} \end{cases} \tag{6.1}$$

6.2.1.1 Case 1 : Positive state

In this case, the input *dc*-link supplies the load directly, providing both active and reactive power support. Only the switch S_3 is turned *on* (see Figure 6.3). The mathematical equations that govern the operation of this case are

$$\begin{aligned} i_{dc} &= i_m; & i_{FC} &= 0; \\ u_m &= u_{dc}\,\mathrm{d(t)}; & \frac{\mathrm{d}}{\mathrm{d}t} u_{FC} &= 0 \end{aligned} \tag{6.2}$$

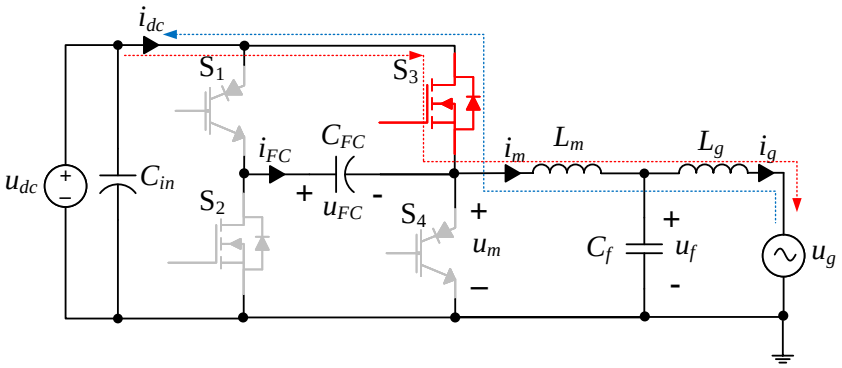


Figure 6.3: Schematic diagram for Case 1, with respective current flow denoted as: ····· active current path, and ····· reactive current path.

6.2.1.2 Case 2 : Zero-state with $i_m > 0$

During the zero state both the switches S_1 and S_4 are turned *on*, although current flow in these switches depends on some additional factors. In this case $i_m > 0$, and the operation of the system can be described by the following mathematical equations

$$\begin{aligned} &i_{dc} = i_m = i_{FC} \neq 0; \\ &u_m = (u_{dc} - u_{FC}) \cdot \mathrm{d(t)}; \\ &\frac{d}{dt} u_{FC} = \frac{1}{C_{FC}} \cdot i_{FC} = \frac{1}{C_{FC}} \cdot i_m = \frac{1}{C_{FC}} \cdot i_{dc} \end{aligned} \tag{6.3}$$

From Figure 6.4 it is observed that whenever $i_m > 0$, charging current i_{FC} of the flying capacitor flows via $S_1 \rightarrow C_{FC} \rightarrow L_m$, while S_4 does not conduct any current. This behavior is due to the reverse biasing of the series diode in switch S_4. Since the flying capacitor voltage is higher than the input *dc*-link, a negative voltage appears across the switch S_4, reverse biasing its series diode.

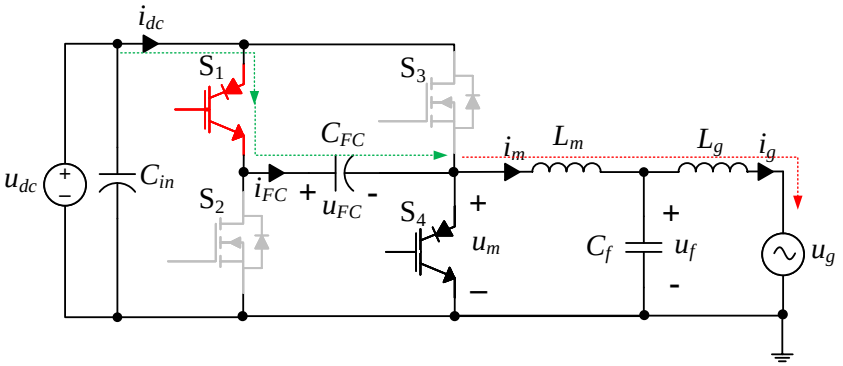


Figure 6.4: Schematic diagram for Case 2, with respective current flow denoted as: ····· active current path, and ····· C_{FC} charging path.

6.2.1.3 Case 3 : Zero-state with $i_m < 0$

This case is observed whenever the current i_m becomes negative, due to its ripple. Again, the switches S_1 and S_4 are both turned *on*. Here the charging current i_{FC} takes the path $S_1 \rightarrow C_{FC} \rightarrow S_4$, see Figure 6.5.

Equations describing the operation are summarized as

$$\begin{aligned} i_{dc} &= i_{FC} = 0; & i_m &< 0 \\ u_m &= 0; & \frac{\mathrm{d}}{\mathrm{d}t} u_{FC} &= 0 \end{aligned} \tag{6.4}$$

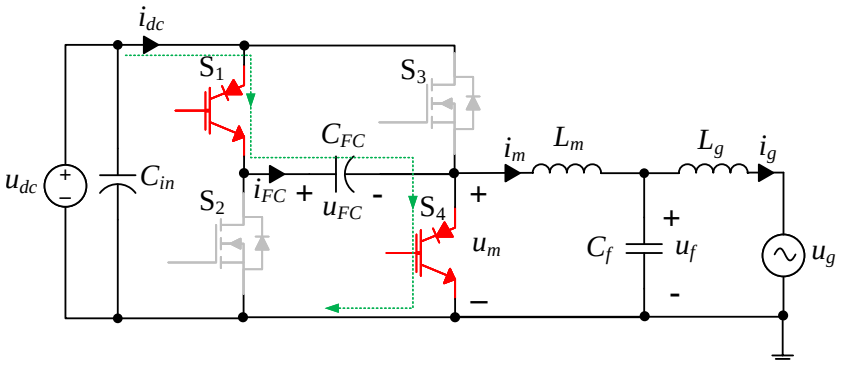


Figure 6.5: Schematic diagram for Case 3, with C_{FC} charging path specified with ····· .

6.2.2 Negative cycle

This cycle can also be separated into three cases. Switch S_3 remains *off* for the complete negative cycle.

6.2.2.1 Case 4 : Negative state

During this state, only the switch S_2 is turned *on*. The flying capacitor, which charges during the zero state, acts as a virtual *dc*-link for the inverter. Figure 6.6 highlights the current flow paths during the negative state. Equations describing the operation can be summarized as

$$\begin{aligned} i_m &= i_{FC} \neq 0, & i_{dc} &= 0; \\ u_m &= -u_{FC}\,\mathrm{d(t)}; \\ \frac{\mathrm{d}}{\mathrm{d}t} u_{FC} &= \frac{1}{C_{FC}} \cdot i_{FC} = \frac{1}{C_{FC}} \cdot i_m \end{aligned} \tag{6.5}$$

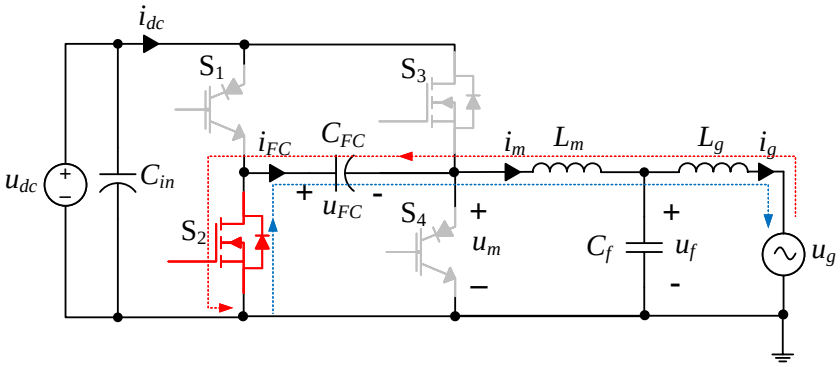


Figure 6.6: Schematic diagram for Case 4, with respective current flow denoted as: ····· active current path, and ····· reactive current path.

6.2.2.2 Case 5 : Zero-state with $u_{dc} < u_{FC}$

During the negative cycle, turning the switch S_2 *off* activates the zero state. When the flying capacitor voltage is higher than the input *dc*-link, the charging current is negligible and therefore no current flows via the switch S_1. However, the negative current i_m flows via S_4 (see Figure 6.7), and the bridge voltage is equal to the voltage drop across the RB-IGBT , i.e., $u_{S_4} = (u_{dc} - u_{FC})$. The mathematical equations governing this case can be summarized as

$$\begin{aligned} & i_{FC} = i_{dc} = 0 \\ & u_m = u_{S_4} = (u_{dc} - u_{FC}) < 0; \text{ will be neglected!} \\ & \frac{\mathrm{d}}{\mathrm{d}t} u_{FC} = 0 \end{aligned} \tag{6.6}$$

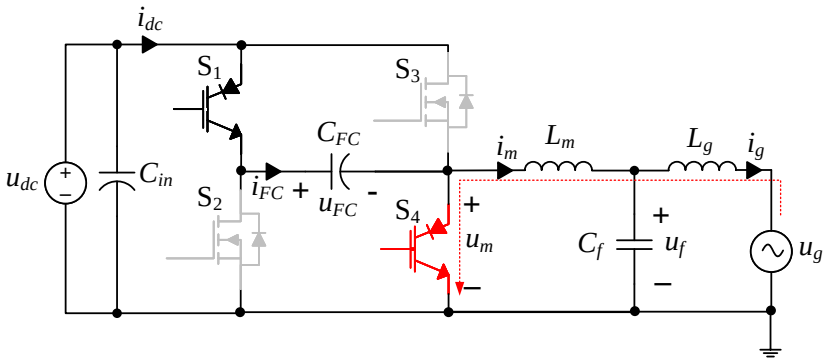


Figure 6.7: Schematic diagram for Case 5, with active current path specified with ····· .

6.2.2.3 Case 6 : Zero-state with $u_{dc} > u_{FC}$

When the flying capacitor voltage drops below the input *dc*-link, the charging current flows via $S_1 \rightarrow C_{FC} \rightarrow S_4$, see Figure 6.8. Additionally, current i_m also flows through S_4, and the bridge voltage is again equal to the voltage drop across the RB-IGBT , i.e., $u_{S_4} = (u_{dc} - u_{FC})$. The governing equations for this case can be summarized as

$$\begin{aligned} & i_{FC} = i_{dc} \neq 0; \\ & u_m = u_{S_4} = (u_{dc} - u_{FC}) > 0; \text{ will be neglected!} \\ & \frac{d}{dt} u_{FC} = \frac{1}{C_{FC}} \cdot i_{FC} = \frac{1}{C_{FC}} \cdot i_{dc} \end{aligned} \tag{6.7}$$

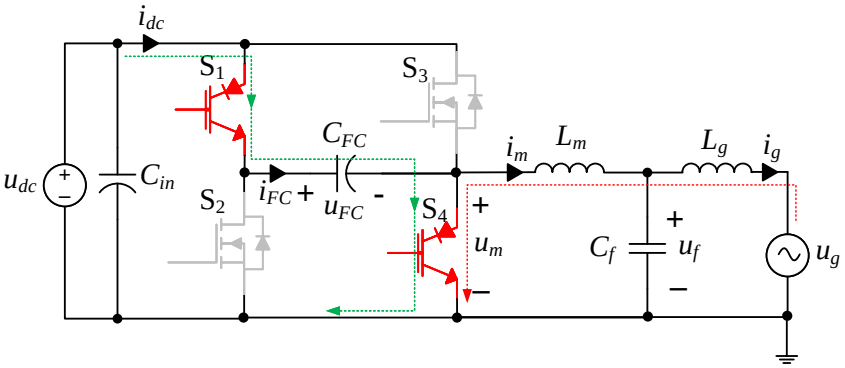


Figure 6.8: Schematic diagram for Case 6, with respective current flow denoted as: ····· active current path, and ····· C_{FC} charging path.

6.3 Non-linear mathematical model

The continuous-time linear system model of the sFCI, described by the system of equations (3.22), can now be extended to include the dynamics of the flying capacitor. Considering the flying capacitor voltage u_{FC} as an additional state, the new state vector becomes $\boldsymbol{x} = [i_m \;\; u_f \;\; i_g \;\; u_{FC}]^\top \in \mathbb{R}^4$. Based on the governing equations presented in the previous section a mathematical model can be written for each case, as follows:

$$\text{Case 1}: \quad \frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \mathbf{F}_1\boldsymbol{x}(t) + \mathbf{G}u_{dc}(t) + \mathbf{T}_1 u_g(t) \tag{6.8a}$$

$$\text{Case 2}: \quad \frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \mathbf{F}_2\boldsymbol{x}(t) + \mathbf{G}u_{dc}(t) + \mathbf{T}_1 u_g(t) \tag{6.8b}$$

$$\text{Case 3}: \quad \frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \mathbf{F}_1\boldsymbol{x}(t) + \mathbf{T}_1 u_g(t) \tag{6.8c}$$

$$\text{Case 4}: \quad \frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \mathbf{F}_2\boldsymbol{x}(t) + \mathbf{T}_1 u_g(t) \tag{6.8d}$$

$$\text{Case 5}: \quad \frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \mathbf{F}_1\boldsymbol{x}(t) + \mathbf{T}_1 u_g(t) \tag{6.8e}$$

$$\text{Case 6}: \quad \frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \mathbf{F}_1\boldsymbol{x}(t) + \mathbf{T}_1 u_g(t) + \mathbf{T}_2 i_{dc}(t) \tag{6.8f}$$

where

$$\mathbf{F}_1 = \begin{bmatrix} -\frac{R+R_m}{L_m} & -\frac{1}{L_m} & \frac{R}{L_m} & 0 \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 \\ \frac{R}{L_g} & \frac{1}{L_g} & -\frac{R+R_g}{L_g} & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}; \quad \mathbf{G} = \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \\ 0 \end{bmatrix}; \quad \mathbf{T}_1 = \begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L_g} \\ 0 \end{bmatrix}$$

$$\mathbf{F}_2 = \begin{bmatrix} -\frac{R+R_m}{L_m} & -\frac{1}{L_m} & \frac{R}{L_m} & -\frac{1}{L_m} \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 \\ \frac{R}{L_g} & \frac{1}{L_g} & -\frac{R+R_g}{L_g} & 0 \\ \frac{1}{C_{FC}} & 0 & 0 & 0 \end{bmatrix}; \quad \mathbf{T}_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{1}{C_{FC}} \end{bmatrix}.$$

The output equation, for all the six cases, remains the same, i.e.,

$$\boldsymbol{y}(t) = \mathbf{C}\boldsymbol{x}(t) \qquad \text{where} \qquad \mathbf{C} = \mathbf{I}_{4\times 4}. \tag{6.9}$$

Note that u_g and i_{dc} are considered as external disturbances, and $\mathbf{I}$ denotes an identity matrix. Figure 6.9 depicts the various regions in reference to the grid voltage and also specifies the operation cases that are valid in respective regions.

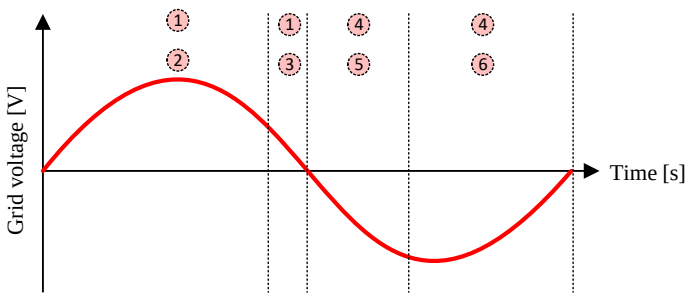


Figure 6.9: Operation cases used in the mathematical model of the sFCI.

6.3.1 Continuous-time model of the system

The various cases of the system model (6.8) can be combined into one model that precisely describes the dynamics of the sFCI when operating in different states. To do so, three auxiliary variables d_{aux_1}, d_{aux_2}, and d_{aux_3} are introduced. These variables together with the cycle of operation, the state variable and operation modes indicate the operating case.

$$d_{aux_1} = \begin{cases} 1 & \text{if} \quad p_1 \cdot s_z = 1 \text{ and } i_m > 0, \text{or } \; p_2 \cdot s_n = 1 \\ 0 & \text{if} \quad p_1 \cdot s_p = 1, \text{or } \; p_1 \cdot s_z = 1 \text{ and } \; i_m < 0, \text{or } \; p_2 \cdot s_z = 1 \end{cases} \tag{6.10}$$

$$d_{aux_2} = \begin{cases} 1 & \text{if} \quad p_1 \cdot s_p = 1, \text{or } \; p_1 \cdot s_z = 1 \text{ and } \; i_m > 0 \\ 0 & \text{if} \quad p_2 = 1, \text{or } \; p_1 \cdot s_z = 1 \text{ and } \; i_m < 0 \end{cases} \tag{6.11}$$

$$d_{aux_3} = \begin{cases} 1 & \text{if} \quad u_{FC} < u_{dc} \text{ and } \; i_m < 0 \\ 0 & \text{if} \quad \text{else} \end{cases} \tag{6.12}$$

Here the binary variables p_1 and p_2 denote the positive and negative half-cycles of operation (w.r.t the grid voltage), respectively. The binary variables s_p, s_n and s_z represent the positive (P), negative (N) and zero (O) states of operation, respectively. Note that $p_1 = (1 - p_2) = S^+$, where S^+ has been defined in (5.5). Taking all the above into account, the complete model of the system is written as:

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \mathbf{F}\boldsymbol{x}(t) + \mathbf{G}u_{dc}(t) + \mathbf{T}_1 u_g(t) + \mathbf{T}_2 i_{dc}(t) \tag{6.13a}$$

$$\boldsymbol{y}(t) = \mathbf{C}\boldsymbol{x}(t) \tag{6.13b}$$

where the system matrices of the complete model are

$$\mathbf{F} = \begin{bmatrix} -\frac{R+R_m}{L_m} & -\frac{1}{L_m} & \frac{R}{L_m} & -\frac{d_{aux_1}}{L_m} \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 \\ \frac{R}{L_g} & \frac{1}{L_g} & -\frac{R+R_g}{L_g} & 0 \\ \frac{d_{aux_1}}{C_{FC}} & 0 & 0 & 0 \end{bmatrix}; \mathbf{G} = \begin{bmatrix} \frac{d_{aux_2}}{L_m} \\ 0 \\ 0 \\ 0 \end{bmatrix}; \mathbf{T}_1 = \begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L_g} \\ 0 \end{bmatrix}; \mathbf{T}_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{d_{aux_3}}{C_{fc}} \end{bmatrix}. \tag{6.14}$$

Figure 6.10 depicts the sFCI represented as an automaton. As can be seen, the transition from one case to another is specified by the auxiliary variables and the state-variables of the inverter.

6.3.2 Discrete-time model of the system

Based on the assumptions (A.4), (A.5) and (A.10), the continuous-time model (6.18), (6.19) is discretized using zero-order-hold method. The discrete-time model is written as

$$\boldsymbol{x}(k+1) = \mathbf{A}\boldsymbol{x}(k) + \mathbf{B}u_{dc}(k) + \mathbf{E}_1 u_g(k) + \mathbf{E}_2 i_{dc}(k) \tag{6.15a}$$

$$\boldsymbol{y}(k) = \mathbf{C}\boldsymbol{x}(k) \tag{6.15b}$$

where k is the discrete-time index, T_s is the sampling interval, and the discretized system matrices are

$$\mathbf{A} = e^{\mathbf{F}T_s}; \;\; \mathbf{B} = \left(\int_0^{T_s} e^{\mathbf{F}\tau} \cdot e^{\mathrm{j}\omega_g \tau} d\tau \right) \mathbf{G}; \;\; \mathbf{E}_v = \left(\int_0^{T_s} e^{\mathbf{F}\tau} \cdot e^{\mathrm{j}\omega_g \tau} d\tau \right) \mathbf{T}_v \;\; \text{where } v \in \{1, 2\}. \tag{6.16}$$

6.4 Direct model predictive control

In section 5.2 a detailed discussion on the design of a controller using the direct MPC approach was presented. The controller was tasked to control the grid current while regulating the main inductor

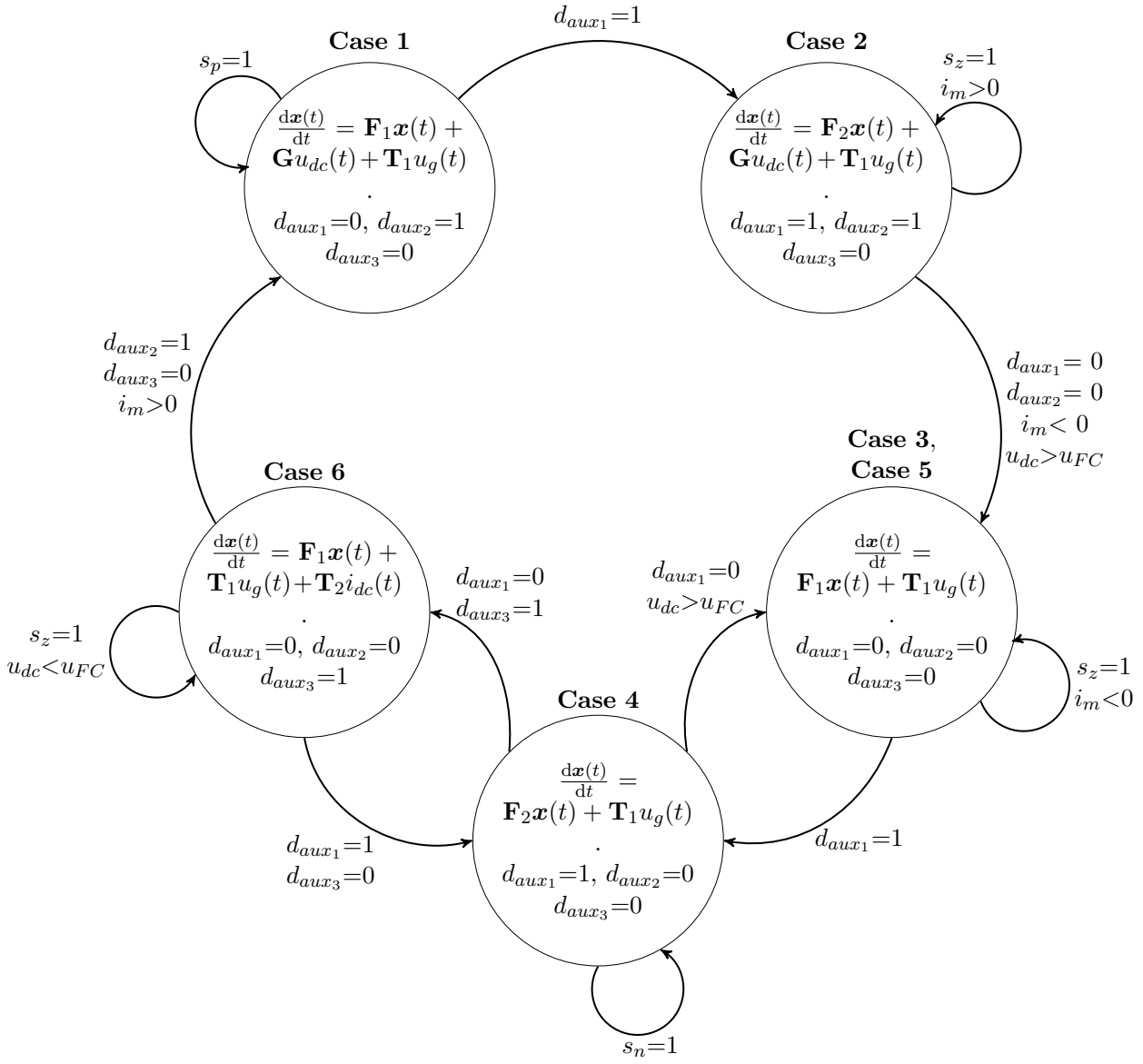


Figure 6.10: sFCI presented as a continuous-time automaton.

current and filter capacitor voltage along their references. A similar approach is adopted to design the predictive controller using the non-linear model-derived in the previous section. However, in addition to controlling the states of the LCL filter, voltage of the flying capacitor must also be controlled, particularly for no-load operation. Therefore, control of the sFCI is split up into two schemes: 1) when the sFCI is under no-load or grid-disconnected condition, and 2) when the sFCI is on-load/grid-connected and/or steady-state operating conditions exist.

In a broader sense, the main objectives of the controller remain the same, i.e., grid current control with regulation of the main inductor current and filter capacitor voltage. To handle the voltage fly-away condition of the flying capacitor, the controller works in the scheme-I. Whenever the system is connected to the grid, control changes to scheme-II where flying capacitor voltage does not require further regulation.

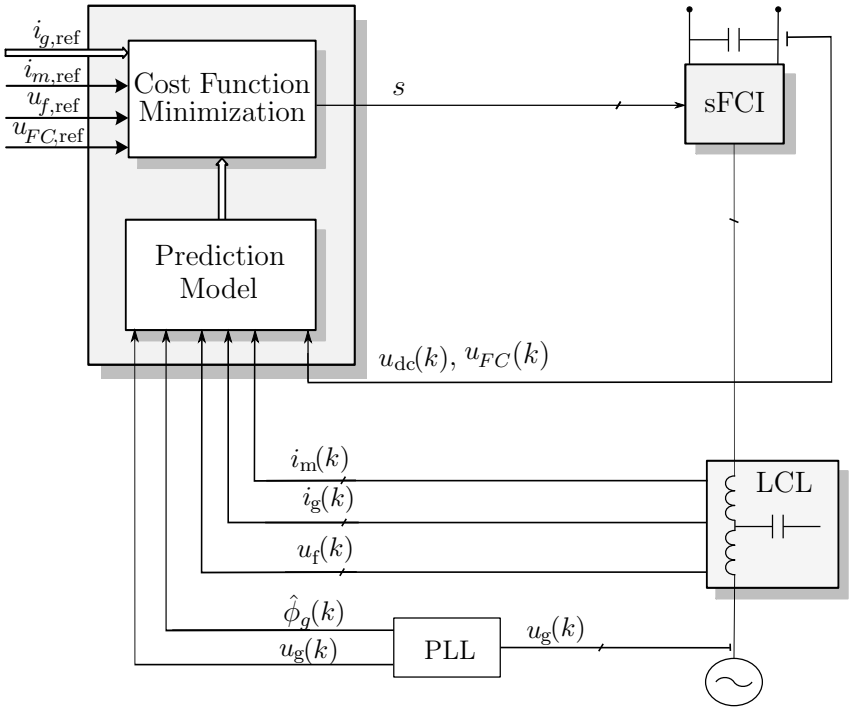


Figure 6.11: Block diagram of the direct MPC for a single-phase sFCI based on the automaton approach.

6.4.1 Control scheme-I

A three-level converter has three switching states, i.e., $\{N,\ 0,\ P\} \approx \{-1,\ 0, 1\}$ (see section 2.1.2). Due to the switching constraints in direct MPC, the transitions between the upper and the lower rails are forbidden, i.e., between -1 and 1. So the converter can either switch between $\{-1,\ 0\}$ or $\{0,\ 1\}$. However, for scheme-I we relax the switching constraints and allow the converter to switch between any of the three switching states, i.e., the constraint

$$\Delta s(k) = |s(k) - s(k-1)| \leq 1 \qquad \text{where} \qquad s \in \mathcal{S} = \{-1, 0, 1\}$$

is not imposed on the controller during scheme-I. This allows the controller to generate a switching pattern wherein the flying capacitor can be discharged even during the positive cycle or the continuous charging operation can be prevented.

6.4.2 Control scheme-II

For scheme-II, the switching constraints are reinstated so that the converter does not switch between the upper and the lower rail, i.e., the transitions between -1 and 1 are forbidden. Additionally, the weighting factor for flying capacitor voltage control is set to zero and thus the system works as a three-level inverter with only three control objectives, i.e., control of i_g, i_m and u_f.

6.4.3 Control problem

The scheme of the proposed controller for the single-phase sFCI is illustrated in Figure 6.11. The desired system performance can be achieved by directly manipulating the inverter switches, without using a modulator. The proposed MPC algorithm first computes the evolution of the plant over

the prediction horizon (i.e. the trajectories of the variables of concern) based on the measurements of the grid current, main inductor current, filter capacitor voltage, flying capacitor voltage, and grid voltage. Following this, the optimal control action (i.e. the switching signals) is chosen by minimizing a performance criterion in real time.

As highlighted previously, constraining the flying capacitor voltage below 450 V is crucial for the working of the sFCI. Control scheme-I is primarily aimed at maintaining the flying capacitor's voltage near a reference value, as it tends to fly-away. This is possible if a discharging path is available or if the flying capacitor is not charged continuously (see the description of zero state in section 3.1.3), during the positive cycle. When the switching constraints are removed, the converter is allowed to switch between -1 and 1. Due to this the flying capacitor does not undergo continuous charging and mitigation of the voltage fly-away condition is possible. However, the converter bridge output for the positive cycle and the negative cycle are different. Figure 6.12(a) shows the converter bridge output when the controller works in scheme-I. As can be seen, the sFCI behaves like a two level inverter for the positive cycle, because of the cost minimization procedure of the direct MPC.

6.4.4 Cost function

The discrete-time model (6.15), (6.16) is used to predict the output $\boldsymbol{y}(t)$ of the system. At time-step k, the cost function that penalizes the error of the output variables over the finite prediction horizon of N_p time steps is written as

$$J(k) = \sum_{l=k}^{k+N_p-1} \|\boldsymbol{y}_{\text{ref}}(l+1) - \boldsymbol{y}(l+1)\|^2_{\boldsymbol{Q}}\,. \tag{6.17}$$

In (6.17) $\boldsymbol{y}_{\text{ref}} \in \mathbb{R}^4$ is a vector encompassing the reference values of the controlled variables (main inductor current, filter capacitor voltage, grid current, and flying capacitor voltage), i.e.

$$\boldsymbol{y}_{\text{ref}} = [i_{m,\text{ref}} \;\; u_{f,\text{ref}} \;\; i_{g,\text{ref}} \;\; u_{FC,\text{ref}}]^\top. \tag{6.18}$$

According to the automaton (see Figure 6.10), the operation case changes based on the auxiliary variables and the measured states of the system. Operation of this type of system where the state-space model of the converter changes continuously depending on binary variables, can be compared to piecewise affine systems.

The diagonal matrix $\boldsymbol{Q} \in \mathbb{R}^{4\times4}$ is a positive semidefinite matrix and its diagonal entries are chosen in a way that the tracking accuracy among the four controlled variables is prioritized. In addition to relaxing the switching constraints during the scheme-I, priority is given to the flying capacitor voltage control by penalizing the corresponding error more heavily. This allows the control of u_{FC} and thus serves as an efficient solution compared to the use of a reverse switch, as highlighted previously in section 6.1.

Control scheme-II has only three control objectives, i.e., control of the three states i_g, i_m and u_f. The diagonal matrix $\boldsymbol{Q}$ is set to highly penalize the grid current error, and offer small penalization to the errors in main inductor current and filter capacitor voltage, while the weighting factor related to flying capacitor voltage is set to zero.

The optimal sequence of control actions is then computed by minimizing the cost function (6.22). Only first element of this optimal sequence is utilized, whereas the rest of the elements are discarded. At the next time step $k+1$, the complete procedure is repeated for the updated measurements over a one-step shifted horizon, according to the receding horizon policy [55].

6.5 Performance evaluation of DMPC

6.5.1 System description

Parameter	Symbol	Value
Nominal power (base power)	P_n	3.3 kVA
Converter side inductance	L_m	680 µH
Converter side resistance	R_m	70 mΩ
Grid side inductance	L_g	80 µH
Grid side resistance	R_g	8.5 mΩ
Filter capacitance	C_f	5 µF
Flying capacitor	C_{FC}	700 µF
Grid inductance	L_{grid}	0.01 mH
Grid resistance	R_{grid}	0.1 Ω
DC link voltage	u_{dc}	400 V
Nominal grid voltage	u_g	230 V(rms)
Sampling time	T_s	3.5 µs
Controller step time	T_{ctl}	3.5 µs
Weighting factor matrices	$\boldsymbol{Q}_1$, $\boldsymbol{Q}_2$	$\boldsymbol{Q}_1 = \text{diag}(10, 40, 1, 10)$ $\boldsymbol{Q}_2 = \text{diag}(20, 90, 1, 0)$

Table 6.1: System parameters and controller implementation data.

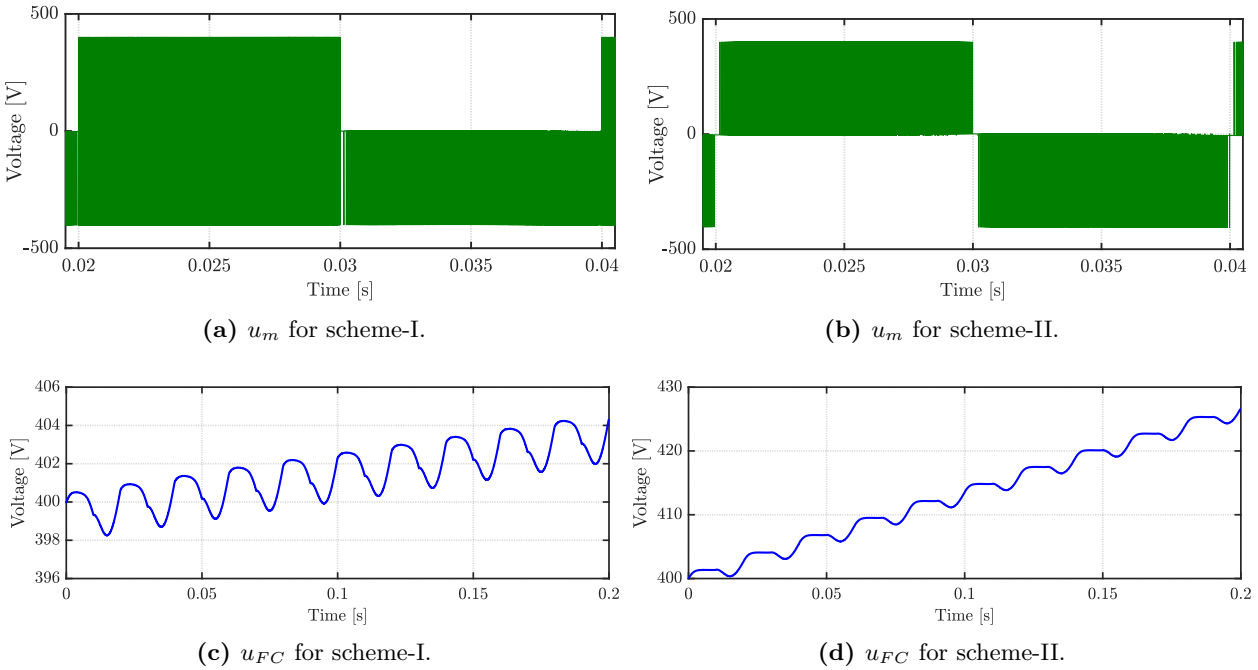
To investigate the performance of the proposed controller using the non-linear converter model, we consider a modified system with the system parameters given in the Table 6.1. The system parameters were modified to decrease the resonant frequency of the LCL filter to 8.29 kHz and make it feasible for implementation of the proposed control approach. In addition to system parameters, the controller implementation data is also provided in the table.

The system under consideration is a single-phase sFCI rated for 3.3 kVA. The working of this control scheme is similar to the direct MPC approach used in Section 5.2. Therefore, the controller step time is set to 3.5 µs as the average switching frequency must be comparable to the state-feedback control. Note that the matrices $\boldsymbol{Q}_1$ and $\boldsymbol{Q}_2$ are the diagonal matrices for penalization of errors and correspond to the schemes I and II, respectively.

6.5.2 Performance of DMPC during control scheme-I

As highlighted earlier, the main aim of the scheme-I is to control the voltage of the flying capacitor during grid disconnected mode or no-load condition. Figure 6.12 compares the output bridge voltage and flying capacitor voltage during the schemes I and II. From Figure 6.12(a) we observe that the bridge voltage output during the positive cycle resembles a two-level inverter. This is due to the fact that the switching constraints have been relaxed and converter is allowed to switch between the upper and lower rails, i.e., -1 and 1.

When the grid is disconnected the controller is tasked to control the voltage of the flying capacitor with the weighting factor matrix $\boldsymbol{Q}_1$. This imposes a large cost on the flying capacitor voltage error and therefore the controller commands the converter to switch between the positive and negative states, in order to prevent continuous charging during the intermediate zero states, and hence the voltage fly-away condition can be mitigated. Figure 6.12(c) shows the voltage increase for 10 cycles of operation when the control scheme-I is used. Compared to the three-level operation (see Figure 6.12(d)) where the capacitor undergoes a voltage increase ≈ 30 V, the operation in scheme-I only sees a voltage rise ≈ 4 V. In this manner the voltage fly-away condition can be mitigated without the use of an extra anti-parallel switch.



(a) u_m for scheme-I. **(b)** u_m for scheme-II.

(c) u_{FC} for scheme-I. **(d)** u_{FC} for scheme-II.

Figure 6.12: (a),(b): Converter bridge voltages, and (c),(d): flying capacitor voltages for the control schemes I and II during grid disconnected mode.

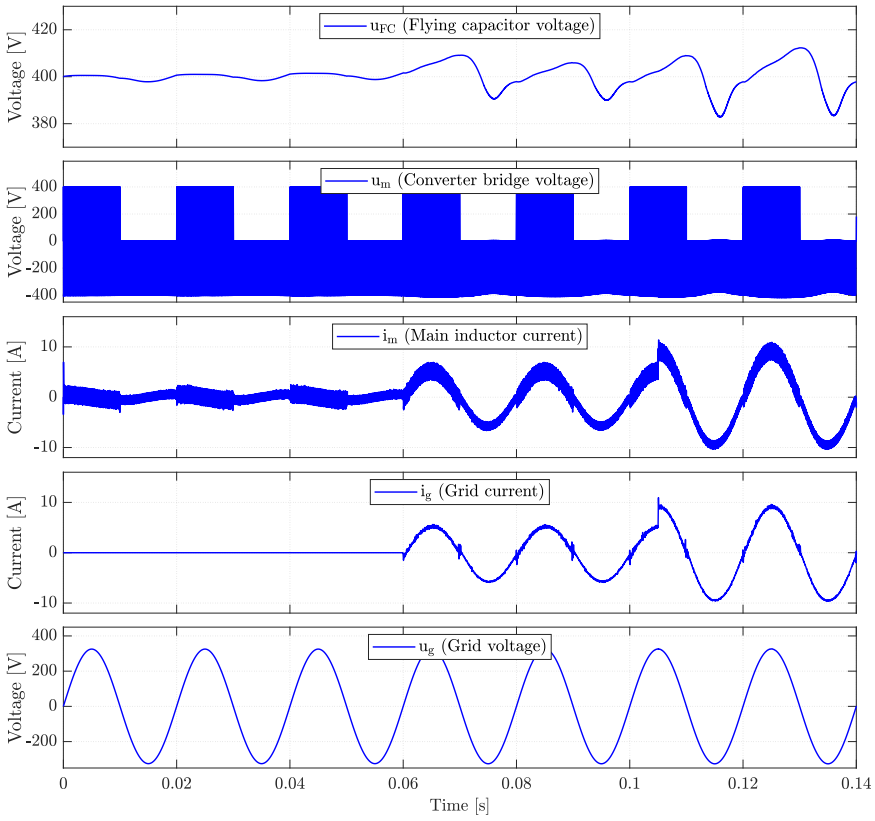


Figure 6.13: Dynamic performance of the control scheme-I after grid connection.

The control scheme-I is not intended for inverter operation during grid-connected mode. Nevertheless, the performance after grid connection is depicted in Figure 6.13. It is observed that the controller

has the following features

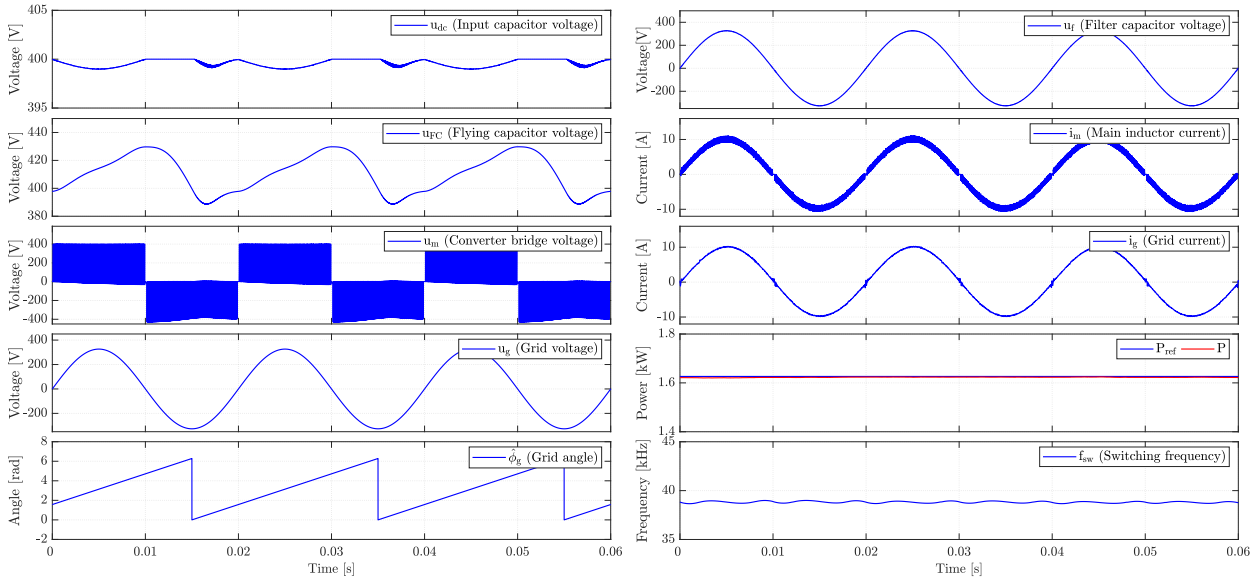
- flying capacitor voltage is maintained around 400 V.
- converter bridge voltage alternates between the two-level and three-level behavior.
- Upon grid connection, the reference tracking of the controller is very fast. Additionally, the dynamic performance is clearly visible when the current reference is stepped from 6 A to 10 A at 0.105 s.

The control scheme-I performs reasonably well even after grid connection. However, THD of the grid current is quite high due to the uneven switching of the converter. Hence, the scheme-II addresses the operation in grid-connected mode.

6.5.3 Performance of DMPC during control scheme-II

Whenever the gird-connected state is detected, controller is switched from the operation scheme-I to scheme-II. In this scheme the switching constraints are reinstated. Therefore the converter is forbidden to switch between the two extreme states and hence the bridge voltage is three level, see Figure 6.12(b). In the following discussion the steady-state and dynamic performances of the proposed DMPC scheme are presented.

6.5.3.1 Steady-state performance



(a) Various voltage waveforms and grid angle.

(b) States of the LCL filter, power tracking and switching frequency.

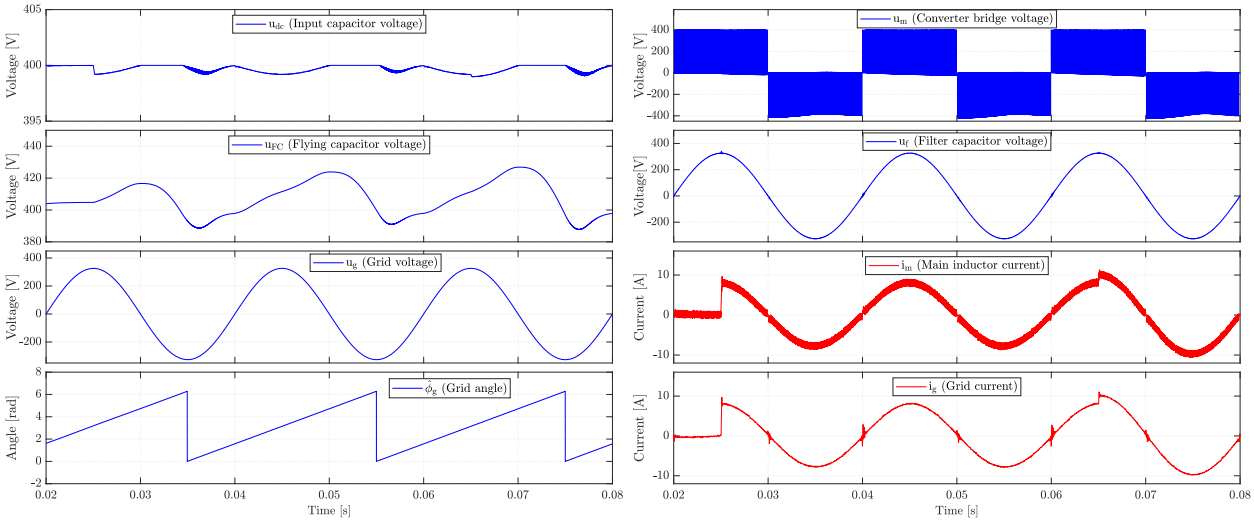
Figure 6.14: Steady-state performance of the DMPC scheme-II (with $N_p = 3$) for grid-connected single-phase sFCI.

The performance of the controller is verified for a reference current of 10 A $\approx$ 1.6 kW (per phase), i.e., half of the nominal power. The steady-state performance results simulated in Matlab/Simulink are given in Figure 6.14. As can be seen, the *dc* side variables are stable, the flying capacitor voltage has a constant ripple and is maintained within the limits. The bridge voltage is uniform and the converter switches evenly between the three levels and therefore follows the grid implying proper grid synchronization. Since the reactive power demand is set to zero, the LCL filter states can be seen to

be in phase to the grid voltage in Figure 6.14(b). The control scheme gives an average switching frequency of 38 kHz.

6.5.3.2 Dynamic performance

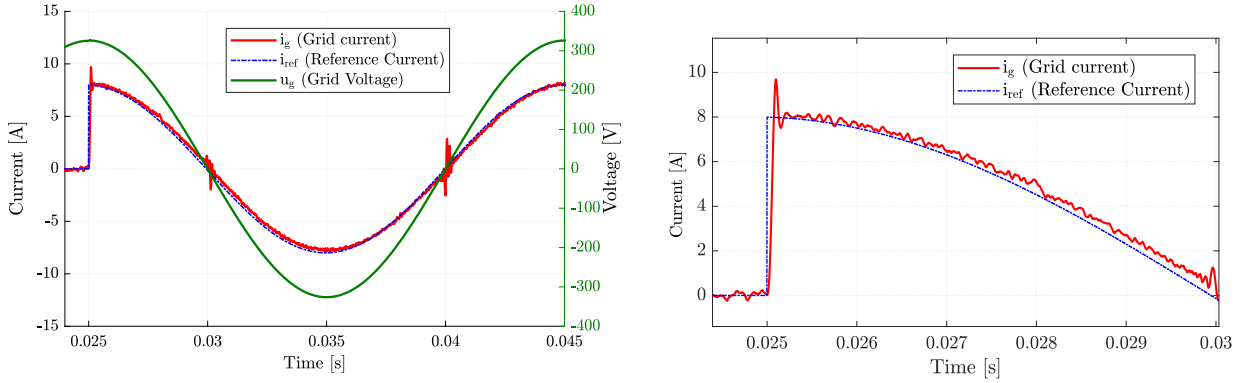
The dynamic performance of the proposed control scheme is shown in Figures 6.15, 6.16 and 6.17. At 0.025 s the active power reference is set to 1.3 kW which is increased to 1.6 kW at 0.065 s. As can be seen, the converter operation is very stable and robust during system transients. In addition to this the transient operation of the grid current and its reference tracking is depicted in Figures 6.16 and 6.17. It is observed that the proposed control approach exhibits very good transient response, small overshoot, less settling time and above all superior reference tracking.



(a) DC-link voltages, grid voltage and PLL output.

(b) Bridge output and states of the LCL filter.

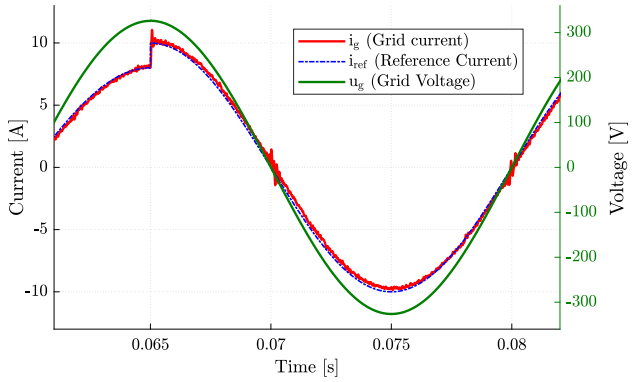
Figure 6.15: Dynamic performance of the DMPC scheme-II (with $N_p = 3$) for single-phase sFCI.



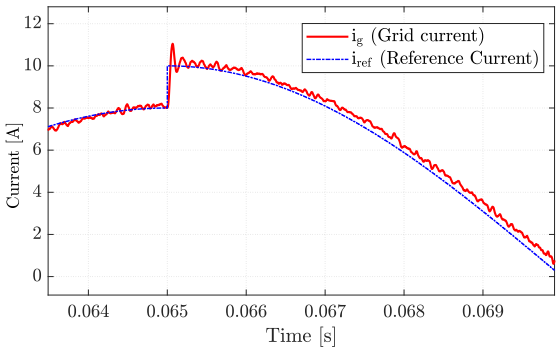
(a) Grid current, its reference and the grid voltage when active power reference is set to 1.3 kW.

(b) Comparison of grid current and its reference.

Figure 6.16: (a) Transient performance of the grid current as its reference is stepped to 6 A. The grid current is in phase with the grid voltage. (b) Grid current reference tracking of the controller with small overshoot and low settling time.



(a) Grid current, its reference and the grid voltage when active power reference changes to 1.6 kW.



(b) Comparison of grid current and its reference.

Figure 6.17: (a) Transient performance of the grid current as its reference changes from 6 A to 8 A . The grid current remains in-phase with the grid voltage. (b) Grid current reference tracking of the controller.

Figures 6.16 and 6.17 show that the output grid current accurately tracks its reference, and produces an average output current THD of 2.5%.

6.6 Summary

In this chapter the main drawback of using the flying capacitor (voltage fly-away condition) has been highlighted and two solutions to mitigate this issue have been presented. The first solution where an extra switch is employed to discharge the capacitor violates the basic construction of the sFCI topology. Hence, an alternative solution whereby the flying capacitor voltage is separately controlled as a state is presented. The proposed control algorithm uses the non-linear converter model and works in two schemes, which have specific control motives. In this manner the grid disconnected and grid-connected modes are taken care of separately.

The performance of the proposed method was investigated in simulations. It has very good performance in both steady-state and transient operating conditions. On one hand the hybrid control technique with its operating scheme-I can control the voltage of the flying capacitor during off-grid conditions, while on the other hand it can work as a reference tracking controller during the scheme-II. It is also shown that the proposed strategy results in grid current THD of 2.5% for a prediction horizon of 3 steps.

Chapter 7

Hardware Implementation of State Feedback Control

In this chapter the implementation of the state-feedback controller on a single-phase hardware testbench is discussed. Experimental results show the working of the converter in grid-connected mode and confirm that the newly proposed sFCI topology can indeed be controlled. Due to time constraints and hardware limitations, only preliminary results obtained at lower power are presented here that prove the working of the designed controller.

7.1 Overview

For hardware implementation, the SFCC designed in section 4.1 was chosen due to limitations on the processing power of the microcontroller and testbench availability. The implementation was carried out using the controller TMS320F28379D from the C-2000 microcontroller family of Texas Instruments (TI). The hardware design of the inverter was carried out previously in [37]. To ease the working of the inverter, two separate PCBs were designed: 1) power PCB which includes the converter bridge and the *dc*-links, and 2) control PCB which includes the various components required for grid connection, measurements circuits and the microcontroller. For details of the design see [37, Ch. 5]. The hardware parameters can be found in Table 3.1, and the testbench is shown in Appendix A.

7.2 Description of the testbench

7.2.1 Hardware setup

Figure 7.1 shows an overview of the setup used for the implementation of the state-feedback current controller. It shows the various components used for enabling grid connection and control of power flow between the inverter and the grid. The control algorithm with associated modules runs on the microcontroller unit (MCU). An additional evaluation board is used to observe the behavior of the MCU and requires a separate software called *Online Oszi* (Fraunhofer internal). Furthermore, for interacting with the controller and setting different values to enable operation a separate in-house software called ISEMON is used which functions via the serial peripheral interface (SPI).

- **DC power supply**: A configurable *dc* power supply from Regatron AG is used to supply variable *dc* input to the sFCI converter.
- **sFCI converter**: A three-phase testbench of the inverter, designed in [37], is available for the controller implementation. However, due to the voltage-flyaway condition of the flying

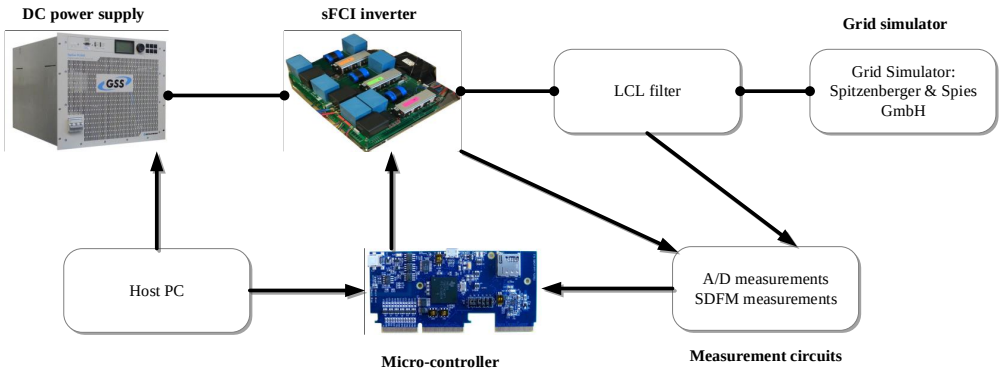


Figure 7.1: Schematic representation of the test setup.

capacitor using the reverse switch during startup is crucial and hence only one of the phases could be used.

- **Control card**: A Delfino F28379D controlCARD (TMDSCNCD28379D) from Texas Instruments (TI) is used for implementation of the contorl algorithm. This 180-pin controlCARD contains the microcontroller, a JTAG emulator and some additional circuitry. The microcontroller is quite versatile as it contains 200 MHz dual C28x CPUs and dual CLAs. This allows independent software development on the CPU_1 and CPU_2 [77].
- **Grid simulator**: To generate customized grid voltages, a 4-quadrant amplifier is used made by Spitzenberger & Spies GmbH & Co. KG. It gives a very clean sinusoidal voltage output.
- **Measurements**: In order to control the system, voltage and current measurements are carried out using analog/digital (A/D) circuits and sigma-delta filter modules (SDFM). These circuits are designed separately onto the control PCB and the measured signals are supplied to the microcontroller.

7.2.2 Data acquisition and synchronization

The different voltage and current sensors used in the sFCI supply analog measurements that have to be processed and supplied to the DSP for subsequent use in the control algorithm. For conversion of analog sensor data to digital form, A/D converters (ADC) are employed. The ADCs used consist of data converters based on SAR (successive approximation) and sigma/delta filter modules (SDFM). Furthermore for grid connection, the filter capacitor voltage must be synchronized in phase and magnitude with the grid voltage. This is achieved using a single-phase PLL.

7.3 Implementation of the controller using C-code

For the implementation of the state-feedback current controller (SFCC) on the microcontroller, various additional modules are required which were previously developed at Fraunhofer ISE. Some blocks are described below:

- **DAQ**: This module takes care of the data acquisition using the ADCs and SDFMs. It contains the code to acquire measurement signals from respective channels and conversion of the data to meaningful values. The contribution to this module was the calibration of the different measurement signals.
- **State machine**: For the proper functioning of the converter and to increase the flexibility of using the microcontroller, a state machine is defined. It consists of different states that

accomplish various objectives. The previously developed state machine at Fraunhofer ISE was modified to suit the working of the controller. More specifically, modules named *dc*-link pre-charge, u_f ramp-up and grid connection were used frequently.

- **Debugging**: It includes modules that allow communication via SPI. This enables the use of *Online Oszi* and ISEMON.

- **ePWM**: The microcontroller has internally provided modules named "enhanced PWM". These are programmed in such a way that the duty cycle generated from the current controller block acts as their reference input.

To enable control of the inverter three modules were developed, i.e., the current controller, phase-locked-loop (PLL), and the observer. To simplify the procedure, code generation feature of Simulink was used to generate the C-code for all of these modules. Later this code was integrated with the modules described above.

7.3.1 Current controller

The state-feedback controller is based on the structure presented in Figure 4.2 and described in sections 4.1 and 4.2. The gain vector is calculated using Matlab scripts, as per the design specifications in section 4.2. Simulink code generation is set up to generate a *non-reusable* function with output argument as the calculated duty cycle. In a *non-reusable* function, the model data structure is statically allocated and can be accessed by model entry point functions directly from the model code.

Note that this module is specified to run from the RAM area of the system memory, as it should be run in parallel to the high speed loop which has a sampling time of 25 µs.

7.3.2 PLL

A single-phase PLL is designed using SOGI based structure presented in [78]. It has a very simple implementation and offers inherent filtering characteristic. This module generates a sine wave that is in-phase with the grid and calculates the magnitude of the grid. Figure 7.2 shows the output of the PLL w.r.t the grid-voltage measurement.

Note that this module is placed into the control law accelerator (**CLA**) (for details see [77]). At each time step the grid voltage measurement is supplied to the *CLAdata*, and the estimated grid magnitude and sine wave are copied into the main memory area.

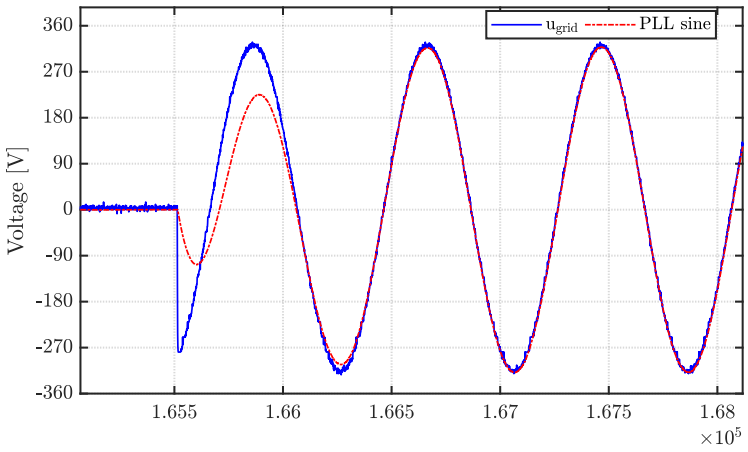


Figure 7.2: Experimental output of the PLL.

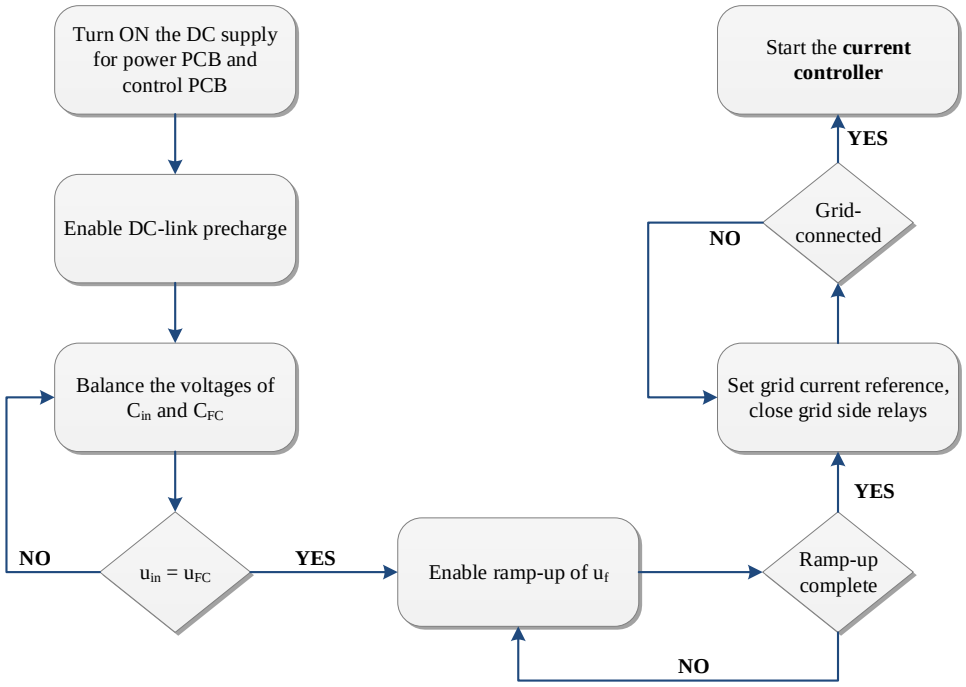


Figure 7.3: Grid connection procedure.

7.4 Grid connection procedure

Before closing the grid-side relays to connect the inverter with the grid, several steps have to be followed. The various steps followed during the connection procedure are depicted in Figure 7.3 and described below.

7.4.1 Pre-charging the *dc*-link capacitors

The *dc*-link of the sFCI is composed of two capacitors, i.e., C_{in} and C_{FC}. The first step is to charge both of these capacitors to the peak of the grid voltage. This is accomplished via the pre-charge circuits and the commands are initiated manually, to avoid any harzards. Once the voltages on both of these capacitors is equal, we can proceed to the next step. Moreover, the PLL is initialized to start the grid tracking.

Note: Switch S_5 is used in this step to prevent the fly-away condition, and its gating signal is equivalent to the gating signal of the switch S_4. However, switching signals of S_4 and S_5 are generated using different ePWM modules to allow separate control.

7.4.2 Filter capacitor voltage ramp-up

In this step the grid voltage measurement is used as the duty cycle for the inverter. However, the value starts from zero and is ramped up in steps. This charges the filter capacitor to the peak of the grid voltage and sets up a sinusoidal voltage on it, which is in-phase with the grid and has the same magnitude. For this step, the switch S_5 is necessary as the inverter is still off-grid. Figure 7.4 shows the ramp-up of u_f in comparison to the grid voltage. Figure 7.5 shows the measurements after ramp-up procedure has been completed. As can be seen, the grid voltage and filter capacitor voltage have the same magnitude and phase.

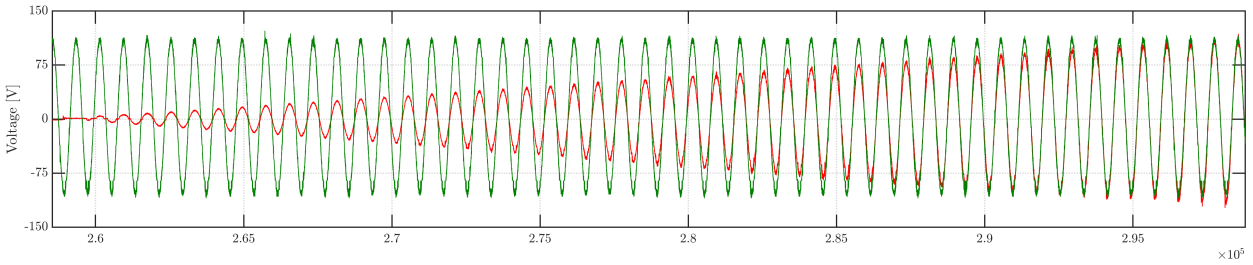
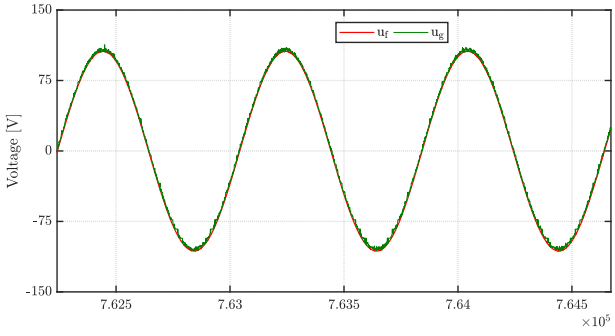
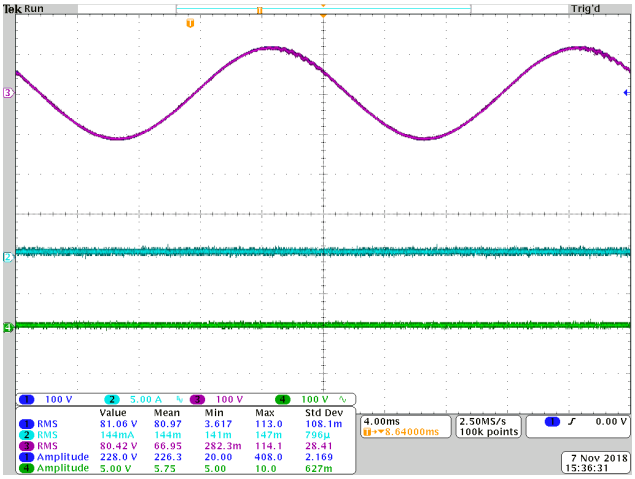


Figure 7.4: Filter capacitor voltage during ramp-up compared to the grid voltage.



(a) u_f and u_g measurements after ramp-up procedure.



(b) Oscilloscope measurements after ramp-up. Grid voltage (dark blue) and filter capacitor voltage (pink).

Figure 7.5: Experimental measurements before grid connection for a grid voltage of 80 V(rms).

7.4.3 Grid connection and current control

This is the last step in this procedure. Once the filter capacitor has a sinusoidal voltage on it the state machine is changed to grid connected mode. In this mode the following steps happen in a sequence

- PWM signals for all the switches are disabled, including S_5.
- Current controller is initialized and the grid side relays are closed.
- After one cycle delay the PWM signals for switches S_1 to S_4 are enabled, while for S_5 the PWM is disabled.
- Based on the current reference the closed-loop controller generates the desired duty-cycle and the inverter starts modulating accordingly.

In this manner the sFCI is connected to the grid and supplies the necessary amount of power as specified by the current reference.

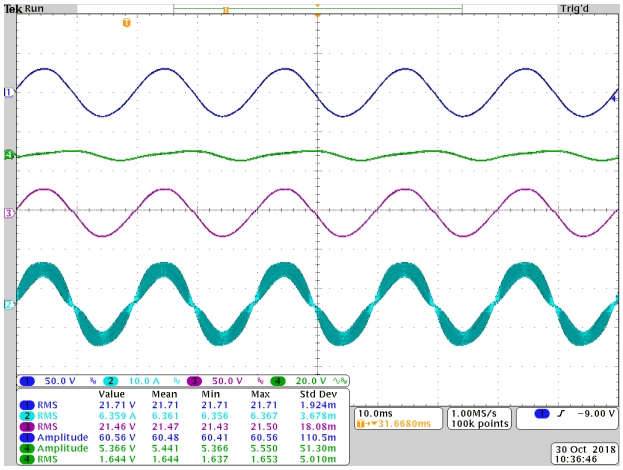
7.5 Experimental measurements

This section presents the experimental measurements for the open-loop and closed-loop operation of the sFCI. Since the converter is relatively new and issues that arise during grid-connection have not been investigated, we start with low values of grid voltage, generated using a grid simulator.

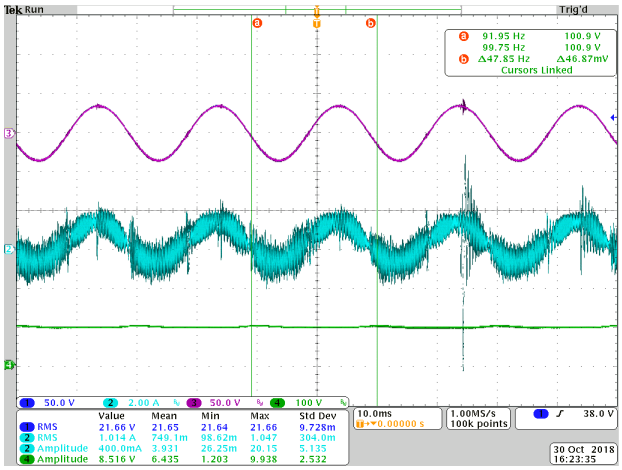
To start with, the operation of the converter was verified in open-loop for an input *dc*-link voltage of 35 V (see Figure 7.6(a)) and subsequently tested for closed-loop grid connected operation with a grid voltage of 20 V(rms), see Figure 7.6(b). After the measurements (in Figure 7.6) confirmed the operation of the single-phase converter and the designed controller, further experiments with more voltage on the grid are presented below. Table 7.1 contains the nomenclature of the oscilloscope measurements, unless specified otherwise.

Measurement signal	**Color**
Load voltage/Grid Voltage	dark blue
Converter bridge voltage	pink
Grid-side inductor current	light blue
Voltage ripple of flying capacitor	green

Table 7.1: Nomenclature of oscilloscope measurements.



(a) Open-loop measurements for a resistor of 34 Ω with input *dc*-link voltage = 42 V.



(b) Closed-loop measurements with a grid voltage of 20 V (rms) and a reference current of 1.5 A.

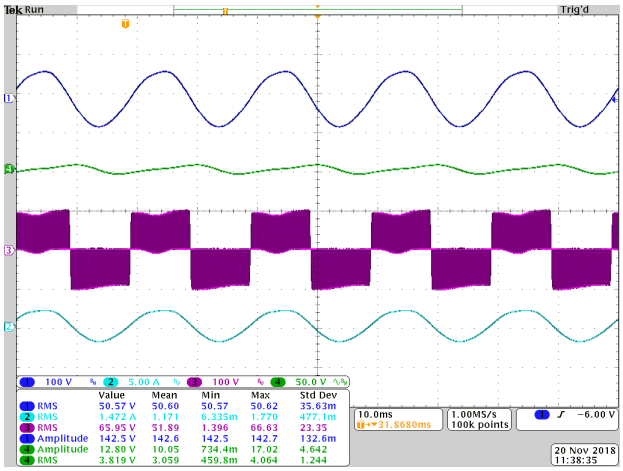
Figure 7.6: Preliminary measurements for control of the single-phase sFCI. Here main-inductor current is depicted in light blue and filter capacitor voltage is depicted in pink.

7.5.1 Converter Response for 50 V grid

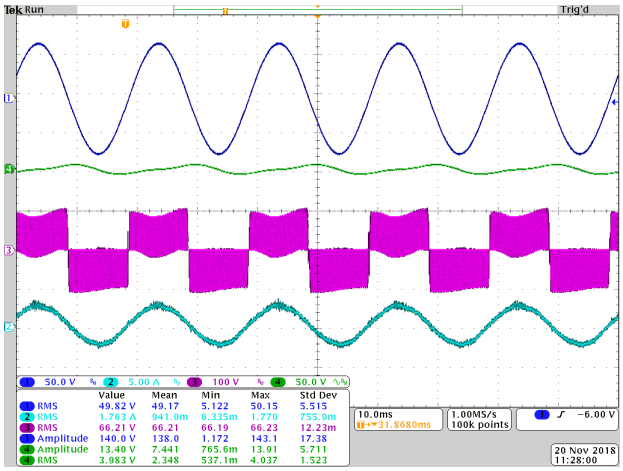
Figure 7.7 shows the open-loop and closed-loop measurements when a grid voltage of 50 V(rms) is selected. Figure 7.7(a) shows the operation of the converter in open-loop with a load resistor of 34 Ω. In this case the input *dc*-link is set to 92 V and the current drawn by the resistor is 1.47 A(rms), while the load voltage is 50.57 V(rms). In order to compare the closed-loop operation of the inverter, the current reference is set to a peak value of 2.4 A while the grid simulator provides a grid voltage of 50 V(rms). Figure 7.7(b) shows the performance of the controller in grid connected mode.

7.5.2 Converter Response for 80 V grid

Figure 7.8 shows the open-loop and closed-loop measurements when a grid voltage of 80 V(rms) is selected. Figure 7.8(a) shows the operation of the converter in open-loop with a load resistor of 34 Ω. In this case the input *dc*-link is set to 140 V and the current drawn by the resistor is 2.3 A(rms), while the load voltage is 79.27 V(rms). The grid simulator provides a grid voltage of 80 V(rms) and



(a) Open-loop measurements for a resistor of 34 Ω with input *dc*-link voltage = 92 V.

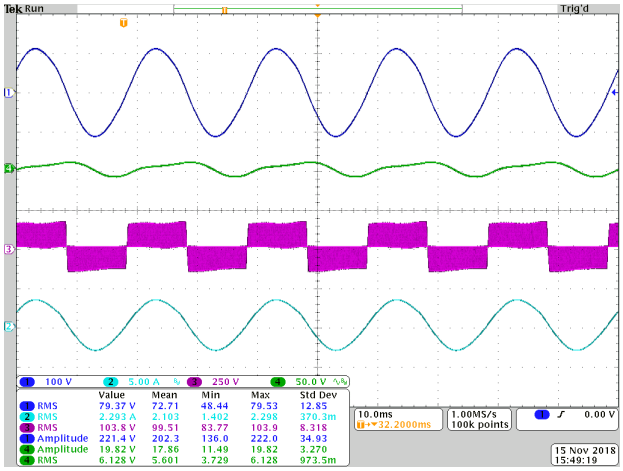


(b) Closed-loop measurements with a grid voltage of 50 V (rms) and a reference current of 2 A.

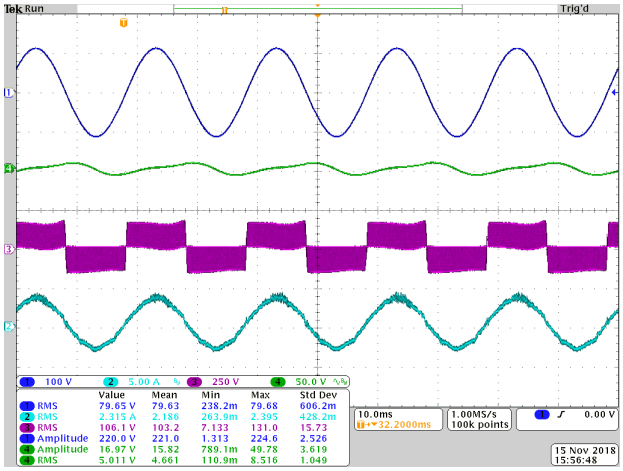
Figure 7.7: Experimental measurements for implementation of the state-feedback control on the single-phase sFCI with 50 V grid.

the current reference is set to a peak value of 3.3 A. Figure 7.8(b) shows the performance of the controller in grid connected mode.

From Figure 7.8(a) it can be observed that the load voltage and current is not purely sinusoidal, as highlighted previously in section 3.2.2. From Figure 7.8(b) it can be seen that the grid current is in-phase with the grid voltage. Additionally, it is observed that the deviation from sinusoidal behavior is present at the transition from positive and negative cycle.



(a) Open-loop measurements for a resistor of 34 Ω with input *dc*-link voltage = 140 V.



(b) Closed-loop measurements with a grid voltage of 80 V (rms) and a reference current of 3.3 A.

Figure 7.8: Experimental measurements for implementation of the state-feedback control on the single-phase sFCI with 80 V grid.

7.6 Discussion and summary

This chapter presented the experimental measurements for the operation of sFCI with the state-feedback controller. It can be concluded that the Siwakoti-H inverter can be controlled in grid-connected mode using SFCC.

Figure 7.9: Thermal image of the sFCI converter with temperature probing spot on switch S_4.

The measured current response contains a lot of distortions due to various contributing factors. Firstly, the topology contains two different switches, i.e., MOSFETs and RB-IGBTs which have a lot of difference in switching behavior, hence more investigation is required in this direction. In addition to this, the hardware test-bench, built at Fraunhofer ISE, was not designed to incorporate RB-IGBTs, instead it used series diodes and MOSFETs. Therefore, the gate driver circuits used previously are not completely compatible and require further improvement. Moreover, a dead-time of 300 ns is used in the PWM block, while the controller does not contain any dead-time compensation.

Experimental measurements could not be carried out at higher voltages as the case temperature of RB-IGBTs (particularly S_4) approached the maximum allowed limit of 110 °C, for a *dc*-link voltage of 190 V (see for example Figure 7.9) and were mostly destroyed due to thermal runaway. Further investigation into this behavior could not be carried out due to time constraints. To sum up, the presented results prove the working of the state-feedback controller for the grid-connected sFCI. The response of the controller can be further improved by enhancing the data acquisition module, tuning the controller parameters and introducing dead-time compensation.

Chapter 8

Conclusion and Future Outlook

In this work, a recently proposed transformerless inverter, i.e., the Siwakoti-H flying capacitor inverter has been investigated. The operating principle, working modes, and performance in open-loop/closed-loop has been discussed. The Siwakoti-H inverter utilized in this thesis has the potential of becoming an attractive alternative to conventional topologies as it can be realized using lesser and smaller components. However, it presents an interesting problem for system modeling and control design due to its additional non-linearities. Therefore, both conventional and modern control techniques for the grid-connected sFCI have been investigated. Emphasized efforts have been put into the predictive control due to its attractive properties (e.g., simple concept and fast control dynamics, etc.) and promising potential. All the presented control algorithms have been validated in simulation. Finally, the state-feedback approach has been verified experimentally for a single-phase sFCI using a microcontroller.

8.1 Conclusion

The work carried out in this thesis can be briefly summarized in the following points.

- In Chapter 2, a literature review was conducted with regards to the conventional three-level inverter topologies and the popular control strategies used in grid-connected inverter applications. The basics of three-level inverters in terms of the switching vectors, was also discussed. Additionally, the sFCI was introduced as an attractive alternative to the conventional topologies. Furthermore, the theoretical and mathematical background of state-feedback control and model predictive control was introduced to build the foundations for the design of these controllers.

- In Chapter 3, first the design of the sFCI and its working in different modes was discussed as proposed by the designer. Then, a detailed analysis of the operating modes was carried out and the additional non-linearities of this topology were highlighted. In order to understand the different voltage and current responses of the sFCI during open-loop operation, a comparison was drawn with the conventional NPC converter. Finally, the three-phase sFCI, equipped with a LCL filter, was introduced and derivation of the mathematical model was presented, which is a prerequisite for the design of any control technique.

- In Chapter 4, a current control scheme based on the concept of state-feedback was designed separately for the single-phase and three-phase sFCI connected to the grid via an LCL filter. The controller designed in the (a, b, c)-reference frame (per-phase basis) was able to fulfill all objectives for the single-phase system. However, for the three-phase system, only a controller designed in (d, q)-reference frame was able to achieve all the control objectives. This highlighted the fact that there exists an in-built coupling between the flying capacitors of the three phases of the sFCI.

A pole-placement based design procedure was presented to achieve better dynamic and steady-state performance. The simulation results show that the resonance of the LCL filter is well damped, and the dynamic performance specified by direct pole placement is obtained for the reference tracking, grid voltage disturbance rejection, and balancing of flying capacitor voltages.

- In Chapter 5, a direct MPC—as a current controller—was proposed for the three-phase sFCI, and designed in the $(\alpha\beta)$-reference frame. The main motivation of using MPC was the uneven deviation in the current response of the state-feedback controller while transitioning from positive to negative cycle. The proposed MPC strategy was set to simultaneously control all the three states of the LCL filter via reference tracking. In a nutshell, the conventional MPC uses the cost function to penalize the errors between the measured values and the reference values. The simulation results highlighted the superior performance of the direct predictive controller compared to the state-feedback controller. The results also proved that the controller was able to achieve resonance damping using a simple passive damping resistor R_d.

  Furthermore, two major drawbacks of the classical direct model predictive control were discussed, namely *heavy computational efforts* and *variable switching frequency*. To overcome the heavy computational efforts, a sophisticated optimization procedure was derived using the concept of unconstrained minimum, which facilitates the use of long horizon control. Additionally, the problem of variable switching frequency was resolved by employing a modulator. This restricts the converter to a fixed switching frequency and hence the controller step time and sampling time were set to realistic values. The presented simulation results show that MPC schemes have a better dynamic performance compared to a linear controller (state-feedback control), shorter settling times, and also achieve superior reference tracking.

- In Chapter 6, one of the main drawbacks of using the flying capacitor, i.e., the voltage fly-away condition was highlighted. It was observed that the C_{FC} undergoes continuous charging under no-load/grid disconnected condition. This behavior is primarily due to the continuous charging procedure of the zero state. To overcome this issue two solutions were proposed. A simple, but effective solution was to use an extra switch S_5—anti-parallel to the switch S_4, with both these switches having the same gating signals. This method was shown to achieve the desired goal of maintaining the flying capacitor voltage near 400 V. However, this violated the actual design of the sFCI converter and was therefore not preferred.

  An alternative solution to this problem was proposed, in which the flying capacitor itself was considered as a system state. With this proposition, the system model was redefined to incorporate the dynamics of the flying capacitor and the converter bridge. This led to the derivation of the non-linear converter model, wherein the system changes cases based on various conditions. For verification of the derived non-linear model, a direct MPC technique was proposed for a single-phase sFCI. The control approach was split up into scheme-I and scheme-II, giving rise to a hybrid controller. During scheme-I the controller was tasked to maintain the C_{FC} voltage around its reference, while during scheme-II the controller worked as a reference tracking controller. In this manner the voltage fly-away condition was mitigated and using an extra switch was avoided.

  The simulation results highlighted the superior performance of the proposed hybrid controller. On one hand the hybrid control technique—with its operating scheme-I—can control the voltage of the flying capacitor during off-grid conditions, while on the other hand it can work as a reference tracking controller—during the scheme-II. The presented results verify the correctness of the non-linear model and working of the proposed hybrid controller.

- Finally in Chapter 7, implementation of the state-feedback controller on the hardware test-bench was presented for the single-phase sFCI. After a brief description of the test-bench,

the design of the control algorithm using C-code was discussed and various modules required for the same were highlighted. Additionally, the procedure adopted for grid connection was detailed. Furthermore, the response of the various modules was also discussed to highlight the performance of the designed control algorithm and affirm the fact that this recently proposed topology can be controlled to deliver desired power in grid connected mode.

Experimental results show the performance of the SFCC for grid current reference tracking and voltage control of the flying capacitor. The performance of the controller in terms of current response is satisfactory, but leaves a lot of room for improvement.

In a nutshell, the presented simulation and experimental results prove that this thesis was able to fulfill the objectives that were stated in the introduction, by providing control algorithms to facilitate grid connection of the sFCI. Although the sFCI has a very simple and robust design, using it during grid-connected mode poses some challenges due to the presence of the flying capacitor. Nevertheless, we can conclude that this newly proposed topology has a lot of potential to serve as an alternative in transformerless inverter applications, but requires further investigation and improvements in the proposed control algorithms.

8.2 Future outlook

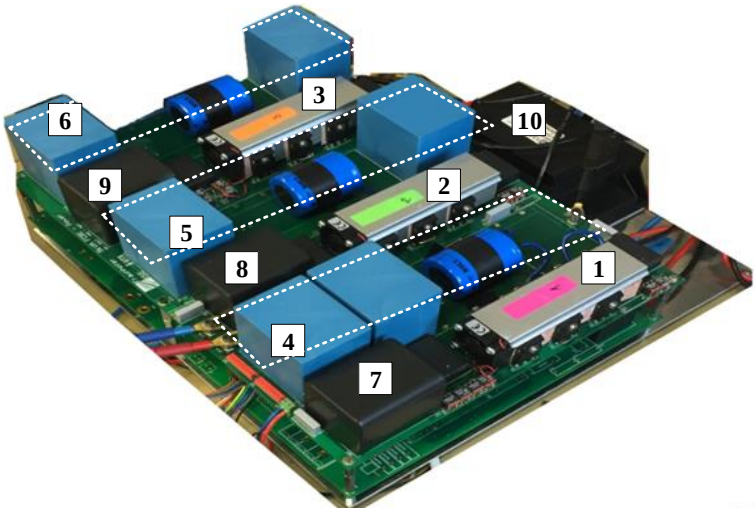
Finally, I would like to put forth some recommendations for future endeavors in this topic.

- In the presented work, the state-feedback control was designed using pole-placement approach which does not give optimal pole locations. An alternative approach would be to use a linear-quadratic-regulator (LQR) for calculation of the feedback gains and then compare the performance of the two approaches.
- In this thesis, the direct MPC scheme used a simple enumeration based approach. However, alternative techniques to reduce the computational burden could be utilized like branch-and-bound technique, move blocking strategy, and switch and extrapolate method. Accordingly, DMPC with longer prediction horizons could be implemented, which results in a remarkable improvement in the system performance and has the possibility of real-time implementation.
- The non-linear converter model of the sFCI resembles the piecewise affine systems and can be further refined. To improve the performance of the proposed direct MPC, a move blocking strategy can be employed which can predict the future responses for very large horizons. This has the potential to improve the performance of the proposed control approach and decrease the sampling frequency. Additionally, an integral state can be incorporated into the controller to improve the steady-state response.
- Finally, the CCS-MPC approach has a potential for real-time implementation, given the fact that it uses a modulator and the sampling time, the controller step time can be set to realistic values. Therefore, this control scheme can be implemented on the hardware test-bench and its response compared to the SFC.

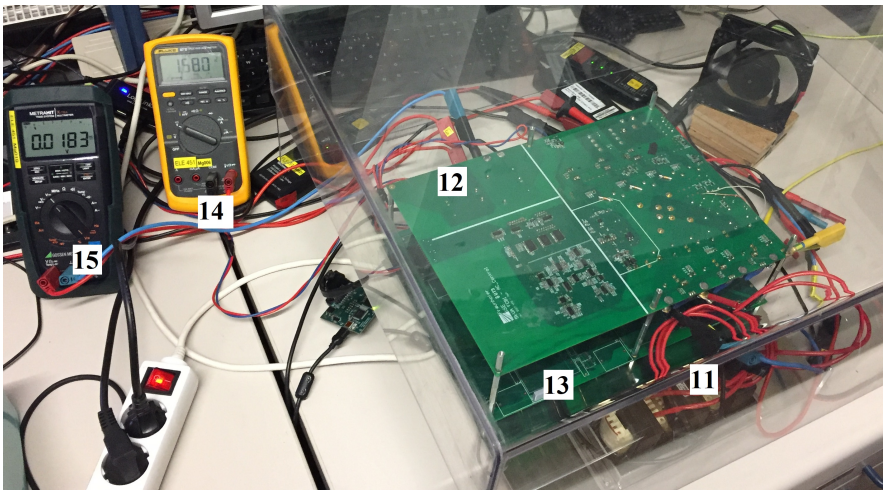
Appendices

Appendix A

Description of the Test Bench



(a) Three level, three-phase prototype of the sFCI constructed at Fraunhofer ISE.



(b) Experimental setup for implementation of state-feedback control using single-phase sFCI.

Figure A.1: Test-bench.

Figure A.1(a) shows the inverter prototype developed previously at Fraunhofer ISE. This setup was used for verification of the inverter operation during open-loop. Figure A.1(b) depicts the single-phase experimental setup that was used for the testing of the controller. The different components

are described below:

1, 2, 3 are the phases *a*, *b*, and *c* of the sFCI, respectively.

4, 5, 6 are the flying capacitors of phase *a*, *b*, and *c*, respectively.

7, 8, 9 are the input capacitors of phase *a*, *b*, and *c*, respectively.

10, 11 is the main inductor for the sFCI.

12 is the control PCB. It mainly consists of the controller and different measurement circuits.

13 is the power PCB. It consists of the topology and the two *dc*-links.

14, 15 are the voltage measurements for flying capacitor and the input *dc*-link, respectively.

Appendix B

Abbreviations and symbols

B.1 List of abbreviations

Abbreviation	Meaning
ac	alternating current
ADC	analog to digital converter
CMV	common-mode voltage
CCS-MPC	continuous-control-set model predictive control
CLA	control law accelerator
dc	direct current
DVFC	dc voltage feedforward compensation
DMPC	direct model predictive control
FCS-MPC	finite-control-set model predictive control
FC	flying capacitor
LCL	inductor-capacitor-inductor filter
LQR	linear quadratic regulator
MPC	model predictive control
MLI	multi-level inverter
MCU	microcontroller unit
NPC	neutral point clamped
PV	photovoltaic
PR	proportional resonant
PLL	phase locked loop
PCC	point of common coupling
PWM	pulse width modulation
PCB	printed circuit board
RB-IGBT	reverse blocking IGBT
sFCI	Siwakoti-H flying capacitor inverter
SFC	state-feedback control
SFCC	state-feedback current control
SOGI	second order generalized integrator
SDFM	sigma-delta filter module
THD	total harmonic distortion
VSI	voltage source inverter
VOC	voltage oriented control
ZOH	zero-order-hold

B.2 List of symbols

Symbol	Meaning
u_{dc}	voltage across dc-link capacitor
u_{FC}	voltage across the flying capacitor
u_m	output voltage of the converter bridge
u_f	voltage across filter capacitor
u_g	grid voltage
i_{dc}	input current to the converter
i_m	current flowing in the main-inductor
i_g	current flowing in the grid-side inductor

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