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Detector Emulation for Athena WFI Performance Verification

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Abstract

The ESA mission Athena is a space-based X-ray observatory scheduled for launch in 2028. One of the two focal plane instruments is the Wide Field Imager, a camera for imaging and spectroscopic applications sensitive in the X-ray range. The WFI detects X-ray photons with a active pixel sensors of DEPFET type. The detected signals are further processed in an electronics chain, which includes digitizing the sensor data, FPGA-based processing of the signal in real-time and transmission to the spacecraft's mass memory.
Currently, the WFI is in technology development phase. In this phase, all components critical for use in space are examined for technical feasibility.

The focus of this work lies on the performance verification of the WFI signal processing chain. Therefore, a new end-to-end method is developed to test, evaluate and verify critical components of this chain. The method substitutes the detector by a programmable emulator which generates output signals in real-time according to the detector signals. With specific models, observations of objects in space in combination with detector characteristics of the later flight camera under environmental conditions can be reproduced in a laboratory setup. Subsequent comparison of the given input data with the output data results in the evaluation and verification of the signal processing chain.

The emulator is realized in a hardware/software codesign. The computation-intensive algorithms for modeling of the input data and detector characteristics are implemented in software on a high-performance PC. The real-time generation of the analog output data takes place on an FPGA-based hardware with eight digital-to-analog converters operated in parallel. This architecture allows to generate image sizes up to 512×512 pixels and an adjustable frame rate of up to $780\,\mathrm{fps}$ which meets the requirements for the WFI camera. With an oversampling of 16 samples per pixel and a resolution of $16\,\mathrm{bit}$ per sample, the maximum data rate is $51.2\,\mathrm{Gbit/s}$.

The emulator can be used during all project phases. At an early stage, technical requirements of the signal processing chain can be derived, while at a later stage the emulator is used as instrument of the electrical ground support equipment for verification of the WFI electronics. With this system, critical submodules can be tested in functionality before they are connected to other flight modules of the WFI. During the in-orbit phase, the emulator can be based on real observation data to model the behavior of the detector in space, in order to ensure integrity of scientific data.

Kurzfassung

Die ESA Mission Athena ist ein Röntgenobservatorium, das 2028 auf einem Satelliten in den Weltraum befördert werden soll. Eins seiner zwei wissenschaftlichen Instrumente ist der Wide Field Imager. Der WFI ist eine Kamera für spektroskopische und bildgebende Anwendungen im Röntgenbereich. Hierfür werden Röntgenphotonen mit aktiven Pixelsensoren vom Typ DEPFET detektiert. Die detektierten Signale werden in einer Signalverarbeitungskette weiter prozessiert. Diese umfasst das Digitalisieren der Sensorsignale, die FPGA-basierte Datenprozessierung in Echtzeit bis hin zur Übertragung an den Massenspeicher im Satelliten.
Derzeit befindet sich der WFI in einer Technologie Entwicklungsphase. In dieser Phase werden alle für den Einsatz im Weltall kritischen Komponenten auf technische Machbarkeit untersucht.

Der Schwerpunkt dieser Arbeit liegt auf der Verifikation der Funktions- und Leistungsfähigkeit der Signalverarbeitungskette des WFI. Dafür wird eine neue Methode entwickelt, um kritische Komponenten der Signalkette zu testen, evaluieren und zu verifizieren. Diese Methode substituiert den Detektor durch einen programmierbaren Emulator, welcher Ausgangssignale entsprechend den Detektorsignalen in Echtzeit erzeugt. Mit speziellen Modellen können Observationen von Objekten im Weltall in Kombination mit Detektoreigenschaften der späteren Flugkamera unter Umgebungsbedingungen in einem Laboraufbau reproduziert werden. Ein anschließender Vergleich der gegebenen Eingangsdaten mit den Ausgangsdaten ermöglicht die Evaluierung und Verifizierung der Signalverarbeitungskette.

Der Emulator ist in einem Hardware/Software-Codesign realisiert. Die rechenintensiven Algorithmen zur Modellierung des Eingangssignals und der Detektoreigenschaften sind in einer Applikationssoftware auf einem leistungsstarken PC implementiert. Die echtzeitfähige Generierung der analogen Ausgangsdaten erfolgt auf einer FPGA-basierten Hardware mit acht parallel arbeitenden Digital-zu-Analog Konvertern. Diese Architektur ermöglicht es, Bildgrößen bis zu 512×512 Pixeln und einer einstellbaren Bildrate von $780\,\mathrm{fps}$ darzustellen um die Anforderungen der WFI Kamera zu erfüllen. Mit einer Überabtastung von 16 Werten pro Pixel und einer Auflösung von $16\,\mathrm{bit}$ pro Ausgabewert ergibt sich die maximale Gesamtdatenrate zu $51.2\,\mathrm{Gbit/s}$.

Der Emulator kann während allen Projektphasen eingesetzt werden. In einer frühen Phase, können technische Systemanforderungen der Signalprozessierungskette abgeleitet werden, während in einer späteren Phase der Emulator als Testsystem zur Verifikation des WFI verwendet wird. Kritische Submodule können auf ihre Funktionalität geprüft werden, bevor sie an andere Flugmodule des WFI angeschlossen werden.

Während der In-Orbit Phase, kann mittels Emulator und realen Observationsdaten das Verhalten des Detektors im Weltall nachgebildet werden um die Integrität der wissenschaftlichen Nutzdaten zu verifizieren.

Contents

1. Introduction

Within this thesis, a new evaluation method has been designed for use within development, verification and test of the Wide Field Imager (WFI) of the space mission Advanced Telescope for High-Energetic Astrophysics (Athena) by the European Space Agency (ESA).

1.1. Objective

There is a fundamental interest of mankind to understand how the Universe did arise and evolves in the future. This gives raise to numerous open questions concerning the mechanisms in interaction of energy and matter. To answer these questions, observations need to be carried out, from celestial, faraway and faint objects which are beyond the reach of current ground and space-based instruments. Therefore a variety of new cutting-edge space telescopes are designed, like the James Webb Space Telescope (JWST) or the Euclid mission which offer sensitivity from visible light to the infrared range [57], [33]. To investigate the Universe in the X-ray energy range, ESA has started the mission Athena as second large class mission within their Cosmic Vision Program. Due to its large mirror system and unique instruments, it will be about hundred times more sensitive than the existing X-ray telescopes Chandra and XMM-Newton [73], [119], [122].

One of two complementary payload instruments of Athena is the WFI, an X-ray camera with a large field of view, high count-rate and spectroscopic measurement capability. The WFI is an outstanding survey instrument, significantly surpassing currently existing capabilities. This instrument will feature unique technologies comprising an X-ray detector with the largest sensitive area and very high frame rates compared to present space cameras. Large detector size and fast readout speed result in an extremely high data rate of approximately $2 \cdot 10^8$ pixels per second, which demands innovative real-time data pre-processing on-board of the satellite.

After the start of the elaborate development in 2014 it is scheduled until 2028 to finish the flight model. Currently, the Athena mission and WFI instrument are in

the technology development phase. During this phase, technology development is performed in order to reach a certain technical maturity of all components, that are critical with regard to an operation in space [81], [27]. Within the WFI, the critical electronic elements are the X-ray detectors and the real-time data pre-processing [70]. Both are part of the signal processing chain, which reaches from the sensing of photons to the output of possibly detected X-ray sources. Its key element is a next generation X-ray detector based on the latest DEPFET sensor technology. Additional features of the processing chain are, for instance, signal digitization, correction, event detection and data reduction in real-time.

This thesis focuses on the performance verification of the WFI signal processing chain. During every project phase, it is indispensable to characterize, further develop and improve this system. This ensures optimized system performance and minimizes the risk of failures. Therefore, a method is developed to evaluate and verify the critical parts of the WFI signal processing chain. Investigations of different methods are carried out in terms of applicability for evaluation and verification. Based on the results, a novel evaluation method is defined which substitutes the detector with a newly developed emulator instrument, called Programmable Real-Time Emulator (PRE). This instrument applies models of the detector system in order to emulate a signal according to the output of the detector. By varying the input and model characteristics, various effects can be generated. These variations can be detector based effects or external effects due to radiation environment in the orbit. Embedding the PRE in the signal processing chain with subsequent comparison of the well-known input with the output data enables to verify the signal processing chain.

Therefore, the PRE is developed in a well-engineered technology to map its characteristics to the challenging WFI science requirements. The PRE is composed in a hardware/software codesign based on a powerful PC for detector modeling and a high performance FPGA platform with eight parallel sampling DACs. An advanced firmware design enables to generate the WFI output data in real-time. In particular, frame sizes of up to 512×512 pixels can be processed with an adjustable frame rate of up to $780\,\mathrm{fps}$. The adjustable frame rate is thereby greater by a factor of approximately 4 than it is required for the large detector of the WFI. For an accurate representation of the individual pixel values, a high-speed timing is introduced to oversample each value by a factor of 16, resulting in a total data rate of $51.2\,\mathrm{Gbit/s}$.

The PRE is realized in a modular and flexible way, to provide the appropriate support in every particular project phase. Accordingly, the main characteristics of the detector as well as X-ray input and environmental influences need to be predicted and repre-

sented by the emulator models. Especially in the early development phase, when the WFI detectors are still under development and are not available for realization of the complete signal processing chain, the emulator presents a very powerful instrument to derive requirements for the system. During the development phase of the WFI, the evaluation method comprising the PRE is applied for performance verification and functional qualification of the signal processing chain as part of the EGSE for electronic subsystems. Throughout mission operation, the PRE can be based on real observation data to model the detector in the satellite. This opens the possibility to detect failures or misbehavior of the WFI signal processing chain on ground. With the method comprising the PRE it is possible to transfer astrophysical requirements to engineering technology.

1.2. Outline

The outline of this thesis is started with an introduction on the Athena mission within chapter 2. A brief abstract of the history of X-ray imaging is given in section 2.1 followed by a description of the ESA science theme of the Athena mission in section 2.2. A summary of the main features and characteristics of the X-ray telescope with its payload instruments is described in section 2.3. This work focuses on the WFI instrument. The working principle and science requirements are detailed in section 2.4.

Chapter 3 discusses evaluation methods of the WFI signal processing chain. Different approaches of evaluation and verification are given in section 3.1. The outline of section 3.2 are investigations with respect to modeling and emulating the detector system. Finally, the new end-to-end evaluation method based on a Programmable Real-Time Emulator (PRE) is introduced.

Within chapter 4, an introduction of the theory behind X-ray detection with semiconductor sensors is given. The interaction of radiation and matter is described in section 4.1 in principle, thereafter details about the noise contributions of an X-ray detector system are outlined in section 4.2. Three different sensor technologies for X-ray detection and their working principle are summarized in section 4.3. In section 4.4, the main advantages of Depleted P-Channel Field Effect Transistor (DEPFET) based sensors are analyzed and compared with respect to alternative technologies for X-ray detection.

Chapter 5 outlines X-ray imaging with the WFI instrument based on DEPFET detectors. First, the detector system is explained in section 5.1, in particular the detector operation and readout. Section 5.2 introduces the data acquisition and processing, which is

performed by the Detector Electronics (DE) subsystem of the WFI. Detector degradation due to environmental conditions in orbit are discussed in section 5.3.

Within chapter 6, the conceptual design of the PRE, an instrument for evaluation of the WFI signal processing chain is described. First, the requirements of the PRE are derived in section 6.1 mainly from WFI science requirements, followed by an investigation of different implementation concepts in section 6.2. Finally, section 6.3 summarizes the overall concept of modeling and emulating of the detector system featured in a PRE.

Chapter 7 describes DEPFET detector modeling using the PRE instrument. Section 7.1 gives an overview of all modeling steps, while section 7.2 to section 7.4 detail the models for signal input, timing and readout and detector characteristics.

Chapter 8 introduces the architecture of the PRE. The firmware concept and real-time processing of the modeled image data is explained in section 8.1. From this, the hardware requirements are derived and the best suited hardware platform is selected in section 8.2. Section 8.3 illustrates the software environment for detector modeling and operation of the PRE.

Within chapter 9, the end-to-end verification method of the WFI signal processing chain is presented. First, results of comparing measured and modeled detector effects are given in section 9.1. Additionally, investigations of the correlation between the PRE models and the SIXTE simulation tool based on a scientific observation as input are described. Further, the setup of WFI signal processing chain verification with the present breadboard model of the Detector Electronics Frame Processor followed by a verification plan is outlined in section 9.2. Finally, in section 9.3, verification examples of the WFI signal processing chain to derive technical requirements are presented.

The conclusion of this work is given in chapter 10. The main features and results based on the end-to-end evaluation method and developed PRE instrument are summarized in section 10.1. In section 10.2 future developments and scientific applications of the PRE are discussed.

2. Athena Mission

This chapter introduces the research field of X-ray astronomy by means of ESA's X-ray observatory Athena. First an overview of the history of X-ray astronomy is given in section 2.1, followed by the scientific objectives of the Athena mission, explained in section 2.2. The Athena telescope with its two scientific instruments is detailed in section 2.3. Section 2.4 focuses on the WFI instrument and its performance requirements.

2.1. X-Ray Astronomy

X-ray astronomy is essential for understanding the Universe. The energy of an X-ray photon is about 1000 times the energy of a photon of visible light. X-rays are emitted from different objects and phenomena within a wavelength range from $0.01\,\mathrm{nm}$ to $10\,\mathrm{nm}$ corresponding to an energy range of approximately $0.1\,\mathrm{keV}$ to $100\,\mathrm{keV}$. An estimate of the necessary conditions for the emission of X-ray photons can be derived from the spectrum of a black body, which is described by Planck's formula [80]

$$\rho(\nu, T)d\nu = \frac{8\pi h\nu^3}{c^3}\frac{1}{e^{\frac{h\nu}{k_B T}} - 1}d\nu. \tag{2.1}$$

The relationship between the temperature T of a black body and the frequency ν and thus the energy E at which it emits the most light can be calculated according to Wien's law [120], [38]

$$\begin{aligned} \nu_{max} &= \frac{2.82 \cdot k_B}{h}T \\ E_{max} &= h\nu_{max} = 2.82 \cdot k_B T. \end{aligned} \tag{2.2}$$

Planck's formula as given in equation 2.1 indicates, that the black body radiation intensity increases in all wavelength as the temperature of the body increases. According to Wien's displacement law, described in equation 2.2, the peak of the intensity curve shifts towards shorter wavelength as the temperature of the body increases. These two properties of the black body radiation are depicted in figure 2.1. This correlation can be exploited in calculating the unknown temperature of a black body by fitting its energy

curve with the theoretical black body radiation curves. In X-ray astronomy, this is done to determine for instance the temperatures of stars, assuming that stars radiate like black bodies by fitting their energy distribution curve approximately with that of a black body of known temperature.

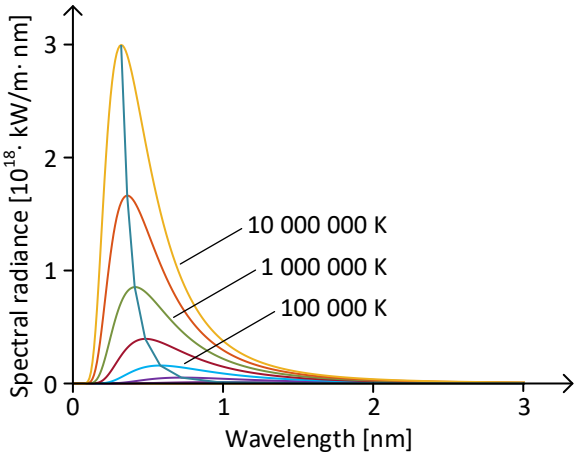


Figure 2.1.: Black body intensity (Planck law) as a function of wavelength for a number of emitting temperatures.

According to equation 2.2, the corresponding temperatures for soft X-rays in the energy range of $0.1\,\mathrm{keV}$ to $10\,\mathrm{keV}$ can be calculated to

$$\begin{aligned} T(E_{max} = 0.1\,\mathrm{keV}) &\approx 4.1 \cdot 10^5\,\mathrm{K} \\ T(E_{max} = 10\,\mathrm{keV}) &\approx 4.1 \cdot 10^7\,\mathrm{K}. \end{aligned} \tag{2.3}$$

Thus, X-ray emission is expected from astronomical objects and phenomena that contain extremely hot gases at temperatures from ten thousand up to several million degrees Kelvin.

These objects and phenomena and much more beyond this can be observed with instruments sensitive in the X-ray range. But gases in the Earth's atmosphere absorb electromagnetic energy at certain wavelengths. Figure 2.2 depicts the opacity of the earth atmosphere over the electromagnetic spectrum. Opacity describes the absorption and scattering of radiation in a medium. In some parts of the spectrum, for instance the visible, the energy is only very less absorbed, while in other energy bands like the Ultraviolet to X-ray band nearly all energy is absorbed. Since X-rays are also absorbed and scattered by the Earth's atmosphere, they cannot be observed from ground. Therefore, instruments to detect X-rays emitted by extraterrestrial objects must be launched to high altitudes by balloons, sounding rockets, and satellites.

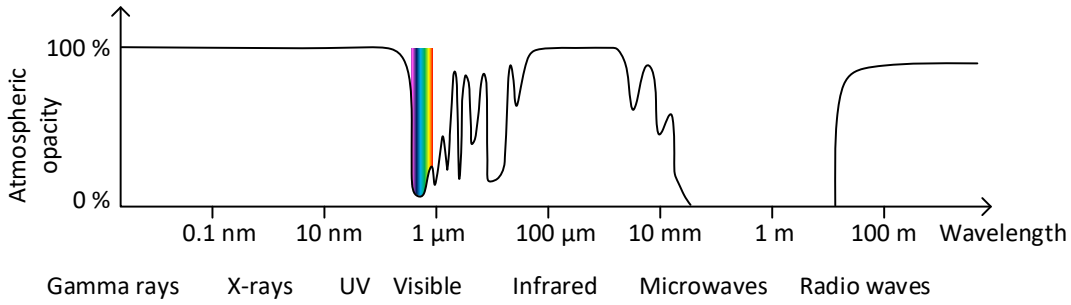


Figure 2.2.: Atmospheric absorption of energy over the electromagnetic spectrum (adapted from [61]).

One of the first measurements of solar X-rays, was taken with a photon counter tube on a V-2 rocket in 1949 [32].
In 1962, another revolutionary rocket experiment tried to observe the scattered X-rays of the Moon caused by radiation from the Sun. Instead, a bright source in the constellation scorpion was discovered, named Scorpius X-1, the first known X-ray source outside the solar system [39].
In order to achieve longer observation times, the X-ray detection instruments needed to be operated on satellites. With the launch of the first dedicated X-ray satellite Uhuru by NASA in 1970, the era of space based X-ray astronomy began. Uhuru, or also known as Small Astronomical Satellite 1 (SAS-1), performed an X-ray sky survey using two sets of conventional proportional counters with a simple honeycomb collimator. The instrument captured the entire sky for the first time and allowed to catalog about 300 objects.
A few years later, in 1978, NASA launched the High Energy Astronomical Observatory 2 (HEAO-2), later renamed to Einstein, the first observatory applying a Wolter-I telescope for X-ray focusing. Einstein provided a sensitivity several 100 times larger than the mission before. It observed shock waves from exploded stars, and made the first X-ray images of hot gas in galaxies and galaxy clusters. Einstein enabled to locate accurately over 7000 X-ray sources [40].
Followed by the Roentgensatellite ROSAT in 1990, a joint venture of Germany, the United Kingdom and the United States, a first all-sky survey with an imaging X-ray telescope in the energy band of $0.1\,\mathrm{keV}$ to $2.4\,\mathrm{keV}$ was possible [112]. In total, the quantity of known X-ray sources was extended to around 125000 by ROSAT's all-sky survey [116].
Two major X-ray observatories are currently in orbit: ESA's XMM-Newton [49] and NASA's Chandra [118], both launched in 1999. After the first detection of an extrasolar

X-ray source, these observatories have achieved an increase in sensitivity to observe high energetic processes, such as accretion processes around black holes, star formation and supernova explosions.
A future mission is the German telescope eROSITA (extended Roentgen Survey with an Imaging Telescope Array) [85]. eROSITA can be regarded as follower mission of ROSAT. An all sky survey will be carried out with a higher energy resolution, a wider energy range and higher sensitivity. The number of discovered X-ray sources is thereby expected to increase up to several millions.
In 2013, ESA accepted the "Hot and Energetic Universe" as science theme for its next large (L-class) mission, which is expected to be launched in 2028 [24], [73]. Therefore the mission Athena was selected as ESA's next space observatory for exploration of the X-ray sky. The scientific objectives of the mission and a detailed description of the telescope with its instruments are covered in the next sections.

2.2. ESA Science Theme: The Hot and Energetic Universe

The "Hot and Energetic Universe" has been selected as the science theme for the second large-class mission, due for launch in 2028, in ESA's Cosmic Vision program [22], [73].

The theme poses two astrophysical key questions:

1. How does ordinary matter assemble into the large-scale structures we see today?
2. How do black holes grow and shape the Universe?

After the big bang, about 13.4 billion years ago, the Universe was almost completely filled by a smooth distribution of matter. Over time, the matter distributed into filaments, the largest-scale structures in the Universe, which extended across space and include clusters of galaxies. Filaments are separated by immense regions, not occupied by matter, creating a vast foam-like structure sometimes called the "cosmic web" [17]. The spaces between galaxies refer to the so-called warm-hot intergalactic medium, with temperatures between hundred thousand to millions degrees Kelvin. Computer simulations reveal that a large part of the ordinary matter (baryonic matter) of the Universe currently exists in the state of the warm-hot intergalactic medium [18].
As the Universe evolved, the matter filing the cosmic web concentrates and the temperature increased drastically, causing the Universe to shine not in optical but in X-ray light. X-ray images show that the hot Universe is dominated by gas with temperatures up to million of degrees. It is crucial to understand how the Universe has evolved over time into today's structure of galaxies and hot gas.

Almost all galaxies contain a Supermassive Black Hole (SMBH) in their center with the mass of millions or even billions times the mass of the Sun. The growth of SMBH and star formation are the two fundamental astrophysical processes which drive galaxy evolution. Accretion onto SMBH release immense amounts of energy, in form of radiation and emitted energy. Massive winds and outflows transport this energy to galaxy scale or larger scale, where it regulates both star formation and accretion during periods of galaxy growth. When SMBHs grow, X-rays originate at the event horizon which can be observed even at obscured environments as they penetrate through significant amounts of obscured gas. However, the exact mechanisms of this feedback process is not known.
Understanding the energetic Universe demands a complete census out to the epoch where accretion and star formation occurred. Moreover, both the inflows and outflows of matter and energy in the vicinity of black holes must be observed [73], [11].

To understand the "Hot and Energetic Universe", the baryonic component of the Universe, locked up in hot gas at temperatures of millions of degrees and high energetic processes, close to the event horizon of black holes need to be observed. This requires space-based observations in the X-ray range of the electromagnetic spectrum [73].

By combining a large X-ray telescope with innovative scientific instruments, it will be possible to deliver an important contribution to answer the questions posed by the "Hot and Energetic Universe" science theme.

2.3. Athena X-ray Observatory

The X-ray observatory Advanced Telescope for High-Energetic Astrophysics (Athena) is selected as next L-class mission in the Cosmic Vision Science program by the European Space Agency (ESA) to address the science theme "Hot and Energetic Universe". Athena is scheduled for launch in 2028 by an Ariane 6 vehicle. It will operate at the second Sun-Earth Lagrangian point in a large halo orbit, providing a very stable thermal environment as well as good uninterrupted sky visibility and high observation efficiency. Athena will perform up to 300 observations of celestial targets per year. Typical observations last $100\,\mathrm{ks}$ but can be in the range of $1\,\mathrm{ks}$ to $1\,\mathrm{Ms}$. The baseline mission lifetime is 5 years with the opportunity to extend the mission by 5 years in addition.

Figure 2.3 depicts the Athena spacecraft in its actual configuration. It consists of four main components: the Mirror Assembly Module (MAM), the Service Module (SVM),

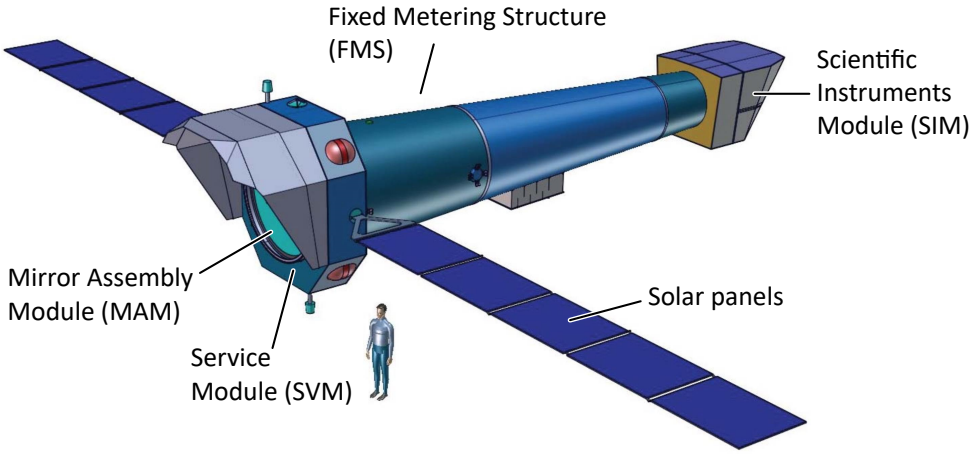
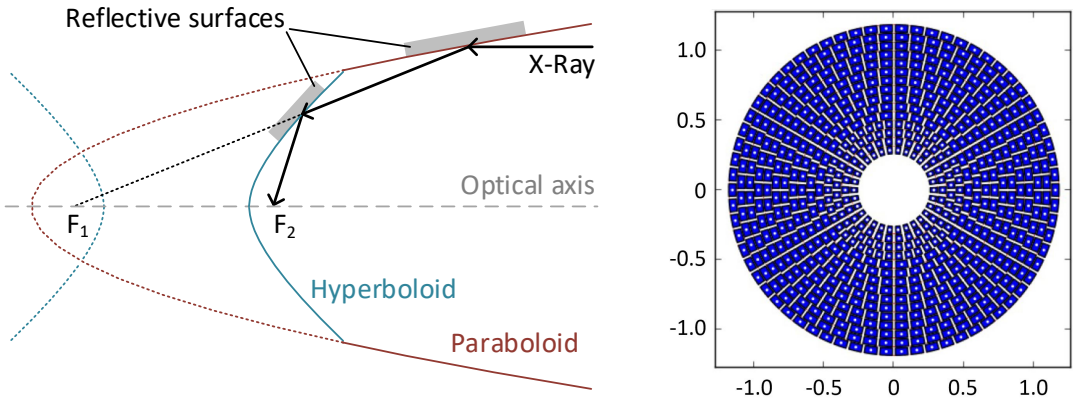


Figure 2.3.: Athena X-ray telescope with the entrance window of approximately $3\,\mathrm{m}$ diameter and $12\,\mathrm{m}$ focal length. The Service Module holds the mirror connected to the Fixed Metering Structure which builds the telescope tube with the scientific instrument module (SIM) at its end. The SIM houses the payload instruments WFI and X-IFU. The length of the spacecraft with deployed sun shield is nearly $16\,\mathrm{m}$, while it spreads with its solar panels across $26\,\mathrm{m}$ [8], [23].

the Fixed Metering Structure (FMS) and the scientific instrument module (SIM). The SVM features all systems necessary to maintain the spacecraft. It is built around the MAM which holds the mirror structure, housing the Silicon Pore Optics (SPO) mirror modules. The FMS forms the telescope tube and holds on its end the SIM which accommodates the two scientific payload instruments: the Wide Field Imager (WFI) and the X-ray Integral Field Unit (X-IFU), depicted in figure 2.5. The observatory provides one large mirror for both payload instruments. Therefore, the mirror system can be tilted to focus either one of the two instruments.

The Athena mirror system is based on a Wolter-I type optics, as depicted in figure 2.4a [123]. Using a parabolic mirror followed by a hyperbolic mirror allows to build the telescope with a focal length of $12\,\mathrm{m}$. As X-rays are only reflected under grazing incidence, a single mirror set would not collect much of the incoming photons. Hence, a set of nested mirrors with different radii but the same focal length is arranged concentrically to the optical axis. Conventional X-ray mirrors are made with gold coated nickel surfaces. The Athena mirror features Silicon Pore Optics (SPO) technology providing an angular resolution of $\sim 5''$. This new technology allows an excellent effective area-to-mass ratio by applying highly polished silicon wafer reflecting plates. Many plates form modular, compact mirror modules which are mounted in concentric

rings, as shown in figure 2.4b [8].



(a) Wolter-I type configuration for focusing X-rays

(b) SPO-based mirror system

Figure 2.4.: (a) Scheme of a Wolter-I type mirror system utilizing two reflections, first by a parabolic surface followed by a hyperbolic surface. By means of double reflection, the focal length can be shortened from the focal point F1 to the focal point F2. (b) Layout of the SPO mirror modules as seen from the front (units are in m) [8].

The X-IFU is a X-ray spectrometer consisting of a large array of microcalorimeters based on superconducting Transition Edge Sensors (TESs) operating at cryogenic temperatures of $\sim 90\,\mathrm{mK}$. A microcalorimeter is a thermal X-ray detector which determines the energy of an X-ray photon by measuring the small temperature rise caused by the absorption of a single photon in the detector. By measuring the temperature rise, the energy of the incident photon can be reconstructed. The X-IFU will provide spatially resolved high-resolution spectroscopy over a small field of view in the soft X-ray range. Detailed information on the X-IFU and its X-ray detection principle can be found in literature [12], [13], [98] and [42].

The WFI is an X-ray camera which provides imaging in the $0.2\,\mathrm{keV}$ to $15\,\mathrm{keV}$ band with state-of-the-art spectroscopy and high time resolution over a wide field of view. This performance is achieved by utilizing active pixel sensors based on DEPFET (Depleted P-Channel Field Effect Transistor) technology. Two different detectors are comprised, a large area detector for observations requiring a large field of view and a high count-rate detector for observations of very bright point sources [88], [70]. Figure 2.6 depicts two simulations of typical observations with the large and fast sensor. A detailed description of the WFI instrument can be found in section 2.4.

The key parameters and scientific requirements of the Athena mission are summarized in literature [73].

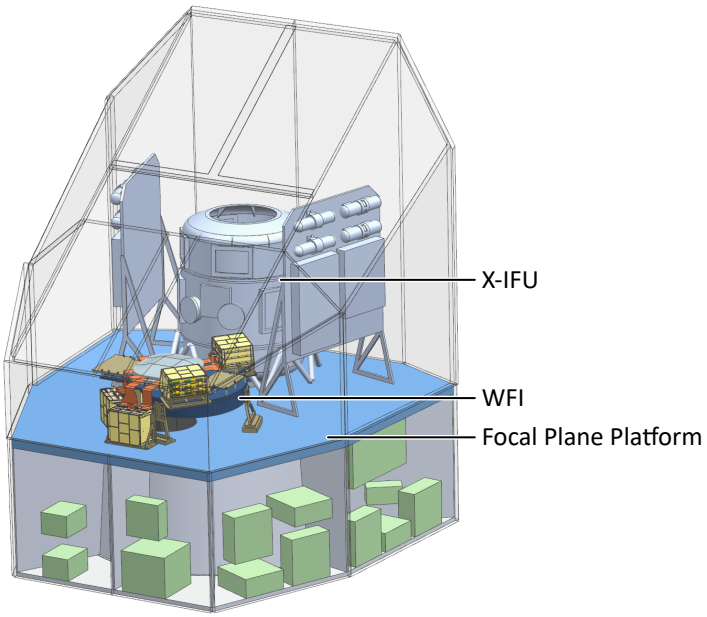


Figure 2.5.: Detailed image of the SIM with the payload instruments WFI and X-IFU (image credit: ESA, Max Planck Institute for Extraterrestrial Physics (MPE)).

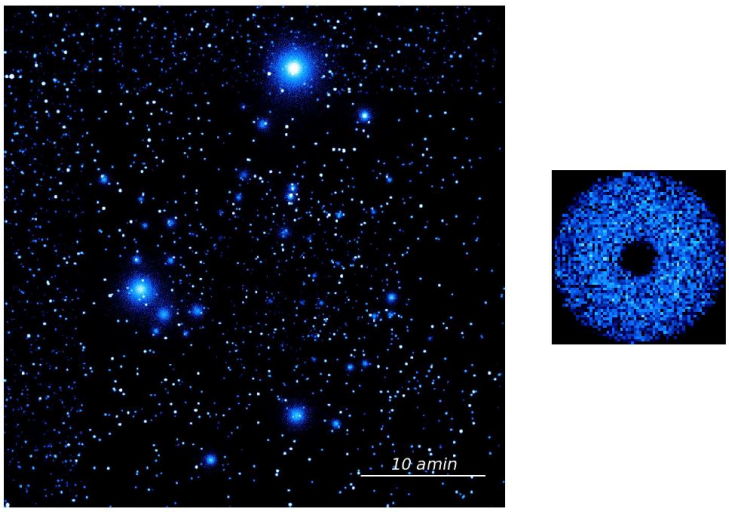


Figure 2.6.: *Left:* 100 ks Simulation of X-ray Telescopes (SIXTE) simulation of an observation with the WFI large field of view detector. Shown is Chandra Deep Field South (CDFS) with objects representing clusters of galaxies observed with the Chandra telescope. *Right:* Simulation of an observation of a bright source with the WFI fast detector. Defocusing of the fast detector (FD) results in a circular photon distribution, which mimics the geometry of the Athena mirror assembly. The image is enlarged by a factor of six and does not represent the true scale compared to the right image [89].

2.4. Wide Field Imager Instrument

The Wide Field Imager is one of two scientific instruments of the Athena X-ray observatory. The main task of the WFI instrument is to measure precisely energy, incidence angle and time from X-ray photons in the planned energy range. To accomplish these goals, it is mandatory that the WFI provides a fast readout and a high frame rate over a wide field of view. In the following, the WFI hardware architecture and its concept of operation is presented.

WFI Architecture

Figure 2.9 depicts a schematic diagram of the WFI instrument with its subsystems. A conceptional 3-dimensional drawing of the WFI with subsystems Filter and Calibration Wheel (FW), Detector Electronics (DE) and Camera Head (CH) is shown in figure 2.7.

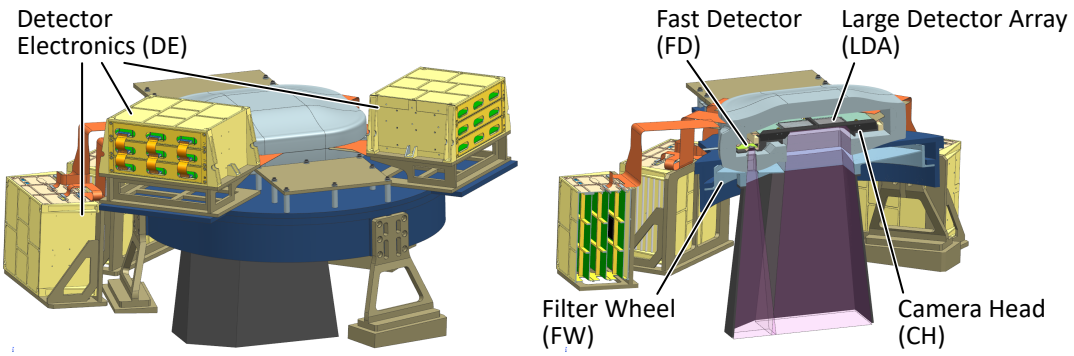
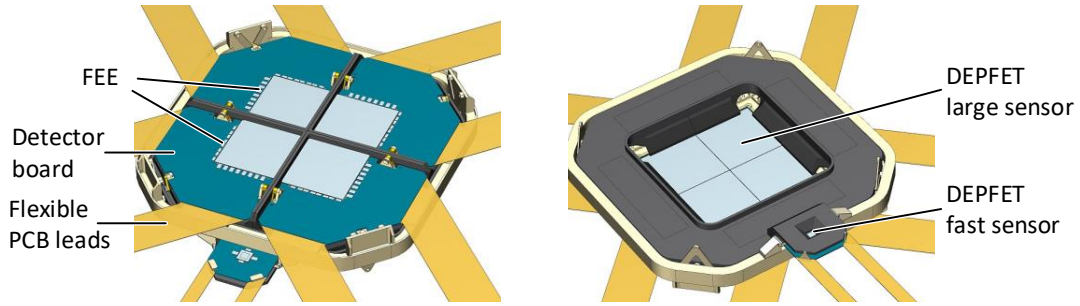


Figure 2.7.: Concept drawing and cross-sectional view of the WFI with subsystems FW, DE and CH including large detector array (LDA) and FD.

Key element of the WFI are the X-ray sensors. These sensors are pixel matrices, utilizing DEPFET technology. A detailed description of the DEPFET principle is given in sections 4.3.4 and 5.1. Two different sensor designs are incorporated in the WFI, a large area sensor and a fast timing sensor. The large sensor consists of a set of four sensors called quadrants, each with 512×512 pixels. The fast sensor is composed of 64×64 pixels. The sensors are connected to dedicated Front-End Electronics (FEE) for row-steering and readout. A sensor with its FEE is considered a detector. Each quadrant of the large area sensor with appropriate FEE is called large detector (LD), all four LDs build the large detector array (LDA). The fast timing sensor with its FEE is designated as fast detector (FD).

Figure 2.8 pictures a front and back view of the WFI detectors on the detector board. The detector boards, including LDA and FD are surrounded by a proton and graded-Z shielding to reduce the instrumental background and minimize radiation damage. They form, together with their electrical, mechanical and thermal interfaces, the CH.



(a) WFI detector front view

(b) WFI detector back view

Figure 2.8.: WFI detectors on the detector board inside the CH. The large detector consists of four quadrants, each with eight Switcher-A and eight Veritas-2 ASICs. The fast detector is mounted defocused to improve its count rate capability. The FEE is mounted at the rigid detector boards next to the sensors in order to enable wire bonding. The flexible leads are used as connections of the detectors inside the CH to the Detector Electronics.

A FW is integrated in the ray path to control the photon flux with four different positions and functions [87], [10]. The first position holds an optical and ultraviolet (UV) light blocking filter which is used during observations. This is necessary because the sensor is also sensitive to UV and visible light, which would degrade the energy resolution of the camera. In addition, the light blocking is enhanced by an Al layer on the photon entrance window of the sensor. A second position holds an on-board calibration source for recalibration of the instrument during the mission. The third is closed, to completely block the radiation path, in order to perform background measurements or to protect the detector. The fourth position is open, which is used for evacuation of the filter wheel and camera head. Additionally, measurements of low X-ray energies with low optical loading are performed with open aperture.

Each detector is connected via flexible PCB leads to one of five DEs, as depicted in figure 2.7. The DEs are linked to the Instrument Control and Power-Distribution Unit (ICPU) which serves as interface to the spacecraft (SC). Further, the ICPU is responsible for controlling the instrument and distributing power to all subsystems.

The WFI CH, DE and ICPU are power consuming subsystems, which have to be cooled. In particular the WFI sensors need to be operated at low temperatures of approximately 190 K for maximum performance. Therefore, the well-proven concept of passive cooling system consisting of heat pipes and radiators is used. Heat pipe interfaces for each subsystem are provided, to thermally connect the system to the radiators (not shown in the pictures) [71].

WFI Concept of Operation

Figure 2.9 depicts the operational and processing concept of the WFI within its subsystems. The incoming X-ray photons are focused through the mirror system of the Athena telescope and a dedicated filter, onto the sensor plane of the WFI. The mirror system can be tilted to focus either the LDA or the FD. The X-ray photons generate signal charges in the sensor, proportional of their energy. Each DEPFET pixel accumulates the generated charges continuously. The signal charges are readout row-wise in a rolling shutter (RS) mode either as a current or a voltage signal. While reading out a row, the collected charge is removed and the next exposure started.

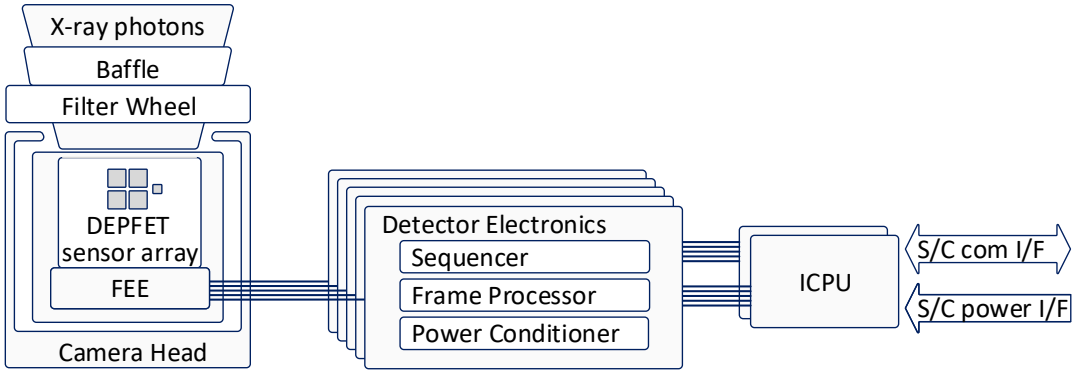


Figure 2.9.: Overview of the WFI signal processing within the subsystems (adapted from [81]).

The switching of the DEPFET rows is performed by the Control Front-End Electronics (CFE), the row-steering ASIC Switcher-A. One Switcher-A is capable of controlling 64 sensor rows, so that in total eight ASICs are implemented in an LD. The FD is readout in two halves, therefore two Switcher-A devices are implemented to activate two rows in parallel.
Readout and shaping of the analog signals of the sensors is utilized by the Analog

Front-End Electronics (AFE), the 64-channel readout ASIC Veritas-2. The four large sensors are connected to eight Veritas-2 ASICs respectively, while the fast sensor is divided in two halves and read out by two ASICs. AFE and CFE are explained in more detail in section 5.1.3 and 5.1.4.
Figure 2.10 shows a picture of a WFI prototype detector with 256×256 DEPFET pixel sensor, four Veritas-2 readout ASICs and four Switcher-A devices.

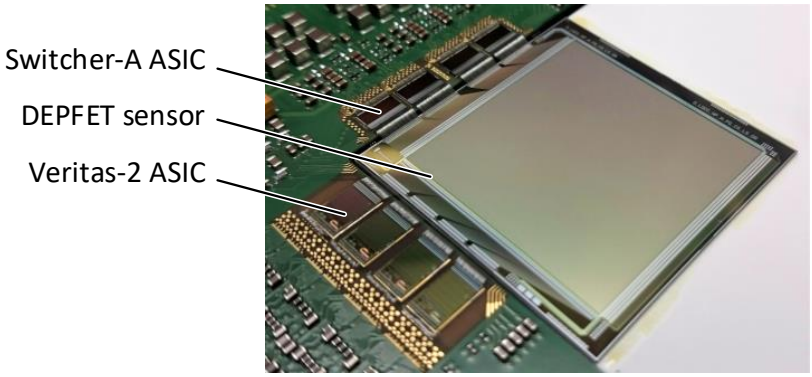


Figure 2.10.: WFI prototype detector with 256×256 pixel sensor, four readout ASICs Veritas-2 and four control ASICs Switcher-A.

All pixels of an active row are readout in parallel by the dedicated Veritas-2 devices. The Veritas-2 ASIC multiplexes 64 pixel signals to one high-speed analog output, which is connected to a dedicated DE, where the analog differential output signals are digitized. The scientific data streams are combined detector-wise in an FPGA based Frame Processor (FP) which performs high-speed data pre-processing in real-time and data reduction. Furthermore, the DE includes a sequencer module to control the CFE and AFE. A Power Conditioner Module (PCM) inside the DE is realized to bias the sensor and FEE. More information about the DE and its subunits can be found in section 5.2.
The data of all DEs is merged in the ICPU, which performs further data processing and compression and serves as interface to the SC.

To achieve the science requirements, the detectors have to be readout with high frames rates. The exposure time for full frame readout of the LD is required to be $5\,\mathrm{ms}$, which corresponds to 200 frames per second (fps). The FD has a minimal exposure time of $80\,\mu\mathrm{s}$ and therefore a frame rate of 12500 fps in full frame readout. Moreover it shall be possible to readout the sensors in a so-called window mode. In this operational mode, only a fraction of the detector is readout, which results in higher frame rates. this shall be possible with a maximum pixel clock of $25.6\,\mathrm{MHz}$.

Table 2.1 summarizes the WFI detector and instrument characteristics and requirements [70], [89].

Table 2.1.: WFI detector characteristics and requirements.

Parameter	**Requirement**
Energy range	$0.2\,\mathrm{keV}$ to $15\,\mathrm{keV}$
Pixel size	$130\,\mu\mathrm{m}$ x $130\,\mu\mathrm{m}$
Operating Mode	rolling shutter mode
Large detector array LDA	1024 x 1024 pixel (divided in 4 quadrants)
Fast detector FD	64 x 64 pixel
Spectral resolution	FWHM $\leq 80\,\mathrm{eV}$ @ $1\,\mathrm{keV}$
(end of life)	FWHM $\leq 170\,\mathrm{eV}$ @ $7\,\mathrm{keV}$
Count Rate Capability	1 Crab (corresponds to approx. $1 \cdot 10^5$ photons/s)
	<1% pile-up, >80% throughput
Time Resolution (full frame readout)	
Fast detector	$80\,\mu\mathrm{s}$
Large detector	$\leq 5\,\mathrm{ms}$

The WFI detector characteristics and specifications as listed in table 2.1, are basis to define the requirements of the PRE instrument, detailed in section 6.1.

3. Evaluation Methods of the Wide Field Imager Signal Processing

The following chapter describes the importance and necessity of an evaluation and verification of instruments for space applications, in particular the signal processing chain of the WFI. For this purpose, various evaluation and verification methods are presented and examined with respect to their applicability to the WFI signal processing chain, as explained in section 3.1. Previous experiences from already implemented and applied methods in space projects are outlined. Finally, in section 3.2, a new end-to-end verification and evaluation method is suggested.

3.1. Scientific Approaches on Evaluation and Verification Methods

Test, evaluation and verification of a system is very important in every stage of development. The WFI project schedule follows a classical model philosophy for space observatories. Currently, the WFI is in the development activity phase. Following this phase, an engineering model, a structural and thermal model and an electrical functions model will be developed. Testing and reviewing these models lead to design of the qualification model. Finally, the flight model will be designed, tested, calibrated and integrated.
Instrument evaluation and test starts at the early phase of the mission when defining verification processes in terms of the model philosophy and test sequence and ends at the last testing phase prior to launch [28]. In the early stage of development, the system design can be defined and improved, while at a later stage the characteristics of the instrument can be studied and optimized. It is possible to avoid mistakes and explain effects occurring in every step of operation.
The overall objectives of the verification process is to demonstrate, through a dedicated process, the qualification of design and performance. It needs to be confirmed that the mission requirements are fulfilled at the specific levels of the project, as well as for the overall system [26].

Bringing and operating systems in space entails large costs, the risk for a potential failure has to be reduced to the minimum. Experience has shown, that incomplete or improper on ground testing approaches significantly increase project risks leading to late discovery of design or workmanship problems or in-orbit failures.
The latest example of a space system failure is the mission Astro-H, renamed to Hitomi, a Japanese X-ray observatory [103]. Some weeks after its start in 2016, multiple incidents with the attitude control system leaded to an uncontrolled spin rate and breakup of structurally weak elements. This resulted in the loss of the satellite in the orbit during its commissioning phase.

In order to avoid system failures, it is important to ensure that an appropriate test and verification process is carried out. In the following, various approaches of evaluation and verification are examined. The advantages and disadvantages of the individual options are described, as well as the suitability for verification of the WFI signal processing chain. The results are summarized in table 3.1.

One method for verification is to model the system in a simulation environment, based on mathematical models, that describe the behavior of the subsystems and components. These simulations generate an output of detected events which can be processed with the mission specific analysis software. In case of WFI, the SIXTE simulation software is used. SIXTE is a software package for X-Ray telescope observation simulations developed at Erlangen Centre for Astroparticle Physics (ECAP) [121], [95].

The most obvious way to test, evaluate and verify the WFI signal processing chain is to build up the whole system and perform measurements in an experimental setup. Output of these measurements are event lists with detected photons, which are further processed for performance evaluation of the system.

Controllable Observation Scenario
In simulation environment, the input can be adapted to the purpose of the corresponding simulation. This can be for instance, real measurement data, such as astronomical observations taken from X-ray source catalogs [29], [117]. Moreover, an arbitrary, simulated input data can be used for specific test cases. Thus, the observation scenario in simulation environment is completely controllable by the user.
Performing measurements in the laboratory, the sensors must be irradiated with X-ray sources like Fe-55 or complex X-ray tubes to generate significant input signals. Unfortunately, this is quite inflexible because no reproducible input data can be generated as X-ray radiation follows the Poissonian distribution. An approach to overcome this, would be to illuminate the sensors with a laser of a specific wavelength. This has the disadvantage of a more complex test setup. It is very time consuming to generate all

required combinations of fast precise timing, high spatial resolution and all possible energy levels.

Transfer of Science Requirements to Technical Specifications
Simulations support the transfer of science requirements of the mission to technical specifications of the instrument. By parametrization of the simulation, different instrument characteristics can be modeled, and the effect on the scientific result can be studied.
By means of measurements, this transfer is only possible to a limited extend. For this purpose, the system to be tested would have to be adapted or individual components replaced in order to display different instrument characteristics.

Performance Verification
Simulations are based on models representing the instrument. Depending on the purpose of the simulation, different components of the instrument are modeled based on key characteristics and behavior of the system. The results of the simulation is strongly dependent on the system characteristics defined in the models. If these characteristics and the behavior of the system is unknown, a performance verification can be done with limitations. With measurements on the real system, system characteristics can be determined more precisely. In case of unexpected behavior of the system, simulations no longer produce correct results. Simulations are supported by measurements on the real system. Instrument characteristics can be determined more precisely, which can be implemented in the simulation models.
Verifying the signal processing chain by measurements on a real system, has the big advantage that the measurement setup is very similar to the later used system. The performance of the instrument can be evaluated and verified correctly and unexpected behavior and failures can be detected.

Flexible Test Environment
Simulations are constantly expandable, adaptable and functions interchangeable. The implemented models can be changed due to later defined specifications or new results on instrument characteristics and behavior. Their input, and thus the simulated observation scenario can be controlled. In this way, simulations provide a very flexible test environment.
The flexibility of testing in measurement environment is limited. Reconfiguration of hardware and firmware of the instrument can be demanding and time consuming. Therefore the risk of instrument damage increases by changes in the system. Moreover, the operation of detectors and X-ray sources is demanding and often the devices are not available at the beginning of the development phase.

Table 3.1.: Comparison of methods for system test and evaluation, either performed by simulation or measurements on the real hardware.

Criteria	Simulation	Measurement
Controllable observation scenario	+	○
Transfer of science requirements to technical specifications	+	−
Performance Verification	−	+
Flexible test environment	+	−

Test and verification of the signal processing chain of the camera of eRosita was carried out by operation of real sensors [69]. However, this process has led to the above-mentioned disadvantages. A corresponding raw data interface in the electronics has made it possible to directly access the digitized, non-processed sensor data. Thus the processing chain of the camera could be bypassed and the raw data could be directly stored. With a mission-specific analysis software of the ground support equipment, the data was analyzed and compared with online pre-processed data generated with the same setup. With this method no reproducible test cases can be generated and no influence on the input data can be taken. Limitations of the system and special test cases are only very difficult to cover.

3.2. Evaluation by Modeling and Emulation of the Detector System

A logical approach for testing and evaluating the signal processing chain is to design a method, which combines the advantages of the evaluation methods compared in table 3.1. This would be to test the signal processing chain not with randomly distributed X-rays, but to define the input by known values, to achieve a controllable observation scenario.
Possible options to generate adequate input data for the signal processing chain is to make use of instruments like arbitrary waveform generators, an emulator instrument proposed by Abba et al. [3] or an CCD emulator designed by Lu et al. [63]. The output of these instruments is based on basic models of a detector system. However, these instruments are not suitable for generating the data from the WFI detectors, since they do not refer to the complex requirements of the mission.

To overcome the issues mentioned above, a new end-to-end evaluation method is suggested for functional and performance test, evaluation and verification of the WFI signal processing chain. This method will be explained in section 3.2.1.

3.2.1. End-to-End Evaluation Method

For test, evaluation and verification of the signal processing chain of the WFI detector system, a new end-to-end method is developed. Figure 3.1 shows the end-to-end evaluation method schematically. This method uses a specifically designed emulator instrument to substitute the crucial parts of the signal processing chain, namely the sensor with FEE. All further components of the WFI are in function and behavior identical to the ones later used. A comparison in the feedback path from output to input closes the chain from end-to-end. With a variation of the input data and the emulator parameters different output data can be obtained. Specific image processing algorithms allow a comparison of the digitized and processed output of the detector electronics with the well known input data. This leads to a complete real-time end-to-end evaluation of the WFI instrument.

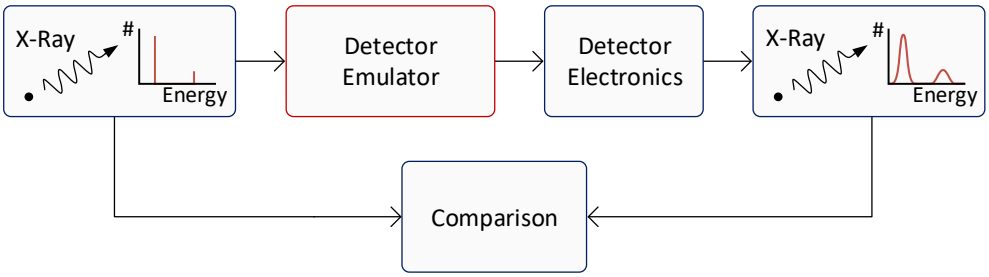


Figure 3.1.: With a parametrization of the emulator and a comparison of input and output data, the method provides a powerful tool to evaluate the WFI camera system from end-to-end.

The variation of the input data of the emulator with variable properties of the emulated hardware followed by the comparison of the input and output data is an iterative process to investigate influences of different parameters and to characterize the processing chain. Analysis of simulated input data and comparison with real measurements allow to study influences of certain effects in detail. This leads to a better understanding of the complete camera system. Obviously, testing with X-ray sources as input and the real detector system is necessary. Moreover, this method provides a further possibility to test, develop and optimize the WFI signal processing chain.

3.2.2. Programmable Real-Time Emulator Concept

To implement the end-to-end evaluation method, an instrument is developed which emulates behavior and characteristics of the WFI detectors. This specifically designed emulation instrument is called Programmable Real-Time Emulator (PRE). The main features of the PRE are listed below:

- Generation of analog output signals according to the detector system in real-time
- Controllable simulated X-ray input
- Programmable and variable detector characteristics

Complementary to the signal processing chain depicted in figure 2.9, the DEPFET detector is substituted by the PRE as shown in figure 3.2 [78].

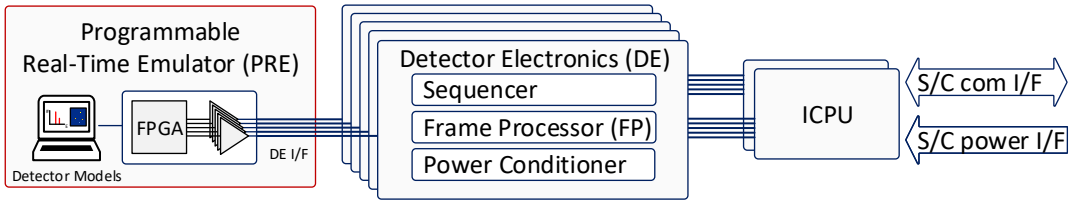


Figure 3.2.: End-to-end evaluation method: The DEPFET detector with front-end electronics is replaced by a PRE.

The end-to-end method with the PRE instrument combines the advantages of the evaluation methods presented in section 3.1 and summarized in table 3.1. Connecting the PRE with the DE allows to fully control the simulated WFI observation scenario. With this approach, the influence of the signal processing chain on the desired astrophysical results can be investigated. Simulated photon fluxes as input of the system enable adaptation of the signal processing algorithms in a way that the measurement results of expected observation scenarios can be determined in advance. Thus, the WFI science requirements can be transferred to technical specifications of the instrument.
In addition to the modeling and real-time generation of scientific astrophysical data, input data can be generated with all combinations of precise timing, high spatial resolution at all required energy levels. This means that not only extreme and complex scenarios can be described, but also uncommon data for test purposes which cannot be produced in a laboratory setup using X-ray sources. This allows optimization and performance verification of the DE and FP, especially with regard to the analysis of data reduction algorithms. This method allows absolutely comparable and reproducible

measurements. Various hardware implementations and different algorithms of the signal processing chain can be tested with exactly the same input data. With this method it is possible to test and verify the processing chain without the operation of valuable WFI sensors. By using the PRE in combination with the DE, there is no need of handling with X-ray sources and handling elaborate test setups, for instance operation in a vacuum chamber and cooling of the detector.

4. X-Ray Detection with Semiconductor Sensors

Within this chapter an introduction of the theory behind X-ray imaging, in particular with semiconductors is given. The interaction of radiation and matter is described in section 4.1. The noise contributions of an imaging device are outlined in section 4.2. Three different sensors for X-ray detection and their working principle are introduced in section 4.3. Especially features and consequences of the DEPFET technology are discussed. The main advantages of this sensor type compared against other technologies for X-ray detection are outlined.

4.1. Interaction of Radiation and Matter

Radiation can be detected due to interaction with the sensor material. In the sensor medium the energy of the radiation is converted into a measurable signal which can be read out by an appropriate electronic. When radiation penetrates the sensor material, a series of interactions occur with the shell electrons and the atomic nuclei.

4.1.1. Particle Radiation

The interaction process between matter and particles changes whether the particle is charged or not. Uncharged particles like neutrons interact in collision with the atomic nuclei and may bounce off (an elastic collision) or stick (an inelastic collision) producing a new nucleus with the same charge.

Charged particles like electrons, protons, muons or pions lose their energy mainly through inelastic Coulomb collisions with electrons from the sensor material. They deposit their energy along their path through the sensor material until the particle is stopped or leaves the material.
The mean rate of energy loss dE, also called stopping power, of a particle due to ionization in a material with a path length dx is given according to the Bethe-Bloch

equation [15] to

$$\left\langle -\frac{dE}{dx} \right\rangle = Kz^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} \ln \left(\frac{2m_e c^2 \beta^2 \gamma^2 T_{\max}}{I^2} \right) - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right] \tag{4.1}$$

with

- $K = 4\pi N_A r_e^2 m_e c^2$,
- N_A being the Avogadro constant,
- r_e being the classical electron radius,
- m_e being the electron rest mass,
- z being the charge of the incident particle in units of e,
- e being the elementary charge,
- Z being the proton number of the absorber material, A being its mass number,
- $\beta = \frac{v}{c}$, v being the particle speed and c being the speed of light,
- $\gamma = \frac{1}{\sqrt{1-\beta^2}}$, being the Lorentz factor,
- T_{max} being the maximum kinetic energy which can be passed to a free electron in a single collision,
- I being the mean excitation energy of the material,
- $\delta(\beta\gamma)$ being a density effect correction factor.

Figure 4.1 shows the energy loss per path length for muons, pions and protons in different materials. The graph holds a minimum. For energies below that minimum, the energy loss is inversely proportional to the energy. That means, the particle loses more energy when it gets slower. At the end of the particles track a peak can be observed, the so-called Bragg peak. Particles with mean energy loss rates around the minimum, are called Minimal Ionizing Particles (MIPs). Particles above the minimum lose its energy along its track with an approximately constant rate.

High-energy particles can induce defects in semiconductor devices. Two fundamental effects can happen: lattice displacement and ionization effects which can cause lasting defects in the semiconductor. Therefore electronic components and sensors need to be resistant to damage or malfunctions caused by ionizing radiation.

4.1.2. Electromagnetic Radiation

X-rays are attenuated during transition through matter. The Lambert-Beer law applies for the intensity after passing through the layer thickness x

$$I(x) = I_0 \cdot e^{-\mu x}. \tag{4.2}$$

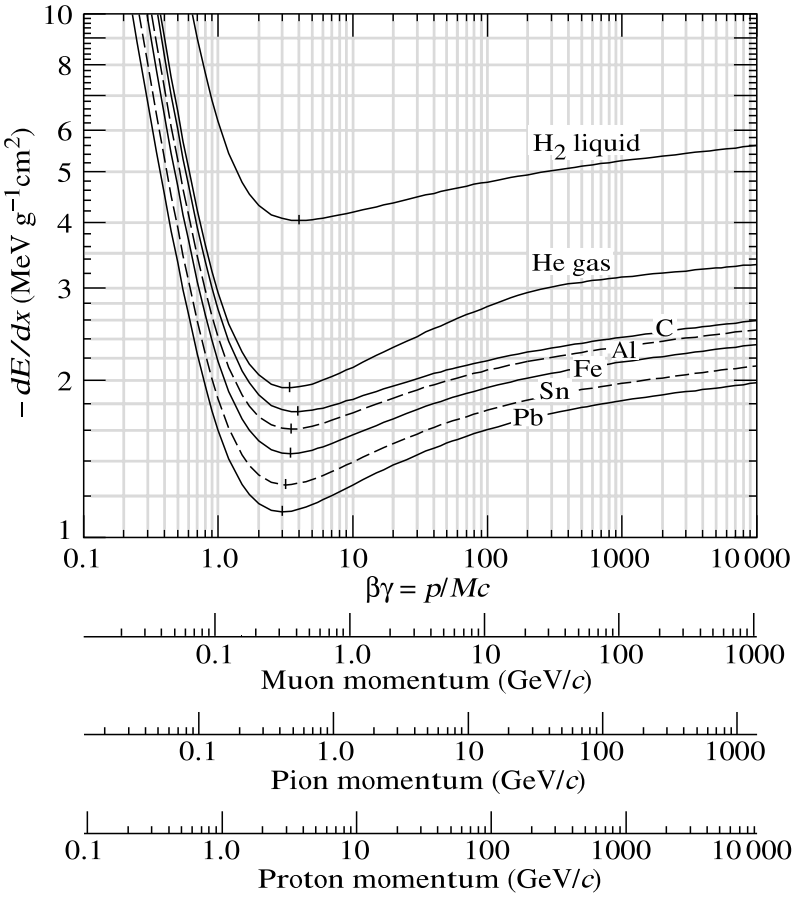


Figure 4.1.: Mean energy loss of a charged particle in a range of materials [15].

$I(x)$ is the remaining intensity after the transition of an initial intensity I_0, μ is the attenuation coefficient dependent on the energy of the radiation [38]. Depending on the radiation energy, three interacting processes occur:

- Photoelectric effect
- Compton effect
- Pair production

These three effects are superimposed in the interaction material, whereby one process dominates in individual energy ranges. The cross section gives the probability of a process to occur. Hence the total probability σ_{total} is given to

$$\sigma_{total} = \sigma_{photo} + \sigma_{compton} + \sigma_{pair}. \tag{4.3}$$

The relation between the attenuation coefficient μ and the cross section σ can be described with the equation

$$\mu = n \cdot \sigma \tag{4.4}$$

where n is the density of the atoms for the respective material. Figure 4.4a shows the dependance of attenuation factor and energy [60].

Photoelectric Effect

The photoelectric effect describes the interaction between a photon and the electrons of an atom of the absorber material. The incident photon transfers all its energy to one (or several) electron, which is rejected from the atom. This electron is called photoelectron. The effect is schematically depicted in figure 4.2. The photoelectron carries now the energy of the photon minus the binding energy E_b as kinetic energy E_{kin}

$$E_{kin} = h\nu - E_b. \tag{4.5}$$

Hence the minimum photon energy must be equal or greater than the binding energy of the absorber material, which is in case of silicon $1.12\,\mathrm{eV}$. The photoelectron releases its energy by excitation or ionization to the atoms of its environment (secondary radiation).

The photoelectric effect preferably takes place, due to momentum conservation, on electrons of the shells near the nuclei (predominantly the K-shell). In addition to the emission of a photoelectron, the vacancy in the atomic shell will be filled by electrons from higher shells causing an emission of a fluorescence photon or an Auger electron which can further interact with the absorber medium.

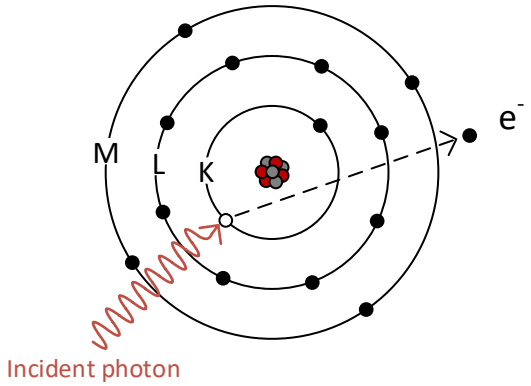


Figure 4.2.: Principle of the photoelectric effect.

Usually the fluorescence photon is reabsorbed, causing a second photoelectron. The photoelectrons and Auger electrons lose their kinetic energy through Coulomb colli-

sions during their movement in the material. In each Coulomb collision a part of the kinetic energy is used to create an electron-hole pair and another part is transferred to a phonon. Finally, the entire energy of the absorbed photon is used to create electron-hole pairs and phonons.

Compton Effect

Compton scattering, discovered by Arthur Holly Compton, describes the process of elastic and incoherent scattering of photons and free or only weakly-bound electrons. The photon transfers only a part of its energy to an electron, which is located in the outer shell of the atom, and is thus separated from the atom (Compton electron). Energy and momentum are transferred to the charged particle while the photon moves with a reduced energy and changed momentum. The electron takes the kinetic energy as the difference between the energy of the incident photon and the energy of the scattered photon. The change in wavelength of the scattered photon is given by

$$\lambda' - \lambda = \frac{h}{m_e c}(1 - cos\Theta) \tag{4.6}$$

where λ' is the wavelength of incident x-ray photon, λ the wavelength of scattered photon, h is the Planck's constant , m_e the mass of an electron at rest, c the speed of light and Θ the scattering angle of the scattered photon.

The scattered photon can produce further effects until it escapes of the medium or its energy has become so low that it is completely consumed by a photoeffect. The Compton electron can lead to ionization and excitations in the interaction material [20].

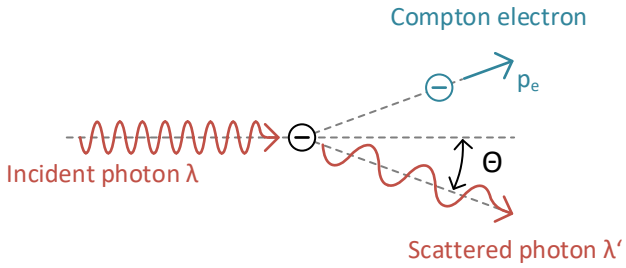
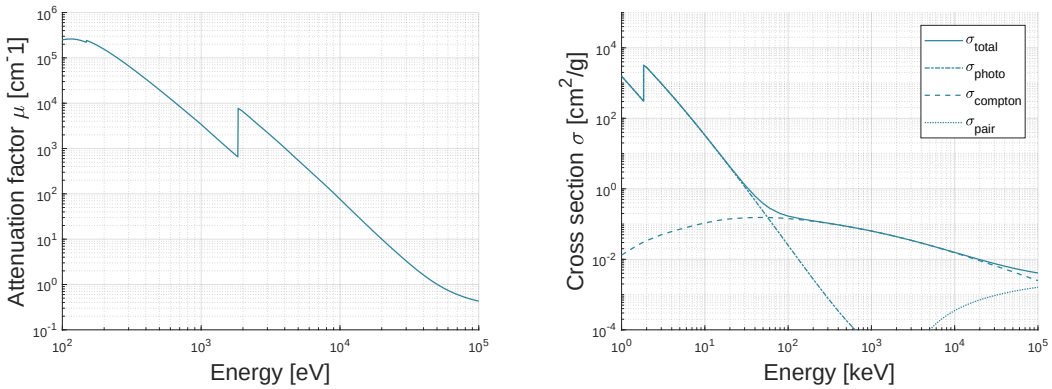


Figure 4.3.: Principle of the Compton Effect. A photon is scattered by a charged particle. Energy and momentum are transferred to the charged particle. The scattered photon continues moving with a reduced energy and a change of momentum.

Pair Production

In the case of higher quantum energy, the effect of pair production is predominant in the interaction material. The photon is converted in the electric field of an atomic nucleus into an electron and a positron.

The photon must have at least an energy of $1.022\,\mathrm{MeV}$ in order to be able to produce the two particles, since the rest mass of the electron and the positron corresponds to an equivalent energy of approximately $0.511\,\mathrm{MeV}$ each [76]. Excessive energy is stored as kinetic energy in an electron and a positron [60].



(a) (b)

Figure 4.4.: Attenuation factor μ and cross section σ for silicon material. (a) Dependence of the attenuation coefficient μ on energy in the range of $100\,\mathrm{eV}$ to $20\,\mathrm{keV}$ for silicon as absorber material. Data from [19]. (b) Cross section as probability function for a interaction between a photon and silicon material. In the relevant energy range up to $15\,\mathrm{keV}$, the photoelectric effect is the dominant effect. Data from [45].

In figure 4.4b the cross sections of the energy loss mechanisms of the photoelectric effect, the Compton effect and the pair production process is shown. The K-edge of silicon can be seen as a step in the graph at an energy of $1.84\,\mathrm{keV}$. For energies lower than $50\,\mathrm{keV}$ the photoelectric effect is the dominant process. Above this energy range the Compton scattering has to be considered. For energy ranges starting at $10\,\mathrm{MeV}$ the pair production process plays a major role.
For this work the lower energy range up to $15\,\mathrm{keV}$ is of interest, thus only the photoelectric effect is considered.

4.1.3. Electron-Hole Pair Creation Energy and Fano Statistics

The average number of generated electron-hole pairs N created by a photon with energy E_{ph} is

$$N = \frac{E_{ph}}{\omega} \tag{4.7}$$

with ω being the electron-hole pair creation energy. The value of the electron-hole pair creation energy depends on the temperature. This correlation was measured for $5.9\,\mathrm{keV}$ X-rays in the range of $80\,\mathrm{K}$ to $270\,\mathrm{K}$ by [62]. A value of $(3.73 \pm 0.09)\,\mathrm{eV}$ was found and can be estimated linear in the stated temperature range. A linear fit through the provided data in [62] gives the temperature dependence of the pair-creation energy ω

$$\omega(T) = 3.8\,\mathrm{eV} - 4.5 \cdot 10^{-4}\,\mathrm{eV/K} \cdot T(\mathrm{K}). \tag{4.8}$$

For the operating temperature of the Athena sensors of $190\,\mathrm{K}$, an electron-hole pair creation energy of $\omega = 3.70\,\mathrm{eV}$ can be assumed.

If all the energy of an interacting photon is spent in the generation of electron-hole pairs, there would be no variation in the number of electron-hole pairs produced. The variance in multiple electron-hole charge generation is described by

$$\sigma_{FN} = \sqrt{F_a \cdot E_{ph} \cdot \omega} \tag{4.9}$$

where F_a is referred to as the Fano factor, which is defined by the variance in the total number of generated electrons divided by the average number of electrons generated per interacting photon [48]. The statistical uncertainty in the number of generated electron-hole pairs is the lower limit of the energy resolution of a semiconductor detector and is referred to as Fano limit. The Fano factor links the measured Full Width at Half Maximum (FWHM) of a histogram and the average energy expected to produce an electron-hole pair by the relation

$$FWHM(eV) = 2\sqrt{2\ln 2} \cdot \sigma_{FN} \approx 2.355 \cdot \sqrt{F_a \cdot E_{ph} \cdot \omega}. \tag{4.10}$$

Empirical values for the Fano factor of silicon can be found in literature in the range of 0.114 to 0.122. In this thesis, a value of 0.118 given in [62] is used. Thus, the theoretical limiting energy resolution for a silicon sensor stimulated with $5.9\,\mathrm{keV}$ X-ray photons at a temperature of $190\,\mathrm{K}$ can be calculated to $FWHM(\mathrm{eV}) = 120\,\mathrm{eV}$.

4.2. Noise of the Detector System

In a detector system, the energy of photons is converted into a voltage or current signal. Voltages and currents in electronic circuits underlie statistical random fluctuations as they are not constant in time. These fluctuations define the smallest electronic signal which a detector system can resolve. Fluctuations dominate the overall resolution of an electronic system, so designing a system with low noise is crucial.
The spectral distribution of noise is described as spectral power density dP_n/df, which is the frequency-related noise power of a signal per unit of bandwidth. In this thesis, the noise contributions are given as voltage and current spectral densities $dv_n/\sqrt{df}$ and $di_n/\sqrt{df}$. The total noise is obtained by integration of the spectral densities over the relevant bandwidth of the system [99].

The three dominant noise contributions are thermal noise, $1/f$ noise and shot noise. In this section, the physical noise sources and their contribution to the overall noise of a DEPFET based camera system are explained.

4.2.1. Thermal Noise

Thermal noise was first investigated by H. Nyquist [75] and J. B. Johnson [50] in 1928 and is also cited in literature as Johnson-Nyquist noise. Thermal noise on resistors is referred as resistor noise, thermal noise on capacitors is called kTC-noise or reset noise.

Thermal noise is a type of electronic noise, generated by random movements of thermally generated free charge carriers inside an electrical conductor due to their thermal or kinetic energy. This results in temporal fluctuations of charge density inside the resistor causing a voltage drop. These statistical fluctuations have a mean value of zero, but lead to a noise in the resistor. The noise is present even without applying an external voltage.

The spectral noise density versus frequency is given by

$$\frac{\mathrm{d}P_n}{\mathrm{d}f} = 4kT \tag{4.11}$$

with k being the Boltzmann constant and T the absolute temperature [107]. According to the power in a resistor $P = u^2/R = i^2R$, the spectral voltage density is

$$\frac{\mathrm{d}u_n^2}{\mathrm{d}f} = 4kTR \tag{4.12}$$

and the spectral current density

$$\frac{\mathrm{d}i_n^2}{\mathrm{d}f} = \frac{4kT}{R} \tag{4.13}$$

for a resistor R in dependance of temperature T.

In case of a transistor, thermal noise is caused by the resistance of the conductive channel. The spectral noise density can be derived from replacing the conductive channel by infinitesimal small resistors in series. Therefore, the interaction of the channel with the gate of the transistor needs to be taken into account [65]. This results in a spectral noise density in the gate of the transistor with a correction factor of $2/3$

$$\frac{\mathrm{d}u_n^2}{\mathrm{d}f} = \frac{2}{3} \cdot 4kT\frac{1}{g_m} \tag{4.14}$$

with g_m representing the small-signal transconductance of the transistor. The current spectral density in the transistor can be deduced to

$$\frac{\mathrm{d}i_n^2}{\mathrm{d}f} = \frac{2}{3} \cdot 4kTg_m \tag{4.15}$$

Thermal noise is approximately white, this means that the power spectral density is nearly constant throughout the frequency spectrum [72].

4.2.2. Low-Frequency Noise

Low-frequency noise also referred to as $1/f$ noise or pink noise has a power spectrum which is inversely proportional to the frequency of the signal

$$\frac{\mathrm{d}u_n^2}{\mathrm{d}f} = \frac{A_n}{f^\alpha} \qquad \alpha = 0.5 \ldots 1.5 \tag{4.16}$$

with α and A_n being factors, which need to be determined experimentally. The physical sources of the noise are not unique, they are caused by widely varying mechanisms among different types of electronic elements. Also, for the same type of component the strength of the noise is depending on the technological production process. Furthermore, the $1/f$ dependence is only a rough approximation [65].

In the case of transistors in DEPFET technology, $1/f$ noise is caused by traps next to the conductive channel. These traps absorb or emit free charge carriers. Mirror charges are generated in the channel and the channel conductivity is modified. The amplitude of modulation varies with the location of the traps. Further, the frequency of

absorbing and emitting free charge carriers depends on the temperature and the depth of the trap. The spectral voltage density of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) can be found in literature [65] as

$$\frac{\mathrm{d}u_n^2}{\mathrm{d}f} = \frac{K_F}{WLC_{ox}^2}\frac{1}{f}, \tag{4.17}$$

with K_F representing a parameter characteristic for the specific device production process. W and L are the gate width and length of the transistor while C_{ox} is the oxide capacitance.

In electronic devices, $1/f$ noise is a low-frequency noise, as the higher frequencies are imposed by white noise from other sources [115].

4.2.3. Shot Noise and Dark Current

Shot noise is a type of electronic noise which can be modeled by a Poisson process. In electronic devices shot noise is caused by the discrete nature of electric charge. Shot noise also occurs in photon counting applications in optical devices, where it is associated with the particle nature of light [106].

In electronics, shot noise stands for the random statistical fluctuation in the number of charge carriers n revealing a charge $Q = n \cdot e$. A constant current $\bar{i}$ entails a charge ΔQ traversing a gap in a short time interval Δt. This results in

$$\bar{i} = \frac{\Delta Q}{\Delta t} = \frac{\overline{n} \cdot e}{\Delta t}. \tag{4.18}$$

The probability $P_n(n)$ that n electrons will cross the plane in a time interval Δt is then given by the Poisson distribution

$$P_n(n) = \frac{\overline{n}^n e^{-\overline{n}}}{n!} \tag{4.19}$$

where $\overline{n}$ is the average number of charge carriers per unit time interval. For large $\overline{n}$, the function $P_n(n)$ can be approximated by a Gaussian distribution [86]. The maximum of this function is at $n = \overline{n}$, with an root mean square (rms) width δn given by

$$\delta n = \sqrt{\overline{n}}. \tag{4.20}$$

With statistical fluctuation $\delta n = \sqrt{\overline{n}}$, the mean-square variation of the current over a small time interval is

$$\delta i_n^2 = \frac{e^2(\delta n)^2}{\Delta t^2} = \frac{e^2\overline{n}}{\Delta t^2} = \frac{e^2}{\Delta t^2} \cdot \frac{\bar{i}\Delta t}{e} = \frac{\bar{i}e}{\Delta t}. \tag{4.21}$$

According to the Nyquist theorem the bandwidth Δf is equivalent to the time slice Δt at $\Delta f = {}^1/_{2\Delta t}$. From this the frequency spectrum of the noise current can be derived

$$\frac{\mathrm{d}i_n^2}{\mathrm{d}f} = 2\bar{i}e. \tag{4.22}$$

Equation 4.22 shows that the shot noise is independent of temperature and bandwidth and thus constant over the frequency range, the frequency spectrum is white. Unlike thermal noise, which is also present when no external voltage is applied, shot noise requires a current flow from an external power source [65].

Electronic shot noise in imaging devices can be associated with the presence of dark current or leakage current. This is a signal produced, by thermal generated charge carriers instead of charge carriers generated by radiation. That means, it is present, even if there is no radiation illumination. In this case, the shot noise contribution of an imaging sensor is given by

$$\frac{\mathrm{d}i_n^2}{\mathrm{d}f} = 2\overline{i_{dark}}e \tag{4.23}$$

with $\overline{i_{dark}}$ being the dark current. Dark current correlates with exposure time and temperature. The number of thermal generated electrons, responsible for dark current flow, can be described by

$$\overline{n_{therm}} = \frac{\overline{i_{dark}}\Delta t}{e} \propto exp\left(-\frac{E_g}{kT}\right) \tag{4.24}$$

where E_g is the band gap of silicon, T is the absolute temperature and k the Boltzmann constant. With this equation, the difference in temperature for halving the charge carriers due to dark noise can be calculated. This leads to equation 4.24 for two different temperatures T and $T + \Delta T$

$$\frac{n_{T+\Delta T}}{n_T} = exp\left(-\frac{E_g}{k\,(T+\Delta T)} + \frac{E_g}{kT}\right) = \frac{1}{2}. \tag{4.25}$$

Assuming the band gap of silicon at a temperature $T = 300\,\mathrm{K}$ around $1.1\,\mathrm{eV}$ and the Boltzmann constant $k = 8.62 \cdot 10^{-5}\mathrm{eV/K}$, a temperature difference of approximately $\Delta T = 4.8\,\mathrm{K}$ is obtained. That means, reducing the temperature from $300\,\mathrm{K}$ to $295\,\mathrm{K}$ reduces the charge carriers by a factor of two. The dependance of the dark current on temperature can be specified by the following empirical relationship [48]

$$I_D = 2.5 \cdot 10^{15} \cdot A \cdot I_{D0} \cdot T^{1.5} \cdot e^{(-\frac{E_g}{2kT})} \tag{4.26}$$

with I_D the dark current rate in $\mathrm{e/(pixel\,s)}$, the pixel area A in cm^2 and the measured dark current I_{D0} at $T = 300\,\mathrm{K}$ in $\mathrm{nA/cm}^2$. The band gap E_g of silicon is also

temperature-dependent and can be empirically expressed by following equation [30]

$$E_g = 1.117 - \frac{(4.73 \cdot 10^{-4} \cdot T^2)}{(636 + T)}. \tag{4.27}$$

The dependance of the dark current generation rate upon temperature is shown in figure 4.5.

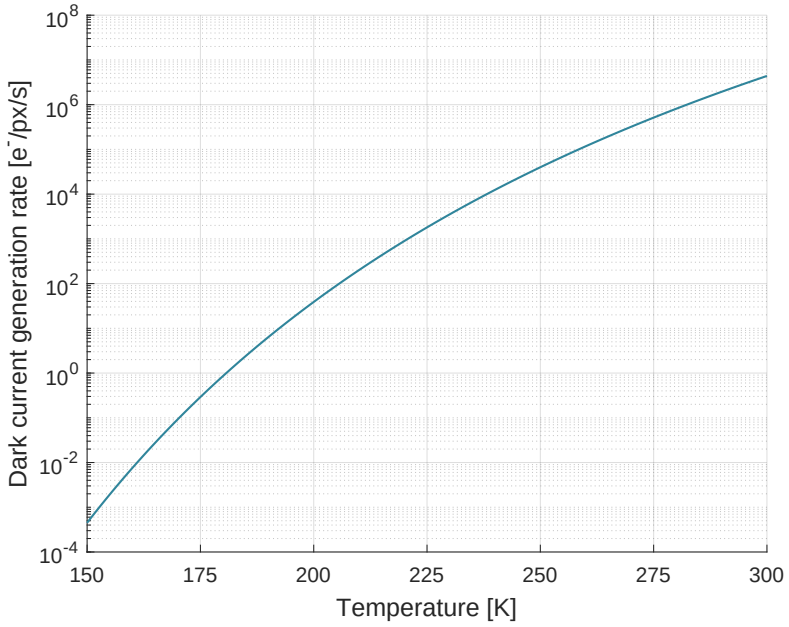


Figure 4.5.: Dark current generation rate in electrons per pixel and seconds versus temperature.

4.2.4. Equivalent Noise Charge

The processing chain of a typical spectroscopic or imaging system is depicted in figure 4.6. The sensor is modeled as a current source, with the signal current approximated here as a dirac-shaped pulse $Q \cdot \delta t$ and a total capacitance C_{tot}. The noise contributions of parallel white noise, which is shot noise, is modeled as parallel current source, while thermal and 1/f noise are modeled as voltage sources in series. The preamplifier and time-variant filter stage are represented by an amplification A_i and frequency transfer function $F(j\omega)$ or respectively by a weighting function $F(t)$ in the time domain.

The total noise can be calculated by integrating the noise spectral densities for shot noise, thermal noise and $1/f$ noise over the full system bandwidth

$$u_n^2 = \int_0^\infty ((\frac{\mathrm{d}u_{th}^2}{\mathrm{d}f} + \frac{\mathrm{d}u_{1/f}^2}{\mathrm{d}f} + \frac{\mathrm{d}u_{shot}^2}{\mathrm{d}f}) \cdot A^2(f))\,\mathrm{d}f. \tag{4.28}$$

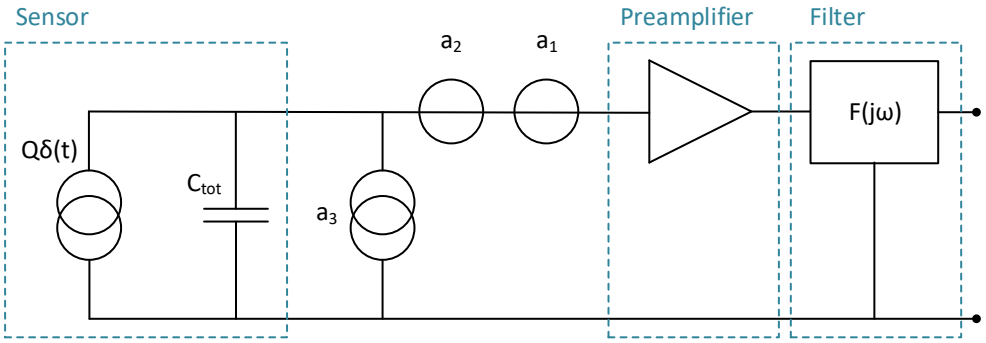


Figure 4.6.: Schematic of a typical processing chain of an imaging or spectroscopic sensor. The sensor is modeled as current source in parallel to a capacitance. The noise sources are represented as current and voltage source. The readout chain consists of a preamplifier and a filter.

The total electronic noise contribution of a detector is usually expressed in equivalent noise charge (ENC). The ENC represents the number of electrons that would create the same signal amplitude in a noiseless device as the noise source. Thus, the ENC is the quotient of the noise signal u_n and the maximum signal $max(u_{sig})$ created by one single electron

$$ENC = \frac{u_n}{max(u_{sig}(e))}. \tag{4.29}$$

A detailed calculation of the ENC can be found in literature [65], [99], [55]. The overall system noise in terms of ENC can be described as [35]

$$\begin{aligned} ENC^2 &= ENC_{th}^2 + ENC_{1/f}^2 + ENC_{shot}^2 \\ &= \frac{a_1}{\tau}\frac{1}{C_{tot}^2}A_1 + 2\pi a_2 C_{tot}^2 A_2 + a_3 \tau A_3. \end{aligned} \tag{4.30}$$

The three terms stated in 4.30 describe the main noise contributions, thermal noise, $1/f$ noise and shot noise. The parameters A_1, A_2 and A_3 are defined by the shaping of the analog weighting function of the readout electronics while τ is the shaping time of the readout filter. Numbers for different filter parameters can be found in literature [66]. The capacitance C_{tot} is the equivalent input capacitance of the system. The noise

sources are stated as shown below.

$$a_1 = \frac{8}{3} kT g_m \qquad \text{thermal noise} \tag{4.31}$$

$$a_2 = \frac{K_F}{WLC_{ox}^2} g_m \qquad 1/f \text{ noise} \tag{4.32}$$

$$a_3 = 2 I_{dark} e \qquad \text{shot noise} \tag{4.33}$$

From equation 4.30 it is obvious that the contribution of the shot noise component of the ENC scales with the shaping time τ of the system. The thermal noise is proportional to $1/\tau$. An optimal processing time τ can be found according to these relationships. The minimal ENC value for a specific detector system is thus only limited by the $1/f$ noise which is independent of the processing time.

4.3. Sensor Technology

This chapter focuses on semiconductor sensors for use in X-ray astronomy for imaging and spectroscopic applications. Semiconductor sensors use the same detection principle as gas-filled ionization detectors but the medium is the semiconductor crystal. The main advantage is that the energy for producing an electron-hole pair is only about $3.7\,\mathrm{eV}$ in silicon while around $20\,\mathrm{eV}$ are required for gas ionization. This means, a higher energy resolution can be reached [92].

The most commonly used semiconductor materials for particle and radiation detection sensors are germanium and silicon, but also other compound materials such as gallium arsenide or cadmium telluride are used. Germanium is suitable for X-ray sensors to measure rather high energies while silicon sensors are limited to measurements in the energy range of some tens of keV due to the much longer photon absorption length. Silicon is the most common material in electronics industry, so it has the advantage of a mature fabrication technology.

This work concentrates on silicon as sensor material. Three major sensor types for use in X-ray astronomy will be presented in the next section: silicon drift detectors (SDDs), charge-coupled devices (CCDs) in particular the pn Charge-Coupled Device (pnCCD) and sensors comprising DEPFET technology. The working principle is based on sidewards depletion. The main advantages and applications of these devices are described in the next sections.

4.3.1. Sidewards Depletion

The principle of sidewards depletion was proposed by E. Gatti and P. Rehak in 1984 [36]. The scheme of sidewards depletion is shown in figure 4.7. The basic structure is a double-sided diode with diodes on both wafer surfaces and an additional small n+ bulk contact on the side. Biasing the diode contacts with a negative voltage and keeping the n+ contact on ground potential, results in an expansion of the depletion region. It grows simultaneously from both wafer surfaces until they reach each other. To deplete a diode, the reverse bias voltage V_{bias} can be expressed as

$$V_{bias} = \frac{qN_D}{2\epsilon\epsilon_0} d^2 \tag{4.34}$$

where N_D is the concentration of activated donors, d the depletion thickness, q the charge of one electron, and $\epsilon\epsilon_0$ the dielectric constants of silicon.

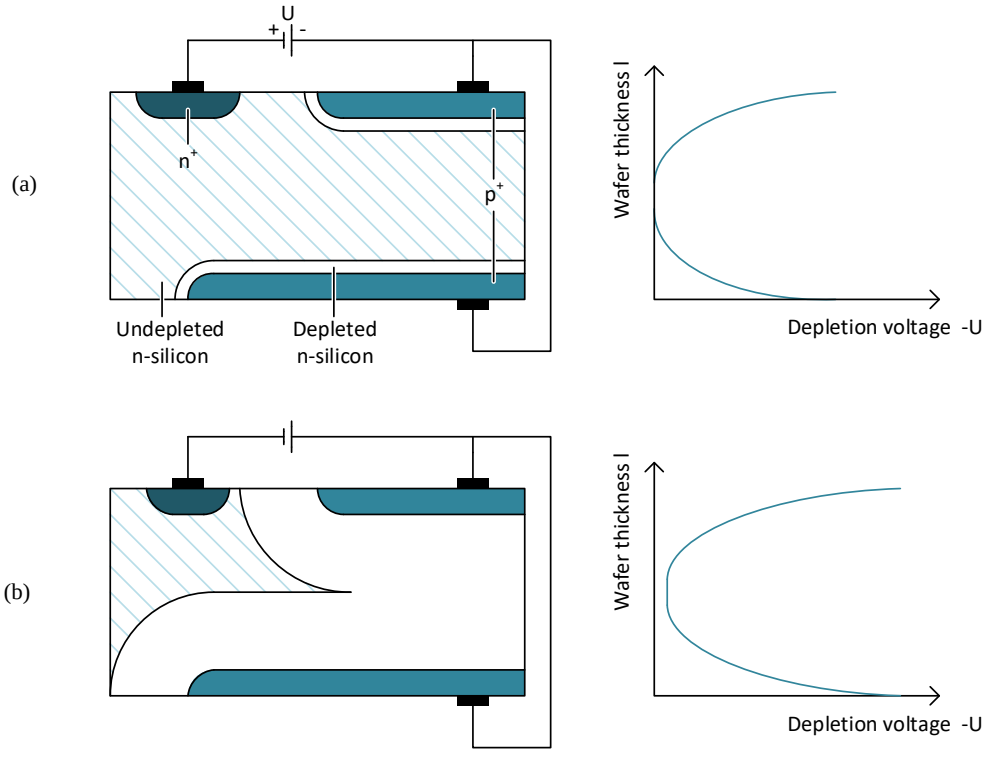


Figure 4.7.: Principle of sidewards depletion. (a) No reverse bias voltage is applied, only the intrinsic depletion zones have developed. Applying a negative voltage to the p^+ contacts forces electrons to the n^+ node and the depletion voltage grows. (b) Fully depleted device starting from the p^+ contacts on both wafer sides.

As it can be seen from equation 4.34 the bias voltage grows quadratic with the depleted depth. With the principle of sidewards depletion, the whole volume can be depleted by using a quarter of the bias voltage as necessary for a simple diode [113]. If front and backside are biased with the same voltage, the potential minimum for electrons will be located at $x = d/2$. Position and value of the potential minimum can be shifted by applying asymmetric bias voltages to front and backside. If electron-hole pairs are created by ionizing radiation, the electrons move to the potential minimum while the holes move towards the p-implant. Once the electron reached the potential minimum, they are transported by diffusion, which is a rather slow process. For use as a sensor, the depletion region has to be superimposed with a transport field which drives the electrons to the readout anode. The capacitance of the readout anode contributes significantly to the noise of the sensor. Further, the capacitance of the readout node is directly related to the size of the anode. In the case of a suitable transport field, the size of the readout anode and thus its capacitance can be minimized by reducing to a point anode.
The main advantages of the sidewards depletion are the reduction of the necessary biasing voltages and the decreased capacitance of the readout node, important for the noise contribution of the sensor.

4.3.2. Silicon Drift Detectors

The principle of SDDs is derived from sidewards depletion, explained in section 4.3.1 and based on the concept of the semiconductor drift chamber invented by Gatti and Rehak in 1984 [36].
To speed up the electron collection process of a sidewards depleted device, the depletion region can be overlaid with a electric field parallel to the wafer surface. This can be achieved by segmenting the p-implantation into strips and applying potentials rising from strip to strip [113].
There are several variations of SDD designs, one of them is a circular SDD as shown in figure 4.8. The drift electrodes are arranged in a circular array with a small readout anode located in the center of the device. The circular drift rings force the generated signal electrons to move towards this readout node from where they are transferred to the readout electronics, an integrated amplifier [59]. As the charge created by the absorbed photon drifts directly to the readout anode, the device needs to be readout continuously to prevent signal loss. Thus each sensor cell needs its own electronics for amplifying and reading the detected signal.
SDDs are used in various fields of application. For example, the instrument Alpha

Particle X-ray Spectrometer (APXS) on-board of the Mars rover Curiosity as part of NASA's Mars Science Laboratory mission. The SDD is used to map the spectra of re-emitted X-rays for determining the elemental composition of samples [43], [37]. SDDs were also part of the space mission Large Observatory for X-ray Timing (LOFT) proposed as Cosmic Vision M-class candidate mission to ESA. For this mission the use of SDDs has been proposed for two scientific X-ray detecting devices, to perform high-time-resolution X-ray observations of compact objects [128].

SDDs are very suitable for X-ray spectroscopy, as they comprise a fast signal detection within a timing precision of nanoseconds. They provide a low readout node capacitance for low noise and fast signal detection.

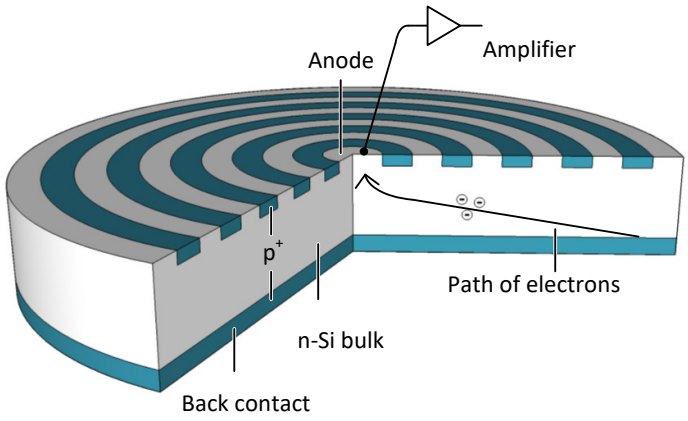


Figure 4.8.: Cylindrical SDD with integrated amplifier for spectroscopic applications. Electrons are forced by an electrical field towards the readout anode in the center of the device.

4.3.3. CCD Sensors

Since several years, CCD based detectors have been used for X-ray satellite missions with main applications in imaging optics. CCDs are capable of measuring energy, position and arrival time of individual X-ray photons covering an energy range from $100\,\mathrm{eV}$ to $15\,\mathrm{keV}$ [111].

CCDs were originally developed as electronic imagers with optical purposes [16]. Only a few micrometers of surface depletion are sufficient to cover the bandwidth of optical light from $350\,\mathrm{nm}$ to $650\,\mathrm{nm}$. The depletion is achieved through a conductor-oxide-semiconductor structure in non-equilibrium condition [111].

To make the devices more sensitive to X-rays, i.e. shorter wavelength, the devices can be adapted by increasing the depletion thickness and enable the devices for back-illumination. Such detectors were used, for example, on the X-ray telescopes Chandra and XMM-Newton in the dispersive spectrometers [34], [102].

A special type of CCD is the pnCCD developed for X-ray spectroscopy and imaging with high time resolution and quantum efficiency and extended high energy response to X-rays up to $30\,\mathrm{keV}$.
Figure 4.9 depicts the principle of a pnCCD device, which is based on sidewards depletion. The potential minimum is shifted to the front side of the device by applying asymmetric bias voltages. The front side strips are not connected in a decreasing cascade, as it is applied by SDDs. Instead, every third strip is connected to a common voltage signal. Three p+ strips (shift registers) with the potentials ϕ_1, ϕ_2 and ϕ_3 spread the sensitive volume in rows. To prevent spread of signal charges along the strips with additional strips placed perpendicular to the gate direction. These strips may be called channel guides [65] and divide the device area with the shift register strips into pixels. Electrons generated in the bulk of the device drift to the potential minimum, where they stay until readout. Readout is performed by applying a periodically varying potential to the shift registers in order to move the potential minimum to the readout nodes. Each pnCCD line is connected to an integrated readout amplifier.

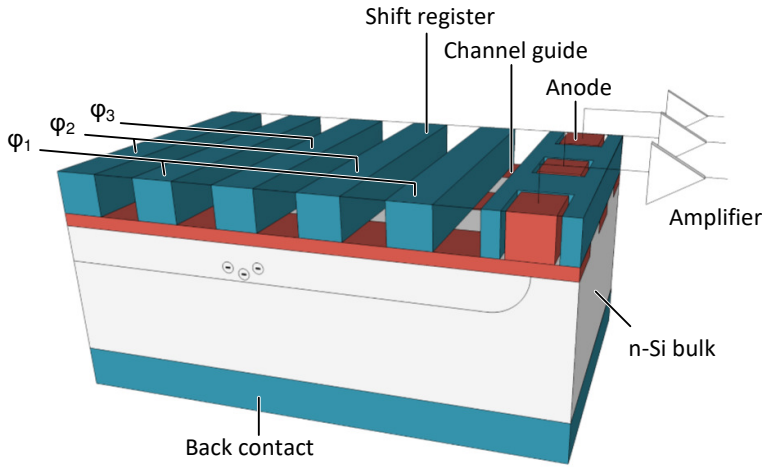


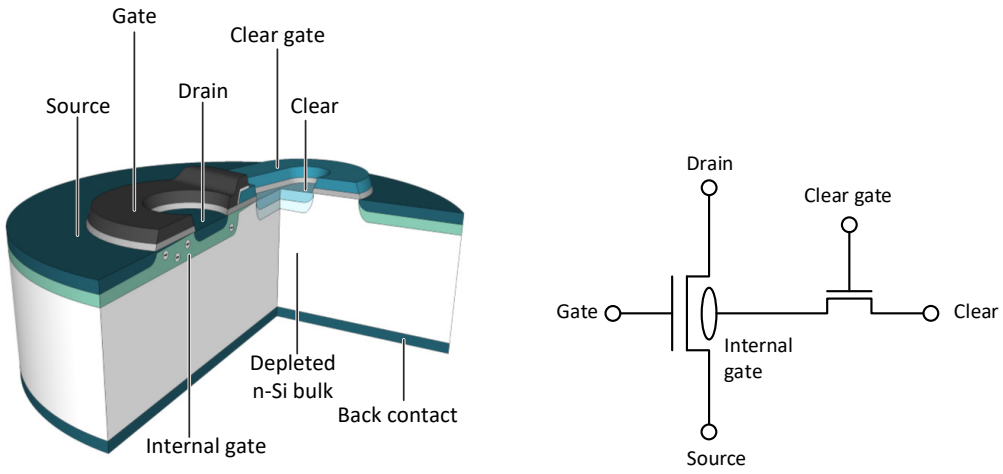
Figure 4.9.: Basic structure of a pnCCD

pnCCDs were successfully operated at space telescopes and on ground. For example, the pnCCD is one of three focal plane detectors on-board ESA's XMM-Newton satellite launched in 1999 and still operates successfully [102]. On ground, the pnCCD sensor is used in various experiments, for example in X-ray microscopy [94].

A special variant of the pnCCD is used in the X-ray telescope eRosita, the framestore pnCCD. This device is extended by a insensitive area. The charge accumulated in the image area is shifted in a fast way to the framestore region to allow a slower readout. This reduces out-of-time events generated by photons which are accumulated during charge transfer and readout [68].

4.3.4. DEPFET Technology

The Depleted P-Channel Field Effect Transistor (DEPFET) concept was first introduced by J. Kemmer and G. Lutz in 1987 [52] and then demonstrated in 1990 [51]. The DEPFET devices are based on the principle of sidewards depletion, as described in section 4.3.1.



(a) DEPFET pixel

(b) Equivalent circuit

Figure 4.10.: Circular DEPFET pixel cell (a) and its equivalent circuit (b).

Figure 4.10 depicts a cut through a DEPFET pixel cell and its equivalent circuit. The DEPFET structure is built up with two coupled MOSFETs:

1. A p-channel metal oxide semiconductor (PMOS) transistor is formed by a p+ doped drain and source contacts on depleted n-silicon bulk and an external gate.

2. An n-channel metal oxide semiconductor (NMOS) transistor, formed by an n-doped implantation below the gate called "internal gate", a voltage controllable barrier called "clear gate" and an n+ doped clear contact, shielded towards the bulk by a deep p-implanted well.

The detection of charge is based on the principle of charge deposition and separation in the DEPFET structure. If an appropriate bias voltage is applied to the front and back side, the device is fully depleted causing a potential minimum below the whole surface. Below the gate the minimum is constricted by the deep n+ doping. If electron-hole pairs are produced in the depleted bulk by ionizing radiation or thermal generation, the holes will drift to the backside and electrons will be accumulated in the potential minimum. When the PMOS transistor is turned on with a specific gate voltage, the transistor current is modulated by mirror charges induced by the collected electrons in the potential minimum. The transistor current is a measure for the amount of electrons collected in the potential minimum. Accordingly the transistor is steered with the collected charge [14].

Contrary to CCD sensors, where the charge has to be shifted, a DEPFET has a readout node at each pixel providing a first amplification stage for the accumulated charge. The characteristics of a DEPFET cell can be described by two small signal parameters g_m and g_q. The gate transconductance (transfer conductance) g_m is given by the change in the drain current I_{DS} divided by the small change in the gate-source voltage U_{GS} with a constant drain-source voltage U_{DS}

$$g_m = \left.\frac{\partial I_{DS}}{\partial U_{GS}}\right|_{U_{DS}=const}. \tag{4.35}$$

In addition to the transconductance g_m of the external gate, g_q describes the charge "steilheit" of the internal gate [65]. The influence of the accumulated charge in the internal gate Q_{int} on the drain current I_{DS} can be expressed as

$$g_q = \left.\frac{\partial I_{DS}}{\partial Q_{int}}\right|_{U_{DS}=const,U_{GS}=const}. \tag{4.36}$$

The value of g_q strongly depends on the DEPFET properties like transistor gate width and length, gate channel capacitance, doping concentrations and biasing conditions. Typical values for the amplification g_q reach from $300\,\mathrm{pA/e}$ to $600\,\mathrm{pA/e}$. Overall, the gain of a DEPFET pixel can be expressed with equation 4.35 and equation 4.36 as

$$G_{DEPFET} = \frac{g_q}{g_m}. \tag{4.37}$$

With typical values of $g_m = 66\,\mu\mathrm{A/V}$ and $g_q = 300\,\mathrm{pA/e}$ a total gain for a DEPFET cell of $G_{DEPFET} = 4.54\,\mu\mathrm{V/e}$ can be obtained. With equation 4.35 and 4.36 the drain-source current I_{DS} trough the transistor can be described as

$$I_{DS} = I_0 + \Delta U_{GS} \cdot g_m + \Delta Q_{int} \cdot g_q. \tag{4.38}$$

Since the internal gate not only collects the electrons generated by X-ray photons but also thermally generated electrons and the non-destructive readout of a DEPFET cell,

the internal gate has to be cleared regularly. Therefore a second NMOS transistor is implemented. To remove the stored charge from the internal gate, a positive pulse is applied to the clear contact, inducing the electrons in the internal gate to drift to the clear region. The clear region is shielded towards the bulk by a deep p-implantation to prevent charge losses.

4.4. WFI Sensor Technology Trade-Off

SDD, CCD and DEPFET-based sensors could be potentially utilized as imaging and spectroscopic sensor of the WFI.
To fulfill the Athena science requirements, the WFI sensor needs to accomplish a high spectral and spatial resolution over a large field of view. Bright point sources with intensities of up to 1 Crab shall be observed, achieving low pile-up and high throughput. A list of the requirements can be found in table 2.1.
The currently operating X-ray observatory XMM-Newton and the future X-ray telescope eROSITA employ pnCCD-based sensors. Although they provide a high spectral and spatial resolution over a wide energy range, the time resolution is limited. With the large effective area of the Athena mirror system a significantly higher photon flux is expected what requires a faster sensor than pnCCDs. The 384×384 pixel detector of eROSITA is readout in $50\,\mathrm{ms}$ per frame, whereas the WFI LDA with 1024×1024 pixel requires a readout of $50\,\mathrm{ms}$ per frame. An even faster sensor would be an SDD, however, the high spatial resolution required for the WFI can not be achieved.

DEPFET active pixel sensors are best suitable for the WFI detector. The major benefits are summarized below [108], [71], [44], [9], [67]:

- DEPFET sensors permit a fast readout as no charge transfer is needed. The readout of CCD sensors is limited by the charge transfer speed.
- Very low readout noise due to the low readout capacitance of the DEPFET and thus excellent energy resolution even at high speed.
- Increased quantum efficiency at high X-ray energies, because the DEPFET is a fully depleted device and the full wafer thickness of $450\,\mathrm{\mu m}$ is sensitive.
- DEPFET based devices are back-illuminated devices, which provide an unobstructed, homogeneous entrance window with 100% fill factor and excellent quantum efficiency (QE) in the low energy range.
- The pixels of the DEPFET matrix can be accessed randomly achieving flexible

readout modes. This allows observing objects in a large range of brightness without being limited by pile-up effects.

- The sensor is power efficient, as the pixels are turned on only during readout in the applied rolling shutter operating mode.
- There is no need of an additional framestore area as used with pnCCDs.
- DEPFET sensors show a good radiation tolerance, as the signal is only broadened by higher leakage current. In CCD based systems, where the charge is transferred parallel to the wafer surface over long distances, trapping (radiation induced defects) is the major reason for degrading the charge transfer efficiency. This does not apply for DEPFET sensors.

5. X-Ray Imaging with the Wide Field Imager

This chapter introduces X-ray imaging with the WFI camera based on DEPFET detectors. First, the detector system is explained in section 5.1, with focus on detector operation and readout. Section 5.2 outlines data acquisition and processing, which is performed in the development phase in a breadboard setup and for flight in the Detector Electronics including a Frame Processor. At last, radiation damage effects on the detector are summarized in section 5.3.

5.1. DEPFET-based Detector System

The WFI detector system consists of a large detector (LD) and a fast detector (FD). Each detector includes a DEPFET sensor matrix with Control Front-End Electronics (CFE) and Analog Front-End Electronics (AFE). The CFE is realized with the row-steering ASIC Switcher-A, the AFE with the readout ASIC Veritas-2. In the following section, the characteristics and operation of the DEPFET sensor matrix, CFE and AFE are explained in detail.

5.1.1. DEPFET Readout

DEPFET devices are readout in a so-called correlated double sampling mode. Correlated double sampling is a method to measure electrical signals that allows to cancel an undesired offset. The output of a sensor is measured twice: once in a known condition and once in an unknown condition. These values are then subtracted from each other to generate a value with a known relation to the physical quantity being measured [48]. In the case of DEPFET detectors, the channel conductance of the transistor is measured with filled and emptied internal gate. The difference of both measurements corresponds to the generated charge. The readout scheme of a DEPFET pixel is described below:

1. charge accumulation in the internal gate
2. turning on of the DEPFET transistor by switching on the external gate

3. first measurement: *baseline + signal*
4. charge removal out of the internal gate by switching on the clear and clear gate
5. second measurement: *baseline*
6. turning off of DEPFET transistor by switching off the external gate

Therefore the DEPFET nodes need to be sequenced in a specific order, shown in figure 5.1. The DEPFET transistor is switched on by applying a negative voltage to the external gate contact. The first measurement of *baseline + signal* can be performed. Then the internal gate of the DEPFET cell is emptied by applying a positive voltage to the clear and clear gate nodes for an appropriate time. At the end, a second readout measures the *baseline* signal and the DEPFET is switched off.

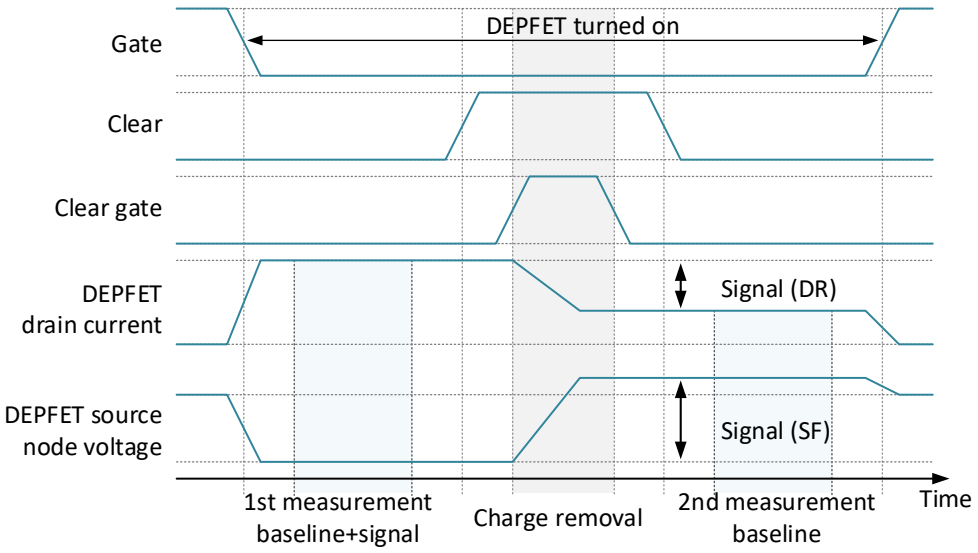


Figure 5.1.: Timing diagram of a DEPFET readout. Correlated double sampling is performed by reading out of the accumulated signal before and after the charge removal out of the internal gate. The signal charge of the internal gate can be either readout as a voltage signal at the source node or as a current signal at the drain of the DEPFET.

The signal on the output node of the DEPFET is fed into the readout electronics. There are two different readout methods: a drain-current readout mode and a source-follower readout mode. Depending on the readout mode, the signal of the output node of the DEPFET is either a voltage step at the source node (source-follower readout (SF)) or a change in the drain-source current (drain-current readout (DR)). Figure 5.1 depicts the DEPFET output node for both readout methods. The resulting signal information is obtained by subtracting the first and second measurement.

Readout Timing Sequence

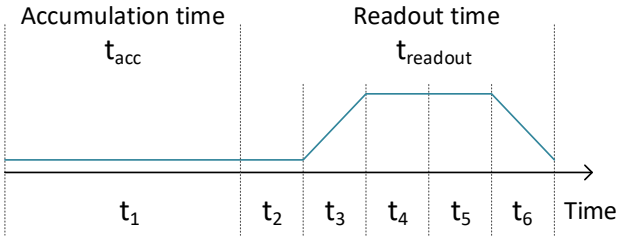
The timing sequence of processing a DEPFET row can be divided into a charge accumulation phase and a readout phase. The readout phase is composed of a first measurement, a clear and a second measurement. In addition, settling times extend the processing time for readout. In source-follower mode they are considerably long, in drain readout mode the settling times are significantly reduced [108]. Figure 5.2 shows the timing process of a DEPFET cell with charge accumulation time t_{acc} and readout time $t_{readout}$. The time t_{row} needed for processing a row is

$$t_{row} = t_{acc} + t_{readout}. \tag{5.1}$$

The readout time $t_{readout}$ can be summarized to

$$t_{readout} = t_2 + t_3 + t_4 + t_5 + t_6. \tag{5.2}$$

As the DEPFET device is always sensitive to incoming photons, charge deposition can also take place during readout phase. If an incoming photon hits the sensor during the readout time, it is not or not completely detected. These effects and the impact on the detected charge are explained in section 7.3.1.



t_1	accumulation time
t_2	settling time
t_3	first measurement
t_4	charge removal
t_5	settling time
t_6	second measurement

Figure 5.2.: Processing of a DEPFET row with charge accumulation phase and readout phase. The readout phase is divided in settling, first measurement, charge removal, settling and second measurement.

Source-Follower Readout

An equivalent circuit of a DEPFET cell, configured in source-follower readout mode is depicted in figure 5.3a. Here, the transistor is biased by a current source, keeping the drain-source current I_{DS} at a constant level. The charge in the internal gate modulates the channel conductance of the transistor. Due to the fixed drain potential, a constant current I_{DS} causes a voltage drop over the transistor channel and changes the potential at the source node and the voltage U_{GS}.

As mentioned in section 5.1.1, DEPFETs are readout, using the method of correlated double sampling. Therefore two measurements with filled and emptied internal gate ($Q_{int} = 0$) are taken. In source-follower configuration, equation 4.38 leads to following assumptions

$$\begin{aligned} I_{DS,before} &= I_0 + 0 \cdot g_m + \Delta Q_{int} \cdot g_q \\ I_{DS,after} &= I_0 + \Delta U_{GS} \cdot g_m + 0 \cdot g_q. \end{aligned} \tag{5.3}$$

As the current I_{DS} is kept constant, before and after charge removal, the terms can be equated with each other, and solved with respect to ΔU_{GS} to

$$\Delta U_{GS} = \frac{g_q}{g_m} \cdot \Delta Q_{int}. \tag{5.4}$$

This means, the change in the source node voltage is proportional to the charge accumulated in the internal gate.

The input signal of the readout circuit results from a voltage drop at the source node. The readout circuit is AC coupled to allow easy biasing and signal adjustment. But this results in a settling time of the voltage signal. The settling time is given by the resistor-capacitor (RC) time constant of the input of the readout chain. The time constant is given by the DEPFET gate transconductance g_m and the capacitance $C_{in,par}$. This capacitance is associated to the parasitic capacitance of the DEPFET source line and the input capacitance of the readout electronics

$$\tau = R \cdot C = \frac{1}{g_m} \cdot C_{in,par}. \tag{5.5}$$

This settling time takes place after DEPFET activation and after clear, see figure 5.2. Typical values of $g_m = 66\,\mu\mathrm{A/V}$ and $C_{in,par}$ in the range of $20\,\mathrm{pF}$ to $40\,\mathrm{pF}$ lead to settling times (10%-90%) around $1\,\mu\mathrm{s}$.

Drain-Current Readout

Figure 5.3b depicts a DEPFET transistor in drain-current readout mode. The DEPFET source node is kept at a fixed potential and the drain is connected to a current source. This current source subtracts a current I_{bias} from the drain-source current I_{DS}, which varies in dependence of the accumulated charge in the internal gate. I_{DS} is the sum of a high biasing current and a small signal current I_{signal}. The remaining signal current is fed into a transimpedance amplifier. Equation 4.38 leads to

$$\begin{aligned} I_{DS,before} &= I_0 + 0 \cdot g_m + \Delta Q_{int} \cdot g_q \\ I_{DS,after} &= I_0 + 0 \cdot g_m + 0 \cdot g_q. \end{aligned} \tag{5.6}$$

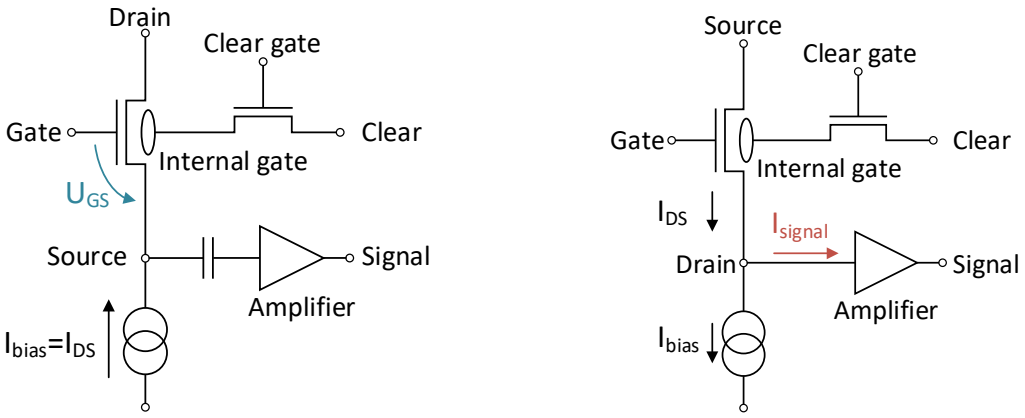
The voltage drop ΔU_{GS} can be set to zero because the transistor voltages are not changed during the measurement and so the gate-source voltage U_{GS}. An ideal clear process is assumed and ΔQ_{int} can be set to zero after the clear process. Effects of incomplete clear procedures are described in section 7.3.2.

I_{signal} can be derived from the difference of the currents before and after the charge removal

$$I_{signal} = I_{DS,before} - I_{DS,after} = \Delta Q_{int} \cdot g_q. \tag{5.7}$$

As it can be seen regarding equation 5.7, the measured current I_{signal} is proportional to the accumulated charge in the internal gate.

The main advantage of the drain-current readout is that all the nodes of the DEPFET are at a fixed potential. In contrast to the source-follower configuration, the settling times can be almost neglected and the readout speed is not limited by the RC time constant of the readout chain. This means that the readout time in drain-current mode is reduced significantly.



(a) source-follower readout

(b) drain-current readout

Figure 5.3.: Schematics of the DEPFET readout modes: (a) Source-follower readout: the current is kept constant by the current source while the source node voltage is measured which depends on the DEPFET channel conductance. (b) Drain-current readout: a biasing current is subtracted from the drain-current, resulting in a signal current which depends on the amount of accumulated charge in the internal gate.

5.1.2. DEPFET Matrices

The DEPFET working principle and the readout of a single DEPFET cell are explained in section 4.3.4 and 5.1.1. Imaging detectors can be built up as an array consisting of several DEPFET pixels. A direct connection between the pixel nodes and the power, control and readout circuits would be possible, but too complex and inefficient because it would increase the overall power consumption of the device.
Figure 5.4 shows a simple interconnection scheme exemplary for a 4×4 pixel matrix. Depending on the readout mode, the source or respectively the drain nodes of all pixels are connected to a global contact. The terminals gate, clear gate and clear are coupled row-wise to the CFE to select one row at a time. The drain or source respectively is connected column-wise to the readout AFE to enable parallel readout.

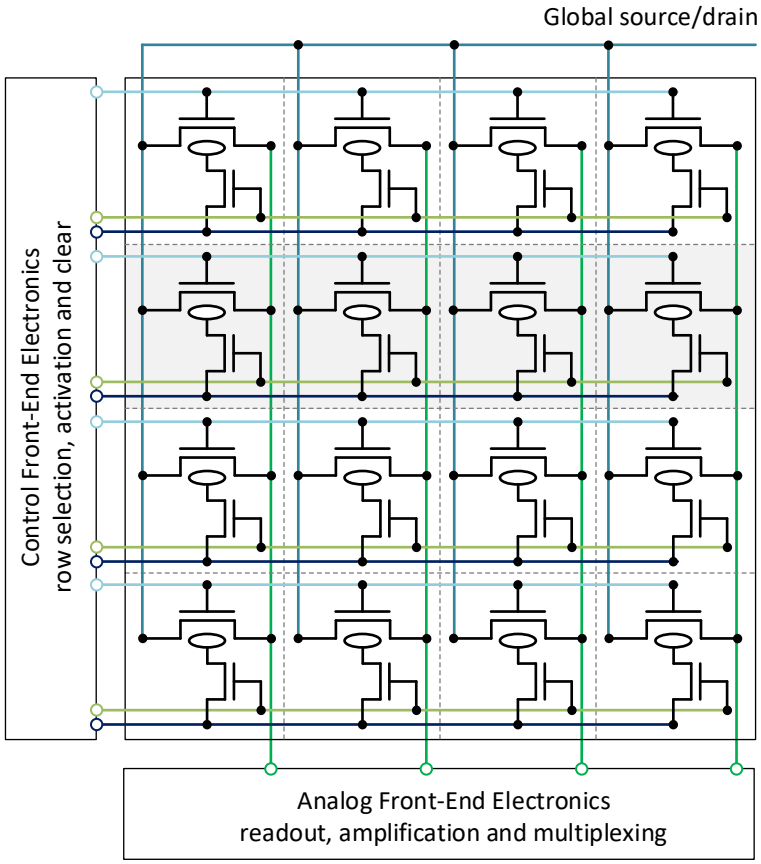


Figure 5.4.: Schematic interconnection scheme for a DEPFET matrix with 4×4 pixels. Depending on the readout mode, either the source or drain is connected globally while the other contact is connected column-wise to the AFE for readout. The DEPFET nodes gate, clear gate and clear are connected row-wise to CFE for row-steering. The active row is highlighted in gray.

The AFE and CFE to be used for the WFI are ASICs called Veritas-2 and Switcher-A. The ASICs are operated to perform row selection, biasing and readout according to the DEPFET readout scheme, depicted in figure 5.1. Details about AFE and CFE can be found in the following sections 5.1.3 and 5.1.4.

Rolling Shutter Mode

Each DEPFET pixel accumulates the generated charges continuously. The charge is readout row-wise in a rolling shutter mode either as a current or a voltage signal. While reading out a row, the collected charge is removed and the next exposure is started. Simultaneously the next row is activated for readout. When the last row is processed, a complete frame is obtained and the readout of the first row is started again. Figure 5.5 illustrates the rolling shutter mode for a DEPFET matrix with four rows schematically.

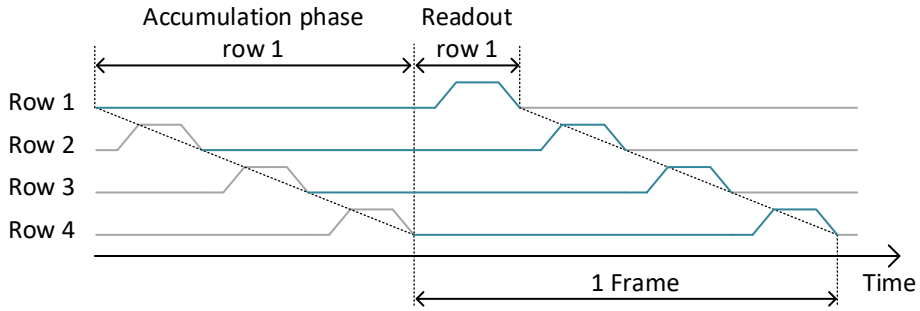


Figure 5.5.: Readout of four rows in rolling shutter mode. After finishing the readout of one row, the next row is activated for processing. A complete frame is obtained after readout of all rows.

The processing of a complete frame is dependent on the time taken for a readout and the number of rows. The total charge accumulation time t_{acc} for a pixel matrix with N rows results to

$$t_{acc} = (N-1) \cdot t_{readout} \tag{5.8}$$

with $t_{readout}$ being the sum of times necessary to read out a row, see equation 5.2. A faster processing can be achieved with configuration of the matrix in drain-current readout mode, as the settling times are smaller.

5.1.3. Analog Front-End Electronics - Readout ASIC Veritas-2

The DEPFET devices are read out with the ASIC Veritas-2 (Versatile Readout based on Integrated Trapezoidal Analog Shapers), developed at the MPE [83], [84]. The readout ASIC is realized in a $0.35\,\mu\mathrm{m}$ CMOS $3.3\,\mathrm{V}$ technology produced by AMS and comprises the following features:

- Three individual input stages for pnCCD readout, DEPFET source-follower voltage readout and DEPFET drain-current readout.
- 64 parallel analog readout channels with a voltage preamplifier to convert the single-ended input signal of the detector into a differential output voltage, a fully differential trapezoidal filter and a sample and hold (S/H) stage. The stages can be configured with different readout speeds and selectable gains.
- A 64:1 multiplexer (MUX) stage with a clock frequency up to $32\,\mathrm{MHz}$. The MUX can be operated in a user defined Region of Interest (ROI) mode, to readout arbitrarily selected areas of the sensor array.
- A set of 7-bit Digital-to-Analog Converters (DACs) in order to bias all the internal analog circuitry using a single external reference voltage. The DACs enable to select the optimum biasing scheme that minimizes the required power consumption for every ASIC operation mode.
- A static random-access memory (SRAM) composed of two memory fields. One memory field provides the dynamic control signals for the analog channels and the other contains the information for the static settings of the ASIC, like e.g. operating mode, selectable gains, DAC configurations and ROIs for the MUX. The SRAM is based on single event upsets (SEU) immune Dual Port Dual Interlocked Storage Cells (DICEs). In addition, the SRAM has a dual port memory architecture. In this way the content of the memory can be readout non destructively and can be rewritten during ASIC operation. This allows SEU check and correction during run time. The memory is programmed through a serial peripheral interface (SPI).

Figure 5.6 depicts a simplified schematic of one of the 64 analog channels of the ASIC. An analog channel is composed of an input stage, a preamplifier, an integrator stage, performing a trapezoidal filter, and an output stage. A set of static and dynamic switches are implemented to control the configuration and timing of the ASIC. The switches are controlled by an internal sequencer.

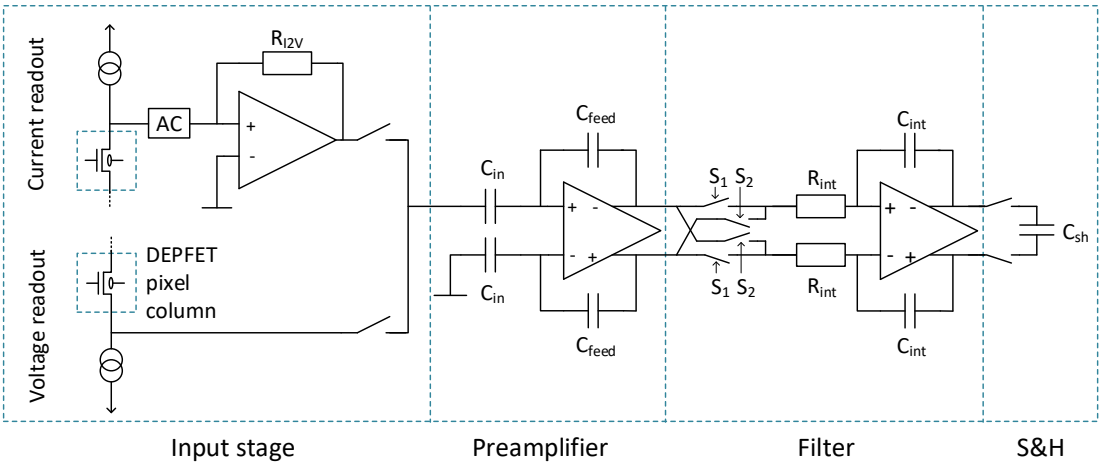


Figure 5.6.: Simplified circuit of an analog processing channel of the Veritas-2 AFE. The analog channel consists of an input stage, a preamplifier, an integrator, and an output stage. The input of the analog channel is either connected to the source (voltage readout) or to the drain (current readout) of the DEPFET transistor column. Static and dynamic controllable switches are implemented to control the analog circuit.

Input Stage

The Veritas-2 includes three individual input stages. For the WFI instrument, only two input stages are of interest: DEPFET source-follower voltage readout and DEPFET drain-current readout. The input node of the Veritas-2 is either connected to the source (source-follower readout) or to the drain of the DEPFET (drain-current readout), as explained in section 5.1.1.
Each input stage consists of an individual current source which provides a constant current through the DEPFET column. If operating in source-follower mode, the current flows from the source through the active DEPFET pixel to the global drain connection of the sensor. In drain-current mode, the current source provides a coarse cancellation of the bias current of the sensor. The residual current flows into a resistor of a transimpedance amplifier (I2V) to convert it into a voltage. This relationship can be described by Ohm's law

$$U_{out,I2V} = -R_{I2V} \cdot I_{signal} \tag{5.9}$$

where $U_{out,I2V}$ is the output signal of the current-to-voltage (I2V) stage, R_{I2V} the transimpedance amplifier feedback resistance, and I_{signal} the current relating to the

accumulated charge. An active cascode is implemented to decouple the input of the I2V stage from the large detector capacitance, which would cause circuit instability and reduce the readout speed.
The advantages of operating a DEPFET matrix in drain-current mode are outlined in section 5.1.1.

Preamplifier

The voltage preamplifier converts the single-ended signal origins at either the sensor or the I2V output into a differential output voltage signal. Different selectable gains of the amplifier allow a huge variety of dynamic ranges. The preamplifier is composed of an input capacitance C_{in} and a feedback capacitance C_{feed}. Thus, the output voltage signal of this stage is given by

$$U_{out,pre} = -U_{in,pre} \cdot \frac{C_{in}}{C_{feed}}. \tag{5.10}$$

Filter

The output of the preamplifier is converted into a current signal by the input resistor of the integrating amplifier. This current is accumulated by the following filter stage. The stage consists of a single differential integrating amplifier and a set of digital controllable switches.

In a first phase, the *baseline + signal* is read out and the filter integrates the two currents, proportional to the preamplifier output, on the feedback capacitors. In a second phase, the *baseline* signal is read out, therefore the switches are toggled and the currents into the amplifier have opposite polarities. This results in discharging the feedback capacitors. At the end, the residual output signal of the filter stage corresponds to the difference of *baseline + signal* and *baseline*. The output voltage of the integrator stage can be calculated to

$$U_{out,filt} = \int_0^{\tau_{int}} \frac{U_{in,filt}}{R_{int} \cdot C_{int}} dt = U_{in,filt} \frac{\tau_{int}}{R_{int} \cdot C_{int}} \tag{5.11}$$

with R_{int} being the input resistance, C_{int} the feedback capacitance and τ_{int} the integration time of the filter stage.

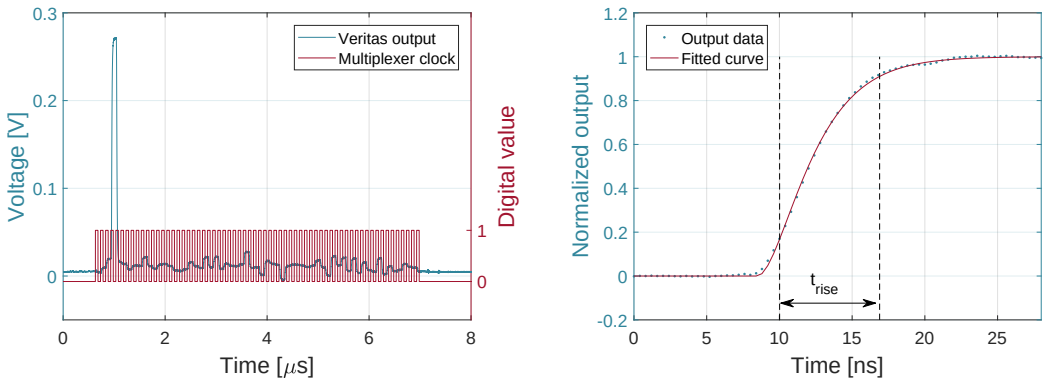
To summarize, the Veritas-2 AFE can be used to readout DEPFET matrices in source-follower and drain-current readout. With the following equations, the output signal of the analog channel can be calculated for SF and DR. The equations assume an

equal integration time for the first and second integration. The voltages U_{in1} and U_{in2} correspond to the input voltage signal of the first and second measurement in SF configuration and I_{in1} and I_{in2} to the input current signal in DR configuration.

$$U_{out,SF} = \frac{C_{in}}{C_{feed}} \cdot \frac{\tau_{int}}{R_{int} \cdot C_{int}} \cdot (U_{in1} - U_{in2}) \tag{5.12}$$

$$U_{out,DR} = R_{I2V} \cdot \frac{C_{in}}{C_{feed}} \cdot \frac{\tau_{int}}{R_{int} \cdot C_{int}} \cdot (I_{in1} - I_{in2}) \tag{5.13}$$

As a final step, the output of the filter stage is stored in the sample and hold stage. The values from 64 S/H stages are serialized by an internal 64:1 analog multiplexer with a maximum clocking speed of 32 MHz and transferred to a fast differential output buffer. Figure 5.7a shows the output of the Veritas-2 measured with an oscilloscope. The plot corresponds to a measurement of one row of a DEPFET matrix with 64 columns. Each pixel value is represented by a voltage step at the Veritas-2 output. A test signal was induced in channel four to simulate a photon hitting the detector.
Figure 5.7b shows the rising edge of the channel four with test signal. The amplitude is normalized and the signal fitted to obtain the rise time t_{rise}. The resulting rise time is approximately 7 ns.



(a) (b)

Figure 5.7.: Output signal of the Veritas-2: (a) difference of the two differential output signals, corresponding to the output of a DEPFET detector row with 64 columns. A test signal was induced in the fourth channel, resulting in a higher amplitude. The clock signal of the multiplexer is depicted in red. (b) enlarged and normalized graph of the rising edge of the channel with test pulse. The rise time is obtained by the fitted signal.

5.1.4. Control Front-End Electronics - Row-Steering ASIC Switcher-A

The row-steering of the DEPFET sensor matrices is performed by the Control Front-End Electronics (CFE). Therefore, analog multiplexing ASICs called Switcher-A are used. The purpose of the CFE is to turn on the sensor matrix row in a rolling shutter mode. This is performed by applying a sequence of voltages to the active row for readout. With the structure of the Switcher-A, a voltage sequence can be applied to the DEPFET nodes gate, clear gate and clear to perform the operations of pixel activation, clear and pixel switch off. The appropriate readout scheme is described in section 5.1.1.
A simplified block diagram of the Switcher-A is depicted in figure 5.8. The Switcher has 64 channels with 3 ports (A, B, C). Each port has two input voltages (High and Low), an enable input and an analog output. The switching channels can be activated with a shift register and additional control logic. If a channel is activated, the output can be switched between the two input levels of the respective port. Fast enable input signals per port allow to enable the switches with a well defined timing.

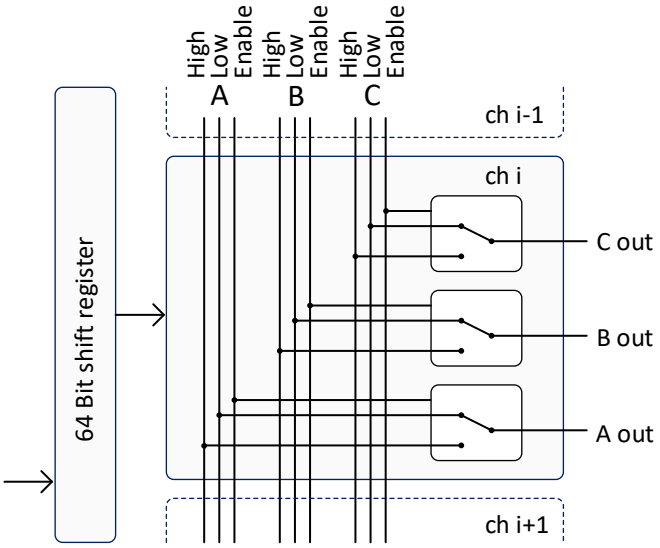


Figure 5.8.: Simplified block diagram of the Switcher-A row-steering ASIC with 64×3 analog switching channels. By clocking the shift register the channels are activated consecutively to operate the matrix in a rolling shutter mode.

The channels can switch voltages up to $30\,\mathrm{V}$ with fast rise- and fall times (<$10\,\mathrm{ns}$ of a $20\,\mathrm{V}$ signal into a $10\,\mathrm{pF}$ load). For operation of matrices with more than 64 rows, the Switcher ASICs can be connected in a daisy chain. The WFI LD, consisting of 512×512 pixels is connected to 8 Switcher chips.

The Switcher-A is specifically developed for space applications. The device is radiation tolerant up to $>100\,\mathrm{krad}$. The SEU tolerance of the chip is maximized as no configuration bits are needed and an output pattern can be monitored to control correct behavior. The ASIC is produced in a high voltage CMOS process developed by AMS.
The Switcher-A is a further development of the Switcher-S, which will be used to steer the DEPFET matrix of the Mercury Imaging X-ray Spectrometer (MIXS) instrument of the BepiColombo mission [110].

5.2. Data Acquisition and Processing

In order to operate the detector as described in section 5.1, different tasks have to be accomplished. For this purpose, a data acquisition system needs to perform the following functions:

- Time control of DEPFET sensor, FEE and peripheral electronics
- Data digitization and pre-processing
- Power conditioning
- Housekeeping

For the WFI, these tasks are fulfilled by the Detector Electronics (DE). At the current development phase, this is performed by a breadboard model of the DE.
In the following sections, the WFI DE with its main functionality and its architecture is explained. An important feature of the DE is the on-board data pre-processing. Detailed information about the processing algorithms and data rates are given. Subsequently, the developed breadboard model of the DE Frame Processor (FP) is introduced.

5.2.1. Detector Electronics

The main functionality of the DE is to provide all clock signals and power supply to operate the detector, digitize the analog detector signals and perform data pre-processing including event detection. At last, the acquired data needs to be provided to other systems for further processing. These tasks are distributed among three units:

- Power Conditioner Module (PCM)
- Frame Processor (FP)
- Interface (I/F) unit

Figure 5.9 presents a schematic block diagram of the DE with its three modules.

In total, there are five DE boxes mounted close to the Camera Head (CH), one for each of the four LDs and one for the FD. Hence, each detector of the CH is connected to its dedicated DE.

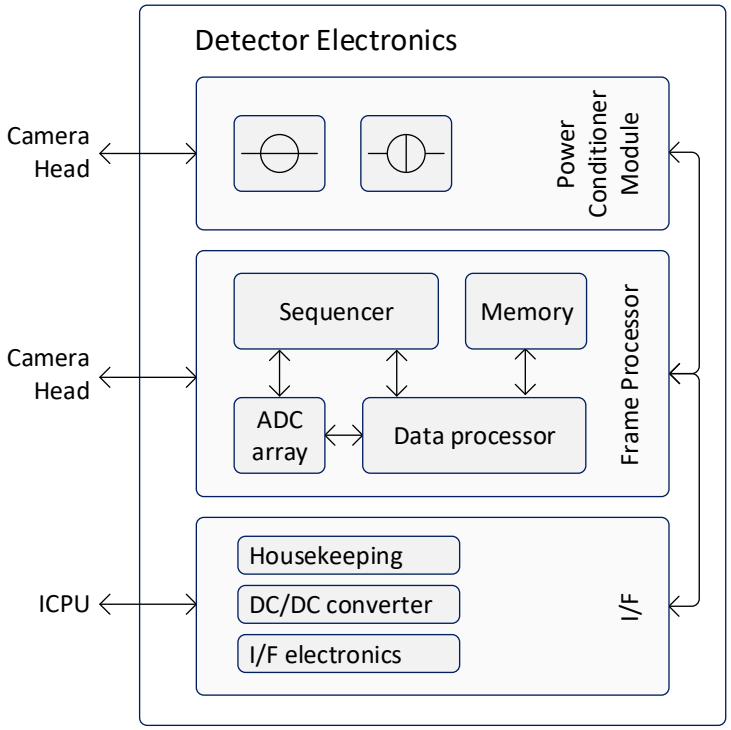


Figure 5.9.: Block diagram of the Detector Electronics with its three modules Power Conditioner, Frame Processor and I/F Unit. The I/F Unit serves as communication interface to the ICPU, whereas the Power Conditioner and the Frame Processor Board are connected to the Camera Head.

Power Conditioner

The power conditioning for CFE, AFE and DEPFET sensors are generated by the Power Conditioner Module (PCM). Input of the PCM is the power distributed by the Instrument Control and Power-Distribution Unit (ICPU). This module shares the power supplied from the spacecraft power bus to all DE subsystems. Approximately up to 30 analog and digital supply and bias voltages or currents need to be provided for the detectors. The provided power supplies are fixed supplies for CFE and AFE biasing, programmable supplies for DEPFET switching and biasing and programmable high-voltage supplies for DEPFET biasing. Furthermore the PCM is responsible for housekeeping and monitoring of supply voltages and currents.

Frame Processor

The Frame Processor (FP) is part of the signal processing chain. The FP board is directly connected to the CH via flexible leads. It includes several important submodules:

- **Sequencer Block**
  A sequencer block is implemented on the FP board inside an FPGA to generate all digital signals required for operation of the detector. This includes a slow control communication with the ASICs. The AFE is programmed through SPI and the static configuration of the CFE can be set. Moreover a pattern generator generates all fast clock signals for operation. Thereby the shaping and multiplexing of the AFE and the row switching of the CFE and steering voltages to the DEPFET nodes are controlled. Furthermore, a timing bus is realized to synchronize all units of the detector and DE. This contains AFE, CFE, analog-to-digital converters and data processing. At last, the sequencer block is responsible for monitoring of the digital output signals of the detector. Both, AFE and CFE have specifically designed output patterns which can be monitored to detect failures in synchronization, operation or to detect single event effects (SEE). The procedure and required signals for control and readout of DEPFET based detectors are detailed in section 5.1.

- **ADC Array**
  The analog output signals of the detector are directly connected to an Analog-to-Digital Converter (ADC) array on the FP board. The DE connected to the LD, involves eight ADCs to digitize eight serial analog data streams from eight Veritas-2 ASICs in parallel. The DE associated to the FD, includes two ADCs for digitization of data streams transferred from two Veritas ASICs. For signal conditioning, buffers are implemented in the processing path between Veritas and ADC, in order to adapt the differential analog signals to the input of the ADCs.
  In order to achieve the energy resolution requirement for the WFI, the ADC needs to provide an effective number of bits (ENOB) of at least $10\,\mathrm{bit}$. Typical space qualified ADCs with an ENOB of minimum $10\,\mathrm{bit}$, have a resolution of $14\,\mathrm{bit}$ [81]. The readout time of the FD is $2.5\,\mu\mathrm{s}$ per sensor row. Thus the pixel frequency results in $64\,\mathrm{pixel}/2.5\,\mu\mathrm{s}$. In order to perform this required readout time, the sample rate of the ADC needs to be larger than $25.6\,\mathrm{MSPS}$.
  For synchronization and to control the sample point of all ADC channels, the ADC array is linked to the sequencer unit.

- **Data Pre-Processing**
  After digitization of the analog data, the FP performs data pre-processing. The downlink rate of the Athena observatory is limited to approximately $75\,\mathrm{Gbit/d}$. The raw data rate of the detectors is many times larger. Therefore, on-board processing and data reduction is indispensable.
  On-board processing needs to be performed in real-time and comprises multiple steps to enhance and reduce the amount of scientific data. These processing steps are pixel-wise offset and common mode correction, event filtering and background reduction as well as event recombination. To accomplish these steps, several LUTs need to be stored for offset and common mode correction, event detection and filtering. Therefore, the processing unit is equipped with an external memory. The processing unit is realized with an FPGA to guarantee high speed computing and real-time behavior.
  A detailed explanation of the processing steps and the resulting data rates is given in section 5.2.2.

I/F Unit

The I/F unit serves as interface towards the ICPU. It includes the primary power supply for the DE and all auxiliary electronics. Furthermore, it comprises controlling and programming commands, housekeeping, debugging information and science data transfer via SpaceWire.

All electrical interfaces between the DE and the spacecraft are situated in the ICPU. The ICPU is responsible for controlling the WFI instrument and distributing spacecraft power to all subsystems [81].

5.2.2. On-board Data Pre-Processing

The data rate of the WFI is many times higher than the downlink rate to Earth which is limited to approximately $75\,\mathrm{Gbit/d}$. Therefore, on-board data pre-processing needs to be performed by the DE before transmitting the scientific data stream to the ground station.

Figure 5.10 depicts a functional block diagram of the processing steps performed by the FP of the DE. These pre-processing tasks are outlined in the following:

Pixel-wise Offset Correction

Even if no photons hit the detector, the DEPFET pixels are collecting charge carriers generated by leakage current. The readout ASIC and the digitization by the ADC is enlarging this pixel-wise effect called offset. The baseline level of each pixel can be calculated by averaging a certain number of frames without illuminating the detector (closed position of the filter wheel). The calculated values are stored as an offset map in a memory on the FP board. In observation mode, the offset value of each pixel is subtracted from the measured pixel raw value.

Common Mode Correction

The baseline fluctuation per row, called common mode, is caused by external disturbances coupling in the DEPFET gates, leading to an increase of current in a whole row or by effects in the readout ASIC affecting all channels in the same way. Thus the common mode has to be corrected per row and readout ASIC. These external disturbances can also appear during observation. Thus, the common mode value per row needs to be corrected continuously although photon signals are present. A robust algorithm is, to subtract the median value of the respective row from each pixel value. By subtracting the median value, the algorithm can also be applied during observations, because the influence of high photon signals within the row is negligibly small.

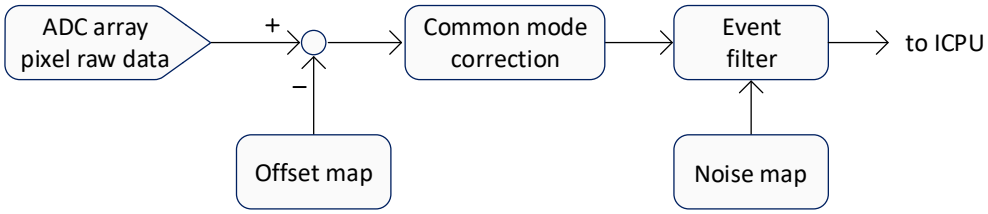


Figure 5.10.: Functional block diagram of the on-board pre-processing steps inside the FP. The data processing is performed in a pipeline to subtract offset, correct common mode effects and filter X-ray events.

Event Filtering

Event filtering reduces the FP data rate significantly, because all signals from pixels that are not hit by photons are eliminated. To distinguish noise signals from signals generated by X-ray photons, a primary threshold value is applied. The threshold value is usually set for each pixel as multiple of its noise. Neighboring pixels are compared to a second threshold to investigate split events. Therefore, a noise value of every pixel is calculated by taking several frames without photons. These pixel-wise values are saved in a noise map in the external memory of the FP. Events outside the WFI energy range, such as high-energy particles, are neglected by applying an additional upper

threshold.
An X-ray photon that hits the WFI detectors is expected to deposit its energy in up to four pixels. All patterns affecting more than four pixels are caused usually by particle hits or pattern pile-up. These invalid pixel patterns can be eliminated from the data stream to additionally reduce the data rate.

After event filtering, the data stream is not organized frame-wise anymore. The output of the FP is an event list, with the detected valid X-ray events. They are listed with their signal and incident location. Once a frame is completely processed, the event list is indexed frame-wise with a timestamp and transferred to the ICPU via SpaceWire.

Data Rates
The LDA is organized as 1024×1024 pixels with a frame rate of $200\,\mathrm{fps}$. The FD has 64×64 with a frame rate of $12\,500\,\mathrm{fps}$. Each pixel is digitized with a resolution of $14\,\mathrm{bit}$. The resulting raw data rate of the detectors are $2.94\,\mathrm{Gbit/s}$ for the LDA and $0.72\,\mathrm{Gbit/s}$ for the FD respectively.
Compared to commercial applications like TV or industrial machine vision products, the WFI internal data rates are on the upper edge. For example, a commercially available 4K resolution sensor, named as Ultra High Definition (UHD), has a resolution of 3840×2160 pixel, $25\,\mathrm{fps}$ full frame readout and a digitization of $10\,\mathrm{bit}$. This results in a bandwidth of approximately $2\,\mathrm{Gbit/s}$, which is in a similar range as the WFI sensors.

From the WFI science requirements, the maximum output data rate of the FP output can be derived. Depending on the observation mode, the maximum number of events varies. If sources are observed e.g. in a sky survey with the LDA, up to $1 \cdot 10^5$ events per second are expected to hit the detector. Observations with the FD of bright sources with intensities up to 2.5 Crab lead up to $3 \cdot 10^5$ events per second [89], [81].
As described above, only pixels within certain thresholds are further processed, the signals of all other pixels are not recorded. In order to preserve the spatial resolution, additional position bits are stored with the pixel signal. To address all pixels of the detector, $20\,\mathrm{bit}$ for the LD and $12\,\mathrm{bit}$ for the FD are needed.
The science requirements assume an usual observation time of $100\,\mathrm{ks}$ [89]. This leads to $2 \cdot 10^7$ frames for the LDA and $1.25 \cdot 10^9$ frames for the FD. To index all frames, a timestamp is introduced. $25\,\mathrm{bit}$ are required for coding the frame number of the LD and $31\,\mathrm{bit}$ for the FD.
An X-ray photon is expected to deposit its energy in up to four pixels. For this calculation, an average number of 2 pixels affected by one event is assumed. To sum up, the output data rate of the FP can be calculated to $6.81 \cdot 10^6\,\mathrm{Mbit/s}$ for the LDA and $16.0 \cdot 10^6\,\mathrm{Mbit/s}$ for the FD.

This yields to a lossless data reduction of 1:430 for the LDA and 1:45 for the FD respectively. It has to be considered that the above calculated values are only theoretical values based on assumptions and could be larger. This can be caused for example by noisy pixels that exceed the lower threshold or an incorrect detection of invalid events. The calculation shows that robust algorithms are needed for frame processing to ensure real-time processing.
Table 5.1 and 5.2 summarize the data rates of the signal processing chain from the output of the Camera Head to the output of the Frame Processor.

Table 5.1.: Calculated raw data rates before frame processing for the LDA and the FD.

	number of pixels	frame rate	pixels per second	ADC resolution	raw data rate
LD array	$4 \cdot 512 \times 512$	200 fps	$2.10 \cdot 10^8$	14 bit	$2.94 \cdot 10^9$ bit/s
FD	64×64	12 500 fps	$5.12 \cdot 10^7$	14 bit	$7.17 \cdot 10^8$ bit/s

Table 5.2.: WFI requirements and calculated data rates after frame processing.

	number of events per second	average pixels per event	position bits	time-stamp	FP output data rate
LD array	$1 \cdot 10^5$	2	20 bit	25 bit	$6.81 \cdot 10^6$ bit/s
FD	$3 \cdot 10^5$	2	12 bit	31 bit	$16.0 \cdot 10^6$ bit/s

For commercial use, there are a lot of data reduction and video compression standards like MPEG-4 Part 10/Advanced Video Coding (AVC) (H.264) [47] or JPEG compression [46]. MPEG is a compression standard used for data reduction of video streams achieving a high compression based on spatial and temporal correlation.
The WFI raw data stream allows no motion-compensated-compression, as the information in the data stream is not correlated with the time as the image content changes in successive frames. The compression method of the WFI data stream can be compared with spatial-based methods applied frame-wise.
The JPEG standard is a lossy compression based on the discrete cosine transformation within blocks of 8×8 pixels and achieves compression ratios of up to 1:20 for subjective acceptable image quality. A more powerful compression mode is JPEG2000, utilizing discrete wavelet transformation in order to achieve a higher compression at the same quality. However, these methods are not lossless and important image information

could be lost. There are also lossless compression algorithms like JPEG-LS, accomplishing reduction factors in the range of 2. Moreover, modern methods can attain a lossless compression of up to 5.
For the WFI, the data reduction algorithms are specifically adjusted to the low information content of the recorded frames. This allows to achieve a high data compression ratio compared to commercially used compression algorithms.

The pre-processed data with a reduced bandwidth is transported inside the WFI and spacecraft via SpaceWire. SpaceWire is a spacecraft communication network created by ESA which allows data rates up to $400\,\mathrm{Mb/s}$ [25]. This bandwidth is roughly equivalent to the bandwidth of USB 2.0 with $480\,\mathrm{Mb/s}$ as maximum rate [114].

5.2.3. Frame Processor Breadboard

During the technology development phase, a breadboard (BB) model of the DE is built in order to support the development process and to validate the feasibility of the design. The BB model represents selected functions to be tested. Size, shape and interfaces do not need to be representative, if they are not objected to be tested [61].
As part of the signal processing chain, a BB model of the FP is developed. The aim is to build up the entire processing chain and to demonstrate the operation of an LD with data pre-processing in real-time as described in section 5.2.2. The BB model of the Frame Processor is schematically depicted in figure 5.11.

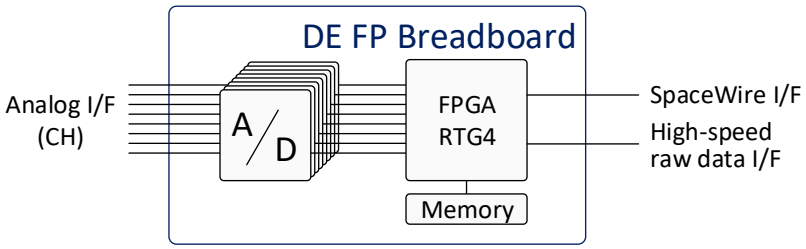


Figure 5.11.: Simplified block diagram of the FP breadboard model.

The central processing unit is a flash-based FPGA RTG4 from Microsemi. Although there are other space qualified FPGAs available, the RTG4 is best suited for this application with respect to performance, I/O resources, power consumption, price and radiation hardness. The ADC array is built up as a modular interchangeable card, which makes it easy to evaluate different types of space qualified ADCs. The on-board data pre-processing algorithms are implemented on this target hardware to demonstrate and verify the processing in real-time. A SpaceWire interface is used to connect the BB to the Electronic Ground Support Equipment (EGSE). Additional, a raw data

interface is implemented to bypass the data pre-processing. The raw data stream can be directly transferred to enable a comparison of raw data and processed data. This allows to evaluate and test the real-time data pre-processing.
Therefore, an appropriate test environment needs to be defined with the capability to stimulate the FP with the complete range of possible signals. This is performed with the PRE instrument introduced in section 3.2.

5.3. Radiation Damage Effects

The WFI is exposed to various environmental influences during its lifetime. For the electronic devices, the radiation environment is the most critical one. High energy cosmic particles passing through matter lose energy through various processes, resulting in two main types of damage: Ionizing damage and atomic displacement damage. Ionizing radiation is indicated as total ionizing dose (TID), the measure of non-ionizing radiation is non-ionizing energy loss (NIEL).

Athena will be operated in an orbit around the Lagrange point 2. Assuming an extended mission lifetime of 10 years, the WFI is stressed with a TID of $8.7\,\mathrm{krad(Si)}$ and a NIEL of $1.1 \cdot 10^8\,\mathrm{MeV/g(Si)}$ with an $5\,\mathrm{mm}$ Aluminum-equivalent shielding [90].

To minimize radiation damage of the detectors, a proton shield with an Aluminum-equivalent shielding of $40\,\mathrm{mm}$ around the Camera Head is foreseen. This reduces TID and NIEL for the WFI detectors significantly by roughly an order of magnitude [81].

Nevertheless, the DEPFET sensors and FEE are subject of radiation damage. Radiation damage effects on the DEPFET sensor due to ionizing radiation are mainly [93]:

- shift of the threshold voltages of the DEPFET transistor
- reduction of the transconductance
- increase of leakage current

The FEE is mainly subject to single event effects (SEE). An SEE is caused by a single massive particle (e.g. protons, neutrons or heavy ions) which causes an effect immediately. This effect can be non-destructive or destructive.

For the Veritas and Switcher ASICs in particular, single event upsets (SEU) errors affecting the digital section are most critical. SEU are soft errors and non-destructive. They normally appear as bit-flips in memory cells and registers leading to a change of the stored information and thus possibly malfunction of the device. This effect can be corrected by overwriting the affected cell.

6. Conceptual Design of the PRE

This chapter describes the conceptual design of the Programmable Real-Time Emulator, an instrument for evaluation of the WFI signal processing chain. The requirements of the PRE are derived from the WFI science requirements. Further, investigations of different implementation concepts are given. Finally, the overall concept of modeling and emulating of the detector system implemented in the PRE is summarized.

6.1. Requirements of the System

As explained in section 3.2, the PRE will be used for evaluation and verification of the WFI signal processing chain. The idea is to have an instrument with controllable parameters and output to replace the detector system. Therefore, it has to fulfill a set of requirements which are mainly derived from the WFI detector specifications, listed in table 2.1.

Flexibility and expandability
Flexibility and expandability are important for development of a new evaluation instrument. First, the new system will be operated with a laboratory setup or breadboard system. For this purpose, other requirements than those for operation with the later flight module are certainly applicable, concerning interfaces or number of parallel output channels. Therefore the PRE needs to be adapted to the respective module and its requirements. Moreover, the system needs to be flexible enough to cope with possible changes of the requirements in the course of the development of the WFI.

Scaling capabilities
On the way from the breadboard system to the flight module of the WFI, various sensor sizes are examined resulting in a variable number of parallel operating output channels. Therefore, the PRE needs to be able to emulate multiple concurrently operating output channels.
From the WFI requirements, listed in table 2.1, the maximum size of a sensor to emulate is 512×512 pixels resulting in 8 parallel readout channels. Moreover, the PRE has to be able to generate signals corresponding to the FD with 64×64 pixels which will be

readout in two halves resulting in two parallel readout channels. Special cases like window mode (see section 2.4) and emulation of the whole LDA should be possible. In addition, the various sensors can be operated in a varying readout time per line. The PRE instrument has to be defined to generate the output data stream with adjustable frequency.

Programmable scientific input
Another requirement for the PRE is that the scientific input of the instrument shall be controllable. That means, it shall be possible to specify different observation scenarios with varying photon rates and energies, as well as spatial and timing distribution. The ranges of photon rate, energy and timing need to be adapted to the WFI observation scenarios, which differ in the energy range and count rate capability stated in table 2.1. Moreover, particle traces need to be implemented as they underlie special treatment in the on-board processing. Emulation of realistic data shall be achieved but not limited. For reasons of testing and debugging, generation of uncommon data should also be considered. This simplifies error handling and realization of integrity check of data and results regarding the signal processing chain.
Despite of generation of scientific input data by the PRE, so-called fits files, generated for instance by simulations with the SIXTE software will serve as input signals [31].

Real-time operation
Real-time capability is an indispensable feature of the PRE as the generated signal output shall exactly match the original output of the FEE. The required processing times per frame can be directly obtained from the relevant science requirements. Therefore, two different processing times per readout channel are necessary. The emulated signal of the LD needs to be generated with a frame rate of $200\,\mathrm{fps}$, respectively a pixel time of approximately $150\,\mathrm{ns}$. The emulation of the FD should be generated with a frame rate of $12\,500\,\mathrm{fps}$, resulting in a pixel time of approximately $40\,\mathrm{ns}$.
For reasons of test and debugging, but also to ensure flexibility of design, higher and lower frame rates should be possible. Therefore, the target pixel time for the LD and FD is $40\,\mathrm{ns}$, equivalent to a pixel clock of approximately $25\,\mathrm{MHz}$ per output channel.

Modeling of adjustable detector characteristics
Another important requirement is the modeling of variable characteristics of the detector system. This includes the modeling of readout modes, properties of the sensor, for instance amplification and full well, characterization of noise or modeling of bad pixels. Furthermore the characteristics of the FEE shall be mapped, for instance gain, saturation and channel offset. All controllable parameters should be variable over a specified range in order to emulate various effects.

Sub-pixel resolution
As the pixel signal is represented by the detector by an analog signal, it has a transient response and a certain noise. The pulse shape of an individual pixel signal at the output should be controllable in order to achieve a so-called sub-pixel resolution. To model a realistic pulse shape, several sampling points within a pixel period need to be inserted. According to measurements of the analog output of the detector depicted in 5.7, an updated sample is needed every $2.5\,\mathrm{ns}$ to describe the pulse shape in a realistic way. This results in an oversampling of each pixel by a factor of 16 and a sampling frequency of $400\,\mathrm{MHz}$.

Accuracy of output signal and reproducibility
In order to use the PRE as a suitable instrument for an end-to-end verification, it has to be ensured that the generated analog output signal exactly corresponds to that of the detector. The error caused by the emulation of the analog signal has to be kept as small as possible. Therefore the signal needs to be generated with a higher bandwidth than the real detector signal. Moreover, the resolution of the generated output signal has to be higher than the resolution of the converter stage of the DE, see section 5.2.3. To investigate specific test cases, the analog output signal has to be reproducible.

Interfacing to flight hardware
For the test with the flight hardware it has to be ensured that the connected flight instruments are not damaged during operation with the PRE by out of range signals. Suitable electronic circuits need to be designed and implemented in the PRE to prevent possible damage to all connected instruments. The interfaces to the flight modules have to be implemented with space qualified components.

6.2. Investigation of different Emulation Concepts

The main requirement for the PRE is the interactively controllable generation of scientific data according to the output of the WFI DEPFET detector.
In the following, various architectures and processing platforms are presented and analyzed whether they can be used for the PRE system and accomplish the above stated requirements. To achieve best system performance, the implemented processing algorithms need to be adapted to the respective processing architecture. The results from this investigation are used for the definition of the system architecture of the PRE.

In order to select a suitable concept, a rough estimate is performed to get an idea of the necessary computational power and memory requirements. To calculate the signal of

one pixel, several mathematical operations and instructions need to be done. These operations are additions, multiplications, divisions, sorting algorithms, non-linear operations such as building the square-root or convolution of signals. Moreover, a large number of memory accesses is necessary to process the pixel data. A rough estimate of approximately 200 instructions and 100 arithmetic operations per pixel can be given. Moreover, look-up-tables and interim results need to be stored in a memory. Its size can be estimated for an observation time of $10\,\mathrm{s}$ with the LD to $33.6\,\mathrm{Gbit}$.

Microcontroller or digital signal processors (DSPs) could be used for the definition and processing of the digital data stream. Generation of the analog output signal could be achieved with implementation of DACs.
To calculate the scientific signal and the detector effects, a large number of computations is needed, requiring a huge amount of memory for storage of interim results, as described above. Modern multi-core DSPs have up to $8000\,\mathrm{MIPS}$ and can perform up to 32 $16\,\mathrm{bit} \times 16\,\mathrm{bit}$ multiplications per clock cycle. This would result with the above estimations to a pixel time of approximately $30\,\mathrm{ns}$. This pixel time is too high for the required sub-pixel resolution which requires an update of the sample every $2.5\,\mathrm{ns}$. Furthermore, interfacing peripherals like external memory or DACs could be limited by the number of I/Os provided by general purpose microcontroller or DSPs.

Another approach is to implement the generation of the scientific data stream on an FPGA and output it with DACs. This concept guarantees a real-time behavior but is also very demanding in the implementation of complex image processing algorithms. Memory interfacing can be time critical and can lead to bottlenecks in the design when it comes to high speed applications. Simulation, test and debugging of the implemented functions can be challenging and time consuming. Moreover, maintenance and extension of the source code is ambitious and may be limited by hardware resources which leads to an inflexible design.

A further method is to use arbitrary waveform generators. These instruments can generate data streams of long sequences with high sample rates (up to 12 GSPS). The data stream is calculated offline on a standard Central Processing Unit (CPU) computation platform to make use of sufficient processing resources. This can be performed with a high-level language like Python, C++ or Java. Advanced numerical analysis packages like Matlab, SciLab or GNU Octave could also be utilized. The use of available image processing libraries can decrease complexity and speed up development time. Offline processing of the data stream facilitates system debugging and assessment of interim results. The generated data can be easily stored, enabling the reproducibility of the data.

Nevertheless, the use of arbitrary waveform generators are not applicable to be applied as PRE. The most efficient tools at present, are limited in resolution, memory and output channels. In addition, changes and adjustments to the hardware are hardly possible. Thus the high requirements on the PRE cannot be fulfilled.

The best suitable solution for the PRE design is a combined design of software and hardware. The modeling of the detector system and thus the generation of the digital data stream is performed offline on a Personal Computer (PC) to make use of high processing power. This data stream is then further processed by an FPGA-based platform with DACs to output an analog signal and to ensure real-time behavior. A detailed description of the implemented concept is outlined in section 6.3.

6.3. HW/SW Codesign

The concept chosen for the PRE is a shared design of software and hardware. The simulation of the scientific data stream including the detector modeling and generation of simulated X-ray input data is done in a software package on a powerful state of the art PC. Result of this simulation is a frame stack which equals a measurement of a real DEPFET detector. This data is transferred to a memory on a target hardware including an FPGA for further processing and fast DACs to output an analog data stream. Figure 6.1 summarizes this concept. One PRE instrument shall be able to substitute an LD. In total four PREs are synchronized to emulate the LDA. To build up the FD, one PRE instrument is used in a down-scaled configuration.
A big advantage of the HW/SW codesign is its modularity. Both environments can work separately. On the one hand, the simulation environment can be used to create digital frame data and to study and analyze special modeled effects. On the other hand, the hardware setup of the emulator can be fed with already simulated data without the need of performing time consuming new simulations of frame stacks.

6.3.1. Concept of Modeling

The aim of detector modeling is to generate a digital user-defined frame stack, which equals the one of a real measurement.
In the field of X-ray astronomy, there is a large number of different mission specific simulation programs. These simulations are focused on the modeling of the entire telescope and the performance effects on the astrophysical observations. The input of these simulations is usually an X-ray source description. They are based on models

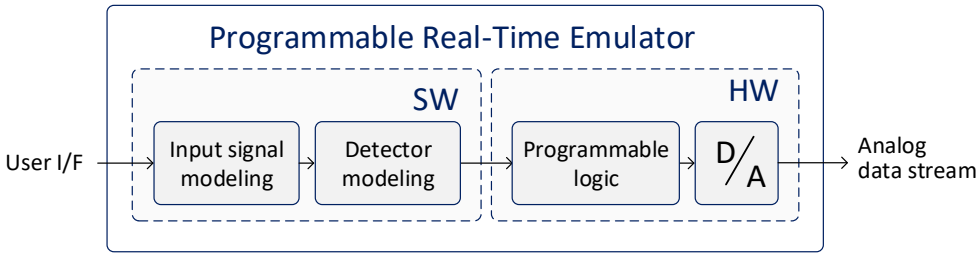


Figure 6.1.: Architecture of the PRE consisting of a software part for simulating signal input and detector characteristics and a hardware part for emulating the signal in real-time.

comprising the imaging process with the X-ray optics and detection in the detector. Output of these simulations is mostly an event list, which can be further processed. In case of Athena's WFI, the mission specific simulator is the SIXTE software package [121].
However, these simulations are less suitable for use in a PRE instrument as the detector model is usually simplified and cannot be influenced by the user. Nevertheless, these simulations can be used as input to the PRE. This can be, for example, a simulation of a faint galaxy, which result is stored as an event list, holding individual detected photon events, time of the detection, and coordinates of affected pixels.

The PRE simulation environment shall comprise mathematical models which describe physical effects and behavior of the sensor and AFE. The model parameters should be adjustable to set different detector and input characteristics. Furthermore it should be possible to set different inputs, regarding photon energy, time and spatial resolution to model realistic scenarios but also to generate extreme or exotic scenarios for special evaluation purposes.

The simplified simulation environment of the PRE is depicted in figure 6.1. Characteristics concerning X-ray input and detector parametrization are defined by the user. All interim results, like event lists or noise maps can be stored for further analysis or later reuse. The output is a digital frame stack calculated and processed according to the defined parameters. The evaluation of the frame stack with the mission specific analysis software and the comparison with the adjusted parameters allows a verification of the modeling performance.

The simulation is performed in MATLAB to benefit from already existing libraries and toolboxes for image processing calculations, fitting algorithms and visualization.

MATLAB internally calculates with arrays and matrices, which fits very well to the pixel- and frame-wise calculations necessary for detector modeling. Processing with MATLAB is only limited by the internal RAM of the PC and a porting to larger systems with more memory and computing power is feasible. MATLAB allows easy debugging, implementation and extension of the source code. All internal signals and used variables are accessible and can be visualized and analyzed in an user friendly way.

6.3.2. Hardware Design

From the requirements listed in section 6.1, the top level hardware requirements can be derived. Table 6.1 summarizes the parameters the PRE platform needs to fulfill.

Table 6.1.: Summary of the top level hardware requirements.

Parameter	**Requirement**
Number of analog output channels	LD: 8 channels FD: 2 channels
DAC resolution	$> 14\,\mathrm{bit}$
Dynamic output range	$V_{min} = -0.8\,\mathrm{V}$, $V_{max} = 2.8\,\mathrm{V}$
Real-time operation	LD: pixel clock = $12.8\,\mathrm{kHz}$ FD: pixel clock = $25.6\,\mathrm{MHz}$
Sub-pixel resolution	oversampling by a factor of 16 sub-pixel clock = $400\,\mathrm{MHz}$

Since the PRE must generate its signals in real-time, only an FPGA-based hardware solution is suitable. The offline generated data is stored in a memory with fast access and adequate size. The FPGA accesses the pixel values stored in the memory and processes them to achieve a so-called sub-pixel resolution, see section 8.1.1. Then, the data is transferred to up to eight simultaneously sampling DACs with appropriate sampling rate. In order to match their output signal to the output signal of the FEE, additional level shifting and common mode adjustment need to be implemented in hardware.
This architecture of the hardware is best suited to be used as PRE as it is programmable and flexibly expandable. Adaptations to future requirements can be carried out well. Multiple platforms can be synchronized with each other, thus covering the whole imaging unit of the WFI. Chapter 8 explains the hardware and firmware design of the PRE in detail.

7. PRE-based Modeling of the Detector System

This chapter describes the modeling of the DEPFET detector system in the scope to use it in the PRE instrument, summarized in section 7.1. Further, scientific input generation comprising modeling of X-ray photons and cosmic particles is outlined in section 7.2. Modeling of timing effects and detector readout is detailed in section 7.3, followed by modeling of the detector characteristics in section 7.4.

7.1. Overview of Modeling Steps

The PRE comprises the modeling of X-ray photons with a particular energy, spatial distribution and hit time. With different parameters corresponding to the detector architecture it is possible to define pixel size, number of pixels and readout channels. Further models of the detector characteristics allow to emulate timing effects like misfits, pile-up artifacts or influences of rolling shutter mode and readout speed. Each pixel can be modeled with a varying offset, common mode and gain per readout channel. The influence of noise can be analyzed by adding thermal, shot and 1/f noise to the signal. Figure 7.1 illustrates the detector models. Each model can be varied in its characteristics or bypassed to study its influence on the output and spectral performance.

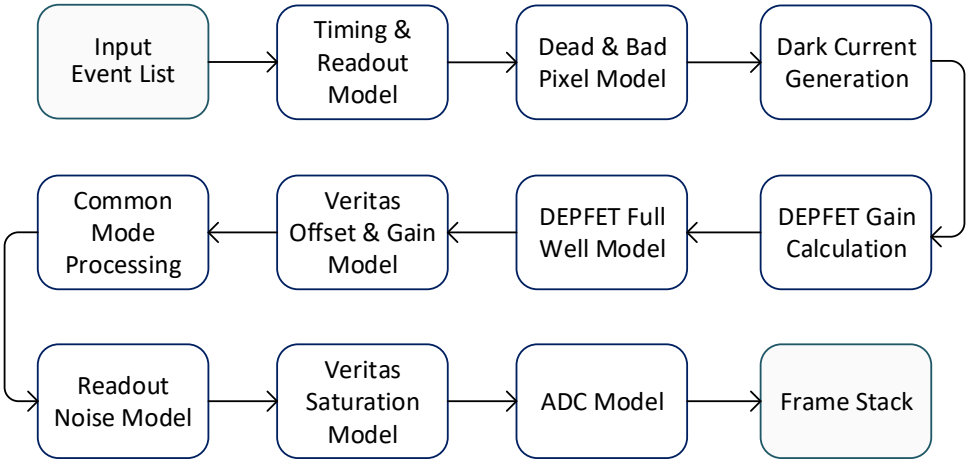


Figure 7.1.: Block diagram of the modeling sequence.

Most models are based on the generation of maps to emulate different effects. These maps are two or three dimensional and have either the size of a frame or the size of the modeled frame stack. The maps are processed with the X-ray input data and all other models. For instance, the DEPFET amplification model is based on a two dimensional gain map including a gain value for each pixel. These maps can be replaced by real measurement data. This allows to adapt the simulation environment of the detector gradually to the latest results.

7.2. Signal Input Modeling

The following section describes the procedure and algorithms of signal input generation. Depending on the configuration, a specific amount of events is created with specified X-ray photon energies, spatial distributions and incident times. The models imply as well modeling of cosmic rays like MIP events. Further, charge splitting over several pixels is entailed.

7.2.1. Modeling of X-Ray Photon Input

The generation of the input data comprises the simulation of X-ray photons with specific energies hitting the sensitive area of the detector at a particular time and a specific spatial position. The modeling of X-ray photons as signal input comprise the following parameters:

- photon rate
- photon energy (mono- or poly-energetic radiation)
- spatial distribution
- timing information

Parameters described above are considered in the input generation model and can be specified and varied.

Photon Rate

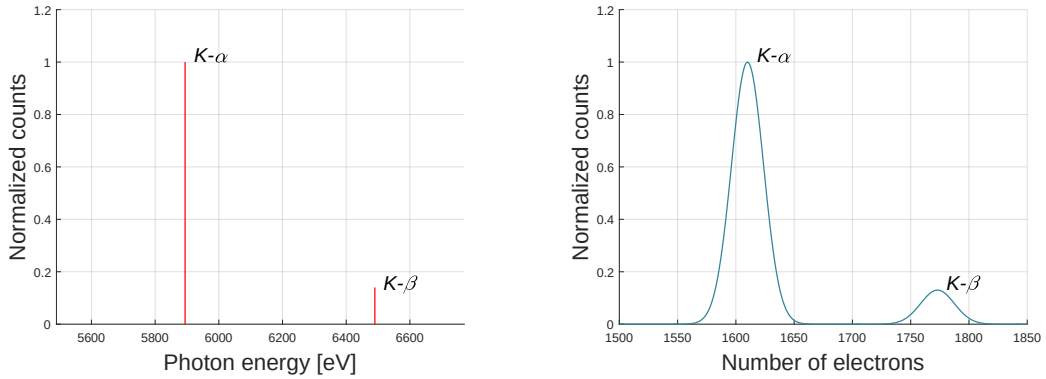
The photon rate is defined as the average number of photons interacting with the silicon sensor per time interval. Depending on the time resolution of the detector, an average number of photons per frame can be specified. To model WFI space observations, the maximum photon rates can be deviated from the WFI science requirements. In order to quantify the brightness of a source and thereby the photon rate, the unit Crab is

used. A Crab is a standard astrophotometrical unit for measurements of the intensity of astrophysical X-ray sources. One Crab is defined as the intensity of the Crab Nebula, an intense space X-ray source, at the corresponding X-ray photon energy [54]. The photon rate depends on the effective area of the Athena mirror configuration. Based on simulations, performed by the SIXTE software [121], a rate of $106\,532$ photons per second can be assumed [21].

To calculate the maximum photon rates, the large and fast detector must be considered separately. Observations with intensities of up to 1 Crab are carried out with the LDA, while with the FD observations with up to 2.5 Crab are performed [64]. With the frame rates given in table 2.1 this results approximately in 530 photons per frame for the LDA and 20 photons per frame for the FD on average.

Photon Energy

For the modeling of the X-ray photon input, the energy of the photons $E_{ph} = h \cdot \nu$ needs to be defined where h is Planck's constant and ν is the frequency of the photon. A distinction is made between monochromatic radiation, which contains photons of a single wavelength and polychromatic radiation comprising photons of various wavelengths. In the latter case, the ratio of the number of incident photons of the individual wavelengths must be considered. Figure 7.2a depicts exemplary the energy lines for an Fe-55 spectrum with Mn-K-α and Mn-K-β peaks. In this case, a ratio of K-β / K-α of 0.14 was assumed.



(a) (b)

Figure 7.2.: (a) Input of energy lines with distribution probability depicted for the example of Mn-K-α and Mn-K-β peaks of the Fe-55 spectrum. (b) Conversion of the photon energy to electrons and convolution with Fano noise.

As explained in section 4.1.3, an interacting photon with energy E_{ph} generates in silicon a number of electron-hole pairs $N = {}^{E_{ph}}/_{\omega}$. This process underlies a statistical variation, called Fano noise. Therefore, the ideal energy lines provoking an average number of electron-hole pairs need to be convoluted with Fano noise. The Fano noise is modeled as Gaussian distribution

$$f(x) = \frac{1}{\sqrt{2\pi\sigma_{FN}^2}} e^{\frac{-x^2}{2\sigma_{FN}^2}} \qquad \text{with} \qquad \sigma_{FN} = \sqrt{F_a \cdot N} \tag{7.1}$$

where σ_{FN} is the variance in multiple electron-hole charge generation, and F_a the Fano factor. The Fano factor is defined as the variance in the number of electrons divided by the expected number of electrons generated per interacting photon [48]. Figure 7.2b depicts the Fe-55 spectrum with influence of Fano noise.

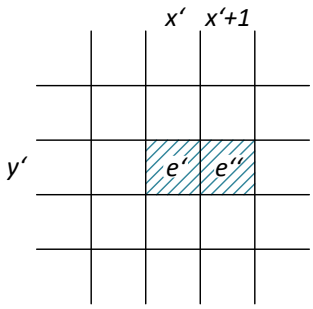
Spatial Distribution

An X-ray photon that hits a sensor can spread its signal charge across one or multiple pixels if the event occurred near a pixel border. These events are called split events and their spatial distribution split patterns. A distinction is made between valid and invalid patterns, see section 7.2.2. Invalid patterns can be caused for example by cosmic particles, pile-up, readout or by data processing effects. For a complete modeling of the spatial distribution of X-ray events on a sensor all these effects are taken into account. The statistics of the spatial distribution of the X-ray photons can be influenced by setting the statistics for split and valid events. Thus a realistic representation of the input data can be modeled. Moreover, by controlling the statistics, modeling of uncommon data is possible.

Timing Information

Every event happens at a specific point in time during observation. Events occurring between or during the readout time need to be considered in a particular way. To do this, every modeled event is tagged with a timestamp. To study the effects of pile-up and misfits the timing information can be set to a distinctive value. Section 7.3.1 describes the further processing of the timing signal in the timing and readout model in detail.

Output of the signal generation model is an event list including the pixel coordinates of affected pixels of all events, stored charge in the pixels and timing information of the event during a frame. With this structure, other inputs like arbitrary test patterns or simulated data from observations can be applied. Figure 7.3 depicts an exemplary event list of a double split event with energy $E = e' + e''$ and timestamp t'.



x coordinate	y coordinate	energy	time
x'	y'	e'	t'
$x'+1$	y'	e''	t'

Figure 7.3.: Exemplary event list of a double split event as shown in the adjacent section of a frame.

7.2.2. Charge Cloud Splitting

As explained in section 4.1.2 an X-ray photon hitting the sensitive medium creates a charge cloud consisting of electron-hole pairs. This charge cloud is separated by the depletion field and the electrons drift towards the sensor front side. The charge cloud is assumed to have an approximately two dimensional Gaussian distribution with an initial size of less than a few micro meters, depending on sensor thickness and operational conditions [58]. By drifting through the sensor, the charge cloud widens due to diffusion and electromagnetic repulsion [53]. When reaching the detector front side the charge cloud has a diameter of less than $100\,\mu\mathrm{m}$. The exact size of the charge cloud at the sensor front side depends on factors like photon energy, drift time and charge carrier mobility [55].

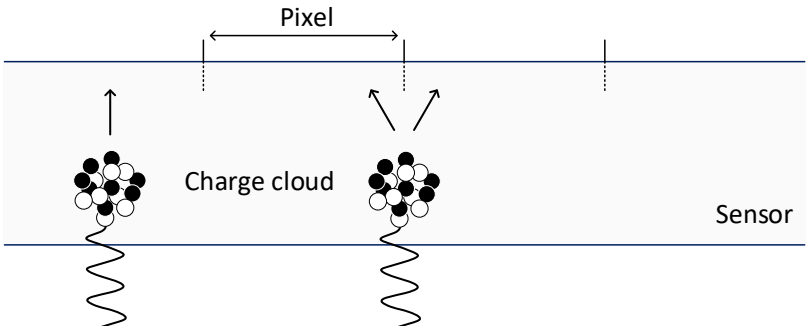


Figure 7.4.: Photons are absorbed in the detector bulk where they generate electron-hole pairs, called charge cloud. The electrons drift towards the detector front side and accumulate in the pixels. According to the impact point, pixel size and charge cloud expansion, the electrons spread up in at least one pixel.

Depending on the lateral incidence point of the photon or the position of the charge

cloud and the pixel edge length, the charge cloud can spread its signal across several pixels, as depicted in figure 7.4. The WFI DEPFET pixels have a pixel edge length of $130\,\mu\mathrm{m}$, this means that the signal can spread up to 4 pixels composing a square of 2×2 pixels.

Adjacent pixels are most likely to have a common origin. These cohesive pixels form a pattern. Patterns, forming a square of 2×2 pixels are denoted as valid patterns. Figure 7.5 shows all combinations of valid patterns. The names of the patterns are defined by the number of pixels involved. The patterns are called singles (SNGs), doubles (DBLs), triples (TRPs) and quadruples (QUDs). Patterns with other shapes are identified as invalid patterns, and referred to as others (OTH). Their shape exceeds a square of 2×2 pixels. A special case is a valid triple pattern, here the pixel with the largest signal fraction needs to be in the center position. Figure 7.6 depicts exemplary a few invalid pattern. Here, a recombination to a common origin is not feasible.

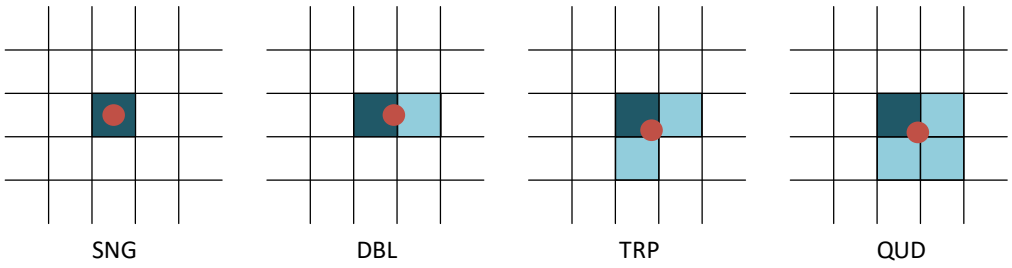


Figure 7.5.: Overview of valid patterns. The photon incident point is marked with a red point, the affected pixels are shown in gray, the respective maximum pixel in black. More valid pattern can be obtained by rotating the pattern around their maximum.

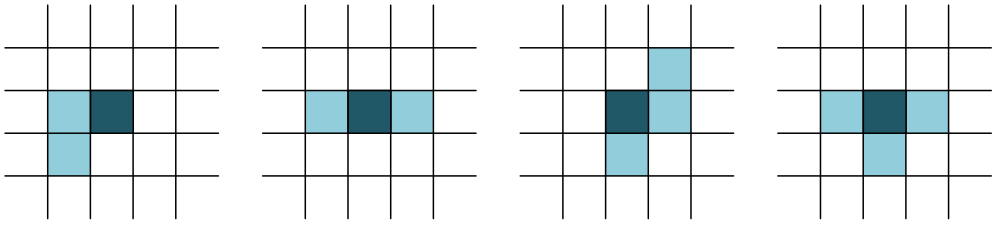


Figure 7.6.: Overview of a selection of invalid patterns. The first pattern is not valid because the maximum pixel is not in the center. In the other patterns, more than 2×2 pixels are affected. Signals from invalid patterns can not be combined to a common source.

The charge distribution of electrons after absorption of a photon is assumed as a two dimensional Gaussian distribution

$$n(x,y) = \frac{Q}{2\pi\sigma_c^2} e^{-\frac{(x-x_0)^2+(y-y_0)^2}{2\sigma_c^2}} \tag{7.2}$$

where σ_c is the size of the charge cloud, Q the number of electrons in the charge cloud and x_0 and y_0 is the point of absorption within a pixel. Depending on the distance of the absorption point to the next pixel edge, a part of the charge is detected in the adjacent pixel. The remaining charge in the pixel, generated within a distance of x_0 from the pixel border, can be calculated to [82]

$$q(x_0,y_0) = \frac{Q}{\sqrt{2\pi\sigma_c^2}} \int_{-a/2}^{a/2}\int_{-a/2}^{a/2} e^{-\frac{(x-x_0)^2+(y-y_0)^2}{2\sigma_c^2}} dxdy \tag{7.3}$$

with a being the length of a pixel edge. Assuming that the charge cloud is split only in one direction, the result of this integration in one direction can be set to 1. This leads to a simplified equation

$$q(x_0) = \frac{Q}{2}(1 + erf(\frac{a/2 - x_0}{\sqrt{2\sigma_c^2}})). \tag{7.4}$$

With equation 7.4 the distribution of charge among two pixels in dependence of absorption point x_0 can be calculated.
Figure 7.7 depicts the splitting distribution of $1 \cdot 10^6$ events within two adjacent pixels and referred to as η-function. On the x-axis, the ratio of a split fraction $q(x_0)$ of an event to its total charge Q is shown. It can be seen that the probability for a double event with equal charge in its split pattern is the smallest. The modeling of double split events is based on this charge cloud distribution function. Distribution for triple and quadruple split patterns are derived from this distribution.

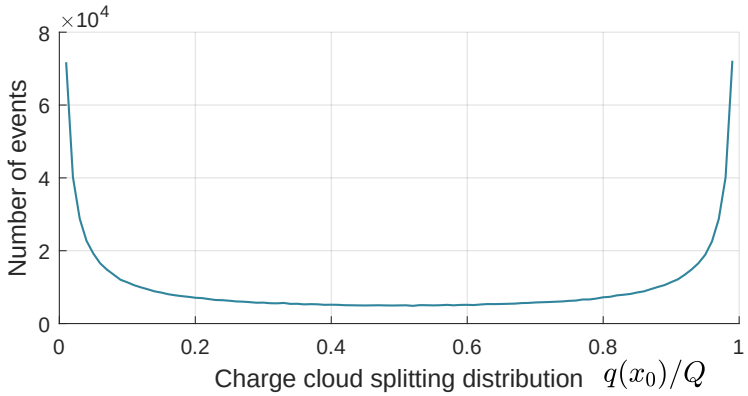


Figure 7.7.: Charge cloud splitting distribution function within two neighboring pixels.

7.2.3. Particle-induced Background

X-ray detectors operated in space are exposed to the whole spectrum of cosmic particles. Cosmic particles contribute to the background of the instrument. Instrument background is composed of low energetic electrons, protons, heavy ions, Compton electrons generated by X- and γ-ray photons, X-ray fluorescence radiation stimulated by the charged particles traversing the entire instrument and Minimal Ionizing Particle (MIP) [101]. MIPs can be separated from X-ray photons on-board to reduce instrument background and data rate.

MIPs deposit a large amount of charge compared to X-ray photons along their track through the sensor volume, see section 4.1. The amount of generated charge depends on the length of the trace and the incident angle between the particle and the sensitive volume. The stopping power in silicon can be approximately given to $dE/dx = 3\,\mathrm{MeV/cm}$. That means, a MIP traversing through the sensor leaves approximately 80 electron-hole pairs per $\mu\mathrm{m}$ in the silicon. Corresponding to their incoming direction, MIPs can deposit their charge in one up to several pixels. It can be assumed that an ionizing particle affects on average ten adjacent pixels [102]. For example, a particle passing $2\,\mathrm{mm}$ through the sensor material, deposits approximately $600\,\mathrm{keV}$. This corresponds to $2.7 \cdot 10^6$ electron-hole pairs, assuming an electron-hole pair creation energy of $3.70\,\mathrm{eV/e}$. In L-2 orbit, the rate of MIPs hitting the sensor can be roughly estimated to a number of $2\,\mathrm{MIPs/cm^2/s}$. This leads to a MIP rate per frame for the LDA of roughly $1.7\,\mathrm{MIPs/frame}$ and for the FD of $0.1 \cdot 10^{-3}\,\mathrm{MIPs/frame}$ assuming the sensor geometry and timing listed in table 2.1.

In order to model the interaction of ionizing particles with the DEPFET sensor, some assumptions were made.

- The trace of the particle follows linear function.
- The mean energy loss rate of each particle is similar and constant over the complete trace.
- The distribution of the length of the trace follows an exponential distribution with an average value of ten pixels.
- The coordinates of the starting point and the angle of the particle trace is randomly distributed over the sensor area.

Figure 7.8 schematically shows the modeling process of events generated by massive cosmic particles. A linear trace of a particle is calculated with a random pixel coordinate as starting point $(x^{'}, y^{'})$ and end point $(x^{''}, y^{''})$. The calculation of the end point assumes

an exponential distribution of the length with an distinctive average value. The trace results to

$$f(x) = y = \frac{y'' - y'}{x'' - x'}(x - x') - y' \tag{7.5}$$

with x and y being the column and row pixel coordinates. The length l_T of the modeled particle trace can be calculated with a quadratic pixel size with edge length a_p to

$$l_t = \sqrt{(x'' - x') + (y'' - y')} \cdot a_p. \tag{7.6}$$

When the particle transverses the sensor, charge is generated in the pixels along the trace but also in the neighboring pixels. This can be modeled by a convolution of the particle trace, see equation 7.5, and a 2-D Gaussian filter

$$G(x, y) = \frac{1}{2\pi\sigma^2} e^{-\frac{x^2+y^2}{2\sigma^2}}. \tag{7.7}$$

The Gaussian filter works with a 2-D distribution as point spread function. Theoretically an infinitely large convolution kernel would be needed as the Gaussian distribution is non-zero. Approximately 99% of the distribution falls within three sigma of the mean, thus the kernel size of the convolution can be limited.

The discrete convolution for two-dimensional functions, e.g. digital images, is defined as

$$I^*(x, y) = \sum_{i=1}^{n} \sum_{j=1}^{n} I(x + i - a, y + j - a)k(i, j) \tag{7.8}$$

where $I^*(x, y)$ is the resulting pixel, I is the image on which the filter is applied, a is the center coordinate of the quadratic convolution kernel and $k(i, j)$ represents an element of the convolution kernel.

The deposited energy of a MIP event in the sensor material and thus the number of created electron-hole pairs depends on the length l_T of the particle trace and the stopping power dE/dx

$$E_P = l_T \cdot \frac{dE}{dx}. \tag{7.9}$$

Distribution of the energy E_P over the modeled MIP trace $I^*(x, y)$, see equation 7.8, leads to a complete model of an MIP event.

Regarding the background reduction, MIP events need to be identified and filtered. The MIP rate in the Athena orbit is very high, thus MIP events cannot be transmitted to ground as they would overload the downlink rate. Therefore, sophisticated processing

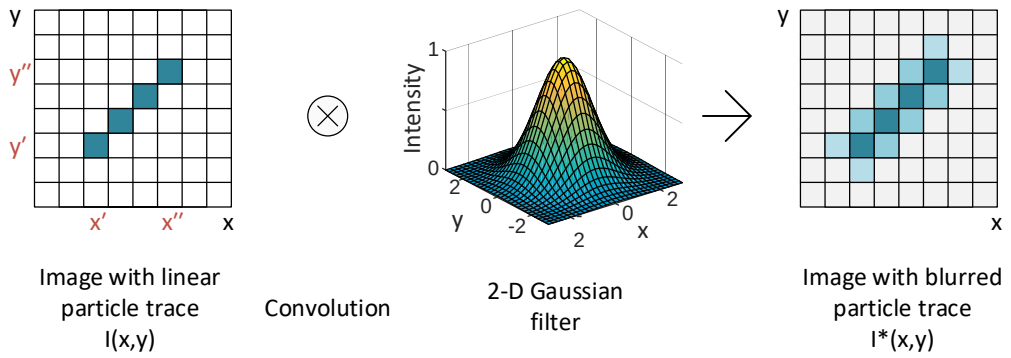


Figure 7.8.: Schematic process of modeling particle traces shown for a 8×8 pixel matrix. Gaussian blurring is used to generate low energetic events along the particle trace.

on-board is necessary to identify and discard these events.
In laboratory environment, processing of MIP events in the on-board processor can hardly be tested. MIPs can be generated with accelerators of elementary particles, having the disadvantage of limited experimental time and high cost. In laboratory conditions, it is possible to use some beta emitters such as Sr-90 or Y-90. Nevertheless, a complex experimental test setup and a handling with radioactive sources would be necessary.

With the PRE, it is possible to model and generate test stimuli with MIP traces. Thus, the complex on-board data processing algorithms and strategies for MIP rejection can be completely tested and verified.

7.3. Readout and Timing Modeling

The WFI DEPFET sensors are read out row-wise in a rolling shutter mode. The accumulated signal is measured by so-called correlated double sampling. Two integrations of the signal, before and after charge removal from the pixel are taken. The difference of these two integrations is returned as pixel signal. Incident photons, hitting the detector during the readout time can lead to incomplete charge detection and thus to misinterpretation of photon energy. The readout model considers the effects of processing the matrix in rolling shutter mode, charge integration and removal as well as incomplete charge removal during clear process.

7.3.1. Timing and Readout Effects

Modeling of the timing effects is based on the detector readout sequence presented in section 5.1.1. Processing of a DEPFET pixel is separated in an accumulation phase and readout phase. The readout phase consists of a first integration, a clear and a settling time as well as a second integration. For this model the first settling time belongs to the accumulation phase.

Figure 7.9 depicts the influence of the DEPFET readout sequence on the measured charge and the charge remaining in the pixel. It is assumed that a photon generates a charge q_0 at different times of the readout sequence. Depending on the photon incident time, the complete signal input q_0 or only a fraction is measured. Further, the complete charge or only a part of the charge accumulated in the pixel is cleared. Table 7.1 summarizes the implemented functions for the different phases of processing a pixel in dependence of the point in time of charge deposition t_{hit}.

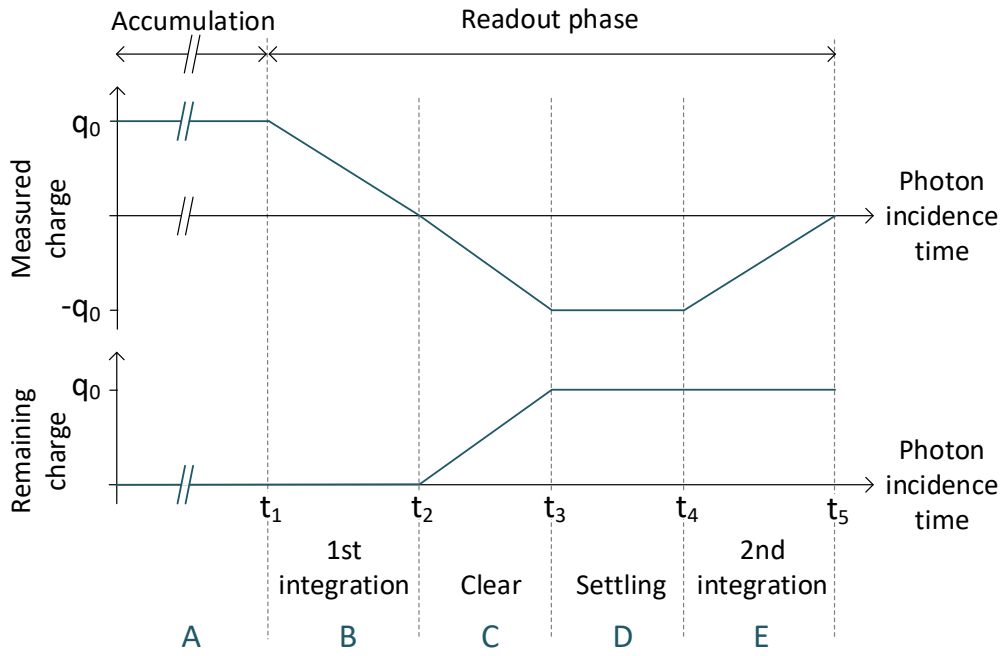


Figure 7.9.: Readout of a DEPFET pixel. Depending on photon incidence time, the complete charge input q_0 or only a fraction can be detected. Further, the charge of photons hitting the sensor during or after the clear process is stored in the pixel until readout of the next frame.

Table 7.1.: Summary of the functions describing the influence of the readout sequence on the measured charge and remaining charge in a pixel. In this model a linear function for integration and clear process is assumed

	pixel processing phase	incidence time	detected charge in actual frame	remaining charge until next readout
A	accumulation	$t_{hit} \leq t_1$	$q = q_0$	$q' = 0$
B	1st integration	$t_1 < t_{hit} \leq t_2$	$q = q_0 \frac{t_{hit}-t_1}{t_1-t_2}$	$q' = 0$
C	clear	$t_2 < t_{hit} \leq t_3$	$q = q_0 \frac{t_{hit}-t_2}{t_2-t_3}$	$q' = q_0 \frac{t_{hit}-t_2}{t_3-t_2}$
D	settling	$t_3 < t_{hit} \leq t_4$	$q = -q_0$	$q' = q_0$
E	2nd integration	$t_4 < t_{hit} \leq t_5$	$q = q_0 \frac{t_{hit}-t_4}{t_5-t_4}$	$q' = q_0$

In the following, the influence of the incident time t_{hit} on the detected signal is summarized. The readout sequence is separated in five time slots A-E.

Normal charge deposition (A)
A photon hitting the sensor during accumulation phase leads to a complete detection of the deposited charge q_0 in the internal gate. The complete charge is removed by the clear process.

Charge deposition during first integration (B)
If the charge is deposited during the first integration of the signal, probably only a fraction of the charge is detected, depending on the point in time of the photon hitting the detector. This incomplete detected event is called a positive misfit.

Charge deposition during clear (C)
A charge deposition during the clear of the internal gate can lead to signal loss, depending on point in time of arrival. If the charge is deposited at the very beginning of the clear phase it is most likely that the charge is completely removed. If it is deposited at the end of the clear process, a larger fraction of the charge remains in the internal gate until the next readout of this pixel. Thus it will be detected in the next frame.

Charge deposition during settling time (D)
A photon hitting the sensor during settling time results in a negative signal, as the difference of the two integrations delivers a negative result. As the clear process already took place, the charge is stored in the pixel until the next readout. It will be detected in the next frame. This type of signal is called a negative misfit.

Charge deposition during second integration (E)
Charge deposition during second integration leads to negative misfits with an incomplete detection of the photon energy. Depending on the point in time of the deposition, only a fraction of the charge is integrated. The difference of the two integrations results in a negative signal. As the charge was not removed from the internal gate through a clear pulse, it remains until the processing of the next frame, where it is recognized as normal event.

The probability p_{misfit} of a photon hitting the detector during readout and thus leading to a misfit event is given to

$$p_{misfit} = \frac{t_{readout}}{t_{acc} + t_{readout}}. \tag{7.10}$$

This leads to a probability for misfits of approximately $3.1\,\%$ for the FD assuming a readout time per row of $2.5\,\mu s$ and $0.2\,\%$ for the LD with a readout time of $10\,\mu s$ per row.

Rolling Shutter Mode

The WFI DEPFET matrices are read out in a rolling shutter mode, introduced in section 5.1.2. Within the readout model, a time-shifted readout phase row-by-row is implemented. Figure 7.10 illustrates the processing of two rows in rolling shutter mode with accumulation and readout phase. Three different time slots for arriving photons are analyzed. The rolling shutter mode only influences the signal of photons depositing their energy in two vertical neighbor pixels, called vertical split events. In the case of the Athena WFI sensors with given pixel size, this occurs for vertical double, triple, and quadruple split events. All consequences of this readout mode are listed in table 7.2.

The probability p_{rs} for a vertical double, triple or quadruple split event is influenced by the rolling shutter mode and can be described by

$$p_{rs} = \frac{2 \cdot t_{readout}}{t_{acc} + t_{readout}}. \tag{7.11}$$

This results in a probability for vertical split events affected by the rolling shutter mode of approximately $6.3\,\%$ for the FD assuming a readout time per row of $2.5\,\mu s$ and $0.4\,\%$ for the LD with a readout time of $10\,\mu s$ per row. These statistical values are independent of the photon rate of observed sources.

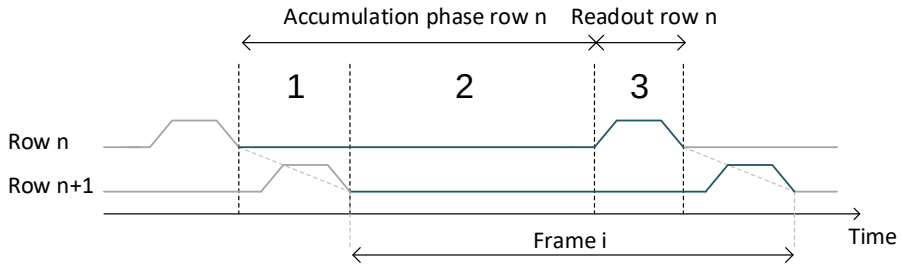


Figure 7.10.: Schematic diagram of processing of two rows in rolling shutter mode. The readout phase of the rows are shifted in time.

Table 7.2.: Effects on vertical split events due to rolling shutter readout mode.

Time	Effect
1	• normal detection of charge in row n • misfit of charge in row n+1 • effect on frames: possible detection of charge in row n+1 in frame i-1 (inter-frame split event)
2	• normal detection of charge in row n and n+1 • no effect on frames
3	• misfit of charge in row n • normal detection of charge in row n+1 • effect on frames: possible detection of charge in row n in frame i+1 (inter-frame split event)

Pile-up

Pile-up occurs when photons hit the same pixel or neighboring pixels during the readout time of one frame. In this case, their generated charge adds up, and they form a pattern together. This either results in a valid or an invalid pattern. In the implemented pile-up model, however, this effect is reproduced with only two photons. Depending on pile-up statistics the charge is distributed either as a valid or invalid pattern.

7.3.2. Clear Correlations

To obtain the signal of a single pixel, the difference of a pixel with filled internal gate and emptied internal gate is taken. Usually after the readout the pixel is reset to start a new acquisition. But there are some pixels which hold some signal after a primary signal was removed without a new deposition of charge in the pixel. This is caused due to an incomplete clear of the charge in the internal gate. A certain part of the primary signal remains in potential pockets of the internal gate. This residual charge is added to the next frames, called follow-up frames. The presence of signal in the pixels from previous frames is also called image lag.
The reasons for the occurrence of clear correlations is still under discussion. A possible explanation is resistivity fluctuations within the silicon crystal [55].

The measured primary signal in the first frame is lower than the signal corresponding to the induced electrons. To obtain the complete signal, the amplitudes of the signals in the follow-up frames have to be integrated. Figure 7.11 illustrates a readout of a pixel with incompletely cleared internal gate within two subsequent frames.

The measured signals in the follow-up frames can be described with the exponential function

$$A(f, A_0) = A_{\max} \cdot e^{-f/\tau} \cdot \left(1 - e^{-A_0 \cdot \nu}\right) \tag{7.12}$$

where A is the amplitude of the measured signal in the follow-up frames f, with the primary signal A_0 deposited in the internal gate. A_{max} is the total amount of charge, which can be stored in the potential pockets. The time constant τ is a factor to describe the exponential decrease of charge in the pockets in the following frames and the slope ν is a factor to describe how the potential pockets fill up depending on the amount of charge in the internal gate.

Figure 7.12 shows a clear correlations sequence for five follow-up frames. The pixel amplitude in electrons is shown as well as the clear correlations amplitude in electrons which is the signal after readout of each follow-up frame. The primary signal is not shown.

To model the effect of clear correlations, the function 7.12 is implemented. The number of pixels, affected by clear correlations can be adjusted. The parameter A_{max} is mapped to an exponential function, shown in equation 7.13

$$A_{max}(x) = \lambda \cdot e^{\frac{-x}{\lambda}} \tag{7.13}$$

with λ setting the slope of the exponential function. Moreover, the minimum and maximum value for A_{max} can be configured. A pseudo random process selects the

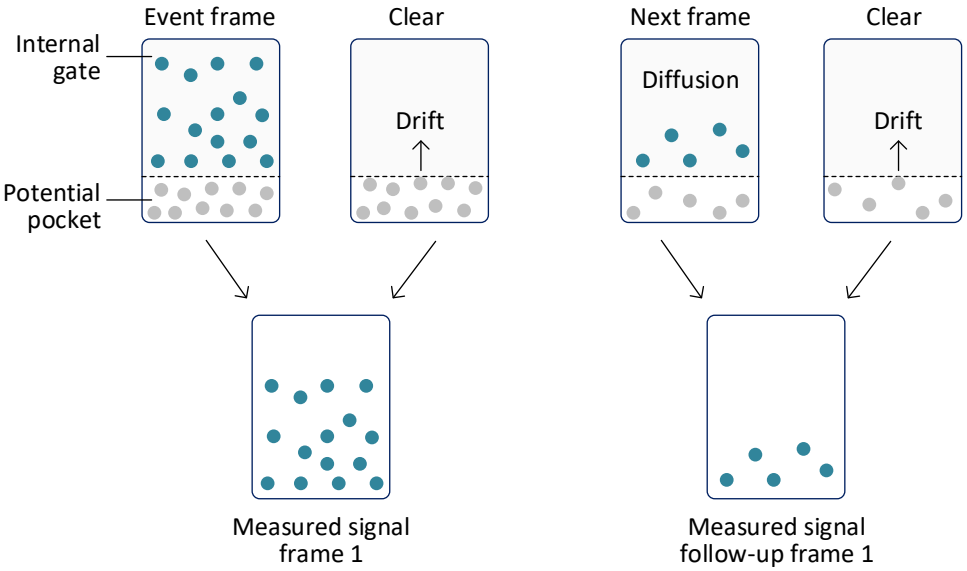


Figure 7.11.: Schematic illustration of a readout of a pixel with incompletely cleared pixel. An incident photon generates charge in a pixel. A fraction of this charge is trapped in a potential pocket of the internal gate. After the clear process, most of the generated charge is removed, but a fraction is stored corresponding to the size of the potential pocket. Thus the measured signal is smaller than the signal generated by the incident photon. In the next frame, some of the trapped charge carriers move due to diffusion and generate a measurable signal. Thus, the total generated charge is read out over several frames.

coordinates of the affected pixels. It can occur that during a follow-up frame another photon hits the pixel. Then the remaining charge adds up with the latest generated charge. This kind of pile-up is also included in the clear correlation model.

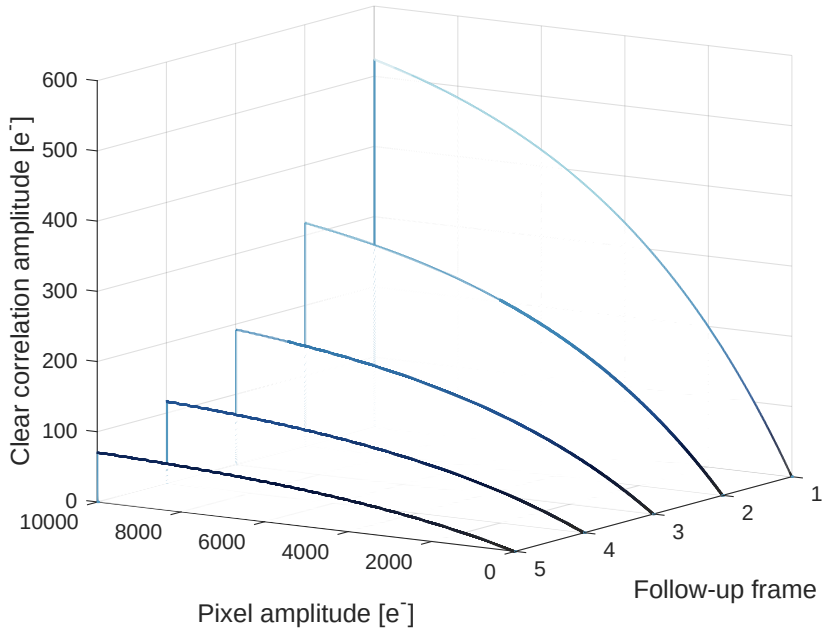


Figure 7.12.: Exponential sequence of clear correlation signals. The signal amplitude in electrons for five follow-up frames is shown in dependence of the pixel amplitude of the primary signal A_0.

7.4. Modeling of Detector Characteristics

The following models describe the detector characteristics. They comprise the detector architecture, DEPFET and AFE properties and performance, noise contributions as well as occurrence of bad pixels. The models are defined to simulate a realistic behavior of the detector. By predicting the detector characteristics based on detector prototype measurements, the models can be parametrized to generate corresponding frame data of the WFI detectors.

7.4.1. Detector Architecture

The geometrical properties of the sensor and associated readout electronics are described in the detector architecture model. Any size of the sensor can be generated to ensure a flexible configuration. The size of the sensor is determined by the number of lines and columns. The number of used Veritas ASICs is calculated from the given sensor size. This flexible design enables the adaption of the models to future requirements or further developments of the system.

In order to model the detector architecture of the WFI LD a configuration based on 512×512 pixels is used. The frame is divided in 8 channels, with each channel being assigned to an individual readout ASIC. For the fast sensor, a readout in two halves is specified. This doubles the number of modeled readout ASICs.

7.4.2. Bad Pixel Model

Some pixels in a sensor matrix can show erroneous behavior. These pixels are outliers or defects in the matrix and are called bad pixels. They are caused for instance by manufacturing impurities, degradation of the sensor or radiation damage. Bad pixels can be classified as follows:

- **Noisy pixel:** A noisy pixel presents a considerably higher noise than its surrounding pixels.
- **Bright pixel:** A bright pixel has a significantly higher gain than its neighboring pixels. Bright pixels can only be seen at the presence of radiation illumination.
- **Hot pixel:** A hot pixel presents an extremely large offset, for example due to excessive dark current. Typically, a hot pixel has a dark current which is 10 times higher than the average dark current [44]. Hot pixels can be seen without illuminating the sensor.
- **Dark pixel and dead pixel:** A dark pixel is a pixel with very low sensitivity to illumination intensity variations. Its gain is very low compared to the average pixel gain resulting in darker spots in an image. A dead pixel is non responsive to illumination.
- **Defective pixel cluster:** A cluster defect is a group of pixels with pixel defects, most likely complete rows or columns of a sensor matrix are affected.

Bad pixels are modeled by generating their effects. For noisy pixels this is performed in the noise model, see section 7.4.6. The occurrence of bright, dark and dead pixels depends on the gain of the matrix and are thus covered by the gain model, described in section 7.4.4. The presence of hot pixels is due to higher dark current and can be generated in the dark current model, explained in section 7.4.3.

7.4.3. Dark Current and Hot Pixel Calculation

Dark current, also called leakage current, is caused due to the thermal generation of electrons and scales with exposure time and temperature, see section 4.2.3. The

dark current increases roughly exponentially with the temperature. The higher the temperature, the higher the leakage current, and thus the shot noise [97].

For DEPFET devices the measured dark current is around $0.3\,\mathrm{nA/cm^2}$ to $2.3\,\mathrm{nA/cm^2}$ at $300\,\mathrm{K}$. According to equation 4.26 and a pixel size of $130\,\mu\mathrm{m} \times 130\,\mu\mathrm{m}$ a dark current up to $5.0 \cdot 10^6$ electrons per second and pixel can be assumed. This leads to problems in the average signal and noise. The dark current can be influenced by changing the temperature.

When images are recorded, some pixels can be observed that appear much brighter than surrounding pixels. These pixels are referred to as hot pixels. Such pixels are mainly caused by charge generation centers within the image sensor chip due to manufacturing inaccuracies. Although the location of the hot pixels are randomly distributed within the sensor, they are in a fixed position.

To model this influences, a mean value of dark current noise in units of electrons is generated, based on the inputs of pixel size, exposure time, temperature and dark current rate. The statistical fluctuation of dark current noise is modeled with a normal distribution, to generate different values of dark currents for each pixel in each frame. The model of dark current noise also covers the presence of hot pixels. Therefore a hot pixel map is implemented which is multiplied with the dark current map. The multiplication factors of the hot pixel map can be set with an exponential distribution. Figure 7.13a shows the modeled dark current for one frame assuming a temperature of 240 K and an exposure time of 5 ms per pixel. A hot pixel map, see figure 7.13c was applied with an exponential distribution (see figure 7.13d). Figure 7.13e and 7.13f depict the combined result of dark current and hot pixel map for one representative frame.

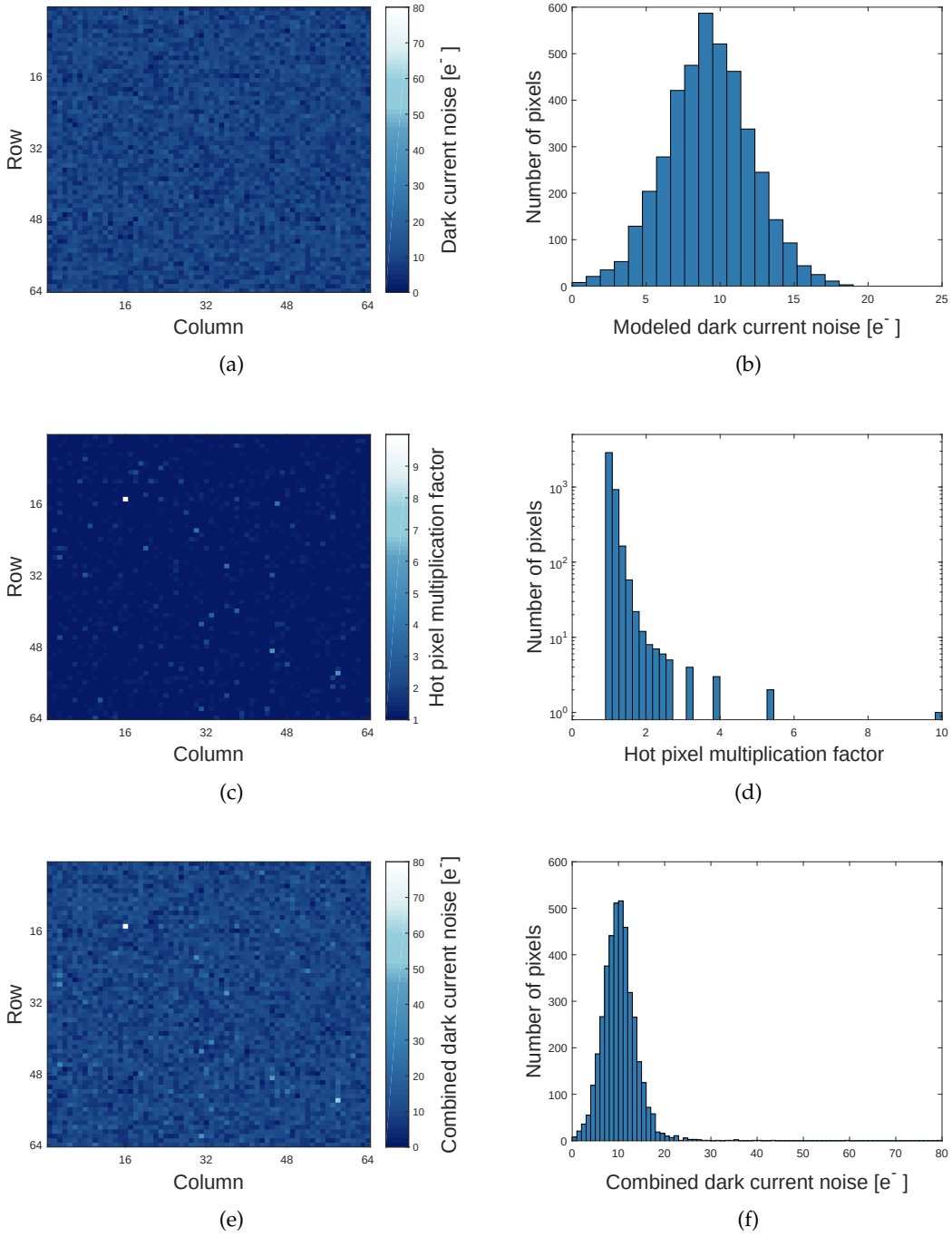


Figure 7.13.: Modeled dark current and hot pixel maps: (a) and (b) Pixel map and histogram of the dark current in electrons of one frame with 64×64 pixels at a temperature of $240\,\mathrm{K}$ and an exposure time of $5\,\mathrm{ms}$. (c) and (d) hot pixel multiplication map and histogram with an exponential distribution to set pixels with a higher dark current than the average pixels. (e) and (f) presents the result of the multiplication of the 2-dimensional hot pixel map and the 3-dimensional dark current map (only one frame is shown).

7.4.4. DEPFET Amplification and Full Well

Each DEPFET pixel consists of a transistor operating as first amplifier in the signal processing chain, as described in section 4.3.4. The amplification is described as transfer function between output signal and stored signal charge in the pixel. The transfer function $f(x)$ of each pixel can be assumed as linear in the range of operation: $f(x) = a \cdot x + b$, with a being the slope and b being the y-intercept. The slope a is defined as $g_D = \frac{\delta U_{GS}}{Q_{int}}$, see section 4.3.4. The y-intercept b is the pixel offset formed by the leakage current, see section 4.2.3.
In the DEPFET amplification model, only the gain g_D is considered, as the pixel offset caused by leakage current is covered already by the dark current model explained in section 7.4.3.

The amplification model describes the ratio of output signal versus stored charge in the pixel. As each DEPFET pixel features individual amplification properties, the sensitivity varies between DEPFET pixels. This sensitivity is assumed to be normally distributed over the whole matrix

$$P(g_{D_{c,r}} \leq x) = \frac{1}{\sigma_{g_D}\sqrt{2\pi}} \int_{-\infty}^{x} e^{\frac{-(t-\mu_{g_D})^2}{2\sigma^2_{g_D}}} dt \tag{7.14}$$

with mean value μ_{g_D} and standard deviation σ_{g_D} giving the dispersion from the mean value per column c and row r. Figure 7.14a illustrates the pixel-wise amplification values of a matrix with 64×64 pixels in the linear region called gain map, the corresponding histogram is shown in figure 7.14b. Figure 7.14c depicts the transfer function of the amplification model with charge input and voltage signal output.

The DEPFET full well describes the maximum charge handling capacity, which is the amount of electrons that can be stored in a pixel without losing any charge to any other node. The pixels of the matrix differ in the maximum number of stored electrons. Therefore, a Gaussian distribution was estimated to model the full well dispersion of every pixel. It is assumed that a DEPFET pixel can store charges up to 1×10^5 electrons, which corresponds to an energy of about $370\,\mathrm{keV}$, which is well above the energy range of X-ray photons.

Figure 7.14d depicts the full well distribution with an assumed mean value of 1×10^5 electrons and standard deviation of 100 electrons.

In general, it cannot be assumed that the variation in amplification is normally distributed. This is only the case, if the variation is totally random distributed, which would neglect any spatial correlation of the variations. For a subsequent and more

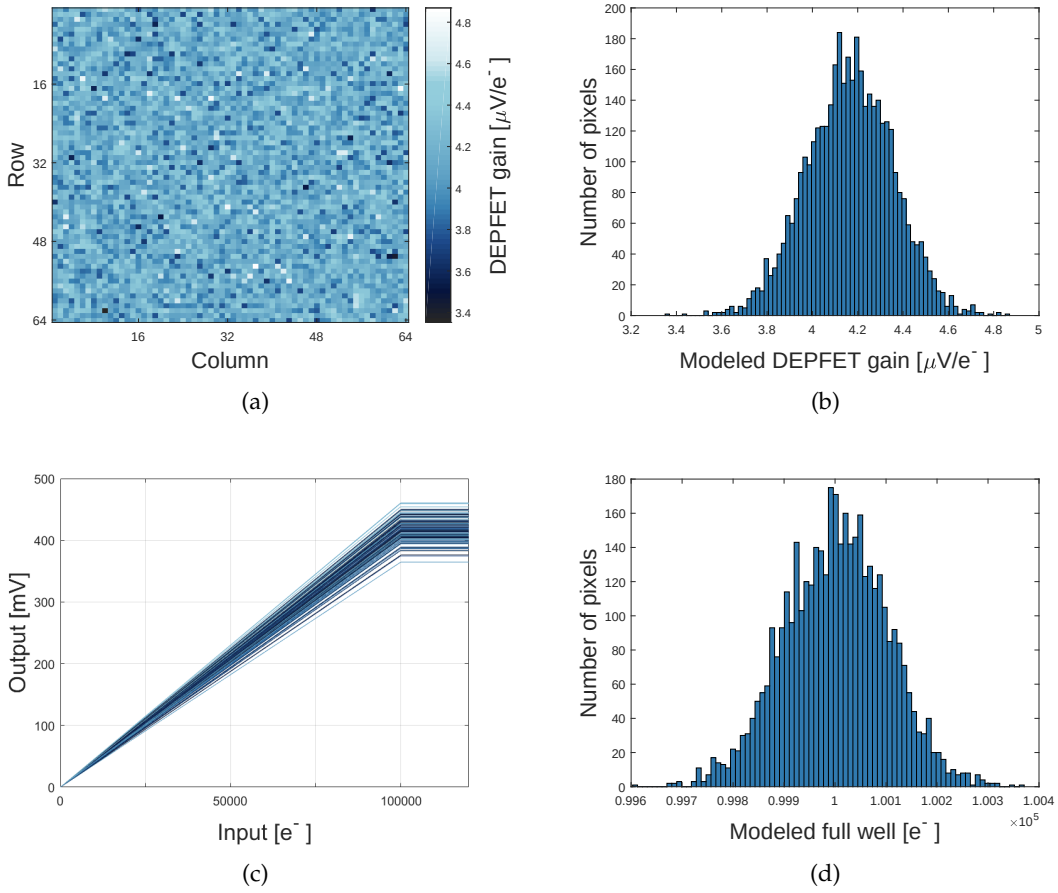


Figure 7.14.: Diagrams of modeled DEPFET characteristics of 64×64 pixels. (a) gain map of a DEPFET matrix (b) histogram of DEPFET gain of all pixels (c) transfer function of representative 128 DEPFET pixels with linear ans saturation region (d) dissipation of full well.

detailed description of the non-uniformity, spatial effects need to be considered. Gradual low-frequency variations over the whole chip due to manufacturing imperfections affect the sensitivity of the device. Moreover outliers can occur. These are single pixels or cluster of pixels that show a significantly deviation from the mean. These pixels are bright pixels, dark or dead pixels, as presented in section 7.4.2. These variations can be measured with an homogeneous irradiation of the device. In order to be able to display outliers due to gain errors, it is possible to load an external gain map. This can be for instance a simulated or experimental measured map.
To model these bad pixels a bad gain map is introduced. This map is multiplied with the original gain map to change the amplification values of individual pixels. For example, a bright pixel can be modeled by setting the corresponding bad gain value

to a value greater than one. A dark pixel can be modeled by adjusting the bad gain value between zero and one. Generation of a dead pixel can be done by setting the multiplication factor to zero which leads to an amplification value of zero.

7.4.5. Modeling of Veritas Characteristics

The DEPFET sensor is read out with the Analog Front-End Electronics Veritas-2, a 64-channel ASIC which performs shaping and amplification of the sensor signal, see section 5.1.3. Differences in the output signal of every channel can occur due to small variations in the characteristics of the semiconductor device. This results in gain and linearity variation as well as divergent offset values per channel. Following effects and characteristics are incorporated in the model:

- Amplification
- Saturation
- Common mode noise
- Channel offset

Figure 7.15 displays a block diagram of the Veritas-2 model with input and output as well as all controllable parameters.

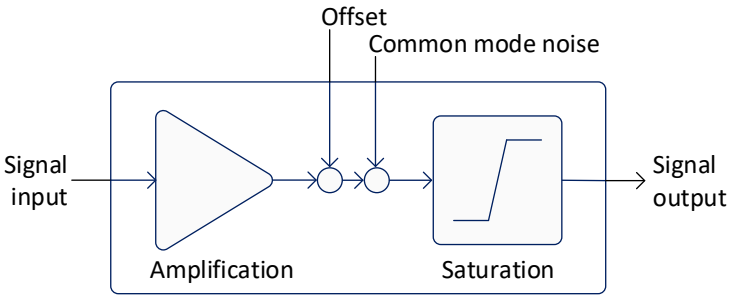


Figure 7.15.: Schematic diagram of the Veritas-2 model with amplification stage, offset and common mode noise addition and saturation stage.

Moreover the readout mode can be chosen between two readout modes: source-follower and drain-current readout. For the LD, eight ASICs are modeled. The FD is readout in two halves, either with one or two ASIC per half. Therefore every parameter of this model can be set for each readout ASIC individually.

Amplification

The amplification of the Veritas-2 ASIC is adjusted in a way that the observed energy range is mapped to the entire output range of the readout ASIC. Therefore the ASIC provides a huge variety of gain configurations, which are considered in this model. The total gain of the readout ASIC g_{V2} is composed of the amplification of the transimpedance amplifier g_{I2V}, preamplifier g_{PRE} and filter stage g_{FILT}, depending on the integration time t_{int}. The amplification of the Veritas-2 can be calculated to

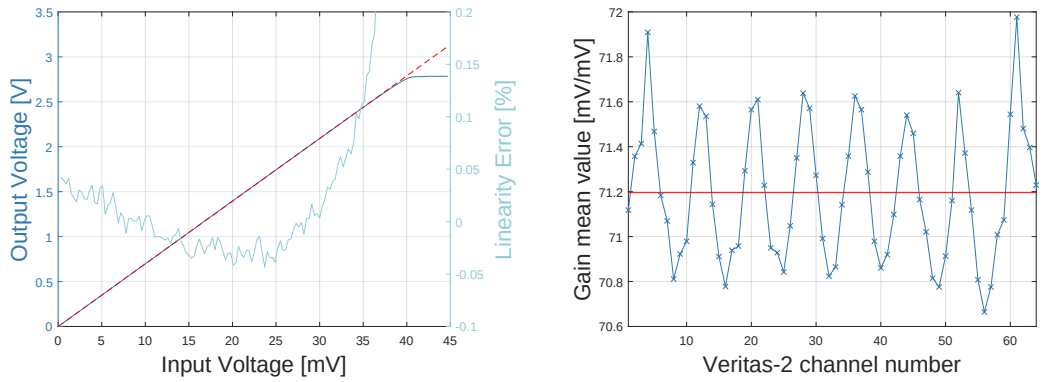
$$g_{V2}(t_{int}) = g_{I2V} \cdot g_{pre} \cdot g_{filt}(t_{int}). \tag{7.15}$$

The appropriate amplification of the ASIC for the WFI, can be derived from the the WFI science requirements, see table 2.1. In order to image the range of $0.2\,\mathrm{keV}$ to $15\,\mathrm{keV}$ with a DEPFET sensor with a amplification around $8\,\mu\mathrm{V/e}$, the gain of the Veritas need to be set to $64\,\mathrm{mV/mV}$ to take full advantage of the dynamic range [109].

Measurements show that the linearity error of the Veritas ASIC is less than 0.15 % in the dynamic range appropriate for the WFI. Furthermore, the individual channels can have slight differences in the mean gain value. The gain dispersion was measured to be less than 0.4 % in total.
Figure 7.16 depicts the linearity error of one channel and the gain dispersion of all readout channels of the ASIC. Gain mismatch is mainly due to technological dispersion in processing the components responsible for the gain of the analog stages in the chip. The maximal gain difference between two channels is less than 2 %, the standard deviation around 0.3 %.

In diagram 7.16b a pattern can be recognized which repeats all eight channels approximately. The background is presumably in the layout of the ASIC, here the analog channels are arranged in a meandering pattern. The power and signal lines have different lengths and thus run times which influence the analog behavior of the ASIC. This effect can also be observed in the saturation and offset values, which are discussed below. This effect is not considered in the model.

The linearity error is quite small, hence the amplification is assumed to be linear within the range of operation. Moreover the gain dispersion of the individual readout channels is not taken into account in the model. All channels of one readout chip are modeled with the same gain value.



(a) (b)

Figure 7.16.: (a) Measured linearity of one output channel of the Veritas-2 readout ASIC. The linearity error is less than 0.15 %, calculated from a linear fit. (b) Measured dispersion of the mean gain values of all output channels.

Saturation

The dynamic range of the analog stages are limited, hence the output of the Veritas-2 can saturate. Figure 7.17a and 7.17b depict the mean saturation values of 64 readout channels for the upper and lower rail. The upper saturation value has its mean at $2.82\,\mathrm{V}$ with a standard deviation of $11.7\,\mathrm{mV}$, while the lower saturation value lies at approximately $-0.85\,\mathrm{V}$ with a standard deviation of $5.9\,\mathrm{mV}$.

The saturation model includes values for lower and upper limits respectively. If an input value is smaller than the lower threshold X_{lo} or higher than the upper threshold X_{hi}, it is set to the value of the passed saturation values. The variation in saturation values for individual analog channels is normally distributed. Therefore the model includes as input a parameter for standard deviation of the saturation values and the upper and lower saturation values itself. The distribution functions for upper and lower saturation limits are given by

$$P(X_{hi} \leq x) = \frac{1}{\sigma_{hi}\sqrt{2\pi}} \int_{-\infty}^{x} e^{\frac{-(t-\mu_{hi})^2}{2\sigma_{hi}^2}}\, dt \tag{7.16}$$

$$P(X_{lo} \leq x) = \frac{1}{\sigma_{lo}\sqrt{2\pi}} \int_{-\infty}^{x} e^{\frac{-(t-\mu_{lo})^2}{2\sigma_{lo}^2}}\, dt. \tag{7.17}$$

Figure 7.17c to 7.17f show the modeled saturation for upper and lower limits and their corresponding histograms. The model was initialized with measured values for upper and lower saturation and deviation.

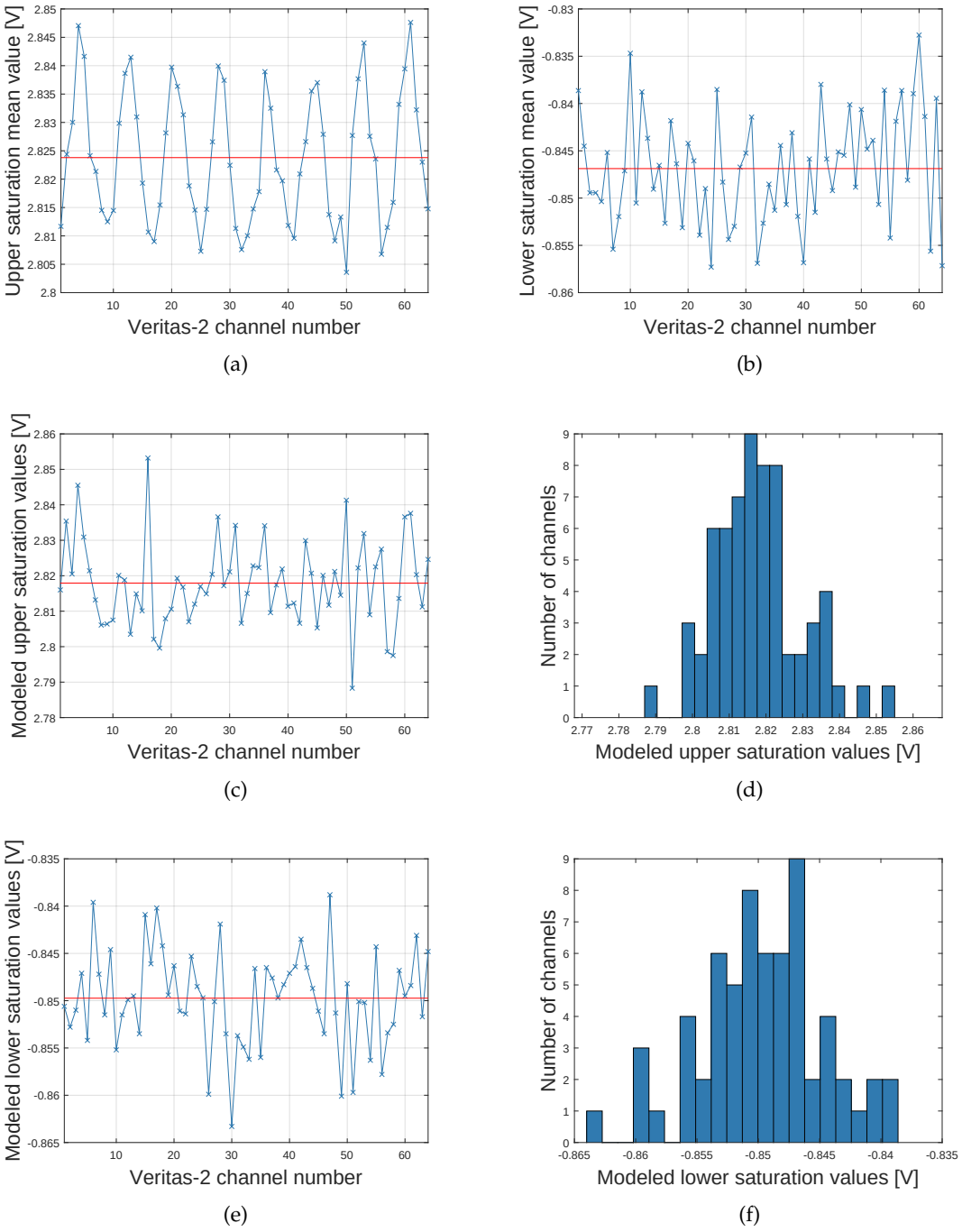


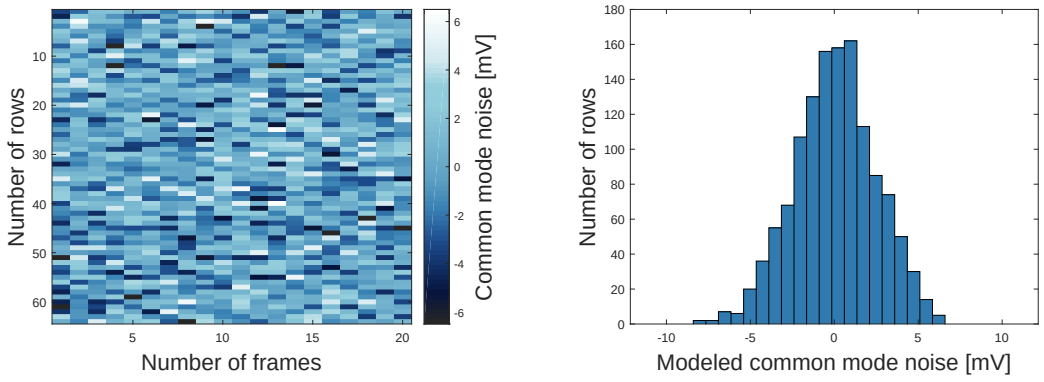
Figure 7.17.: Measured and modeled saturation values of all output channels of the Veritas-2 ASIC. The values for upper and lower saturation are normally distributed. (a) Upper saturation mean values: the maximal deviation from the mean value (red) is less than 0.8 %. (b) Lower saturation mean values: the maximal deviation from the mean value is approximately 1.6 %. (c) Upper saturation mean values with respective histogram (d). (e) Lower saturation mean values and respective histogram (f).

Common mode noise

The common mode noise is not an effect caused by the Veritas ASIC but rather by interaction of sensor and electronic system and originates from low-frequency baseline fluctuations. It is stated here because it influences directly the output of the Veritas ASIC. Common mode noise is a row-wise correlated noise caused by the row-wise read out of the pixel matrix. This correlated variation in the pixel signal is usually raised by external disturbances of the electronic systems, which controls the sensor, row-steering and readout electronics. These disturbances can also be caused by effects in the readout ASIC which affect all channels similarly. Especially, instability of gate pulses or changes of system voltages can induce common mode noise. Common mode noise correlates to the currently processed row and respective readout ASIC. A part of the common mode noise is filtered by correlated double sampling, but still a fraction of this noise is present in the data and worsens the noise performance of the system.
To model this noise source, a common mode value for each processed detector row i by the respective readout ASIC is calculated and then added to each pixel signal in this row. There is no correlation of the noise of a row with the same row of the subsequent frame. Measurements confirm that the common mode noise is $N(0, \sigma_{cm}^2)$-distributed

$$P(X_i \leq x) = F(x) = \frac{1}{\sigma_{cm}\sqrt{2\pi}} \int_{-\infty}^{x} e^{\frac{-t^2}{2\sigma_{cm}^2}} dt. \tag{7.18}$$

Figure 7.18 details the modeled common mode map and histogram for a DEPFET matrix with 64 rows and a readout of 20 frames.

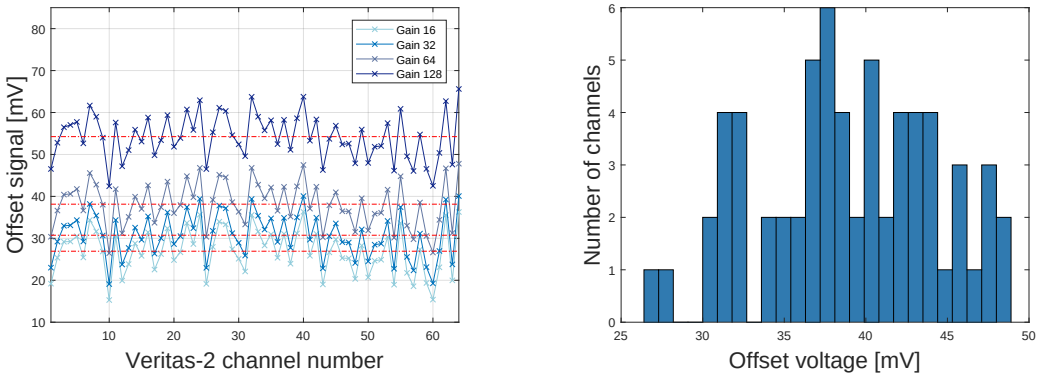


(a) (b)

Figure 7.18.: Common mode of the Veritas-2 readout ASIC, generated for 64 rows and 20 frames with a Gaussian distribution and a standard deviation of $2500\,\mu V$. (a) Common mode map of 64 rows and 20 frames. (b) Histogram of the common mode noise of 20 frames with each 64 rows.

Channel offset

Each readout channel of the ASIC has an offset, caused by small differences in the layout and technology processing of the ASIC. This offset is the output voltage when zero input voltage is applied. Since the DEPFET sensor is readout row-by-row, the channel offset results in a column-wise pattern.
The Veritas channel offset should not be confused with the definition of the offset of a DEPFET measurement which is a pixel individual value influenced by sensor, control and readout electronics.
The offset of the readout ASIC is defined channel-wise. The mean value increases with higher gain, as it can be seen in figure 7.19a. The ratio of the offset values between two gain configurations does not correspond to the ratio of the amplification. The deviation per channel from the mean value is almost constant for different gain configurations. Figure 7.19b shows the offset values of the ASIC in WFI gain configuration in a histogram. It can be recognized that the offset values are normally distributed.



(a) (b)

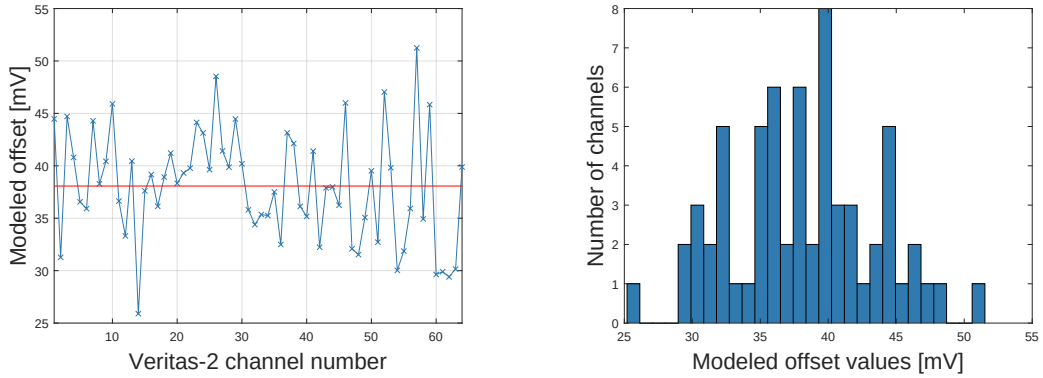
Figure 7.19.: Measured Veritas-2 channel offsets: (a) Channel offset acquired at different gain configurations. (b) Histogram of the offset voltages at WFI gain configuration (gain 64) showing a Gaussian distribution. A mean value of approximately $38\,\mathrm{mV}$ and a deviation of $5.4\,\mathrm{mV}$ were determined.

The offset values of an ASIC are modeled by generating a normally distributed signal for each channel. The distribution of the channel offset is described by the normal distribution function

$$P(X_j \leq x) = F(x) = \frac{1}{\sigma_{off}\sqrt{2\pi}} \int_{-\infty}^{x} e^{\frac{-(t-\mu_{off})^2}{2\sigma_{off}^2}} dt \tag{7.19}$$

with mean value μ_{off} per row j and standard deviation σ_{off} giving the dispersion from the mean value. The offset model can be influenced by setting the mean value

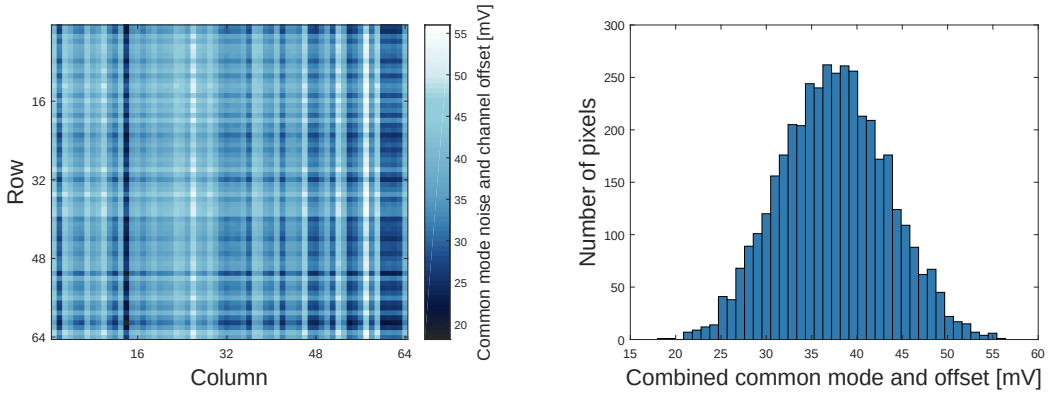
μ_{off} and standard deviation σ_{off}. The offset is modeled as a voltage signal. Figure 7.20 displays generated offset values for one readout ASIC.



(a) (b)

Figure 7.20.: Modeled offset of the Veritas-2 readout ASIC: (a) Offset values generated for 64 channels with a standard deviation of $5.4\,\mathrm{mV}$ and mean value of $38\,\mathrm{mV}$. (b) Corresponding histogram of 64 offset values.

The channel offset is a row independent effect, the offset values of the individual readout channels are added on the common mode value of the respective row. Figure 7.21a depicts one modeled frame of 64×64 pixel containing the combination of common mode noise and channel offset effect. The vertical structure in the frame is due to the channel offset, the horizontal pattern is caused by the common mode noise. A corresponding histogram of all pixels is shown in figure 7.21b.



(a) (b)

Figure 7.21.: Combined common mode noise and channel offset depicted as pixel map (a) and histogram (b).

From equations 7.18 and 7.19 follows the function for combined common mode noise

and channel offset distribution

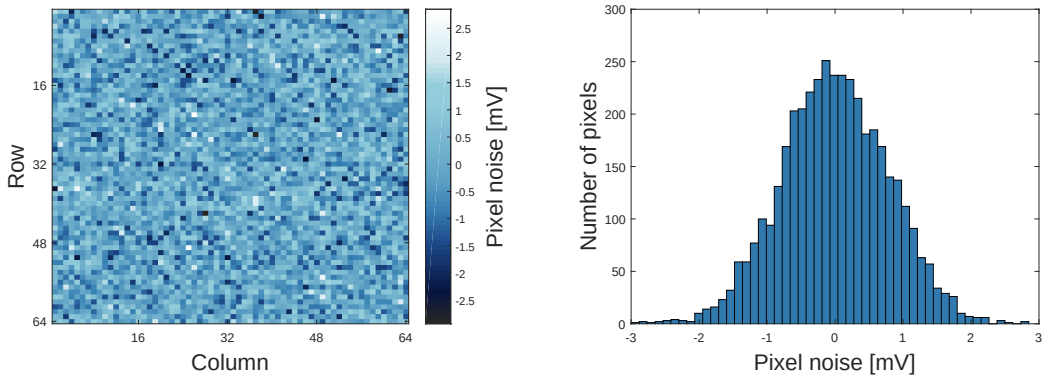
$$P(X_{i,j} \leq x) = \frac{1}{\sqrt{2\pi \cdot (\sigma_{cm}^2 + \sigma_{off}^2)}} \int_{-\infty}^{x} e^{\frac{-(t-\mu_{off})^2}{2(\sigma_{cm}^2+\sigma_{off}^2)}} dt. \tag{7.20}$$

7.4.6. Readout Noise Model

All noise contributions, except dark current noise, see section 7.4.3, depend on specific design of the sensor and readout electronics. The readout noise model summarizes the main noise contributions thermal noise and 1/f noise. All noise sources add up to

$$\sigma_{noise}^2 = \sigma_{shot}^2 + \sigma_{thermal}^2 + \sigma_{1/f}^2. \tag{7.21}$$

A noise map is calculated pixel and frame-wise. Measurements reveal a Gaussian distribution of the total noise. Figure 7.22 depicts a noise map and a histogram of the noise values of one modeled frame with 64 × 64 pixels.



(a) (b)

Figure 7.22.: Summarized readout noise of the detector, generated for a detector with 64 × 64 pixels. The noise values are generated with a standard deviation of 800 µV. (a) noise map of one frame, (b) histogram of the noise contribution of the corresponding frame.

To model noisy pixels, which present a considerably higher noise than their adjacent pixels, the noise values of the corresponding pixels are frame-wise multiplied with a particular factor. These factors are stored in a noisy pixel map. By varying the noisy pixel multiplication factors, the intensity of the outliers can be adjusted flexibly. Moreover individual pixels or cluster of pixels showing significantly deviating noise behavior can be modeled.

8. Architecture of the PRE

Within this chapter, the architecture of the Programmable Real-Time Emulator is summarized. The firmware concept and real-time processing of the modeled frame stack is outlined in section 8.1. From this, the hardware requirements are derived and the best suitable hardware platform with its components is presented in section 8.2. The software environment for detector modeling and operation of the PRE is illustrated in section 8.3.

8.1. Real-Time Data Processing

The main task of the data processing system is to output the offline generated frame stacks in real-time appropriate to the output of the detector system.
As derived in section 6.3, the PRE is built up as HW/SW codesign. According to the hardware requirements established in section 6.3.2, a basic scheme of the hardware architecture of the processing system is depicted in figure 8.1. Best suited for the PRE is an FPGA-based platform with fast sampling DACs.

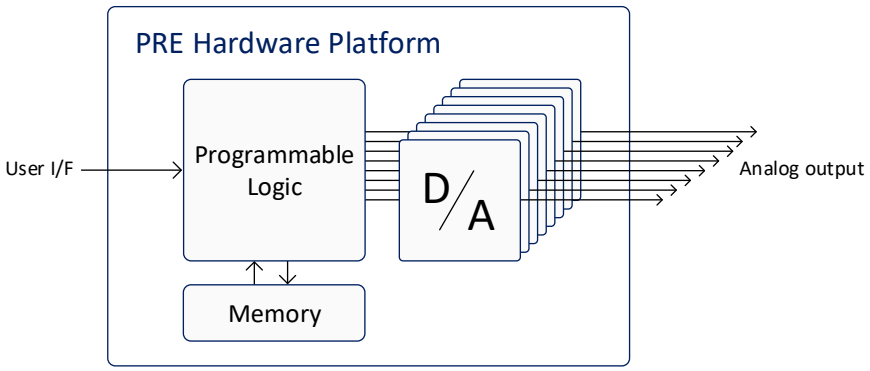


Figure 8.1.: Basic concept of the PRE hardware. A fast user link interfaces the hardware. A memory holds the huge image stacks, while an FPGA performs the processing of the image data. Eight fast sampling DACs generate the analog output data stream.

A fast user interface establishes a link to transfer the image data to a memory with appropriate size and speed on-board of the hardware system. An FPGA performs the data stream processing of the image data and calculates a sub-pixel resolution per pixel signal. Furthermore it interfaces the necessary eight DACs to output the analog signal.

The processing flow is depicted in figure 8.2. The system is configured with huge frame stacks and sub-pixel resolution data. Further the pulse shape of each individual pixel signal is calculated in the block data stream processing. The last unit interfaces the DACs and converts the processed data to analog signals.

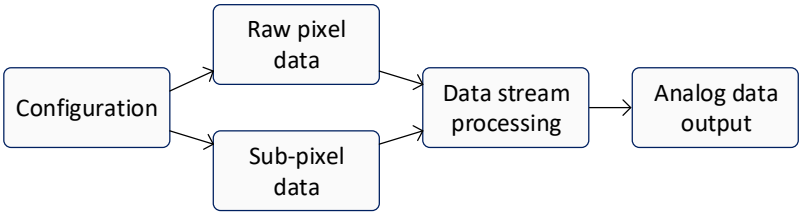


Figure 8.2.: Overview of the PRE processing concept. After configuration and loading the pixel raw data and sub-pixel resolution data in a memory, the data stream processing is performed. At last, the data stream is converted to an analog output signal with DACs.

8.1.1. Sub-pixel Processing

In simulation environment, the individual values of a pixel signal, called pixel base values, are represented as static signals over the time period of the respective pixels. In order not only to output a static value of a pixel but to display a nearly realistic illustration of the analog output of the detector, the signal pulse of each pixel needs to be shaped.
Therefore, a sub-pixel resolution is introduced to accurately represent the pulse shape of each pixel as required in section 6.1. The shape of the output pulse is characterized in section 5.1.3

Shaping the pulse of a pixel signal and thus achieving sub-pixel resolution can be performed by a special processing of the pixel base value. This is done by multiplying and adding of particular values to the pixel base signal. Therefore a timing register for multiplication and a noise register for addition is introduced. As the shaping of the pulse is mainly a characteristic of the readout ASIC, it is sufficient to model the pulse shape in a same way for each channel. That means, each of the eight readout ASIC channels is mapped to a noise and timing register. Thus each pixel in a channel is

processed with the same timing and noise configuration.
The minimum pixel time defined for the WFI is approximately $40\,\mathrm{ns}$. To achieve the required new sample every $2.5\,\mathrm{ns}$, see table 6.1, each register holds 16 factors for processing with the base values.
As the output values need to be represented with a resolution higher than $14\,\mathrm{bit}$, the resolution of the timing and noise register is set to $16\,\mathrm{bit}$ to gain small increments. The timing register signals are interpreted to achieve an output signal between 0% and 200% of the pixel base signal with a step size of 0.003%. Applying the noise register values, a digital value in the range of $-2^{15} - 1$ to 2^{15} can be added to the pixel base value. This means that a maximum of half of the output signal of the DACs used can be added to the pixel base values.

Figure 8.3 outlines the computation of the pixel base values with the timing and noise register. This structure is implemented for every parallel channel.

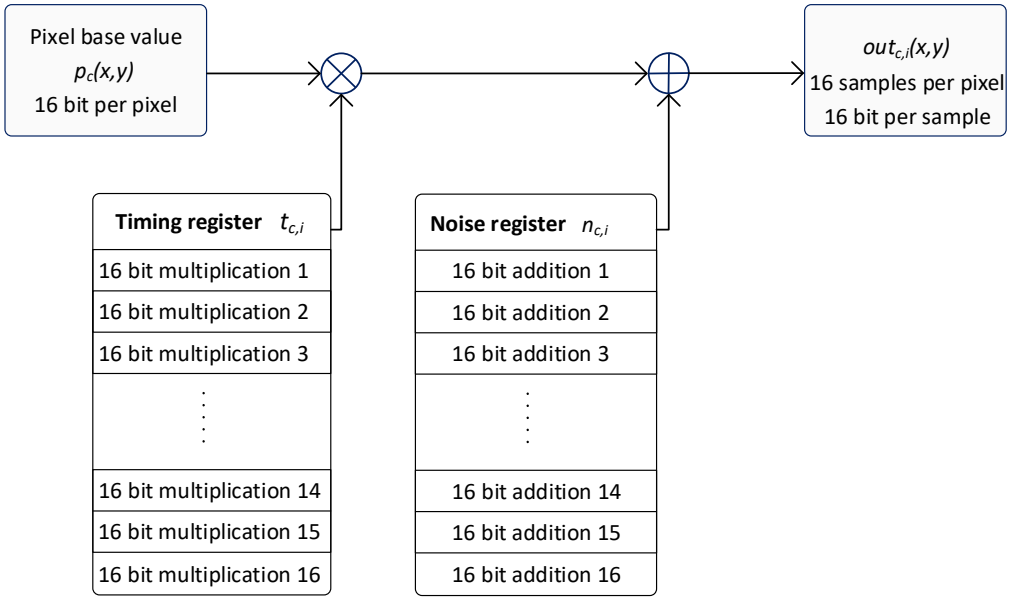


Figure 8.3.: High speed sub-pixel processing for one modeled readout channel. The pixel base values are first multiplied with a timing value and then imposed with a noise value. In total, 16 multiplications and additions lead to the output consisting of 16 samples of $16\,\mathrm{bit}$ pit per pixel signal.

Since the transient response of a pixel signal is dependent on the previously processed pixel signal, the difference between these two signals needs to be processed with the timing multiplication factor and added to the former pixel signal. Afterward, the noise

factor is imposed to that signal. This results in a processing algorithm for one analog channel

$$out_{c,i}(x,y) = p_c(x-1,y) + t_{c,i} \cdot (p_c(x,y) - p_c(x-1,y)) + n_{c,i} \tag{8.1}$$

with $p_c(x,y)$ being the pixel base value with c indicating the readout channel respectively per readout ASIC, x and y representing the pixel coordinates. The oversampled output is indicated as $p_{c,i}(x,y)$ with i being the index for the sub-pixel samples. The timing and noise registers per readout channel are indicated as $t_{c,i}$ and $n_{c,i}$. It is to note that the former pixel signal $p_c(x-1,y)$ is needed for the processing of the timing calculation. The output is indicated as $out_{c,i}(x,y)$.

Sub-pixel processing increases the data rates of the PRE drastically. Emulation of the FD is performed with a processing time of a row of $2.5\,\mu s$, resulting in a pixel time of approximately $40\,\mathrm{ns}$. With updating the output signal every $2.5\,\mathrm{ns}$ and emulation of the detector in two halves results in a data rate of $12.8\,\mathrm{Gbit/s}$.
Emulation of the LD demands a processing time per row of $10\,\mu s$. Nevertheless, the LD can be emulated with the fast processing speed of the FD. This helps to ensure that the connected Detector Electronics with the on-board real-time frame processor is not a limiting factor in the WFI signal processing chain. Emulation of the LD with the processing speed of $40\,\mathrm{ns}$ per pixel and high speed sub-pixel processing results in a data rate of $51.2\,\mathrm{Gbit/s}$.

Figure 8.4 depicts simulations of the sub-pixel processing. Three pixel signals are shown, pixel n, pixel $n+1$ and pixel $n+2$. The first graph shows the ideal waveform, with instantaneous transition between one pixel signal and the next one. However, this behavior is not realizable in physical systems.

By multiplication of the pixel base values with the timing register, it is possible to emulate for example rise times, glitches or overshoot, as depicted in the second and third graph. By adding positive or negative noise signals to the pixel base value, additional high frequency noise can be imposed to the signal, as shown in the fourth graph. The last graph depicts a combination of timing and noise.
The sub-pixel processing can be bypassed by setting the values for the timing register and the noise register to a fixed value. For the timing register, a multiplication factor of 1 can be set and the noise is imposed with a value of 0. This results in an almost ideal waveform, which is only limited by the characteristics of the electronic circuit and cables.

With this shaping of the pixel signal with respect of noise and time, the ADCs of the DE can be tested and adjusted. Different sampling points can be defined to find the

best suitable point according to the waveform. It is also conceivable, that the ADC performs a fast oversampling of the individual pixel values and averages them with the possibility to reduce noise. This implementation of the DE can be tested with the emulator and various shapes of the pixel signal in advance. The influence of noise and timing to the analog signal and thus the physical data and results can be studied to find the optimal processing in the DE.

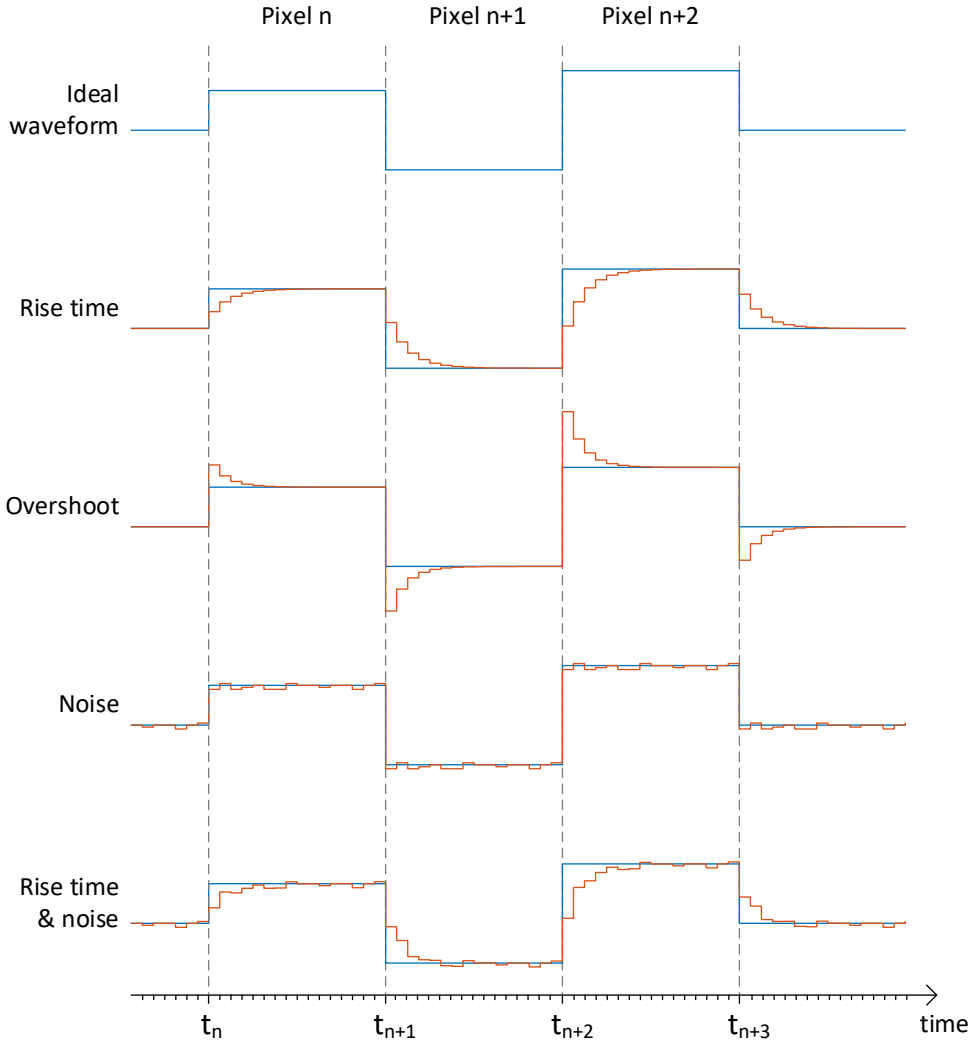


Figure 8.4.: Examples of sub-pixel processing. The ideal waveform of pixels signals is compared to various sub-pixel processing emulating a rise time, overshoot, noise and combination of rise time and noise.

8.1.2. Scaling Capabilities and Timing Concept

Scaling capability with respect to emulation of different detector sizes and readout rates is a major requirement to the system, as listed in section 6.1. An advanced design is developed to achieve a flexible solution.

To emulate detectors with different sizes, and thus number of pixels, a different number of parallel sampling DACs is required. In order to develop a flexible instrument for a wide range of applications, detectors with a number of pixels per row of 64, 128, 256 or 512 shall be emulated. Therefore 1, 2, 4 or 8 DACs have to be operated simultaneously. The processing concept of the PRE hardware is designed for the demanding case of eight parallel output channels. But this concept is also designed in such a way that less channels can be addressed without sacrificing performance. The basic framework of the design stays the same, while only the data rate of the inputs and their applied order are changed to obtain a different number of output channels. By means of parallelization, the fewer channels are operated, the faster the output can be generated.
The system design consists of eight parallel operating sub-pixel processing units. Figure 8.5 depicts such a sub-pixel unit for a channel c.

Figure 8.5.: Block diagram of one out of eight parallel operating sub-pixel processing units. Input is a pixel base value and a sub-pixel word, output is a processed sub-pixel value.

Input of this sub-pixel processing unit is a $16\,\mathrm{bit}$ pixel base value $p_c(x, y)$ and a $32\,\mathrm{bit}$ sub-pixel configuration word, which consists of a $16\,\mathrm{bit}$ timing $t_{c,i}$ and a $16\,\mathrm{bit}$ noise value $n_{c,i}$. In total, 16 words build a sub-pixel configuration register as depicted in figure 8.6. Output of the processing unit is a calculated sub-pixel value $out_{c,i}(x, y)$ with $16\,\mathrm{bit}$.

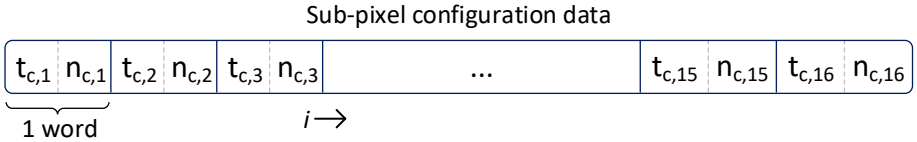


Figure 8.6.: Configuration register for a modeled channel c. A timing and noise value build a word, in total 16 words form a sub-pixel configuration register.

For emulation of eight parallel output channels, the sub-pixel processing needs to be performed eight times in parallel. The processing of the pixel base values with the sub-pixel configuration words for emulation of eight channels is illustrated in figure 8.7. Once a new pixel base value is loaded, it is calculated with the timing and noise word as stated in equation 8.1. This is performed 16 times in a pipeline to achieve the required oversampling of a pixel. As soon as the calculation of 16 words is finished, the next pixel base value is loaded to start a new sub-pixel processing. In this case, a sub-pixel processing unit computes sequentially all sub-pixel output values of a pixel.

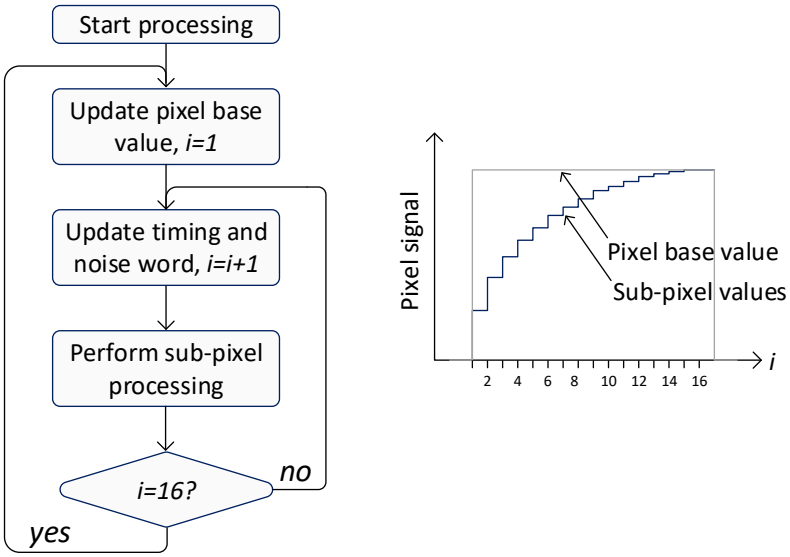


Figure 8.7.: Flow chart of the sub-pixel processing in case of emulation of a detector with 512×512 pixels requiring 8 parallel channels. In total, 16 calculations are performed by this unit to achieve the sub-pixel resolution shown at the right.

The timing scheme of one of eight processing units for modeling of the pixels of eight channels in parallel is illustrated in figure 8.8. A pixel base value is applied for 16 cycles, while the sub-pixel configuration words are updated each cycle resulting in an output each cycle. The update rate of the sub-pixel configuration words and thus the rate of the output values is by a factor of 16 higher compared to the update rate of the pixel base values.

For emulation of a detector with less than 512 pixels per row, only the necessary number of parallel operating units could be used. The unused units could be switched off. That will meet the requirements concerning generation of output data with a given pixel rate, see section 6.1. As the requirement for flexibility and scalability with respect to processing speed, real-time operation and adaptability to later defined changes must

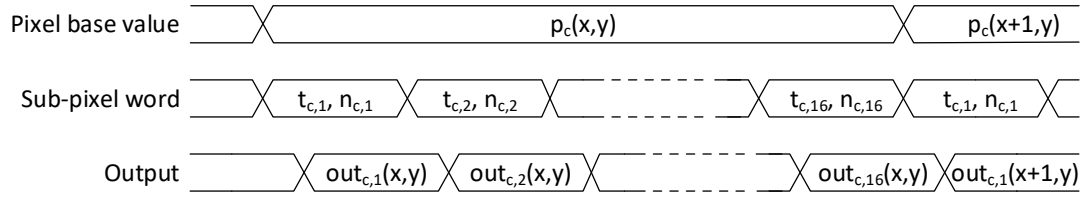


Figure 8.8.: Sub-pixel processing timing diagram for modeling eight output channels. A pixel base value is applied while 16 sub-pixel words are sequentially processed in a pipeline structure. Once all sub-pixel words are processed, the next pixel base value is applied.

also be met, a more elaborate design is proposed. This leads to a higher output speed of the processed data, if less than eight channels need to be operated.

The already presented design of eight parallel processing units is also used for the generation of data requiring less than eight channels. By using several processing units for calculations on the same pixel base values and by a sophisticated distribution of the timing and noise words, it is possible to process the data with a higher rate than with the sequential pipeline structure.

Emulation of a detector with 256 pixel per row would demand four parallel operating units. To benefit from the structure of eight parallel working sub-pixel processing units, respectively two units are used to calculate the values of one pixel. The timing and noise words are alternately applied to the two processes so that the full processed output is already available after eight cycles. Afterward, the next four pixel base values can be applied to the eight processing units. Figure 8.9 shows the flow charts for two parallel working units operating on the same pixel base value input.

Figure 8.10 depicts the timing diagram for two parallel operating processing units. They have the same pixel base value as input but different sub-pixel words. The odd words of the sub-pixel configuration register are applied to unit c while the even words are applied to unit $c + 4$. After eight calculation cycles, the next pixel base value can be applied to the two processes. Thus the processed output of a pixel value can be achieved in half of the time than processing with only four units.
The mapping of individual processing units with dedicated pixel base values and sub-pixel words is performed in a way that the output data of the processing units is in the right order.

Generation of output data for two output channels, representing 128 pixels per row, or even for one output channel, representing 64 pixels per row, follows the same way.

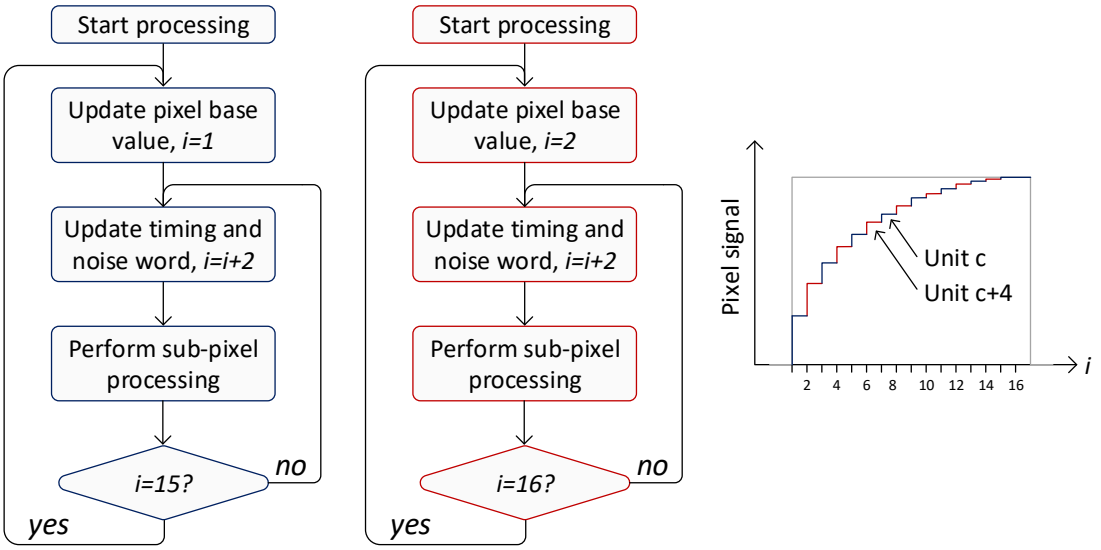


Figure 8.9.: Flow chart of the sub-pixel processing for four channels. Two parallel processing units calculate the sub-pixel resolution of one pixel base value with alternately applied sub-pixel words. The process marked in blue calculates the odd sub-pixels, while the red marked process computes the even values. By parallel processing, the output can be obtained in half of the time compared to operation of four channels.

Two output channels are processed by loading two pixel base values simultaneously and applying them to four parallel channels respectively. The sub-pixel configuration words are distributed over the eight units in a way that the processed output is in the right sequence. After four cycles all 16 words are calculated and the next two pixel base values can be loaded.
Emulation of only one channel is implemented by using all eight processing units to calculate the sub-pixel output values. Processing of one pixel can be achieved within two cycles. Therefore one pixel base value is applied to all units in parallel. In the first cycle the upper half of the sub-pixel words are processed, while in the second cycle the lower half is processed. This leads to a very fast processing of the output values.

The data rate to load the pixel base values is independent on the number of parallel operating channels. In case of eight parallel channels, eight values are fetched every 16 cycles, or in case of one operating channel, one value is fetched every two cycles. This leads to a data rate with a cycle time of $2.5\,\mathrm{ns}$ to $1 \cdot 16\,\mathrm{bit}/2/2.5\,\mathrm{ns} = 3.2\,\mathrm{Gbit/s}$.
The sub-pixel words need to be updated to eight units every cycle. This results in a

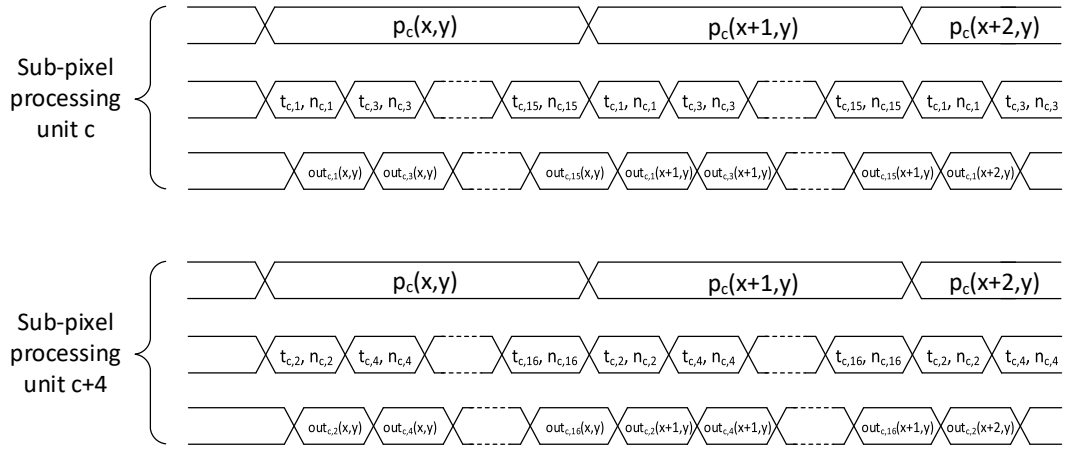


Figure 8.10.: Sub-pixel processing timing diagram for processing of four channels. A pixel base value is applied to two parallel working processes while eight sub-pixel words are sequentially processed in a pipeline structure respectively. Once all sub-pixel words are processed, the next pixel base value is applied to both processes.

data rate of $8 \cdot 32\,\mathrm{bit}/2.5\,\mathrm{ns} = 102.4\,\mathrm{Gbit/s}$.
These data rates demand a memory for the pixel base values with moderate timing and a very fast memory for storage of the sub-pixel configuration data.

This design of the sub-pixel processing units with the DAC logic block to interface the DACs is depicted in figure 8.11. The sub-pixel processing runs with a fixed speed to generate the outputs of this unit with a data rate of $102.4\,\mathrm{Gbit/s}$. This is also the maximal data rate to interface the DACs. Since these shall also be operated with other rates, a First In, First Out (FIFO) buffer is introduced between the signal processing units and the DAC logic block. This FIFO ensures data transfer between the two clock domains of the sub-pixel processing units and the DAC logic unit. A higher process controls the level of the FIFO. If the content of the buffer approaches its upper limit, the sub-pixel processing is paused. For a real-time generation of the analog output signal, it must be ensured that the buffer runs not empty resulting in no data output. This means, that the sub-pixel processing unit must run at least as fast as the output of the analog signal.

Table 8.1 summarizes the possible timings which can be reached with the presented design for different number of parallel outputs. The achievable times depend on the number of channels to be generated. If less channels are required, the output can be calculated faster, since less data needs to be processed with the same number of resources.

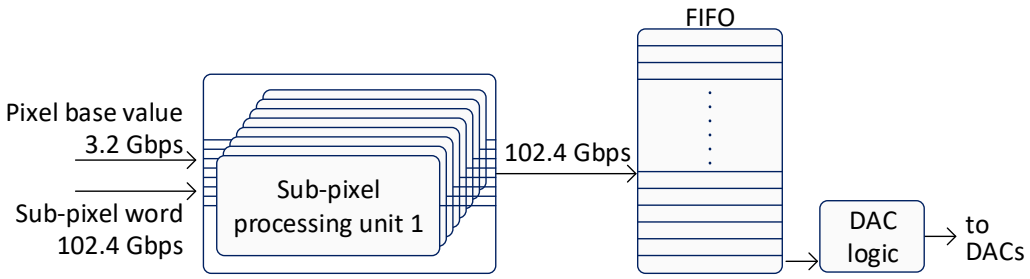


Figure 8.11.: Overview of the design with eight parallel sub-pixel units and a DAC logic to interface the converters. A FIFO buffer is inserted to interface the different clock domains of sub-pixel processing and DAC logic block.

With this design, for example, one channel representing a detector with 64 pixel per row, could be generated with a pixel clock of $200\,\mathrm{MHz}$, or a pixel time of $5\,\mathrm{ns}$ and a sub-pixel resolution of $0.3125\,\mathrm{ns}$. These times are only theoretical values, however, since it is very demanding to find and interface a suitable DAC that generates this signal in the required configuration. This fast configuration of the timing is not necessary as a WFI emulator. But with this design, pixel frequencies can be generated that exceed the required frequency. Data streams can be generated that are flexibly adjustable in timing with regard to possible upcoming, faster sensor designs which may change the WFI requirements.

Table 8.1.: Summary of the results of sub-pixel processing with different emulated detector sizes.

Number of channels	**sub-pixel processing cycles**	**minimal pixel processing time**	**theoretically achievable sub-pixel resolution**
8 channel	16 cycles	$40\,\mathrm{ns}$	$2.5\,\mathrm{ns}$
4 channel	8 cycles	$20\,\mathrm{ns}$	$1.25\,\mathrm{ns}$
2 channel	4 cycles	$10\,\mathrm{ns}$	$0.625\,\mathrm{ns}$
1 channel	2 cycles	$5\,\mathrm{ns}$	$0.3125\,\mathrm{ns}$

With the presented design, data from detectors with eight channels, consisting of 512 pixels per row can be processed. The design works independently of the number of channels to be generated. By parallelization of processes, the channel output can be achieved in a shorter time. Separating the processing and DAC transmission clock domain, the DACs can be triggered with the required timing. Thus, the timing and scalability requirements are clearly fulfilled.

8.2. Hardware Implementation

From the design presented in section 8.1.1 and 8.1.2, as well as from the top level specification of section 6.3.2, the hardware requirements of the PRE can be derived. These requirements are summarized in table 8.2. A suitable hardware platform would be the Xilinx FPGA evaluation board VC707 in combination with two digital-to-analog converter cards FMC204. The features of these components are also listed in table 8.2. Comparison shows that the proposed hardware is appropriate as PRE setup, as the majority of requirements are fulfilled. Only in a few points the hardware has to be adapted to meet the requirements.

Table 8.2.: Summary of the hardware requirements.

Parameter	**Requirements**	**VC707 & FMC204 Features**	**Compliance**
Processor	FPGA	Virtex-7	✓
	Microcontroller	MicroBlaze	✓
DAC characteristics			
Number of outputs	8	8	✓
Resolution	$> 14\,\mathrm{bit}$	$16\,\mathrm{bit}$	✓
Sampling frequency	$400\,\mathrm{MSPS}$	$500\,\mathrm{MSPS}$	✓
Memory			
Pixel base values	$> 4\,\mathrm{GB}$	1 GB DDR3 SDRAM (expandable)	○
Data rate	$> 3.2\,\mathrm{Gb/s}$	$12.8\,\mathrm{Gb/s}$	✓
Sub-pixel data	$> 4\,\mathrm{kb}$	$37\,\mathrm{Mb}$ BRAM	✓
Data rate	$> 102.4\,\mathrm{Gb/s}$	approx. $32\,\mathrm{Gb/s}$	○
Input			
User interface	Interface to PC	Ethernet, PCIe, etc	✓
Output			
Analog Output	$V_{min} = -0.8\,\mathrm{V}$ $V_{max} = 2.8\,\mathrm{V}$	$V_{out} = 1\,\mathrm{V}$ (peak-peak)	×
	differential output	single-ended output	○
Digital Output	8 signals, LVDS	User I/Os, MGT, etc.	✓

With this hardware, the pixel base values would be stored in the DDR3 Synchronous Dynamic Random Access Memory (SDRAM), and the sub-pixel configuration data in the internal block random access memory (BRAM). The capacity of the DDR3 SDRAM memory for storing the pixel base values is to small. As this is implemented as a SODIMM device, it is exchangeable to a suitable memory with higher storage capacity. The data rate of interfacing the BRAM memory in terms of sub-pixel processing are quite high. By generation of eight parallel BRAMs with a size of one sub-pixel configuration register, this demanding data rate can be achieved [127].
Moreover, the output signal of the DAC converter cards must be adapted to the required dynamic output range. In addition, a single-to-differential conversion needs to be performed. The necessary circuits are implemented on an additional board together with a protection circuit for interfacing the DE flight module.
These adjustments, however, are marginal and therefore the suggested platform is very well suited as processing system of the PRE.

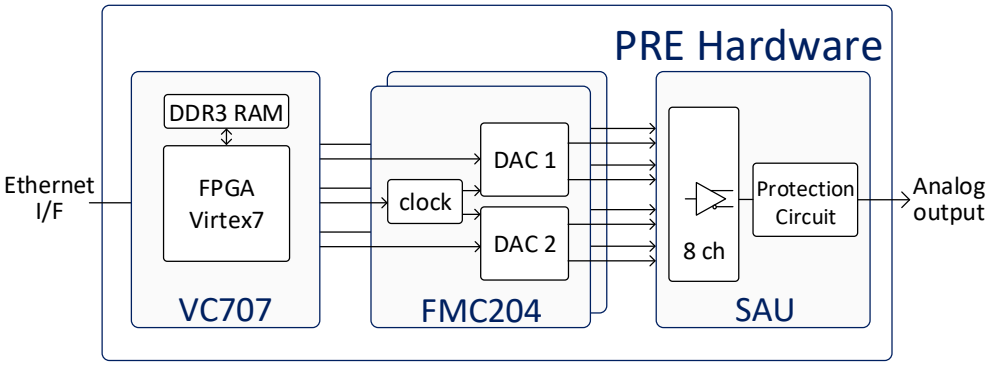


Figure 8.12.: Overview of the PRE hardware architecture consisting of an FPGA board, two DACs comprising eight channels and a Signal Adaption Unit (SAU).

Figure 8.12 depicts the hardware system of the PRE. It consists of an FPGA board for the processing of the frame data. Two converter cards with a total number of 8 DAC channels convert the digital data into an analog signal. The Signal Adaption Unit (SAU) has the function of adapting the signal to the output signal of the AFE and limiting it to a certain range for protection of interfaced flight electronics.

8.2.1. Processing Unit

The processing unit of the PRE is a VC707 board from Xilinx populated with a Virtex-7 (XC7VX485T-2FFG1761C) FPGA [124], [126]. This device provides highest system performance in the 7-series FPGA family with 485 760 logic cells, 2800 DSP slices,

37 Mbit of Block RAM and up to 700 user I/Os.
Furthermore, the board features a DDR3 memory module, which provides 4 Gbyte volatile SRAM for storing data. This memory provides a width of 64 bit and a data rate up to 1600 MT/s.
Additionally the VC707 utilized an Ethernet PHY device for communications at 10, 100 or 1000 Mb/s.
Moreover, the board comprises two instances of FPGA mezzanine card (FMC) HPC ANSI/VITA57.1 specification connector [6]. One FMC HPC connector provides a variety of user-defined I/O signals, transceivers, clocks and power connections. There is a variety of FMC daughter cards available, comprising a high bandwidth of different applications.
Peripheral electronics for configuration and debugging are implemented, like a JTAG interface, a USB-to-UART bridge, user switches, buttons, and LEDs. The power supply of the board is 12 V. A power management system consists of switching and linear regulators and generates all internally used voltages.
Figure 8.13 depicts the VC707 FPGA board equipped with two FMC daughter cards providing a digital-to-analog conversion stage explained in the next section.

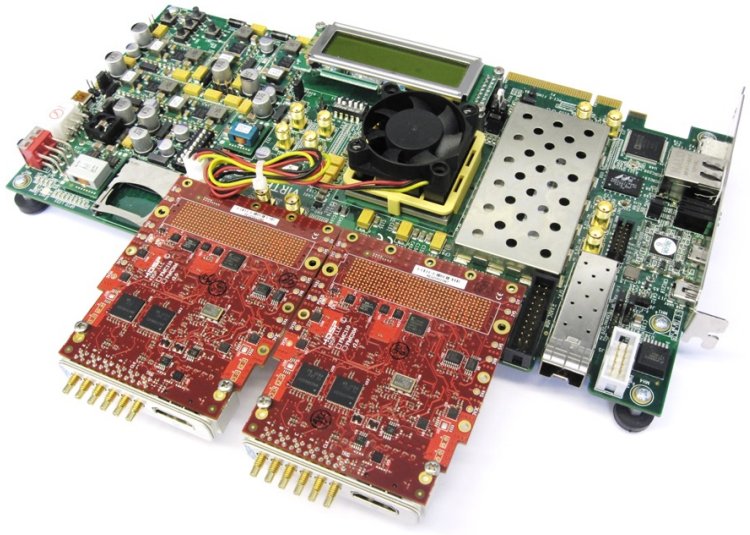


Figure 8.13.: Picture of the PRE hardware setup comprising an VC707 FPGA baseboard and two FMC204 mezzanine cards with DACs.

8.2.2. Digital-to-Analog Converter Stage

The digital-to-analog converter stage is realized by two FMC daughter cards FMC204 provided by the vendor 4DSP. A block diagram of an FMC204 is shown in figure 8.14, a picture in combination with the FPGA motherboard is shown in figure 8.13.

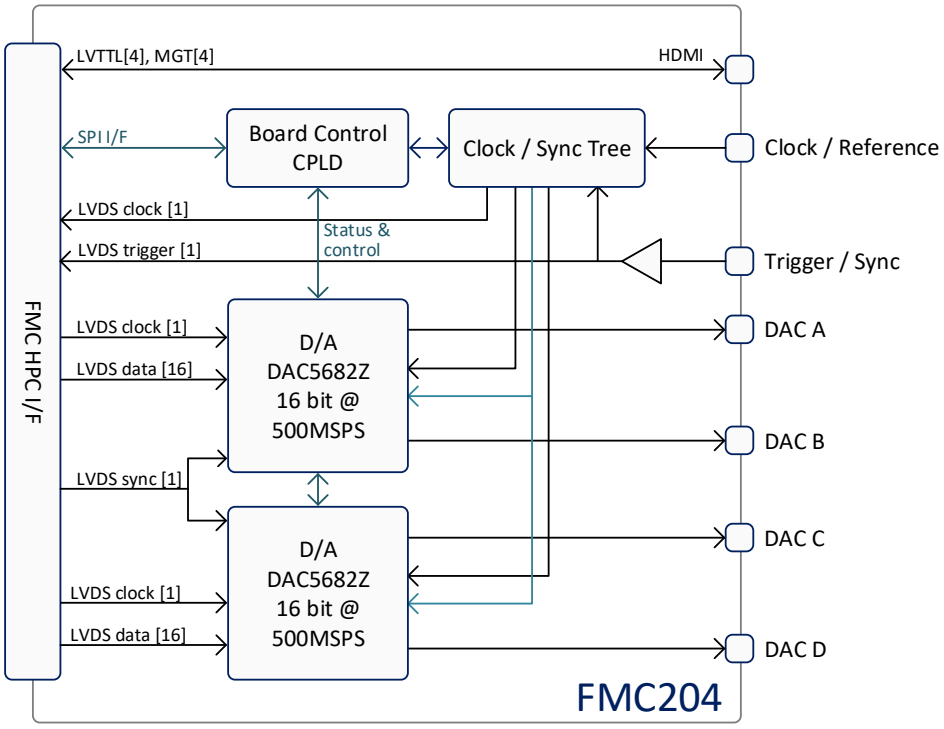


Figure 8.14.: Block diagram of the FMC204 quad-channel analog-to-digital conversion card.

Each card is populated with two dual-channel DACs DAC5682Z fabricated by Texas Instruments accessible through front panel coax connectors. The DAC5682Z provides $16\,\mathrm{bit}$ conversion with simultaneous sampling at a maximum rate of $1.0\,\mathrm{GSPS}$. When the DAC device is operated in dual-channel mode, the maximum data rate is $500\,\mathrm{MSPS}$. The DAC integrates a wideband LVDS data input, interpolation filters, on-board clock multiplier and internal voltage reference. It offers superior linearity, noise, crosstalk and PLL phase noise performance. An on-chip delay locked loop (DLL) simplifies LVDS interfacing by providing skew control for the LVDS input data clock [104].

The FMC204 offers a clock architecture circuitry that combines high flexibility and performance. Components have been chosen to minimize jitter and phase noise resulting in reduced degradation of the data conversion performance. The sample clock can be supplied externally through a coax connection or by an internal clock source,

optionally locked to an external reference. The clock tree has a phase-locked loop (PLL) and clock distribution section. The PLL ensures locking of the internal clock to an externally supplied reference. There is also an on-board reference which can be used if no external reference is present. A voltage-controlled oscillator (VCO) is used as internal clock source and can be connected to the distribution section instead of the external clock input. The distribution section drives the DAC devices. An LVDS clock output is connected to the FMC connector as a reference for the digital data transferred to the DAC devices. Additionally a trigger input for customized sampling control can be enabled [2].
The FMC204 allows flexible control on clock source, sampling frequency and calibration through a SPI communication bus. In addition, multi-gigabit transceiver I/O pairs and LVTTL lines are available on the front panel for digital control and timing signals [1].

8.2.3. Signal Adaption Unit

The Signal Adaption Unit (SAU) is used to adapt the analog output of the DACs to the output signal of the Front-End Electronics (see section 7.4.5). Amplitude and level of the signal must be adjusted without limiting the bandwidth or falsifying the signal. Moreover, the single-ended output of the DACs need to be converted into a differential signal. In figure 8.15 a schematic circuit of the buffer for signal adaption is shown.

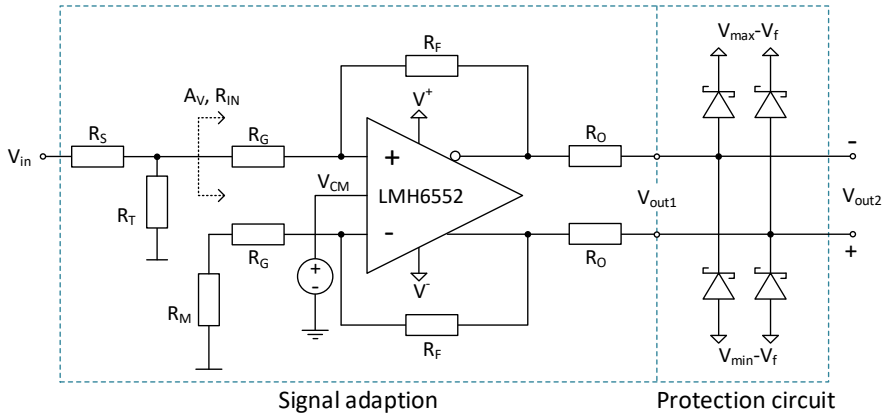


Figure 8.15.: Circuit of signal adaption and protection unit. A high-speed operational amplifier performs single-to-differential conversion with appropriate common mode and magnitude. A network of fast diodes can limit the signal to maximum allowed values.

For this application, a high-speed fully differential amplifier with a small signal $-3\,\mathrm{dB}$ bandwidth of $1.5\,\mathrm{GHz}$ at gain $A_V = 1$ is used. The resistors shown in figure 8.15,

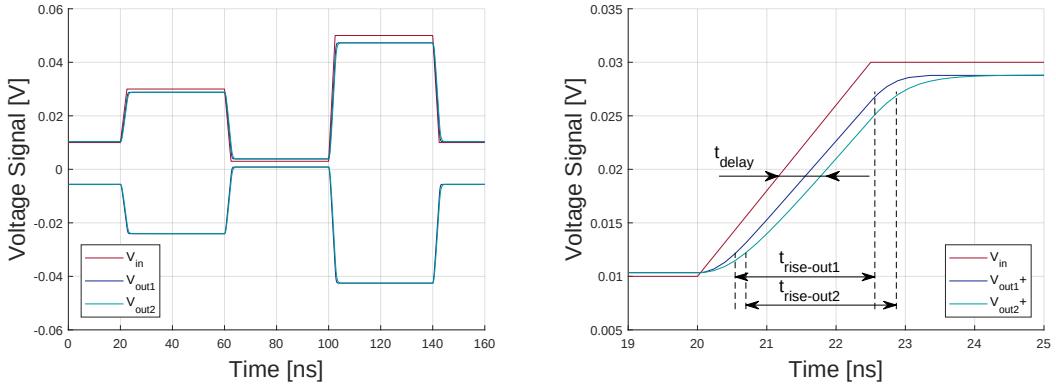
were calculated according equation 8.2 to adapt the different dynamic ranges of the emulation and the DEPFET system.

$$\begin{aligned} \beta_1 &= \frac{R_G}{R_G + R_F} & \beta_2 &= \frac{R_G + R_M}{R_G + R_F + R_M} \\ A_V &= \frac{2(1-\beta_1)}{\beta_1 + \beta_2} & R_{IN} &= \frac{2R_G + R_M(1-\beta_2)}{1+\beta_2} \\ R_S &= R_T \parallel R_{IN} & R_M &= R_T \parallel R_S \end{aligned} \tag{8.2}$$

As the SAU is the stage of the PRE interfacing the flight module of the DE, it has to be ensured that the output signals of the SAU are in the allowed range of the DE. Signals outside the allowed range can cause latch up or even damage to the input stage of the DE.
A protection circuit is implemented, which limits the signal to the specified range of the DE interface. In figure 8.15 an example of such a protection circuit is shown. A network of rectifying diodes, in this case fast schottky barrier diodes, limit the peak voltages of positive and negative signal alternations, referenced to the minimum and maximum dc levels $V_{max} - V_f$ and $V_{min} - V_f$. This circuit allows signals to pass unchanged whose amplitudes are less than the sum of the forward voltage V_f of the diode and the potential to which the diode is connected. Signals with larger voltage amplitudes force the diode into conduction and the output signal is clamped.

Figure 8.16 and 8.17 depict graphs from SPICE simulations of the electrical circuit of the SAU as shown in figure 8.15 with a amplification $A_V \approx 6\,\mathrm{dB}$. First a simulation within the allowed operating range was performed, depicted in figure 8.16. The input signal is a single-ended signal, with every voltage step corresponding to a pixel value. The influence of the protection circuit can be seen in the enlarged part of the simulation. The circuit affects delay time t_{delay} as well as rise and fall times of the signal t_{rise} and t_{fall}. The rise time is defined by the time a signal rise from 10% to 90% of its final value, respectively for fall time.
For this specific example, the rise times of the output signal of the buffer V_{out1} and the rise time of output signal of the buffer in combination with the protection circuit V_{out2} are compared. The protection circuit worsens the rise time by approximately $0.1\,\mathrm{ns}$. Furthermore, an additional delay time of approximately $0.7\,\mathrm{ns}$ is added. The simulation shows the same behavior for the falling edge of the signal. For application as PRE, these influences are negligibly small.
In figure 8.17 a simulation of an out-of-range voltage is depicted. The maximum allowed range was exemplary set from $V_{min} = 0\,\mathrm{V}$ to $V_{max} = 3.3\,\mathrm{V}$. The common mode voltage of the operational amplifier was adjusted to $V_{CM} = 1.7\,\mathrm{V}$, the resistors were set to achieve an amplification of approximately $A_V \approx 6\,\mathrm{dB}$. The input signal representing

a pixel was set to 2 V resulting in an out-of-range signal at the output.
The output signal with and without protection circuit was simulated. Without protection circuit, the amplitude of the output signal will be as large as the parameters of the amplifier allow. With protection circuit, the diodes become conductive and clamp the output voltage to the maximum and minimum specified range.
Moreover, other interferences can also occur on the signal, which can be intercepted by the protection circuit. Nevertheless, on the side of the DE an appropriate input protection must be implemented in addition.



(a) (b)

Figure 8.16.: SPICE simulation of the SAU circuit illustrating the influence of the protection circuit. (a) Simulation of a sequence of pixel signals with a pixel time of 40 ns and single-to-differential conversion. (b) Graph of the rising edge of a pixel signal. The additional delay, rise and fall times are negligible.

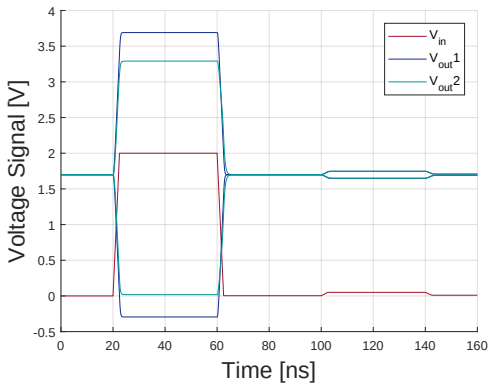


Figure 8.17.: SPICE simulation of the SAU circuit with a voltage input exceeding the allowed limits. The rectifying diodes become conductive and clamp the signal to their applied voltage.

8.2.4. Firmware Implementation

This section presents the implementation of the design proposed in the previous sections, to perform the real-time generation of modeled detector signals on the suggested FPGA-based hardware. Figure 8.18 details the implemented firmware on the PRE hardware setup.

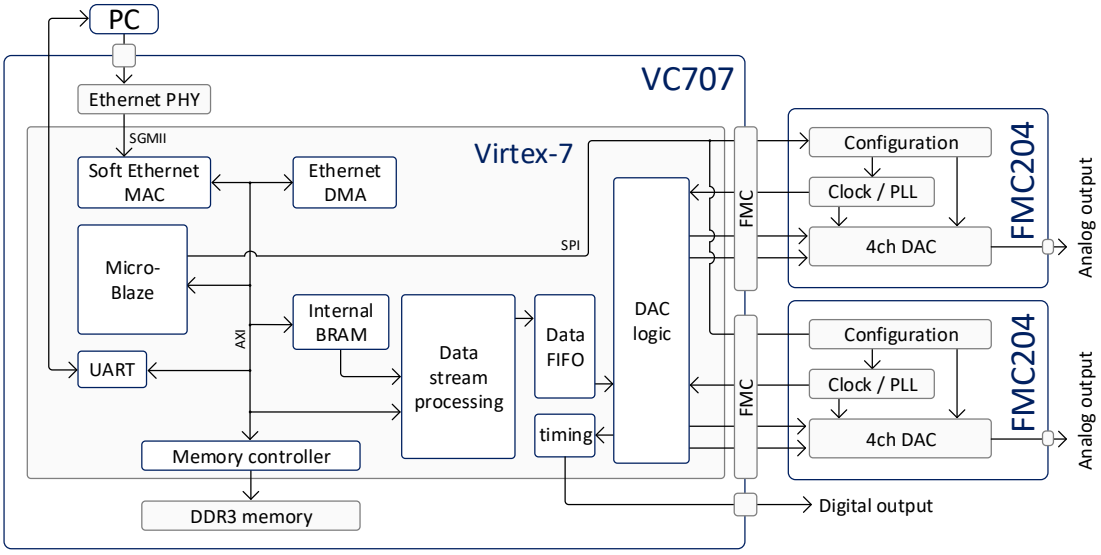


Figure 8.18.: Overview of the system setup with VC707 and FMC204.

The communication between the PRE software and the FPGA hardware is performed via an Ethernet network. An Ethernet-based communication enables to control and operate multiple PRE systems in an easy way with the same PC. For transferring the image data and control communication the Transmission Control Protocol (TCP) is used. A soft-core processor is implemented in the FPGA to handle the Ethernet connection by use of a LightWeight IP (lwIP) stack provided by Xilinx. The implemented processor is a Xilinx MicroBlaze, a 32-bit Reduced Instruction Set Computer (RISC) soft-core processor developed for XILINX FPGAs. The task of the MicroBlaze is to control operations and communications among different peripherals like double data rate (DDR) memory controller, BRAM interface or Universal Asynchronous Receiver Transmitter (UART). The interfaces of these blocks within the processor are performed via AXI4.0 streaming bus. Furthermore, the MicroBlaze is used to configure the parameters of the DAC and clock tree on FMC204 via an SPI interface, see section 8.2.2.

The main core of this system is the data processing unit which processes the offline generated data stream, a detailed description of this processing structure is given in section 8.1.1. This unit interfaces the image data stored in the DDR3 memory and sub-pixel configuration values stored in BRAM. The processed results are transferred to a dual port data FIFO. A DAC logic block fetches the data from the FIFO and interfaces the DACs. The FIFO separates the clock domains of data processing and data output. A clock distribution device on the FMC204 board generates a configurable, proper clock for triggering the DACs and the DACs logic units. A timing block generates digital timing signals like clock, trigger and synchronization signals for the DE to indicate a valid pixel or the start or end of a frame.

High-speed Analog-to-Digital Conversion Unit

The unit DAC logic is responsible for generating and transmitting digital signals to the high-speed DAC. Figure 8.19 depicts a block diagram of interfacing the DACs. The digital interface of the DAC is made up of $16\,\mathrm{bit}$ of DDR. In the required configuration, the digital interface of the DAC works with $200\,\mathrm{MHz}$, which corresponds to a data rate of $400\,\mathrm{Mbit/s}$ for each data bit. To operate at high frequencies, built-in output serializer/deserializer (SERDES) were used. Using SERDES blocks eases design of high external data rates, while keeping the internal data rate at a moderate level. For interfacing the DAC, only the serializer functionality of this block is needed. SERDES drivers accept a lower rate parallel input data and output a serial stream using a shift register at a frequency multiple of the data bit width. The SERDES block uses two clocks, CLK and CLKDIV, for data rate conversion. CLK is the high-speed serial clock, CLKDIV is the divided parallel clock [125].
In this case, the SERDES were used in an 4:1 DDR configuration with a parallel clock of $50\,\mathrm{MHz}$ and a high-speed serial clock of $200\,\mathrm{MHz}$. The internal signals are running in single data rate (SDR) and the external signals are configured in double data rate.

Successful generation of high-speed signals depends on a proper clocking scheme and synchronized clocks. A clock generator device AD9517-3 from Analog Devices is used to generate all clocks within the DAC interfacing logic [5]. This device is generating two clocks, a $100\,\mathrm{MHz}$ clock for FPGA internal, and a $400\,\mathrm{MHz}$ high-speed DAC sample clock.
This $100\,\mathrm{MHz}$ FPGA internal clock is driven to an internal PLL primitive to generate two clocks from this input. A $200\,\mathrm{MHz}$ high-speed clock for the serializer block and a $50\,\mathrm{MHz}$ clock for parallel data. The digital clock (DCLK) of the DAC is generated by placing a "1010" vector at a SERDES block, resulting in a $200\,\mathrm{MHz}$ clock. This ensures

precise alignment with the data stream. This clock is driven to an internal DLL within the DAC to generate two clocks with 0° and 180° phase shift. With these clocks the DDR data is transferred into a DAC FIFO. The data is clocked out from this FIFO with the high-speed sample clock of 400 MHz.

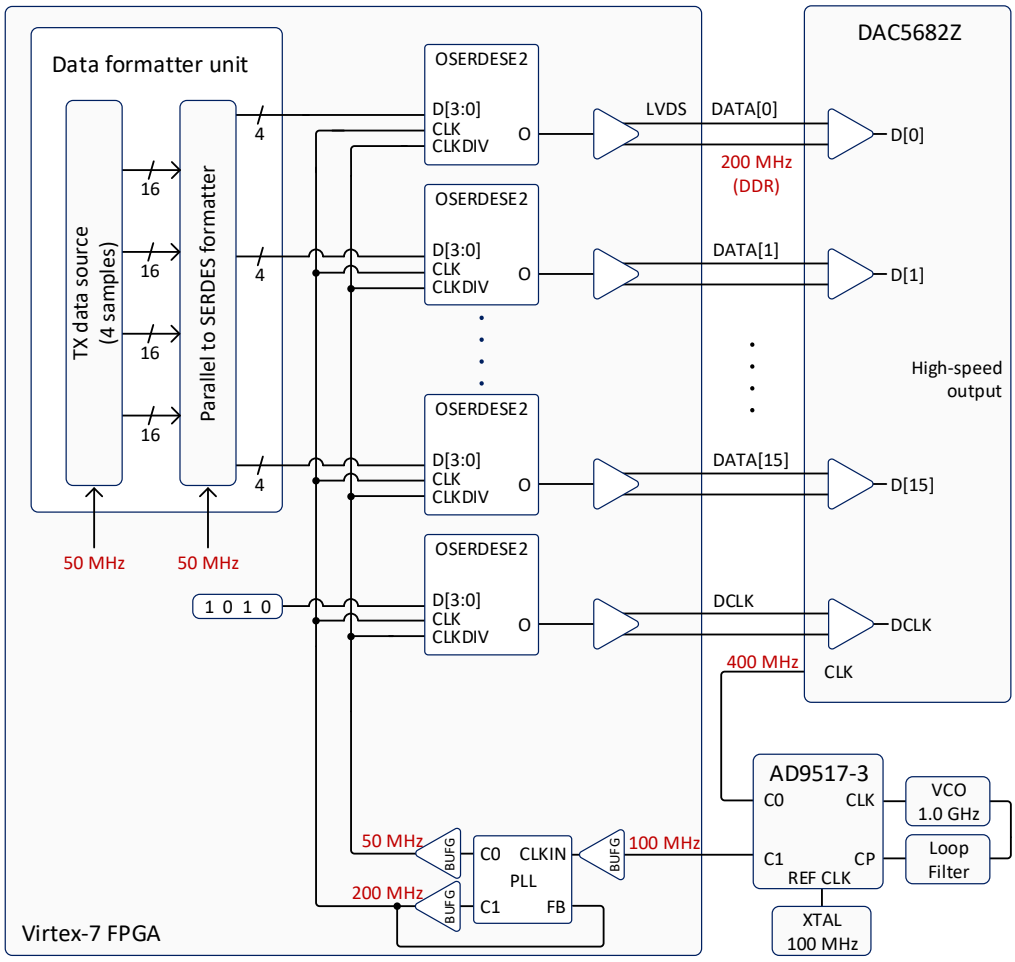


Figure 8.19.: Block diagram of FPGA-based LVDS data flow to DAC as well as clock generation and distribution. Driving the data to the DAC using SERDES blocks requires a parallel load of four consecutive samples to shift registers performed in the data formatter unit [104].

8.3. Emulator Software System

A clear graphical user interface (GUI) is designed to set the parameters of the models to perform an efficient simulation, see figure 8.20. The parameters for signal generation, detector configuration and detector characteristics can be varied to obtain different output signals. The modeled frame stack is displayed and can be interactively inspected frame- and pixel-wise. By switching the parameters on and off, the direct influence on the pixels and frame can be observed. Moreover, the GUI provides an interface to transmit the generated frame stack to the PRE hardware via Ethernet and to define the setup of the hardware emulator, like configuration mode, number of used DACs or output speed.

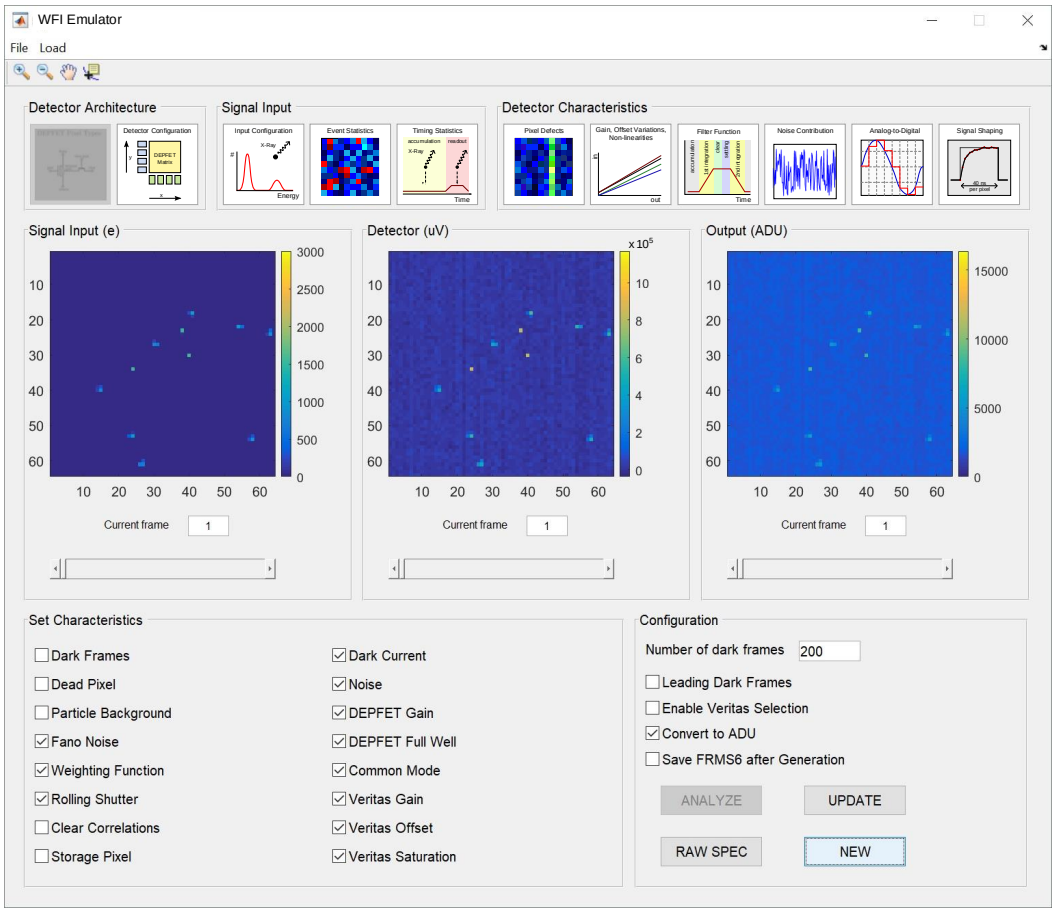


Figure 8.20.: Screenshot of the WFI DEPFET detector modeling user interface. Simulation parameters for signal generation, detector configuration and detector characteristics can be set. The main window illustrates the signal input in electrons and the output in Volts or Analog-to-Digital Unit (ADU).

9. End-to-End Verification of the Wide Field Imager

Within this chapter, the end-to-end verification method of the WFI signal processing chain is presented. First, results of verification of the PRE models are given. This is done by comparing measured detector effects with modeled detector effects, given in section 9.1. Further, the PRE processing is compared against the SIXTE simulation tool with a scientific observation as input. Afterward, the WFI verification setup with the present breadboard model of the Detector Electronics Frame Processor is outlined in section 9.2, followed by a verification plan. Finally, scientific verification examples of the WFI signal processing chain are presented.

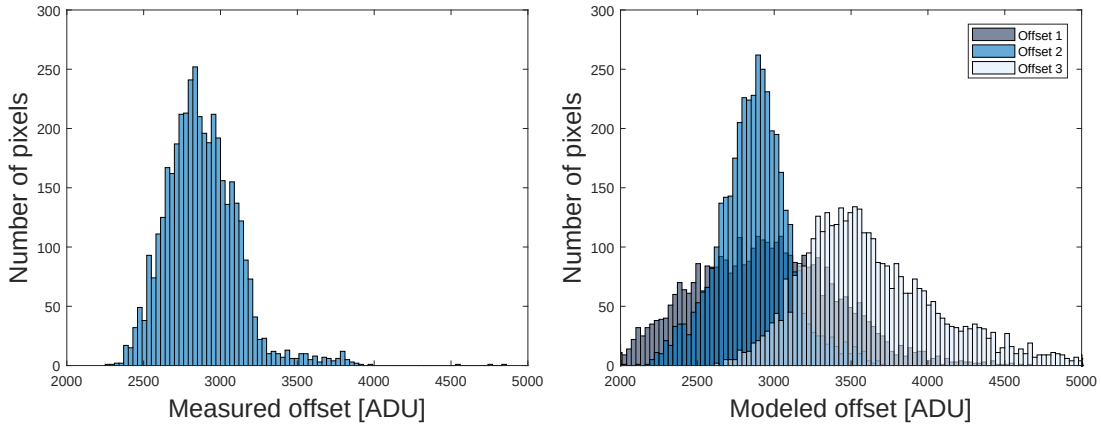
9.1. Verification of PRE Models

The PRE models introduced in section 7 can be verified by comparing simulated frame stacks with real detector measurements. The parameters of the models are set to fit the characteristics of the detector system. In addition, the parameters are adjusted in a range beyond the measured range to display special scenarios that can not be generated with a real system in a simple way.
The emulated data is stored in a so-called frame file and analyzed in the same way as the measured data. The used software for data analysis is a ROOT based offline Analysis ROAn [56]. The measured and modeled data are analyzed regarding offset, common mode, noise, gain, pattern statistics and spectral performance. In the following, the measured and modeled effects are compared.

All measurements shown in this chapter were performed with a WFI DEPFET prototype sensor with 64 $\times$ 64 pixels and a pixel size of $130\,\mu\mathrm{m}$ in square. The sensor was read out with a Veritas ASIC in source-follower mode. The detector was illuminated with a Fe-55 source, which is used as standard calibration source. For this thesis, the source is considered to emit X-ray photons with energies of $5.895\,\mathrm{keV}$ (Mn-K-α) and $6.492\,\mathrm{keV}$ (Mn-K-β). Following emission probabilities of Fe-55 were determined:
$p(Mn-K_\alpha, 5.895\,\mathrm{keV}) = 0.2450$ and $p(Mn-K_\beta, 6.492\,\mathrm{keV}) = 0.0338$
The ratio of $p_{K\beta}/p_{K\alpha}$ results to 0.138 [96].

Offset

The offset signal consists of the pixel leakage current in addition to the respective Veritas channel offset, amplified with the respective channel gain. The offset is calculated by taking a pixel-wise average of a distinctive number of non-illuminated frames. Figure 9.1a depicts the histogram of the measured offset values. In figure 9.1b, histograms from three modeled frame stacks with different offset characteristics are shown.



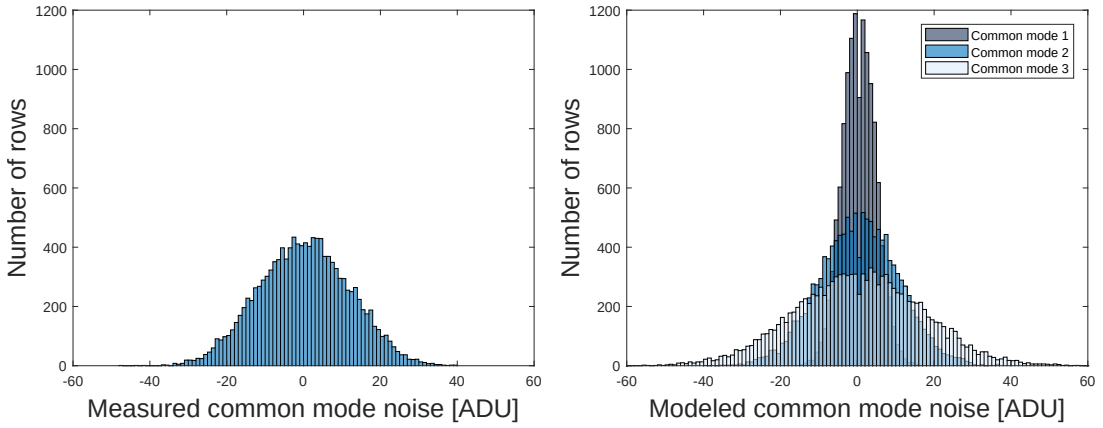
(a) (b)

Figure 9.1.: Measured versus modeled DEPFET detector offset. (a) Histogram of measured offset values showing a typical distribution. (b) Histogram of three modeled offset distributions.

The three offset histograms in figure 9.1b show the performance of the PRE models. Despite emulation of a realistic data compared to the measurement (*offset2*), two different offset characteristics are shown. *offset1* represents offset values with the same mean value as the measured data but a wider distribution. Thus, the offset characteristics are more inhomogeneous. This behavior can occur due to manufacturing effects or shift of threshold voltages due to radiation damage in orbit.
offset3 illustrates an offset histogram with a higher mean value. This can be caused by a higher leakage current in consequence of radiation exposure in the orbit or temperature drift. By modeling an offset drift over time, the degradation of the detector performance and the influence on data analysis and scientific results can be studied on ground.

Common Mode Noise

The common mode noise is defined as row-wise correlated noise due to external disturbances of the electronic systems, see section 7.4.5. The common mode noise is obtained by taking the median value of each row of the respective readout ASIC.
Figure 9.2a shows the measured common mode noise values plotted in a histogram for representative 200 frames. Figure 9.2b depicts the histograms of three modeled frame stacks with different common mode noise.



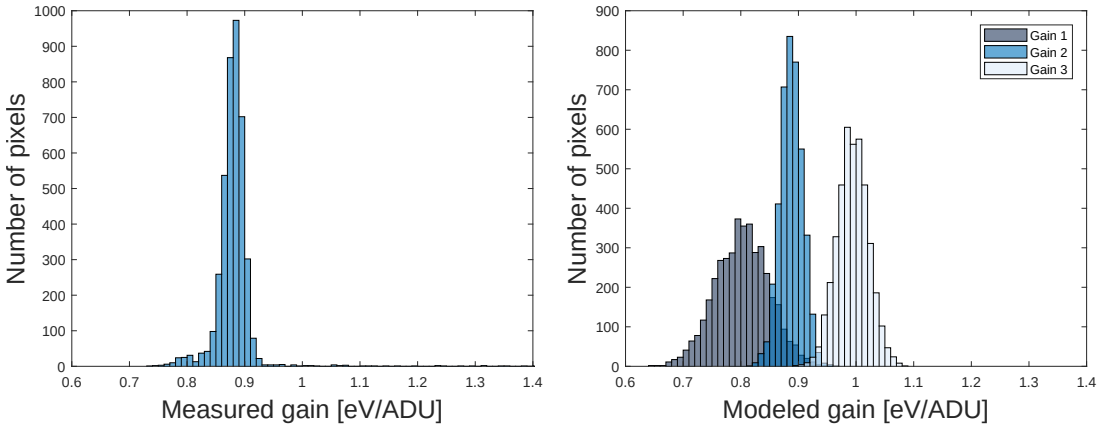
(a) (b)

Figure 9.2.: Measured versus modeled DEPFET detector common mode noise for 200 frames. (a) Histogram of measured common mode noise values. (b) Histograms of three modeled frame stacks with varying common mode noise contributions.

In figure 9.2b, *common mode 2* is modeled to fit the measurement. The parameters of the common mode model can be set to generate data with higher common mode effect (*common mode 3*) or lower noise contribution (*common mode 1*).
The common mode noise directly influences the quality of the captured data and thus the noise performance and energy resolution of the camera system. As presented in section 5.2.2, the common mode noise needs to be extracted by subtracting the median of each row on-board of the instrument. There are different approaches to calculate the median value of a set of data [7]. By emulation of different common mode noise distributions or different common mode noise per readout ASIC, different algorithms and their robustness can be evaluated.

Gain

Since every DEPFET pixel has its own integrated first amplifier, the gain homogeneity is an important issue. The gain is the product of DEPFET pixel gain and Veritas column amplification. The gain of a detector is calibrated by determining the $Mn - K_\alpha$ peak from the calibration spectrum for every pixel.
The measured and calibrated gain distribution is shown in figure 9.3a. Figure 9.3b depicts three modeled gain distributions.



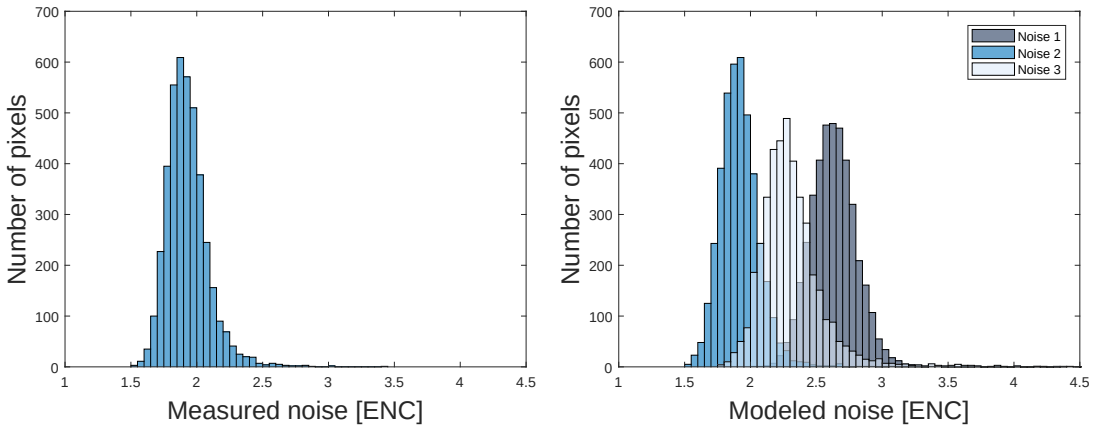
(a) (b)

Figure 9.3.: Measured versus modeled calibrated DEPFET detector gain. (a) Histogram of a measured gain distribution. (b) Histograms of three modeled gain distributions showing a more inhomogeneous gain distribution, a fitted distribution to the measurement and a distribution with higher gain.

The gain distribution in histogram *gain 2* is adjusted to the gain distribution of the performed measurement. Two other gain distributions are modeled, *gain 1* has a wider distribution, representing a more inhomogeneous gain dispersion. *Gain 3* has a similar distribution function as the measured gain, but with a higher mean value.
The pixel-wise gain of a sensor is determined by the geometric structure of the transistors of the pixels. Various sensors with different gain characteristics and dispersions can be modeled, by adjusting the gain model. Moreover, it is expected that the gain distribution will become more inhomogeneous due to radiation exposure in orbit over time, see section 5.3.

Noise

The noise in the detector system is mainly caused by thermal, shot and $1/f$ noise, as explained in section 4.2. Noise in an imaging or spectroscopic sensor cannot be corrected. It directly influences the energy resolution of the device. The pixel-wise noise is calculated by taking the rms value of offset and common mode corrected pixel signals without illumination.
A typical noise distribution of a DEPFET detector measurement is shown in figure 9.4a. An extracted gain map is used to calculate the noise values in units of eV. With equation 4.7 this can be translated to an equivalent noise charge (ENC). Figure 9.4b depicts histograms of three modeled frame stacks with divergent noise distribution.



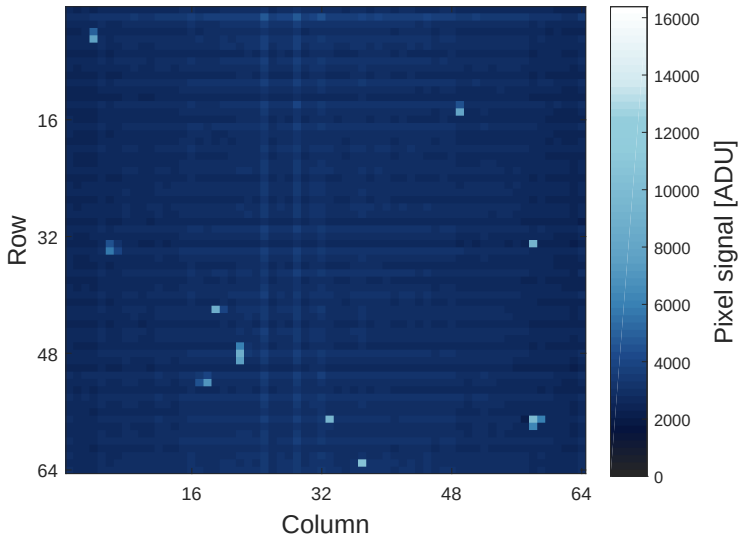
(a) (b)

Figure 9.4.: Measured versus modeled DEPFET detector noise. (a) Typical noise distribution of a DEPFET measurement. (b) Histograms of three modeled noise distributions with varying noise contribution.

The modeled noise distribution *noise 2* in figure 9.4b is modeled according to the measured noise. The noise distribution *noise 1* and *noise 3* show a higher noise mean value and wider distribution function as the measured one.
A higher noise can be caused for example by radiation damage, crosstalk on sensitive lines, temperature drift or external disturbances. By investigation of different noise values on the signal processing chain, the influences of the noise on system performance can be studied.

Pattern Analysis

The charge of an X-ray photon splits up across up to four pixels, as explained in section 7.2.2. Furthermore, pattern arise which extend over more than 2×2 pixels caused by effects like pile-up, inter-frame splits or misfits. Figure 9.5a depicts a measured frame, with signals from X-ray photon input. Figure 9.5b to 9.5f are segments of this frame, illustrating individual events. Valid and invalid patterns are included in this frame.



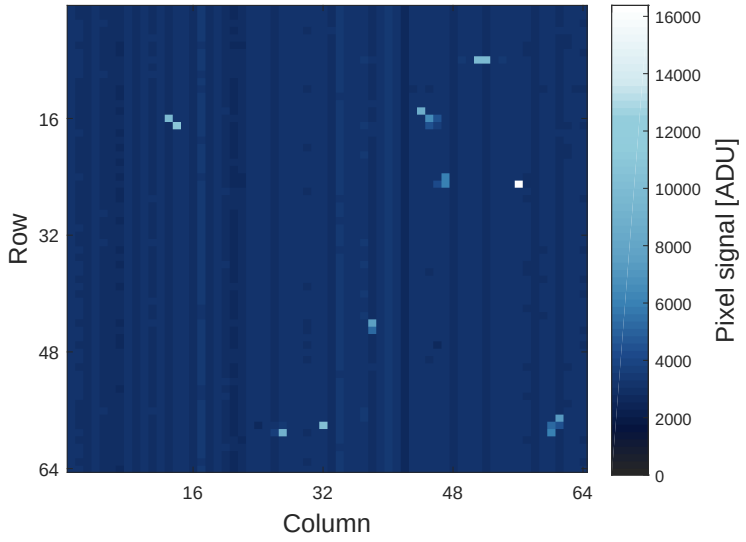
(a) measured full frame

(b) SNG (c) DBL (d) TRP (e) QUD (f) invalid

Figure 9.5.: Pattern analysis of a measured frame. Cutouts of the frame show valid and invalid pattern.

Complementary to the measured frame, a modeled frame is depicted in 9.6a. All patterns included in the measured frame shown above can be modeled. Moreover, it is possible to set specific patterns which represent special challenges in on-board processing, as depicted in figure 9.6b to 9.6d. Figure 9.6e and 9.6f depict two special cases of valid pile-up. In figure 9.6e the effect is illustrated, caused by the deposition of the energy of two photons in just one pixel. Figure 9.6f shows two neighboring pixels, each exposed with an individual photon. In both cases, a valid pattern is detected. It

cannot be recognized that the measured charge origins from two photons. Thus the measured result is misinterpreted, a higher energy identified for this pattern.



(a) modeled full frame

(b) invalid (c) 2x SNG (d) SNG & QUD (e) valid pile-up (f) valid pile-up

Figure 9.6.: Pattern of a modeled frame. Sections of this frame show special constellations of pattern: (b) invalid pattern caused by pile-up, (c) two single events which are diagonally opposite, (d) a single and a quadruple event, touching at the edge, (e) a valid single pattern, but with higher signal amplitude caused by pile-up, (f) a valid double pattern caused by two neighboring single patterns.

Energy Spectrum

A detector spectrum is obtained by feeding all pixel values of a measurement in a histogram. Processing of the measured data in advance leads to a calibrated detector spectrum. Therefore, offset and common mode correction, gain calibration, event filtering and recombination are performed.

Figure 9.7 depicts a measured and a modeled detector spectrum of an Fe-55 source. The simulated energy spectrum corresponds very well to the measured one. All expected spectral features are visible. In the measured spectrum a slightly decrease at the main peaks to lower energies can be observed. This is most likely due to partial charge losses. Furthermore, a difference in the peak-to-background of about a factor of 1.5 can be noticed. This can be caused by effects in the entrance window, which can be considered in a future model.

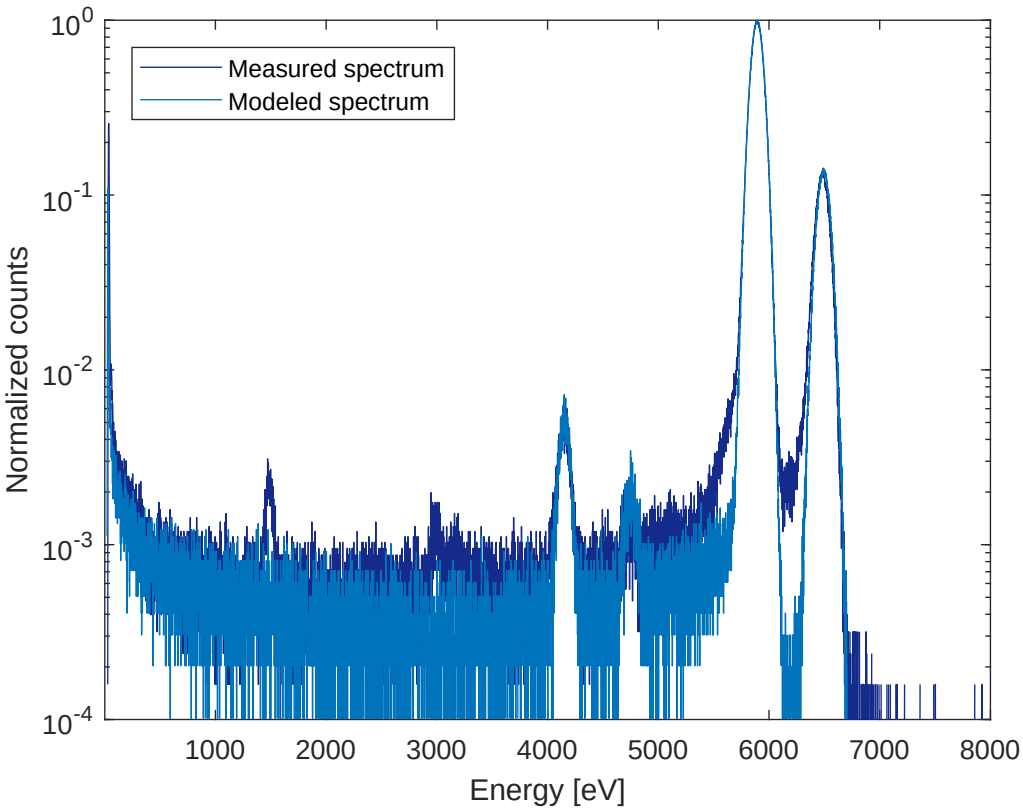


Figure 9.7.: Comparison of the calibrated energy spectrum performed by an Athena prototype detector with a simulated spectrum by the PRE models.

Verification of the PRE based on SIXTE Simulations

Another method for verifying the performance of the emulator models is the comparison with scientific simulation tools. The official simulation program of the Athena mission is the SIXTE simulator, developed by ECAP, introduced in section 6.3.1. SIXTE allows to undertake instrument performance analysis and to generate simulated event files for mission- and analysis studies. These simulations start with a description of a real measurement, such as an astronomical observation and simulate the outcome by modeling the whole instrument.
Input of a SIXTE simulation is a source description, which specifies the properties of X-ray sources taken from an X-ray source catalog. The source description includes a list of source positions, fluxes, corresponding spectrum or images. Starting from this source description and a precise model of the telescope, a list is generated which contains all photons emitted from all sources that are visible to the instrument. In a further step, these photons are projected onto the detector by using the energy and position dependent Point Spread Function (PSF) of the X-ray optics. This list is called impact list and includes arrival time in second, energy in $\mathrm{electronvolt}$ and position in meter of all photons hitting the detector. Output of the simulation is an event list which reflects the output of the detector. This is performed by models including detector effects and readout [121].

To further verify the PRE models, the outcome is compared against the output of a SIXTE simulation. Figure 9.8 depicts the applied method. An impact list, generated with the SIXTE simulator, is either processed by the SIXTE models or the PRE models. The outcome for both is an event list with entries of energy, arrival time and pixels, which can be compared against each other.

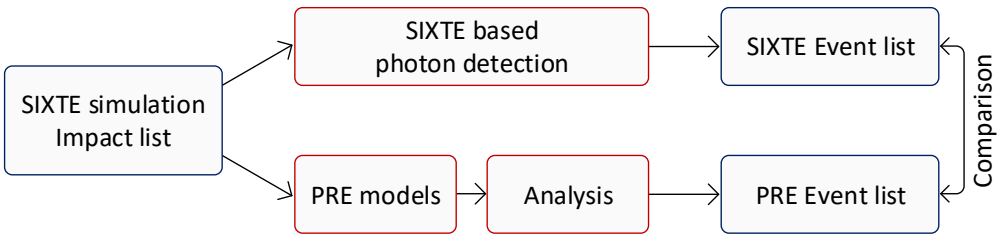
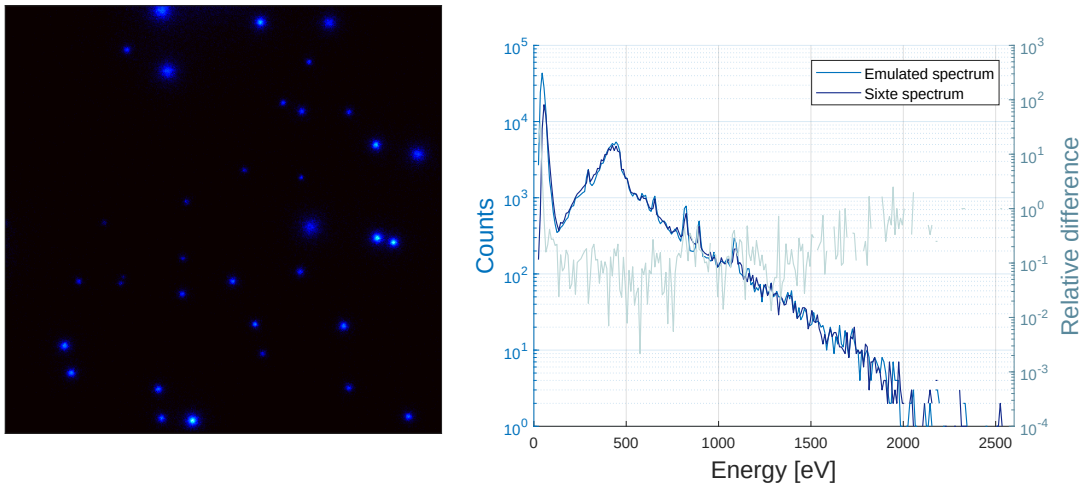


Figure 9.8.: Verification method of the PRE models against the SIXTE simulations.

For this verification, the simulated impact list is based on a $100\,\mathrm{ks}$ observation of the Chandra Deep Field South (CDFS) with only one quadrant of the WFI large detector. Based on the impact list, the SIXTE event list and the PRE event list can be calculated.

Figure 9.9a shows the intensity map of the CDFS observation derived from the PRE event list. The energy spectrum of all sources within this simulation, obtained from the PRE and SIXTE event list, and the relative difference of the two spectra, is depicted in figure 9.9b. The two spectra show a satisfying accordance.



(a) (b)

Figure 9.9.: SIXTE simulation in comparison to the emulator performance. (a) 100 ks observation of the Chandra Deep Field South with one quadrant of the WFI large detector. (b) Energy spectra, obtained either by SIXTE simulation or the PRE models with the relative difference of the spectra.

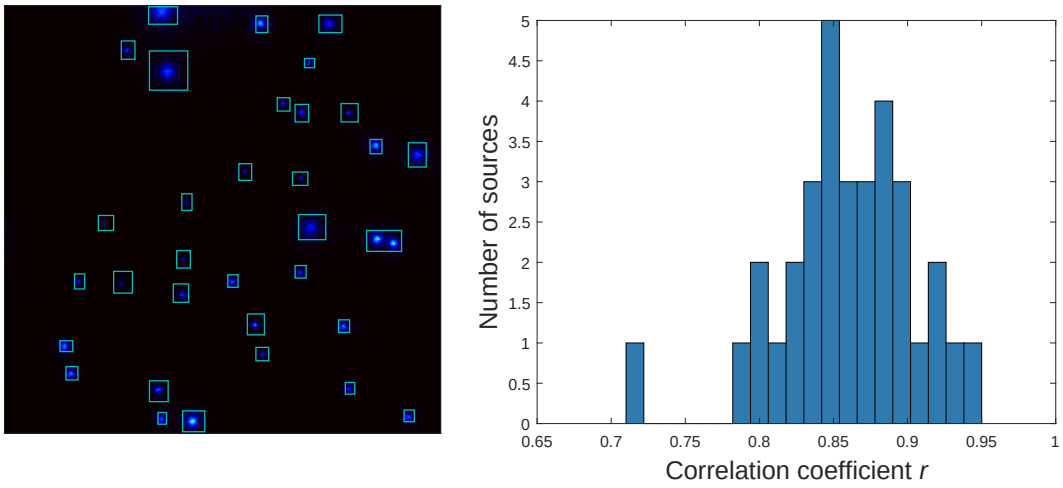
The mean relative deviation of the simulated and the emulated spectrum in a limited energy range of 200 eV to 2000 eV is lower than 9.5 %.

Further, the correlation of two observation maps, obtained either by the PRE event list or the SIXTE event list can be performed. Therefore, all energies in the individual pixels are integrated over the entire observation time.
The correlation between two images can be described by the Pearson's correlation coefficient, which is defined as

$$r = \frac{\sum (x_i - x_m)(y_i - y_m)}{\sqrt{\sum (x_i - x_m)^2}\sqrt{\sum (x_i - x_m)^2}} \tag{9.1}$$

where x_i and y_i are intensity values of the i_{th} pixel in 1st and 2nd image respectively. Also, x_m and y_m are mean intensity values of 1st and 2nd image respectively [91]. The correlation coefficient has the value $r = 1$ if the two images are absolutely identical, $r = 0$ if they are completely uncorrelated and $r = -1$ if they are completely anti-correlated [41].

For the whole images a correlation coefficient of $r = 0.91$ was obtained, according to equation 9.1. For a closer examination of the correlation of the two images, the algorithm is applied only to the areas of the image that contain X-ray sources. Thereby, dark areas that hold no image information are not included in the calculation as they would falsify the result. Depending on the spatial extension of the X-ray sources, areas with a size of about up to 50 times 50 pixels were chosen.
Figure 9.10a depicts the observation map with selected X-ray sources for which the correlation coefficient is calculated individually. The distribution of the coefficients is shown in figure 9.10b. The obtained correlation coefficient for the selected X-ray sources range from $r = 0.72$ to $r = 0.95$ with a mean value of $r = 0.85$.



(a) (b)

Figure 9.10.: (a) Selected X-ray sources for the image correlation of the integrated energy maps. (b) Histogram of the coefficients r of the correlation of the emulated energy map and the simulated energy map with SIXTE.

Comparing the outcome of the PRE models with the SIXTE simulation tool is a good way of estimating the performance of the PRE models. The spectral performance, depicted in figure 9.9b, shows a relative difference of less than $10\,\%$. The correlation of the outcome which also considers spatial information as depicted in figure 9.10b, has a value of around $r = 0.85$ with $r = 1$ indicating full consistency.
The differences in the outcome of the PRE models and the SIXTE simulation can be due to different models concerning photon detection, charge splitting, detector characteristics and signal readout or parametrization of the models in the simulation chain. Further, adjustments of the models and comparisons could be considered in order to achieve a higher level of conformity. Nevertheless, the PRE models show a satisfactory accordance.

9.2. Verification Setup and Plan

The PRE is designed in such a way that it can be used in all phases of the project. At present, the project is in development phase. The signal processing chain of the WFI in this phase is built up with a DE FP breadboard model as outlined in section 5.2.3.
To apply the end-to-end evaluation method, the developed system is setup according the scheme in figure 3.1. Therefore, the PRE is interfaced to the FP breadboard model, as depicted in figure 9.11.

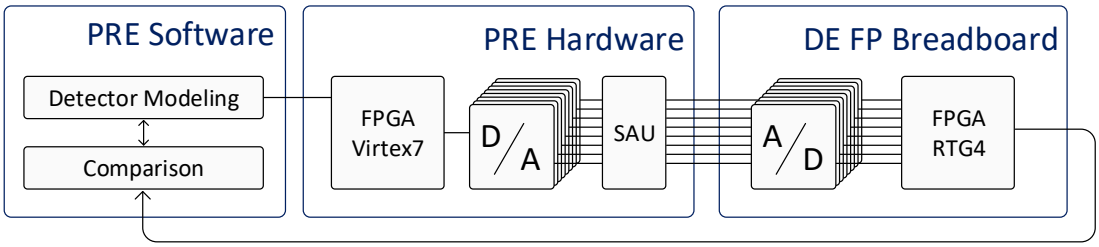


Figure 9.11.: Overview of the verification setup. The PRE is connected to the breadboard model of the DE FP.

The PRE consists of a software part to model the detector characteristics and X-ray input and to generate frame stacks. A hardware part serves for data processing of the frame stack and conversion into an analog output signal in real-time. Main task of the FP breadboard model is to digitize the analog data and perform pre-processing as explained in section 5.2.2. Output of the FP breadboard is an event list, which stores the filtered events, with pixel coordinates and a timestamp. A feedback loop from the processed output data of the FP breadboard to the PRE software opens the possibility to compare input and output signals.

In the following, consecutive steps for verification of the signal processing chain are presented.

1. X-ray input and detector modeling
First the system characteristics of the modeling environment are set. Depending on the requested test scenario, X-ray input and detector parameters are adjusted. This is performed with a comprehensive software packet and a GUI, illustrated in section 8.3.

2. Frame stack generation
Subsequently of configuration of all emulator parameters, the frame stack is generated and can be stored as a frames file (frms6, [55]). This file can be analyzed offline with the mission specific analysis tool in advance, to have a first-look on the results including spectroscopic performance of the modeled frame stack.

3. Sub-pixel resolution configuration
Next step is to configure the sub-pixel resolution data, as explained in section 8.1.1 and 8.1.2 in order to model high-speed characteristics and disturbances pixel-wise. Depending on emulated matrix size, each modeled ASIC can be configured with a separate set of sub-pixel parameters.

4. Hardware processing and generation of analog signal
Following the configuration of the scientific data, the PRE hardware is configured with the number of used DACs and output speed of the generated data. All modeled data and parameters are transferred on the PRE hardware platform.

5. Raw data measurement with DE FP breadboard
The analog output of the PRE is connected to the DE FP breadboard. At first, the analog data is converted into a digital signal. The FP breadboard offers the possibility to obtain this data for debugging purposes via a high-speed raw data interface. By comparing the digitized data and the modeled frame stack pixel-wise, conclusions can be drawn about the quality of the emulation process, the transmission path between the converters and the digitization.

6. Data pre-processing on DE FP breadboard
Subsequently, the measurement can be iterated with on-board data pre-processing on the DE FP breadboard model in real-time. The pre-processing steps include, offset and common mode correction as well as event filtering, as described in section 5.2.2. Output is an event list containing the signal of the filtered events, their coordinates and a timestamp. Different implementations and configurations of the on-board processing can be analyzed and evaluated with the same stack of input data to determine the optimal performance.

7. Closed-loop: Comparison of input and output
A feedback path from the FP output to the PRE software environment enables comparisons of the processed output data and the adjusted input data. Specific image processing algorithms allow to state conclusions about performance and quality of the signal processing chain.

8. Iterative process
Continuous variation of the X-ray input signal and modeled detector characteristics with subsequent data pre-processing and comparison of input and output data is an iterative process, which leads to optimization of the signal processing chain. Various scenarios can be implemented to determine the influence on the processing chain and the astrophysical data in advance.

9.3. PRE-based Verification Examples

For performance verification of the WFI signal processing chain with the PRE and for transfer of WFI requirements (see table 2.1) to technical specifications, various scenarios are tested and analyzed. In the following, four exemplary verification approaches are given.

9.3.1. Noise Threshold Analysis

An important task of the DE FP is to perform event filtering. To distinguish noise signals from those generated by X-ray photons, a primary threshold is applied to the signals. Pixels with a signal below the primary threshold are discarded and pixels with a signal above the threshold are further processed. Neighboring pixels are compared with a secondary threshold to investigate them on split events. Usually the threshold values are set for each pixel as a multiple of the standard deviation σ its noise. It is essential to find suitable values for the thresholds, with regard to the energy resolution and data reduction rate.
With the PRE, effects of different threshold levels can be studied. This is performed by applying various threshold values to the same frame stack generated with the PRE. Output of the event filtering is an event list with pixel signals, pixel coordinates and frame numbers which can be compared to the input event list.
Therefore a frame stack is generated with signals from X-ray photons with an energy of $6\,\mathrm{keV}$ distributing their charge affecting one to four pixels of a DEPFET matrix with 64×64 pixels. The data is generated without timing effects like misfits, pile-up and influences due to rolling shutter mode. Only valid patterns are modeled. In total $1.2 \cdot 10^6$ events are generated with an equivalent noise charge of 4 electrons.
The generated data stack is analyzed with different values of primary and secondary threshold values. Figure 9.12 depicts the number of detected, recombined events in percentage of the number of generated input events. It can be seen that more events are detected than in the input frame stack. If the threshold level is too low, noisy pixels are detected as valid events.
Figure 9.13 shows the percentage of incorrectly detected pixels, which are noisy pixels and not detected pixels. A lower secondary threshold value decreases the number of not detected pixel signals but increases the number of incorrectly detected signals.

By applying different threshold values to the frame data, more or less events are registered. Especially for detection of small signal energies, relevant for the WFI, it is indispensable to set the appropriate threshold values. With lower energies it becomes

more likely, that in case of a split pattern, not all the pixel signal is detected, due to signals lower than the second threshold.

Moreover noisy pixels can be detected as events, which worsens spectral performance. Measured noise values, obtained during operation of the WFI in space, can be loaded to the PRE. Thus realistic investigations on the threshold levels can be performed on ground. Influences of the levels on event detection and data rate can be gained.

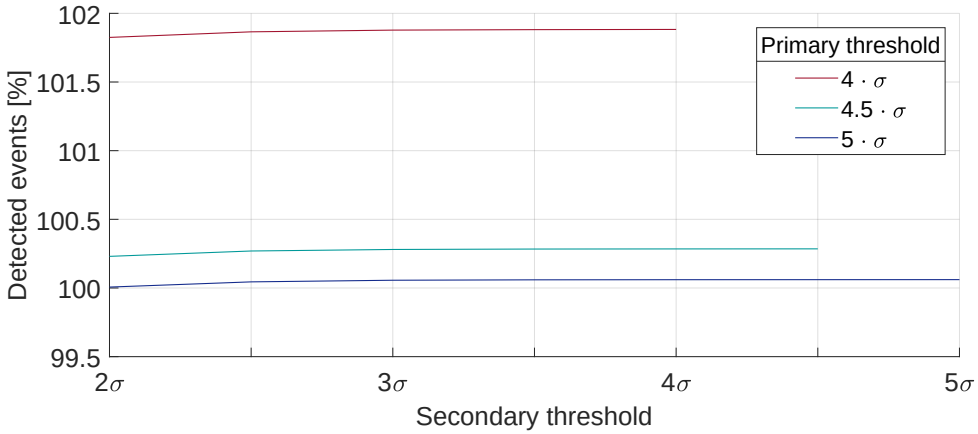


Figure 9.12.: Analysis of different threshold levels on detected events: A lower primary threshold value leads to more detected events while influence of the secondary threshold value is quite low [77].

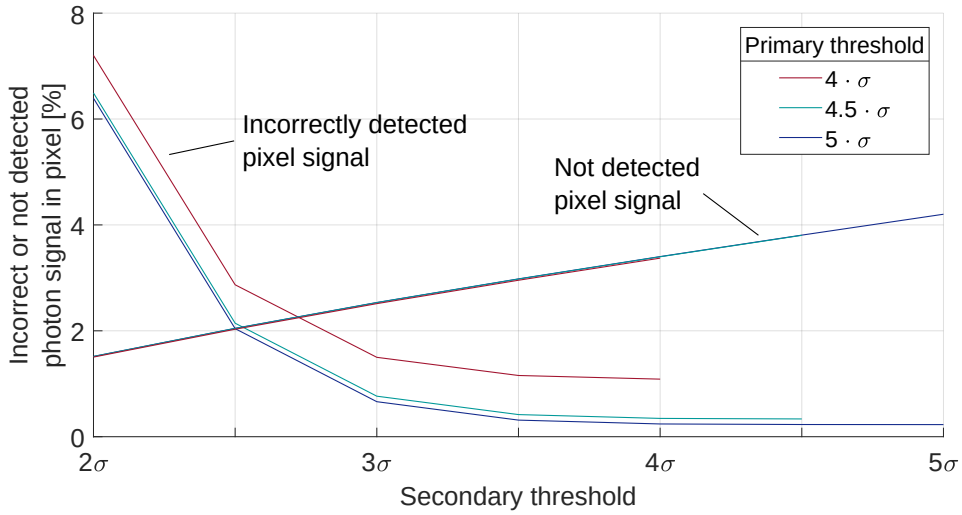


Figure 9.13.: Analysis of different threshold levels on detected pixel signal: An increasing primary threshold leads to more incorrectly detected pixels. An increasing secondary threshold decreases the number of incorrectly detected pixels but increases the number of not detected pixels [77].

9.3.2. Investigation of ADC Resolution on Spectral Resolution

The selection of a suitable ADC for the DE of the WFI strongly depends on the science requirement of the project. Factors such as resolution, sampling rate, number of channels, power consumption and radiation hardness must be investigated. Studies have shown that many available space qualified ADCs can already be excluded and three converters need to be considered more closely. Table 9.1 lists three eligible components and their relevant parameters [4], [100], [105]. The relevant space qualified

Table 9.1.: Overview of the key parameters of three space qualifies analog-to-digital converters.

Parameter	**AD9254S** (Analog Devices)	**RHF1401** (STMicroelec.)	**LM98640QML** (Texas Instruments)
Number of channels	1	1	2
Resolution (bit)	14	14	14
ENOB (bit)	11.3	10.6	10.3
Sample rate $(MSPS)$	150	20	40
Power (mW)	515	85	178/ch
TID $(krad(Si))$	100	300	100
SEL $(Mev - cm^2/mg)$	120	120	120

ADCs provide an ideal resolution of $14\,\mathrm{bit}$ but differ in the effective number of bits (ENOB). ENOB is a measure of the dynamic range of an ADC. The resolution of an ADC is specified by the number of bits used to represent an analog value. However, all real ADC circuits introduce noise and distortion. ENOB specifies the resolution of an ideal ADC circuit that would have the same resolution as the circuit under consideration [79].

The influence of the resolution of the ADCs on the measured spectrum of the observed source can be performed by simulation. Therefore the simulation environment of the PRE is used. The applied method is to perform a simulation of a source in the required energy range and to process it further with a simplified simulation model of an ADC with adjustable resolution, reference voltage, gain and offset, as shown in Figure 9.14. The transfer function is assumed as ideal and linear without distortion. The generated frame stacks are analyzed and compared to examine the influence of the ADC.

The parameters of the PRE were set to realistic values according to measurements performed with the Athena prototype detectors. The gain of the FEE model was set

to cover the range from $0\,\mathrm{keV}$ to $18\,\mathrm{keV}$ to cover the WFI science requirements, see table 2.1. Three simulations were performed with mono-energetic X-ray photons at an energy level of $200\,\mathrm{eV}$, $1\,\mathrm{keV}$ and $7\,\mathrm{keV}$.

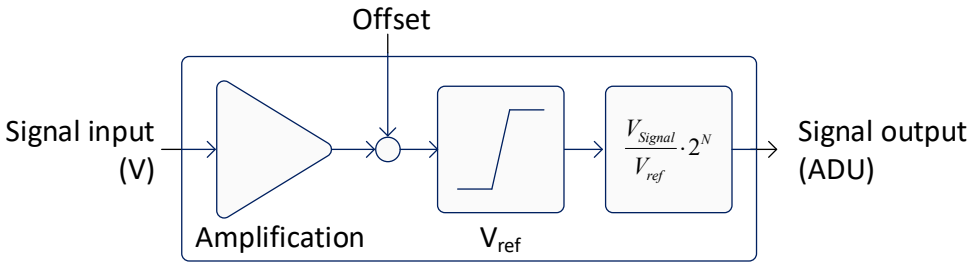


Figure 9.14.: Block diagram of a simplified ADC model with parameters gain, offset, reference voltage V_{ref} and resolution N.

Figure 9.15 depicts the results of the investigations of different ADC resolutions on spectral energy resolution and calibrated noise for simulated X-ray photon energies of $200\,\mathrm{eV}$, $1\,\mathrm{keV}$ and $7\,\mathrm{keV}$. The analyzed data is fitted with an exponential function.
For input of $200\,\mathrm{eV}$ X-ray photons, the results are shown in figure 9.15a and 9.15b. In the range of the three relevant ADCs the spectral energy resolution of all valid events worsens by approximately $3\,\mathrm{eV}$ with decreasing ADC resolution.
The value of calibrated noise changes from 2.8 electrons for an ADC with ENOB of $10.3\,\mathrm{bit}$ to 2.4 electrons for an ADC with ENOB of $11.3\,\mathrm{bit}$.
Figure 9.15c and 9.15d show the spectral energy resolution and calibrated noise versus ADC resolution for simulated X-ray photons with an energy of $1\,\mathrm{keV}$. The energy resolution decreases by almost $2\,\mathrm{eV}$ changing the ADC resolution from $11.3\,\mathrm{bit}$ to $10.3\,\mathrm{bit}$. The calibrated noise worsens by approximately 0.4 electrons.
Figure 9.15e and 9.15f depict the correlation of energy resolution, noise and ADC resolution for an X-ray input of $7\,\mathrm{keV}$. In this higher energy range, the reduction of ADC resolution has a lower impact on spectral resolution. This impact on the energy resolution is only about $1\,\mathrm{eV}$. The reason for this is the higher amplitude of the input signal compared to the noise floor of the frame data. The calibrated noise worsens for the relevant ADCs by 0.4 electrons. Table 9.2 summarizes the results of the ADC investigation comparing spectral energy resolution and calibrated noise.

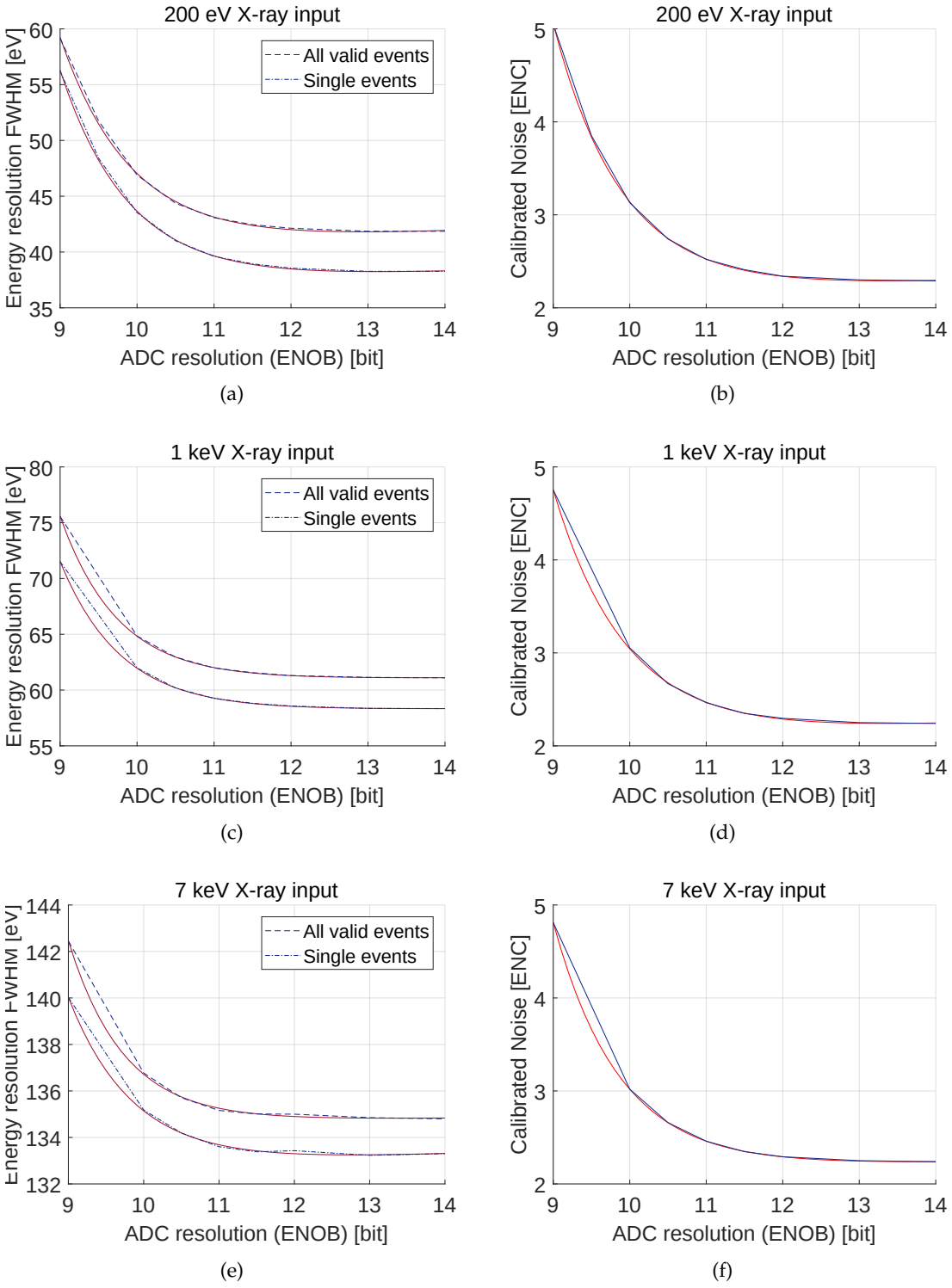


Figure 9.15.: Energy resolution and calibrated noise versus ADC resolution simulated with X-ray photons with energies of 200 eV, 1 keV and 7 keV.

Figure 9.16 summarizes the results of ADC resolution analysis. The degradation of the energy resolution is depicted over the ADC resolution with the value of $11.3\,\mathrm{bit}$ ENOB as baseline reference. Comparing these values and the results summarized in table 9.2 with the WFI science specifications, all three ADCs fulfill the requirements. Since it can be assumed that the detector will deteriorate in performance over time in orbit, it is recommended to design the electronics with sufficient margin.

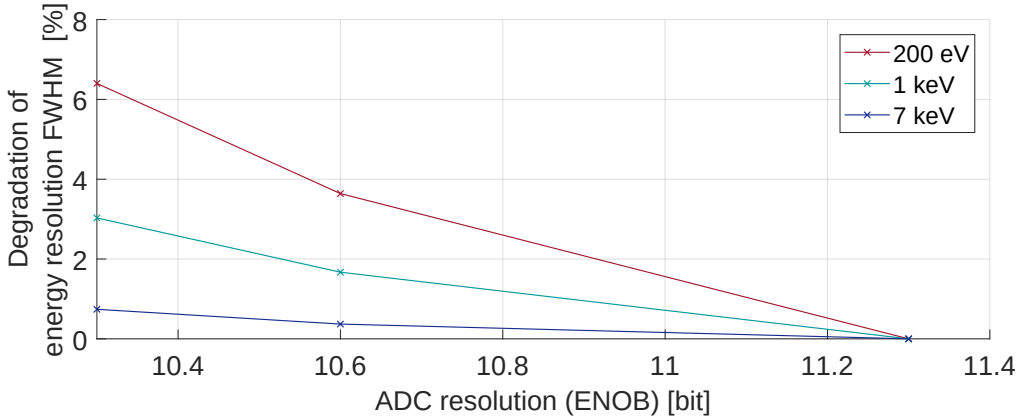


Figure 9.16.: Degradation of energy resolution (FWHM) with $11.3\,\mathrm{bit}$ ENOB as baseline reference.

Table 9.2.: Summary of the simulated results comparing the ENOB of the three ADCs.

ADC	**AD9254S** (Analog Devices)	**RHF1401** (STMicroelectronics)	**LM98640QML** (Texas Instruments)
ENOB (bit)	11.3	10.6	10.3
Energy Resolution FWHM (eV**)**			
@ 200 eV	42.63	44.18	45.36
@ 1 keV	61.69	62.72	63.56
@ 7 eV	135.1	135.6	136.1
Noise ENC (e^-)			
@ 200 eV	2.4	2.7	2.9
@ 1 keV	2.4	2.6	2.8
@ 7 eV	2.4	2.6	2.8

Moreover, additional ADC characteristics and errors should be considered when selecting a component. Particular for high-resolution imaging applications the differential and integral non-linearity is an important parameter since it can not be calibrated to remove non-linearity.

9.3.3. Verification of Event and Pattern Filtering Techniques

Data pre-processing is performed by the DE FP and includes event filtering and event recombination. An X-ray photon that hits the detector can spread its signal charge across up to four pixels resulting in a valid event. Invalid events arise usually due to particle hits, pile-up, misfits or readout and affect more than four pixels. These invalid events can be identified by appropriate filtering techniques to reduce the data rate.

There are different approaches to design the on-board data pre-processing for eight parallel output channels. One method is to separate the data of the LD in eight slices and process each of the eight slices in a parallel operating unit. Each unit performs offset and common mode correction, event filtering and valid or invalid pattern recognition. After this, the event lists of each unit are combined for further processing. This leads to the problem that the signals of pixels on the border of the slices cannot be easily compared to their neighboring pixel signal. Thus an invalid pattern cannot be identified. For this reason, subsequent filters must be defined, which recognize possible invalid patterns to delete them from the event list.

Figure 9.17 illustrates an LD frame with 512 $\times$ 512 pixels. A segment of the frame depicts split events on the slice border. By filtering only the pixels in the slice, the invalid event would be recognized as two double split patterns. This would further increase the data rate.
With the PRE this scenario can be emulated to develop, test and analyze efficient filtering algorithms for the on-board data pre-processing. Further, special test frames can be generated to verify the filtering algorithms.

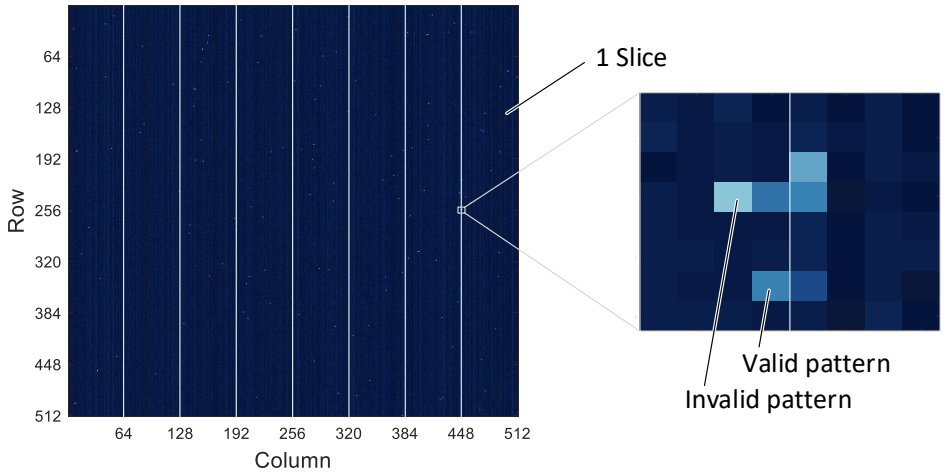


Figure 9.17.: Generated LD frame, separated in eight slices with split events generated at the slice borders.

9.3.4. Influence of Bad Pixels

Bad pixels were introduced in section 7.4.2. It can be distinguished between noisy, hot, bright, dark and dead pixel. Bad pixels influence the result of the measurement. Therefore, pattern including bad pixels need to be identified and filtered. Especially in orbit, it is expected that the amount of bad pixels increases over time due to radiation or mechanical damage. Bad pixels can be identified on-board and on ground by analysis of the offset, gain and noise map. Identified pixels are marked in a so-called bad pixel map.
For on-board common mode correction bad pixels need to be excluded as they would falsify the outcome. Common mode correction is performed by median subtraction of the respective column. Most median calculation algorithms demand a fixed number of values. By excluding pixels of a column, the number of pixels would change. This could lead to signal and timing problems. It is challenging to design the common mode algorithm in a robust and flexible way.
Moreover, the event filtering and pattern recognition is influenced by the presence of bad pixels. Recognized pattern in direct neighborhood to bad pixels represent a problem. It can not be distinguished whether the signal of the bad pixel contributes as split partner of the recognized event. It is demanding to find the right strategy in order to store no erroneous data, but also not to discard any important events.
Figure 9.18 depicts a segment of a modeled frame with a dead pixel. This pixel is insensitive to radiation illumination. There are two neighboring pixels containing a signal. It cannot be discerned if the two adjacent pixel are two single pattern or if they form a triple pattern together with the dead pixel. Thus, it is extremely important to recognize bad pixels and interpret neighboring pixels correctly.

Bad pixels can be modeled with the PRE in order to analyze identification and mapping of bad pixels. Further, common mode and event recognition algorithms can be evaluated and verified. The influence of an increasing number of bad pixels on scientific results can be studied.

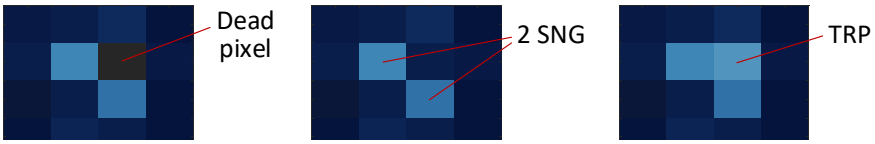


Figure 9.18.: Extraction of a modeled frame including a dead pixel. It cannot be distinguished whether the adjacent pixels form two single pattern or a triple pattern.

10. Conclusion

Within this thesis a new method for end-to-end evaluation and performance verification of the WFI signal processing chain has been investigated and realized, which uses a Programmable Real-Time Emulator (PRE). This instrument consists of a simulation environment involving mathematical models of the detector system and a hardware platform for real-time generation of the image data. Section 10.1 summarizes the main features and results of the end-to-end verification method and the developed PRE instrument. In section 10.2 future developments and scientific applications of the PRE are discussed.

10.1. Summary

The WFI is a scientific X-ray camera on-board ESA's next generation space observatory Athena. The signal processing chain of the WFI ranges from the detection of incoming photons by a DEPFET based detector to digitization and on-board processing up to the telemetry transmission via the spacecraft down to the ground station.
Within this thesis, a new method has been developed for test, evaluation and verification of the WFI signal processing chain, see chapter 3. Therefore a PRE has been designed to substitute the detector. The PRE is a scientific instrument that generates output signals according to the WFI detector system. The novelty of this system is that detector physics and scientific observation scenarios of the later flight camera in combination with environmental conditions in orbit can now be reproduced in a laboratory instrument. The PRE is completely adjustable in its features and thus its output characteristic. Integrating the PRE in the WFI signal processing chain allows the complete control of the simulated observation scenario. A comparison of the DE digital output data after frame processing with the well-known input data is now feasible.

The PRE is developed based on HW/SW codesign. In the software part, a simulation environment has been created to model the WFI detector and X-ray photon input, outlined in chapter 7. With the PRE models, physical characteristics and behavior of the sensor including its Front-End Electronics can be simulated. The model parameters

can be adjusted to reflect different detector and input characteristics. The hardware part represents data post-processing and real-time generation of the analog output data stream.

In the simulation environment, the first stage is the generation of the input data, a stack of X-ray photons with a particular energy, spatial distribution and incident time. In addition, a model was designed to simulate the timing effects like misfit generation, pile-up or the influence of the rolling shutter mode. Depending on the incident point of time of the simulated X-ray photons, the signal is weighted in a different way. Furthermore, a model to constitute defects affecting single or a cluster of pixels, like a row or column is available. These defects can be a dark or dead pixel, where the respective pixel is less or non-responsive compared to others and hot or noisy pixels with obviously higher noise than the surrounding pixels. Moreover, complex algorithms to analyze an incomplete clear process were studied. Due to the matrix structure of the sensor, columns or pixels have different gain and offset characteristics. Therefore, each pixel can be modeled with varying offset, common mode and gain per readout channel. Additionally, a specific noise stage is derived. It is possible to simulate dark current in dependence of the observation temperature and exposure time. Influences of the readout noise on the signal chain can be analyzed by adding thermal, shot and $1/f$ noise to the signal.
The models are verified with measurements of a WFI DEPFET prototype sensor. Comparisons of various effects are performed and discussed in section 9.1. The implemented models can be configured to fit the measurements, but also to display specific scenarios which are hard to induce in laboratory with an experimental setup. A comparison of a simulated energy spectrum with a measured energy spectrum shows a satisfying correlation.

The hardware part of the PRE consists of an FPGA-based computing platform with eight fast sampling DACs to generate the analog output signal of a large detector in real-time, presented in chapter 8.2. An innovative firmware concept was implemented to process the modeled data with a high-speed sub-pixel timing resolution. This allows to oversample each pixel by a factor of 16 to shape the pixel signal. This is important for modeling rise times and additional noise per pixel. The required pixel clock of $40\,\mathrm{ns}$ can be achieved by this design, leading to an output data rate of $6.4\,\mathrm{Gbit/s}$ per channel. This platform can be configured with a lower number of output channels to allow higher data rates per channel by use of parallelization without re-configuration of the hardware. Separate timing domains of data processing and data output enable a wide range of output speeds.
A Signal Adaption Unit (SAU) is designed consisting of high-speed buffers to adapt

the output signal of the DACs to the output signal of the Front-End Electronics. A protection circuit is integrated to ensure that the output signal is in an allowed range and thus avoid possible damage to the flight grade DE due to out-of-range signals. Simulations prove that the influence of the SAU on the analog output signal is negligibly small in terms of delay and speed.

The end-to-end evaluation method by modeling and emulation of the detector system is a novel method to develop, characterize and verify the signal processing chain of the WFI. With the structure of the PRE consisting of detector modeling environment and a real-time capable hardware, the PRE is an appropriate instrument for use in an end-to-end evaluation system. By applying the end-to-end method, WFI science and instrument requirements can be transferred to technical specifications. Approaches on this are given in section 9.3.
Due to a modular design of the PRE, several instruments can be synchronized to build up an emulator for the whole WFI detector system. By connecting the PRE with the DE, significant information on the signal quality and processing performance of the signal transmission path can be obtained.

10.2. Outlook

Following the conclusion of the previous section 10.1, the PRE-based end-to-end verification method is well suited for evaluation and verification of the WFI signal processing chain and will serve as core instrument for the Electronic Ground Support Equipment (EGSE) of the WFI. The PRE offers excellent possibilities to emulate the characteristics and the behavior of the detector system. With this setup the DE can be completely tested and verified before interfacing to other flight instruments. Further developments have to be carried out to extend the functionality of the PRE to a comprehensive EGSE. With this EGSE all relevant functionality of the DE can be studied. These are, for instance, tests of the detector power supply or influences of digital control signals. This could be realized by extending the PRE with a digital logic analyzer for testing the sequencer block, a set of power loads for interfacing the power conditioner module and to test monitoring of voltages and currents. Further an additional SpaceWire interface to command the DE and data transfer is needed. These enhancements would result in a comprehensive instrument for flight grade verification of the DE.

Despite of PRE-based modeling of results of laboratory measurements, one additional feature is to model also the expected environmental influences of space and their effects

on the detector. This could be the impact of radiation damage on the sensor which is expected to cause higher leakage current due to bulk damage (NIEL) and thus higher noise, defective pixels and cluster of pixels or inhomogeneities of gain distribution due to threshold voltage shifts (TID). By modeling these effects, the influence on the scientific data can be shown and studied. The subsequent results can be used for improving the DE hardware design, for instance by adjusting detector supply voltage ranges. Moreover, the performance of the on-board data processing algorithms can be enhanced, for example by adaption of noise cancellation algorithms.
The Front-End Electronics can also be affected by radiation damage. Some ASICs might fail or have malfunctions. There is a huge variety of possible errors leading to different effects and characteristics of the device. The PRE is suited to emulate this behavior. Thus, effects on the system resulting in a failure state can be investigated in advance and without destruction of devices. Thus, the hardware and firmware of the DE can be optimized regarding the behavior in case of an error, leading to a single-point or even multi-point error-free design.

During mission operation phase E, which is the utilization phase defined by ESA, the end-to-end method can be applied for in-orbit verification in terms of fault-detection, fault-isolation and recovery (FDIR) [74]. In case of a failure or misbehavior of the flight camera in orbit, observation maps can be transferred to ground. These maps, containing for instance offset values, detected MIP events, noise values, bad pixels and event lists, can be loaded to the PRE. Thus, the PRE-based flight camera system including observation scenario and environmental conditions can be reconstructed on ground. This results in an on ground verification of the instrument parallel to in orbit operation of the WFI. With the PRE as diagnostics tool, an option to reconstruct the observed errors or effects is provided to identify the source of the failure and thus extend the duration of the mission.

A. APPENDIX

List of Acronyms

ADC	Analog-to-Digital Converter
ADU	Analog-to-Digital Unit
AFE	Analog Front-End Electronics
AMS	Austria Microsystems
ASIC	Application Specific Integrated Circuit
Athena	Advanced Telescope for High-Energetic Astrophysics
AVC	Advanced Video Coding
BB	breadboard
BRAM	block random access memory
CCD	charge-coupled device
CDFS	Chandra Deep Field South
CFE	Control Front-End Electronics
CH	Camera Head
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DBL	double
DDR	double data rate
DE	Detector Electronics
DEPFET	Depleted P-Channel Field Effect Transistor
DICE	Dual Interlocked Storage Cell
DLL	delay locked loop
DR	drain-current readout
DSP	digital signal processor
ECAP	Erlangen Centre for Astroparticle Physics
EGSE	Electronic Ground Support Equipment
ENC	equivalent noise charge
ENOB	effective number of bits

ESA	European Space Agency
FD	fast detector
FDIR	fault-detection, fault-isolation and recovery
FEE	Front-End Electronics
FIFO	First In, First Out
FMC	FPGA mezzanine card
FMS	Fixed Metering Structure
FP	Frame Processor
FPGA	Field-Programmable Gate Array
fps	frames per second
FW	Filter and Calibration Wheel
FWHM	Full Width at Half Maximum
GUI	graphical user interface
HPC	high pin count
I/F	Interface
I2V	current-to-voltage
ICPU	Instrument Control and Power-Distribution Unit
JPEG	Joint Photographic Experts Group
JWST	James Webb Space Telescope
LD	large detector
LDA	large detector array
LUT	look-up table
LVDS	low-voltage differential signaling
MAM	Mirror Assembly Module
MIP	Minimal Ionizing Particle
MIXS	Mercury Imaging X-ray Spectrometer
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MPE	Max Planck Institute for Extraterrestrial Physics
MPEG	Moving Picture Experts Group
MUX	multiplexer
NASA	National Aeronautics and Space Administration
NIEL	non-ionizing energy loss
NMOS	n-channel metal oxide semiconductor
PC	Personal Computer
PCB	printed circuit board
PCM	Power Conditioner Module
PLL	phase-locked loop

PMOS	p-channel metal oxide semiconductor
pnCCD	pn Charge-Coupled Device
PRE	Programmable Real-Time Emulator
PSF	Point Spread Function
QE	quantum efficiency
QUD	quadruple
RC	resistor-capacitor
RISC	Reduced Instruction Set Computer
rms	root mean square
ROI	Region of Interest
RS	rolling shutter
S/H	sample and hold
SAU	Signal Adaption Unit
SC	spacecraft
SDD	silicon drift detector
SDRAM	Synchronous Dynamic Random Access Memory
SEE	single event effects
SERDES	serializer/deserializer
SEU	single event upsets
SF	source-follower readout
SIM	scientific instrument module
SIXTE	Simulation of X-ray Telescopes
SMBH	Supermassive Black Hole
SNG	single
SPI	serial peripheral interface
SPO	Silicon Pore Optics
SRAM	static random-access memory
SVM	Service Module
TES	Transition Edge Sensor
TID	total ionizing dose
TRP	triple
UART	Universal Asynchronous Receiver Transmitter
UHD	Ultra High Definition
UV	ultraviolet
VCO	voltage-controlled oscillator
WFI	Wide Field Imager
X-IFU	X-ray Integral Field Unit

Bibliography

[1] 4DSP: *FMC204 Digital-to-Analog Converter Board: Quad Channel 16-bit 1 Gsps D/A (rev-1.1)*, 2014. `http://www.4dsp.com`.

[2] 4DSP: *FMC204 User Manual (r1.14)*, 2014. `http://www.4dsp.com`.

[3] Abba, A. *et al.*: *Digital Programmable Emulator and Analyzer of Radiation Detection Setups*. 18th IEEE-NPSS Real Time Conference, pages 1–4, 2012.

[4] Analog Devices Inc.: *AD9254S: Aerospace 14-Bit 150 MSPS, 1.8V Analog-to-Digital Converter (Rev. B): Datasheet*, 2013. `http://www.analog.com`.

[5] Analog Devices Inc.: *AD9517-3: 12-Output Clock Generator with Integrated 2.0 GHz VCO (Rev. E): Datasheet*, 2013. `http://www.analog.com`.

[6] ANSI/VITA 57.1-2010: *FMC: FPGA Mezzanine Cards Base Standard*. 2010.

[7] Aschauer, F.: *Real-time data acquisition system for X-ray imaging spectroscopy*. PhD thesis, Technische Universität München, München, 2015.

[8] Ayre, M. *et al.*: *ATHENA - System studies and optics accommodation*. Proceedings of SPIE Space Telescopes and Instrumentation: Ultraviolet to Gamma Ray, 2016:990526–3, 9905.

[9] Bähr, A. *et al.*: *Development of DEPFET active pixel sensors to improve the spectroscopic response for high time resolution applications*. Proceedings of SPIE Space Telescopes and Instrumentation: Ultraviolet to Gamma Ray, 9144:914411, 2014.

[10] Barbera, M. *et al.*: *The optical blocking filter for the ATHENA Wide Field Imager: ongoing activities towards the conceptual design*. Proceedings of SPIE UV, X-Ray, and Gamma-Ray Space Instrumentation for Astronomy XIX, 9601:960109, 2015.

[11] Barcons, X. *et al.*: *Athena: The X-ray observatory to study the hot and energetic Universe*. Journal of Physics: Conference Series, 610:012008, 2015.

[12] Barret, D. *et al.*: *The Hot and Energetic Universe: The X-ray Integral Field Unit (X-IFU) for Athena+*. arXiv:1308.6784, 2013.

[13] Barret, D. *et al.*: *The Athena X-ray Integral Field Unit (X-IFU)*. Proceedings of SPIE Space Telescopes and Instrumentation: Ultraviolet to Gamma Ray, 9905:99052F, 2016.

[14] Bergbauer, B.: *Study of macroscopic and microscopic homogeneity of DEPFET X-ray detectors*. PhD thesis, Technische Universität Chemnitz, 2015.

[15] Beringer, J. *et al.*: *Review of Particle Physics (Particle Data Group)*. Physical Review D, 86(1), 2012.

[16] Boyle, W. S. and Smith, G. E.: *Charge Coupled Semiconductor Devices*. Bell System Technical Journal, 49(4):587–593, 1970.

[17] Carroll, B. W. and Ostlie, D. A.: *An Introduction to Modern Astrophysics*. Pearson Addison-Wesley, San Francisco, 2007.

[18] Cen, R. *et al.*: *Revealing the Warm-Hot Intergalactic Medium with OVI Absorption*. The Astrophysical Journal, 559(1):L5–L8, 2001.

[19] Chantler, C. T. *et al.*: *X-Ray Form Factor, Attenuation, and Scattering Tables*. http://physics.nist.gov/ffast, 2005.

[20] Compton, A. H.: *The Spectrum of Scattered X-Rays*. Physical Review, 22(5):409–413, 1923.

[21] Dauser, T. *et al.*: *Bright Source Capabilities of the Athena WFI and X-IFU Instrument*. Exploring the Hot and Energetic Universe: The first scientific conference dedicated to the Athena X-ray observatory, Madrid, ES, 2015.

[22] ESA: *Athena: The extremes of the Universe: from black holes to large-scale structure*. Assessment Study Report, 2011.

[23] ESA: *CDF Study Report: Athena: Assessment of an X-Ray Telescope for the ESA Cosmic Vision Program*. (CDF-150(A)), 2014.

[24] ESA Senior Survey Committee: *Report of the Senior Survey Committee on the selection on science themes for the L2 and L3 missions*. 2013. `http://sci.esa.int/ssc_report`.

[25] European Cooperation for Space Standardization: *Space Engineering: SpaceWire – Links, nodes, routers and networks*. (ECSS-E-ST-50-12C), 2008.

[26] European Cooperation for Space Standardization: *Space Engineering: Verification*. (ECSS-E-ST-10-02C), 2009.

[27] European Cooperation for Space Standardization: *Verification guidelines*. (ECSS-E-HB-10-02A), 2010.

[28] European Cooperation for Space Standardization: *Space Engineering: Testing*. (ECSS-E-ST-10-03C), 2012.

[29] Evans, I. N. *et al.*: *The Chandra Source Catalog*. The Astrophysical Journal Supplement Series, 189(1):37–82, 2010.

[30] Eversberg, T. and Vollmann, K.: *Spectroscopic Instrumentation: Fundamentals and Guidelines for Astronomers*. Springer-Praxis books in space exploration. Springer, Heidelberg, 2015.

[31] FITS Working Group: *Definition of the Flexible Image Transport System (FITS): The FITS Standard - Version 4.0*, 2016. `http://fits.gsfc.nasa.gov/iaufwg/`.

[32] Friedman, H. *et al.*: *Photon Counter Measurements of Solar X-Rays and Extreme Ultraviolet Light*. Physical Review, 83(5):1025–1030, 1951.

[33] Gardner, J. P. *et al.*: *The James Webb Space Telescope*. Space Science Reviews, 123(4):485–606, 2006.

[34] Garmire, G. P. *et al.*: *Advanced CCD imaging spectrometer (ACIS) instrument on the Chandra X-ray Observatory*. Proceedings of SPIE X-Ray and Gamma-Ray Telescopes and Instruments for Astronomy, 4851:28, 2003.

[35] Gatti, E.: *Suboptimal filtering of 1/f-noise in detector charge measurements*. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 297(3):467–478, 1990.

[36] Gatti, E. and Rehak, P.: *Semiconductor drift chamber - An application of a novel charge transport scheme*. Nuclear Instruments and Methods in Physics Research, 225(3):608–614, 1984.

[37] Gellert, R. *et al.*: *The Alpha-Particle-X-Ray-Spectrometer(APXS) for the Mars Science Laboratory (MSL) Rover Mission*. In *40th Lunar and Planetary Science Conference*, volume 2364, pages 23–27.

[38] Gerthsen, C. and Vogel, H.: *Physik*. Springer, Berlin, Heidelberg, 17th edition, 1993.

[39] Giacconi, R. *et al.*: *Evidence for X-Rays From Sources Outside the Solar System*. Physical Review Letters, 9(11):439–443, 1962.

[40] Giacconi, R. *et al.*: *The Einstein (HEAO 2) X-ray Observatory*. The Astrophysical Journal, 230:540, 1979.

[41] Gonzalez, R. C. and Woods, R. E.: *Digital Image Processing*. Prentice-Hall, Upper Saddle River, NJ, 2nd edition, 2002.

[42] Gottardi, L. *et al.*: *Development of TES-based detectors array for the X-ray Integral Field Unit (X-IFU) on the future X-ray Observatory ATHENA*. Proceedings of SPIE Space Telescopes and Instrumentation: Ultraviolet to Gamma Ray, 9144:91442M, 2014.

[43] Grotzinger, J. P. *et al.*: *Mars Science Laboratory Mission and Science Investigation*. Space Science Reviews, 170(1-4):5–56, 2012.

[44] Holst, G. C.: *CCD arrays, cameras, and displays*. SPIE Optical Engineering Press, Bellingham, WA, 2nd edition, 2000.

[45] Hubbell, J. H. and Seltzer, S. M.: *Tables of X-Ray Mass Attenuation Coefficients and Mass Energy-Absorption Coefficients from 1 keV to 20 MeV for Elements Z = 1 to 92*. 2004. `http://physics.nist.gov/xaamdi`.

[46] ISO/IEC 10918-1:1994: *Digital compression and coding of continuous-tone still images: Requirements and guidelines*.

[47] ISO/IEC 14496-10:2014: *Coding of audio-visual objects - Part 10: Advanced Video Coding*.

[48] Janesick, J. R.: *Scientific charge-coupled devices*, volume PM83. SPIE, Bellingham, WA, 2001.

[49] Jansen, F. *et al.*: *XMM-Newton observatory*. Astronomy and Astrophysics, 365(1):L1–L6, 2001.

[50] Johnson, J. B.: *Thermal Agitation of Electricity in Conductors*. Physical Review, 32, 1928.

[51] Kemmer, J. *et al.*: *Experimental confirmation of a new semiconductor detector principle*. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 288(1):92–98, 1990.

[52] Kemmer, J. and Lutz, G.: *New detector concepts*. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 253(3):365–377, 1987.

[53] Kimmel, N.: *Analysis of the charge collection process in solid state x-ray detectors*. PhD thesis, Universität Siegen, 2008.

[54] Kirsch, M. G. *et al.*: *Crab: the standard X-ray candle with all (modern) X-ray satellites*. Proceedings of SPIE UV, X-Ray, and Gamma-Ray Space Instrumentation for Astronomy XIV, 5898:589803, 2005.

[55] Lauf, T.: *Analysis and Operation of DePFET X-ray Imaging Detectors*. PhD thesis, Technische Universität München, 2011.

[56] Lauf, T. and Andritschke, R.: *ROOT based Offline and Online Analysis (ROAn): An analysis framework for X-ray detector data*. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 762:142–148, 2014.

[57] Laureijs, R. J. *et al.*: *The Euclid Mission*. Proceedings of SPIE Space Telescopes and Instrumentation: Optical, Infrared, and Millimeter Wave, 2010(7731):77311H–1.

[58] Lechner, P.: *Zur Inoisationsstatistik in Silizium*. PhD thesis, Technische Universität München, 1998.

[59] Lechner, P. *et al.*: *Silicon drift detectors for high resolution room temperature X-ray spectroscopy*. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 377(2-3):346–351, 1996.

[60] Leo, W. R.: *Techniques for Nuclear and Particle Physics Experiments*. Springer, Berlin, 2nd edition, 1994.

[61] Ley, W. *et al.*: *Handbuch der Raumfahrttechnik*. Hanser, München, 3rd edition, 2008.

[62] Lowe, B. G. and Sareen, R. A.: *A measurement of the electron–hole pair creation energy and the Fano factor in silicon for 5.9keV X-rays and their temperature dependence in the range 80–270K*. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 576(2-3):367–370, 2007.

[63] Lu, W. *et al.*: *CCD emulator design for LSST camera*. Proceedings of SPIE High Energy, Optical, and Infrared Detectors for Astronomy VII, 9915:99152O, 2016.

[64] Lumb, D. and den Herder, J. W.: *Athena Science Requirements Document (Rev. 1.5)*. SRE-S/ATH/2015/01. ESA, Science Support Office, 2016.

[65] Lutz, G.: *Semiconductor Radiation Detectors*. Springer, Berlin and New York, 2nd edition, 2007.

[66] Manfredi, P. F. and Speziali, V.: *Noise Limits in Detector Charge Measurements*. In Ferbel, T. (editor): *Techniques and Concepts of High-Energy Physics VI*, NATO ASI Series, Series B. Springer, Boston, MA, 1991.

[67] Meidinger, N. *et al.*: *pnCCD for photon detection from near-infrared to X-rays*. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 565(1):251–257, 2006.

[68] Meidinger, N. *et al.*: *Development of the focal plane PNCCD camera system for the X-ray space telescope eROSITA*. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 624(2):321–329, 2010.

[69] Meidinger, N. *et al.*: *Report on the eROSITA camera system*. Proceedings of SPIE Space Telescopes and Instrumentation: Ultraviolet to Gamma Ray, 9144:91441W, 2014.

[70] Meidinger, N. *et al.*: *The Wide Field Imager Instrument for Athena*. Proceedings of SPIE Space Telescopes and Instrumentation: Ultraviolet to Gamma Ray, 9905:99052A, 2016.

[71] Meidinger, N. *et al.*: *The Wide Field Imager Instrument for ATHENA*. Proceedings of SPIE UV, X-Ray, and Gamma-Ray Space Instrumentation for Astronomy XX, 103970:103970V, 2017.

[72] Müller, R.: *Rauschen*. Halbleiter-Elektronik. Springer, Berlin, Heidelberg, NewYork, 1979.

[73] Nandra, K. *et al.*: *The Hot and Energetic Universe: A White Paper presenting the science theme motivating the Athena+ mission*. arXiv:1306.2307, 2013.

[74] Nasa Engineering Network: *Fault-Detection, Fault-Isolation, and Recovery (FDIR) Techniques: DFE-7*. Johnson Space Center, 1994.

[75] Nyquist, H.: *Thermal Agitation of Electric Charge in Conductors*. Physical Review, 32, 1928.

[76] Olive, K. A. *et al.*: *Review of Particle Physics*. Chinese Physics C, 40(10):100001, 2016.

[77] Ott, S. *et al.*: *Modeling of DEPFET based X-ray Detectors for Athena's Wide Field Imager*. IEEE Nuclear Science Symposium, Medical Imaging Conference and Room-Temperature Semiconductor Detector Workshop (NSS/MIC/RTSD), pages 1–8, 2016.

[78] Ott, S. *et al.*: *New evaluation concept of the Athena WFI camera system by emulation of X-ray DEPFET detectors*. Journal of Instrumentation, 11(01):C01028, 2016.

[79] Pelgrom, Marcel: *Analog-to-Digital Conversion*. 3rd edition, 2017.

[80] Planck, M.: *Ueber das Gesetz der Energieverteilung im Normalspectrum*. Annalen der Physik, 309(3):553–563, 1901.

[81] Plattner, M. *et al.*: *WFI Electronics and On-Board Data Processing*. Proceedings of SPIE Space Telescopes and Instrumentation: Ultraviolet to Gamma Ray, 9905:99052D, 2016.

[82] Popp, M.: *Untersuchung und analytische Modellierung der Systemantwort von pn-CCD Detektoren*. PhD thesis, Ludwig-Maximilians-Universität München, 2000.

[83] Porro, M. *et al.*: *VERITAS: a 128-channel ASIC for the readout of pnCCDs and DEPFET arrays for X-ray imaging, spectroscopy and XFEL applications*. Nuclear Science Symposium and Medical Imaging Conference, 951–958, 2011.

[84] Porro, M. *et al.*: *VERITAS 2.0 a multi-channel readout ASIC suitable for the DEPFET arrays of the WFI for Athena*. Proceedings of SPIE Space Telescopes and Instrumentation: Ultraviolet to Gamma Ray, 91445N, 2014.

[85] Predehl, P. *et al.*: *eROSITA on SRG*. AIP Conference Proceedings 1248, (543), 2010.

[86] Quimby, R. S.: *Photonics and Lasers: An Introduction*. Wiley-Interscience, Hoboken, NJ, 2006.

[87] Rataj, M. *et al.*: *The Filter and Calibration Wheel for the ATHENA Wide Field Imager*. Proceedings of SPIE Space Telescopes and Instrumentation: Ultraviolet to Gamma Ray, 9905:990568, 2016.

[88] Rau, A. *et al.*: *The Hot and Energetic Universe: The Wide Field Imager (WFI) for Athena+*. arXiv:1308.6785, 2013.

[89] Rau, A. *et al.*: *Athena Wide Field Imager Key Science Drivers*. Proceedings of SPIE Space Telescopes and Instrumentation: Ultraviolet to Gamma Ray, 9905:99052B, 2016.

[90] Rodgers, D. *et al.*: *ATHENA Environmental Specification*. TEC-EES/2014.89/DR. ESA, ESTEC, Noordwijk, 2015.

[91] Rodgers, J. L. and Nicewander, W. A.: *Thirteen Ways to Look at the Correlation Coefficient*. The American Statistician, 42-1, 1988.

[92] Rossi, L. *et al.*: *Pixel Detectors: From Fundamentals to Applications*. Particle Acceleration and Detection. Springer, Berlin and Heidelberg and New York, 2006.

[93] Rummel, S. *et al.*: *Intrinsic properties of DEPFET active pixel sensors*. Journal of Instrumentation, 4(03):P03003–P03003, 2009.

[94] Ryll, H. *et al.*: *The pnCCD for Applications in Transmission Electron Microscopy: Further Development and New Operation Modes*. Microscopy and Microanalysis, 20(S3):1122–1123, 2014.

[95] Schmid, C.: *X-ray Telescopes in the Digital Lab: Instrument Performance Simulations*. PhD thesis, Friedrich-Alexander-Universität Erlangen-Nürnberg, 2012.

[96] Schötzig, U.: *Half-life and X-ray emission probabilities of Fe-55*. Applied Radiation and Isotopes, 53(3):469–472, 2000.

[97] Segneri, G. *et al.*: *Measurement of the Current Related Damage Rate at -50Â°C and Consequences on Macropixel Detector Operation in Space Experiments*. IEEE Transactions on Nuclear Science, 56(6):3734–3742, 2009.

[98] Smith, S. J. *et al.*: *Transition-edge sensor pixel parameter design of the microcalorimeter array for Transition-edge sensor pixel parameter design of the microcalorimeter array for the X-ray Integral Field Unit on Athena*. Proceedings of SPIE Space Telescopes and Instrumentation: Ultraviolet to Gamma Ray, 9905:99052H–99052H–19, 2016.

[99] Spieler, H.: *Semiconductor Detector Systems*, volume 12. Oxford University Press, Oxford, 2. edition, 2009.

[100] STMICROELECTRONICS: *RHF1401: Rad-hard 14-bit 20 Msps A/D converter*, 2014.

[101] Strüder, L. *et al.*: *X-ray pn-CCDs on the XMM Newton Observatory*. Proceedings of SPIE X-Ray Optics, Instruments, and Missions III, 4012:342–352, 2000.

[102] Strüder, L. *et al.*: *The European Photon Imaging Camera on XMM-Newton: The pn-CCD camera*. Astronomy & Astrophysics, 365(1):L18–L26, 2001.

[103] Takahashi, T. *et al.*: *The ASTRO-H X-ray astronomy satellite*. Proceedings of SPIE Space Telescopes and Instrumentation: Ultraviolet to Gamma Ray, 914425, 2014.

[104] Texas Instruments: *DAC5682Z: 16-Bit, 1.0 GSPS 2x-4x Interpolating Dual-Channel Digital-to-Analog Converter (Rev. E): Datasheet*, 2012. `http://www.ti.com/product/DAC5682Z`.

[105] Texas Instruments: *LM98640QML: Dual Channel, 14-Bit, 40 MSPS Analog Front End with LVDS Output (Rev. D): Datasheet*, 2015. `http://www.ti.com/product/LM98640QML-SP`.

[106] Theuwissen, A. J.P.: *Solid-state imaging with charge-coupled devices*. Kluwer Academic Publishers, New York and Boston and Dordrecht and London and Moscow, 1995.

[107] Tietze, U. and Schenk, C.: *Halbleiter-Schaltungstechnik*. Springer, Berlin, Heidelberg, 4. edition, 1978.

[108] Treberspurg, W.: *Studies of prototype DEPFET sensors for the wide field imager of Athena*. Proceedings of SPIE Space Telescopes and Instrumentation: Ultraviolet to Gamma Ray, 9905:99052C, 2016.

[109] Treberspurg, W. *et al.*: *Studies of prototype DEPFET sensors for the Wide Field Imager of Athena*. Proceedings of SPIE UV, X-Ray, and Gamma-Ray Space Instrumentation for Astronomy XX, 103970:103970U, 2017.

[110] Treis, J. *et al.*: *MIXS on BepiColombo and its DEPFET based focal plane instrumentation*. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 624(2):540–547, 2010.

[111] Truemper, J. and Hasinger, G.: *The universe in X-rays*. Astronomy and astrophysics library. Springer, Berlin and New York, 2008.

[112] Trümper, J.: *The ROSAT mission*. Advances in Space Research, 2(4):241–249, 1982.

[113] Tsuji, K., Injuk, J., and van Grieken, R.: *X-Ray Spectrometry: Recent Technological Advances*. John Wiley & Sons, Ltd, Chichester, UK, 2004.

[114] USB Implementers Forum, Inc.: *Hi-Speed USB*, 2017. `http://usb.org`.

[115] Vaseghi, S. V.: *Advanced digital signal processing and noise reduction*. Wiley, Chichester, West Sussex, 4th edition, 2008.

[116] Voges, W. *et al.*: *The ROSAT All-Sky Survey Bright Source Catalogue*. arXiv:astro-ph/9909315, 1999.

[117] Watson, M. G. *et al.*: *The XMM-Newton serendipitous survey: V. The Second XMM-Newton serendipitous source catalogue*. Astronomy & Astrophysics, 493(1):339–373, 2009.

[118] Weisskopf, M. C. *et al.*: *Chandra X-ray Observatory (CXO): Overview*. Proceedings of SPIE X-Ray Optics, Instruments, and Missions III, 4012:2–16, 2000.

[119] Weisskopf, M. C. *et al.*: *An Overview of the Performance and Scientific Results from the Chandra X–Ray Observatory*. Publications of the Astronomical Society of the Pacific, 114(791):1–24, 2002.

[120] Wien, W.: *Temperatur und Entropie der Strahlung*. Annalen der Physik, 288(5):132–165, 1894.

[121] Wilms, J. *et al.*: *Athena end-to-end simulations*. Proceedings of SPIE Space Telescopes and Instrumentation: Ultraviolet to Gamma Ray, 9144:91445X, 2014.

[122] Wilson, A.: *ESA achievements: More than thirty years of pioneering space activity*, volume 250 of *ESA BR*. ESA Publications, Noordwijk Netherlands, 3rd edition, 2005.

[123] Wolter, H.: *Spiegelsysteme streifenden Einfalls als abbildende Optiken für Röntgenstrahlen*. Annalen der Physik, 445(1-2):94–114, 1952.

[124] Xilinx, Inc.: *VC707 Evaluation Board for the Virtex-7 FPGA: User Guide UG885 (V1.6)*, 2015. `https://www.xilinx.com`.

[125] Xilinx, Inc.: *7 Series FPGAs SelectIO Resources: User Guide UG471 (V1.8)*, 2016. `https://www.xilinx.com`.

[126] Xilinx, Inc.: *7 Series FPGAs Data Sheet: Overview DS180 (V2.5)*, 2017. `https://www.xilinx.com`.

[127] Xilinx, Inc.: *Virtex-7 T and XT FPGAs Data Sheet: DC and AC Switching Characteristics: Product Specification DS183 (v1.27)*, 2017. `https://www.xilinx.com`.

[128] Zane, S. *et al.*: *LOFT — Large Observatory for X-ray Timing*. Journal of Instrumentation, 9(12):C12003–C12003, 2014.