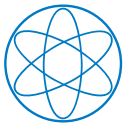

Dissertation

Studies of Read-Out Electronics and Trigger for Muon Drift Tube Detectors at High Luminosities

von

Sebastian Nowak

eingereicht an der

Fakultät für Physik

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Studies of Read-Out Electronics and Trigger for Muon Drift Tube Detectors at High Luminosities

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Vollständiger Abdruck der von der Fakultät für Physik der Technischen Universität München zur Erlangung des akademischen Grades eines

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Wer immer strebend sich bemüht,
den können wir erlösen.

(Faust. Der Tragödie zweiter Teil)

Abstract

The Large Hadron Collider (LHC) at the European Centre for Particle Physics, CERN, collides protons with an unprecedentedly high centre-of-mass energy and luminosity. The collision products are recorded and analysed by four big experiments, one of which is the ATLAS detector. For precise measurements of the properties of the Higgs-Boson and searches for new phenomena beyond the Standard Model, the LHC luminosity of $L = 10^{34}cm^{-2}s^{-1}$ is planned to be increased by a factor of ten leading to the High Luminosity LHC (HL-LHC). In order to cope with the higher background and data rates, the LHC experiments need to be upgraded.

In this thesis, studies for the upgrade of the ATLAS Muon Spectrometer are presented with respect to the read-out electronics of the Monitored Drift Tube (MDT) and the small-diameter Muon Drift Tube (sMDT) chambers and the Level-1 muon trigger. Due to the reduced tube diameter of sMDT chambers, background occupancy and space charge effects are suppressed by an order of magnitude compared to the MDT chambers.

The rate capability of the sMDT chambers is limited by signal pile-up effects of the MDT read-out electronics using bipolar signal shaping. In order to profit from the full potential of sMDT chambers, prototype read-out electronics with improved signal shaping and baseline restoration has been developed. Measurement and simulation of the sMDT drift-tubes with the new read-out electronics show that the high-rate performance of the sMDT chambers is substantially increased.

At HL-LHC, muon trigger rates are expected to be about 10 times higher than at the LHC design luminosity. In order to fully exploit the physics potential of the HL-LHC, the selectivity of the ATLAS Muon Trigger system has to be improved. This is achieved by using the MDT chambers of the ATLAS Muon Spectrometer in the muon trigger to obtain the optimum achievable muon momentum resolution in the trigger. Simulations and measurements with a demonstrator of the MDT based trigger at the CERN Gamma Irradiation Facility demonstrate the feasibility of this concept.

Contents

1. Motivation and Outline

> The Organization shall provide for collaboration among European States in nuclear research of a pure scientific and fundamental character, and in research essentially related thereto. The Organization shall have no concern with work for military requirements and the results of its experimental and theoretical work shall be published or otherwise made generally available.
>
> *(CERN Convention, Article 2 [1])*

Since the foundation of CERN[1] in 1953 many important discoveries in particle physics have been made. In 1983 the W- and Z-Bosons were discovered by the UA1 and UA2 experiments using proton-antiproton collisions in the Super-Proton Synchrotron (SPS) which started operation in 1976. Between 1989 and 2000 Large Electron-Positron Collider (LEP) was operated at CERN with four experiments which performed precision measurements of the electroweak interaction.

With the start of the Large Hadron Collider (LHC) a new era for particle physics has begun. The first highlight was the discovery of the Higgs-Boson in 2012 [2,3]. For precise measurements of the Higgs-Boson properties and searches for new phenomena beyond the Standard Model the centre-of-mass energy of the LHC will be raised to 13 TeV in 2015 and the luminosity will be increased in several steps over the next ten years (see Section 2). The luminosity increase necessities upgrades of LHC experiments.

In this thesis, studies for the upgrade of the ATLAS Muon Spectrometer are presented, in particular of the Level-1 muon trigger and of the read-out electronics of the Monitored Drift Tubes (MDT) chambers and small-diameter Muon Drift Tube (sMDT) chambers.

After a short introduction about the LHC, the ATLAS Experiment and the planned luminosity upgrades, the principles of the MDT and sMDT chambers are discussed in Chapter 4. In Chapter 5, improvements of their read-out electronics for operation at high luminosities are presented. Chapter 6 is devised to studies of using the MDT chambers in the ATLAS Level-1 muon trigger.

[1] Conseil Européen pour la Recherche Nuclaire

2. The Large Hadron Collider

The Large Hadron Collider (LHC) [4], colliding protons in a circular storage ring of 27 km circumference since end of 2009, is the largest scientific instrument ever build. The accelerated protons of the LHC circle the ring in bunches with a design separation in time of 25 ns corresponding to a bunch crossing rate of 40 MHz. In addition to the proton beams, the LHC can also accelerate and collide heavy ion beams, in particular lead ions. The LHC is designed for a nominal instantaneous luminosity of $L_0 = 10^{34} cm^{-2} s^{-1}$ of proton-proton collisions at a centre-of-mass energy of 14 TeV with 2808 bunches of protons [5].

The LHC has been built in the already existing accelerator tunnel of the Large Electron Positron Collider (LEP) which has been shut down at the end of 2000. The already existing pre-accelerators are being reused, namely the LINAC2, the BOOSTER, the Proton Synchrotron (PS) and the Super Proton Synchrotron (SPS). An overview of the CERN accelerator complex is given in Fig. 2.1.

The LHC started at a center-of-mass energy of 900 GeV end of 2009 and 7 TeV in 2010. In 2012, the center-of-mass energy was raised to 8 TeV. A peak luminosity of about $L = 8 \cdot 10^{33} cm^{-1} s^{-1}$ was also reached in 2012.

Without an additional LHC luminosity increase the running time necessary to half the statistical error in the measurements will be more than a decade. Therefore, the LHC luminosity has to be increased [7], the planned time-line (2014) is shown in Fig. 2.2. It is planned to upgrade the LHC in several steps. In Run 2 the LHC is going to be operated slightly below its design energy. During the one year LS 2 the Phase-1 upgrade is going to take place, leading afterwards to a luminosity increase of a factor of 3. Finally, between 2023 and 2025 the Phase-2 upgrade is going to lead to the so-called High-Luminosity LHC (HL-LHC). The main objective of the HL-LHC is to reach a peak luminosity of $L = 5 \cdot 10^{34} cm^{-2} s^{-1}$ with levelling, leading to a integrated luminosity of $250 fb^{-1}$ per year and to $3000 fb^{-1}$ over 12 years [7].

Due to the luminosity increase after the upgrades, the LHC experiments have to be adapted to cope with the changed conditions. Therefore, LS1 and LS2 are also used to upgrade the experiments and conduct the necessary maintenance.

The implications of the Phase-2 upgrade for the ATLAS Muon Spectrometer and the development of new detector components to operate under the changed conditions are discussed in the following.

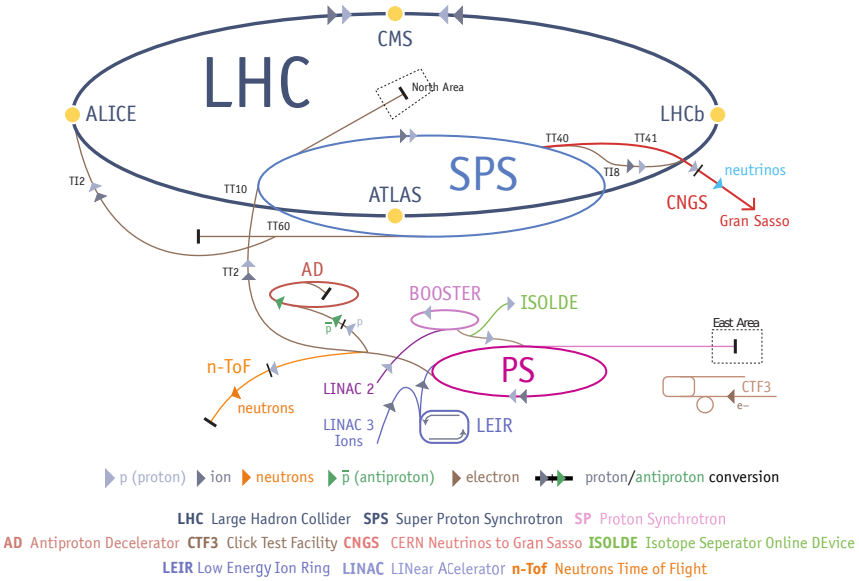


Figure 2.1.: Overview of the CERN accelerator complex [6]. Starting with LINAC2 and the BOOSTER and after pre-acceleration in the PS and SPS, the protons are injected into the LHC ring.

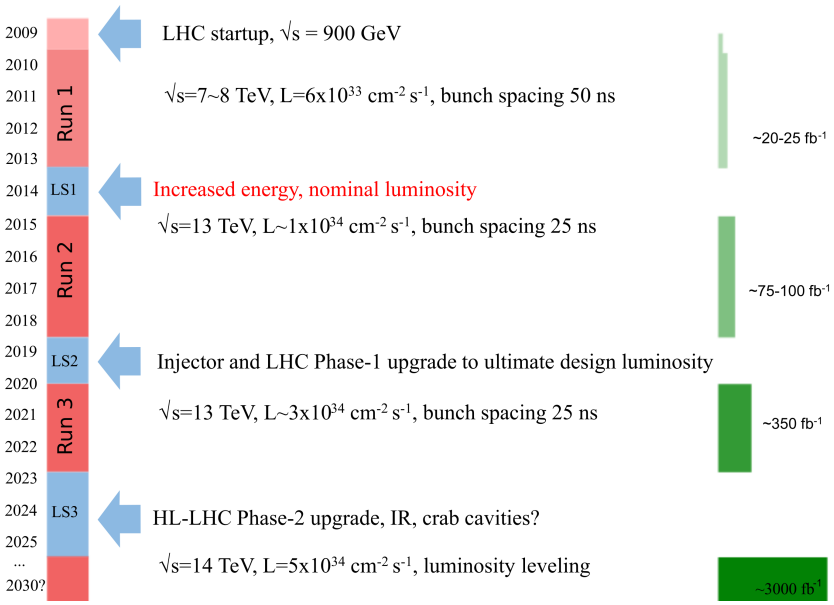


Figure 2.2.: Planned time schedule of the LHC high luminosity upgrades [8]. Upgrades to Phase-1 and Phase-2 (HL-LHC) take place during the Long shutdowns LS2 amd LS3, respectively. The green boxes represent the accumulated integrated luminosity of the accelerator.

3. The ATLAS Muon Spectrometer

The goals of the ATLAS[1] experiment [9] (see Fig. 3.1) are to measure Standard Model processes indicating Higgs boson production and decays with high precision and to discover new physics beyond. With a length of 44 m, a diameter of 25 m and a weight of 7000 tons, the ATLAS detector is the largest experiment at the LHC. Its construction took place between May 2003 and end of 2008.

3.1. The Muon Detectors

The Muon Spectrometer [10] is the outer-most and largest part of the ATLAS detector (see Fig. 3.1 and Fig. 3.3). It provides precise muon track and momentum reconstruction with a momentum resolution of

$$\frac{\Delta p_T}{p_T} < 10^{-4} \frac{p}{GeV} \tag{3.1}$$

for $p_T > 300$ GeV and

$$\frac{\Delta p_T}{p_T} < 3\% \tag{3.2}$$

for $p_T < 300$ GeV [10]. The resolution in the lower momentum range is limited by multiple scattering in the detector structures and by energy loss fluctuations in the calorimeters.

The Muon Spectrometer is split into the barrel and two end-cap regions (see Fig. 3.3), each with three layers of precision tracking detectors. The barrel consists of inner, middle and outer layers, each end-cap of a Small Wheel, Big Wheel and the Outer Wheel. With the exception of the very forward regions of the Small Wheels where cathode strip chambers (CSC) are used, the muon tracking detectors are Monitored Drift Tube (MDT) chambers (see Section 4).

To achieve the required muon momentum resolution in the toroidal magnetic field of the Muon Spectrometer, the track points in each layer have to be measured with an accuracy of better than 50 μm. This sets the requirements on the intrinsic resolution and the mechanical precision of the MDT chambers [10] (see Section 4.1). In addition, the operating parameters, the relative alignment of the chambers and the magnetic field strength have to be monitored with high precision to be taken into account in muon track reconstruction.

[1] ATLAS - A Toroidal LHC AparatuS

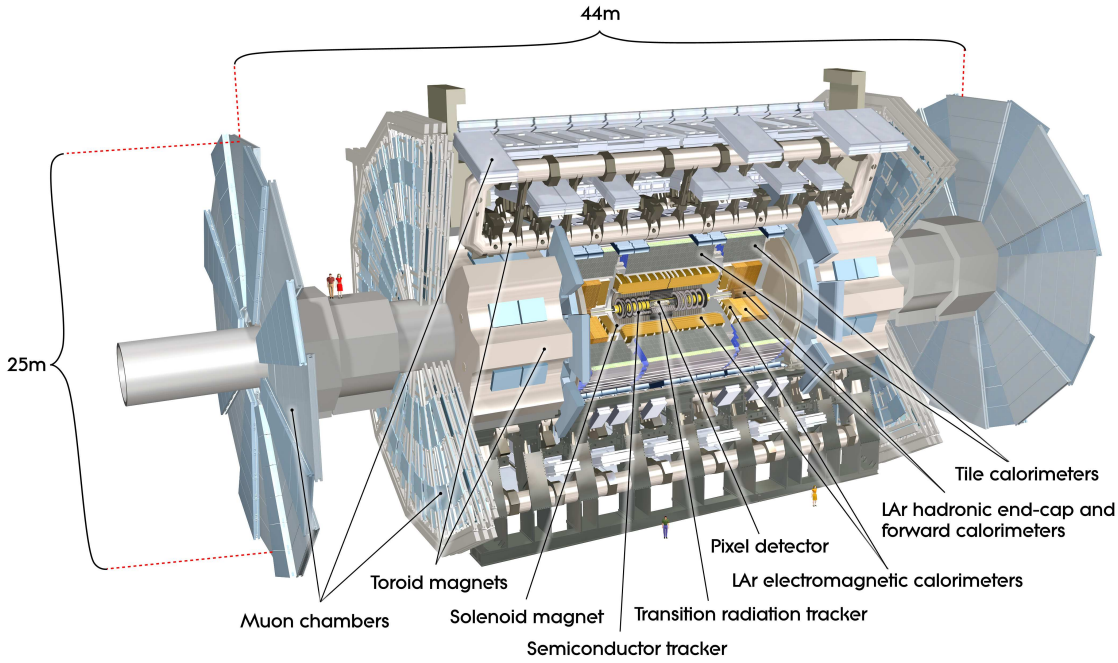


Figure 3.1.: Cut-away view of the ATLAS detector [9]. The inner tracking detector and the calorimeters for particle and jet energy measurements are surrounded by the Muon Spectrometer consisting of three layers of muon chambers in a toroidal magnetic field of superconducting air-core magnets.

Special, fast trigger chambers are used for the Level-1 muon trigger, Resistive Plate Chambers (RPC) in the middle and outer layers of the barrel and Thin Gap Chambers (TGC) in the end-caps. They also measure the track coordinates along the MDT drift-tubes with reduced resolution.

3.2. The Trigger and Data Acquisition System

The ATLAS trigger system consists of three levels. A simplified overview of the trigger and DAQ system is given in Fig. 3.4.

3.2.1. The Level-1 Trigger

The Level-1 (L1) trigger decision is based on reduced-granularity information from the calorimeter and muon trigger chambers (see Section 3.1). As shown in Fig. 3.4, the decisions of calorimeter and muon trigger are combined in the Central Trigger Processor. In addition, the L1 trigger provides Regions of Interest (RoI) which are passed on to the next trigger level. During the L1 trigger latency of 2.5 μs, the information of all detector

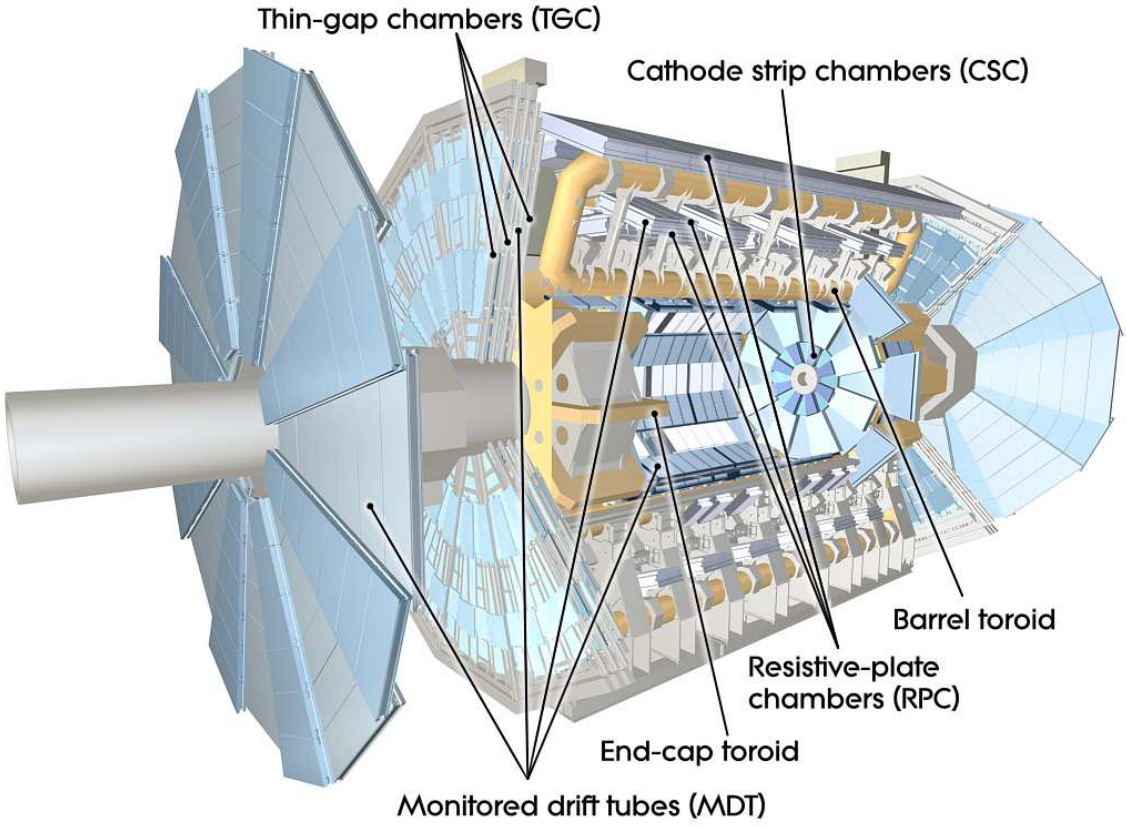


Figure 3.2.: Cut-away view of the ATLAS Muon Spectrometer. RPCs and TGCs are used as trigger chambers, CSCs and MDTs are used for precision measurement [9].

read-out channels is kept in buffers of the front-end electronics (FE). The front-end system was originally designed for a maximal Level-1 trigger rate of 75 kHz. It has been upgraded to a maximal rate of 100 kHz in 2014 [11].

Finally, the event data selected by the Level-1 trigger is read-out from the FE buffers into the read-out buffers (ROBs) via the readout drivers (RODs). The Level-1 trigger decision is based on combinations of calorimeter and muon detector informations [12]. The trigger implementation is programmable to adjust to varying luminosities and background conditions.

3.2.2. The High-Level Trigger

The High-Level Trigger consists of two parts: The Level-2 trigger and the Event Filter (EF).

The Level-2 trigger uses the RoI information provided by the Level-1 trigger which includes the position (η, ϕ), the transverse momentum (p_{T}) range and the energy sums of

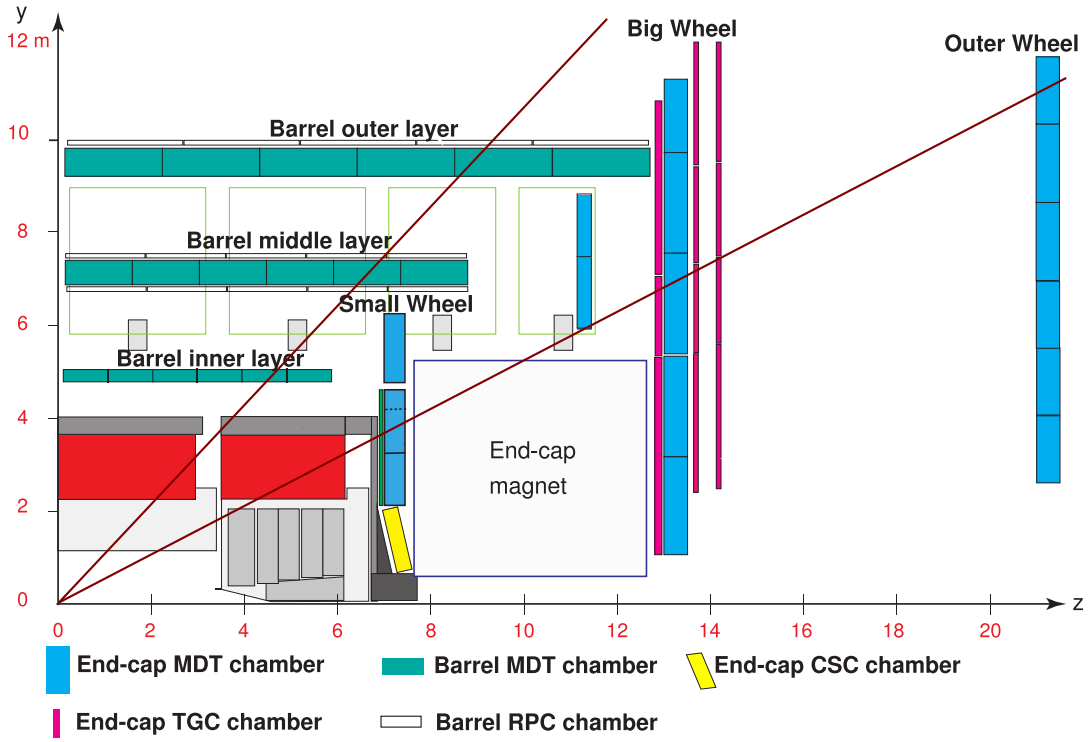


Figure 3.3.: Schematic view of one quadrant of the ATLAS muon spectrometer. The red lines indicate tracks of muons with infinite momentum. They typically traverse three detector layers allowing for a track sagitta measurement.

calorimeter cells belonging to candidate objects. While the RoI information is transmitted for all events selected by the Level-1 trigger over a dedicated data path, the data required in order to make the Level-2 trigger decision is accessed selectively. The Level-2 trigger has access to the complete event data with the full granularity, but typically needs only data from a small fraction of the detector.

The ROBs keep the complete data of the selected bunch crossing until the event is rejected or accepted by the Level-2 Trigger. The Event Filter (EF) applies the full offline reconstruction algorithms to the complete event data. Events selected by the EF are sent to mass storage while rejected trigger events are deleted.

3.3. Background Radiation in the Muon Spectrometer

The ATLAS muon detectors are exposed to unprecedentedly high background radiation of photons and of neutrons with typical energies of 1 MeV which originate from interactions of the collision products in the detector and the shielding of the beams and is uncorrelated in time with the bunch-crossings and fills the whole detector cavern [13].

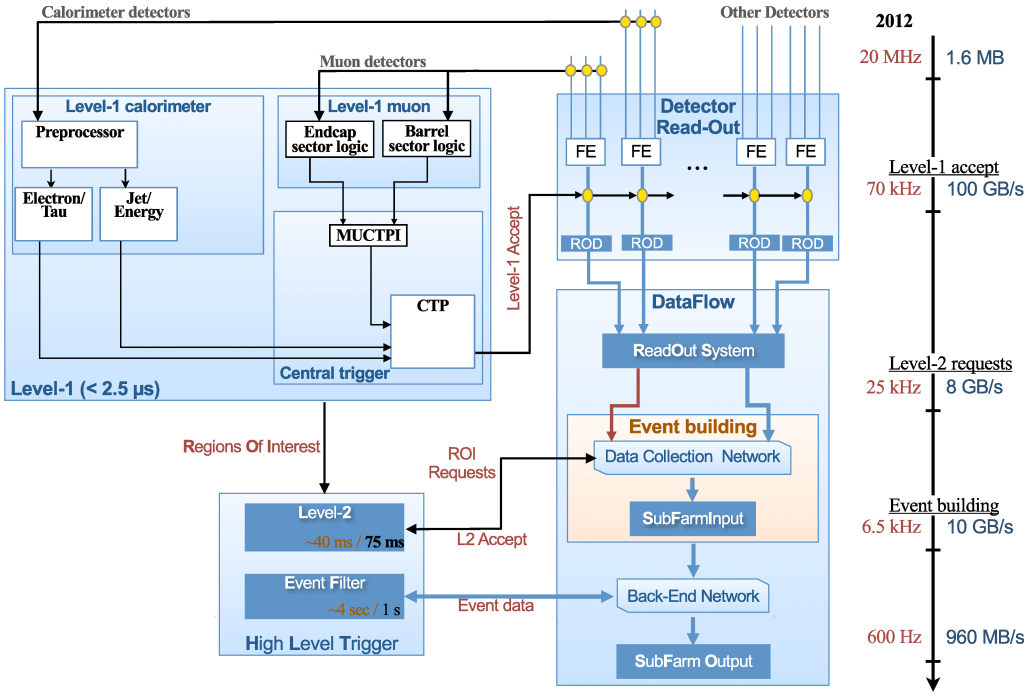


Figure 3.4.: Schematic overview of the trigger and DAQ system for collision data taking operations [12] (see text).

In the Muon Spectrometer the highest background rates occur in the innermost detector layers of the end-cap regions. The impact of the background radiation on the operation of the Monitored Drift Tube chambers is discussed in Section 4.3. This uncorrelated background radiation increases proportionally with the luminosity.

3.4. Upgrade of the ATLAS Detector at High Luminosity

Due to the the increased luminosity at the HL-LHC (see Section 2), the ATLAS detector has to be upgraded to cope with the increasing event rates and background radiation. The main limitations of the currently installed detectors are the lifetimes of the components, the increasing background, the increasing event and background rates and the radiation damage to detectors and electronic components.

Besides the inner tracking detector, which will be completely replaced for Phase-II because of radiation damage and increasing particle rates, the calorimeter and muon detector electronics as well as the trigger and data acquisition supplies have to be upgraded [14]. Developments for the MDT chamber read-out electronic and the new MDT-based Level-1 muon trigger are discussed in this thesis.

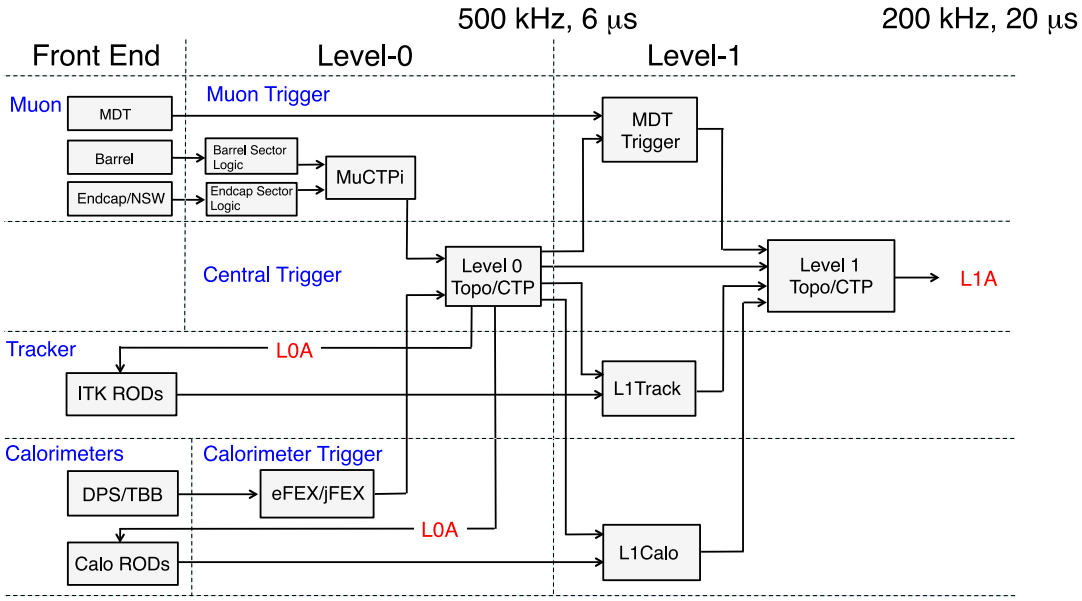


Figure 3.5.: Block diagram of the split Level-0/Level-1 trigger proposed for ATLAS Phase-II operation [14]. The MDT trigger may also be implemented already at Level-0.

3.4.1. Upgrade of the Trigger and Data Acquisition System

In order to cope with HL-LHC luminosities, it is planned to upgrade the ATLAS trigger system for Phase-II operation with splitting of the current Level-1 trigger into Level-0 and Level-1 [14].

The following properties are envisaged [14]:

- The Level-0 trigger provides the functionality of the current Level-1 trigger with an output rate of 500 kHz after a latency of 6 μs.
- The Level-1 trigger reduces the event rate to at least 200 kHz within an additional latency of at least 20 μs[2]. The rate reduction is accomplished by new track trigger in the inner detector within a RoI provided by the Level-0 trigger.
- The High-Level trigger uses offline-reconstruction algorithms to reduce the final read-out rate to 5-10 kHz.

A block diagram of the architecture of the ATLAS Level-0 and Level-1 trigger system for the Phase-2 operation is shown in Fig. 3.5. The Level-1 Calorimeter trigger will have access to the full calorimeter granularity. The Level-1 Muon trigger will use the MDT precision tracking chambers to sharpen the trigger threshold as a function of p_{T} of the muons. The Level-1 Central Trigger Processor finally combines the results of the individual Level-1 trigger systems.

[2]A latency of 60 μs is in discussion (begin 2014).

4. Muon Drift-Tube Chambers

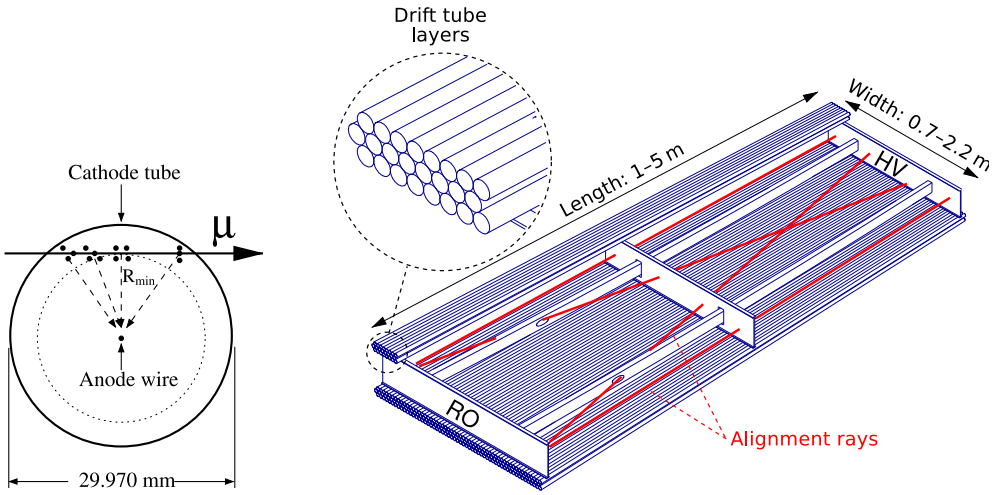
The majority of the precision tracking chambers in the ATLAS Muon Spectrometer are Monitored Drift Tube (MDT) chambers [10]. These kind of particle tracking detectors, which are high accuracy wire chambers and, therefore, commonly used in high-energy particle physics [15], provide high tracking efficiency and spatial resolution, but their performance suffers at high counting rates. Hence, drift-tube chambers with reduced tube diameter for the operation at high background rates have been developed. The first two of this small-diameter Muon Drift tube (sMDT) chambers have been installed in the ATLAS detector in 2014 [16]. More sMDT chambers are currently under construction for installation in 2017 and 2018/19 [17, 18]. Functionality and performance of MDT and sMDT chambers are discussed in the following.

4.1. Monitored Drift Tube Chambers

MDT chambers consists of aluminium drift-tubes assembled into two multi-layers with 3 or 4 layers each (see Fig. 4.1b). The tungsten-rhenium anode wire in the centre is set to a potential of 3080 V with respective to the tube wall. The main MDT parameters are listed in Tab. 4.1.

When a muon passes through an MDT tube, the Argon atoms are ionised along the path of the particle. A 100 GeV muon creates on average about 100 clusters separated typically by 100 μm per cm of typically 3 electrons in it [19]. The ionisation electrons drift towards the wire in the electric field, the ions to the tube wall (see Fig. 4.1a). The electric field strength increases with $\frac{1}{r}$ towards the wire. In the vicinity of the wire, the field is strong enough for the drifting ionisation electrons to gain enough energy to ionise the Ar gas atoms, leading to an avalanche of secondary electrons and amplification of the primary ionisation charge. For a potential of 3080 V between tube wall and anode wire of the MDT tubes, the gas gain is 20000. The passing muon can also knock out an electron from an atom of the tube wall, a so called δ-electron, which frequently passes the tube at a shorter distance to the wire than the muon (see Fig. 4.2a) masking the muon hit and leading to wrong drift-time measurement.

The minimal distance between muon track and wire can be determined by measuring the time between the muon passing and the ionised signal arriving at the wire (see Fig. 4.1a) and using a calibrated space-to-drift-time relation. In Fig. 4.6 the drift-time spectrum recorded with a uniformly irradiated MDT tube is shown. The drift velocity of the electrons depends on the drift gas. Therefore, the purity of the gas is important for the precise drift distance measurement.

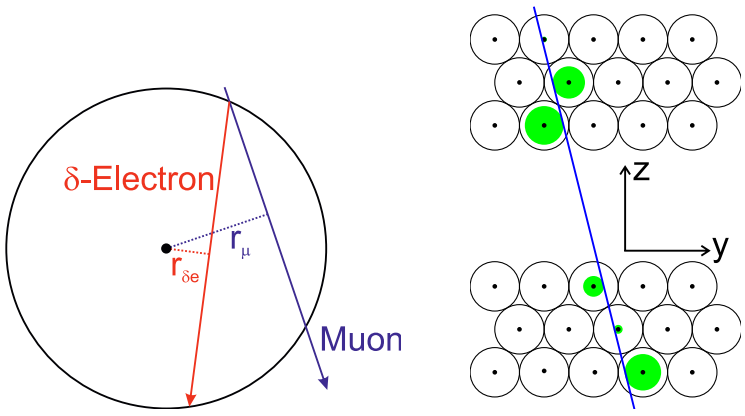


(a) (b)

Figure 4.1.: (a) Cross section of an MDT tube and (b schematic view of an ATLAS MDT chamber in the barrel region) [9].

Parameter	**MDT design value**	**sMDT design value**
Tube material	Aluminium	
Outer tube diameter	29.970 mm	15.0 mm
Tube wall thickness	0.4 mm	
Wire material	gold-plated W/Re (97/3)	
Wire diameter	50 μm	
Gas mixture	$Ar/CO_2/H_2O$ (93/7/$\leq$1000 ppm)	
Gas pressure	3 bar (absolute)	
Gas gain	20000	
Wire potential	+3080 V	+2730 V
Maximum drift-time	$\sim$700 ns	$\sim$185 ns
Average drift-tube resolution	80 μm	105 μm

Table 4.1.: Parameters of the MDT and sMDT chambers [9].



(a) (b)

Figure 4.2.: (a) Illustration of the effect of δ-electrons [20]. A muon knocks an electron out of the tube wall which may cross the tube closer to the wire than the muon and, therefore, masks the real muon hit leading to a wrong drift-time measurement.
(b) Principle of track reconstruction in the drift-tube chambers. The track is fitted to the measured drift-radii [20].

Fig. 4.2b illustrates the muon track reconstruction by minimising the distances between track and measured drift-circles (see also Section 6.3.5.5).

4.1.1. MDT Chamber Read-out Electronics

Fig. 4.3 gives an overview of the electronics circuits connected to the drift-tubes. The electrical connections are implemented on so-called hedgehog boards which supply 24 tubes each. One end of the tube is used for high-voltage supply and is terminated with the drift-tube impedance of 383 Ω to avoid signal reflections. Noise is suppressed with a low-pass filter. At the other end of the tube, the signal is capacitively decoupled from the high-voltage and further processed by active read-out electronics circuits on the so-called Mezzanine boards [21], which each contains three 8-channel ASD[1] chips which amplify and shape the signal (see Section 5) and send the digital signal to a Time-to-Digital converter (TDC) if the analogue pulse is above a predefined threshold. In order to minimise noise, the ASD circuits are differential. A block diagram of one channel is shown in Fig. 4.4.

Parameters of the chip can be set using the JTAG[2] protocol. Besides the discriminator threshold, the most important parameter is the artificial (programmed) dead time after a pulse exceeding the threshold which can be set between a minimum of 220 ns and a maximum of 820 ns and is discussed in Section 4.3.2.1. For a detailed description of all ASD parameters see [22].

[1] Amplifier Shaper Discriminator
[2] Joint Test Action Group, IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture

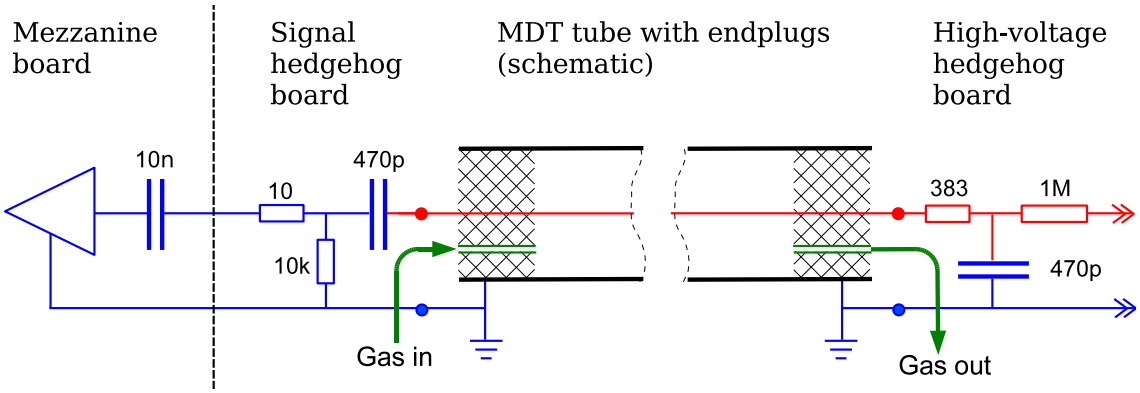


Figure 4.3.: Electrical connections to an ATLAS MDT tube [21]. One end of the tube is used for high-voltage supply and terminated with the drift-tube impedance of 383 Ω to avoid signal reflections. The other end of the tube, the signal is capacitively decoupled from the high voltage and processed by preamplifier and shaper circuits on the so-called Mezzanine boards.

The ASD chip provides two options to determine the input charge from the shaped signal. The first one is to measure the time interval during which the signal is above the threshold and the second one is to measure the pulse charge using a Wilkinson ADC [22] at the first threshold crossing time of the signal.

The digital output pulses of the ASD are sent to a 24-channel Time-to-Digital-Converter (TDC) on the Mezzanine card, which measures the threshold crossing time corresponding to the arrival time of the ionisation signal of the wire with respect to the trigger signal. The ATLAS Muon Spectrometer uses the AMT-3 chip [23] as TDC.

Up to 18 AMT chips, corresponding to 432 MDT channels (the maximum number of channels of an MDT chamber in ATLAS), are read out by a so-called Chamber Service Module (CSM) on the chamber. The CSM transmits the LHC clock and trigger signals (TTC[3]) and JTAG code to the ASD-chips and the temperature sensor measurements on the Mezzanine cards to the detector control system (DCS) via the ELMB[4]. The data of the TDCs are sent via an optical fibre from the CSM to a read-out driver (MROD[5]) module for further processing [21]. An overview of the whole read-out chain is shown in Fig. 4.5. For further details on the ATLAS MDT read-out system and its performance see [21, 24].

[3]Timing Trigger and Control
[4]Embedded Local Monitor Board
[5]MDT Readout Driver

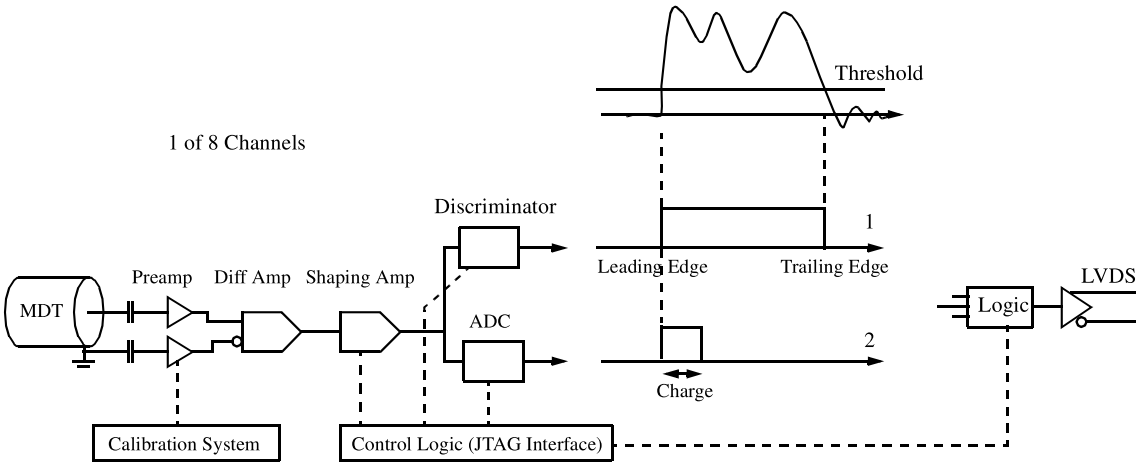


Figure 4.4.: Block diagram of one ASD channel [21]. The incoming signal is amplified, bipolar shaped (see Section 5) and digitised. The ASD chip can be operated in (1) time over threshold or (2) charge measurement mode. The ASD can be configured using the JTAG protocoll. The digital output of threshold crossing time is LVDS.

4.2. Small-Diameter Muon Drift Tube Chambers

The MDT chambers installed in the ATLAS Detector show a very good efficiency and resolution up to the highest background counting rates expected at the LHC design luminosity. But at much higher background rates as expected at the high-luminosity upgrade of the LHC (HL-LHC) they suffer from a degradation of the spatial resolution and muon detection efficiency (see Section 4.3). Therefore, drift-tube chambers with reduced tube diameter of 15 mm, so-called small-Diameter Muon Drift Tube (sMDT) chambers have been developed. For compatibility reasons, all other drift-tube parameters, especially gas mixture and pressure and the gas gain, are kept the same (see Tab. 4.1). Due to the smaller diameter, the wire potential has to be decreased to 2730 V in order to obtain the gas amplification of 20000.

The drift-tubes with the two times smaller diameter are expected to two times lower hit rate at the same background flux. The maximum drift-time of sMDT tubes is only about 185 ns [27], a factor of $\sim$3.8 smaller than for MDT tubes. Altogether, the drift-tube occupancy is reduced by a factor of $2 \cdot 3.8 = 7.6$. In addition, the reduced tube diameter leads to strong suppression of space-charge effects [25] deteriorating the spatial resolution (see Section 4.3) and allows for higher redundancy and efficiency in track segment reconstruction due to the up to two times larger number of tube layers fitting into the same volume. The average spatial resolution without background irradiation is slightly worse by about 20 μm compared to MDT tubes (see Fig. 4.7) due to the shorter average drift distances (see Fig. 4.9).

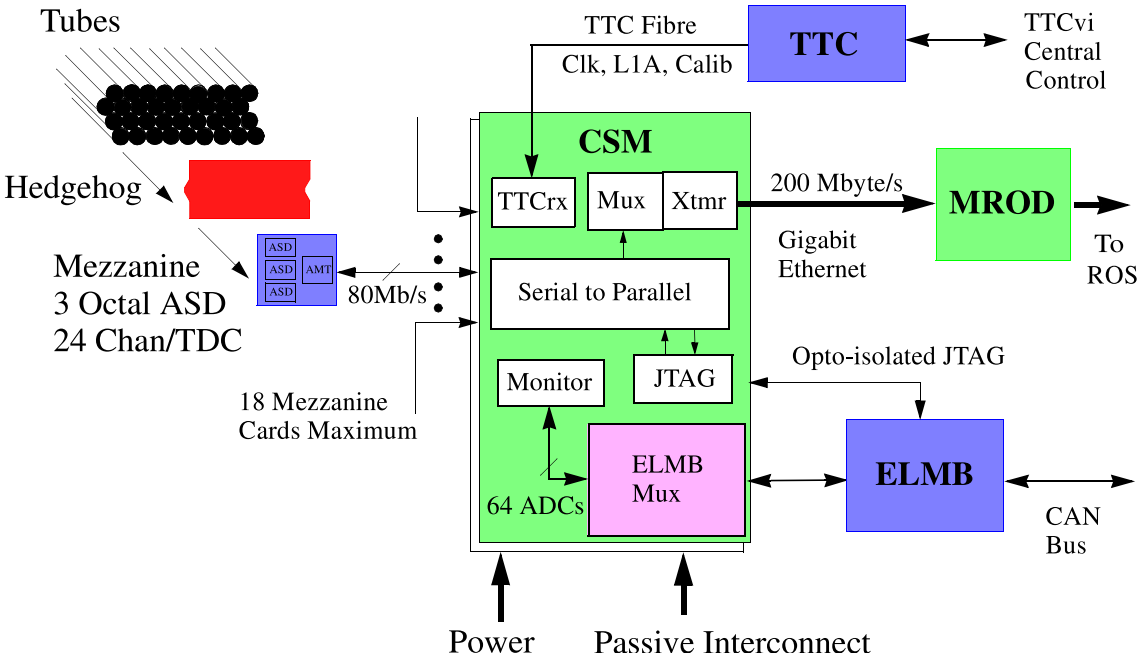


Figure 4.5.: Block diagram of the on-chamber data processing with Mezzanine boards, CSM, ELMB, TTC, and MROD [21]. While the TTC trigger signals and the data transmissions are to the MROD, the connections to the CSM are through the passive interconnect.

4.2.1. Spatial Resolution and Muon Efficiency

The performance of the sMDT tubes has already been studied extensively using the standard MDT read-out electronics [28–30].

Fig. 4.7 and Fig. 4.8 show the average MDT and sMDT single-tube spatial resolution and 3σ muon detection efficiency[6] depending on the flux and counting rate of photon conversions, respectively. In addition, the sMDT resolution is shown with the requirement $\Delta t > 600$ ns on the time interval between two successive hits, which is equivalent to operation with a dead time of 600 ns.

The read-out electronics behaviour has a strong impact on the resolution and 3σ-efficiency of the sMDT tubes at very high background rates. The sMDT resolution and efficiency depend strongly on the electronics dead time and the signal shaping. By optimisation of signal shaping the resolution and efficiency at high background rates of the sMDT tubes operated with short dead time settings can be improved significantly (see Section 5).

[6]The probability for a hit to be measured on the extrpolated muon trajectory within three times the drift-tube spatial resolution as a function of the drift-radius.

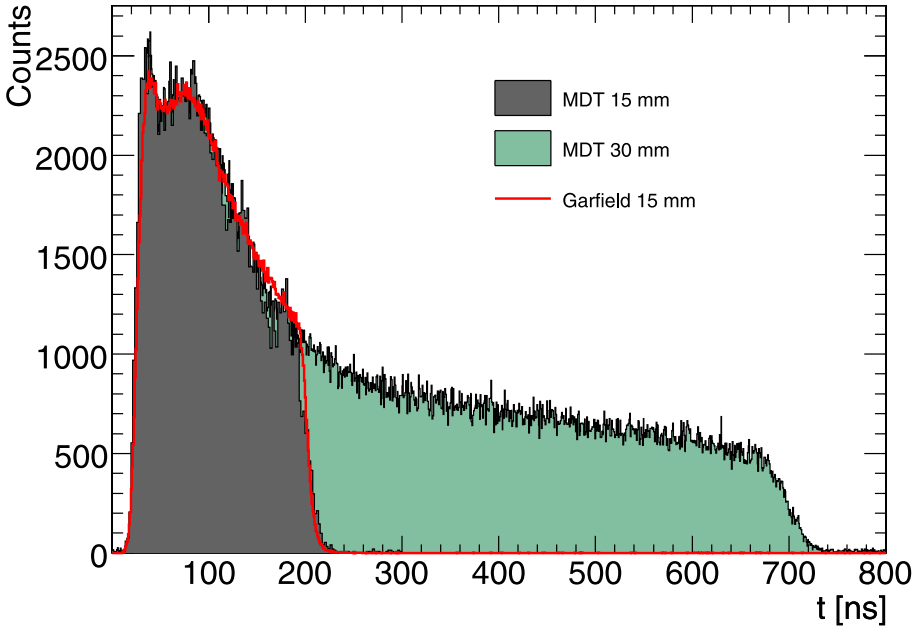


Figure 4.6.: Drift-time spectra of MDT and sMDT tubes operated with Ar:CO2 (93:7) gas mixture at 3 bar absolute pressure and a gas gain of 20000 [25]. The measurement with cosmic ray muons is compared with simulation (Garfield [26]) for the 15 mm diameter tubes.

4.3. High-Rate Phenomena

Most of the hits in the MDT chambers are caused by the γ and neutron background radiation in the ATLAS cavern (see Section 3.3), which cause space charge of slow drifting ions in the tubes and mask muon hits due to the dead time of the read-out electronics.

4.3.1. Space Charge Effects

The ion space charge in the drift-tubes caused by the background hits modifies the electric field and, hence, the drift-velocity and the gas amplification. Due to the stochastic nature of the background hits, the space charge and, therefore, the drift velocity vary in time, leading to a degradation of the spatial resolution increasing with the drift-distance. This effect of space charge fluctuations, which cannot be taken into account in calibration of the space to drift-time relationship, is shown in Fig. 4.9.

The shielding of the wire potential by the ion space charge leads to loss in gas gain (see Fig. 4.10), smaller signals and, therefore, degradation of the time resolution. This effect dominates for muon tracks passing the tube close to the wire.

Close to the tube wall, the effect of space charge and, consequently, of the electric field and of the drift-velocity on the spatial resolution dominates [32].

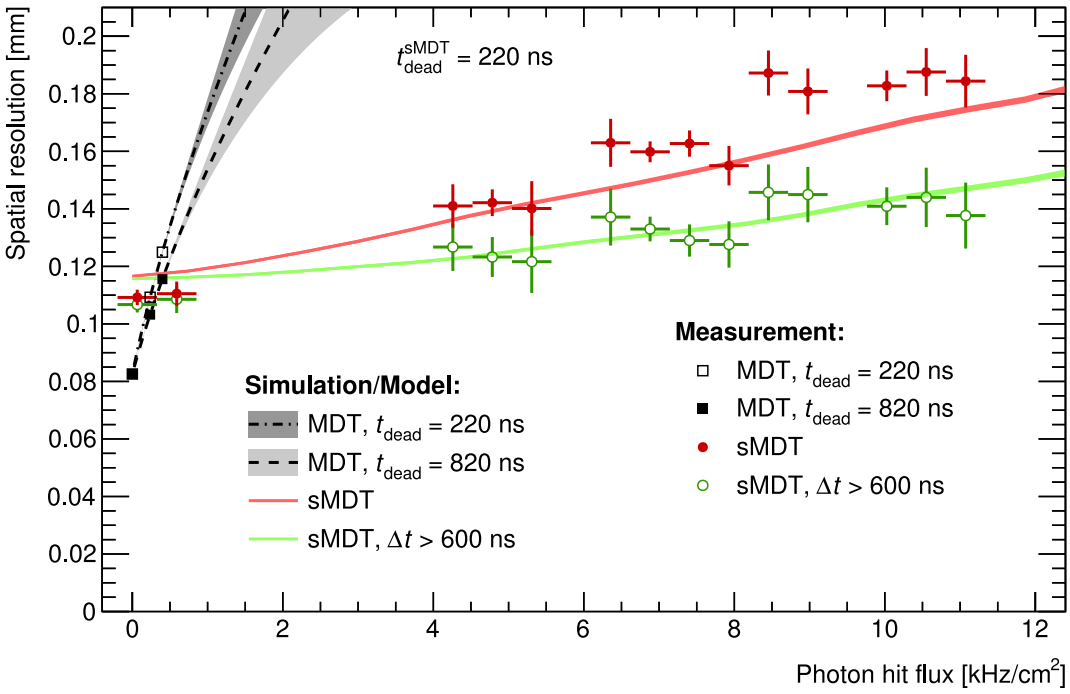


Figure 4.7.: Average spatial resolution of 1 m long sMDT and MDT drift-tube depending on the flux of background photon conversions for different electronics dead time settings of the read-out electronics [27]. In addition, the sMDT resolution is shown for the requirement $\Delta t > 600$ ns on the time interval between two successive hits is shown, which is equivalent to operation with a dead time of 600 ns. Solid coloured lines show the simulated sMDT resolution for different dead time settings.

4.3.2. Read-Out Electronics Effects

In Fig. 4.11 a typical amplified signal from an sMDT tube muon is shown. The fast rising leading edge is caused by the electron avalanche, while the slowly drifting ions cause the long trailing edge of the unshaped pulse.

Due to the different arrival times of the ionisation electron clusters along the muon path, the signals can show several peaks which may result in several discriminator threshold crossings while only the first threshold crossing time is of interest for the drift-time measurement. In order to suppress these secondary discriminator threshold crossings, electronics dead time programmable between a minimum of 220 ns and a maximum of 820 ns which covers the maximum drift-time of the MDT tubes during which electron clusters may arrive, is used in the ASD chip (see Section 5.2).

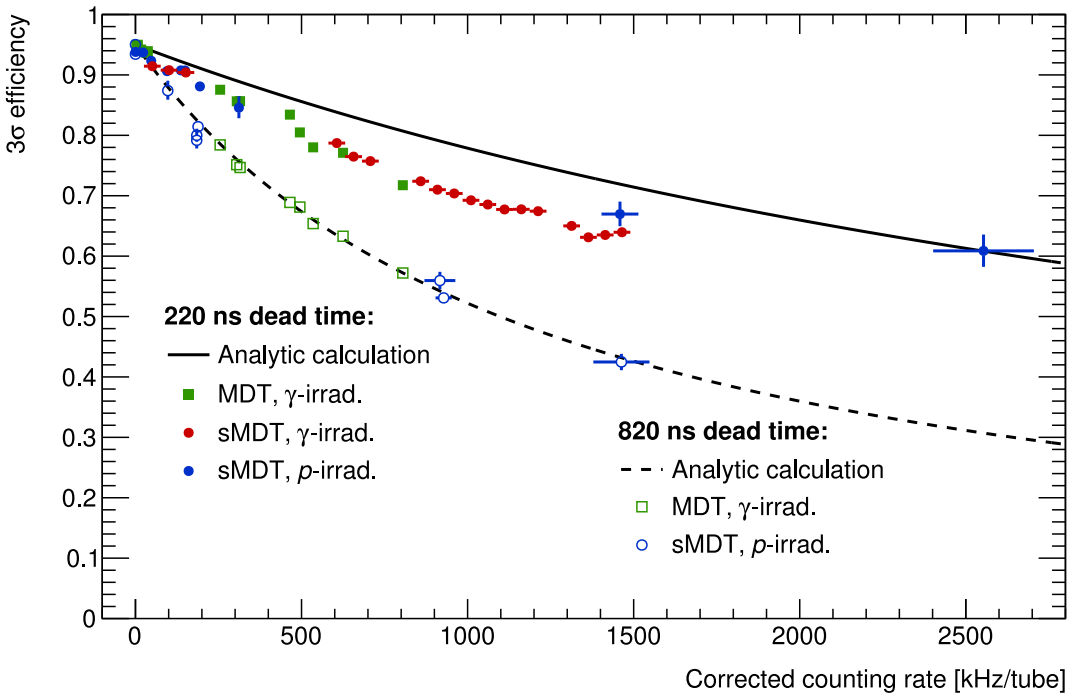


Figure 4.8.: 3σ-efficiency of MDT and sMDT tubes depending on the dead time-corrected background γ counting rate (see Section 4.3.2.1) for minimum and maximum electronics dead time settings of the ASD chip [27]. The analytic calculation is based on Eq. 4.4.

Without additional signal shaping, the tails cause a shift of the baseline at high counting rates. From different signal shaping options (see Section 5.1), the ASD uses bipolar shaping (see the blue curve in Fig. 4.11). Bipolar shaping differentiates the signal suppressing low frequencies. It provides baseline stability up to high rates, but causes an undershoot with a length corresponding to the length of the ion tail.

4.3.2.1. Dead Time Effects

During the electronics dead time τ, the read-out electronics is insensitive to any further hits arriving. Therefore, the muon detection efficiency decreases with increasing background rate depending on the dead time. When m is the true counting rate and k counts are registered in a read-out time window T, a total dead time $k\tau$ is accumulated, since each detected hit triggers the electronics dead time. During the total dead time, $mk\tau$ counts are lost. The true number of hits in the time window is (see [33])

$$mT = k + mk\tau \ , \tag{4.1}$$

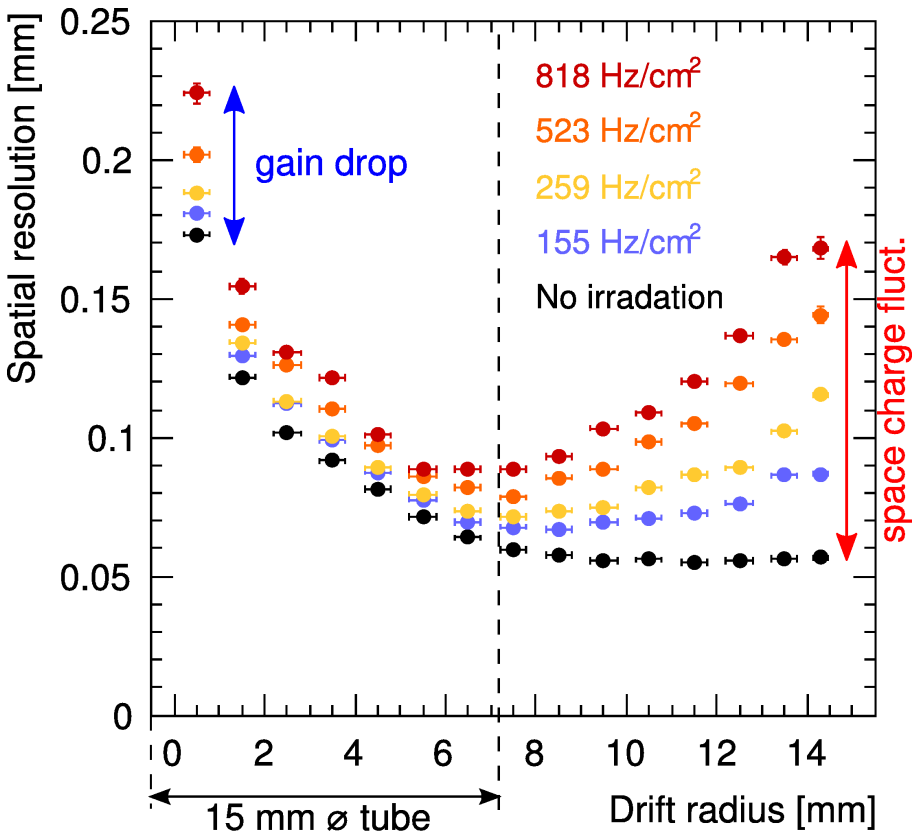


Figure 4.9.: Radial dependence of the MDT spatial resolution for different photon irradiation rates [31]. The degradation of the resolution with increasing background flux due to fluctuations of the space charge and, therefore, of the drift-field is limited to the region r > 6 mm and increases with the drift distance. Loss of gas gain due to shielding of the wire potential decreases the signal amplitude which leads to a worsening of the resolution in particular near the wire.

leading to

$$m = \frac{\frac{k}{T}}{1 - \frac{k}{T}\tau} \ . \tag{4.2}$$

Taking into account the linear dependence of the muon efficiency on the observed counting rate $r = \frac{k}{T}$

$$\epsilon(r) = \epsilon_0 \cdot (1 - r \cdot \tau) \ , \tag{4.3}$$

where ϵ_0 is the muon efficiency in the case of negligible hit rate, one obtains

$$\epsilon(m) = \frac{\epsilon_0}{1 + m\tau} \ . \tag{4.4}$$

The observed and the true counting rate differ because also background hits are masked by preceding hits. In order to obtain maximum efficiency, the dead time has to be as short as possible while minimising the probability for secondary threshold crossings.

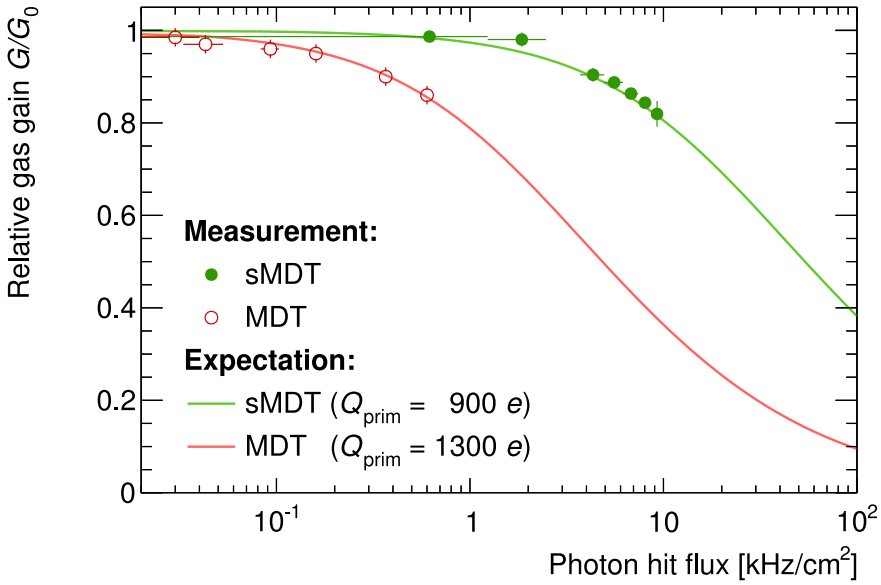


Figure 4.10.: Dependence of the relative gas gain G/G0 in MDT and sMDT tubes on the flux of photon conversions ($G_0 = 2 \cdot 10^4$) [27]. The expectation is based on primary ionisation charges Q_{prim} of the converted photons.

For the sMDT tubes, the electronics dead time can be reduced to at least the maximum drift-time of 185 ns, about 3.8 times shorter than for the MDT tubes. The ASD chip, of the moment, only allows for a minimum dead time of ∼200 ns determined by the time needed by the Wilkinson ADC for the signal charge measurement.

4.3.2.2. Signal Pile-Up Effects

With bipolar shaping and short electronics dead times scheme, muon signal pulses may be overlaid at high counting rates on top of the undershoot of preceding photon or neutron background pulse leading to a reduction of amplitude and rise time of the secondary muon pulse at the baseline and the discriminator threshold and to a shift of the threshold crossing time (see Fig. 4.12).

These signal pile-up effects lead to hit efficiency loss and degrade the time resolution. The time slewing corrections (see Section 5.4.2.1) based on the signal charge measurement using the Wilkinson ADC implemented on the ASD chip recover only very little of the pile-up degradation (see [27]).

The pile-up effects can be effectively suppressed by optimisation of the shaping or baseline restoration (see Section 5).

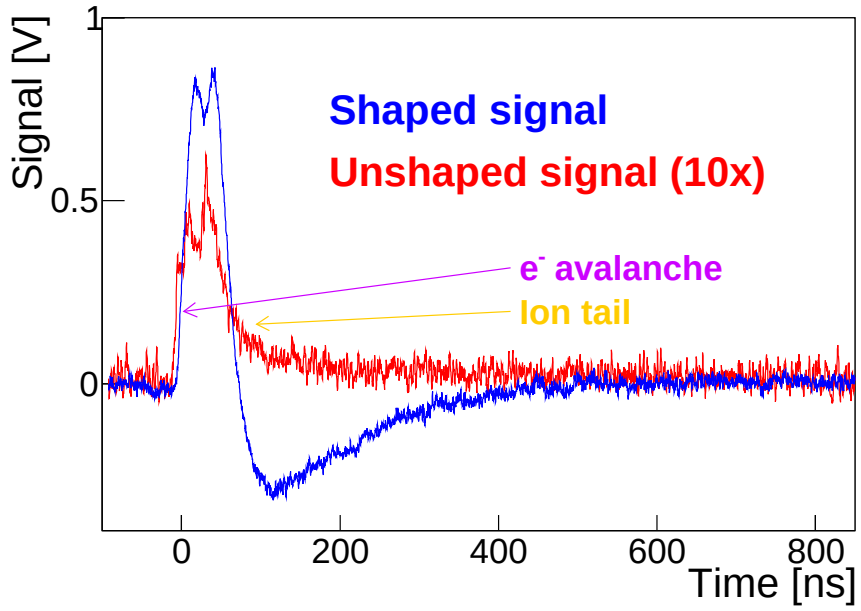


Figure 4.11.: Typical signal of a muon in an sMDT tube amplified with a 10 kΩ transimpedance amplifier before (red line) and after (blue line) bipolar shaping. While the electron avalanche causes the steeply rising leading edge of the signal pulse, the slow drifting ions lead to the long trailing edge of the unshaped pulse which is removed by signal shaping (Measurement bandwidth: 200 MHz).

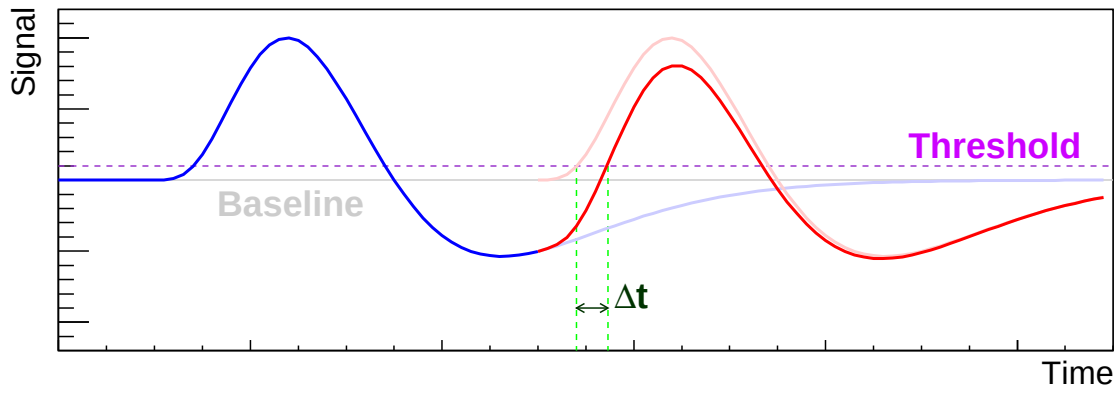


Figure 4.12.: Illustration of signal pile-up effect with bipolar shaping. Due to the signal undershoot, the threshold crossing time of the successive pulse is shifted by Δt and the amplitude is reduced.

5. Optimisation of Drift-Tube Read-Out Electronics for High Counting Rates

At high counting rates, the read-out electronics has strong impact on the performance of sMDT tubes. Bipolar shaping as used in the present version of the read-out electronics provides baseline stability, but its performance is limited by signal pile-up. In order to reach a higher rate capability, baseline restoration can be used.

In the following, the application of baseline restoration for the sMDT tube read-out electronics is discussed. Parts of this chapter are also presented in [34–36].

5.1. Signal Shaping

In order to minimise the effect of noise and baseline shifts due to slowly decreasing trailing pulses edges, analogue detector signals need to be processed. This processing is called signal shaping.

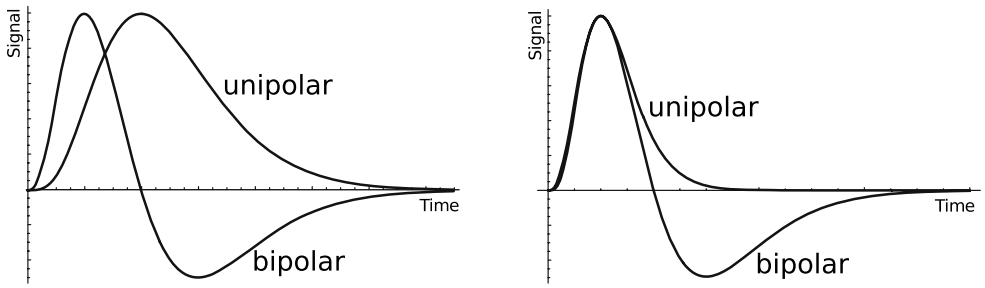
Two commonly used signal shaping concepts are the so-called unipolar and bipolar shaping [32].

5.1.1. Unipolar and Bipolar Signal Shaping

If linear[1] filters with negligible differentiation behaviour are used for signal shaping, the pulse processing is called unipolar shaping (an overview about different kind of unipolar shaping is given in [37]). Besides the simple CR high-pass and RC low-pass filter, also more complex filter types can be used. Details on signal shaping are discussed in Appendix A.2.1.

Signals with slow decreasing falling edges processed with unipolar shaping can cause a shift of the baseline (see Section 4.3.2). Hence, the differentiation of the shaped signal has been proposed in [38], leading to the so-called bipolar shaping. Due to the differentiation slow changing edges are set to the baseline, so even in case of a sequence of pulses the baseline stays stable. The differentiation of the trailing edge causes a response with contrary polarity, this effect is the undershoot of the bipolar shaping, see Fig. 5.1 (the corresponding circuits and calculation are presented in Appendix A.2.1). Due to charge conservation, the area below the pulse is zero (the area of overshoot and undershoot are equal). When the bandwidth of the differentiator is limited, this argument is not valid any more and the total area below the pulse may not be zero (see Appendix A.2.3).

[1] A given input pulse $I_{in}(t)$ results in an output pulse $V_{out}(t)$, where $V_{out}[c \cdot I_{in}(t)] = c \cdot V_{out}[I_{in}(t)]$.



(a) (b)

Figure 5.1.: δ-response illustration of unipolar and bipolar shapings [32]. (a) shows shapings with identical parameters, hence the bipolar shaped response is the derivative of the unipolar shaped response. In (b), the shaping parameters of the bipolar shaper are chosen in order to the gain the same peaking time.

In Fig. 5.1a-5.1b the δ-responses for unipolar and bipolar shaping are illustrated. If the shaping parameters are identical (see Fig. 5.1a), bipolar shaping shows a smaller peaking time[2] with respect to unipolar shaping due to the derivative of the signal (see Fig. 5.1b). In order to gain the same peaking time, the parameters of the bipolar shaper needs to be modified, leading to a longer signal response. Hence, the advantage of baseline stability of the bipolar shaping trades off against pulse length.

A more detailed description of unipolar and bipolar shaping and its application for MDT read-out electronics is given in [32, 39]. Electrical circuits for differentiation are discussed in Appendix A.2.3.

5.1.2. Baseline Restoration

In order to minimise the pile-up effect of bipolar shaping at high counting rates (see Section 4.3.2.2), the undershoot of the signal response needs to be minimised. This minimisation is called baseline restoration (BLR).

If all input pulses have similar pulse height and length, baseline restoration can be realised by the use of additional filters (see [40]). Otherwise, a non-linear solution have to be chosen, where the decision depends on the application.

The principle of the simplest one is shown in Fig. 5.2a. During the undershoot the switch S is closed, leading to signal suppression (CR filter). The switch can be implemented using passive components (diode with capacities and resistors) as shown in Fig. 5.2b. Due to its switching time and its non-linear voltage-current characteristic curve, it may be useful to set a working point for the diode using the current I_{Base}. In case of a fixed current, the concept is called passive BLR (see [41]). By setting the current depending on the input signal, this concept can be further improved, leading to the so-called active baseline restoration, see [42, 43].

[2] Time when the δ-response reaches the maximum.

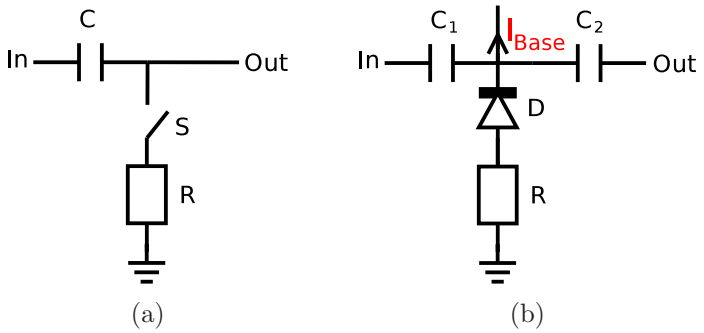


Figure 5.2.: (a) Basic principle of passive, active and gated baseline restoration. During the undershoot the switch S is closed, leading to signal suppression (CR filter). (b) Possible implementation of passive (Current I_{Base} is zero or fixed) and active (Current I_{Base} depends on signal on In) baseline restoration.

If an additional circuit for undershoot detection controlling the switch S is used, the concept is called gated BLR, for further information see [44, 45]. Alternatively, it is also possible to restore the baseline by adding the inverted signal to input signal, this concept is discussed in [45, 46].

5.2. The ASD Chip

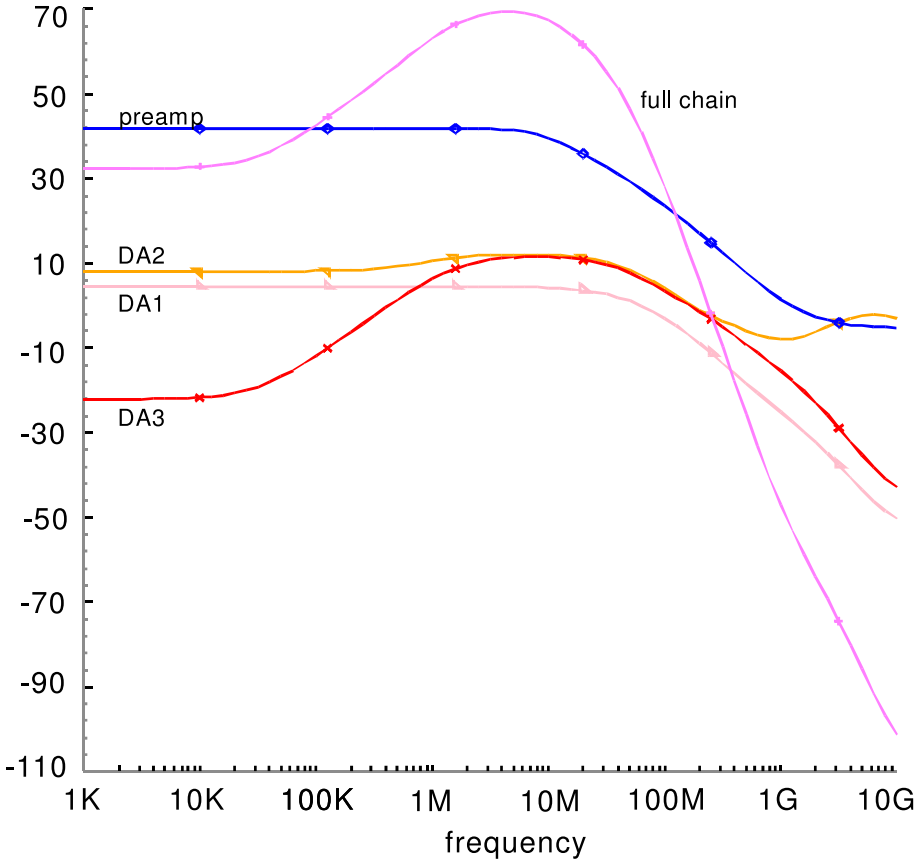
The ASD chip [22] is an octal CMOS Amplifier/Shaper/Discriminator using bipolar shaping optimised for the ATLAS MDT chambers (see Section 4.1). In Fig. 5.4 one channel is shown as block diagram. The circuit is fully differential and consists of four stages.

Pre-Amplifier The pre-amplifier (preamp) consists of an "active" and an associated "dummy" amplifier. While the active amplifier is capacitively coupled to the drift-tube, the dummy amplifier is left floating providing DC balance to the subsequent stages as well as some degree of noise suppression. The gain of the pre-amplifier is shown in Fig. 5.3a as a function of the frequency. It has a 3dB-bandwidth[3] of 11.94 MHz.

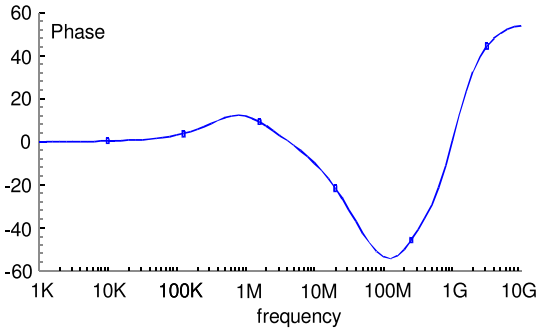
Shaper The shaper consists of three stages:

- ***DA 1*** is a simple amplifier with a 3dB-bandwidth of 45 MHz. Its main purpose is to ensure the differential signal being completely complementary.
- ***DA 2*** implements a pole/zero network (see Appendix A.2) in order to cancel the very long time constant component of the positive ion MDT pulse.

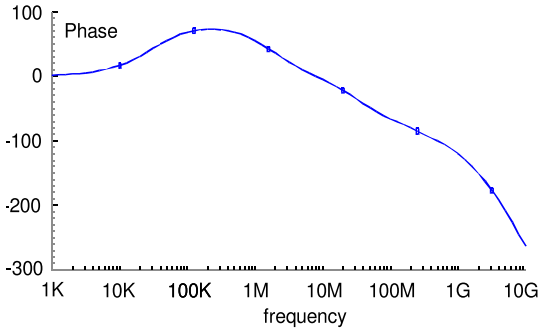
[3]Frequency where the gain is reduced by 3 dB with respect to the maximum gain.



(a) Gain (dB)



(b) *DA 2*



(c) *DA 3*

Figure 5.3.: (a) Gain (dB) of ASD pre-amplifier (preamp), of the filter stages *DA 1-3* and full chain of theses stages depending on the frequency [22].
Frequency dependent phase of (b) the *DA 2* stage (pole/zero filter) and (c) the *DA 3* stage (RC network) [22].

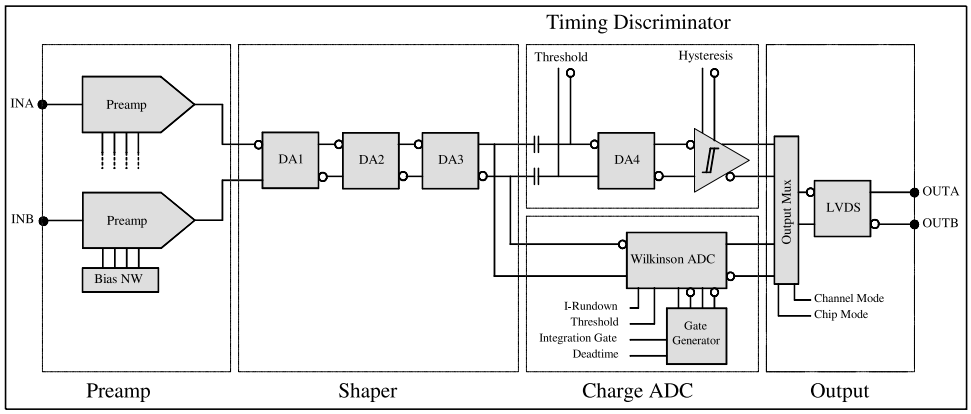


Figure 5.4.: Block diagram of one channel of the ASD chip consisting of four stages [22] (see text).

- ***DA 3*** uses a simple series RC network with a RC product of approximately 50 ns to effect a bipolar shaping stage. In contrary to the preamp and *DA 1-2*, *DA 3* is non-linear for signals larger than one third of the maximum signal range.

The gain depending on the frequency of *DA 1-3* is plotted in Fig. 5.3a.

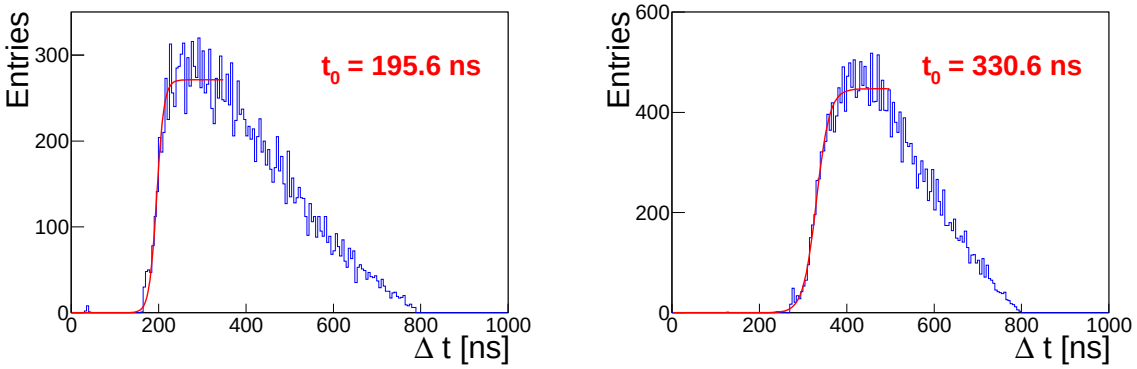
Discriminator The discriminator consists of a timing discriminator and a Wilkinson ADC[4] operated in parallel. The timing discriminator applies the threshold voltages and amplifies the signals with an additional amplifier (*DA 4*) with a gain of 16 dB and a 3dB-bandwidth of 85.7 MHz.

The ADC measures the leading edge pulse charge in order to perform time slew correction in offline analysis to enhance timing resolution. Due to measurement time of the Wilkinson ADC, a programmable dead time between 200 and 800 ns for the discriminator is implemented differing between unique ASD chips. The actual dead time can be measured in operation by plotting the time difference between two proceeding hits and determine the minimum of the distribution. In Fig. 5.5 this distribution for the two different ASD chips is shown. For the measurement results presented in this thesis, the ASD chip of Fig. 5.5a has been used.

Besides in the ADC mode, the ASD chip can also operated in time-over-threshold mode which provides information about the pulse length above the threshold.

The final output information consists of the threshold carrying signal of the leading edge pulse and either of threshold carrying signal of the falling edge in time-over-threshold mode or of the digitised input pulse charge in ADC mode. These signals are converted by a LVDS driver into low-level output signals.

[4]The Wilkinson ADC integrates the signal charge onto a holding capacitor and measure its value by running it down at constant current.



(a) (b)

Figure 5.5.: Time difference between two successive hits measured with two different ASD chips. The onset t_0 of the distribution, which is determined by fitting a Fermi function, corresponds to the effective dead time.

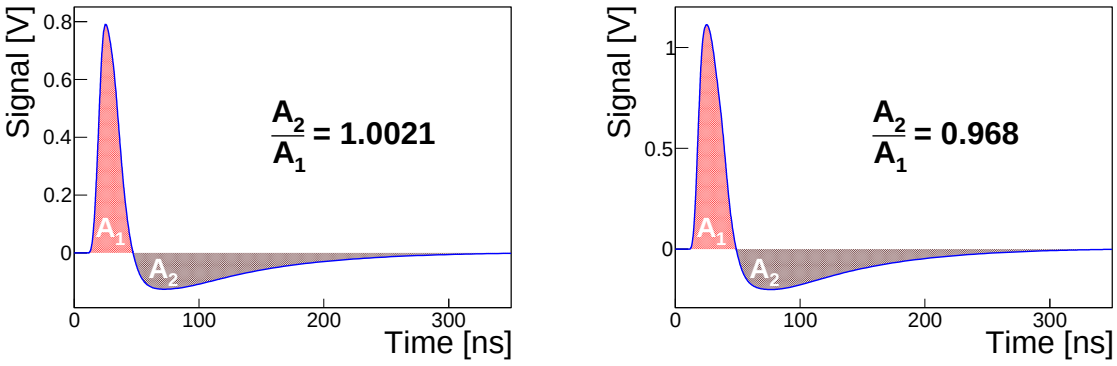
Besides the shaper stages *DA 2-3*, the preamp and *DA 1* are also essential for the shaping due to their limited bandwidth. Fig. 5.3a shows clearly that the magnitude of the preamp and *DA 2/3* 3dB-bandwidth is the same.

In order to set a starting point for a successor of the ASD chip, a LTSpice[5] simulation has been set up (see [47]). The δ-response for two different signal amplitudes obtained with this simulation is shown together with the ratio of the area below over- and undershoot in Fig. 5.6. Due to the bipolar shaping scheme (see Appendix A.2.1), the ratio is approximately one. In the following, the results obtained with this simulation are used for comparison.

5.3. A Discrete Pulse Shaper for sMDT Tubes (ASBC)

In order to test and understand the application of baseline restoration for the sMDT read-out, a shaping circuit with properties similar to the ASD has been designed. It is called ASBC - Amplifier, Shaper, Baseline-Restorer, Comparator.

The design was carried out according to the gain of the ASD shaper stages *DA 2* and *DA 3*, the gain of preamp and *DA 1* were approximated to be constant. The relevant frequency range has been defined with 2 MHz to 100 MHz, according to the parameters of a typical muon pulse (∼10 ns rise time and ∼500 ns fall time, see Fig. 4.11).



(a) (b)

Figure 5.6.: ASD δ-response (8 ns rise time, shaped on 1.2 pF) for (a) 50 mV and (b) 100 mV amplitude obtained from [47]. Due to the bipolar shaping scheme, the area below over- and undershoot are approximately equal. The signal amplitudes indicate the non-linearity of *DA 3* (twice the input does not lead to twice the output).

5.3.1. The ASBC Circuit

The structure and a photograph of the ASBC are shown in Fig. 5.7a and 5.7b. For the sMDT signal amplification, a transimpedance amplifier[6] with 10 kΩ transimpedance[7] and 700 MHz bandwidth is used, corresponding to the combination of the pre-amplifier and *DA 1* of the ASD. The signal shaping is conducted in three stages, where the first one does ion tail cancellation, the second one additionally shapes and differentiate the signal and the third one restores the baseline. The resulting amplified and shaped signal is then digitised, using a comparator[8] with 1.6 ns propagation delay with 1 ps rms random jitter. The voltage on the second input of the comparator can be modified to gain an adjustable signal threshold.

5.3.1.1. Filter Stage 1

The schematic of the filter stage 1 (purpose ion tail cancellation, corresponding to *DA 2* of ASD) is shown in Fig. 5.8. The circuit consists of a voltage divider, which is also used for cable termination, and an AC-coupled inverting amplifier, where a pole-zero network is used as input resistor of the inverter.

[5]SPICE (Simulation Program with Integrated Circuit Emphasis) implementation of Linear Technology.
[6]HMC799LP3E, Hittite Microwave Corporation (*PreAmp*), see [48].
[7]A transimpedance amplifier is a current-to-voltage converter (inverted). Therefore, the gain g is described with $g = \frac{U}{I} = [\Omega]$.
[8]ADCMP605, Analog Devices, see [49].

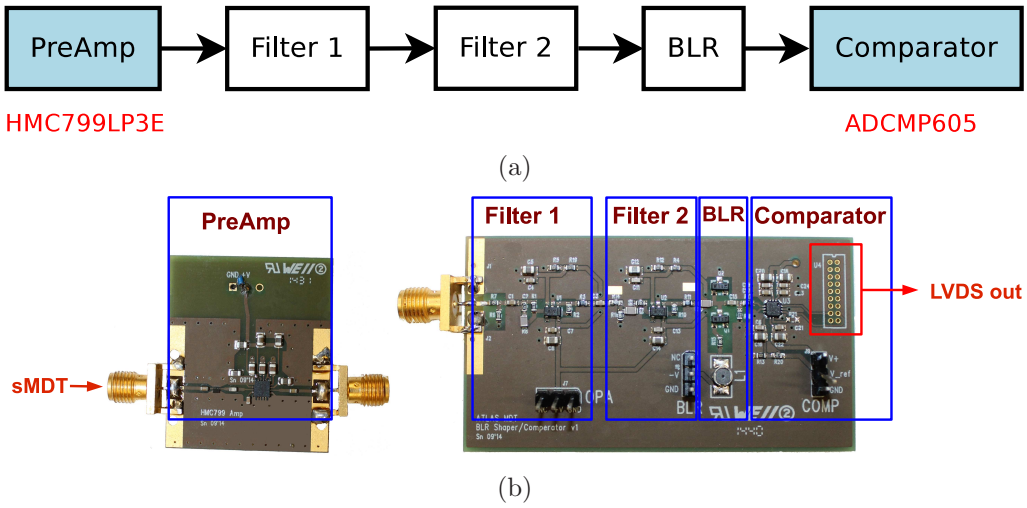


Figure 5.7.: (a) Structure and (b) photograph of the ASBC (Amplifier, Shaper, Baseline-Restorer, Comparator) electronics. For sMDT signal amplification (*PreAmp*) a transimpedance amplifier (HMC799LP3E, see [48]) and for digitisation a comparator (ADCMP605, see [49]) is used. The pulse shaping is conducted in three stages, where the third one also restores the baseline.

The complex resistance Z_{pz} of the pole-zero network is[9]

$$Z_{pz}(\omega) = R_3 \| (R_4 + \frac{1}{i\omega C_2}) \tag{5.1}$$

In case of an ideal operational amplifier[10] (OPA_1), a large resistance of the pole-zero network with respect to R_2 and a big capacity of C_1[11], the complex gain G_1 is calculated with

$$G_1(\omega) = -\frac{R_2}{R_1 + R_2} \cdot \frac{R_5}{Z_{pz}(\omega)} = -\frac{R_2 \cdot R_5}{R_1 + R_2} \cdot \frac{(R_3 + R_4) \cdot \omega C_2 - i}{R_3 \cdot (R_4 \cdot \omega C_2 - i)} \,. \tag{5.2}$$

The magnitude and phase of Eq. 5.2 are shown in Fig. 5.9a and Fig. 5.9b. While the magnitude is bounded between the limits defined by the pole-zero network, the phase show a maximum for a certain frequency (see Section A.2.5).

Eq. 5.2 describes the high-pass behaviour of the circuit, indeed, it is necessary to include the low-pass features the ASD DA2 (see Fig. 5.3a). Thus, the limited bandwidth of a real operational amplifier[12] is used and the value of the feedback resistor R_5 is chosen to gain the necessary bandwidth. The values of the parts shown in Fig. 5.8 are listed in Tab. A.2. The resulting gain[13] is shown Fig. 5.12. The magnitude and phase are in accordance with the corresponding ASD parameters.

[9] $\|$ indicates parallel arrangement.
[10] Infinite input resistance, infinite gain, infinite bandwidth
[11] The capacity has to be big enough to provide AC-coupling without signal shaping.
[12] For this application, THS4304 [50] is used.
[13] Calculation based on the gain-bandwidth-product GBW=870 MHz (see [50]).

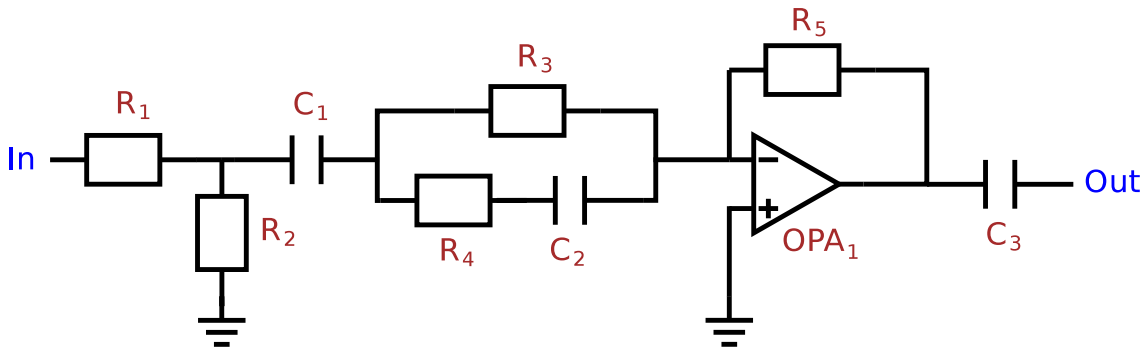
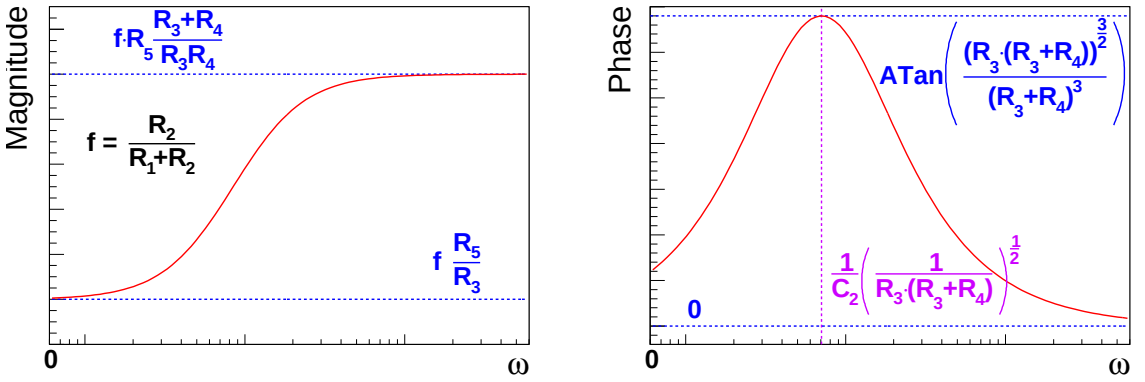


Figure 5.8.: Schematic of filter stage 1, see Fig. 5.7a. It consists of an AC-coupled inverting amplifier, where a pole-zero network is used as input resistor of the inverter. Filter stage 1 is a high-pass for sMDT signal ion tail cancellation.



(a) (b)

Figure 5.9.: Filter stage 1 magnitude (a) and phase (b) (see Eq. 5.2) depending of the frequency. The determination of the bounds is discussed in Section A.2.5.

5.3.1.2. Filter Stage 2

The schematic of the filter stage 2, which consists of a voltage divider and an inverting amplifier with an RC-circuit as input resistance, is shown in Fig. 5.10. The circuit corresponds the differentiator shown in Fig. A.2c, its purpose is signal shaping and signal differentiation (see Eq. A.17) and its functionality corresponds to *DA 3* of the ASD.

The complex resistance Z_{RC} of the RC-circuit is

$$Z_{RC} = R_8 + \frac{1}{i\omega C_4} \ , \tag{5.3}$$

leading to a complex gain $G_2(\omega)$ of the circuit under the assumption of an ideal operational amplifier and a large resistance of the RC-circuit with respect to R_7

$$G_2(\omega) = -\frac{R_7}{R_6 + R_7} \cdot \frac{R_9}{Z_{RC}} = -\frac{R_7 \cdot R_9}{R_6 + R_7} \cdot \frac{\omega C_4}{\omega R_8 C_4 - i} \ . \tag{5.4}$$

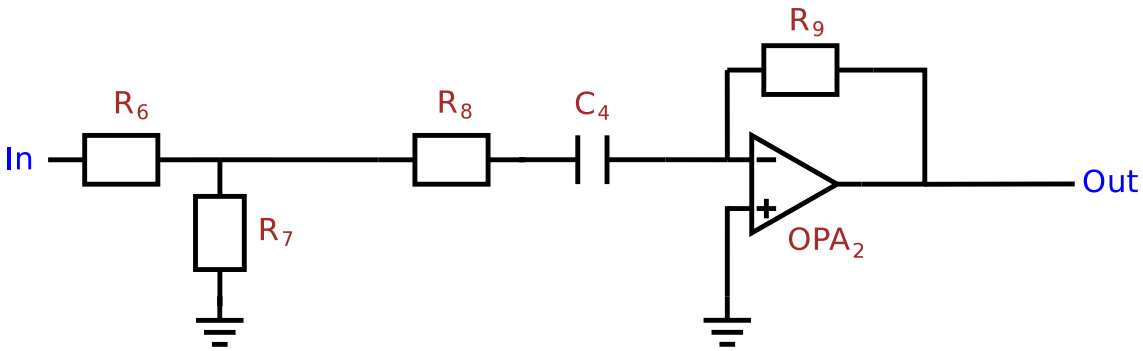
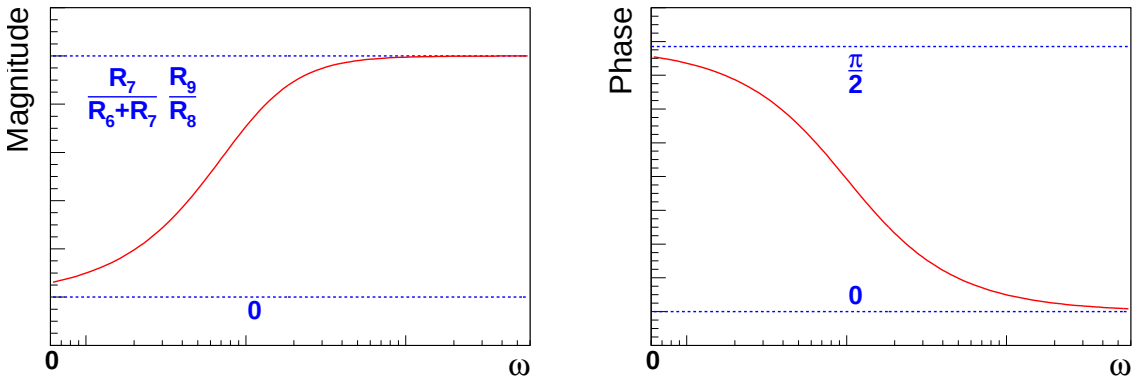


Figure 5.10.: Schematic of filter stage 2 (see Fig. 5.7a). It consists of an inverting amplifier, where an RC-circuit is used as input resistor of the inverter. Filter stage 2 is used as differentiator.



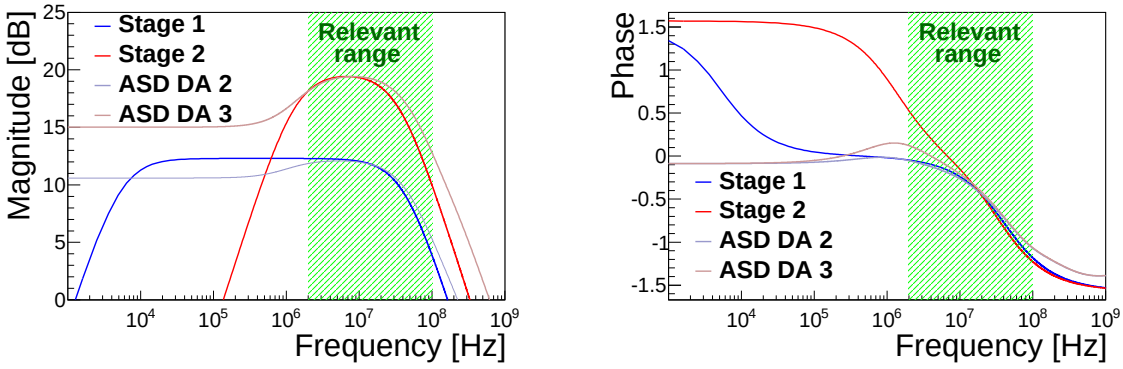
(a) (b)

Figure 5.11.: Filter stage 2 magnitude (a) and phase (b) (see Eq. 5.2) versus frequency. The determination of the bounds is discussed in Section A.2.6.

The magnitude and phase of Eq. 5.4 are shown in Fig. 5.11a and Fig. 5.11b. The circuit behaves as filter stage 1 with $R_3 \to \infty$ in Eq. 5.2. Fig. 5.11a is Fig. 5.9a shifted and Fig. 5.11b shows the falling edge of Fig. 5.9b. In order to obtain the same gain as DA3 of the ASD (see Fig. 5.3a), low pass behaviour has to be added to filter stage 2. Thus, the amplifier bandwidth is adjusted with the feedback resistor R_9. The resulting gain is illustrated in Fig. 5.12. The magnitude shows a small difference for high frequencies of the relevant range and the phase for lower frequencies, respectively.

5.3.1.3. BLR Stage

The schematic of the BLR stage is shown in Fig. 5.13a. It uses a passive baseline restoration concept and corresponds to the circuit shown in Fig. 5.2b, where the resistor R_{10} and the inductance L_1 are used together as current source and the transistor T_2 is connected in a



(a) (b)

Figure 5.12.: (a) Gain magnitude and (b) phase of stage 1 and stage 2 including the frequency behaviour (gain-bandwidth-product) of the operation amplifiers in comparison with ASD *DA 2* and *DA 3*, where the ASD magnitude is multiplied and the phase is shifted to reach the ASBC level.

way to act as diode. The second transistor T_2 defines the current pointer and compensates the impact of small temperature changes, the capacitor C_6 provides AC-coupling and R_{11} is a pull-down resistor defining the baseline.

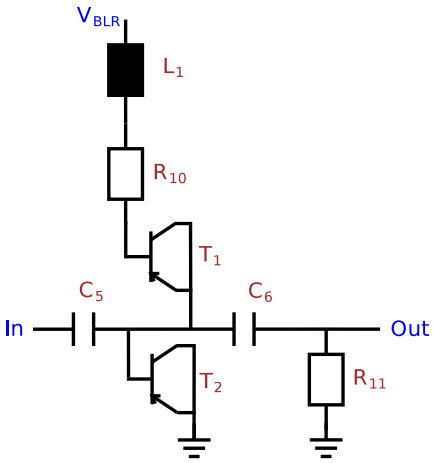
The reason for using a transistor[14] as diode is caused by its low capacity in comparison to commonly used diodes. Its characteristic line is shown in Fig. 5.13b. Together with C_5 the transistor capacity acts as voltage divider and together with the diode as RC-circuit, so the transistor capacity should be small and C_5 should be large. On the other hand, C_5 affects the timing behaviour of the transistor and should be as small as possible[15].

Due to the interaction of all parts, the non-linear behaviour of the diode and, hence, the shaping behaviour of the BLR stage, the parameter selection is a trade-off and the optimal values according to simulation and tests are shown in Tab. A.2.

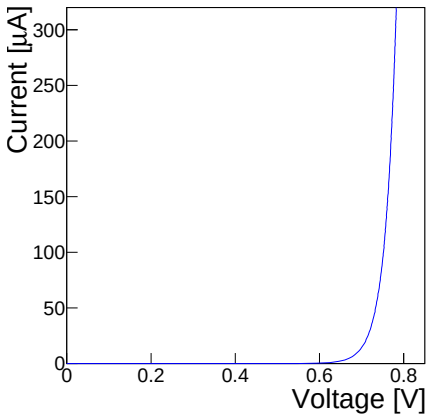
The voltage at V_{BLR} defines the current over T_1 and T_2 and sets, consequently, the working point. The operating principle is shown in Fig. 5.13c, the three different operating states are

- **Baseline input:** Due to the current flowing over R_{10} the diode is slightly conducting, so the potential between the diodes is stable, causing the baseline at Out.
- **Positive input:** The positive input voltages compensates the current over R_{10} and shifts the diode into the non-conducting mode. If the BLR-current is small with respect to the signal current over C_5, the signal at Out is the same as at In.
- **Negative input:** The negative input voltage shifts the diode into the full conducting mode, causing a short-circuit of the signal to ground and, therefore, restoring the baseline.

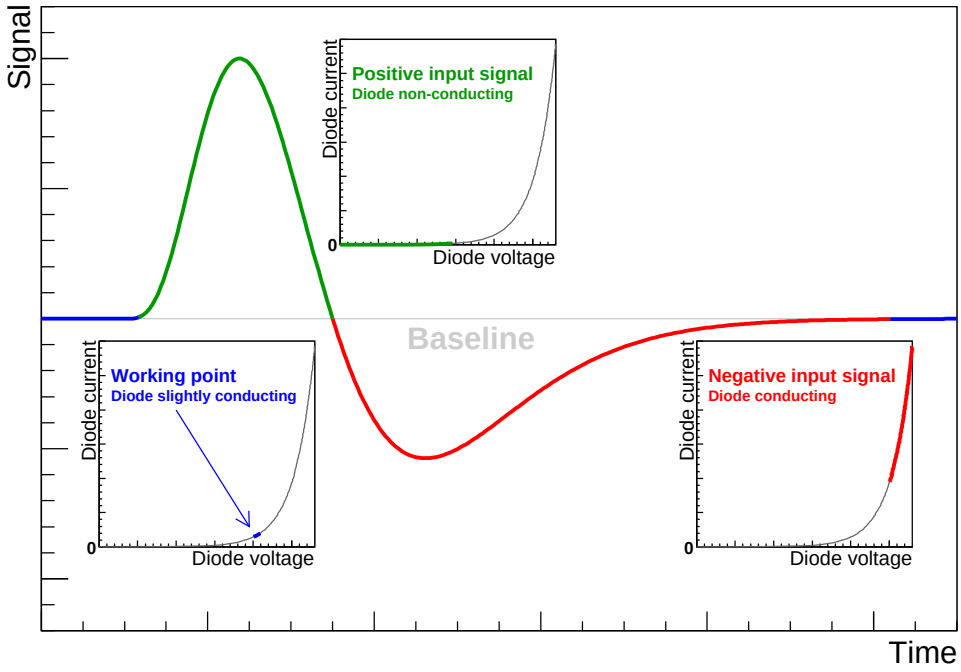
[14] The used transistor (PNP) is a BFT92, see [51].
[15] For details on the timing behaviour of semi-conductors see [52].



(a)



(b)



(c)

Figure 5.13.: (a) Schematic of baseline restoration stage, see Fig. 5.7a. The circuit is based on the passive BLR concept, where a transistor is used as diode due to its low capacity. The working point is defined by the voltage at V_{BLR}, R_{10} and L_1, which together act as current source.
(b) Characteristic line of BFT92 used as diode (wiring corresponding to (a)).
(c) Operating principle of the baseline-restorer shown in (a). On the working point (baseline input), the diode is slightly conducting, for positive input signals it become non-conducting and negative signals are drained to ground.

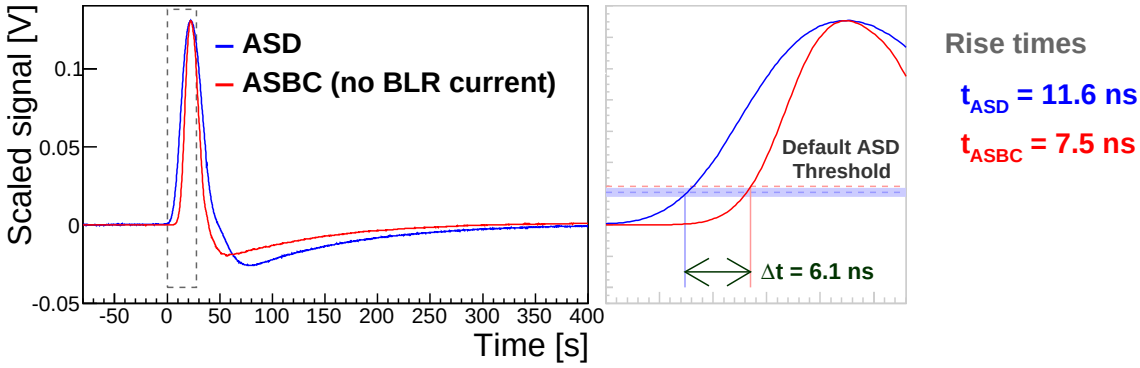


Figure 5.14.: δ-response of ASD and ASBC (scaled to fit the amplitude of the ASD response). The δ-signal was obtained by shaping a square pulse of 800 mV amplitude with 1.2 pF capacity. The right plot indicates the difference of the rise times for an ASD threshold of 38 mV.

If the working point is too low, the diode does not shift into conducting mode, if, however, it is too high, the diode never becomes non-conducting. So the working point has to be chosen with care, and the behaviour of the ASBC depending of V_{BLR} has to be measured.

In this thesis, the following definitions are used:

- *ASBC without BLR:* The diode current is zero.
- *ASBC with BLR:* The diode is operated at the working point.

5.3.2. Comparison of ASD and ASBC δ-Response

In Fig. 5.14 the δ-response of ASD and ASBC without BLR measured in front of the discriminator is shown. The input pulse is obtained from an AC-coupled (1.2 pF) square signal.

There are two major differences between ASD and ASBC

- The rise time[16] of the ASBC is smaller.
- The bipolar undershoot is smaller and faster.

The smaller rise time which is caused by higher bandwidth of the ASBC electronics PreAmp (the ASD chip Preamp and *DA 1* are part of the signal shaper, see Section 5.2) is expected to have a positive impact on resolution and efficiency, because the faster rising edge minimises the time-slewing effect. Likewise, the signal pile-up effect for high counting rates is expected to be suppressed.

In addition, further pile-up suppression by the smaller bipolar undershoot is expected.

[16]Time between 10% and 90% of the signal amplitude.

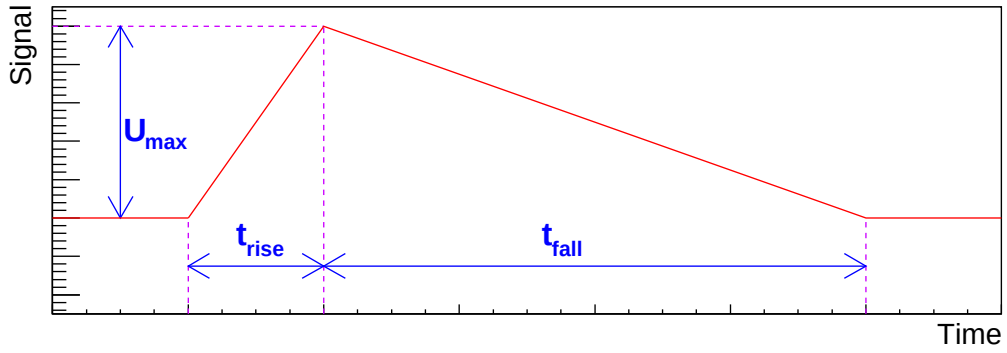


Figure 5.15.: Parametrisation of input pulse with rise time (t_{rise}), fall time (t_{fall}) and amplitude (U_{max}). Due to AC-coupling of the shaping circuit, the absolute level of the baseline does not matter and the difference between baseline and peak is the relevant parameter.

5.3.3. ASBC Response for a Parametrised Pulse

The first approach to evaluate the behaviour of baseline restoration implementation is the ASBC response measured in front of the comparator for a simplified pulse representing the actual muon and background caused pulses.

In Fig. 5.15 the pulse shape, which is a δ-pulse with different rise and fall time, used for the following measurements is shown. The three pulse parameters are the amplitude U_{max}, the rise time t_{rise} and the fall time t_{fall}. Due to AC-coupling of the shaping circuit, the absolute level of the baseline does not matter and the difference between baseline and peak is the relevant parameter.

Due to its high bandwidth with respect to the shaper, the ASBC pre-amplifier has no shaping effect on the signals. Hence, the following measurements were obtained from the ASBC without pre-amplifier.

In Fig. 5.16 the response for different BLR currents is shown. The BLR current has impact on the amplitude as well as on the undershoot. Following the diode characteristic line shown in Fig. 5.13b, the undershoot suppression increases with the BLR working point until a certain current value. The value is the optimal working point. As soon the working point is set in the linear range of the diode, further suppression of the bipolar undershoot with respect to the response amplitude is not possible.

In Fig. 5.17a the amplitude and in Fig. 5.17b the recovery time[17] of the ASBC response depending on the working point for different input pulse amplitudes are shown. These measured functions can be explained with the diode threshold and characteristic line. As soon the working point is above the diode threshold, the BLR impact increases until a certain value. Fig. 5.17b shows that the optimal working point is approximately 90 μA.

[17]Definition: The time after the input signal when the mean of the next 30 ns has the same value as 30 ns of the baseline.

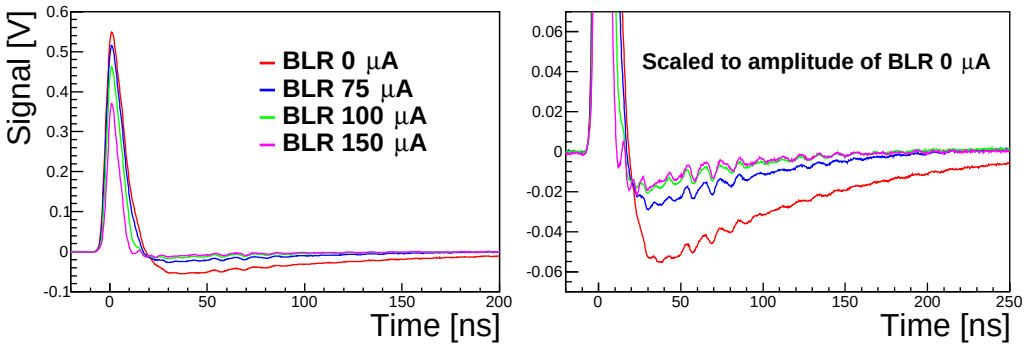


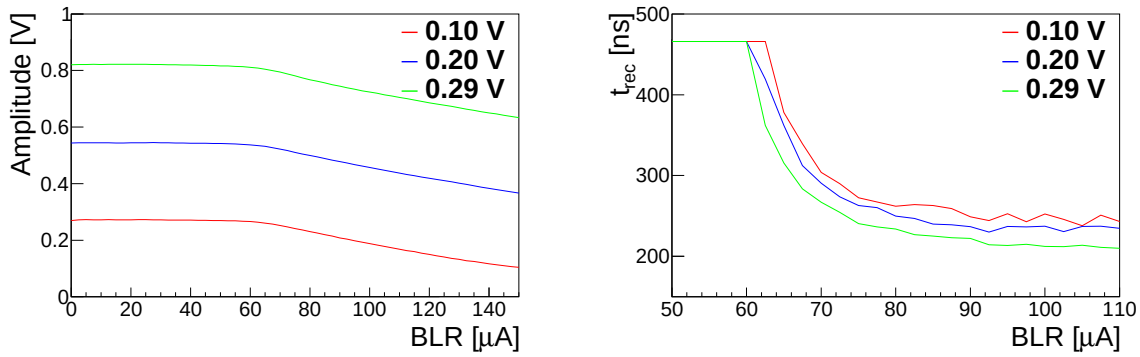
Figure 5.16.: δ-response (5 ns rise time, 5 ns fall time, 0.2 V amplitude) of ASBC (without PreAmp) for different baseline restoration (BLR) currents. Besides a faster baseline recovery, an increasing BLR current causes a reduction of the signal amplitude. Therefore the graphs of the left plots are scaled to the same amplitude. The signal fluctuations of the undershoot are caused by reflections on the signals lines.

The ratio of the areas below the δ-response undershoot and overshoot is expected to be one for bipolar shaping (assuming infinite bandwidth, see Appendix A.2.1). Fig. 5.18 shows this ratio for the ASBC depending on the BLR current. Without baseline restoration the ratio is smaller than one, due to the bandwidth of filter stage 2 (see Section 5.3.1.2). With increasing BLR current, the ratio stays constant until the diode threshold and then decreases very fast until it saturates slightly above zero.

Due to the additional shaping behaviour of the dynamic diode capacity (see Section 5.3.4), it is expected to obtain an additional overshoot after the bipolar undershoot. This overshoot occurs for slowly decreasing pulses, it is shown in Fig. 5.19. In order to avoid additional comparator threshold crossings caused by noise increasing the signal height of the undershoot, it has to be as low as possible.

In Fig. 5.20a the amplitude of this second overshoot and in Fig. 5.20b its time of occurrence with respect to the input pulse depending on the working point is shown. The second overshoot shows a maximum for working points in vicinity of the diode threshold, then it decreases with increasing working point. For the 90 μA working point, the amplitude of the overshoot is smaller than in case of no BLR current.

The functions of Fig. 5.20b[18] shows a similar shape as the recovery time of Fig. 5.17b. At the 90 μA working point, the overshoot time is approximately halved.



(a) (b)

Figure 5.17.: Amplitude (a) and recovery time (b) of the ASBC (without PreAmp) δ-response depending on the BLR current for different input amplitudes (5 ns rise time, 5 ns fall time, see text.

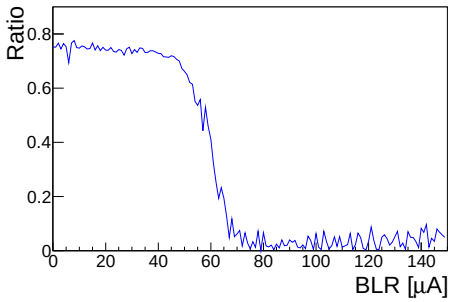


Figure 5.18.: Ratio of the areas below successive undershoot and first overshoot of the δ-response (5 ns rise time, 5 ns fall time, 0.05 V amplitude) depending on the BLR current for the ASBC (without PreAmp).

5.3.4. Response Simulation

The pulse shaping of the ASBC (without the PreAmp[19]) for arbitrary input pulses can be described with a two-tiered simulation, where the result of the first simulation is used as feed for the second one.

- **Tier 1**
  Using scattering parameters, Tier 1 simulates the linear parts of the shaper (filter stages 1 and 2). The impact of the PCB is included because the scattering parameters are measured[20]. The magnitude and phase of the forward transmission coefficient are shown in Fig. 5.21.

[18]Noise and reflections on the signals have a strong impact on the time measurements.
[19]The PreAmp can be approximated by multiplying the input current signal with a factor of 10000.
[20]Due to its layer structure, the PCB acts as capacitor.

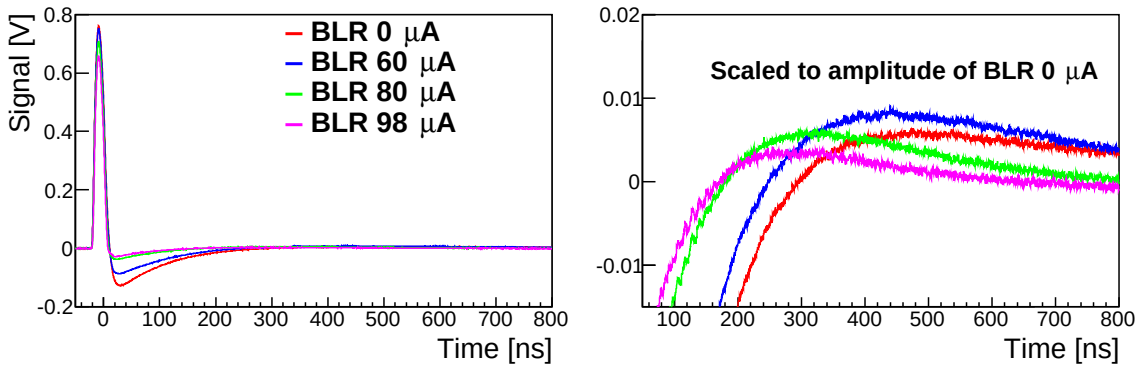


Figure 5.19.: ASBC (without PreAmp) δ-response (5 ns rise time, 20 ns fall time, 0.1 V amplitude) for different BLR currents. The right plot illustrates the impact of the BLR current on the second overshoot.

The Fourier transformed response $\tilde{X}(\mu)$ of the shaping stages can be determined using the relation

$$\tilde{X}(\mu) = X(\mu) \cdot s(f) \ , \tag{5.5}$$

where $X(\mu)$ is the Fourier transform of the input pulse, $s(f)$ is the forward transmission coefficient (complex scattering parameter S_{21}) for the frequency corresponding to the integer index μ[21]. $X(\mu)$ can be described by the discrete Fourier transform[22]

$$X(\mu) = \frac{1}{N} \sum_{n=0}^{N-1} x(n) e^{-\frac{2i\pi\mu n}{N}} \tag{5.6}$$

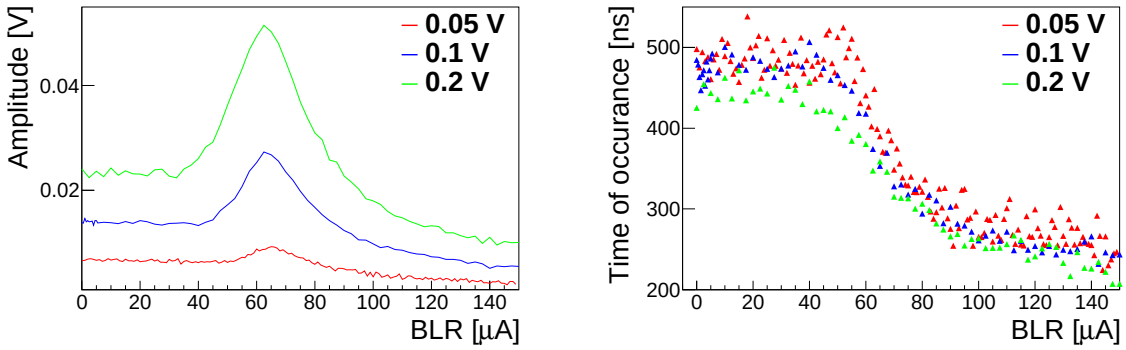
with the inversion

$$x(n) = \sum_{\mu=0}^{N-1} X(\mu) e^{\frac{2i\pi\mu n}{N}} \ , \tag{5.7}$$

where N is the total number of data points and the integer index n in time domain.

The following simulation results are obtained using the discrete Fourier transform library FFTW3 [54].

- **Tier 2**
  Based on the SPICE library *ngspice* (see [55]) the BLR stage is simulated. This simulation includes non-linear effects, because SPICE is based on solving differential equations. In order to describe the diode behaviour of BFR92A[23], a diode model had to be established.



(a) (b)

Figure 5.20.: Amplitude (a) and time (b) of the late overshoot of ASBC shaped δ-pulses (without PreAmp) depending of the BLR current for different input signal amplitudes (in Volt).

5.3.4.1. The Diode Model

The schematic of the SPICE diode model [56] is shown in in Fig. 5.22a. Here the behaviour of the diode is described with additional serial ($GMIN$) and parallel (RS) resistors and a parallel capacitance (C). The static diode forward[24] voltage and current (so-called DC large-signal model) can be calculated iteratively with

$$V = V_D + I_D \cdot RS \tag{5.8a}$$

$$I_D = I_S \cdot \left(e^{\frac{V_D}{N \cdot V_t}} - 1 \right) + V_D \cdot GMIN \ , \tag{5.8b}$$

where V is the voltage on the circuit, V_D the voltage on the diode, I_D the current on the diode, I_S the diode saturation current, N the ideality factor of the diode and $V_T = 25\ mV$ the thermal voltage.

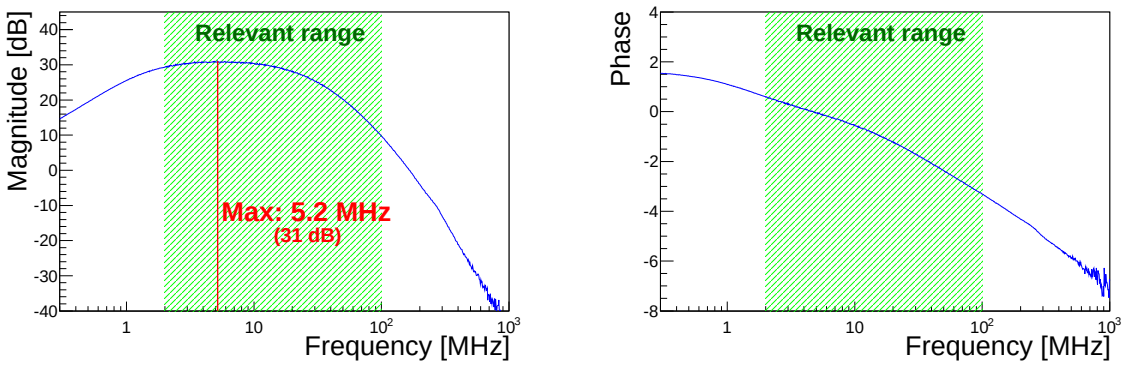
The so-called AC small-signal model approximates the dynamic diode forward behaviour with an parallel capacitance, which includes junction and diffusion effects.

The parameters of the diode SPICE model (see Section A.2.7) are obtained using the minimisation with MINUIT2 [57] of the results obtained with measurement and simulation of

- the static diode model,
- Tier 1 and Tier 2, where the values of the static model are used as basis.

The fit of the characteristic line of the diode (the parallel resistance $GMIN$ is fixed at the default value of $10^{12}\ \Omega$) is shown in Fig. 5.23. The diode shows nearly ideal behaviour

[21] Index of the discrete data table.
[22] Definition according to [53].
[23] NXP does not provide any simulation model for BFR92A used as diode.
[24] Forward refers to the diode conducting polarity.



(a) (b)

Figure 5.21.: (a) Magnitude and (b) phase of the measured forward transmission coefficient of ASBC filter stage 1 and 2.

(ideality factor[25] $N \approx 1$) and its saturation current of $2.93 \cdot 10^{-17}$ A is small with respect to standard diodes[26]. Due to the basis resistance of the transistor, the serial resistor RS=17.2 Ω is huge.

In Fig. 5.24 the results of the full simulation (Tier 0 and 1) based on the SPICE model fit for δ-responses with different working points is shown. Measured data and fit show a minor discrepancy which may be caused by the SPICE model approximations and parasitic effects of the baseline restorer PCB area. Furthermore, the fit converges for a probe[27] inductance of 30 nH and a probe capacitance of 3.8 pF (see Fig. 5.22b). These values correspond to the expectation [58].

Overall, the simulation describes the BLR behaviour well which proves that the transistor circuit discussed above can be used as a diode.

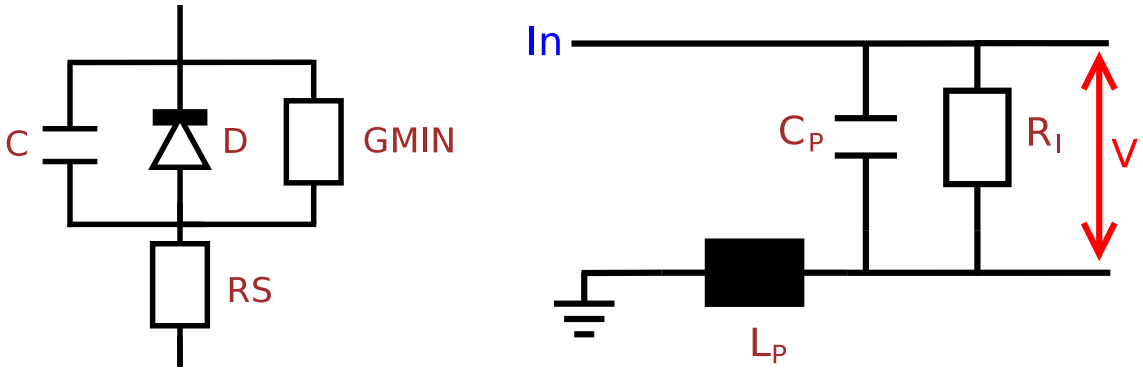
5.3.5. Threshold Determination

Due to the signal suppression caused by the BLR stage, the comparator threshold with and without baseline restoration differs. In order to obtain the values corresponding to the ASD default value of -39 mV (see [22]), two different methods were used.

5.3.5.1. ASBC Without Baseline Restoration

The ASD and ASBC discriminator levels in response to a δ-pulse have been compared. The δ-signal was obtained by shaping a square pulse with an 1.2 pF capacitor.

[25] The ideality factor of a diode is a measure of how closely the diode follows the ideal diode equation.
[26] 1N4148: IS = $3.5 \cdot 10^{-11}$ A, N = 1.24, RS = 0.064 Ω
[27] Inner resistance according to datasheet: 1 MΩ.



(a) (b)

Figure 5.22.: (a) Schematic of the SPICE diode model. The static behaviour of the diode is approximate with a serial and parallel resistor, the dynamic behaviour with a parallel capacitance, respectively.
(b) Description of the measurement probe. The ground connection is approximated with an inductance, the conductance of the probe and the inner resistance are included.

Square pulse amplitude	*ASD threshold*	*ASBC threshold (no BLR current)*
36 mV	-39 mV	191 mV

5.3.5.2. ASBC With Baseline Restoration

Due to the switching time of the diode, the shaping differs for very small (level of the threshold) and big signals (level of actual muon responses). Therefore, the default threshold was determined by comparing the measured hit rate (see Section 5.4.2.5) of a radiated sMDT tube read out with the ASBC with and without baseline restoration.

In Fig. 5.25 this measurement is shown, leading to a threshold of 116 mV.

5.3.6. Noise Considerations

The voltage noise N_{tot} of a system consisting of l amplifiers can be described with its root mean square and, therefore, can be calculated by summing up the squares of the single noise sources and taking into account the gain of the amplifiers:

$$N_{tot} = \sqrt{\sum_{i=0}^{l} \left(U_i^2 \prod_{j=i+1}^{l} g_j \right)} \,, \tag{5.9}$$

where U_0 is the input noise and U_i the noise of the i^{th} amplifier with gain g_i.

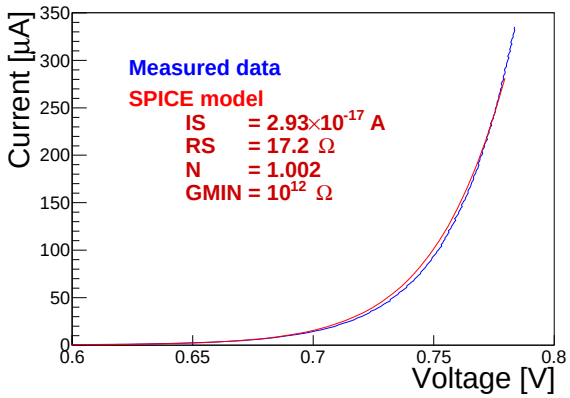


Figure 5.23.: Fit of the characteristic line of BFT92 used as diode (*GMIN* is set to default value). Besides its huge serial resistor *RS* (basis resistance of the transistor), the diode shows an nearly ideal behaviour (ideality factor $N \approx 1$).

For the ASBC the voltage noise N_{tot} results into

$$N_{tot} = \sqrt{N_0^2 \cdot g_{all}^2 + N_{TI}^2 \cdot g_1^2 + N_1^2 \cdot g_2^2 + N_2^2 \cdot g_{BLR}^2 + N_{BLR}^2} \tag{5.10}$$

where N_0 is the input noise (sMDT tube), N_{TI} the transimpedance amplifier noise, N_i the noise of shaper stage i and N_{BLR} the noise of the BLR stage. Furthermore, g_{all} is the gain of all stages, g_1 the gain for all stages after the transimpedance amplifier, g_2 the gain of the second filter and BLR stage and g_{BLR} the gain of the BLR stage.

The BLR stage is expected to have negative impact on the noise level ($g_{BLR} < 1$), so in the following calculation g_{BLR} is used as variable.

The calculation of N_{tot}[28] is based on the following assumptions:

- Noise is caused by resistors, amplifiers and diodes. The square U_t^2 of the thermal noise of a resistor is described by

  $$U_t^2 = 4Rk_BT\Delta\nu \ , \tag{5.11}$$

  where R is the resistance, k_B the Boltzmann constant, T the temperature and $\Delta\nu$ the frequency interval.
  The square I_n^2 of the shot noise current of a diode is described by

  $$I_n^2 = 2qI_0\Delta\nu \ , \tag{5.12}$$

  where q is the elementary charge and I_0 the current flowing through the diode.
- Capacitors do not have any parasitic resistance and, therefore, do not cause noise.
- Due to total ASBC gain, the relevant noise frequency range is between 1.4 MHz and 19.8 MHz (3 dB bandwidth with respect to the maximum gain).

[28] For details on noise level determination, see [59–61].

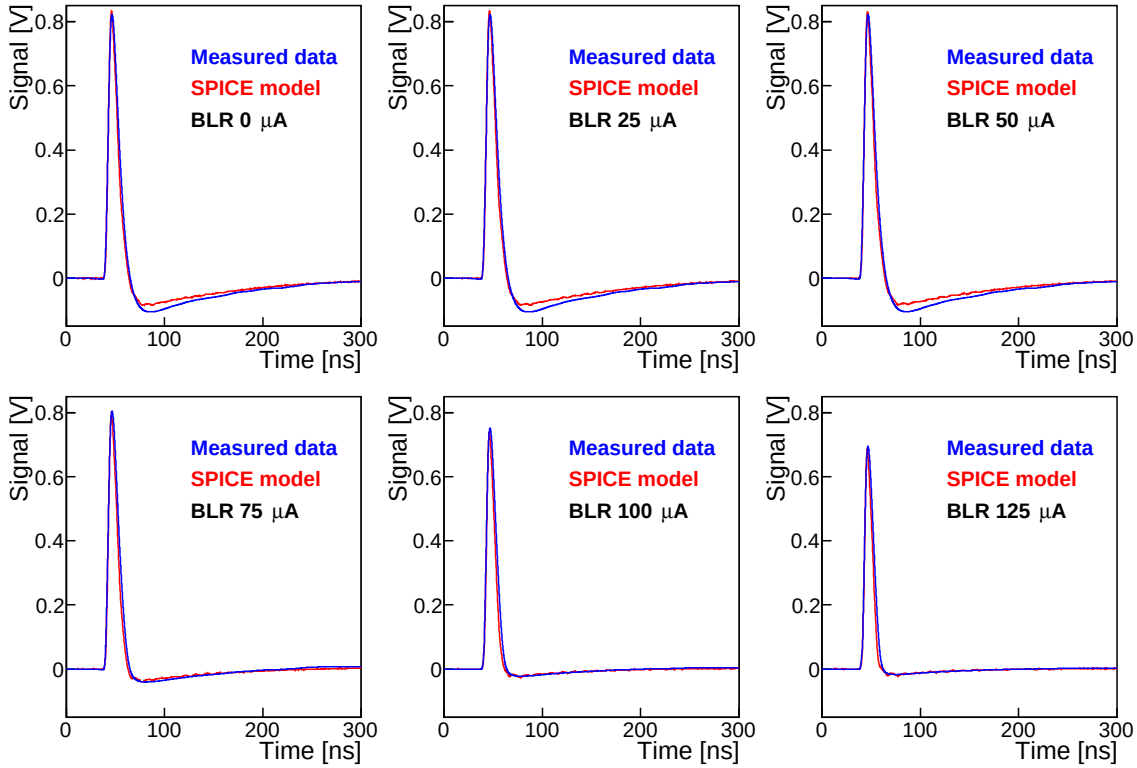


Figure 5.24.: Comparison of the ASBC electronics δ-response with the simulation for 6 different diode working points. The δ-pulse had 2 ns rise time, 2 ns fall time and 80 mV amplitude.

- The circuit is operated at a temperature of 290 K.
- g_{BLR} does not dependent on the working point of the baseline restorer which is fixed with $I_{BLR} = 90$ μA.
- The gain of filter stage 1 and 2 is fixed at their highest value.

Typically, the input RMS current noise of the transimpedance amplifier[29] is 174 nA over its 700 MHz bandwidth, leading to an output noise signal for the relevant frequency range of

$$N_{ti} = 49.7\ [\mu V]\ . \tag{5.13}$$

In Fig. 5.26a the equivalent circuit for noise determination of both filter stages and in Fig. 5.26b of the BLR stage is shown. These circuits include the impact of thermal noise of the resistors (U_1, U_3, I_1, I_3), the noise of the operational amplifiers[30] (U_2 and I_2) and the thermal and Schottky-Noise of the transistors used as diodes (I_{T1} and I_{T2}).

[29] Transimpedance R_{TI}=10 kΩ. (see [48])
[30] For details see [50].

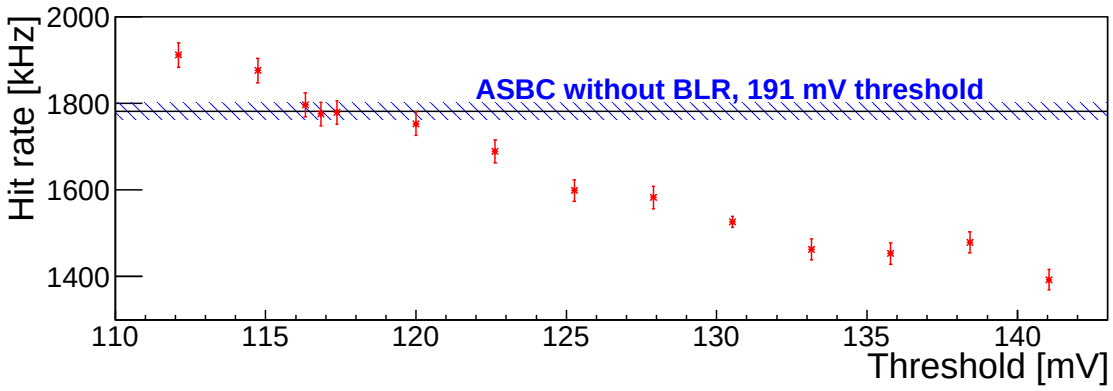
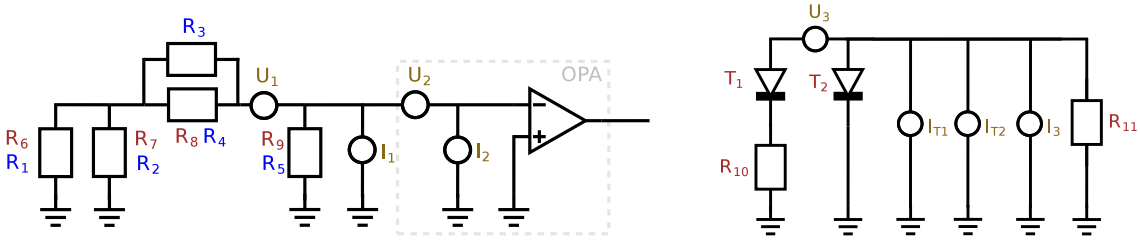


Figure 5.25.: Measured hit rate of a radiated sMDT tube for different threshold voltages of the ASBC with (red) and without baseline restoration.



(a) (b)

Figure 5.26.: Equivalent circuit for noise determination of (a) filter stage 1 (blue labels) and 2 (red labels) and (b) BLR stage. U_1, U_2, U_3 and U_4 are voltage noise sources, I_1, I_2, I_{T1} and I_{T2} are current noise sources.

The voltage noise of filter stage 1 (N_1) sums up to

$$N_1 = \sqrt{(I_1^2 + I_2^2) \cdot (R_1 \| R_2 + R_3 \| R_4) + U_1^2 + U_2^2} = 2.0 \; [nV] \; , \tag{5.14}$$

and of stage 2 (N_2) to

$$N_2 = \sqrt{(I_1^2 + I_2^2) \cdot (R_6 \| R_7 + R_8) + U_1^2 + U_2^2} = 75 \; [pV] \; . \tag{5.15}$$

For the voltage noise of the BLR stage N_{BLR}, it follows

$$N_{BLR} = \sqrt{(I_3^2 + I_{T1}^2 + I_{T2}^2) \cdot (R_{11} \| R_{T2} \| (R_{T2} + R_{10})) + U_3^2} = 76.8 \; [\mu V] \; . \tag{5.16}$$

Under the assumption that the noise of an sMDT tube is caused by its termination resistor of 383 Ω (see Fig. 4.3) and using Eq. 5.10, the total ASBC voltage noise is

$$N_{tot} = 11 \cdot g_{BLR} + 0.076 \; [mV] \; . \tag{5.17}$$

Further assuming a signal threshold of $n_e = 23.7$ primary electrons (see [22]) and a signal length of $t_0 = 200$ ns, the input current (I_0) is

$$I_0 = \frac{n_e \cdot q \cdot g_{gas}}{t_0} = 0.4\ [\mu A]\ , \tag{5.18}$$

where q is the elementary charge and g_{gas} the gas gain. Due to $g_{BLR} > 0.5$ (see Fig. 5.17a), the the signal-to noise ratio R_{ASBC} for the threshold is

$$R_{ASBC} = \frac{I_0 \cdot g_{all}}{N_{ASBC}} = \frac{144 \cdot g_{BLR}}{11 \cdot g_{BLR} + 0.076} \approx 13\ . \tag{5.19}$$

Taking into account a safety-factor of 2, the threshold is still outside the 5σ region of the noise.

5.3.7. Muon, Electron and γ Analog Response

Due to the discrete circuits of the ASBC board, muon, electron (^{90}Sr) and γ (^{137}Cs) signals could be recorded at the same time before and after the shaping circuits. In Fig. 5.27 typical muon, electron and gamma signals from sMDT tubes after the first amplifier stage and after shaping with and without baseline restoration are shown. Without baseline restoration, the bipolar shaped signals have an succeeding undershoot extending about as long as the trailing edge of the unshaped signal. The BLR circuit of the ASBC suppresses this undershoot as expected[31]. The amplitude is reduced with BLR at the working point of the diode in the BLR circuit chosen for measuring the signals in Fig. 5.27.

The muon signals show structure from the successive arrival of ionisation clusters. The electron pulses show less structure from ionisation clusters, because the ^{90}Sr electrons loose their energy of maximum 0.546 MeV after only a few ionisations. They also have lower amplitudes because of their low energies. Due to their high energy (sharp peak at 0.662 MeV), the gamma cause high pulses which push the ASBC into saturation.

More pulses are shown in Appendix A.2.4.

5.4. Performance of the ASBC Electronics at High Counting Rates

In order to test the performance of the ASBC electronics and to understand the effect of the baseline restoration, an sMDT chamber was irradiated with several ^{90}Sr β^- sources. In the following the experimental set-up and the obtained results of the measurements are discussed.

[31] Due to saturation effects, the amplitude of the first overshoot is reduced leading to $R > 1$, see Fig. 5.27.

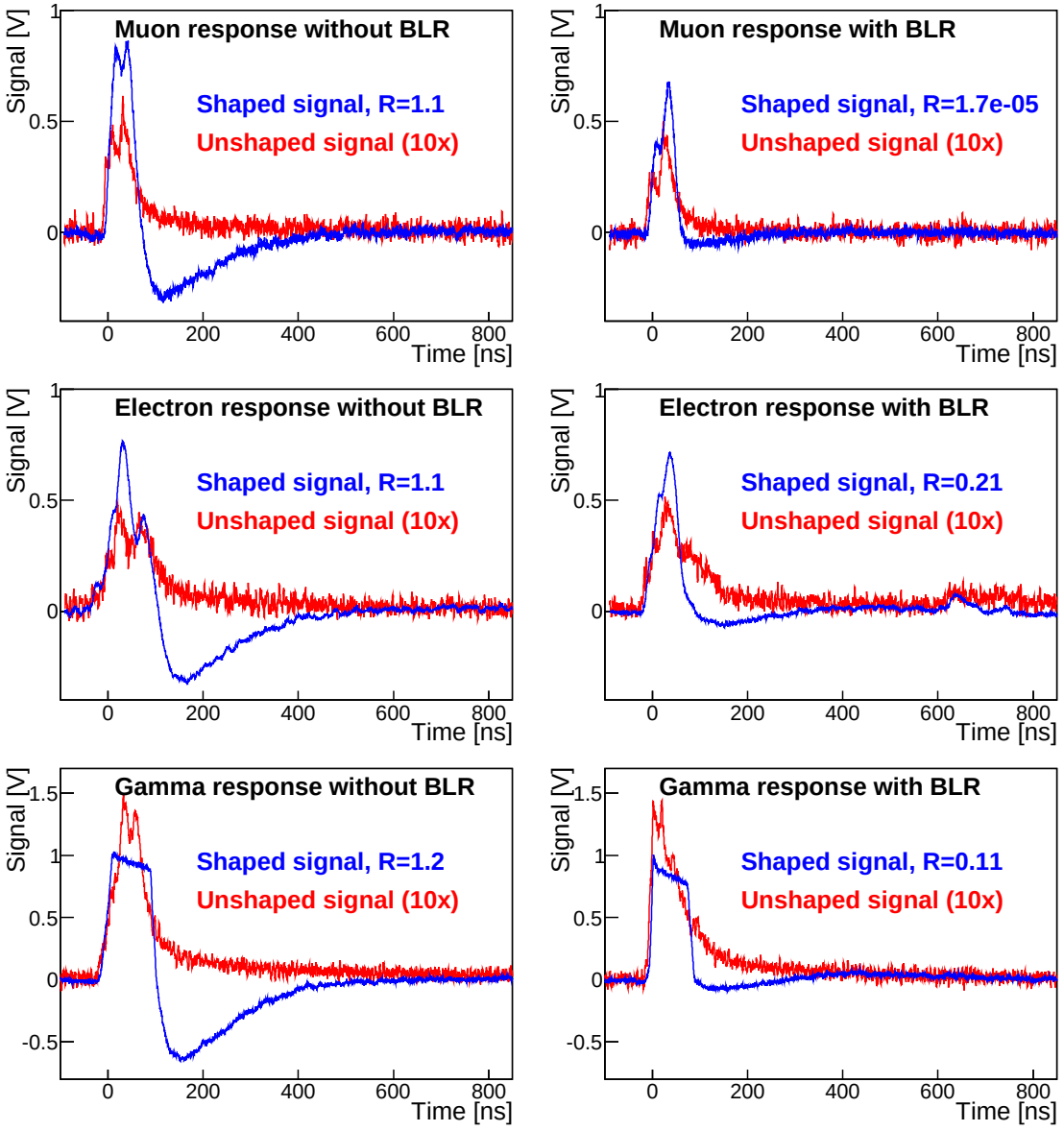


Figure 5.27.: Typical muon, electron (^{90}Sr) and gamma (^{137}Cs) pulse shapes from an sMDT tube after the pre-amplifier (red lines) and after shaping (blue lines) with and without baseline restoration, respectively (Measurement bandwidth: 200 MHz). R indicates the ratio of areas below successive undershoot and first overshoot.

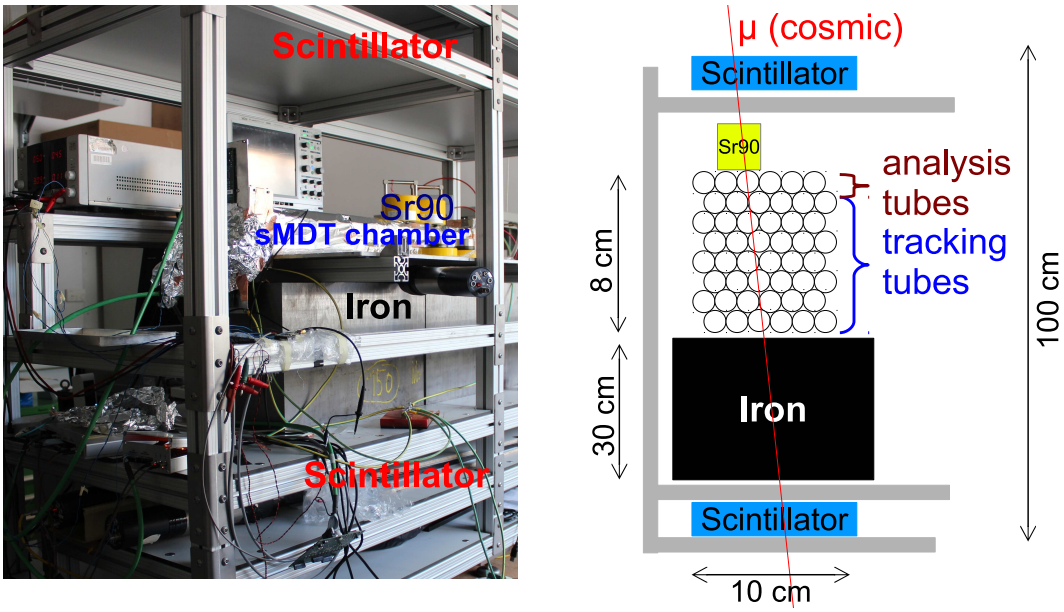


Figure 5.28.: Photograph and schematics of the experimental set-up. While one layer of an sMDT chamber with e^- (^{90}Sr) irradiated was read out with the ASBC electronics and used for performance studies, the other seven layers were used for the reconstruction of the cosmic muon tracks. The scintillation detectors formed the trigger. The iron block hardened the muon momentum spectrum.

5.4.1. Experimental Setup

The experimental set-up is shown schematically in Fig. 5.28. Tracks of cosmic muons were measured with an sMDT chamber, installed between two trigger scintillators. A 30 cm thick iron block underneath the chamber was used for hardening of the muon spectrum.

While one tube in the top layer layer of the sMDT chamber read out with ASBC electronics was locally irradiated with electrons from several ^{90}Sr sources to simulate background, the other seven layers were read out with MDT Mezzanine cards with ASD chips and used for the reconstruction of cosmic muon tracks. A block diagram of the data acquisition is shown Fig. 5.29.

The trigger signal was provided by the logical AND of the two scintillator signals. The scintillators were read-out on both ends in order to obtain position information along the drift-tubes with a few centimetres accuracy.

In order to achieve different e^- hit rates, three different ^{90}Sr-source with 1.5, 12 and 24 MBq were used. While the weaker sources were rod sources with a length of 1 cm and 4 cm, the strong source was a point source with a diameter of approximately 0.5 cm open to the bottom. The rod sources and the positioning on the sMDT chamber is shown in Fig. 5.30. Due to the small size of the ^{90}Sr-source, gain loss due to space charge was only expected for the electron background and not the muon signals (see Section 5.4.2.6).

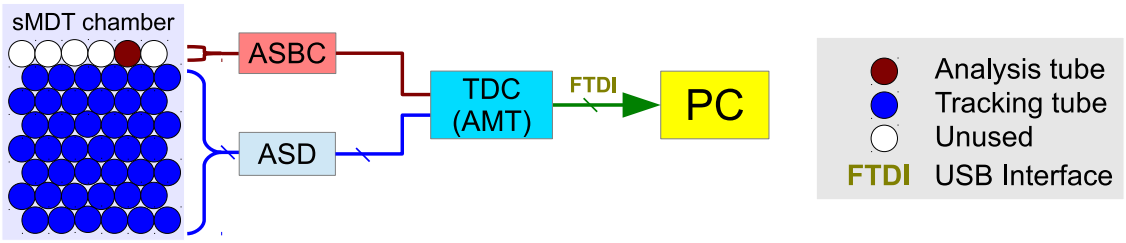


Figure 5.29.: Block diagram of the data acquisition. While the analysis tube was read out with the ASBC electronics, the tracking tubes were read out with ASD chips. The drift-times were measured with the AMT chip [23] and send to the PC for offline analysis.

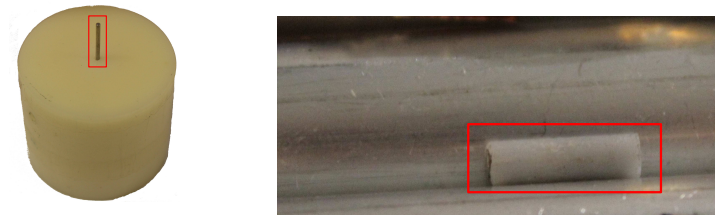


Figure 5.30.: Photograph of the 12 MBq (length ∼4 cm) and 1.5 MBq (length ∼1 cm) ^{90}Sr rod sources used in the experiment. While the left picture show the source stored partially inside its containment, the right picture illustrates the positioning of the source on the sMDT chamber.

5.4.2. Data Analysis

In order to determine and understand the resolution and efficiency of sMDT tubes read out with the ASBC, the following analysis and data correction methods have been applied.

5.4.2.1. Drift-Time Corrections

The drift-radius is determined from the measured drift-time

$$t_{drift} = t_{TDC} + t_0 + t_{Trigger} + t_{slewing} \ . \tag{5.20}$$

with the following

- The time $\boldsymbol{t_{TDC}}$ measured by the TDC (AMT) with respect to the time of the trigger.
- The time offset $\boldsymbol{t_0}$ for the different TDC channels due to different signal path lengths along the wires to the read-out and on the electronics boards is taken into account. It is determined by fitting the leading edge of the drift-time spectrum of each individual drift-tube.

- The time of the trigger $\boldsymbol{t_{Trigger}}$ in the test setup is corrected for the light travel time within the scintillators and for the 25 ns time jitter of the TDC[32].
- Due to the fixed discriminator threshold of the ASD (see Section 4.1.1), the threshold crossing time and, therefore, the TDC time measurement are delayed roughly proportional to the pulse amplitude. This effect is called time slewing and is estimated using the signal charge measurement Q_{ADC} of the Wilkinson ADC on the ASD chip:

$$t_{slewing} = -c(r) \cdot \left(Q_{ADC} - \bar{Q}_{ADC}(t)\right) \tag{5.21}$$

  where $c(r)$ is a correction function depending on the drift-radius r (6th order polynomial), Q_{ADC} the measured ADC value for the hit and $\bar{Q}_{ADC}(t)$ the average ADC value for the measured drift-time corrected for t_0 and $t_{Trigger}$ (see [62]). This correction is not applied to sMDT tubes of the analysis layer, because the ASBC electronics does not provide charge measurement.

The leading edge of the drift-time spectrum is described by a modified Fermi function

$$G(t) = \frac{A_0}{1 + e^{-\frac{t-t_0}{T_0}}} + p_0 \ , \tag{5.22}$$

where A_0 is the maximum of the spectrum, t_0 the turning point of the function, $4 \cdot T$ the rise time of the spectrum from 10% to 90% of the maximum and p_0 a pedestal.

In Fig. 5.31 drift-time spectra of cosmic muon tracks in an sMDT tube measured with the ASD chip and with the ASBC electronics with and without baseline restoration, after time corrections described above, is shown. Due to the shorter signal rise time (see Fig. 5.14), a shorter rise time of the drift-time spectra is observed for the ASBC measurement leading to a better single-tube spatial. The resolution σ_r in vicinity of the wire can be estimated by using the rise time as time resolution $\sigma_t = t_{rise}$ and the relation

$$\sigma = \dot{r}(t) \cdot \sigma_t \ , \tag{5.23}$$

where $r(t)$ is the drift-time to space relation. With a maximal drift-time of 185 ns and a linear drift-time to space relation, it follows

$$\sigma_{ASD} = 248 \ \mu m \tag{5.24a}$$

$$\sigma_{ASBC} = 195 \ \mu m \ . \tag{5.24b}$$

Therefore, the ASBC resolution is 20% lower in vicinity of the wire compared to the ASD.

5.4.2.2. Determination of the Space-to-Drift-Time Relationship

The drift-radius is determined from the measured drift-time using the space-to-drift-time relationship $r(t)$ which needs to be calibrated. A first estimate is obtained by integrating

[32] In ATLAS the AMT chip measures the drift-time with respect to the 40 MHz LHC clock as trigger. Therefore a 25 ns time jitter occurs for the measurement of cosmic muons.

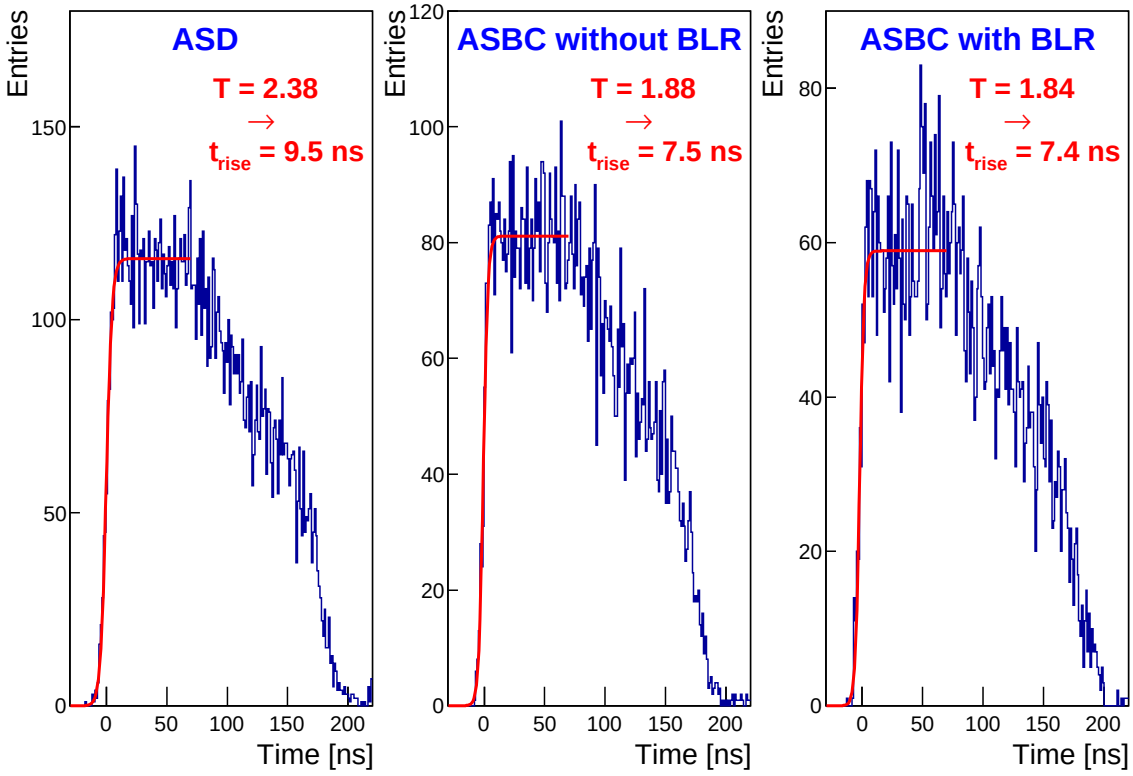


Figure 5.31.: Cosmic muon drift-time spectra of the same sMDT tube measured with the ASD chip (without time slewing corrections) and the ASBC circuit with and without baseline restoration. The leading edge (fitted with a Fermi function; see Eq. 5.22) for the ASBC measurements has a shorter rise time t_{rise}, which leads to an improved drift-tube spatial resolution.

the derivative of the drift-time spectrum,

$$r(t_i) = \int_0^{t_i} \dot{r}(t)dt \ \text{, with } 0 \leq t_i \leq t_{max} \ , \tag{5.25}$$

where t_{max} is the maximum drift-time.

An improved $r(t)$ relationship is obtained by the so-called autocalibration method [63,64] which is based on redundant measurements of muon tracks in several drift-tube layers. The algorithm starts from an initial $r(t)$ relationship, obtained for instance by the integration method, and estimates and improves the $r(t)$ relationship by minimising the track residuals.

The algorithm converges after five to ten iterations. An accuracy of better than 20 μm can be achieved. A typical space-to-drift-time relationship determined with the experimental set-up described above is shown in Fig. 5.32.

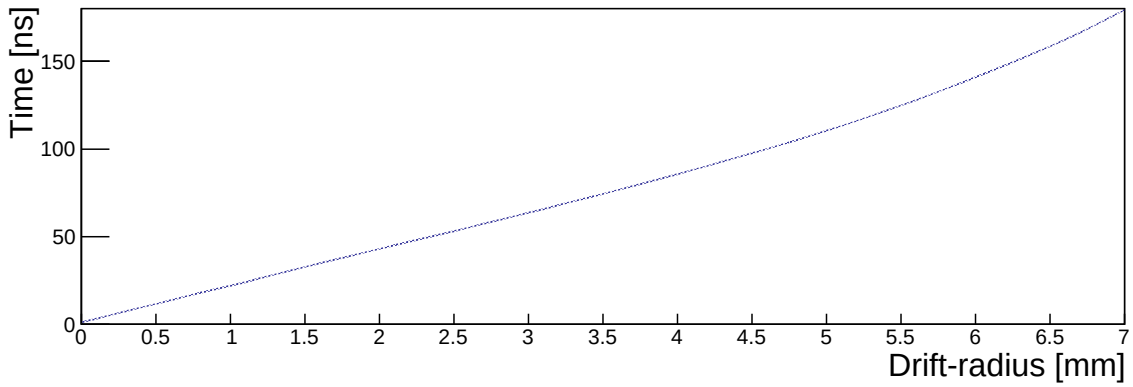


Figure 5.32.: Space-to-Drift-Time relationship of an sMDT tube (20 μm systematic uncertainty, see [64]).

5.4.2.3. Track Reconstruction

The straight track reconstruction (no magnetic field) in drift-tube chambers is a two-step process:

1. **Pattern recognition:**
   All tubes within straight tracks defined by hit tubes of the two top-most layers are selected and clusters of hits are searched for within these tracks. This algorithm resolves the two-fold ambiguity of the drift-radii (left and right of the wire) and results in track points [65].
2. **Track fit:**
   A straight line $y = \alpha_1 + \alpha_2 z$ is fitted to the selected track points (y_i, z_i) in the layers $i = 1, .., n$ by minimising

$$\chi^2 = \sum_i^n \frac{1}{\tilde{\sigma_i}^2} (y_i - \alpha_1 - \alpha_2 z_i)^2 \,, \tag{5.26}$$

   where $\tilde{\sigma_i}(r)$ is the spatial resolution of each hit as a function of the drift-radius (see Fig. 5.33).

5.4.2.4. The Single-Tube Spatial Resolution and Efficiency

The track reconstruction uses the single-tube spatial resolution depending on the drift-radius as input. The latter is determined using an iterative method described in [66] which starts with track reconstruction without the tube under study using an approximate single-tube resolution and compares the drift-radius r_{ana} in the tube to the distance r_{track} between sense wire of the tube and extrapolated track . The variance of the residual

$$\delta := r_{ana} - r_{track} \tag{5.27}$$

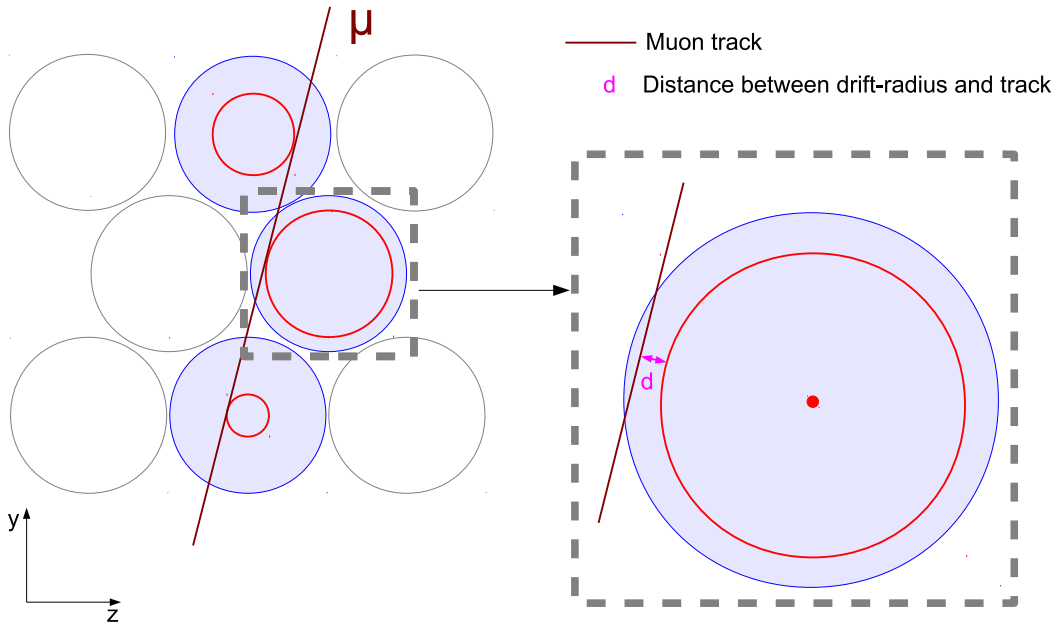


Figure 5.33.: Illustration of the straight track reconstruction (see text).

is the quadratic sum of the drift-tube spatial resolution $\tilde{\sigma}(r_{ana})$ for the measured drift-radius and the uncertainty σ_{track} in the track distance r_{track}:

$$Var\,(\delta) = \tilde{\sigma}^2\,(r_{ana}) + \sigma^2_{track}\,(r_{track}) \quad . \tag{5.28}$$

With σ_{track} determined from the track fit (see [65]), $\tilde{\sigma}$ is derived from the width of the residual distribution and used as new single-tube resolution for the next iteration.

This algorithms typically converges after few iterations. The average spatial resolution of the drift-tube is given by

$$\bar{\sigma} = \sqrt{\frac{1}{r_{max}} \int_0^{r_{max}} \tilde{\sigma}^2\,(r)\,dr} \quad , \tag{5.29}$$

where r_{max} is the maximum drift-radius (r_{max} =7.1 mm for sMDT tubes with 400 μm wall thickness).

After determination of the spatial resolution of the sMDT tubes used for track reconstruction, the same method is used for the determination of the single-tube resolution of the tubes within the analysis layer. Because of the rather soft cosmic muon momentum spectrum, the single-tube resolution has to be corrected for multiple scattering which cause a deterioration of 127 μm determined by from subtracting the spatial resolution of the analysis track layer from the spatial resolution of the middle tracking layer.

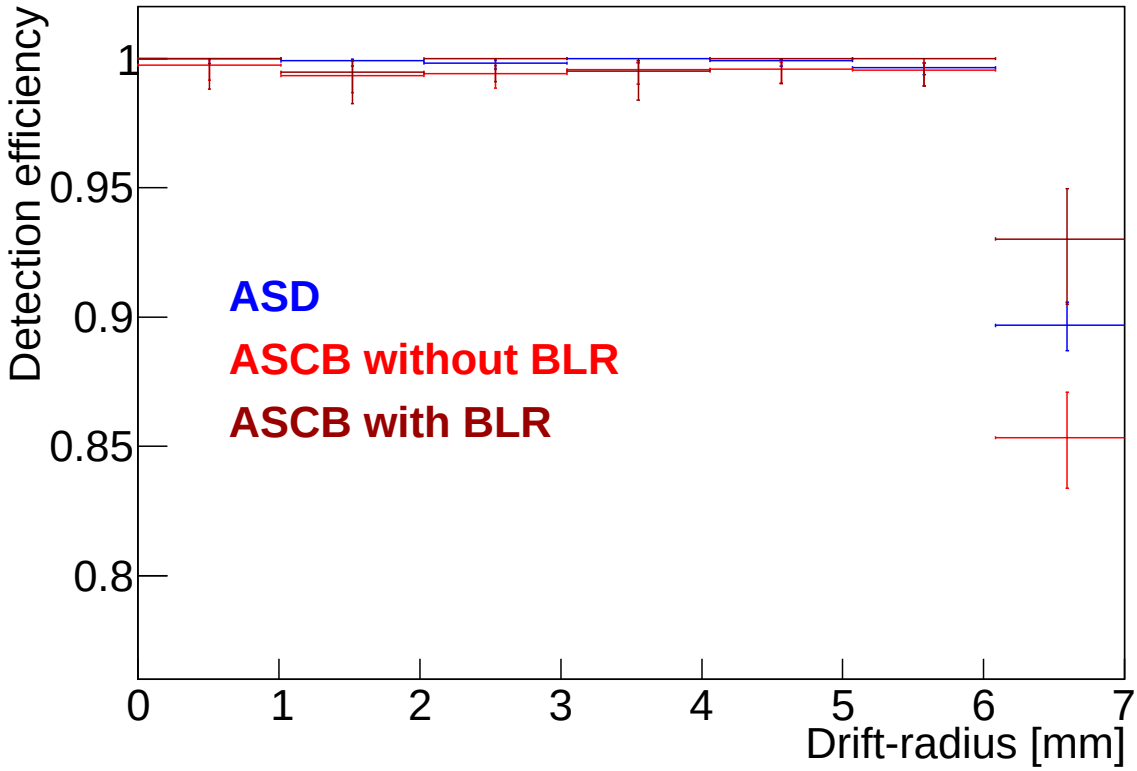


Figure 5.34.: Muon detection efficiency with ASD and ASBC read-out with and without baseline restoration of sMDT tubes. Except for close to the tube wall, the detection efficiency is consistent with 100%.

The detection efficiency ϵ_{det} of a drift-tube is defined by

$$\epsilon_{det} = \frac{n_{reg}}{n_{imp}} \ , \tag{5.30}$$

where n_{reg} and n_{imp} are the numbers of registered and impinging muon tracks, respectively. The detection efficiencies for ASD and the ASBC measurements, the latter with and without baseline restoration, are shown in Fig. 5.34. Except for close to the tube wall, where the muon path length in the tubes becomes shorter, the detection efficiency is consistent with 100%.

Since this quantity does not discriminate between real muon and background hits, including δ-electrons induced by muons, the so-called 3σ muon efficiency is defined which is the probability to measure the drift-radius within a range of 3σ of the reconstructed muon track, where σ is the spatial resolution of the tube. A muon hit is expected with a Gaussian probability of 99.73% within 3σ if the tube is fully efficient and there is no masking of the muon hit by background hits.

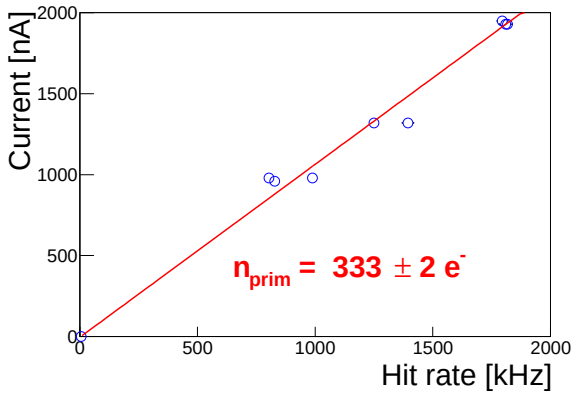


Figure 5.35.: Drift-tube current of an electron irradiated (^{90}Sr) sMDT tube depending on the hit rate. The number of primary electrons n_{prim} is obtained by applying Eq. 5.32 on the measured data.

5.4.2.5. Background Rate Determination

The background rate is determined from the side band in front of the muon drift-time spectrum or from a drift-time spectrum recorded with random trigger in a time intervall T. The observed background counting rate (see Section 4.3.2.1) is given by

$$k = \frac{n_{hit}}{T \cdot n_{trigger}} \ , \tag{5.31}$$

where n_{hit} is the number of detected hits and $n_{trigger}$ the number of triggers.

5.4.2.6. Gain Drop for Electrons

The drift-tube current I_{tube} depends on the hit rate ν:

$$I_{tube} = n_{prim} \cdot q \cdot g \cdot \nu \ , \tag{5.32}$$

where q is the elementary charge, n_{prim} the number of primary electrons caused by a background hit and $g(\nu)$ the gas gain of the drift-tube.

Due to the small size of the ^{90}Sr sources used in the experiment, local space-charge effects leading to a drop of the gas gain were expected to occur for background electrons:

$$g = g(\nu) \ . \tag{5.33}$$

In order to obtain $g(\nu)$, the current I_{tube} as a function of the hit rate has been measured and is shown in Fig. 5.35. Contrary to expectations, $g(\nu)$ is linear and, therefore, the gas gain did not drop under irradiation with the ^{90}Sr sources.

With the nominal sMDT gas gain of 20000 (see Section 4.1), each background hit causes $n_{prim} = 334$ primary electrons.

The number of primary electrons can be estimated using the energy distribution of the ^{90}Sr electrons[33] (see [67]), the drift-tube geometry and the stopping power of aluminium and the drift-gas. The stopping power of a material as a function of the penetrating particle energy is defined as energy loss per distance:

$$S(E) = -\frac{dE}{dx} \tag{5.34}$$

and can be calculated for each material[34] (see [33]).

Considering an energy loss for the electrons due to the tube wall of 400 μm aluminium, and calculating the mean transferred energy to the drift-gas (Ar/CO_2 - 93/7, temperature 290 K, 30 eV ionisation energy) under the assumption of cosinusoidal weighted parallel electron tracks leads to $n_{prim} \approx 170$ primary electrons explaining the measurement results within an order of an magnitude[35].

Compared to ^{137}Cs photon conversions ($n_{prim} = 900$, see Section 4.3.1 and [27]), the number of primary electrons is rather small. Therefore, the electron irradiation can be described as combination of electron and muon pulses without any further effect.

5.4.2.7. Pulse Height and Length

While the ASD discriminator has an ADC and time over threshold mode (see Section 5.2), the ASBC comparator is limited to the time over threshold measurement. In Fig. 5.36a and 5.36b the time over threshold distribution taking into account only the first muon pulse crossing the threshold measured with ASBC electronics without BLR[36] and ASD chip is shown. Due to the ASBC electronics faster shaping, the probability multiple threshold crossings is higher for the ASBC electronics than for the ASD chip (see pulse shapes illustrated in Appendix A.2.4), leading to a lower mean muon time over threshold.

In Fig. 5.36c and 5.36d the muon pulse height non- and irradiated measured with the ASD chip is shown[37]. Due to the pile-up effects, irradiation leads to a reduction of the muon pulse height, but the electron background pulse undershoot amplitudes overlaying with the muon pulses were not high enough to shift the muon signals below the threshold. Otherwise, the pulse height distribution would already start at zero. Due to the similar shaping, the background electron pulse height distribution of the ASBC electronic is expected to correspond to Fig. 5.36c and 5.36d (the ASBC electronics does not contain an ADC).

[33] Due to the long half-life of ^{90}Sr (28.9 a) and the short half-life of its decay product ^{90}Y (64.1 h), ^{90}Y is in secular equilibrium and has to be taken into account for the electron energy spectrum.

[34] Details see `http://physics.nist.gov/PhysRefData/Star/Text/ESTAR.html`

[35] This rough estimation does not included the containment of the ^{90}Sr source, δ-electrons in the tube wall and the distribution of electron tracks due to penetration angle and scattering.

[36] As shown in Section 5.3.3, the BLR only affects the undershoot and, therefore, the pulse length with and without BLR are identical.

[37] Due to electrons masking the muon hits, the irradiated distribution also contains the length of electron pulse (220 μm spatial resolution, 1.8 MHz $\rightarrow$ 3% probability to measure an electron within 3σ of an muon hit).

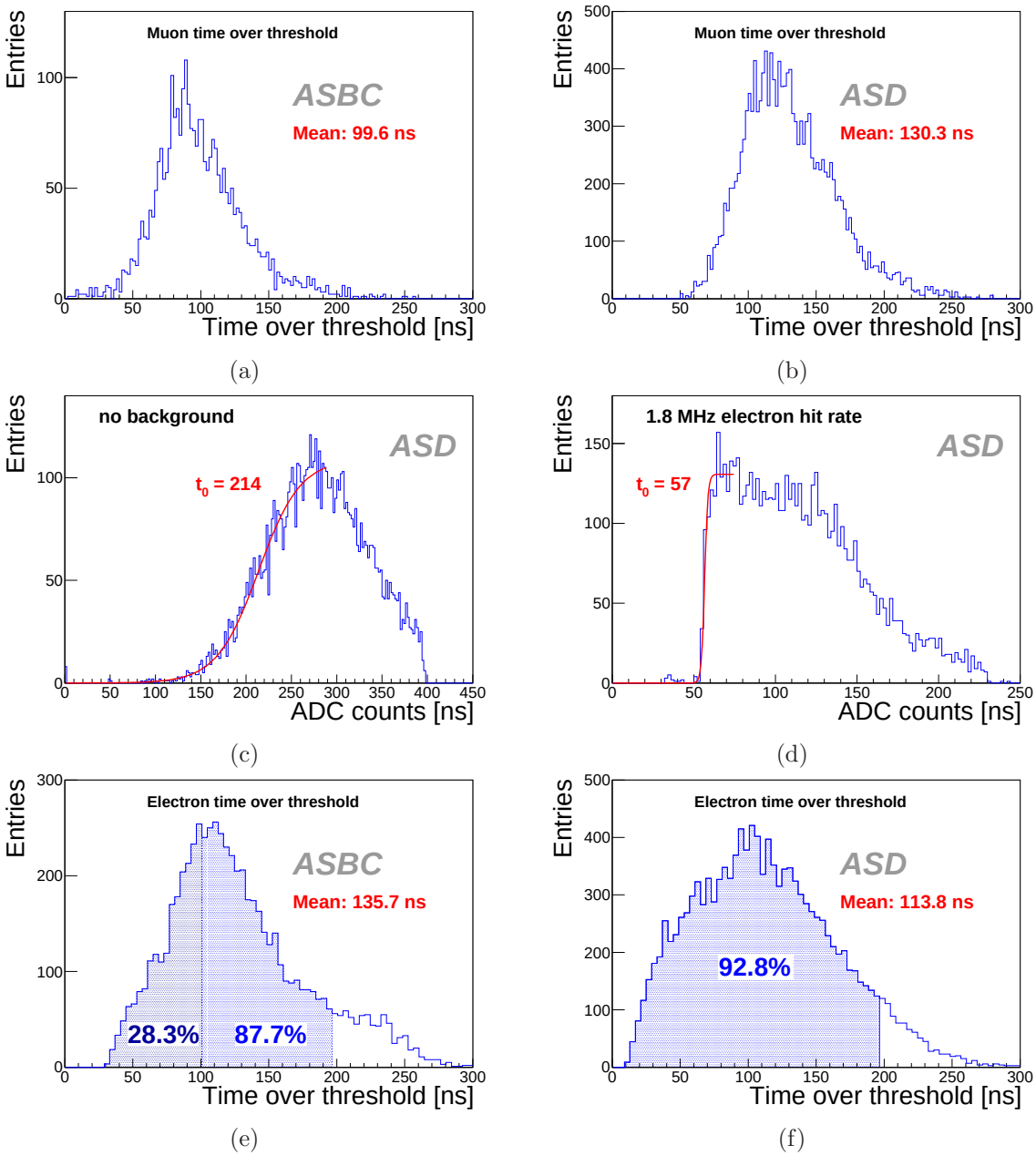


Figure 5.36.: Time-over-threshold distributions of muon pulses from sMDT tubes measured with the (a) ASBC electronics without BLR and the (b) ASD chip, respectively.
Muon pulse-height spectrum measured with the ASD chip (c) non and (d) irradiated. The irradiated spectrum also contains electron pulses which are masking the muon pulses.
Time-over-threshold distributions of ^{90}Sr electron pulses from sMDT tubes measured with the (e) ASBC electronics without BLR and the (f) ASD chip, respectively. The hatched areas indicate the fractions of pulse lengths below 100 and 195 ns.

In Fig. 5.36e and 5.36f the time-over-threshold distribution of background electrons measured with the ASBC electronics in Fig. 5.36e is shown.

5.4.2.8. Programmable and Effective Dead Time

While the effective ASD chip dead time was measured (195 ns, see Section 5.2), the ASBC electronics dead time was taken into account in the offline analysis, because no programmable dead time is implemented in the ASBC (see Section 5.3.1). The maximal length of the programmed offline applied dead time was limited by the length of the side band in front of the muon drift-time spectrum with a length of 210 ns.

When the programmed dead time τ becomes shorter than the background pulse length t, the effective dead time $\tilde{\tau}(t)$ depends on the background pulse time-over-threshold[38]

$$\tilde{\tau}(t) = \tau \cdot \Theta(\tau - t) + t \cdot \Theta(t - \tau) \ . \tag{5.35}$$

The length of only 7 % of the electron pulses measured with ASD read-out (see Fig. 5.36f) and of 12 % of the pulses measured with the ASBC electronics, is below 195 ns and, therefore, the effective and the programmed dead time match approximately.

For lower dead time settings (e.g. 100 ns), the effective dead time depends on the pulse length distribution which has to be considered for the calculation of the 3σ-efficiency $\tilde{\epsilon}(m)$ (see Eq. 4.4 in Section 4.3.2.1)

$$\tilde{\epsilon}(m) = \int_0^\infty \frac{\epsilon_0 \cdot T(t)}{1 + m \cdot \tilde{\tau}(t)} \, dt \ , \tag{5.36}$$

where $T(t)$ is the standardised background pulse time over threshold distribution, m the true hit rate and ϵ_0 the efficiency in the case of negligible hit rate.

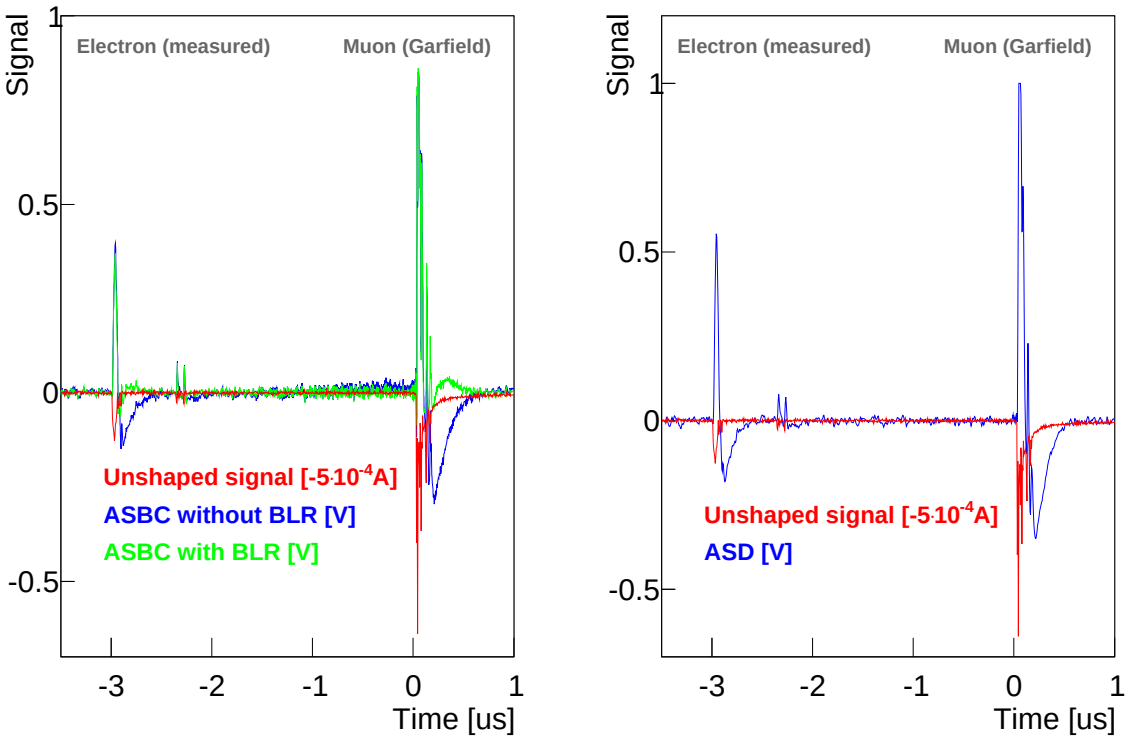
A lower effective dead time leads to an increase of efficiency, but also causes a higher hit rate due to multiple threshold crossings of background and muon hits. In the ATLAS Muon Spectrometer the programmable dead time of the ASD chip is set to the maximum drift-time of MDT tubes in order to suppress spurious hits from the same muon track [9].

5.4.3. Simulation of the Performance of the sMDT Read-Out Electronics

In order to simulate the performance of sMDT tubes read out with ASBC electronics and ASD chip, 700 sMDT muon pulses generated with Garfield [26] with 50 measured ^{90}Sr electron pulses have been statistically combined to give 7000 events each for ASD and ASBC in order to simulate the effect of background hits on the muon track measurement (see Fig. 5.37a).

The impact of δ-electrons is approximated by a time shift of the muon pulse according to the space-to-drift-time parametrisation discussed in Appendix A.1.

[38] $\tau < t$: $\tilde{\tau} = \tau$; $\tau \geq t$: $\tilde{\tau} = t$



(a) (b)

Figure 5.37.: Simulated detector response and signal shaping for muon and background electron hits in sMDT tubes read out with (a) ASBC electronics and (b) ASD chip (see text).

While the shaping of the ASBC was obtained by applying 10 kΩ transimpedance[39] (see Section 5.3) and the simulation discussed in Section 5.3.4, the ASD response was simulated by using its scattering parameters obtained from [47][40]. Amplifier saturation effects were approximated by setting the voltages at saturation to the maximal possible according to the circuit (0.9 V for the ASBC electronics and 1 V for the ASD chip). After applying the discriminator thresholds as used for the measurements (see Section 5.3.5.2), dead time settings were applied and the resolution and 3σ-efficiency determined.

In order to obtain a smooth curve for comparison with measured data and minimise the impact of statistical uncertainty, the resolution as a function of rate and dead time has been approximated to be linear and, therefore, has been fitted (see Appendix A.2.8).

[39] Multiplication of the current pulses with 10 kΩ leading to the output voltage signal of the PreAmp.
[40] The ASD scattering parameter take the current input of the ASD chip into account.

Limitations The ASD chip simulation does not take the non-linearity of the *DA 3* into account, because scattering parameters can not describe non-linear systems[41] (see Section 5.3.4) leading to a slightly different shaping compared to the real chip.

The ASBC electronics simulation does not take into account that operation amplifiers at saturation loose their linearity (for details see [68]). This effect is expected to have very low impact.

5.4.4. Results

5.4.4.1. Spatial Resolution

In Fig. 5.38 and 5.39a the average single tube resolution measured with the ASD chip and ASBC electronics with and without baseline restoration are shown for different dead time settings and compared to the simulation discussed in Section 5.4.3. The ASBC electronics simulation describes the results quite well, but the ASD chip simulation suffers from the limitations discussed above leading to a qualitatively description.

While the results with ASD chip show a degradation due to pile-up of high rates, with ASBC electronics pile-up effects seem to be suppressed. At high counting rates, the pulses of the ASBC electronics also pile up, but due to the faster rise time compared to the ASD chip (see Section 5.3.2), the shift of the threshold crossing times is reduced with respect to the ASD chip. With baseline restoration, the undershoots succeeding to the electron pulses are suppressed leading to slight further improvement of the resolution measured with the ASBC.

In Fig. 5.39b the average single tube resolution for a irradiated sMDT tube measured with the ASBC as a function of the programmed dead time is shown and compared with simulation. While the hatched areas show the uncorrelated statistical error, the error bars indicate the correlated uncertainty between two neighboured points.

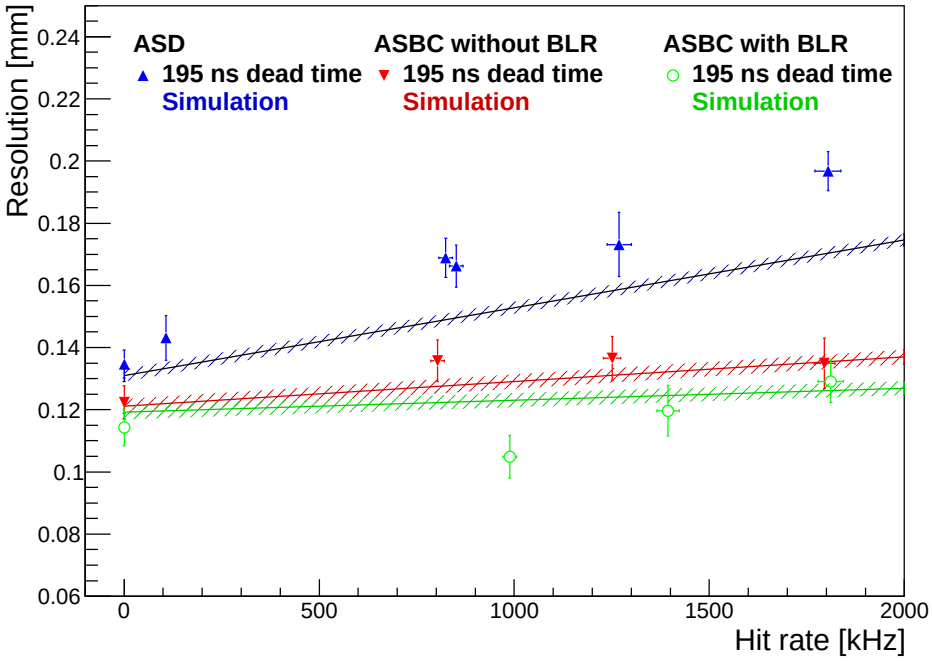
It is expected that in contrary to the ASBC with BLR a reduction of the programmed dead time has impact on the measured resolution. Although, the results indicate so, the simulation does not confirm. Due to the high statistical uncertainty, the expectation can neither confirmed or disproved.

5.4.4.2. 3σ-Muon Detection Efficiency

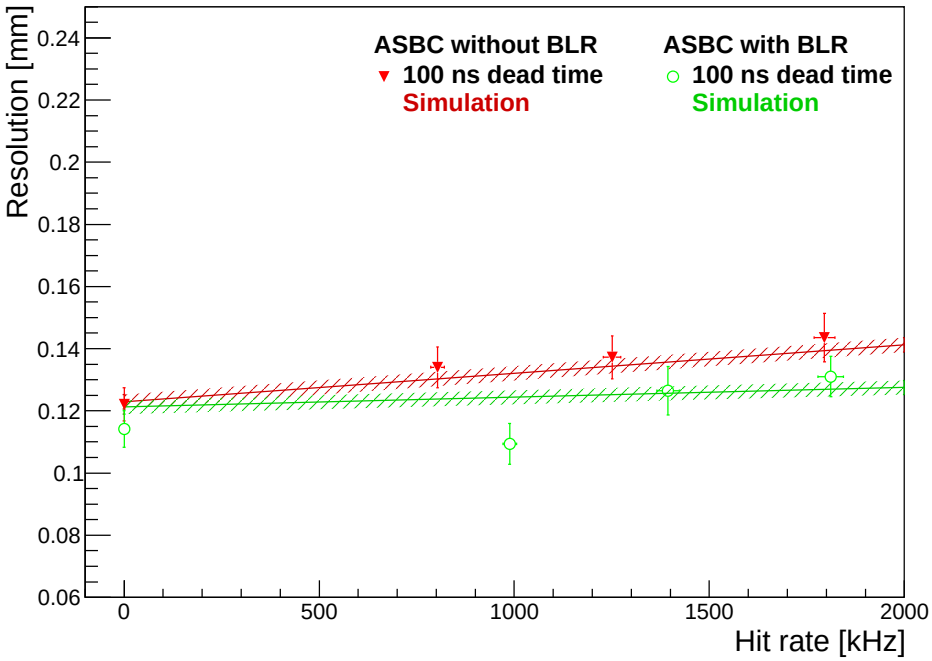
In Fig. 5.40a the 3σ-muon efficiency measured with the ASD chip and ASBC electronics with and without baseline restoration are shown for different dead time settings and compared with the statistical efficiency prediction described in Section 5.4.2.8.

The statistical prediction, which assumes that the undershoot amplitude of the electron pulses is too small to shift the muon pulses below threshold (see Section 5.4.2.7) and takes into account the pulse length distribution of Fig. 5.36e, describes the measured 3σ-efficiency well.

[41] The simulation uses the mean amplification of *DA 3*.

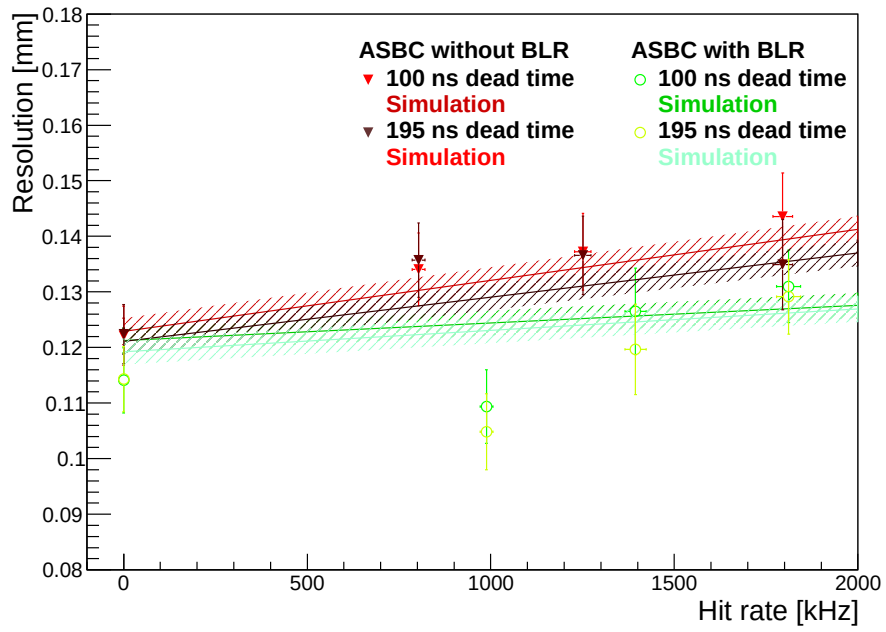


(a)

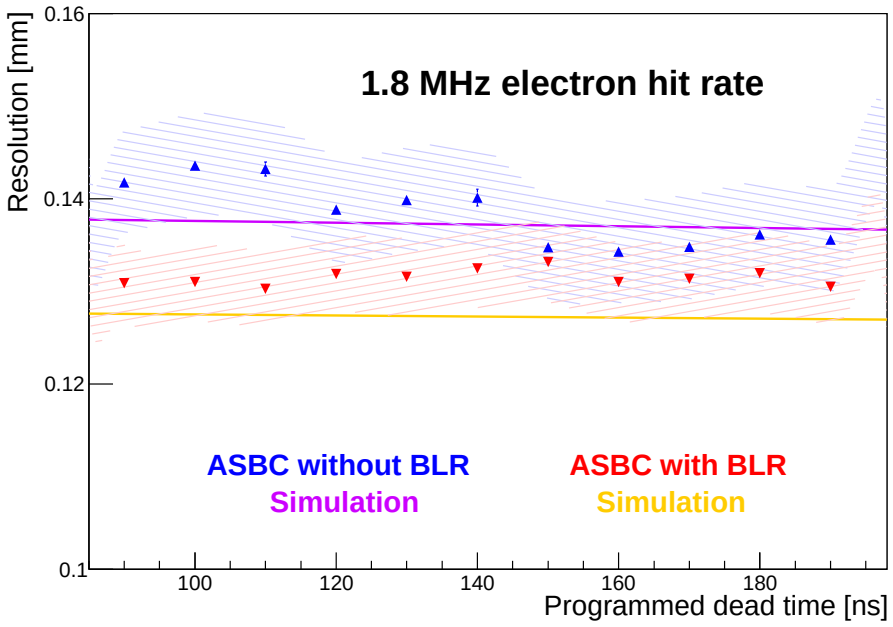


(b)

Figure 5.38.: Average single tube spatial resolution for different dead time settings measured with ASD (without time slewing correction) and with ASBC with and without baseline restoration depending on the background electron hit rate.

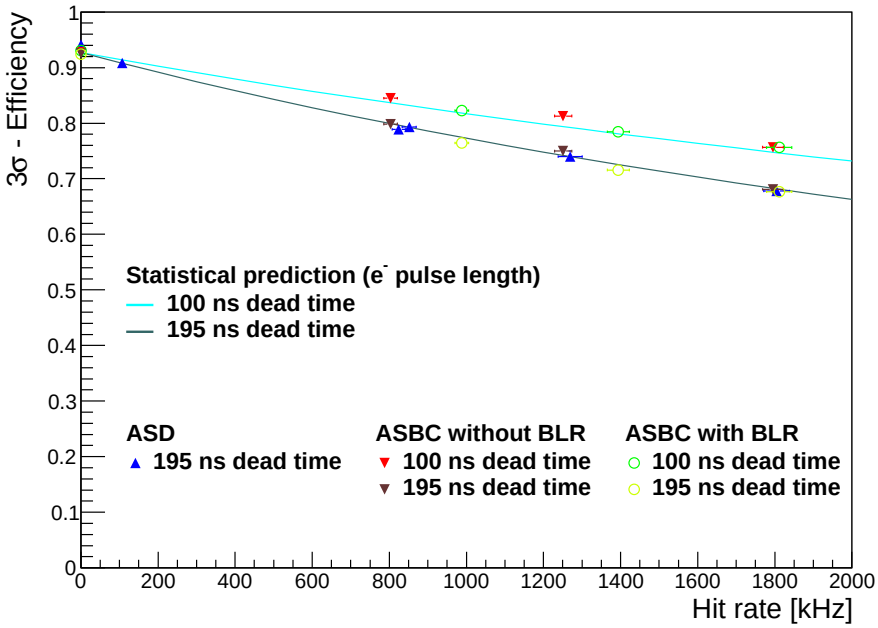


(a)

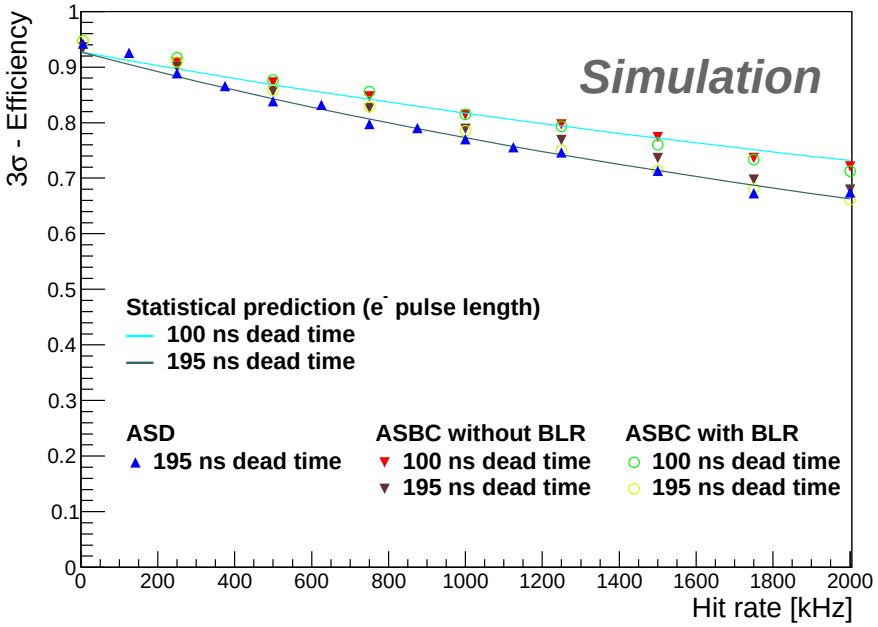


(b)

Figure 5.39.: (a) Average sMDT single tube spatial resolution for different dead time settings measured with ASD (without time slewing correction) and with ASBC with and without baseline restoration depending on the background electron hit rate.
(b) Average sMDT single tube resolution measured with the ASBC as a function of the dead time. While the hatched areas show the uncorrelated statistical error, the error bars indicate the correlated uncertainty between two neighboured points.



(a)



(b)

Figure 5.40.: (a) 3σ-efficiency depending on the background electron hit rate measured with the ASD chip and the ASBC electronics with and without baseline restoration (BLR) for different dead time settings in comparison with statistical prediction.
(a) Statistical prediction and full simulation of the ASD and ASBC with and without baseline restoration (BLR) of the 3σ-efficiency depending on the background electron hit rate.

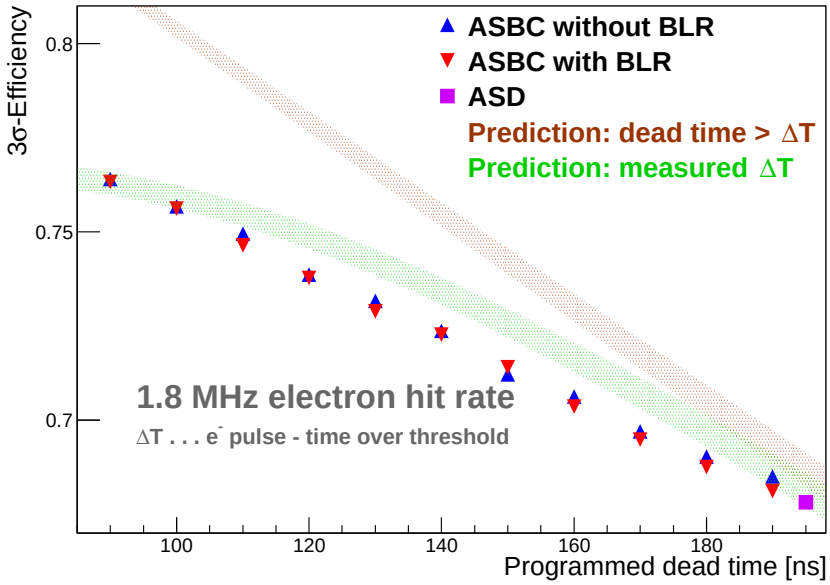


Figure 5.41.: 3σ-efficiency measured with the ASBC electronics as a function of the dead time compared with the ASD chip measurement and statistical predictions for constant and effective dead time.

In Fig. 5.40b the statistical prediction is compared with the results of the full simulation discussed in Section 5.4.3. Despite fluctuations due the statistical uncertainty, the full simulation is in accordance with the prediction.

Fig. 5.41 shows the 3σ-efficiency of sMDT tubes measured with the ASBC electronics with and without baseline restoration as a function of the programmed dead time setting together with the result with ASD read-out. The data are compared to the predictions for constant and effective dead time. With decreasing dead time, the fraction of electron pulses longer than the programmed dead time increases leading to a degradation of the 3σ muon detection efficiency. The statistical prediction describes measurement results well.

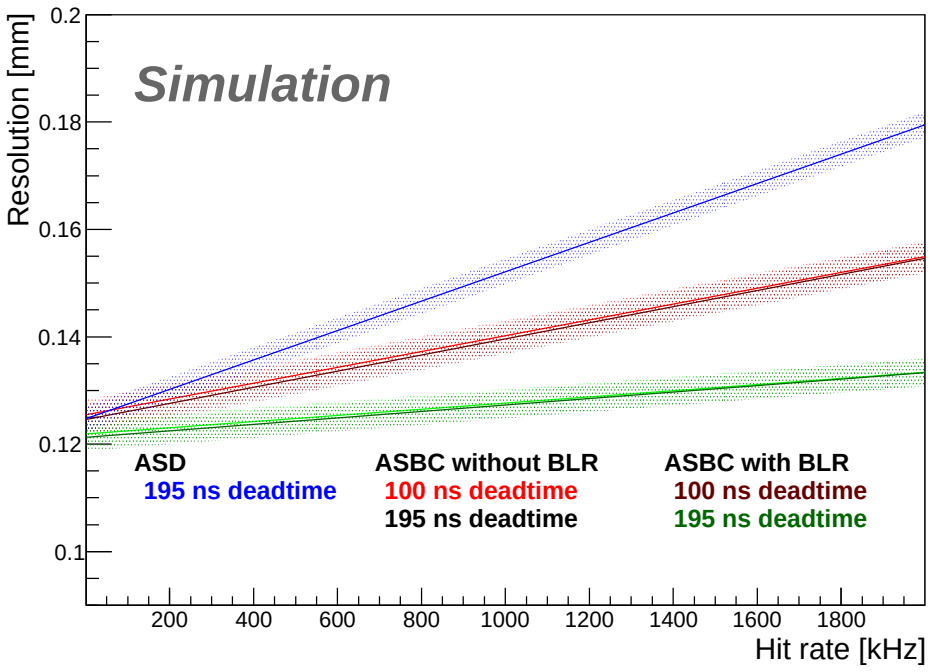
5.4.5. Performance under Irradiation with ^{137}Cs

Based on simulation of Section 5.4.3 and the results discussed above, the performance of the ASD chip and ASBC electronics under irradiation with a ^{137}Cs γ source can be estimated.

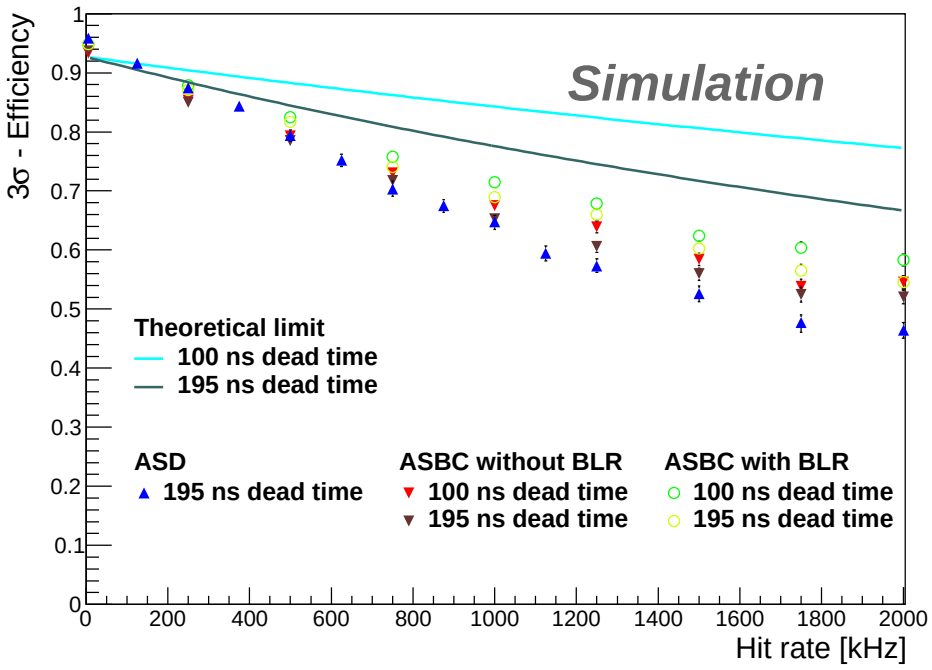
In order to obtain the same background pulse height, the electron pulses used for simulation are scaled with a factor

$$k = \frac{n_\gamma}{n_e} = \frac{900}{333} \approx 2.7 \ , \tag{5.37}$$

where n_γ and n_e are the number of primary electrons in a sMDT tube for γ (see [27]) and electron, respectively.



(a)



(b)

Figure 5.42.: Simulation of (a) the average spatial resolution and (b) the 3σ-efficiency of a sMDT tube for ASD and ASBC read-out electronics with and without baseline restoration with different dead time settings depending on the ^{137}Cs γ-hit rate (see text).

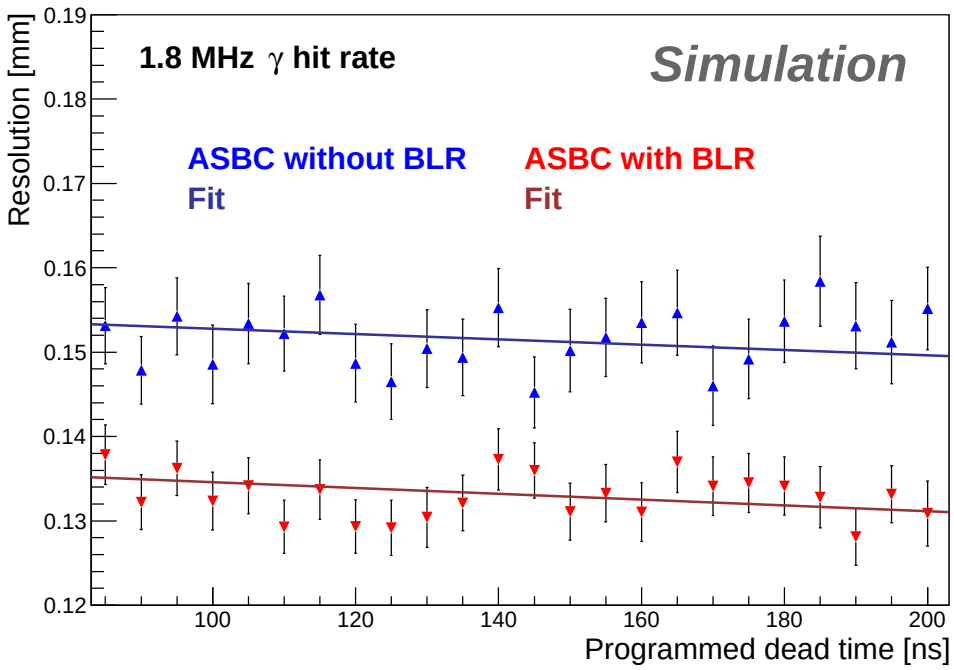


Figure 5.43.: Simulation of the average spatial resolution of a sMDT tube under γ irradiation read-out with ASBC electronics with and without baseline restoration as a function of the dead time (see text).

The gain drop for γ irradiation due to space charge fluctuations is taken into account by assuming an sMDT tube with 1 m length reducing the simulation input according to Fig. 4.10.

In Fig. 5.42a and 5.42b the results of the simulation, the average single tube resolution and 3σ-efficiency for different dead time settings as a function of ^{137}Cs γ-hit rate, is shown (see Appendix A.2.8 for the linear fit of the resolution).

While the resolution measured with the ASBC electronics with and without baseline restoration does not depend on the dead time setting (see Fig. 5.43), the efficiency increases with the dead time. Furthermore, the simulation results show that baseline restoration increases the 3σ detection efficiency and suppress the resolution degradation due to the signal pile-up effects.

5.4.6. Conclusion and Outlook

The measurement and simulation results of the experiment show that by suppressing signal pile-up effects, the rate capability of sMDT can be increased with respect to the ASD.

The programmed dead time of the discriminator can be reduced leading to a slight loss of resolution by a substantial gain of 3σ-efficiency.

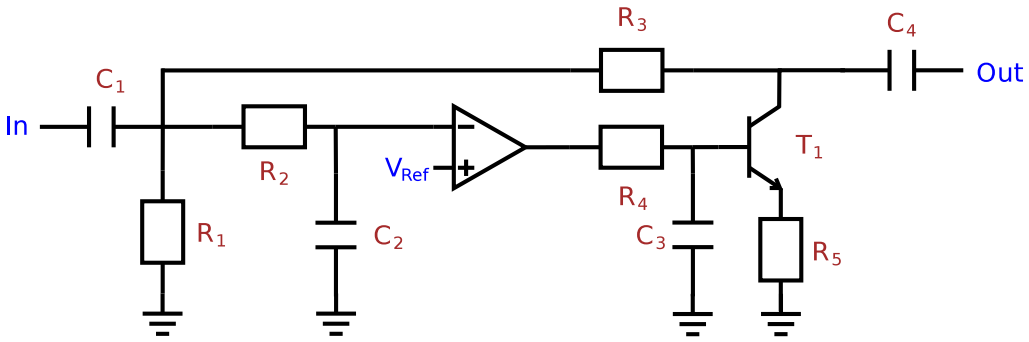


Figure 5.44.: Alternative implementation of baseline restoration. When the signal level moves below V_{Ref}, the transistor T_1 drains the current of the undershoot to ground.

Signal pile-up effect can be suppressed by reducing the rise time of the signal as well as by minimising the bipolar undershoot. Due to the fast rise time of the ASBC pulses, baseline restoration has only minor additional impact on the rate capability with respect to spatial resolution and 3σ-muon efficiency.

The results show that the shaping of the ASD chip can be further optimised to improve the resolution without background irradiation and to suppress the degradation of resolution and efficiency at high rates. The implementation of the complex baseline restoration functionality, which is also difficult to realize on CMOS chip, may not be necessary to archive this goal.

In order to fully compare the high hit rate behaviour of the ASBC electronics with previous measurements with the ASD chip, measurements with MDT and sMDT tubes have to be performed at the Gamma Irradiation Facility GIF++ at CERN [69] in a high-energy muon beam. In these measurement also space-charge effects can be studied which did not occur in the measurements discussed in this thesis.

In addition to the optimisation of the signal shaping, different options for the implementation of baseline restoration can be considered which are suitable for implementation on a CMOS chip.

The first option is the use of Schottky diodes instead of the transistor for passive baseline restoration (Schottky diodes can be implemented in CMOS [70]). Besides the faster switching times of Schottky compared to semiconductor diodes, their capacity is lower by a magnitude and, therefore, the second signal overshoot (see Fig. 5.19 in Section 5.3.3) can be avoided.

In order stabilise the working point of the diode used in the baseline restorer, an active current source, which avoids the shift of the diode working point in highly non-conducting (positive input signals) and highly conducting (negative input signals) regions of the diode characteristic line, can be used. The stabilisation reduces the recovery time of the diode, and, therefore, leads to lower switching times and a faster restoration of the baseline.

The schematic of an alternative concept for baseline restoration, which is set up succeeding to a bipolar shaper and based on a comparator which activates a pull-down resistor when the voltage level is below a certain limit, is illustrated in Fig. 5.13a). When V_{Ref} is set slightly below the baseline, there are three possible states:

- $In > V_{Ref}$: The comparator output is low and the transistor T_1 is non-conducting. Out and In are identical.
- $In < V_{Ref}$: The comparator output is high and the transistor T_1 is conducting and, therefore, pulls the potential at Out towards to the baseline leading.
- $In = V_{Ref}$: The comparator oscillates.

In order to avoid the oscillation state, a low pass filter (R_2 and C_2) is used and V_{ref} has to be chosen carefully. A second low pass filter (R_4 and C_3) is foreseen to avoid switching noise caused by fast output state changes of the comparator.

6. Drift-Tube Based First-Level Muon Trigger for ATLAS at HL-LHC

The luminosity of HL-LHC will exceed the luminosity of the LHC by an order of magnitude leading to about 10 times higher particle production rates and, consequently, causing up to 10 times higher trigger rates. In order to fully exploit the physics potential of the HL-LHC, the selectivity of the ATLAS Muon Trigger system must be improved. In this chapter a concept of improving the selectivity of the ATLAS first-level muon trigger is described.

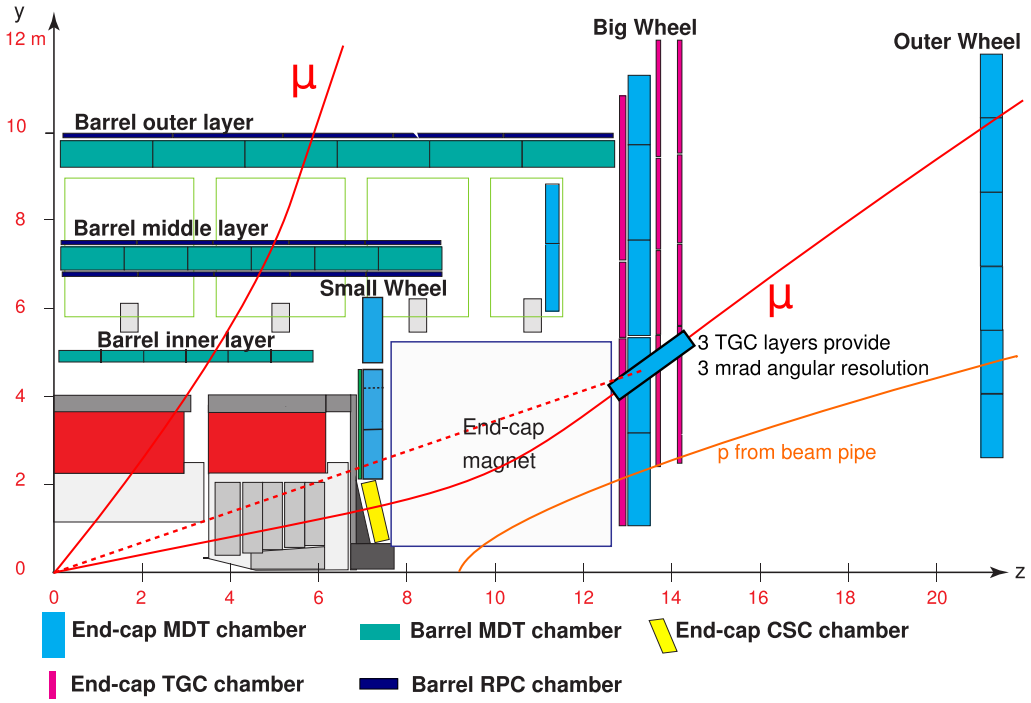
6.1. The ATLAS Muon Trigger at the LHC

The ATLAS experiment uses three trigger levels (see Section 3.2) with increasing selectivity: the Level 1 (L1) and Level 2 (L2) trigger, and the Event Filter (EF). The Level-1 muon trigger uses coincidences in different RPC and TGC detector layers. The L2 muon trigger and the EF use simplified and full offline muon reconstruction software for confirmation of the L1 decision.

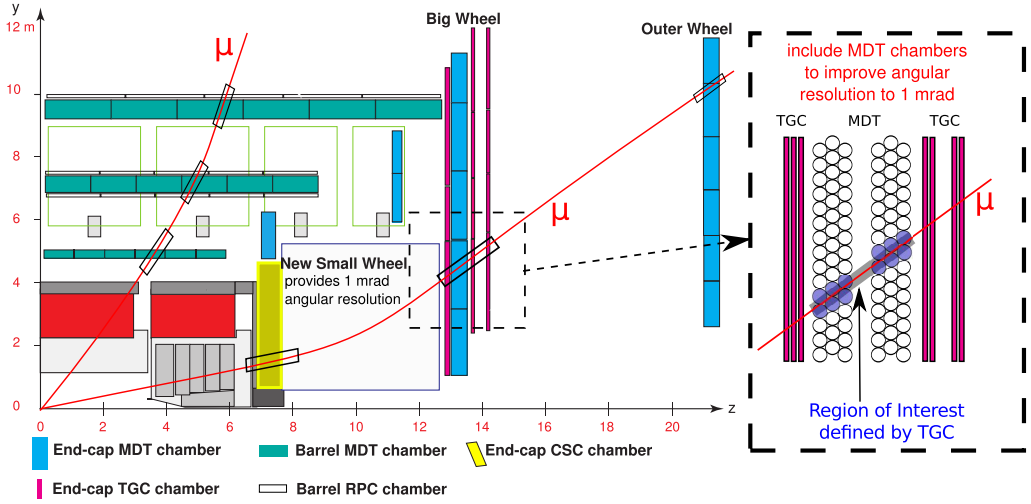
Fig. 6.1a shows a schematic of a quadrant of the ATLAS Muon Spectrometer illustrating the principle of the Level-1 muon trigger. The bending of muon trajectories in the toroidal magnetic field in the barrel and in the end-cap is shown. While in the barrel the muon trajectories are deflected between the inner and outer muon chamber layers, the magnetic field in the end-caps is restricted to the end-cap toroid region between the Small Wheel (inner layer) and the Big Wheel (middle layer) such that the muon tracks are straight lines after the magnet.

In the barrel part of the Muon Spectrometer, a coincidence of hits in the two middle RPC layers for the low-p_{T} and a coincidence between RPC hits in the middle and outer layer for the high-p_{T} trigger is required. The deviation of the hit coordinates in the outer layer from the straight extrapolation of the muon trajectory from the middle layers is a measure of the transverse momentum [9].

In the end-caps a coincidence of hits in the three TGC layers of the Big Wheel is required. At the HL-LHC, after the upgrade of TGC trigger electronics, the track angle will be known with 3 mrad resolution. The muon momentum is determined from the direction of flight measurement in the Big Wheel comparing to the straight line from the interaction point to the first trigger layer. In order to reduce fake high-p_{T} muon triggers due to charged particle tracks emerging from the beam pipe and shielding behind the Small Wheel and entering the Big Wheel by bending in the end-cap toroidal field (see Fig. 6.1a), also TGC



(a) Present ATLAS Level-1 muon trigger.



(b) ATLAS Level-1 muon trigger after the Phase-II Upgrade.

Figure 6.1.: The principle of the ATLAS Level-1 muon trigger at present and after the Phase-II Upgrade illustrated in a quadrant of the ATLAS Muon Spectrometer (see text). By adding the New Small Wheel (Phase-I Upgrade) and including the MDT chambers in the Level-1 muon trigger, the selectivity of the muon trigger can be increased and the trigger rates substantially reduced.

hits in the Small Wheel are taken into the coincidence [71].

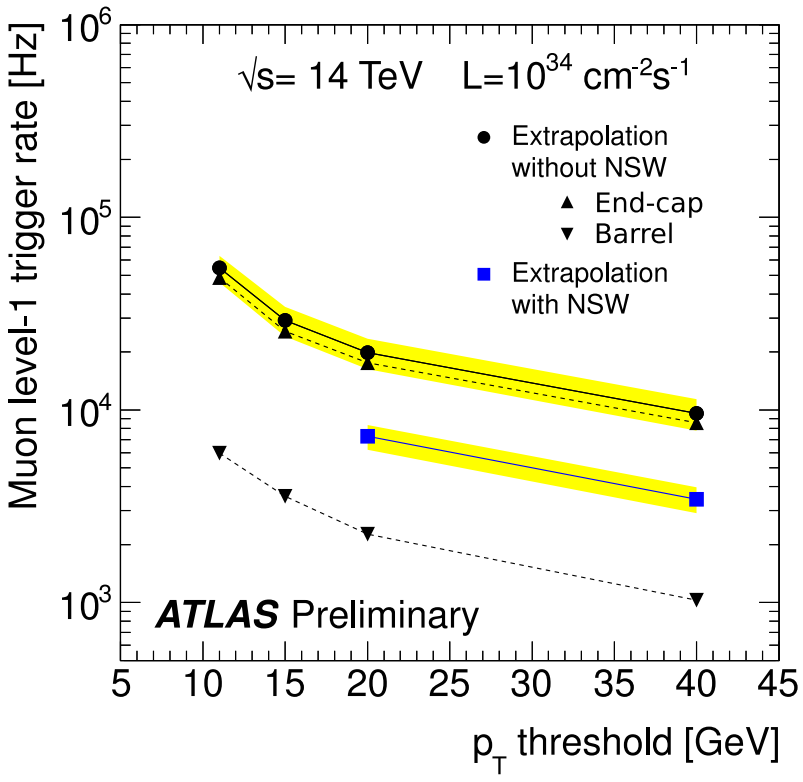


Figure 6.2.: Estimates of Level-1 muon trigger rates as a function of the nominal p_{T} with and without the New Small Wheel, which is planned to be installed in the Phase-I Upgrade at LHC design energy and luminosity [72].

Fig. 6.2 shows the Level-1 muon trigger rate as a function of the nominal p_{T} threshold expected at a centre-of-mass energy of $\sqrt{s}$=14 TeV and a luminosity of L=10^{34} cm^{-2}s^{-1}. For 20 GeV p_{T} threshold, the trigger rate in Run 2 is expected to be about 2 kHz in the barrel and about 20 kHz in the end-cap regions.

In 2018, the existing Small Wheels are planned to be replaced by so-called "New Small Wheels" (NSW) with TGCs with higher spatial resolution (see [71]) providing an angular resolution of 1 mrad in the L1 trigger leading to an expected end-caps muon trigger rate of 8 kHz of the nominal p_{T} of 20 GeV single-muon trigger threshold.

If one was able to measure the direction of flight in the Big Wheel with the same precision already at the first trigger level, one could measure the muon momentum much more precisely than presently and would reduce the trigger rate substantially close to the present Level-2 muon trigger rate. In the following section it will be elaborated how the MDT chambers can be used to provide a direction measurement with 1 mrad resolution at the first trigger level.

6.2. The Concept of an MDT Based Level-1 Muon Trigger

The present ATLAS trigger scheme will be modified for the operation of the ATLAS detector at the HL-LHC. The existing three-level system will be changed to a three-level system in which the current Level-1 muon trigger is replaced by two levels, a so-called Level-0 (L0) and Level-1 (L1) and the L2 and EF are merged to the so-called High-Level-Trigger (HLT).

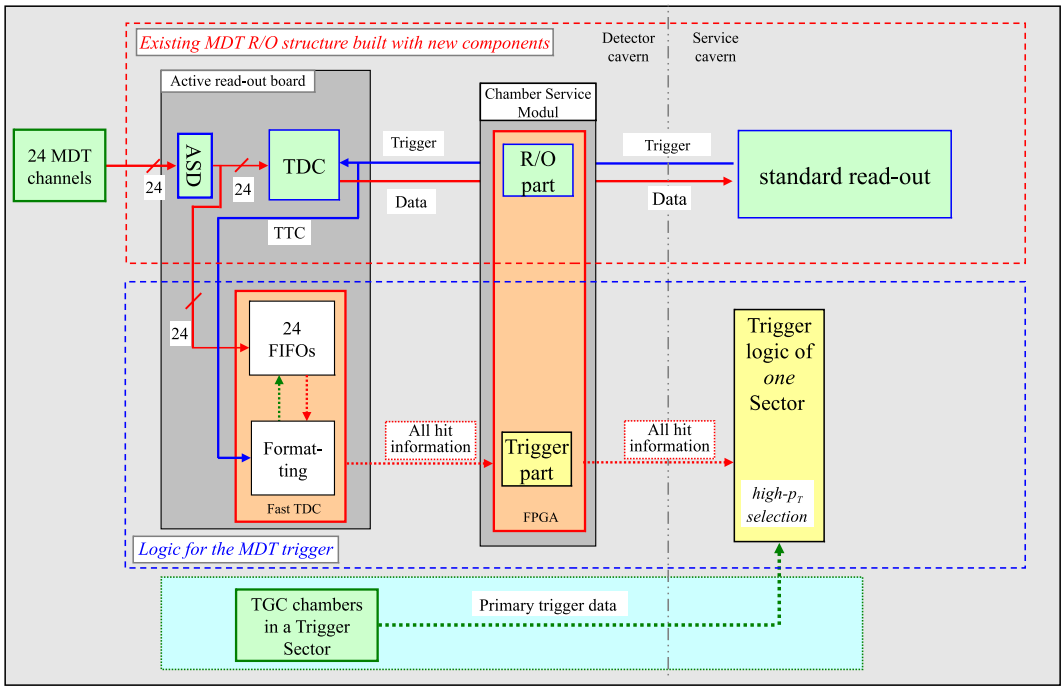
The new L0 trigger will be very similar to the current L1 trigger, however with ten times higher rate capability, namely 1 MHz instead of 100 kHz, and a latency of 6 μs, see [14]. The new L1 will cope with 400 kHz trigger rate capability and 60 μs latency to allow for complex operations such as fast track reconstruction in the Inner Detector[1].

In order to gain precision in the muon momentum determination, the MDT chamber data has to be integrated into the Level-0 muon trigger at the HL-LHC, see Fig. 6.1b. The TGCs at L0 define a Region of Interest, a few centimetre wide search road where the muon hits lie within, and the corresponding MDT drift-time information is used for track reconstruction with higher precision than provided by the TGCs. This requires a redesign of the MDT chamber read-out electronics [73], because the MDT chambers have to be read-out in a trigger mode.

To allow for the measurement of the muon direction after the end-cap toroid with 1 mrad resolution, it is planned to implement an additional continuous data stream containing the hit data of the MDT tubes, however with a drift-time resolution 10 times worse than in the standard read-out to reduce the volume of the transferred data [74]. This reduced time resolution is sufficient for reaching the required 1 mrad angular resolution.

Fig. 6.3 shows the principle of the new read-out scheme. The MDT signal pulses are amplified, shaped and discriminated by the amplifier, shaper, discriminator (ASD) chip (see Section 5) and then feed to two read-out chains. While in the standard read-out chain the times of the MDT signals are measured with a TDC with a time resolution of 0.78 ns and only extracted after a L1 trigger, in the additional fast read-out chain the signal times are measured with reduced precision (12.5 ns) and the measured times are sent to the trigger logic in the continuous data stream mentioned above. When the TGCs detect a trigger candidate, the information of the Fast TDC can be used for fast track reconstruction, leading to a more precise p_{T} determination [75].

[1] According to [14], 200 kHz trigger rate capability and 20 μs latency are planned. The higher values are in discussion now (begin 2014).



ASD: Amplifier Shaper Discriminator
TDC: Time to Digital Converter
FIFO: Buffer (first in first out)

Figure 6.3.: Concept of the technical implementation of the MDT based Level-0 muon trigger. Besides the standard read-out chain, the MDT signals are digitised by an additional fast TDC which sends the data over the CSM to the trigger logic where it can be used for fast track reconstruction in the region of the primary muon trigger candidate.

6.3. Development of an Algorithm for the Fast Reconstruction of Muon Tracks in MDT Chambers

6.3.1. Initial Considerations

This thesis is focussed on using the MDT data to reduce the Level-0 muon trigger rate in the end-cap region, which is dominating the Level-0 muon trigger rate. The concept can be also adopted in the barrel region.

The rate reduction requires the fast reconstruction of a muon track inside an MDT chamber, under the high radiation background in the ATLAS Muon Spectrometer.

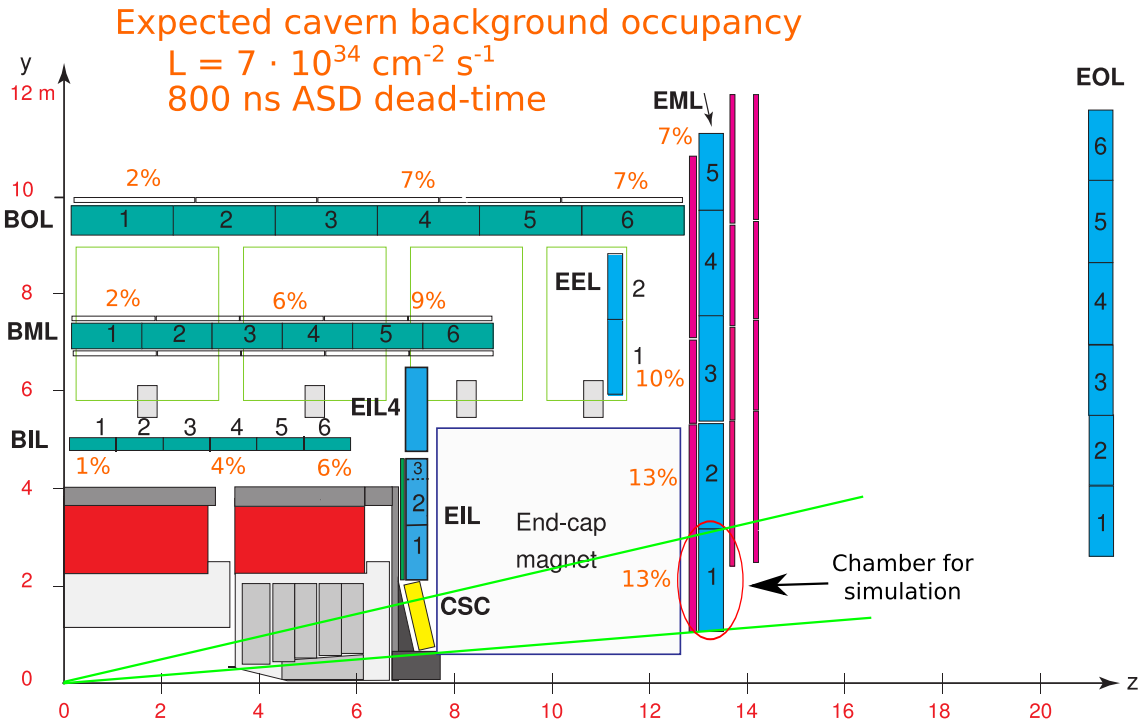


Figure 6.4.: Background counting rates in the MDT chambers expressed as occupancies [76].

In Fig. 6.4 one quarter of the ATLAS Muon Spectrometer with the expected uncorrelated background occupancies for the HL-LHC luminosity is shown. The occupancies range from 7% to 13% in the Big Wheel with the maximum close to the beam pipe. EML 1 is the chamber with highest uncorrelated background occupancy, so it can be seen as *worst case scenario* for track reconstruction. It has 6 MDT tube layers with 56 tubes per layer and a multilayer distance of 170 mm [77]. Infinite momentum tracks have incidence angles between 0.123 rad and 0.238 rad. In the following studies, an ASD dead-time of 800 ns is used.

6.3.2. Fast Track Reconstruction Algorithm

Besides the precision, the main requirements for a fast track recognition algorithm is its background capability and its simplicity to cope with the Level-0 muon trigger latency. Therefore, non-iterative algorithms are preferred. Due to the trigger level architecture, the fast track reconstruction algorithm is based on a L0 trigger candidate and can, therefore, be based on an approximate track position and angle from the L0 muon trigger candidate.

One possible algorithm is the so-called “histogram based pattern recognition” with track reconstruction. It is split into a pattern recognition and a track reconstruction part.

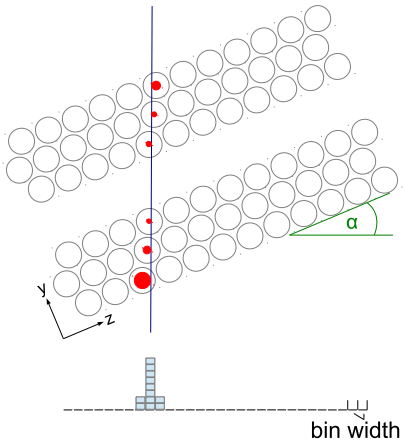


Figure 6.5.: Principle of the histogram based pattern recognition. The black circles represent the drift-tubes, the red ones the drift-radii and the blue line the muon track. The algorithm projects the drift tubes hit positions along the track direction of the L0 candidate and searches for peaks in the resulting one-dimensional hit histogram.

6.3.2.1. Histogram Based Pattern Recognition

The principle of the pattern recognition is illustrated in Fig. 6.5. The algorithm projects the drift-tubes hit positions in the plane orthogonal to the approximate track direction (so-called "seed angle", given by the primary trigger) and searches for peaks in the resulting one-dimensional hit histogram. Due to the two-fold ambiguity two positions (left and right side of the wire) are added for each hit to the histogram. The hit projection $d^{\pm}$ is given by

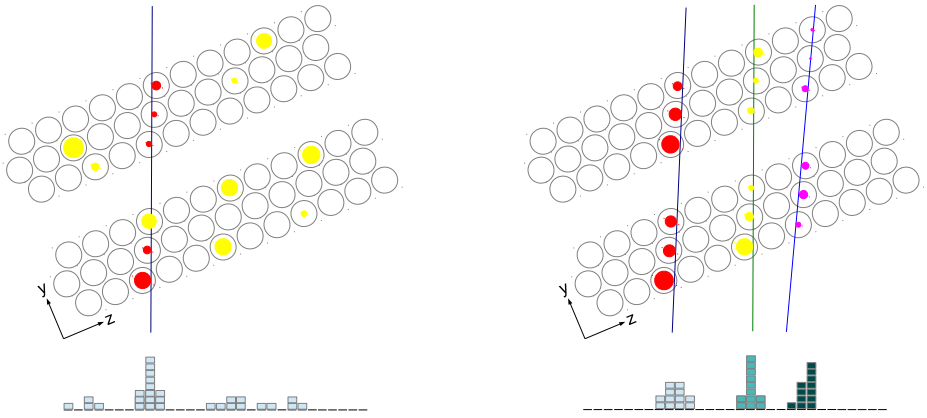
$$d^{\pm} = x_i \cdot \cos\alpha + y_i \cdot \sin\alpha \pm r_{drift} \ , \tag{6.1}$$

where (x_i, y_i) are the tube positions and r_{drift} are the drift-radii of the hits.

The histogram based pattern recognition has two parameters whose values need to be optimised.

- **Bin width of the histograms** which has to be chosen with respect to the resolution of the drift-tube and read-out electronics.
- **Trigger threshold** which is defined as the minimum number of hits in a peak. This parameter has to correspond to the tubes efficiency, the expected uncorrelated background MDT occupancy and the δ-ray probability. In Fig. 6.6a the impact of uncorrelated background (additional hit clusters in the hit histogram) is illustrated.

The histogram based pattern recognition requires the knowledge of the muon incidence angle with a certain precision. A wrong seed causes a widening of the hit distribution, which is illustrated in Fig. 6.6b.



(a) Influence of uncorrelated background.

(b) Influence of wrong sees incidence angle.

Figure 6.6.: (a) Impact of background hits and (b) seed incidence angle on the histogram based pattern recognition. While uncorrelated background hits lead to additional entries in the histogram, a wrong incidence angle washes the peak out.

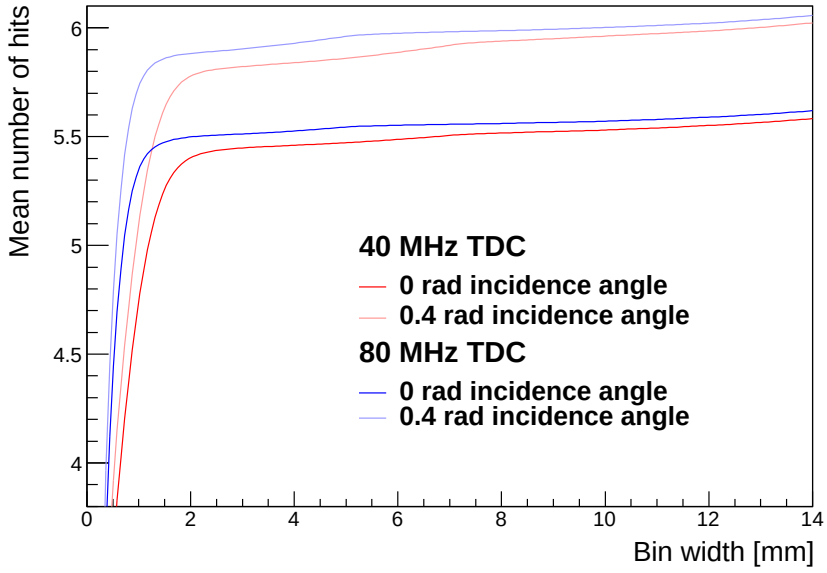
The probability distribution of the number of muon hits in a bin of a given width depends on the muon incidence angle distribution, the geometry of the muon chamber under consideration and the spatial hit distribution $\tilde{\sigma}$ which is given by

$$\tilde{\sigma} = \sqrt{\sigma^2(r) + \sigma^2_{TDC}(r)} \tag{6.2}$$

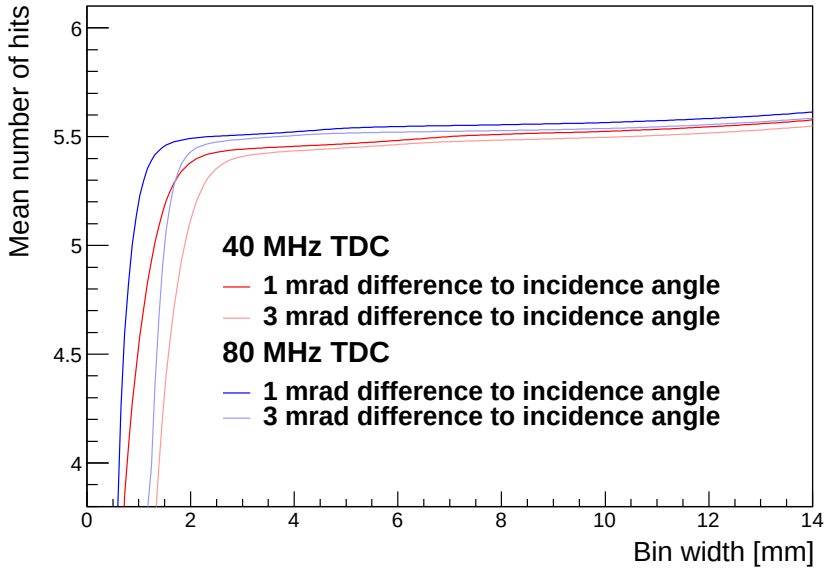
where $\sigma(r)$ denotes the single tube resolution at radius r and $\sigma_{TDC}(r)$ takes into account the influence of the limited precision of the TDC and equals the product of the time resolution of the TDC and the drift-velocity at radius r.

Fig. 6.7a shows the mean number of hits in the peak for different incidence angles and two different TDC resolutions[2] (7 ns and 3.5 ns). Fig. 6.7b shows the mean number of hits for an incidence angle of 0 rad and wrong seed angles. The distributions show fast rise followed by a nearly constant behaviour. This plateau is reached at a smaller bin width for the higher resolution TDC. The starting point of the plateau is shifted towards larger bin width with decreasing seed angle precision. However, for a seed angle resolution of 3 mrad which will be provided by the TGC trigger at the HL-LHC, 2 mm bin width is a good choice for both TDC resolutions.

[2] 40 MHz $\rightarrow \sigma_t = \frac{25ns}{\sqrt{12}} = 7ns$; 80 MHz $\rightarrow \sigma_t = \frac{12.5ns}{\sqrt{12}} = 3.5ns$



(a)



(b)

Figure 6.7.: Mean number of hits within a bin for the histogram based pattern recognition without background hits. (a) shows the mean hits for different TDC time resolution, different incidence angles and a correct assumed angle. (b) shows the mean hits for different TDC time resolution, an incidence angle of 0 rad and a wrong assumed angle.

6.3.2.2. Track Reconstruction and Measure of Quality

In order to improve the track resolution, the hits within the peak of the hit histogram can be used in a straight line fit. The straight track $y = \alpha_1 + \alpha_2 z$ through the track points (y_i, z_i), $i = 1, .., n$ is reconstructed by minimising

$$\chi^2 = \sum_i^n \frac{1}{\tilde{\sigma_i}^2} (y_i - \alpha_1 - \alpha_2 z_i)^2 \ , \tag{6.3}$$

where $\tilde{\sigma_i}$ is the spatial resolution of each hit. Further details on the straight-line reconstruction are given in Section 6.3.5.5.

The main purpose of including the MDT hit information in the Level-0 muon trigger is to veto triggers on muons with a p_T below the nominal threshold. If a low-p_T muon is identified as high-p_T muon, the correct momentum is determined in a higher trigger level. If a high-p_T muon is identified as low-p_T muon resulting in a rejection of the trigger, this muon is lost for physics analysis. Care must be taken to not veto tracks above the trigger threshold. A measure of the reliability of the reconstructed MDT track is therefore desirable. For straight track reconstruction the χ^2 per degree of freedom ($\chi^2_{p.d.o.f.}$) can serve as such a measure.

It is proposed to apply the following strategy: If the track reconstruction quality is high, the MDT chamber track is used for muon p_T determination, but if the track reconstruction quality is poor, the primary trigger candidate is confirmed and the measurement of the p_T of the trigger candidates has to be refined at a higher trigger level. If no track can be reconstructed at all, the primary trigger is also confirmed (see [75]).

6.3.3. Monte-Carlo Simulation Studies

The histogram based pattern recognition with track reconstruction has been studied with simulated data generated with a Monte-Carlo simulation programme written by the author of this thesis.

6.3.3.1. The Simulation Framework

The simulation programme generates random muon tracks within the given position and incidence angle limits (see Section 6.3.1) and calculates the hit position for all tubes on the track according to the chamber geometry. In order to obtain the drift-time, the hit position is smeared out with the single-tube resolution (Gaussian distributed) and converted into the drift-time using the space to drift-time relationship (see Fig. 4.6). The hit efficiency at a given background rate and the impact of δ-electrons are taken into account. Uncorrelated background hits are simulated with a rate corresponding to the occupancy of interest. If a background hit occurs in a tube on the muon track and its appearance time is smaller than the muon drift-time, the muon hit is masked. If a background hit occurs in any other tube, the appearance time is treated in the same way as muon hit. By setting the drift-tube read-out inefficient after each hit, an effective dead time is simulated.

The resulting drift-times are then divided by the length of one TDC clock cycle (40 MHz and 80 MHz clock), leading to a digitised drift-time equivalent to the ATLAS read-out. For pattern recognition and track reconstruction, the digitised drift-times are converted to drift-radii and processed according to the algorithm.

6.3.3.2. Study of the Performance of the Fast Track Reconstruction Algorithm

In order to optimise the parameters of the histogram based pattern recognition, the resolution and efficiency for different parameter configurations and background occupancies are simulated. In a first step $\chi^2_{p.d.o.f.}$ of the track fit is not used.

The straight-line track fit provides two quantities, the muon direction of flight and the muon position in the chamber.

Fig. 6.8a shows the angular and Fig. 6.8b the position resolution of the algorithm for different spatial grid and trigger threshold settings. While the TDC clock frequency has a strong impact on the resolution, the histogram bin width is of minor importance, whereas a smaller histogram bin width leads to a better resolution.

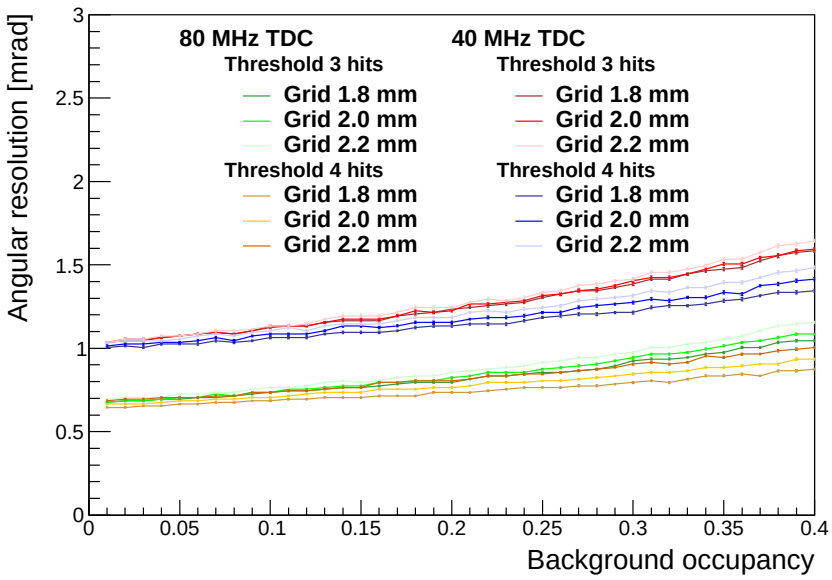
The reconstruction efficiency, defined as the probability that the highest peak of the histogram is above the threshold, is shown in Fig. 6.9. The reconstruction efficiency is increasing with a decreasing threshold, an increasing hit histogram bin width and increasing TDC resolution.

In order to obtain information about the quality of the track reconstruction, the ratio of the 3 mrad detection efficiency (which is defined as the fraction of tracks with reconstructed angle deviating from the true angle by less than 3 mrad, corresponding to the envisaged 1 mrad angular resolution) and the reconstruction efficiency is shown in Fig. 6.10. The ratio shows a small decrease with increasing background occupancy. It is about 90% if one requires at least four hits on a reconstructed track segment and about 88.0% if one requires at least three hits on the track.

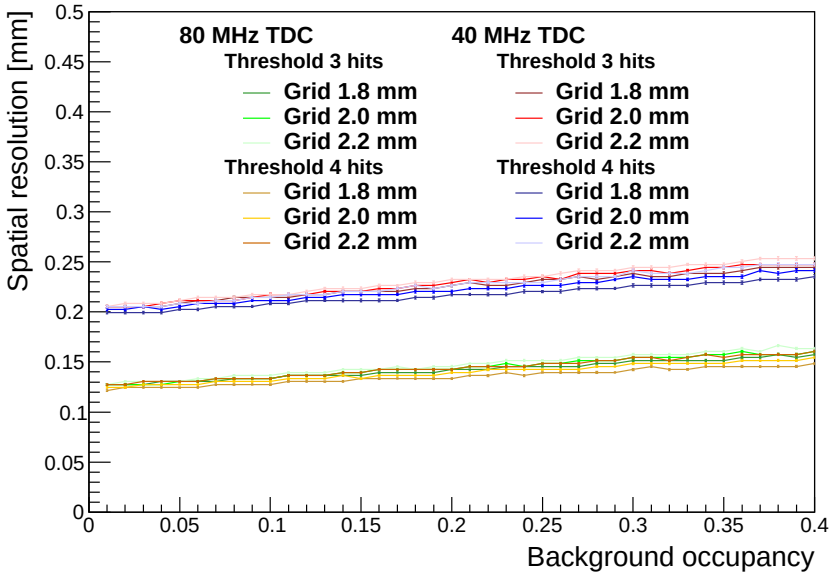
This parameter study results in the conclusion, that for angular and spatial resolution the histograms bin width is of lower importance compared to the clock frequency of the TDC. Therefore, a bin width of 2 mm is considered for further simulations. Since the fast track reconstruction is related to a reduction of the trigger rate with maximum track reconstruction quality and minimal processing time, a trigger threshold of 4 is proposed.

The second study uses the measure of quality strategy discussed before to investigate the impact on the probability of wrong angle determination. Corresponding to the seed angular resolution of 3 mrad, two categories for successfully reconstructed tracks are defined. Events with a difference between the angle of the reconstructed track α_{rec} and the true track angle α_{true} below 3 mrad are part of the first category, the category *good*. All other events are part of the second category, the category *poor*.

Fig. 6.11 shows the ratio of events within the category *good* and *bad* depending on the requirement of a the maximum $\chi^2_{p.d.o.f.}$. When an event results in several track candidates, the candidate with the lowest $\chi^2_{p.d.o.f.}$ has been used.

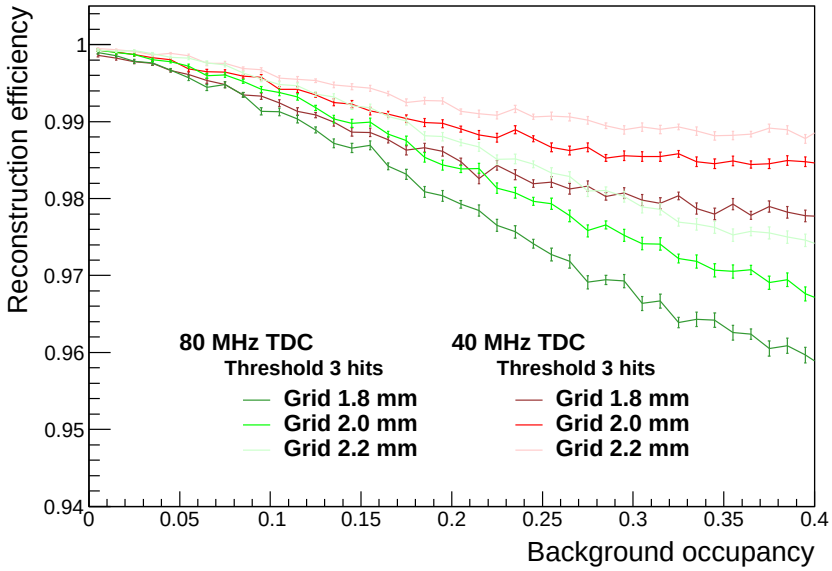


(a) Angular resolution.

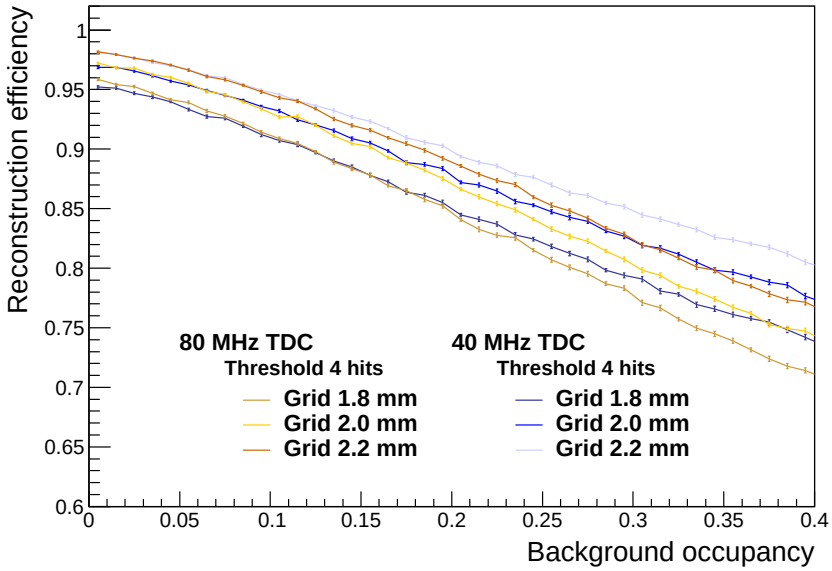


(b) Spatial resolution.

Figure 6.8.: (a) Angular and (b) spatial resolution of the histogram based pattern recognition with track reconstruction as a function of uncorrelated background occupancy for different grid sizes and hit requirements. The plots are based on a simulation of the tracks through an EML 1 chamber with a seed angle resolution of 3 mrad with 4 million Monte-Carlo events for each parameter set.

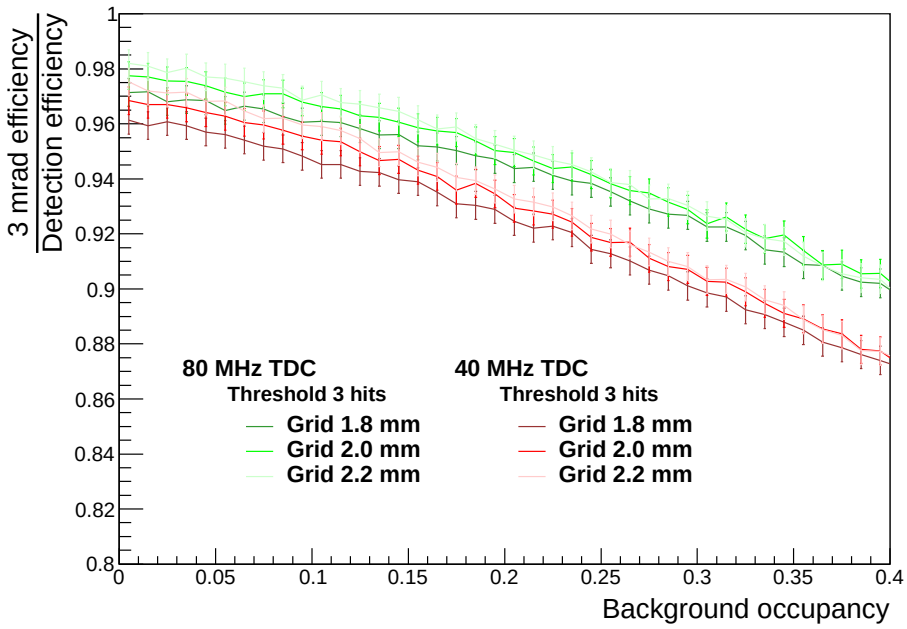


(a) Requirement 3 hits.

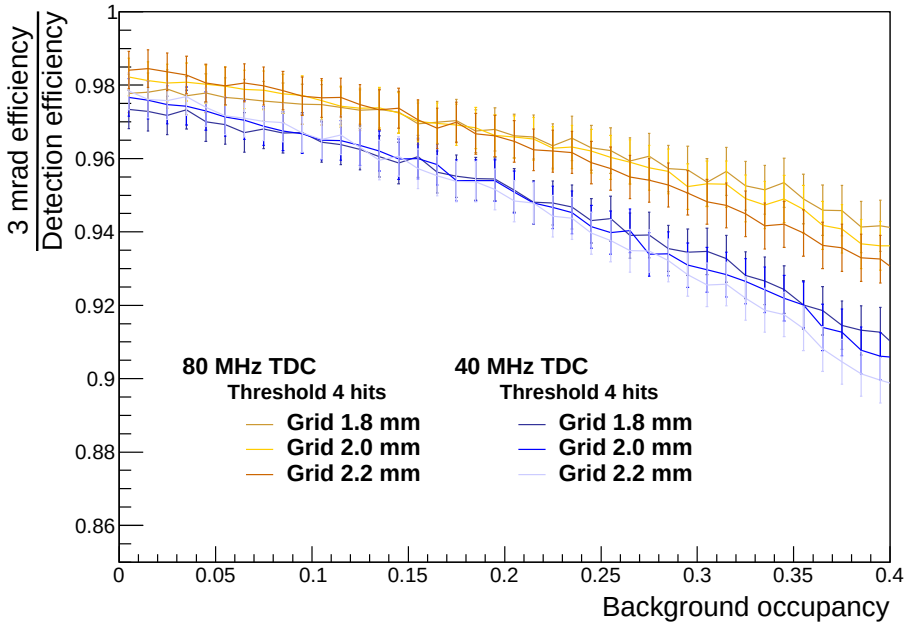


(b) Requirement 4 hits.

Figure 6.9.: Reconstruction efficiency of histogram based pattern recognition depending on uncorrelated background occupancy for different different grid sizes and the requirement of (a) 3 and (b) 4 hits. The plots are based on a simulation of the EML 1 chamber with a seed angle resolution of 3 mrad with total 4 million Monte-Carlo events for each parameter set.



(a) Requirement 3 hits.



(b) Requirement 4 hits.

Figure 6.10.: Ratio of the 3 mrad efficiency and reconstruction efficiency of the histogram based pattern recognition as a function of the uncorrelated background occupancy for different grid sizes and the requirement of (a) 3 and (b) 4 hits. The plots are based on a simulation of the EML 1 chamber with a seed angle resolution of 3 mrad with total 4 million Monte-Carlo events for each parameter set.

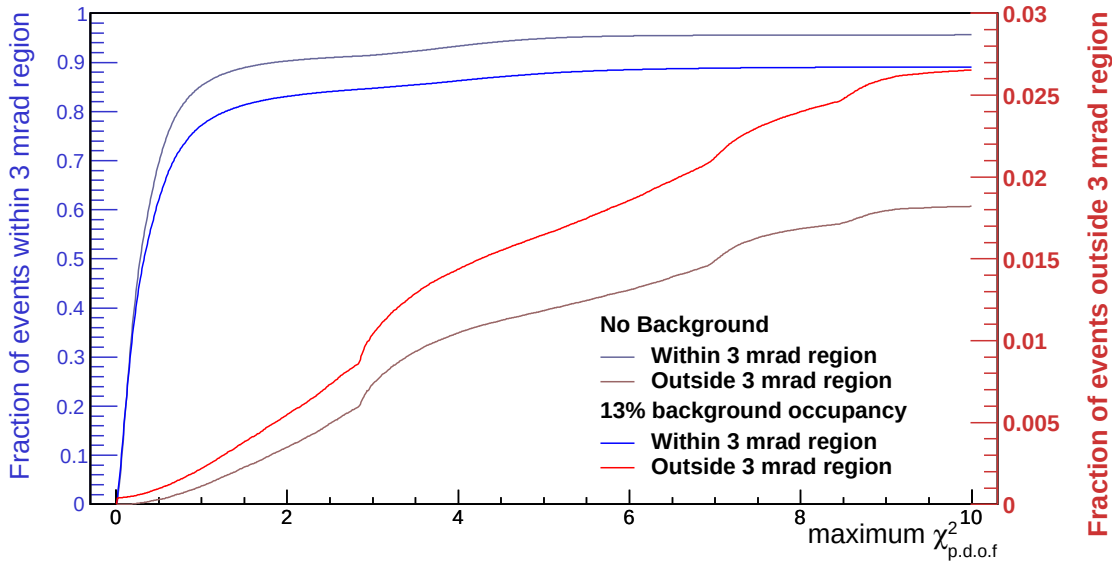


Figure 6.11.: Fraction of events where the reconstructed track α_{rec} is within or outside a 3 mrad range of the true track angle α_{true} as a function of the maximum allowed value of $\chi^2_{p.d.o.f.}$. The tracks, which are based on 800000 Monte-Carlo simulated events, are reconstructed using the histogram based pattern recognition with track reconstruction (2 mm histogram bin width, 4 hits threshold). In case of more than one reconstructed track of the pattern recognition, the one with the lowest $\chi^2_{p.d.o.f.}$ is used.

In contrast to the rate of events within the category *good*, the rate of events within the category *poor* shows a strong dependence on the measure of quality for a $\chi^2_{p.d.o.f.} > 2$.

In order to reach a 1% probability to neglect a high-p_T trigger candidate for 13% uncorrelated background occupancy (strategy to minimise fake identification, see Section 6.3.2.2), the requirement of $\chi^2_{p.d.o.f.} < 6.6$ has to be set. Due to the situation in ATLAS, half of all *poor* events are low-p_T muons which can be identified at a higher trigger level (see the symmetry of the distributions shown in Fig. 6.12).

The simulation with the final parameters with and without the measure of quality is shown in Fig. 6.12. While the use of the measure of quality effects the total efficiency insignificantly (1.9% relative efficiency loss), the neglected high-p_T trigger are reduced substantially (23% relative reduction).

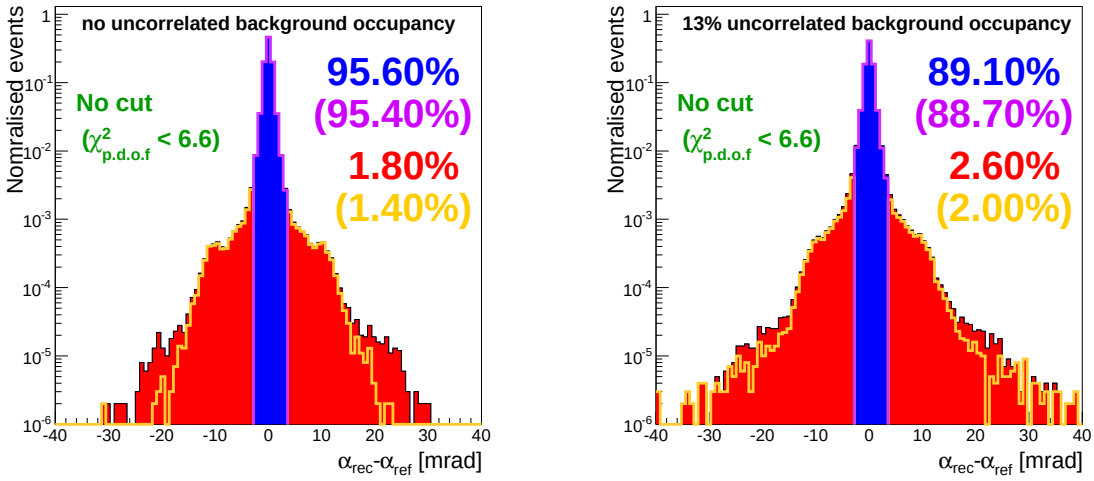


Figure 6.12.: Distribution of the difference between the true angle α_{true} and the reconstructed angle α_{rec} of the track with and without measure of quality ($\chi^2_{p.d.o.f.}$). The tracks, which are based on an 800000 event Monte-Carlo simulation, are reconstructed using the histogram based pattern recognition with track reconstruction (2 mm histogram bin width, 4 hits threshold). In case of several results of the pattern recognition, the one with the lowest $\chi^2_{p.d.o.f.}$ is used.

6.3.4. Measurement of the Performance of the Fast Read-out with Experimental Data

In order to test the technical concept described before and to study the fast track reconstruction algorithm with real data, a hardware demonstrator set-up, the so-called Test Set-up Board (TSB) was designed. The TSB was operated on an MDT chamber under γ irradiation at the CERN Gamma Irradiation Facility (GIF) [78].

6.3.4.1. The Experiment at the Gamma Irradiation Facility

In Fig. 6.13 the set-up of the experiment consisting of an MDT chamber read-out with the TSB (see Section 6.3.4.2) and an sMDT chamber used as reference is shown. The MDT chamber had 6 layers with 8 drift tubes each and the sMDT chamber 8 layers with 6 tubes each, respectively. During irradiation with a 500 Bq ^{137}Cs-source, which flux has been attenuated with configurable filters leading to different background occupancies, tracks of cosmic muons have been measured. The trigger has been set up with two scintillators in coincidence which were shielded from the γ irradiation to avoid fake triggers causes by gamma irradiation. Furthermore, a 10 cm thick layer of lead has been added between the sMDT chamber and the lower scintillator to harden the cosmic muon spectrum.

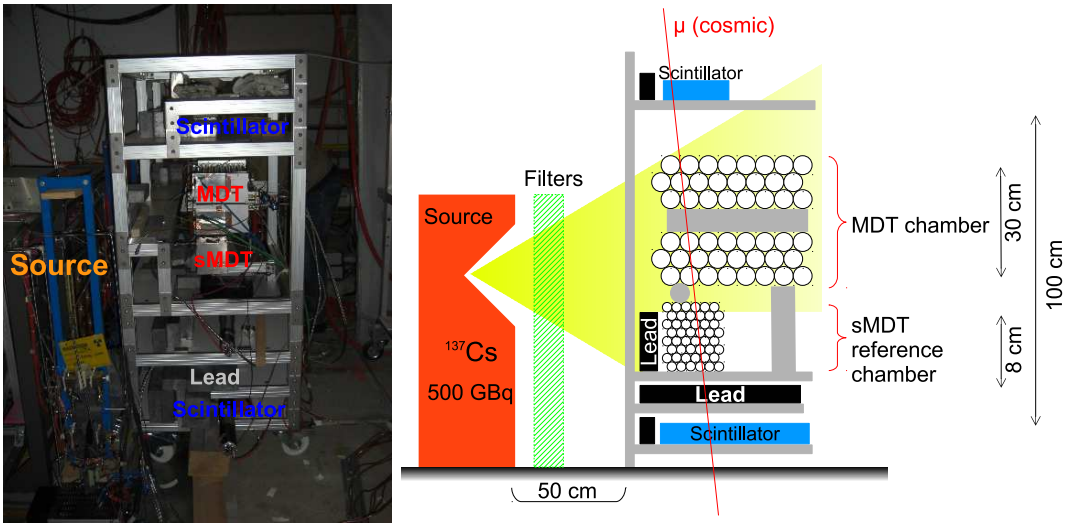


Figure 6.13.: Photograph and schematic of the experiment set-up for investigating the performance of fast track reconstruction with experimental data. While the MDT chamber was irradiated with γ-radiation of an ^{137}Cs source, the shielded sMDT chamber was used for reference track measurement. The cosmic muon trigger has been set up with scintillators, whereas the energy spectrum of the muons was hardened by the lead layer.

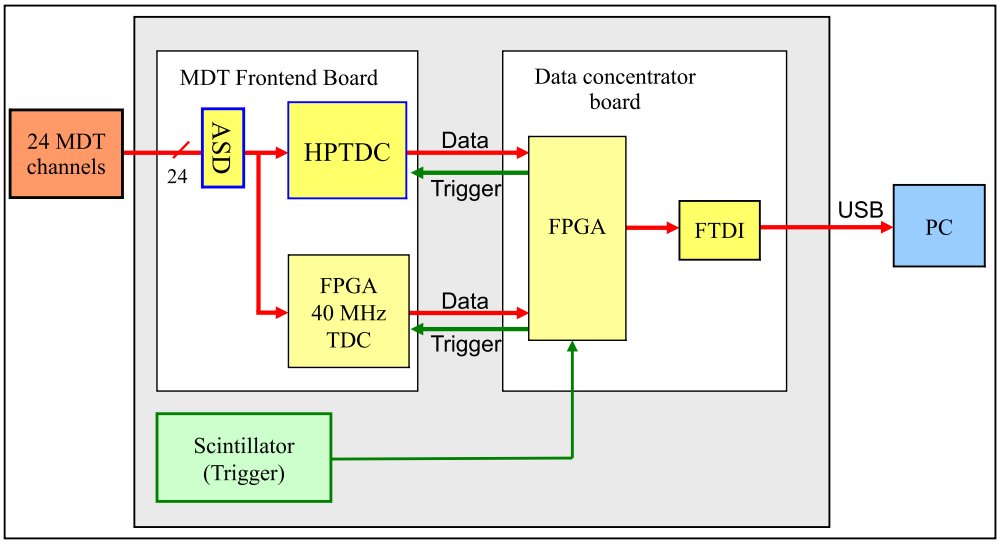
6.3.4.2. Demonstrator Set-up

In the TSB the standard slow read-out (SRO) path is accompanied by a fast read-out (FRO) path as illustrated in the schematic in Fig. 6.14. The HPTDC[3] [79] from CERN is utilized for the slow read-out with high time resolution. A single-hit TDC with 7 ns resolution is implemented for the FRO on the TDC. Hit buffering, which would have been needed for multi-hit capability was avoided to keep the TSB as simple as possible. So the FRO was operated with an effective dead time of 1500 ns. Both read-out paths were triggered synchronously and their data were recorded for offline analysis.

An MDT drift-time spectrum measured with the standard and fast read-out is shown in Fig. 6.15. The lower time resolution of the fast read-out than the slow standard read-out is reflected in the shallower rising edge of the drift-time spectrum recorded by the FRO. Since the low precision TDC of the FRO measures times in multiples of 25 ns, the corresponding drift-time spectrum shows spikes every 25 ns, which are smeared out by the trigger time correction (see Section 5.4.2.1).

The single tube resolution measured with standard read-out is compared with the resolution of the fast read-out in Fig. 6.16. The resolution was determined with the technique described in Section 5.4.2. Due to its lower TDC time resolution (7 ns), the spatial resolution measured with the FRO is worse than measured with the standard read-out (0.23 ns).

[3]High Performance Time to Digital Converter



ASD: Amplifier Shaper Discriminator
HPTDC: High Performance Time to Digital Converter
FTDI: USB interface

Figure 6.14.: Schematic of the data flow on the demonstrator set-up (Test Set-up Board), see text.

The degradation of the spatial resolution in the FRO compared to the SRO is caused by the low time resolution of its TDC. The expected resolution for such a TDC is in agreement with the measurement.

6.3.4.3. Simulation

In order to interpret the results of the test measurements, the experimental set-up was simulated with a detailed GEANT-4 [80] based simulation programme called MT-Geant4 [81].

The configuration used in the simulation is illustrated in Fig. 6.17. Besides the MDT and sMDT chambers, the simulation includes the material of the frame, all scintillator layers and the lead layer absorber between the sMDT chamber and the scintillation counters on the bottom.

The energy spectrum of the muon impinging on the set-up is assumed to be proportional to the inverse square of the kinetic muon energy which is a good approximation for the energy range relevant for the measurement [82]. The limited time resolution of the scintillator based trigger of the experimental set-up is taken into account by smearing the trigger time in the simulation by a normal distribution with 2.6 ns standard deviation. The time resolution of the trigger was determined by comparing the measured single-tube resolution with the simulated single-tube resolution without the smearing.

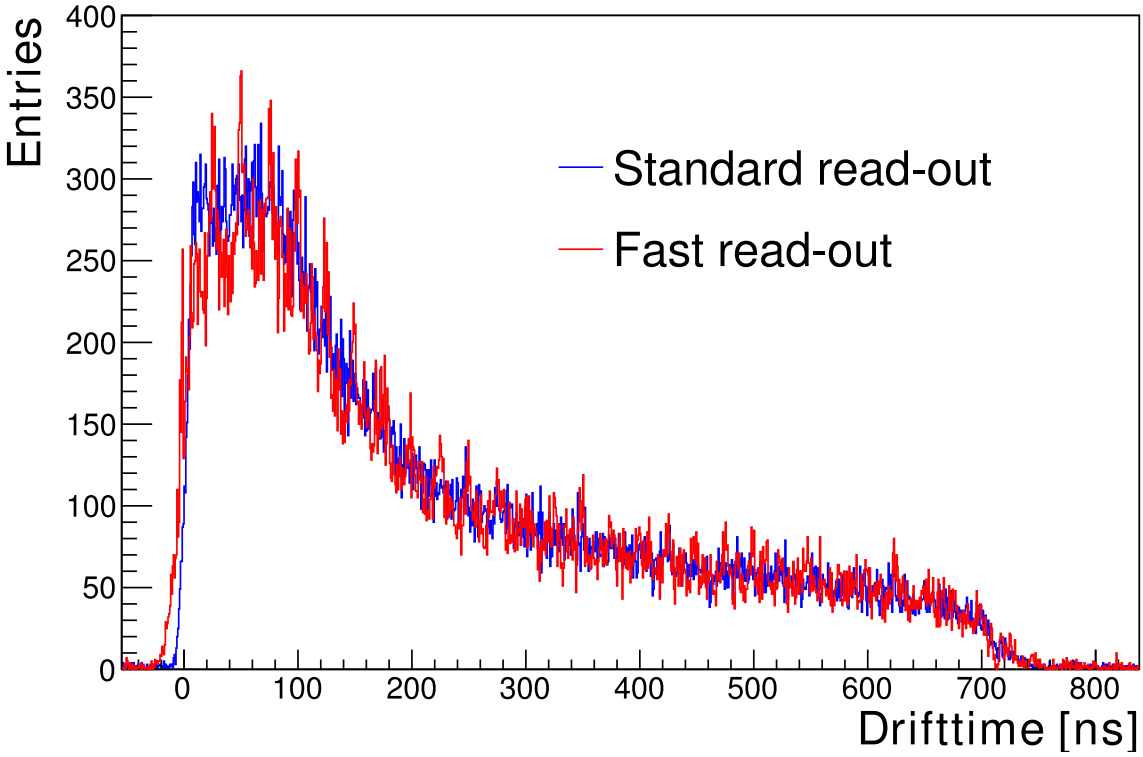


Figure 6.15.: MDT drift-time spectrum measured with standard read-out and fast read-out of the TSB after trigger time correction [75].

Furthermore, the simulation takes into account that cosmic muons arrive uncorrelated to the 40 MHz reference clock by smearing out the drift-times with the fast TDC clock cycle length (25 ns).

6.3.4.4. Data Analysis

Data Preparation Besides using the analysis procedures already discussed in Section 5.4.2 (t_0-determination, calibration, time slewing correction, resolution determination), the alignment of the MDT and sMDT chamber is determined by minimising the distance between tracks reconstructed in the sMDT chamber and the drift-circles in the MDT chamber with the minimisation package MINUIT2 [57].

The parameters of this minimisation were the relative spatial position and rotation of the second chamber. A spatial shift leads to a shift (shift in direction perpendicular to the muon tracks) and widening (shift in direction of the tracks) of the distribution, rotation causes a double peak structure.

After conducting the minimisation in several iterations with decreasing parameter range and using the results of the previous iteration as initial values, the parameters converge.

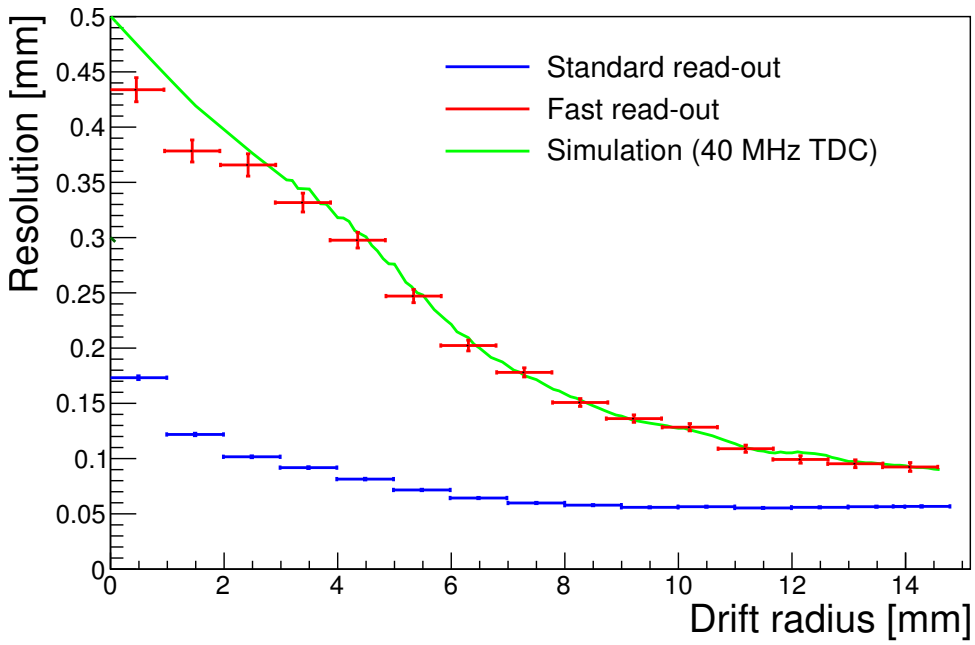


Figure 6.16.: MDT resolution measured with standard and fast read-out with a TDC based on a 40 MHz clock [75]. In addition, the expected resolution for a 40 MHz TDC and a 80 MHz TDC is shown.

In Fig. 6.18a the impact of chamber alignment is illustrated, whereat the blue line are the distribution of the distance between tracks of the first chamber and the drift-circles of the second chamber before the alignment procedure, the red line after the procedure, respectively. Due to relative rotation of the second chamber, the non-aligned distribution shows a double peak structure. The tails of the distribution are not symmetric, which is caused by δ-electrons.

Reference Tracks In order to determine the resolution and efficiency of the fast track reconstruction algorithm using the hits measured with the additional fast read-out, a reference track has to be determined. Due to the high impact of multiple scattering, the track measured with the sMDT chamber cannot be used as direct reference.

Fig. 6.18b illustrates the analysis methode used instead: The sMDT track is used to select all MDT standard read-out hits within a 26.2 mrad symmetric region of interest, this value corresponds to 99.73% of all tracks. These hits are the basis for the final MDT reference track reconstruction (see Section 5.4.2.3), which is less affected hits due to uncorrelated background.

The reference track includes the impact of single tube resolution and multiple scattering, therefore the result of the fast track reconstruction depends mainly on the fast read-out time resolution and the capability of the track reconstruction algorithm.

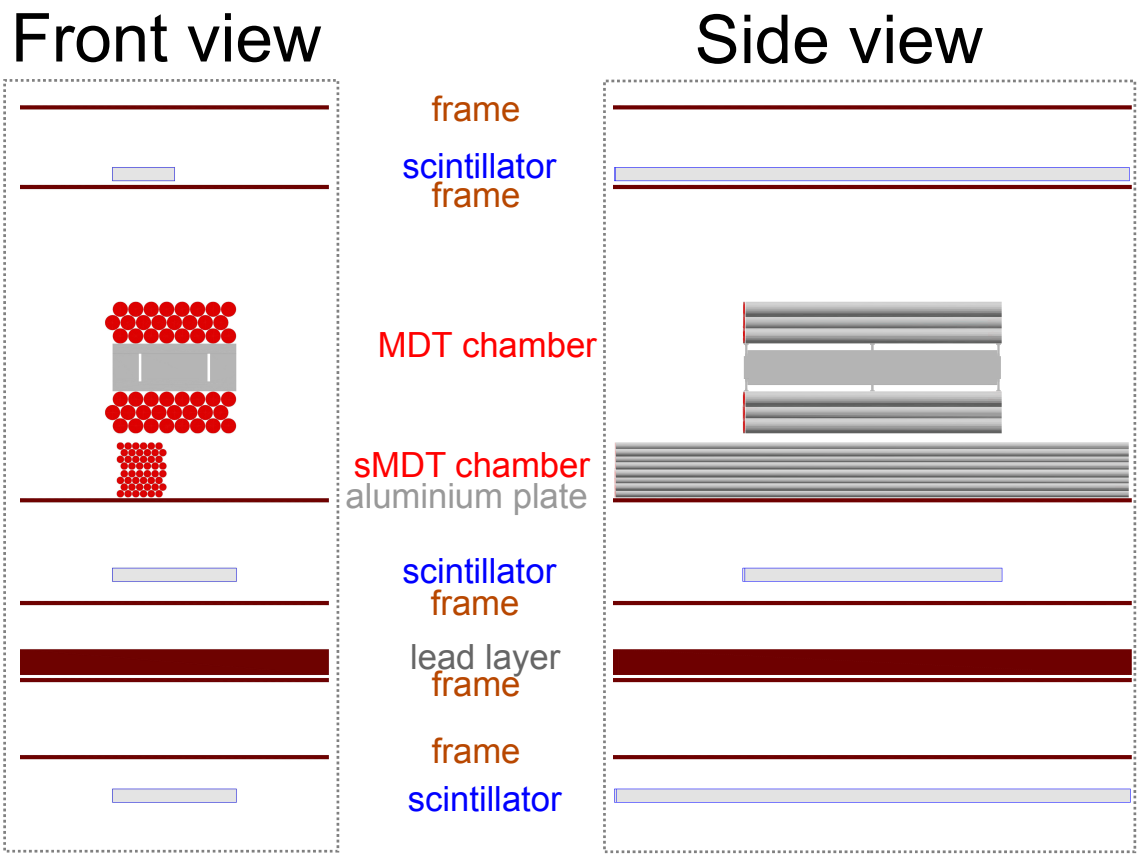
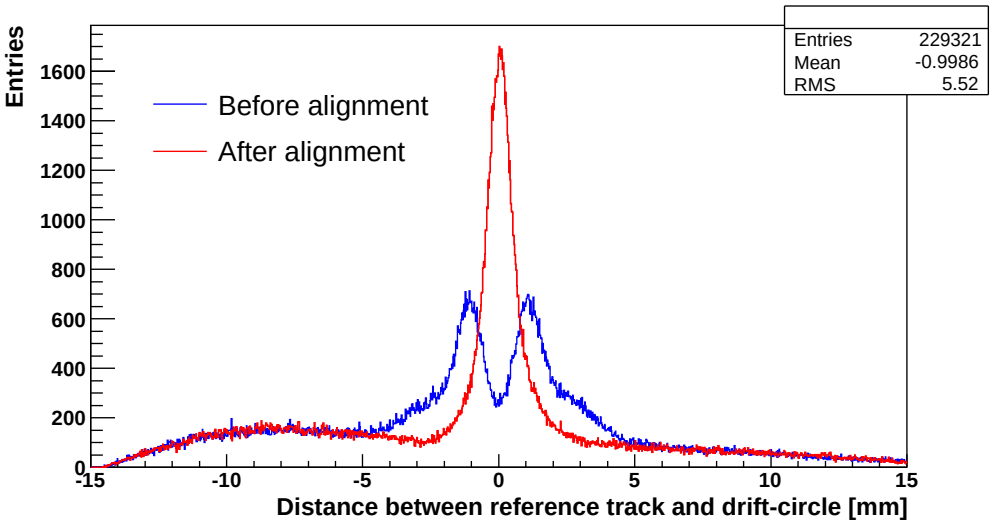


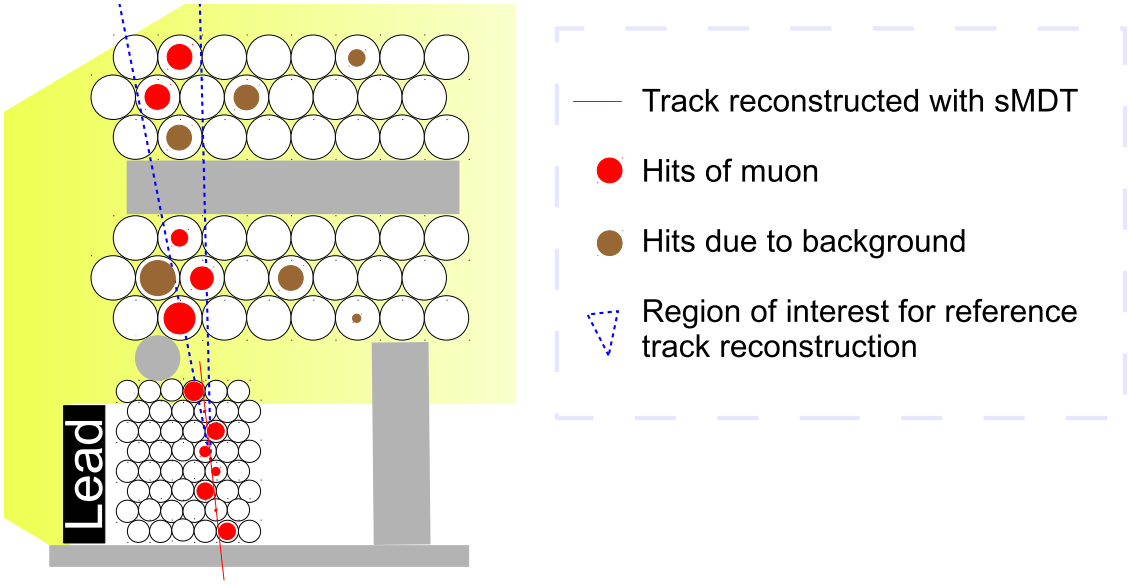
Figure 6.17.: Front and side view of the configuration of the MT-Geant4 [81] simulation describing the experimental set-up shown in Fig. 6.13.

Background Rates The uncorrelated background rate was measured using a random trigger. The rate determination was conducted by integrating over the time spectrum measured with the standard read-out TDC, see Section 5.4.2.5. The corresponding plots are shown in Section A.9.

Modification for Simulation The probability for δ-electrons is not set correctly in the used Geant4 simulation. The hit on track distributions (no background irradiation) shown in Fig. 6.19 indicates that the ratio of events with 6 hits on the track is higher in measurement than in simulation. This discrepancy is solved by selecting events according to the measured data to obtain the same distribution of hits on the track.



(a)



(b)

Figure 6.18.: (a) MDT hit residual distribution before and after the alignment of the MDT and the sMDT chamber. By rotating and spatial shifting one chamber relatively to the other the residual distribution can be narrowed. The asymmetry of the distribution is caused by δ-electrons.
(b) Principle of the data analysis. The sMDT chamber is used to reconstruct a reference track, which defines a region of interest used for MDT track reconstruction. Doing so, the impact of uncorrelated background can be minimised.

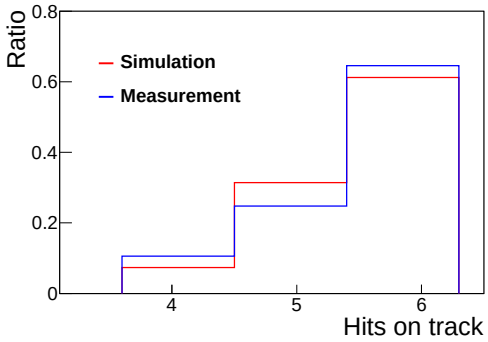


Figure 6.19.: Distribution of hits on the track for the experimental measurement and GEANT4-based simulation. In order to describe the measurement, simulated events are chosen in a way to obtain the measured hits on track distribution.

6.3.4.5. Results

In Fig. 6.20-6.21 the results of the experiment at the GIF, the difference between the standard read-out true angle α_{true} and the fast-read-out reconstructed angle α_{rec}, and the corresponding simulation are shown. The fast track reconstruction has been conducted with the histogram based pattern recognition (2 mm histogram bin width, 4 hits threshold) with track reconstruction and different angular seeds (0 mrad and 3 mrad in respect to the reference track angle).

The results show the following properties:

- The efficiency decreases strongly with the uncorrelated background occupancy.
- The width of the $\alpha_{rec} - \alpha_{true}$ distribution increases with increasing uncorrelated background occupancy.
- There is a slight difference between measurement and simulation increasing with angular seed spread and background occupancy.

Due to the long dead time of the FRO, the reconstruction efficiency is substantially lower than in the simulation of the ATLAS situation presented in Section 6.3.3. The discrepancy between simulated and experimental data are caused by an underestimation of the δ-hit probability in the Monte-Carlo simulation. Furthermore, for the simulation of 19.5% background occupancy approximations for the determination of space drift-time relation and reference resolution had to be used in order to deal with the high occupancy.

6.3.4.6. Conclusion

It has been showed that the demonstrator set-up with the additional fast-read behaves as expected. Due to the missing hit buffering of the demonstrator set-up causing a long dead time, the fast track reconstruction efficiency is strongly decreasing with uncorrelated background occupancy. In order to gain a higher efficiency, hardware with a shorter dead time should be considered for further studies.

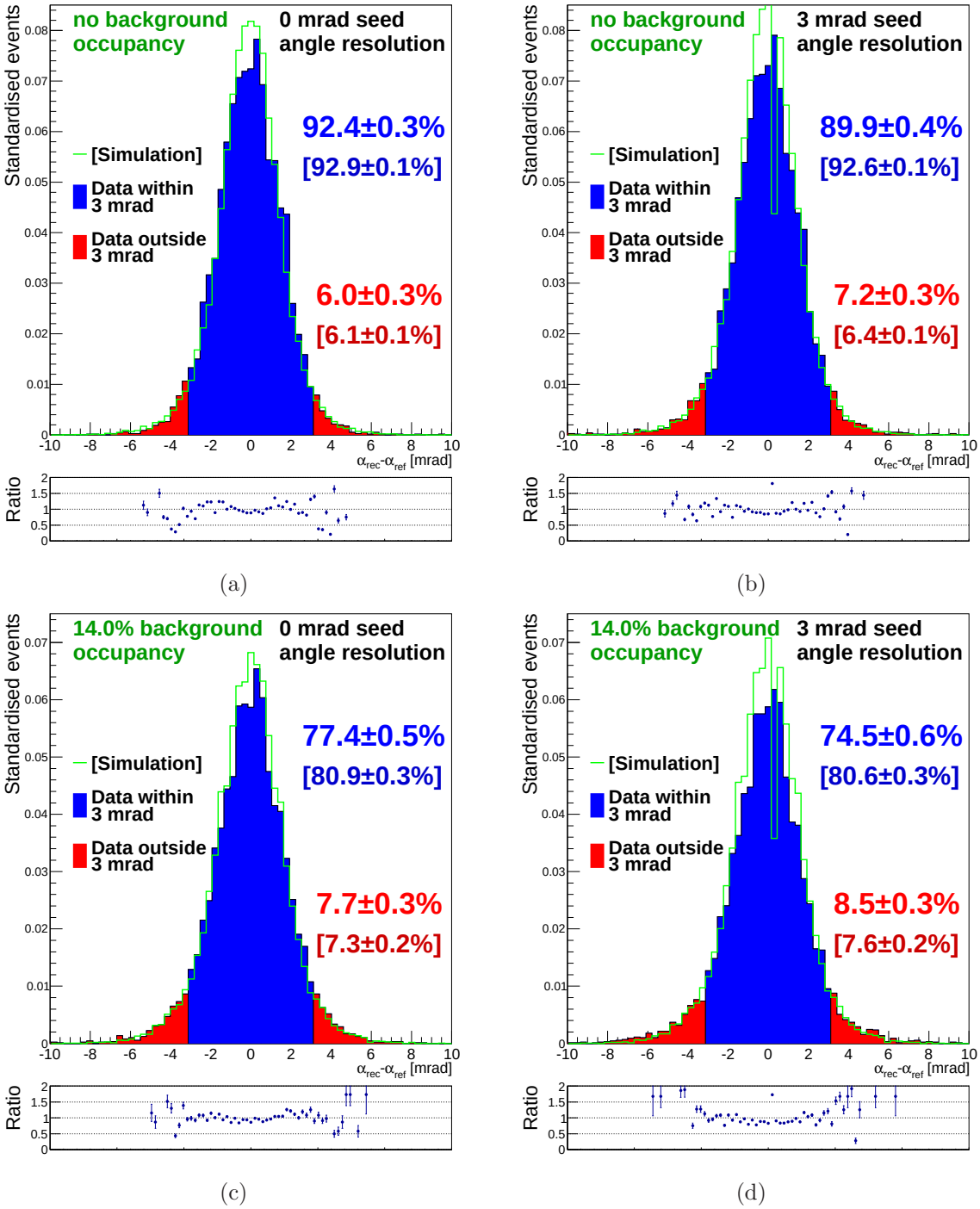
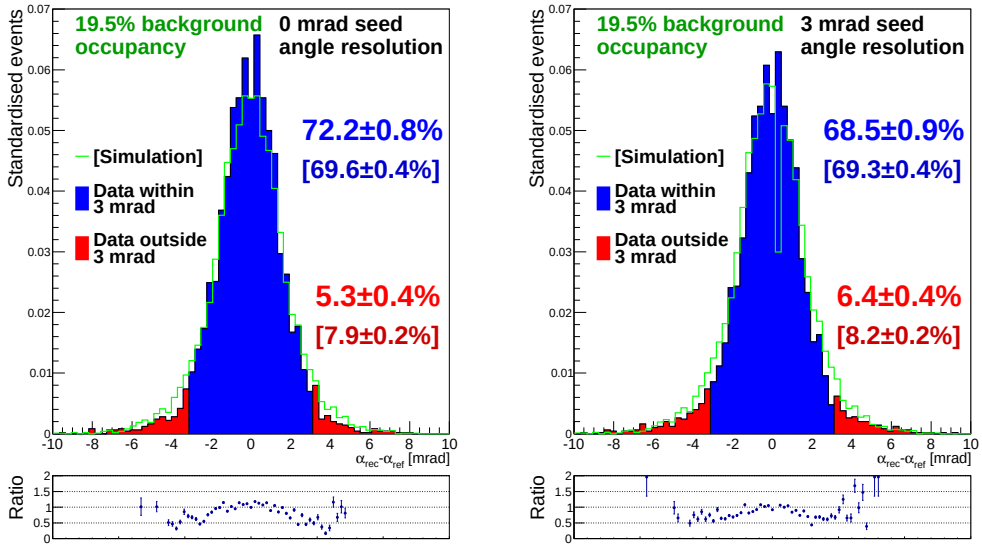


Figure 6.20.: Distribution of the difference between the true angle (standard read-out) α_{true} and the reconstructed angle (fast read-out with 40 MHz TDC, histogram based pattern recognition with track reconstruction) α_{rec}. The angle of the reference track is used as pattern recognition (2 mm bin width, 4 hits threshold) seed angle (a, c) without and (b, d) with an additional spread of 3 mrad. Ratio shows the ratio between measured data and simulation.



(a) (b)

Figure 6.21.: Distribution of the difference between the true angle (standard read-out) α_{true} and the reconstructed angle (fast read-out with 40 MHz TDC, histogram based pattern recognition with track reconstruction) α_{rec} for 19.5% uncorrelated background occupancy. The angle of the reference track is used as pattern recognition (2 mm bin width, 4 hits threshold) seed angle (a) without and (b) with an additional spread of 3 mrad. Ratio shows the ratio between measured data and simulation.

6.3.5. Timing Performance Estimation of a Technical Implementation for the Track Finding Algorithm

The constraints for track reconstruction performance is set by the maximum Level-0 muon trigger rate of 40 kHz for the HL-LHC luminosity [14] (rate of primary trigger). This means, that the Level-1 muon trigger has to reconstruct 40000 tracks per second within 1150 MDT chambers, corresponding to 104.3 tracks per three chambers and second or to a track reconstruction in each chamber every 9.9 ms. While the result of the Level-0 muon trigger has to be ready within the the Level-0 latency of 6 μs, the Level-1 muon trigger has to be ready within the Level-1 latency of 60 μs. Taking into account that the Level-0 muon trigger events are Poisson distributed and in some detector region more events occur in respect to other regions, fast track reconstruction implementation has to be capable of two reconstructions within the latency. Furthermore, cable latencies (data transfer) in the order of 3 μs have to be considered [74].

The main goal is to processes the fast track reconstruction within the Level-0 muon trigger latency. Nevertheless, the implementation of the the fast track reconstruction with regard to L0 and L1, respectively, is discussed in the following.

6.3.5.1. Initial Considerations

The first approach for hardware implementation of such tasks as track finding is using an FPGA. Even for a simple algorithm like the histogram based pattern recognition, a full implementation in an FPGA is hardly possible, because the processing speed is lowered by state-machines, and avoiding slow mathematical operations like divisions leads to huge look-up tables which cause the need for more expensive FPGA-types. In principle, the histogram based pattern recognition can be optimised to avoid complex mathematical expressions and be processed by easy shift operations as described in [83], even though the track reconstruction has to be implemented in the mathematical common way.

Therefore, it seems useful to use a modern micro-processor in the environment a SoC[4] for data processing. The basic idea is to make use of all the properties of the system and share all tasks between the FPGA part and the processor part to optimise system performance. Due to the difficulty of divisions and multiplications implementation in a generic way in an FPGA with the same duration in clock cycles as a micro-processor, all mathematical operations should be processed by the micro-processor [84, 85], while sub-processes with extensive memory access should be processed by the FPGA-part. This way memory access time and memory wait-states which can occur when micro-processor clock and memory clock differ can be avoided.

As the SoC will operate in a radiation-shielded area, all commercially available units are candidates for the implementation of the track finding algorithm. In the following a possible implementation of the histogram based pattern recognition with track reconstruction on basis of the ARM Cortex-M4F architecture [86] is described. Due to the uniformity of the ARM instruction sets, the code can easily be transferred to other ARM architectures. The Cortex-M4F is intended for deeply embedded applications and, therefore, is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, see [87]. This architecture leads to the fast processing properties of the micro-computer shown in this chapter. In addition the ARM Cortex-M4F has a floating-point unit with single precision which offers additional 32 floating point registers to the already available 12 core registers, a feature which may result in improved performance due to the fact that less memory operations are necessary for program execution. For further details see the overview of the use of registers in Tab. A.4.

The following study is based on the ARM Cortex-M4F commands described in [87] and their durations listed in [88]. It is assumed that the MDT hit information and the bunch crossing ID of the trigger candidates, given by the primary trigger chambers, are already available in the memory. Further assumptions are that the memory and CPU share the same clock, all necessary numbers (e.g. number of bins of the histogram, bin width) are stored in the code section and the number of bins is fixed.

[4] **S**ystem **o**n a **C**hip, an FPGA-processor combined system

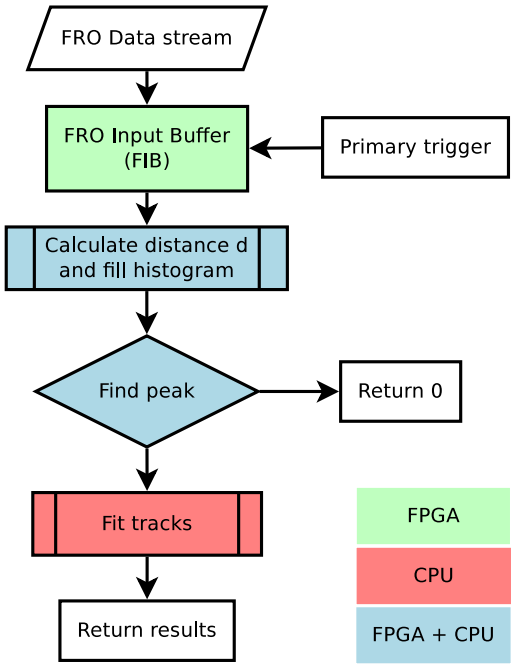


Figure 6.22.: Overview of the histogram based pattern recognition and track reconstruction implementation in a SoC. The green process is implemented in the FPGA-part, the blue ones are split between FPGA and micro-processor and the red one is processed by the micro-processor.

Due to the fact that the ARM Cortex-M4F is based on a reduced instruction set[5] [88] and, therefore, cannot directly address memory outside the 1 KB region [86], the following time estimation assumes that the input data is stored outside this memory region. Micro-processor and FPGA usually do not use the same clock, we use τ_1 for the duration of one FPGA clock cycle and τ_2 for one micro-processor clock cycle, respectively.

6.3.5.2. Schematic principle of the implementation

The overview of the technical implementation of the histogram based pattern recognition with track reconstruction is shown in Fig. 6.22. This schematic shows the single processes of the algorithm and how they should be shared between FPGA and micro-processor.

The data input buffer, the so-called FRO Input Buffer (FIB) takes care of buffering the in-streaming data and prepares the data in the case of a primary trigger signal for pattern recognition. Subsequently the data is Hough transformed, the histogram and corresponding hit buffers are filled and the histogram is searched for peaks above the threshold. In case of a successful pattern recognition the hits on the resulting tracks are used for track reconstruction.

[5] ARM Thumb Code

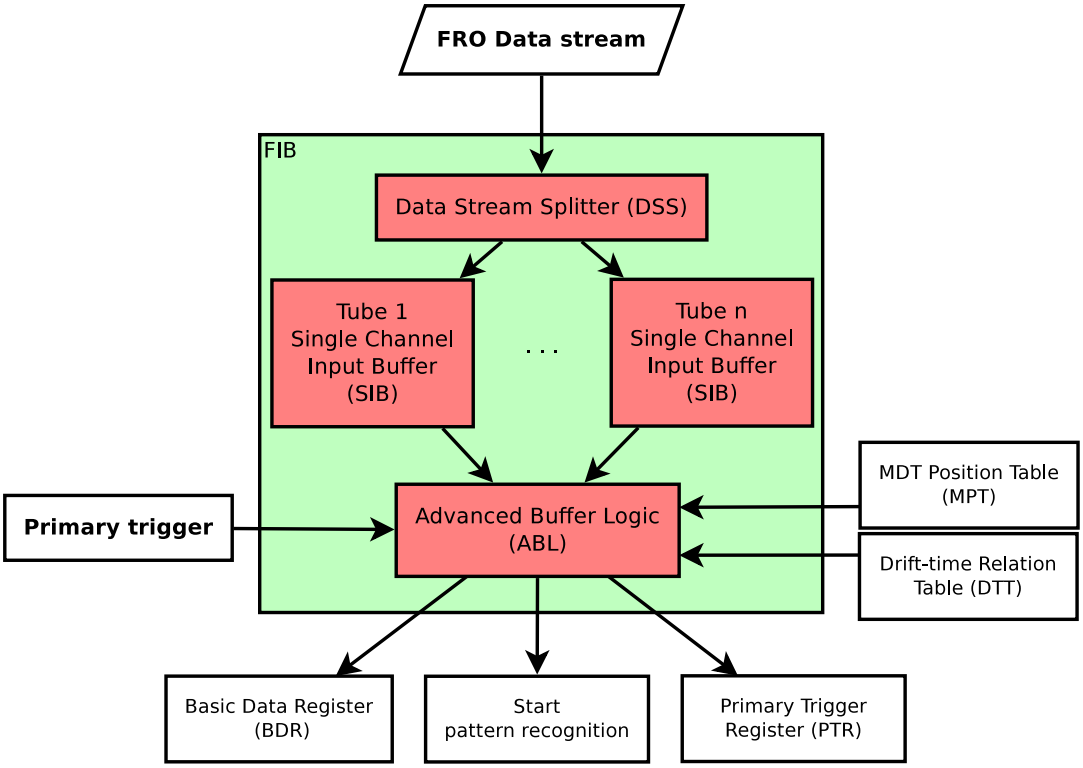


Figure 6.23.: Schematic of the FRO Input Buffer (FIB) used for buffering the FRO data stream and preparing the data for pattern recognition and track reconstruction. The incoming data stream is stored by the DSS in the SIBs. Whenever a primary trigger occurs, the ABL stores the data of the DSS together with the corresponding tube position given by the MPT in BDR and starts the pattern recognition process.

6.3.5.3. The FRO Input Buffer and Data Preparation

The FRO Input Buffer (FIB), see Fig. 6.23, is implemented in the FPGA part and consists of the Data Stream Splitter (DSS) which shares the data between n separate Single Channel Input Buffers (SIB) (n is the total number of drift-tubes which are used for track reconstruction), and the Advanced Buffer Logic (ABL) which takes care of data processing. The SIB buffer has to be large enough to store all hits within the defined latency with respect to the minimal dead-time of the MDT read-out electronics.

When the primary trigger sends the information about a trigger candidate, the ABL selects all hits within the RoI, converts their drift-time to the corresponding drift-radii and stores the tube coordinates together with the drift-radius of each hit in the Basic Data Register. The information of the tubes coordinates, the drift-time relation and the corresponding tubes in each RoI have to be known. This information will be stored in a look-up tables.

As the incidence angle of the triggering track is needed for pattern recognition, the FIB stores the primary trigger information accessible to the further processing steps by using the Primary Trigger Register.

As the timing performance is strongly depending on the actual implementation on the FPGA, the performance can only be estimated with some uncertainty. The RoI selection takes at least one clock cycle (t_s), the drift-time and tube-position conversion another cycle (T_c) and assuming another four cycles for receiving and storing data (T_r), the FIB processing time results in

$$t_1 \approx (T_s + T_r + x \cdot T_c) \cdot \tau_1 = (5 + x) \cdot \tau_1 \tag{6.4}$$

with x being the number of hits within the RoI.

6.3.5.4. Pattern Recognition

Fig. 6.24 shows an overview of the histogram based pattern recognition together with the duration in clock cycles for the implementation in a micro-processor and a combined FPGA-processor system, for a more detailed description see Section A.4. The blue fields indicate the expected duration of the operation in a ARM Cortex-M4F micro-processor, the green fields indicate the corresponding quantity a possible FPGA implementation.

The following algorithm description follows the process structure of Fig. 6.24.

1. To run the algorithms on a micro-processor, basic data has to be loaded into its core registers, but the duration of this operation strongly depends on the actual implementation.
2. Before processing the MDT hits, the bin values of the histogram are cleared. If this task is processed by the micro-processor and the histogram is implemented as byte-array, four bins can be cleared at once and thus the processing duration depends on the number of pins. If this task is processed by the FPGA-part, it does not take any time, because all bins can be cleared when the pattern recognition sub-process is started.
3. For the practical calculation, sine and cosine can be approximated by the first three elements of their Taylor-expansion

$$\sin(\alpha) \approx \alpha - \frac{\alpha^3}{3!} + \frac{\alpha^5}{5!} = \alpha - \frac{\alpha^3}{6} + \frac{\alpha^5}{120} \tag{6.5a}$$

$$\cos(\alpha) \approx 1 - \frac{\alpha^2}{2!} + \frac{\alpha^4}{4!} = 1 - \frac{\alpha^2}{2} + \frac{\alpha^4}{24}\ . \tag{6.5b}$$

   Therefore the calculation can be executed in a sequence of multiplications and additions.
4. The actual data processing starts where the duration of the histogram filling depends on the amount of hits x to fill.
   a) Each hit information is loaded from the memory into the core registers.

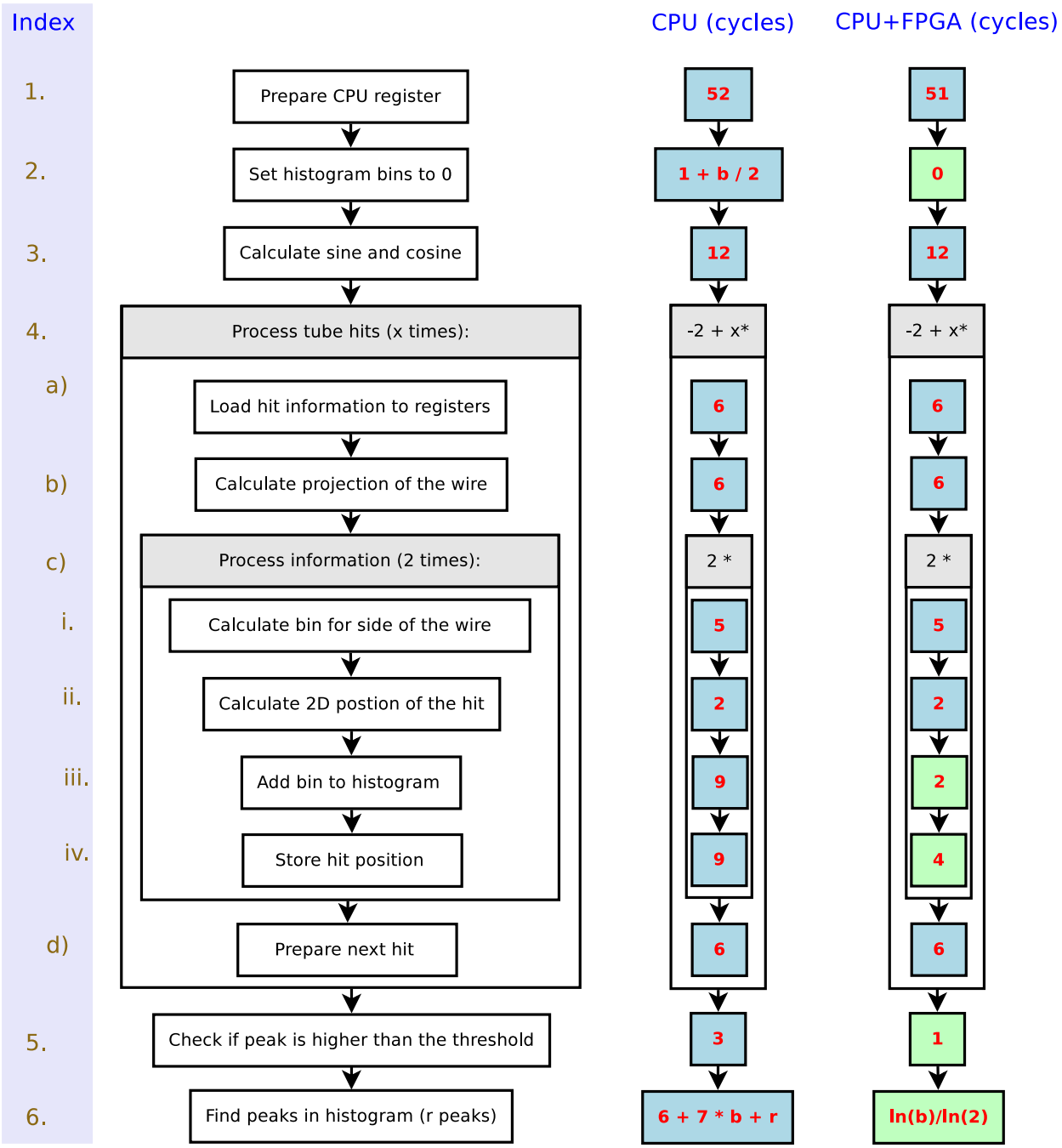


Figure 6.24.: Schematic overview and expected processing cycles of the pattern recognition process, see Fig. 6.22. b defines the number of bins of the histogram, x the number of hits to be processed. The blue fields show the expected duration of the calculation for an ARM-Cortex-M4F, assuming a memory wait time of 0. The green fields show the corresponding duration for an implementation in an FPGA-CPU combined system. Details on the processing duration are given in Section A.4.

b) Then the projection of the tube position into the direction perpendicular to the expected track is calculated, using

$$d = z_0 \cdot \sin(\alpha) + y_0 \cdot \cos(\alpha), \tag{6.6}$$

where z_0, y_0 are the position of the wire and α is the muon angle given by the primary trigger. To solve the ambiguity of the hit position, the corresponding bin for each side of the wire is determined.

i. The bin position is calculated bz adding the drift-radius to the projection of the tube position, dividing this value by the bin width of the histogram.

ii. In addition, the 2D position (z', y') of the hit

$$z' = z_0 \pm r_d \cdot \cos(\alpha) \tag{6.7a}$$

$$y' = y_0 \pm r_d \cdot \sin(\alpha) \tag{6.7b}$$

with the drift-radius r_d, necessary for later track reconstruction, is determined and stored into a buffer corresponding to the bin of the histogram.

iii. Now the bin can finally be stored in the histogram. Incrementing the value of a bin means loading, increasing and overwriting the original value. To simplify the peak position in finding in the histogram in case of several peaks, the micro-processor implementation need to know the peak height of the histogram. Therefore this sub-process is also used for peak height determination.

Due to fact that the memory has to be accessed several times, the micro-processor needs many clock cycles, while this tasks can be executed much faster in the FPGA-part.

iv. The 2D position of the hit is stored in order. This buffering can be processed faster by using the FPGA part.

c) At the end of this loop, the registers for the next hit are prepared.

5. Before the peak positions are determined, it is checked whether the highest peak is above the threshold, as discussed in Section 6.3.2.1.

6. Finally, the histogram is searched for peaks, a task which needs memory access for each bin if it is processed with a micro-processor, but which can more easily be implemented in an FPGA, using the "knock-out system" system, see Fig. 6.25. In this scheme, peak-finding is done by comparing two adjacent bins, reducing the total amount of bins with each cycle by a factor of two. Therefore the peak-finding in the FPGA-part needs

$$t_{peak} = \frac{\ln b}{\ln 2} \cdot \tau_1 \ . \tag{6.8}$$

Summing up all contributions leads to a total duration of

$$t_2 = \left(72 + \frac{15 \cdot b}{2} + 68 \cdot x + r\right) \cdot \tau_2 \tag{6.9}$$

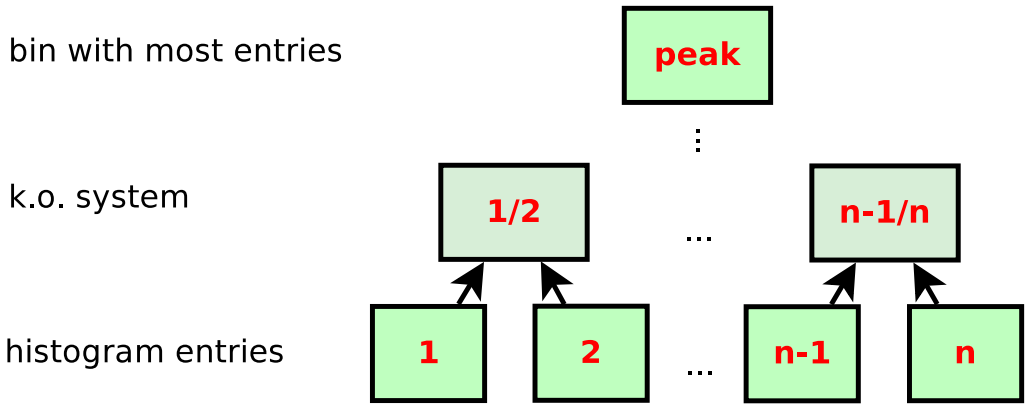


Figure 6.25.: Principle of the algorithm for peak-finding in a histogram implemented in an FPGA. The principle is based on the knock-out system, with each clock cycle the number of bins is reduced by a factor of two by comparing two neighboured bins.

with an ARM Cortex-M4F micro-processor. With an FPGA-CPU combination the duration is:

$$t_2' = \left(1 + \frac{\ln b}{\ln 2}\right) \cdot \tau_1 + (63 + 44 \cdot x) \cdot \tau_2 \tag{6.10}$$

where x is number of hits, b the number of bins of the histogram and r the number of entries in the highest peaks.

Comparing t_2 and t_2' shows, that both durations depend on b, but t_2 is dominated by b. The following table shows t_2 and t_2' for different parameters and a 200 MHz CPU and FPGA clock ($\tau_1 = \tau_2 = 5$ ns).

b	x	r	t_2 [μs]	t_2' [μs]
128	6	1	7.20	1.68
128	8	1	7.89	2.12
128	12	2	9.25	3.00
256	6	1	12.01	1.68
256	12	2	14.05	3.00
256	24	4	18.14	5.64

While the histogram peak-finding with the CPU dominates t_2, t_2' does not show this effect.

6.3.5.5. Fast Track Reconstruction

A straight track $y = \alpha_1 + \alpha_2 z$ can be reconstructed through the track points (y_i, z_i), $i = 1, .., n$ using the minimisation of

$$\chi^2 = \sum_i^n \frac{1}{\tilde{\sigma_i}^2} (y_i - \alpha_1 - \alpha_2 z_i)^2 \quad . \tag{6.11}$$

The parameters α_1 and α_2 can be obtained by

$$\alpha_1 = \frac{1}{D}\left(g_1\Lambda_{22} - g_2\Lambda_{12}\right) \tag{6.12a}$$

$$\alpha_2 = \frac{1}{D}\left(-g_1\Lambda_{12} + g_2\Lambda_{11}\right) \ , \tag{6.12b}$$

see [66]. D is the determinate

$$D = \Lambda_{11}\Lambda_{22} - \Lambda_{12}^2 \ . \tag{6.13}$$

This leads to

$$(\Lambda_{11}, \Lambda_{12}, \Lambda_{22}) = \sum_{i=1}^{n} \frac{(1, z_i, z_i^2)}{\tilde{\sigma}_i^2} \tag{6.14a}$$

$$(g_1, g_2) = \sum_{i=1}^{n} \frac{y_i(1, z_i)}{\tilde{\sigma}_i^2} \tag{6.14b}$$

where $\tilde{\sigma} := \tilde{\sigma}(y_i)$ is the spatial resolution of each hit.

For fast track reconstruction we assume that $\tilde{\sigma}$ is constant which leads to

$$\alpha_1 = \frac{g_1\Lambda_{22} - g_2\Lambda_{12}}{\Lambda_{11}\Lambda_{22} - \Lambda_{12}^2} = \frac{\sum_i y_i \sum_i z_i^2 - \sum_i y_i z_i \sum_i z_i}{n\sum_i z_i^2 - \sum_i z_i \sum_i z_i} \tag{6.15a}$$

$$\alpha_2 = \frac{-g_1\Lambda_{12} + g_2\Lambda_{11}}{\Lambda_{11}\Lambda_{22} - \Lambda_{12}^2} = \frac{n\sum_i y_i z_i - \sum_i y_i \sum_i z_i}{n\sum_i z_i^2 - \sum_i z_i \sum_i z_i} \tag{6.15b}$$

and a $\chi^2_{p.d.o.f.}$, of

$$\chi^2_{p.d.o.f.} = \frac{1}{n-2}\frac{1}{\tilde{\sigma}^2}\sum_{i=1}^{n}\left(y_i - \alpha_1 - \alpha_2 z_i\right)^2 . \tag{6.16}$$

Calculating the sums $\sum_i y_i$, $\sum_i z_i$, $\sum_i z_i^2$ and $\sum_i y_i z_i$ and combining them according to Eqs. 6.15 the determination of α_1 and α_2 can be processed using summation, multiplications and only two divisions.

The following description follows the schematic overview of the linear fit algorithm shown in Fig. 6.26.

The pattern recognition described before can result in several track candidates with the same peak height. Therefore the following track reconstruction implementation is designed to process multiple track fits.

1. Before starting the actual calculation, the core registers have to be prepared.
2. Then the track reconstruction is processed for each result:
   a) The buffer data for the corresponding bin is loaded.
   b) Each hit is processed separately.
      i. The hit information is loaded.

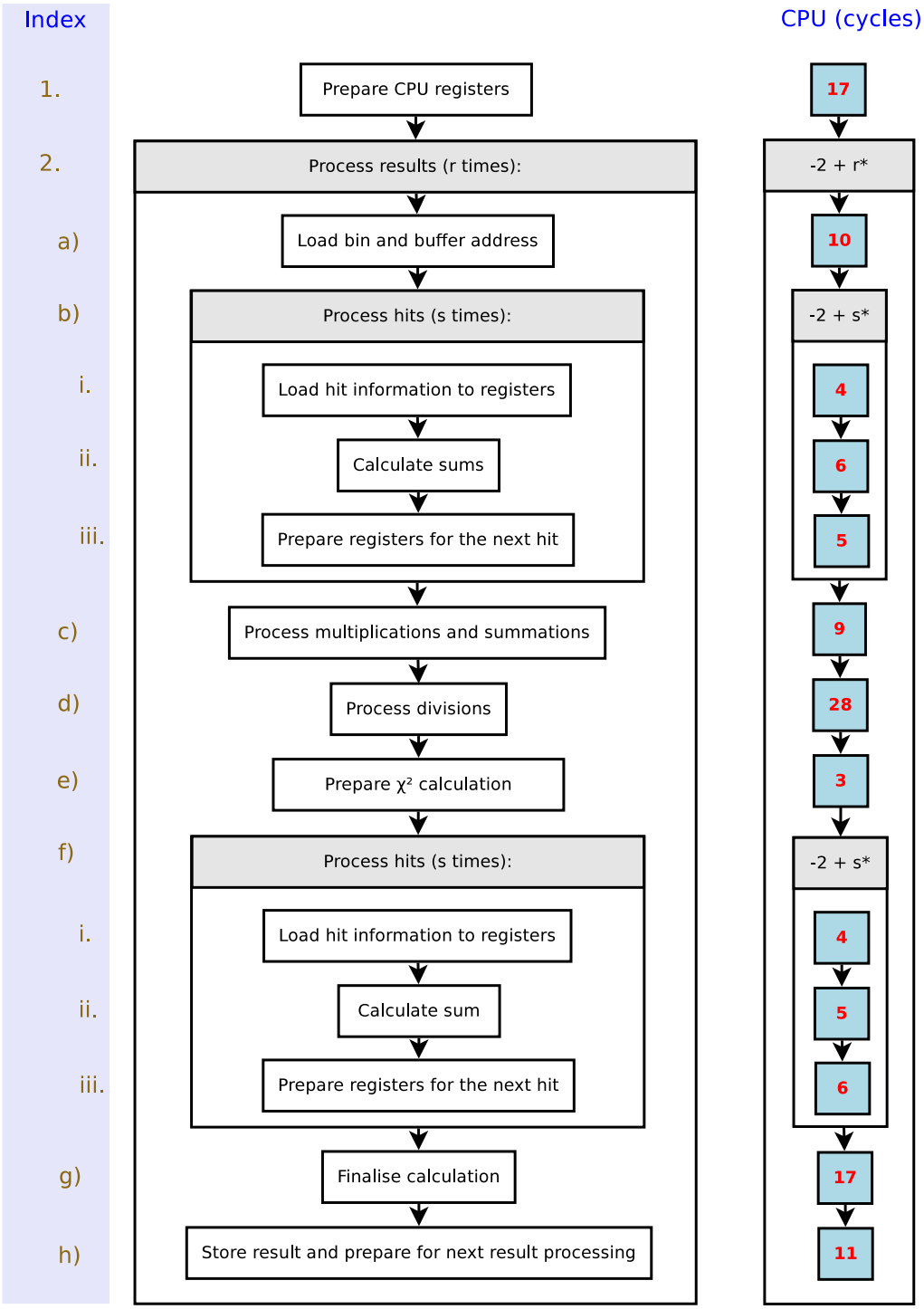


Figure 6.26.: Schematic overview of the fast track fit process with expected processing time in clock cycles of the sub processes. s indicates the number of hits to be processed, r the number of tracks to fit. The clock cycles are calculated for an ARM Cortex-M4F with a memory wait time of 0.

ii. The summands in to Eqs. 6.15 are calculated and added to the corresponding sum.

iii. Finally the registers are prepared for processing the next hit.

c) After summation up, the multiplications and the summations of the products are executed.

d) Finally the divisions are executed, leading to the results α_1 and α_2.

e) Now the registers are prepared for $\chi^2_{p.d.o.f.}$ determination.

f) For calculating the $\chi^2_{p.d.o.f.}$ all hits have to be loaded again.

i. The hit information is loaded.

ii. The distance between reconstructed track and hit is calculated and added to the corresponding sum.

iii. The register are prepared for processing the next hit.

g) Now the $\chi^2_{p.d.o.f.}$ can be calculated.

h) Finally, the results are stored in memory.

The calculation of α_1, α_2 and $\chi^2_{p.d.o.f.}$ implemented in an ARM Cortex-M4 micro-processor takes

$$t_3 = [15 + r \cdot (74 + 30 \cdot s)] \cdot \tau_2 \tag{6.17}$$

with r being the number of fits to process and s being the hits on each track.

Obviously, t_3 is mainly influenced by r, the number of tracks to reconstruct. The following table, which shows t_3 for different parameters and a 200 MHz CPU clock ($\tau_2 = 5$ ns), support this fact.

r	s	t_3
1	4	1.05
1	6	1.35
2	4	2.02
2	6	2.62
5	4	4.93
5	6	6.43

6.3.5.6. Timing Performance Estimation

Summing up the durations in the sub-processes described before leads to

$$t_a = (5 + x) \cdot \tau_1 + \left\{87 + \frac{15 \cdot b}{2} + 68 \cdot x + (75 + 30 \cdot s) \cdot r\right\} \cdot \tau_2 \tag{6.18}$$

for using the FPGA part of the SoC just as buffer and

$$t'_a = \left(6 + \frac{\ln b}{\ln 2} + x\right) \cdot \tau_1 + [78 + 44 \cdot x + r \cdot (74 + 30 \cdot s)] \cdot \tau_2 \tag{6.19}$$

for sharing the tasks according to their best possible performance between the FPGA part and the micro-processor-part of the SoC with b as number of bins of the histogram, x as number of hits within the RoI, s as number of hits on the track, r as number of results to fit τ_1 as the duration of one FPGA clock cycle and τ_2 as the duration of one micro-processor clock cycle.

As mentioned before, the processing duration t_a is strongly dominated by the time needed for peak search in the pattern recognition histogram. This time omits for the combined CPU-FPGA implementation, therefore t'_a is considerably smaller.

The following table shows t_a and t'_a for different parameter combination.

b	x	s	r	t_a	t'_a
128	6	4	1	8.31	2.78
128	6	6	1	8.61	3.08
128	12	6	2	11.95	5.70
128	16	6	3	14.61	7.87
256	6	6	3	15.96	5.62
256	24	6	4	23.44	10.94

It points out, that by using the CPU-FPGA combined implementation, the processing time can be halved in respect to the CPU implementation. In reality the parameters are not fixed, thus the performance of the implementation has been tested in simulation with data taken in the GIF, see Section 6.3.4.

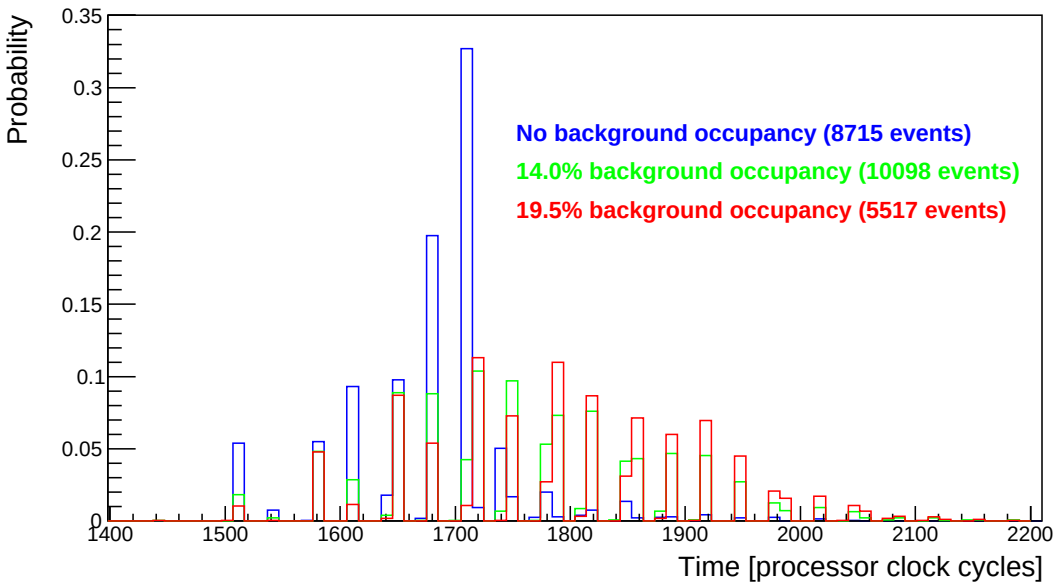
The micro-processor implementation (t_a) has been simulated using *Keil µVision*[6]. The simulation includes all steps between loading the raw data and storing the results[7]. The results of the processing time simulation are shown in Fig. 6.27. Obviously, the mean processing duration in case of radiation is bigger, already in Eq. 6.9 it had been pointed out, that the pattern recognition scales with the number of hits to process. Due to the huge impact of peak-finding, the time distributions are small compared to their absolute values. Comparison between Fig. 6.27a and Fig. 6.27b is hardly possible, as the angle of incidence and thus the mean number of hits on the muon track the differs. In general it can said, that a higher TDC time resolution causes a lower processing duration, due to sharper peaks in the pattern recognition histogram.

6.3.5.7. Conclusions

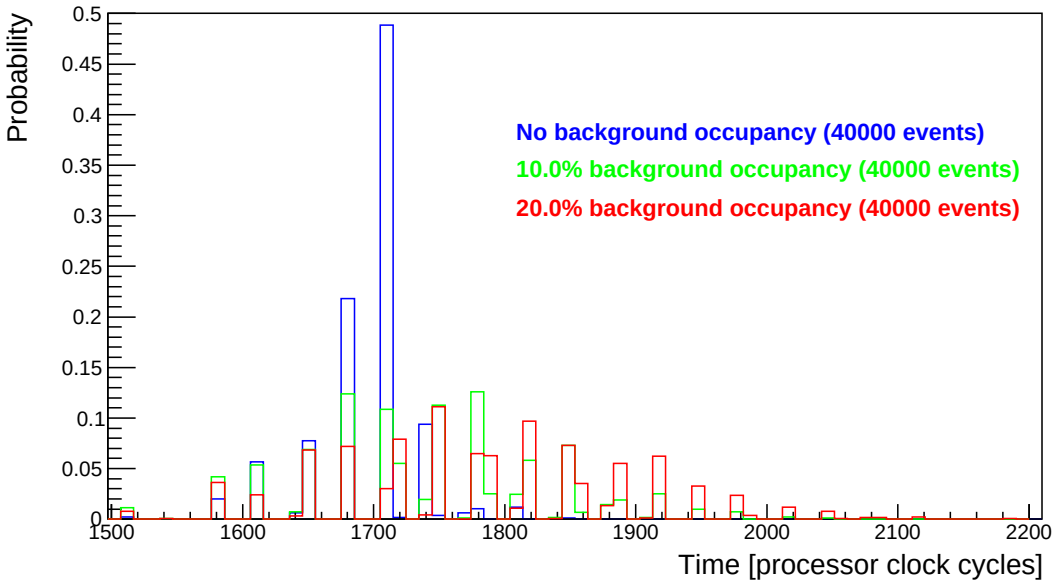
Based on a 200 MHz clock, the slowest track reconstruction of Fig. 6.27a last 10.725 µs. Taking the maximal primary trigger rate into account and demanding that two track reconstructions have to be processed within the latency, see Section 6.3.1, it is possible to do so within the Level-1 muon trigger latency of 60 µs.

[6] `http://www.keil.com/uvision/`

[7] Raw data import and resulting data export has been processed using the Intel Hex Format [89].



(a) 40 MHz TDC, data taken at GIF (see Section 6.3.4).



(b) 80 MHz TDC, simulated data (see Section 6.3.1).

Figure 6.27.: Processing duration of histogram based pattern recognition with track reconstruction for a pure micro-processor based implementation. (a) shows the performance for real data, (b) for simulated data, respectively.

The implementation explained before is based on several prejudicial assumption (e.g. the core registers are at default value at the begin of each track reconstruction task, so several register preparation steps are included). If the micro-processor core is only used for histogram based pattern recognition and track reconstruction, the implementation can be further optimised in respect to processing duration[8].

Instead of an SoC with a ARM Cortex-M4F, an SoC with a ARM Cortex-A9 [90] could be used. Besides the higher CPU clock frequency of up to 1 GHz, the ARM Cortex-A9 contains up to four cores and thus a track reconstruction implementation with parallelisation is possible. An implementation based on such an architecture leads to a dramatic reduction of processing duration, it can be roughly estimated to be faster by a factor of 5 (Factor 5 due to the increased frequency, a factor of 4 due the 4 cores and a factor of one quarter due to the complex architecture and the administration of parallelisation). Furthermore, additional performance can be achieved by making use the FPGA part for specific taks (see discussion in Section 6.3.5.6).

The reduced processing duration due the advanced SoC technology allows for including the MDT hit information in the Level-0 muon trigger (6 μs latency).

6.4. Further Considerations

In addition to the Level-1 muon trigger concept based on a primary trigger discussed before, one can think of two further scenarios: Bunch crossing identification using the MDT and track reconstruction without the knowledge of the muon incidence angle.

6.4.1. Bunch Crossing Identification

The Drift Tube Trigger of the CMS Experiment (for details see [91]) provides stand-alone bunch crossing identification and muon track measurement. The resulting information is then combined with the results of other trigger detector systems, leading to a high redundancy. In the following, the concept of bunch crossing identification with drift-tubes and the possibility for implementation in the ATLAS experiment is discussed.

6.4.1.1. The CMS Drift Tube Trigger

The Drift Tube Trigger is based on Drift Tubes (DT), which are cuboid drift gas detectors with similar functionality as the ATLAS MDT chambers (see Section 4).

It is split in the so-called local trigger which processes the data of a single DT chamber and into the so-called regional trigger which combines the data given by the local trigger.

The local trigger resolves time ambiguities and, therefore, performs bunch-crossing identification by using the so-called mean-timer technique which is described in detail in [92].

[8] Some preparation steps can be processed at start-up once and this leads to a further reduction of several clock cycles.

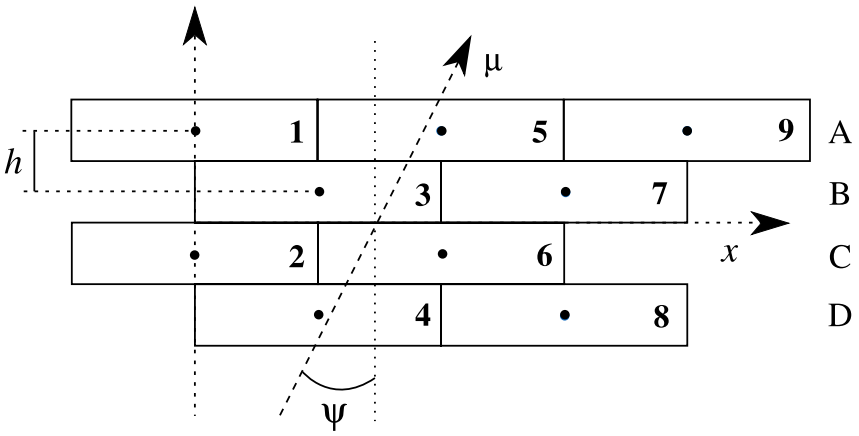


Figure 6.28.: Schematic showing the CMS Muon Drift Tubes channel number allocation where the capital letters represent the four layers and the and h indicates the distance between two layers [93].

This method is based on the fact that the space to drift-time relationship is nearly linear in case of the CMS DT chambers, the particle track is a straight line and the wire position along the track are equidistant. The sum of the drift times of two staggered and adjacent tubes for a non inclined track corresponds to the maximum drift time T_{max}. This principle can be extended to inclined tracks by using a triplet of DT planes and calculating the mean of both possible drift time sums.

Using the channel allocation illustrated in Fig. 6.28 and considering the the layers A, B and C for calculation, the maximum drift time T_{max} is given by the relation

$$T_{max} = \frac{T_A + 2 \cdot T_B + T_C}{2} \ , \tag{6.20}$$

where T_A is the drift time of DT 5, T_B of DT 3 and T_C of DT 6. In order to obtain the time of the muon hit, the drift-times have to be adjusted, because the calculation gives T_{max} only for the right drift-times.

For bunch and track identification of the DT local trigger the mean-timer technique is computed in parallel for several track patter hypothesis, see Fig. 6.28, for each bunch crossing cycle using the hit arrival time with 12.5 ns resolution. The use of four DT layers gives redundancy and background capability to the bunch crossing identification system.

6.4.1.2. Bunch Crossing Identification with MDT chambers

In order to use the CMS Drift Tube Trigger mean-timer technique for the ATLAS MDT chambers, instead of the drift-times the drift-radii have to be used. Due to the MDT chamber geometry, the mean-timer technique leads to ambiguous results for an incidence angle of 30°, see Fig. 6.29.

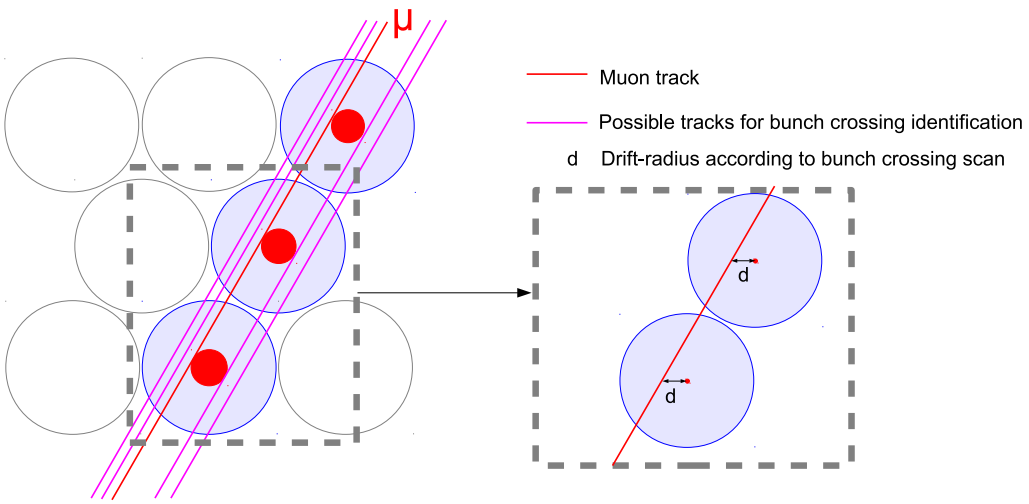


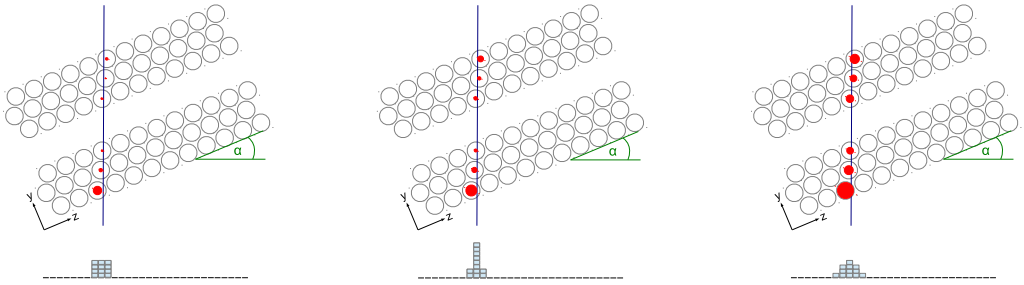
Figure 6.29.: MDT chamber with muon track (red) and possible tracks determined with the mean-timer technique. This schematic shows that due to geometry of the MDT chamber, the mean-timer technique can not be used for bunch crossing identification.

Thus, the histogram based pattern recognition already discussed in Section 6.3.2.1 has been proposed for bunch crossing identification [74]. As shown in Fig. 6.30a-6.30c, a wrong assumed trigger time (bunch crossing) leads to a widening of the hit distribution in the pattern recognition histogram, if the muon incident angle is known.

Similar to the mean-timer technique, the bunch crossing identification algorithm identifies the correct bunch crossing by modifying the drift-times and searches for peaks above a certain threshold.

Based on the simulation discussed in Section 6.3.3.1, the performance of the histogram based bunch crossing identification has been studied. Fig. 6.31 shows the probability for an event exceeding a certain threshold in the histogram (2 mm bin width) depending on the difference between muon passing time and the assumed bunch crossing in clock cycles. This probability can be interpreted as detection efficiency.

Besides the double peak structure caused by the two-fold ambiguity of the drift-radii, the simulation results for a threshold of 3 hits show a very high probability for identification of the wrong bunch crossing. Thus, a higher threshold has to be set, but it has to be taken into account that the efficiency is decreasing with the threshold. Despite the fact that even for a threshold of 4 and 5, the fake probability is too high for being actual used in the ATLAS experiment, the threshold of 4 hits seems to be a good choice to be the basis for further simulations.



(a) Preceding BC. (b) Correct BC. (c) Following BC.

Figure 6.30.: Principle of histogram based bunch crossing identification. For the preceding and the following bunch crossing (BC) the distribution is widened, for the correct BC the distribution shows a sharp peak.

So far, the simulation has been based on the assumption of knowing the muon incidence angle. Taking into account a spread of the muon incidence angle, the detection efficiency for the correct bunch crossing depending on the uncorrelated background occupancy is shown in Fig. 6.32. This plot indicates that the detection efficiency strongly decreases with spread of the incidence angle and background.

The need for bunch crossing identification with MDT chambers originate from the idea of avoiding a primary trigger source. So, the muon incidence angle is not known precisely and has to be estimated according to the hit position in the MDT chamber.

Summarising the simulation results shown in Fig. 6.31 and Fig. 6.32, the histogram based bunch crossing identification can not be considered to be implemented in ATLAS, due to the high fake probability and low detection efficiency.

Furthermore, due to calculation of the histogram for each bunch crossing to test, the algorithm needs a lot of computing power and a possible implementation leads to major hardware modification.

6.4.2. Hough transform based pattern recognition

The histogram based pattern recognition discussed in Section 6.3 is based on an assumed muon incidence angle. Taking into account, that this algorithm is a special-case of the so-called Hough transform, which has been developed as method for detecting complex patterns of points in binary image data and has been patented in 1962 [94], an extension to determine the track angle can be considered.

The Hough transform for straight line recognition [95] is based on equation of a straight line

$$x \cdot \cos\alpha + y \cdot \sin\alpha = d \ , \tag{6.21}$$

where α is the angle of the line and d is the minimal distance between line and origin. When $0 < \alpha < \pi$, the parameter of the line are unique.

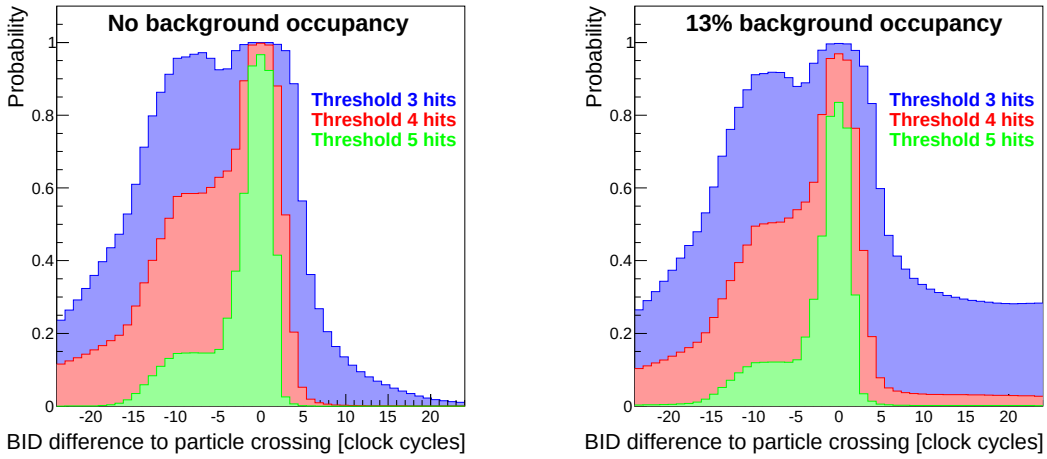


Figure 6.31.: Probability for an event exceeding a certain threshold in the histogram (2 mm bin width) depending on the difference between muon passing time and the assumed bunch crossing in clock cycles. The distribution is based on a 400000 event Monte-Carlo simulation with histogram based bunch crossing identification (2 mm spatial bin width, 12.5 ns time resolution), no angular spread and the parameters defined in Section 6.3.1.

Supposing a set $(x_1, y_1), ..., (x_n, y_n)$ of n points and the need of finding straight lines in them, the points (x_i, y_i) can be transformed into sinusoidal curves in the $\alpha - d$ plane defined by

$$d = x_i \cdot \cos\alpha + y_i \cdot \sin\alpha \ . \tag{6.22}$$

By calculating this equation for all points (x_i, y_i), using α as free parameter within its limits and filling the resulting d into a two-dimensional histogram, the peaks in the histogram represent the straight lines where the points lay on.

In order to use this algorithm for MDT fast track reconstruction, both possible hits positions (drift-radius r_{drift}, twofold ambiguity) have to be added to the two-dimensional histogram, leading to

$$d^{\pm} = x_i \cdot \cos\alpha + y_i \cdot \sin\alpha \pm r_{drift} \ . \tag{6.23}$$

When α is fixed, this algorithm results in the histogram based pattern recognition, otherwise it is called Hough transform based pattern recognition.

Due to the angular dimension, the Hough based pattern recognition has one additional parameter, the angular bin width, in respect to the histogram based pattern recognition.

Based on the simulation framework described in Section 6.3.3.1, the parameters of Section 6.3.1 and the results of the simulation of the histogram based pattern recognition (2 mm spatial bin width, 4 hits threshold), the performance of the Hough transformed track reconstruction has been studied.

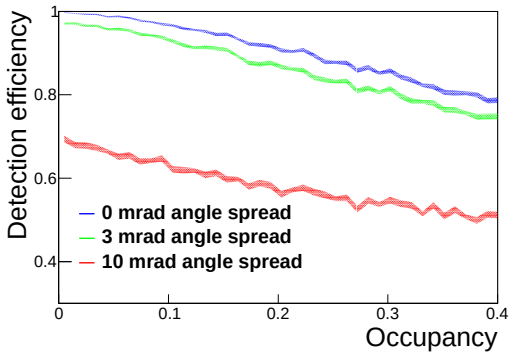


Figure 6.32.: Correct bunch crossing identification efficiency of the histogram based algorithm in dependency of uncorrelated background occupancy with different incidence angle spread. The plot is based on a Monte-Carlo simulation with 400000 events.

Fig. 6.33a and Fig. 6.33b show the obtained spatial and angular resolution for different uncorrelated background occupancies depending of the angular bin width. While the spatial resolution is constant for an angular bin width smaller than 7 mrad, the angular resolution has a minimum at 7 mrad. Due to the two-fold ambiguity of the drift-radii and the effect of δ-electrons, the probability finding a wrong peak in the 2-dimensional histogram is decreasing with the angular bin width.

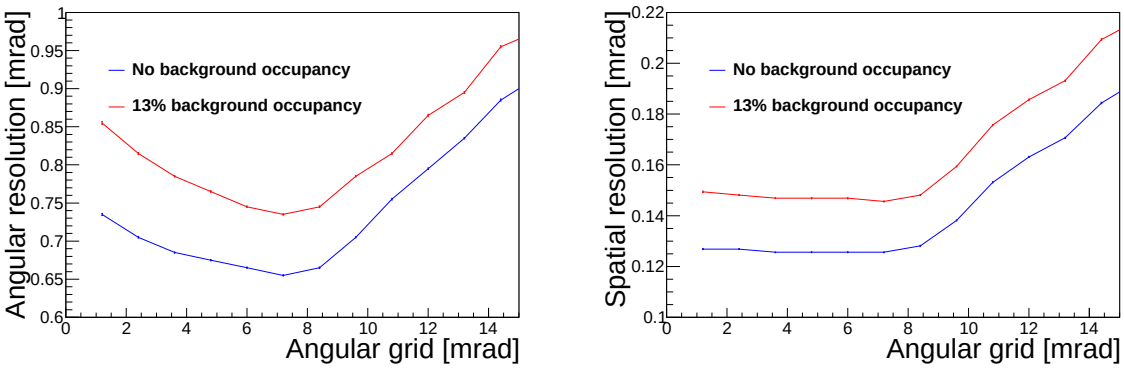
This explanation is supported by the probability of track candidates depending on the angular bin width shown in Fig. 6.34b. While the probability for many track candidates is decreasing with the angular bin width, the probability for exact one track candidate shows a maximum for an angular bin width of 7 mrad. The detection efficiency and subsequently the 3-σ efficiency depending on the angular bin width (see Fig. 6.34a) are constant until a certain value and then decrease with increasing angular bin width, because the probability for smeared-out peaks is increasing with the bin width size (see Fig. 6.6b).

Summarising Fig. 6.33-6.34, an angular bin width of 7 mrad is a good choice.

In order to reduce the rate of poorly reconstructed events, the $\chi^2_{p.d.o.f.}$ as measure of quality can be used, see Section 6.3.3.2. In Fig. 6.35 the distribution of the difference between reconstructed angle α_{rec} and true angle α_{true} with and without the requirement of a maximum $\chi^2_{p.d.o.f.} < 1.9$ is shown. This requirement is chosen to obtain less than 2% within the category *poor*[9] for 13% background occupancy. Using the measure of quality reduces the ratio of events within the category *poor* from 8% to 2%, but also the events within the category *good* are reduced from 89.4% to 83.3%.

The Hough transform based track reconstruction shows a poor performance in respect to the histogram based track reconstruction (see Fig. 6.12), whereas it is obvious that the Hough transform based pattern recognition is more sensitive to uncorrelated background occupancy.

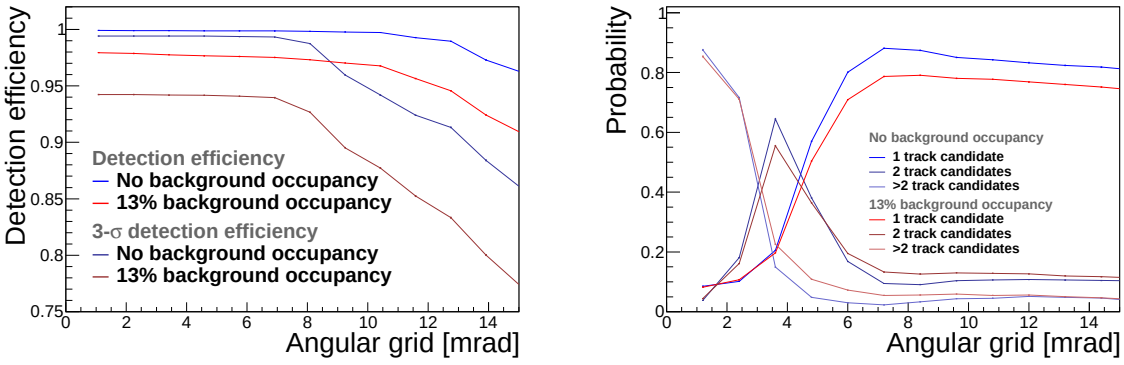
[9] $|\alpha_{rec} - \alpha_{true}| < 3mrad$, see Section 6.3.3.2



(a) Angular resolution.

(b) Spatial resolution.

Figure 6.33.: Angular and spatial resolution of the Hough transform based pattern recognition with track reconstruction in dependency of the angular bin width for different uncorrelated background occupancies. The plots are based on a simulation of the EML 1 chamber 400000 Monte-Carlo events for each occupancy.



(a) Detection and angular 3-σ efficiency.

(b) Ratio of number of track candidates.

Figure 6.34.: Detection, angular 3-σ efficiency and ratio of number of track candidates of the Hough transform based pattern recognition in dependency of the angular bin width for different uncorrelated background occupancies. The plots are based on a simulation of the EML 1 chamber, see Section 6.3.1, with 400000 Monte-Carlo events for each occupancy.

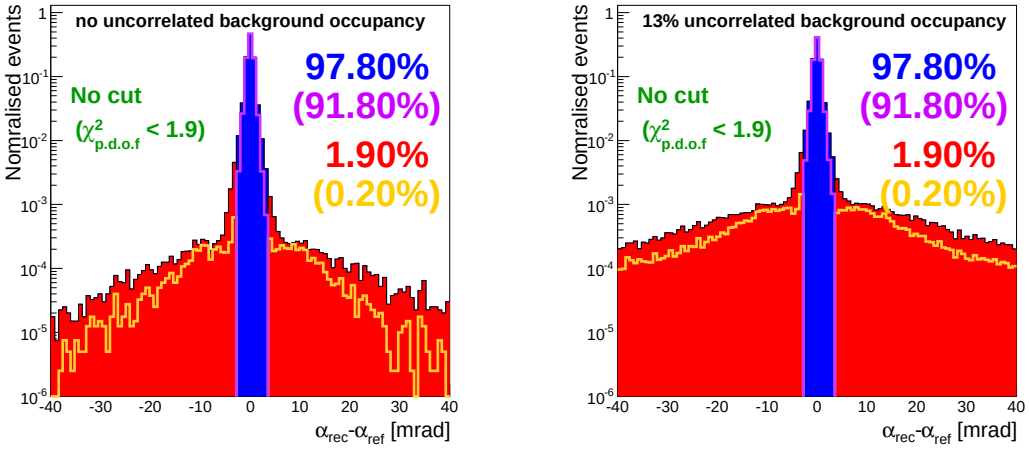


Figure 6.35.: Distribution of the difference between the true angle α_{true} and the reconstructed angle α_{rec} of the track with and without measure of quality ($\chi^2_{p.d.o.f.}$). The tracks, which are based on an 400000 event Monte-Carlo simulation, are reconstructed using the hough transform based pattern recognition with track reconstruction (2 mm spatial bin width, 3 mrad angular bin width, 4 hits threshold). In case of several results of the pattern recognition, the one with the lowest $\chi^2_{p.d.o.f.}$ is used.

Furthermore, the Hough transform based pattern recognition needs way more computing power and results in more track candidates, because it can be seen as a parallelisation of the histogram based pattern recognition. Taking into account the timing performance results discussed in Section 6.3.5, it seems impossible to implement the Hough transform based pattern recognition neither in the L0, nor in Level-1 muon trigger.

6.5. Conclusion and Outlook

In order to fully exploit the physics potential of the HL-LHC, the selectivity of the ATLAS Muon Trigger system must be improved. Thus, it has been proposed to include the MDT chambers of the ATLAS Muon Spectrometer in the ATLAS muon trigger leading to the necessity of an additional fast read-out (FRO) path for the MDT chambers and a fast track reconstruction algorithm which can be conducted within the Level-0 latency of 6 μs.

Simulations and an experiment at the CERN Gamma Irradiation Facility using cosmic muons have shown that the histogram based pattern recognition with track reconstruction fulfils the requirements and that the implementation of the additional fast read-out is possible.

Due to initial simplifications, the FRO did not contain hit buffering leading a effective dead time of 1500 ns and the fast track reconstruction algorithm hardware implementation was simulated. So, the next development steps are the implementation of hit buffering and porting the fast track reconstruction algorithm to a hardware demonstrator set-up.

Then, this new hardware has to operated at a γ irradiated MDT chamber at a high-energy muon beam[10].

[10]Gamma Irradiation Facility GIF++ at CERN [69].

Summary

In order to measure the properties of the Higgs-Boson with high precision and search for new phenomena beyond the Standard Model, the centre-of-mass energy of the LHC will be raised to 13 TeV in 2015 and the luminosity will be increased in several steps over the next ten years leading to the necessity to upgrade the LHC experiments to cope with the increased data and background rates up to 14 $\frac{\text{kHz}}{\text{cm}^2}$ in the Muon Spectrometer.

The precision tracking detectors of the ATLAS Muon Spectrometer are mainly Monitored Drift Tube (MDT) chambers consisting of layers of aluminium drift tubes with 30 mm diameter. The MDT chambers can cope with background rates up to 500 $\frac{\text{Hz}}{\text{cm}^2}$ due to occupancies above 30% and space charge effects deteriorating the spatial resolution. Hence, new muon drift-tube detectors with smaller tube diameter of 15 mm (sMDT chambers) and a single-tube spatial resolution without irradiation of 106 μm have been developed. Besides the four times shorter maximum drift-time of 185 ns compared to MDT tubes allowing for operation with much shorter electronics dead time settings, and occupancy reduced by a factor of 8, the reduced tube diameter improves the spatial resolution by an order of magnitude due to the elimination of space charge effects.

Previous measurements showed that the sMDT chamber performance is limited by the current read-out electronics taken from the ATLAS MDT chambers, using bipolar shaping in order to prevent baseline shift at high counting rates. With increasing rate muon signals tend to pile up on the large and long undershoots of preceding background pulses which leads to an effective amplitude reduction and jitter in the threshold crossing time and, therefore, to a degradation of the spatial resolution and muon detection efficiency. By suppressing the undershoot and, therefore, the pile-up effects by baseline restoration methods, the high rate performance of sMDT tubes can be increased substantially.

In order to investigate the performance of sMDT tubes with read-out electronics with baseline restoration, a discrete bipolar shaping circuit with optional baseline restoration has been developed and used for testing an sMDT chamber under irradiation with electrons from ^{90}Sr sources with activities between 1.5 and 24 MBq leading to electron hit rates up to 2 MHz. The measurements and corresponding simulation results show that even by only optimising the bipolar shaping parameters without use of baseline restoration, the resolution and efficiency of sMDT tubes at high rates is considerably increased. Baseline restoration further improves the high rate performance of sMDT chambers. The single-tube spatial resolution is improved from 180 μm for the ATLAS MDT read-out electronics to 120 μm at 2 MHz electron background rate.

At HL-LHC, the proton collisions and, therefore, the trigger rates are expected to be about 10 times higher than at the LHC design luminosity of $10^{34}\text{cm}^{-2}\text{s}^{-1}$. In order to

fully exploit the physics potential of the HL-LHC, the selectivity of the ATLAS Level-1 muon Trigger has to be improved by increasing the momentum and, therefore, the spatial resolution of the trigger electronics. In particular in the end-caps, the angular resolution of the inner and middle chamber layer has to be improved from 3 to 1 mrad. The only practical solution is to include the MDT precision tracking chambers in the trigger leading to the necessity of an additional fast read-out path for the MDT chambers and a fast track reconstruction algorithm which can take the decision within the latency of Level-0 of the muon trigger system of 6 μs.

Simulations and test with cosmic ray muons at the CERN Gamma Irradiation Facility (GIF) of a demonstrator set-up with an prototype fast read-out path showed that a histogram-based track reconstruction algorithm is suitable for fast track reconstruction. At the highest expected MDT background occupancy at HL-LHC of 13%, the muon track finding efficiency of the algorithm is 99%. The algorithm has been implemented on the ARM Cortex-M4F architecture using the ARM assembly language. Simulations of the program with data taken at the GIF show that the track reconstruction can be performed in less than 11 μs. With a faster processor multi-core architecture, e.g. ARM Cortex-A9, the processing time can be reduced to well below the available 6 μs.

A. Appendix

A.1. Parametrisation of the Space-Drift-Time Relationship

According to [96] the conditional probability distribution $P(t|r)$ with

$$\int_{-\infty}^{\infty} dt P(t|r) = 1 \text{ (for all r} \in [0{,}15 \text{ mm}]) \tag{A.1}$$

of an MDT can be parametrised with

$$\begin{aligned} P(t|r) &= \frac{p_1(r)}{p_3(r)} e^{\frac{p_2(r)-t}{p_3(r)} - e^{\frac{p_2(r)-t}{p_3(r)}}} \\ &+ [1 - p_1(r) - p_4(r) \cdot p_2(r)] \cdot \frac{1}{\sqrt{2\pi} p_3(r)} e^{-\frac{[t-p_2(r)]^2}{2[p_3(r)]^2}} \\ &+ p_4(r) \cdot \Theta\left[p_2(r) - t\right] \cdot \Theta(t) \end{aligned} \tag{A.2}$$

with

$$p_1(r) = f_0 e^{-f_1 r} \tag{A.3a}$$

$$p_2(r) = \sum_{i=0}^{7} a_i P_i(u) \tag{A.3b}$$

$$p_3(r) = s_0 e^{-s_1 r} + s_2 + s_3 r + s_4 r^2 + e^{\frac{r-s_5}{s_6}} \tag{A.3c}$$

$$p_4(r) = \sum_{i=0}^{5} d_i P_i(u) \ . \tag{A.3d}$$

The constants f_i, a_i, s_i and d_i are shown in Tab. A.1, the parameters p_2 and p_4 involve Legendre polynomials $P_i(u)$ with $u = 2 \cdot \frac{r}{r_{tube}-1}$.

Parameter	Value
f_i	0.8480 0.5879
a_i	241.7 322.6 103.3 18.42 -6.560 0.3810 1.007 -1.451
s_i	3.041 0.8311 2.485 -0.1250 0.02603 14.72 0.2000
d_i	0.2686e-3 -0.6065e-4 -0.4431e-4 0.1541e-3 -0.3894e-4 0.9484e-4

Table A.1.: Constants for the radial parametrisation shown in Eq. A.3. The f_i is dimensionless, the units of the other components are such that p_2 and p_3 are in ns, p_4 in ns^{-1}.

A.2. Read-Out Electronics for Drift-Tubes

In the following additional information to signal shaping and their technical realisation is given. After the theoretical description of simple uni- and bipolar shaping circuits (δ-response see Fig. A.2), RC filters and an operational amplifier based differentiation circuit are discussed.

A.2.1. Unipolar and Bipolar Shaping Scheme

In Fig. A.2 the circuits of the unipolar and bipolar shaper used to obtain the δ-response shown in Fig. 5.1 are illustrated. While the unipolar circuit consists of $n+1$ identical RC filters which are separated by ideal voltage buffers, the bipolar circuit consists of n identical RC filters and a single CR filter.

The δ-response (voltage $V(t)$ for a δ current input $I(t)$) can be calculated with the inverse Fourier transform of product of $I(t)$ and the transfer function $W(\omega)$ of the system[1]

$$V(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} d\omega \; I(t) \cdot W(\omega) \cdot e^{i\omega t} = \frac{1}{2\pi} \int_{-\infty}^{\infty} d\omega \; \cdot W(\omega) \cdot e^{i\omega t} \; . \tag{A.4}$$

Obviously, the unipolar and bipolar transfer function W_{uni} and W_{bi} are

$$W_{uni} = kA \frac{1}{(1+i\omega\tau)^{n+1}} \tag{A.5a}$$

$$W_{bi} = kA \frac{\omega\tau}{(1+i\omega\tau)^{n+1}} \; , \tag{A.5b}$$

where $\tau = RC$ and $A = \prod G_i$. For the inverse Fourier-transform the relations [53]

$$f(t) = \frac{1}{(n-1)!} t^{n-1} e^{-at} \theta(t) \;\; \rightarrow \;\; F(t) = \frac{1}{(a+i\omega)^n} \; (a > 0, n = 1, 2, 3, ...) \tag{A.6a}$$

[1] The Fourier transform of $\delta(t)$ is 1.

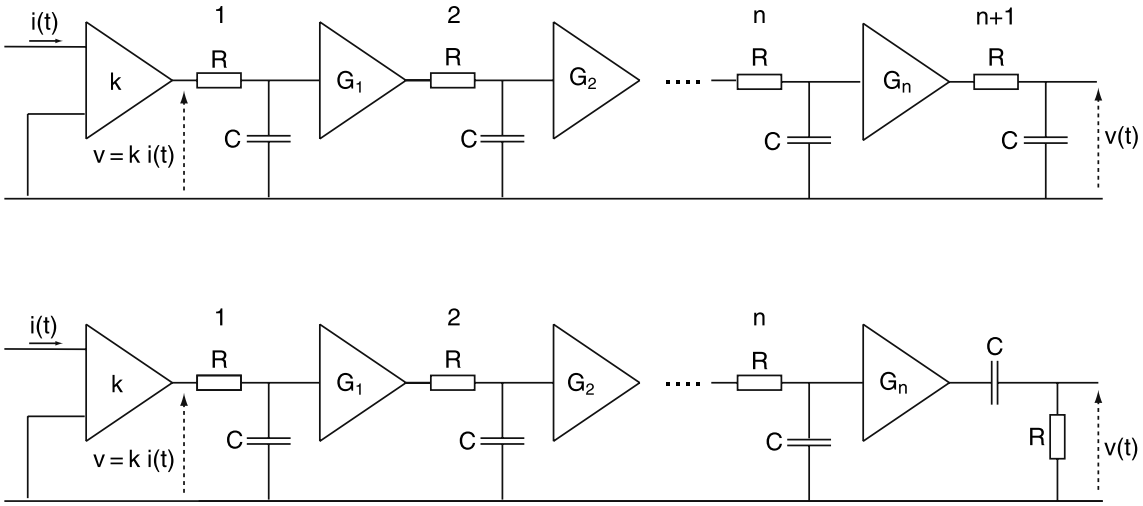


Figure A.1.: Circuits of unipolar (top) and bipolar (bottom) shaper used to obtain the δ-response shown in Fig. A.2 [32].

$$f(t) = \left(\frac{d}{dt}\right)^n g(t) \;\rightarrow\; F(t) = (i\omega)^n G(\omega) \tag{A.6b}$$

are applied, where $f(t)$ and $g(t)$ are functions in the time domain and $F(t)$ and $G(t)$ there Fourier-transformed, respectively. It follows[2]

$$V_{uni}(t) = \frac{k \cdot A}{\tau^{n+1}} \, \frac{1}{n!} \, t^n \, e^{-\frac{t}{\tau}} \, \theta(t) \tag{A.7a}$$

$$V_{bi}(t) = \frac{d}{dt} V_{uni} = \frac{k \cdot A}{\tau^{n+1}} \, \frac{1}{n!} \, (n - \frac{t}{\tau}) \, t^{n-1} \, e^{-\frac{t}{\tau}} \tag{A.7b}$$

A.2.2. The RC-Circuit

The complex resistance Z_{RC} of the RC-circuits (resistance between In and ground) shown in Fig. A.2a and Fig. A.2b is

$$Z_{RC} = R + \frac{1}{i\omega C} \tag{A.8}$$

and hence

$$I = I_C = I_R = U_{In} \cdot \frac{1}{Z_{RC}} = U_{In} \cdot \frac{1}{R + \frac{1}{i\omega C}} \; . \tag{A.9}$$

Setting the constraint $\omega \ll \frac{1}{RC}$ (the current is dominated by the resistance of the capacitor, the impact of R is negligible) leads to

$$I = U_{In} \cdot i\omega C \; . \tag{A.10}$$

[2] $\theta(t)$ is used as domain of definition and, therefore, not differentiated.

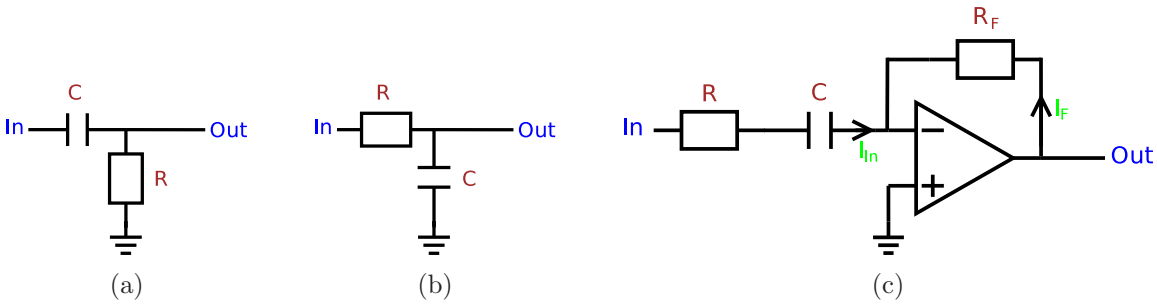


Figure A.2.: (a) CR high-pass filter, (b) RC low-pass filter and (c) circuit for differentiation based on an inverting amplifier (if R is small, otherwise the circuit shows an additional shaping behaviour).

For the circuit shown in Fig. A.2a, this leads to a voltage at Out U_{Out} (time-domain)

$$U_{Out} = R \cdot I = RC \cdot \dot{U}_{In} \ . \tag{A.11}$$

So, for low frequencies, the CR-circuit is differentiating the signal, while obviously for high frequencies the circuit becomes transparent.

In case of $\omega \gg \frac{1}{RC}$ (the current is dominated by the resistor, the capacitor is transparent) Ohm's law is obtained

$$I = \frac{U_{In}}{R} \ . \tag{A.12}$$

For the circuit shown in Fig. A.2b, the voltage at Out U_{Out} is

$$U_{Out} = \frac{Q}{C} = \frac{1}{C} \int_0^t I dt = \frac{1}{RC} \int_0^t U_{In} dt \ , \tag{A.13}$$

where Q is the charge of the capacitor. So, for high frequencies, the RC-circuit is integrating the signal, while obviously for low frequencies the circuit becomes transparent.

A.2.3. Operational Amplifier Based Differentiator

A circuit for differentiation without frequency dependency based on an inverting amplifier circuit is shown in Fig. A.2c. The voltage between the input of the amplifier is zero, thus the voltage at In U_{In} is

$$U_{In} = U_R + U_C = R \cdot I_{In} + \frac{Q_C}{C} \ , \tag{A.14}$$

where U_R is the voltage on the resistor R, U_C is the voltage on the capacitor C, I the current flowing into the circuit and Q the charge on C. If functions are identical, there derivatives are identical too

$$\dot{U}_{In} = R \cdot \dot{I}_{In} + \frac{I_{In}}{C} \tag{A.15}$$

Due to the infinite input resistance of the operational amplifier, the current I_{In} has to be equal to the current flowing over R_F

$$I_{In} = I_F = -R_F \cdot U_{Out} \ , \tag{A.16}$$

where V_{Out} is the voltage at Out. Applying this relation to Eq. A.15 leads to

$$CR \cdot \dot{U}_{Out} + U_{Out} = -CR_F \cdot \dot{U}_{In} \ . \tag{A.17}$$

Eq. A.17 shows that the voltage at *Out* is the derivative of the voltage at *In* plus an additional shaping feature caused by R. In case of $R = 0$ the voltage at Out U_{out} is

$$U_{Out} = -R_F \cdot C \cdot \dot{U}_{In} \ . \tag{A.18}$$

The resistor R is necessary to avoid infinite gain for high frequencies and, hence, suppress noise. In order to minimise its impact on the behaviour of the circuit, its value should be small. Nevertheless, it can be also used for additional shaping of the input pulse (see Section 5.3.1.2).

Describing the circuit of Fig. A.2c in Fourier space ($I_{in} = I_F$) leads to

$$U_{Out} = -\frac{i\omega CR_F}{1 + i\omega CR} \dot{U}_{In} \ . \tag{A.19}$$

In case of limited bandwidth of the operational amplifier, Eq. A.19 becomes

$$U_{Out} = -\frac{i\omega CR_F}{1 + i\omega CR} A(\omega) U_{In} \ , \tag{A.20}$$

where $A(\omega)$ $(0 < A(\omega) < 1)$ is a continuous function describing the attenuation depending on the frequency.

The area below a shaped signal can be calculated by transforming Eq. A.20 into the time-domain and integrating over the time. Using the inverse Fourier-transform the area S is

$$S = -\frac{1}{2\pi} \int_{-\infty}^{\infty} dt \int_{-\infty}^{\infty} d\omega \ e^{i\omega t} \cdot \frac{i\omega CR_F}{1 + i\omega CR} \cdot A(\omega) \cdot U_{In} \ . \tag{A.21}$$

Solving the integral over the time with the relation

$$\delta(\omega) = \int_{-\infty}^{\infty} dt \ e^{i\omega t} \tag{A.22}$$

leads to

$$S = -\frac{1}{2\pi} \int_{-\infty}^{\infty} d\omega \ \delta(\omega) \cdot \frac{i\omega CR_F}{1 + i\omega CR} \cdot A(\omega) \cdot U_{In} \ . \tag{A.23}$$

If $A(\omega) = 1$ or linear decreasing, $I = 0$. In order to gain $I \neq 0$, a limited amplifier bandwidth is necessary with

$$A(\omega) \sim \frac{1}{\omega} \text{ for a band } \omega_0 < \omega < \omega_1 \ . \tag{A.24}$$

Assuming a finite input resistance of the operational amplifier[3], the input bias current I_B is (see Fig. A.2c)

$$I_B = I_F + I_{In} = \frac{1}{R_F} U_{out} + \frac{i\omega C}{1 + i\omega CR} U_{In} \ . \tag{A.25}$$

It follows

$$U_{out} = -R_F \cdot \left(\frac{i\omega C}{1 + i\omega CR} U_{In} - I_B \right) \ . \tag{A.26}$$

Applying Eq. A.26 in Eq. A.23 leads to

$$A(\omega) = 1 - \frac{1 + i\omega CR}{i\omega C} \frac{1}{U_{In}} \cdot I_B \ . \tag{A.27}$$

Obviously, $A(\omega)$ shows the behaviour of a high-pass. Strategies in order to minimise I_B are discussed in [97].

[3]The current due to the finite input impedance of an operational amplifier is called input bias current (see [97]).

A.2.4. The ASBC

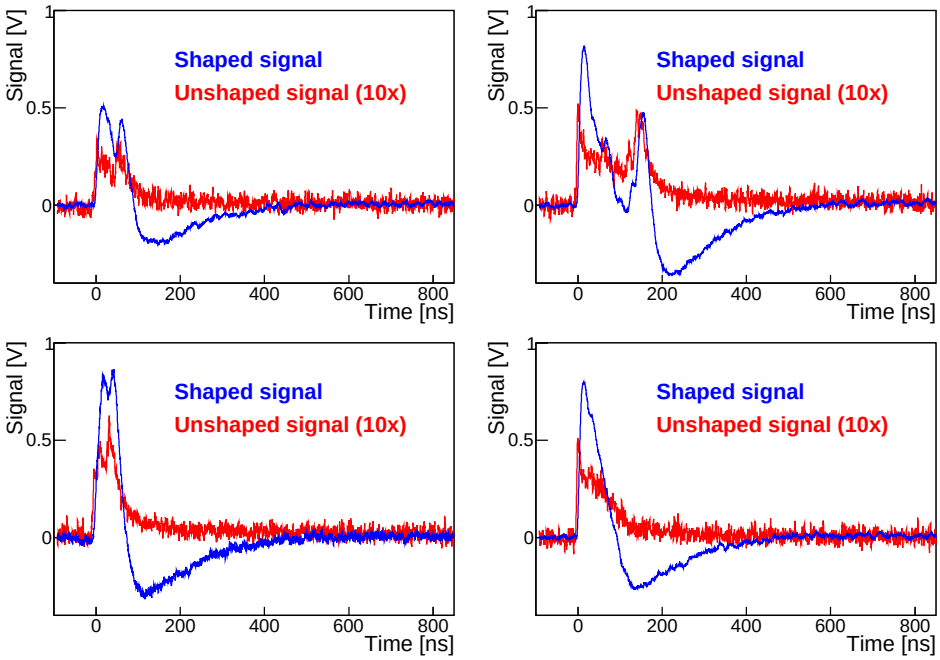
In Tab. A.2 the values of the parts used for the ASBC (the circuits are shown in Fig. 5.8, Fig. 5.10 and Fig. 5.13a are listed.

Part	**Value**
R_1	39 Ω
R_2	10 Ω
R_3	560 Ω
R_4	820 Ω
R_5	6k8 Ω
C_1	100 nF
C_2	220 pF
C_3	100 nF
R_6	27 Ω
R_7	18 Ω
R_8	560 Ω
R_9	13k3 Ω
C_4	220p pF
R_{10}	20k Ω
R_{11}	22k Ω
C_5	30 pF
C_6	100n nF
L_1	50 mH

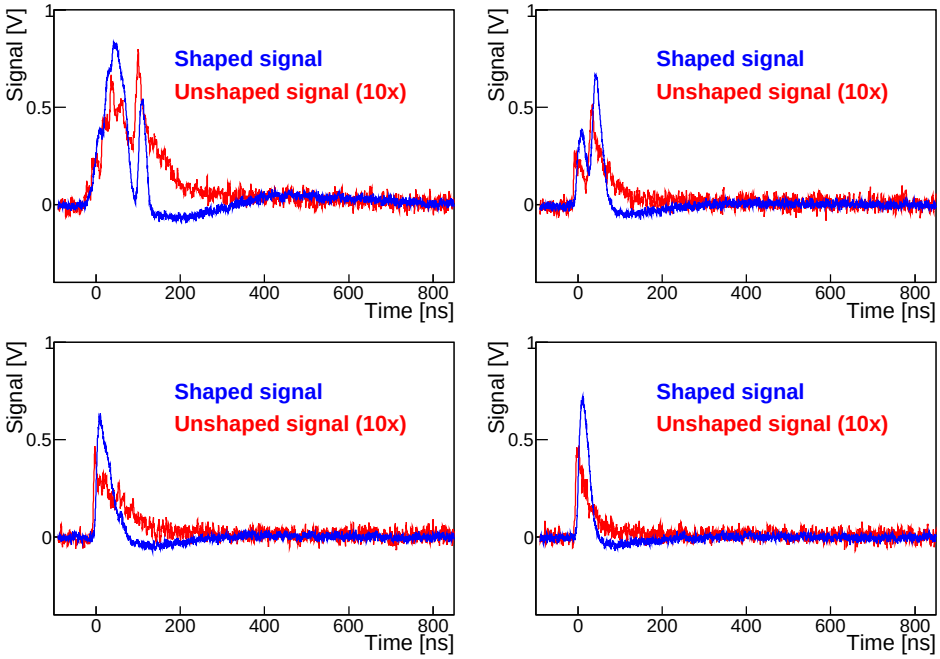
Table A.2.: Part values of the ASBC (see Section 5.3).

In Fig. A.3-A.5 typical muon, electron and γ pulses of an sMDT tube measured with the ASBC electronics with and without baseline restoration are shown.

In the following, the magnitude and phase of the complex gain of filter stage 1 and 2 are calculated.

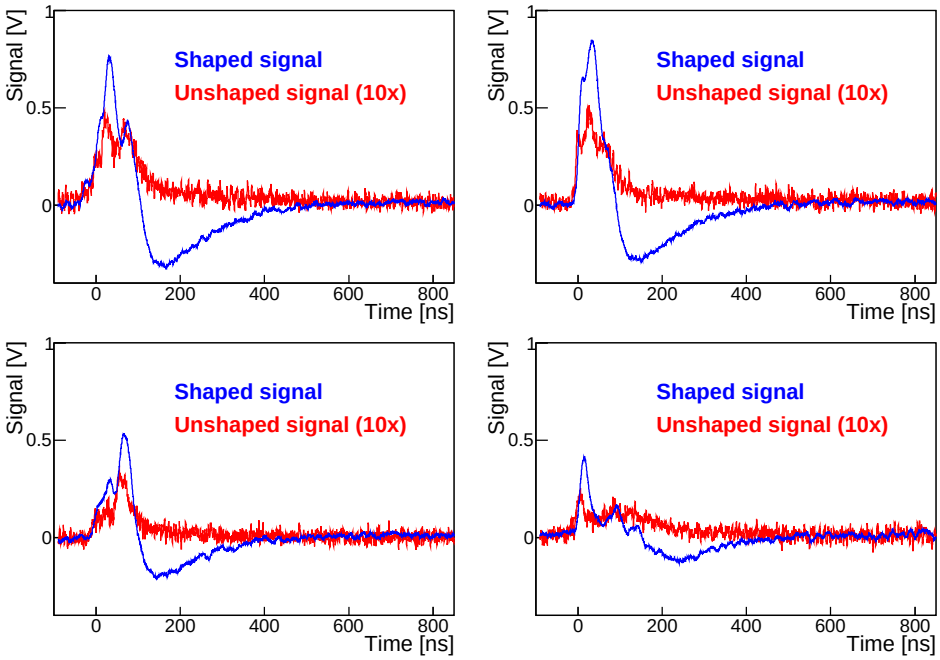


(a) Muon response without baseline restoration.

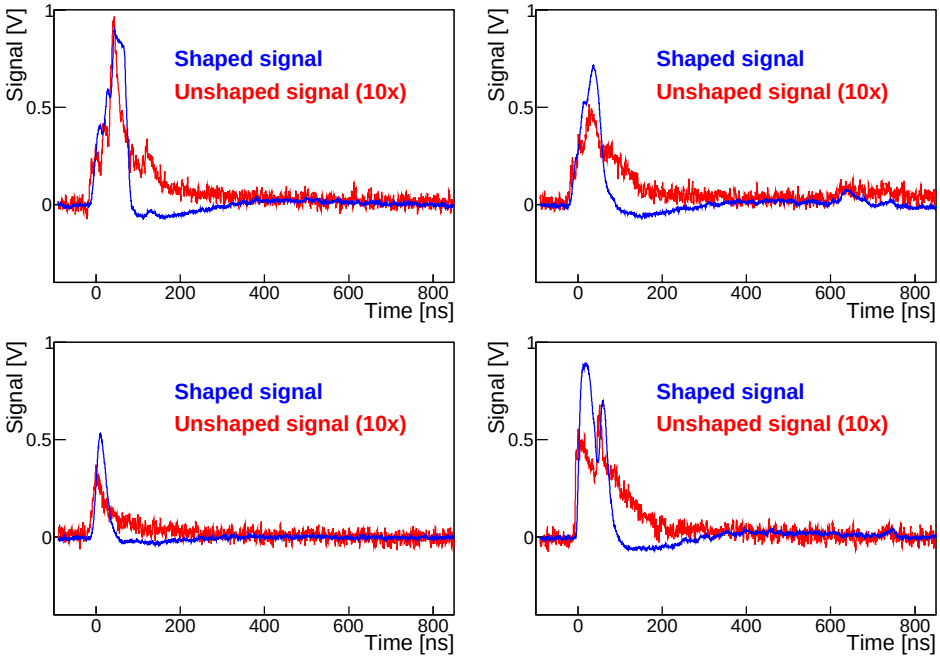


(b) Muon response with baseline restoration.

Figure A.3.: Typical muon pulse shapes from an sMDT tube after the pre-amplifier (red lines) and after shaping (blue lines) with and without baseline restoration, respectively (Measurement bandwidth: 200 MHz).

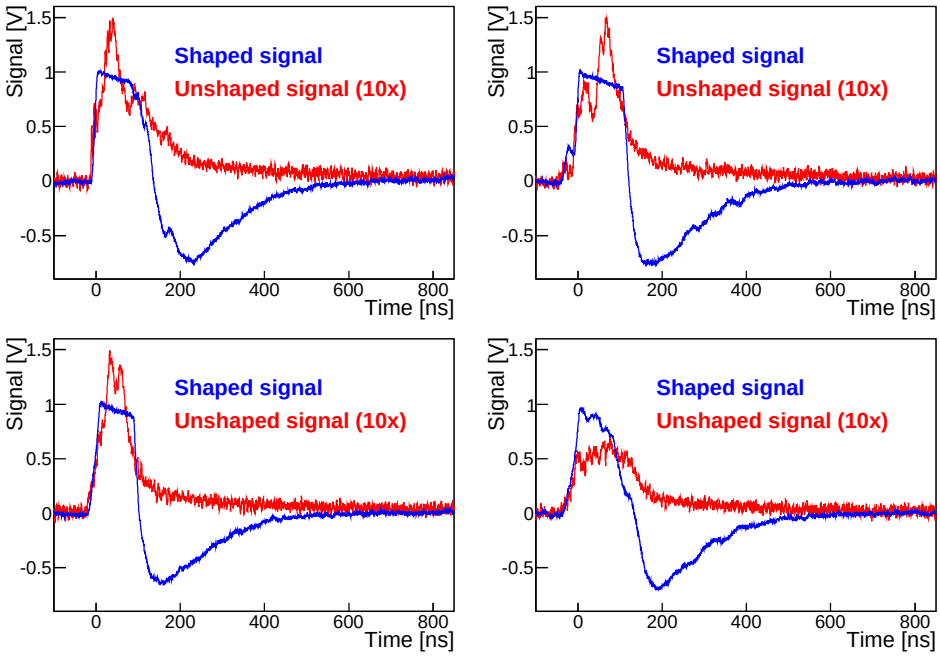


(a) Electron response without baseline restoration.

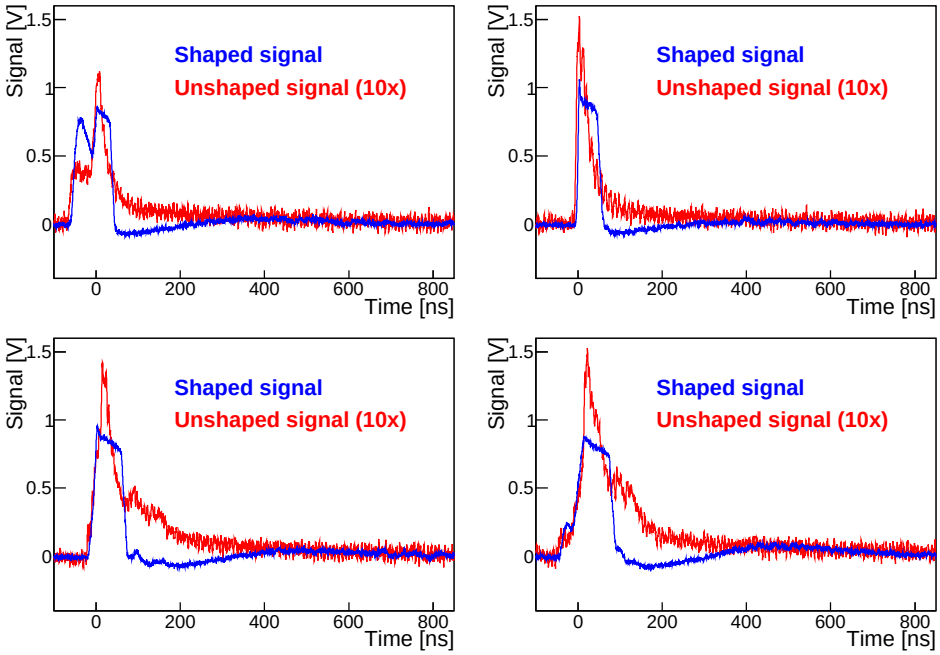


(b) Electron response with baseline restoration.

Figure A.4.: Typical electron (^{90}Sr) pulse shapes from an sMDT tube after the pre-amplifier (red lines) and after shaping (blue lines) with and without baseline restoration, respectively (Measurement bandwidth: 200 MHz).



(a) Gamma response without baseline restoration.



(b) Gamma response with baseline restoration.

Figure A.5.: Typical γ (^{137}Cs) pulse shapes from an sMDT tube after the pre-amplifier (red lines) and after shaping (blue lines) with and without baseline restoration, respectively (Measurement bandwidth: 200 MHz).

A.2.5. Stage 1

The complex function $G_1(\omega)$ (see Eq. 5.2 describing the complex gain of Fig. 5.8) can be written in polar form

$$G_1(\omega) = g_1(\omega) \cdot (\cos\phi_1 + i \cdot \sin\phi_1) \tag{A.28}$$

with the magnitude $g_1(\omega)$ and the phase[4] $\phi_1(\omega)$

$$g_1(\omega) = \frac{R_2}{R_1+R_2} \cdot \frac{R_5}{R_3} \cdot \sqrt{\frac{(R_3+R_4)^2\omega^2C_2^2+1}{R_4^2\omega^2C_2^2+1}} \tag{A.29a}$$

$$\phi_1(\omega) = -ATan\left(\frac{R_4\omega C_2}{R_3\omega^2C_2^2(R_3+R_4)-1}\right) \ . \tag{A.29b}$$

The magnitude $g_1(\omega)$ is bounded. For $\omega = 0$ the resistance of the pole-zero network is $R_{pz} = R_3$ and for $\omega \to \infty$ it becomes $R_{pz} = R_3 \| R_4$. Taking into account the voltage divider and the inverting amplifier, it follows

$$\frac{R_2}{R_1+R_2} \cdot \frac{R_3+R_4}{R_3R_4} < g_1(\omega) < \frac{R_2}{R_1+R_2} \cdot \frac{R_5}{R_3} \ . \tag{A.30}$$

The phase $\phi_1(\omega)$ shows a global minimum at

$$\omega_{min} = \frac{1}{C_2\sqrt{R_3 \cdot (R_3+R_4)}} \ , \tag{A.31}$$

which can be determined by solving the equation

$$\frac{d}{d\omega}\phi_1(\omega) = 0 \ , \tag{A.32}$$

leading to

$$\phi_1(\omega_{min}) = -ATan\left(\frac{(R_3 \cdot (R_3+R_4))^{\frac{3}{2}}}{(R_3+R_4)^3}\right) \ . \tag{A.33}$$

For $\omega = 0$ and $\omega \to \infty$ the phase converges to 0, which can be easily shown using Eq. A.29b.

A.2.6. Stage 2

The complex function $G_2(\omega)$ (see Eq. 5.4 describing the complex gain of Fig. 5.10) can be written in polar form

$$G_2(\omega) = g_2(\omega) \cdot (\cos\phi_2 + i \cdot \sin\phi_2) \tag{A.34}$$

with the magnitude $g_2(\omega)$ and the phase $\phi_2(\omega)$

$$g_2(\omega) = \frac{R_7 \cdot R_9}{R_6+R_7} \cdot \frac{\omega C_4}{\sqrt{R_8^2\omega^2C_4^2-1}} \tag{A.35a}$$

[4] $\phi_1(\omega) = ATan\left(\frac{1}{(R_3+R_4)\omega C_2}\right) - ATan\left(\frac{1}{R_4\cdot\omega C_2}\right)$, then the relation $ATan(x) - ATan(y) = ATan\left(\frac{x+y}{1-x\cdot y}\right)$ is applied.

$$\phi_2(\omega) = -ATan\left(\frac{1}{R_8\omega C_4}\right) \ . \tag{A.35b}$$

The magnitude and phase are bounded

$$0 < g_2(\omega) < \frac{R_7}{R_6 + R_7}\frac{R_9}{R_8} \tag{A.36a}$$

$$0 < \phi_2(\omega) < \frac{\pi}{2} \ . \tag{A.36b}$$

A.2.7. Diode Model Determination (SPICE)

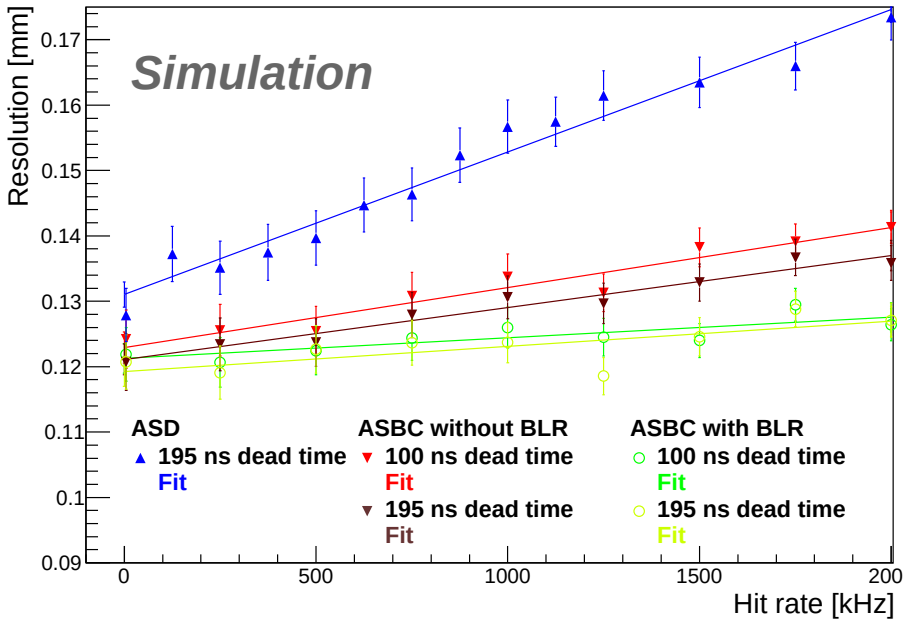
In Tab. A.3 the result of the SPICE diode model fit is shown. All other parameters are set to default.

Parameter	Value	Description
IS	$2.9001 \cdot 10^{-17}$ A	Diode saturation current
RS	17.17 Ω	Diode serial resistance
N	1.00175 Ω	Emission coefficient (ideality factor)
CJO	$9.71521 \cdot 10^{-16}$ F	Zero-bias junction capacitance
VJ	0.253 V	Junction potential
EG	1.11 V	Activation energy (fixed for silicon)
TT	$8.327 \cdot 10^{-8}$ s	Transit time

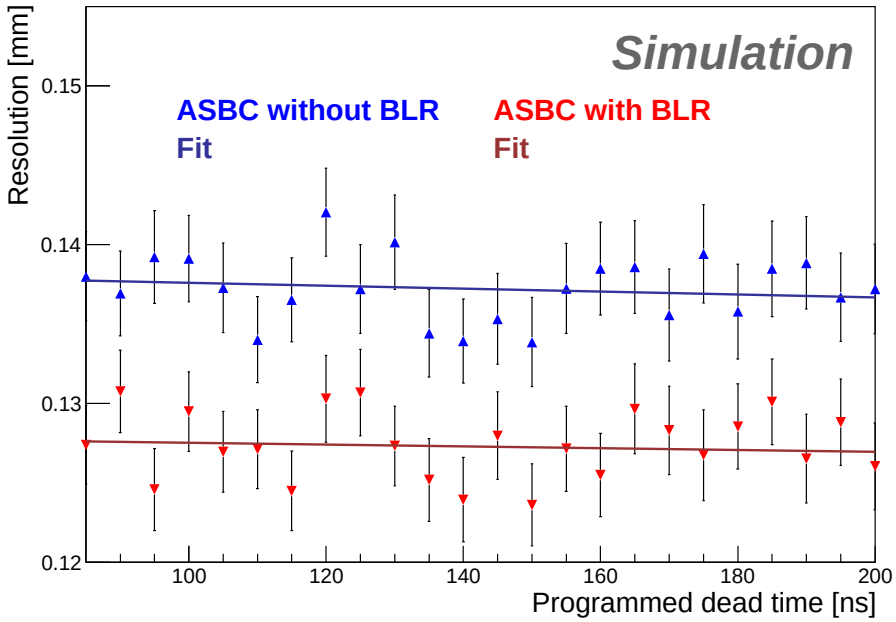
Table A.3.: Fitted parameters of the SPICE diode model (see Section 5.3.4).

A.2.8. Simulation

Fig. A.6a shows the fits of simulation results of the average single tube spatial resolution for different dead time settings measured with ASD (without time slewing correction) and with ASBC with and without baseline restoration depending on the background electron hit rate (see Fig. 5.38). Fig. A.6b shows fits of the simulation of the average sMDT single tube resolution measured with the ASBC as a function of the dead time (see Fig. 5.39b). Fig. A.7 shows the the fits of simulation results of the average single tube spatial resolution for different dead time settings measured with ASD (without time slewing correction) and with ASBC with and without baseline restoration depending on the background gamma hit rate (see Fig. 5.42a).



(a)



(b)

Figure A.6.: (a) Fits of simulation results of the average single tube spatial resolution for different dead time settings measured with ASD (without time slewing correction) and with ASBC with and without baseline restoration depending on the background electron hit rate (see Fig. 5.38).
(b) Fits of the simulation of the average sMDT single tube resolution measured with the ASBC as a function of the dead time (see Fig. 5.39b).

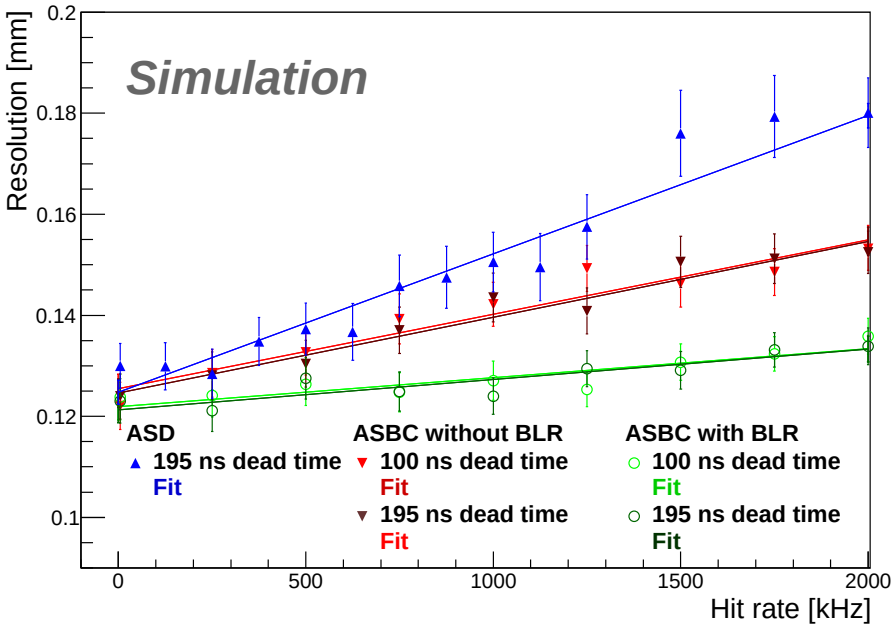
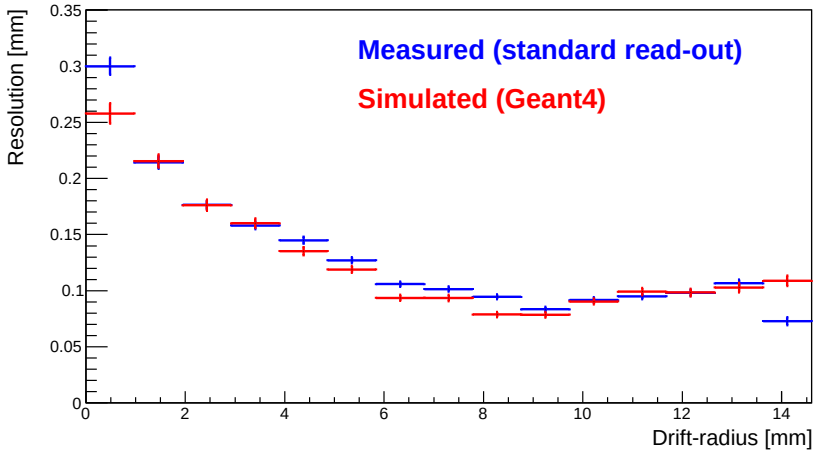


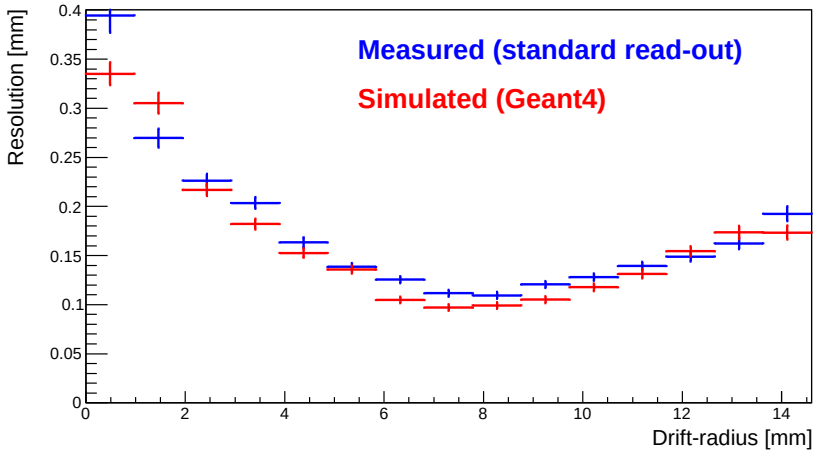
Figure A.7.: Fits of simulation results of the average single tube spatial resolution for different dead time settings measured with ASD (without time slewing correction) and with ASBC with and without baseline restoration depending on the background gamma hit rate (see Fig. 5.42a)

A.3. Performance of the Trigger Demonstrator Set-up

In Fig. A.8 the reference resolution of the MDT chamber measured and obtained with simulation is shown (see Fig. 6.3.4.4). Fig. A.9 illustrate the MDT chamber γ hit rates and occupancies for the results presented in Section 6.3.4.5.

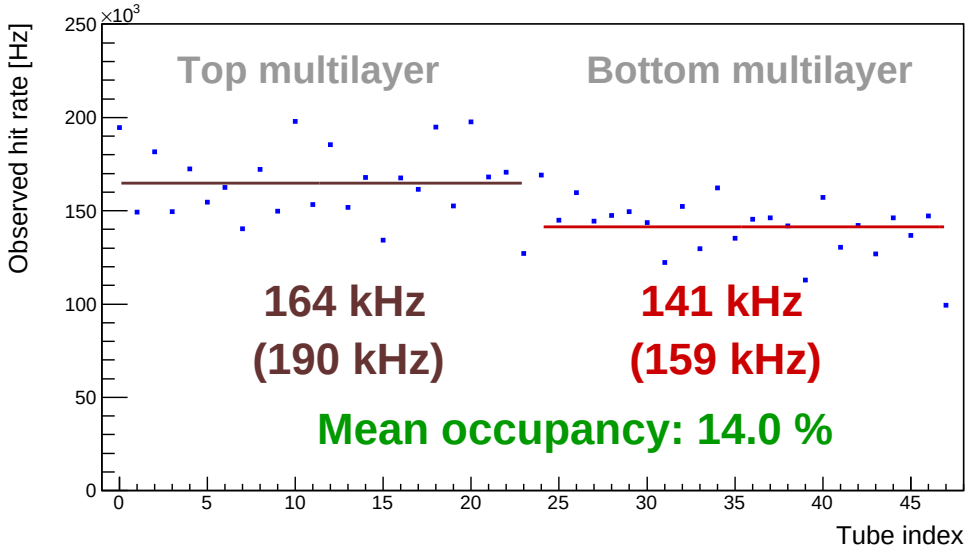


(a) No uncorrelated background occupancy.

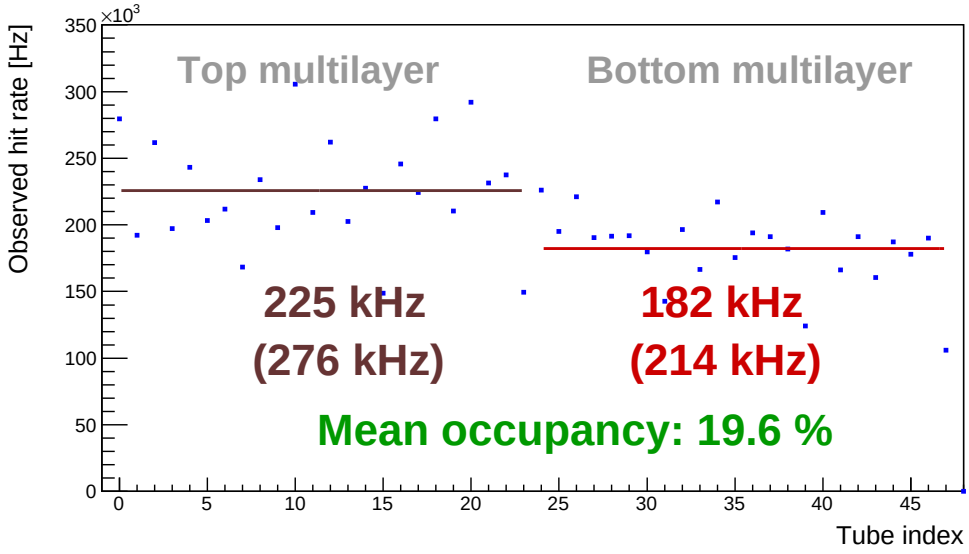


(b) 13.0% uncorrelated background occupancy.

Figure A.8.: Measured and simulated (MT-Geant4) MDT resolution (standard read-out) in dependency of the drift-radius of the setup shown in Fig. 6.13 in case of no and 11.3% uncorrelated background occupancy.



(a)



(b)

Figure A.9.: Uncorrected γ hit rates of the experiment described in Section 6.3.4 as a function of the tube index. The lower 24 tubes are within the top multilayer and the upper 24 tubes within the bottom multilayer, respectively. The mean hit rates are determined for each multilayer separately, the true hit rate is shown in round brackets, the occupancy in square brackets.

A.4. ARM Cortex-M4F Implementation of the Track Finding Algorithm

Tab. A.4 shows the use of the ARM Core-Registers and the ARM FPU-Registers for the implementation of the histogram based pattern recognition and linear fit. Tab. A.5, Tab. A.6 and Tab. A.7 show the commands and the corresponding duration in clock cycles for the histogram based pattern recognition with track reconstruction.

Register	Pattern recognition	Linear fit
R0	General use / Hit counter	Hit counter
R1	General use	Final result address
R2	General use	Number of highest bins
R3	General use	Address of highest bin positions
R4	General use	Detail buffer address of highest bin
R6	Histogram base address	
R7	Value of highest bin	Value of highest bin
R8	Detail buffer address	
R9	Detail buffer size	
R10	BDR address	
R11	BDR size	
S0-S4	1, $\frac{1}{2}$, $\frac{1}{3}$, $\frac{1}{4}$, $\frac{1}{5}$	
S5	Angle of Primary Trigger	
S6	Position of Primary Trigger	
S7		error for χ^2 determination
S8	Bin width of histogram	
S9	Cosine of angle	
S10	Sine of angle	
S11	Tube coordinate z	
S12	Tube coordinate y	
S13	Tube drift-radius	
S14	Projection of tube coordinates to z-axis	
S15	Projection of tube with drift-radius to z-axis	
S16	Resulting bin	
S17	Drift-radius * cos	
S18	Drift-radius * sin	
S19	Final hit coordinate y	
S20	Final hit coordinate z	
S21		Hits to process (n)
S22		$\sum_i y_i$
S23		$\sum_i z_i$
S24		$\sum_i z_i^2$
S25		$\sum_i (y_i \cdot z_i)$
S26		General use
S27		General use
S28		Numerator
S29		Resulting α_1
S30		Resulting α_2
S31		Resulting χ^2

Table A.4.: Description of the use of the registers for the implementation of the histogram based pattern recognition (see Fig. 6.24) and linear track reconstruction (see Fig. 6.26)in an ARM Cortex-M4F processing unit.

Command	*Comment*	*Cycles*
Prepare CPU registers		
LDR R0, =_address_histogram	Load histogram base address	2
LDR R6, [R0]		2
MOV R7, #0x00	Clear register for highest peak in histogram	1
LDR R0, =_address_detail_buffer	Load detail buffer address	2
LDR R8, [R0]		2
LDR R0, =_size_detail_buffer	Load detail buffer size	2
LDR R9, [R0]		2
LDR R0, =_address_BDR	Load BDR address	2
LDR R10, [R0]		2
LDR R0, =_size_BDR	Load BDR size	2
LDR R11, [R0]		2
LDR R11, [R11]		2
LDR R0, =_address_angle	Load primary trigger angle address	2
LDR R0, [R0]		2
VLDR.F32 S5, [R0]		2
LDR R0, =_address_position	Load primary trigger position	2
LDR R0, [R0]		2
VLDR.F32 S6, [R0]		2
LDR R0, =_bin_width	Load bin width	2
VLDR.F32 S8, [R0]		2
MOV R1, #0x0	Set R1 to zero	1
VMOV.F32 S0, #1e0	Set S0 to 1	1
VMOV.F32 S1, #0.5e0	Set S1 to 2	1
LDR R0, =_number_third	Set S2 to 1/3	2
VLDR.F32 S2, [R0]		2
VMOV.F32 S3, #0.25e0	Set S3 to 4	1
LDR R0, =_number_fifth	Set S4 to 5	2
VLDR.F32 S4, [R0]		2
MOV R0, #0x0		$1 \rightarrow \mathbf{52}$
Set histogram bins to 0		
MOV R2, [R6]		1
STR R1, [R2], #4	Clear 4 bin and change bin address	$2 \rightarrow \mathbf{1} + \frac{bins}{2}$

Table A.5.: ARM Cortex-M4F commands and their duration in clock cycles of the subprocesses of the algorithm shown in Fig. 6.24, part 1/3.

Command	*Comment*	*Cycles*
Calculate sine and cosine		
VMUL.F32 S9, S5, S5	α^2	1
VMUL.F32 S9, S9, S1	$\frac{\alpha^2}{2}$	1
VMUL.F32 S10, S9, S5	$\frac{\alpha^3}{2}$	1
VMUL.F32 S10, S10, S2	$\frac{\alpha^3}{6}$	1
VMUL.F32 S11, S10, S5	$\frac{\alpha^4}{6}$	1
VMUL.F32 S11, S11, S3	$\frac{\alpha^4}{24}$	1
VMUL.F32 S12, S11, S5	$\frac{\alpha^5}{24}$	1
VMUL.F32 S12, S12, S4	$\frac{\alpha^5}{120}$	1
VSUB.F32 S9, S0, S9	$1 - \frac{\alpha^2}{2}$	1
VADD.F32 S9, S9, S11	$1 - \frac{\alpha^2}{2} + \frac{\alpha^4}{24}$	1
VSUB.F32 S10, S5, S10	$\alpha - \frac{\alpha^3}{6}$	1
VADD.F32 S10, S10, S12	$\alpha - \frac{\alpha^3}{6} + \frac{\alpha^5}{120}$	$1 \rightarrow$ **12**
Load hit information into registers		
VLDR.F32 S11, [R10]	Load tube coordinate z	2
VLDR.F32 S12, [R10, #4]	Load tube coordinate y	2
VLDR.F32 S13, [R10, #8]	Load radius r	$2 \rightarrow$ **6**
Calculate projection of the wire		
VMUL.F32 S14, S11, S10	$z \cdot \cos\alpha$	1
VMUL.F32 S15, S12, S9	$z \cdot \sin\alpha$	1
VADD.F32 S14, S14, S15	$z \cdot \cos\alpha + y \cdot \sin\alpha$	1
VSUB.F32 S14, S14, S6	Remove RoI	1
VMUL.F32 S17, S13, S9	$r \cdot \cos\alpha$	1
VMUL.F32 S18, S13, S10	$r \cdot \sin\alpha$	$1 \rightarrow$ **6**
Calculate bin for the side of the wire		
VADD.F32 S15, S14, S13	Add radius	1
VMUL.F32 S16, S15, S8	Calculate bin	1
VCVT.U32.F32 S16, S16	Round	1
VMOV R1, S16	Move it to ARM core	$2 \rightarrow$ **5**
Calculate 2D position of hit		
VADD.F32 S19, S11, S17	$z + r \cdot \cos\alpha$ modified for other side	1
VADD.F32 S20, S12, S18	$y + r \cdot \sin\alpha$ modified for other side	$1 \rightarrow$ **2**
Add bin to histogram		
ADD R2, R1, R6	Calculate bin address	1
LDRB R3, [R2]	Load bin	2
ADD R3, #0x01	Add 1 to bin	1
CMP R3, R7	Check if peak is the highest	1
IT GT	conditional	1
MOVGT R7, R3	save value as highest	1
STRB R3, [R2]	Store bin	$2 \rightarrow$ **9**

Table A.6.: ARM Cortex-M4F commands and their duration in clock cycles of the sub-processes of the algorithm shown in Fig. 6.24, part 2/3.

Command	*Comment*	*Cycles*
Store hit position		
MLA R4, R9, R1, R8	Calculate first address of detail buffer	2
MOV R2, #0x08	Load size for one hit in the detailed buffer	1
MLA R4, R3, R2, R4	And add right position	2
VSTR.32 S19, [R4,#-0x08]	Store detail z	2
VSTR.32 S20, [R4,#-0x04]	Store detail y	2 $\rightarrow$ **9**
Prepare next hits		
ADD R0, #0x01	Add 1 to the hit counter	1
ADD R10, #0x0C	Increment to load next element	1
CMP R0, R11	Compare with hit count	1
BNE Process_Tube	and jump	3 $\rightarrow$ **6**
Check the peak		
CMP R7, #0x04	Compare peak with threshold	1
IT LT	conditional	1
BLT	Jump out if necessary	1 $\rightarrow$ **3**
Find peaks in histogram		
MOV R0, #0x00	Reset bin counter	1
MOV R2, #0x00	Reset result counter	1
LDR R3, =_hresult_address	Load address for storing results	2
LDR R3, [R3]		2
LDRB R1, [R6], #0x01	Load next bin value and increment address	2
CMP R1, R7	Compare	1
ITT EQ	conditional	1
STRBEQ R1, [R3], #0x01	Store index in buffer	1 (2)
ADDEQ R2, #0x01	Increment result counter	1
ADD R0, #0x01	Increment bin counter	1 $\rightarrow$ $\mathbf{6 + 7 \cdot b + r}$

Table A.7.: ARM Cortex-M4F commands and their duration in clock cycles of the subprocesses of the algorithm shown in Fig. 6.24, part 3/3. b ... bins, r ... results

Command	*Comment*	*Cycles*
Prepare registers		
LDR R1, =_chi2_error	Load error for χ^2 calculation	2
VLDR.F32 S7, [R1]	And move it to S7	2
LDR R1, =_result_count_address	Load address for number of results	2
LDR R1, [R1]		2
STR R2, [R1]	Store number of results	2
LDR R1, =_result_address	Load address of result	2
LDR R1, [R1]		2
VMOV.F32 S21, R7	Load number of hits to FPU	2
VCVT.F32.U32 S21, S21	Convert to float	1→ **17**
Load bin and buffer address		
SUB R3, #0x01	Decrement bin address	1
LDRB R4, [R3]	Load bin index	2
MUL R4, R4, R9	Calculate buffer address	1
ADD R4, R4, R8		1
VSUB.F32 S22, S21, S21	clear sums by subtracting S21 of S21	1
VSUB.F32 S23, S21, S21		1
VSUB.F32 S24, S21, S21		1
VSUB.F32 S25, S21, S21		1
MOV R0, #0x00	Clear counter	1→ **10**
Load hit informations into registers		
VLDR.F32 S12, [R4], #0x4	Load z coordinate	2
VLDR.F32 S11, [R4], #0x4	Load y coordinate	2→ **4**
Calculate sums		
VADD.F32 S22, S22, S12	$\sum y$	1
VADD.F32 S23, S23, S11	$\sum z$	1
VMUL.F32 S26, S11, S11	$z \cdot z$	1
VADD.F32 S24, S24, S26	$\sum z^2$	1
VMUL.F32 S26, S11, S12	$y \cdot z$	1
VADD.F32 S25, S25, S26	$\sum y \cdot z$	1→ **6**
Prepare registers for next hit		
ADD R0, #0x01	Add 1 to counter	1
CMP R0, R2	Compare with hit count	1
BNE Fit_Process_Tube	If data left, restart	3→ **5**

Table A.8.: ARM Cortex-M4F commands and their duration in clock cycles of the subprocesses of the algorithm shown in Fig. 6.26, part 1/3.

Command	*Comment*	*Cycles*
Process multiplications and sums		
VMUL.F32 S28, S21, S24	$n \cdot \sum z^2$	1
VMUL.F32 S26, S23, S23	$\sum z \cdot \sum z$	1
VSUB.F32 S28, S28, S26	Calculate denomerator	1
VMUL.F32 S26, S22, S24	$\sum y \cdot sumz^2$	1
VMUL.F32 S27, S25, S23	$\sum yz \cdot \sum z$	1
VSUB.F32 S29, S26, S27	α_1 numerator	1
VMUL.F32 S26, S21, S25	$n \cdot \sum yz$	1
VMUL.F32 S27, S22, S23	$\sum yz \cdot \sum y$	1
VSUB.F32 S30, S26, S27	α_2 numerator	1→ **9**
Process divisions		
VDIV.F32 S29, S29, S28	Divison for α_1	14
VDIV.F32 S30, S30, S28	Divison for α_2	14→ **28**
Prepare χ^2 calculation		
MOV R0, #0x00	Reset counter	1
SUB R4, R4, #0x08	Now the hist are loaded backwards	1
VSUB.F32 S31, S30, S30	Clear χ2 sum	1→ **3**
Load hit informations into registers		
VLDR.F32 S12, [R4]	Load z coordinate	2
VLDR.F32 S11, [R4, #0x04]	Load y coordinate	2→ **4**
Calculate sum		
VMUL.F32 S26, S30, S11	$\alpha_2 \cdot z$	1
VSUB.F32 S27, S12, S29	$y - \alpha_1$	1
VSUB.F32 S27, S27, S26	$y - \alpha_1 - \alpha_2 \cdot z$	1
VMUL.F32 S27, S27, S27	$(y - \alpha_1 - \alpha_2 \cdot z)^2$	1
VADD.F32 S31, S27, S31	Add it to χ^2 sum	1→ **5**
Prepare registers		
ADD R0, #0x01	Add 1 to counter	1
SUB R4, R4, #0x08	Calculate address for next point	1
CMP R0, R2	Compare with hit counter	1
BNE Calc_chi2	If data left, restart	3→ **6**
Finalise calculation		
VSUB.F32 S26, S21, S0	Degrees of freedom +1	1
VSUB.F32 S26, S26, S0	Degrees of freedom	1
VMUL.F32 S26, S26, S7	Multiplied with the error	1
VDIV.F32 S31, S31, S26	Final division	14→ **17**

Table A.9.: ARM Cortex-M4F commands and their duration in clock cycles of the sub-processes of the algorithm shown in Fig. 6.26, part 2/3.

Command	*Comment*	*Cycles*
Store result and prepare		
VSTR.32 S29, [R1], #0x04	Store resulting α_1	2
VSTR.32 S30, [R1], #0x04	Store resulting α_2	2
VSTR.32 S31, [R1], #0x04	Store resulting $\chi^2_{p.d.o.f.}$	2
SUB R2, #0x01	Decrement number of results to process	1
CMP R2, #0x00	Check if still results are left to process	1
BNE Next_fit	If still data left, jump	3→ **11**

Table A.10.: ARM Cortex-M4F commands and their duration in clock cycles of the subprocesses of the algorithm shown in Fig. 6.26, part 3/3.

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(Faust. Der Tragödie erster Teil)