Measurement Results of the DTCNN-Universal Chip

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Abstract

The paper gives the measurement results of the analog current-mode implementation of Discrete-Time Cellular Neural Networks, which has been described in [HNRC94]. A chip for an analog programmable network was fabricated with the ORBIT 2.0 μm process containing 12 by 12 regular cells and 52 border cells. The effective chip area amounts to 0.38 cm^2 with a power consumption of 0.8 W. The measurements include the statistical distribution of the 2880 cascoded current mirrors and the dynamic processing of the connected component detector, the shadow detector, the increasing and decreasing of objects with a clock frequency of 1 MHz.

1 Introduction

Discrete-Time Cellular Neural Networks (DTCNNs) are derived from Cellular Neural Networks [CY88] and Threshold Networks [She69]. Their local connectivity and translationally invariant weights allow efficient analog VLSI implementations with high cell density [CC91], [HNS92], [RVEDC+93], [VSSA93]. In [HNRC94], a current-mode implementation of the DTCNN is introduced, which includes the most important parts of the Universal Chip [RC93]. The main advantage of a time-discrete implementation is an easy adjustment of the processing speed to a given application by changing the clock rate. The clocked transfer of the outputs allows a simple cascading of multiple chips on a board.

Fig. 1 shows the block diagram for a single cell using differential signals. The state current,

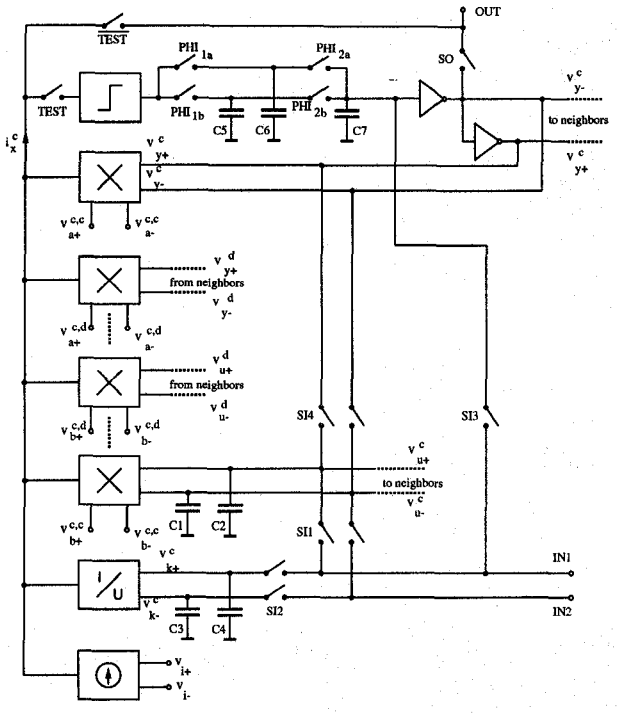

Figure 1: Block structure for a single cell.

which is computed from adding the binary outputs weighted with the feedback coefficients, the analog inputs weighted with the control coefficients, the local analog memory, and, the threshold current, is expressed by

$$
\begin{aligned}
&i_x^c(k) = \\
&\sum_{d\in N_r(c)} (v_{a+}^{c,d}(k) - v_{a-}^{c,d}(k))(v_{y+}^{d}(k) - v_{y-}^{d}(k))g_a + \\
&\sum_{d\in N_r(c)} (v_{b+}^{c,d}(k) - v_{b-}^{c,d}(k))(v_{u+}^{d}(k) - v_{u-}^{d}(k))g_b + \\
&(v_{k+}^{c}(k) - v_{k-}^{c}(k))g_k + (v_{T+}(k) - v_{T-}(k))g_T .
\end{aligned}
\tag{1}
$$

The conductances g_a, g_b, g_k and g_T are circuit specific constants [HNRC94].

The binary output is obtained by extracting the sign of the state current with a current comparator [RVDCM+] and storing the value on either C_5 or C_6.

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The subsequent output state is transferred to C_7 during the high phase of φ_{2a} or φ_{2b}.

The signals SI1, ..., SI4, SO and TEST are used for controlling the data transfer of the inputs, initials and outputs via the global bus lines IN1, IN2 and OUT, which are common for a whole row in the network.

During the normal operation of the DTCNN, the switch TEST is closed and the switch $\overline{\text{TEST}}$ is open. For a dc-measurement of the analog components, the state current can be read out by applying a complementary switch configuration.

The regular cells are surrounded by a ring of specific border cells, which provide the inputs and outputs at the boundary of the network for the regular cells. Besides, they decode the column select signals SI1, ..., SI4, SO, and, TEST from a global address bus and support a fast exchange of the outputs between neighboring chips on a printing board. A foto of the fabricated chip is shown in Fig. 2, from which the regular structure of the cells is clearly recognized. The size for a single cell was 619 μm by 425 μm.

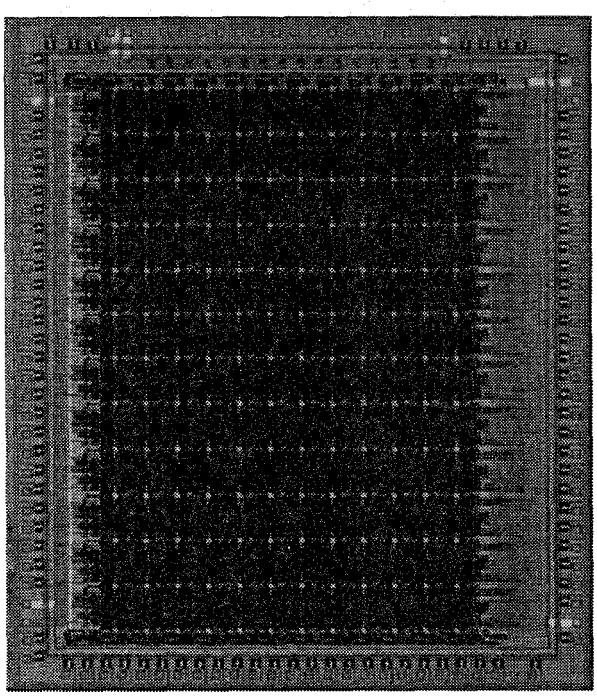

Figure 2: Foto of the chip.

For testing, the flexible PC-controlled CNN testset in [KSHN92] has been used, where the modules have been expanded by static output channels with 12 bit d/a converters and a static input channel with a 12 bit a/d converter. The accuracy of the testset has been experimentally determined to approximately 3 mV.

The measurements showed that a design rule violation in the poly 2 plane due to an erronous technology file of the design rule checker short-cutted all differential capacitors. From the local analog memories one was working, which could be evaluated for the dc transfer characteristic. However, the measurement of the feedback coefficients and the dynamic behavior could be completely performed. Actually, a redesign is in fabrication with the corrected layout.

2 Measurement of the Feedback Coefficients

The multiplication of the binary feedback coefficients has been realized by cascoded current mirrors [HNRC94]. Here, a nonlinear relationship between weight voltage and output current was not disturbent and could be eliminated by a suited preprocessing transformation of the weights. The transistor sizes have been chosen to $\frac{W}{L} = \frac{12\mu m}{8\mu m}$ and $\frac{W}{L} = \frac{12\mu m}{4\mu m}$. The p-channel transistors are supplied with $V_{dd} = 8V$.

Fig. 3 (a) shows the spread of the measured currents depending on their weight voltage, where the deviation area has been drawn for positive and negative feedback coefficients and the threshold.

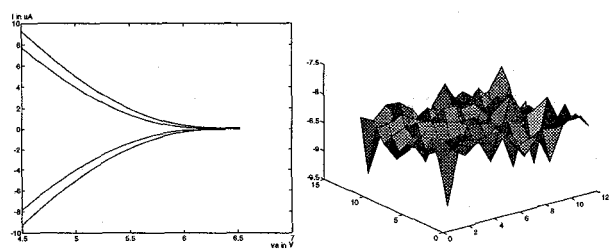

Figure 3: (a) Spread of the feedback coefficients and (b) spatial distribution of the feedback coefficients on the cell grid.

The x-axis corresponds to the applied weight voltage in V, which is identical for all cells, and the y-axis gives the absolute current in μA. In contrast to the simulation, where a maximum current of 10.6 μA has been observed, the measurements showed a smaller absolute current. This can be explained by a voltage drop of the protecting resistor of the input pads.

The state current has been measured separately with the computer-controlled test set for all 2880 current mirrors and the thresholds (number of cells $\times$ number of cascoded current mirrors per cell). The statistical distribution is shown in Fig. 4 for positive and negative coefficients. The x-axis gives the

state current in μA for a weight voltage of 4.5 V and the y-axis corresponds to the number of current mirrors within a single bar. The mean value amounts to $8.28\mu A$ ($-8.42\mu A$) and has a standard deviation of 2.93 % (2.81 %) for positive (negative) weights. The worst case deviation of a single cell was 10.8 %. The measurements have shown that the spread of the coefficients has been larger than expected. Because the feedback coefficients have been realized by two current mirrors for a positive and a negative weight, where only one of them is active, this realization has not a real differential structure, where process fabrications are compensated in first approximation.

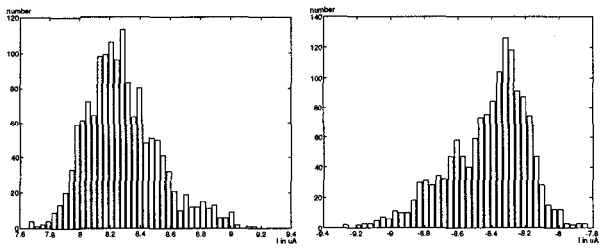

Figure 4: (a) Statistical distribution of the maximum current for positive (left) and negative (right) coefficients.

Because the cells are only locally connected, it is important to know how large are the local worst case deviations for the coefficients within a single cell. An evaluation of the measurement data showed a worst case deviation of 6.7 % within a cell.

Next, it is investigated if the spread is a systematic error depending on the position of the cell on the grid. Here, the surface plot of a weight coefficient has been evaluated as exemplarily shown in Fig. 3 (b). The x- and y-axis correspond to the spatial position on the grid, while the z-axis gives the state current for a weight voltage of 4.5 V. The evaluation of all surface plots showed that there was no preferrable location of current valleys or mountains depending on the position.

3 Measurement of the Analog Memories

The dc-transfer characteristic of the analog memory [BW87], which converts a differentially stored input voltage into a single-ended output current, could be measured for only a single cell of all chips (Fig. 5 (a)). The x-axis corresponds to the differential voltage $v^c_{k+} - v^c_{k-}$ and the y-axis gives the generated state current in μA. The observed behavior corresponds closely to the expected results from the simulation.

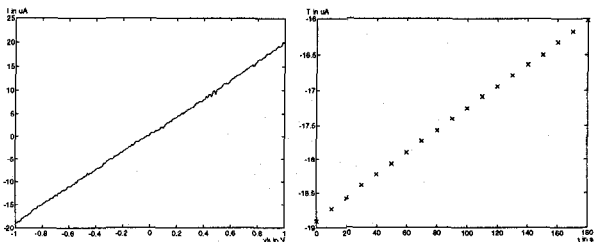

Figure 5: (a) Dc transfer characteristic of the analog memory and (b) measurement of the storage time.

Fig. 5 (b) shows a measurement of the storage time, where the differential 2pF capacitors are loaded to $v^c_{k+} - v^c_{k-} = 1$ V. The state current (y-axis) is measured in μA and the time (x-axis) in s. The leakage current has a constant value of 21.9 $\frac{\text{nA}}{\text{s}}$. The storage time of the binary outputs has been determined to about 20s ($C_5 = C_6 = C_7 = 0.1pF$).

The short cut of the capacitors caused an operation of the local analog memories with a constant input of $v^c_{k+} - v^c_{k-} = 0$ V. For a statistical evaluation, only the offset could be measured in Fig. 6 (a).

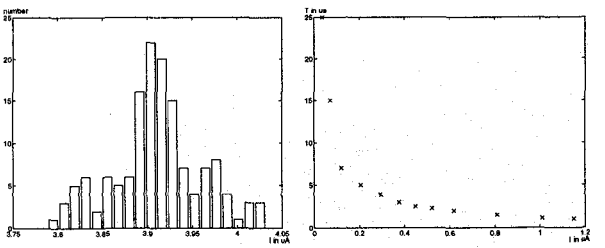

Figure 6: (a) Statistical distribution of the offset and (b) maximum processing speed.

4 Dynamic Measurements

The dynamic measurements proved the correct behavior of templates, where only feedback coefficients and the threshold are used. The multipliers and the local analog memories have been switched off by setting their corresponding input signals to 0 V and, therefore, cutting off the bias trail of the transistors. The following templates have been successfully tested with a speed of 1 MHz, where the chip has been programmed by the weight coefficients.

- connected component detector in eight directions

- shadow detector in eight directions
- increasing objects
- decreasing objects
- inverting objects

Fig. 7 shows the time-dependent development of the letter "A" for a connected component detection towards the right border by using the voltages

$$\mathbf{v}_{a+,-} = \begin{array}{|c|c|c|}\hline (6.5,6.5) & (6.5,6.5) & (6.5,6.5) \\ \hline (4.5,6.5) & (4.5,6.5) & (6.5,4.5) \\ \hline (6.5,6.5) & (6.5,6.5) & (6.5,6.5) \\ \hline \end{array} V$$

$$\mathbf{v}_{b+,-} = \begin{array}{|c|c|c|}\hline (3.6,3.6) & (3.6,3.6) & (3.6,3.6) \\ \hline (3.6,3.6) & (3.6,3.6) & (3.6,3.6) \\ \hline (3.6,3.6) & (3.6,3.6) & (3.6,3.6) \\ \hline \end{array} V$$

$$v_{i+,-} = (6.5,6.5)V \qquad (2)$$

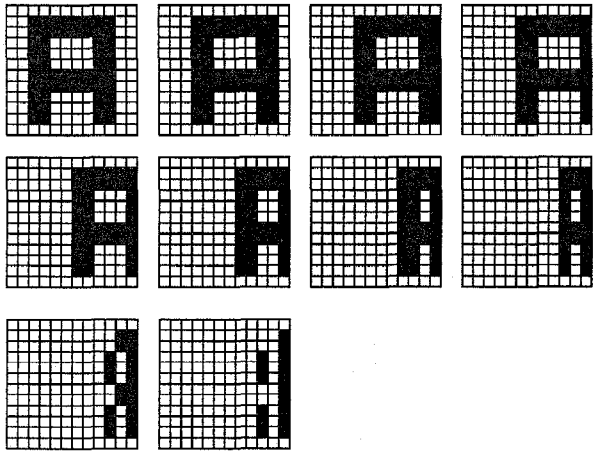

Figure 7: Time-dependent development of the letter"A".

for the template coefficients. Because the cascoded current mirrors have a positive supply voltage of 8 V, a voltage of 6.5 V can be considered as a zero weight coefficient. After 10 iterations a convergent output pattern has been obtained.

Next, the dependency of the maximum operation speed on the minimum value of the state current is investigated. The inverter template was used for this measurement having only a negative self-feedback coefficient. Fig. 6 (b) shows the measured points, where a weight voltage has generated a given state current (x-axis in μA) and the maximum operating frequency has been observed with an oscilloscope at the output of a cell (y-axis with the time period in μs). A state current of about 1 μA allows an operation speed of 1MHz. The clock frequency is restricted by the transient behavior of the current comparator. This is dominated by the parasitic capacitance of the summing current line at the input of the comparator. For higher frequencies, the transient of the current mirrors becomes significant, too.

5 Conclusion

The dynamic measurements have shown that analog circuits are ideally suited for the realization of Discrete-Time Cellular Neural Networks with high cell density. The high performance allows a very fast preprocessing of future image processing applications. The use of sequential templates increases the complexity of the algorithm and allows an operation with an analog template code. Then, the data transfer is minimized, because the locally stored output image of the previous iterations is processed with the new template. The data transfer of the border cells between adjacent chips enables an array configuration on a board with drastically increased cell density.

Another important aspect is the down-scaling for more advanced technology processes. Here, it is important to notice that for the analog part a linear down-scaling is not possible, because the statistical process tolerances are not reduced in the same way. However the digital part and the global routing lines can be significantly shrinked leading to larger network sizes.

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