Phase Stabilization and Calibration Techniques for High-Fidelity Integrated Photonic Processors

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ABSTRACT

Multimode photonic processors—reconfigurable interferometers realised in low-loss stoichiometric silicon nitride—are central to large-scale optical quantum and classical information processing. Their performance, however, is limited by phase jitter from active cooling and by fabrication-induced phase- and amplitude errors.

We demonstrate a self-referenced feedback loop that drives an on-chip phase shifter, cutting multi-port phase fluctuations by over an order of magnitude and enabling stable, repeatable 2x2 Hadamard operations. We then introduce a calibration protocol that iteratively compares measured and ideal transfer matrices to retune each Mach–Zehnder and external phase shifter, eliminating systematic errors and paving the way for high-fidelity optical transforms in advanced photonic processors.

Keywords: photonic processor, feedback control, phase stabilization

1. INTRODUCTION

Photonic processors—reconfigurable multimode interferometers—are now central to quantum information processing, machine learning, Joint Detection, RF signal handling and quantum-repeater links.[1–10]

Their capacity for real-time matrix–vector multiplication promises exponential speed-ups over classical hardware;[13] however, realising this advantage requires low loss and long-term phase coherence to preserve quantum interference,[14] and it could ultimately enable next-generation joint-detection receivers.[11]

State-of-the-art chips already reach 20 modes with high fidelity.[15] Among the proposed meshes—triangular, rhomboidal and square[3,16,17]—stoichiometric silicon nitride (Si_3N_4) offers the best balance of low propagation loss and tight confinement, enabling large, fully reconfigurable interferometers.[18]

We observe that fan-induced motion of the fibre array injects phase noise between input channels, blurring interference fringes and degrading computational accuracy. A kilohertz feedback-control (FBC) loop stabilises the relative phase, cutting fluctuations by more than an order of magnitude. With FBC engaged, 2×2 and 4×4 Hadamard transforms remain locked to their target output powers over extended runs.

To combat static fabrication and thermal errors we implement a systematic calibration routine: measured transfer matrices are iteratively fitted to theory and each Mach–Zehnder or external phase shifter retuned. Applied to a low-loss Si_3N_4 processor, this protocol suppresses residual amplitude- and phase offsets and lays the groundwork for high-fidelity transformations in next-generation photonic computers.

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2. PHOTONIC PROCESSOR

This work was based on the 8-mode reconfigurable quantum photonic processor (PP) based on silicon nitride waveguides from "QuiX Quantum",[3,15] which is composed of three main components: a Si_3N_4 photonic chip, a peripheral system with control electronics and software, and a connected polarization-maintaining (PM) optical fiber array. The Si_3N_4 photonic chip integrates 56 thermo-optic tunable elements, arranged in a universal square interferometer. Each unit cell consists of a tunable beam splitter (TBS), implemented as a Mach-Zehnder Interferometer (MZI), followed by a phase shifter (PS).

The tunability of the 1 mm-long platinum phase shifters is achieved through the thermo-optic effect, allowing for a π phase shift at $V_\pi \approx 10$ V with a power consumption of approximately 385 mW per element. The photonic chip exhibits low propagation losses, measured at 0.07-0.1 dB/cm at a wavelength of 1562 nm. Additionally, the thermo-optic tunable elements support switching speeds up to the 1 kHz range.

The photonic processor is integrated into a control system that includes electronic modules and temperature regulation. The processor is optically packaged with polarization-maintaining (PM) fiber arrays for light input and output, with fibers secured to the front panel for easy access.[3,19] There is a printed and wire-bonded circuit board (PCB) connected to the processor, with 56 voltage drivers that enable independent tuning of the thermo-optic PSs via serial communication with a computer. Temperature stability is maintained through active cooling using a Peltier element placed beneath the metallic mount holding the processor, fiber arrays, and PCB, with optional water cooling available to enhance the cooling capacity.[3,19]

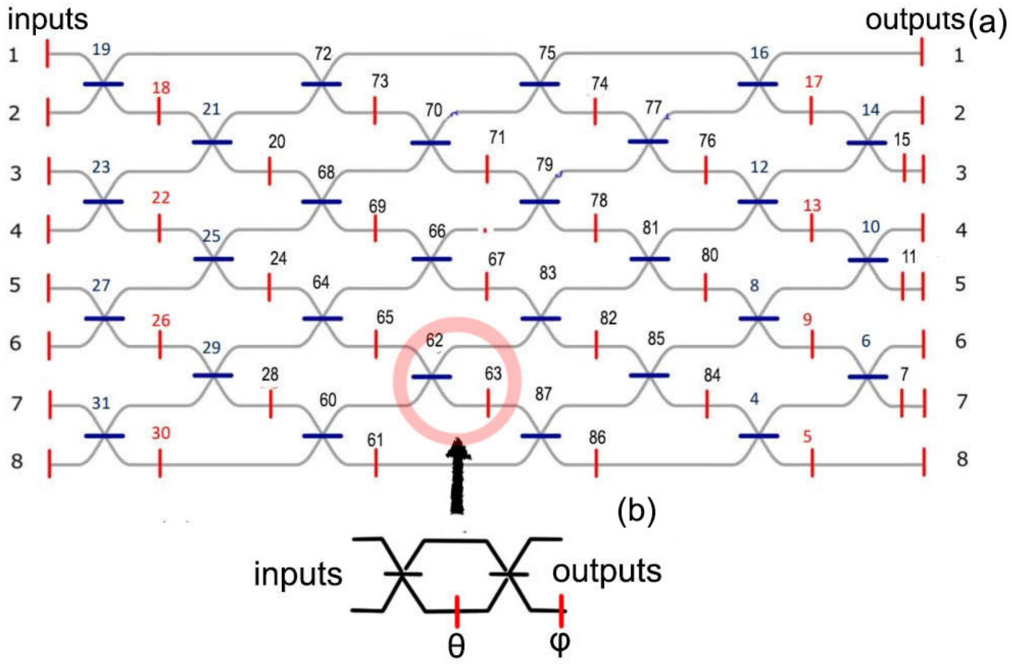

Figure 1. (a) Scheme (8-mode) of QuiX photonic processor chip. (b) The scheme of MZI implemented as single unit cell of the QuiX PP where the blue line represents the MZI with two inputs with two 50/50 directional couplers with an additional thermo-optical phase shifter (ϕ).

The layout of our 8-mode QuiX photonic processor chip, which incorporates 56 phase-tunable shifters (heaters), is shown in Fig. 1. The transformation within the PP by a single unit cell, featuring two inputs and two outputs (as depicted in Fig. 1(b)), can be mathematically represented by the matrix multiplication of the input state with the transformation matrix:

$$T_{\mathrm{MZ}}(\theta,\phi) = \frac{1}{2}\begin{pmatrix} 1-e^{-i\theta} & -i(1+e^{-i\theta}) \\ -ie^{-i\phi}(1+e^{-i\theta}) & -e^{-i\phi}(1-e^{-i\theta}) \end{pmatrix}. \tag{1}$$

Here, θ represents the internal phase shift of MZI, and ϕ denotes the external phase shift (see Fig. 1 (b). By varying θ and ϕ across a range of 2π, it is possible to implement any transformation within the special unitary group, SU(2), which is a critical capability for implementing a wide variety of quantum algorithms and quantum information processing tasks.

3. PHASE STABILIZATION

As previously mentioned, temperature control for the calibrated phase shifters (heaters) of the processor is achieved through active cooling. A thermo-electric Peltier element is placed beneath the sub-mount of the packaged processor, which consists of a metallic mount holding the processor, the fiber arrays, and the PCB. The Peltier element facilitates vertical heat transfer from the on-chip PS to the heat sink. The three fans provide the necessary airflow to ensure the proper functioning of the PP. It is essential to cool the chip to prevent overheating and maintain a stable temperature for the PSs, which are calibrated to operate at specific temperatures.[3, 19]

However, the vibrations caused by the air-cooling fans and the resulting airflow in the photonic processor lead to unwanted shaking of the connecting optical fibers. This shaking results in phase instability between the input signals, causing unstable interference within the PP. Consequently, this instability makes it impossible to achieve a stable and repeatable output from the processor when multiple input signals are used. On the other hand, with a single input signal, the phase delivered to the PP does not produce undesirable time-evolving interference due to fiber shaking. Thus, the processor can be effectively used with a single input signal or by employing a "fiber switch".[15, 20] Due to the "fiber switch" sequentially feeding the input ports of the PP, the propagated signals with randomly oscillating phases do not interfere.

To identify and quantify the phase instability of a beam before and after it passes through a photonic processor, we employed an interference experiment. We recorded a video of the interference fringes generated by a beam that was split externally, both before it entered the processor and after it propagated through it. All PSs were set to the cross-state configuration ($\theta = 0$), where input ports 3 and 6 correspond to output ports 6 and 3, respectively (see Fig. 1.

To analyze the video, we used the Lucas-Kanade optical flow method to track specific points of the video image. The resulting value of the phase instability and phase-changing velocities before and after the photonic processor are shown in Table 1.

Table 1. The velocity of the phase changes before and after the photonic processor.

Parameters	**Before PP**	**After PP**
Mean velocity (%π/sec)	0.820	5.813
Standard deviation of velocity (%π/sec)	0.900	14.467
Max velocity (%π/sec)	7.231	422.786
Median velocity (%π/sec)	0.400	1.370

3.1 Feedback control

Table 1 shows that fibre-induced vibration multiplies the phase-change rate by almost an order of magnitude once the signal enters the chip. We compensate this motion with a self-referenced feedback controller that drives the first on-chip phase shifter, PS 22. The thermo-optic heater can be updated at 1 kHz—more than twenty times higher than the dominant 20–40 Hz vibration band (the cooling fan rotation rate) —so the loop tracks and cancels the disturbance in real time.

Table 2. Mean phase-velocity for two inputs and two outputs with the loop open and closed.

Channel	**FBC off** (rad s^{-1})	**FBC on** (rad s^{-1})
Output 1	-6.8×10^{-2}	-2.3×10^{-3}
Output 2	3.9×10^{-2}	2.7×10^{-3}
Difference	1.07×10^{-1}	4.97×10^{-3}

With the loop engaged, the residual phase velocity drops by more than 8×, and the output powers become stable (Fig. 3.1c and Table 2).

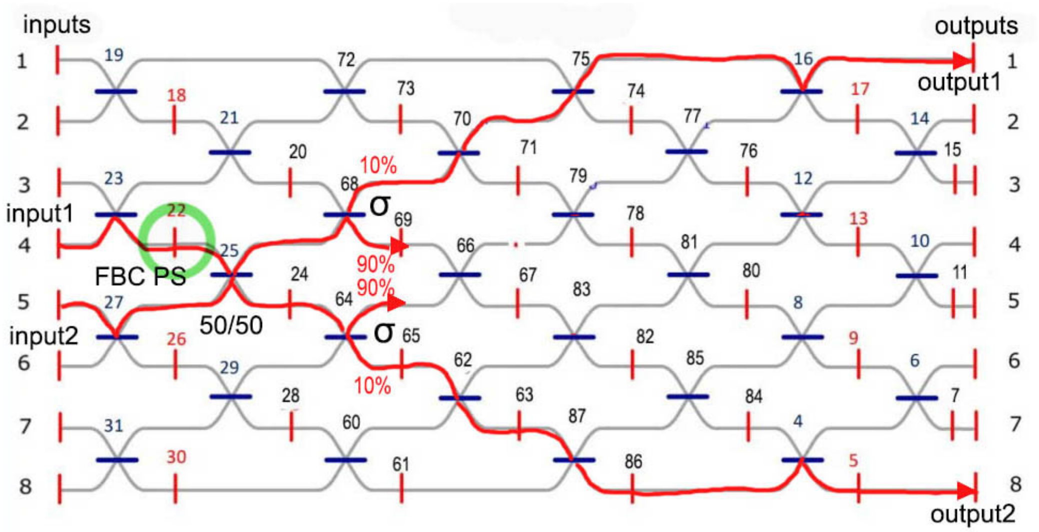

Figure 2. Processor layout. The internal phase shifter PS 22 (highlighted) is driven by the FBC to stabilise the relative phase between two inputs.

Benchmark experiment. To test computational repeatability we programmed a 2×2 Hadamard on MZI 66 (“bar” state, $\theta = \pi$) and monitored outputs 3 and 4, while the FBC continued to run on outputs 1 and 8.

The loop restores stable interference and allows matrix-vector products to be executed repeatably—an essential prerequisite for larger, multi-port transformations implemented via Reck or Clements decompositions.[17, 24]

4. CALIBRATION

Reliable matrix operations demand that every tunable element of the photonic processor (PP) deliver its target phase and amplitude. Even sub-degree deviations in a phase shifter or splitting ratio alter interference and accumulate across the mesh, lowering fidelity in both classical and quantum tasks. Such errors stem from fabrication tolerances, thermo-optic drift and environmental perturbations. A robust calibration routine must therefore (i) correct the initial offsets and (ii) track slow drifts during operation, especially in thermo-optic platforms where phase depends on both temperature and drive voltage.[25]

4.1 Calibration of MZIs

Despite the factory calibration, residual alignment errors sometimes exceed our acceptable threshold. When this occurs, we execute the recalibration algorithm outlined below.

Algorithm.

1. Use Eq. (1) to compute the ideal response of the target unit cell.
2. Inject light into a single input port to avoid parasitic interference, and record the actual output.
3. The phase offset between ideal and measured curves is Δ_{clb}; adjust the heater voltage until the curves align.

Figure 6(a) (solid lines) contrasts the processor’s initial response with the ideal (dashed), revealing non-negligible error. After a single pass of the routine, Fig. 6(b) shows near-perfect overlap: the mean phase error drops from 3.8%π to 1.7%π. Furthermore, our calibration protocol strategically employs the 0 (cross) and π (bar) phase points during the calibration process. These phase settings are inherently stable because they lie in regions where the derivative of the phase response is minimal; that is, small variations in the applied voltage

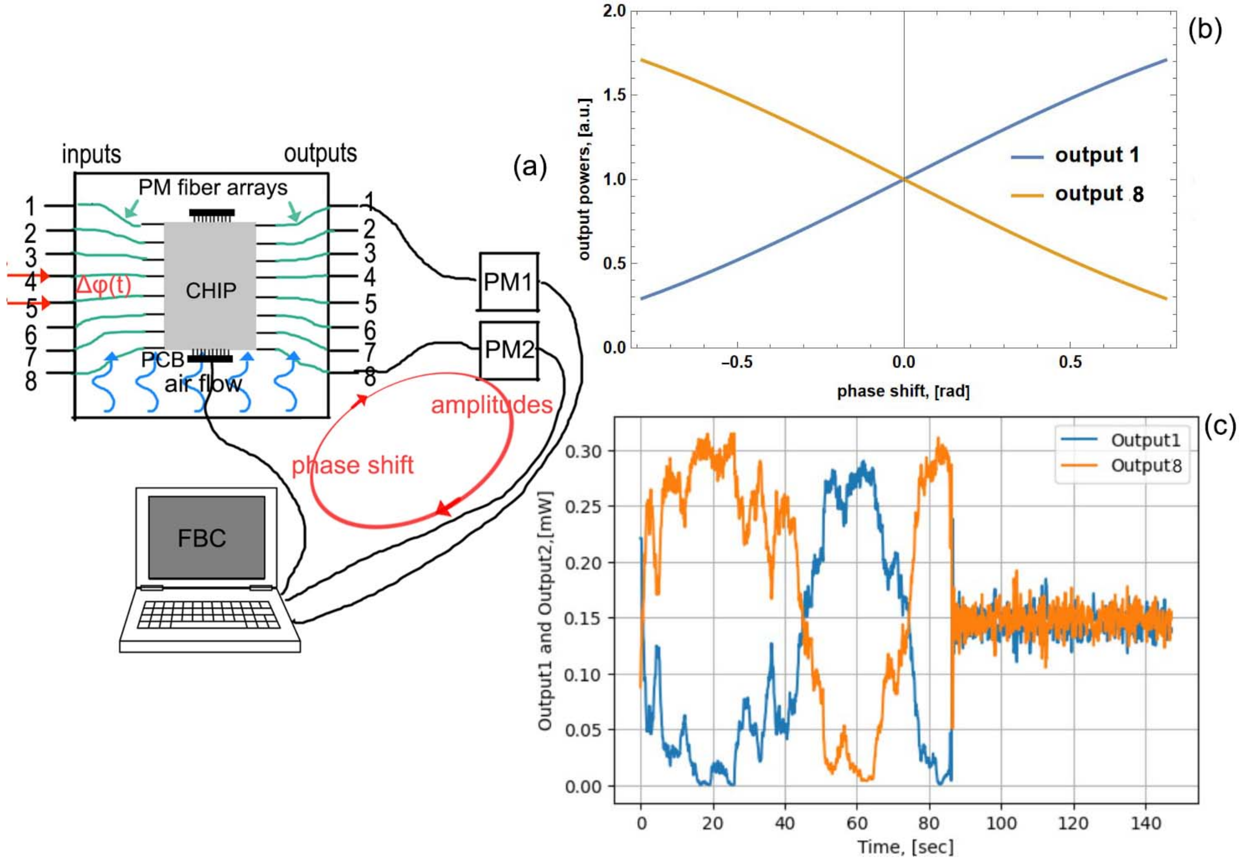

Figure 3. Feedback-control architecture. (a) Optical–electronic layout: the differential photocurrent between outputs 1 and 8 is converted to an error signal that drives phase shifter PS 22 (see Fig. 2). (b) Simulated output powers at ports 1 and 8 as a function of uncontrolled phase drift $\Delta\varphi$, with MZI 25 biased at $\theta = \pi/2$. (c) Experimental traces with the FBC disabled (open loop, left) and enabled (closed loop, right); the controller suppresses phase fluctuations and locks the output powers.

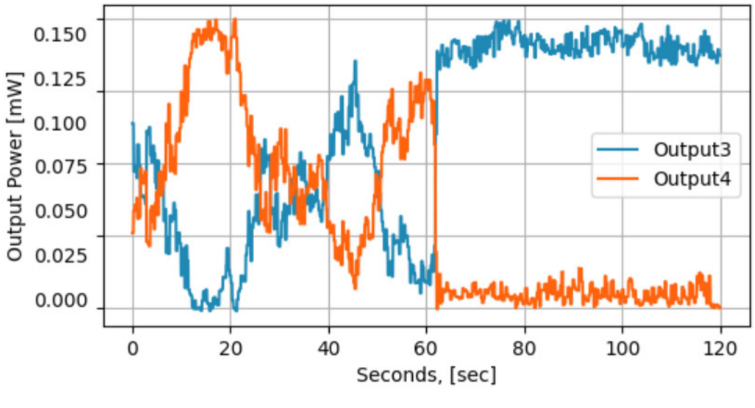

Figure 4. Long-term trace of the 2×2 Hadamard operation. The FBC is enabled at $t = 60$ s; thereafter the powers on outputs 3 and 4 lock to their ideal values and remain steady.

result in only slight phase changes. In contrast, around $\pi/2$ the phase response exhibits a steep gradient, making the system highly sensitive to even minor errors. By anchoring the calibration at the more robust cross (0) and bar (π) points, we effectively minimize the impact of phase noise and voltage fluctuations.

Overall, the updated calibration greatly enhances MZIs and PSs accuracy, ensuring that subsequent opti-

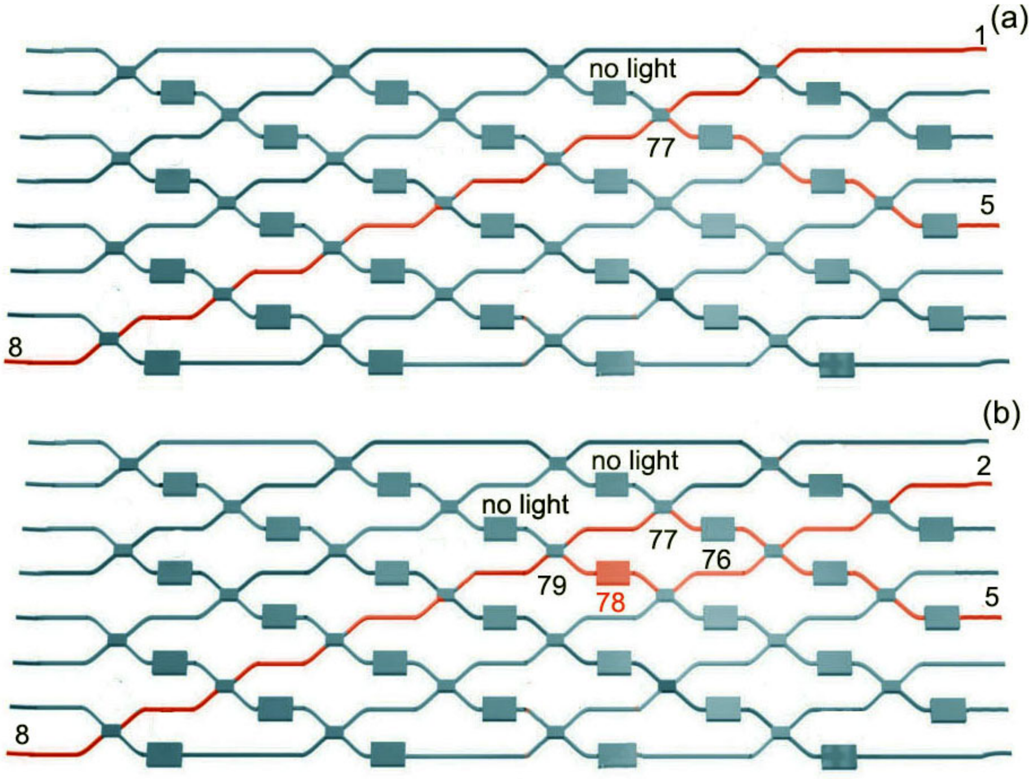

Figure 5. (a) Optical path for recalibrating MZI 77: light enters port 8 and exits ports 1 and 5, while the second input remains dark. Red lines indicate the optical paths in the PP used during calibration via input 8. (b) Schematic representation of the calibration setup for PS 78.

cal transformations meet the fidelity requirements of advanced photonic computing and quantum-information protocols.

4.2 Calibration of external phase shifters

The external phase shifters are recalibrated with the arrangement shown in Fig. 5(b). Light is launched into port 8, while the neighbouring MZIs 79 and 12 are frozen at $\theta = \pi/2$, turning them into 50/50 couplers. We then change the phase of PS 78 from 0 to 2π and record the powers at outputs 2 and 5. Fitting the resulting transfer curve to the ideal response yields the corrective offset Δ_{clb}.

Figure 6(c, d) illustrates the calibration results for PS 20. Before calibration (c) the measured traces diverge significantly from theory; after a single iteration (d) they coincide, reducing the mean phase error from $4.8\%\pi$ to $1.5\%\pi$.[26]

Conclusion

We have demonstrated that the principal roadblock to high-fidelity operation of silicon-nitride photonic processors fan induced phase noise can be overcome in real time. A self-referenced feedback loop acting on on-chip phase shifter PS 22 suppresses the residual phase velocity by more than an order of magnitude, unlocking stable multi-port interference across the mesh. When the loop is engaged, a programmed 2×2 Hadamard gate remains locked to its ideal power distribution for extended durations, providing the first direct evidence of repeatable matrix–vector multiplication on this platform.

Complementing the active stabilisation, we have introduced a calibration protocol that iteratively compares measured and ideal transfer matrices, then retunes every Mach–Zehnder interferometer and external phase shifter. A single calibration pass halves the mean phase error—from $3.8\%\pi$ to $1.7\%\pi$ for internal MZIs and from $4.8\%\pi$

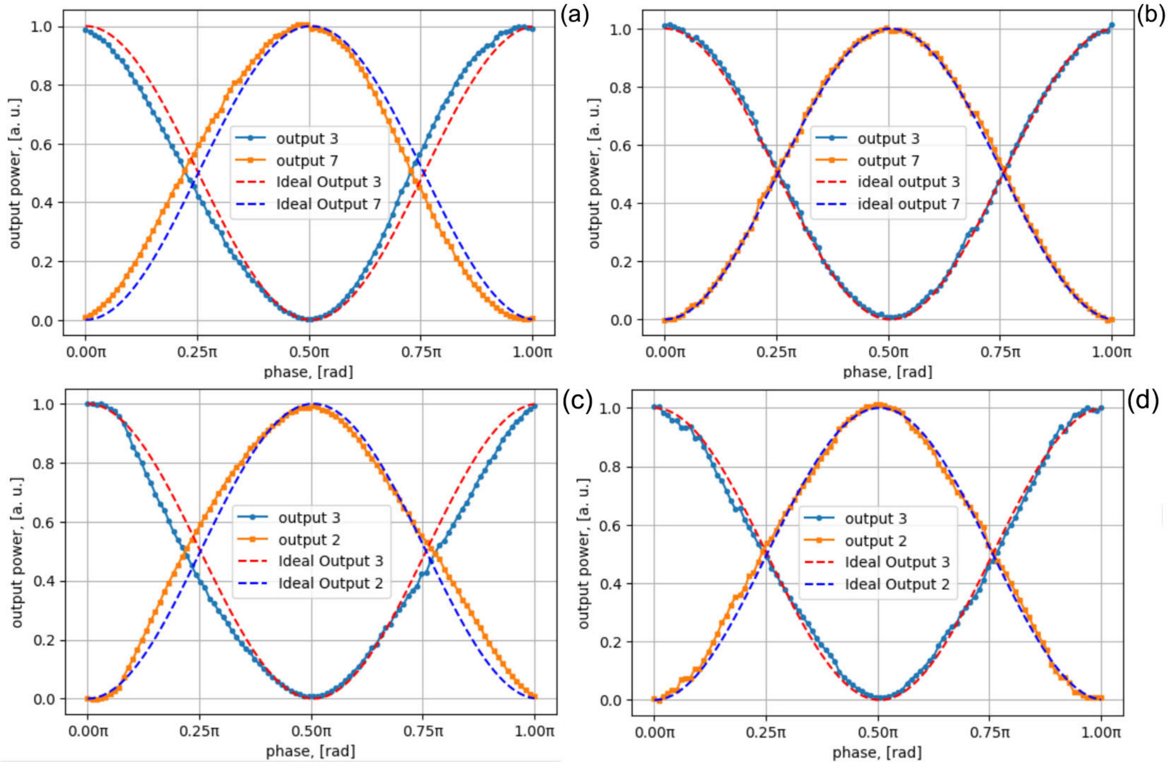

Figure 6. Calibration examples. (a)–(b) MZI 14: normalised output power (solid) versus ideal (dashed) before and after recalibration. (c)–(d) PS 20: measured response before and after correction, showing the same convergence to theory.

to 1.5%π for external shifters—while anchoring the fit at the inherently stable *cross* (0) and *bar* (π) points minimises sensitivity to voltage noise.

Taken together, high-speed feedback and systematic recalibration elevate both the stability and fidelity of reconfigurable photonic processors, closing the gap between laboratory prototypes and deployable hardware. These results lay a practical foundation for large-scale optical computing, quantum signal processing, and next-generation joint-detection receivers, and they highlight a clear roadmap: faster detectors and fully integrated control electronics will further widen the operational bandwidth, enabling ever larger meshes without sacrificing precision.

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Disclosures

The author declares no conflict of interest.

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