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ORIGINAL RESEARCH

Efficient switched-capacitor multilevel inverters for high-power solar photovoltaic systems

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Abstract

Switched-capacitor multilevel inverters are suitable topologies for renewable and sustainable energy due to a low number of dc-link voltages. This article presents two extendable configurations for switched-capacitor multilevel inverters to be applied to solar photovoltaic systems. The first extendable configuration applies only to two DC supplies, and the number of levels is increased by connecting several capacitors in series, while the second extendable configuration uses a combination of DC sources and capacitors. The proposed inverters have a self-voltage balancing capability, and they reduce the voltage stress of switches, which leads to a reduction in the value of switching losses. The comparison indicates that both extendable topologies have advantages over most reported multilevel inverters, such as a low number of capacitors and semiconductors, low voltage stress, high boost factors, and a low-cost factor. An efficiency assessment is also presented, which shows the efficiency of the proposal is higher than recent topologies. The proposed inverter is tested and simulated for a high-power solar photovoltaic system that shows it possesses excellent performance with a high-quality output waveform. The functionality of the proposal is tested and evaluated by building a laboratory prototype.

1 | INTRODUCTION

The benefits of solar photovoltaic (PV) technology are that there are no existing moving parts, a long lifetime, and no need for maintenance [1, 2]. The main core of a PV system is a power inverter, which is the interface between the PV panel and the load/grid. Multilevel Inverters (MLIs) are suitable topologies to operate high-power PV systems because they overcome the voltage rating constraint of power switches, making them more efficient and cheap [3, 4]. Another benefit of MLIs is that they use several semiconductor components to generate high voltage levels, which results in low voltage distortion, low dv/dt, and a low natural point voltage [5, 6]. Generally, classical MLIs are categorized into three inverter groups, consisting of switched-diode base MLIs (SD-MLIs), DC-Source base MLIs (DCS-MLIs), and switched-capacitor based MLIs (SC-MLI). Switched-diode base MLIs use discrete diodes instead of switches to decrease the switching device count [7, 8]. The second group is dc source base MLIs that use multiple independent dc voltage sources. Therefore, they don't need any capacitors to regulate DC link voltage and can operate in all resistive and resistive-inductive load ranges [9–11]. The third group is switched-capacitor MLIs that only need a single or a few DC sources to generate high voltage levels and other sources are replaced by capacitors. Due to the use of single or fewer DC power supplies, SC-MLIs have recently attracted the attention of many academics among all types of multilevel inverters [12]. These MLIs, like other topologies (SD-MLI and DCS-MLI), require a significant number of components (power semiconductors, drivers, and capacitors) to produce high voltage levels, resulting in complex control and reduced efficiency [13]. In addition, several of the SC-MLI topologies provided require a proper algorithm to manage the capacitor voltages, making them more expensive [14]. Furthermore, in low input power supply applications (such as PV systems), a high amount of current drawn from the DC supplies can reduce the power

level of SC-MLIs because some power semiconductors must withstand a high current rating [15]. Recently, numerous MLI topologies have been presented for renewable energy sources in literature with an emphasis on element count reduction, low input DC supplies, low tolerate voltage on power switches, control approaches, etc [16–21].

Two 25-level MLI topologies have been presented in [16, 17]. Ten switches and three asymmetric DC sources are used in the first reduced structure in [16] to provide fifteen voltage levels. Although this topology can create twenty-five voltage levels with twelve power switches, the stress voltage of the power switches is high, and the separated DC links cannot be replaced by capacitors because of the design of the configuration. The second presented 25-level topology in [17] switches two unequal DC voltage sources through four capacitors and fourteen IGBTs.

The advantage of this topology is the voltage control of input capacitors without the use of any extra balancing circuits. A 25-level MLI structure has been reported in [18, 19] that employs four DC link voltages and ten switches. By using a low driver circuit count, [18, 19] reduced control complexity. For PV systems, the input DC sources of this MLI require four independent capacitors, which increases the inverter's elements, size, and overall cost. The presented 25-level inverter in [19] has the same circuit as [18], but the bidirectional switches have been replaced with one IGBT and four diodes, reducing the number of IGBTs to ten, but with six extra diodes. The disadvantage of this topology is similar to [18] due to the use of four DC sources that increase the elements. [20] suggested a cascading SC-MLI by proposing a basic unit that generates five voltage levels (consisting of seven IGBTs, and two capacitors) with the objective of low blocking voltage on semiconductor devices. It can generate a 25-level by cascading two basic units (fourteen IGBTs and four capacitors), which is still a high IGBT and capacitor count, which makes it have high stored energy and high cost.

A modified PUC has been presented in [21]. This topology replaces the capacitors of the PUC by using multiple DC voltage sources. This topology reduces the power electronics parts while increasing the number of levels. It has the problem of requiring several DC link voltages without the use of capacitors. [22] suggested multiple SC-MLI topologies that remove the requirement for H-bridge inverters. Instead of two H-bridge inverters, this topology employs six power switches to reduce the number of components. [23] introduced a multiple SC-MLI that uses asymmetric switched-capacitor units to minimize the number of elements. Two switches, one discrete diode, and one DC link voltage, along with a capacitor, are included in each MLI basic unit. As a result, a large number of capacitors and DC sources are employed to consider a wide range of voltage levels. [24, 25] two switched-capacitor MLI topologies have been reported. The first MLI [24] reduces the number of switches and voltage stress, but it is difficult to generate high voltage levels because it is non-scalable and has a large number of capacitors. The second SC-MLI [25] has been offered as an enhanced basic unit that makes use of a small number of power diodes and the capacitor's current path. For PV systems, [26] proposed a multi-source SC-MLI topology. Asymmetric multiple DC sources and switched capacitors have been used in the described structure, which is charged in parallel mode at the highest DC-link voltage and discharged in series mode. An H-bridge inverter is also used to produce negative levels. An extendable MS-SCMLI with the capability of the self-balancing capacitor is introduced in [27]. The basic topology of this structure uses more than twelve power switches to generate 25-level, therefore to generate more voltage levels it requires a large number of elements and capacitors. Also, the boosting factor of this topology is low which is not suitable for solar PV systems.

A hybrid switched-capacitor MLI is introduced in [28]. The introduced basic topology is using a single dc source and several capacitors to obtain a high number of levels. The disadvantage of this topology is using several capacitors and power electronics devices because the capacitors are charged only in the value of input dc sources. The presented cascaded topologies use n number of dc sources and n number of capacitors, so they need more asymmetric dc sources and capacitors to increase voltage levels. In addition, in the presented cascaded topology the dispersed value of dc voltage sources are far (1,5,125,...) making the control of dc-link voltage more difficult for Solar PV applications. A symmetric cascaded SC-MLI has been presented for a high-frequency AC distribution system in [29]. The drawback of this MLI is using several dc voltage sources and operating in symmetric operation mode. Therefore, the capacitors are charged in symmetric values like [28] which requires a lot of switches and capacitors to create a high number of voltage levels. In addition, the boosting factor of these topologies is low which is an essential factor for solar PV systems. An extended high step-up switched-capacitor MLI is reported in [30], which uses only two dc sources and several switched-capacitor units. It uses an improved H-bridge circuit (six switches) to change voltage polarity. The capacitors in this extended topology are charged in symmetric value at the input dc voltage source, so its boosting factor is low which is not a good topology for solar PV systems. In addition, it needs more devices to generate more voltage levels which reduced the efficiency of the inverter. Furthermore, since this MLI only uses two dc-link voltages to generate high voltage levels, it is lost flexibility to design especially when it is applied to PV solar systems.

In this paper, first is a basic switched-capacitor multilevel inverters topology with the capability of balancing capacitor voltage automatically. Then the basic topology is extended into two different configurations. The extended topologies are proposed for multilevel inverters. For each extended topology, the magnitude of dc sources is presented so that they can generate all voltage levels (even and odd). One of the features of the proposed structures is the self-balancing voltage of the capacitors, so they do not need any sensor or special control algorithm. To determine the benefits and drawbacks of the proposed topology with other MLIs the performance parameters such as the number of elements and voltage stress of the switches are extracted and compared with the state-of-art MLI topologies.

In addition, the optimal design of the proposed topologies for different objectives like minimizing the number of dc sources, power switches, and voltage stress of the switches are

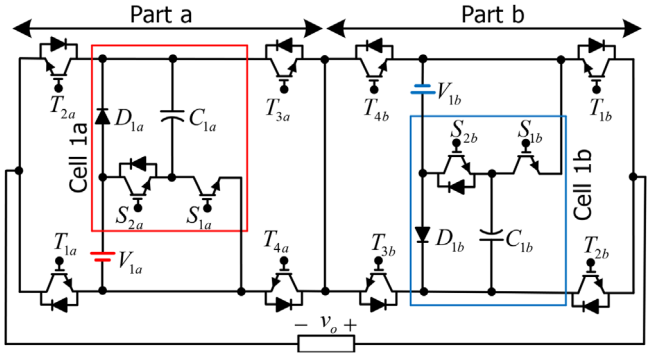


FIGURE 1 Proposed basic MC-SCMLI topology

presented. The efficiency of the proposed basic topology for different output power is obtained and compared with four recently switched-capacitor MLI topologies, which confirm efficiency improvement. In the following, the application of the proposed topology for a solar system is investigated in two cases: stand-alone and grid-connected with the necessary control scheme. Lastly, the hardware and software findings are presented to demonstrate the functionality of the proposal.

2 | PROPOSED BASIC MULTICELL SWITCHED-CAPACITOR MLI

The schematic power circuit of the suggested basic multicell SC-MLI (MC-SCMLI) structure is exhibited in Figure 1. According to the switched-capacitor idea, the suggested topology is made up of two parts (part-a and part-b). It means that two capacitors (C_{1a}, C_{1b}) can be charged in parallel mode (without any extra balancing circuit) through input dc-links (V_{1a}, V_{1b}), respectively, which is one of the main advantages of the suggested structure. Therefore, it comprises two DC link voltages, two capacitors, and two diodes that are connected by twelve unidirectional switches. The proposed MC-SCMLI has several benefits, including the ability to create both positive and negative voltage levels, eliminating the requirement for an h-bridge inverter to shift polarity, and reducing switch voltage stress.

In the suggested basic structure, all switches operate in complementary modes, which provide paths that produce positive and negative voltage levels. The suggested basic MLI creates 9 levels if the number of two dc-links is selected equally ($V_{1a} = V_{1b} = V_{dc}$). It is possible to achieve various voltage levels with the same number of elements if the magnitudes of the two DC-links are determined unequally. As a consequence, the suggested basic MLI produces distinct voltage levels by choosing values of V_{1b} different amounts of V_{1a}, as shown in Table 1. Table 2 summarizes all the possible switching states of the used switches for making each voltage level.

The type and rating of power semiconductors are determined by the standing voltage (SV) factor. Thus, in the suggested basic MC-SCMLI, the highest stress voltage of each power switch can

TABLE 1 Selection of DC link voltage to create voltage levels differently within the suggested MC-SCML

	V_{1a}	V_{1b}	$V_{omax} = 2(V_{1a} + V_{1b})$	$N_{level} = 2V_{omax} + 1$
1	V_{dc}	$2V_{dc}$	$6V_{dc}$	13
2	V_{dc}	$3V_{dc}$	$8V_{dc}$	17
3	V_{dc}	$4V_{dc}$	$10V_{dc}$	21
4	V_{dc}	$5V_{dc}$	$12V_{dc}$	25

TABLE 2 All possible switching states of the suggested MC-SCMLI structure

States	On switches	C_{1a}	C_{1b}	Output voltage
1	$T_{1a}, T_{4a}, T_{1b}, T_{4b}$	–	–	0
2	$T_{1a}, T_{4a}, T_{2b}, T_{3b}$	–	–	
3	$T_{2a}, T_{3a}, T_{1b}, T_{4b}$	–	–	
4	$T_{2a}, T_{3a}, T_{2b}, T_{3b}$	–	–	
5	$T_{1a}, T_{3a}, S_{1a}, T_{2b}, T_{3b}$	↑	–	$+V_{dc}$
6	$T_{1a}, T_{3a}, S_{1a}, T_{1b}, T_{4b}$	↑	–	
7	$T_{2a}, T_{4a}, S_{1a}, T_{2b}, T_{3b}$	↑	–	$-V_{dc}$
8	$T_{2a}, T_{4a}, S_{1a}, T_{1b}, T_{4b}$	↑	–	
9	$T_{1a}, T_{3a}, S_{2a}, T_{2b}, T_{3b}$	↓	–	$+2V_{dc}$
10	$T_{1a}, T_{3a}, S_{2a}, T_{1b}, T_{4b}$	↓	–	
11	$T_{2a}, T_{4a}, S_{2a}, T_{2b}, T_{3b}$	↓	–	$-2V_{dc}$
12	$T_{2a}, T_{4a}, S_{2a}, T_{1b}, T_{4b}$	↓	–	
13	$T_{2a}, T_{4a}, S_{2a}, T_{1b}, T_{3b}, S_{1b}$	↓	↑	$+3V_{dc}$
14	$T_{1a}, T_{3a}, S_{2a}, T_{2b}, T_{4b}, S_{1b}$	↓	↑	$-3V_{dc}$
15	$T_{2a}, T_{4a}, S_{1a}, T_{1b}, T_{3b}, S_{1b}$	↑	↑	$+4V_{dc}$
16	$T_{1a}, T_{3a}, S_{1a}, T_{2b}, T_{4b}, S_{1b}$	↑	↑	$-4V_{dc}$
17	$T_{2a}, T_{3a}, T_{1b}, T_{3b}, S_{1b}$	–	↑	$+5V_{dc}$
18	$T_{1a}, T_{4a}, T_{1b}, T_{3b}, S_{1b}$	–	↑	
19	$T_{2a}, T_{3a}, T_{2b}, T_{4b}, S_{1b}$	–	↑	$-5V_{dc}$
20	$T_{1a}, T_{4a}, T_{2b}, T_{4b}, S_{1b}$	–	↑	
21	$T_{1a}, T_{3a}, S_{1a}, T_{1b}, T_{3b}, S_{1b}$	↑	↑	$+6V_{dc}$
22	$T_{2a}, T_{4a}, S_{1a}, T_{2b}, T_{4b}, S_{1b}$	↑	↑	$-6V_{dc}$
23	$T_{1a}, T_{3a}, S_{2a}, T_{1b}, T_{3b}, S_{1b}$	↓	↑	$+7V_{dc}$
24	$T_{2a}, T_{4a}, S_{2a}, T_{2b}, T_{4b}, S_{1b}$	↓	↑	$-7V_{dc}$
25	$T_{2a}, T_{4a}, S_{2a}, T_{1b}, T_{3b}, S_{2b}$	↓	↓	$+8V_{dc}$
26	$T_{1a}, T_{3a}, S_{2a}, T_{2b}, T_{4b}, S_{2b}$	↓	↓	$-8V_{dc}$
27	$T_{2a}, T_{4a}, S_{1a}, T_{1b}, T_{3b}, S_{2b}$	↑	↓	$+9V_{dc}$
28	$T_{1a}, T_{3a}, S_{1a}, T_{2b}, T_{4b}, S_{2b}$	↑	↓	$-9V_{dc}$
29	$T_{2a}, T_{3a}, T_{1b}, T_{3b}, S_{2b}$	–	↓	$+10V_{dc}$
30	$T_{1a}, T_{4a}, T_{1b}, T_{3b}, S_{2b}$	–	↓	
31	$T_{2a}, T_{3a}, T_{2b}, T_{4b}, S_{2b}$	–	↓	$-10V_{dc}$
32	$T_{1a}, T_{4a}, T_{2b}, T_{4b}, S_{2b}$	–	↓	
33	$T_{1a}, T_{3a}, S_{1a}, T_{1b}, T_{3b}, S_{2b}$	↑	↓	$+11V_{dc}$
34	$T_{2a}, T_{4a}, S_{1a}, T_{2b}, T_{4b}, S_{2b}$	↑	↓	$-11V_{dc}$
35	$T_{1a}, T_{3a}, S_{2a}, T_{1b}, T_{3b}, S_{2b}$	↓	↓	$+12V_{dc}$
36	$T_{2a}, T_{4a}, S_{2a}, T_{2b}, T_{4b}, S_{2b}$	↓	↓	$-12V_{dc}$

be estimated as:

$$SV_{T_{1a}} = SV_{T_{2a}} = SV_{T_{3a}} = SV_{T_{4a}} = 2V_{1a}, \quad (1)$$

$$SV_{T_{1b}} = SV_{T_{2b}} = SV_{T_{3b}} = SV_{T_{4b}} = 2V_{1b}, \quad (2)$$

$$SV_{S_{1a}} = SV_{S_{2a}} = V_{1a}, \quad (3)$$

$$SV_{S_{1b}} = SV_{S_{2b}} = V_{1b}. \quad (4)$$

Therefore, the total standing voltage of basic structure TSV_{Basic} is:

$$TSV_{Basic} = 10(V_{1a} + V_{1b}) = \frac{5}{2}(N_{level} - 1)V_{1a}. \quad (5)$$

3 | PROPOSED EXTENDED MC-SCMLI TOPOLOGIES

As the number of levels in multilevel inverters increases, they need more power switches to approach the sinusoidal waveform with less harmonic content. Therefore, MLIs require more gate driver circuits which control of them will be more complex. Furthermore, by increasing the number of levels the conduction losses of MLIs are increased which causes the efficiency to be decreased. An extended switched-capacitor MLI is introduced in [30]. This topology has drawbacks such as only using two dc sources (low design flexibility), a low boosting factor (capacitors have symmetric values), and a high number of capacitors and power semiconductors to generate a large number of levels. The proposed extended structures are designed in such a way that it has higher flexibility to design (due to using two or more dc sources) and they provide a high boosting factor (capacitors have asymmetric value). Since they operate asymmetrically the need for power electronics components is reduced. In addition, they have a low dispersed dc-link voltage ratio than previously published SC-MLIs [28, 29] which causes their control simpler for solar PV applications.

3.1 | Suggested first configuration

The first suggested extendable topology can be configured into two shapes. In the first shape, the capacitors of each cell in each part are charged in a symmetric pattern in the magnitude of the input dc-links. In the second shape, the capacitors of each cell in each part are charged in an asymmetric pattern.

3.1.1 | Symmetric shape

Figure 2 shows the symmetric shape of the first suggested MLI (FS-MLI). It comprises of two parts, part-a, and part-b. Each cell is comprised of two switches, one capacitor, and one diode.

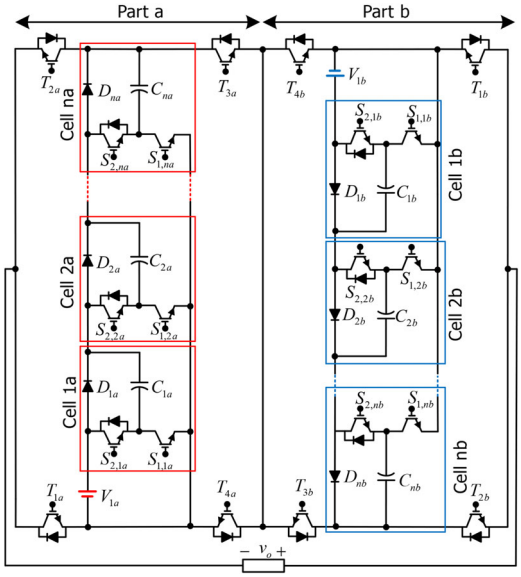


FIGURE 2 Symmetric shape of proposed first MLI configuration

All capacitors in part-a are charged at the magnitude of V_{1a} by ON-state switches ($S_{1,1a}, \ldots, S_{1,na}$). Similarly, all capacitors part-b are charged at the magnitude of the dc voltage of V_{1b} by turning on the switches ($S_{1,1b}, \ldots, S_{1,nb}$). Hence, the magnitude of DC link voltage can be considered as follows in order to achieve a large number of levels:

$$V_{1a} = V_{C_{1a}} = \cdots = V_{C_{na}} = V_{dc}, \quad (6)$$

$$V_{1b} = V_{C_{1b}} = \cdots = V_{C_{nb}} = (2N_{cell,a} + 3)V_{1a}. \quad (7)$$

Therefore, the symmetric shape of the first suggested configuration requires only two dc link voltages, the quantity of cells ($N_{cell,FS}$), capacitors ($N_{Cap,FS}$), IGBTs ($N_{IGBT,FS}$), driver circuits ($N_{Driver,FS}$), discrete diodes ($N_{Diode,FS}$), and voltage levels ($N_{L,FS}$) can be calculated as follows:

$$N_{cell,FS} = N_{cell,a} + N_{cell,b}, \quad (8)$$

$$N_{Cap,FS} = N_{cell,FS} = N_{cell}, \quad (9)$$

$$N_{IGBT,FS} = N_{Driver,FS} = 2N_{cell} + 8, \quad (10)$$

$$N_{Diode,FS} = 2N_{cell} + 10, \quad (11)$$

$$N_{L,FS} = (N_{cell} + 3)^2. \quad (12)$$

It should be noted that the above equations are derived from the assumption that $N_{cell,a}$=$N_{cell,b}$. The stress voltage of switches involving part-a capacitors ($S_{1,1a}, S_{2,1a}, \ldots, S_{1,na}, S_{2,na}$) equals the

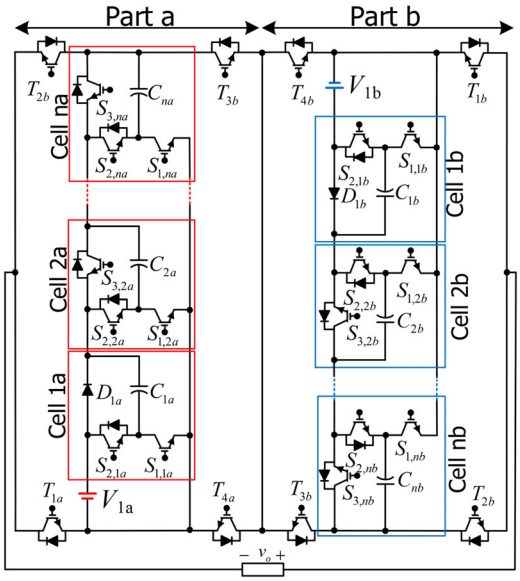


FIGURE 3 Asymmetric shape of first proposed configuration

capacitor voltages, which can be expressed as follows:

$$V_{S_{1,ja}} = V_{S_{2,ja}} = N_{cell,a} V_{1a}. \tag{13}$$

The stress voltage four switches of (T_{1a}, T_{2a}, T_{3a}, T_{4a}) for part-a is equal to:

$$V_{T_{1a}} = V_{T_{2a}} = V_{T_{3a}} = V_{T_{4a}} = (N_{cell,a} + 1) V_{1a}. \tag{14}$$

As a result, the maximum standing voltage for part-a $SV_{FS,a}$ can be obtained based on eqs. (13) and (14) as:

$$SV_{F,a} = [6N_{cell,a} + 4] V_{1a}. \tag{15}$$

Similarly, the standing voltage of part-b ($SV_{FS,b}$) is:

$$SV_{FS,b} = [6N_{cell,b} + 4] V_{1b}. \tag{16}$$

Therefore, the total SV of the suggested first symmetric structure, TSV_{FS-MLI} can be expressed as:

$$TSV_{FS-MLI} = SV_{FS,a} + SV_{F,b} = [3N_{cell} + 4](V_{1a} + V_{1b}). \tag{17}$$

3.1.2 | Asymmetric shape

Figure 3 displays the asymmetric shape of the first MLI (FA-MLI). In this configuration, we replaced the diodes with IGBTs, so each capacitor is connected by three switches. Hence, the capacitors of part-a and part-b are charged in an asymmetric pattern, as follows:

$$V_{C_{ja}} = 2^{j-1} V_{1a}, \tag{18}$$

$$V_{C_{jb}} = 2^{j-1} V_{1b}. \tag{19}$$

Here j is the number of cells. The DC voltage source amplitudes to achieve a high quantity of levels are chosen as follows:

$$V_{1a} = V_{dc}, \tag{20}$$

$$V_{1b} = (2^{N_{cell,a}+1} + 1) V_{1a}. \tag{21}$$

As a result, the quantity of DC link voltage is two for the asymmetric shape, and the quantities of cells ($N_{cell,FA}$), capacitors ($N_{Cap,FA}$), diodes ($N_{Diode,FA}$) are obtained from eqs. (8), (9) and (11), respectively. The number of IGBTs ($N_{IGBT,FA}$), drivers ($N_{Driver,FA}$) and levels ($N_{L,FA}$) are obtained as:

$$N_{IGBT,FA} = N_{Driver,FA} = 3N_{cell} + 6, \tag{22}$$

$$N_{L,FA} = \left(2^{\frac{N_{cell}}{2}+1} + 1\right)^2. \tag{23}$$

The total SV of asymmetric shape (TSV_{FA-MLI}) can be calculated within eqs. (13)-(16), therefore, it can be expressed as:

$$TSV_{FA-MLI} = [7\left(2^{\frac{N_{cell}}{2}}\right) - 4](V_{1a} + V_{1b}). \tag{24}$$

It is worth mentioning since the switched-capacitor cells in both parts of Figures 2 and 3 are located inside of the power switches of two H-bridge circuits. Therefore, vertical or horizontal expansion does not make a difference in the advantages of the proposed extended structures, and the same results are obtained in both cases.

3.2 | Suggested second configuration

Figure 4 illustrates the power circuit of the second suggested MLI (S-MLI). As it is obvious, the second MLI uses multiple asymmetric DC voltage sources and capacitors. Each cell comprises one DC source, one capacitor, four switches, and one diode. The capacitors in each cell are charged with the value of the DC link voltage involved. Therefore, the amplitude of the DC-link voltage will be:

$$\begin{aligned} &V_{1a} = V_{C_{1a}} = V_{dc}, V_{2a} = V_{C_{2a}} = 2V_{1a}, \\ &V_{3a} = V_{C_{3a}} = 3V_{1a}, \ldots, V_{na} = V_{C_{na}} = nV_{1a}. \end{aligned} \tag{25}$$

And for part-b are considered as:

$$\begin{aligned} &V_{1b} = V_{C_{1b}} = \left(2N_{cell,a}^2 + 2N_{cell,a} + 1\right) V_{1a}, \\ &V_{2b} = V_{C_{2b}} = 2V_{1b}, V_{3b} = V_{C_{3b}} = 3V_{1b}, \ldots, V_{nb} = V_{C_{nb}} = nV_{1b}. \end{aligned} \tag{26}$$

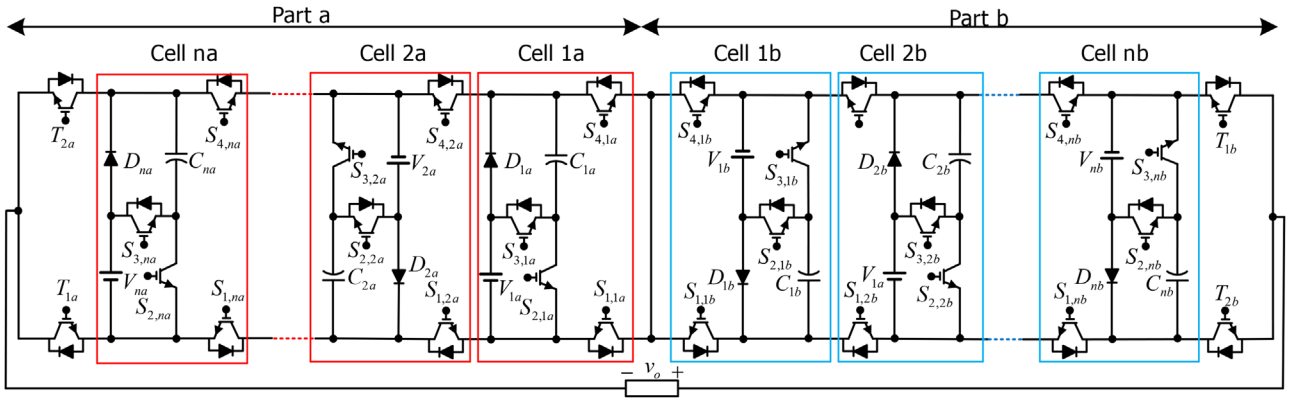


FIGURE 4 Second proposed MLI configuration

The number of components and voltage levels ($N_{L,S}$) for this configuration are obtained as:

$$N_{Cap,S} = N_{DC,S} = N_{cell} = N_{cell,a} + N_{cell,b}, \tag{27}$$

$$N_{IGBT,S} = N_{Driver,S} = 4N_{cell} + 4, \tag{28}$$

$$N_{Diode,S} = 5N_{cell} + 4, \tag{29}$$

$$N_{L,S} = \left(\frac{N_{cell}^2}{2} + N_{cell} + 1\right)^2. \tag{30}$$

In this configuration, the total standing voltage of the switches is:

$$TSV_{S-MLI} = \left(\frac{6N_{cell}^2}{4} + 2N_{cell}\right)(V_{1a} + V_{1b}). \tag{31}$$

4 | OPTIMAL DESIGN CONFIGURATIONS

In cascaded MLI structures, the aim of obtaining an optimum design is to minimize component count to achieve the desired voltage levels. Two factors, (k) and (N_{cell}), influence the peak amplitudes of the output voltage when determining an optimal topology. The quantity of cascaded basic units is k. We use the variable (N_{cell}) to determine the best design and (k) to determine the output voltage peak. By considering the following relationship to obtain the maximum voltage levels in the cascaded configurations:

$$N_{cell,1} = N_{cell,2} = \cdots = N_{cell,k} = N_{cell}. \tag{32}$$

So, the components and levels counts, and TSV for the first suggested configuration will be obtained as:

$$N_{IGBT,F,cas} = N_{Driver,FA,cas} = 3k(N_{cell} + 2), \tag{33}$$

$$N_{Cap,F,cas} = kN_{cell}, \tag{34}$$

$$N_{DC,F,cas} = 2k, \tag{35}$$

$$N_{L,F,cas} = \left(2^{\frac{N_{cell}}{2}+1} + 1\right)^{2k}, \tag{36}$$

$$TSV_{F,cas} = V_{dc} \times \left(\frac{7(2^{\frac{N_{cell}}{2}}) - 4}{4}\right)(N_{L,FA,cas} - 1). \tag{37}$$

Also, for the second suggested cascaded structure, they will be obtained as:

$$N_{IGBT,S,cas} = N_{Driver,S,cas} = 2k(2N_{cell} + 2), \tag{38}$$

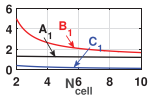
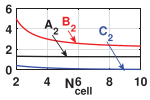
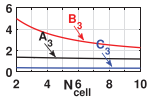
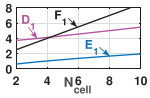
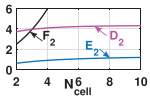
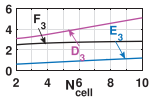
$$N_{Cap,S,cas} = N_{DC,S,cas} = kN_{cell}, \tag{39}$$

$$N_{L,S,cas} = \left(\frac{N_{cell,i}^2}{2} + N_{cell,i} + 1\right)^{2k}, \tag{40}$$

$$TSV_{S,cas} = V_{dc} \times \left(\frac{6N_{cell} + 8}{2N_{cell} + 4}\right)(N_{L,S,cas} - 1). \tag{41}$$

To obtain optimal configurations, there are two approaches. In the first approach, the quantity of components and TSV are constant. Through the second approach to providing the desired levels, the component counts and the TSV value are optimized. Table 3 shows the outcomes of the two proposed approaches for obtaining optimal topologies for both cascaded configurations. In order to make a large number of levels, in the first approach, all indexes (A1, B1, C1), (A2, B2, C2), and (A3, B3, C3) should have a maximum value. Figures 1–3 inside Table 3 are labeled $N_{cell} \geq 2$. All indexes, as shown in these figures, reach their maximum at N_{cell}=2. The second approach is to optimize the component counts and TSV's value to have a fixed number of levels. As can be seen from Table 3 and Figures 4–6, the number of cells for the first and second

TABLE 3 Optimal design of the suggested first and second cascaded configurations

Configurations	First approach: Maximizing N_L with constant N_{com} and TSV		N_{cell}	Second approach: Minimizing N_{comp} with constant N_L and TSV	
First MLI (Sym)	$N_{L,FS,cas} = \underbrace{[(N_{cell}+3)^{\frac{1}{N_{cell}+4}}]}_{A_1}{}^{N_{IGBT}}$		2	$\frac{N_{IGBT}}{lnN_{L,FS,cas}} = \frac{N_{cell}+4}{ln(N_{cell}+3)} = D_1$	
	$N_{L,FS,cas} = \underbrace{[(N_{cell}+3)^{\frac{2}{N_{cell}}}]}_{B_1}{}^{N_{Cap}}$		2	$\frac{N_{Cap}}{lnN_{L,F,cas}} = \frac{N_{cell}}{2[ln(N_{cell}+3)]} = E_1$	
	$\frac{N_{L,FS,cas}-1}{TSV_{FS,cas}/V_{dc}} = \frac{4}{3N_{cell}+4} = C_1$	Figure 1	2	$\frac{TSV_{FS,cas}}{V_{dc}(N_{L,F,cas}-1)} = \frac{3N_{cell}+4}{4} = F_1$	Figure 4
First MLI (Asym)	$N_{L,FA,cas} = \underbrace{[(2^{\frac{N_{cell}}{2}}+1)^{\frac{2}{3N_{cell}+6}}]}_{A_2}{}^{N_{IGBT}}$		2	$\frac{N_{IGBT}}{lnN_{L,FA,cas}} = \frac{3N_{cell}+6}{2[ln(2^{\frac{N_{cell}}{2}}+1)]} = D_2$	
	$N_{L,FA,cas} = \underbrace{[(2^{\frac{N_{cell}}{2}}+1)^{\frac{2}{N_{cell}}}]}_{B_2}{}^{N_{Cap}}$		2	$\frac{N_{Cap}}{lnN_{L,F,cas}} = \frac{N_{cell}}{2[ln(2^{\frac{N_{cell}}{2}}+1)]} = E_2$	
	$\frac{N_{L,FA,cas}-1}{TSV_{FS,cas}/V_{dc}} = \frac{4}{7(2^{\frac{N_{cell}}{2}})-4} = C_2$	Figure 2	2	$\frac{TSV_{FA,cas}}{V_{dc}(N_{L,F,cas}-1)} = \frac{7(2^{\frac{N_{cell}}{2}})-4}{4} = F_2$	Figure 5
Second MLI Topology	$N_{L,S,cas} = \underbrace{[(\frac{N_{cell}^2}{2}+N_{cell}+1)^{\frac{1}{2N_{cell}+2}}]}_{A_3}{}^{N_{IGBT}}$		2	$\frac{N_{Driver}}{lnN_{L,S,cas}} = \frac{2N_{cell}+2}{ln(\frac{N_{cell}^2}{2}+N_{cell}+1)} = D_3$	
	$N_{L,S,cas} = \underbrace{(\frac{N_{cell}^2}{2}+N_{cell}+1)^{\frac{2}{N_{cell}}}]}_{B_3}{}^{N_{Cap}}$		2	$\frac{N_{Cap}}{lnN_{L,F,cas}} = \frac{N_{cell}}{2[ln(\frac{N_{cell}^2}{2}+N_{cell}+1)]} = E_3$	
	$\frac{N_{L,S,cas}-1}{TSV_{F,cas}/V_{dc}} = \frac{2N_{cell}+4}{6N_{cell}+8} = C_3$	Figure 3	2	$\frac{TSV_{S,cas}}{V_{dc}(N_{L,S,cas}-1)} = \frac{6N_{cell}+8}{2N_{cell}+4} = F_3$	Figure 6

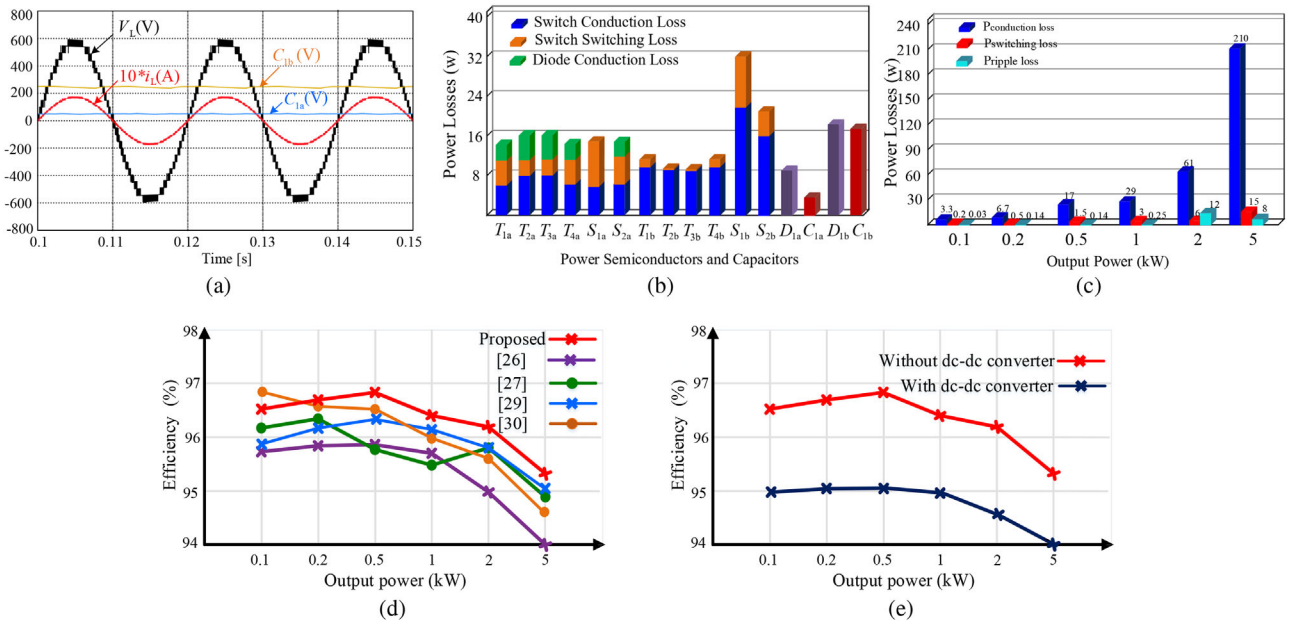


FIGURE 5 {R4-4} Simulation results of power losses and efficiency in PLECS software; (a) output waveform and capacitor voltages of proposed topology based on PSC-PWM; (b) power semiconductors and capacitor losses of proposed 25-level MS-SCMLI; (c) power loss distribution of the proposed topology at different power range; (d) efficiency comparison of proposed topology and presented 25-level MS-SCMLIs in [26,27] and [29,30]; (e) efficiency of the proposed topology with and without using boost converter in the input

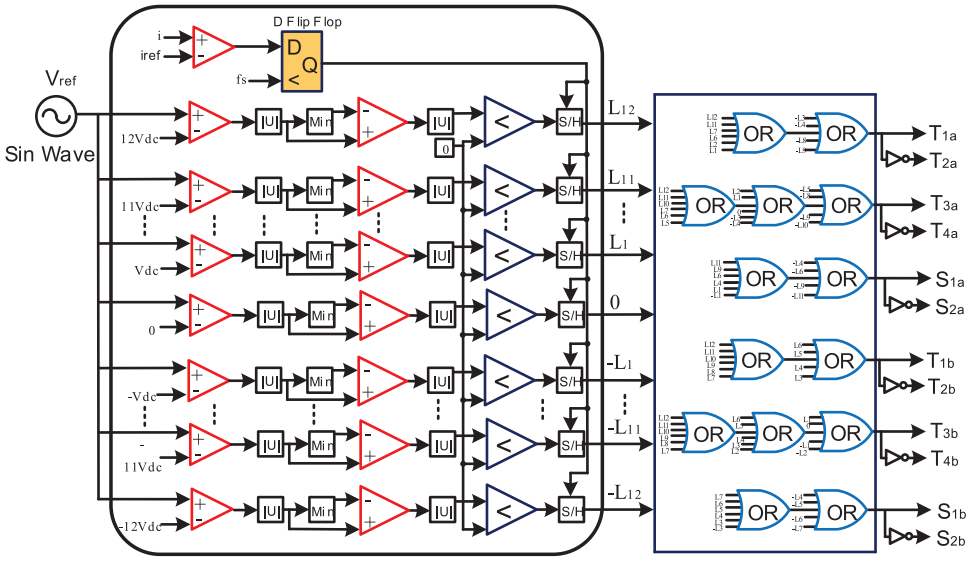


FIGURE 6 Block diagram of the proposed fundamental frequency modulation technique for the suggested 25-level multilevel inverter

suggested cascaded topologies in all indexes (D1, E1, F1), (D2, E2, F2), and (D3, E3, F3) is a minimum at N_{cell}=2.

5 | COMPARISON STUDIES

A fair comparison is set up between the suggested multilevel inverter configurations and other similar structures [8–30] to demonstrate the pros and cons of the proposal. The comparative study was performed on aspects of DC-link voltage count, capacitors, IGBTs, driving circuits, power diodes, the maximum on-state IGBTs, and the TSV magnitude. In addition, the suggested topologies are compared in terms of cost by defining a cost function (CF). The biggest part of the cost of multilevel inverters depends on components count and voltage stress, so CF can be expressed as:

$$CF = N_{DC} \times (N_{Cap} + N_{IGBT} + N_{Driver} + N_{Diode} + \alpha TSV_{p.u}), \quad (42)$$

where α is TSV's weighting factor. The comparison outcomes are shown in Table 4. As can see from this table, the number of levels is set from low-level (13) to high-level generation (289) based on the capability level generation of MLI topologies.

5.1 | 25-Level

to compare low levels, both proposed MLIs and [16–20], [26] and [28, 29] can generate 25 voltage levels, while other MLIs generate 17-level except for [21] and [24, 25], [29] which can generate 31-level. Most of the topologies to generate 25-level need more than 12 IGBT, except for [19] and [28], which uses a low number of 10 IGBT. Although the proposed topology requires the same or two more IGBTs than [19], it reduces the number of DC sources by 50% which leads to reducing the (CF/N_{Level}) significantly. Furthermore, in comparing the topologies that the 17-level generates except for [30], the proposed topology with the same component count can produce a 25-level that leads to high power quality and a small output filter size.

5.2 | 49-level and 81-level

the first proposed MLI (symmetric shape) and presented MLIs in [21–23], [25, 26] and [30] can generate 49-level. The proposed topology (CF/N_{Level}) has a lower value than other MLIs. The first proposed MLI (asymmetric shape) can produce an 81-level with 18 IGBTs at (CF/N_{Level}) 1.65, while MLI [25] produces a 71-level with 22 IGBTs at (CF/N_{Level}) 2.09. In addition [30] generate a 49-level with the same number of IGBTs as the proposal but it uses a high number of capacitors than the proposal. As a result, the proposed MLI reduces the number of components and cost factors for this level of generation.

5.3 | 169-level and 289-level

with the use of four DC sources, the second suggested MLI and [25] generate 169-level, and [22] produces 137-level. For this level, the second suggested MLI reduces the quantity of components more than [25] and needs two more IGBTs than [22], but it has a lower value in terms of (CF/N_{Level}) than other MLIs. The first proposed MLI (asymmetric shape) and [23] can generate 289-level. The proposed MLI requires two dc sources, six capacitors, and 24 IGBTs, and [23] needs four dc sources, four capacitors, and 20 IGBTs, so the dc link voltage count reduces considerably, which leads to having a low (CF/N_{Level}) as compared to [23].

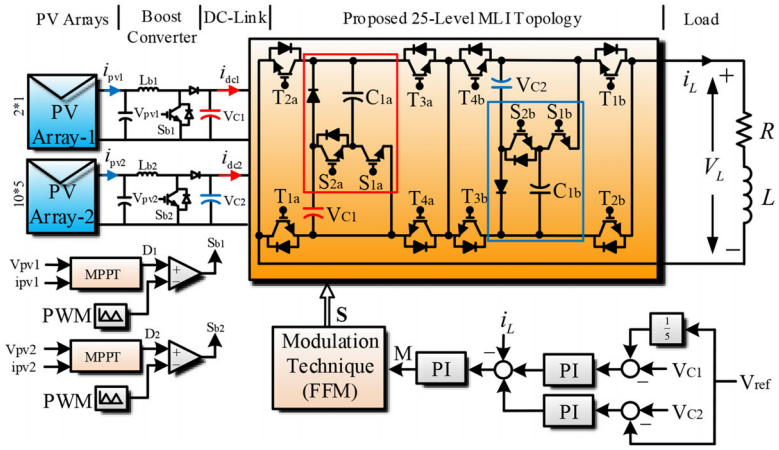


FIGURE 7 Standalone PV applications of the suggested inverter

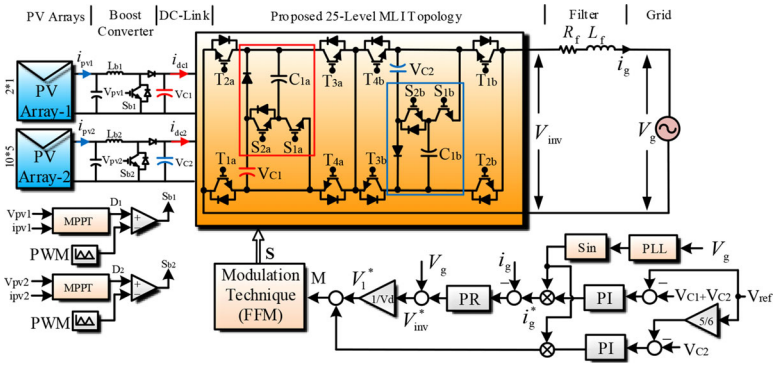


FIGURE 8 Grid-connected PV applications of the suggested inverter

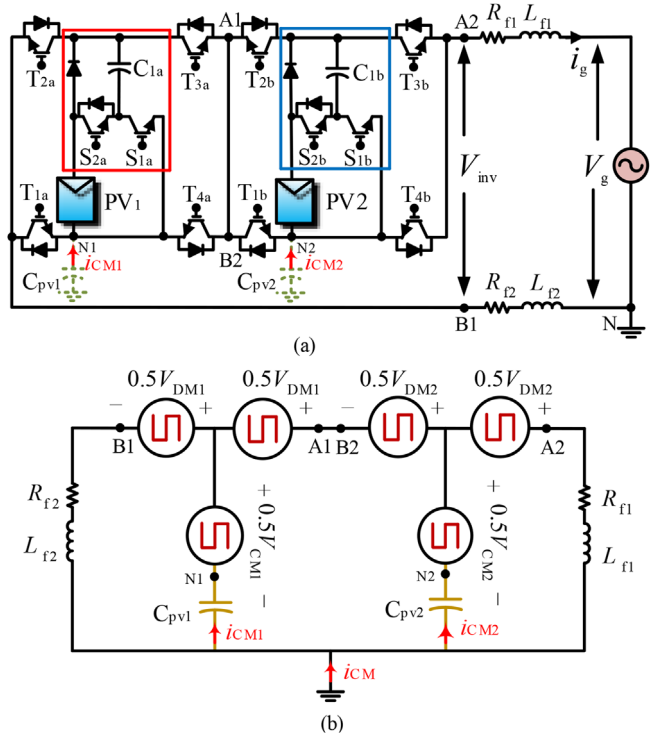


FIGURE 9 (a) Grid-connected of the proposed topology with considering parasitic capacitors; (a) equivalent circuit of the common mode voltage, differential mode voltage and leakage current of each part

6 | POWER LOSSES AND EFFICIENCY ASSESSMENT

A piece-wise linear electrical circuit simulation (PLECS) environment is used for the thermal loss study of the suggested structure. For the power switches of the proposed 25-level MS-SCMLI, we used IGBT IKFW60N60DH3E. The value of the DC link voltage is set to $V_1 = 50[V]$, $V_2 = 250[V]$. To obtain 5[KW] output power, the proposed inverter's output is coupled to a pure R-load. The value of R_{on} for the IGBTs and discrete diodes in thermal modeling is determined from the voltage-current curve in the datasheet of the used IGBT and diode. To show the switching losses of the power semiconductors, a high-frequency phase-shift carrier PWM (PSC-PWM) approach is adjusted for the control of the proposed topology. The output waveform and capacitor voltages that correspond to the PSC-PWM are shown in Figure 5a. Figure 5b depicts the loss distribution across power semiconductors and capacitors. From this figure, switches S_{1b}, S_{2b} have higher power losses than other components because they switch to charge and discharge the capacitor C_{1b}. Moreover, the comparison of the efficiency of the proposed 25-level MS-SCMLI, the thermal model, and the loss analysis of two recent 25-level MS-SCMLIs was conducted in the PLECS environment in which they are controlled by PSC-PWM. For these topologies, the same IGBTs and thermal models as in the proposal are employed.

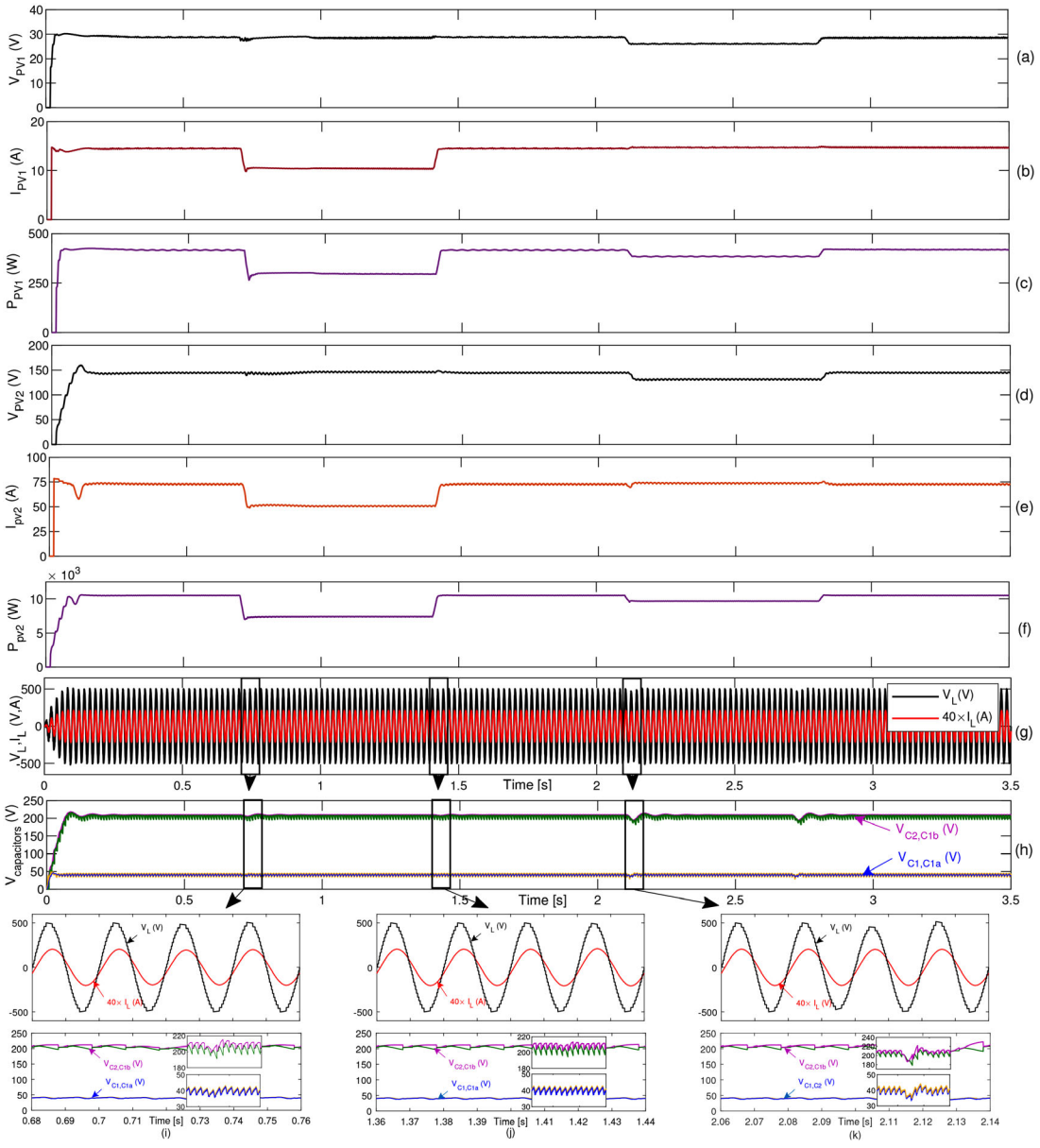


FIGURE 10 Simulation results of the dynamic state of a proposed 25-level multilevel inverter in standalone PV mode; (a) low voltage PV panel; (b) low current PV panel; (c) low power PV panel; (d) high voltage PV panel; (e) high current PV panel; (f) high power PV panel; (g) load voltage and current; (h) capacitor voltage; (i) zoomed view of load voltage, load current and capacitor voltages at t=0.705[s]; (j) at t=1.405[s]; (k) at t=2.105[s]

The power loss distribution of the proposed topology for different power (0-5[Kw]) is shown in Figure 5c. The power losses of the proposed switched capacitor topology are conduction losses, switching losses, and capacitor ripple losses. As can see from this figure, by increasing the output power the power losses of the proposed topology are increased which makes efficiency is decreased. It is also observed that the conduction losses of the proposed topology constitute the major part of power losses which is normal in MLI topologies. Because MLIs require more switches in the current path to generate high number of levels.

Figure 5d shows the efficiency assessment for the proposal and [26], [27]. The proposed topology, as shown in this diagram, is more efficient than [26,27] and [29,30]. The proposal, [26], [29] achieve maximum efficiency at a power of 500[W], whereas [27] achieves maximum efficiency at a power of 200[W] and [30] achieves it at a power of 100[W]. The efficiency of multilevel inverters falls as power increases because of semiconductor conduction loss, which is a function of output current and produces the majority of power losses. Furthermore, due to the considerable voltage difference between the DC link and the capacitor voltages, capacitor ripple losses increase as output power rises, affecting the decreasing efficiency. The proposed twenty-five-level MS-SCMLI has a total loss of 234[W] at a power output of 5[KW], with an efficiency of 95.52%, which is better than [26,27] and [29,30].

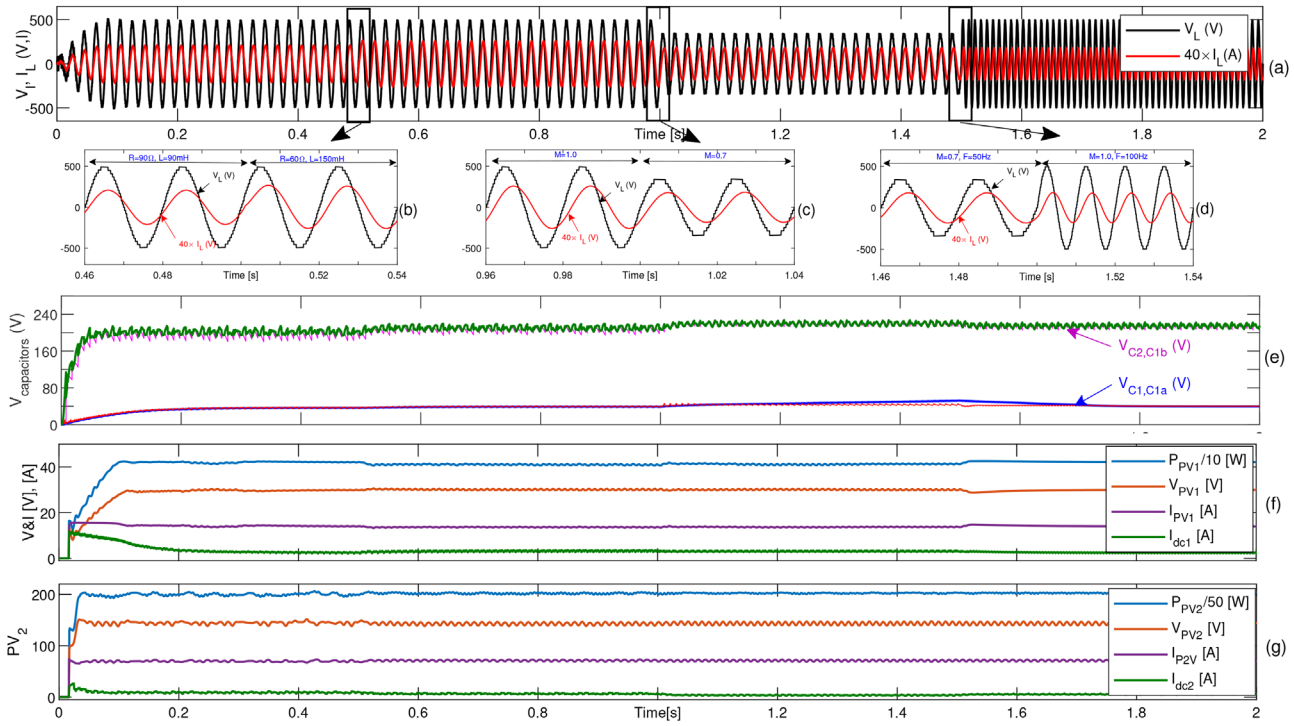


FIGURE 11 Simulation results of the dynamic response of the proposed 25-level multilevel inverter in standalone PV mode for different step changes; (a) load voltage and load currents; (b) zoomed view of load voltage and load current for sudden load change at t=0.5[s]; (c) for decreasing modulation index at t=1.0[s]; (d) for increasing modulation index and the frequency at t=1.5[s]; (e) capacitor voltages; (f) voltage, current and power of PV-1 and dc current of PV-1 ; (g) voltage, current and power of PV-2 and dc current of PV-2

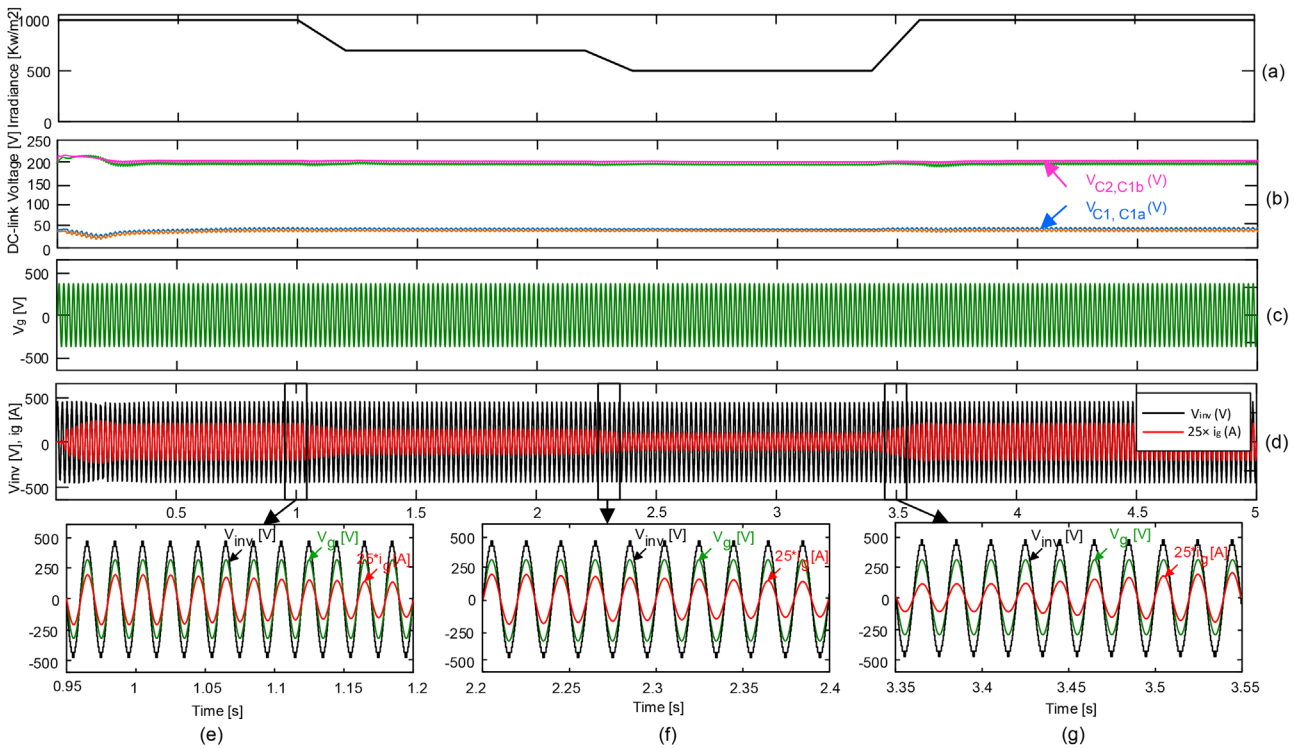


FIGURE 12 Simulation study of grid-connected PV application for irradiance variations; (a) PV irradiance; (b) DC-link voltages; (c) grid voltage; (d) inverter voltage and grid current; (e) zoomed inverter voltage and grid waveform at decreasing irradiance from 1000 to 700[Kw/m^2]; (f) zoomed inverter voltage and grid waveform at decreasing irradiance from 700 to 500[Kw/m^2]; (g) zoomed inverter voltage and grid waveform at increasing irradiance from 500 to 1000[Kw/m^2]

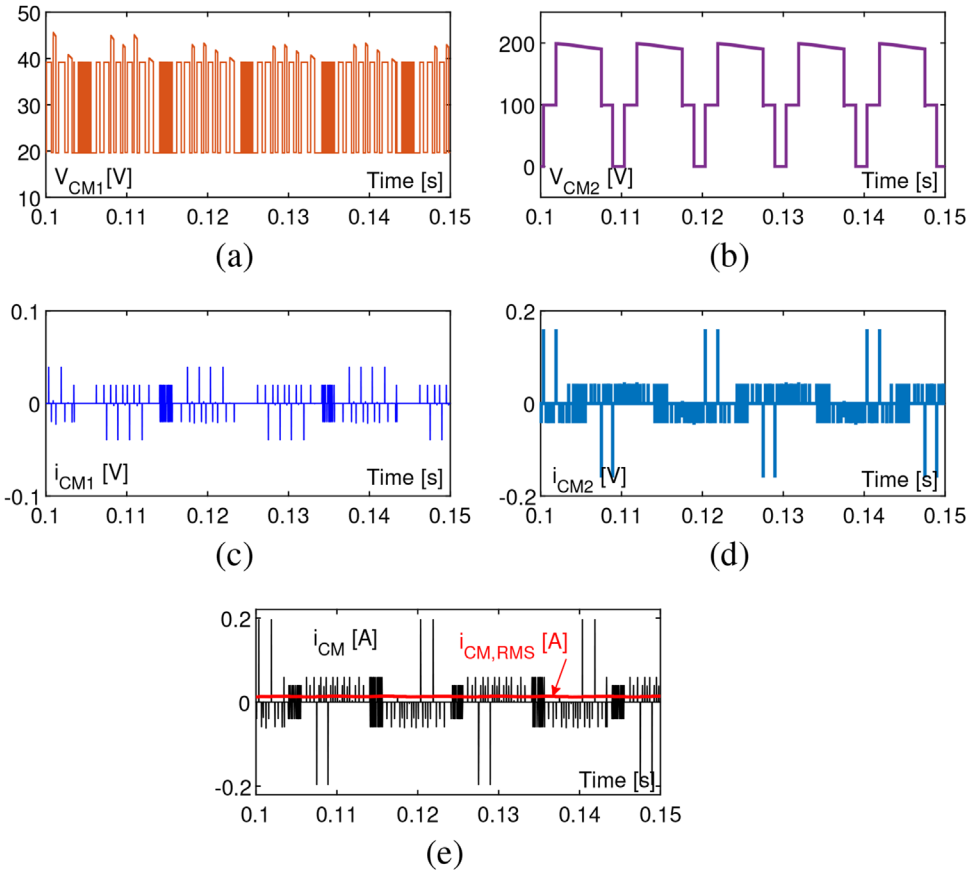


FIGURE 13 Simulation studies of the proposed grid-connected inverter considering stray capacitors; (a) CM voltage of low power PV panel (V_{CM1}); (b) CM voltage of high power PV panel (V_{CM2}); (c) leakage current of low power PV panel (I_{CM1}); (d) leakage current of high power PV panel (I_{CM2}); (e) total leakage current (I_{CM}) and its RMS value ($I_{CM,RMS}$)

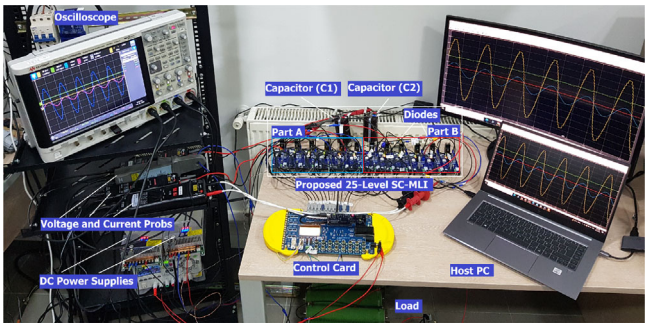


FIGURE 14 Laboratory prototype of suggested twenty-five level topology

Since the proposed topology is proposed for the solar system, the efficiency is also assessed when a DC-DC converter is used between PV panel and inverter to control MPPT and dc-link voltage. The type of switches and diodes of the boost converters are similar to the switch type of proposed topology, the switching frequency is 10[kHz] with a duty cycle of 0.3, and the values of inductors are 0.1[mH]. The voltage of PV panels is set at 30[V] and 150[V]. As can see from Figure 5e, the efficiency of the proposed inverter is shown in both cases: with and without a dc-dc converter. The overall efficiency is reduced when a dc-dc converter is used due to the power loss of boost converter semiconductors.

7 | CONTROL SCHEME OF SUGGESTED MLI IN PV APPLICATIONS

One of the applications of the suggested MLIs is in PV applications (stand-alone or grid-connected). In standalone PV applications, the main concern of multilevel inverters is delivering high-quality electricity to the load while maintaining good inverter efficiency [31]. Nevertheless, the proposed topologies enhance the power quality due to creating a high quantity of levels that make a pure sinusoidal current shape and also enhance the efficiency due to the use of small numbers of power electronics devices.

7.1 | Modulation technique

to generate pulses of the suggested structure, fundamental frequency modulation (FFM) is employed. The block diagram of FMM technique for the suggested 25-level structure is

TABLE 4 Comparison of proposed MLIs with other MLIs for producing different levels

Topologies	N_L	N_{DC}	N_C	N_S	N_{Dr}	N_D	N_{On}	$TSV_{p.u}$	CF/N_L α=0.5	CF/N_L α=1.5
[8]	13	6	0	14	14	14	8	4.5	20.423	22.5
[9]	17	4	0	12	10	12	5	5	8.588	9.764
[10]	17	4	0	12	9	12	5	5	8.352	9.529
[11]	17	4	0	10	10	10	5	4.5	7.588	8.647
[12]	17	2	3	12	12	13	7	6.6	5.094	5.87
[13]	19	2	4	18	18	18	9	4.9	6.363	6.878
[14]	17	1	4	16	16	16	8	5.75	3.227	3.566
[15]	13	2	2	14	11	14	6	5.3	13.43	15.061
[16]	25	4	0	12	10	12	6	5	5.84	6.64
[17]	25	2	4	14	12	14	6	5.8	3.752	4.216
[18]	25	4	0	12	10	12	6	4.5	5.8	6.52
[19]	25	4	0	10	10	16	6	4.5	6.12	6.48
[20]	25	2	4	14	14	22	6	4.5	4.5	4.86
[21]	31	6	0	18	14	18	6	1.8	9.851	10.2
	49	8	0	22	16	22	8	1.5	9.918	10.163
[22]	17	2	2	10	10	12	5	5.5	4.323	4.97
	49	3	3	14	14	17	7	5	3.091	3.397
	137	4	4	18	18	22	9	6	1.897	2.072
[23]	17	2	2	10	10	12	5	5	4.294	4.882
	49	2	4	16	16	20	8	6.25	2.413	2.668
	289	4	4	20	20	24	8	5.25	0.977	1.05
[24]	31	2	4	16	16	18	13	5.6	3.664	4.025
	103	2	4	16	16	18	13	5.66	2.354	2.519
	199	2	8	26	26	30	16	6.22	0.935	0.998
[25]	31	2	4	14	14	12	5	7.2	2.903	3.29
	49	2	4	14	14	12	5	7.2	2.27	2.566
	71	2	8	22	22	8	7	8.2	1.863	2.096
	169	4	8	28	28	20	10	6	2.059	2.201
[26]	25	2	2	16	14	14	7	8.9	4.036	4.748
	49	2	3	19	14	21	10	6.67	2.462	2.734
	113	3	3	24	21	26	14	6.94	2.056	2.24
[27]	25	2	2	13	12	13	6	1.7	3.268	3.404
	49	2	4	17	16	20	8	1.6	2.359	2.424
	141	4	5	25	22	25	13	1.56	2.206	2.25
[28]-Figure 4a	25	2	2	12	12	14	6	5	3.24	3.64
	125	3	3	18	18	20	9	5	1.74	1.59
Figure 4b	25	2	2	14	14	18	8	5.5	4.06	4.5
	125	3	3	21	21	23	11	7.11	1.71	1.88
[29]	25	4	8	28	28	40	16	2.56	15.88	16.29
	125	3	3	18	18	20	9	5	1.74	1.59
[30]	17	2	2	10	10	12	7	5.3	4.311	4.93
	31	2	4	12	12	16	9	5.6	3.019	3.38
	49	2	6	18	18	22	11	5.7	2.728	2.95
F&S-MLIs	**25**	**2**	**2**	**12**	**12**	**12**	**6**	**5**	**3.08**	**3.48**

(Continues)

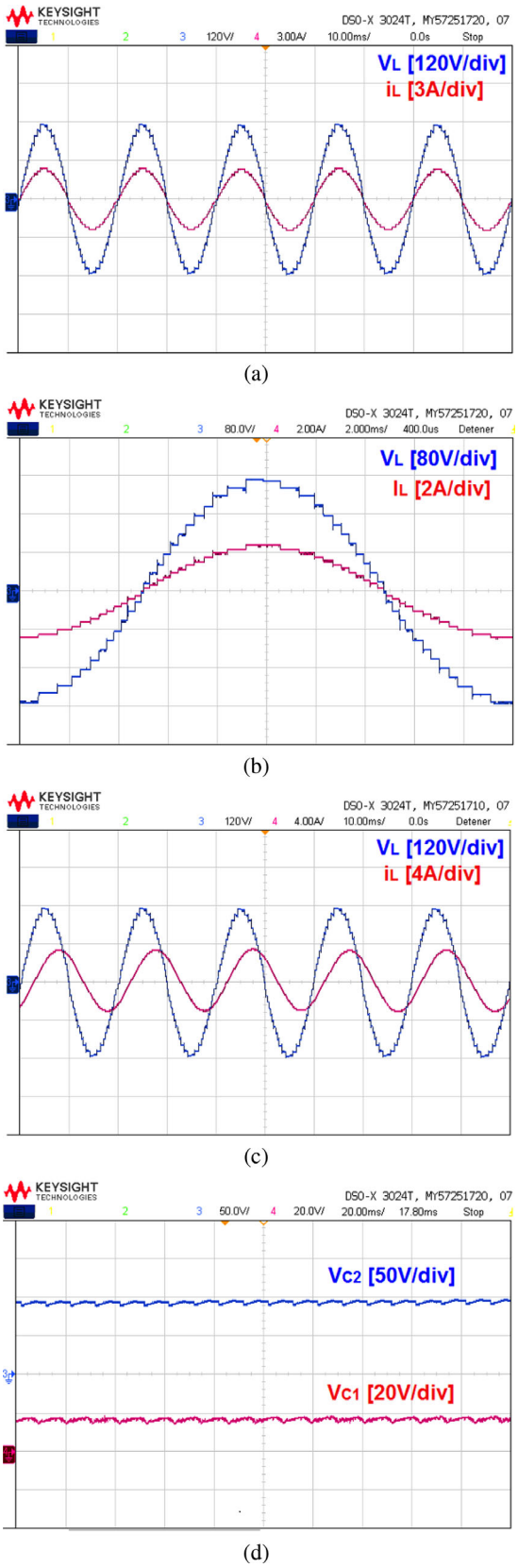


FIGURE 15 (a) the experimental output waveform of the suggested 25-level structure for a pure resistance load; (b) output waveform in zoomed view 2[ms]; (c) for R-L load; (d) the voltage of the capacitors

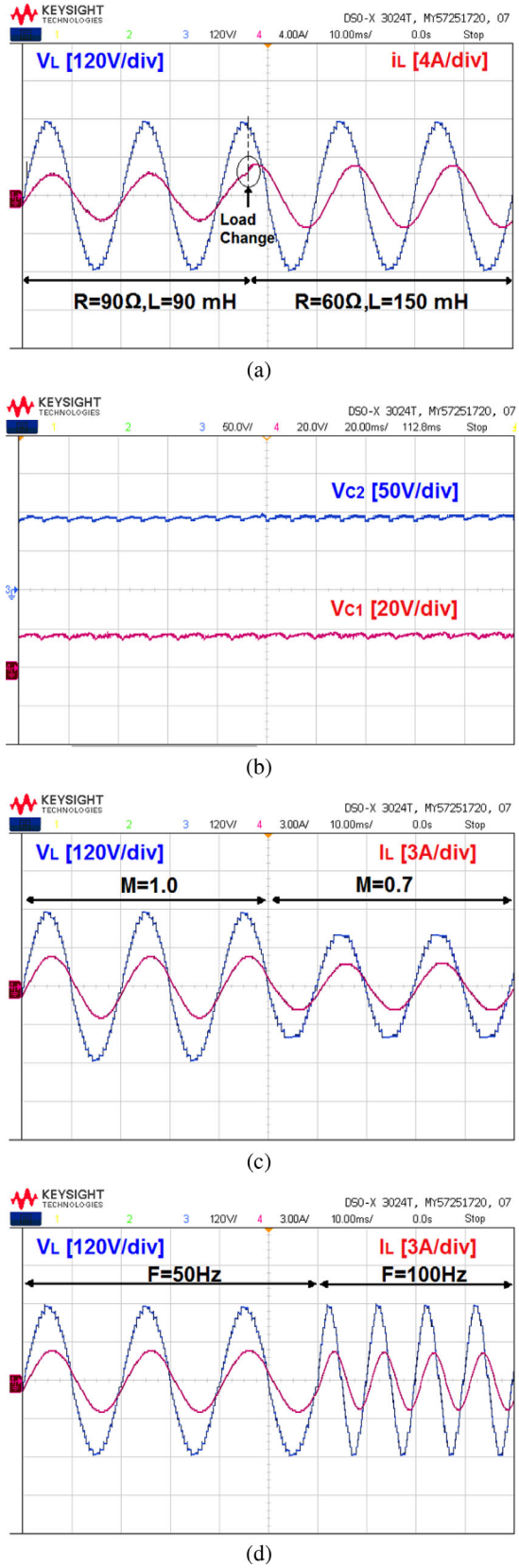


FIGURE 16 Suggested topology response (a) for unexpected load change; (b) voltage of capacitors; (c) for step modulation index variation; (d) for step frequency change

TABLE 4 (Continued)

Topologies	N_L	N_{DC}	N_C	N_S	N_{Dr}	N_D	N_{On}	$TSV_{p.u}$	CF/N_L α=0.5	CF/N_L α=1.5
FS-MLI	49	2	4	16	16	16	8	5.3	2.230	2.446
FA-MLI	81	2	4	18	18	16	10	6	1.308	1.456
FA-MLI	289	2	6	24	24	20	10	6.8	0.535	0.557
S-MLI	169	4	4	20	20	20	14	5.3	1.577	1.702

TABLE 5 Simulation study parameters

Parameter	Value	Unit
Irradiation & Temperature (Ir & Tr)	1000,25	[KW/m^2], [°C]
Total PV power (P_{pv})	11.1	[KW]
No. of parallel modules (N_{p1}, N_{p2})	2,10	–
No. of series modules (N_{s1}, N_{s2})	1,5	–
Short-circuit current (I_{sc})	7.84	[A]
Open circuit voltage (V_{oc})	36.3	[V]
Maximum current (I_m)	7.35	[A]
Maximum voltage (V_m)	29	[V]
Maximum power (P_m)	213.15	[W]
Boost inductors (L_a, L_b)	0.2,6.8	[mH]
Boost converter switching frequency (f_{sb})	5	[KHz]
DC-link Voltage ($V_{dc1} = V_{dc}$)	40	[V]
DC-link Voltage ($V_{dc2} = 5V_{dc}$)	200	[V]
Inverter output frequency (f_o)	50	[Hz]
Low voltage capacitors (C_1, C_{1a})	2200	[μF]
High voltage capacitors (C_2, C_{1b})	1200	[μF]
Load (R,L)	90,90	[Ω],[mH]
PI-VC1 (k_{p1}, k_{i1})	0.007,0.01	–
PI-VC2 (k_{p2}, k_{i2})	0.003,0.01	–
PI Current Control (k_p, k_i)	0.01,0.08	–
Grid Voltage (V_g)	311	[V]
Grid frequency (f_o)	50	[Hz]
Output filter (R_f, L_f)	3,10	[mΩ],[mH]
PI-VC1+VC2 (k_{p3}, k_{i3})	0.89,0.08	–
PI-VC2 (k_{p4}, k_{i4})	0.52,0.07	–
Parasitic capacitance (C_{PV1})	50	[nF]
Parasitic capacitance (C_{PV2})	100	[nF]

exhibited in Figure 6. In this method, the reference voltage of the suggested multilevel inverter is compared with the constant dc input voltage, and then, in a logic-based function [7, 9], the pulses of the power switches are generated according to the switching table (Table 2). This control technique can be easily applied to the proposed extended and cascading MLIs.

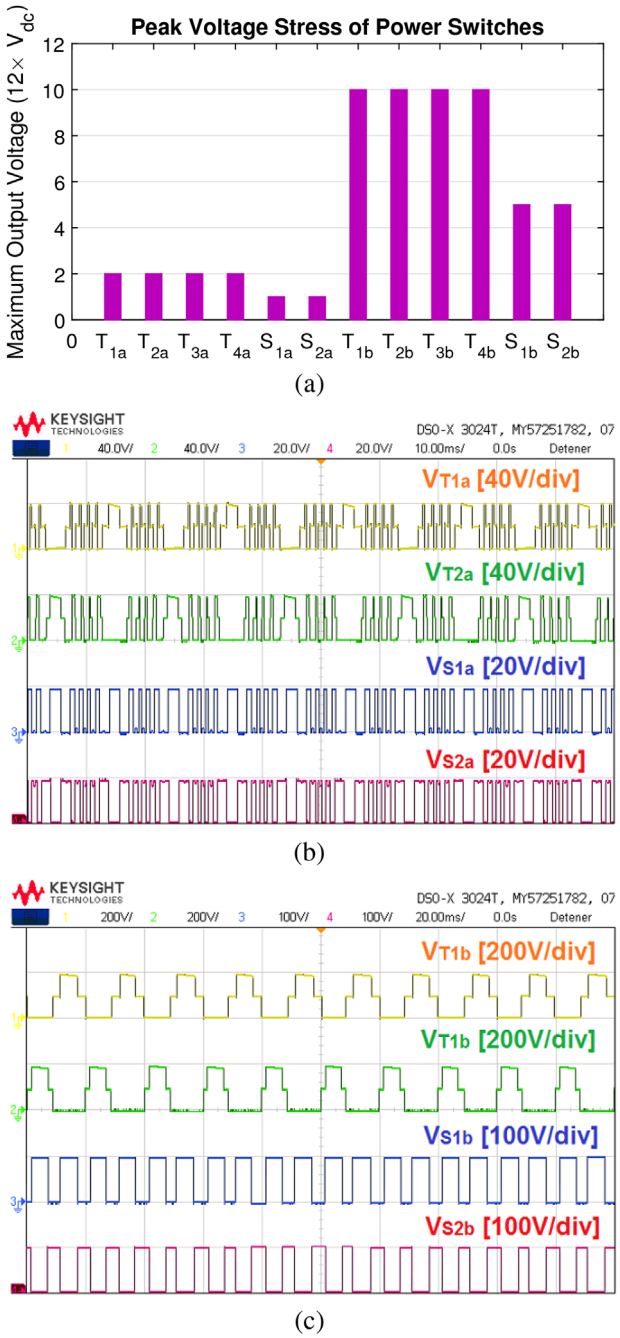


FIGURE 17 Voltage stress of IGBTs; (a) steers voltage distribution; (b) stress voltage of power switches T_{1a}, T_{2a}, S_{1a}, S_{2a}; (c) SV of T_{1b}, T_{2b}, S_{1b}, S_{2b}

7.2 | Standalone PV application

Figure 7 exhibits the control scheme to control the suggested 25-level structure in PV systems. The DC-link voltage of the suggested topology uses two PV panels with different powers, which use two independent boost converters to achieve high power efficiency. The type of boost converters used is standard DC-DC converters. The duty cycles of two switches of the dc-dc converters (S_{b1}, S_{b2}) regulate the voltage of capacitors (V_{C1}, V_{C2}). Therefore, the magnitude of DC-link voltages (V_{C1}, V_{C2}) based on the duty cycle of switches (D_1, D_2) and PV panel voltages (V_{PV1}, V_{PV2}) are calculated as follows:

$$V_{C1} = \frac{V_{PV1}}{1 - D_1}, V_{C2} = \frac{V_{PV2}}{1 - D_2}. \quad (43)$$

The input DC-link voltages are adjusted to desired magnitudes by changing the number of series PV modules and the pulse width of DC-DC converter switches. By monitoring the voltage and current of PV panels and applying a good MPPT algorithm, the maximum power can be derived. In order to generate switching pulses for DC-DC converter switches, the output of MPPT is compared with the PWM signals.

The load voltage must be managed by the suggested inverter in order to give energy to the load at a constant nominal voltage. Hence, to have a constant voltage at the output of the inverter, the input capacitor voltages should be adjusted to their reference values. By using independent PI controllers, the capacitor voltages can be balanced and fixed to their references. In order to prevent the voltage drop caused by the filter and series impedance, an extra PI controller is incorporated into the suggested control scheme. The output of this PI controller gives the proper modulation index and the switching pulses of the proposed inverter are produced by the proposed FFM technique (see Figure 6).

7.3 | Grid-connected PV application

the control scheme to control the suggested 25-level structure in grid-connected PV systems is shown in Figure 8. The DC-link voltage of the suggested topology is obtained similar the stand-alone case. The overall DC-link voltage is monitored by comparing the DC-link voltage reference (V_{ref}) with two inputs measured capacitor voltage ($V_{C1} + V_{C2}$). At this point, by tune-up a Proportional-Integral (PI) controller, the highest current is generated. A typical phase-locked loop (PLL) control is employed to produce a sinusoidal reference current and follow the grid frequency, as appeared in Figure 8.

A Proportional Resonance (PR) current control technique is used to handle grid current. The reference current is made by reproducing the output of PLL (i_g^*), then it is compared with the measured grid current (i_g). The output of the PR controller maximizes the current and sums it up with the grid voltage to generate a proper reference signal under grid voltage variations. Finally, since the magnitude (V_{inv}^*) is inappropriate to apply to the proposed inverter, it is scaled down to produce the part of the reference voltage (V_1^*) of the proposed inverter.

In order to produce 25-level with the proposed inverter, the ratio of DC-link voltages is kept at ratio 1:5. The overall DC-link voltage controller is controlled at the total DC link voltage of the inverter equal to $6V_{C1}$. To maintain the second DC-link voltage (V_{C2}), which should have amplitudes equal to $5V_{dc}$ an individual voltage controller is added to the control system, as shown in Figure 8. Therefore, by using these three independent (PI) controllers, the DC-link voltages are balanced and set in their references.

The capacitor sizes (C_1, C_2) are calculated using well-known formulate: $C=I_{L,peak}/\triangle V_C \times f_s$. Here, $I_{L,peak}, \triangle V_C, f_s$ are the load peak current, the ripple voltage of the capacitor, and the switching frequency of the voltage, respectively.

7.4 | Common-mode voltage and leakage current

In the proposed transformerless PV inverter, due to no direct connection of negative terminals of PV panels and grid exist a stray capacitance which causes a varying voltage which is known as common-mode voltage (CMV). The stray parasitic capacitor with the inductor of the output filter of the inverter forms a resonant circuit that is excited by this CM voltage, thus producing a high common-mode current (leakage current) i_{CM} [32]. Figure 9a shows the grid-connected of the proposed topology considering parasitic capacitors and Figure 9b indicates an equivalent circuit of the common-mode voltage (CMV), differential mode voltage (DMV), and leakage current of each part of the proposed topology. From Figure 9, the common-mode voltage and differential-mode voltage (DMV) corresponding to the phase voltages in each part of the proposed topology can be obtained as follows [33]:

For the first part:

$$V_{CM1} = \frac{V_{A1N1} + V_{B1N1}}{2}, V_{DM1} = V_{A1N1} - V_{B1N1}. \quad (44)$$

For the second part:

$$V_{CM2} = \frac{V_{A2N2} + V_{B2N2}}{2}, V_{DM2} = V_{A2N2} - V_{B2N2}. \quad (45)$$

Therefore, the common mode current or leakage current of the proposed topology can be obtained as:

$$i_{CM} = i_{CM1} + i_{CM2}. \quad (46)$$

8 | SIMULATION STUDIES

MATLAB/Simulink software is used to evaluate the suggested twenty-five level inverter for both 11.1[Kw] standalone and grid-connected solar photovoltaic applications. Table 5 gives the list of single-phase system parameters.For both evaluations the input dc-link voltage of the suggested inverter is set through two DC-DC converters (see Figure 7) which are controlled by (P & O) MPPT [34]. The boost converters duty cycles are set by eq. (43). The capacitor voltage balancing and the control of the system are based on the presented control system that is depicted in Figure 7. The values of capacitors are calculated for 5% ripple, 2200[μF] for (C_1, C_{1a}) and 1200[μF] for (C_2, C_{1b}).

The lower dc-link voltage associated with (C_1) is kept at 40[V], while the higher dc-link voltage associated with (C_2) is kept at 200[V].

8.0.1 | Standalone evaluations

for standalone evaluation the suggested inverter is verified to feed an AC load of 90[Ω]-90[mH] under various PV panel environmental conditions. The results are shown in Figure 10. The irradiance of PV modules at t=0.705[s] decreases from 1000 to 700[W/m^2]. It then returns to 1000[W/m^2] at t = 1.405[s]. The temperature of PV panels is increased from 25[°C] to 45[°C] at t=2.105[s] and then returns to 25[°C] at t=2.705[s]. Figures 10a–f show the voltage, current, and power for both PV panels. These figures confirm that the MPPT operates properly during environmental changes and that the maximum power of PV panels is always extracted. The voltage and current shapes of the load are shown in Figure 10g, and the voltage of the capacitors is shown in Figure 10h. The proposed inverter delivers power to the load by generating twenty-five levels of voltage with a maximum output voltage of 480[V] and a pure sinusoidal output current, as shown in Figure 10g. Figure 10h confirms that the proposed capacitor voltage balancing controllers work properly during irradiance and temperature changes with rapid responses and low voltage ripples.

Figures 10i–k show the zoom view of load voltage, load current, and capacitor voltages at the different step-change times. These figures reveal that during irradiance and temperature variations, a steady voltage is supplied to the load, and the voltage of the capacitors is quickly adjusted to their references, confirming the suggested control scheme.

The simulation of the proposed inverter is also performed on sudden load change, modulation index, and frequency changes. Figure 11 depicts the output voltage and current waveforms. In this case, in the first, the inverter feeds an R-L load 90[Ω]-90[mH] then at t=0.5[s] the load's value changes to 60[Ω]-150[mH]. After that, at t=1.0[s] the modulation index reduces from 1.0 to 0.7, and finally, at t=1.5[s] the modulation index increases to 1.0, and at the same time, the frequency is increased from 50[Hz] to 100[Hz]. A zoomed view of the load voltage and currents is shown in Figures 11a–c to see the better performance of the proposed inverter in different step changes. Figure 11a shows that the sudden load change does not affect the load voltage shape. The output voltage levels are reduced from 25 to 17 in Figure 11b. Figure 11c indicates that the modulation index increased to 1.0 and the frequency increased from 50[Hz] to 100[Hz]. This figure demonstrates that the new topology works at various frequencies with no changes in the shape of the output waveforms.

Figure 11e shows the capacitor voltages of the proposed topology. It can see that the voltage of capacitors is charged and kept balanced with a little variation when the step changes happen. The voltage, current, and power of low and high power PV panels are shown in Figures 11f and 11g, respectively. In addition, the dc currents of both PV panels I_{dc1}, I_{dc2} (they are average values) are indicated inside these figures. As can see from Figures 11(e)-(g) low and high power PV panels operate in maximum power point properly when a sudden load change, modulation change, and output frequency change happen.

8.0.2 | Grid-connected evaluations

for grid-connected evaluation under different solar panel conditions, the proposed inverter is connected to the grid through a low R-L filter. The evaluations are done based on the suggested closed-loop control scheme that appeared in Figure 8. Figure 12 is indicated the results. Figure 12a shows the variations of the PV modules irradiance which are decreased at t=1.0[s] and 2.2[s] from 1000 to 700 and 500[W/m^2], and finally it returns to 1000[W/m^2] at t = 3.4[s]. The temperature of PV panels is set to 25[°C].

Figure 12b shows the DC-link voltage which are capacitor's voltages (C_1, C_2). In addition the voltage of capacitors (C_{1a}, C_{1b}) are shown in this figure which has the same value as DC-link capacitor voltages. These figures confirm that voltages of input DC-links and both internal capacitors are kept balanced in their references 40[V] and 200[V] in various PV panel conditions. Figure 12c shows the grid voltage and Figure 12d shows the inverter voltage in grid current. As can see from Figure 12d, the voltage of the inverter is constant and the grid current is changed with the irradiance of PV panels. Figures 12e–g indicated zoomed view of grid waveforms and inverter voltage at different irradiance change points. These figures confirm the inverter voltage, grid voltage and current are in phase together in different environmental conditions of PV panels and inject maximum power to the grid.

The simulation results of common-mode voltage and leakage current of the proposed topology based on Figures 8 and 9 are illustrated in Figure 13. Figures 13a and 13b show common-mode voltage PV-1 and PV-2. Normally, the peak value of common-mode voltage should be less than the rated maximum system voltage (600/800/1000 V) of the PV panels. Therefore, Figures 13a and 13b confirm that the peak of CMV in both PV panels is lower than the rated voltages. As we presented in Figure 9, we split the output fitter sizes to reduce the leakage current which is a common method for grid-connected PV inverters. Thus, the leakage current of both PV panels is very low, which causes a reduction in the total leakage current of the proposed system.

9 | EXPERIMENTAL VALIDATION

The hardware results of a suggested 25-level MLI are used to validate the performance of the proposal. The utilized components in the experimental set-up are listed in Table 6.

To provide switching pulses for the inverter, the suggested control modulation technique described in section VII is used. Figure 14 shows the experimental prototype of the proposed 25-level MLI. Two laboratory DC power supplies are utilized for the DC-link voltage. To produce pulses for the switches, digital signal processing TMS320F28375 is used. Through the optic wires, the gating signals are sent to the IGBTs. The magnitudes of the input DC power supplies are V_1=20[V], $V_2 = 5V_1$=100[V]. As a result, the suggested topology provides a 25-level output with a 240[V] peak.

The hardware findings of the suggested 25-level MS-SCMLI are shown in Figure 15. Figures 15a and 15b display the load voltage and current for a pure resistance load 90[Ω]. The output waveform and the voltage of capacitors are displayed in Figure 15c,d for an AC load of 60[Ω], 150[mH]. Due to the existing inductive load, in this case, the load current has a sin shape. Additionally, both capacitors are regulated in their references (dc voltage magnitudes), V_{C1}=20[V] and V_{C2}=100[V]. The hardware findings prove that the suggested structure can provide all 25 levels using the presented modulation approach, and the capacitor's voltage is regulated properly at the magnitude of the DC-link voltages.

Furthermore, the performance of the proposed MLI is verified with different step variations such as load, modulation index, and frequency. The results of the experiment are depicted in Figure 16. The suggested topology first powers an AC load of 90[Ω], 90[mH], then the load switches to other AC load of 60[Ω], 150[mH]. The suggested inverter, as shown in Figure 16a, has a valid response to rapid changes in load and it can also control the load current without varying the phase of output voltage. Figure 16b indicates the voltage of capacitors for load variations. During this shift, the voltages of capacitors (C_{1a}, C_{1b}) are regulated near the input dc-link magnitudes.

The evaluations for modulation and frequency fluctuations are then performed. The modulation index reduces from 1.0 to 0.7. As indicated in Figure 16c, the hardware findings are consistent with the software findings in that the voltage levels dropped from twenty-five levels to seventeen levels. Figure 16d depicts the response of the suggested inverter to frequency fluctuations ranging from 50 to 100 [Hz]. The suggested inverter can run at 100[Hz] without creating any changes in the output waveform's shape, as seen in this diagram.

Figure 17a depicts the peak voltage of each switch in the proposed topology versus the maximum output voltage levels. This graph illustrates that none of the switches tolerate the maximum output voltage. Figures 17b and 17c depict the experiment findings of the stress voltage for some IGBTs of the suggested inverter. Figure 17b displays the voltage stress on IGBTs of part-a ($T_{1a}, T_{2a}, S_{1a}, S_{2a}$). IGBTs of ($S_{1a}, S_{2a}$) withstand a low voltage of 20[V] and IGBTs of ($T1a, T2a$) withstand twice that, which is 40[V]. Figure 17c depicts the IGBTs stress voltage for part-b. (S_{1b}, S_{2b}) tolerate high dc-link voltage of 100[V] while

TABLE 6 Experimental parameters

Parameters	Value	Unit
Laboratory DC Sources	V_1 = 20, V_2 = 100	[V]
IGBT	FGH80N60FDTU, 600, 40	[V],[A]
Diode	SKKD 100/12 1.2k,100	[V],[A]
DSP	TMS320F28375	–
Inverter output frequency (f_o)	50	[Hz]
capacitors (C_{1a}, C_{1b})	2200	[μF]
Load (R,L)	90,90 and 60,150	[Ω], [mH]
Dead time	2	[ns]

others withstand twice that, namely 200[V]. The efficiency of the suggested MS-SCMLI is 96.1% for an output power of 250[W].

10 | CONCLUSION

In this paper, we present a simple multicell switched-capacitor MLI architecture appropriate for PV applications with fewer power electronics devices. The main topology was expanded to three other circuits, and their cascading topologies were investigated in order to reach a wide range of voltage levels. Furthermore, the optimal topologies were extracted using different criteria to increase the number of levels and minimize component counts. Comparing the suggested topologies to previous MLIs yielded thorough findings, demonstrating that the proposed structures needed minimal power electronics devices, DC link voltages, and capacitors. Furthermore, we have shown that the suggested MC-SCMLI topologies have a lower cost factor (CF) than previously published MLIs, making them more affordable. The simulation results of the suggested basic topology for stand-alone and grid-connected PV applications were also given, proving that it offers great performance in these applications while lowering the cost. Finally, the practical findings were presented in order to validate the proper operation of the proposed topologies through several evaluations.

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CONFLICT OF INTEREST

The authors have declared no conflict of interest.

DATA AVAILABILITY STATEMENT

Data sharing not applicable - no new data generated.

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REFERENCES

1. Obeidat, F.: A comprehensive review of future photovoltaic systems. Solar Energy 163, 545–551 (2018)
2. Baccoli, R., Kumar, A., Frattolillo, A., Mastino, C., Ghiani, E., Gatto, G.: Enhancing energy production in a PV collector–Reflector system supervised by an optimization model: Experimental analysis and validation. Energy Conv. Management. 229, 113774 (2021)
3. Rodriguez, J., Bernet, S., Wu, B., Pontt, J.O., Kouro, S.: Multilevel voltage-source-converter topologies for industrial medium-voltage drives. IEEE Trans. Ind. Electron. 54(6), 2930–2945 (2007)
4. Weidong, J., et al.: A carrier-based virtual space vector modulation with active neutral-point voltage control for a neutral-point-clamped three-level inverter. IEEE Trans. Ind. Electron. 65(11), 8687–8696 (2018)
5. Babaei, E.: A cascade multilevel converter topology with reduced number of switches. IEEE Trans. Power Electron. 23(6), 2657–2664 (2008)
6. Babaei, E., Gowgani, S.S.: Hybrid multilevel inverter using switched capacitor units. IEEE Trans. Ind. Electron. 61(9), 4614–4621 (2014)
7. Hosseinzadeh, M.A., Sarebanzadeh, M., Rivera, M., Babaei, E., Wheeler, P.: A reduced single-phase switched-diode cascaded multilevel inverter. IEEE J. Emerg. Sel. Top. Power Electron. 9(3), 3556–3569 (2021)
8. Mohamed Ali, J.s, et al.: A new generalized multilevel converter topology based on cascaded connection of basic units. IEEE J. Emerg. Sel. Top. Power Electron. 7(4), 2498–2512 (2019)
9. Shalchi Alishah, R., Hosseini, S.H., Babaei, E., Sabahi, M.: Optimization assessment of a new extended multilevel converter topology. IEEE Trans. Ind. Electron. 64(6), 4530–4538 (2017)
10. Samadaei, E., Sheikholeslami, A., Gholamian, S.A., Adabi, J.: A square T-type (ST-Type) module for asymmetrical multilevel inverters. IEEE Trans. Ind. Electron. 33(2), 987–996 (2018)
11. Mohamed Ali, J.S., Shalchi Alishah, R., Krishnasamy, V.: A new generalized multilevel converter topology with reduced voltage on switches, power losses, and components. IEEE J. Emerg. Sel. Top. Power Electron. 7(2), 1094–1106 (2019)
12. Ngo, B., Nguyen, M., Kim, J., Zare, F.: Single-phase multilevel inverter based on switched-capacitor structure. IET Power Electron. 11(11), 1858–1865 (2018)
13. Dargahi, V., Sadigh, A.K., Abarzadeh, M., Pahlavani, M.R.A., Shoulaie, A.: Flying capacitor reduction in an improved double flying capacitor multicell converter controlled by a modified modulation method. IEEE Trans. Power Electron. 27(9), 3875–3887 (2012)
14. Roshankumar, P., Kaarthic, R.S., Gupakumar, K., Leon, J.I., Franquelo, L.G.: A seventeen-level inverter formed by cascading flying capacitor and floating capacitor H-bridge. IEEE Trans. Power Electron. 30(7), 3471–3478 (2015)
15. Samadaei, E., Kaviani, M., Bertilsson, k.: A 13-levels module (k-type) with two dc sources for multilevel inverters. IEEE Trans. Ind. Electron. 66(7), 5186–5196 (2019)
16. Siddique, M.D., Mekhilef, S., Shah, N.M., Sarwar, A., Iqbal, A., Memon, M.A.: A new multilevel inverter topology with reduce switch count. IEEE Access 7, 58584–58594 (2019)
17. Taheri, A., Rasulkhani, A., Ren, H.: An asymmetric switched capacitor multilevel inverter with component reduction. IEEE Access 7, 127166–127176 (2019)
18. Sarebanzadeh, M., Hosseinzadeh, M.A., Garcia, C., Babaei, E., Islam, S., Rodriguez, J.: Reduced switch multilevel inverter topologies for renewable energy sources. IEEE Access 9, 120580–120595 (2021)
19. Saeedian, M., Adabi, J., Hosseini, S.M.: Cascaded multilevel inverter based on symmetric-asymmetric DC sources with reduced number of components. IET Power Electron. 10(12), 1468–1478 (2017)
20. Saeedian, M., Hosseini, S.M., Adabi, J.: A five-level step-up module for multilevel inverters: topology, modulation strategy, and implementation. IEEE J. Emerg. Sel. Top. Power Electron. 6(4), 2215–2226 (2018)
21. Nazemi Babadi, A., Salari, O., Mojibian, M.J., Bina, M.T.: Modified multilevel inverters with reduced structures based on packed u-cell. IEEE J. Emerg. Sel. Top. Power Electron. 6(2), 874–887 (2018)
22. Zamiri, E., Vosoughi, N., Hosseini, S.H., Barzegarkhoo, R., Sabahi, M.: A new cascaded switched-capacitor multilevel inverter based on improved series-parallel conversion with less number of components. IEEE Trans. Ind. Electron. 66(6), 3582–3594 (2016)
23. Barzegarkhoo, R., Moradzadeh, M., Zamiri, E., Madadi Kojabadi, H., Blaabjerg, F.: A new boost switched-capacitor multilevel converter with reduced circuit devices. IEEE Trans. Power Electron. 33(8), 6738–6754 (2018)
24. Roy, T., Sadhu, P.K., Dasgupta, A.: Cross-switched multilevel inverter using novel switched capacitor converters. IEEE Trans. Ind. Electron. 66(11), 8521–8532 (2019)
25. Roy, T., Sadhu, P.K.: A step-up multilevel inverter topology using novel switched capacitor converters with reduced components. IEEE Trans. Ind. Electron. 68(1), 236–247 (2021)

26. Ramaiah, S., Lakshminarasamma, N., Mishra, M.K.: Multisource switched capacitor based boost multilevel inverter for photovoltaic-based systems. IEEE Trans. Power Electron. 35(3), 2558–2570 (2020)
27. Bana, P.R., Panda, K.P., Padmanaban, S., PandaG.,: Extendable switched-capacitor multilevel inverter with reduced number of components and self-balancing capacitors. IEEE Trans. Ind. Appl. 57(3), 3154–3163 (2021)
28. Babaei, E., Gowgani, S.S.: Hybrid multilevel inverter using switched capacitor units. IEEE Trans. Ind. Electron. 61(9), 4614–4621 (2014)
29. Liu, J., Cheng, K.W.E., Ye, Y.: A cascaded multilevel inverter based on switched-capacitor for high-frequency AC power distribution system. IEEE Trans. Power Electron. 29(8), 4219–4230 (2014)
30. Alishah, R.S., Hosseini, S.S., Babaei E., Sabahi, M.: Extended high step-up structure for multilevel converter. IET Power Electron. 9(9), 1894–1902 (2016)
31. Rosas-Caro, J.C., et al.: A dc-dc multilevel boost converter. IET Power Electron. 3(1), 129–137 (2018)
32. Khan, H.M.D.N., et al.: Transformerless inverter topologies for single-phase photovoltaic systems: a comparative review. IEEE J. Emerg. Sel. Top. Power Electron. 8(1), 805–835 (2020)
33. Shahabadini, M., Iman-Eini, H.: Leakage current suppression in multilevel cascaded H-bridge based photovoltaic inverters. IEEE J. Emerg. Sel. Top. Power Electron. 36(12), 13754–13762 (2021)
34. Chen, G., Peng, H., Zeng, R., Hu, Y., Ni, K.: A fundamental frequency sorting algorithm for capacitor voltage balance of modular multilevel converter with low-frequency carrier phase shift modulation. IEEE J. Emerg. Sel. Top. Power Electron. 6(3), 1595–1604 (2018)

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