Apl. Prof. Dr.-Ing. habil. Helmut Graeb – Curriculum Vitae

Technical University of Munich
School of Computation, Information and Technology (CIT)
Department of Computer Engineering (CE)
Chair of Electronic Design Automation (EDA)
Arcisstr. 21, 80333 Munich, Germany

Short Bio

Helmut Graeb received Master's and Dr.-Ing. degrees in Electrical Engineering from the Technical University of Munich (TUM) in 1986 and 1993, respectively.

Since 1987, he has been with the Chair of Electronic Design Automation, TUM, where he has been the Head of a research group since 1993. His research interest is in the area of design automation for analog circuits. He is an IEEE Fellow and co-founder of MunEDA GmbH (now part of Cadence).

He was a recipient of the 2021 Best Doctoral Advisor Award and the 2020 Best Teaching Award of the Department of ECE at TUM, the 2008 Prize of the German Information Technology Society (ITG), the 2004 Best Teaching Award of the TUM EE Faculty Students Association, and the Third Prize of the 1996 Munich Business Plan Contest.

He served as VP of Publications of IEEE CEDA, as a member of the Executive Committee of ICCAD, as a member or Chair of the Analog Program Subcommittees of the ICCAD, DAC, and DATE conferences, and as associate editor of IEEE TCAS and TCAD.

Research (Advised Doctoral Projects (Dr.-Ing.) Analog Group)

- Structural Analysis in Machine Learning for Analog Integrated Circuits (Markus Leibl)
- Automatic Synthesis of Operational Amplifiers (Post-doc project Abdelaziz Lberni, 12/2025)
- Hierarchical Verification and Hierarchical Synthesis of the Power-Down Mode of Analog Circuits (Max Neuner, Dr.-Ing. 12/2023)
- Functional Block-Based Synthesis and Sizing of Integrated Operational Amplifiers (Inga Abel, Dr.-Ing. 06/2022))
- Automatic Analog Layout Synthesis – from Capacitor Arrays in Data Converters to General Design with Routing (Pang-Yen Chou, Dr.-Ing.12/2020)
- Modeling in Analog/Mixed-Signal Simulation, Sizing and Layout (Florin Burcea, Dr.-Ing. 10/2020)
- Concepts for Multi-Level Cell Operation of Embedded Flash in Automotive Applications (Sebastian Kiesel, Dr.-Ing. 03/2020)
- Design-Dependent Monitors to Track the Timing of Digital CMOS Circuits (Jahnavi Kasturi Rangan, Dr.-Ing. 12/2019)
- Reliability Considerations in Analog Synthesis (Andreas Herrmann)
- Development of Analytical Behavioral Models for Digitally Controlled Edge Interpolator (DCEI) based Digital-to-Time Converter (DTC) Circuits (Sebastian Sievert, Dr.-Ing. 08/2017)
- Verification and Synthesis of Analog Power-Down Circuits (Michael Zwerger, Dr.-Ing. 01/2017)
- Advanced Aging Simulation (Post-doc project Husni Habal, 09/2015)
- Structure and Signal Path Analysis for Analog and Digital Circuits (Michael Eick, Dr.-Ing. 06/2013)

- On the Sizing of Analog Integrated Circuits towards Lifetime Robustness (Xin Pan, Dr.-Ing. 07/2013)
- Constraint-Based Layout-Driven Sizing of Analog Circuits (Husni Habal Dr.-Ing. 02/2013)
- Discrete Sizing of Analog Integrated Circuits (Michael Pehl Dr.-Ing. 11/2012)
- Methods for Built-In Self-Test of Analog/Mixed-Signal Integrated Circuits (Aurelien Tchegho Kamdem, Dr.-Ing. 03/2011)
- Deterministic Performance Space Exploration of Analog Integrated Circuits Considering Process Variations and Operating Conditions (Daniel Mueller-Gritschneder, Dr.-Ing. 06/2009)

Research (Co-Advised Ph.D. Projects Analog Group)

- Deterministic Hierarchical Placement of Analog Integrated Circuits (Martin Strasser, Dr.-Ing. 04/2011)
- On the Structural Analysis of CMOS and Bipolar Analog Integrated Circuits (Tobias Massier, Dr.-Ing. 05/2010)
- Hierarchical Optimization of Large-Scale Analog/Mixed-Signal Circuits based on Pareto-Optimal Fronts (Jun Zou, Dr.-Ing. 06/2009)
- Test Design for Analog Integrated Circuits (Michael Pronath, Dr.-Ing. 11/2005)
- On the Performance Space Exploration of Analog Integrated Circuits (Guido Stehr, Dr.-Ing. 09/2005)
- Design methods for implicit functional testing of analog integrated circuits (Volker Gloeckel, Dr.-Ing. 06/2004)
- Tolerance Analysis and Design Centering of Analog Circuits with Consideration of Mismatch (Frank Schenkel, Dr.-Ing. 12/2003)
- Automatic analog integrated circuit sizing using structural constraints (Robert Schwencker, Dr.-Ing. 06/2002)
- Numerical behavioral modeling of analog CMOS circuits considering sizing rules (Stephan Zizala, Dr.-Ing. 10/2001)
- Circuit sizing of analog integrated circuits considering structural constraints (Josef Eckmueller, Dr.-Ing. 11/1998)
- Interconnect simulation considering nonlinear driver properties (Martin Ruhwandl, Dr.-Ing. 10/1998)
- Robust methods for worst-case and yield analysis of analog integrated circuits (Gunter Strube, Dr.-Ing. 04/1998)
- Test design for analog integrated circuits based on characteristic observation inference (Walter Lindermeir, Dr.-Ing. 07/1997)
- Fast gate-level simulation of power and noise of VLSI circuits (Wolfgang Eisenmann, Dr.-Ing. 03/1996)

Services/Memberships

- 2022: Member of the TUM Task Force for the TUM Researcher Profile
- 2021: Topic Co-Chair for AMS at DATE 2022 and DAC 2022
- 2018: General Chair and Program Chair of the VDE/GMM ANALOG conference
- 2018-2021: Member of DATE TPC, IEEE ICECS TPC, and SMACD TPC
- 2018-: Member of the Board of Directors of the TUM EE Faculty Graduate School
- 2014-2017: IEEE Council on Electronic Design Automation (CEDA) Vice President Publications

- 2014: Member of the Technical Program Committee DATE 2015
- 2012-2013: Member of the Technical Program Committee DAC 2013-2014
- 2012: Member of the Technical Program Committees SMACD 2012, edaWorkshop 2012, ICCAD 2012, ZuE 2012, Member of the “MIP Award” Selection Committee ICCAD 2012
- 2010-2013: Member of the Executive Committee of IEEE ICCAD (Tutorial Chair, Vice Program Chair, European Representative)
- Organizer of Panel and Designer Track sessions at ICCAD 2011
- 2006-2013: Associate Editor IEEE Trans. CAD
- 2011: Special Session Co-Organizer ECCTD
- 2010: DATE Technical Program Co-Chair “Analogue and Mixed-Signal Systems and Circuits”
- Member of the Technical Program Committees DATE 1999-2002/2005-2011/2015/2018
- Member of the Technical Program Committees Analog1999, 2002/03/05/06/08/10-14
- Member of the Technical Program Committees edaWorkshop and ZuE 2007-2014
- 2010, 2009: Member of the Program Committee ACM ISPD 2010, 2011
- 2010, 2009: Chair of the EDAA Best Ph.D. Award Committee Topic 3, New directions in physical design, design for manufacturing, and CAD for analog circuits and MEMS
- 2009: Special Session "Analog placement" Organizer DATE 2009, Special Session "Analog verification" Co-Presenter DATE 2009
- 2008: Member of the Best Paper Committee IEEE ICCAD 2008
- 2008: Special Session "Analog design and EDA" Co-Presenter DATE 2008, Exhibition Panel "Analog verification" Co-Presenter DATE 2008
- 2008: Tutorial "Analog verification" co-organizer and co-presenter Analog'08
- 2006: Member of the ISLPED´06 Program Committee on Analog/Mixed-Signal
- 2005: Tutorial "Yield maximization algorithms" organizer and co-presenter ICCAD 2005
- 2005: Special session "Hierarchical Design and Design Space Exploration of Analog Circuits" organizer DAC 2005
- 2004-2005: Member of the DAC 2005-2006 Program Committee
- 2004-2006: Project leader within edacentrum/BMBF project SAMS
- 2002-2004: Member of the ICCAD 2002, 2003 and 2004 Program Committees
- 2002-2004: Associate Editor IEEE Trans. CAS-II
- 2006,2004: Member of the Program Committee of VLSI Circuits and Systems of EMT Microtechnologies for the New Millennium 2007,2005
- since 2001: Co-Founder and Member of the Technical Advisory Board of MunEDA GmbH Munich
- 2001-2003: Technical Program Chair "Interconnect and Analog/Mixed-Signal CAD" for DATE 2002, "Analog/Mixed-Signal CAD and Symbolic Techniques" for DATE 2003, "RF/Analog/Mixed-Signal CAD" for DATE 2004
- 2001-2005: Subcontract project leader within MEDEA+ project: ANASTASIA+ "Analog Enhancements for a System to Silicon Automated Design"
- 2001-2005: Chair of the GI/GMM/ITG Special Interest Group on Analog Circuit Design
- 2001-2008: Member of the GI/GMM/ITG Steering Committee "Computer-Aided Circuit and System Design"
- 1997-2004: Project leader within DFG Priority Program "Design and design methodology of embedded systems"

- since 1993: Head of the research group on analog design automation at TUM Inst. of EDA
- Member of the Technical Program Committees E.I.S.'01, FDL '01, E.I.S. '03
- Frequent reviewer for IEEE Trans. CAS, IEEE Trans. CAD, JETTA, IJCTA
- Reviewer for ICECS03-02, DAC02-99/97/95, ECCTD 01, D.A.T.E 98, ISCAS00 EURO-DAC96/95
- Review Support for IEEE ICCAD95/94, Special Issue Int. J. CTA 1995, DAC98
- 1997-2000: Member of the department´s committee for teaching evaluation
- 1992-1996: Member of the department´s council
- Since 2014: IEEE Fellow
- since 2003: Senior Member of IEEE
- since 2000: Member of VDE/ITG
- since 2010: Member of VDE/GMM

Honors/Awards

- 2021 Supervisory Award of the TUM ECE Graduate Council
- ICECS 2020 Best Paper Award 3rd place winner
- 2019 TUM Commendation for Excellence in Teaching
- Best Paper Award Runner-Up SMACD 2019
- Elevation to 2014 IEEE Fellow
- Best Paper Award ZuE 2012, together with Michael Zwerger
- Nomination for DATE Best Paper Award 2010
- 2 nominations for ANALOG Best Paper Award 2010
- Best Paper Award ("ITG-Preis") 2008 of the Information Technology Society (ITG) of the German Association for Electrical, Electronic &Information Technologies (VDE)
- Nomination for DATE Best Paper Award 2008
- ACM/IEEE DAC Best Paper Candidate 2006
- Full Professorship offer TU Ilmenau 2005
- Best Teaching Award 2004 of the Faculty Students Association
- Nomination for IEEE ICCAD Best Paper Award 2003
- Full Professorship offer University Frankfurt/Main 2003
- Selected for "Best of ICCAD 20 Years of Excellence in CAD" 2002
- Nomination for DATE Best Paper Award 2002
- ACM/IEEE DAC Best Paper Candidate 1993
- Munich Business Plan Contest 1996 3rd Prize
- Humboldt Research Fellowship Host or Co-Host of: Jiang Hu, Po-Hung Lin, Tsung-Yi Ho, Bo Liu, 2012-2015

Honors/Awards for PhD/MSc candidates in my group

- Inga Abel: Study Award 2020 of the SEW EURODRIVE Foundation 2020 for her MSc Thesis "Automatic Sizing of Analog Operational Amplifiers Using Constraint Programming".
- Inga Abel: VDE Award 2019 for her MSc Thesis "Automatic Sizing of Analog Operational Amplifiers Using Constraint Programming".
- Maximilian Neuner: ICECS 2020 Best Paper Award 3rd place winner,
- Maximilian Neuner: Best Paper Award Runner-Up SMACD 2019
- Michael Zwerger, Maximilian Neuner: Best Paper Award ("GMM-Preis") 2019 of the VDE/VDI-Society Microelectronics, Microsystems and Precision Engineering (GMM)

- Ye X. Ding: Master Thesis Award CDNLive EMEA 2019
- Ye X. Ding: 2nd place Synopsys Annual International Microelectronics Olympiad of Armenia 2018
- Michael Zwerger: Kurt Fischer Dissertation Award 2017 for his Ph.D. thesis “Verification and Synthesis of Analog Power-Down Circuits”
- Florin Burcea: 1st place Synopsys Annual International Microelectronics Olympiad of Armenia 2017, 2016, 2015
- Florin Burcea: VDE Award 2016 for his MSc thesis “Verification and Synthesis of Analog Power-Down Circuits”
- Maximilian Neuner: Kurt Fischer Master Award 2016
- Florin Burcea: 1st place 10th Annual International Microelectronics Olympiad of Armenia 2015
- Michael Eick: VDE Dissertation Award 2013 for his Ph.D. thesis “Structure and Signal Path Analysis for Analog and Digital Circuits”
- Michael Pehl: Kurt Fischer Dissertation Award 2013 for his PhD thesis "Discrete Sizing of Analog Integrated Circuits"
- Michael Eick: Best Paper Award (“GMM-Preis”) 2012 of the VDE/VDI-Society Microelectronics, Microsystems and Precision Engineering (GMM)
- EDA Achievement Award 2012 for MunEDA and the WiCkeD team
- Xin Pan: National Award for Outstanding Self-financed Chinese Students Study Abroad 2011
- EDA Achievement Award 2010 for the VeronA project
- Michael Eick: Kurt-Fischer-Award for an outstanding diploma thesis in 2008

Funding

- 2023-2025 BMBF project HoLoDEC 3 person-years
- 2020-2023 DFG 3 person-years “Verification and synthesis of structural properties of AMS circuit by means of constraint programming, e.g., for ESD and Level Shifters”
- 2016-2019 BMBF project RoMulus 3 person-years
- 2015-2018 BMBF project RESIST 3 person-years
- 2012-2015 BMBF project MEMS2015 3 person-years
- 2012-2015 DFG 3 person-years “Methods for automatic optimization of analog integrated circuits with regard to aging”
- 2011-2014 BMBF project RELY 3 person-years
- 2008-2011 BMBF project HONEY 3 person-years
- 2007-2010 Infineon 1 Research Grant
- 2006-2009 BMBF project VeronA 3 person-years
- 2004-2007 Infineon 1 Research Grant
- 2004-2007 edacentrum project SAMS "Analog synthesis" 3 person-years
- 2003-2006 FLÜGGE program 2 person-years
- 2001-2006 MEDEA+ project: ANASTASIA+ "Analog Enhancements for a System to Silicon Automated Design" 5 person-years
- 1997-2003 Deutsche Forschungsgemeinschaft (DFG), Priority Program "Design and design methodology of embedded systems" 12 person-years
- 1997-2000 Siemens Corp. 2 Research Grants
- 1993-1997 DFG 4 person-years
- 1992-1996 JESSI AC 12 "Analog Design Expert System" 3 person-years

- 1993-1996 Siemens Corp. Research Grant

Professional History

- 2016: Technische Universität: außerplanmäßiger Professor
- 2009: Technische Universitaet Muenchen: Privatdozent (Private Lecturer) in Analog Design Automation
- 2008: Technische Universitaet Muenchen: Habilitation in Analog Design Automation
- since 2004: Academic Director
- since 1993: Institute of Electronic Design Automation, Researcher with Tenure
- 1987-1993: Institute of Electronic Design Automation, Tech. Univ. Munich, Research and Teaching Assistant
- 1986-1987: Siemens Corp., Design Engineer for 4M DRAM test chips

Education

- 1993: Technische Universitaet Muenchen: Dr.-Ing. (~Ph. D.) in Electrical Engineering
- 1986: Technische Universitaet Muenchen: Dipl.-Ing. (~M. Sc.) in Electrical Engineering
- 1982: Darmstadt Institute of Technology: cand.ing.

Teaching

- since 2013: Circuit Simulation (Bachelor course with lecture, tutorial, and lab)
- since 2008: Simulation and Optimization of Analog Circuits at GIST/TUM-Asia (Master course with lecture, tutorial and lab)
- since 2005: Optimization Methods for Circuit Design (earlier title: Simulation and Optimization of Analog Circuits, Master course with lecture, tutorial, and lab)
- since 2011, and 2008, 2004: Layout Synthesis Methods for Integrated Circuits, since 2014 as part of Electronic Design Automation (Master course with lecture and tutorial)
- 2003: Electronic Design Automation, tutorial in Logic Synthesis and Logic Test Design
- 2000-2002, 1987-1988: Tutorial in Computer-Aided Circuit Simulation (Antreich)
- 1993-1998: Assistant for Methods for Business Administration (Hoerbst)
- 1992-1993: Selected Topics of Electronic Design Automation (Antreich)
- 1988-1992: Tutorial in Mathematical Methods of Electrical Engineering (Antreich)

Invited Talks

- IEEE CASS Rio Grande do Sul Chapter Talks, 08.07.2022, “Analog (Layout) Synthesis - Back to the Future”, https://www.youtube.com/watch?v=MZN730AXCkY&t=6s
- ACM Int. Symposium on Physical Design (ISPD) 2022: Analog Synthesis – The Deterministic Way
- 11th IEEE CASS Rio Grande do Sul Workshop: Circuit-Level Yield Analysis and Optimization – The Deterministic Way, 01.10.2021
- Symposium Y: Reliability and Variability of Devices for Circuits and Systems of the 2015 Int. Conf. on Materials for Advanced Technologies, Singapore, 29.06.2015, Performance Evaluation and Lifetime Yield Analysis of Analog Circuits in Consideration of Charge Carrier Trapping and Detrapping

- Instituto Superior Técnico, IST/IT - Integrated Circuits Group, Lisboa, 12.12.2013, On design centering and constraint handling of analog circuits
- ICCAD 2013, International Workshop on Design Automation for Analog and Mixed-Signal Circuits, 21.11.2013, Constraints - The Key to Analog Design Automation
- TUM-Institute of Advanced Study, Garching, 11.03.2013, Challenges in Design Automation of Analog Integrated Circuits
- Infineon Technologies AG, Neubiberg, 04.10.2012: Worst-Case and Yield Analysis
- SMACD Conference, Sevilla, 18.09.2012: Member of the panel (with Günhan Dündar, Georges Gielen, Sani Nassif, Rob Rutenbar) on "Challenges and solutions for electronic circuit design in nanometer CMOS"
- SMACD Conference, Sevilla, 18.09.2012: Worst-case – what you always wanted to know about it and never dared to ask
- DATE Conference, Dresden, 15.03.2012: ITRS 2011 Analog EDA Challenges and Approaches
- TUM Workshop Statistical Methods and Models, Garching, 07.02.2012: The Deterministic Approach to Statistical Design of Electronic Circuits
- NANO-TEC Workshop, Granada, 20.01.2011: Analog/Mixed-Signal Design
- IBM Austin Research Laboratories, Austin TX, 12.11.2010: Hot topics in analog design automation
- Scientific Computing in Electrical Engineering (SCEE), Toulouse, 19.-24.9.2010: From Sizing over Design Centering and Pareto Optimization to Tolerance Pareto Optimization of Electronic Circuits
- MunEDA UGM, 13.11.2009, Towards Reliability Optimization of Analog Integrated Circuits
- Univ Ulm, 10.7.2009, Structural Analysis of Analog Circuits – A Key to Analog Design Automation
- TU München, 9.7.2009, Towards Reliability Optimization of Analog Integrated Circuits
- edaWorkshop, 27.5.2009, Challenges in Analog Sizing for Yield and Reliability
- Design, Automation, and Test in Europe (D.A.T.E) Conference, 2009, Panelist Analog layout synthesis – light at the end of the tunnel?
- Design, Automation, and Test in Europe (D.A.T.E) Conference, 2009, Panelist Formal Approaches to Analog Verification – Now or Never?
- Technische Universität München, 03.07.2008, Pareto Optimization of Analog Integrated Circuits Considering Parameter Tolerances.
- Design, Automation, and Test in Europe (D.A.T.E) Conference, 2008, Panelist Formal Methods to Verify Analog Circuit Design – Key or Phantasm?"
- Design, Automation, and Test in Europe (D.A.T.E) Conference, 2008, Part of Tutorial From Transistor to PLL – Analog Design and EDA Methods
- Technische Universität München, 20.12.2007, Tolerance Design of Analog Integrated Circuits.
- UniBW München, 20.11.2007, Kolloquium Schaltungstechnik, Zur Pareto-Optimierung analoger Schaltungen.
- Technische Universität München, 13.11.2007, Kolloquium Technologienaher Schaltungsentwurf.
- IMMS gGmbH und Technische Universität Ilmenau, 10.10.2007: Dimensionierungsnebenbedingungen bei analogen Schaltungen
- MunEDA User Group Meeting, München, 25.09.2007: A Hierarchical Optimization Method for Phase-Locked Loops

- European Conference on Circuit Theory and Design (ECCTD), Sevilla, 27.08.2007, Pareto Optimization of Analog Circuits Considering Variability
- edacentrum, 21.06.2007: Tutorial Pareto-Optimierung
- ASIM-Fachgruppentagung, 26.02.2007, Hierarchische Optimierung einer Phasenregelschaltung
- IEEE International Conference on CAD, 10.11.2005, Tutorial on Yield Maximization Algorithms
- University of Catania, Sicilia, Summer School on Computational Methods in Electrical Engineering, 13.-16.09.2005: Fundamentals of Design Centering
- IMMS gGmbH und Technische Universität Ilmenau, 11.12.2004: Zur hierarchischen Dimensionierung analoger Schaltungen, Automatenbasierte Synthese digitaler Schaltungen
- Infineon Technologies, München, 13.07.2004: Zum impliziten funktionalen Testentwurf für analoge integrierte Schaltungen
- Kolloquium Schwerpunktprogramm Eingebettete Systeme, Leonberg, 18.11.2003: Simulationsbasierter Testentwurf für analoge Komponenten
- GI/GMM/ITG-Leitungsgremium Rechnergestützter Schaltungs- und Systementwurf, Frankfurt am Main 14.03.2003: Worst-Case-Parametersätze als Schlüssel zur Dimensionierung analoger integrierter Schaltungen
- Technical University Eindhoven, Colloquium Scientific Computing, 12.02.2003: Circuit Sizing and Design Centering of Analog Integrated Circuits
- Philips Eindhoven, 11.02.2003: Circuit Sizing and Design Centering of Analog Integrated Circuits
- Technische Universität Wien, 28.10.2002: Dimensionierung und Testvorbereitung analoger Komponenten
- ANASTASIA+ Workshop "Statistical Methods in Circuit Design", Munich 15.10.2002: Circuit Sizing and Design Centering of Analog Integrated Circuits
- Technische Universität Braunschweig, 15.08.2002: Zur rechnergestützten Dimensionierung analoger integrierter Schaltungen
- Johann Wolfgang Goethe-Universität Frankfurt am Main, 01.08.2002: Zum Entwurf und Testentwurf analoger integrierter Komponenten
- Universität Freiburg, 25.07.2002: Zum rechnergestützten Abgleich beim Entwurf nichtlinearer, kontinuierlicher Schaltungen und Systeme
- GMM/ITG-Diskussionssitzung Entwurf von analogen Schaltungen mit CAE-Methoden (ANALOG), Bremen 14.05.2002: Eine Systematik von Dimensionierungsregeln für den Entwurf analoger integrierter Schaltungen
- Infineon Technologies, Villach, Austria, 15.01.2002: Sizing on System Level
- IEEE International Conference on Computer-Aided Design (ICCAD), Santa Clara, CA, 06.11.2001: The Sizing Rules Method for Analog Integrated Circuit Design
- GI/GMM/ITG-Fachgruppe 2, VDE-Haus, Frankfurt, 12.10.2001: Eine schnelle Methode zur Identifikation mismatch-relevanter Transistorpaare in analogen CMOS-Schaltungen
- Lehrstuhl für Technische Elektronik, Technische Universität München, 19.06.2001: Nominal- und Toleranzentwurf analoger integrierter Schaltungen
- Technische Universität Braunschweig, 12.06.2001: Simulations- und Optimierungsmodelle für analoge Mixed-Signal-Komponenten auf Systemebene

- Kolloquium Schwerpunktprogramm Eingebettete Systeme, Paderborn, 17.10.2000: Simulationsbasierter Testentwurf für analoge Komponenten mittels deterministischer und statistischer Verfahren
- Infineon Technologies AG, München, 27.06.2000: Nominal and Tolerance Design of Analog Integrated Circuits
- Workshop Schwerpunktprogramm Eingebettete Systeme, Frankfurt, 18.05.2000: Modellierung und Test analoger Systemkomponenten
- Advantest, München, 13.01.1999: Dimensionierung und Testentwurf analoger Schaltungen
- Johann Wolfgang Goethe Universität Frankfurt, 22.10.1998: Testentwurf analoger integrierter Schaltungen
- Kolloquium Schwerpunktprogramm Eingebettete Systeme, München, 09.10.1998: Analogtestentwurf mit Versorgungsstrommessungen für parametrische und katastrophale Fehler
- Design, Automation, and Test in Europe (D.A.T.E) Conference, Paris, 26.02.1998: Analog test design with IDD measurements for the detection of parametric and catastrophic faults
- Kolloqium Schwerpunktprogramm Eingebettete Systeme, Stuttgart, 16.04.1997: Simulationsbasierter Testentwurf für gemischt analog-digitale Systeme
- GMM/ITG-Diskussionssitzung Entwurf von analogen Schaltungen mit CAE-Methoden (ANALOG), Berlin, 2.10.1996: WiCkeD: Worst-Case- und Ausbeute-Analyse
- TEMIC Semiconductor, Ulm, 28.09.1995: Worst-Case-Analyse, Ausbeute-Analyse und Entwurfszentrierung für analoge Schaltungen
- TEMIC Semiconductor, Heilbronn, 07/1995: Worst-Case-Analyse, Ausbeute-Analyse und Entwurfszentrierung für analoge Schaltungen
- Universität Hannover, 03.12.1993: Toleranzentwurf analoger integrierter Schaltungen
- Technische Universität Braunschweig, 16.06.1992: Zur Entwurfszentrierung analoger integrierter Schaltungen
- CSEM Swiss Center for Electronics and Microtechnology, Neuchatel, 09.01.1992: Circuit optimization driven by worst-case distances
- IEEE International Conference on Computer-Aided Design (ICCAD), Santa Clara, CA, 11.11.1991: Circuit optimization driven by worst-case distances
- GMM/ITG-Diskussionssitzung Entwurf von analogen Schaltungen mit CAE-Methoden (ANALOG), Paderborn, 11.10.1991: Zur Entwurfszentrierung analoger integrierter Schaltungen
- International Association for Mathematics and Computers in Simulation (IMACS) World Congress, Ireland, 24.07.1991: A unified approach to nominal and tolerance design
- Siemens AG, München, 13.12.1990: Ein einheitlicher Ansatz zum Nominal- und Toleranzentwurf

Advised Student Projects 2013-2016 (many more since then)

- Benedikt Gottinger, Improving Scan Diagnosis of Fails during 1-Pin Test, Master Thesis, November 2016
- Amine Gouiaa, Development of a Debug Tool based on Bit-banging for Aurix Microcontrollers, Bachelor Thesis, August 2016
- Tauseef Siddiqui, Analysis of an isolated communication channel and data path, Master Thesis, July 2016

- Zhe Chen, Design and Optimization of a Permanent Magnet Synchronous Machine by Finite Element Method, Master Thesis, July 2016
- Avantika Singh, Investigation of the potential of an analog implementation of a Gb/s higher linearity Feed Forward Equalizer (FFE) at the receiver side, Master Thesis, June 2016
- Benedikt Gottinger, Machbarkeitsstudie für eine neue X-Masking-Architektur, Master Internship, May 2016
- Michael Werner, Beschleunigung von bildverarbeitenden Reverse-Engineering-Prozessen, Master Internship, May 2016
- Xiaoming Huang, Large Scale Chip Circuit Reverse Engineering, Master Thesis, April 2016
- Alexander Preißner, Design, Implementation, and Verification of an FPGA-Based IC evaluation platform control unit featuring accurate timing capability, Bachelor Thesis, February 2016
- Gaurav Shrivastava, Sizing of Power-Down Switches for Analog Circuits, Master Thesis, February 2016
- Shwetha Ramachandran, Development of Firmware for IRXP Crypto Simulator of LTR 400-C Transponder, Master Internship, November 2015
- Vivin Richards Allimuthu Elavarasu, Development, Design, and Validation of the Test Environment for a System-In-Package Test Chip, Master Thesis, November 2015
- Maximilian Neuner, Power-Down-Schaltungs- und Schaltbildsynthese, Master Thesis, October 2015
- Ali Ferchichi, Optimization of a Successive-Approximation Analog-to-Digital Converter, Master Thesis, October 2015
- Patrik Valentin Ulrich Sandoval, Interpretation digitaler CMOS-Schaltungen, Bachelor Thesis, September 2015
- Anke Jönck, Integration and evaluation of a software-driven hardware verification tool in the MSP430 mixed-signal-microcontroller verification methodology, Bachelor Thesis, April 2015
- Matthias Meyer-Jungclaussen, Entwicklung eines OpenAccess Schematic-Viewers mit Qt, Master Internship, December 2014
- Inga Abel, Ingenieurpraxisbericht - Entwurf und Test von Bauelementen und Schaltungen, Bachelor Internship, October 2014
- Felix Schillmaier, Power-Down Synthese unter Verwendung konstruktiver Regeln, Bachelor Thesis, October 2014
- Pantelis-Rafail Vlachas, Verification of the Power-Down Mode or Analog Circuits using Constraint Programming, Bachelor Thesis, July 2014
- Nick Burmester, Hochspannungsmodul Feinstaubpartikelabscheider, Bachelor Internship, May 2014
- Rakesh Jha, Reverberation cancellation of ultrasonic sound waves generated by multiple sources on a cylindrical shell, Master Thesis, October 2013
- Hentati Houcem, Verifikation von Aging-Constraints fuer analoge Schaltungen, Bachelor Internship, October 2013
- Akshaya Prashanthi LAKSHMI NARAYANAN, Development of Reusable and Self-Checking Mixed Signal Testbench using UVM, Master Thesis, September 2013
- Maximilian Neuner, Power-Down-Synthese unter Verwendung von Constraint-Programmierung, Bachelor Thesis, August 2013
- Radhouane Bradai, Design, Sizing, and Parametric Yield Analysis of a 2nd-Order Sigma-Delta Analog-to-Digital Converter, Master Internship, July 2013

- Sharad Shukla, Robustness Validation under the Influence of Operating Condition Variations, Master Thesis, March 2013

Scientific Accomplishments that led to IEEE Fellow Elevation

Helmut Graeb has contributed seminally to the design automation of analog circuits, which are crucial components of integrated circuits. His work comprises many topics, including Pareto optimization considering parameter tolerances, analog design for yield and reliability, hierarchical analog sizing, analog/mixed-signal test design, discrete analog sizing, structural analysis of analog and digital circuits, and analog layout synthesis.

Two outstanding contributions have had a significant and lasting impact on design automation and design methodology of integrated circuits.

The first outstanding contribution is to yield optimization and design centering.

Helmut Graeb has developed a theory of worst-case and yield analysis and optimization. Based on mathematical optimization theory, it provides a rigorous formulation of three constitutive types of worst-case analysis, yield analysis by a geometric approach, and fundamental formulations of circuit optimization. His theory has strongly impacted design practice in the industry in two respects. On the one hand, with Graeb's worst-case theory, the requirements on process technologists' and analog designers' contributions to worst-case design are now much better understood and handled in industrial practice. On the other hand, he proposed a perspicuous measure for circuit reliability, the so-called worst-case distance. It provides a one-dimensional x-sigma robustness measure of a performance feature in the presence of a multi-parameter statistical variability space. The worst-case and yield analysis and optimization objectives have become more articulate and easy to interpret in daily design practice.

The Helmut Graeb group has developed sophisticated solution methods for analysis and optimization of worst-case and yield. The tool "WiCkeD" ("W"orst-"C"ase "D"istance) is based on deterministic nonlinear programming and is especially efficient.

An example of how Graeb and his group get to the mathematical bottom of technical problems is the identification of "mismatch" with semidefinite Hessian matrices of performance models and the development of corresponding solution algorithms in worst-case analysis.

The tool WiCkeD has been extensively proven in industrial practice. Two members of his group founded MunEDA GmbH, successfully commercialized the tool, and further developed it. It is worth mentioning that MunEDA, co-founded by Graeb, is an independent company that has been running successfully for now 15 years.

The second prominent contribution is on structural analysis of circuits.

Numerical optimization/simulation-based sizing of analog circuits had long been impossible: too many implicit constraints whose absence leads numerical optimization to unfeasible solutions exist. Analytical model-based optimization tools that include such constraints without making them available outside the tool have been presented. In 2001, Graeb, as principal author, published a new systematic

and transparent method to capture comprehensive design knowledge of fundamental analog building blocks for the sizing process.

This method was essential to enable automatic analog circuit sizing by numerical optimization and simulation. The core of the method is a structural analysis of a flat netlist, which identifies pairs and groups of transistors with specific functionality in a hierarchical way according to a well-defined library and then instantiates corresponding constraints for geometries and voltages of single transistors and groups of transistors. It is worth mentioning that Cadence adopted this so-called sizing rules method in its analog optimization tool suite.

In the meantime, Graeb and his group have done essential extensions of the method to bipolar and digital circuits. Further research recently led to another significant result: an automatic method to analyze the signal flow through basic building blocks. This method provides a qualitative signal flow graph along structural components considering symmetrical signals. It opens new opportunities to move between the structural and behavioral description of analog circuits, which is the core of synthesis. Advanced generation of matching and symmetry constraints have been presented by Graeb and his group, with a significant impact on design quality and design efficiency of analog sizing as well as analog placement. Even more, they presented an advanced automatic generation of a hierarchical placement "plan," which enabled a new constructive method for analog placement.

With these and other excellent contributions, published in around 150 papers, Graeb has gained outstanding international acknowledgment in the area of analog design automation, which is also indicated by regular invitations and services to the community in the form of invited talks, reviews, editorships, and conference topic chair positions.

Evidence of technical accomplishments mentioned above:

1. K. Antreich, H. Graeb: Circuit optimization driven by worst-case distances, IEEE International Conference on Computer-Aided Design (ICCAD), 1991. (Selected for "Best of ICCAD - 20 Years of Excellence", 2003)

   (Contributor to work) Helmut Graeb developed a new deterministic method for the design centering of integrated circuits on the transistor level with a user-friendly objective used in a divide-and-conquer approach. Yield can now be related to x-sigma reliability measures based on a general, mathematically sound method. CAD developers and designers have widely adopted the approach, and it has become a standard for tolerance design. It is especially suited in the case of rare-event statistics.

2. H. Graeb, S. Zizala, J. Eckmueller, K. Antreich: The Sizing Rules Method for Analog Integrated Circuit Design, IEEE International Conference on Computer-Aided Design (ICCAD), 2001.

   (Leader of the group) This is a new systematic and transparent approach to automatically identify analog building blocks and generate design constraints. Guided by Helmut Graeb, an exemplary approach to capture analog circuit design knowledge in a form that can be exploited by electronic design automation was developed. It was the enabling technology for the automatic sizing of analog circuits and has been integrated into the tool suites of major EDA vendors.

3. M. Eick, M. Strasser, Kun Lu, U. Schlichtmann and H. Graeb: Comprehensive Generation of Hierarchical Placement Rules for Analog Integrated Circuits, IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), 2011. (VDE-GMM Best Paper Award 2012)

   (Leader of the group) Based on new ideas to switch between behavioral and structural views of analog circuits, a new approach to generating both rules and constraints for placement from the netlist of an analog circuit has been presented. Automatic computation of constraints for, e.g., alignment, matching, or symmetry and a hierarchical plan for the placement now enable a more practicable analog layout synthesis. The method has received a Best Paper Award and is transferred into an industrial design flow.

Evidence of further technical accomplishment:

Analog structural analysis

1. T. Massier, H. Graeb, U. Schlichtmann: The Sizing Rules Method for CMOS and Bipolar Analog Integrated Circuit Synthesis, IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), 2009.

   (Leader of the group) Advanced structural analysis and sizing constraint generation for analog circuits, including bipolar circuits, and arbitration of ambiguities during the detection process.

2. M. Eick, H. Graeb, MARS: Matching-driven analog sizing, IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), 2012.

   (Leader of the group) A new method to analyze the signal flow through the internal circuit structure and automatically determine matching constraints, leading to greater efficiency of the optimization process and better design quality.

Analog tolerance design

3. K. Antreich, H. Graeb, C. Wieser: Circuit analysis and optimization driven by worst-case distances, IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), 1994.

   (Leader of the group) New problem formulations and deterministic optimization algorithms for worst-case and yield analyses are developed.

4. K. Antreich, J. Eckmüller, H. Graeb, M. Pronath, F. Schenkel, R. Schwencker, S. Zizala: WiCkeD: Analog Circuit Synthesis Incorporating Mismatch, IEEE Custom Integrated Circuit Conference (CICC), 2000.

   (Leader of the group) The mismatch is formally identified as the semidefiniteness of the second-order derivative of the performance function, and an algorithm for tolerance analysis and optimization that copes with the mismatch is presented.

5. H. Graeb: Analog Design Centering and Sizing, Springer 2007, ISBN 978-1-4020-6003-8.

   This is a standard work on mathematical problem formulations of different types of worst-case analysis, yield analysis, yield optimization, and design centering.

Analog test design

6. W. Lindermeir, H. Graeb, K. Antreich: Analog Testing by Characteristic Observation Inference, IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), 1999.

(Contributor to work) This new statistical method is used to compute test specifications for surrogate measurements that match the original analog circuit specification.

Analog Pareto optimization

7. G. Stehr, H. Graeb, K. Antreich: Analog Performance Space Exploration by Normal-Boundary Intersection and Fourier-Motzkin Elimination, IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), 2007. (VDE-ITG Best Paper Award 2008)

   (Leader of the group) New deterministic methods for design space exploration of analog circuits, together with a piecewise linear approximation of the feasible performance space, which has been applied by other researchers in analog synthesis, are presented.

8. D. Mueller-Gritschneder, H. Graeb, U. Schlichtmann: A Successive Approach to Compute The Bounded Pareto Front of Practical Multi-Objective Optimization Problems, SIAM Journal on Optimization (SIOPT), 2009.

   (Leader of the group) A new mathematical contribution and algorithm to compute high-dimensional Pareto fronts with constructive methods has been given.

Analog placement

9. M. Strasser, M. Eick, H. Graeb, U. Schlichtmann, F. Johannes, Deterministic Analog Circuit Placement using Hierarchically Bounded Enumeration and Enhanced Shape Functions, IEEE Int. Conference on Computer-Aided Design (ICCAD), 2008.

   (Contributor to work) Hierarchical analog placement with a constructive approach using hierarchical placement rules, which mimics the proceeding of layout engineers.

10. H. Habal, H. Graeb, Constraint-based Layout-driven Sizing of Analog Circuits, IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), 2011.

    (Leader of the group) A new, template-free, yet efficient method for sizing with in-loop entire layout generation and parasitic extraction is presented.

Publications

Books

1. H. Graeb (Editor): Analog Layout Synthesis – A Survey of Topological Approaches, Springer 2011, ISBN: 978-1-4419-6931-6.
2. H. Graeb: Analog Design Centering and Sizing, Springer 2007, ISBN 978-1-4020-6003-8.
3. H. Graeb: Optimization of Analog Circuits - Compendium, Exercises, Technische Universitaet Muenchen 2008-2016.

International Journal Articles and Book Chapters

4. M. Putz, M. Ludwig, B. Lippmann and H. Graeb: PLaNe: Reverse Engineering of Planar Layouts to Gate-Level Netlists. IEEE Physical Assurance and Inspection of Electronics (PAINE), 2023.
5. Inga Abel, Maximilian Neuner, Helmut Graeb: A Functional Block Decomposition Method for Automatic Op-Amp Design, Integration – the VLSI journal, 2022. arxiv.org: https://arxiv.org/abs/2012.09051, 2020.

6. Inga Abel, Helmut Graeb, FUBOCO: Structure Synthesis of Basic Op-Amps by FUnctional BlOck Composition, ACM Trans. Design Automation of Electronic Systems (TODAES), 2022. arxiv.org: https://arxiv.org/abs/2101.07517, 2021.
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8. Alessandro Girardi, Helmut Graeb, Process-Variation Aware Design Optimization of an Integrated Microprobe Detector, Analog Integrated Circuits and Signal Processing, 2021.
9. Inga Abel, Maximilian Neuner, Helmut Graeb, COPRICSI: COnstraint-PRogrammed Initial Circuit Sizing, Integration – the VLSI Journal, 2021.
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11. Florin Burcea, Dani Tannir, Helmut Graeb, Fast SPICE-Compatible Simulation of Low-Power On-Chip PWM DC-DC Converters with Improved Ripple Accuracy, IEEE Trans. on Power Electronics (TPE), 2020.
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15. Ye Ding, Florin Burcea, Husni Habal, Helmut Graeb, PASTEL: Parasitic Matching-Driven Placement and Routing of Capacitor Arrays with Generalized Ratios in Charge-Redistribution SAR-ADCs, IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), 2019.
16. Vittorio Latorre, Husni Habal, Helmut Graeb, Stefano Lucidi, Derivative-free methodologies for circuit worst-case analysis, Optimization Letters, Springer 2018, https://doi.org/10.1007/s11590-018-1364-5.
17. F. Santoro, R. Kuhn, N. Gibson, N. Rasera, T. Tost, H. Graeb, B. Wicht, R. Brederlow, A Hysteretic Buck Converter with 92.1% Maximum Efficiency Designed for Ultra-Low Power and Fast Wake-Up SoC Applications, IEEE Journal of Solid-State Circuits (JSSC), 2018.
18. Michael Zwerger, Maximilian Neuner, Helmut Graeb, Analog Power-Down Synthesis, IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), 2017. **(GMM-Prize 2019)**
19. Pang-Yen Chou, Nai-Chen Chen, Mark Po-Hung Lin, Helmut Graeb, Matched-Routing Common-Centroid 3-D MOM Capacitors for Low-Power Data Converters, IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2017.
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21. F. Burcea, H. Habal, H. Graeb, A new chessboard placement and sizing method for capacitors in a charge-scaling DAC by worst-case analysis of nonlinearity, IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), 2016.

22. Mark Po-Hung Lin, Po-Hsun Chang, Shuenn-Yuh Lee, Helmut E. Graeb, DeMixGen: Deterministic Mixed-signal Layout Generation with Separated Analog and Digital Signal Paths, IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), 2016.
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57. Maximilian Neuner, Helmut Graeb, Hierarchical Analog Power-Down Synthesis, IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2020. (**Best Paper Award 3rd place winner**)
58. Inga Abel, Helmut Graeb, Structural Synthesis of Operational Amplifiers Based on Functional Block Modeling, IEEE Int. Conference on Computer-Aided Design (ICCAD), 2020.
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60. Alessandro Girardi, Helmut Graeb, Modeling and Optimization of a Microprobe Detector for Area and Yield Improvement, Symposium on Integrated Circuit and Systems Design (SBCCI), 2020.
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