Late Breaking Results: Efficient Built-in Self-Test for Microfluidic Large-Scale Integration (mLSI)

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ABSTRACT

Control channels on microfluidic large-scale integration (mLSI) chips are prone to blockage and leakage defects. In this work, we propose a built-in self-test (BIST) method that drastically improves the test efficiency. Given n to-be-tested control channels, we reduced the number of test patterns for blockage and leakage tests from $\lceil \frac{n}{2} \rceil$ to 1, and from $\lceil \log_2(n+1) \rceil$ to $\lceil \log_2(\chi(G)+1) \rceil$, respectively, where $\chi(G)$ denotes the vertex chromatic number of a graph G consisting of n vertices. We fabricated our design and demonstrated the feasibility and efficiency of our method.

1 INTRODUCTION

Microfluidic large-scale integration (mLSI) is a promising platform for bio-assays [5]. By integrating micro-channels and valves onto a small multi-layer chip, functional modules can be formed for various operations. To date, valves can be integrated onto mLSI chips at a density of 1 million valves per cm^2 [1], demonstrating great potential for ultra-high-throughput applications.

An mLSI chip consists of a *flow layer* with *flow channels* for bio-reactions, and a *control layer* with *control channels* for operating valves. While a flow channel is typically hundreds of micrometers wide, a control channel is only tens of micrometers wide and more prone to *blockage* and *leakage* defects. Blockage happens when a channel is broken or blocked so that pressure cannot pass through; leakage happens when two independent channels are accidentally connected so that pressure will leak from one channel to the other. To ensure normal execution, mLSI chips need to be tested before use. State-of-the-art mLSI test methods include *functional test* (FCT) [3] and *built-in self-test* (BIST) [4]. FCT tests control channels through flow channels. Due to the usually limited number of flow ports on a chip, defects may be masked. Besides, the tests require extra pressure meters and commercial ATPG software, which results in additional costs. BIST directly tests the control channels by connecting them to an integrated test module. Thus, the fault coverage is not limited by the flow ports, and the test patterns can be carried out without extra equipment, software, or high skill. However, as the integration scale increases, the state-of-the-art BIST suffers from efficiency concerns. Specifically, each blockage test pattern can only test two control channels at a time; and the leakage test patterns unnecessarily test every pair of different control channels, although leakage defects happen mostly only between parallel control channels that are close to each other [6].

In this work, we propose a novel blockage module to test an arbitrary number of control channels with constantly one test pattern; and we develop a vertex-coloring model to customize the leakage module so that only relevant control channels [1] are tested, and the number of test patterns can stay ≤ 3 even for large designs. The two modules are then combined to reduce implementation overhead.

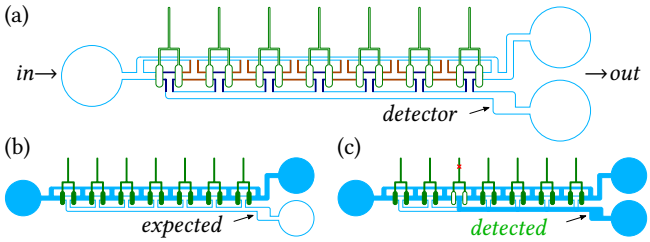

Figure 1: (a) A blockage module. Type-I and type-II segments are colored in dark blue and brown, respectively. (b) If there is no blockage, the detector will be empty. (c) If any control channel is blocked, fluids can be observed in the detector.

2 METHOD

We divide an mLSI chip into a *main circuit* and a *test module*. Control channels are extended from the main circuit to the test module, but flow channels of the main circuit and the test module stay independent, so that control channel defects can propagate to and be tested at the test module without polluting the main flow circuit.

Our blockage module consists of three flow channels, referred to as the top, central and bottom flow channels. As shown in Figure 1(a), each to-be-tested control channel addresses two valves in the central flow channel. We refer to the central flow channel segments between valves addressed by the same and different control channels as type-I and type-II segments, respectively. In particular, type-I segments are connected with the bottom flow channel, and type-II segments are connected with the top flow channel. There is a larger chamber, referred to as the *detector*, at the bottom flow channel near the bottom output flow port for inspection.

In a blockage test, we pressurize all control channels and send fluids from the input flow port. Regardless of potential control channel defects, a stable flow path through the top flow channel is always available. If there is no blockage, as shown in Figure 1(b), the type-I segments will be isolated from the flow path. Thus, no fluids can enter the bottom flow channel or the detector. On the other hand, if there is a blockage defect in any control channel, as shown in Figure 1(c), a flow path will branch off through the type-I segment addressed by the defected control channel to the bottom flow channel. Thus, fluids will appear in the detector.

Our leakage module consists of a few parallel flow channels connected to two opposite flow ports, and each to-be-tested control channel is assigned an index in binary and connected to certain valves on the flow channels, so that a control channel addresses the i^{th} flow channel, if and only if the i^{th} bit of its index is '1', as shown in Figure 2(a). In particular, relevant control channels are assigned with different indices. In the i^{th} test pattern, we pressurize

[1]We refer to a pair of control channels that should (should not) be considered for leakage test as a pair of *relevant* (*irrelevant*) control channels.

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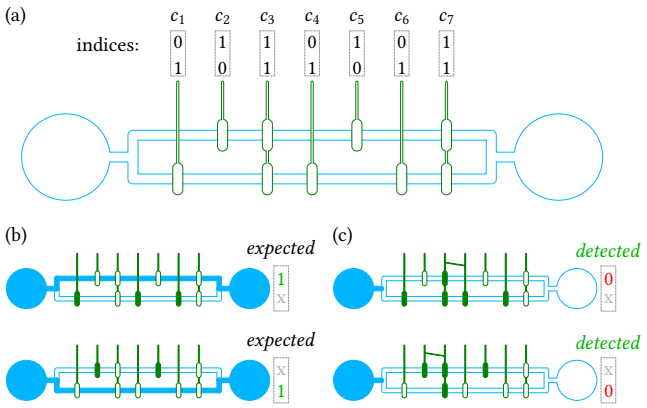

Figure 2: (a) A customized leakage module. Besides neighboring control channels, (c_1, c_3), (c_2, c_4), (c_3, c_5) and (c_5, c_7) are also given as relevant control channel pairs. (b) Leakage test patterns and expected results. (c) If there is a leakage between c_3 (11) and c_4 (01), with the 1st test pattern, no fluids can be deteced in the 1st flow channel. Similarly, if there is a leakage between c_2 (10) and c_3 (11), with the 2nd test pattern, no fluids can be detected in the 2nd flow channel.

all control channels that do not address the i^{th} flow channel, so that fluids are expected to be observed at the end of the i^{th} flow channel, as shown in Figure 2(b); but if there is a leakage between any two channels that differ in the i^{th} bit, pressure will leak from the control channel that does not address the i^{th} flow channel to the control channel that addresses the i^{th} flow channel, and thus fluids will not be observed at the end of the i^{th} flow channel, as shown in Figure 2(c). Since the indices of a pair of relevant control channels must differ by at least one bit, there is at least one pattern for the leakage test between any two relevant control channels.

To index relevant control channels differently, we propose a *vertex coloring model* $G = (V, E)$, in which each control channel $c \in V$ is modeled as a vertex, every pair of relevant control channels $(c_x, c_y) \in E$ is modeled as an edge, and every index $i_c \in \mathbb{N}$ is modeled as the color of c. The chromatic number $\chi(G)$, i.e., the smallest number of colors to color G so that adjacent vertices are in different colors, thus represents the largest control channel index. Starting from 1, the control channels can be indexed with $\lceil \log_2(\chi(G)+1) \rceil$ bits, i.e., $\lceil \log_2(\chi(G)+1) \rceil$ flow channels are required to implement the leakage module, and $\lceil \log_2(\chi(G)+1) \rceil$ test patterns are required to carry out the leakage tests. According to Brook's theorem, $\chi(G)$ is limited by ΔG, i.e. the degree of graph G. Since only close and parallel control channels are relevant, we can empirically expect $\Delta G \leq 7$, and thus $\lceil \log_2(\chi(G)+1) \rceil \leq 3$ even for large designs.

3 ANALYSIS AND EXPERIMENTAL RESULTS

Given n control channels, compared to the state-of-the-art BIST, we reduce the number of blockage and leakage test patterns from $\lceil \frac{n}{2} \rceil$ to 1, and from $\lceil \log_2(n+1) \rceil$ to $\lceil \log_2(\chi(G)+1) \rceil$, respectively. For example, for a chip with 114 control channels [2], the state-of-the-art BIST requires 57 and 11 patterns for blockage and leakage tests, respectively, and 11 flow channels in the test module; while our method only requires 1 and 2 patterns for blockage and leakage tests, respectively, and 3 flow channels in the test module.

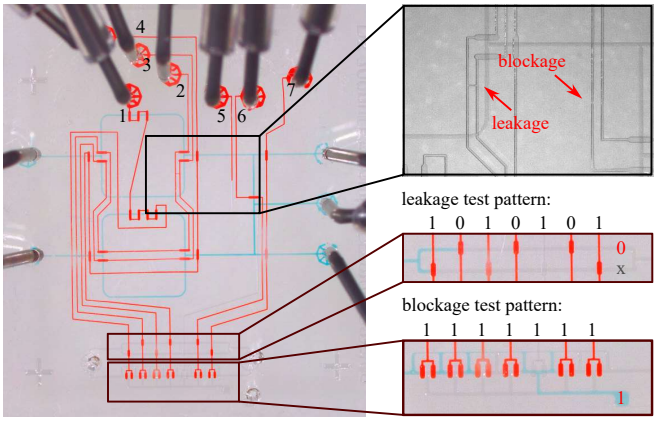

Figure 3: An mLSI chip integrated with the test module.

To verify the feasibility of our designs, we fabricated an mLSI chip with leakage (between control channels 2 and 3) and blockage (in control channel 5) defects, as shown in Figure 3. The blockage and leakage modules are combined to share flow ports. We dye the control layer red and the flow layer blue to demonstrate the channel structure. The chip consists of seven control channels. Neighboring control channels are considered relevant and address different flow channels in the leakage module. Specifically, channels with odd indices only address the second flow channel, and channels with even indices only address the first flow channel. In the leakage test, we pressurize all control channels with odd indices and send fluids from the left flow port. Since there is a leakage defect between channels 2 and 3, the second left valve in the first flow channel is unexpectedly closed, and no fluids can be detected at the right end of the first flow channel. Also, in the blockage test, due to the blockage defect in channel 5, the corresponding valves keep open despite the pressurization. Thus, fluids are found in the detector.

4 CONCLUSION

We propose a novel BIST method with two integrated test module designs for blockage and leakage tests. In particular, the number of test patterns and hardware resources required by our method does not increase with the number of to-be-tested control channels. As the integration scale of mLSI chips approaches 1 million valves per cm^2 [1], our method shows significant advantages in scalability compared to the state-of-the-art method.

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