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Optimized Stabilization and Validation of Fast Transients in Vehicular Power Systems

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Abstract

The transport sector aims to reduce anthropogenic greenhouse gas emissions to decelerate the prevailing global warming. Motor vehicles are increasingly electrified and equipped with automated driving functions. The power supply of safety-critical vehicular components needs to be secured to provide evidence of fail-operational functions. This elevates the effort required for the development of the vehicular power system. To cope ambitious vehicle development targets in an appropriate time, virtual design methods were introduced in the literature. However, power system disturbances in a frequency of up to 150 kHz were detected but not sufficiently studied.

This research project focuses on modeling methods for the power distribution and consumption in vehicular low-voltage power systems. Major consumers with a significant influence on fast transients are identified. They are modeled on the basis of system identification and an adapted RLC-synthesis method. DC/DC converters interconnect different voltage levels. Calculating their switched models requires high computational efforts. The proposed state-space average algorithm reduces the computation time by up to 95 %, while preserving a high level of accuracy for fast transients.

Vehicular components with passive RLC-filters are connected to each other by means of a low-impedance wiring harness. The predominant system-inherent resonance behavior leads to oscillating voltages at the occurrence of fast transients. Considering oscillating poles in transfer functions, a new metric for voltage stability is proposed. To suppress the negative impact on the power supply, stabilization measures are identified. The wiring harness geometry significantly influences the voltage stability during high dynamic power fluctuations. Therefore, a nonlinear control method applied on distributed converters stabilizes the voltage imbalances at different connection points. Furthermore, system-designed multi-stage passive band-pass filters suppress voltage oscillations due to the system's resonance behavior.

Established simulation models of power distribution and consumption are separated according to their validity in the frequency domain. Their validation up to 150 kHz is carried out by measurements on a conceptualized vehicular power system test bench. Design algorithms and a multi-criteria heuristic particle-swarm optimization framework are used to both increase voltage stability and reduce energy loss of novel stabilization measures. A band-pass filter equipped with a total of 200 µF of capacitance leads to a similar voltage stability as a 140 mF reference capacitor could achieve. Prototype hardware of stabilization approaches is measured and contrasted to simulation results.

Contents

Glossary

AC	Alternating Current
ADAS	Advanced Driver Assistance Systems
ADC	Analog-to-Digital Converter
AP	Access Point
APA	Audio Power Amplifier
API	Application Programming Interface
ASIL	Automotive Safety Integrity Level
BB	Busbar
BEV	Battery Electric Vehicle
CAN	Controller Area Network
CCU	Central Control Unit
CMC	Current Mode Control
DCR	Direct-Current-Resistance
DFT	Discrete Fourier Transform
DISMC	Double-Integral Sliding Mode Control
DLC	Double-Layer Capacitor
DRL	Daytime Running Lamp
DUT	Device under Test
EBP	Electric Brake Pump
ECU	Electronic Control Unit
EFD	Electric Fan Drive
EMF	Electromotive Force
EMI	Electromagnetic Interference
EPS	Electric Power Steering
ESR	Equivalent Series Resistance
FDNE	Frequency Dependent Network Equivalent
FEM	Finite Element Method
FFT	Fast Fourier Transform
FID	Fault Injection Device
FTA	Fault Tree Analysis
HEV	Hybrid Electric Vehicle
HLi	Headlights
HV	High Voltage
ICE	Internal Combustion Engine Vehicle
KBL	Kabelbaumliste

LF	Low-Frequency
LV	Low Voltage
O/L	Open-Loop
OCV	Open Circuit Voltage
ODE	Ordinary Differential Equation
PCB	Printed Circuit Board
PD	Power Distributor
PFD	Partial Fraction Decomposition
PMSM	Permanent Magnet Synchronous Machine
PS	Parallel-Series
PSFB	Phase-Shifted Full-Bridge
PVC	Polyvinyl Chloride
PWM	Pulse Width Modulation
QM	Quality Management
RAS	Rear Axle Steering
RLC	Resistor-Inductor-Capacitor
S/C	Short Circuit
SMA	Simple Moving Average
SMC	Sliding Mode Control
SOA	Safe Operating Area
SoC	State-of-Charge
SOP	Start of Production
SP	Series-Parallel
TLi	Taillights
TVS	Transient Voltage Suppressor
VBR	Voltage-behind-Reactance
VMC	Voltage Mode Control
WIP	Windshield Wiper

Mathematical Symbols

A	Wire Cross-Section	mm^2
C	Capacitance	F
C'	Per-Unit-Length Capacitance	F/m
$C(s)$	Control Transfer Function in Laplace Domain	1
D	Damping	1
E	Electrical Energy	Ws
$G(s)$	Transfer Function in Laplace Domain	1
I	Constant Electrical Current	A
K	Auxiliary Parameter	n/a
L	Self-Inductance	H
L'	Per-Unit-Length Self-Inductance	H/m
M	Mutual Inductance	H
M'	Per-Unit-Length Mutual Inductance	H/m
P	Electrical Power	W
R	Ohmic Resistance	Ω
R'	Per-Unit-Length Ohmic Resistance	Ω/m
$R(s)$	Auxiliary Transfer Function in Laplace Domain	1
S	Scattering Parameter	1
T	Period	s
V	Constant Electrical Voltage	V
Y	Electrical Admittance	$1/\Omega$
Z	Electrical Impedance	Ω
Δ	Relative or Absolute Deviation	%
δ	Relative or Absolute Deviation	%
λ	Wavelength	m
$\mathbf{0}$	Zero Vector	1
$\mathbf{C}$	Capacitance Matrix	F
$\mathbf{G}$	Transfer Function Matrix	1
$\mathbf{I}$	Identity Matrix	1
$\mathbf{L}$	Inductance Matrix	H
$\mathbf{S}$	Scattering Matrix	1
$\mathbf{Y}$	Admittance Matrix	$1/\Omega$
$\mathbf{Z}$	Impedance Matrix	Ω
$\mathbf{e}$	Canonical Basis Vector	1
$\mathbf{u}$	Input Vector	1

$\mathbf{x}$	State Vector	1
Q_{v}	Voltage Stability, Voltage-Time Integral	Vs
ε_{v}	Settling Time Criterion	s
r_{s}	Resistance Selection Scalar	1
μ	Magnetic Permeability	H/m
ω	Angular Frequency	rad/s
ρ	Specific Electrical Resistance	$\Omega\,$m/mm
$\underline{p}, \underline{r}$	Complex Pole, Residue	$1{+}j$
ε	Dielectric Permittivity	F/m
φ	Phase Angle	°
c	Speed of Light	m/s
d	Duty Cycle	1
f	Frequency	Hz
h, l, r, w	Height, Length, Radius, Width	m
i	Time-Domain Electrical Current	A
k	Integer constant	1
m	Slew Rate of Electrical Current	A/s
n	Integer constant	1
s	Laplace variable	$1{+}j$
t	Time	s
v	Time-Domain Electrical Voltage	V

Figures

Tables

1 Introduction

This chapter provides an overview of the motivation of this research project. The specific goals are stated and possible challenges are presented. Finally, the structure of this dissertation is outlined.

1.1 Motivation

A central challenge of our society is global warming. The combustion of fossil fuels boosts the amount of greenhouse gases in the atmosphere. The transport sector contributes 14 % to 15 % of anthropogenic carbon dioxide emissions to global warming [1, p. 1491]. Beyond, the United Nations (UN) estimates that the world population will grow to 9 billion by 2050 [2, p. 2]. People will largely settle in the urban region [3, p. 1233]. The rising population is accompanied by an increasing demand for mobility [3, p. 524].

To counter global warming, one approach is the electrification of vehicles [4]. According to the report by the German Federal Ministry for the Environment, Nature Conversation, Nuclear Safety and Consumer Protection (BMU), electrified vehicles can significantly reduce environmental and climate pollution. However, a growing share of renewable energies in electricity generation is necessary. Taking into account the entire life cycle of the vehicle, greenhouse gas emissions of Battery Electric Vehicles (BEVs) are at least 20 % lower than those of Internal Combustion Engine Vehicles (ICEs) [5, p. 7]. The life cycle of a vehicle includes production, maintenance, disposal, recycling, energy consumption and the generation of electricity or the production of fuel.

To bring down the risk of road accidents, driving functions of vehicles are increasingly being automated. Approximately 90 % of all accidents are attributable to human error [2, p. 5]. Automated driving functions can lead to more synchronization with traffic. This enhances the road safety. Pischinger and Isermann published studies on driver assistance systems confirming the safety benefits of automated driving. In addition, introduced functions can help improve the energy efficiency of vehicles. [3, pp. 966]

Europe's largest automotive association Allgemeiner Deutscher Automobil Club e.V. (ADAC) cites electrical faults as the major cause for vehicle breakdowns at 52 % [6, p. 2]. Automated driving functions take control of steering, braking and acceleration. In the case of hard- and software errors, the power supply system must stay operational. This allows a reliable supply of safety-critical components or their redundancy. Exemplary safety-critical components include Electronic Control Units (ECUs), the communication network, actuators for steering and braking and their power supply [2, pp. 10]. Functional safety requires additional components such as electronic switches or more sophisticated power system architectures with redundant supplies [6, p. 11].

To ensure the supply of all safety-critical functions, system testing is crucial but associated with great efforts. The traditional power system development is supported by virtual development methods. Simulation models are used to verify hard- and software requirements. Additionally, virtual design aims to shorten the time required for physical testing [7]. Various modeling methods for vehicular power systems have been established. However, the focus is limited to dynamic effects below 10 kHz or Electromagnetic Interference (EMI) related issues above 150 kHz [8, p. 9]. High-frequency disturbances have been measured, but modeling of vehicular power systems for frequencies between 10 kHz and 150 kHz has not been sufficiently studied. Valid models for this frequency range are needed to demonstrate functional safety through virtual development.

The electrification and automation of vehicles leads to an apparent contradiction between the introduction of high power, high-frequency switching dynamic systems (e.g. DC/DC converters) and susceptible electronics such as sensors and computing units. To achieve the required robustness against disturbances, stabilization measures were brought in [3, p. 966] [9, 10]. However, less attention has been paid to 10 kHz to 150 kHz, as well.

This research project addresses both the establishment of verified resource-saving dynamic simulation models and the disturbance suppression for frequencies up to 150 kHz.

1.2 Objectives and Challenges

This project aims to explore disturbances within vehicular power systems for frequencies up to 150 kHz utilizing virtual development methods. This section describes the imminent challenges and the approach indicated in this project.

The primary question concerns the effects to be simulated. System-inherent disturbances have been standardized. Disturbance immunity is required to ensure the fail-operational functionality of vehicular components, modules and their reliable power supply. However, it should also be discovered which effects are dominant and have a crucial impact on voltage stability. The architecture of future power systems decisively influences the selection of relevant disturbances. Thus, a reasonable and appropriate choice of the power system to be examined is particularly important.

From a modeling perspective, there are several difficulties. Firstly, the validity of existing models must be reviewed. A statement should be made about the types of disturbances that can be mapped with existing models. The model generation in the early vehicle development phase is challenging. Frequent modifications of both hard- and software, as well as the limited availability of information, need to be taken into account. Component manufacturers only release basic information or black-box models.

Another challenge is the computational effort for the calculation of interconnected models for frequencies up to 150 kHz. With the help of the established models, a future-oriented power system, relevant disturbances and stabilization approaches can be drafted. Available stabilization measures are to be compared and examined for their suitability.

Validation of simulation models of designed circuits proves difficult in the context of rapidly changing vehicle prototypes. These prototypes are developed to examine dissimilar aspects of the vehicle. Due to the constant short-term improvements, the electrical power system is modified throughout the system test phase. Reproducible measurements within prototype vehicles can only be carried out in a short time frame.

Fig. 1.1 illustrates the objectives of the research project. The visualization represents a simplified vehicular power system of a BEV consisting of a High Voltage (HV) and two Low Voltage (LV) subsystems. The power system includes both safety-critical components $\underline{Z}_{2a}$, $\underline{Z}_{3a}$ and non-safety-critical components $\underline{Z}_1$, $\underline{Z}_2$. The supply is provided for limited periods of time by a machine (G/M) within the HV system e.g. regenerative braking. Each subsystem includes its energy storage c. Associated components are classified with their Automotive Safety Integrity Level (ASIL). The presented power system is designed to be fail-operational by providing a redundant supply of safety-critical components with high integrity B(D). ASIL D can be achieved by decomposing individual B(D) subsystems. [11]

A dynamic load fluctuation as highlighted in red stresses surrounding components. The non-safety-critical component $\underline{Z}_2$ (QM) causes dynamic voltage changes at the terminals of the supply (DC/DC, c_2) and safety-critical components $\underline{Z}_{2a}$. Such dynamic stresses are caused, for example, by driving maneuvers or malfunctions like Short Circuits (S/Cs). Distributed electrolyte capacitors (contained in corresponding components) and the battery c_2 together supply the transient power demand. The characteristics of the transient (amplitude, temporal graph, etc.) and its potential impact on the reliable power supply depend on the electrical impedance of the wiring harness and attached devices.

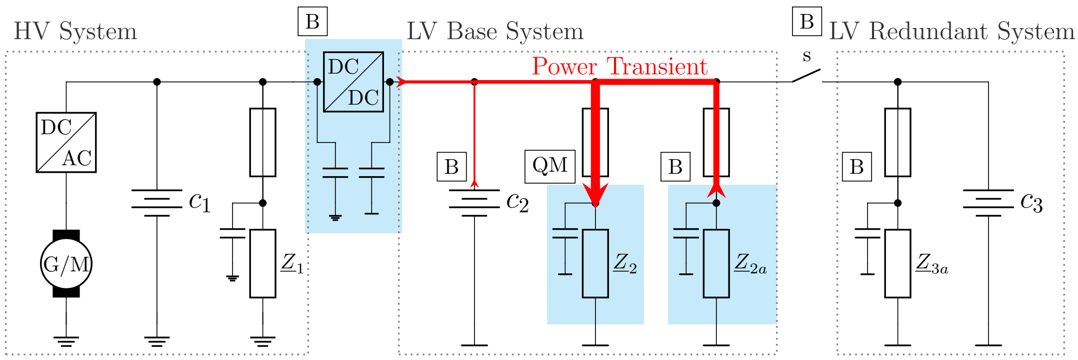


Figure 1.1: A power transient of a quality consumer (QM) burdens surrounding ASIL classified components within a fail-operational power system. The research project aims to create a modeling methodology for the study of comparable effects. [12]

This research project aims to validly simulate comparable processes as presented in Fig. 1.1. Moreover, stabilization measures are to be designed virtually in order to avoid possible malfunctions of safety-critical components. Power systems with a very small LV storage c_2 are of particular interest for this research project. Also, the omission of c_2 should be evaluable with the created methods.

1.3 Structure

To address the challenges above, this research project proposes novel simulation models, their test bench-based validation and an optimized parameterization of newly designed stabilization measures. Future power systems and relevant disturbances are identified based on the literature review. Research is carried out on the virtual power system development, available power system architectures and trends, available modeling methods, automotive disturbances and stabilization measures. Moreover, Chapter 2 identifies fundamentals for the established modeling methodology.

The modeling methodology is based on a reduced systematic approach. Only selected components are studied in detail. The modular modeling methodology of power system components is based on system identification, passive Resistor-Inductor-Capacitor (RLC) synthesis and the integration of a time-variant load. Computationally intensive models are simplified by a newly developed state-space average algorithm. The developed modeling methodology is presented in Chapter 3.

Obtained simulation results are validated by means of an established power system test bench. It contains a state-of-the-art power system architecture of a BEV with both safety-critical and non-safety-critical high power components. Chapter 4 introduces the requirements, the conceptual design as well as its physical implementation. A prototype of the voltage-scaled power supply has been implemented and is presented here. Furthermore, the capabilities of the test bench are contrasted. This includes the validation of simulation models and the analysis of stress tests.

Novel stabilization measures are introduced in Chapter 5. Transients (below 10 kHz) and subtransients (below 150 kHz) can be sufficiently suppressed by distributed non linearly controlled converters and system-designed adaptive band-pass filters. Stabilization measures are implemented and their effectiveness is validated.

The optimized design of the proposed stabilization measures for a specified power system is presented in Chapter 6. A calculation method for the evaluation of transient voltage stability is proposed. After defining the optimization problem, two approaches for calculating the objective function are described. An analytical state-space based and a numerical calculation are suggested. Beyond, the optimization results are implemented in the test bench. Simulation results and measurements are contrasted.

The results of this research project are briefly summarized in Chapter 7. Open research questions are discussed. A possible approach to these questions is suggested.

2 Fundamentals of Vehicular Power System Modeling

In this chapter, the process of vehicle development and its extension by virtual methods is presented. Power supply systems known from the literature are described in terms of their structure and available simulation models. For a better allocation of the modeling methods, the three abstraction levels steady-state, transient and subtransient are introduced. Electrical disturbances and possible countermeasures are contrasted. Finally, the necessary basics for the developed methods are presented. This includes an introduction to the modeling of passive structures by system identification and synthesis. Furthermore, control methods for DC/DC converters are explained.

2.1 Virtual Power System Development

Automobiles are developed according to the V-development scheme. The process model is suitable for developing mechatronic systems according to VDI/VDE 2206 [13]. This includes the integration of mechanical, electrical and information technology systems.

The development process is divided into three parts. It begins with the system definition. Here the system is planned, concepts are developed and the designs of system, subsystem, modules and components are derived. The traditional V-development scheme is visualized in gray in Fig. 2.1. The left side represents the system definition. The closer the individual process step is to the timeline, the higher the level of detail. The specifications of hard- and software are implemented in the physical design, and the second half of the development process involves their integration and testing. The assembled system, consisting of components, modules and subsystems, forms a physical product. This product must be maintained or improved during its operation. [3, p. 1258]

The virtual design supports the development process according to [14]. Fig. 2.1 highlights the virtual design elements in blue. System specifications are reviewed and verified by simulations in the early design phase. Virtual product development is performed prior to physical design. Simulation models are created based on the requirements and specifications. The vehicle is tested virtually before it is put into practice. Consequences, such as the revision of individual physical designs, can already be determined virtually and transferred directly to the physical design. The goal of virtual development is to reduce testing and integration time. According to Bouscayrol [7, p. 6], time-to-market could be reduced by up to 30 % by virtual development.

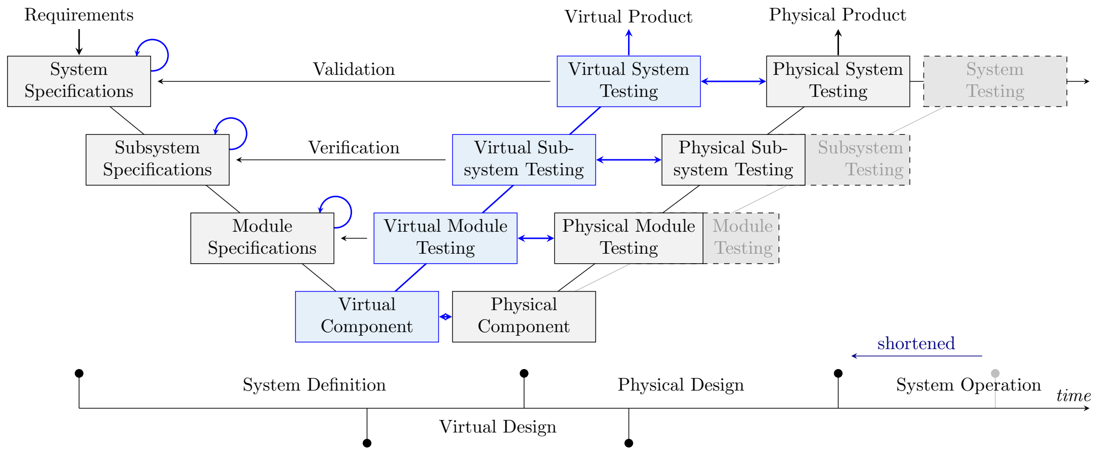


Figure 2.1: Virtual development methods support the V-shape development process and shorten the development process of the physical product based on [7, p. 5].

The use of valid simulation models is particularly important for virtual development. A library of simulation models is targeted by the Powerful Advanced N-Level Digital Architecture (PANDA) [7] project and the German Association of the Automotive Industry (VDA) [15]. In particular, open-access models should be used for interconnecting models in the development process of Battery Electric Vehicles (BEVs).

Implemented projects that use the principles of virtual development were recently published. Desreveaux performed a technical and economic analysis of the energy consumption of diesel-based Internal Combustion Engine Vehicle (ICE) vehicles and BEVs in [16, 17]. In addition, [4, 18] further describe approaches to improve and accelerate the development of virtual BEV simulation models.

2.2 Vehicular Power Systems

Vehicular power systems are facing exponential growth of technologies with high computing power, the need for reliable communication and dynamic power requirements. These requirements should be met by revised power system architectures, redundancy and innovative technologies. Section 2.2.1 introduces current state-of-the-art power system architectures as well as their components and long-term development trends. Subsequently, the abstraction levels steady-state, transient and subtransient are introduced in Section 2.2.2. Section 2.2.3 summarizes available modeling methods and reviews their suitability for the research project's objective of frequencies up to 150 kHz. In addition, power system disturbances are discussed in Section 2.2.4. Appropriate stabilization measures are presented in Section 2.2.5. The Low Voltage (LV) power system is discussed in more detail due to its importance in this research project.

2.2.1 Architecture and Components

Automotive power systems can be divided into five groups at the component level. The components belonging to the power generation supply the system or charge the energy storage. When the power generation is not active, the energy storage system supplies the loads with the necessary amount of energy. Different voltage levels are connected via converters. The grid distributes the energy to the corresponding electrical loads.

Power Generation

Conventional ICEs, Hybrid Electric Vehicles (HEVs) or BEVs contain a generator that can supply the power system. Typically, ICEs contain three-phase, inverter-driven claw-pole generators coupled to the internal combustion engine via a belt drive. In the absence of the High Voltage (HV) system, the generator is integrated into the LV power system. [9, p. 6] [19, p. 42]

HEVs include more powerful generators that can increase the efficiency of the internal combustion engine. For instance, start-up operations can be assisted by the generator's electric drive. BEVs embody only the traction engine (denoted as G/M in Fig. 2.2). Electricity is generated by regenerative braking. [20]

Energy Storage

The electrochemical storage ensures a stable and reliable power supply when no energy is being generated. In particular, the battery is discharged when the engine is off or the vehicle is parked. The idle power of the Electronic Control Units (ECUs) is provided and the battery ensures the engine's starting capability. In addition, the battery supports the needs of the power grid when power generation is low [9]. The storage is charged either by power generation or by external charging. Therefore, AC and DC charging systems are part of the HV system (referred to as Z_{ANC} in Fig. 2.2). [21]

HEVs and BEVs contain two independent batteries. The HV battery (HV Bat in Fig. 2.2) powers the HV system with the inverter-driven traction machine (G/M). The LV Battery (Bat) is used to power the logic of the HV/LV converter and the LV loads. [21]

Various battery cells have been discussed in the literature. Common batteries are based on lead-acid [9, p. 15], lithium-ion, or nickel-metal hydride (NiMH) [22, p. 13]. The integration of lead-acid and lithium-ion batteries into a common LV power system has been investigated in [23]. In addition, multiple batteries create redundancy, which is required for Advanced Driver Assistance Systems (ADAS) according to [24].

Double-Layer Capacitors (DLCs) provide less energy but more power [9, p. 9]. Stabilization measures use them in combination with power electronic circuits (see Section 2.2.5) [9, pp. 45].

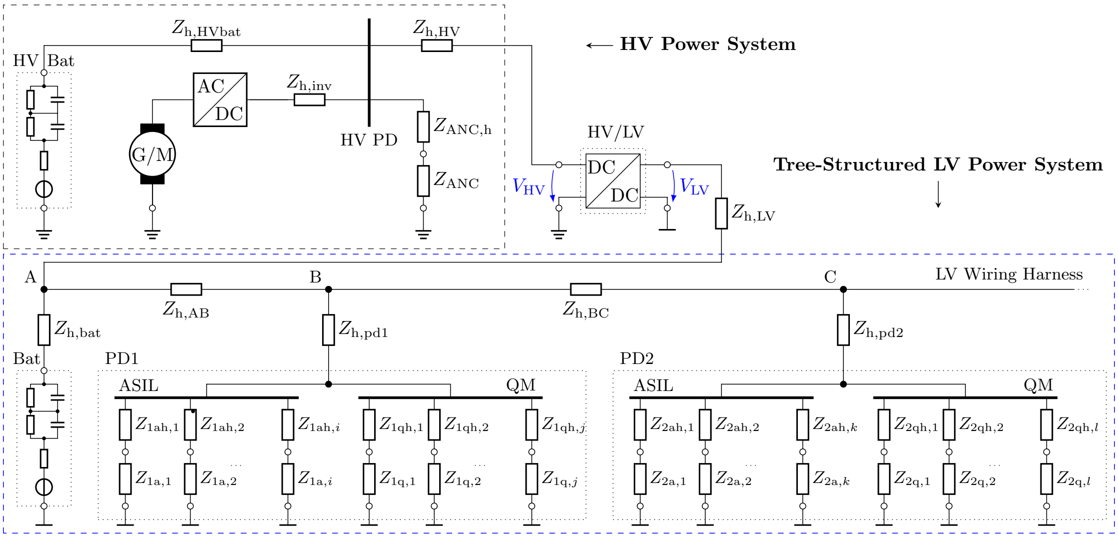


Figure 2.2: Simplified vehicular power system of a Battery Electric Vehicle (BEV). The power system includes energy storages, electric loads and components for the power generation, conversion and distribution.

Power Conversion

Since there are multiple voltage levels in the vehicular power system, energy-efficient power conversion is performed by DC/DC converters. Their task is, in particular, to carry out a stable DC voltage transformation for arising load scenarios [21]. This is to ensure the stability of the two interconnected subsystems. Furthermore, converters can couple additional energy storage devices for stabilization [9, pp. 46].

The requirement for redundancy to enable ADAS satisfies power conversion to the same extent as the supply [25]. This motivates the introduction of power systems with multiple converters [26–28].

The physical topology of DC/DC converters depends on the electrical requirements. For example, it is designed based on voltage, power, galvanic isolation, bidirectionality, and required power dynamics [9, p. 7]. If the power system exhibits particularly high power fluctuations, the converter must be adjusted accordingly. Therefore, fuzzy-controlled bidirectional DC/DC boost converter topologies are suitable, as proposed in [29].

Power Distribution

The generated and stored energy is distributed to the connected loads via the wiring harness. In addition to low-loss distribution, its task is to protect the cables from overload. Fuses also provide selective isolation from faults such as Short Circuits (S/Cs).

The wiring harness comprises more than 1000 cables, which together account for about 51 % of the weight of about 80 kg (extensively equipped sedan, including canals, grommets and housings) [30, p. 12]. Cable cross-sections range from $0.35\,\mathrm{mm}^2$ to $120\,\mathrm{mm}^2$ [31, p. 10]. The electrical ground is connected to the steel body of the vehicle. In contrast, lightweight vehicles contain carbon-fiber-reinforced plastic in the body. Separate ground cables are part of the wiring harness [9, p. 10].

The power distribution is supported by Power Distributors (PDs) with integrated fuses [9, p. 11]. More recent approaches replace melting fuses by electronic fuses. These switches are capable of meeting the increased safety objectives of ADAS as presented in [32–34]. In addition, electronic fuses can be reset and diagnosed. They show less dependence on ambient temperature and arcing, as shown in [35]. In addition, these fuses can be extended to include monitoring functions as proposed in [24].

The industry standard for automotive LV wiring harness is the topology of a tree structure as visualized in Fig. 2.2. In [27, 36] other possibilities of arranging the components in a rail or ring topology were presented. Current research in the area of ring-structured power systems implements selective separation of faults and powering of all unaffected subsystems to maintain fault-tolerant operation [28].

Electric Load

The HV power system includes auxiliary components such as AC compressors, heaters, and chargers [21]. These components are summarized in Z_{ANC} in Fig. 2.2. In contrast, the LV power system can include up to 200 loads connected to multiple PDs. The tree-structured LV system in Fig. 2.2 shows two exemplary PDs, each containing both Automotive Safety Integrity Level (ASIL) and Quality Management (QM) associated components. Safety-critical components such as Electric Power Steering (EPS), Headlights (HLi), Taillights (TLi), or the Windshield Wiper (WIP) are part of ASIL according to ISO 26262 [37]. QM components include heating, Audio Power Amplifiers (APAs), and entertainment systems. Other examples of LV electrical loads are indicated in [9, 20, 22] and categorized by their power consumption in [19, p. 38].

Fail-operational loads for automated driving functions require redundant communication buses, actuators and power supplies. Exemplary designs of such components are discussed in [38–42]. Appropriate designs are derived using a Fault Tree Analysis (FTA) and a mapping to an ASIL, as described in [11, pp. 59] [43, 44].

2.2.2 Introduction of Abstraction Levels

In order to adequately evaluate all effects of interest up to 150 kHz by means of virtual development, the creation of an extensive model library of previously named subsystems in Section 2.2.1 is inevitable. However, the degree of necessary modeling of each subsystem for a target frequency range can be assessed by means of a preliminary analysis.

Furthermore, connecting such subsystems of very different time constants or complicated nonlinearities leads to stiff Ordinary Differential Equation (ODE)-systems [45]. However, there is no clear definition for stiff systems. The stiffness is not only conditioned by the system equations but only in connection with the accuracy requirement and the time interval of a numerical solver. Especially, when high frequency events occur, the solver step size control is crucial for the performance of a numerical solver. [46]

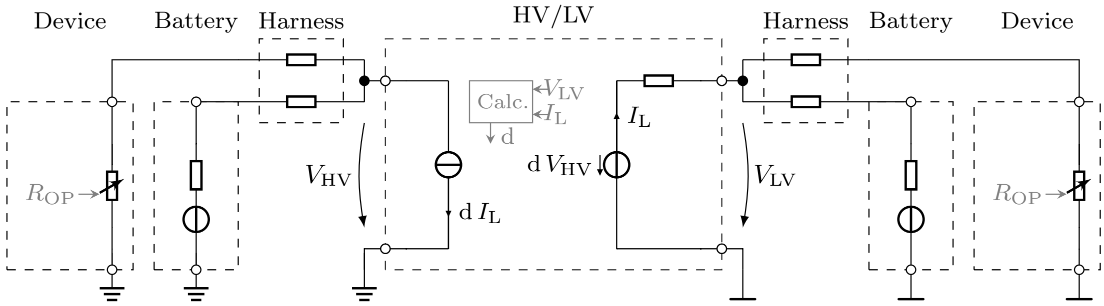
A continuous consideration of the entire dynamic range for all applications is very costly and is avoided with the help of the introduced degrees of abstraction. A similar approach was introduced in [47, pp. 10-13] as a design procedure for the controller of a DC/DC converter. However, the introduced abstraction levels do not take the details outside of the DC/DC converter into account. The levels differ in valid frequency range and their structure. In contrast to [47, p. 12], [48], transient events within the power system cannot be considered significantly slower compared to the DC/DC converter for the analysis of system-inherent switching events and faults. The following approach proposes different power system simulation models for certain simulation aspects and tasks.

Three levels of abstraction are defined: steady-state, transient, and subtransient. The naming was introduced by analogy to S/C transients in AC power systems according to [49, p. 252]. Therefore, a S/C current has a high amplitude with a strong damping within the first cycles after the fault. The transient current decays at a lower rate. In the steady-state phase, the current returns to normal.

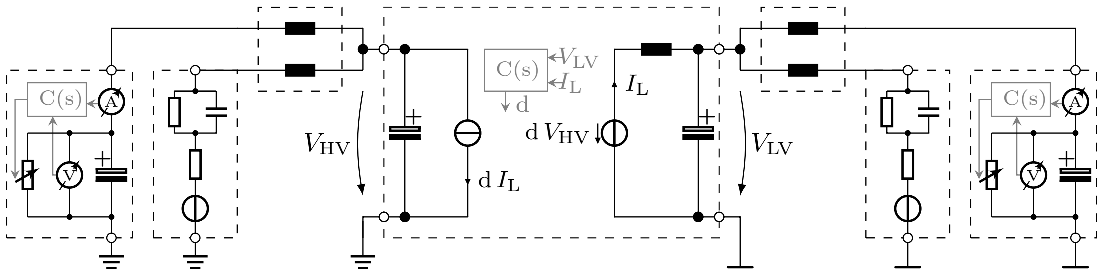
Fig. 2.3 visualizes the abstraction levels using two power systems (HV and LV) connected by a DC/DC converter. The level of detail of the power system simulation model increases while the DC/DC converter can be considered as an isolation between the two systems. The basis for the opposite abstraction is the frequency range of interest.

The steady-state simulation model of the power system is used for processes with a frequency of less than 100 Hz. The focus is on the system losses due to the distribution of the load current. The ohmic resistances of the devices, the battery and the DC/DC converter dominate this level of abstraction. The converter uses a duty cycle d without control dynamics. Steady-state simulation models are used for driving cycle analysis in terms of loss calculation. The advantage of these models is their simplicity and superior computational performance for the analysis of stationary power systems.

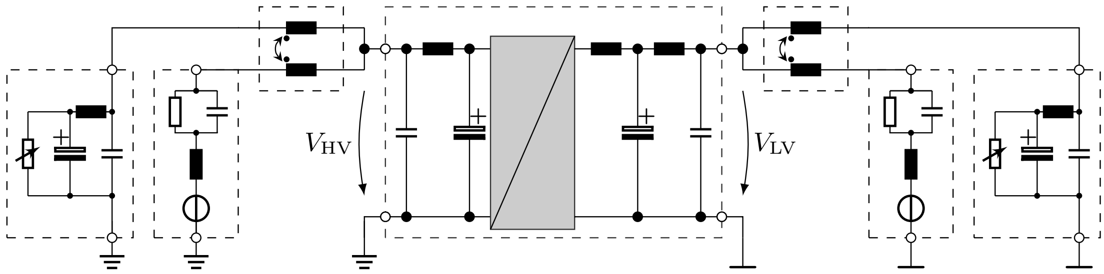
Transient simulation models are valid up to approximately 10 kHz. The focus lies on the oscillation of large system states such as bus capacitors. Their increased validity originates from the inclusion of control dynamics and Low-Frequency (LF) filter components such as electrolytic capacitors. The resistors introduced earlier must also be considered, but are left in the figure for simplification. The models of the connected devices include their control behavior $C(s)$ and their LF filters. The simulation model of the battery is extended to include one or more serial RC-stages. The wiring harness is dominated by the inductance. Transient simulation models are beneficial for the analysis of LF control stability and effects of power fluctuations on the terminal voltages of attached components.



(a) Steady-state abstraction level.



(b) Transient abstraction level.



(c) Subtransient abstraction level.

Figure 2.3: Exemplary visualization of abstractions levels from the perspective of the High Voltage (HV) and the Low Voltage (LV) power system: steady-state (a), transient (b) and subtransient (c).

Subtransient simulation models further include Electromagnetic Interference (EMI) filter components to validly represent effects up to 150 kHz. The focus lies on system-inherent effects due to switching actions within the power system. Passive electronics with their parasitics are dominant. The control dynamics of attached devices are neglected while the passive electronics are of interest. The simulation model of the battery includes its terminal inductance and higher-order RC-stages. The simulation model of the wiring harness also takes coupling effects into consideration. The DC/DC converter isolates subtransient effects within the two power systems and is therefore present through its passive input and output electronics. Subtransients are damped toward the interior of the converter. Subtransient simulation models are beneficial for analysis of stimulated resonant behavior and fault simulations such as S/Cs.

2.2.3 Model Description of Power System Components

In this section, simulation models available in the literature for the above subsystems are compared. These models are reviewed for their suitability for this research project. In addition, introduced levels of abstraction are assigned to the models.

Power Generation

Detailed subtransient models of generators can be found in [50, 51]. The equivalent circuit includes the machine as an excited synchronous machine with a three-phase bridge rectifier. Gradev developed Voltage-behind-Reactance (VBR) models in [52, 53].

Apart from the physical model as shown in [54, pp. 11], abstractions of the machine such as current sources were published. The modeled current source depends on the mechanical number of revolutions, the machine's physical structure, the environmental conditions and the mechanical load as presented in [8, pp. 21] and [30, p. 25]. There is a distinctive limitation of its control dynamics to avoid negative influences on the combustion engine dynamics due to the mechanical coupling of generator and engine [8, pp. 22]. These models belong to the transient abstraction level.

Energy Storage

Batteries are modeled as multiple series elements of capacitance and resistance in parallel. The number of RC stages depends on the required model accuracy. Both fourth-order [50, p. 32] and second-order models [55, pp. 26] have been implemented.

Moreover, an ohmic resistance, an inductance and a voltage source are included. The voltage source represents the Open Circuit Voltage (OCV) of the battery which primarily is determined by the battery's State-of-Charge (SoC) [56]. Impedance based modeling is applied to generate the equivalent circuit of battery cells according to [57, pp. 49]. Dynamic simulation models of Lead-Acid batteries were published in [P1]. DLC models can be found as a series connection of capacitance and its Equivalent Series Resistance (ESR) as shown in [58, pp. 40]. Depending on the level of detail of the model, it can belong to the steady-state, the transient or the subtransient abstraction level.

Power Conversion

Subtransient models of switched DC/DC converters require high computational resources due to their high frequency switching behavior. Models of the semiconductors are needed to perform calculations to evaluate the EMI characteristics [59].

The modeling of isolated buck-derived converter topologies such as Phase-Shifted Full-Bridge (PSFB) converters was explored in [60–64] and [65, pp. 11]. Further topologies with the ability of zero-voltage switching were modeled in [66].

To reduce the computation effort needed by subtransient switching models, transient average models were introduced. Not every single switching process is calculated, rather, an average value of the switching behavior is formed. The basis for average models is the Pulse Width Modulation (PWM) switch model [64, 67]. The procedure for deriving a small-signal model is presented in [63]. [68] compares the transient responses of a transient model with a subtransient model and reaches a deviation of less than 2 %. Improved state-space average models of DC/DC converters were established [69, pp. 17]. Smaller deviations can be achieved when using precise models for switches and diodes [70].

Power Distribution

The wiring harness of the vehicular power system for a validity up to 10 kHz is modeled by lumped-parameter models [71]. Electrically short lines and quasi-stationary conditions are assumed. The insignificant influence of capacitive parasitics below 10 kHz reduces the transient simulation model to a series circuit of temperature-dependent resistance (neglecting Skin-Effect) and inductance [8, pp. 37], [55, pp. 33].

The ground of the vehicle body can be calculated in a simplified way. In [8, pp. 47], an electrically conductive plate with constant thickness and constant material was proposed for the calculation of the resistances between the ground bolts of the vehicle body.

Melting fuse models are composed of ohmic resistances [8, p. 40]. The temperature dependency is calculated using a thermal equivalent circuit diagram as presented in [55, pp. 33]. Arcs between contacts of different potentials are modeled as a series combination of voltage source and resistance. Both depend on the electric current [55, pp. 68].

Electric Load

The literature suggests a categorization of loads into resistive, power constant and current constant. Resistive loads increase their current at elevated voltages, current constant loads draw a constant current independent of the voltage. Power constant loads increase their current at declining voltages. Electric loads are characterized as controlled resistances or current sinks [8, p. 24], [9, pp. 21], [72]. The abstraction of these reduced steady-state models is justified by current slew rates of less than 50 A/ms [50, p. 53].

For transient events within the power system, the component should be modeled with respective EMI/ LF filters and a controllable resistance [8, p. 25]. At least the bus capacitances of components should be modeled [55, p. 28]. Further, [19, pp. 72] showed an exemplary multi-domain simulation model of chassis control systems. Co-simulations combine the electrical, thermal and mechanical domains. The transient model of the EPS includes the electrical contacts, steering angle, the axle load, longitudinal and lateral dynamics.

Assessment of the Suitability for Subtransient Processes

This project aims at simulating disturbances with dominant frequencies below 150 kHz. In addition, S/C currents and dynamic power fluctuations with current slew rates above 1 A/µs are of interest. This long-term behavior is of secondary importance. The focus is on future-oriented BEV architectures and investigations within the LV power system with a reduced LV battery and electronic fuses. In addition, the computation effort should be as low as possible, with subtransient component models obtained by system identification.

As for the component model, the approach taken in the literature is to use recorded control signals. The dynamics of these signals depend on the location of the recording. For example, the current slew rate is limited by the connected harness inductance of the measurement setup. A transfer to another system should be verified carefully. The impedance of the connected components also affects the response of the system and the recorded signals. A current is fed by distributed capacitors and the supply. Recharging of the filter capacitors affects the terminal voltages of the corresponding components.

Consequently, the validity of the transient wiring harness and component models must be investigated. Furthermore, it should be investigated whether the HV power system has major dynamic influences on the LV system, since only the LV system is of interest. Therefore, a separate abstraction must be found for the HV system.

2.2.4 Vehicular Disturbances

In vehicular power systems, disturbances arise and can lead to malfunction, premature failure or destruction of the attached devices. To protect components from breakdown, test pulses and transients are standardized in ISO 7637 [73] and ISO 16759 [74]. CISPR 25 [75] shows the EMI corresponding limits and procedures from 150 kHz to 5.825 GHz. Automotive manufacturers specify test procedures for components. They must meet the immunity tests to qualify for the integration in the vehicle. Therefore, conducted immunity is a measure of an electronic component's ability to withstand a disturbance and operate as intended [76].

Tab. 2.1 compares exemplary power system disturbances and their causes being categorized by their occurrence in the frequency domain. Steady-state disturbances are characterized by a long duration. Such disturbances are caused by faulty software, incorrect operation or incorrectly designed energy balance (e.g. low battery capacity).

Transient disturbances are assigned to a frequency range up to 10 kHz. Oscillations are caused by e.g. rapidly changing loads or by starting ICE driven vehicles. Subtransient disturbances above 10 kHz arise from electrical faults or the stimulation of oscillation frequencies. Several faults cannot be assigned exclusively to one of the two groups. The causes of faults overlap in the group of (sub)transient faults. For example, very rapidly changing loads stimulate oscillation frequencies due to unstable control. [73]

Above 150 kHz, EMI disturbances occur due to insufficient physical design, resulting in emissions or high disturbance absorption. [75]

Numerous disturbances in motor vehicles were published in the literature. Test pulses similar to those in the ISO 7637 standard have been reproduced [77, 78]. The standardized load dump (test pulse 5) can result in excessive energy of more than 10 J, which stresses the protection electronics. Less energetic harness coupling transients lasting less than 320 µs [79, 80] occur more frequently. The most severe voltage change is achieved by switching inductive loads (such as the wiring harness or electrical machines) [76, 81, 82]. Radio interference, software and hardware lockups or resets were noted [76].

Table 2.1: Categorization of electrical disturbances in vehicle power systems according to the introduced abstraction levels. Subtransient disturbances are of particular interest for this work (highlighted in blue).

Group	Disturbance	Exemplary Causes
Steady-State < 10 Hz	longterm over-/ undervoltage	failure of supply control (e.g. alternator), assisted starting with 24 V system, weak power supply
	reverse polarity	faulty assisted starting
	quiescent current exceeded	ECU does not change to idle, certain components do not switch off in locked state of the vehicle
Transient < 10 kHz	over-/ undervoltage	control inertia of power supply at load dump
	voltage oscillations	dynamic load change, fluctuations, flickers
	power cycling	LF voltage fluctuations occurring during initial start of the vehicle's engine at low temperature
(Sub-)Transient 10 Hz to 150 kHz	over-/ undervoltage	load switching due to selective separation of an overload by means of a relay or electronic switch
	alternating voltage	unstable control, stimulating load oscillation
	ground offset	dynamic load change leads to different ground potentials of component with multiple supplies
	voltage interruption	loose contact or defective connection
Subtransient 10 kHz to 150 kHz	over-/ undervoltage	elevated current slew rate through recharging of bus capacitances, short circuits
	voltage spike	supply disconnection from inductive loads
	repetitive voltage spikes	switching of inductive-capacitive networks and stimulation of their oscillation frequency
	voltage oscillations	stimulation of system-inherent oscillation frequencies, unstable control, oscillations due to faulty bus capacitor of system attached device
EMI > 150 kHz	voltage oscillations	EMI emissions of system attached device due to insufficient passive filter, inappropriate vehicle shielding, EMI amplification due to system impedance, insufficient electromagnetic compatibility

Actions to suppress interference below 150 kHz from switching power electronics in AC power systems have been published. Malfunctions, acoustic disturbances, and increased power losses due to flicker have been observed. [83, pp. 153]

However, the standards do not explain all observed transients, as shown in [84]. S/Cs strongly depend on the inductance of the supply cable [85] and the architecture of the system [86]. The interconnection and arrangement of components affects the steady-state and the slew rate of the fault current. Short undervoltage pulses can cause communication errors and delay recovery beyond fault clearance [87].

The HV power system exhibits similar disturbances. Electrical transients at the beginning of BEVs charging has been investigated. Detected disturbances negatively affect communication between the vehicle and the charging station [88].

If the resilience to disturbances is exceeded, component failures could occur. Faults such as breakdown of rectifier diodes [89] or electrolytic capacitors [83, pp. 66] were noted. Architectural countermeasures include redundant design of converter phases. Lower fault probability was demonstrated in [90].

2.2.5 Voltage Stabilization Measures

If a component is not compatible with the transient or subtransient disturbances that occur, there is an increased risk of undesirable conditions. These negative effects include component malfunctions, failures, destructive effects on the power supply or neighboring components and additional losses. Therefore, destabilization of the power system should be prevented.

In the event of a failure of the immunity test, countermeasures can be applied. For example, the electronics can be adjusted and protective circuits such as reverse polarity protection or Transient Voltage Suppressor (TVS) diodes can be added. [91]

Another possibility is to revise the power system. Available stabilization measures can be sorted by their origin according to Fig. 2.4. Energy management stabilization measures make system level decisions influencing the steady-state behavior of affected components [22, 92, 93]. An energy management architecture is connected to the components via a communication interface with a certain transmission time of more than 10 ms. The energy management system requests to reduce the power consumption, reduce the load or carry out a priority-based shutdown [8, pp. 89], [10, pp. 28], [94, pp. 71]. Timing of power consumption can be coordinated by predictive power management [30], [10, pp. 39]. Further, the voltage (e.g. for the generator) can be lifted after the energy management detects an upcoming energy demand.

The module or component can make decisions independently of the higher-level energy management. In this transient level, the software of the individual electronic load makes its contribution. Autonomous load reduction and shutdown mechanisms have been proposed in [9, pp. 32] and [95]. The supply can be controlled to maintain system stability.

In [26, 27], multiple converters were proposed in a rail-based power system. Increasing the supply capacity by parallel converters within a component and controlling them was outlined in [96–98]. In this dissertation, a control method is proposed for distributed converters connected to different Access Points (APs) of the power system.

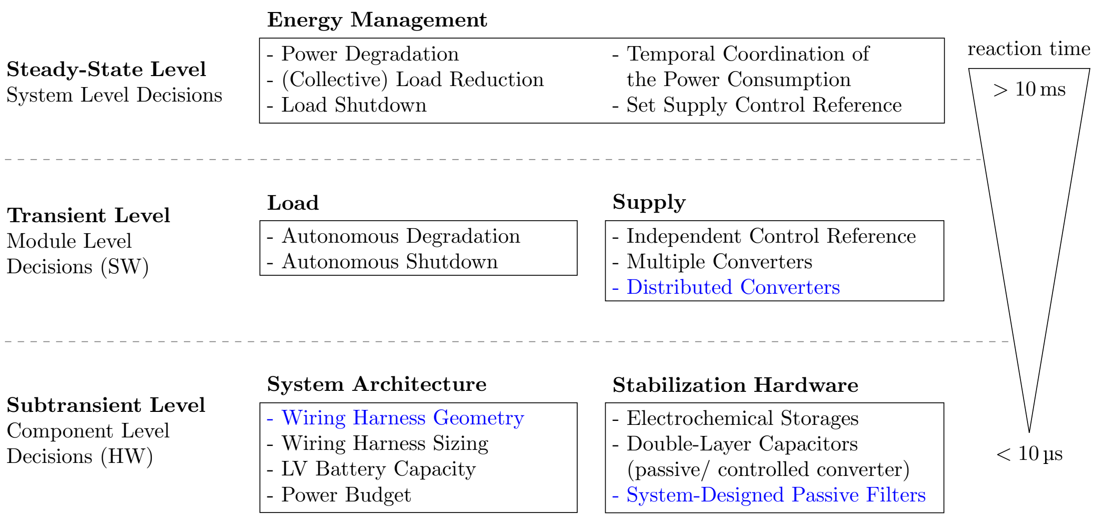


Figure 2.4: Overview of power system stabilization measures sorted according to their origin. Proposed stabilization measures of this project are highlighted in blue.

The subtransient level provides two different options for system stabilization. Rearranging components can be realized by developing the system architecture. The literature mentions the adaption of the wiring harness by adjusting cable lengths or cross sections. Increasing the battery capacity and the improvement of the power budget enable a more stable power system [8–10, 19, 30, 82, 94]. Sizing of the DC-Link capacitors was proposed as a suitable method for voltage stabilization in HV power systems [99].

The voltage stability can be increased by introducing an elevated voltage level. Certain high-power loads are then supplied by a 48 V power system. The voltage class has become accepted because it meets the standardized protection against accidental contact under 60 V according to ISO 6469 [100]. In addition, the lower current with the same output power significantly reduces the power loss and weight of the wiring harness [101, 102]. Moreover, the revision of the system geometry has a crucial impact on the system stability. Ring- and rail-structured power system architectures were proposed in [27, 36].

The integration of stabilization hardware represents another opportunity to stabilize the voltage within the power system. Adding a second battery storage was proposed in [23]. DLC based stabilization architectures were invented. A high degree of stabilization is possible with active or passive interconnection of DLCs [9, 30, 94, 103]. The choice of its AP was discussed in [8, p. 87]. Power systems with lithium-ion batteries and DLCs are realized by special customized DC/DC converters [104].

Major drawbacks of DLCs are its high tendency to self-discharge and its weight [29, pp. 10]. Therefore, a new system-oriented design methodology for passive filters is proposed in this dissertation. Passive filters for harmonic suppression were applied to HV AC transmission and distribution grids already. Typical topologies of these filters are the C-type, the shunt, and the bandpass filter [105–108] and [109, pp. 149]. Passive band-pass filters were applied to vehicular HV systems to suppress oscillations due to power electronic devices [110]. Passive and active EMI filters were sufficiently investigated in [111–114]. This contribution aims to create a decentralized approach to reduce disturbances within LV power systems.

The protection of components by electronics such as TVS diodes and reverse polarity protection are suggested in [80, 115]. Derived suppression circuits include shutdown relays as a fallback for defective TVS diodes [116]. If the transient cannot be adequately suppressed, the component must be designed to tolerate it [76].

This dissertation focuses on stabilization within the transient and subtransient level. The stabilization procedure is intended to achieve a fast response to a detected disturbance with low implementation effort, as shown in Fig. 2.4. The control of distributed power supplies can be implemented by software adaptations. Passive filters are of minimal weight and capacitance and can be inserted at predefined locations such as PDs.

2.3 Modeling of Passive Structures

The virtual development of vehicular power systems and the derivation of stabilization measures require high model quality. The impedance is important for ripple simulations, for example [117]. Large bandwidth simulations are time and memory intensive. Reduced-order models generate low-order approximations while providing the necessary accuracy [118]. Due to missing data or insufficient model accuracy, models must be built manually. Within the modeling methodology of this dissertation in Chapter 3, component models are obtained by system identification and synthesis methods.

2.3.1 Linear Time-Invariant System Identification

To generate passive equivalents of measured responses, system identification must be performed. In [119, 120] methods for the identification of dynamic systems are presented. The underlying methods are based on system responses. An analytical evaluation of e.g. step responses allows the parameterization of dynamic systems in the frequency domain. The publication [P2] applies the available methods to an automotive DC/DC converter.

These methods for simulating system responses are based on numerical convolution. Since numerical convolutions are computationally expensive, rational function approximations of frequency-domain responses are preferred. [121–123]

To obtain frequency-domain responses of a physical system, measurements are made using impedance analyzers such as Keysight Technologies E5061B. In [124], more information on impedance measurements in HV power systems is presented.

Gustavsen proposes a vector fitting procedure to compute rational approximations of frequency-dependent information. In vector fitting, an initial set of poles is iteratively relocated to better positions while solving a linear least-squares problem. Detailed information on this method is given in [121, 122]. Previous methods of vector fitting resulted in pronounced deviations for frequency-domain inputs with multiple resonances. Vector fitting overcomes this limitation by using complex starting poles. Publication [121] demonstrates the accuracy, robustness, and computational efficiency of the method.

To ensure passivity, poles and residuals are shifted by a quadratic programming problem [123]. This guarantees the generation of a positive real function. The methodology generates a transfer function $G(s)$ as shown in (2.1). The number of partial fractions n can be of any size depending on the target accuracy and complexity of underlying data. Residues c_k and poles a_k are real or complex conjugated pairs. Corresponding values of both numerator and denominator are calculated by vector fitting. Additionally, a gain d or inductive behavior h could exist. [125]

$$G(s) \approx \sum_{k=1}^{n} \frac{c_k}{s - a_k} + d + h \cdot s \tag{2.1}$$

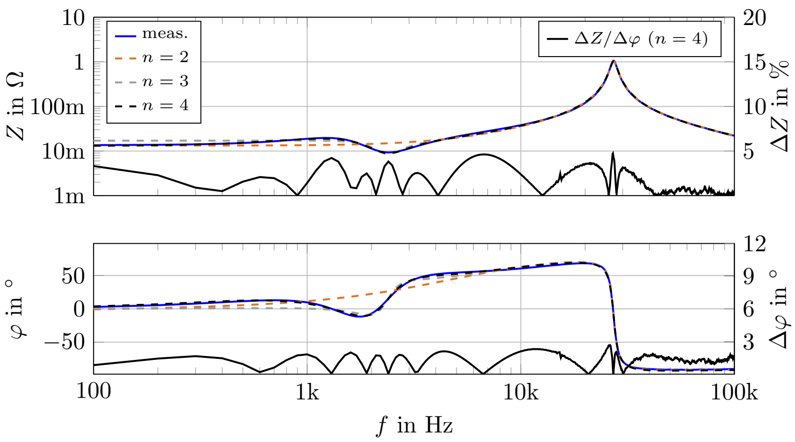


Figure 2.5: Approximation of an exemplary impedance using vector fitting. Approximating with order $n = 4$ leads to a sufficient accuracy with deviations ΔZ of less than 5 %.

Fig. 2.5 shows a measured impedance (highlighted in blue). The graph visualizes a pronounced anti-resonance of 1 Ω at approximately 30 kHz. Vector fitting leads to the dashed highlighted approximations. The measured original spectrum highlighted in blue in the frequency range 0.1 kHz to 100 kHz is contrasted to three approximations. A number of poles and residues of $n = 4$ sufficiently replicates the original with a maximum deviation of 5 % in amplitude and 3° in phase in the entire frequency range displayed. Stronger abstractions $n = 2$, $n = 3$ result in deviations of 61 % and 26 %, respectively. The transfer functions are simplified by neglecting poles and zeros above the frequency range of interest. Additionally, pole-residue terms with small c_n/a_n ratios are excluded since they do not contribute to the model behavior. [121]

2.3.2 RLC Network Synthesis

The resulting impedance spectra need to be transformed into passive Resistor-Inductor-Capacitor (RLC) networks by means of network synthesis. Numerous synthesis methods are available in the literature and are briefly introduced within this section.

Fundamental methodologies used for network synthesis follow the theorems by Helmholtz-Thévenin, Norton, Tellegen and Millman [126, pp. 160]. Depending on the number and type of elements forming the impedance, three synthesis methods can be distinguished:

- Two-Element Impedance (e.g. Foster and Cauer Networks)
- Three-Element Impedance with Transformers
- Three-Element Impedance

Two-Element Impedance

Wing evaluates the Foster and the Cauer methods in his survey of classical RLC synthesis methods [127, pp. 99]. Both methods result in parallel and series stages of inductance-resistance or capacitance-resistance. These methods find application in battery modeling [57, p. 71] or the generation of thermal equivalents [55, pp. 34], for example.

Three-Element Impedance with Transformers

Brune (1931), Darlington (1939), Youla and Tissi (1966) established RLC synthesis methods resulting in passive RLC networks with transformers. Brune defined the positive real function for his synthesis. Thereby, he showed that an impedance of passive networks must be positive real. Moreover, any positive-real function can be realized as an impedance of RLC with transformers. Unfavorably, negative inductors arise during the calculation. They are replaced by mutual inductances [128]. Darlington's synthesis generates lossless two-ports (consisting of RLC with transformers) [127, p. 164].

Three-Element Impedance

In [128], the method according to Bott and Duffin (1949) is described. Their synthesis does not need transformers. With the help of an auxiliary function following Richard's transformation, a pure RLC network with positive values is obtained. The fundamentals of the synthesis process and its extension are introduced in Chapter 3.

The minimality and the uniqueness of the Bott-Duffin procedure was presented in [128, 129]. The Bott-Duffin generated network is confirmed as the simplest possible result among series-parallel circuits. The produced circuits contain the least number possible of reactive elements and resistors for the description of a given frequency function. The prerequisite is the synthesis of a positive-real function. The synthesis procedure provides the proof of any positive-real function being able to be realized as a RLC circuit.

The RLC synthesis method according to Bott and Duffin was applied to automotive HV systems. The realization of artificial networks with all elements of positive values was confirmed in [125]. A recursive method is set up to piecewise extract single passive elements or combinations of inductance and capacitance. The remaining impedance is a positive real function. The calculated equivalent circuit can be extensive. Empirical deleting passive elements without significantly violating the impedance accuracy is proposed. Publication [P3] applies the Bott-Duffin synthesis on an automotive EPS.

2.4 Control of DC/DC Converters

The vehicular HV and LV power systems are interconnected by DC/DC converters. Since they are used as a means of stabilization in this dissertation, a brief introduction to their control is given in this section. The output voltage of the converter depends on the input voltage, the duty cycle and the load current. Beyond, the output voltage depends on converter circuit elements. Both input voltage and load current are subjected to fluctuations due to the SoC of the HV battery and loads within both systems. [130]

To maintain a constant voltage of the LV system, the duty cycle is controlled on the basis of the current and voltage. The controller is designed with focus on safety and stability. To increase the power or the reliability, converters can be set up in parallel stages or distributed units.

Linear Control

Several control topologies are available for linear control. Voltage Mode Control (VMC) controls the output voltage of the converter but does neither monitor nor limit the load current [130]. Current Mode Control (CMC) typically contains an inner current control and outer voltage control. This ensures reaching the voltage reference within given current limits and quickly saturate the current (amplitude, slew rate) for high load conditions [131–134]. The monitored current for current control is the filter inductor current with a pronounced ripple due to the switching behavior. Consequently, there is the possibility to control either the average or the peak current [135].

The control parameters are set according to different procedures. Reiter [47] proposes to iteratively adapt the parameters and calculate the step responses. The parametrization space is constrained by stability and robustness criteria. Moreover, Schröder describes two optimization methods for the control parametrization [136, pp. 46].

To reach good reference tracking, magnitude optimization is proposed. The magnitude of the closed-loop frequency response should be as ideal as possible over a wide frequency range. The controlled signal follows the target up to a certain frequency. This ensures a low overshoot in the event of step excitation and a short settling time. To reach good disturbance rejection, symmetrical optimization is suggested. This method is used for control paths with integral components (e.g. inner control loop of the cascaded CMC of converters). The control parameters for common plants are given in [136, p. 81].

The stability of linear controlled systems can be evaluated by the phase margin and Nyquist stability criteria. Due to parameter uncertainties caused by tolerances, temperature dependence and aging, a certain safety level must be guaranteed for control parametrization. The control loop gain contains a crossover frequency with unity gain. The phase margin to $-180°$ at this frequency should be more than $60°$ to ensure stability [136, p. 33]. When there are multiple crossover frequencies, the phase-margin stability criterion leads to ambiguous results. Then, the Nyquist criterion is employed. This criterion investigates the relative position of the critical point $(-1+j\,0)$ with respect to the frequency-dependent locus of the loop gain in the complex s plane [130].

Nonlinear Control

In addition to the linear control, nonlinear control strategies for DC/DC converters were examined. Feedback linearization was applied to balancing methods as found in [137]. In addition to feedback linearization, sliding mode control is used particularly for switching systems. Detailed information about nonlinear control methods and their application on switched power electronic devices is provided in [138, 139]. Especially, the robustness with respect to disturbances [140] and parameter variations [141] can be improved compared to traditional linear control methods.

Double-Integral Sliding Mode Control (DISMC) for PSFB converter applications was proposed in [142]. The improvement in both robustness and dynamic step response was validated. Further sliding mode control applications for bidirectional DC/DC converters are discussed in [143–148].

Stability analysis of nonlinear control is carried out according to Lyapunov-Krasavoskii stability theorems. In contrast, the tendency of a nonlinear control to become unstable is investigated by means of Chietaev and LaSalle Invariance instability theorems. [149]

Multiple Converters

Multiple converters can be parallelized to increase the output power and to generate a redundancy of the power supply. This reduces the power loss for high loads. In contrast, a parallel stage can also be switched off to reduce switching losses. In general, parallel converters are not directly tied to a specific type of control. Both linear and nonlinear control can be applied. Chen published the application of nonlinear DISMC on parallelized converter stages in [96], for instance.

For locally distributed converters supplying one common system, circulating currents between the individual converters need to be considered. Output voltages differ due to the impedance between the individual APs. Master-slave-based control topologies help to stabilize the current sharing between converters [150]. Moreover, a low-latency communication bus should be implemented to share information about the electrical states of converters [98]. As a control reference for the distributed converters either a similar load sharing is targeted [97] or a maximum efficiency tracking algorithm increases the overall efficiency of the power system [26, 27].

Available nonlinear control strategies have neither been applied on vehicular power systems nor adapted to its requirements. This contribution proposes a distributed DISMC strategy with consideration of vehicular low-voltage power systems.

3 System-Oriented Modeling to Simulate Fast Transients

As presented in Chapter 2, previous literature on modeling vehicular power systems focuses on a validity up to 10 kHz. This chapter introduces modeling methods to accurately calculate dynamic stress for frequencies up to 150 kHz. These models allow the calculation of transient and subtransient system-inherent disturbances as presented in Section 2.2.4.

This chapter introduces the modeling methods for system attached devices, the power supply by DC/DC converters and the wiring harness. First, the chapter explains the reduced modeling approach by analyzing the components for their system perturbations. Subsequently, a system identification and synthesis-based modeling approach for system attached devices is presented. The DC/DC converter model is based on a state-space algorithm. In addition, various abstractions of the wiring harness model are examined for their suitability. The results of this chapter are briefly summarized.

3.1 Analysis of Components for their System Perturbations

Devices attached to the power system have a similar structure from the system perspective. As visualized in Fig. 3.1, passive elements such as protection technology, Electromagnetic Interference (EMI) filter and Low-Frequency (LF) filter interconnect the internal actuator (right side, e.g. an inverter driven machine) with the power system (left side). The states of the passive filter electronics can load the power system (e.g. charging of capacitors) or support the system stability (e.g. discharging of capacitors). Moreover, the combination of electronic components with the low impedance power system can lead to resonances endangering the (sub-)transient power system stability.

The protection technology can be designed in various ways. Four frequently occurring circuits are visualized in Fig. 3.1. The circuits include overvoltage protection by Transient Voltage Suppressor (TVS) and Zener diodes, reverse current protection by horizontal Schottky barrier rectifiers and reverse polarity protection by vertical MOSFETs.

The attached EMI filter ensures a bidirectional interference suppression of disturbances above 150 kHz. Containing components are mostly metallized foil capacitors in the range of several µF, common mode and differential mode chokes.

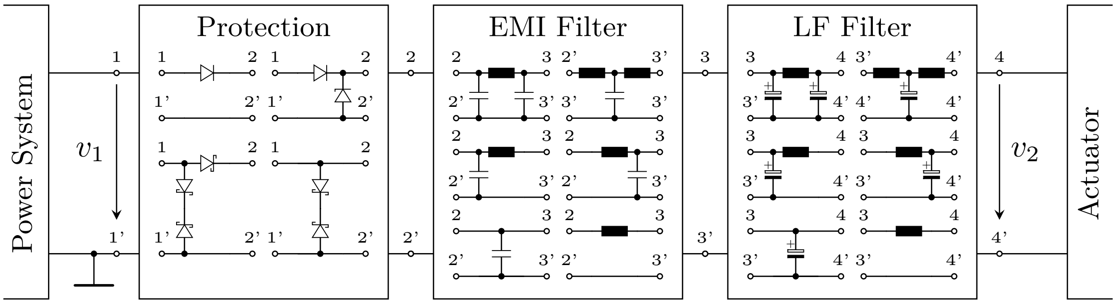


Figure 3.1: Generic block diagram showing the passive elements of automotive components.

There is a LF filter directly at the terminals of the actuator. This LF filter ensures a smoothing of the low-frequency power fluctuations. The input voltage of the actuator is stabilized and the current ripple is reduced. Mostly, larger electrolytic capacitors and filter inductances are installed as presented in [P4].

The dynamic characteristics of the components depend on the topology, the parameters of the elements and the load profile of the actuators. Thirteen exemplary components are investigated by simulation to identify components leading to high power system perturbations.

Each individual component is attached to an exemplary subsystem consisting of a battery Z_{Bat} and a cable Z_{L} with a length of 1 m as presented in Fig. 3.2. The behavior of the actuator is modeled as a current sink i_2 with a step to the maximum load of the individual component. This immediate power demand leads to voltage oscillations at the battery terminals v_{Bat} and a voltage drop due to the internal battery impedance Z_{Bat}.

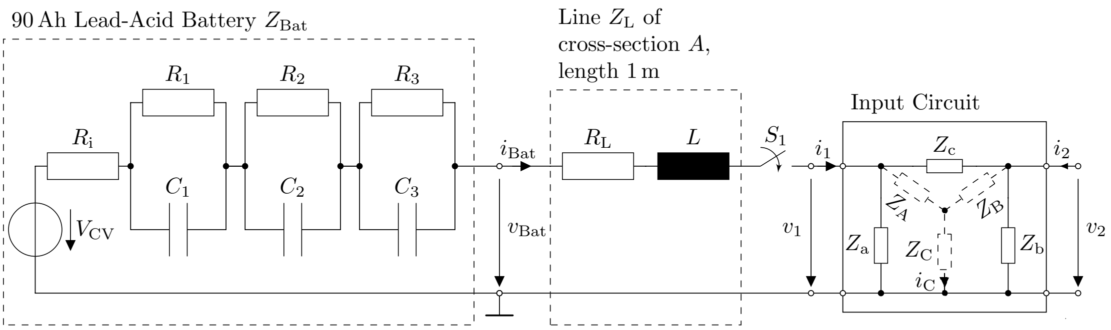


Figure 3.2: Exemplary circuit for the investigation of power system perturbations due to the individual load. The battery terminal voltage v_{Bat} is influenced by a load current i_2. The input circuit of the device dampens the impact on the power system.

The power supply is provided by a 90 Ah lead-acid battery. Its model consists of a voltage source V_{CV} =14 V, a resistance R_{i} =4.1 mΩ and three RC-stages (R_1 =6.9 mΩ, R_2 =61.6 mΩ, R_3 =70.6 mΩ, C_1 =29 F, C_2 =122 F, C_3 =2266 F). The battery model is based on [9, p. 15]. The wiring harness is modeled as an ohmic resistance R_{L} and an inductance L. The wire possesses a length of 1 m and the cross-section A. The wire resistance $R_\mathrm{L} = R_0$ is calculated by (3.31) and the inductance by means of (3.32) with h =50 mm. The inductance calculation is therefore based on [8, p. 35].

To perform the two-port-based analysis of input circuits, delta-star transformation is carried out. The equations (3.1) oppose the mathematical relationships for a delta-star transformation according to Fig. 3.2. The following applies here: $Z_{12} = Z_{21}$.

$$
\begin{aligned}
Z_{11} &= \frac{Z_\mathrm{a}\,(Z_\mathrm{b}+Z_\mathrm{c})}{Z_\mathrm{a}+Z_\mathrm{b}+Z_\mathrm{c}} & Z_{12} &= \frac{Z_\mathrm{a}\,Z_\mathrm{b}}{Z_\mathrm{a}+Z_\mathrm{b}+Z_\mathrm{c}} & Z_{22} &= \frac{Z_\mathrm{b}\,(Z_\mathrm{a}+Z_\mathrm{c})}{Z_\mathrm{a}+Z_\mathrm{b}+Z_\mathrm{c}} \\
Z_\mathrm{A} &= \frac{Z_\mathrm{a}\,Z_\mathrm{c}}{Z_\mathrm{a}+Z_\mathrm{b}+Z_\mathrm{c}} & Z_\mathrm{B} &= \frac{Z_\mathrm{b}\,Z_\mathrm{c}}{Z_\mathrm{a}+Z_\mathrm{b}+Z_\mathrm{c}} & Z_\mathrm{C} &= \frac{Z_\mathrm{a}\,Z_\mathrm{b}}{Z_\mathrm{a}+Z_\mathrm{b}+Z_\mathrm{c}} \\
&= Z_{11} - Z_{12} & &= Z_{22} - Z_{12} & &= Z_{12}
\end{aligned}
\tag{3.1}
$$

The minimal system consists of a voltage supply V_CV with source impedance $Z_\mathrm{Bat} + Z_\mathrm{L}$. This supply is connected to the terminals of a star two-port with impedance Z_A, Z_B, Z_C. The established system is described by the equation system (3.2).

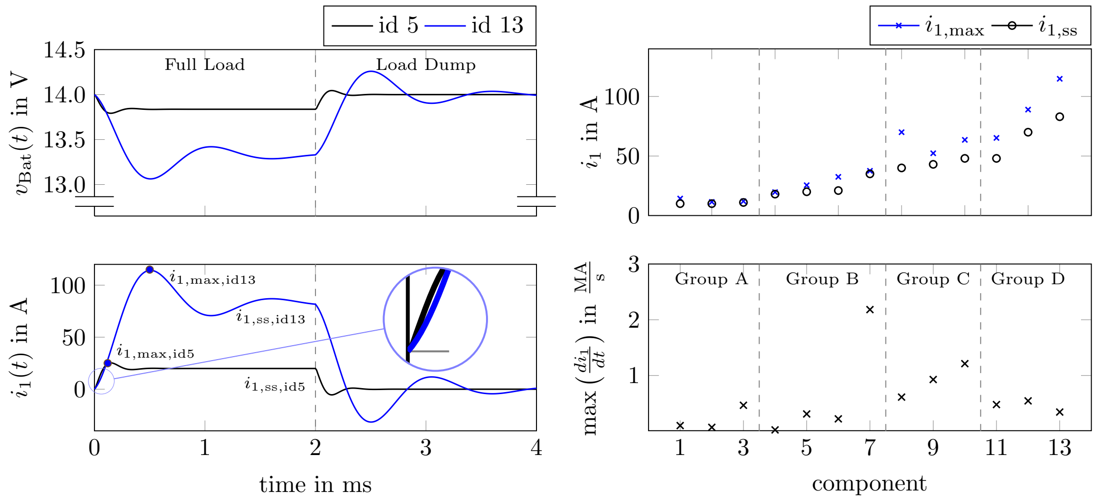
$$
\mathbf{0} = \begin{bmatrix} Z_\mathrm{Bat}+Z_\mathrm{L}+Z_\mathrm{A} & Z_\mathrm{C} \\ -1 & 1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_\mathrm{C} \end{bmatrix} + \begin{bmatrix} 0 & -1 \\ -1 & 0 \end{bmatrix} \begin{bmatrix} i_2 \\ V_\mathrm{CV} \end{bmatrix} \tag{3.2}
$$

Transfer functions between input current i_1 and load current i_2 are calculated using (3.3).

$$
\frac{i_1(s)}{i_2(s)} = \frac{Z_\mathrm{C}}{Z_\mathrm{A}+Z_\mathrm{C}+Z_\mathrm{Bat}+Z_\mathrm{L}} = \frac{Z_{12}}{Z_{11}+Z_\mathrm{Bat}+Z_\mathrm{L}} \tag{3.3}
$$

The simulation results are visualized in Fig. 3.3. Fig. 3.3a compares transient currents and battery voltages v_Bat during this load cycle. Two components (id 5 and id 13) are compared. Noticeably, the low power component id 5 has a slightly steeper current slew rate, but the strong oscillation damping leads to a shorter settling time. Fig. 3.3b contrasts the overshoot $i_{1,\mathrm{max}}$ and the steady-state current $i_{1,\mathrm{ss}}$ being caused by the load step at the actuator side of the two-port i_2.

Simulated load jumps influence the power system. To quantify the impacts, the voltage stability at the terminals of the battery is calculated. The voltage stability analysis is quantified according to [94, pp. 33]. The main parameter is the frequency of occurrence $f(V_\mathrm{k})$ of a certain voltage V_k. Voltage stability parameters are generated using a quantitative evaluation of voltages with respect to voltage limits V_min, V_N and V_max. The implemented parameters in this example: $\{V_\mathrm{min}, V_\mathrm{N}, V_\mathrm{max}\}$=$\{10, 14, 16\}$ V. The defined calculation of stability degree G_st and stability reserve R_st can be taken from (3.4).



(a) Time domain comparison of battery voltage and supply current during the actuator load jump.

(b) Maximum current overshoot, steady-state current and current slew rate.

Figure 3.3: Analysis of transfer characteristics $\frac{i_1}{i_2}$ for thirteen loads. A load jump and a load dump of the actuator load i_2 cause voltage oscillations v_{Bat} and current dynamics i_1 within the power system whereby adjacent components could be influenced.

$$
\begin{aligned}
G_{\mathrm{st}} &= \sum_{V_{\mathrm{k}}=V_{\min}}^{V_{\mathrm{N}}} f(V_{\mathrm{k}}) \left(1 - \frac{V_{\mathrm{N}} - V_{\mathrm{k}}}{V_{\mathrm{N}} - V_{\min}}\right) + \sum_{V_{\mathrm{k}}>V_{\mathrm{N}}}^{V_{\max}} f(V_{\mathrm{k}}) \left(1 - \frac{V_{\mathrm{k}} - V_{\mathrm{N}}}{V_{\max} - V_{\mathrm{N}}}\right) \\
R_{\mathrm{st}} &= \min \left[\underbrace{\left(1 - \frac{V_{\mathrm{N}} - \min(V_{\mathrm{k}})}{V_{\mathrm{N}} - V_{\min}}\right)}_{=R_-}, \underbrace{\left(1 - \frac{\max(V_{\mathrm{k}}) - V_{\mathrm{N}}}{V_{\max} - V_{\mathrm{N}}}\right)}_{R_+} \right]
\end{aligned}
\tag{3.4}
$$

Fig. 3.4 demonstrates the evaluation of the voltage v_{Bat} within the test routine (load jump, load dump as presented in Fig. 3.3a). The load cycle leads to a steady-state voltage drop being visible by the red median. Beyond, voltage oscillations can be detected based on extremes and whiskers. The quartiles provide information about the duration of the oscillation. The ratio of quartiles and extremes represents the damped decay and high over-/ undershoots. For instance, component 8 shows a short-time oscillation. The oscillation has a strong damping effect since quartiles disclose a smaller voltage range for 50 % of the time.

The second ordinate axis visualizes voltage stability degree G_{st} and stability reserve R_{st} being calculated according to [94, pp. 33] and (3.4). They quantify the relative frequency of voltages at the component terminals in comparison to an ideal stable voltage supply. The closer G_{st} to 1, the more stable the system is. The smaller R_{st}, the more the voltage approaches to the voltage limits during an investigated load cycle. Improving the system stability by improved electronic components is published in [I1, P5].

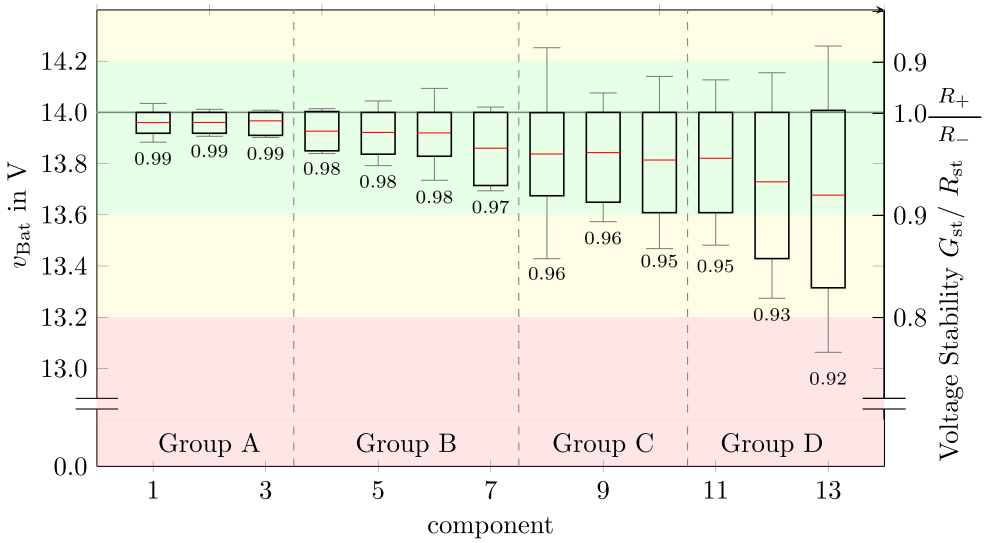


Figure 3.4: Boxplot visualizing the voltage stability and battery terminal voltage in an exemplary system during maximum load transients of thirteen components.

Four groups of components are derived from the results. Group A contains components being connected to the system via cable cross-sections 1 mm^2 to 2.5 mm^2. They stand out by a low power consumption (high median), a high degree of stability G_{st} and small oscillations. Corresponding components: driving stabilization Electronic Control Unit (ECU), interior power supply ECU, vehicle door ECU.

Group B summarizes components being connected with cross-sections in the range of 2.5 mm^2 to 4 mm^2. Corresponding components can demand elevated power such as the tailgate ECU, Windshield Wiper (WIP), vehicle roof ECU, media graphical unit. The oscillations possess elevated amplitudes.

Group C comprises components such as Central Control Unit (CCU) and Audio Power Amplifier (APA) being connected via 10 mm^2 cables. Larger load currents reduce the median values and oscillations possess elevated amplitudes but strong damping. The extreme values are distant from the quartiles, indicating a fast settling of the oscillation.

High power consumers stand out in Group D. Representatives are Electric Power Steering (EPS), Rear Axle Steering (RAS) and Electric Fan Drive (EFD). They are connected via 16 mm^2 to 35 mm^2 cables due to a high power demand. In addition to the small median value and stability degree G_{st}, voltage oscillations exhaust more stability reserve R_{st}. The area of the stability reserve marked in red is entered by group D, only.

Passive components have a decisive influence on the system-inherent voltage stability. Group D affiliated components contain high filter inductances and capacitances ensuring a noticeable decoupling from the system. Special emphasis is placed on Group C and D components for modeling due to their significant impact on the voltage stability.

The presented method shows an approach to estimate the dynamic influence of certain components. However, the actual voltage stability strongly depends on the actual power system impedance. Moreover, the analysis only identifies components with a high influence on the system stability. It does not take into account the opposite path. Safety-critical components from any group must also be considered to ensure their supply.

Weak system decoupling due to a very small power reserve in the passive filter would require more accurate modeling of the actuator. For the investigation of the subtransient, the modeling of the passive input circuits is pursued in more detail.

3.2 System-Identified Component Model

Since in vehicle development often only few information is available to characterize the components, their models are formed by means of system identification methods. First, the impedance of the component is measured. From this, additional relevant nonlinear effects can be extracted. Measured impedances are transformed into real passive transfer functions using vector fitting. The subsequent Resistor-Inductor-Capacitor (RLC)-synthesis of the transfer functions enables the integration of nonlinear models, the transient and steady-state behavior of the component. In this section, the modeling process is described and illustrated with an example.

3.2.1 Acquisition of the Impedance and Protection Technology

The subtransient part of the model contains the system identified RLC-circuit of the passive elements. As described in Section 2.3, Bott-Duffin synthesis is selected to generate the RLC-circuit on the basis of the measured impedance. The method, which originated in 1949, is still used today because of its proven minimality and uniqueness [128, 129].

Passive nonlinear components cannot be represented by pure RLC-circuits. In addition, automotive devices incorporate protection technology as presented in Fig. 3.1. Three different types are distinguished: The overvoltage protection (TVS or zener diodes), the feedback protection (horizontal barrier rectifiers) and the reverse polarity protection.

Mentioned nonlinear components within the input circuit need to be considered. Especially, the feedback protection prevents the connected capacitors from stabilizing the power system. Corresponding capacitors can only be discharged by the internal actuator. The overvoltage protection limits the voltage at the terminals of the device. The reverse polarity protection protects the actuator from critical negative voltage.

In contrast to the straightforward impedance measurement, the identification of nonlinear elements requires more effort. The measurement setup is extended by blocking capacitors C_{B}, a controllable external voltage supply v_{E} and a switch S as indicated in Fig. 3.5.

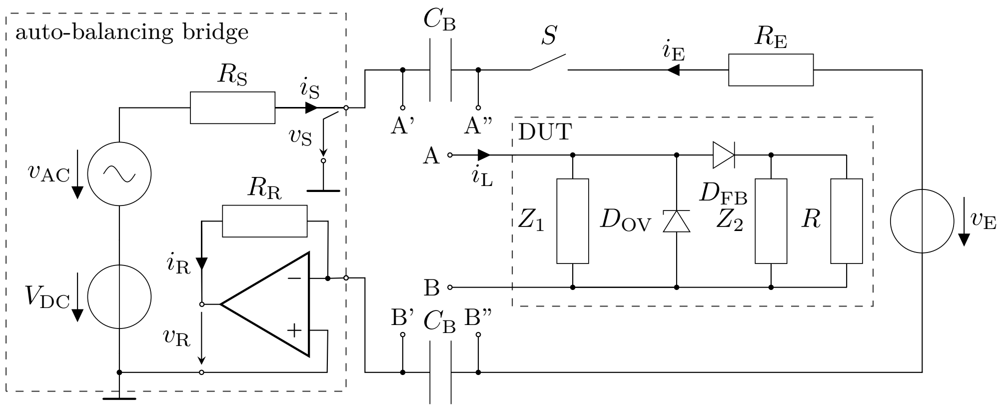


Figure 3.5: Impedance measurement and identification of nonlinear protection technology using an auto-balancing bridge. The nonlinear devices are identified by means of a controllable external supply v_E and blocking capacitors C_B. Alternatively, the bias voltage V_{DC} of the auto-balancing bridge is used.

The circuit in Fig. 3.5 illustrates the measurement method of an impedance measurement device in a simplified form. It typically contains an auto-balancing bridge for LF characterization. A test signal v_{AC} generates a source current i_S into the Device under Test (DUT) being the automotive component to be characterized.

The operational amplifier of the auto-balancing bridge generates the same current by R_R on the negative feedback loop i_R as i_S. The measured voltage v_R equals the product of current i_R and feedback resistor R_R. The measured impedance corresponds to $R_R \frac{v_S}{v_R}$ due to the equality of i_R and i_S. Further details on the technical implementation can be found in [151, pp. 31].

By the following measurement method the DUT is divided into two impedances Z_1, Z_2. The diodes D_{FB} (feedback protection) and D_{OV} (overvoltage protection) separate Z_1, Z_2 from each other. The resistance R emulates the internal actuator. By means of a DC bias voltage v_E or V_{DC}, these components can be characterized separately.

When measuring without an additional voltage supply, the amplitude of the measurement signal of v_{AC} must be smaller than the forward voltages V_f of D_{FB} and D_{OV}. Otherwise, these diodes would distort the detection of the impedances Z_1, Z_2. For example, D_{OV} clamps negative v_{AC} amplitudes above V_f or D_{FB} lets $v_{AC} > V_f$ pass.

To prevent the measurement from distortions, a DC voltage supply biases the nonlinear components. However, the internal DC voltage V_{DC} of the measurement device only drives high DUT resistances. The voltage drops across the source resistor R_S of typically $50\,\Omega$. For small DUT resistances R, a non-negligible bias current flows into R_R. This raises the DC potential of the virtual ground. Thus, the DC voltage V_{DC} cannot be applied for small R or measurement errors are recorded. The internal voltage does not supply typical automotive ECUs at their operating voltage of e.g. 12 V. [151, pp. 34].

The standard auto-balancing bridge integrated DC supply is therefore not suitable for all DUTs. However, with the help of an applied DC voltage, the individual components of the DUT can be distinguished. Multiple options could be used to supply the DUT:

- The internal supply V_{DC}: A high-impedance ECU with high resistance R ($R \gg R_{\mathrm{S}}$) can be supplied by V_{DC} of the auto-balancing bridge (connection of ports A,B to ports A',B').

- The external supply v_{E}: Supplying the DUT with v_{E} until the actuator R increases its resistance. This happens at the transition of the internal microcontrollers to the sleep-state. The actuator only consumes the quiescent current, which can be supplied by V_{DC} in some cases. First, ports A,B are connected to ports A",B" (DUT supplied by v_{E}) and switch S is opened once the component reduces its consumption. At the same time, ports A,B are connected to A',A" (DUT supplied by V_{DC}).

- Charging with the external supply v_{E}: Supplying the DUT with v_{E} (with ports A,B connected to A",B"). Open switch S and measure the impedance in a short limited time frame. The actuator is supplied by the capacitors within Z_1 and Z_2. This keeps a current flow through D_{FB}. Thus, the positive and negative amplitudes of the input current i_{S} are not disturbed by D_{FB} (as long as the discharging current of the capacitors does not fall below the amplitude of i_{S}).

- The internal reduced supply V_{DC}: Supplying the DUT with a smaller V_{DC} than its nominal voltage. Only when exceeding a certain minimum voltage, the actuator R will awake and draw a high current (connection of ports A,B to ports A', B').

The result of the DC biased measurement is the parallel impedance of Z_1, Z_2, R. Since Z_1 was identified without DC bias, Z_2 in parallel to R ($Z_2||R$) can be easily extracted. Both impedances Z_1 and $Z_2||R$ are system identified and RLC-synthesized separately. Then the circuits are set up and connected by a diode D_{FB}.

The existance of an overvoltage breakdown of D_{OV} can be identified by ramping up the voltage v_{E} (ports A,B connected to A",B"). The external supply v_{E} with a safe current limited is ramped up until the measured voltage at the terminals A,B is limited and a current i_{L} equal to the current limit of the external supply flows. The identified voltage is implemented as the breakdown voltage of D_{OV}. The same setup is used to identify a reverse polarity protection of the DUT. Therefore, the negative current limited external supply v_{E} is attached. Increasing the negative voltage will break down at the forward voltage V_{f} of D_{OV} if a reverse polarity protection is included. In contrast, identifying a high negative breakdown voltage confirms the existence of a bipolar TVS-diode. The measured voltage is implemented as the forward voltage V_{f} of the overvoltage protection device D_{OV}.

3.2.2 Rational Approximation of the Impedance

The vector fitting method proposed by Gustavsen and introduced in Section 2.3.1 is applied to characterize the time-invariant behavior of the DUT. The system identification method is applied to extracted subimpedances Z_1, Z_2 of Section 3.2.1. The resulting partial fractions as shown in (2.1) can be reformed to a transfer function (3.5) with a numerator polynomial of order n and a denominator polynomial of order m.

$$Z(s) \approx \frac{\sum_{k=0}^{n} a_k\, s^k}{\sum_{i=0}^{m} b_i\, s^i} \tag{3.5}$$

The calculation result must be a minimum-phase system to satisfy the necessary conditions for the RLC-synthesis. Both zeros and poles must not have a positive real part. Passivity enforcement is applied to the vector fitting result as described in [123]. Therefore, the extracted impedance and its inverse (admittance) are causal and stable. Positive real functions are minimum phase. Eq. (3.6) confirms that the impedance $Z(s)$ is minimum phase by means of the properties of positive real functions [126, pp. 759].

$$\begin{aligned} \mathfrak{Re}\{Z(s)\} > 0 \qquad & \text{if } \mathfrak{Re}\{s\} > 0 \\ \mathfrak{Im}\{Z(s)\} = 0 \qquad & \text{if } \mathfrak{Im}\{s\} = 0 \end{aligned} \tag{3.6}$$

3.2.3 Bott-Duffin based RLC-Network Synthesis

There are three reasons for applying the RLC-synthesis instead of directly implementing the system identification results in form of transfer functions:

- Load Actuator: The control (as part of the transient and steady-state behavior) contains nonlinear mechanisms. These include sudden commanded adjustments of reference values, control saturation thresholds, voltage-based degradation of the load profile or undervoltage-triggered turnoff. These events are part of the actuator but not the RLC-circuit. Therefore, an integration of the active load to the identified transfer function needs to be established. A static implementation of a transfer function model would not be effective.

- Physical Reproducibility: The RLC-synthesis should facilitate a prototypical rebuild of the automotive load on the basis of discrete passive components. A further analysis and a mapping of instability causing time constants (e.g. EMI or LF filter) should be permitted.

- Protection Technology and Fault Mechanisms: Protective nonlinear devices should be added and component fault models such as electrolytic capacitor failure mechanisms [152] should be integrated in the component model in further research. The simulative analysis of system-inherent failures aims to achieve the high integrity requirements towards the supply of safety-critical components.

An identified matched positive real transfer function such as an impedance $Z(s)$ is translated into a real passive RLC-network using the synthesis procedures described below. A distinction is made between single element extraction and Bott-Duffin impedance splitting synthesis. Both approaches are necessary for a comprehensive synthesis of an identified impedance.

Minimum Resistance Extraction

At the beginning of each synthesis, the minimum ohmic resistance R is extracted from the present impedance $Z_k(s)$. The leftover impedance of a synthesis is indicated as $Z_{k+1}(s)$. Before the next synthesis step, the value k is incremented. A local minimum of the real part of $Z(s) = Z_k(s)$ is identified with the two conditions given in (3.7). The derivative of the real part $\mathfrak{Re}\{Z(s)\}$ is zero for a frequency ω_0. Moreover, the second derivative is greater than zero at the same frequency. Since multiple solutions cannot be ruled out, a final check for global validity must be performed. The minimum resistance results as the minimum real part of $\underline{Z(s = j\,\omega)}$ at $\omega = \omega_0$.

$$
\begin{aligned}
&\text{Necessary condition:} \qquad \mathfrak{Re}\left\{\frac{\mathrm{d}}{\mathrm{d}\omega}\underline{Z(j\omega)}\right\} = 0 \qquad \text{for} \qquad \omega = \omega_0 \\
&\text{Sufficient condition:} \qquad \mathfrak{Re}\left\{\frac{\mathrm{d}^2}{\mathrm{d}\omega^2}\underline{Z(j\omega_0)}\right\} > 0
\end{aligned}
\tag{3.7}
$$

The frequency at which the minimum resistance occurs decisively influences the further procedure of the synthesis on the remaining impedance $Z_{k+1}(s)$. Tab. 3.1 and Fig. 3.6 provide an overview of other synthesis processes. Four different results are distinguished:

The most trivial case is the occurrence of a frequency-independent ohmic resistance. This means that the remaining impedance $Z_{k+1}(s)$ has an imaginary part only. Thus, a sole network of capacitors C and/or inductors L remains.

If the minimum resistance occurs in steady-state ($\omega_0 = 0$), the calculated real part of the impedance Z_k at ω_0 corresponds to the quotient of a_0 and b_0. The inverse of the resulting impedance $Z_{k+1}(s)$ corresponds to a marginally stable admittance. Due to the missing constant term in the numerator $a_0 = 0$, the extraction of a parallel inductor (Lp structure) is possible in the next step.

If the minimum resistance for $\omega_0 \to \infty$ occurs, it can be calculated from the quotient of a_n and b_m. Reducing the impedance $Z_k(s)$ by the resistance R reduces the degree of the numerator polynomial. Consequently, $Z_{k+1}(s)$ is a strictly-proper impedance. In the next synthesis step the extraction of a parallel capacitor (Cp structure) is performed.

If the minimum resistance occurs for a very specific frequency $0 < \omega_0 < \infty$, LC stages are extracted in the next step. Single series or parallel LC stages (LCs, LCp structures) are extracted for low-order impedances $Z_{k+1}(s)$ $(n, m < 6)$. Larger degrees are treated by Bott-Duffin synthesis resulting in the PS or SP structures.

Non-Biproper or Marginally Stable Immitance Functions

From the remaining impedance $Z_{k+1}(s)$ (after the minimum resistance extraction), single structures can be extracted under certain conditions [125]. Before, the value k is incremented. The next impedance to be examined is indicated as $Z_k(s)$.

A marginally stable impedance contains a series capacitor. The impedance $Z_k(s)$ has a pole at the origin. The denominator polynomial $\mathrm{Den}\{Z_k(s)\} = Q(s)$ does not include a constant term ($b_0 = 0$). The degree of denominator polynomial generally but not necessarily equals the degree of the numerator polynomial $\mathrm{Num}\{Z_k(s)\} = P(s)$ ($n = m$). The corresponding capacitor C and the leftover-impedance $Z_{k+1}(s)$ of this structure (Cs) are calculated by means of Tab. 3.1. This zero-gain admittance is shown in Fig. 3.6a. This Cs structure corresponds to an Open-Loop (O/L) for steady-state ($\omega = 0$) with leading current by 90°.

A strictly-proper impedance ($a_m = 0$) contains a parallel capacitor. The degree of the denominator polynomial $Q(s)$ is larger than the degree of the numerator polynomial $P(s)$ ($n = m - 1$). Therefore, the impedance has one more pole than zeros. The corresponding capacitor C and the leftover-impedance $Z_{k+1}(s)$ of this structure (Cp) are calculated by means of Tab. 3.1. The structure is visualized in Fig. 3.6b. This Cp structure corresponds to an Short Circuit (S/C) for $\omega \to \infty$.

An improper impedance ($b_n = 0$) contains a series inductor. The degree of denominator polynomial $Q(s)$ is smaller than the degree of the numerator polynomial $P(s)$ ($n = m + 1$). Therefore, the impedance has one more zero than poles. The calculation of the corresponding inductor L and the leftover-impedance $Z_{k+1}(s)$ of this structure (Ls) is stated in Tab. 3.1. The structure is presented in Fig. 3.6c. This Ls structure corresponds to an O/L for $\omega \to \infty$ with lagging current by 90°.

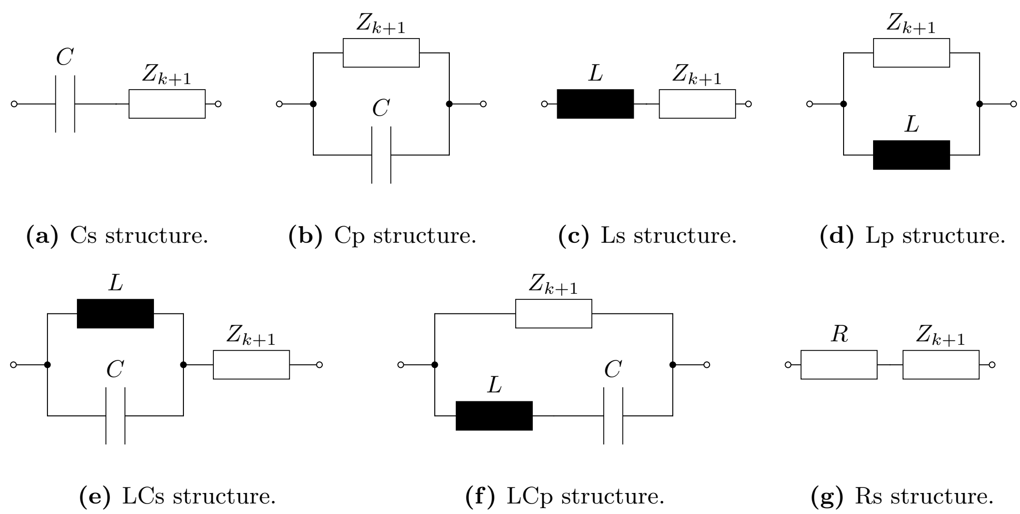


Figure 3.6: Equivalent circuit diagrams of single element extraction results.

Table 3.1: The extraction of RLC elements and LC stages is carried out by means of seven synthesis procedures. The table contrasts both conditions and synthesis calculation for the individual RLC-structures [125].

Structure	Conditions	Synthesis
Series Resistor (Rs)	$\min\{\underline{Z(s=j\omega)}\} > 0$	$R = \min\{\frac{a_0}{b_0}, \frac{a_n}{b_m}, \mathfrak{Re}\{\underline{Z(j\omega_0)}\}\}$ $Z_{k+1}(s) = Z_k(s) - R$
Series Capacitor (Cs)	$b_0 = 0 \qquad n = m$ (gen.)	$C = \frac{b_1}{a_0} \qquad Z_{k+1}(s) = \frac{P(s) - 1/sC\, Q(s)}{Q(s)}$
Parallel Capacitor (Cp)	$a_m = 0 \qquad n = m - 1$	$C = \frac{b_m}{a_n} \qquad Z_{k+1}(s) = \frac{P(s)}{Q(s) - s\, C\, P(s)}$
Series Inductor (Ls)	$b_n = 0 \qquad n = m + 1$	$L = \frac{a_n}{b_m} \qquad Z_{k+1}(s) = \frac{P(s) - s\, L\, Q(s)}{Q(s)}$
Parallel Inductor (Lp)	$a_0 = 0 \qquad n = m$ (gen.)	$L = \frac{a_1}{b_0} \qquad Z_{k+1}(s) = \frac{P(s)}{Q(s) - 1/sL\, P(s)}$
Series LC stage (LCs)	$\mathrm{PFD}\{Z_k(s)\} \exists \left[\underline{r_{\mathrm{a,b}}}, \underline{p_{\mathrm{a,b}}}\right]$: - $\left[\underline{r_{\mathrm{a}}}, \underline{p_{\mathrm{a}}}\right] = \left[\overline{\underline{r_{\mathrm{b}}}}, \overline{\underline{p_{\mathrm{b}}}}\right]$ - $\mathfrak{Im}\{\underline{r_{\mathrm{a,b}}}\} = \mathbf{0}$ - $\mathfrak{Re}\{\underline{p_{\mathrm{a,b}}}\} = \mathbf{0}$ - $a, b \in \{1, ..., m\} \wedge a \neq b$	$\mathrm{PFD}\{Z_k(s)\} \rightarrow \sum_{i=1}^{m} \frac{\underline{r_i}}{s - \underline{p_i}}$ $C = \frac{1}{2 r_{\mathrm{a}}} \qquad Z_{k+1}(s) = \sum_{\substack{i=1 \\ i \neq a,b}}^{m} \frac{\underline{r_i}}{s - \underline{p_i}}$ $L = \frac{1}{C\, \lvert\underline{p_{\mathrm{a}}}\rvert^2}$
Parallel LC stage (LCp)	$\mathrm{PFD}\{Y_{\mathrm{k}}(s)\} \exists \left[\underline{r_{\mathrm{a,b}}}, \underline{p_{\mathrm{a,b}}}\right]$: - $\left[\underline{r_{\mathrm{a}}}, \underline{p_{\mathrm{a}}}\right] = \left[\overline{\underline{r_{\mathrm{b}}}}, \overline{\underline{p_{\mathrm{b}}}}\right]$ - $\mathfrak{Im}\{\underline{r_{\mathrm{a,b}}}\} = \mathbf{0}$ - $\mathfrak{Re}\{\underline{p_{\mathrm{a,b}}}\} = \mathbf{0}$ - $a, b \in \{1, ..., n\} \wedge a \neq b$	$\mathrm{PFD}\{Y_k(s)\} \rightarrow \sum_{i=1}^{n} \frac{\underline{r_i}}{s - \underline{p_i}}$ $L = \frac{1}{2 r_{\mathrm{a}}} \qquad Z_{k+1}(s) = \frac{1}{\sum_{\substack{i=1 \\ i \neq a,b}}^{n} \frac{\underline{r_i}}{s - \underline{p_i}}}$ $C = \frac{1}{L\, \lvert\underline{p_{\mathrm{a}}}\rvert^2}$

A marginally stable admittance $Y_k(s) = 1/Z_k(s)$ contains a parallel inductor. The impedance $Z_k(s)$ has a zero at the origin. The numerator polynomial $P(s)$ does not include a constant term ($a_0 = 0$). The degree of denominator polynomial $Q(s)$ generally but not necessarily equals the degree of the numerator polynomial $P(s)$ ($n = m$). The synthesis calculation of the inductor L and $Z_{k+1}(s)$ of this structure (Lp) is recorded in Tab. 3.1. This zero-gain impedance has a parallel inductor as presented in Fig. 3.6d. This Lp structure corresponds to an S/C for steady-state ($\omega = 0$).

Single LC Stage Extraction

Single LC stages in series or in parallel to the remaining impedance $Z_{k+1}(s)$ are extracted by means of Partial Fraction Decomposition (PFD) of the minimum-resistive impedance $Z_k(s)$. This method is preferably applied to impedances of reduced order ($n, m < 6$), since the same structures can be calculated within the Bott-Duffin synthesis.

A parallel LC stage in series to $Z_{k+1}(s)$ is determined in the presence of two partial fractions with residues $\underline{r}_{\mathrm{a}}$, $\underline{r}_{\mathrm{b}}$ and poles $\underline{p}_{\mathrm{a}}$, $\underline{p}_{\mathrm{b}}$. These must satisfy the conditions shown in Tab. 3.1 for this LCs structure to be synthesized. Residues are real values and equal, poles are imaginary and complex conjugated. The capacitance C is the inverse of the double residue $\underline{r}_{\mathrm{a}}$ and the inductance L is calculated based on C and $\underline{p}_{\mathrm{a}}$. Remaining partial fractions are added up to represent the remaining impedance $Z_{k+1}(s)$. The LCs structure is visualized in Fig. 3.6e.

A series LC stage in parallel to $Z_{k+1}(s)$ is found based on the PFD of the admittance $Y_k(s)$. Two partial fractions with residues $\underline{r}_{\mathrm{a}}$, $\underline{r}_{\mathrm{b}}$ and poles $\underline{p}_{\mathrm{a}}$, $\underline{p}_{\mathrm{b}}$ must satisfy the conditions shown in Tab. 3.1 for this LCp structure to be synthesized. Residues are real values and equal, poles are imaginary and complex conjugated. The inductance L is the inverse of the double residue $\underline{r}_{\mathrm{a}}$ and the capacitance C is calculated based on L and $\underline{p}_{\mathrm{a}}$. Remaining partial fractions are added up and inverted to represent the remaining impedance $Z_{\mathrm{k}+1}(s)$. The LCp structure is illustrated in Fig. 3.6f.

A series inductive-capacitive combination in series to the impedance $Z_{k+1}(s)$ was excluded since the extraction of the single series capacitors or inductors with Cs and Ls structures is possible. A parallel inductive-capacitive combination in parallel to $Z_{k+1}(s)$ was excluded since the synthesis is feasible analogous to the Cp and Lp structure.

Bott-Duffin Synthesis

For impedances $Z_k(s)$ (with $m, n > 6$) and no applicability of the previously mentioned methods, Bott-Duffin synthesis is applied. The Bott-Duffin is selected due to its proven minimality and uniqueness. The synthesis generates the simplest possible result among series-parallel circuits [128, 129]. The prerequisite is the occurrence of a minimum resistance R at a certain frequency ω_0 with $0 < \omega_0 < \infty$.

The Bott-Duffin synthesis uses the auxiliary function $R(s)$ (3.8). $R(s)$ is positive real for any positive real $Z(s)$ with positive real constant k according to Richards Theorem being presented in [127, p. 122] and applied in [P3].

$$R(s) = \frac{k\,Z(s) - s\,Z(k)}{k\,Z(k) - s\,Z(s)} \tag{3.8}$$

The impedance $Z(s)$ is reformulated by means of $R(s)$ as shown in (3.9). Inductance L_0 with parallel impedance $Z_1(s)$ and C_0 with parallel impedance $Z_2(s)$ are extracted.

$$\begin{aligned} Z(s) &= \frac{1}{\frac{R(s)}{Z(k)} + \frac{k}{Z(k)\,s}} + \frac{1}{\frac{1}{Z(k)\,R(s)} + \frac{s}{k\,Z(k)}} \\ &= \frac{1}{\frac{1}{Z_1(s)} + \frac{1}{L_0\,s}} + \frac{1}{\frac{1}{Z_2(s)} + C_0\,s} \end{aligned} \tag{3.9}$$

Therefore, k needs to be calculated. A distinction is made between two cases:

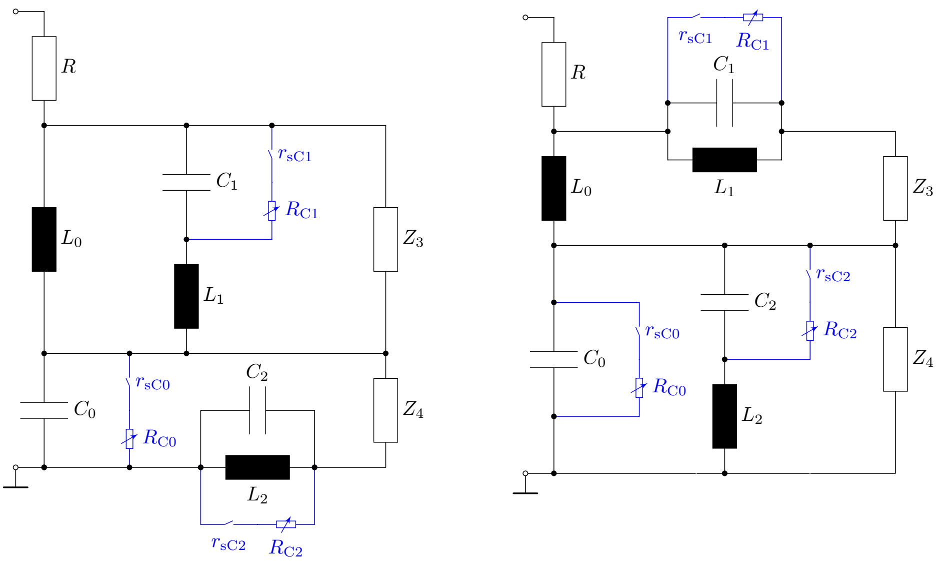
- $\mathrm{Im}\{\underline{Z(j\,\omega_0)}\} < 0$, then k is to be found from $\mathrm{Num}\{\underline{R(j\,\omega_0)}\} = 0$. Thus, zeros for $R(s)$ at $\pm j\,\omega_0$ are forced. This leads to structure Parallel-Series (PS) in the further synthesis as shown in Fig. 3.7a.
- $\mathrm{Im}\{\underline{Z(j\,\omega_0)}\} > 0$, then k is to be found from $\mathrm{Den}\{\underline{R(j\,\omega_0)}\} = 0$ forcing poles for $R(s)$ at $\pm j\,\omega_0$. This creates structure Series-Parallel (SP), see Fig. 3.7b.

Remaining impedances $Z_1(s)$ and $Z_2(s)$ for $\mathrm{Im}\{\underline{Z(j\,\omega_0)}\} > 0$ (corresponding to structure SP) are calculated according to (3.10). For structure PS the opposite arises: $Z_1(s)$ has a zero at $\pm j\,\omega_0$, $Z_2(s)$ has a pole at $\pm j\,\omega_0$. [P3]

$$Z_1(s) = \frac{2\,k_1}{s^2+\omega_0^2} + Z_3(s) \qquad \frac{1}{Z_2(s)} = \frac{2\,k_2}{s^2+\omega_0^2} + \frac{1}{Z_4(s)} \tag{3.10}$$

The coefficients k_1, k_2 are obtained by partial fraction decomposition of $Z_1(s)$, $Z_2(s)$. Both coefficients are residues of the partial fractions with poles at $\pm j\,\omega_0$. Adding up of remaining fractions yields $Z_3(s)$ and $Z_4(s)$. The parameters in (3.11) are derived for SP. Switching the values of C and L yields the parameters for structure PS.

$$L_1 = \frac{2\,k_1}{\omega_0^2},\; C_1 = \frac{1}{2\,k_1},\; L_2 = \frac{1}{2\,k_2},\; C_2 = \frac{2\,k_2}{\omega_0^2}. \tag{3.11}$$



(a) Parallel-Series (PS) structure.

(b) Series-Parallel (SP) structure.

Figure 3.7: Bott-Duffin synthesis network structures. The actuator is emulated by a selectable, controllable resistance r_{s}, R_{C}. The load resistance is in parallel with a capacitance to affect the LF part of the Frequency Dependent Network Equivalent (FDNE).

Reduction of the Synthesis Result

The accuracy of the measurement and the underlying identified impedance have a crucial influence on the result of the RLC-synthesis. Therefore, the RLC-synthesis yields very extensive structures in some cases. To reduce the computation time, certain elements can be erased without significant impact on the impedance [125]. They can be eliminated (O/L) or substituted by a S/C (red in Fig. 3.11a).

Substituting extracted elements by S/C or O/L follows the iterative elimination by comparison with an accuracy threshold value δ. An exemplary threshold δ of 1 % is empirically chosen. If a structure (parallel or series) of two impedances Z_1, Z_2 contains an impedance with a particularly small influence on the combination of both in the frequency range of interest ω, the insignificant part is substituted by S/C or O/L.

The following list contrasts the elimination of an negligible impedance. The comparison of two impedances Z_1, Z_2 over the stated frequency range provides an replacement instruction. In dependence of their electrical topology either S/C or O/L is chosen as their replacement.

Analysis of: $\frac{Z_2}{Z_1}(\omega)$ | **for** $\omega < 2\pi\,150\,\mathrm{kHz}$

max $\left\{\frac{Z_2}{Z_1}(\omega)\right\} < \delta$**:**

- series structure: $Z_2 \rightarrow$ S/C
- parallel structure: $Z_1 \rightarrow$ O/L

min $\left\{\frac{Z_2}{Z_1}(\omega\}\right) > 1/\delta$**:**

- series structure: $Z_1 \rightarrow$ S/C
- parallel structure: $Z_2 \rightarrow$ O/L

Typically, S/Cs are inserted for C >1 F, L <1 nH while O/L substitutions are carried out for C <1 nF, L >1 H when applying δ =1 % for ω below $2\pi\,150\,\mathrm{kHz}$.

3.2.4 Integration of the Transient and Steady-State Behavior

The sensitivity analyses in Section 3.2.5 and [P3] present an influence of the actuator in the LF range of the measured impedance only. Therefore, the high-impedance part at LF of the FDNE must be adjusted in order to map the behavior of the actuator.

Accordingly, both PS and SP structures include controllable resistances in parallel to each extracted capacitance as presented in Fig. 3.7. By vector $\mathbf{r}_\mathrm{s}$ a specific resistance is chosen to be electrically connected and controllable. The selected resistance emulates the actuator.

Fig. 3.8 shows the vertical structure of the entire component model being divided into steady-state, transient and subtransient behavior. The subtransient behavior is influenced by the RLC-circuit of the passive elements. Its parametrization and topology are found on the basis of system identification and network synthesis as presented in Sections 3.2.2 and 3.2.3. The modular FDNE includes controllable resistances as an interface to the transient behavior.

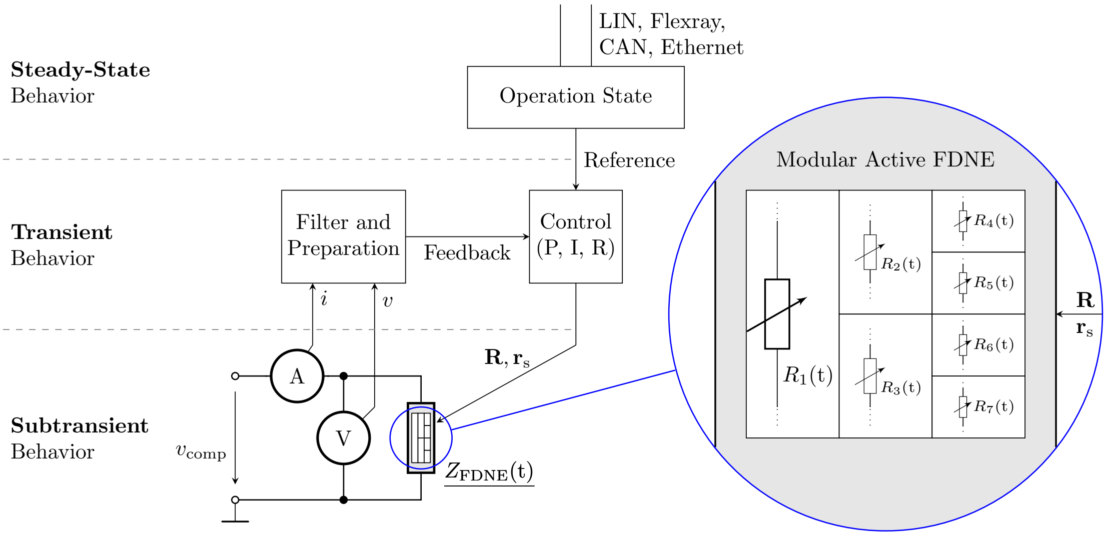


Figure 3.8: Generic block diagram showing the three abstraction levels of the identified component model. The passive circuit forms the subtransient behavior. Controllable resistors within the circuit model the transient behavior. The control reference is set by the steady-state behavior on the communication link.

The transient behavior ensures tracking of an operating point (power P, current I, resistance R) by controlling a selected resistance (with selection vector $\mathbf{r}_\mathrm{s}$) from vector $\mathbf{R}$ of the RLC-circuit. The transient behavior prepares and filters simulated current and voltage values for comparison with the communicated control target.

The steady-state behavior reflects the component link to the vehicular communication system. Setting the objective of an operating point (e.g. Headlights (HLi) in high beam mode) corresponds to an electrical reference value (e.g. power P). Translating the operating point to the electrical value is carried out in the form of a tabular mapping.

A piece-wise linear description is applied on the operating point: P_op for power constant, I_op for current constant or R_op for a resistive behavior. Turn-off thresholds are considered by V_min, V_max and the load degradation is integrated by V_deg as presented in (3.12). The control target is chosen in dependence of the measured voltage v_comp. The component switches its actuator off below the minimal voltage V_min and above V_max, operates in degraded mode between V_min and V_deg and operates regularly between V_deg and V_max. The degradation behavior is approximated with linear regressions with slew rates $m_{\{\mathrm{P,I,R}\}}$ and thresholds $n_{\{\mathrm{P,I,R}\}}$. $P_\mathrm{op}, I_\mathrm{op}, R_\mathrm{op}$ represent the power, current demand or ohmic resistance of the target operating point.

$$\{\mathrm{P,I,R}\}_\mathrm{ref} = \begin{cases} \{0, 0, \infty\} & \text{for } v_\mathrm{comp} < V_\mathrm{min} \vee \geq V_\mathrm{max} \\ m_{\{\mathrm{P,I,R}\}} \{P, I, R\}_\mathrm{op} + n_{\{\mathrm{P,I,R}\}} & \text{for } V_\mathrm{min} \leq v_\mathrm{comp} < V_\mathrm{deg} \\ \{P, I, R\}_\mathrm{op} & \text{for } V_\mathrm{deg} \leq v_\mathrm{comp} < V_\mathrm{max} \end{cases} \tag{3.12}$$

3.2.5 Exemplary Sensitivity Analysis and Modeling Result

Fig. 3.9 shows an identified model of an EPS consisting of EMI filter, LF filter and a field-oriented controlled Permanent Magnet Synchronous Machine (PMSM). The PMSM has been modeled as Voltage-behind-Reactance (VBR) which was proven to be a suitable model description for high dynamics according to [153, 154].

The EMI filter contains two metallized foil capacitors C_E and a common mode choke L_CMC. The LF filter includes a filter inductance L_F and an electrolyte capacitor C_F with the corresponding parasitics. As published in [P3], the EMI filter and LF filter dominate the high-frequency behavior of the EPS. The corresponding parameters are listed in Tab. 3.2.

The impedance of the EPS in Fig. 3.10a exhibits disturbances at multiples of the measurement pulse length $n{\cdot}6.66\,\mathrm{kHz}$ (highlighted in red) and multiples of the Pulse Width Modulation (PWM) switching frequency $n{\cdot}10\,\mathrm{kHz}$ (highlighted in black). Disturbances are reduced by injecting multiple pulses of different pulse widths. Switching frequency dependent disturbances are reduced by calculating a Simple Moving Average (SMA).

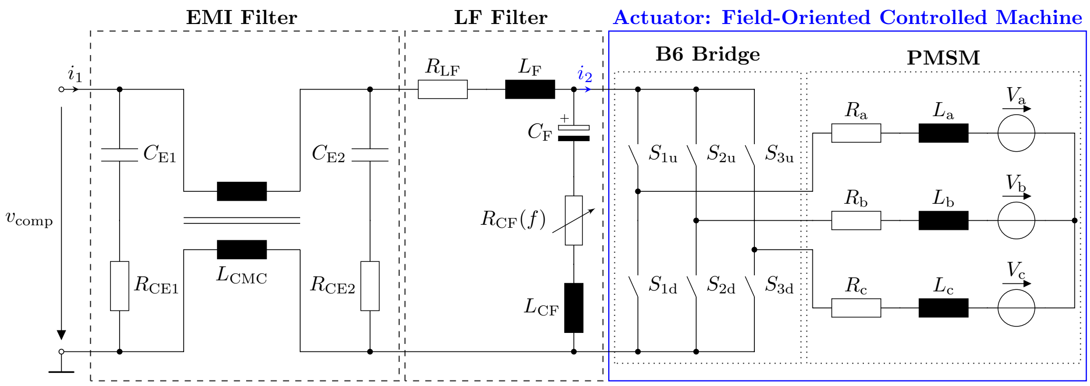
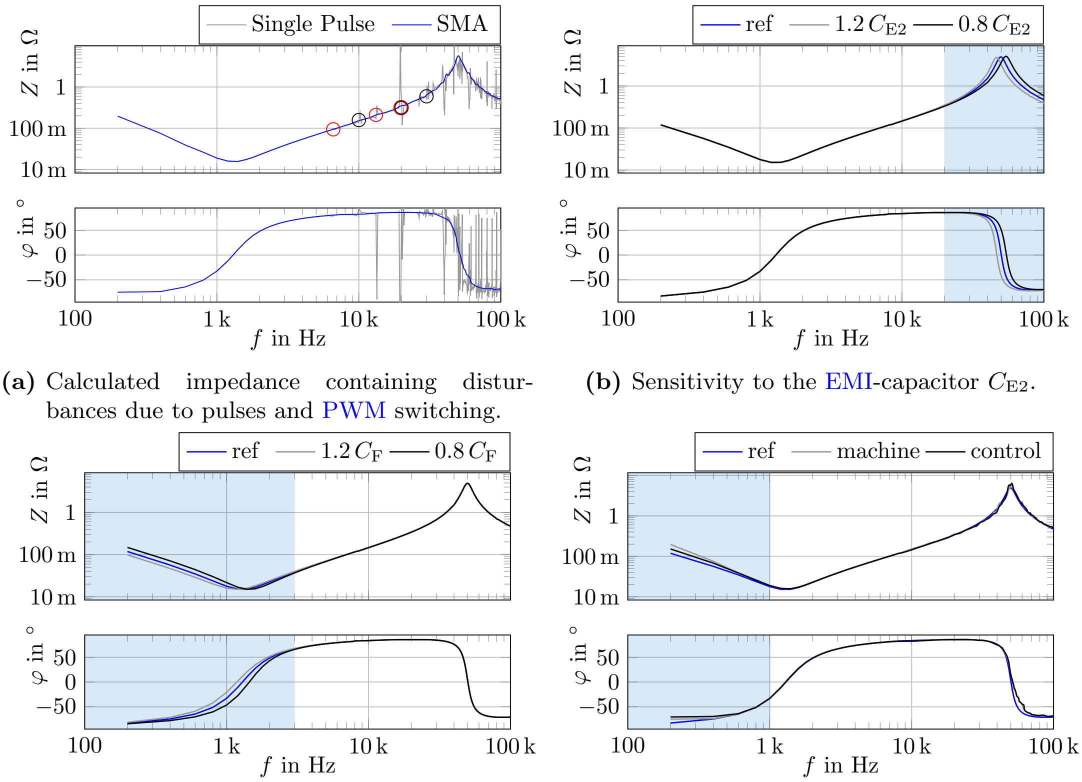


Figure 3.9: Identified model of the EPS consisting of EMI, LF filters and a field-oriented controlled PMSM.

Table 3.2: Identified electrical parameters describing the EPS of Fig. 3.9.

R in mΩ						
R_CE1	R_CE2	R_M	R_LF	R_CF	R_DS	R_abc
4.9	13.4	0.5	0.7	8.5	1	39

C in µF			L in µH				
C_E1	C_E2	C_F	L_CMC	L_F	L_CF	L_d	L_q
10	3.3	6600	4.7	2.3	0.02	97	105



(a) Calculated impedance containing disturbances due to pulses and PWM switching.

(b) Sensitivity to the EMI-capacitor C_{E2}.

(c) Sensitivity to the filter capacitor C_F.

(d) Passive input circuit in contrast to the entire model and different machines speed control.

Figure 3.10: The acquired impedance of the EPS depends on the actuator (machine, control) in LF. Above 10 kHz the impedance is dominated by the passive filter electronics and the switching frequency of the actuator.

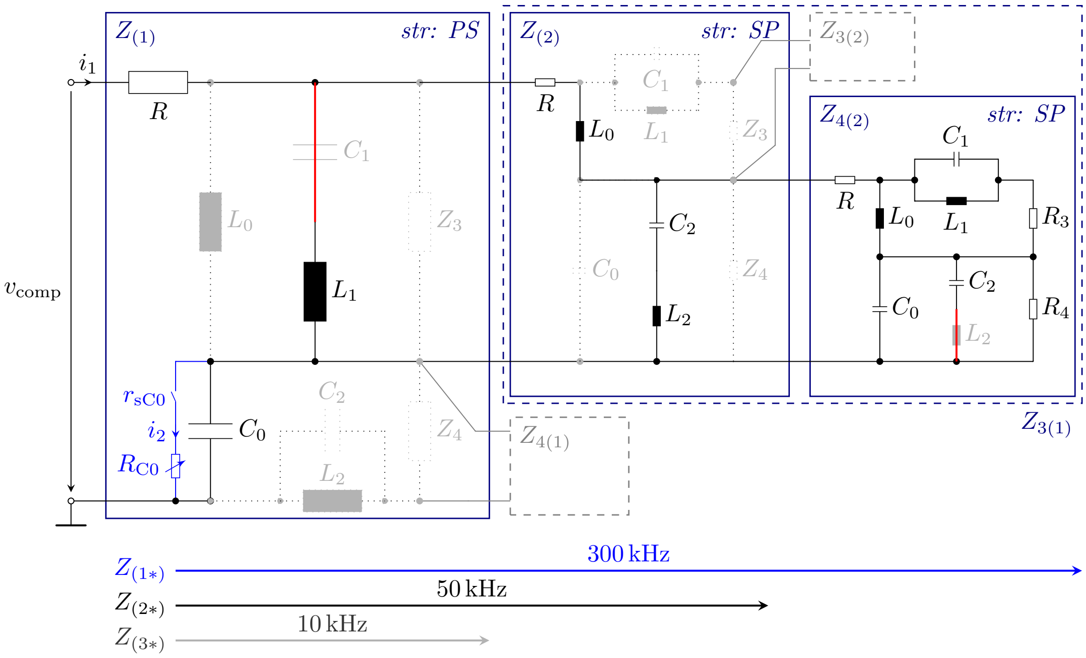
The impedance displays an anti-resonance at 50 kHz. Both its amplitude and frequency are dependent on the parametrization of the EMI-filter. Fig. 3.10b shows the sensitivity to the EMI-filter capacitor C_{E2}. The impedance above 20 kHz is modified.

The resonance at 1.5 kHz is dependent on the LC-filter parameters. Fig. 3.10c presents the influence of filter capacitor C_F on the impedance below 3 kHz.

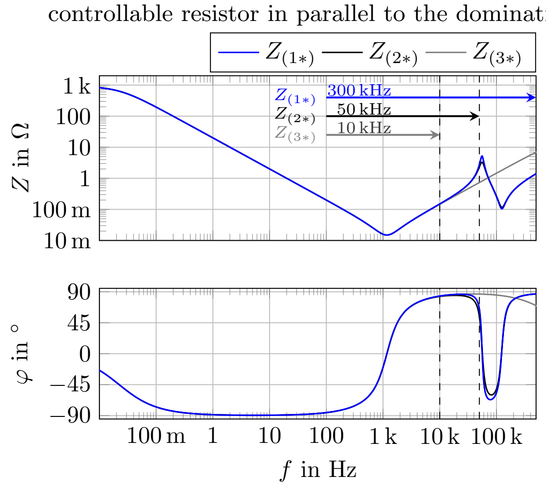
The operating point and switch positions within the B6-bridge mainly influence the impedance in the LF range. Fig. 3.10d contrasts the passive circuit to the model with the controlled machine. The operation of the machine determines the behavior below 1 kHz. The parametrization of the speed controller (as part of the is shown in the same figure. Its major influence is located below 500 Hz.

The presented sensitivity analysis showed an influence of the actuator on the LF part of the impedance. Therefore, a system identification and synthesis is carried out on the impedance of the EPS with opened switches within the B6 bridge (switched off actuator).

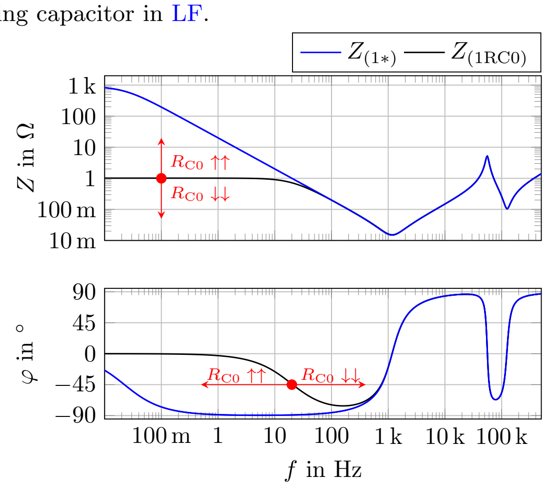
Applying the synthesis to the measured impedance of the EPS (amplitude and phase of the impedance are highlighted in blue in Fig. 3.10) results in a FDNE consisting of five structures as visualized in Fig. 3.11a. The synthesis with an accuracy of δ=1 % leads to substitutions with O/L (grey) and S/C (red).



(a) The modular active FDNE of an EPS consists of three reduced Bott-Duffin structures with one controllable resistor in parallel to the dominating capacitor in LF.



(b) Bode diagram of FDNE structures.



(c) Bode diagram of the impedance with the integrated controllable resistor.

Figure 3.11: Frequency domain analysis of partial FDNE structures and the EPS model. Depending on the accuracy required, different abstractions can be chosen.

Ultimately, the impedance can be reduced to a total of only three structures $Z_{(1)}$ (PS), $Z_{(2)}$ (SP) and $Z_{4(2)}$ (SP). The individual structures map a certain frequency range of the impedance. Fig. 3.11b shows the in Fig. 3.11a indicated differentiation in the frequency domain. The sole consideration of $Z_{(1)} = Z_{(3*)}$ is valid up to 10 kHz. Considering $Z_{(2*)}$ (combination of both $Z_{(1)}$, $Z_{(2)}$) is valid up to 50 kHz. The whole extracted FDNE is able to capture the impedance of the EPS up to 300 kHz.

In addition, Fig. 3.11c demonstrates the impact of the controllable resistance R_{C0} on the impedance in black. Only the LF part is adapted by the resistance as it was published in [P3] and is observed in Fig. 3.10d.

3.3 State-Space Average Algorithm

Subsystems of dissimilar voltage levels are interconnected via DC/DC converters. The Phase-Shifted Full-Bridge (PSFB) converter is one common topology for the vehicular power systems. PSFB converter models are described in [60–64].

Available average models do not accurately represent the dynamic behavior for negative load conditions. Short-time processes such as phase-shift errors need to be modeled to replicate the transient behavior [155]. This section introduces a resource-saving average model being able to represent major dead time and load-dependent effects.

The equivalent circuit diagram of the PSFB is shown in Fig. 3.12. The primary side full-bridge includes switches Q_i where $i \in \{1, 3, 2, 4\}$ with body-diodes and drain-source capacitors. The full-bridge is connected with a low inductive center-tapped planar transformer with the leakage inductance L_{k}. The primary side resistance R_{p} includes Printed Circuit Board (PCB) traces and a blocking capacitor resistance. The secondary rectifier includes switches Q_5, Q_6 and a LF filter. Inductance L_{f} exceeds L_{k} by an order of magnitude. Resistance R_{s} contains resistances of transformer, shunt and PCB traces. The model of C_{o} contains its parasitic resistance R_{C}.

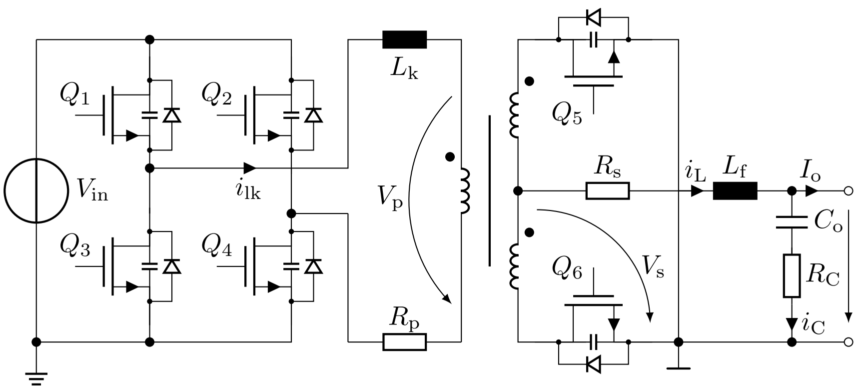
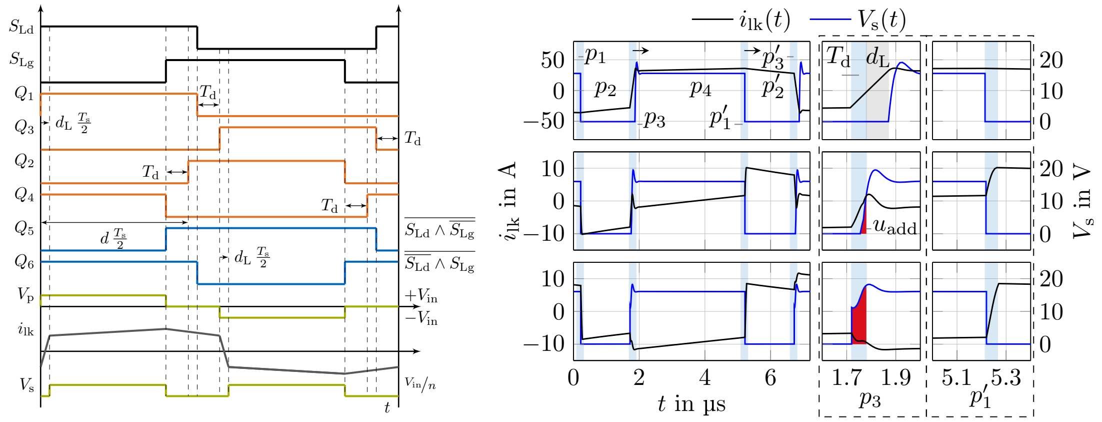


Figure 3.12: Equivalent circuit diagram of a PSFB converter.



(a) Switching scheme and exemplary buck operation.

(b) Operating the PSFB converter in different load conditions: buck operation (top), low load (middle), boost operation (bottom).

Figure 3.13: The working principle of the PSFB converter for different load conditions and the applied switching scheme.

Switching signals are derived from logical signals S_{Ld}, S_{Lg}. Leading lag switch signals Q_1, Q_3 differ from lagging lag switch signals Q_2, Q_4 by the phase shift d. Full-Bridge signals are delayed by a dead time T_{d} compared to logical signals S_{Ld}, S_{Lg}. Switching signals of the output rectifiers are based on logically linking S_{Ld}, S_{Lg} by a NAND logic as presented in Fig. 3.13a. In high load operation a duty cycle loss d_{L} becomes noticeable since output voltage V_{s} is delayed and the load voltage V_{o} is smaller. It arises due to the limited current slew rate by leakage inductance L_{k}.

Fig. 3.13b reveals a view on the working principle of the converter for different loads and magnifies the dead time behavior of both secondary voltage V_{s} and primary current i_{lk}. The upper figures show the buck operation. At Phase p_1 (transition from power delivery to freewheeling mode), the current i_{lk} reaches its absolute maximum. Subsequently, freewheeling mode takes place in Phase p_2. The load conditions show a different behavior in Phase p_3 (transition from freewheeling to power delivery mode). The output voltage V_{s} appears earlier reducing the duty cycle loss d_{L} or rather introducing a voltage gain (in red) in boost operation. The longer the dead time, the more significant the influence. [P6]

The developed state-space average algorithm proposes to analytically analyze this effect of the duty cycle loss shift. The algorithm is presented in Fig. 3.14. The idea is to predict the secondary voltage V_{s} by precalculating the leakage current i_{lk} in dependence of average values V_{in}, I_{o}, V_{o} and duty cycle d. Thus, the switching part is substituted by an algorithmic approach. First, the ripple current I_{r} is calculated. Subsequently, Phase 1 is computed. Since in Phase 1 different diodes could conduct, an algorithmic case distinction (highlighted in blue) must be made. Phase 2 is linearly approximated. Within Phase 3 and its diode conduction possibilities, the influence on system dynamics comes about. The algorithm returns voltage gain V_{add} or duty cycle loss d_{L}.

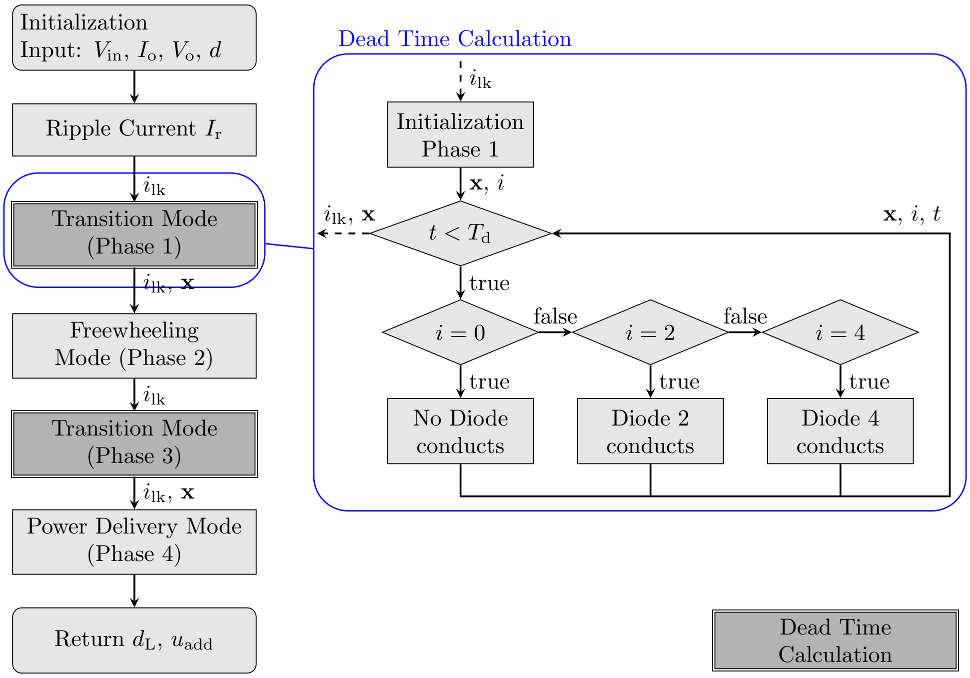


Figure 3.14: The state-space average algorithm for the calculation of converter dynamics. Each dead time calculation of Phase 1 and Phase 3 is carried out by a case distinction as highlighted in blue. Each diode conduction mode is computed on the basis of its individual state-space system.

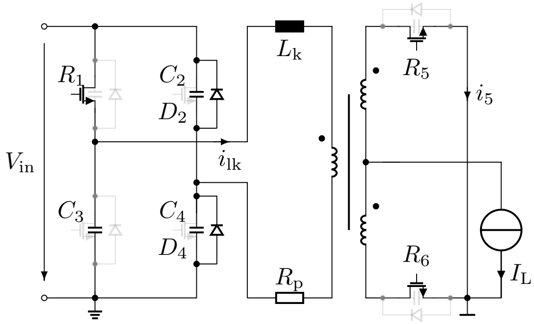
3.3.1 Initialization by Precalculation of the Ripple Current

Equation (3.13) visualizes the calculation of the ripple current I_r of the output filter current i_L. The equation depends on the average values and includes resistances $R_{prim} = 2\,R_{dsp} + R_p$ and $R_{sek} = R_{dss} + R_s$. Furthermore, the equation depends on duty cycle loss d_L. Including duty cycle loss into this equation leads to quadratic expressions. Neglecting d_L here will only lead to slight deviations later on. [P6]

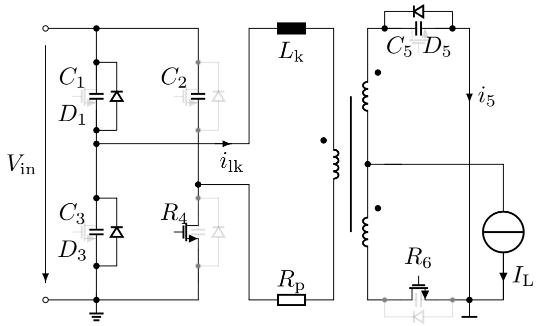
$$I_r = \frac{\frac{T_s}{2}\left(V_o - \frac{1}{n}\,V_{in} + I_o\left(R_{sek} + \frac{R_{prim}}{n^2}\right)\right)\left(d_L - d + \frac{2\,T_d}{T_s}\right)}{\left(L_f + \frac{1}{n^2}\,L_k\right)} \tag{3.13}$$

3.3.2 Transition from Power Delivery to Freewheeling Mode

Fig. 3.15a shows the equivalent circuit of the PSFB converter during Phase 1. Switches Q_1, Q_5, Q_6 are closed and being present with their resistances R_{dsp}, R_{dss}. The primary on-resistance is defined as R_{dsp} while the secondary on-resistance is R_{dss}. Switches Q_2, Q_3, Q_4 are opened. Their influence becomes visible due to capacitances and diodes.



(a) Equivalent system during Phase 1.



(b) Equivalent system during Phase 3.

Figure 3.15: The iterative dead time calculation uses a circuit analysis depending on individual switch positions and corresponding diode conduction times.

Further explanations and calculations are carried out using state-space equations (3.14).

$$
\begin{gathered}
\mathbf{A}_{\dot{\mathrm{x}}} s\, \mathbf{x} = \mathbf{A}_{\mathrm{x}}\, \mathbf{x} + \mathbf{B}_{\mathrm{u}}\, \mathbf{u} \\
\mathbf{A} = \mathbf{A}_{\dot{\mathrm{x}}}^{-1}\, \mathbf{A}_{\mathrm{x}} \qquad \mathbf{B} = \mathbf{A}_{\dot{\mathrm{x}}}^{-1}\, \mathbf{B}_{\mathrm{u}} \\
s\, \mathbf{x} - x_0 = \mathbf{A}\, \mathbf{x} + \mathbf{B}\, \mathbf{u} \\
\mathbf{y} = \mathbf{C}\, \mathbf{x} + \mathbf{D}\, \mathbf{u}
\end{gathered}
\tag{3.14}
$$

The state-space formulation for Phase 1 is shown in (3.15). R_{cp} represents the resistance of switch capacitors C_{p}. Similar switch parameters for Q_i with $i \in \{1, 3, 2, 4\}$ are assumed. Initial conditions are expressed with vector $\mathbf{x}_0$. Capacitors C_2, C_3 are charged at the beginning while C_4 is discharged. The current in inductance L_{k} equals the peak current $I_{\mathrm{L}} = I_{\mathrm{o}} + \frac{1}{2} I_{\mathrm{r}}$ reduced by the turns ratio n.

$$
\begin{gathered}
\mathbf{A}_{\dot{\mathrm{x}}} = \begin{bmatrix} 0 & -\left(R_{\mathrm{dsp}} + R_{\mathrm{cp}}\right) C_{\mathrm{p}} & 0 & 0 \\ -R_{\mathrm{cp}}\, C_{\mathrm{p}} & 0 & -R_{\mathrm{cp}}\, C_{\mathrm{p}} & 0 \\ 0 & R_{\mathrm{cp}}\, C_{\mathrm{p}} & -R_{\mathrm{cp}}\, C_{\mathrm{p}} & -L_{\mathrm{k}} \\ C_{\mathrm{cp}} & 0 & -C_{\mathrm{cp}} & 0 \end{bmatrix} \\
\mathbf{A}_{\mathrm{x}} = \begin{bmatrix} 0 & 1 & 0 & R_{\mathrm{dsp}} \\ 1 & 0 & 1 & 0 \\ 0 & -1 & 1 & R_{\mathrm{p}} + \frac{n^2}{4} R_{\mathrm{dss}} \\ 0 & 0 & 0 & -1 \end{bmatrix} \quad \mathbf{B}_{\mathrm{u}} = \begin{bmatrix} -1 & 0 \\ -1 & 0 \\ 0 & \frac{n}{4} R_{\mathrm{dss}} \\ 0 & 0 \end{bmatrix} \\
\mathbf{x} = \begin{bmatrix} v_2 & v_3 & v_4 & i_{\mathrm{lk}} \end{bmatrix}^{\top} \qquad \mathbf{u} = \begin{bmatrix} V_{\mathrm{in}} & I_{\mathrm{L}} \end{bmatrix}^{\top} \\
\mathbf{x}_0 = \begin{bmatrix} V_{\mathrm{in}} & V_{\mathrm{in}} & 0 & \frac{1}{n}\left(I_{\mathrm{L}}\right) \end{bmatrix}^{\top}
\end{gathered}
\tag{3.15}
$$

The algorithm examines the initial diode conduction capability on the basis of the state-space system (3.15). Diode 2 only conducts when $v_{\mathrm{Q2}} = v_2 + (s\, v_2 - v_{2,0}) C_{\mathrm{p}} R_{\mathrm{cp}} < -V_{\mathrm{d}}$ with V_{d} being the body diode forward voltage. Similar analysis applies to diodes 3 and 4. Using Laplace final value theorem leads to the initial voltage across switches (3.16).

$$
\begin{aligned}
v_{\mathrm{Q2}}(t_0) &= V_{\mathrm{in}} - \frac{1}{2} R_{\mathrm{cp}} I_{\mathrm{lk}} \\
v_{\mathrm{Q3}}(t_0) &= V_{\mathrm{in}} - I_{\mathrm{lk}} R_{\mathrm{dsp}} \\
v_{\mathrm{Q4}}(t_0) &= \frac{1}{2} R_{\mathrm{cp}} I_{\mathrm{lk}}
\end{aligned}
\tag{3.16}
$$

If one of these voltages is below the negative diode forward voltage V_{d}, the respective diode conducts. Since R_{dsp} is comparably small, diode 3 usually does not conduct during Phase 1. Therefore, diode 3 is grayed out in Fig. 3.15a. For negative leakage currents, diode 4 conducts. This typically occurs in boost operation. In high load buck operation, diode 2 conducts.

The algorithm first exposes the conducting diode to further choose the state-space system for Phase 1 to be calculated. Then, the selected system is chosen and by means of stored time domain equations for $v_{\mathrm{Q}i}$ with $i \in \{2, 3, 4\}$, the time of the next diode conducting is computed. If the calculated time is bigger than the total dead time, T_{d} is chosen as the next point to be calculated. Otherwise, final values are calculated for the shortest time of $v_{\mathrm{Q}i}$ and the next system is chosen. [P6]

The time domain representation of states $\mathbf{x}$ or switch voltage $v_{\mathrm{Q}i}$ is a decaying offsetted oscillation as shown in (3.17). Coefficients K_{A}, K_{B}, K_{C}, K_{D}, K_{E} are system characteristic constants or dependent on initial conditions $\mathbf{u}$.

$$
\begin{aligned}
x(t) &= K_{\mathrm{A}}\, e^{-t\, K_{\mathrm{B}}} \left(\cos\left(t\, K_{\mathrm{C}}\right) + \sin\left(t\, K_{\mathrm{C}}\right) K_{\mathrm{D}}\right) + K_{\mathrm{E}} \\
&= K_{\mathrm{A}}\, e^{-t\, K_{\mathrm{B}}} \sqrt{K_{\mathrm{D}}^2 + 1}\, \sin\left(t\, K_{\mathrm{C}} + \arctan\left(\frac{1}{K_{\mathrm{D}}}\right)\right) + K_{\mathrm{E}}
\end{aligned}
\tag{3.17}
$$

To solve $x(t)$, Newton's procedure is chosen, since $x(t) = 0$ for a certain t cannot be determined analytically. The first guess for a possible approximate solution is calculated by means of a simplified trigonometric addition theorem as shown in (3.18). The approximation is allowed since the decaying factor K_{B} comprises a comparably large time constant while the calculation of dead time effects is in focus. Typical dead times are smaller than 100 ns.

$$
\begin{aligned}
t_0 &= \frac{1}{K_{\mathrm{C}}} \left(\arcsin\left(\frac{-K_{\mathrm{E}}}{K_{\mathrm{A}} \sqrt{K_{\mathrm{D}}^2 + 1}}\right) - \arctan\left(\frac{1}{K_{\mathrm{D}}}\right)\right) \\
\dot{x}(t_0) &= K_{\mathrm{A}}\, e^{-t_0\, K_{\mathrm{B}}} \left(\left(-K_{\mathrm{B}} + K_{\mathrm{C}}\, K_{\mathrm{D}}\right) \cos\left(t_0\, K_{\mathrm{C}}\right)\right. \\
&\qquad \left. + \left(-K_{\mathrm{D}}\, K_{\mathrm{B}} - K_{\mathrm{C}}\right) \sin\left(t_0\, K_{\mathrm{C}}\right)\right) \\
x(t_0) &= K_{\mathrm{A}}\, e^{-t_0\, K_{\mathrm{B}}} \left(\cos\left(t_0\, K_{\mathrm{C}}\right) + \sin\left(t_0\, K_{\mathrm{C}}\right) K_{\mathrm{D}}\right) + K_{\mathrm{E}} \\
t &= t_0 - \frac{x(t_0)}{\dot{x}(t_0)}
\end{aligned}
\tag{3.18}
$$

After determining the final time of the selected diode or no diode conducting phase, the end values of this period are computed following (3.19) (with the identity matrix $\mathbf{I}_n$, where n is the number of states $\mathbf{x}$). Only the final value of i_{lk} is of interest since it needs prediction. However, the system could change within the dead time T_{d} due to different diode conducting phases. This makes the calculation of capacitor voltages necessary. They serve as initial conditions for subsequent processes.

$$\mathbf{x} = \left(s\,\mathbf{I}_n - \mathbf{A}\right)^{-1}\left(\mathbf{B}\,\mathbf{u} + \mathbf{x_0}\right) \tag{3.19}$$

3.3.3 Freewheeling Mode

Phase 2 is much longer than Phase 1. The full-bridge has both high-side switches Q_1, Q_2 closed while low-side switches are opened. The current circulates between switches 1 and 2. The expression (3.20) characterizes this relation analytically.

$$\frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{lk}} = -\frac{1}{L_{\mathrm{k}}}\left(\frac{n^2}{2} R_{\mathrm{dss}} + 2\,R_{\mathrm{dsp}} + R_{\mathrm{p}}\right) i_{\mathrm{lk}} = m_2\, i_{\mathrm{lk}} \tag{3.20}$$

A system-dependent factor is defined as a second phase slew rate m_2. An iterative calculation sets the end value of the leakage current i_{lk}. The first guess of the final current i_{lk} is carried out by $i_{\mathrm{lke}} = i_{\mathrm{lk}}\,(m_2\,t + 1)$. Subsequently, the derivation of i_{lk} is calculated at the predetermined current ${}^{\mathrm{d}i_{\mathrm{lke}}}/_{\mathrm{d}t} = i_{\mathrm{lk}}\,(m_2\,t + 1)\,m_2$. The derivation is assumed to be constant for this long term process. The mean derivation of the initial current and end current is calculated. The result is shown in (3.21).

$$i_{\mathrm{lk}}\left(t = (1-d)\,\frac{T_{\mathrm{s}}}{2} - T_{\mathrm{d}}\right) = 1 + \frac{m_2}{2}\,(2 + m_2\,t)\,t \tag{3.21}$$

3.3.4 Transition from Freewheeling to Power Delivery Mode

The calculation of Phase 3 follows the dead time calculation as described for Phase 1 being visualized in Fig. 3.14. Since Phase 3 is the origin of the duty cycle loss d_{L}, it presents the major influence on the dynamics. Fig. 3.15b shows the initial switch lineup.

As shown in state-space system (3.22), system dynamics highly depend on the initial value $x_0(4) = I_{\mathrm{lk}}$. This confirms the meaningfulness of the prediction of i_{lk} .

$$
\begin{aligned}
&\mathbf{A}_{\dot{\mathrm{x}}} = \begin{bmatrix} -R_{\mathrm{cp}}\,C_{\mathrm{p}} & -R_{\mathrm{cp}}\,C_{\mathrm{p}} & 0 & 0 \\ C_{\mathrm{p}} & -C_{\mathrm{p}} & 0 & 0 \\ 0 & 0 & \frac{2}{n}\,C_{\mathrm{s}} & 0 \\ 0 & R_{\mathrm{cp}}\,C_{\mathrm{p}} & -\frac{n}{2}\,(R_{\mathrm{cs}} + R_{\mathrm{dss}})\,C_{\mathrm{s}} & -L_{\mathrm{k}} \end{bmatrix} \\
&\mathbf{A}_{\mathrm{x}} = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 \\ 0 & -1 & \frac{n}{2} & R_{\mathrm{dsp}} + R_{\mathrm{p}} \end{bmatrix} \quad \mathbf{B}_{\mathrm{u}} = \begin{bmatrix} -1 & 0 \\ 0 & 0 \\ 0 & \frac{-1}{n} \\ 0 & \frac{n}{2}\,R_{\mathrm{dss}} \end{bmatrix} \\
&\mathbf{x} = \begin{bmatrix} v_1 & v_3 & v_5 & i_{\mathrm{lk}} \end{bmatrix}^\top \qquad \mathbf{u} = \begin{bmatrix} V_{\mathrm{in}} & I_{\mathrm{L}} \end{bmatrix}^\top \\
&\mathbf{x}_0 = \begin{bmatrix} V_{\mathrm{in}} & 0 & 0 & I_{\mathrm{lk}} \end{bmatrix}^\top
\end{aligned}
\tag{3.22}
$$

The final value theorem illustrates the diode conduction capability for Phase 3 according to (3.23). A diode conducts, if a certain switch voltage is below $-V_{\mathrm{d}}$. The diode conduction process is calculated with the respective state-space system. Phase 3 has the property to enable several diodes conducting concurrently. [P6]

$$
\begin{aligned}
v_{\mathrm{Q1}}(t_0) &= V_{\mathrm{in}} + \frac{1}{2}\,i_{\mathrm{lk}}\,R_{\mathrm{cp}} \\
v_{\mathrm{Q3}}(t_0) &= -\frac{1}{2}\,i_{\mathrm{lk}}\,R_{\mathrm{cp}} \\
v_{\mathrm{Q5}}(t_0) &= -\frac{R_{\mathrm{cp}}\,C_{\mathrm{p}}}{2\,C_{\mathrm{s}}}\,(I_{\mathrm{L}} - n\,i_{\mathrm{lk}})
\end{aligned}
\tag{3.23}
$$

After the selection of the appropriate state-space system and the calculation of the transition time according to Newton's procedure, final states $\mathbf{x}$ of the system are found similar to the procedure of Phase 1. An additional voltage during dead time occurs when diode 5 does not conduct. This typically occurs in boost operation or at a very low load. The secondary voltage increases within the dead time leading to a change of the system's dynamics. The secondary voltage is calculated according to (3.24). Voltage V_{s} is integrated over time and divided by half of the switching period $1/2\,T_{\mathrm{s}}$ in order to achieve an average value for this period. Afterwards, the voltage is added as v_{add} to the voltage source of the proposed model.

$$
V_{\mathrm{s}} = \frac{v_3 + R_{\mathrm{cp}}\,C_{\mathrm{p}}\,\frac{\mathrm{d}}{\mathrm{d}t}v_3 - L_{\mathrm{k}}\frac{\mathrm{d}}{\mathrm{d}t}i_{\mathrm{lk}} - (R_{\mathrm{p}} + R_{\mathrm{dsp}})i_{\mathrm{lk}}}{n}
\tag{3.24}
$$

3.3.5 Power Delivery Mode

If diode 5 still conducts at the end of Phase 3, a duty cycle loss d_{L} occurs. The secondary voltage V_{s} is created for a shorter time and thus reduces the average voltage in power delivery mode (Phase 4). This happens in buck operation of the converter.

The duty cycle loss is calculated by means of an average current at the leakage inductance i_{lka}, a current slope i_{slp} and a secondary voltage V_{s} as shown in (3.25). The diode 5 conducting time directly corresponds to the duty cycle loss d_{L}.

$$\begin{aligned}
I_{\mathrm{L}} &= I_{\mathrm{o}} - \frac{1}{2} I_{\mathrm{r}} \\
i_{\mathrm{lka}} &= \frac{1}{2}\left(\frac{1}{n} I_{\mathrm{L}} + i_{\mathrm{lk}}\right) \qquad i_{\mathrm{slp}} = \frac{1}{n} I_{\mathrm{L}} - i_{\mathrm{lk}} \\
V_{\mathrm{s}} &= \left(\frac{1}{4}(I_{\mathrm{L}} + n\, i_{\mathrm{lk}}) - \frac{I_{\mathrm{L}}}{2\,n} + I_{\mathrm{L}}\right) R_{\mathrm{dss}} - \frac{V_{\mathrm{d}}}{2} \\
t &= \frac{L_{\mathrm{k}}}{V_{\mathrm{in}} - i_{\mathrm{lka}}\,(2\,R_{\mathrm{dsp}} + R_{\mathrm{p}}) + V_{\mathrm{s}}\,\frac{n}{2}}\, i_{\mathrm{slp}} \\
d_{\mathrm{L}} &= 2\,\frac{t}{T_{\mathrm{s}}}
\end{aligned} \tag{3.25}$$

3.3.6 Equivalent Circuit Diagram

The model is shown in Fig. 3.16 with the expressions in (3.26). The influence on the dynamics of the model is transferred to the substitute voltage source V_{s} and the resistance R_{ave} with the help of the duty cycle loss d_{L} and the additional voltage v_{add}. A comparison of the performance of the model is attached in Appendix A.1.

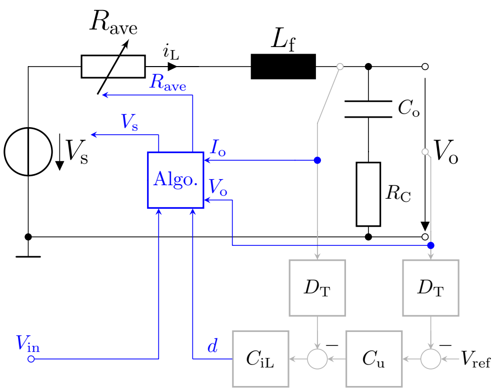


Figure 3.16: Equivalent circuit of the proposed state-space average model. The algorithm integrates dynamic effects in the substitute voltage source V_{s} and resistance R_{ave}.

$$\begin{aligned}
V_{\mathrm{s}} &= \frac{1}{n} V_{\mathrm{in}} \left(d - \frac{2\,T_{\mathrm{d}}}{T_{\mathrm{s}}}\right) - d_{\mathrm{L}}\,\frac{V_{\mathrm{in}}}{n} - \frac{2 I_{\mathrm{r}}\, L_{\mathrm{k}}}{n^2\, T_{\mathrm{s}}} + v_{\mathrm{add}} \\
R_{\mathrm{ave}} &= \frac{1}{n^2}(2\,R_{\mathrm{dsp}} + R_{\mathrm{p}})\left(d - \frac{2T_{\mathrm{d}}}{T_{\mathrm{s}}} - d_{\mathrm{L}}\right) \\
&\quad + \frac{R_{\mathrm{dss}}}{2}\left(1 + d - \frac{2T_{\mathrm{d}}}{T_{\mathrm{s}}} - d_{\mathrm{L}}\right)
\end{aligned} \tag{3.26}$$

3.4 Wiring Harness

The wiring harness as system interconnection is particularly important. It includes cables, fuses, contacts and the grounded vehicle body. Due to the high degree of branching and its local extent, a simplified model of the wiring harness is essential.

3.4.1 Model Types

A distinction is made between transmission-line and lumped-parameter models according to [71]. Transmission-line models consider the propagation delay times of electromagnetic waves, in particular. The underlying transfer functions depend on both time and location. In contrast, lumped-parameter models consist of lumped elements and can be described by Ordinary Differential Equations (ODEs) of reduced order. The suitability of lumped-parameter models can be detected by the relationship shown in (3.27). The maximum cable length l_{max} for a targeted maximum frequency f_{max} or minimum wavelength λ_{min} is calculated by means of k ranging from 10 to 60 [8, p. 28].

The maximum cable length in state-of-the-art vehicular power systems is 5 m. With a maximum cable loop length of 10 m and a value for k of 60, the maximum frequency being valid with lumped-parameter models is 500 kHz according to (3.27).

$$l_{\text{max}} \leq \frac{1}{k}\,\lambda_{\text{min}} \rightarrow f_{\text{max}} \leq \frac{c}{k\,l_{\text{max}}} \tag{3.27}$$

For the frequency range of interest below 150 kHz lumped-parameter models are sufficient, although a cable length of 33.3 m is the boundary between the two types of models for the wiring harness. Because both, the maximum cable length and the factor k are used with a safety margin, cables can be assumed to be electrically short.

3.4.2 Model Reduction

This section presents a sensitivity analysis of the lumped-parameter model of the wiring harness. A modeling analysis is included in [8, pp. 26]. The research results prove the suitability of the per-unit-length parameters for multiconductor lines above an infinite, perfectly conducting plane as presented in [71, pp. 160]. A model reduction to ohmic resistance and self-inductance is proposed for frequencies below 10 kHz. This section investigates further parasitics to establish an abstraction for frequencies up to 150 kHz.

A simplified model is employed for the analysis of the lumped-parameter model as shown in Fig. 3.17. The system includes a power supply and two wires with a disturbance and a load connected. The voltage source v =12 V provides a suitable Low Voltage (LV) supply. The source is connected to the wires by Z_{S} =1 mΩ+s1 µH corresponding to a 2 m wire with a cross-section of 35 mm^2 according to [8, pp. 32].

The load (disturbance receiver) is modeled by Z_{R} =100 mΩ to 1 MΩ. Therefore, the load current can be varied between 12 µA (quiescent, leakage current) and 120 A (high-load condition, similar to [9, p. 41]). The per-unit-length parameters of the wiring harness (resistance R', inductance L', M', capacitance C', C'_{12}) are stated in (3.28) and scaled to the cable length l_{AB}. The conductance is neglected due to its minor role for typical insulation materials in the frequency range of interest [71, p. 132].

$$\begin{aligned} Z_{\mathrm{R}}^{\mathrm{AB}} &= Z_{\mathrm{D}}^{\mathrm{AB}} = (R' + s\,L')\,l_{\mathrm{AB}} & M &= M'\,l_{\mathrm{AB}} \\ Z_{\mathrm{Rg}}^{\mathrm{A}} &= Z_{\mathrm{Dg}}^{\mathrm{A}} = Z_{\mathrm{Rg}}^{\mathrm{B}} = Z_{\mathrm{Dg}}^{\mathrm{B}} = \frac{1}{s\,\frac{C'}{2}\,l_{\mathrm{AB}}} & Z_{\mathrm{RD}}^{\mathrm{A}} &= Z_{\mathrm{RD}}^{\mathrm{B}} = \frac{1}{s\,\frac{C'_{12}}{2}\,l_{\mathrm{AB}}} \end{aligned} \tag{3.28}$$

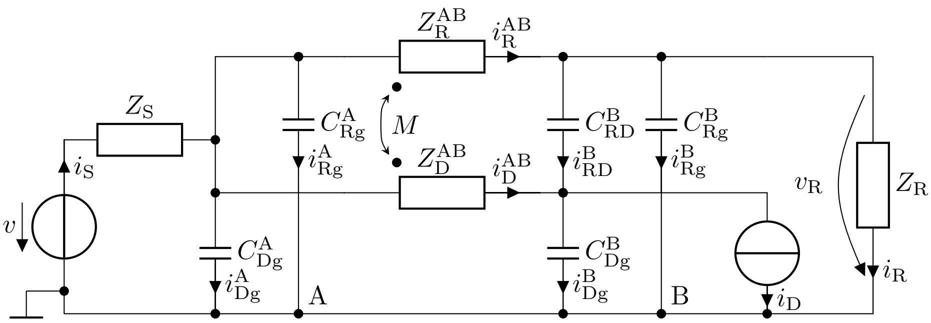


Figure 3.17: Lumped-parameter model of two wires above an infinite ground plane. A disturbance i_{D} influences the terminal voltage v_{R} of a disturbance receiver Z_{R}. The model is used to identify the suitable abstraction of vehicular wiring harnesses for the frequency of interest.

Using Kirchhoff's laws, the circuit of Fig. 3.17 is described by the state-space system (3.29). Equations are simplified by lumping $Z_{\mathrm{Rg}}^{\mathrm{A}}$ and $Z_{\mathrm{Dg}}^{\mathrm{A}}$ together in $Z_{\mathrm{g}}^{\mathrm{A}}$. This leads to $i_{\mathrm{g}}^{\mathrm{A}} = i_{\mathrm{Rg}}^{\mathrm{A}} + i_{\mathrm{Dg}}^{\mathrm{A}}$ and $Z_{\mathrm{g}}^{\mathrm{A}} = Z_{\mathrm{Rg}}^{\mathrm{A}} || Z_{\mathrm{Dg}}^{\mathrm{A}}$ (in parallel). The state-space output equation is left out since the focus is on the electrical description of the whole system.

$$\mathbf{0} = \underbrace{\begin{bmatrix} Z_{\mathrm{S}} & Z_{\mathrm{R}} & Z_{\mathrm{R}}^{\mathrm{AB}} & Ms & 0 & 0 & 0 & 0 \\ Z_{\mathrm{S}} & 0 & Z_{\mathrm{R}}^{\mathrm{AB}} & Ms & 0 & 0 & Z_{\mathrm{Rg}}^{\mathrm{B}} & 0 \\ Z_{\mathrm{S}} & 0 & Z_{\mathrm{R}}^{\mathrm{AB}} & Ms & 0 & Z_{\mathrm{RD}}^{\mathrm{B}} & 0 & Z_{\mathrm{Dg}}^{\mathrm{B}} \\ Z_{\mathrm{S}} & 0 & Ms & Z_{\mathrm{D}}^{\mathrm{AB}} & 0 & 0 & 0 & Z_{\mathrm{Dg}}^{\mathrm{B}} \\ Z_{\mathrm{S}} & 0 & 0 & 0 & Z_{\mathrm{g}}^{\mathrm{A}} & 0 & 0 & 0 \\ -1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & -1 & 0 & -1 & 0 & 1 \end{bmatrix}}_{=\mathbf{A}} \mathbf{x} + \underbrace{\begin{bmatrix} 0 & -1 \\ 0 & -1 \\ 0 & -1 \\ 0 & -1 \\ 0 & -1 \\ 0 & 0 \\ 0 & 0 \\ 1 & 0 \end{bmatrix}}_{=\mathbf{B}} \mathbf{u} \tag{3.29}$$

$$\mathbf{x} = \begin{bmatrix} i_{\mathrm{S}} & i_{\mathrm{R}} & i_{\mathrm{R}}^{\mathrm{AB}} & i_{\mathrm{D}}^{\mathrm{AB}} & i_{\mathrm{g}}^{\mathrm{A}} & i_{\mathrm{RD}}^{\mathrm{B}} & i_{\mathrm{Rg}}^{\mathrm{B}} & i_{\mathrm{Dg}}^{\mathrm{B}} \end{bmatrix}^{\top} \qquad \mathbf{u} = \begin{bmatrix} i_{\mathrm{D}} & v \end{bmatrix}^{\top}$$

The corresponding transfer function between disturbance current i_{D} (part of the input vector $\mathbf{u}$) and terminal voltage $v_{\mathrm{R}} = i_{\mathrm{R}}\, Z_{\mathrm{R}}$ at the disturbance receiver Z_{R} is calculated according to (3.30). The load current i_{R} is one system state within the state vector $\mathbf{x}$. Two canonical basis vectors $\mathbf{e_1}$ (in the Euclidean plane) and $\mathbf{e_2}$ (in $\mathbb{R}^8$) extract the corresponding transfer function $G_{\mathrm{i_D}\to\mathrm{v_R}}(s)$ from the matrix $\mathbf{G_{u\to x}}(s)$.

$$\begin{aligned} \mathbf{G_{u\to x}}(s) &= (-\mathbf{A})^{-1}\,\mathbf{B} \\ G_{\mathrm{i_D}\to\mathrm{v_R}}(s) &= \mathbf{e_2}^{\top}\,\mathbf{G_{u\to x}}(s)\,\mathbf{e_1} Z_{\mathrm{R}} \qquad \text{with } \mathbf{e_1} \in \mathbb{R}^2 \wedge \mathbf{e_2} \in \mathbb{R}^8 \end{aligned} \tag{3.30}$$

Sensitivity to the Frequency-Dependent Resistance

The resistance R' of metallic wires is dependent on the frequency f. The skin effect is calculated according to [156, pp. B13]. The current displacement is described by partial functions (3.31). The parameter $w = 0.064 \cdot {}^{1.03}/\sqrt{f}$ is used for estimating the conductive thickness of the copper wire. The expression includes the specific resistance of $\rho = 17.1\,\mathrm{m\Omega\,mm^2/m}$, the cross-section A and radius r according to (3.31).

$$R' = \underbrace{\frac{\rho}{A}}_{=R_0'} \begin{cases} 1 & \text{for } \frac{2\,r}{w} < 2 \\ \left[1 + \left(\frac{2\,r}{5.3\,w}\right)^4\right] & \text{for } 2 < \frac{2\,r}{w} < 4 \\ \frac{1}{4} + \frac{2\,r}{4\,w} & \text{for } 4 < \frac{2\,r}{w} < 10 \\ \frac{2\,r}{4\,w} & \text{for } \frac{2\,r}{w} > 10 \end{cases} \tag{3.31}$$

To be valid up to 10 kHz, the wire is modeled as R_0 in series to the self-inductance L. For LF, R_0 is dominant while for high frequencies L is dominant. Between these subareas, an increase of $R(f)$ due to the skin effect influences the cable impedance. [8, p. 38]

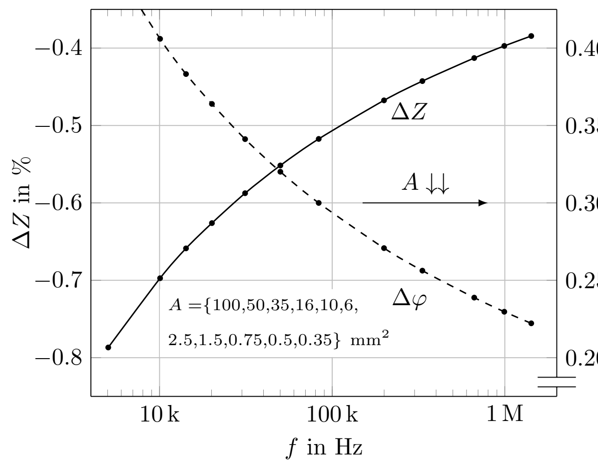
A calculation is carried out to estimate the error for neglecting the skin effect. The wire impedance $\underline{Z(j\,2\pi f)} = R(f) + j2\pi f L$ contains the wire resistance R' and the self-inductance L' according to (3.31) and (3.32), respectively. The parameters for L' are chosen to be a height above ground of $h = 20\,\mathrm{mm}$ (low inductance [8, p. 35]) and cross-sections A between $0.35\,\mathrm{mm}^2$ to $100\,\mathrm{mm}^2$ (standard A for LV power systems [31, p. 10]).

Fig. 3.18a visualizes the maximum deviation of the impedance Z for cable models without versus with skin effect for cable cross-sections A. The maximum deviation occurs between low and high-frequency due to the dominance of R_0 or L. When neglecting the skin effect, the appearing deviation is less than 1 % and 0.5° for all stated A.

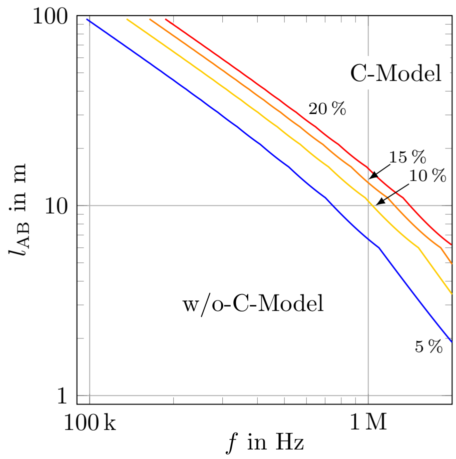
Thus, the frequency-dependence of the ohmic resistance can be omitted without greatly influencing the accuracy of the cable impedance. In contrast, the skin effect according to [71, p. 142] or [156, p. B13] should be considered for the analysis of the power loss across cables due to high-frequency oscillating load profiles. In the following the per-unit-length ohmic resistance of the wire is assumed to be $R' = R_0'$.

Sensitivity to the Line Capacitance

Fig. 3.17 includes the line-line capacitance within $Z^{\mathrm{A}}_{\mathrm{RD}}$, $Z^{\mathrm{B}}_{\mathrm{RD}}$ and the line-ground capacitance within $Z^{\mathrm{A}}_{\mathrm{Rg}}$, $Z^{\mathrm{A}}_{\mathrm{Dg}}$, $Z^{\mathrm{B}}_{\mathrm{Rg}}$, $Z^{\mathrm{B}}_{\mathrm{Dg}}$. The corresponding wire parameters are calculated by means of the multi-conductor wire model above an infinite, perfectly conducting ground plane [71, pp. 173]. The model is suggested and verified for the application on vehicular wiring harnesses in [8, p. 29].



(a) Maximum deviation of the cable impedance in absolute value ΔZ and phase $\Delta\varphi$ when considering DC resistance only or the frequency-dependent ohmic resistance. Different cross-sections in the range of 0.35 mm² to 100 mm² demonstrate that the skin effect can be neglected due to the dominating inductance.



(b) Deviation of the transfer function $\Delta G_{i_{\mathrm{D}}\rightarrow v_{\mathrm{R}}}$ in dependence of the cable capacitance. The transfer functions differ by 5 % at 150 kHz only with cable lengths of more than 70 m.

Figure 3.18: Influence of the skin effect and the cable capacitance on the transfer function between system-attached devices. Both can be neglected when modeling high inductive networks for frequencies up to 150 kHz.

The per-unit-length self-inductance L' for a wire with the radius r and the height above ground h is calculated by means of (3.32). The permeability μ equals μ_0=0.4πµVs/(Am). The inverse hyperbolic cosine can be approximated by the natural logarithm for $r << h$. This wide-separation approximation is applied for $h > 5\,r$, which results in an error of less than 2.7 %. [71, pp. 126]

$$L' = \frac{\mu}{2\pi} \cosh^{-1}\left(\frac{h}{r}\right) \overset{r<<h}{\approx} \frac{\mu}{2\pi} \ln\left(\frac{2h}{r}\right) \tag{3.32}$$

The mutual inductance M' between two cables with the distance d_{12} and both at the same height h above ground is calculated according to (3.33). [71, p. 174]

$$M' = L'_{12} = \frac{\mu}{4\pi} \ln\left(1 + \frac{4h^2}{d_{12}^2}\right) \tag{3.33}$$

The line-ground capacitance with the permittivity ε (being ε_0=8.854 $\cdot\, 10^{-12}$As/(Vm) for vaccum) is calculated with (3.34). For $h < 5\,r$ the wide-separation approximation underestimates the capacitance. The actual capacitance is bigger. [71, pp. 125]

$$C' = \frac{2\pi\varepsilon}{\cosh^{-1}\left(\frac{h}{r}\right)} \overset{r<<h}{\approx} \frac{2\pi\varepsilon}{\ln\left(\frac{2h}{r}\right)} \tag{3.34}$$

The line-line capacitance is calculated according to (3.35) with $\mathbf{L}$ being the inductive matrix including self-inductances on the diagonal and mutual inductances on the remaining places [71, p. 173]. Closed-form solutions for the line capacitance are further presented in [157, p. 29].

$$\mathbf{C} = \mu\,\varepsilon\,\mathbf{L}^{-1} \tag{3.35}$$

A scenario with high capacitance is utilized for an assessment of its impact on transfer functions between distributed system attached devices. Two 35 mm^2 wires with a separation of d_{12} =1 cm, both h =5 mm above the ground plane (vehicle body) are selected. The assumptions are based on the identified conditions in [8, p. 36]. This results in a line-ground capacitance C' of 56 pF/m and a line-line capacitance C'_{12} of 24 pF/m. The self-inductance amounts to L' =192 nF/m and the mutual inductance to M' =69 nF/m. The load impedance Z_{R} is chosen to be either 100 mΩ or 1 MΩ. The analysis iterates through transfer functions $G_{\mathrm{i_D}\rightarrow\mathrm{v_R}}$ for wire lengths between 1 m to 100 m. The relative deviation of the model without capacitance compared to the model with capacitance included is calculated.

Fig. 3.18b visualizes the deviation of the transfer function $\Delta G_{\mathrm{i_D}\rightarrow\mathrm{v_R}}(s)$ when considering the model without capacitance (w/o C'_{12}, C') versus with capacitance. The applied load impedance Z_{R} is selected to be 1 MΩ. The deviation between the transfer functions is applied on the applicate axis and four contour lines are highlighted in color. The abscissa axis visualizes the frequency at which the deviation occurs. The ordinate axis shows the cable length of the system being considered. A longer cable length corresponds to an increased absolute capacitance.

Only very long cables above 70 m hold enough capacitance to lead to deviations of more than 5 % at a frequency of 150 kHz. Typical vehicular power systems with a cable loop length of less than 10 m are free of capacitive effects up until 700 kHz. When reducing the load impedance Z_{R} the deviations shift to higher frequencies. Therefore, the actual deviations are smaller for low-impedance loads and more beneficial geometric conditions of the wiring harness. Thus, capacitive effects can be left out in wiring harness modeling for the frequency range of interest. If higher frequencies or cable lengths are required, the capacitance needs to be considered. Further analysis is presented in [S1].

Sensitivity to the Line Inductance

A calculation of the line inductance is presented in [71, p. 173]. Tight cable bundles can lead to the wire distance d_{12} falling below 20 mm. Supply cables with cross-sections of up to 50 mm^2 cannot be twisted to reduce the induced voltages due to inductive coupling. Therefore, a sensitivity analysis of mutual inductances according to (3.33) is carried out. In Fig. 3.17 the mutual inductance M is visualized between the supply lines of both the disturbance source i_{D} and the receiver (i_{R}, Z_{R}).

Similar to the capacitance analysis, a minimal state-space system is developed to calculate the influence of the mutual inductance on the transfer function between disturbance source with current i_{D} and disturbance receiver with impedance Z_{R}, current i_{R}. Branches are mutually connected via mutual inductance M and supplied by a voltage source v with impedance Z_{S}, current i_{S}.

For the transfer function calculation the state-space system (3.36) is used. This is equivalent to the system (3.29) but without capacitance.

$$\mathbf{0} = \underbrace{\begin{bmatrix} Z_{\mathrm{S}} & Z_{\mathrm{R}}^{\mathrm{AB}} + Z_{\mathrm{R}} \\ -1 & 1 \end{bmatrix}}_{=\mathbf{A}} \underbrace{\begin{bmatrix} i_{\mathrm{S}} \\ i_{\mathrm{R}} \end{bmatrix}}_{=\mathbf{x}} + \underbrace{\begin{bmatrix} M\,s & -1 \\ 1 & 0 \end{bmatrix}}_{=\mathbf{B}} \underbrace{\begin{bmatrix} i_{\mathrm{D}} \\ v \end{bmatrix}}_{=\mathbf{u}} \tag{3.36}$$

The system is further simplified by applying $i_{\mathrm{R}}^{\mathrm{AB}} = i_{\mathrm{R}}$ and $i_{\mathrm{D}}^{\mathrm{AB}} = i_{\mathrm{D}}$. The transfer function $G_{i_{\mathrm{D}} \to v_{\mathrm{R}}}$ is calculated by means of (3.30). The result is presented in (3.37).

$$G_{i_{\mathrm{D}} \to v_{\mathrm{R}}}(s) = -\frac{Z_{\mathrm{S}} + M\,s}{Z_{\mathrm{S}} + Z_{\mathrm{R}}^{\mathrm{AB}} + Z_{\mathrm{R}}}\, Z_{\mathrm{R}} \tag{3.37}$$

Fig. 3.19 shows the mutual inductance M versus cable bundle length l_{AB} for distances d_{12} of the two cables in the range 10 mm to 50 mm. The values are based on [8, p. 35]. The left and center plots differ in the height above ground h of the examined cables. In this example, mutual inductances of up to 800 nH can be reached. Small separation d_{12} and large heights above ground h increase the mutual inductance M.

The obtained transfer function $G_{i_{\mathrm{D}} \to v_{\mathrm{R}}}$ from (3.37) with $M = 0$ is contrasted to the transfer function with $M \neq 0$. The right plot of Fig. 3.19 shows the deviation of the transfer function $\Delta G_{i_{\mathrm{D}} \to v_{\mathrm{R}}}$ between the disturbance source i_{D} and the disturbance receiver v_{R} when considering the model without (L-Model) or with mutual inductances (M-Model). The deviation is applied on the applicate axis and contour lines are highlighted in color. The ordinate axis shows the mutual inductance and the abscissa axis contrasts the frequency at which the deviation of the respective contour line occurs.

Small mutual inductances of less than 90 nH do not influence the accuracy of the model. The L-Model leads to sufficient results. Such small inductances occur in tight cable bundles with d_{12} of 10 mm and lengths l_{AB} of less than 30 cm (left plot), for example. Exemplary values are highlighted with colored markers within the left plots of Fig. 3.19.

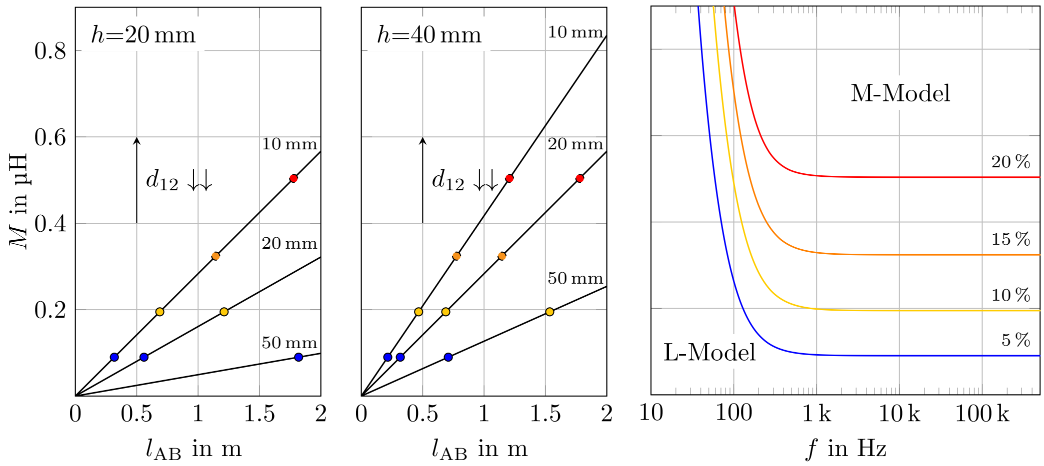


Figure 3.19: The influence of omitting mutual inductances on the modeling accuracy: Mutual inductance in dependence of bundle length l_{AB}, distance between cables d_{12} and height above ground h. The right plot demonstrates the deviation of transfer functions $\Delta G_{i_D \to v_R}$ when neglecting mutual inductances. The mutual inductance needs to be less than 90 nH to satisfy the maximum deviation of 5 %.

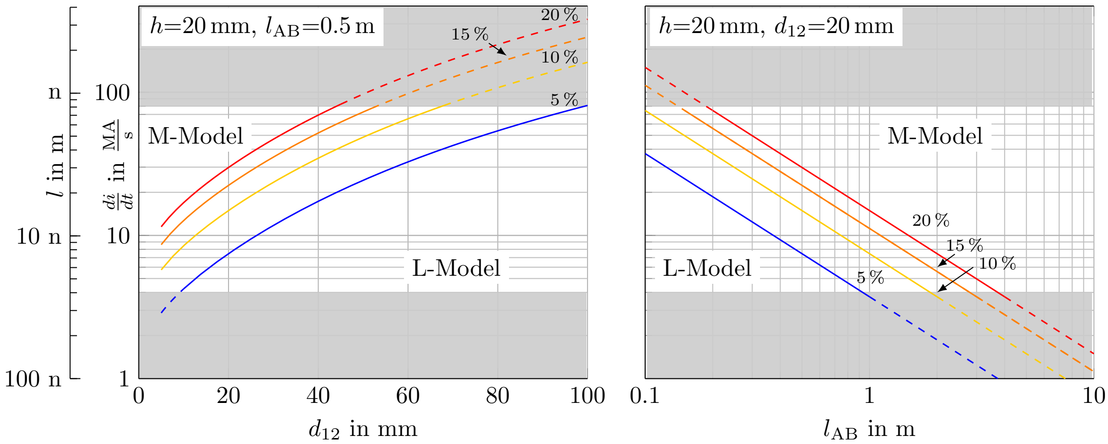
Bundle lengths l_{AB} of more than 1 m within cable bundles with d_{12} =10 mm are identified within this project in state-of-the-art vehicular wiring harnesses. Thus, mutual inductances cannot be neglected for wiring harness lumped-parameter models.

Furthermore, the mutual inductance can be very decisive in the event of a fault such as a S/C. In the case of a S/C inside of an attached device, the maximum current slew rate along the supplying cable is limited due to its self-inductance L, the impedance of the power supply Z_S and the supply voltage V. The following analysis assumes a supply voltage of 12 V.

Fig. 3.20 demonstrates the induced voltage due to a S/C in a mutually connected branch via inductance M. The cable bundle is characterized by height above ground h =20 mm, distance between cables d_{12} and bundle length l_{AB}. To analyze the impact of S/Cs on the induced voltage ΔV, another relationship is developed using (3.32), (3.33). Disturbance receiver i_R and source i_D are mutually connected via a cable bundle with the length l_{AB} and the distance between wires d_{12}. The cable length l of i_D is iterated to analyze its influence. The longer the cable of i_D, the smaller the maximum current slew rate and the smaller ΔV for a given supply voltage V (3.38).

$$\frac{\Delta V}{V} = \frac{1}{2}\,\frac{l_{AB}}{l}\,\frac{\ln\left(1+4\,\frac{h^2}{d_{12}^2}\right)}{\ln\left(2\,\frac{h}{r}\right)} \qquad V = L'\,l\,\frac{\mathrm{d}i_D}{\mathrm{d}t} \tag{3.38}$$

The maximum current slew rate is limited due to the self-inductance L' scaled to the disturbance source cable length l and the supply voltage V according to (3.38).



A in mm^2	0.35	0.75	1.5	2.5	6	10	16	35
n in cm	12.5	13.6	14.8	15.8	17.8	19.3	20.9	24.2

Figure 3.20: Relative induced voltage due to a S/C in a neighboring branch being mutually coupled by inductance M. The mutual inductance is characterized by bundle length l_{AB}, cable distance d_{12} and height above ground h. The S/C supplying cable is characterized by the length l and the maximum S/C current slew rate as described in the respective table.

The relative induced voltage with respect to the supply voltage when considering the model without (L-Model) versus with mutual inductance (M-Model) is applied on the applicate axis in Fig. 3.20. Four contour lines are highlighted and 5 % corresponds to 600 mV. The abscissa axis visualizes the distance between cables d_{12} or bundle length l_{AB}, respectively. The ordinate axis displays the maximum current slew rate of the S/C $\frac{di}{dt}$. This current slew rate occurs with supply cables of different cross-sections A and lengths l. The cable length for each cross-section can be calculated by means of the second ordinate axis and the associated Table in Fig. 3.20. Atypical values are grayed out.

According to the left plot, the L-Model leads to sufficient results for supply cables longer than l =3 m (current slew rate of less than 6 A/µs) and cable distances d_{12} above 20 mm. The M-Model is selected for elevated current slew rates and smaller d_{12}.

Moreover, the right plot demonstrates that longer bundle lengths l_{AB} increase the sensitivity of the induced voltage to S/Cs. Cable bundles with lengths of more than 1 m and cable distances of less than 20 mm are typical for state-of-the-art vehicular wiring harnesses. Since fast transients embody high current slew rates approaching those of S/Cs, mutual inductances need to be considered.

In summary, mutual inductances M can be neglected for LF signals <100 Hz (L-Model). Especially for transient and subtransient disturbances up to 150 kHz or fault simulation like S/Cs, wiring harnesses have to be modeled with their mutual inductances (M-Model).

Translation of Standardized Wiring Harness Data

The data of automotive wiring harnesses is stored in standardized file formats. Available descriptions (such as Kabelbaumliste (KBL) files) include data about the conductor and insulation [8, p. 54]. Fig. 3.21 lists available data within selected files. To further calculate mutual inductances, the wiring harness geometry is added. The description of cable bundles in terms of the distance between cables and lengths is required.

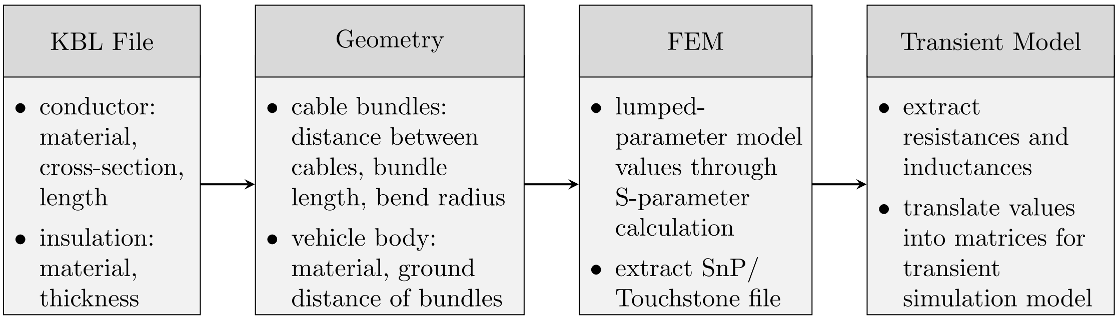


Figure 3.21: Translation of standardized wiring harness data to the transient simulation model.

EM Consulting and Software PEEC solver is selected for the calculation of parasitic effects [158–161]. It is suitable for LF electromagnetic fields and allows a fast field calculation [162]. The software platform is able to decode automotive KBL files. The Finite Element Method (FEM) calculation generates a Touchstone file including relevant scattering parameters $\mathbf{S}$. They describe the modeled wiring harness based on defined pins. Resistances $\mathbf{R}$ and self-inductances as well as mutual inductances $\mathbf{M}$ are extracted by means of (3.39) according to [71, p. 716].

$$\mathbf{Z} = Z_0\,\mathbf{I}_n \left(\frac{\mathbf{I}_n + \mathbf{S}}{\mathbf{I}_n - \mathbf{S}}\right) = \mathrm{diag}(\mathbf{R}) + j\,2\pi f\,\mathbf{M} \tag{3.39}$$

The equation includes n electric current branches. Parameters are calculated in dependence of the reference impedance Z_0 being $50\,\Omega$, for instance. The unit matrix $\mathbf{I}$ of the order n is used for compatibility reasons. The S-parameter matrix $\mathbf{S}$ includes diagonal elements S_{mm} where $m \leq n$ for the description of a branch (resistance, self-inductance). Also, the matrix $\mathbf{S}$ includes S_{mk} on the remaining places where $k \leq n \wedge k \neq m$ for the description of mutual coupling. The resistance vector $\mathbf{R}$ is created with n elements as shown in (3.40). Inductances are stated within the symmetric matrix $\mathbf{M}$. This includes self-inductances L and mutual inductances M. In this case $M_{mk} = M_{km}$ applies.

$$\mathbf{R} = \begin{bmatrix} R_1 & R_2 & R_3 & \cdots & R_n \end{bmatrix}^\top \qquad \mathbf{M} = \begin{bmatrix} L_1 & M_{12} & M_{13} & \cdots & M_{1n} \\ M_{21} & L_2 & M_{23} & \cdots & M_{2n} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ M_{n1} & M_{n2} & M_{n3} & \cdots & L_n \end{bmatrix} \tag{3.40}$$

3.5 Frequency Based Differentiation of Modeling Methods

The obtained findings with respect to modeling of the wiring harness and attached devices such as consumers and power electronic supplies are briefly assigned to the corresponding frequency ranges.

Fig. 3.22 contrasts different model abstractions of the wiring harness. There are two model types to be distinguished: lumped-parameter and transmission-line models. The lumped-parameter model consists of lumped RLC-elements and can be described by simplified ODEs. Lumped-parameter models can be applied to vehicular power systems up until 800 kHz. The prerequisite for validity is the compliance with the set premises of a typical tree-structured vehicular power system (e.g. restriction of cable cross-sections, cable lengths). Above 800 kHz, transmission-line models become necessary. This also confirms [8, pp. 26].

The lumped-parameter model can be reduced to R_{dc} for low-frequency behavior until 10 Hz. Up until 100 Hz the self-inductance L of the cable needs to be added to the model. At higher frequencies, also mutual inductances M between cables need to be considered. In the range of 1 kHz to 10 kHz, the frequency-dependent resistance influences the cable impedance. However, this impact is minor and can be neglected for system-inherent transfer function analysis, see Section 3.4.2. At frequencies above 10 kHz and below 800 kHz, the cables inductance L and the mutual inductive coupling M to neighboring cables dominate the cable impedance. Mutual inductances need to be considered for transfer function analysis. Above this frequency of 800 kHz, the coupling capacitances C become noticeable.

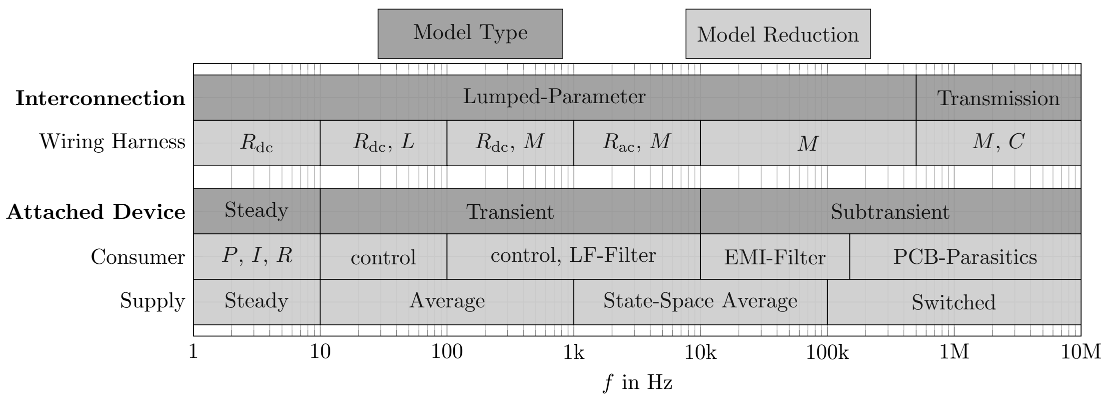


Figure 3.22: Frequency dependence of reduced model abstractions of wiring harness, system attached devices and power electronic supplies. Depending on the required validity in a certain frequency range, stated abstractions can be distinguished.

Fig. 3.22 also shows the model types of attached devices versus frequency. The classification of model types is carried out according to the introduced modeling methodology of the modular modeling approach with: steady-state, transient and subtransient behavior.

Consumers and the supply can be modeled with their nominal power load P, current load I or resistance R and steady-state models below 10 Hz as proposed in [P2], respectively.

Within the transient model type, the consumer models are dominated by their control and LF filter characteristics. The subtransient behavior is dominated by the EMI filter characteristics up until 150 kHz. Above, the PCB parasitics dominate the measured impedance from the system's perspective. The proposed modeling methodology of consumers can also be utilized to generate different models of one component being valid for delimited ranges of frequency.

Power electronic supplies in the presence of converters can be modeled as a steady-state model (below 10 Hz), an average model (below 1 kHz) or a switched model. The accuracy of the switched model is the most extensive, but also requires the most computational effort. Therefore, an alternative model was developed within this work.

The proposed state-space average model increases the accuracy of the dynamic behavior in the frequency range up until the switching frequency of typically 100 kHz at reduced computation effort. The algorithm can also be applied to other switching converter topologies or inverters. Moreover, the algorithm could help to reduce the computation effort needed for Wide-Bandgap semiconductor converters being switched at a frequency of e.g. 1 MHz [27].

4 Power System Test Bench for the Transient Model Validation

Established (sub-)transient simulation models need to be validated. The validation can be carried out by means of test benches, prototype or series production vehicles. First of all, this chapter explains why a test bench was selected. Subsequently, the designed test bench is presented in detail. Initial requirements, the derived conceptual design and the physical implementation are described. Moreover, simulation models are validated and two power system stress tests are pictured.

4.1 Physical Vehicle Development

Three vehicle abstractions can be identified during the physical vehicle development as visualized in Fig. 4.1. After setting up the requirements, system specifications are derived. These definitions are implemented in a simulation model. The model needs the smallest effort of implementation. For instance, changes in parameters or software can be translated directly. However, the simulation results can only be transferred to the series production power system with a valid parameterization. This stage of development is characterized by a volatility of the underlying information. [50, pp. 44]

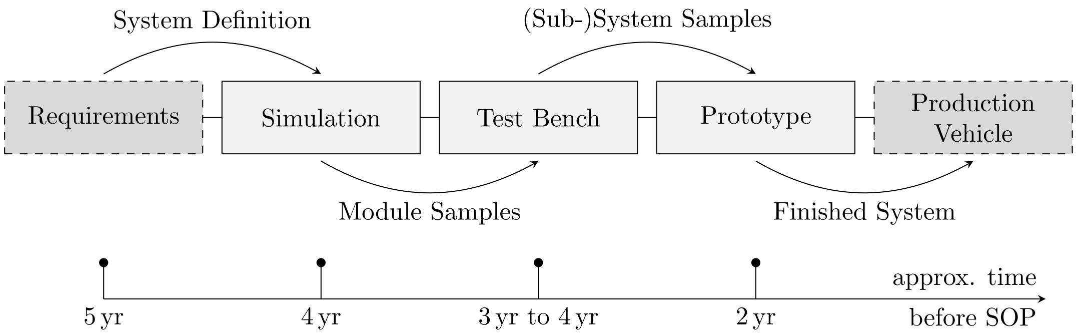


Figure 4.1: Temporal comparison of physical vehicle development methods and their inputs.

Several test benches are created to ensure the functionality of hard- and software. A power system test bench contains the first module samples. Early versions of test benches include complete subsystems. The completeness of the entire power system can only be guaranteed in a late phase when all components have been fully developed.

Prototype vehicles are used to place tested subsystems. The completeness of the power system is not guaranteed. For example, drive train prototypes do not necessarily include all the electric components for the entertainment system. In contrast, later stage prototypes and series production vehicles include the complete tested power system. Usually, only software troubleshooting and active diagnostic jobs are carried out. Diagnostics are used to prevent early module failures and to generate maintenance instructions.

A power system test bench proves as the most reliable validation platform for simulation models. Early concept system architectures can be implemented with reduced effort. The test bench also offers a high level of flexibility. For example, several equipment variants of a vehicle can be mapped within one test bench. A suitable replica of the series production power system is achieved by a sophisticated conceptual design and upgradability throughout the physical vehicle development process.

4.2 Test Bench Requirements

The target power system test bench should be designed to allow a transient model validation. This includes the emulation of typical vehicular operating points and fault conditions. The focus is set on the investigation of (sub-)transient processes such as power fluctuations or Short Circuits (S/Cs).

The identified requirements are divided into four parts:

- **Power System Replica**

  One central component of the test bench is the Device under Test (DUT). It is a replica of a future-oriented power system. The impedance of the replica should be similar to that of a series production vehicle in the frequency range of interest (below 150 kHz). The DUT contains all safety-critical components (such as Electric Power Steering (EPS), Electric Brake Pump (EBP), Windshield Wiper (WIP) and lights). Additional comfort consumers should be integrated to emulate a realistic load. Ideally, a concept is developed which allows the examination of several power system architectures.

  The aim is to design a modular concept that allows the DUT to be substituted by a prototype vehicle. Essential interfaces for the communication and measurement data acquisition should be reconfigurable for both variants, therefore.

- **Control of the DUT**

  The DUT being either an abstracted test bench or a prototype vehicle needs to be controlled in order to achieve specific operating points. Therefore, a simulation of the environment of the vehicle (e.g. brightness, subsurface conditions) and target references (e.g. velocity, Daytime Running Lamp (DRL), turn signals) must be transmitted to the Central Control Unit (CCU) of the vehicle on typical automotive communication buses.

Further ancillaries must be operated safely. Therefore, separate hardware such as power supplies, electronic loads and hardware prototypes need communication interfaces to the controller.

- **Measurement and Evaluation**

  Distributed voltages and currents need to be measured. Electrical values should be properly resolved up to a frequency of 150 kHz. Voltages range from 0 V to 32 V resulting from the standardized voltages according to DIN 7637 [73]. Currents can be up to 1.5 kA (resulting from the Low Voltage (LV) level of 12 V and typical loop resistances of approximately 8 mΩ).

  Acquired measurements should be evaluated automatically. Post-processing of signals in the frequency range is intended. In general, a measurement should be repeatable and reproducible. An automated test chain must be implemented on a controller.

- **Assuring a Development Method Consistency**

  The main application of the power system test bench is the validation of (sub-)transient simulation models. A software coupling between acquired measurements and the stimulation of the simulation model is necessary. Measurements and simulation results should be compared automatically. To ensure consistency of the development methods (simulation, test bench and prototype vehicle), a physical modular design must be considered.

  Another application is the testing of sample hardware. Technical innovations for the voltage stabilization can be investigated. Fail-operational functions of safety-critical components should be examined. Electrical requirements towards components can be derived (e.g. trip times and thresholds of electronic fuses).

4.3 Conceptual Design

Previous LV power system test benches do not focus on preserving the electrical impedance up to 150 kHz. Some test benches do not include the wiring harness of the vehicle [163, 164] but others do have an automotive tree-structured wiring harness as in [8, 50, 94, 165]. Mostly, physical components are emulated by electronic loads. This allows the combination of multiple components as a baseload or to replicate recorded power profiles. Integrating such atypical components as electronic loads influences the impedance of the system. Previous literature did not pay attention to this. [50, 94, 163–165]

The focus was placed on electro-mechanical components such as generators in [163, 166] or an EPS [94, 165]. Moreover, arc tests were carried out using 48 V/12 V power system test benches in [55, 163]. The measurement systems of test benches were designed for frequencies below 10 kHz [94, p. 58], [165] and current slew rates below 50 A/ms [50, p. 53]. Higher current slew rates due to S/Cs are expected in this project.

Similar studies were carried out for High Voltage (HV) power systems. The impedance of the power system was measured up to 150 kHz for a validation of voltage ripple simulation models. Maintaining the impedance without adding further components enables a valid representation of the vehicle in this frequency range. [167]

4.3.1 Power System Architecture

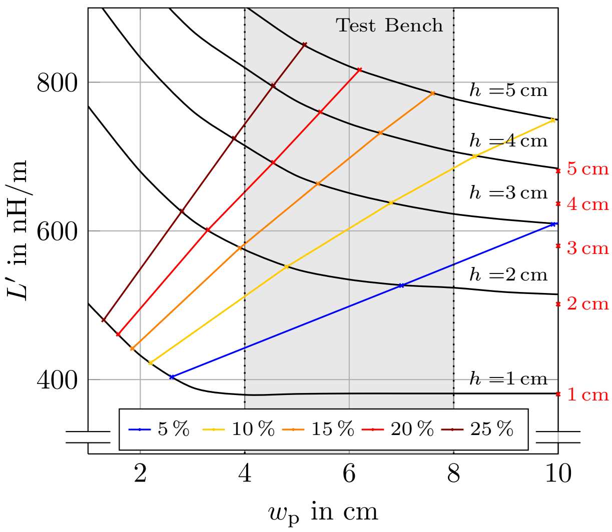
The power system of the upcoming Battery Electric Vehicle (BEV) BMW iX is chosen. Its tree-structured architecture is capable of supplying a total of 3.5 kW of loads and includes an aluminum Busbar (BB). The BB can carry a continuous current of 300 A and extends the power capacity of the wiring harness architecture. Due to the elevated electrification of vehicles, high power ratings can be assumed in the future [8, pp. 2].

The industry standard tree-structured wiring harness will continue to be preferred in the medium term. Research projects with ring power system topologies as proposed in [36] are not considered further in this work.

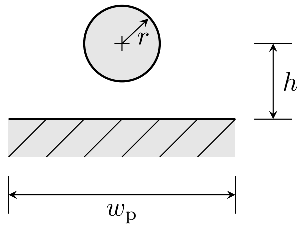
The modular power system test bench concept is based on an aluminum frame. The wiring harness is mounted on top of aluminum frame elements with a certain width. Fig. 4.2a visualizes the expected deviations of the wiring harness self-inductance when using an aluminum frame instead of the vehicle body as the ground connection. The calculation is carried out for a constellation as shown in Fig. 4.2b in EMCoS® (refer to Section 3.4.2). The self-inductance per-unit-length of 1 m is shown in Fig. 4.2a in dependence of the plane width w_{p} and the height h. The cable cross-section is $35\,\mathrm{mm}^2$. For an infinite plane width, the self-inductance L' highlighted in red would arise.

Colored contour lines in Fig. 4.2a visualize the relative deviation of the self-inductance between width-restricted and infinite ground planes. Aluminum profiles with widths ranging from 4 cm to 8 cm have been installed. The deviation of the self-inductance can be kept below 5 % when the height of mounted cables does not exceed a third of the plane width. For instance, when mounting a cable above an aluminum frame element of 8 cm , the distance to the surface of the element should not exceed 2.5 cm. During installation, a maximum cable height of about 3 cm was implemented. Thus, the self-inductance of the test bench wiring harness should deviate from that of the vehicle by a maximum of 10 %.

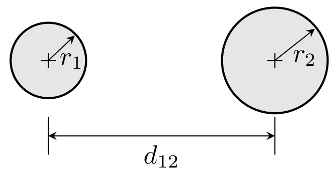
The selected future oriented-wiring harness includes several components with ground cables as a return path. This ground cable is not necessarily connected to the vehicle body, since the body of the BMW iX partly consists of non-conductive carbon fiber parts. For these cable constellations, the loop inductance between two cables does not depend on the height above ground h. The analytical expression (4.1) is used for the calculation of the per-unit-length loop inductance L'. The inductance arises between two cables of distance d_{12} and radii r_1, r_2 as demonstrated in Fig. 4.2c. [71, p. 121]



(a) Characteristic self-inductance L' per-unit-length of 1 m for a cable with a cross-section of 35 mm^2 for different heights h above the surface of a perfectly conducting plane with width w_p. Colored contour lines visualize the relative deviation of inductance compared to an infinite plane (red).



(b) Illustration of the inductance calculation for a cable above a width-restricted plane.



(c) Illustration of the calculation of the per-unit-length inductance for two adjacent cables.

Figure 4.2: The test bench does not contain a vehicle body but width-restricted ground planes. The self-inductance of the wiring harness in the test bench differs from that of a vehicle by up to 10 %.

$$L' = \frac{\mu}{2\,\pi} \ln\left(\frac{d_{12}^2}{r_1\,r_2}\right) \tag{4.1}$$

The distance between the cables and the aluminum elements must be observed. It is important to mind the distance between the cables and the aluminum elements. Mounted cables should be of similar height as the ones in the vehicle. Many components do have a separate return path instead of the ground plane of the vehicle for the chosen power system architecture. For these constellations, the height above ground can be neglected.

Composition of Physical Components

Maintaining the impedance of the power system is of high importance. Therefore, only the vehicular components are attached to the wiring harness. Electronic load emulators are not installed since they would affect the impedance.

Safety-critical components as well as high power consumers are installed. The selection of the necessary components is based on the method introduced in Section 3.1. Only series production components are integrated.

The focus is on the investigation of short-time processes with a validity below 150 kHz. The mechanical counter actuators for electromechanical drives such as EPS or EBP are not implemented. Rather, the impedance of the input circuit is decisive for the short-term processes of interest [P3].

4.3.2 Voltage-Scaled Dynamic Equivalent Power Supply

A DC/DC converter prototype has been built within this project. It connects the HV and the LV power systems. A 400 V/12 V converter model has been designed on the basis of the initial formulated requirements and system definitions. The converter has been implemented in a voltage-scaled version whilte maintaining its dynamic properties. This section introduces the voltage-scaling methodology.

Motivation for Voltage-Scaling and Selected Converter Topology

In order to satisfy the requirements for contact protection below 60 V according to [100, 102], the primary voltage of the converter 400 V has been scaled down to the automotive standard of 48 V. This has several advantages and challenges. Satisfying the voltage level allows a simpler test setup. Safety specifications for the protection of persons against electric shock below of 60 V are manageable.

According to the literature, the galvanic isolation for switch-mode power supplies is needed for voltages above 60 V [102]. Isolated converter topologies under review were half-bridge resonant LLC converters with resonance tank and full-bridge topologies [168]. Resonant converters achieve higher switching frequencies and lower switching losses by zero voltage switching. The disadvantage of resonant converters is the reliance on the frequency modulation for its control. Thus, the complex control technique requires a precise execution. Further, elevated conduction losses occur due to circulation currents within the resonance tank [169, 170].

Another topology for isolated HV/LV converters is the Phase-Shifted Full-Bridge (PSFB) converter. Its switches are rated for half the input power. The flux-imbalance during positive transient load changes is a known weakness. Asymmetric gate driving signals can lead to a saturation of the transformer. Blocking capacitors filter the DC bias from the transformer. The reasons given lead to a preference for the PSFB converter. Its topology is chosen as the basis for the voltage-scaling method.

The idea of voltage scaling is to keep the same topology as the converter. This helps to generate similar physics. For instance, the galvanic isolation by the transformer leads to a duty cycle loss as introduced in Section 3.3. Moreover, parasitic effects can be replicated. To ensure a similar behavior in the frequency domain, the transfer functions are used as design criteria. Voltage-scaled converters have similar transient responses but can differ in their power class.

Another reason to keep the isolated topology of the HV/LV converter is the application of the control. The control strategy can be applied to both the original and the scaled converter. This enables a consistency of the investigations. An alternative approach would be to use dissimilar topologies but to force the transient responses by control parameters. However, the parasitic properties would lead to different responses.

Voltage-Scaling Methodology

The voltage-scaling method of a DC/DC converter follows a conversion according to the following six steps. The stated sequence allows to keep the dynamic properties being defined as the design target.

1. Establishing the Ordinary Differential Equation (ODE) system of the original HV/LV converter to describe the dynamics of the converter (e.g. description of the electrical domain by means of a state-space system).
2. Extracting the transfer characteristics of interest (e.g. control-to-output-voltage, or control-to-inductor-current) by small-signal analysis.
3. Identifying the influence of the voltage on dynamics and transfer characteristics.
4. Calculating the scaling ratio and transferring to physical parameters on the basis of the target voltage of the voltage-scaled converter.
5. Adapting the scaling ratio if infeasible physical parameters arise (e.g. adaption of the DC gain as a compromise).
6. Verifying the scaling results (e.g. by means of frequency domain analysis and a comparison with the original system).

It should be noted that the scaling process is reversible as it can be used to scale the input or the output voltage separately. The voltage-scaling method has been performed on an exemplary PSFB converter. Each single design step for the input voltage-scaling from 400 V to 48 V is described in detail in A.3 and [P7].

Hardware Implementation of a Voltage-Scaled Converter

The exemplary voltage-scaling procedure has been executed and transferred to a 1.5 kW PSFB converter. The results are documented within [S2, S3].

The scaled converter has been implemented in a modular compact design. This allows the integration of multiple converters in a distributed arrangement. A novel control method for distributed converters is documented in Section 5.2. Moreover, high reliability, efficiency and energy density are targeted. Achieving low Electromagnetic Interferences (EMIs) and a small output voltage ripple are also aimed for.

The physical implementation follows the fundamental principles of DC/DC converter designs [171]. Special focus lies on the design of isolated PSFB converters [172, 173].

The transformer has been customized in order to reach replicate the dynamic behavior of the original 400 V/12 V converter. The duty cycle loss d_L mainly depends on the leakage inductance of the transformer. Since higher currents and current slew rates for a voltage-scaled version occur in the primary side, the leakage inductance needs to be particularly small. A planar transformer has been chosen for the design. The small leakage inductance of planar transformers and their design principles are presented in [174].

4.3.3 Modular Design of the Test Bench

The power system test bench contains three modules: the DUT, the controller and ancillaries. The modules are separable for flexibility and upgradability purposes.

The DUT is a LV power system replica. The replica can either be a customized test bench or be substituted by a prototype vehicle. This project designs a test bench based on an upcoming BEV of BMW AG. Its test bench includes the series production wiring harness mounted on an aluminum frame. The attached devices are physical components of the vehicle. Safety-critical and high power components have been selected.

A modular control system is used for several tasks. The controller initiates a certain operating point by a simulation of the environment. By means of a communication bus to the CCU, attached devices are requested to control an internal actuator in a particular way. Moreover, the controller is able to measure distributed voltages and currents at a trigger event. The operation of further ancillaries such as power supplies or electronic loads is influenced by the modular controller, as well.

4.4 Physical Implementation

The test bench concept has been implemented on a BMW iX based DUT. Automated test procedures follow the sequence of five subroutines as visualized in Fig. 4.3.

1. The stationary host initiates a simulation of the environment on the basis of user input. This communication-bus-simulation outputs commands being transmitted via an Ethernet interface to the controller. The controller translates commands into vehicle bus signals (e.g. Controller Area Network (CAN)). Subsequently, the vehicular components receive and run the requested operation. The achievement of the operating point is checked via received bus signals within the communication-bus-simulation.

2. The power system is disturbed by an injected fault (as required). By means of a serial bus, the corresponding hardware prototype receives a command and injects the requested disturbance by controlling its resistance.

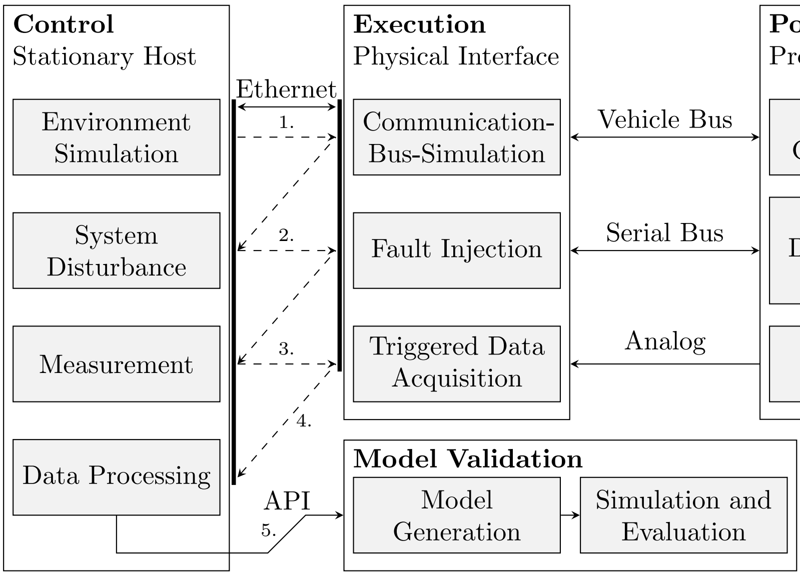


Figure 4.3: Implemented toolchain of the test bench. The block diagram displays the interaction of the control, the execution, the validation with the physical power system.

3. A measurement of all relevant values is performed on a trigger signal. Analog test leads connect the controller with the voltage, current and temperature probes.

4. The measurements are processed. For instance, an analysis in frequency domain is executed or fuse triggering times are evaluated.

5. Processed data is trimmed for the simulation model. A simulation framework is opened via an Application Programming Interface (API). First, the model is generated on the basis of user input. Then, the simulation is carried out with the trimmed stimulation/ disturbance from the system measurement. Subsequently, an automatic simulation of the previously measured scenario takes place. The simulation results and measurement results are contrasted to identify deviations.

The executing interface has been chosen to be a modular measurement instrument from NI®. The software was implemented in LabVIEW® and VeriStand®. The communication-bus-simulation is performed in Vector CAPL® environment. All data processing and simulation preparation jobs are carried out in Python®. The simulation itself runs in Dymola Modelica®. The test bench setup has been published in [P8].

Sequences as shown in Fig. 4.3 can be called automatically. The framework implemented in Python® enables an accurate evaluation and preparation of measurement data.

4.4.1 Measurement Data Acquisition

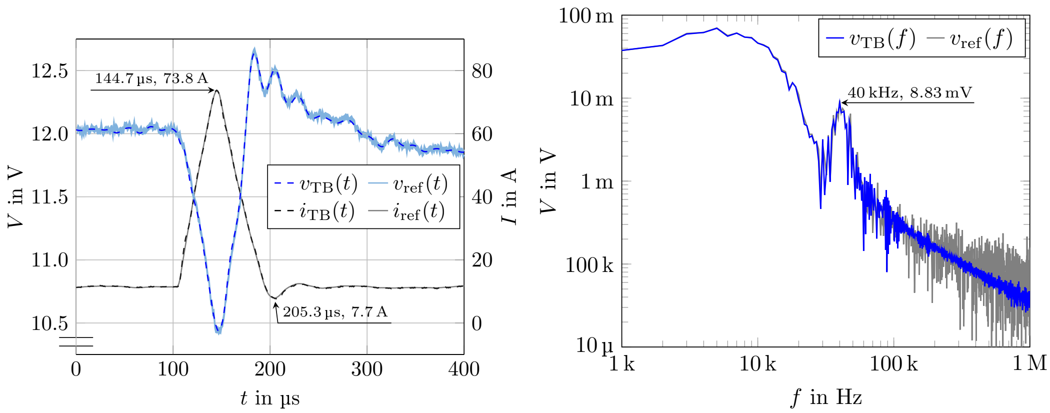
The test bench requirements formulate a minimum bandwidth of 150 kHz. To reach this bandwidth, the modular control instrument has been expanded by 3.5 MS/s Analog-to-Digital Converter (ADC) measurement modules. The measurement module is connected via test leads to the electrical terminals within the test bench.

A differential voltage measurement with capacitive compensation is implemented. The precise calculation of ceramic trim capacitors and the connection setup is visualized in Appendix A.4. The achieved bandwidth for voltage measurements is 500 kHz.

The current is measured with clamp-on current transformer (CCT) probes. Their bandwidth is approximately 150 kHz according to the data sheet [175]. The sampling rate of the measurement system is at least seven times higher than the bandwidth of the voltage and current probes. Thus, signal aliasing errors can be avoided.

A validation of the implemented measurement setup has been carried out. Fig. 4.4 contrasts the measurements with the test bench (TB) to an oscilloscope reference. The comparison shows an electric current pulse and the associated voltage response at an Access Point (AP) within the power system. The reference system is an oscilloscope with a differential 500 MHz voltage probe and a 10 MHz current probe. Its sampling rate is 100 MS/s.

The upper frequency amplitudes are suppressed due to the reduced bandwidth of the measurement system. However, voltages and currents up to 150 kHz can be recorded accurately. The visualized resonance of 8.83 mV at 40 kHz deviates less than 5 % from the reference. Consequently, the measurement system suits the requirements.



(a) Time domain comparison of measurements. **(b)** Frequency domain comparison of voltages.

Figure 4.4: The test bench (TB) measurement setup. Diagrams contrast recorded values with an oscilloscope (ref). Accurate measurements can be obtained up to 150 kHz.

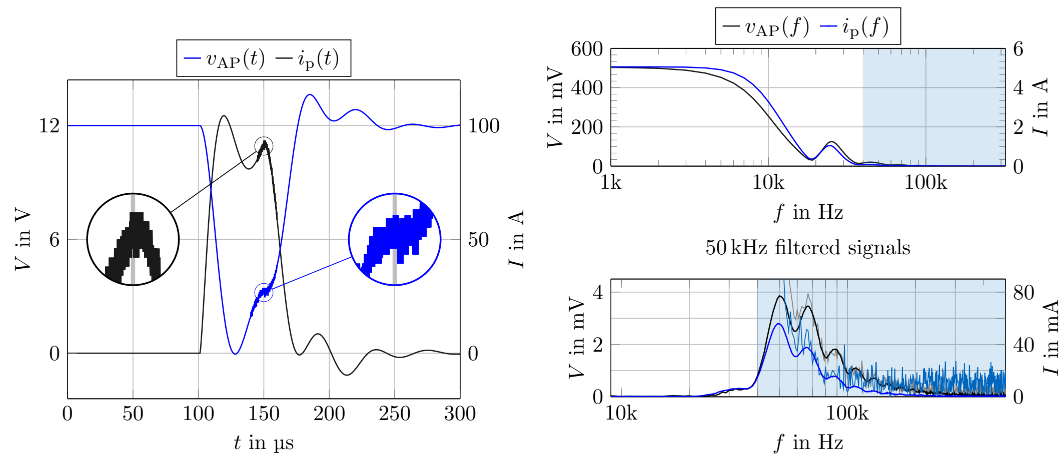
4.4.2 Stimulation of Resonances

Different electronic loads with current slew rates of up to 30 A/ms were industrially produced [176]. Electronic loads were designed for low power [177] and high power applications [178–180]. Other publications name emulators for photovoltaic systems [181] and electric machines [182]. High dynamic load emulators use voltage-controlled audio amplifiers [87]. The injection of S/C pulses via power electronic devices was proposed in [183]. Based on the measured signals, the impedance for a defined AP can be calculated. Multiple current pulses of different pulse lengths were deployed to reduce both stochastic noise.

The method of pulse injection is picked up by a high-dynamic Fault Injection Device (FID) using linear mode controlled MOSFETs. The FID is documented in Appendix A.5. Fig. 4.5 visualizes a current pulse i_p with a width of 50 µs. The pulse is enforced at $t =$100 µs. At the occurrence and the release of the current pulse, the system voltage at an AP v_AP oscillates.

Fig. 4.5a visualizes the time domain behavior of both current and voltage. The signals have an inaccuracy due to measured noise. Beyond, vertical quantization due to the ADCs of the measurement instrument leads to an imprecision. The impedance quality suffers from these disturbances.

In order to reduce the influence of disturbances, the test bench includes high-pass filters. White noise and quantization lead to significant deviations above 50 kHz according to Fig. 4.5b. The quantization inaccuracy can be diminished by enlarging the high-pass filtered signal to the maximum scale of the ADC.



(a) Voltage oscillations in result of an injected 100 A current pulse in an exemplary vehicular power system.

(b) Spectra of current pulse and voltage oscillation. High-frequency components can be obtained accurately using high-pass filters.

Figure 4.5: Measured high-dynamic current pulse injection $i_\mathrm{p}(t)$ at an automotive AP and its amplitude. Using high-pass filters elevates the measurement accuracy above 50 kHz.

The impedance or transfer function at an investigated AP should be obtained in order to analyze system-inherent resonance effects. For the frequency analysis of continuous, periodic signals, the Fourier transform is applied. For continuous, non-periodic signals, the Laplace transform is applied. For discrete, periodic time functions, the Discrete Fourier Transform (DFT) was developed. In addition, a Fast Fourier Transform (FFT) was integrated into the measurement analysis software. This is a particularly effective algorithm for the calculation of the DFT. [184, p. 29] [185, p. 220].

The signals at hand are non-periodic and discretely sampled. The DFT of such signals implicitly assumes that the signal is periodic. This is acceptable when time series signals are aligned at their boundaries. In addition, time series signals are absolutely integrable and can are corrected by the step offset (e.g. $v_{\mathrm{AP}}(t = 0\,\mathrm{s}) = 12\,\mathrm{V}$). [185, p. 203]

In contrast, FFT of signals not being coherent can lead to errors in the frequency domain. Discontinuities at the boundaries of the data set can lead to a pretense of non-realistic frequency bands. Such time series are multiplied by a symmetric weighting sequence (e.g. Hanning, Flattop, Blackman) to achieve a weaker weighting of the data boundaries. The signal smoothly vanishes at the borders. This makes the signal more acceptable for a periodic consideration. [186, pp. 185], [187, pp. 213], [188]

The basis of the applied DFT is given in (4.2). N equally spaced samples of the discretized voltage at the AP $v_{\mathrm{AP}}[k]$ and measured pulse current $i_{\mathrm{p}}[k]$ were recorded, where k represents the integer number of each sample. The Fourier transform $\underline{V}_{\mathrm{AP}}[n], \underline{I}_{\mathrm{p}}[n]$ is calculated according to [185, pp. 207]. Because of symmetry properties, the spectral functions are complex quantities. The value range of the frequencies f associated with the DFT is specified in (4.2) for both odd and even sample counts N. The sampling period is noted as T_{s}. [185, pp. 207]

$$\begin{gathered}
\underline{V}_{\mathrm{AP}}[n] = \sum_{k=0}^{N-1} v_{\mathrm{AP}}[k]\, e^{-j\,2\pi \frac{n}{N} k} \qquad \underline{I}_{\mathrm{p}}[n] = \sum_{k=0}^{N-1} i_{\mathrm{p}}[k]\, e^{-j\,2\pi \frac{n}{N} k} \\
f = \frac{n}{N T_{\mathrm{s}}} \text{ for } \begin{cases} 0 \le n \le \frac{N}{2} - 1 & \text{for } N \in \{2k : k \in \mathbb{Z}\} \\ 0 \le n \le \frac{N-1}{2} & \text{for } N \in \{2k+1 : k \in \mathbb{Z}\} \end{cases}
\end{gathered} \tag{4.2}$$

The ADC resolution of 12 bit enables accurately calculating the system impedance up to 30 kHz out of pulse measurements. Noise can be reduced by averaging multiple measurements. Moreover, averaging three single pulses with different lengths (e.g. 28 µs, 35 µs, 50 µs) elevates the impedance accuracy by about 20 kHz as presented in [P9]. High-pass filtering can further elevate the signal accuracy above 50 kHz. High-amplitude Low-Frequency (LF) signals are filtered out. The remaining signal is scaled according to the maximum resolution of the ADC. A more detailed analysis has been carried out in Appendix A.6. The pulse response analysis helps to stimulate and identify anti-resonances up to 150 kHz. Moreover, (sub-)transient simulation models can be validated.

4.4.3 Modular Structure of the Test Bench

The central element of the test bench is a power system replica. The DUT represents a replica of a future-oriented power system. Included are both safety-critical and comfort consumers. Furthermore, an aluminum BB is provided for high power applications.

Fig. 4.6 shows an abstracted equivalent circuit of the DUT. For simplification, the circuit of the wiring harness does not include mutual coupling. Additionally, components are symbolized as resistors. Distributed converters are represented as voltage sources (Master, Slave 1, Slave 2). Moreover, the individual cable cross-sections are labeled. Each Power Distributor (PD) is displayed as a horizontal busbar. The BB consisting of BBF, BBC, BBR is the 50 mm^2 aluminum power rail connecting the front with the rear.

A Master supply is connected to the main power distributor PD1. Other connected components are the high power consumers EPS, EBP and Electric Fan Drive (EFD). In the front part of the vehicle PD2 is located, which supplies the Electronic Control Units (ECUs) of EPS, EBP and Rear Axle Steering (RAS). Furthermore, the WIP is connected here.

The CCU is supplied via four lines. The load of the ECU is represented as ECU PS, PS1 and PS2. Furthermore, the CCU supplies components such as Headlights (HLi), Taillights (TLi) and rear WIP. The BB connects the front with the rear of the vehicle. There are two more supplies Slave 1 and Slave 2 for voltage stability (see Chapter 5). There are also two more PDs in the rear: PD3 and PD4. High power consumers Audio Power Amplifier (APA) and RAS are attached here.

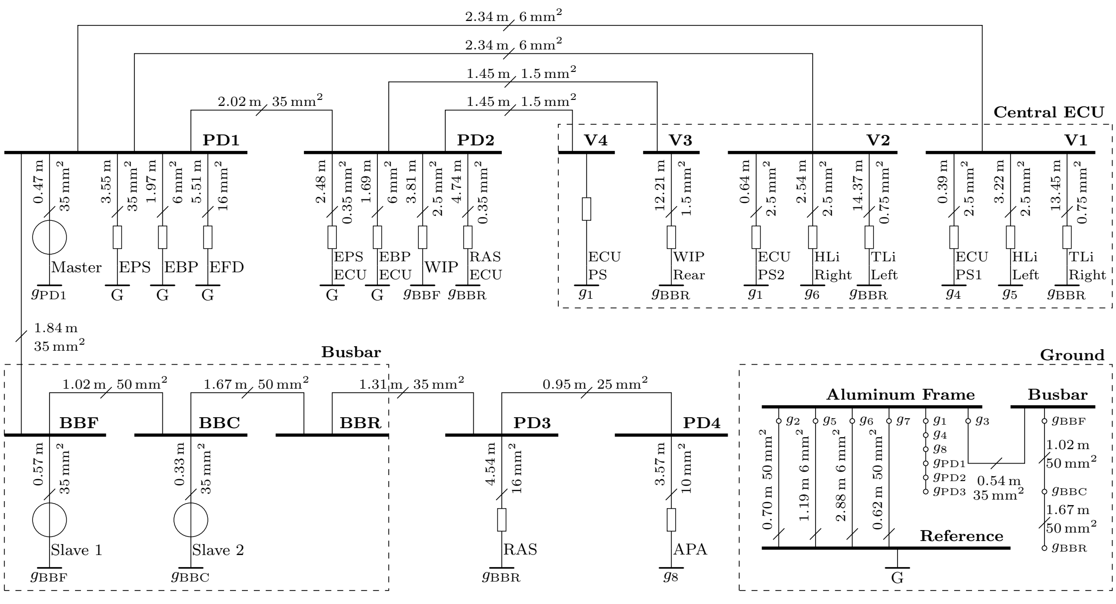
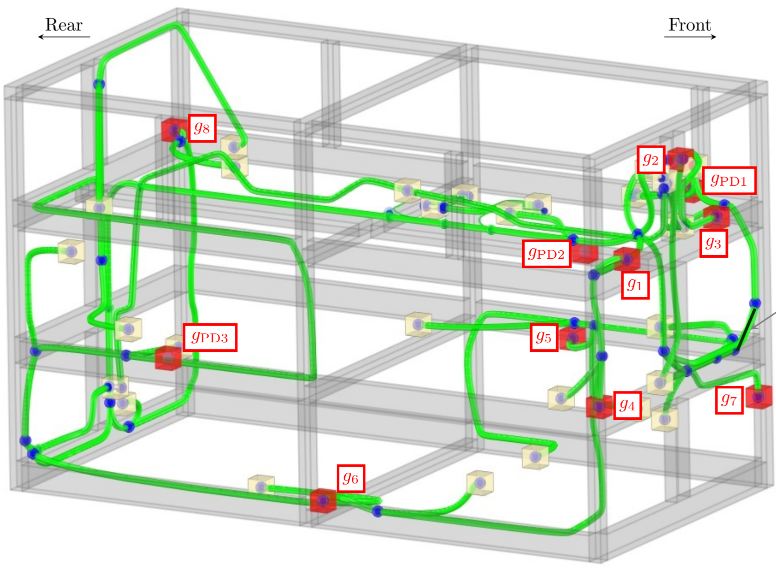


Figure 4.6: Equivalent circuit of the power system test bench. The circuit includes power distributors, vehicular components, multiple supplies and ground connections.

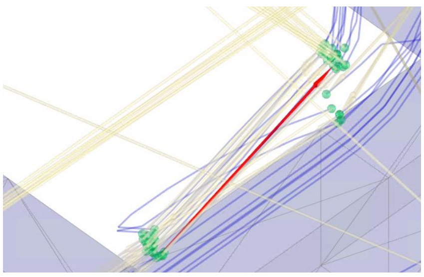
The ground connection to the vehicle body results in a 55 branching network. The number results from a combination $\binom{n}{k}$ of $n = 11$ pins (g_i with $i \in 1...8$, g_{PD1}, g_{PD2}, g_{PD3}) and $k = 2$ pins to be connected. The network is visualized on the bottom right in Fig. 4.6. Additional grounds g_{BBF}, g_{BBC}, g_{BBR} are part of the BB and not directly connected to the frame.

To calculate the wiring harness parameters such as resistances $\mathbf{R}$ and inductance matrix $\mathbf{M}$ of the individual wires, a Finite Element Method (FEM) model has been created using EMCoS®. Fig. 4.7a gives an overview of the DUT. The model includes all relevant power supply cables of the following types with the respective cross-sections:

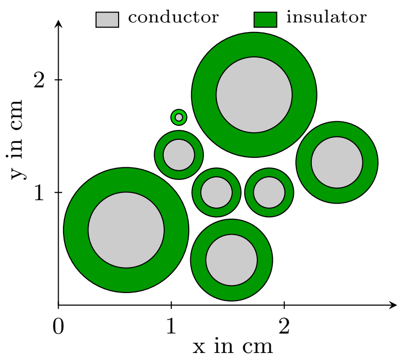
FLR-Y: $\{50, 35, 16, 10, 6, 0.35\}\mathrm{mm}^2$ FLU-Y: $\{2.5, 1.5, 0.75\}\mathrm{mm}^2$ Busbar: $50\,\mathrm{mm}^2$



(a) DUT with highlighted ground pins on the aluminum frame.



(b) The cable bundle b (right of Fig. 4.7a).



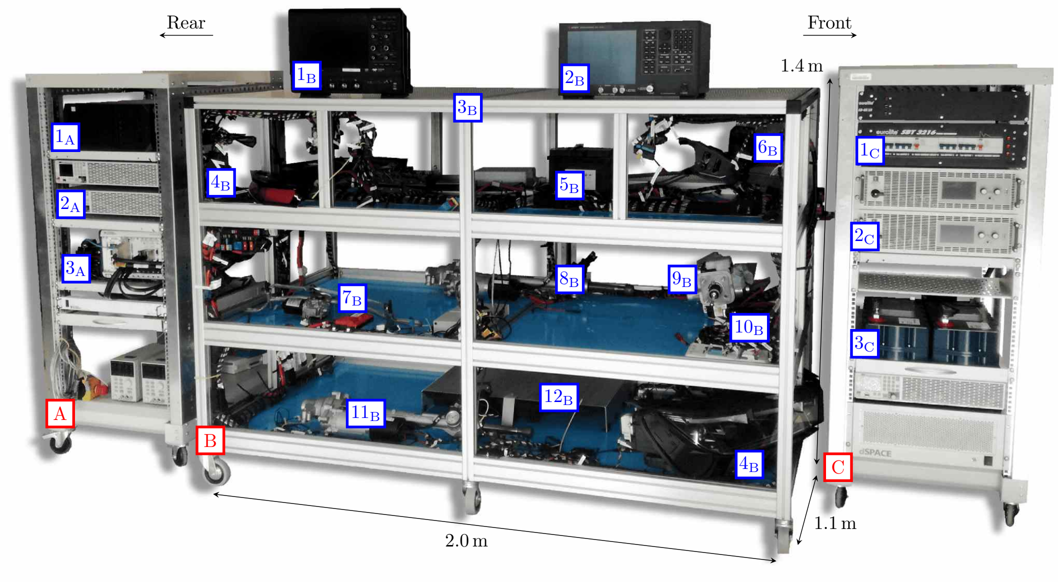
(c) Cross-section of the cable bundle b.

Figure 4.7: The established FEM wiring harness model of the test bench. Detailed views on the cable bundle b in Fig. 4.7a are shown in Fig. 4.7b, 4.7c.

The cable designations above are standardized in DIN ISO 6722 [189, 190]. Selected cables are suitable for automotive purposes and low voltages (less than 60 V) (**FL**x) and are made of copper according to the standards. The insulation material is Polyvinyl Chloride (PVC) (FLx-**Y**). It has a reduced (FL**R**) or greatly reduced thickness (FL**U**). The BB is a customized PVC insulated aluminum conductor.

Fig. 4.7b shows cable bundle b (on the right in Fig. 4.7a). It consists of eight cables with different cross-sections $\{0.35, 4, 16, 35\}\text{mm}^2$ as shown in 4.7c. The corresponding wiring harness model includes both self and mutual inductance according to Section 3.4.2.

The established test bench consists of three modules: the control & acquisition, the DUT and the power supply. The test bench is visualized in Fig. 4.8. Moreover, each module has individual components being described within the table underneath.



A Control & Acquisition		B DUT		C Power Supply	
1_A	Stationary Host	1_B	Oscilloscope	1_C	Circuit Breaker
2_A	Electronic Loads	2_B	Impedance Analyzer	2_C	HV Power Supply
3_A	Modular Instrument	3_B	Aluminum Frame	3_C	Super Capacitor

B: Vehicular Power System Components

4_B	HLi & TLi	7_B	PD3	10_B	CCU
5_B	LV Power Supply	8_B	EPS	11_B	RAS
6_B	PD1	9_B	EBP	12_B	EFD

Figure 4.8: Structure of the power system test bench. The test bench consists of the control & acquisition (A), the DUT (B) and the power supply (C).

The control & acquisition module contains the stationary host (control) and the modular instrument (execution). The DUT is the power system replica. A few safety-critical (such as HLi, TLi, EPS, EBP, RAS) and high power components (such as EFD) are labeled. Moreover, some PDs are highlighted. The power supply contains electronic supply units and Double-Layer Capacitors (DLCs) for the emulation of the HV power system. Detailed photographs and close-ups are attached to Appendix A.4.

4.5 Test Bench Capabilities

This section gives a brief overview of test bench applications. First, the model validation is demonstrated. Then, fault measurements are recorded. Performed investigations focus on the high-dynamic load emulation and disturbances within the system.

4.5.1 Model Validation

The main objective of the power system test bench is to validate transient simulation models from Chapter 3. This section indicates the validation of the wiring harness model and the reduced modeling approach. The causes of occurring deviations are discussed.

Wiring Harness Model Validation

The wiring harness simulation model of the established power system as shown in Fig. 4.6 consists resistances, self- and mutual inductances in form of lumped parameters as presented in Section 3.4.2. The established model is to be validated below.

Fig. 4.9 shows the stimulation of the power system by means of a current pulse with the FID at the AP of the APA. The pulse has a length of 48 µs, an amplitude of 77 A and current slew rate of 2.5 A/µs. Only the Master converter supplies the system. Its maximum current limit is set to 50 A. Other components are physically disconnected. The injected current by the FID is used as a stimulation profile for the simulation model.

The result plot contrasts the simulation results and measurements at the terminals of named components or PDs. A deviation of less than 7 % can be achieved throughout the entire simulation time. For 99 % of the time, the deviation is less than 4 %. The deviation is obtained by opposing simulated voltage (blue) and measurement (grey) for voltages. The deviation of the current is calculated in contrast to 100 A resulting in an equality of 1 % and 1 A of difference.

Furthermore, the simulation results for the power system model without mutual inductances M are contrasted to the established model. A significant impact of mutual inductances on voltages at some APs can be identified. Neglecting M would lead to significant deviations of 14 % (1.3 V) at the EBP or 32 % (2.5 V) at the RAS, for instance.

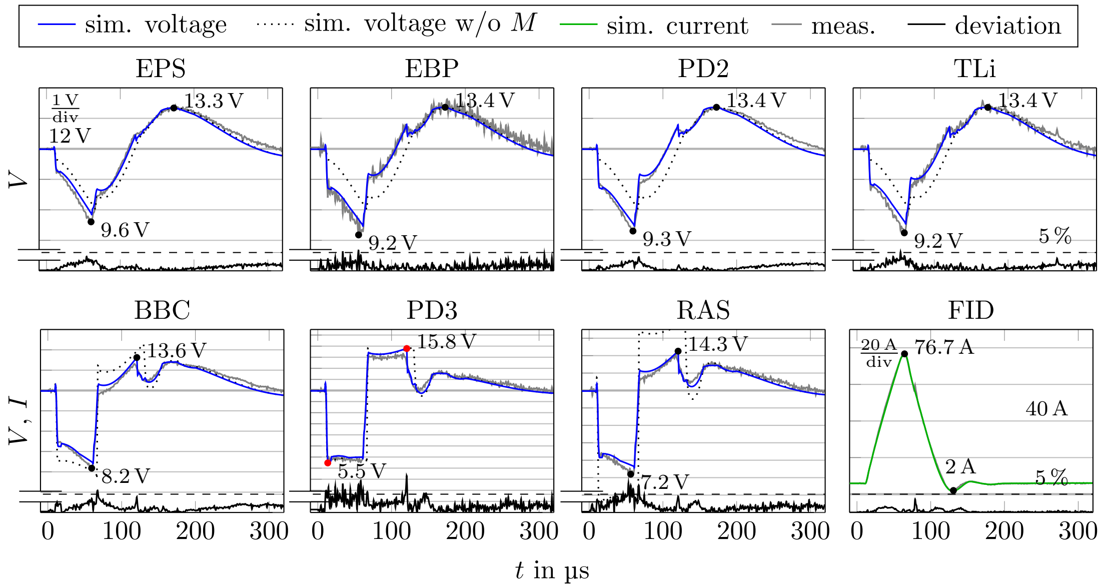


Figure 4.9: Wiring harness model validation: a current pulse is injected at the APA by the FID. Voltage disturbances at open component terminals are stimulated. Measurements are contrasted to the simulation results and to the simulation without mutual coupling M.

Due to the wiring harness geometry, the mutual coupling can stabilize or destabilize the power system. For example, the voltage of the EBP is destabilized. The voltage shows a pronounced drop due to the mutual coupling compared to no coupling. In contrast, the voltage at the RAS is stabilized due to the predominant wiring harness geometry. Without mutual coupling M the voltage would drop as low as 5.5 V (in contrast to 7.2 V). Furthermore, the voltage at the RAS shoots over to 15.8 V without mutual coupling (in contrast to 14.3 V). If there would be no mutual inductance M, the RAS would experience similar voltages as PD3. That's because PD3 is directly connected to the RAS as shown in the equivalent circuit in Fig. 4.6. The impact of mutual inductances is visible at other components and PDs such as the EPS, the TLi, PD2 and BBC.

Reduced Modeling Approach Validation

Another simulation is carried out in order to validate the established power system model with attached components. The Master converter supplies the power system. All components as being stated in Fig. 4.6 are physically connected to the system. During the current pulse injection by the FID at the AP of the APA, a maximum voltage of about 17.1 V and a minimum voltage of 6.4 V are measured at PD3. At the injection and the release deviations at PD3 of about 10 % occur for about 3 µs. On all other components, the deviation is held below 5 % during the entire simulation time.

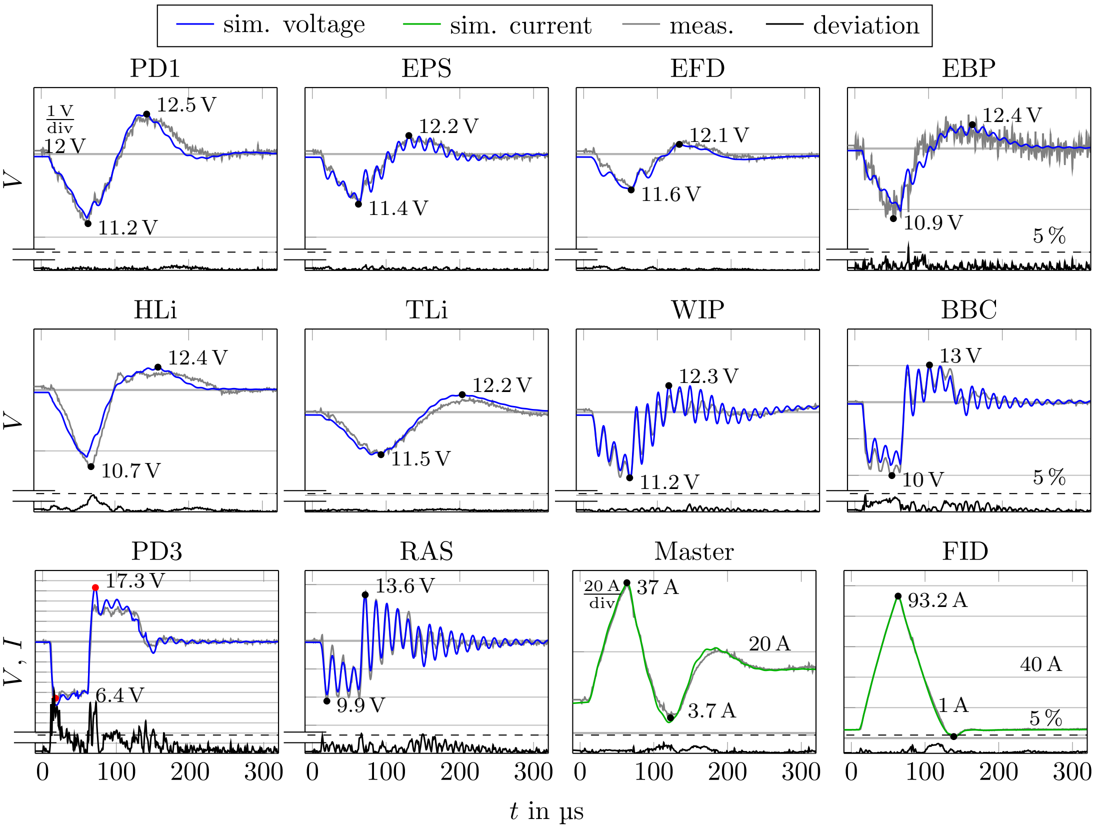


Figure 4.10: Reduced modeling approach validation: a current pulse is injected at the APA by the FID. Simulated voltages at the terminals of attached components are contrasted to measurements.

Fig. 4.10 contrasts simulation results (blue, green) and measurements (grey) of selected components. Currents at the output terminal of the Master converter and the FID are recorded as well. Pronounced oscillations can be observed at components EPS, EFD, WIP and RAS. These oscillations arise due to system-inherent anti-resonances. The oscillations can be reproduced by the simulation model with deviations of less than 5 %.

The current of the Master converter ramps up to 37 A while the injected fault current rises up to 93 A. This difference arises due to distributed capacitors of the components. Their stored energy stabilizes the power system during the transient current pulse.

Deviations can be observed in the Master converter current after $t = 100\,\mu s$. The ECUs have not been modeled within this power system model. Their current demand (below 1 A in total) can not be pictured, therefore. Moreover, a higher damping of the oscillations at the WIP and fewer oscillations at the EPS can be found in the measurements. However, the deviations are below 2 % and are, therefore, not considered as relevant.

Discussion of Deviations

The simulation examples in this section reveal deviations. Major causes are stated in the following. A distinction is made between stochastic and systematic errors.

Stochastic errors arise due to thermal and quantization noise. The power system test bench allows the automated injection of several pulses. This can further be used to increase the confidence. Stochastic errors such as thermal and quantization noise can be reduced to a great extent. A similar approach has been described in Section 4.4.2 for the impedance spectroscopy out of current pulse injections.

However, further systematic deviations between the established power system model and the measurements arise. Deviations mainly come from the uncertainties within the wiring harness model. Deviations in the range of 10 µs to 70 µs occur due to an overestimation of mutual inductances. Thus, simulated voltages of BBC, PD3, RAS are slightly higher (in Fig. 4.9) leading to a deviation of at maximum 7 %. The simulated voltage (with M) is above the measurement and the second simulation without M. An underestimation of mutual inductance is visible at EPS, EBP, PD2 and TLi. Simulated voltages (with M) are located between the measurement and the simulation without M.

The declining current of the FID flows through a Transient Voltage Suppressor (TVS) diode. A simplified model has been used with a fixed clamping and breakdown voltage. Deviations of the measurement setup with respect to voltages can be assumed to be less than 1 % due to the accurate calibration using trim capacitors (see Section 4.4). A deviation of 9 % comes about at 120 µs at PD3 in Fig. 4.9. This happens due to the transition of the TVS diode conduction to the open-loop impedance of the FID. The model of the TVS diode can be identified as the root cause for deviations at this time.

The accuracy of the current measurement influences the simulation results. The simulation model of the current controlled FID uses the measured current as its control reference. The controllable resistor influences the dynamic behavior of the power system. The current probes have a bandwidth of 200 kHz and a sensitivity threshold of 1 A.

To further increase the simulation model accuracy, the model of the TVS diode could be enhanced. The dependence of the clamping voltage with respect to the current could be included. Integrating more precise current probes can also help to improve the accuracy of the model. Multiple measurements have been executed (three measurements and pulse injections). Visualized measurements represent arithmetic average values of recordings. A piece-wise interpolation is applied on the current of the FID to further reduce noise.

4.5.2 Fault Investigation

Two measurements are presented to show the versatility of the test bench. The first measurement visualizes the overload of a single power supply. The second measurement shows a S/C in a power system being supplied by three distributed DC/DC converters.

Overload Measurement

A very high load condition with a single converter-supplied power system is demonstrated. Only, the Master converter supplies the power system. Its maximum saturation current is set to 50 A. The power system is initially burdened with 250 W of load. Such a case can occur, for example, if a load has an unacceptably high power demand or the supply does not meet its power rating (e.g. unavailability of a parallel supply converter).

A high load occurs after the first 5 ms of the measurement in Fig. 4.11. The high load is emulated by the FID at the AP of the APA. The load current rises up to 101.5 A. The load current stays above the current limit of the power supply for more than 50 ms. During this time, the FID is supplied by distributed capacitors. The power supply reduces its voltage during the active current control. This causes a relay to switch off. The relay connects the EFD to the power system. Consequently, a current drop in the load can be observed. The voltage at PDs falls down to 1.6 V at 60 ms.

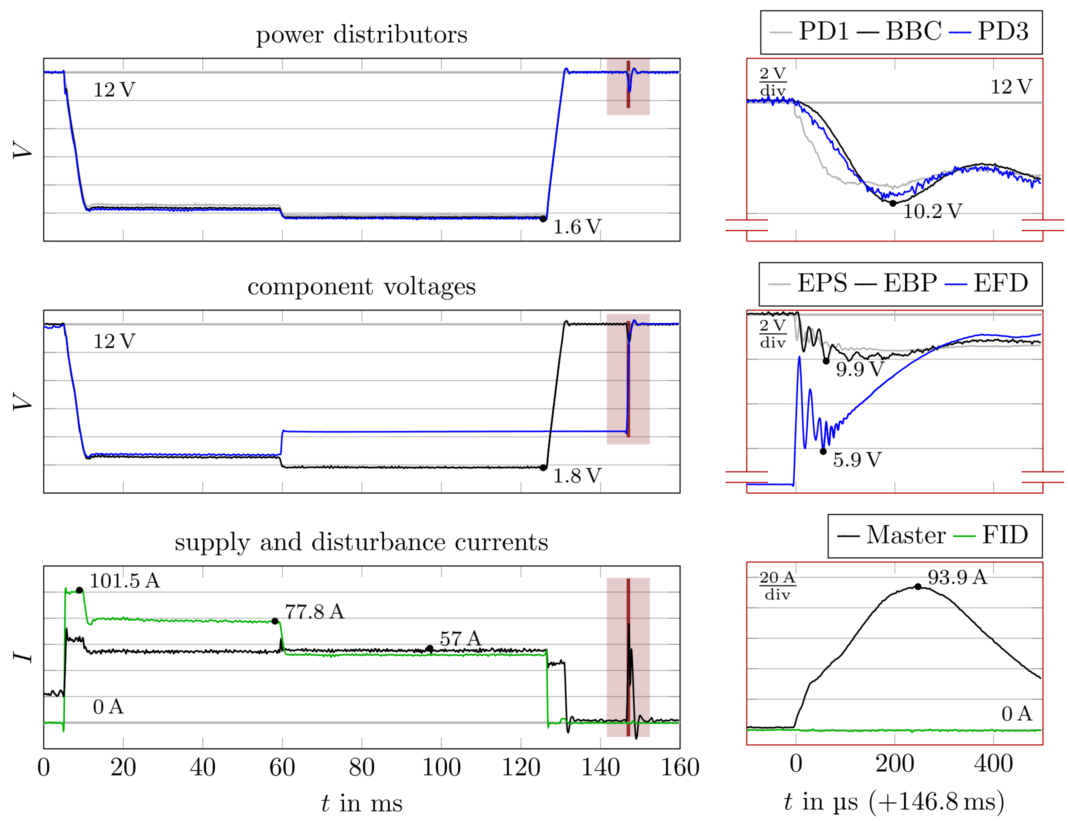


Figure 4.11: Overload measurement: the FID at the terminals of the APA emulates a high load. Measured voltages at the terminals of attached power distributors and components are shown. A relay switches on at 146.8 ms leading to an excessive current and a cross-system voltage drop as magnified on the right.

The load is supplied by the converter operating in its upper current limit. The load switches off at 125 ms. Capacitors within the power system are charged with the maximum current of the supply. A slow voltage increase of about 2 V/ms at t =130 ms is visible.

The relay switches on at 146.8 ms. This event is magnified on the right of Fig. 4.11. Input capacitors of the EFD are charged. This leads to a current of 93.9 A during a transient with a length of 400 µs. Voltages of components such as EPS and EBP are oscillating. The voltage at BBC drops to 10 V when the relay switches on.

Short Circuit Measurement

Fig. 4.12 shows a S/C measurement. The S/C occurs at the component APA and is emulated by means of the FID. Distributed converters operate at their upper current limit. The current of the Master converter is visualized as an example. Voltages at PDs and components drop to 4 V during the S/C.

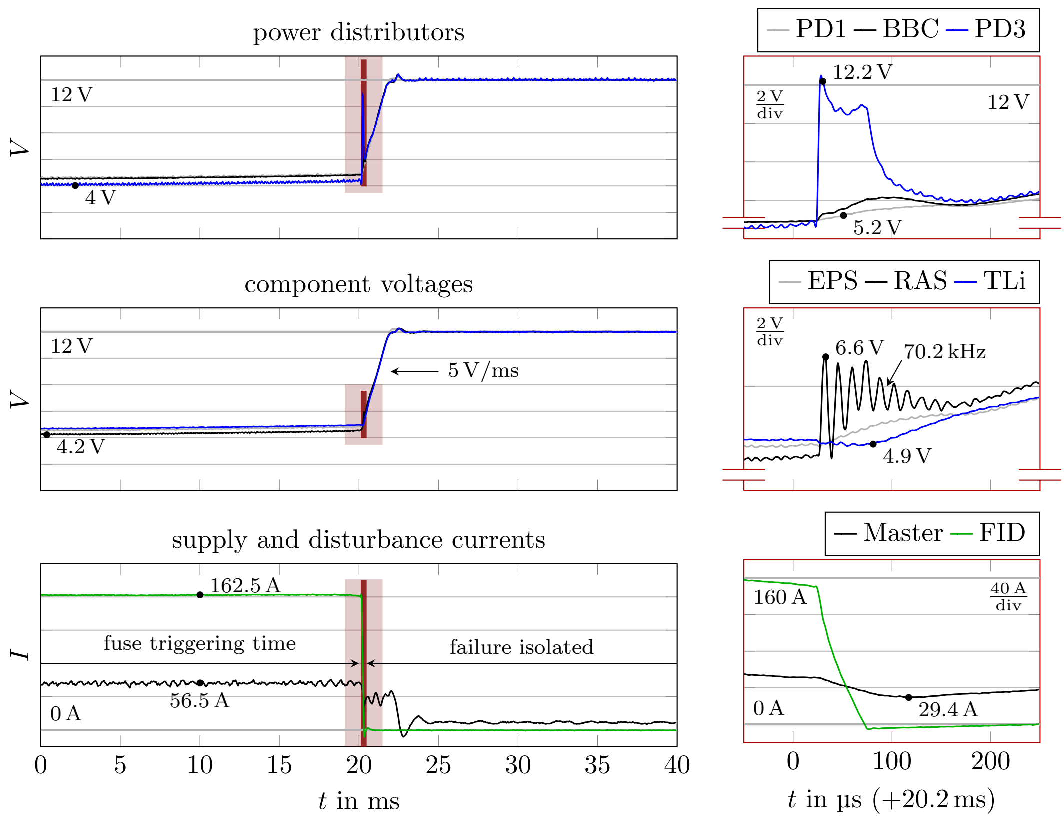


Figure 4.12: S/C measurement: the FID emulates a short circuit at the APA. The melting fuse triggers at 20 ms and isolates the short circuit location. A TVS diode close to PD3 conducts. Corresponding transients are magnified on the right.

At 20.2 ms the melting fuse opens and disconnects the S/C from the power system. The energy stored within the inductance of the power system is discharged within the TVS diode of the FID. The voltage at the closest PD to the FID (PD3) is above 12.2 V for a time of about 70 µs. The voltages at other PDs is about 5.2 V. Thus, a maximum voltage imbalance of 7 V can be observed during this period of time. The corresponding measurements are highlighted in the plots on the right of Fig. 4.12.

The voltage at the terminals of the RAS highly oscillates at a frequency of 70.2 kHz with a peak-to-peak amplitude of 2 V. Other components are not affected. For instance, the EPS does not show a stimulation of anti-resonances. The EPS is connected to PD1.

In contrast, the component TLi is subjected to a small voltage drop of about 200 mV to 4.9 V. This voltage drop occurs due to the power system impedance. A mutual coupling within the wiring harness causes this destabilizing effect.

After the fuse is triggered, the capacitors within the power system are charged back to the reference voltage at the current limit of the converters of approximately 50 A. The voltage slope in this example is about 5 V/ms.

5 Stabilization of Transients

This chapter introduces novel stabilization concepts to suppress system-inherent disturbances. This work limits its scope on transients and subtransients between 1 kHz and 150 kHz. The frequency range is characterized by a pronounced resonant behavior and a strong influence of mutual inductive coupling within the wiring harness. Proposed stabilization measures focus on the adaption of the control of the power supply and the customization of the physical system by integrating adaptive band-pass filters. Further stabilization measures are tabulated in Section 2.2.5.

5.1 Conceptual Design of Stabilization Measures

A provided wiring harness with its Power Distributors (PDs) is used as a design basis. This architecture remains unmodified. In this way, a comparatively low effort can be ensured. High power fluctuations such as Short Circuits (S/Cs) should influence the supply quality of Automotive Safety Integrity Level (ASIL) affiliated components as little as possible.

Two suitable stabilization measures have been identified: distributed non linearly controlled converters and system-designed passive band-pass filters. Their designs have been published in [P10, P11].

Fig. 5.1 shows an application example of introduced stabilization measures to an exemplary tree-structured power system. Three distributed converters are connected to the grid via wiring harness impedances Z_{h}. Automotive components can be assigned to PDs and categorized as safety-critical components according to their individual ASIL or quality consumers Quality Management (QM).

An exemplary disturbance path is highlighted in red. A high dynamic current demand at the component Electric Fan Drive (EFD) ($Z_{1\mathrm{q},1}$) leads to a voltage imbalance at the terminals of ASIL affiliated components. The exemplary component Electric Brake Pump (EBP) ($Z_{1\mathrm{a},1}$) is a potential disturbance receiver. Its terminal voltage oscillates due to the system-inherent resonant behavior. At the worst, the EBP could fail or break down during a high dynamic transient of the EFD.

The suggested stabilization measures are highlighted in blue. PDs contain passive filters Z_{f} being able to suppress disturbances between components. Distributed converters contribute to better voltage stability. The proposed method defines one converter as Master and adjacent converters as Slaves.

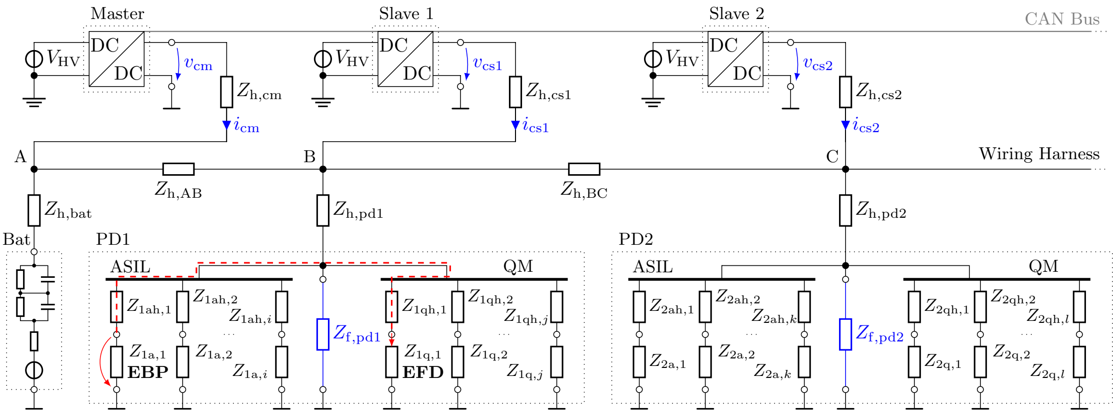


Figure 5.1: Equivalent circuit diagram of a power system with proposed stabilization measures. Distributed converters (Master, Slave 1, Slave 2) supply the system, while system-designed passive filters Z_f within the PDs provide suppression of subtransients.

Tree-structured wiring harnesses have pronounced parasitic inductances as presented in Section 3.4.2. Consequently, the geometry of the wiring harness represents another degree of freedom. A voltage stabilization due to induced voltages during high current slew rates can be achieved by adjusting the geometry. For example, cable bundle associated cables can be reassigned or the cable bundle length can be adjusted. A more in-depth investigation will not be examined in this work.

5.2 Non Linearly Controlled Distributed Converters

Distributed converters secure a reliable power supply of ASIL affiliated components. Their task is to stabilize the voltage level of the grid in order to meet the Safe Operating Area (SOA) of safety-critical components.

Voltage imbalances between nodes occur due to current fluctuations within the wiring harness impedance. Distributed fast controlling of the power supply is introduced. Individual converters switch on or off in dependence of their terminal voltage. Thus, they autonomously change between buck and boost mode to stabilize the power system. In Fig. 5.1, the measured voltages of the converters are highlighted in blue being v_cm, v_cs1, v_cs2. Additionally, multiple converters increase the reliability via redundancy. Available stages can take over the supply in case of a break down.

This section introduces the application of the industry-standard Current Mode Control (CMC) based control method. The preferred Voltage Mode Control (VMC)-based control method Double-Integral Sliding Mode Control (DISMC) and its application to distributed converters are discussed in more detail.

5.2.1 Control Methods

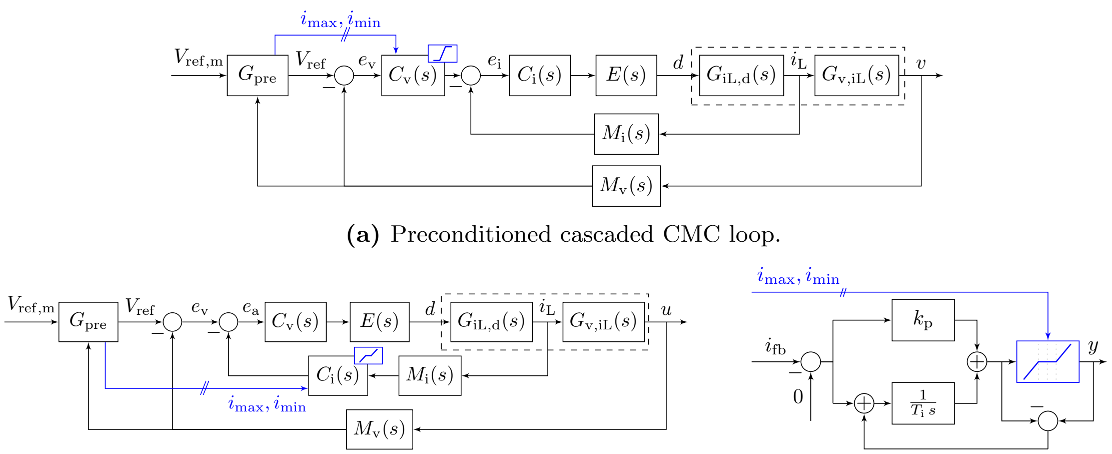
The physical system for the application of the developed control methods is the voltage-scaled Phase-Shifted Full-Bridge (PSFB) converter. Its parameters and design procedure are attached to Appendix A.3.

Its control ensures that the voltage at its terminals v_c follows a predefined reference voltage V_{ref}. Moreover, the output inductor current i_L needs to stay within given limits. This ensures the converter not being overloaded for both power flow directions. Typically, there are current saturation limits. These limits are defined by the specifications of the implemented hardware.

Linear Control

Linear control methods for single-phase buck-derived topologies have been sufficiently investigated within [131, 132]. The industry-standard for the control is the linear CMC.

The cascaded control loop consists of the linear voltage $C_v(s)$ and the current controller $C_i(s)$ as presented in Fig. 5.2a. The measured signals pass feedback delays $M_{i,v}(s)$ due to isolation amplifiers, sensor transfer functions and Analog-to-Digital Converter (ADC) quantization. A Padé-approximated command delay $E(s)$ of the switching time of 10 µs (at 100 kHz) and control paths of the converter $G_{iL,d}(s)$, $G_{v,iL}(s)$ are included in the control loop. The specific equations for the control paths are introduced in Appendix A.3. A detailed design procedure of the CMC is shown in [P10].



(a) Preconditioned cascaded CMC loop.

(b) Preconditioned cascaded VMC loop.

(c) Current control with deadzone anti-windup for VMC control.

Figure 5.2: Preconditioned CMC and deadzone-compensated VMC-based control for distributed converters.

Nonlinear Control

Another approach is the usage of nonlinear control methods. Wang and Gao [142, 143] proposed Sliding Mode Control (SMC) for buck-derived converter topologies. Their method is applied to the distributed converters. The applied method on the PSFB converter is briefly summarized in Appendix A.7 and Publication [P10].

The SMC based control method uses VMC. In order to ensure the consideration of current limits, a current control $C_{\mathrm{i}}(s)$ has been integrated within the feedback loop as demonstrated in Fig. 5.2b. The current controller has a deadzone-type anti-windup with a linear PI control design. Fig. 5.2c shows the structure of the current controller $C_{\mathrm{i}}(s)$. It clamps its output to 0 for measured currents in the permitted range of $i_{\mathrm{min}} \leq i_{\mathrm{L}} \leq i_{\mathrm{max}}$.

The behavior of the designed DISMC favors the dynamic response of the converter. Fig. 5.3 shows the measured and the simulated dynamic responses of the converter to transient power fluctuations of about 1/4 kW, 1/2 kW and 1 kW. Injected power fluctuations have a respective duration of 600 µs. The emulated load by the Fault Injection Device (FID) is switched off between the pulses. The current slew rate of the injected high dynamic load pulses is approximately 3 A/µs.

The performance of the controller is contrasted to the Open-Loop (O/L) system (dotted line). Publication [P10] further contrasts the performance of industry-standard designed linear VMC and CMC control methods. Especially, settling time and voltage overshoot can be perceptibly improved by using the proposed DISMC.

Additionally, Fig. 5.3 offers a validation of the controlled state-space average simulation model. The transient response of the converter can be simulated with a maximum deviation of about 2.7 % (for the most part being less than 2 %).

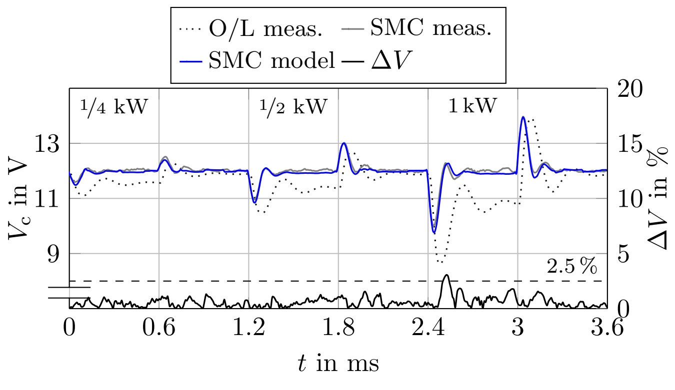


Figure 5.3: State-space average model voltage response in contrast to measurements in the physical system resulting from high dynamic load pulse injections of about 1/4 kW, 1/2 kW and 1 kW. The figure shows the voltage responses for the O/L and the SMC controlled voltage-scaled PSFB converter.

5.2.2 Master-Slave Control for Distributed Converters

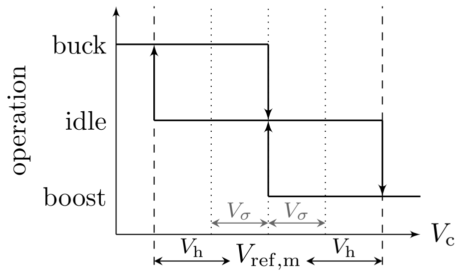
As shown in Fig. 5.2 both CMC and VMC based control methods can be applied to buck-derived converters with consideration of current limits and voltage references. A preconditioning function G_{pre} for the voltage reference V_{ref} is introduced as shown in Fig. 5.2a and 5.2b. This is the key element to enable the parallel operation of the distributed converters for both CMC and VMC control methods.

The Master converter holds $V_{\text{ref}} = V_{\text{ref,m}}$ as voltage reference. On the contrary, V_{ref} of the Slave converters is defined on the basis of (5.1). The reference of the Master converter $V_{\text{ref,m}}$ and the individual measured voltage V_{c} are used to define the control targets. The Master reference voltage $V_{\text{ref,m}}$ can either be chosen to be a default value or be transmitted via a Controller Area Network (CAN) bus as indicated in Fig. 5.1. The default value or the last received value is preferred in case of an interrupted communication.

The logic for the definition of individual operation of each Slave follows a double hysteresis as shown in Fig. 5.4. Hysteresis voltage V_{h} and the master reference voltage $V_{\text{ref,m}}$ define the switch-on points of single Slave converters. The reference is defined with margin V_σ. The margin follows the convention $0 < V_\sigma < V_{\text{h}}$. Both hysteresis and margin are introduced to avoid control instability and circulating currents between parallel converters.

Additionally, the preconditioning function G_{pre} defines the saturation limits of the electric current anti-windup. The respective anti-windup is highlighted in blue in Fig. 5.2a and 5.2b. The specific Slave converter is allowed to operate in boost mode for $i_{\text{min}} < 0$ and in buck mode for $i_{\text{max}} > 0$. Otherwise, it operates in idle mode.

Consequently, the measured v_{c} and the Master reference voltage $V_{\text{ref,m}}$ (being transmitted or default set) determine the operation of the Slave converters. Applied parameters to the prototypes: $V_{\text{ref,m}} = 12\,\text{V}, V_\sigma = 0.5\,\text{V}$, $V_{\text{h}} = 1\,\text{V}, i_{\text{max}} = 50\,\text{A}, i_{\text{min}} = -50\,\text{A}$.



$$\left[V_{\text{ref}}, \boldsymbol{i}_{\text{sat}}{}^\top\right] = \begin{cases} [V_{\text{ref,m}} - V_\sigma, 0, i_{\text{max}}] & \text{for buck} \\ [V_{\text{ref,m}}, 0, 0] & \text{for idle} \\ [V_{\text{ref,m}} + V_\sigma, i_{\text{min}}, 0] & \text{for boost} \end{cases} \tag{5.1}$$

Figure 5.4: Double hysteresis for the adjustment of operation of Slave converters based on the individual measured output voltage v_{c}.

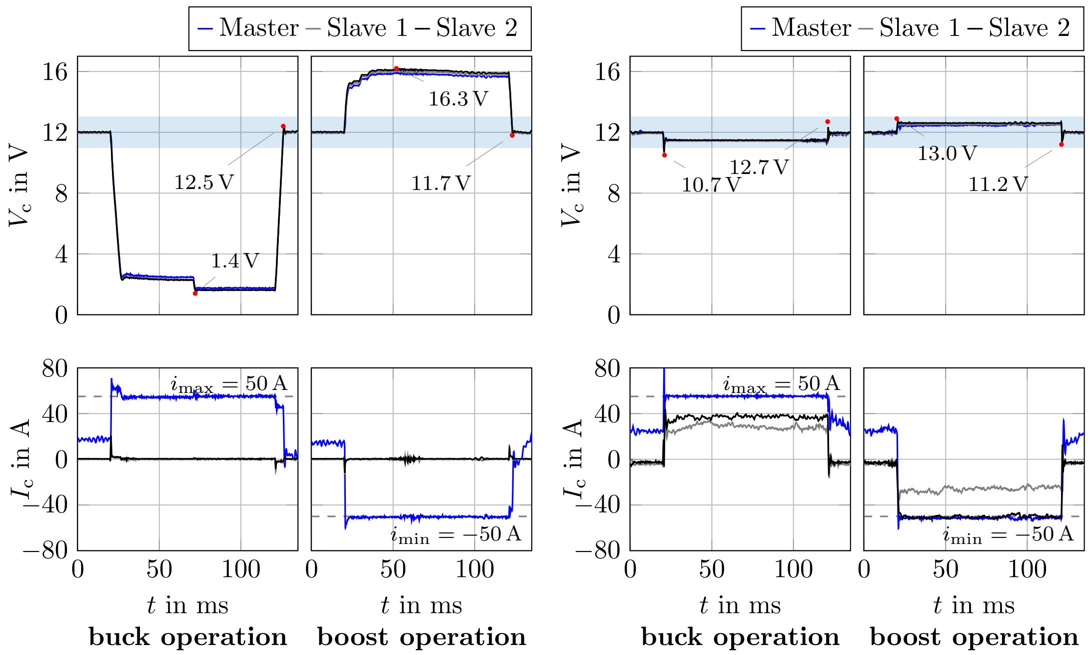
5.2.3 Contribution to Voltage Stabilization

Test bench measurements have been carried out to analyze the contribution of distributed converters to voltage stabilization.

Fig. 5.5 compares the operation of a single converter and distributed converters as introduced above. The terminal voltages and the output currents of a single converter-in operation are shown in Fig. 5.5a. Three distributed converters run in parallel in Fig. 5.5b. The converters are subjected to current-controlled pulse injections of 100 A with a length of 100 ms.

Distributed converters can reduce the voltage imbalances for both demonstrated conditions. One reason is exceeding the current limit of the single converter. In buck mode, the terminal voltages are at minimum 10.7 V for distributed converters while they are 1.4 V for a single converter.

In boost mode, the excessive voltage for the single Master converter amounts to 16.3 V, while three distributed converters can effectively limit the voltage to 13 V. An excessive voltage within the power system is achieved by means of a charged 80 F Double-Layer Capacitor (DLC) being connected to the power system by means of electronic switches.



(a) Master converter in operation with switched off Slaves connected.

(b) Three converters operating in parallel (Master, Slave 1 and Slave 2).

Figure 5.5: Comparison of power system voltages for single and distributed converters operating in buck and boost mode. The results are obtained from measurements within the vehicular test bench introduced in Chapter 4.

5.3 System-Oriented Passive Filter Design

The system-inherent resonant behavior is adjusted by system-designed passive band-pass filters. They are integrated in PDs as introduced in Fig. 5.1.

5.3.1 Passive Filter Topology and Physical Components

An investigation on different filter topologies such as c-type, shunt and band-pass filters was carried out in [S1]. The band-pass filter has been selected as a suitable topology. A selective adjustment in the frequency range can be implemented without affecting the low or high frequency behavior of the power system. They are specifically designed for frequencies from 10 kHz to 150 kHz. This ensures that they are effective for subtransients only. Lower frequency transients due to the control behavior of components will not be adapted by the band-pass filters. AN excessive energy dissipation can be avoided.

The proposed circuit includes switchable parallel band-pass filter stages as shown in Fig. 5.6. To reach a low impedance connection to the respective PD, the filter circuit is connected via an electronic fuse Q_{fuse}. The exemplary topology is back-to-back in order to block fault currents from both directions. A Transient Voltage Suppressor (TVS) diode D_1 ensures the protection of capacitors and switches Q_i with $i \in \{1, 2, k\}$.

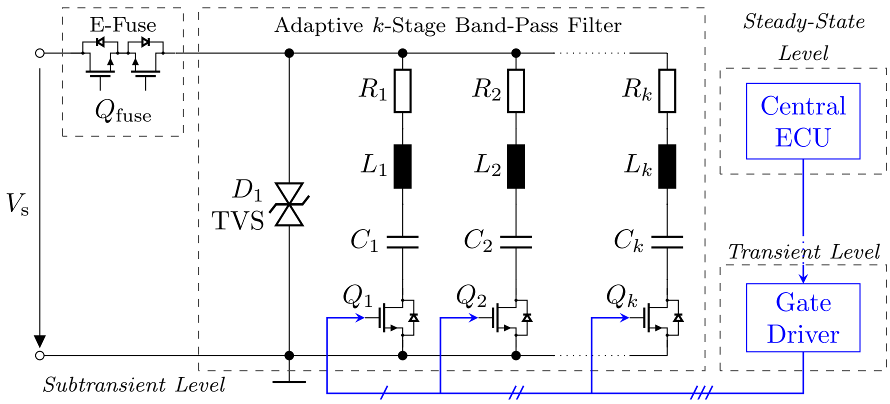


Figure 5.6: Equivalent circuit diagram of the adaptive k-stage band-pass filter. The filter stages are controlled by the corresponding gate driver units. Logical signals are provided by a central Electronic Control Unit (ECU) on a communication bus.

The MOSFETs Q_i are able to connect a respective band-pass filter stage to the power system. Their gate drivers receive the commands from the central ECU. Due to its possibility of short-term intervention, the gate driver belongs to the transient level. The central ECU decides which filter stage to connect or disconnect. This decision is based on the current system state. For example, connecting a redundant Low Voltage (LV) power system changes the transfer function between disturbance and receivers. Thus, the filter needs to be adapted.

Another possibility for different system states arises due to system integrated relays or electronic fuses. These switching devices connect or disconnect individual components. This could have an influence on the transfer function as well. Since the central ECU is connected via an automotive bus with the transceiver on the filter Printed Circuit Board (PCB), this interaction corresponds to the steady-state level according to Section 2.2.2.

The subtransient level includes all band-pass filter stages, the electronic fuse and the TVS diode. The filter does not require an elevated switching frequency for MOSFETs. The state of the power system changes at large intervals. Thus, the gate driver is chosen to be a driver circuit with a pull-up resistor and active-low logic. Its supply is implemented by means of a low-dropout regulator being connected to the power system.

The PCB implementation of the adaptive band-pass filter is shown in Fig. 5.7. Three parallel stages are installed. Two filter stages are equipped with the respective components. Zero ohm resistors bridge empty contacts.

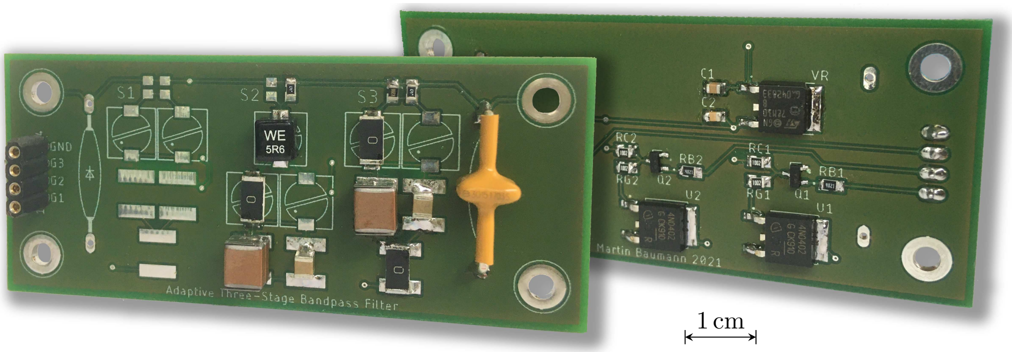


Figure 5.7: Adaptive three-stage band-pass filter PCB implementation. The top layer (left) includes two filter stages being assembled and a TVS diode. The bottom layer (right) shows corresponding MOSFETs with their gate circuitry and power supply. Individual stages can be switched by TTL signals.

The parameters of series-connected filter components depend on the impedance of the power system. Components with minimum parasitic resistance are chosen. Capacitors and inductors should have a small sensitivity with respect to frequencies below 150 kHz. For capacitors, multi-layer ceramic versions are preferred. They have comparably high lifetimes, a small Equivalent Series Resistance (ESR), reduced geometric dimensions and no polarity. Therefore, they are able to withstand positive and negative voltages. However, multi-layer ceramic capacitors are only available up to 100 µF with consideration of the voltages of 32 V. These voltages can occur in the vehicular LV power systems according to DIN 7637 [73]. If bigger capacitors are needed, a parallel connection of ceramic capacitors on the PCB is intended. Moreover, ceramic capacitors are preferred due to their low ESR and their comparatively stable capacitance with increasing frequency. Only above the frequency of 1 MHz the inductive parasitic has a significant influence on the impedance. Aluminum polymer capacitors are considered as an alternative.

Fig. 5.8a shows the measured impedance of selected capacitors. The bigger the capacitance, the more significant the influence of the parasitic inductance. The smaller the capacitance, the more suitable for passive filters. The frequency of interest is below 150 kHz (highlighted in blue). Multi-layer ceramic capacitors show an influence of the inductance above 150 kHz. The measurement method for the data generation is accurate for an impedance above 10 mΩ. Therefore, uncertainties around the resonance frequencies can be detected. All selected capacitors are listed in Tab. 5.1b.

As for the inductors, components WE-HCM and WE-HCI manufactured by Würth Elektronik are chosen. Their high current ratings and their anti-resonance frequencies above 10 MHz are the decisive arguments for their suitability. However, bigger inductances also have larger series resistances as shown in Tab. 5.1c. Fig. 5.8b demonstrates data sheet values of selected inductors. The anti-resonance frequency f_{AR} is the frequency at which the dominating behavior changes. Above that frequency, the component is dominated by capacitive behavior. Below f_{AR} a model of Direct-Current-Resistance (DCR) resistance R_{L} and inductance L is sufficient.

An additional series resistance can be added to the band-pass filter stage. Selected resistances are listed in Tab. 5.1a. The MOSFETs are selected to be Infineon Technologies IPD100N04S4-02 OptiMOS-T2. Their drain-source resistance is as low as 2 mΩ.

Manufacturer	Panasonic Corporation, Vishay Intertechnology											
Package	0805											
R in mΩ	0	1	2	5	6.8	10	20	50	100	200	470	1000

(a) Parameters of twelve selected resistors with 0805 packaging.

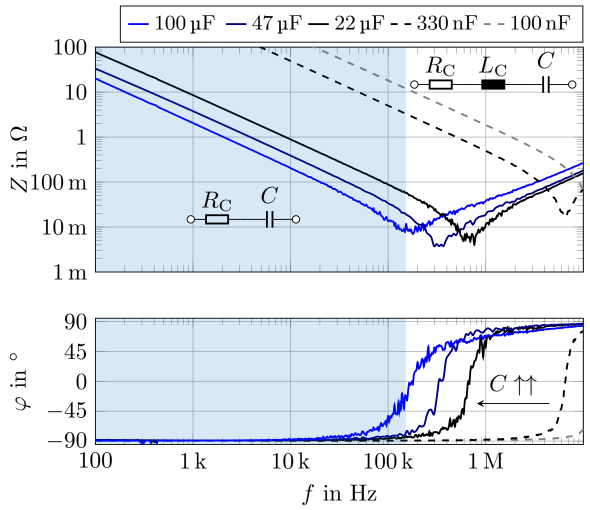
Manufacturer	KEMET, Samsung Electronics, TDK						Würth Elektronik		
Package	0805	0805	1210	1210	1206	2220	SMD radial		
Voltage in V	50			25		16	25		
Type	MLCC						Al-Polymer		
C in µF	0.1	0.33	10	22	47	100	47	100	220
ESR in mΩ	10	10	6	5	3	2	15	15	15

(b) Parameters of nine selected capacitors. Both MLCC and aluminum-polymer types are used.

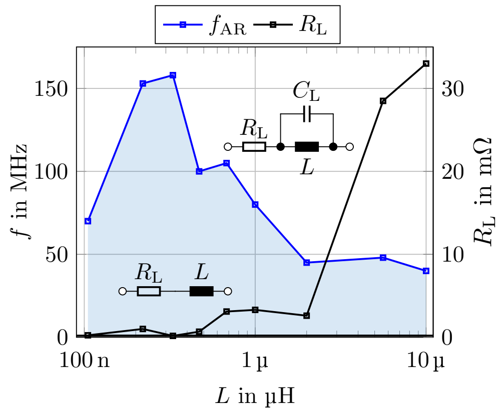
Manufacturer	Würth Elektronik								
Package	7050	1040	1390	1365	7040	1040	1365	5040	7050
L in µH	0.105	0.22	0.33	0.47	0.68	1	2	5.6	10
DCR in mΩ	0.235	0.8	0.165	0.67	3.1	3.3	2.6	28.5	33

(c) Parameters of nine selected inductors being sorted in ascending order by inductance.

Table 5.1: Data sheet parameters of passive components used for the adaptive passive filters.



(a) Multi-layer ceramic capacitors are modeled as an ESR in series with a capacitance below 150 kHz.



(b) Data sheet anti-resonance frequencies of selected inductors. They can be modeled as series connection of DCR and inductance below 1 MHz.

Figure 5.8: Parasitic properties of selected band-pass filter components.

5.3.2 Algorithmic Filter Design

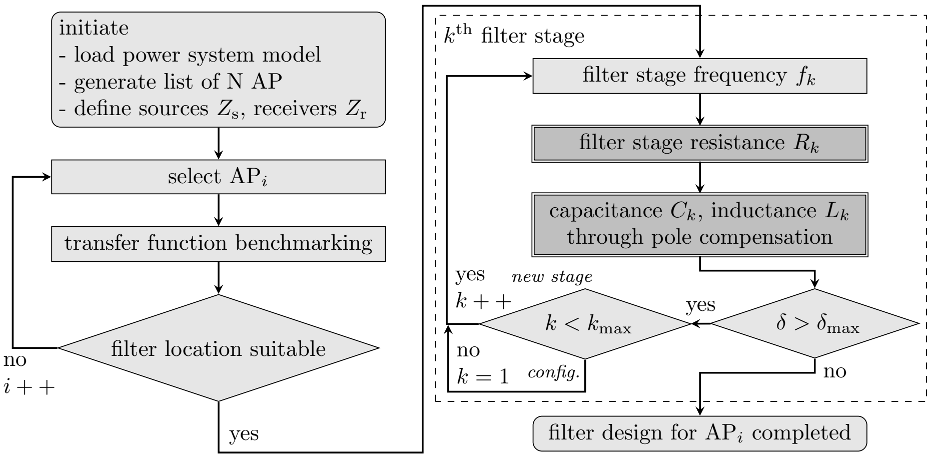
An algorithm has been designed to parameterize the band-pass filter stages. The entire filter design algorithm is visualized in Fig. 5.9. The prerequisite is the model description of the power system to be stabilized. For example, the power system can be described as an Ordinary Differential Equation (ODE) system or with a numerical simulation model.

First, the power system model is loaded. Access Points (APs) for a filter are generated. Advantageous APs are all PDs. Filters can effortlessly be installed since the space in the vehicle is already available. PDs are located directly in the supply path of the components. Thus, there will be an impact on the resonant behavior. During the initialization, potential disturbance paths are generated. For that, disturbance sources and susceptible receivers or safety-critical ASIL components are examined.

One of the APs is chosen. Ideal transfer functions between disturbance sources and receivers are calculated. This benchmark calculation is carried out by using a DLC (e.g. 1 F, 1 mΩ). The AP is suitable as a filter AP if a reduction of the amplitude at the anti-resonance frequencies of transfer functions can be achieved. This check might reveal any unfavorable mutual coupling within the wiring harness with respect to the AP.

Band-pass filter parameters are calculated. The first filter stage is designed to diminish the anti-resonance. The amplitude is adjusted close to the benchmark result of the DLC. If positive deviations occur from the initial transfer functions, further filter stages are calculated. In this context, positive deviations indicate a worse result compared to the initial state. For instance, installing one filter stage can cause a new anti-resonance at a lower frequency. This can be reversed by adding further filter stages.

The filter design is completed once the maximum number of filter stages $k_{\max}$ has been created. Another reason to terminate occurs when achieving positive deviations from the initial state below a defined tolerance $\delta_{\max}$. [P11]



**new stage*: new filter stage is created
**config.*: new filter configuration is targeted (change of target capacitance or smaller damping)

Figure 5.9: Flowchart of the filter design algorithm.

An exemplary filter impedance is visualized in Fig. 5.10. The filter design algorithm yields the filter impedance Z_f for the transfer function $Z_{s\to r}$. Two filter stages have been designed in order to reduce the anti-resonance amplitude at f_1 =32 kHz to the benchmark result. A reduction of the amplitude by 92 % can be achieved. The damping comes along with a shift to higher frequencies as visualized (e.g. 37 kHz). The second filter stage at frequency f_2 reaches a positive deviation from the initial transfer function $Z_{s\to r}$ of less than $\delta_{\max}$. The transfer functions result is named $Z^f_{s\to r}$.

Filter Stage Frequency

The filter stages are designed to dampen anti-resonances from 10 kHz to 150 kHz. A differentiation is carried out between three transfer functions Z_{init} (initial impedance), Z_{ideal} (ideally damped by 1 F DLC, benchmark result) and Z_{filtered} (filtered impedance with integrated filter). In order to identify relevant frequencies, step responses of transfer functions $Z(j\,2\pi f)$ are examined. This allows a worst-case transient stimulation of anti-resonances. A unit step response is equivalent to a current step of 1 A. The resulting voltages $v(j\,2\pi f)$ are used to define the filter stage frequency.

The first filter stage ($k = 1$) attempts to reach Z_{ideal}. Its frequency f_1 is identified with the maximum damping $\max\{V_{\text{init}}(j\,2\pi f) - V_{\text{ideal}}(j\,2\pi f)\}$. The filter has its maximum influence on the transfer function at the determined frequency. More damping cannot be achieved, because the benchmark result represents an ideal voltage stabilization.

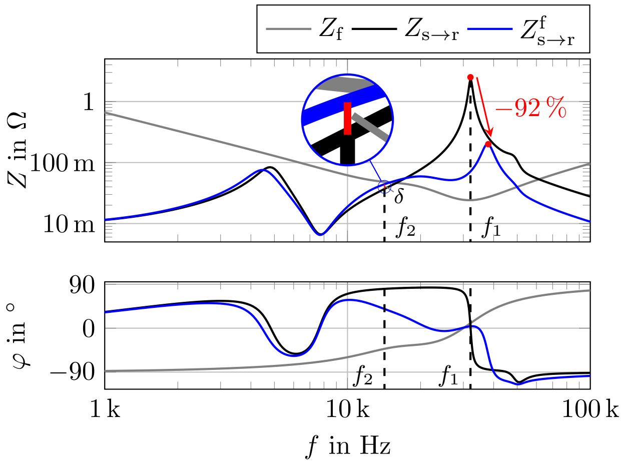


Figure 5.10: The exemplary calculated two-stage passive filter reduces the amplitude of the anti-resonance by 92 %. The original transfer function between disturbance source and receiver $Z_{\mathrm{s}\to\mathrm{r}}$ is modified to $Z^{\mathrm{f}}_{\mathrm{s}\to\mathrm{r}}$. Filter stages frequencies are f_1, f_2.

Further filter stages $(k+1)$ are designed to reach a compensation of positive deviations from Z_init. The corresponding frequency is identified by $\max\{V_\mathrm{init}(j\,2\pi f) - V_\mathrm{filtered}(j\,2\pi f)\}$. If the detected deviation exceeds δ_max (e.g. 5 %), a new filter stage is added with the corresponding frequency. This ensures the creation of an effective stabilization measure without exceeding the initial state.

Filter Stage Resistance

For the calculation of the filter stage resistance, a distinction is made between the first and further filter stages. An iterative approach with initial estimations is used.

The **first filter stage** uses the absolute value of the ideal transfer function as the initial filter stage resistance $R_1 = |Z_\mathrm{ideal}(j\,2\pi f_1)|$ at the identified frequency f_1. The resistance is gradually decreased until a deviation of δ_max between $V_\mathrm{filtered}(f_1)$ and $V_\mathrm{ideal}(f_1)$ is observed. If the initial resistance is chosen too small, the initial deviation is smaller than δ_max. In this case the resistance is increased. Resistance values are adapted using the discrete resistance values of selected components from Tab. 5.1a.

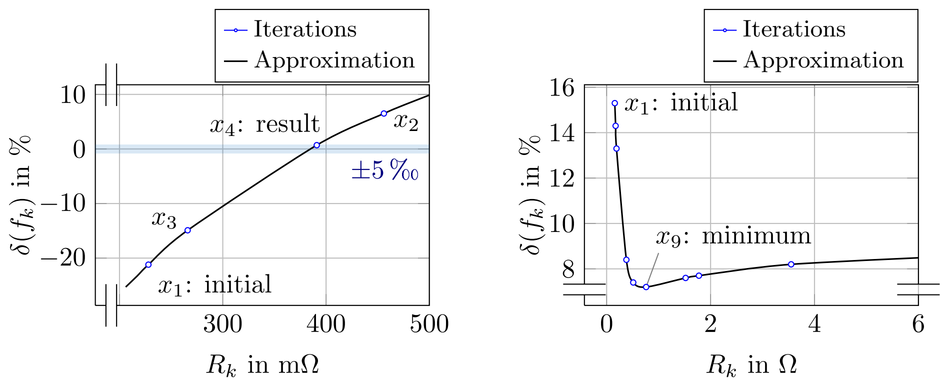
The reason for not decreasing the resistance further is the generation of low-frequency deviations. Smaller resistances lead to higher positive deviations at lower frequencies. Further filter stages would, therefore, have to be designed for an elevated power loss. Rather, an optimal resistance can be observed as shown in Fig. 5.11b. This resistance leads to minimum leftover deviations δ.

Further filter stages use Z_{init} for the initial resistance estimation $R_{\text{k+1}} = |Z_{\text{init}}(j2\pi f_k)|$. The resistance is calculated by means of a n-order polynomial approximation. Fig. 5.11a shows an exemplary approximation with a second-order polynomial. Initially, three iterations have been executed x_1, x_2, x_3. The result of x_4 is obtained by a second-order polynomial and the calculation of its zeros. A tolerance of $\pm 5\,‰$ is introduced. Thus, the numerical iterations of reaching the result can be limited. Numerous examples resulted in a sufficient accuracy using three initial resistances and calculating the target resistance by a second-order polynomial $\delta(f)$ being shown in (5.2).

$$\delta(f) = K_1\,R(f)^2 + K_2\,R(f) + K_3 \tag{5.2}$$

Parameters K_1, K_2, K_3 are solved with the auxiliary variable K_4 and test points (R_1, δ_1), (R_2, δ_2), (R_3, δ_3) as shown in (5.3). Test points are obtained by the three iterations.

$$\begin{aligned} K_1 &= \frac{(\delta_1 - \delta_2) - K_4\,(\delta_1 - \delta_3)}{(R_1^2 - R_2^2) - K_4\,(R_1^2 - R_3^2)} & \qquad K_2 &= \frac{(\delta_1 - \delta_3) - K_1\,(R_1^2 - R_3^2)}{R_1 - R_3} \\ K_3 &= \delta_1 - K_1\,R_1^2 - K_2\,R_1 & K_4 &= \frac{R_1 - R_2}{R_1 - R_3} \end{aligned} \tag{5.3}$$



(a) A second-order polynom is used to approximate the resistance of further filter stages (k^{th} filter stage).

(b) The resistance of the stabilization constraint approach is calculated by striving for the smallest δ.

Figure 5.11: The filter resistance is calculated with estimations and polynomial approximations.

Filter Stage Capacitance

The choice of capacitance and inductance has a significant influence on the impedance of the filter. The smaller the capacitance, the more selective the filter. Thus, a smaller frequency range is influenced by the designed filter stage. In contrast, a big capacitance leads to better voltage stability but it draws more current through the filter during transients. As a result, the filter stage with big capacitance operates at elevated losses.

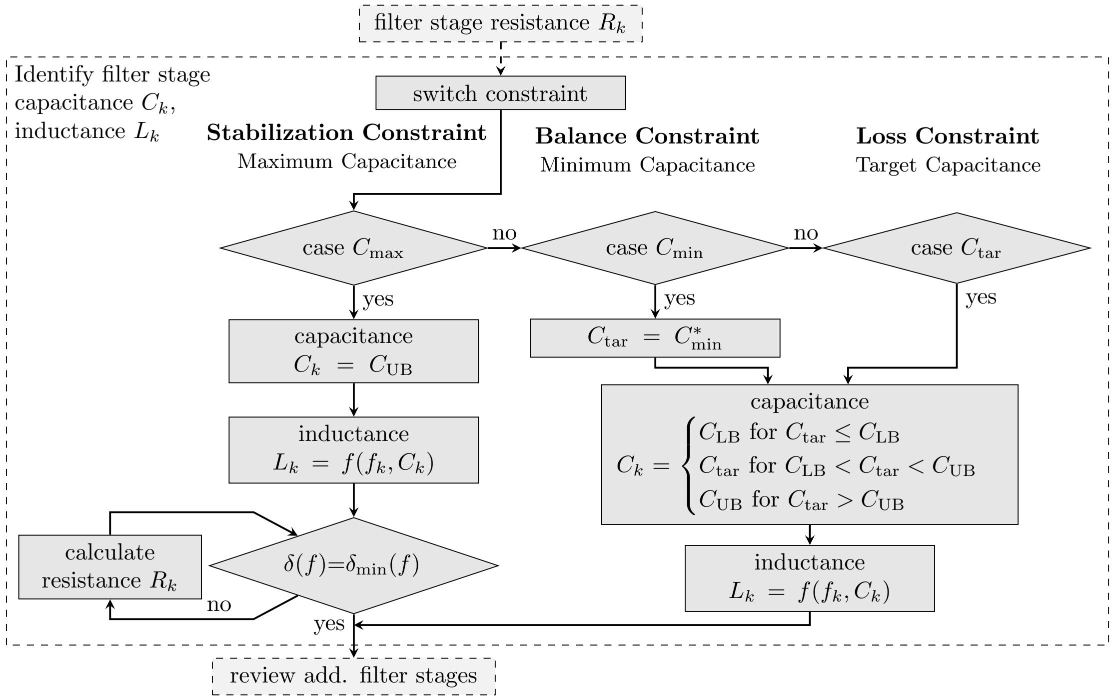


Figure 5.12: Flowchart of the capacitance design.

To obtain diversified results, three strategies are established as presented in Fig. 5.12. A maximum capacitance approach leads to pronounced voltage stability. On the contrary, using a small capacitance leads to minimal losses but could reach higher leftover deviations δ. A third strategy namely target capacitance calculates a filter on the basis of a target capacitance value. It keeps the specifications regarding deviation.

Stabilization constraint filters use an upper boundary capacitance C_{UB}. The upper boundary can be the maximum capacitance of available capacitors (see Tab. 5.1b). Alternatively, it is limited due to the minimal inductance $L_{\min}$ and the filter's frequency f_{k} according to (5.4). The corresponding inductance is calculated according to (5.5).

After setting C_k, L_k, the leftover deviation δ is evaluated. The minimum deviation $\delta_{\min}(f)$ in the entire frequency range (below 150 kHz) is searched. Therefore, initial $v_{\text{initial}}(2\,\pi f)$ and filtered $v_{\text{filtered}}(2\,\pi f)$ step responses are contrasted. Fig. 5.11b shows the exemplary selection of the minimum deviation by 9 iterations.

$$C_{\text{LB}} = \max\left\{C_{\min}, \frac{1}{4\,\pi^2\,f(k)^2\,L_{\max}}\right\} \qquad C_{\text{UB}} = \min\left\{C_{\max}, \frac{1}{4\,\pi^2\,f(k)^2\,L_{\min}}\right\} \tag{5.4}$$

$$L_k = \frac{1}{4\,\pi^2\,f(k)^2\,C_k} \tag{5.5}$$

The **balance constraint filter** uses a target capacitance C_{tar}. This capacitance is equal to the minimum capacitance $C_{\min}$ within the solution space (Tab. 5.1b). It is iteratively scaled up when the fully equipped filter ($k = k_{\max}$) cannot underestimate $\delta_{\max}$. This configuration change is considered as the second decision node in Fig. 5.9.

The **loss constraint filter design** calculates the filter parameterization on the basis of a user-defined target capacitance C_{tar}. The respective boundary restricted capacitance C_k is used to calculate the inductance L_k. If the fully equipped filter cannot undercut $\delta_{\max}$, the resistance of the first filter stage is iteratively increased. This loss of damping reduces the amplitude of positive deviations and can be used to reach the filter specifications. The resistance change is considered in the second decision node in Fig. 5.9.

An exemplary demonstration of the filter design algorithm is included in the initial population calculation of the optimization framework in Section 6.2.4.

5.4 Comparison of Introduced Methods

The control method for **three distributed converters** has been validated using the power system test bench of Chapter 4. A current pulse was injected at the terminals of the Audio Power Amplifier (APA) by the FID. The current pulse with an amplitude of 220 A and a rise time of 180 µs leads to a maximum current slew rate of 2.5 A/µs. Fig. 5.13 contrasts measurements of the initial and the stabilized power system.

As visualized in Fig. 4.6, the distributed converters are attached to PDs: PD1, Busbar (BB)F and BBC. Voltages at PD1 and BBC are ranging from 9 V to 13.5 V during the transient in the initial system. In contrast, the converters hold their voltages in the range of 10.3 V to 12.8 V. Both the upper and the lower voltage values can be improved by 1.3 V or 0.7 V, respectively. The voltage at the distant PD3 shows an influence on the dynamic load change. The first interval from 70 µs to 250 µs is characterized by a low load impedance at the APA. This pulls the voltage at the distributor PD3 down. However, distributed converters stabilize the minimum voltage to 8 V (instead of 7 V). The second interval until 380 µs is dominated by the conduction of the TVS diode within the FID. A voltage of 15 V is reached. The voltage is influenced by the characteristics of the TVS diode. Voltages could only be reduced if it exceeds 13 V at the converter nodes. Then, the converters would stabilize with a transition to boost operation.

Additionally, component voltages can be stabilized by distributed converters. The lower and upper voltage at the Windshield Wiper (WIP) can be improved by 0.8 V and 0.1 V. Voltages stick close to the control target of the converter (from 11 V to 13 V). They cannot exactly follow due to the wiring harness impedance.

The currents reveal less stress on the Master converter due to redistributing the current demand. In fact, the initial system burdens the output capacitor of the converter leading to a current of 64.4 A exceeding the converter current limit of 50 A. Distributed converters Slave 1 and 2 stabilize immediately when their node voltages fall below 11 V.

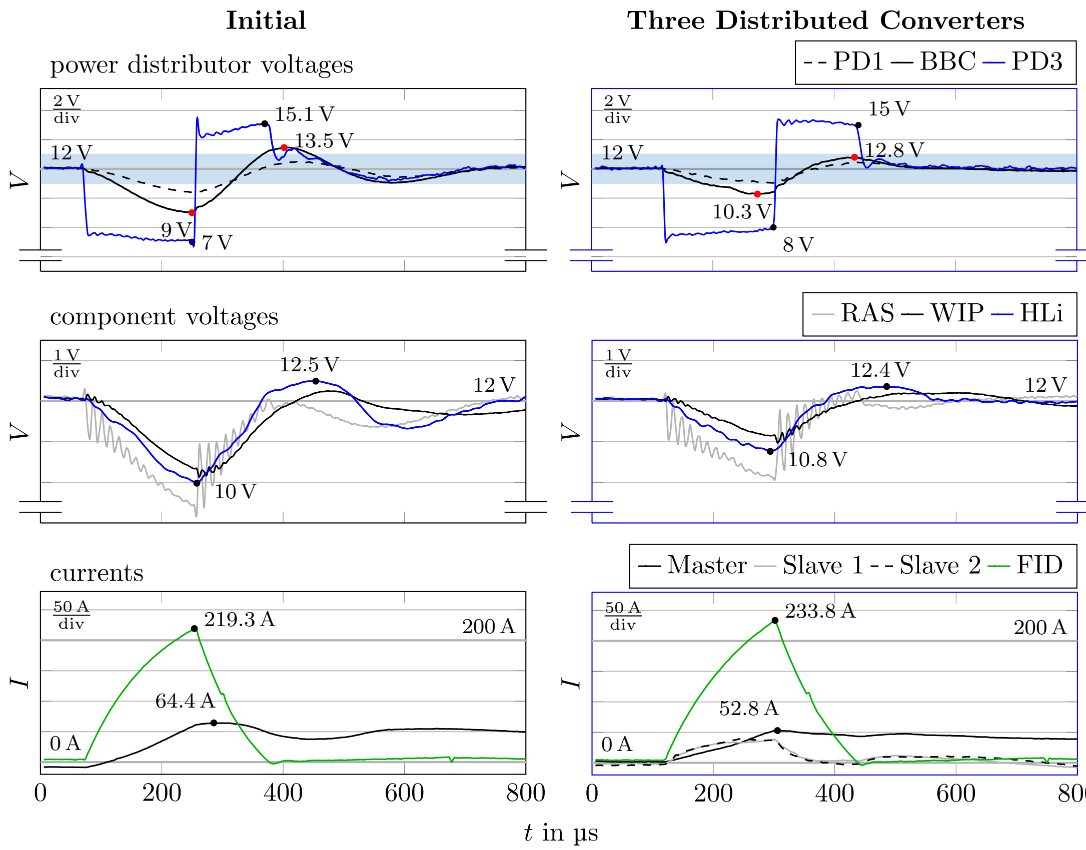


Figure 5.13: Stabilization measurements using distributed converters. The FID current of 220 A with a rise time of 180 µs is injected at the APA and stimulates the voltage imbalances. Voltages at the terminals of PDs and components are contrasted. Left plots show the original power system (with one Master converter) and the right plots show the values with the distributed converter control algorithm.

In this example, they support with approximately 40 A until the power system reaches a voltage of 12 V. The current of the FID rises faster due to the supply by the Slave converters. Therefore, a pronounced amplitude of 233.8 A is recorded. High-frequency oscillations at the Rear Axle Steering (RAS) are not stabilized by the converters. To reduce their amplitudes and settling times, adaptive band-pass filters should be used.

For the validation of the introduced **band-pass filter based stabilization measure**, a current transient with a slew rate of 2.5 A/µs and a rise time of 50 µs has been injected to the Device under Test (DUT) of the power system test bench of Chapter 4. The current transient stimulates anti-resonances as visualized in Fig. 5.14.

The voltages at BBC and PD3 oscillate at approximately 70 kHz. The voltage at PD1 does not show an excitation. The WIP and the RAS do react with a pronounced voltage oscillation. The component RAS shows an initial peak-to-peak amplitude of 3.6 V.

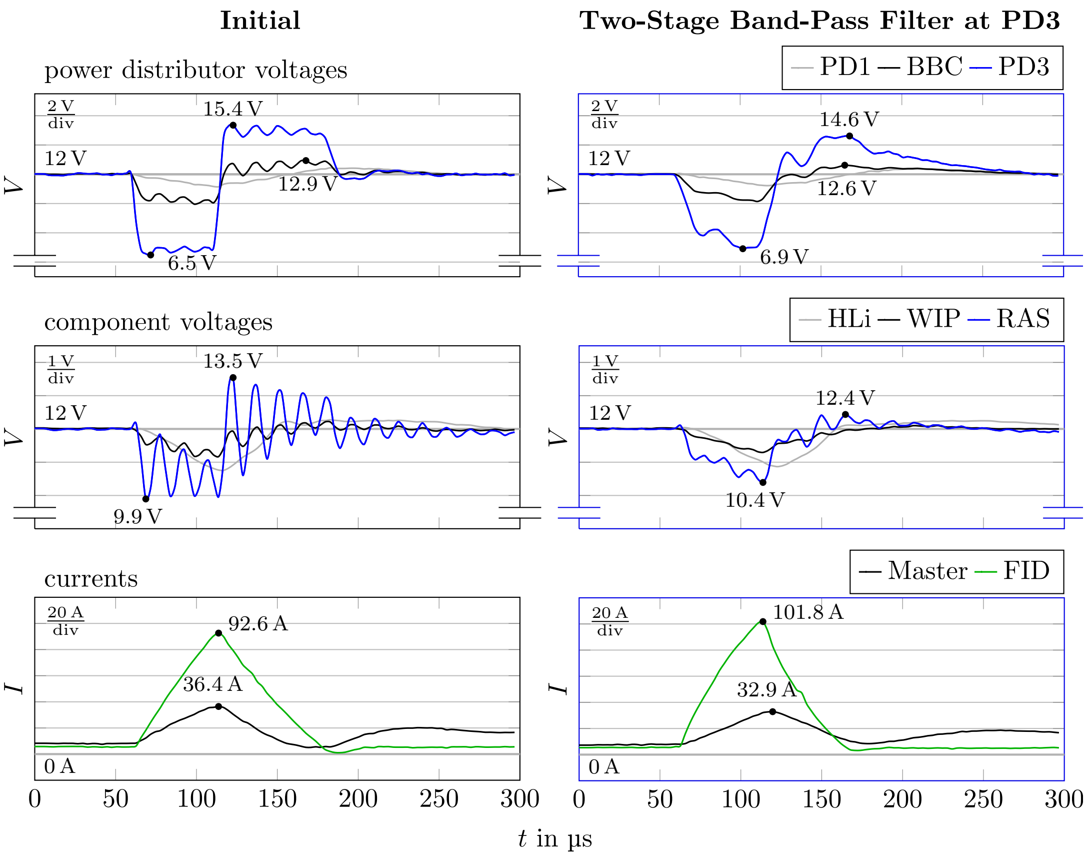


Figure 5.14: Stabilization measurements using system-designed band-pass filters. The FID injects a current at the APA. Measured voltages at the terminals of attached power distributors and components are contrasted. The left plots show the initial power system. The right plots show the resulting values with the introduced two-stage band-pass filter being attached to PD3.

By integrating the two-staged band-pass filter at PD3, oscillations can widely be damped. The filter has been designed according to a target capacitance of 100 µF with the loss constraint strategy. Visible oscillations of both PDs and components demonstrate a smaller oscillation amplitude and settling time. For instance, the oscillations at the terminals of the RAS can be reduced from 3.6 V to 2 V fulfilling a stabilization of about 44 %. Moreover, the oscillations at the terminals of the WIP are no longer perceptible.

The gain in voltage stability can be achieved in spite of a higher current slew rate occurring. The filter integrated capacitors excite a current at the AP of the disturbance. In fact, the current slew rate increases by 8 % from 2.5 A/µs to 2.7 A/µs. Since the current can be supplied to a great extent from distributed and the capacitors of filters, the output of the Master converter is less stressed.

6 Optimization Framework

The introduced stabilization measures from Chapter 5 show that various solutions for the parameterization of filters are possible. This chapter investigates the optimized parametrization of distributed passive band-pass filters. The focus is set on the sufficient suppression of subtransient voltage imbalances arising due to the stimulation of system-inherent anti-resonances.

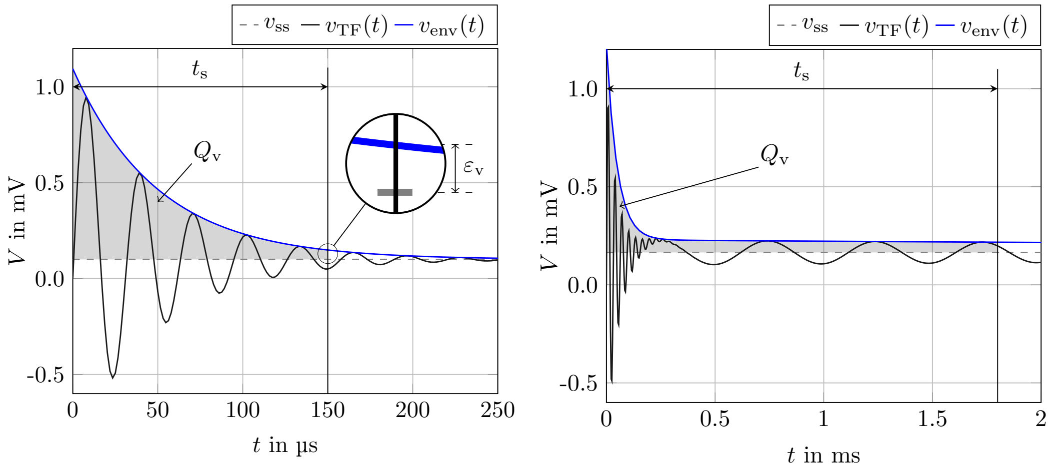
Previous vehicular power system-related optimizations were carried out by Ruf, Schwimmbeck and Vu. Ruf proposed the optimized integration of selected Double-Layer Capacitor (DLC) based stabilization measures. The aim is to achieve a low weight of stabilization measures and to fulfill fixed minimum voltage values during simulated peak loads [191, 192]. Schwimmbeck decreased the stress on Automotive Safety Integrity Level (ASIL) affiliated components during Short Circuits (S/Cs). The enhancements can be achieved by relocating batteries, DC/DC converters and adapted cable lengths [193]. Vu investigates GaN on-board chargers on their volume and losses [194].

6.1 Metric for the Evaluation of Voltage Stability

A new metric to quantify voltage stability needs to be established. The time-dependent behavior of oscillations (such as frequency, decaying amplitudes) cannot be recorded with the voltage stability measure proposed in [94, pp. 33] and introduced in Section 3.1.

This work investigates the transient response of excited transfer functions between potential disturbance sources and susceptible safety-critical components. Therefore, the power system has beneficial voltage stability if a high load fluctuation only affects the terminal voltages of selected components to a small extent. Fig. 6.1 visualizes the idea of this voltage stability definition. A step of 1 A at a load leads to a decaying voltage oscillation at the terminals of a component. The voltage oscillation has a certain amplitude, settling time t_s and voltage-time integral Q_v. This voltage-time integral is used to quantify voltage stability. Thus, both step response amplitude and settling time are taken into account.

To quantify the oscillating behavior of transfer functions, a Partial Fraction Decomposition (PFD) is applied to the identified transfer function. The complex poles are examined for their tendency to oscillate. A single complex pole $\underline{p}$ ($|\mathfrak{Im}\{\underline{p}\}| > 0$) with its respective complex residue $\underline{r}$ leads to a second-order transfer function as stated in (6.1). The equation includes conjugated complex quantities of the pole $\overline{\underline{p}}$ and the residue $\overline{\underline{r}}$.



(a) Single partial fraction's step response.

(b) Multiple partial fraction's step response.

Figure 6.1: Transient occurring at the step response of a transfer function with complex poles. The voltage stability value Q_v is defined as voltage-time integral between envelope curve $v_{env}(t)$ and steady-state value v_{ss} until the settling time criterion ε_v is reached.

$$G_{PF}(s) = \frac{\underline{r}}{s-\underline{p}} + \frac{\overline{\underline{r}}}{s-\overline{\underline{p}}} = \frac{\underline{r}\,(s-\overline{\underline{p}}) + \overline{\underline{r}}\,(s-\underline{p})}{s^2 - s\,(\underline{p}+\overline{\underline{p}}) + \underline{p}\,\overline{\underline{p}}} \tag{6.1}$$

Characteristic values have been identified to transform the step response of the transfer function into the time domain. The characteristics are listed in (6.2). Undamped oscillation frequency ω, damping coefficient D and damped frequency F form the core values. Parameters K_1, K_2 and A are auxiliary values for the representation of the resulting equation. The Laplace inverse transform has been identified by means of [184, pp. 227].

$$\begin{aligned} \omega &= \sqrt{\mathfrak{Re}\{\underline{p}\}^2 + \mathfrak{Im}\{\underline{p}\}^2} & D &= -\frac{\mathfrak{Re}\{\underline{p}\}}{\omega} \\ K_1 &= -2\,\big(\mathfrak{Re}\{\underline{p}\}\,\mathfrak{Re}\{\underline{r}\} + \mathfrak{Im}\{\underline{p}\}\,\mathfrak{Im}\{\underline{r}\}\big) & K_2 &= 2\,\mathfrak{Re}\{\underline{r}\} \\ F &= \omega\,\sqrt{1-D^2} & A &= \frac{D\,K_1 - \omega\,K_2}{K_1\,\sqrt{1-D^2}} \end{aligned} \tag{6.2}$$

The step response of the pole-residue transfer function $G_{PF}(s)$ corresponds to a decaying oscillation with an offset. Its time domain representation $v_{PF}(t)$ is shown in (6.3).

$$v_{PF}(t) = \frac{K_1}{\omega^2}\left(e^{-D\,\omega\,t}\,[\cos F\,t + A\,\sin F\,t] - 1\right) \tag{6.3}$$

To quantify the oscillation on the basis of the oscillation's amplitude and settling time, the envelope curve is calculated. The envelope curve $v_{env}(t)$ of the decaying oscillation $v_{PF}(t)$ is shown in (6.4). The trigonometric expression of $v_{PF}(t)$ is replaced by a constant K. The trigonometric expression leads to an oscillation with a certain frequency and amplitude. Its amplitude corresponds to the maximum value of the expression. This amplitude is found at peak time $t = t_{\text{pk}}$ according to (6.4).

$$\begin{gathered} v_{\text{env}}(t) = \frac{K_1}{\omega^2}\left(e^{-D\,\omega\,t}\,K - 1\right) \\ \cos F\,t + A\,\sin F\,t \overset{t=t_{\text{pk}}}{=} \max \qquad K = \cos F\,t_{\text{pk}} + A\,\sin F\,t_{\text{pk}} \end{gathered} \tag{6.4}$$

When generating multiple complex poles by the PFD, resulting envelope functions are added up. The voltage stability parameter Q_{v} corresponds to the voltage-time integral between steady-state v_{ss} and envelope $v_{\text{env}}(t)$ voltages until a settling time criterion ε_{v} is reached. It is further defined by a relative proportion to the envelope's maximum value (at $t = 0$). A settling time criterion of $\varepsilon_{\text{v}} = 1\,\%\;(v_{\text{env}}(t = 0) - v_{\text{ss}})$ is chosen.

Fig. 6.1a shows the time domain representation of the single complex pole's step response. The exemplary pole's oscillation frequency ω is chosen to be 32 kHz. The voltage stability parameter Q_{v} is calculated as voltage-time integral of the envelope curve $v_{\text{env}}(t)$ until the settling time criterion ε_{v} is reached. On the contrary, Fig. 6.1b shows the step response of a transfer function with two complex poles. Their exemplary frequencies ω have been chosen to be 32 kHz and 2 kHz. The individual envelope functions have been added up to $v_{\text{env}}(t)$. It forms the upper envelope of the oscillating voltage.

6.2 Optimization Problem

This section introduces the multi-criteria optimization problem for the parametrization of distributed passive band-pass filters. This includes the objective functions, the solution space, the boundary conditions and the initial population of possible solutions. Furthermore, a suitable optimization algorithm is selected.

6.2.1 Objective Functions

To calculate an optimized suppression of system-inherent disturbances, the best voltage stability is aimed for. The best voltage stability would be achieved by integrating a big DLC. However, this would lead to a significant increase in the power system's weight and its required installation space. The novel introduced electronic fuses [33, 35] would require separate consideration of the long capacitive charging times.

The additional weight or the energy dissipation of stabilization measures can be quantified. An optimized stabilization with little weight gain can be achieved with smaller capacitors. Therefore, the stabilization method must be adjusted to the correct frequencies. A small additional weight could be aimed for. In this work, the additional energy dissipation due to the stabilization measures is chosen as the second optimization goal.

Voltage Stability

The first optimization goal is to enhance voltage stability. The introduced metric of Q_{v} (see Section 6.1) enables a quantification of the transient voltage stability. Accordingly, improving the voltage stability corresponds to a reduction of Q_{v}. The voltage-time integral below the decaying exponential envelope function of the transfer function's step response should be minimal. Poles and residues are obtained by the partial fraction decomposition of identified transfer functions.

A power system to be stabilized contains multiple transfer functions to be considered. The power system consists of n_{A} ASIL and n_{Q} high-dynamic Quality Management (QM) components. QM components are potential disturbance sources that could lead to malfunctions of n_{A} components. Usually, lighting modules such as Headlights (HLi) and Taillights (TLi) are part of n_{A} safety-critical components. Furthermore, some components can be assigned to both groups. The class of n_{AQ} components stands out as being safety-critical and a potential disturbance source at the same time. An example for the group of n_{AQ} components is the Electric Power Steering (EPS). It is one of the most powerful Low Voltage (LV) components but needs a reliable power supply.

Important transfer functions to be considered are $n_{\mathrm{Q}} \to n_{\mathrm{A}}$, $n_{\mathrm{Q}} \to n_{\mathrm{AQ}}$, $n_{\mathrm{AQ}} \to n_{\mathrm{A}}$, $n_{\mathrm{AQ}} \to n_{\mathrm{AQ}}$. The number of critical transfer paths n_{t} can be calculated by (6.5). The established power system test bench includes five high-dynamic QM, nine safety-critical ASIL and four components being assigned to both groups n_{AQ}. For this example, a total number of 113 critical transfer paths n_{t} can be identified.

$$n_{\mathrm{t}} = n_{\mathrm{Q}} \left(n_{\mathrm{A}} + n_{\mathrm{AQ}}\right) + n_{\mathrm{AQ}} n_{\mathrm{A}} + n_{\mathrm{AQ}} \left(n_{\mathrm{AQ}} - 1\right) \tag{6.5}$$

The total voltage stability of the power system Q_{v} considers all critical transfer paths n_{t}. It is defined as the sum of all transfer path specific transient voltage-time integrals $Q_{\mathrm{v},p}$ according to (6.6).

$$Q_{\mathrm{v}} = \sum_{p=1}^{n_{\mathrm{t}}} Q_{\mathrm{v},p} \qquad\qquad E_{\mathrm{dis}} = \sum_{f=0}^{n_{\mathrm{f}}} \sum_{s=0}^{n_{\mathrm{f},s}} \int_0^{t_{\mathrm{s}}} i_{f,s}(t)^2 \, R_{f,s} \, \mathrm{d}t \tag{6.6}$$

Energy Dissipation

The second optimization goal is chosen to be a minimal energy dissipation within the introduced stabilization measures. The total energy dissipation E_{dis} is calculated for all system integrated adaptive band-pass filters n_{f} with their corresponding filter stages $n_{\mathrm{f},s}$. The individual filter stage's energy dissipation is calculated as integral over the squared filter stage current $i_{f,s}(t)$ during a voltage transient multiplied by the filter stage resistance $R_{f,s}$.

The individual energy dissipation is calculated by means of the band-pass filter stage's impedance and an applied voltage step. The necessary expression is described in (6.7). The filter stage consists of the series connection of R, inductance L and capacitance C. The applied voltage $V(s)$ causes the electric current $I(s)$.

$$V(s) = I(s)\left(R + L\,s + \frac{1}{C\,s}\right) \qquad I(s) = \frac{1}{L}\,\frac{1}{s^2 + \frac{R}{L}\,s + \frac{1}{L\,C}} \tag{6.7}$$

A voltage step with an amplitude of 1 V is applied to the individual filter stage. The corresponding electric current in the Laplace domain is illustrated in (6.7). The voltage $V(s)$ has been substituted with a unit step. The time domain representation of $I(s)$ is obtained by the Laplace inverse transform according to [184, pp. 227] in (6.8). The corresponding poles are calculated by (6.9).

$$\frac{1}{(s+a)\,(s+b)} \quad \bullet\!\!-\!\!\circ \quad \frac{1}{b-a}\left(e^{-a\,t} - e^{-b\,t}\right) \tag{6.8}$$

$$\begin{pmatrix} a \\ b \end{pmatrix} = \frac{R}{2\,L} \pm \sqrt{\left(\frac{R}{2\,L}\right)^2 - \frac{1}{L\,C}} \tag{6.9}$$

The power loss $P(t)$ is calculated as the product of the resistance R and the squared electric current. The solution is stated in (6.10). The individual energy dissipation $E_{\mathrm{dis},p}$ corresponds to the integral of $P(t)$. It is obtained within the integration limits of $t = \{0, \infty\}$ as shown in (6.10). A numeric integration approach is chosen for $\frac{1}{L\,C} > \left(\frac{R}{2\,L}\right)^2$. Partial energies $E_{\mathrm{dis},p}$ are added up for all filter stages and filters within the power system. Their sum complies with the total energy dissipation E_{dis}.

$$P(t) = R\left[\frac{1}{L}\,\frac{1}{b-a}\left(e^{-a\,t} - e^{-b\,t}\right)\right]^2 \qquad E_{\mathrm{dis},p} = \frac{R}{L^2}\,\frac{1}{(b-a)^2}\left(\frac{1}{2\,a} - \frac{2}{a+b} + \frac{1}{2\,b}\right) \tag{6.10}$$

6.2.2 Boundary Conditions

Two boundary conditions concern the location and the parameter limits. Additionally, the achieved transfer functions are contrasted to the initial system state.

Access Point

The band-pass filter is preferably attached to Power Distributors (PDs) as described in Section 5.3. Thus, specific Access Points (APs) are selected for the potential band-pass filter. The initial simulation model generation defines the APs of n_{f} filters with a maximum number of filter stages n_{s}.

Parameter Limits

The optimization result should be physically implemented in a Printed Circuit Board (PCB). Consequently, the hardware parasitics need to be taken into account. The individual filter stage resistance R is limited by the minimum/ maximum achievable resistance R_{min}, R_{max} with the PCB via resistance R_{via} and the parasitic resistance of available inductors and capacitors R_{LC}.

The filters inductance L is increased by the PCB via parasitic L_{via}. However, the influence of the PCB on the capacitance C can be neglected. The inequalities (6.11) specify the implemented boundary conditions of the filter parameters R, L, C.

$$\begin{aligned} R_{\mathrm{LC,min}} + R_{\mathrm{via}} + R_{\mathrm{min}} \overset{!}{<} R \overset{!}{<} R_{\mathrm{LC,max}} + R_{\mathrm{via}} + R_{\mathrm{max}} \\ L_{\mathrm{via}} + L_{\mathrm{min}} \overset{!}{<} L \overset{!}{<} L_{\mathrm{via}} + L_{\mathrm{max}} \\ C_{\mathrm{min}} \overset{!}{<} C \overset{!}{<} C_{\mathrm{max}} \end{aligned} \tag{6.11}$$

The passive band-pass filter should be effective below 150 kHz to not influence the Electromagnetic Interference (EMI) characteristics. Moreover, the filter should be of high impedance below 10 kHz. This ensures to not absorb any high-energy dynamic load change transients. The resulting condition is written in (6.12).

$$10\,\mathrm{kHz} \overset{!}{<} \frac{1}{2\pi\sqrt{L\,C}} \overset{!}{<} 150\,\mathrm{kHz} \tag{6.12}$$

Transfer Function Review

The filter implementation could significantly improve the voltage stability of a certain transfer path but other transfer functions obtain an increased anti-resonance. The last condition refers to the achieved resulting transfer functions with integrated filters. Adjusting the transfer functions should only lead to stabilization. This condition (6.13) checks if transfer functions have been negatively influenced in the frequency domain.

$$|G_{\mathrm{f},i}(j\,2\,\pi\,f)| \overset{!}{\leq} (1+\delta_{\mathrm{max}})\,|G_{\mathrm{init},i}(j\,2\,\pi\,f)| \qquad \text{for } i \in \{1,...,n_{\mathrm{TF}}\} \wedge f < 150\,\mathrm{kHz} \tag{6.13}$$

Transfer functions $G_{\mathrm{f},i}$ with the maximum number of n_{TF} are contrasted to the initial transfer functions $G_{\mathrm{init},i}$. A maximum relative deviation of δ_{max} (for instance, $\delta_{\mathrm{max}} = 5\,\%$) is allowed. The check is carried out below 150 kHz due to the limited model validity.

6.2.3 Solution Space

The parameters of band-pass filter components are restricted due to available components. Data sheet parameters of passive components used for the adaptive passive filters have been stated in Tab. 5.1 of Chapter 5. It should be noted that these values may have manufacturing tolerances. The tolerance for resistors is specified to be less than 1 %, for capacitors from 10 % to 20 % and for inductors below 20 %.

The solution space can be expanded by adding parallel or serial components. The PCB implementation of the band-pass filter has been designed to allow parallel component additions. The number of parallel combinations possible n_{par} for number of elements n and number of maximum parallel components allowed k is given in (6.14). This corresponds to a k-multicombination or a combination with repetition, respectively.

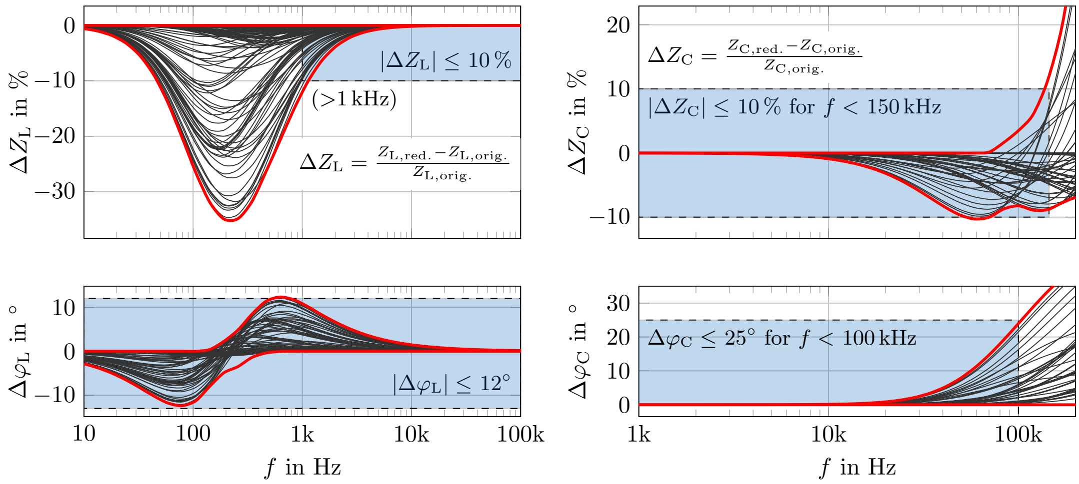
$$n_{\mathrm{par}} = \sum_{i=1}^{\mathrm{k}} \binom{\mathrm{n}+i-1}{i} = \sum_{i=1}^{\mathrm{k}} \frac{(\mathrm{n}+i-1)!}{i!\,(\mathrm{n}-1)!} \tag{6.14}$$

For a simplified calculation, parallel components are lumped in one component. This model reduction brings down the system states to be calculated. Capacitors have been modeled with their Equivalent Series Resistance (ESR) and inductors with their Direct-Current-Resistance (DCR). The parallel combination of multiple capacitors and inductors is reduced to Z_{C} and Z_{L}, respectively. Their components C_{r}, L_{r} and respective resistances $R_{\mathrm{C,r}}$, $R_{\mathrm{L,r}}$ lead to first-order model reductions according to (6.15).

The applied reduced-order approximation was carried out on the basis of the balancing-free square-root algorithm for computing singular perturbation approximations [195]. The first-order approximation of parallel capacitors includes a gain (corresponding to $R_{\mathrm{C,r}}$), a pole at $s = 0$ and a zero (corresponding to $\frac{-1}{R_{\mathrm{C,r}}\,C_{\mathrm{r}}}$). The first-order approximation of parallel inductors is used to extract $R_{\mathrm{L,r}}$ and L_{r}. The resistance is found as steady-state value $R_{\mathrm{L,r}} = Z(j\,0)$. The inductance is extracted at high frequencies $L_{\mathrm{r}} \approx Z(j\,2\,\pi\,1\,\mathrm{MHz})$. A frequency of 1 MHz is selected to obtain the inductance. Due to the inductance's dominance, the resistance is neglected.

$$Z_{\mathrm{L}} = \frac{1}{\sum_{i=1}^{\mathrm{k}} \frac{1}{R_{\mathrm{L},i}+L_i\,s}} \approx R_{\mathrm{L,r}} + L_{\mathrm{r}}\,s \qquad Z_{\mathrm{C}} = \frac{1}{\sum_{i=1}^{\mathrm{k}} \frac{1}{R_{\mathrm{C},i}+\frac{1}{C_i\,s}}} \approx R_{\mathrm{C,r}} + \frac{1}{C_{\mathrm{r}}\,s} \tag{6.15}$$

The proposed first-order model reduction delivers a sufficient approximation. The properties from 10 kHz to 150 kHz can be retained. Fig. 6.2a shows the deviation of the reduced-order model from the actual impedance of parallel inductors. The deviation between 10 kHz and 150 kHz is below 1 % in the amplitude and less than 2° in the phase angle. Below of 1 kHz, the parallel inductor model leads to significant deviations of about −30 % in the worst case. Fig. 6.2b demonstrates the deviations of the reduced model of parallel capacitors. Up to 150 kHz, the deviations are less than 10 %.



(a) Deviation of the simplified inductor model. **(b)** Deviation of the simplified capacitor model.

Figure 6.2: The first-order model reduction of parallel capacitors and inductors leads to deviations in their impedance. The envelope curves highlight the minimum and maximum deviations of 714 parallel combinations.

The deviations outside of the frequency range of 10 kHz to 150 kHz can be neglected. One reason for this is the limited validity of the model itself. The models of the capacitor with ESR and inductor with DCR are only valid below 150 kHz. Additionally, the filter's band-pass frequency is designed to be above 10 kHz and below 150 kHz. Below 10 kHz, the filter's capacitance dominates. The model reduction of parallel capacitors does not have deviations in this frequency range. Above 150 kHz, the filter's inductance dominates. There are no deviations of parallel inductors here either.

Fig. 6.2 contrasts the deviations due to the parallel combination of at maximum four from the selected components in Tab. 5.1. With nine selectable components and four maximum parallel components allowed the number of combinations is 714 each. Red envelope curves demonstrate deviations of all combinations.

Beyond, Tab. 6.1 contrasts number of realizable resistances $n_{R,par}$, inductances $n_{L,par}$ and capacitances $n_{C,par}$ by a parallel combination of k components at maximum. This includes component combinations with less than k components. The resulting filter stage's band-pass frequency f_C can be adjusted for a limited number of frequencies. Beyond, Tab. 6.1 states the number of possible center frequencies f_C in the preferred range below 150 kHz. Moreover, $\Delta f_{C,max}$ demonstrates the quantization of filter's band-pass frequencies. The more parallel components allowed, the more feasible solutions for resistances $n_{R,par}$, inductances, capacitances $n_{L/C,par}$ are possible. By allowing a maximum of four parallel combinations of the selected components, a quantization of 129 Hz can be generated. The number of realizable resistances is 1819 and 714 inductances or capacitances can be implemented. Every inductance and capacitance combination has an individual parasitic resistance being not shown in the table.

k	$n_{\mathrm{R,par}}$	$n_{\mathrm{L/C,par}}$	f_{C}	f_{C} <150 kHz	$\Delta f_{\mathrm{C,max}}$
1	12	9	81	64 (79.0 %)	1710 Hz
2	90	54	2916	2629 (90.2 %)	652 Hz
3	454	219	47961	45582 (95.0 %)	424 Hz
4	1819	714	509796	495984 (97.3 %)	129 Hz

Table 6.1: Numbers of feasible passive components, tunable center frequencies f_{C} and their maximum quantization step $\Delta f_{\mathrm{C,max}}$ in dependence of the maximum parallel components allowed k.

Discretization

Due to the presented calculation methods of the filter design algorithm and the optimization framework, filter parameters R, L, C belong to floating-point numbers. Accordingly, the continuous values must be discretized. Discrete values can be translated to real components.

First, the inductance L and the capacitance C are mapped to the closest value within the solution space of parallel components. This sets their values L_{r}, C_{r} and the band-pass filter stage's frequency.

The selected components include parasitic resistances DCR ($R_{\mathrm{L,r}}$) and ESR ($R_{\mathrm{C,r}}$). The discrete filter resistance corresponds to the closest value to $R - R_{\mathrm{L,r}} - R_{\mathrm{C,r}}$ within the solution space. From Tab. 5.1 it becomes apparent that the sum of parasitic resistances can be 48 mΩ in the worst case. This increases the minimum resistance of the solution space for certain LC-combinations. However, introduced system-designed filter resistances R are commonly above as shown in Section 6.2.4.

6.2.4 Initial Population

An initial population for suitable filter parametrizations is computed according to the filter design algorithm presented in Section 5.3.2. Three strategies have been established. The balance constraint filter design iteratively increases the capacitance until the maximum deviation is less than δ_{max}. On the contrary, the stabilization constraint filter design uses the maximum capacitance to achieve pronounced voltage stability. The loss constraint filter design parameterizes the filter on the basis of a given target capacitance and a reduced damping. These proposed strategies are shown using an exemplary initial pool generation.

Balance Constraint Filter Design

Fig. 6.3 visualizes the iterations of an exemplary balance constraint filter design. The frequency spectra of the transfer function's step responses are shown. The initial transfer function (black solid), the stabilized result (blue) and the benchmark result (black dashed) are compared. The benchmark result is achieved by substituting the passive filter by a 1 F DLC.

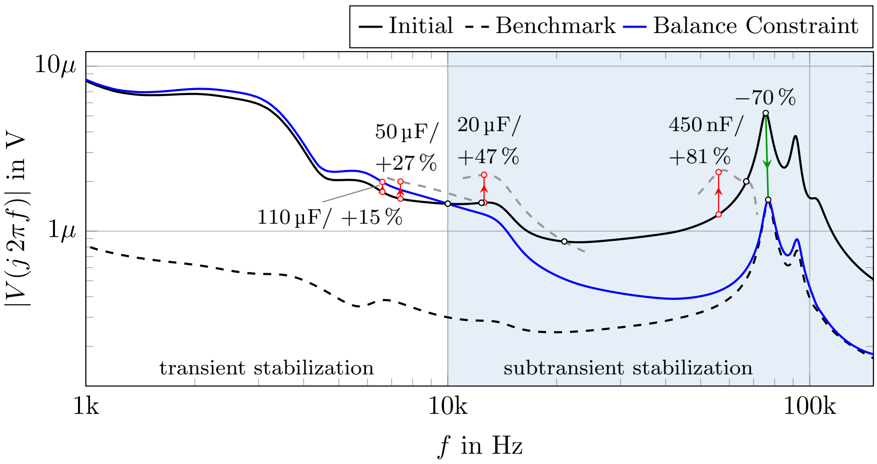


Figure 6.3: Balance constraint filter design for a two-staged band-pass filter. Several iterations of the minimum capacitance qualify 110 µF as minimum suitable capacitance to reach a negative deviation of less than 15 %.

Since the transfer function depicts the oscillation due to a current, the step response $V(j\,2\,\pi\,f)$ corresponds to a voltage. Beyond, the transient and subtransient stabilization areas are highlighted. A two-stage filter is applied. The designed filter reduces the anti-resonance (green) by 70 % to the ideally damped transfer function. Increasing the minimum capacitance C_{min} reduces the deviation δ as demonstrated.

The corresponding values to the iterations are presented in Tab. 6.2. The first stage resistance R_1 is kept throughout the calculation to ensure a damping of the anti-resonance by 70 % (maximum possible damping at the chosen AP). The elevation of the capacitances of both stages requires a recalculation of both second stage resistance R_2 and inductances (L_1, L_2). The deviation δ can be significantly decreased. However, a minimum deviation of 14.9 % can only be reached with the capacitance of 110 µF. The second filter stage is designed to be effective at the lower frequency limit of the band-pass filter of 10 kHz. The first filter stage's capacitance of 85 µF cannot be further increased due to the minimum inductance L_1 and the frequency at f_1.

<table>
<tr><th rowspan="2">x</th><th colspan="2">R in mΩ</th><th colspan="2">L in nH</th><th colspan="2">C in µF</th><th colspan="3">f in kHz</th><th rowspan="2">δ in %</th></tr>
<tr><th>R_1</th><th>R_2</th><th>L_1</th><th>L_2</th><th>C_1</th><th>C_2</th><th>f_1</th><th>f_2</th><th>f_δ</th></tr>
<tr><td>1</td><td rowspan="12">157</td><td>1435</td><td>10000</td><td>10000</td><td>0.45</td><td>0.57</td><td rowspan="12">75.2</td><td>66.8</td><td>56.0</td><td>80.5</td></tr>
<tr><td>2</td><td>575</td><td>448</td><td>3012</td><td colspan="2">10</td><td>29.0</td><td>18.4</td><td>62.9</td></tr>
<tr><td>3</td><td>472</td><td>224</td><td>2872</td><td colspan="2">20</td><td>21.0</td><td>12.6</td><td>47.3</td></tr>
<tr><td>4</td><td>437</td><td>149</td><td>2854</td><td colspan="2">30</td><td>17.2</td><td>10.2</td><td>38.4</td></tr>
<tr><td>5</td><td>427</td><td>112</td><td>3054</td><td colspan="2">40</td><td>14.4</td><td>8.4</td><td>31.4</td></tr>
<tr><td>6</td><td>406</td><td>90</td><td>3295</td><td colspan="2">50</td><td>12.4</td><td>7.4</td><td>27.1</td></tr>
<tr><td>7</td><td>403</td><td>75</td><td>3366</td><td colspan="2">60</td><td>11.2</td><td>6.8</td><td>23.3</td></tr>
<tr><td>8</td><td>403</td><td>64</td><td>3478</td><td colspan="2">70</td><td>10.2</td><td>6.4</td><td>19.8</td></tr>
<tr><td>9</td><td>446</td><td>56</td><td>3166</td><td colspan="2">80</td><td rowspan="4">10.0</td><td>6.4</td><td>17.5</td></tr>
<tr><td>10</td><td rowspan="3">484</td><td rowspan="3">53</td><td>2815</td><td rowspan="3">85</td><td>90</td><td>6.4</td><td>16.3</td></tr>
<tr><td>11</td><td>2533</td><td>100</td><td>6.6</td><td>15.5</td></tr>
<tr><td>12</td><td>2303</td><td>110</td><td>6.6</td><td>14.9</td></tr>
</table>

Table 6.2: Tabular comparison of iterations x for the balance constraint filter design (starts at the minimum capacitance). A leftover deviation δ of less than 15 % is achieved.

Stabilization and Loss Constraint Filter Design

The stabilization constraint filter design uses the maximum available capacitance to reach the maximum damping of the anti-resonance. Fig. 6.4 shows the maximum capacitance filter result in blue. A deviation δ of 7 % is obtained by using the maximum capacitance of 440 µF. The maximum capacitance designed filter leads to a decrease in the amplitude for frequencies in the transient stabilization area.

The loss constraint filter aims to reach the deviation specifications of $\delta_{\max}$ while reaching the maximum damping of the prominent anti-resonance for a given target capacitance C_{tar}. Fig. 6.4 contrasts three loss constraint filter designs. The higher the capacitance the more damping can be implemented and the lower the frequency at which the maximum deviation of $\delta_{\max}$ appears.

Tab. 6.3 shows the parameterization of the visualized filter designs. Noticeably, the first filter stage resistance R_1 is different for the loss constraint filter designs in order to reach a small deviation δ at the frequency f_δ. The stabilization constraint filter design is highlighted in green. The minimum inductance has not been limited to 53 nH with the allowance of a maximum of four components in parallel. The analysis of the stabilization approach showed that a capacitance as high as 560 µF would be needed to reach a deviation of less than 5 %. This capacitance is not included within the possible solution space.

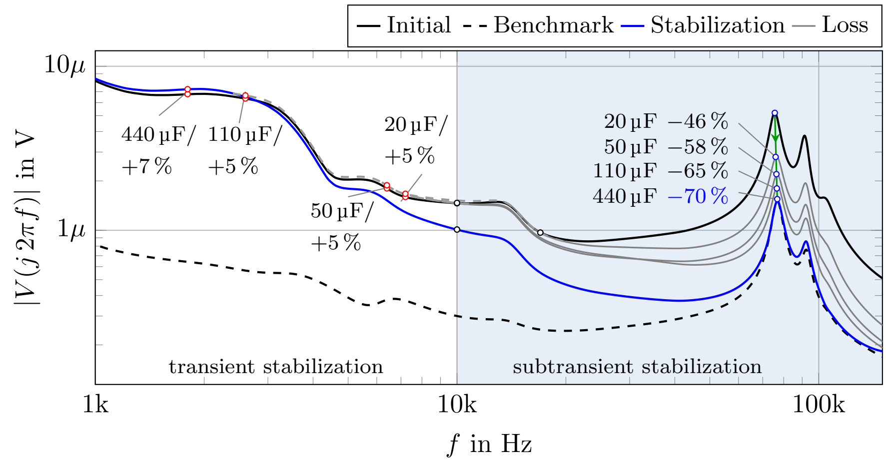


Figure 6.4: The stabilization constraint filter (highlighted in blue) largely reduces the anti-resonance and other frequencies. The loss constraint filter design for multiple selected small capacitances reaches a weaker damping of the anti-resonance but keeps the leftover deviation to the initial setup below 5 %.

<table>
<tr><th colspan="2">R in mΩ</th><th colspan="2">L in nH</th><th colspan="2">C in µF</th><th colspan="3">f in kHz</th><th rowspan="2">δ in %</th></tr>
<tr><th>R_1</th><th>R_2</th><th>L_1</th><th>L_2</th><th>C_1</th><th>C_2</th><th>f_1</th><th>f_2</th><th>f_δ</th></tr>
<tr><td>1256</td><td>1563</td><td>224</td><td>4382</td><td colspan="2">20</td><td rowspan="4">75.2</td><td>17.0</td><td>7.2</td><td>4.6</td></tr>
<tr><td>565</td><td>1124</td><td>90</td><td>5066</td><td colspan="2">50</td><td rowspan="3">10.0</td><td>6.4</td><td>4.5</td></tr>
<tr><td>380</td><td>11886</td><td>41</td><td>2303</td><td colspan="2">110</td><td>2.6</td><td>4.5</td></tr>
<tr><td>157</td><td>612</td><td>10</td><td>576</td><td colspan="2">440</td><td>1.4</td><td>6.8</td></tr>
</table>

Table 6.3: Stabilization constraint filter parameters are highlighted in green. Remaining parameters belong to loss constraint filter designs.

6.2.5 Multi-Objective Optimization Algorithm

The filter design according to the initial pool approach reaches some suitable results. The integration of multiple filters cannot be covered with the algorithms. Multiple filters must be checked for mutual influencing. An optimization algorithm is used to carry out an accelerated design evaluation. Moreover, a trade-off between stabilization and energy dissipation is assumed. Non-intuitive designs may be found by means of optimization.

Algorithm Requirements

The described problem of the filter parametrization to both stabilize selected transfer paths and achieve a low energy dissipation cannot be described analytically. Information about continuity or differentiability is not present for this multi-criteria problem. Moreover, the problem has a large solution space and the number of dimensions depends on the filters and filter stages to be configured.

In contrast to the topology design optimization in [192], the solution space has very narrow quantization steps due to the parallel combination of selected components (see Tab. 6.1). Thus, the solution space should be searched continuously within given limits. Subsequently, the continuous results should be transferred to discrete values. The algorithm should allow multi-processing or multi-threading function evaluations to reduce computation times.

Metaheuristic Algorithms

Metaheuristic optimization algorithms are suitable for the stated requirements of the multi-criteria problem. Available algorithms follow random, evolutionary or nature-inspired principles. Evolutionary or Genetic Algorithms mimic successful evolutionary principles. These include survival selection, recombination and mutation. Nature-inspired algorithms consider the swarm behavior of birds or fish as a basis [196].

Representatives for nature-inspired algorithms include Simulated Annealing and Swarm Intelligence. Simulated Annealing imitates the cooling of a metal. Slow cooling leads to the desired result of an optimal crystal grid. Starting at a random parameter set, the algorithm strives for fulfilling boundary conditions and achieving an optimum objective function value. The temperature of the fictional material keeps dropping during the evaluations. Thus, it is less likely to achieve an unfavorable functional value. [197]

Swarm Intelligence algorithms are characterized by an interaction of individuals with each other and with the environment. Accordingly, derived algorithms have been established such as the Ant Colony, the Social Spider, the Fish Swarm, the Krill Herd or the Seven-Spot Ladybird algorithm. Beyond, the Particle Swarm Optimization uses agile particles within a search space to strive for an optimal objective function value. Belonging particles own a mass, a velocity and a position. [9, 197]

Parallel-processing implementations of multi-objective optimization algorithms for both evolutionary and nature-inspired approaches were presented in [198]. Therefore, multi-objective Swarm Intelligence optimization algorithms use a fixed population size throughout the process.

Particularities and Appropriate Selection

Non-directed random (such as Tabu Search), Evolutionary Algorithms and Simulated Annealing are not further considered. The large solution space indicates a low convergence performance of the mentioned algorithms. Especially, evolutionary algorithms would require a high population size to get through the available search space by means of evolutionary processes. Fewer design evaluations are expected by applying the Particle Swarm Optimization. The algorithm is particularly useful for a problem of this high dimensionality and versatile variability.

The computationally intensive evaluation of the objective function and boundary conditions requires the implementation of parallel processing. Particle Swarm Optimization fulfills the above-mentioned algorithm requirements. [197]

6.3 Implementation

This section introduces two possibilities to carry out the optimization on the basis of a given power system. The analytical state-space calculation offers a quick way for investigations of the subtransient stability only. All passive transfer functions can be mapped above 10 kHz. Below, the control of components affects the voltage stability. The multiprocessing numerical calculation has been developed for this application.

6.3.1 Analytical State-Space Calculation

This framework is based on a state-space formulation of the power system. Wiring harness and component impedances as well as associated Kirchhoff equations must be implemented analytically. The state-space representation is shown in (6.16). The system's states are the branch currents $\mathbf{i}_{\text{br}}$. A branch current corresponds to the electrical current in one cable of the power system. For instance, the power system test bench presented in Chapter 4 contains 96 individual cables/ system states.

The system inputs $\mathbf{u}$ include voltage sources such as the Open Circuit Voltage (OCV) of an electrochemical storage. The matrix $\mathbf{A_1}$ displays the inductance matrix of the wiring harness. This includes self- and mutual inductance. The matrix $\mathbf{A_2}$ describes component impedances where the branch currents $\mathbf{i}_{\text{br}}$ flow through due to the series connection. To consider the system inputs $\mathbf{u}$ the matrix $\mathbf{B_2}$ is set up. The state-space output equation is left out since the focus is on the description of the whole system.

$$(\mathbf{A_1}\, s + \mathbf{A_2})\ \mathbf{i}_{\text{br}} = \mathbf{B_2}\, \mathbf{u} \tag{6.16}$$

A disturbance of an electric current is included by converting a branch current (system state) into a system input. The voltage equation across the disturbance source impedance is removed. The disturbance source impedance does not have an influence on the behavior of the stimulated system. The current mesh equation is transferred to the system input. The wiring harness impedance are integrated into $\mathbf{B_1}$, $\mathbf{B_2}$.

Integrating a passive filter is carried out by adding equations to the system. Each filter stage gets a respective branch current. The new Kirchhoff equations are added within the system matrices $\mathbf{A_1}$, $\mathbf{A_2}$ according to (6.17).

$$(\mathbf{A_1}\, s + \mathbf{A_2})\ \mathbf{i}_{\text{br}} = (\mathbf{B_1}\, s + \mathbf{B_2})\ \mathbf{u} \tag{6.17}$$

Transfer functions can be evaluated by (6.18). They are multiplied by component impedance vector $\mathbf{Z}_{\mathrm{comp}}$ to obtain the transfer impedance $\mathbf{Z}_{\mathrm{u}\rightarrow\mathrm{x}}$. For the energy dissipation $\mathbf{E}_{\mathrm{dis,u}\rightarrow\mathrm{x}}$, the multiplication of transfer functions is carried out with filter resistances $\mathbf{R}_{\mathrm{comp}}$. The power loss is integrated over time up until the transient settling time t_{s}.

$$\begin{aligned} \mathbf{Z}_{\mathrm{u}\rightarrow\mathrm{x}} &= \left(\mathbf{A}_1\, s + \mathbf{A}_2\right)^{-1} \left(\mathbf{B}_1\, s + \mathbf{B}_2\right) \mathbf{Z}_{\mathrm{comp}} \\ \mathbf{E}_{\mathrm{dis,u}\rightarrow\mathrm{x}} &= \int_0^{t_{\mathrm{s}}} \left(\left(\mathbf{A}_1\, s + \mathbf{A}_2\right)^{-1} \left(\mathbf{B}_1\, s + \mathbf{B}_2\right)\right)^2 \mathbf{R}_{\mathrm{comp}}\, dt \end{aligned} \tag{6.18}$$

The analytical stabilization of the power system is suitable for ordinary systems. Setting up the equations for larger highly meshed power systems can be rather challenging. Additionally, the control behavior of components can only be implemented with great effort or leads to a numerical approach. Publication [P5] presents an approach to include linear control in the state-space formulation.

6.3.2 Multiprocessing Numerical Calculation

Typically, power system models are integrated into multi-domain simulation environments [199]. An optimization framework has been established to take these models into account. This section introduces the framework and individual functions in detail.

The optimization framework implemented in Python® is visualized in Fig. 6.5. Initially, the framework generates the simulation model of the power system and calculates the solution space for passive filter components. Afterwards, filter components are parametrized. The parameters are generated by the benchmark approach, the initial population calculation (filter design algorithm) or the application of the optimization algorithm. Parallel time domain simulations are carried out in Modelica® [200, 201]. The trajectories of currents (n_{s} disturbance sources) and voltages (n_{t} safety-critical components) are passed to the analysis function within the optimization framework. For each disturbance source, the terminal voltages of n_{t} components is obtained ($n_{\mathrm{s}} \times n_{\mathrm{t}}$). Extracted frequency-dependent transfer functions $\boldsymbol{Z}(j\,2\,\pi\,f)$ are analyzed on poles and residues by means of system identification. Relevant partial fractions are used to calculate the target function within the optimization framework.

Simulation Model Generation

First, the established optimization framework generates the power system model to be stabilized. A given power system model is expanded by passive band-pass filters at its PDs. This is implemented by manipulation of the power system's Modelica® code description. Moreover, potential selected disturbance source models are substituted by adjustable resistors. For each disturbance source another Modelica® file is created. The control input of the resistor is a smooth pulse generator. The pulse specifications such as length and time of occurrence are freely configurable.

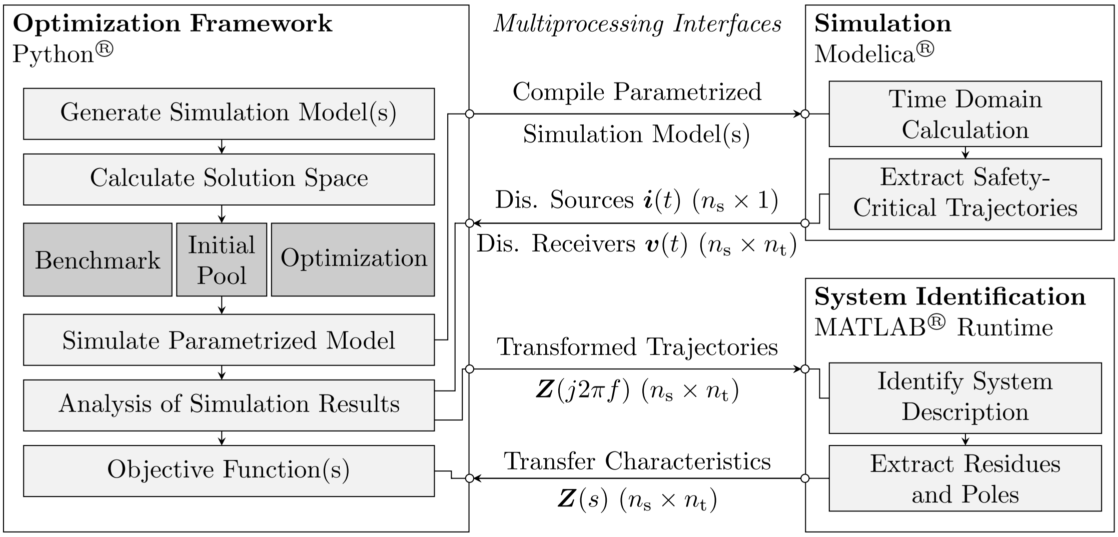


Figure 6.5: Block diagram of the multiprocessing optimization framework.

Solution Space Calculation

As proposed in Section 6.2.2 the parameters of passive filter components depend on their configuration. The solution space is calculated by defining a maximum number of parallel components and loading the stored parameters of selected components. The maximum and minimum values for each component R, L, C are stored and used as the boundary conditions for the subsequent simulation model parametrization.

Simulation Model Parametrization

The parameters of the power system included passive filters are generated by means of three different approaches: Benchmark, initial population and optimization.

The benchmark parameterization strives for the maximum possible stabilization at a given AP. An attached filter is substituted by a DLC of 1 F (see Section 6.4). The resulting voltage stability represents the best value for the selected AP. This achieves a reference value and the benchmark approach examines the suitability of an AP.

The initial population parametrization is carried out according to the filter design algorithm of Section 5.3.2. Three parameter sets for stabilization, loss and balance constraint filter designs are generated. The iterative process yields parameters for every single filter on the basis of all possible disturbances. A mutual influence of the individual passive band-pass filters on each other is not taken into account in this population generation.

The implemented optimization algorithm is the Non-Dominated Sorting Particle Swarm Optimizaton. It is based on Particle Swarm Optimization but achieves a superior convergence performance when using a well-designed initial population.

The algorithm is presented in [202]. The implemented parallel global multi-objective optimization framework is PAGAMO by Biscani [203]. The problem is unconstrained by introducing the death penalty to parameter sets outside the boundary conditions. This ensures compliance with the boundary conditions. The optimization algorithm is configured to run in batch mode. Thus, a group of parameter sets can be evaluated in parallel.

The multiprocessing call of simulations is carried out by the simulation model compilation in different directories. The manipulated Modelica® code description is stored in the folder. Passive filter parameters are transferred to the description. The simulation model is compiled by means of Dassault Systems Dymola® . The simulation is executed, resulting trajectories are passed to the optimization framework and the folder is deleted.

Analysis of Simulation Results

Bünte [204] presented a possibility to record frequency responses of Modelica® implemented models. A given simulation model is stimulated at individual frequencies.

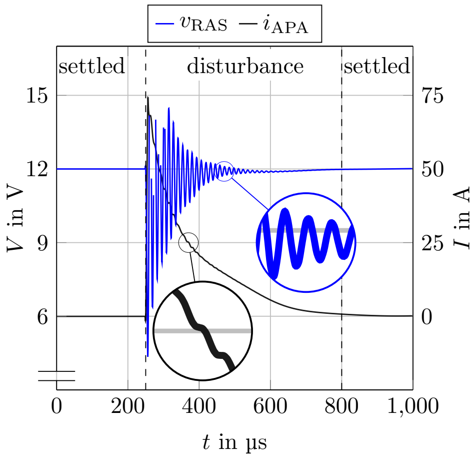
For a faster frequency domain analysis, pulse spectroscopy is carried out. The resulting time domain trajectories of voltages and currents are transformed to frequency domain by means of Discrete Fourier Transform (DFT) as presented in Section 4.4.2. Recorded signals are settled at the beginning and at the end. [186, pp. 185], [187, pp. 213]

Fig. 6.6a shows exemplary time domain simulation results. The current i_{APA} is the disturbance signal injected at the Audio Power Amplifier (APA). This exemplary disturbance has an amplitude of 74 A and a rise time of 40 µs. The voltage at the terminals of the Rear Axle Steering (RAS) v_{RAS} includes a 75 kHz oscillation. Fig. 6.6b shows the corresponding frequency domain signals. The voltage (blue) has an strong amplitude at 75 kHz as observed from the time domain signals. The transfer function $Z_{\mathrm{APA}\rightarrow\mathrm{RAS}}$ (dashed blue) is obtained by dividing voltage v_{RAS} and disturbance current i_{APA}.

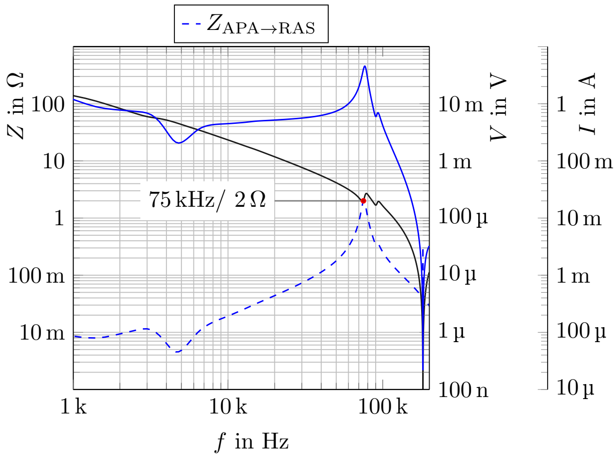
Beyond, the simulation environment's solver settings need to be selected carefully. The power system simulation model could be considered numerically stiff due to incorrect solver settings [205]. The Frequency Dependent Network Equivalent (FDNE) based simulation models of components are valid up to a user-defined frequency. High computing times need to be avoided. Liu showed the superior performance of DASSL and LSODAR solvers in terms of efficiency and velocity [46]. These solvers are to be preferred, especially for stiff simulation models. DASSL has been chosen.

Objectives

The frequency domain transfer functions are passed to a performance-oriented system identification framework. Gustavsen's vector fitting procedure [121] for the extraction of residues and poles is transferred to a Python® package. The generated package is called by means of MATLAB® Runtime.



(a) Time domain simulation results of the current pulse injection.



(b) Frequency domain analysis of simulated signals and their transfer function.

Figure 6.6: High dynamic current pulse injection in the time and the frequency domain. The resulting transfer function is calculated by DFT.

The identified residues and poles are used to calculate the voltage stability and the energy dissipation as described in 6.2.1. Calculated objective function values (voltage stability Q_v and energy dissipation E_dis) are passed to the optimization algorithm. Further evaluations follow the same procedure (continues from simulation model parametrization).

6.4 Optimization Results

An optimization has been carried out for the distributed converter-supplied system. Three two-stage filters have been parametrized with one disturbance source at the APA. The objective function depicts the voltage stability of eight safety-critical components.

Fig. 6.7 shows the energy dissipation E_dis of one filter at PD3. It is selected since it leads to a comparably high dissipation for the selected disturbance at the APA. Moreover, the voltage stability Q_v at component RAS is shown. The initial power system has a voltage stability of 10.2 µVs. This can be improved by 64 % by applying parameters p_1. The results highlighted in red are the initial population parameters (p_1 stabilization constraint, p_2 loss constraint C_tar =20 µF, p_3 loss constraint C_tar =110 µF), see Section 5.3.2.

Beyond, Fig. 6.7 highlights the voltage stability when applying different capacitors such as 1 mF (maximum capacitance of a two-stage filter), 100 mF and 140 mF. The resulting filters perform better than the pure integration of the maximum capacitance. The reason is the missing compensation of a Low-Frequency (LF) anti-resonance. The passive filters are able to achieve a voltage stabilization similar to the capacitance of 140 mF. Integrating the benchmark capacitor (DLC) of 1 F leads to a voltage stability of 2.5 µVs. Further increasing the capacitance does not noticeably improve the stability.

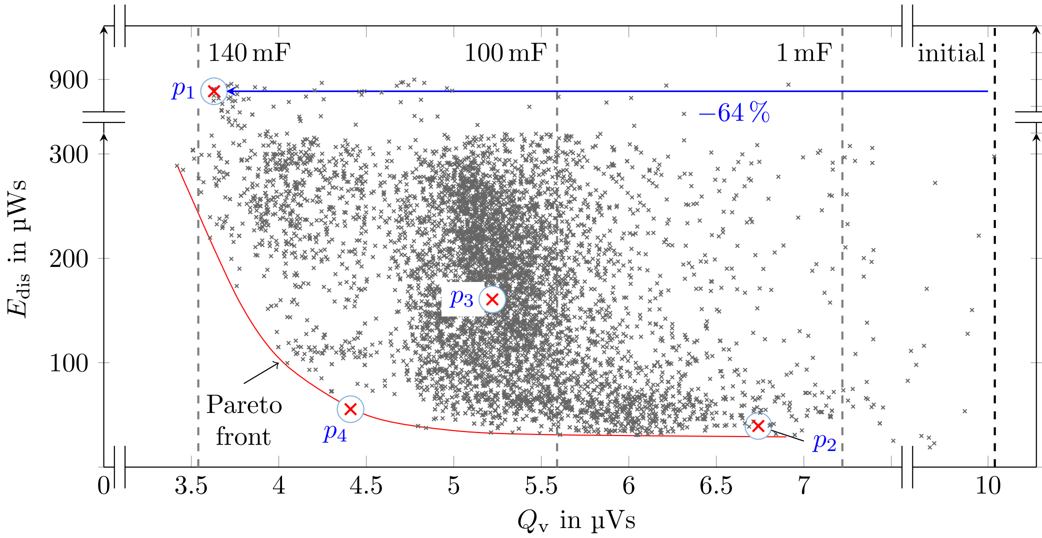


Figure 6.7: Optimization results for the filter parametrization at PD3 for eight transfer functions and three two-stage filters. 30.000 design evaluations result in the highlighted Pareto front of energy dissipation E_{dis} and voltage stability Q_{v}. The red highlighted values correspond to the initial population calculated parameter sets.

To obtain the Pareto front, 30.000 evaluations of the objective function have been carried out. One evaluation takes approximately 20 s using an Intel® CPU Core i7-8700K 3.7 GHz. DASSL solver is used to calculate 10 ms. By distributing the optimization task on eight parallel processes, a computation time of 21 h is achieved.

The Pareto front is highlighted in red in Fig. 6.7. Noticeably, the initial population generation already achieves competitive results. Since the filter design algorithm does not consider the mutual influence of the three distributed passive filters, better results can be achieved by the optimization framework.

There are several feasible approaches to select a parameter set on the Pareto front:

- The best voltage stabilization. By restricting the maximum capacitance within the solution space, a certain level of stabilization cannot be hit. The maximum capacitance restriction might come about due to space or weight limitations. Charging times of electronic fuses could set this limit due to the energy dissipation.
- The best energy dissipation for a particular stabilization. The specification of a minimum stabilization is possible. This can come about in order to stabilize the terminal voltages of power system components to permissible limits.
- A suitable energy dissipation. During a given driving cycle, voltage oscillations at the APs of the filters can occur. They lead to dissipated energy. A restriction of these losses can be defined based on a maximum value allowed or due to heatsink requirements such as only air convection cooling should be implemented.

An arbitrarily chosen parameter set p_4 has been selected for further analysis. For a better understanding, the signals of red highlighted results in Fig. 6.7 are analyzed in the time and the frequency domain in Fig. 6.8.

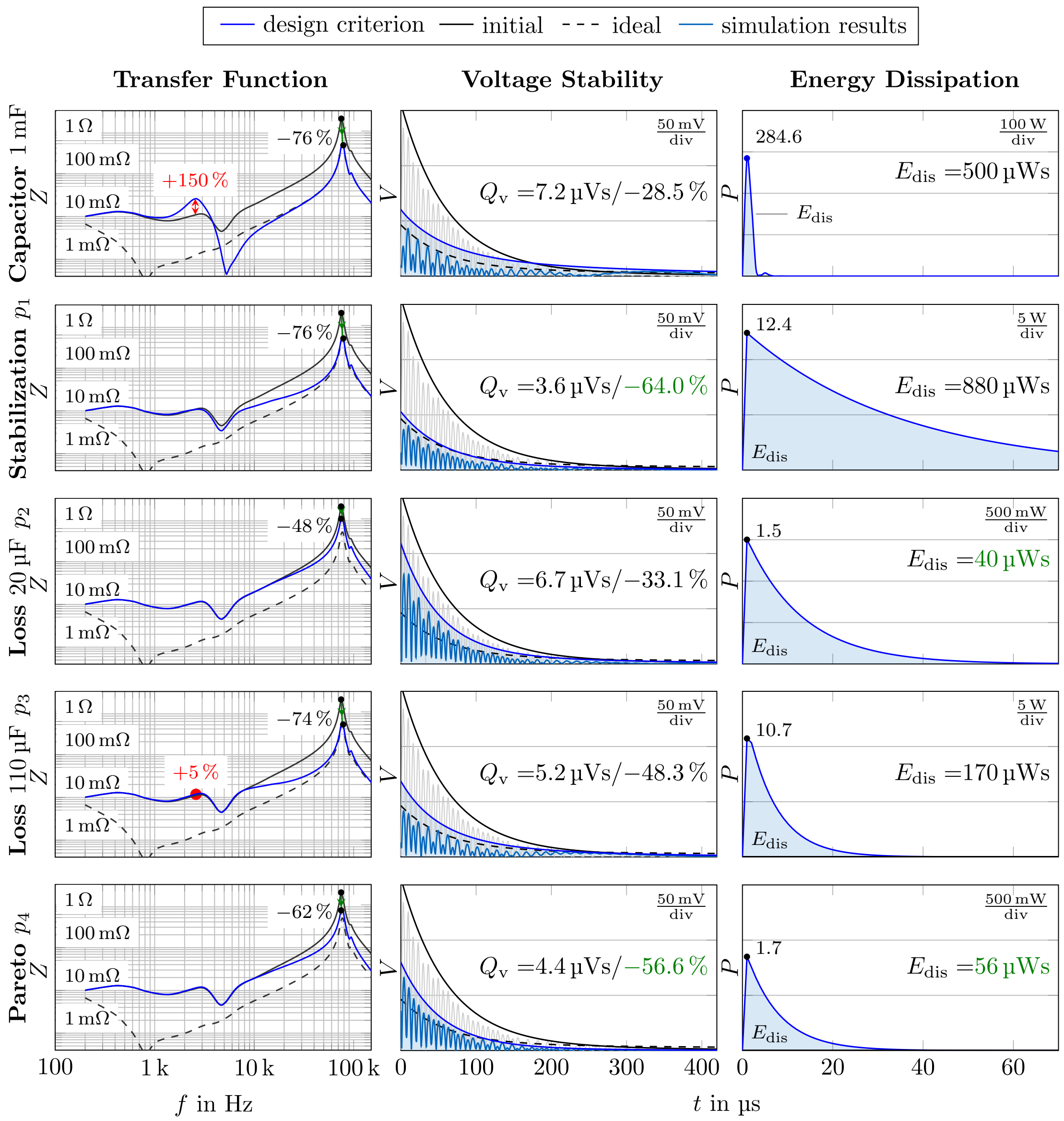


Figure 6.8: Time and frequency domain analysis of the optimization results. The transfer function of APA → RAS is visualized. The envelope functions of the RAS terminal voltage (blue) resulting from a step of the current at the APA are shown. The envelope function is contrasted to the initial (black) and the ideal function (dashed black). The filter's power loss due to a voltage step is presented. Its integral corresponds to the energy dissipation E_{dis}.

The figure contrasts the achieved (blue), the initial (black) and the benchmark (dashed black) transfer function (APA→RAS) and voltage oscillation. The voltage oscillation at the RAS occurs due to a current step at the APA. Noticeably, the maximum capacitance (1 mF) leads to a new anti-resonance at 2.5 kHz. The amplitude's elevation by 150 % leads to a long settling time of the blue envelope curve (top center). Therefore, the voltage stability is reduced by 28.5 %.

A better stabilization can be achieved by the stabilization constraint filter design. A voltage stabilization by 64 % is visible. Both settling time and amplitude of the voltage V are comparably small. The loss constraint filter design with a target capacitance of 20 µF only achieves a damping of the anti-resonance at 75 kHz by 48 %. Consequently, the voltage is stabilized by 33.1 %. The achieved stabilization with the second loss constraint filter design (110 µF) lies in the middle.

Fig. 6.8 also shows the energy dissipation through the filter due to a voltage step. Apparently, the maximum capacitance has the highest power loss of about 284.6 W. The best energy dissipation can be achieved with the loss constraint filter design (20 µF). Thus, the energy dissipation of 40 µWs is about 95 % smaller than the energy dissipation of the stabilization constraint filter design. The energy dissipation of the second loss constraint filter is only 170 µWs, although a voltage stabilization of about 48.3 % can be achieved.

The Pareto front corresponding parameter set p_4 achieves both beneficial voltage stabilization of 56.6 % and low energy dissipation 56 µWs.

6.5 Validation of Optimization Results

The selected Pareto front belonging parameter set p_4 has been implemented in the adaptive band-pass filter PCBs. Fig. 6.9 shows the simulation results and measurements on the test bench. Three different system configurations are contrasted. The original system configuration (left) has one converter applied at the supply at PD1. The center plots show the power system with distributed converters installed. Three converters supply at PD1, Busbars (BBs) BBF and BBC. The right plots show the system supplied by distributed converters at the same APs. Beyond, this system configuration has Pareto optimized band-pass filters p_4 integrated at PD1, BBC and PD3.

Each system configuration is disturbed by a high dynamic current injection with an amplitude of approximately 220 A to 234 A and a rise time of 180 µs. The current pulse is injected at the component APA. The current slew rate is limited due to the power system's impedance. The maximum current slew rate is in the range of 2.5 A/µs to 3.6 A/µs. It occurs within the third system configuration (converters and filters). The filter's capacitance at the PD3 feeds the disturbance current.

The figure demonstrates the effectiveness of the introduced stabilization measures. The voltage drop at the PD1 can be reduced by 0.7 V with distributed converters and by 0.8 V with the converters and filters.

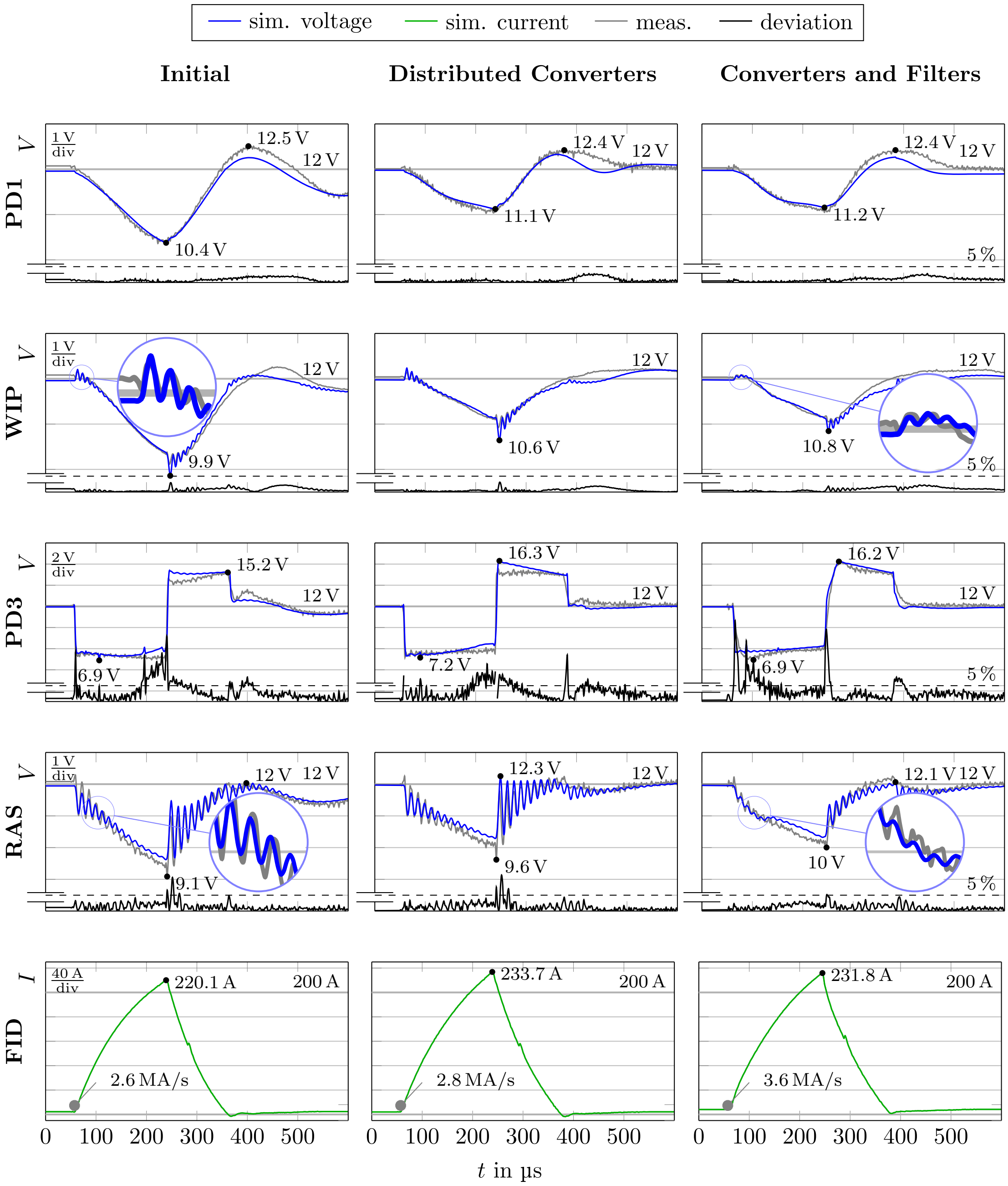


Figure 6.9: Validation of optimization results. The Fault Injection Device (FID) injects a current transient at the APA and stimulates voltage disturbances. Measured voltages at the terminals of attached power distributors and components are contrasted to simulation results. From left to right: initial power system, power system with introduced distributed converters, optimized band-pass filters and distributed converters.

Moreover, the voltage at the Windshield Wiper (WIP) can be stabilized by 0.7 V and at the RAS by 0.5 V. The passive filter's effectiveness becomes clear in both voltages at the WIP and the RAS. Both terminals are exposed to voltage oscillations at a frequencies of 67 kHz (WIP) and 75 kHz (RAS), respectively. Both oscillations can be greatly damped by the integration of optimized system-designed passive band-pass filters within three PDs.

Beyond, Fig. 6.9 visualizes the validity of the simulation models. Steady-state, transient and subtransient voltages can be accurately simulated with a deviation of less than 5 %. Larger deviations of about 10 % for 50 µs (9 % of the total simulation time) occur at the PD3. Reasons for the deviations have been listed in Section 4.5.

7 Summary

In this work, new modeling methods and stabilization measures for vehicular power systems are proposed. The simulation results are validated by an established Low Voltage (LV) power system test bench. This chapter briefly summarizes the results of this work and provides starting points for further research.

7.1 Results

Available simulation models in the literature focus on a validity below 10 kHz or above 150 kHz. However, the area in between is important to demonstrate the fail-operational supply of safety-critical loads. Moreover, models in assigned abstraction classes are advantageous to simulate different design criteria (e.g. effects of a Short Circuit (S/C), energy consumption within a driving cycle) in a computationally efficient way.

A three-stage classification according to the frequency range is introduced: steady-state (up to 100 Hz), transient (up to 10 kHz) and subtransient (up to 150 kHz). The introduced classification can be transferred to the modeling method, occurring power system disturbances and stabilization measures. Moreover, hardware concepts and designs can be subdivided based on this classification.

Power system components are investigated according to their system perturbations. High power components have been identified as particularly important. Their wiring harness connections favor a strong dynamic power flow influencing node voltages at decisive Power Distributors (PDs). The attached safety-critical devices could be disturbed. Consequently, a focus is placed on both high power and safety-critical components.

The attached devices are modeled employing system identification and Resistor-Inductor-Capacitor (RLC) network synthesis. Resulting Frequency Dependent Network Equivalents (FDNEs) are extended by controllable resistances for the integration of the controlled operating point. Important nonlinear components are included in the FDNEs. Thus, the steady-state, the transient and the subtransient behavior can be mapped.

Switched power electronic devices are modeled by a state-space average algorithm. The algorithm reduces the computation effort (in contrast to the switched model) while the accuracy is elevated (in contrast to the average model available in the literature). In particular, switching effects during the body-diode conduction phases or the switching dead time are considered. The lumped-parameter model of the wiring harness for the frequency range below 150 kHz contains resistances, self- and mutual inductance.

The modeling methods can generate simulation models for power system analysis of up to 150 kHz. This allows valid simulations of resonance stimulations. The switching behavior of electronic fuses and its effects on the power system can be looked for precisely.

A test bench was established for the investigation of power system-inherent transients up to 30 A/µs. The basis of the test bench is formed by a Battery Electric Vehicle (BEV) power system being released by BMW AG in 2021. The power supply of the LV power system is emulated by voltage-scaled distributed DC/DC converters. The test bench is used to analyze (sub-)transients and failures such as S/C currents. Moreover, simulation models are validated within the power system.

This work proposes stabilization measures to improve the subtransient voltage stability within the power system. Therefore, distributed converters with a double-hysteresis control are introduced. The master-slave-based control reacts to voltage imbalances in less than 10 µs. The individual converter is reconfigured to buck, boost or idle operation. Critical voltage spikes due to high current dynamics can be prevented. Furthermore, adaptive multi-stage band-pass filters are introduced to stabilize subtransients above 10 kHz. The parameterization is carried out using a filter design algorithm and a multi-criteria heuristic particle-swarm optimization framework. Distributed filters aim for both high voltage stability and reduced energy loss within the stabilization hardware. Stabilization measures are implemented in the test bench to investigate their effectiveness. Exemplary designed distributed filters stabilize by about 60 %. Although the capacitance of the filter is limited to only 200 µF, this result is comparable to the integration of a 140 mF capacitor at the same Access Point (AP).

7.2 Outlook

The modeling method could be expanded by the thermal domain to facilitate the simulation of temperature-dependent effects up to 150 kHz. Both influence on the component impedance and the stabilization effectiveness could be researched. The method focuses on the normal operation. Another expansion of the FDNEs by component failures might be researched. The state-space average algorithm for switched converters can be applied to inverter-driven electro-mechanical loads. Proposed modeling methods could be considered for further DC micrografts such as High Voltage (HV) airplane power systems.

The introduced stabilization measure of adaptive multi-stage band-pass filters could be expanded by the temperature dependence of system impedance. Research into active impedance analysis and autonomous filter adaption would be conceivable. Transient stabilization of power systems could be achieved by active damping as proposed in [206]. Its application on LV power systems concerning the current ripple has not been sufficiently studied yet.

The proposed optimization framework allows the integration of further stabilization measures. The geometry of the wiring harness could be adapted. Destabilizing induced voltages during high current slew rates within tight cable bundles can be avoided.

A Appendix

A.1 State-Space Average Algorithm

This appendix section shows a comparison of the created state-space average model of a Phase-Shifted Full-Bridge (PSFB) converter in contrast to a switched model and the literature standard average model. The mathematical framework behind the state-space average model is described in Section 3.3 and published in [P6]. Applied parameters of the PSFB under investigation are listed in Tab. A.1.

Table A.1: Parameters of the PSFB converter (Fig. 3.12).

V in V	t in µs	L in µH	L in nH	C in mF		C in nF	
V_{in}	T_{s}	L_{f}	L_{k}	C_{in}	C_{o}	C_{p}	C_{s}
48	10	1.5	124	4.8	1.1	5	10

R in mΩ						R in Ω	
R_{dsp}	R_{dss}	R_{p}	R_{s}	R_{cin}	R_{c}	R_{cp}	R_{cs}
4.5	2.6	0.2	2.1	2	2	3	3

Fig. A.1 contrasts the simulation results of an extensive switched model, the conventional duty cycle loss model from the literature and the proposed model including d_{L} and v_{add}. All systems face high dynamic load changes from buck to Open-Loop (O/L) to boost and O/L within a time of 2 ms. In buck mode all systems show similar average values. In low load and boost operation the proposed algorithm outperforms the conventional duty-cycle loss model. Output voltage V_{o} deviations are reduced by 95 % in dynamic boost operation. Also the inductor current deviation is reduced by more than 92 %. [P6]

An 8 ms simulation implemented in Plexim® PLECS was carried out on a portable machine housing a 8$^{\mathrm{th}}$ generation 1.7 GHz Intel® Core i5 CPU. While the switched model computation lasts 15.06 s, the proposed average model is solved in 1.39 s and computing a the literature standard average model takes 0.70 s. Thus, the proposed model cuts the computation time by about 91 % and the conventional average model reduces the time by 95 % in contrast to the switched model. [P6]

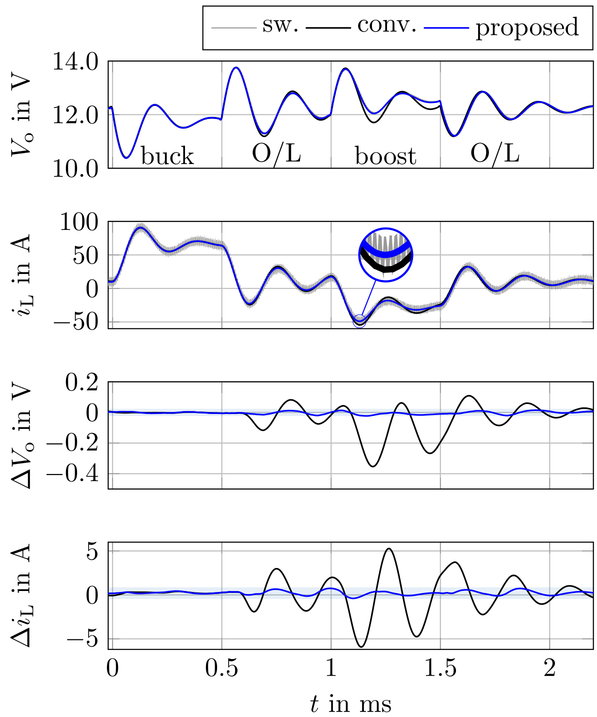


Figure A.1: Dynamic comparison of switched model, conventional duty cycle loss model and proposed average model.

A.2 Voltage Measurement

Modular measurement instruments are connected to the power system via breakout boxes. They protect the instrument from damage and also allow a flexible connection. The flexibility comes at the expense of longer test leads with parasitic capacitances.

In order to scale the voltage to a harmless range for the instrument, voltage dividers are being used for both positive and negative analog inputs. To reduce the bandwidth limitation due to the introduced voltage dividers and parasitic capacitances, a measuring circuit based on Fig. A.2 is used. $C_{1,\mathrm{ai}+}$ and $C_{1,\mathrm{ai}-}$ are ceramic trimming capacitances, which are manually adapted to the connected ancillaries.

Respective trim capacitor's values can be analytically calculated by means of (A.1). The Low Voltage (LV) vehicular power system needs a measurement accuracy up to 32 V according to Section 2.2.4. An exemplary voltage divider of 3.2:1 can be used with the instrument's voltage acceptance of 10 V.

To achieve low ohmic load on the Device under Test (DUT) in the range of a few µA, the following parameters are integrated: R_1=220 kΩ, R_2=100 kΩ and a detected parasitic capacitance of C=280 pF. This leads to a capacitive adaptation of $C_{1,\mathrm{ai}}$=127 pF.

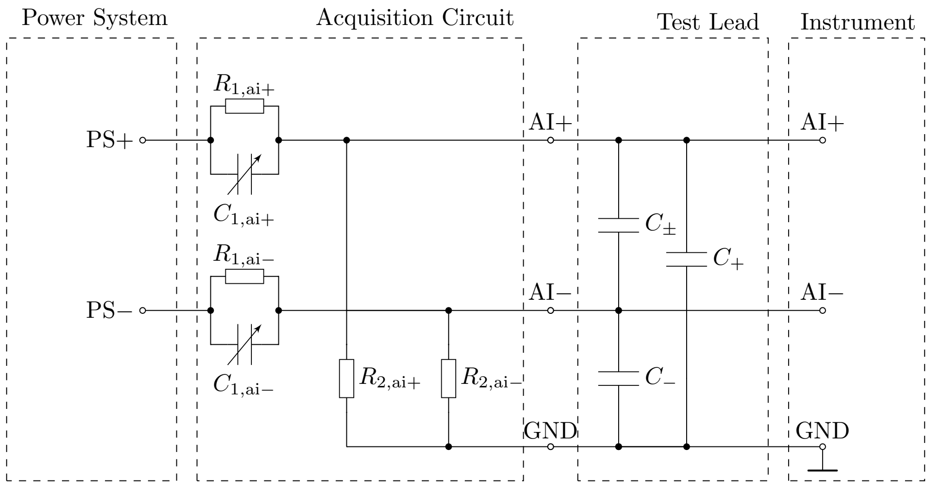


Figure A.2: Acquisition circuit for voltage scaling and bandwidth adjustment of the power system signal.

$$\frac{C_{1,\text{ai}+}}{C_{+}} = \frac{R_{2,\text{ai}+}}{R_{1,\text{ai}+}} \qquad \frac{C_{1,\text{ai}-}}{C_{-}} = \frac{R_{2,\text{ai}-}}{R_{1,\text{ai}-}} \tag{A.1}$$

A.3 Voltage-Scaled Converter Prototype

The voltage-scaling method is carried out based on a converter prototype [S2], [S3], [P7]. The 48/12 V PSFB converter is designed for a power of 1 kW. Multiple units are used to supply the power system test bench. This chapter presents the applied scaling method following the introduced convention of Section 4.3.2.

1. Establishing the ODE System

The Ordinary Differential Equation (ODE) system is established by means of the converter's average model. The average model is generated according to [63, 130].

Fig. A.3 presents the average model of the converter consisting of two galvanically isolated, though transformer-coupled circuits (High Voltage (HV) and LV). V_{in} is the voltage supply of the HV system and v_{o} is the converter's output voltage supplying the resistive load R_{L}. R_{eq} includes parasitic resistances of the converter such as the secondary side resistances R_{s} and rectifiers resistances R_{dss}. Furthermore, the leakage inductance of the transformer leads to a damping being expressed as switching frequency f_{s} dependent ohmic resistance according to (A.2). All ohmic resistances which are dependent on the duty cycle d are summarized in resistance R_{d}. HV system resistances R_{dsp}, R_{p} are scaled by the turns ratio n^2 as presented. Moreover, the secondary side rectifier's resistance R_{dss} is dependent on the duty cycle and, therefore, present within R_{d}.

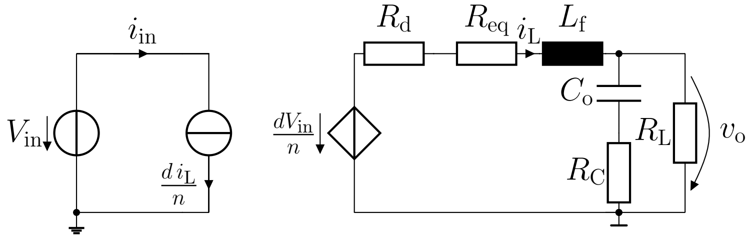


Figure A.3: Average model of the PSFB converter.

$$R_{\text{eq}} = \frac{4\, L_{\text{k}} f_{\text{s}}}{n^2} + R_{\text{dss}}\, \frac{1}{2} + R_{\text{s}} \qquad R_{\text{d}} = (2\, R_{\text{dsp}} + R_{\text{p}})\, \frac{d}{n^2} + R_{\text{dss}}\, \frac{d}{2} \tag{A.2}$$

The describing state-space system is shown in (A.3). It is further used to derive the transfer functions of interest.

$$\begin{bmatrix} -L_{\text{f}} & -R_{\text{c}}\, C_{\text{o}} \\ 0 & -\left(R_{\text{L}} + R_{\text{C}}\right) C_{\text{o}} \end{bmatrix} s \begin{pmatrix} i_{\text{L}} \\ v_{\text{C}} \end{pmatrix} = \begin{bmatrix} R_{\text{eq}} + R_{\text{d}} & 1 \\ -R_{\text{L}} & 1 \end{bmatrix} \begin{pmatrix} i_{\text{L}} \\ v_{\text{C}} \end{pmatrix} + \begin{pmatrix} -d/n \\ 0 \end{pmatrix} V_{\text{in}} \tag{A.3}$$

2. Extracting the Transfer Characteristics

To calculate the control-to-output-voltage v_{o}/d and control-to-inductor-current i_{L}/d transfer functions, small signal analysis is carried out. The duty cycle d becomes the input of the state-space system as shown in (A.4). The multiplication of R_{d} with states $\mathbf{x}$ results in second-order variables. Linear AC variations are assumed to be much smaller than the DC components. Second-order variables are much smaller than the linear first-order variables. Second-order terms are neglected. Consequently, R_{d} does not appear in state-space system (A.4). [130]

$$\begin{gathered} \begin{bmatrix} -L_{\text{f}} & -R_{\text{c}}\, C_{\text{o}} \\ 0 & -\left(R_{\text{L}} + R_{\text{C}}\right) C_{\text{o}} \end{bmatrix} s \begin{pmatrix} i_{\text{L}} \\ v_{\text{C}} \end{pmatrix} = \begin{bmatrix} R_{\text{eq}} & 1 \\ -R_{\text{L}} & 1 \end{bmatrix} \begin{pmatrix} i_{\text{L}} \\ v_{\text{C}} \end{pmatrix} + \begin{pmatrix} -V_{\text{in}}/n \\ 0 \end{pmatrix} d \\ \mathbf{A}_{\dot{\text{x}}}\, s\, \mathbf{x} = \mathbf{A}_{\text{x}}\, \mathbf{x} + \mathbf{B}\, u \\ G_{\text{u}\to\text{x}} = \left(\mathbf{A}_{\dot{\text{x}}}\, s - \mathbf{A}_{\text{x}}\right)^{-1} \mathbf{B} \end{gathered} \tag{A.4}$$

The transfer functions of states $\mathbf{x}$ in dependence of system input u (duty cycle d) are obtained by means of the expression (A.4). The solved transfer functions are shown in (A.5). For simplification, parameters R_1 and R_2 have been introduced as in (A.6).

$$\begin{aligned}\frac{v_\mathrm{o}}{d} = (R_\mathrm{C}C_\mathrm{o}+1)\frac{v_\mathrm{C}(s)}{d(s)} &= \frac{V_\mathrm{in}R_\mathrm{L}}{n}\frac{R_\mathrm{C}C_\mathrm{o}\,s+1}{R_2\,L_\mathrm{f}C_\mathrm{o}\,s^2+(L_\mathrm{f}+R_1\,C_\mathrm{o})\,s+R_\mathrm{L}+R_\mathrm{eq}} \\ \frac{i_\mathrm{L}}{d} &= \frac{V_\mathrm{in}}{n}\frac{R_2\,C_\mathrm{o}\,s+1}{R_2\,L_\mathrm{f}C_\mathrm{o}\,s^2+(L_\mathrm{f}+R_1\,C_\mathrm{o})+R_\mathrm{L}+R_\mathrm{eq}}\end{aligned} \tag{A.5}$$

$$\begin{aligned}R_1 &= R_\mathrm{L}\,R_\mathrm{C}+R_\mathrm{eq}\,(R_\mathrm{L}+R_\mathrm{C}) \\ R_2 &= R_\mathrm{L}+R_\mathrm{C}\end{aligned} \tag{A.6}$$

3. Identifying the Influence of Scaling on the Dynamics

When performing voltage scaling of the converter, the turns ratio n necessarily needs to be adapted in the same way the input voltage V_in is adapted. This idea arises due to the fraction V_in/n as DC gain as multiplier of both transfer functions (A.5). Furthermore, the leakage inductance L_k and primary resistances R_dsp, R_p as part of R_eq and R_d (A.2) need to be scaled when n is changing due to their analytic expressions. Both need to be scaled by the square of the scaling factor to keep the transfer functions identical.

Since the damping resistance in dependence of L_k within R_eq is three magnitudes bigger than resistances of R_d, only L_k needs to be scaled and primary resistances are neglected. Dependencies on L_k, n are highlighted in blue in (A.2), (A.3), (A.4), (A.5), (A.6).

4. Scaling Ratio and Feasibility

Keeping the same dynamics while scaling the converter to a lower voltage requires maintaining the characteristic polynomial of the transfer function (A.5).

Scaling the input voltage from 400 V to 48 V is equal to a downscale of $25/3$. Turns ratio n has to be reduced. Auxiliary parameters R_1, R_2 (A.6) depend on R_eq which in turn depend on n. Only changing the turns ratio n will change natural frequency and damping as the influence of L_k within R_eq strongly depends on the ratio of L_k and n^2. The leakage inductance L_k also needs to be changed by $(25/3)^2$.

5. Physical Implementation of a Feasible Scaling Ratio

In practice a turns ratio of 2.4 means the number of turns has to be at least 12:5 primary-to-secondary, but the scaled leakage inductance 79.2 nH cannot be achieved. To achieve a smaller L_k, turns ratio n is rounded up to 3, leading to a downscaling factor of $20/3$. The leakage inductance value then is 123.8 nH, being a reasonable value for a turns ratio of 3:1 primary-to-secondary.

The DC gain V_{in}/n then only is 80 % of the original one reducing the DC steady-state value, however dynamic properties are kept the same. That applies above all for oscillations, damping ratio, settling time. The deviating gain can be corrected with a programmable gain within the Electronic Control Unit (ECU).

6. Verifying the Scaling Results

The control-to-output-voltage transfer function v_o/d is visualized in Fig. A.4 for both the original HV converter (400/20 V) and the scaled converter (48/16 V). The gain $|G|$ and the phase φ show similar characteristics in frequency domain. The deviating DC gain is noticeable for low frequencies below 1 kHz. The average model generated transfer characteristics (dashed) are compared to the switched model transfer function for verification purposes (solid lines). Deviations in the phase φ at the converter's switching frequency of 75 kHz (original) and its multiples are visible. A phase margin at 16.1 kHz and an anti-resonance at 3.8 kHz are obtained from both systems.

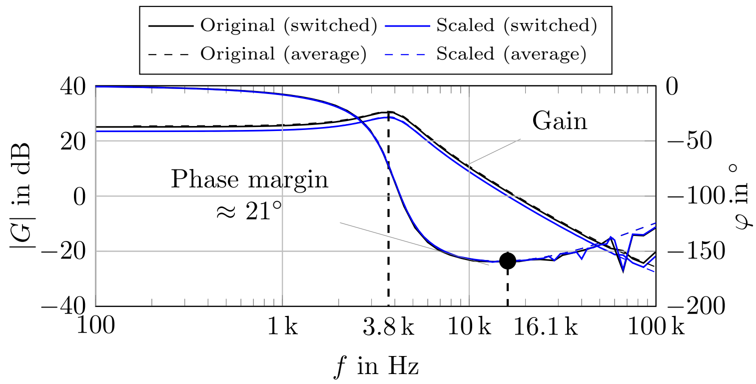
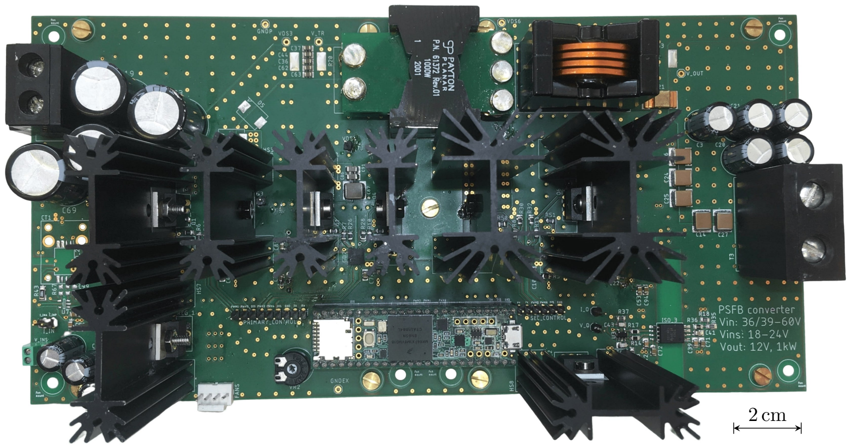


Figure A.4: Control-to-output-voltage transfer function of the original and scaled converter.

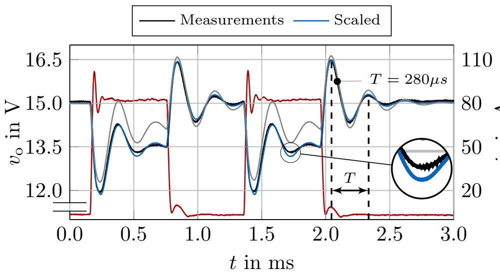
A prototype of the scaled converter was built up to further verify the scaling results and to physically supply the power system test bench. The prototype converter is presented in Fig. A.5a. Parameters of the original and scaled converter, as well as the physical implementation, are contrasted in Tab. A.2. All converters also include a primary resistance of R_p=200 µΩ, being the Equivalent Series Resistance (ESR) of the transformers blocking capacitor.

The measured values of the physical implementation of the scaled converter differ from calculated ones (scaled) due to manufacturing tolerances. To get closer to the original HV converter, further measures could be implemented. Especially switch resistances R_{dsp}, R_{dss} can be reduces by parallel MOSFETs.

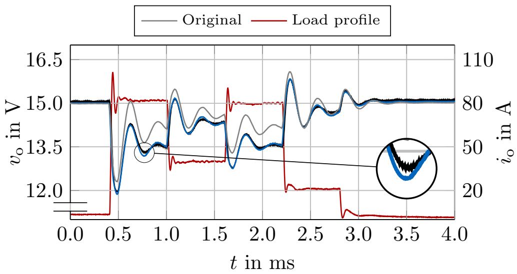
Fig. A.5 visualizes the open-loop response of the converter's output voltage for repeated (Fig. A.5b) and alternating pulses (Fig. A.5c). The measurements on the hardware prototype, the simulation results of the scaled converter and the original HV converter



(a) Top view of the PSFB converter prototype developed by B. Haj Ali.



(b) Repeated load pulses at full load.



(c) Alternating load pulses.

Figure A.5: Photo of the PSFB converter prototype. Open-loop response of the output voltage contrasted to the original and scaled converter simulations to load pulse scenarios.

are contrasted. The underlying red line highlights the injected load current. The full power of the converter is drawn at a current of 80 A. This corresponds to 1 kW.

The scaled converter model fits very well to the measurements. Deviations of less than 1 % occur during the load pulse tests. A larger deviation occurs when contrasting the scaled prototype to the original HV system. The elevated switch resistances of the implementation cause the differences in particular. However, the system dynamics in form of oscillation amplitudes, frequency and settling time can be portrayed sufficiently.

Table A.2: Parameters of the HV original, scaled and prototype converter.

	n	L_f	C_o	R_s	R_{dsp}	R_{dss}	R_C	L_k
Prototype	3	1.45 µH	1111 µF	1.6 mΩ	6.5 mΩ	5.1 mΩ	2.0 mΩ	100 nH
Scaled	3	1.50 µH	1110 µF	2.1 mΩ	5.2 mΩ	3.4 mΩ	0.9 mΩ	124 nH
Original	20	1.50 µH	1110 µF	1.0 mΩ	1.0 mΩ	3.0 mΩ	1.0 mΩ	5.5 µH

A.4 Power System Test Bench

This chapter contains photos of the power system test bench. Fig. A.6 shows the DUT consisting of the BMW iX wiring harness and selected components integrated into an aluminum frame. Photos were taken from different perspectives being visualized with corresponding arrows or points.

Tab. A.3 includes the introduced nomenclature of associated components. A grouping was made according to control & acquisition, vehicular components, power distribution and hardware prototypes. The following figures contain labels for allocation. Figures A.7, A.8, A.9, A.10, A.11, A.12 show all areas indicated with arrows in Fig. A.6.

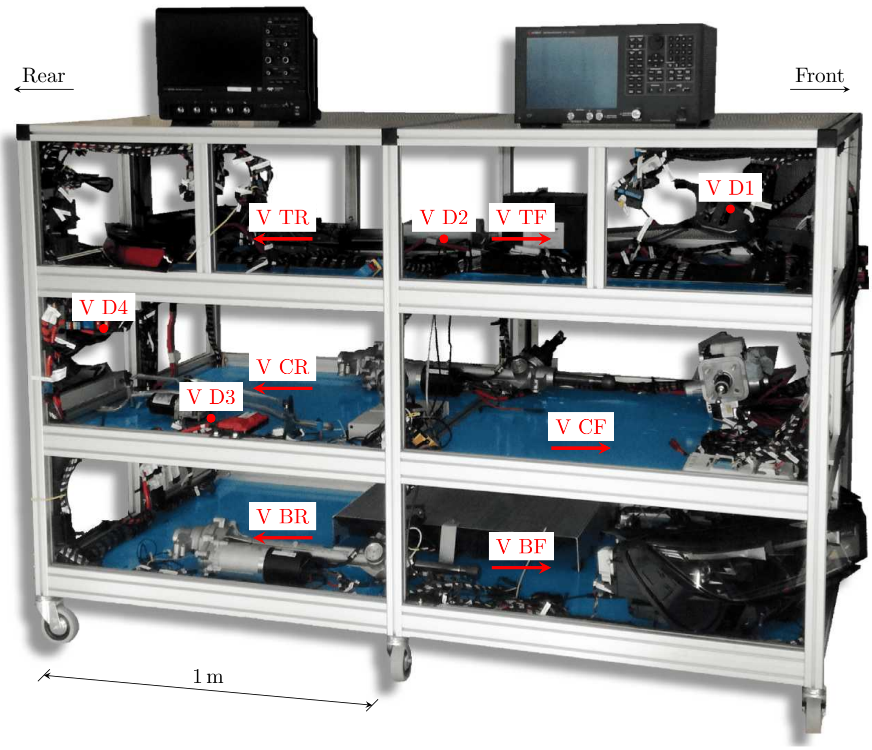


Figure A.6: Overview of the power system test bench with highlighted perspective views being photographed and documented in this chapter.

A Control & Acquisition	
1_A	Analog Adapter
2_A	Communication-Simulation Connector
3_A	Voltage Probe
4_A	Current Probe

B Vehicular Power System Components			
1_B, 2_B	HLi, TLi	6_B	WIP
3_B	EPS	7_B	RAS
4_B	EBP	8_B	APA
5_B	EFD	9_B	Central ECU

C Power Distribution			
1_C	PD1	5_C	BBF
2_C	PD2	6_C	BBC
3_C	PD3	7_C	BBR
4_C	PD4		

D Hardware Prototypes			
1_D	Master	5_D	Filter BBC
2_D	Slave 1	6_D	Filter PD3
3_D	Slave 2	7_D	FID
4_D	Filter PD1		

Table A.3: The established vehicular power system test bench consists of control & acquisition technology (A), a vehicular components (B) with power distributors (C) and hardware prototypes for supply, stabilization and load emulation (D).

More detailed views of some selected angles are visualized in figures A.13, A.14, A.15, A.16, A.17, A.18, A.19. Their locations of photography are marked with red dots in Fig. A.6.

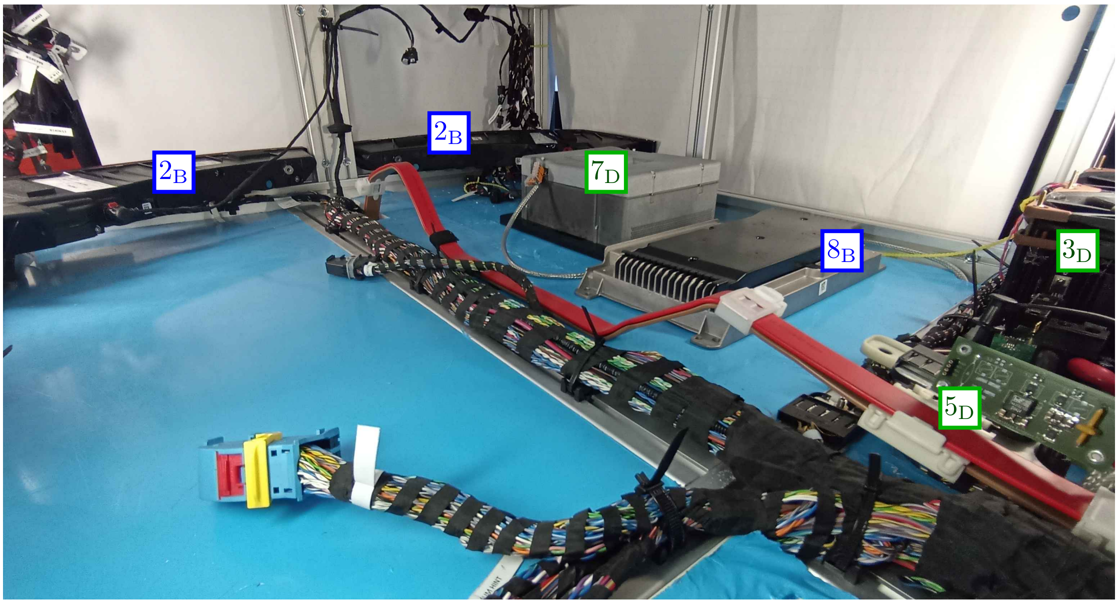


Figure A.7: Power system test bench view TR (Top Rear).

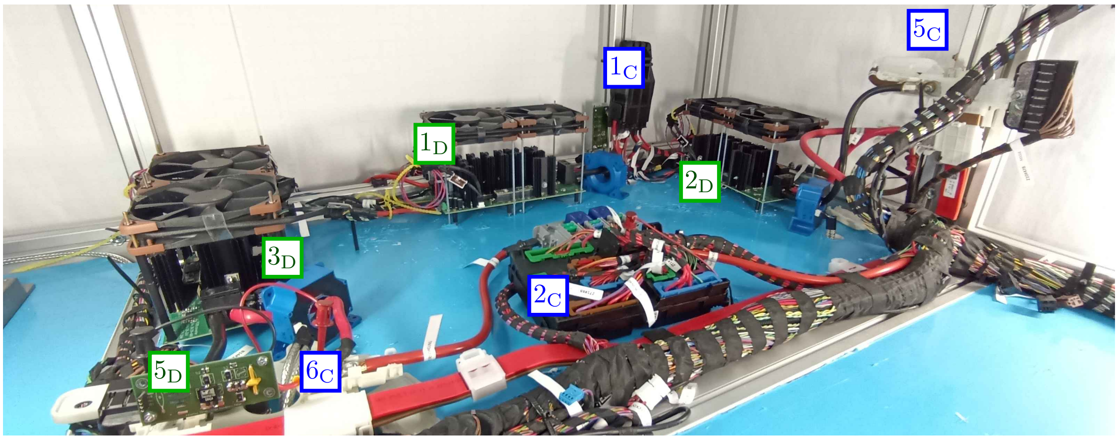


Figure A.8: Power system test bench view TF (Top Front).

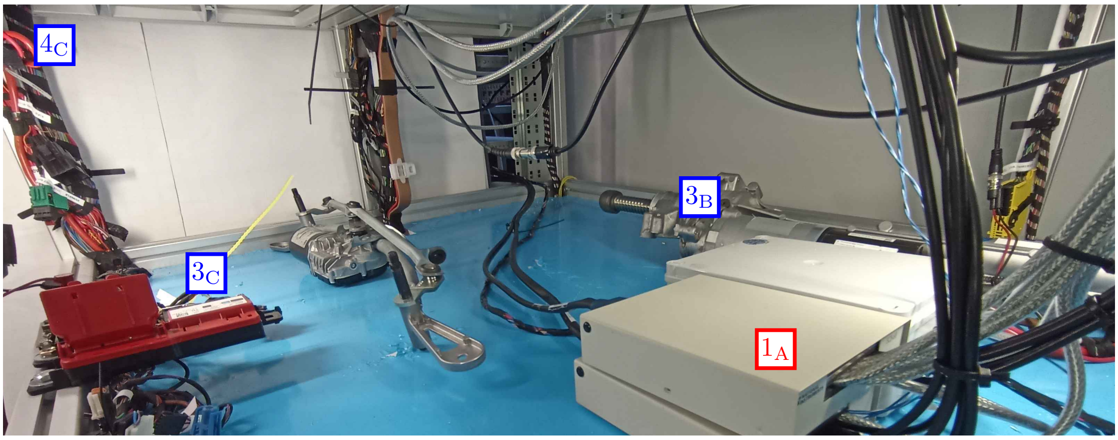


Figure A.9: Power system test bench view CR (Center Rear).

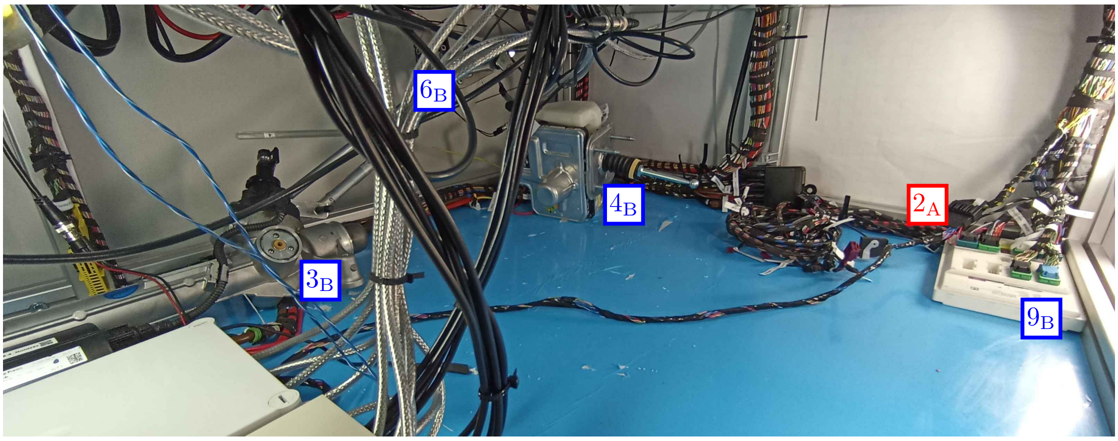


Figure A.10: Power system test bench view CF (Center Front).

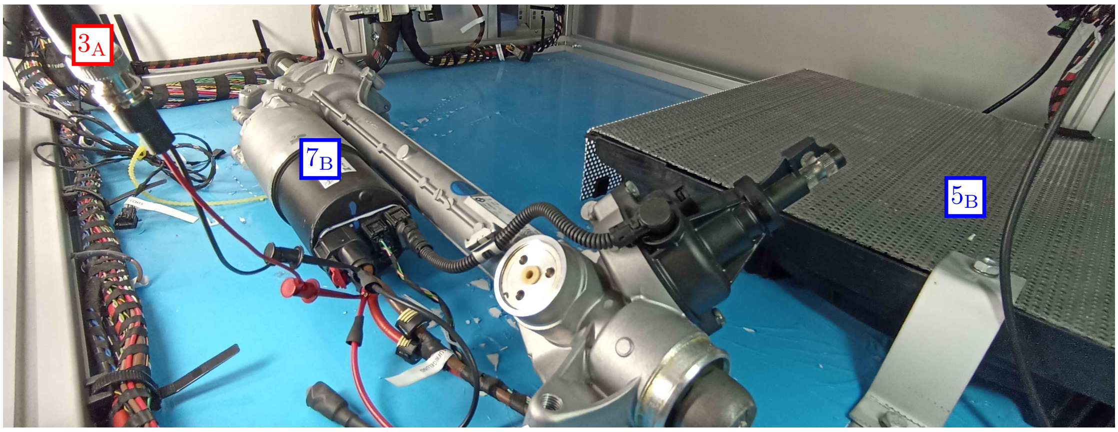


Figure A.11: Power system test bench view BR (Bottom Rear).

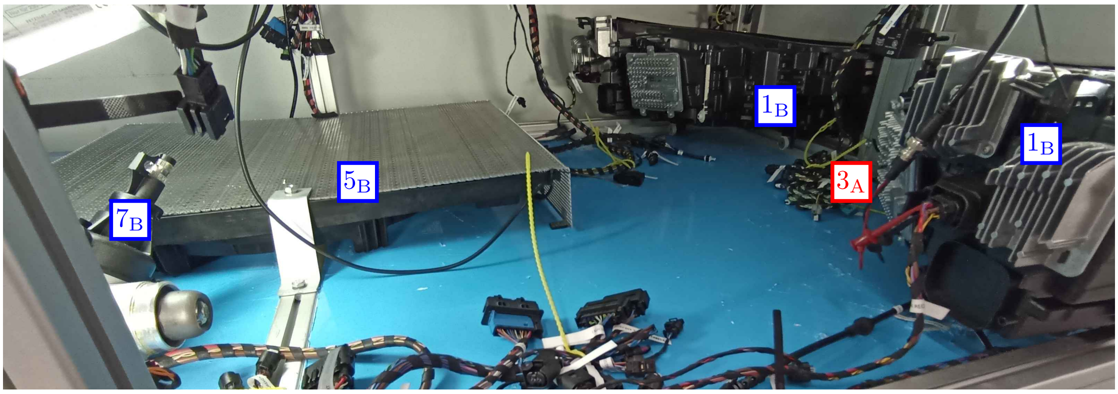


Figure A.12: Power system test bench view BF (Bottom Front).

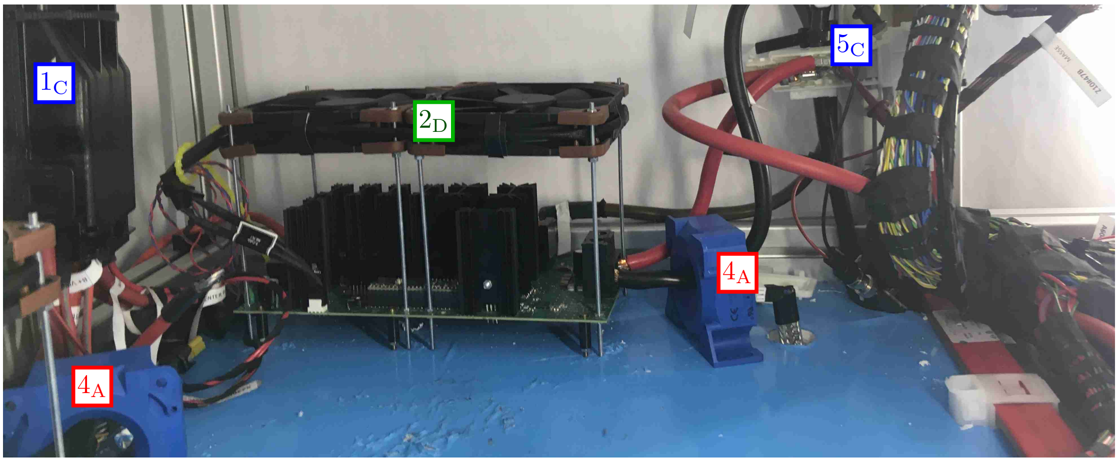


Figure A.13: Detailed view of the point D1 (power distributor BBF and Slave 1 converter).

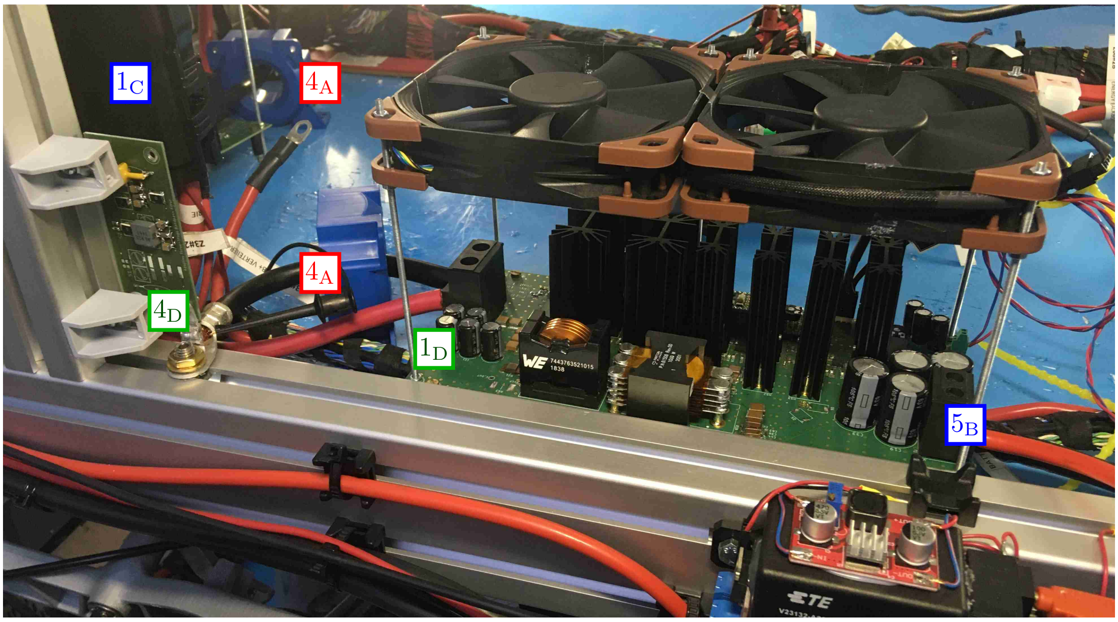


Figure A.14: Detailed view of the point D1 (power distributor PD1, Master converter and band-pass filter PD1).

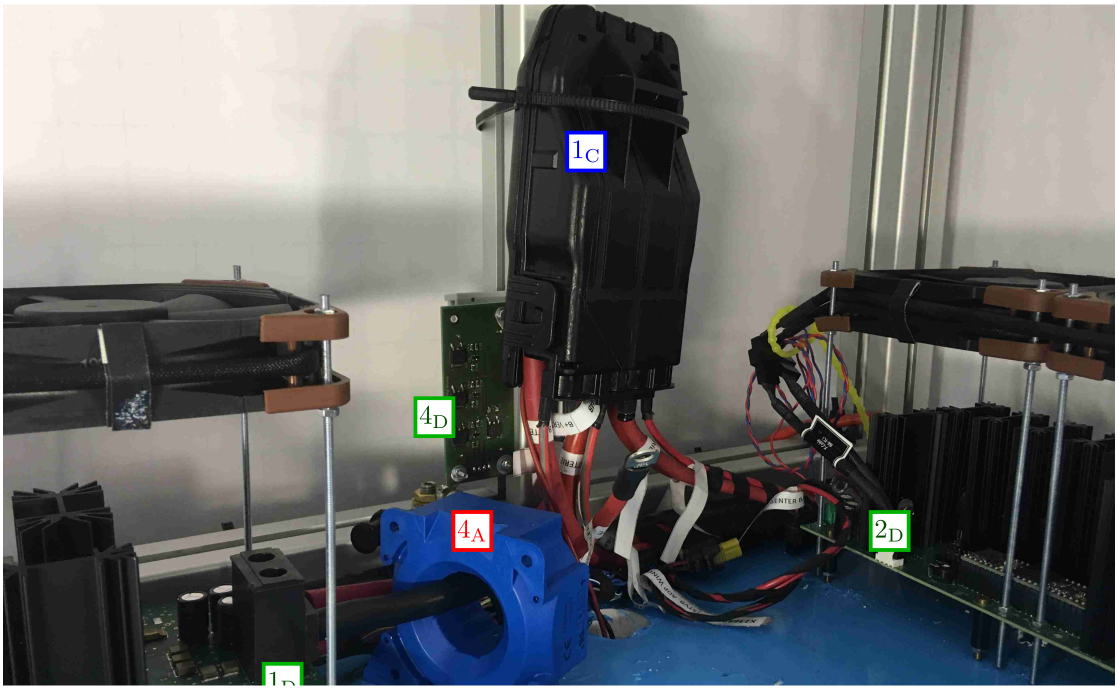


Figure A.15: Detailed view of the point D1 (power distributor PD1 and band-pass filter PD1).

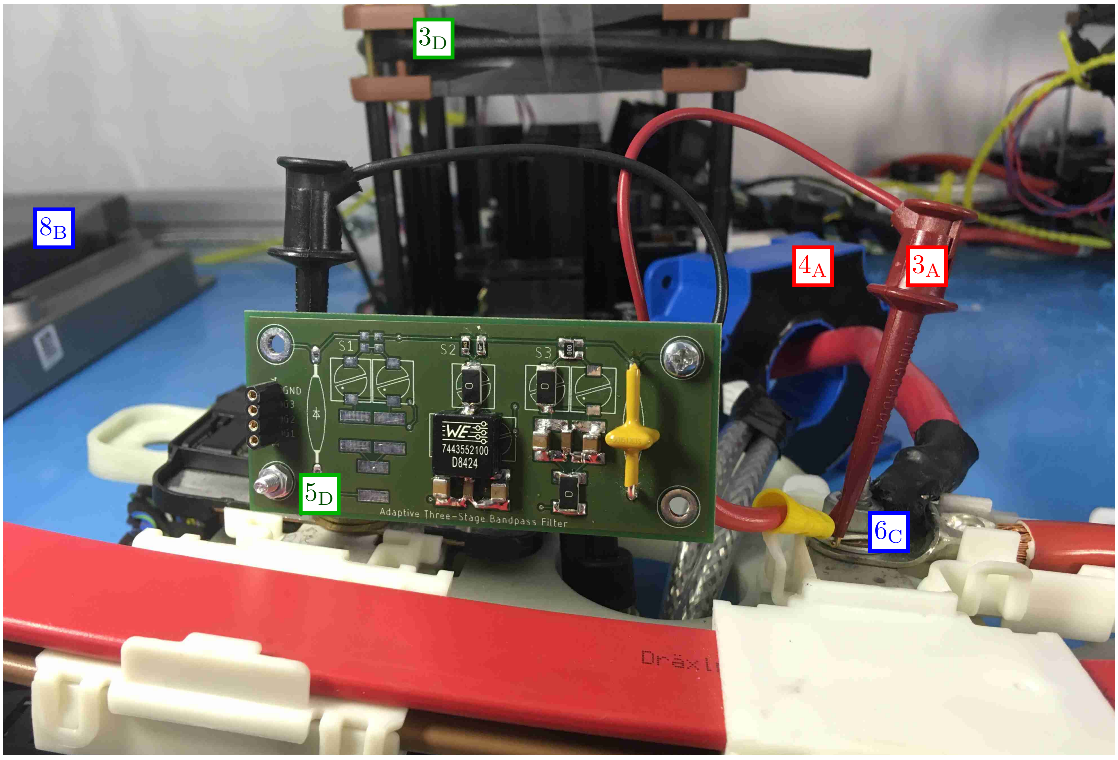


Figure A.16: Detailed view of the point D2 (power distributor BBC with band-pass filter BBC and converter Slave 2).

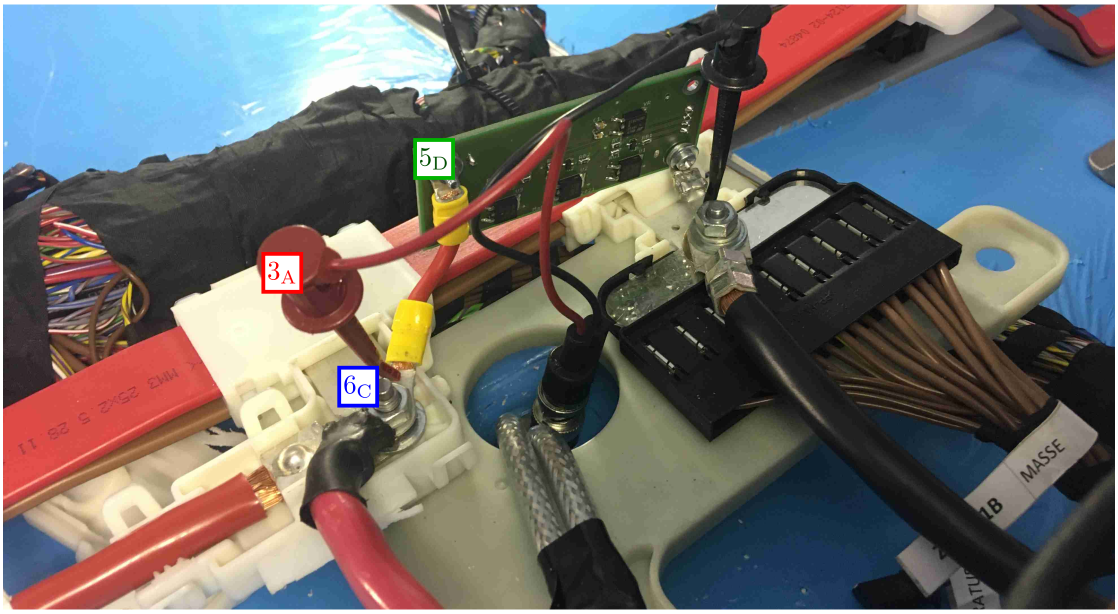


Figure A.17: Detailed view of the point D2 (power distributor BBC with band-pass filter BBC).

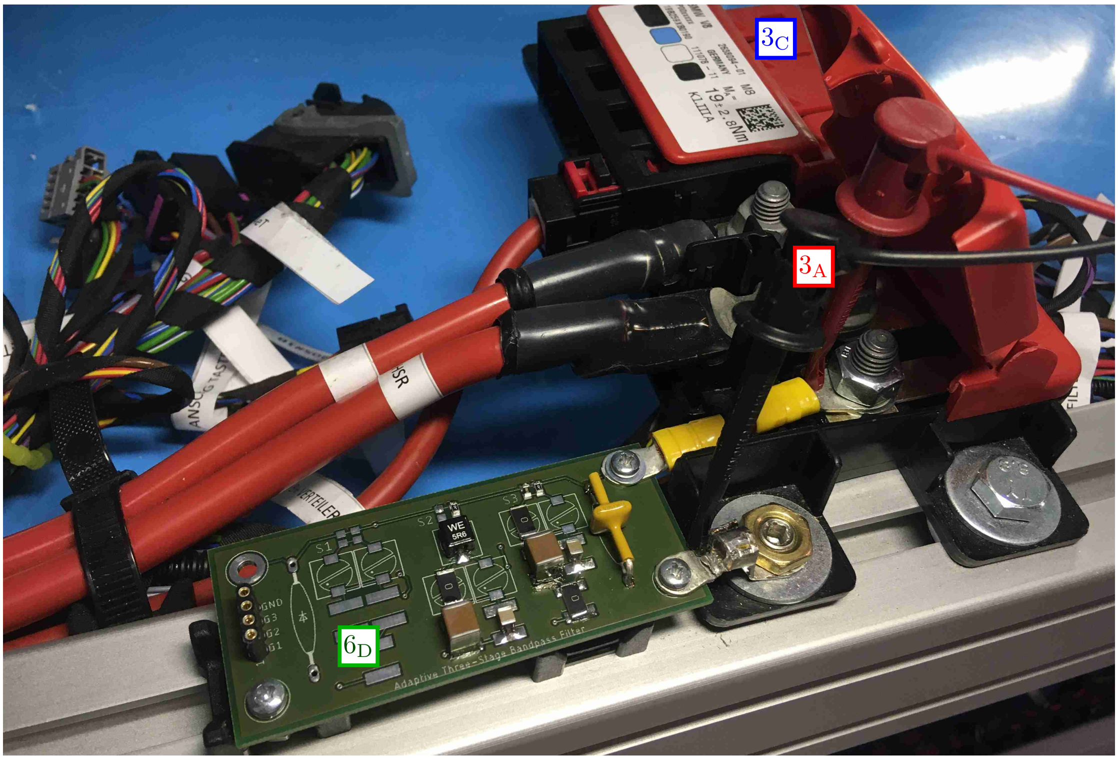


Figure A.18: Detailed view of the point D3 (power distributor PD3 with band-pass filter PD3).

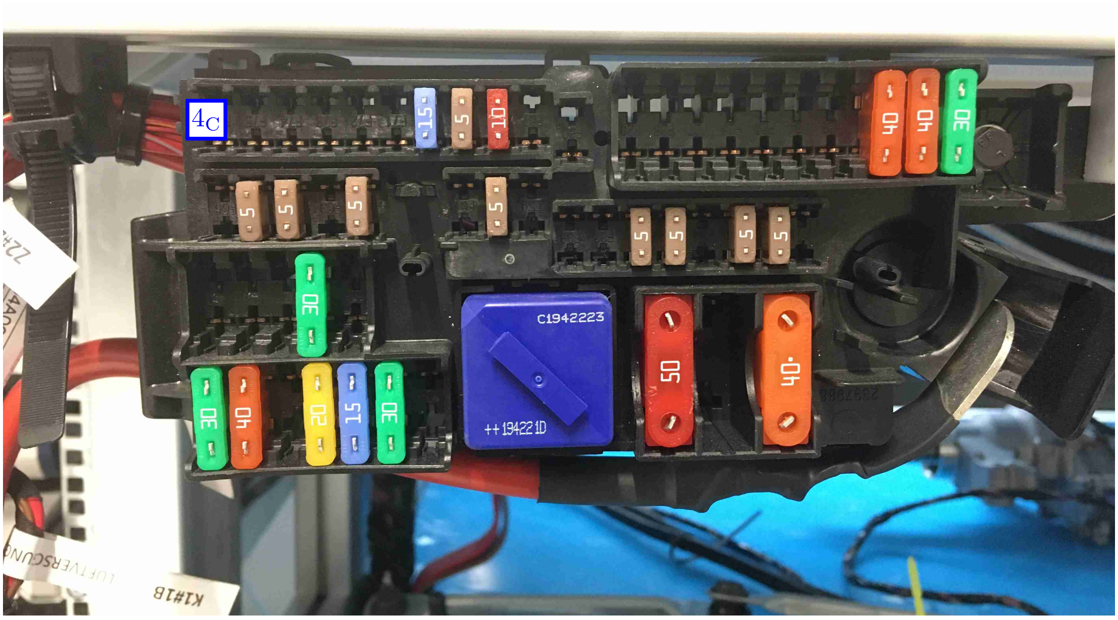
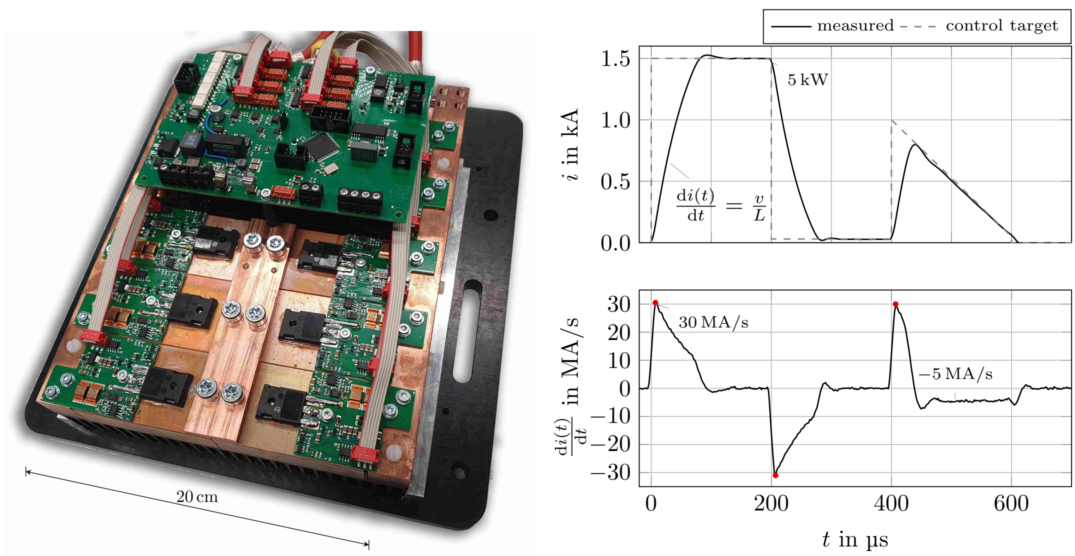


Figure A.19: Detailed view of the point D4 (power distributor PD4).

A.5 Fault Injection Device

For the injection of specified current profiles, L. Peters developed a Fault Injection Device (FID) being published in [P12]. The device consists of parallel controllable Trench Power MOSFETs IXYS IXTH500N04T2. They are each able to carry a current of 150 A and to dissipate a power of 500 W. The analog PID controller follows a control target up to its bandwidth restriction of 20 kHz. However, the bandwidth strongly depends on the connected system to be controlled. The FID is presented in Fig. A.20a. A simplified equivalent circuit is shown in Fig. A.21. The input capacitance is shown with C_{p}, $R_{\mathrm{p,c}}$. The MOSFET's controllable Drain-Source resistance is visualized as $R_{\mathrm{p,s}}$ in series with the switch S_{p}.

The device operates as a load between two terminals of a connected power supply. Compared to conventionally available electronic loads, much steeper current slew rates can be achieved. This qualifies the device to simulate dynamic error processes such as short circuits or current pulses. Moreover, the FID can be used to validate models of vehicular power system components as demonstrated in [P9].



(a) The FID prototype developed by L. Peters. **(b)** Measurements and the control reference.

Figure A.20: Photo and measurements of the Fault Injection Device (FID).

To measure high dynamic current pulses, a test setup consisting of Power Supply Electro Automatik EA-PSI 9040 3.3 kW, parallel super capacitor Eaton XLR 170 F and the FID connected via 30 cm low-inductive, low-resistive cables with a cross-section of 25 mm^2 was built up. Fig. A.20b shows the measurement results contrasted to the control target. A maximum current slew rate of about 30 A/µs could be achieve. This current slew rate is majorly limited by the self-inductance L of the supply cable and the supercapacitors voltage v.

Furthermore, a maximum power dissipation of 5 kA at 1500 A and a voltage of 3.3 V were measured. The voltage drops from 17 V to 3.3 V due to the cable and supercapacitor's internal resistance of about 10 mΩ. The second triangular current graph visualizes the control behavior of the FID with a control target of −5 A/µs.

Moreover, the device is able to carry a maximum current of 1000 A for a maximum of 15 s. A copper heatsink of a weight of 5 kg is used as the thermal capacitance to cushion thermal load peaks, while a minimum pulse length of 20 µs can be achieved.

A.6 Pulse Response Analysis

This chapter gives a brief overview of the performed pulse response analysis. The pulse response is explained using the example visualized in Fig. A.21. The FID is used to inject a high dynamic current pulse at a chosen Access Point (AP). Distributed voltages and the pulse current i_{pulse} are measured in time domain to further carry out a frequency domain analysis after signal processing.

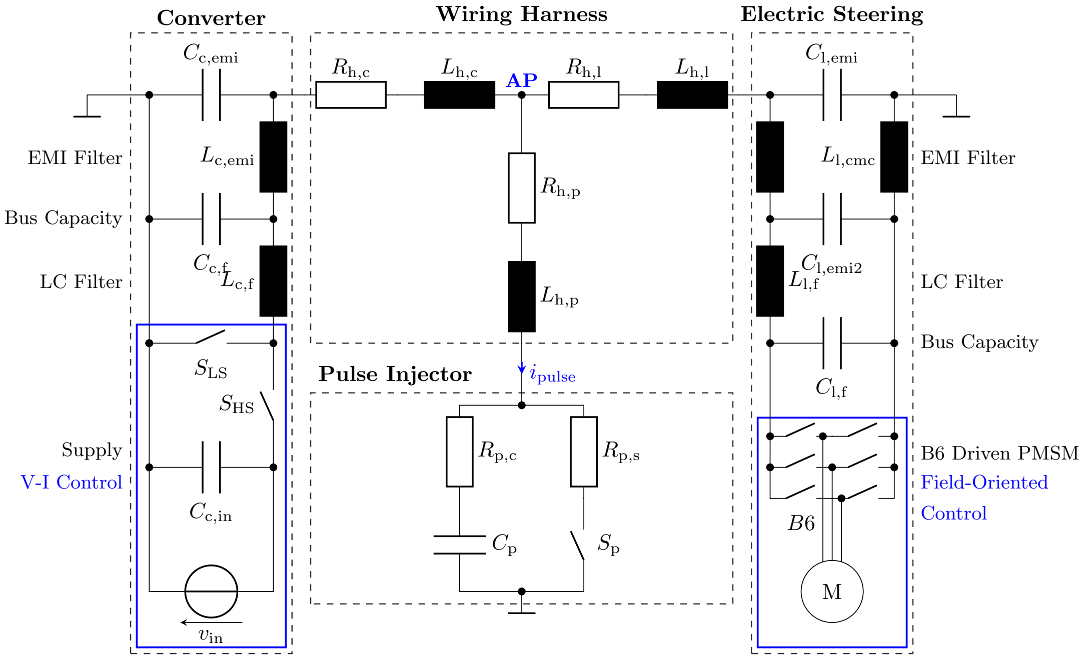


Figure A.21: Simplified model of a converter supplied automotive steering. A power electronic current pulse injection device is used to determine the systems impedance based on a measured short-time disturbance.

Fig. A.22 contrasts the time domain measurements of the pulse current and voltage (top). Signals are filtered by means of 22 kHz (center) and 50 kHz (bottom) high-pass filters. By rescaling the signal amplitude to the maximum vertical scaling of the oscilloscope's Analog-to-Digital Converter (ADC), the quantization noise can be significantly reduced.

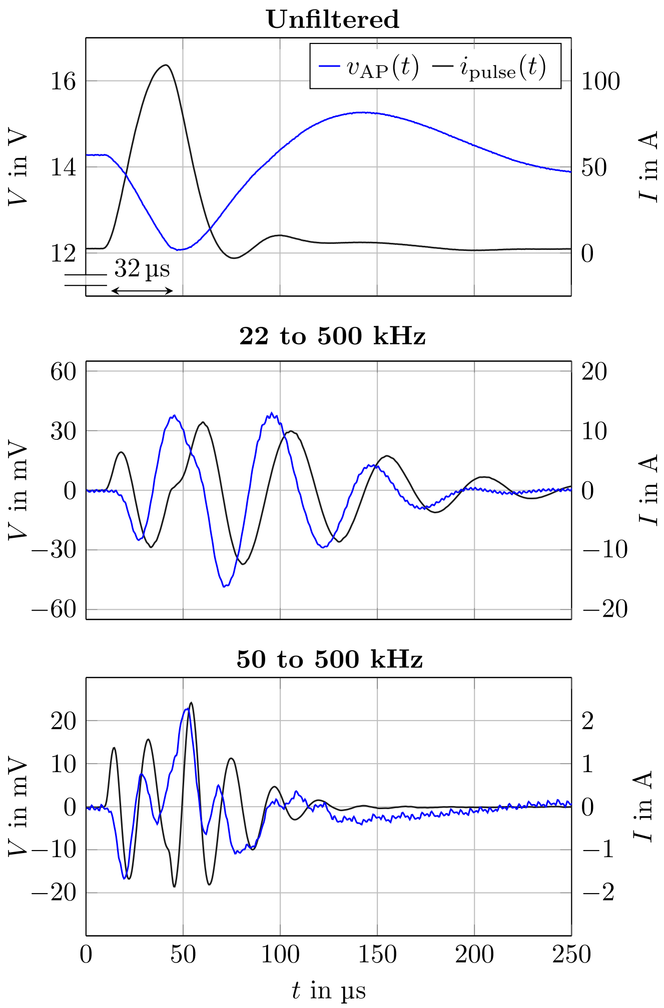


Figure A.22: Time domain measurements of current and voltage with unfiltered, 22 kHz and 50 kHz high-pass filtered measurement set-up.

Frequency domain values are generated by Discrete Fourier Transform (DFT) (if applicable). Fig. A.23 shows the amplitude and phase of the transfer impedance Z. The result contains multiple disturbances due to the current pulse width $T_\mathrm{p} = 32\,\mu\mathrm{s}$ and the switching frequency of the DC/DC converter (power supply) $f_\mathrm{S} = 200\,\mathrm{kHz}$. The high-frequency behavior of the transfer impedance can only be generated by high-pass filtered signals (blue). The calculated transfer impedance without applied high-pass filters can only be verified below 20 kHz. Above, high-pass filters need to be applied. An anti-resonance at 70 kHz would remain undetected without a high-pass filter.

Consequently, the impedance spectroscopy using the pulse injection method needs a compensation of noise. Both random and quantization noise can be reduced by applying multiple pulse measurements. However, a lot of pulses need to be injected to sufficiently suppress the noise. By applying high-pass filters and scaling the filtered signals to the maximum vertical scale of oscilloscope's ADCs, high-frequency disturbances can be corrected.

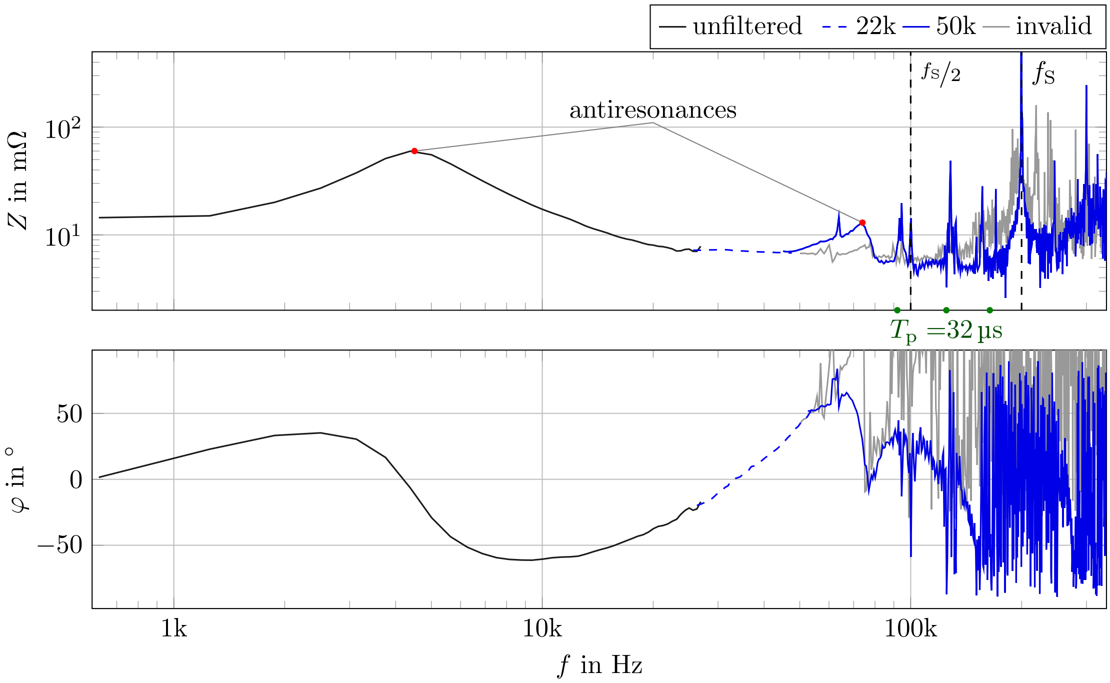


Figure A.23: DFT transformed of the measured signal. The access points impedance consists of three short time disturbance measurements of unfiltered, 22 kHz and 50 kHz high-pass filtered.

Fig. A.24 shows two high-pass filters (red) attached to a Lecroy® oscilloscope. The power subsystem's structure is similar the equivalent circuit of Fig. A.21. A DC/DC converter (not visible in the figure) supplies an Electric Power Steering (EPS) (right in Fig. A.24). The FID (left in Fig. A.24) injects a high-dynamic current pulse by means of linear mode controlled MOSFETs. The voltages are measured by means of passive voltage probes and the current is measured with current probes.

A closer view on applied high-pass filters is presented in Fig. A.25. Filters (red) are attached to an oscilloscope. The oscilloscope's screen contrasts time domain measurements (top) and frequency domain transformed signals (bottom).

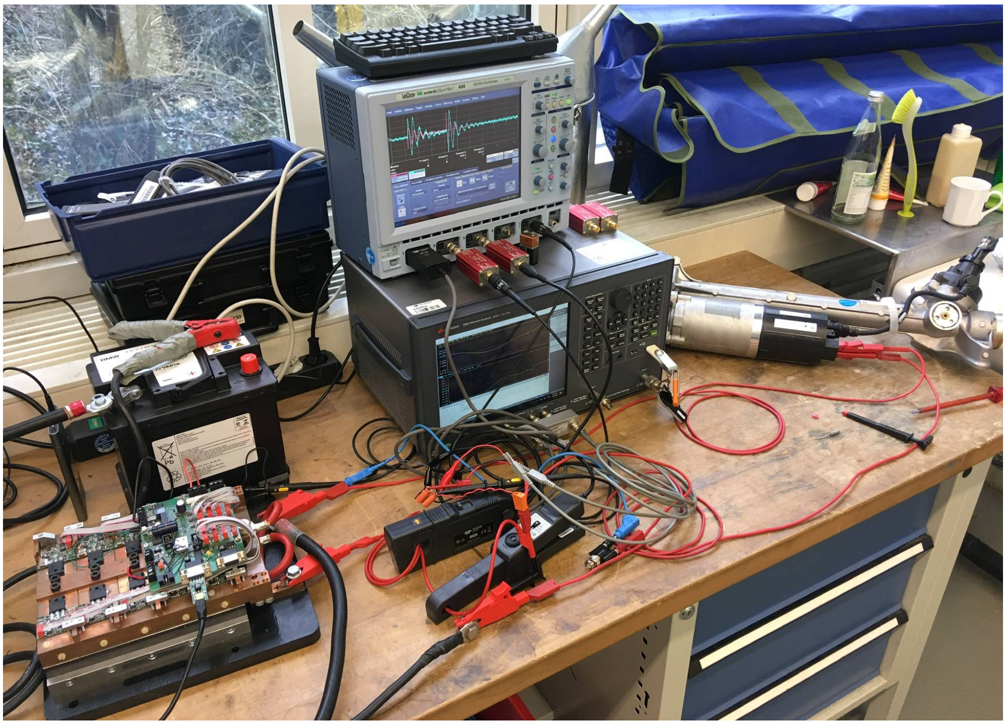


Figure A.24: Power subsystem consisting of a converter supplied EPS with the FID.

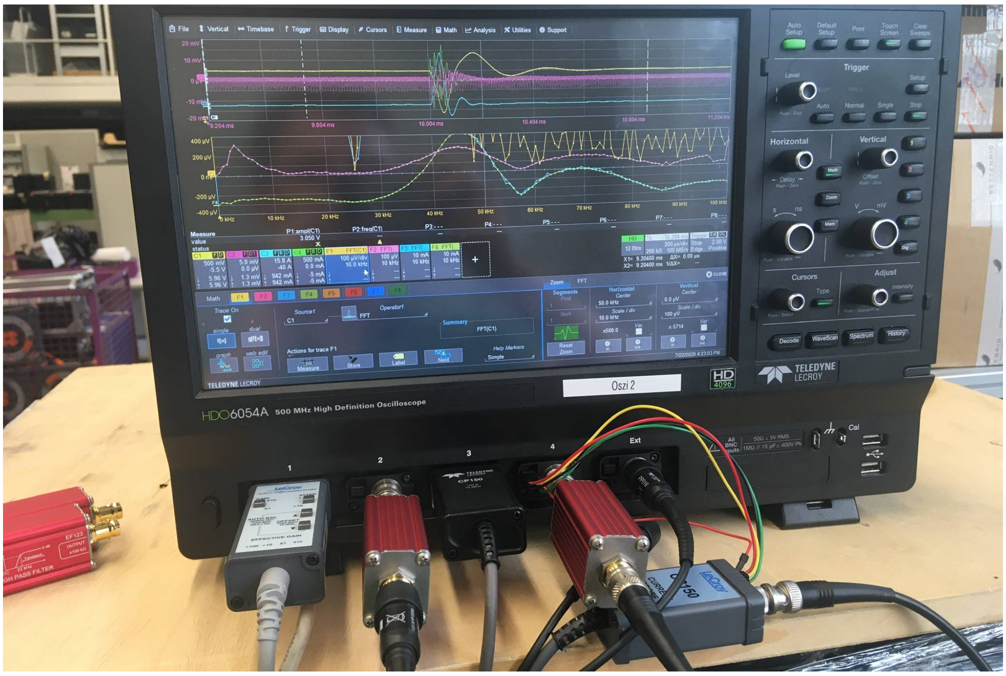


Figure A.25: Oscilloscope with attached high-pass filters (red).

A.7 Double-Integral Sliding Mode Control

The Double-Integral Sliding Mode Control (DISMC) design is based on a simplified state-space function (A.7) of the PSFB converter. Its circuit was presented in Appendix A.3 and in Section 3.3. The state-space system represents the on- and off-states by the variable u.

This appendix section provides a brief summary of Publication [P10]. Yue Sun's Masters Thesis [S4] gives more details about the Sliding Mode Control (SMC) methodology.

$$\begin{bmatrix} \frac{i_\mathrm{L}}{\mathrm{d}t} \\ \frac{\mathrm{d}v_\mathrm{o}}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_\mathrm{f}} \\ \frac{1}{C_\mathrm{o}} & -\frac{1}{Z_\mathrm{o}C_\mathrm{o}} \end{bmatrix} \begin{bmatrix} i_\mathrm{L} \\ v_\mathrm{o} \end{bmatrix} + \begin{bmatrix} \frac{V_\mathrm{in}}{nL_\mathrm{f}} \\ 0 \end{bmatrix} u \tag{A.7}$$

Sliding mode control applied on converters leads to a steady-state error according to [142, 143]. In order to prevent the error, Wang [142] introduces a new design of the SMC. Another integral term e_4 is introduced to design the sliding surface. Corresponding control objects $\mathbf{E}$ and derivatives $\dot{\mathbf{E}}$ are shown in (A.8).

$$\mathbf{E} = \begin{cases} e_1 = V_\mathrm{ref} - v_\mathrm{o} \\ e_2 = \dot{e_1} = -\frac{1}{C_\mathrm{o}} L_\mathrm{f} + \frac{1}{Z_\mathrm{o}C_\mathrm{o}} v_\mathrm{o} \\ e_3 = \int e_1 dt = \int (V_\mathrm{ref} - v_\mathrm{o}) dt \\ e_4 = \int\int e_1 dtdt = \int\int (V_\mathrm{ref} - v_\mathrm{o}) dtdt \end{cases} \qquad \dot{\mathbf{E}} = \begin{cases} \dot{e_1} = e_2 \\ \dot{e_2} = -\frac{1}{C_\mathrm{o}} \dot{i}_\mathrm{L} + \frac{1}{Z_\mathrm{o}C_\mathrm{o}} \dot{v}_\mathrm{o} \\ \dot{e_3} = e_1 \\ \dot{e_4} = e_3 \end{cases} \tag{A.8}$$

The state-space system of $\mathbf{E}$ is shown in (A.9). It is derived by substituting (A.7) into (A.8).

$$\begin{bmatrix} \dot{e_1} \\ \dot{e_2} \\ \dot{e_3} \\ \dot{e_4} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ -\frac{1}{C_\mathrm{o}L_\mathrm{f}} & -\frac{1}{Z_\mathrm{o}C_\mathrm{o}} & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \\ e_4 \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{V_\mathrm{in}}{nC_\mathrm{o}L_\mathrm{f}} \\ 0 \\ 0 \end{bmatrix} u + \begin{bmatrix} 0 \\ -\frac{V_\mathrm{ref}}{C_\mathrm{o}L_\mathrm{f}} \\ 0 \\ 0 \end{bmatrix} \tag{A.9}$$
$$\dot{\mathbf{E}} = \mathbf{AE} + \mathbf{B}u + \mathbf{D}, \; \mathbf{E} = \begin{bmatrix} e_1 & e_2 & e_3 & e_4 \end{bmatrix}^T$$

The coefficient vector $\mathbf{G}$ records the sliding surface s and its derivative $\dot{s}$ in (A.10).

$$\begin{aligned} s &= g_1e_1 + g_2e_2 + g_3e_3 + g_4e_4 = \mathbf{GE} \\ \mathbf{G} &= \begin{bmatrix} g_1 & g_2 & g_3 & g_4 \end{bmatrix}, \; \{g_1, g_2, g_3, g_4 \,|\, g_i > 0\} \\ \dot{s} &= \mathbf{G}(\mathbf{AE} + \mathbf{B}u + \mathbf{D}) \end{aligned} \tag{A.10}$$

The linear equivalent controller u_{equ} is derived by satisfying $\dot{s} = 0$. It only contains e_1, e_2, e_3 and a constant term. The second integral of e_4 does not exist. Single-Integral SMC does not include e_3. This justifies the steady-state error for Single-Integral SMC. The equivalent controller acts as linearly while the switching controller acts as a nonlinear controller. The linear controller u_{equ} contains e_3 as shown in (A.11).

$$\begin{aligned} u_{\text{equ}} &= -(\mathbf{GB})^{-1}\mathbf{G}(\mathbf{AE}+\mathbf{D}) \\ &= \frac{nC_{\text{o}}L_{\text{f}}}{V_{\text{in}}}\frac{g_3}{g_2}e_1 + \frac{nC_{\text{o}}L_{\text{f}}}{V_{\text{in}}}\left(\frac{g_1}{g_2} - \frac{1}{Z_{\text{o}}C_{\text{o}}}\right)e_2 + \frac{n}{V_{\text{in}}}v_{\text{o}} + \frac{nC_{\text{o}}L_{\text{f}}}{V_{\text{in}}}\frac{g_4}{g_2}e_3 \\ &= k_1e_1 + k_2e_2 + k_3v_{\text{o}} + k_4e_3 \\ u_{\text{sw}} &= l\,\text{sign}(s),\ \ l > 0 \end{aligned} \tag{A.11}$$

The switching controller u_{sw} satisfies the existence condition. The parameter l is the coefficient of the function $\text{sign}(s)$ as presented in (A.11). The structure of the designed DISMC with both equivalent and switching controllers is visualized in Fig. A.26.

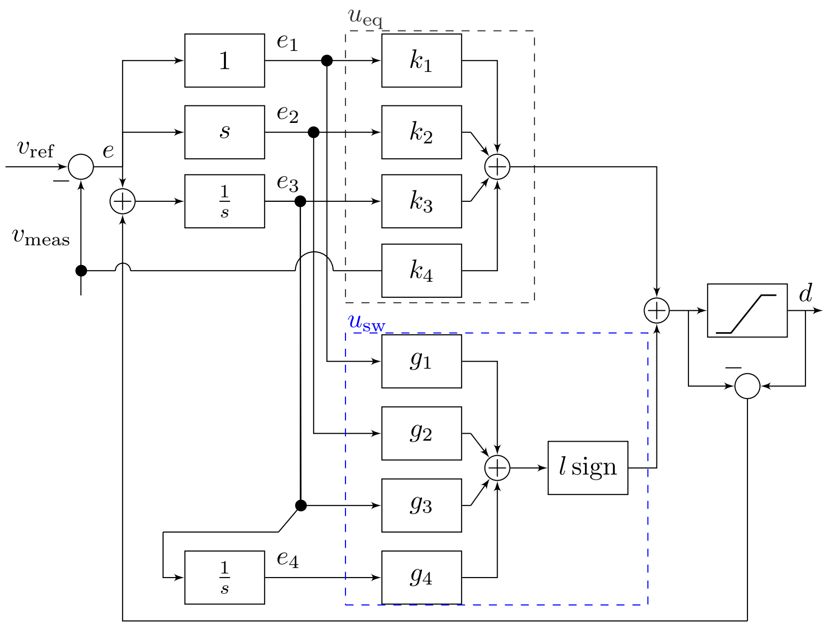


Figure A.26: Double Integral Sliding Mode Control (DISMC).

The existence condition is applied to calculate the parameters of the switching controller. The existence condition is verified for $s\dot{s} < 0$ as stated in (A.12) being fulfilled. Then, the system can be stabilized as it can reach convergence. If $s > 0$, then $\text{sign}(s) > 0$ and the product $s\,\text{sign}(s) > 0$. If $s < 0$, then $\text{sign}(s) < 0$ and the product $s\,\text{sign}(s) > 0$. The existence condition is fulfilled due to g_2, V_{in}, n, C_{o}, L_{f} and l are positive parameters.

$$\begin{aligned} s\dot{s} &= s\mathbf{G}(\mathbf{AE} + \mathbf{B}(u_{\mathrm{equ}} + u_{\mathrm{sw}}) + \mathbf{D}) = s\mathbf{GB}u_{\mathrm{sw}} \\ &= -g_2 \frac{V_{\mathrm{in}}}{nC_{\mathrm{o}}L_{\mathrm{f}}} ls\,\mathrm{sign}(s) \end{aligned} \tag{A.12}$$

The Laplace-form from (A.10) yields (A.13). Further design parameters are derived: b is the damping characteristic parameter, zero s_0 is determined to be non-dominant by defining $b = 3$. The Laplace variable is s.

$$\begin{aligned} s^3 + \frac{g_1}{g_2}s^2 + \frac{g_3}{g_2}s + \frac{g_4}{g_2} &= 0 \\ (s + s_0)(s^2 + 2\zeta\omega_{\mathrm{n}}s + \omega_{\mathrm{n}}^2) &= 0 \\ s_0 = b\zeta\omega_{\mathrm{n}} \quad \tau &= \frac{1}{\zeta\,\omega_{\mathrm{n}}} \end{aligned} \tag{A.13}$$

The control coefficients are calculated based on (A.13) with the critical damping ratio assumed to be $\zeta = 1$ as presented in (A.14).

$$\frac{g_1}{g_2} = (2 + b)\omega_{\mathrm{n}}, \ \frac{g_3}{g_2} = (1 + 2b)\omega_{\mathrm{n}}^2, \ \frac{g_4}{g_2} = b\omega_{\mathrm{n}}^3 \tag{A.14}$$

The decay time constant τ, the system adjusting time $T_{\mathrm{a}} = 5\,\tau$ and the transient frequency $\omega_{\mathrm{n}} = 2\pi\,3.8\,\mathrm{kHz}$ are empirically designed on the basis of measurements of the system response and according to (A.13). The frequency of 3.8 kHz corresponds to the identified natural oscillation frequency of the system. Design rules are summarized in (A.15), (A.16).

$$\frac{g_1}{g_2} = \frac{5(2 + b)}{T_{\mathrm{a}}}, \ \frac{g_3}{g_2} = \frac{25(1 + 2b)}{T_{\mathrm{a}}^2}, \ \frac{g_4}{g_2} = \frac{125b}{T_{\mathrm{a}}^3} \tag{A.15}$$

$$\begin{aligned} k_1 &= \frac{nC_{\mathrm{o}}L_{\mathrm{f}}}{V_{\mathrm{in}}}\frac{25(1 + 2b)}{T_{\mathrm{a}}^2}, & k_2 &= \frac{nC_{\mathrm{o}}L_{\mathrm{f}}}{V_{\mathrm{in}}}\left(\frac{5(2 + b)}{T_{\mathrm{a}}} - \frac{1}{Z_{\mathrm{o}}C_{\mathrm{o}}}\right), \\ k_3 &= \frac{n}{V_{\mathrm{in}}}, & k_4 &= \frac{nC_{\mathrm{o}}L_{\mathrm{f}}}{V_{\mathrm{in}}}\frac{125b}{T_{\mathrm{a}}^3} \end{aligned} \tag{A.16}$$

The designed control's working principle is based on Voltage Mode Control (VMC). A current control with SMC does not meet the existence condition. Control objects would be $e_1 = i_{\mathrm{ref}} - i_{\mathrm{L}}$ resulting in $e_2 = \dot{e_1} = f(u)$. The control object's state-space system is obtained by derivation being $\dot{e_2} = f(\dot{u})$ according to the second line of (A.7). This expands the state-space matrix by $\dot{u}$ which does not match the SMC design procedure.

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