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Hybrid Multilevel Converters: New Topologies and Enhanced Model Predictive Control Techniques

Ibrahim Ahmed Mohamed Harbi

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1. Prof. Dr.-Ing. Dr. h.c. Ralph Kennel
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3. Prof. Dr.-Ing. Abdellah Kouzou

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To my children: Ahmed & Ayla

Ibrahim

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Abstract

The increasing demand for electrical energy from renewable sources has been driven by the growing awareness of its environmental and economic benefits and by remarkable advances in power electronics components. DC/AC power converters hold a vital role in the energy harvesting process from renewable energy (RE) sources. Their ability to optimise energy harvest from these sources, along with their impact on system efficiency, reliability and cost-effectiveness, make them a crucial step in seamlessly integrating renewable energy into the power grid for sustainable energy production. Multilevel inverters (MLIs) have gained significant attention in advanced power conversion systems due to their attractive merits such as low harmonic contents, low dv/dt stress, minimum filtering requirements, low switching frequency, low electromagnetic interference (EMI), modularity, and fault-tolerant operation. Notably, these advantages are directly related to the number of voltage levels generated by the MLI. Nevertheless, the increase in levels number poses significant challenges concerning the complexity of the topology and the implementation of control strategies.

This research focuses on the topological structures and advanced control methods for MLIs applications. The dissertation is structured into two main parts. The first part focuses on upgrading established commercialized topologies to enable nine-level operation, with a specific emphasis on addressing structural complexity and enhancing converter efficiency. In this regard, two new nine-level topologies are proposed with an optimal modulation method to achieve balanced operation of the flying capacitors (FCs) and the neutral point (NP) of the dc-link. The first topology enhances the commercially available five-level active-neutral-point-clamped (5L-ANPC) converter, enabling nine-level operation by incorporating a four-quadrant switch and one additional FC per phase-leg while reducing the voltage rating of the FCs. The second nine-level converter is designed using the conventional three-level T-type converter (3L-T^2C) for high-efficiency operation of grid-connected distributed generation. The second part of this dissertation focuses on exploiting the powerful of model predictive control (MPC) in the challenging multi-objective control problem of MLI applications. Through the introduction of new MPC-based control methods, common challenges and limitations of MPC in MLI applications have been addressed. These challenges include high computational load, tuning of weighting factors, sensitivity to parameters mismatch and variable switching frequency. All proposed topologies and control methods in this dissertation have been experimentally validated in the laboratory.

Zusammenfassung

Die Nachfrage nach elektrischer Energie aus erneuerbaren Energiequellen wurde durch das wachsende Bewusstsein für ihre ökologischen und wirtschaftlichen Vorteile sowie durch bemerkenswerte Fortschritte bei leistungselektronischen Komponenten gesteigert. DC/AC-Stromrichter spielen eine wichtige Rolle im Energiegewinnungsprozess aus erneuerbaren Energiequellen (RE). Ihre Fähigkeit, die Energiegewinnung aus diesen Quellen zu optimieren, sowie ihre Auswirkungen auf die Systemeffizienz, Zuverlässigkeit und Kosteneffizienz machen sie zu einer Schlüsselkomponente bei der nahtlosen Integration erneuerbarer Energien in das Stromnetz. Multilevel-Wechselrichter (MLIs) haben in fortgeschrittenen Stromumwandlungssystemen erhebliche Aufmerksamkeit erlangt, aufgrund ihrer attraktiven Vorteile wie niedrige Oberwellenanteile, geringe du/dt-Belastung, minimale Filteranforderungen, niedrige Schaltfrequenz, geringe elektromagnetische Störungen (EMI), Modularität und fehlertolerante Betrieb. Bemerkenswerterweise stehen diese vorteilhaften Eigenschaften in direktem Zusammenhang mit der Anzahl der vom MLI erzeugten Spannungspegel. Dennoch bringt die Erhöhung der Anzahl der Ebenen erhebliche Herausforderungen in Bezug auf Komplexität der Topologie und der Implementierung von Regelungsstrategien mit sich.

Diese Forschung konzentriert sich auf die topologischen Strukturen und fortschrittlichen Regelungsmethoden für MLI-Anwendungen. Die Dissertation ist in zwei Hauptteile gegliedert. Der erste Teil befasst sich mit der Aufrüstung etablierter, kommerzieller Topologien, um einen Neun-Level-Betrieb zu ermöglichen. Dabei liegt ein besonderer Schwerpunkt auf der Bewältigung der strukturellen Komplexität und der Verbesserung der Wandlereffizienz. In diesem Zusammenhang werden zwei neue neunstufige Topologien mit einer optimalen Modulationsmethode vorgeschlagen, um einen ausgeglichenen Betrieb der fliegenden Kondensatoren (FCs) und des Neutralpunkts (NP) des dc-Links zu erreichen. Die erste Topologie verbessert den kommerziell erhältlichen Fünf-Stufen-Aktiv-Neutralpunkt-Klemmen (5L-ANPC)-Wandler und ermöglicht einen neunstufigen Betrieb, indem ein Vier-Quadranten-Schalter und ein zusätzlicher FC pro Phasenabschnitt integriert werden, während die Nennspannung der FCs reduziert wird. Der zweite neunstufige Konverter ist unter Verwendung des konventionellen Drei-Stufen-Typs (3L-T^2C) für einen hoch effizienten Betrieb der netzgekoppelten dezentralen Stromerzeugung konzipiert. Der zweite Teil befasst sich mit der Nutzung der Leistungsfähigkeit der modellprädiktiven Regelung (MPC) bei dem anspruchsvollen Mehrobjektiv-Regelungsproblem von MLI-Anwendungen. Durch die Einführung neuer MPC-basierter Regelungsmethoden wurden allgemeine Herausforderungen und Einschränkungen von MPC in MLI-Anwendungen ange-

gangen. Zu diesen Herausforderungen gehören eine hohe Rechenlast, die Abstimmung von Gewichtungsfaktoren, die Empfindlichkeit gegenüber nicht übereinstimmenden Parametern und die variable Schaltfrequenz. Alle in dieser Dissertation vorgeschlagenen Topologien und Regelungsschemata wurden im Labor experimentell validiert.

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CHAPTER 1

Introduction

This work focuses on topologies and control of hybrid multilevel inverters (MLIs) for grid-connected applications. In this chapter, the background, motivations, and contributions of this dissertation are presented.

1.1 Overview

The demand for electrical energy from renewable sources has been rapidly increasing in recent years. According to the "Renewables 2022" report by the International Energy Agency (IEA), renewable electricity generation is expected to increase by almost 2400 GW between the years 2022 and 2027, representing an increase of 75% [1]. Solar and wind energy have emerged as promising sources of renewable energy (RE). In recent years, there has been a substantial surge in power generation from these sources, with further growth anticipated, as illustrated in Fig. 1.1. This upward trend can be attributed to the increasing awareness of the environmental and economic benefits of REs, as well as advancements in power electronics systems, making REs more cost-effective and efficient. This trend is expected to continue as the need for sustainable and clean energy sources increases to meet the growing energy demand and combat climate change.

DC/AC power converters play a critical role in the energy harvesting process from REs. Their ability to optimize the energy produced by these sources, as well as their impact on the efficiency, reliability and cost-effectiveness of these systems, make them a crucial stage in the integration of RE into the power grid. The use of conventional two-level converters in medium- and high-power applications is typically limited by the voltage ratings of the power switches available on the market. With these converters, the use of series-connected switches is necessary when the available switches cannot meet the voltage requirements of the application. However, this approach raises the problem of dynamic voltage sharing among the switches [2]. For the sake of solving this issue, the concept of a multilevel converter (MLC) was invented [3, 4].

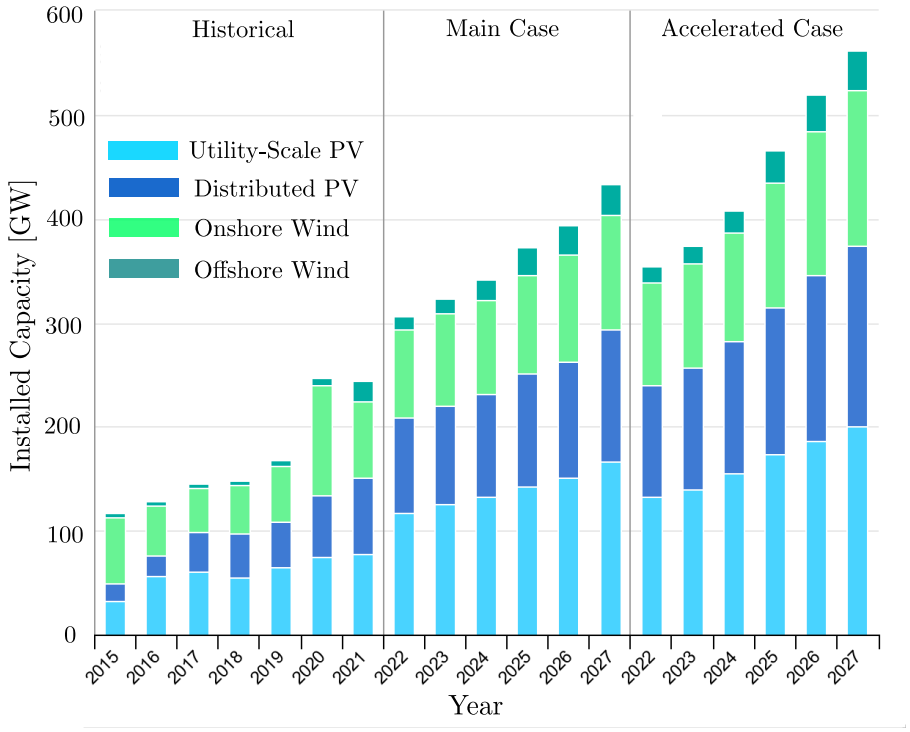


Figure 1.1: Renewable annual net capacity additions by technology, main and accelerated cases, 2015-2027 [1].

1.2 Multilevel inverters

MLIs use an arrangement of power devices and DC sources in a way to create a staircase output voltage waveform, as shown in Fig. 1.2. They provide numerous attractive merits compared to conventional two-level converters [5–9]. The key advantages of the MLIs include:

- The ability to deliver higher-quality waveforms with lower harmonic contents at a lower switching frequency, reducing bulky and expensive filter requirements and electromagnetic interference (EMI);
- Reducing power losses and cooling system requirements in the filter components through size reduction, which considerably enhances the efficiency and cost-effectiveness of grid-connected systems, especially in medium and high-power applications;
- The ability to handle medium/high-voltage applications using standard commercial power devices without the need for series-connected switches, eliminating the associated dynamic voltage sharing problem;
- Low switching losses by reducing the operating switching frequency of the power devices and reducing the voltage step Δv across the switches during the commutation process;
- Reduction of dv/dt on switches and low/zero common-mode voltage (CMV), which are highly desirable in various applications such as medium-voltage (MV) drive systems to

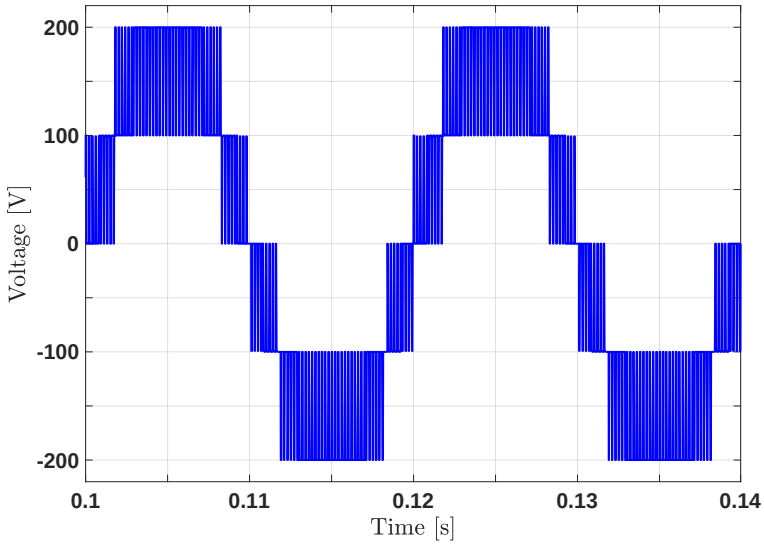


Figure 1.2: Typical five-level voltage waveform.

reduce the insulation stress on the machine windings and the bearing failure; and

- The capability for fault-tolerant operation thanks to the existing redundancies in the switching states, improving the reliability of the power conversion system.

Thanks to their outstanding advantages, MLIs have become the preferred choice for medium- and high-voltage/power applications [9, 10]. Moreover, the use of MLIs has been extended to low-voltage/power applications to avoid the problematic issues of two-level converters associated with the operation at a high switching frequency and the EMI [11–13]. MLIs offer a compact and efficient solution for low-voltage applications where space constraints and power density are crucial considerations. By generating multiple voltage levels, MLIs can achieve the desired power output while minimizing the size and weight of the system, especially filtering and cooling system requirements. In addition, the remarkable advancements in wide-bandgap devices, such as SiC and GaN power devices, have spurred significant research efforts aimed at leveraging their potential to enhance the power density and efficiency of MLIs in low-voltage applications [14–16]

Since the inception of the MLI concept, several topologies have been introduced, and some of them are currently mature technologies in the industry for different application fields. Fig. 1.3 shows the major evolution of MLIs during the last decades. MLI innovation has been started with the cascaded H-bridge (CHB) converter in the 1970s [3], followed by the neutral-point-clamped (NPC) converter in the 1980s [17–19] and the flying capacitor (FC) converter in the 1990s [20, 21]. These three converters are known as conventional topologies and form the basis for other topologies that were later developed. In the early 2000s, the modular multilevel converter (MMC) [22] and stacked multicell converter (SMC) were introduced with high modularity for high-voltage applications [23]. Combining the robustness of the NPC with the flexibility of the FC topology, the five-level active NPC (5L-ANPC) converter was introduced later in 2005 for industrial MV applications up to 6.9 kV [24, 25]. Over the past decade, several hybrid topologies have been introduced with the aim of reducing the required components. However,

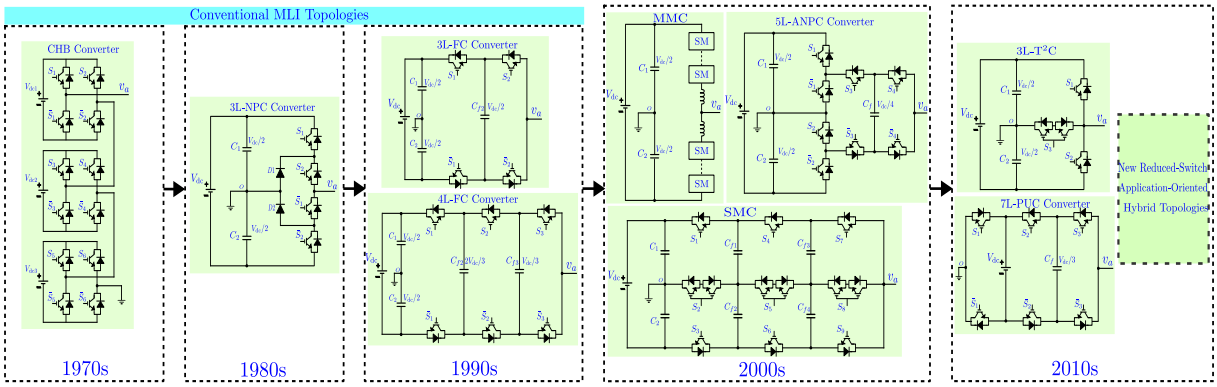


Figure 1.3: Major evolutions of MLI topologies over the past decades.

only a few topologies have been employed successfully in industry, such as the 3L T-type (3L-T^{2}C) and 5L packed u-cell (5L-PUC) converters for low-voltage applications [12, 26, 27].

The advantages of MLIs are directly related to the number of voltage levels they can generate. By increasing the number of output voltage levels in an MLI, the aforementioned advantages are maximized. When examining the advantage of reducing the filter size and losses, as an example of the advantages, in grid-connected applications, it is possible to establish a relationship between the peak-to-peak current ripple ΔI and the number of voltage levels (N_{level}) by utilizing a piece-wise approximation of the inductor volt-second balance as [28]

$$\Delta I = \frac{V_{dc}}{(N_{\text{level}} - 1)^2 f_{sw} L_f}, \tag{1.1}$$

where L_f is the filter inductance and f_{sw} is the switching frequency. As it is clear, the current ripple is inversely proportional to $(N_{\text{level}} - 1)^2$. Consequently, maintaining the same power quality at the output results in lower filtering requirements, while keeping the current rating similar. This reduction in filtering requirements leads to lower copper losses, specifically $I^2 * R$ losses. Moreover, the presence of ripple increases the RMS current, resulting in additional losses. These losses can further impact the overall performance and efficiency of the system.

1.3 Control problem of MLIs

Typically, the control of MLIs is a challenging and multi-objective task, e.g. current control, and internal voltages regulations. The objectives of the control problem are determined by the MLI topology and the application under consideration. Accordingly, they can be divided into two groups; topology-related objectives and application-related objectives, as shown in Fig. 1.4.

Topology-related objectives are included to ensure proper operation of the MLI topology and mainly depend on the configuration of the inverter. For example, a dc-link balancing is a necessary objective for topologies with a mid-point clamped, such as NPC [29] and 5L-ANPC [30] inverters. Also, capacitor voltage control in FC-based topologies is an inevitable target, like FC [31] and 5L-ANPC inverters. In addition, thermal stress distribution among switches [32] and switching frequency reduction [29] are considered secondary objectives that can improve the converter operation and increase the power density and/or efficiency.

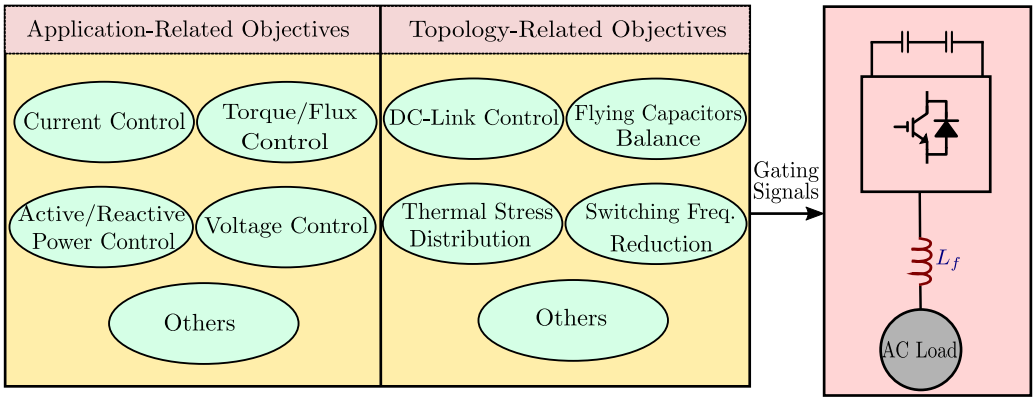


Figure 1.4: Control objectives of MLIs applications.

Application-related objectives are considered to meet the requirements of the load. For example, reference current tracking is a major goal in various applications such as in electric drives after generating the reference current according to the required machine speed/torque [33]. Also, torque and flux control are common objectives in drive systems [34]. Another example for application-related objectives is the active and reactive power control in grid-connected systems [35, 36] and voltage control in UPS applications [37].

Effectively controlling MLIs applications using conventional linear control techniques, such as proportional-integral (PI) controllers, is challenging, particularly when dealing with hybrid topologies that encompass multiple topology-based objectives with a limited number of redundant switching states. In addition, the difficulty of dealing with nonlinearities and constraints, parameter tuning problems in the cascaded structure with multiple goals, and poor dynamic performance are problematic issues of the conventional control methods [38]. In response to these challenges, alternative approaches involving nonlinear control algorithms, such as sliding mode control [39] and fuzzy control [40] have been recently adopted.

1.4 Model predictive control for multilevel inverters

Among the various nonlinear advanced methods, model predictive control (MPC) has proven to be a promising control method for power converters in general and MLIs in particular. Although MPC was first introduced in the 1960s [41], its investigations into power electronic systems started in the 1980s and its actual popularity emerged in the 2000s as a result of massive technological advances in digital platforms [42–44]. The industrial implementation of MPC has been realized by ABB Ltd. in some products, such as ACS2000 for medium-voltage drives [45]. The notable superiority of MPC primarily stems from its implementation in a single-loop, in contrast to the conventional methods that employ a cascaded structure. As a consequence, MPC exhibits a much faster response to disturbances. MPC offers several advantages such as simplicity of design, high dynamic performance, and the ability to include the constraints and nonlinearities of the system in a straightforward way [44]. In addition, an outstanding feature of MPC is the capability to handle multiple control objectives using a well-designed cost function in conjunction with constraints. Therefore, it has been widely applied to different MLI topologies in various application areas such as neutral point clamped (NPC) converter in medium-

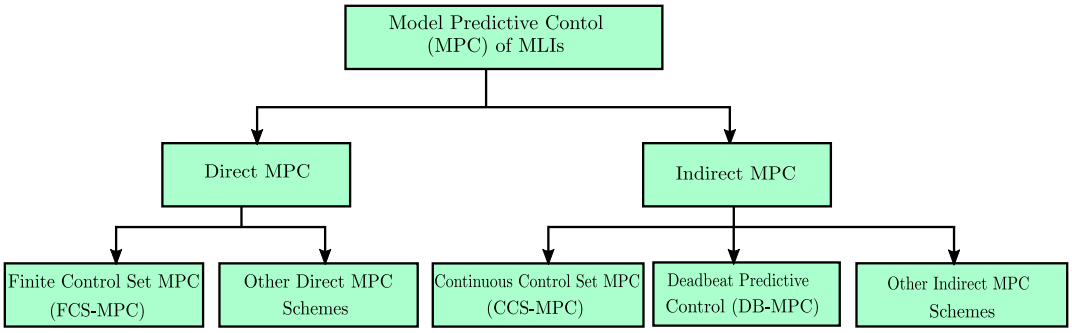


Figure 1.5: Classification of MPC methods applied to multilevel inverters.

voltage (MV) grid-connected applications [46], flying capacitor (FC) converter in active power filter (APF) [47], cascaded H-bridge (CHB) converter in renewable energy systems [48], and five-level active NPC (5L-ANPC) converter in electrical drives [49], to name a few.

In general, MPC uses the model of the system under control to predict its behaviour in a defined prediction horizon. Then, using a cost function that defines the system objectives, the control action is determined by minimizing the errors between the predicted and reference values. The output of the MPC is a sequence of control actions in each control cycle, but only the first action is applied. Several MPC schemes have been reported in the literature for MLIs. According to the output of the optimization problem, MPC methods can be categorized into two groups; direct MPC and indirect MPC, as shown in Fig. 1.5. In direct MPC, The controller action is an integer vector and is applied directly to the system without the need for a modulation stage, i.e., the controller outputs the switching signals. Whereas with indirect MPC, the MPC controller outputs the control action as a real-valued vector and then a modulator is used to generate the switching pulses.

Considering the first category, direct MPC, finite control set MPC (FCS-MPC) is considered the most popular MPC scheme in MLIs applications. FCS-MPC has the ability to directly exploit the discrete nature of the power converters. By evaluating the finite converter states in a cost function containing the control objectives, the optimal control action can be identified [29]. One prominent merit of FCS-MPC is the ease of solving the control problem, even when there are multiple control objectives and system constraints. However, the required online calculations for variable predictions and cost function minimization increase the computational burden, especially for high-level MLIs. In addition, variable switching frequency, tuning of weighting factors (WFs), and long-horizon implementation are considered challenges in FCS-MPC [29, 44, 50–52]. Several developments and improvements have recently been reported to compensate for these disadvantages, which will be discussed in Chapter 5.

In contrast to direct MPC, where control and modulation take place in one computational stage, indirect MPC solves these problems in a sequential manner. Hence, indirect MPC computes the control action, e.g., the modulating signal or the duty ratio, which is subsequently fed into a modulator for generation of the switching commands. Continuous control set MPC (CCS-MPC) methods are the most common in this category, where the optimization problem is formulated as a constrained or unconstrained quadratic program (QP). Although the latter has higher computational load, it is relatively modest compared to FCS-MPC because the computational cost does not rely on the number of levels in MLI topologies, and part of the optimiza-

tion problem is solved offline [53, 54]. However, constructing the linear system model for the CCS-MPC is not an easy task, especially for the MLI topologies, which are typically bilinear systems [53].

1.5 Motivation and objectives

The increasing need for more efficient power converters is driven by the demand to optimize the utilization of renewable energy sources and enable a sustainable energy future. MLIs have been introduced as alternative solutions to conventional two-level converters, aiming to overcome their limitations while offering numerous advantages, as discussed in Section 1.2. The aforementioned features of MLIs are directly correlated with the number of voltage levels they can generate. The three-level operation of NPC, FC, and CHB topologies have been well investigated and successfully penetrated the industry [19, 55–59]. However, these conventional topologies face significant practical challenges regarding topological and control complexity, cost, and efficiency in high-level operation. Extending the three-level NPC converter to higher levels not only increases the number of diodes required, but the neutral points (NPs) resulting from DC-link splitting also become a challenge to be balanced. A high-level operation of the FC topology necessitates a large number of capacitors and a complex control to stabilize their voltages, which adversely affect the reliability and cost of the system. The extension of the CHB converter to higher voltage levels has been successfully implemented, however, a separate DC source is required for each H-bridge unit, which increases the system cost and makes its applications limited to renewable energy systems.

Recently, hybrid MLI (HMLI) topologies have gained lots of interest in both academic and industrial fields because they combine several merits of the conventional ones with the ability to generate higher voltage levels [12, 24, 60–66]. One of the most competitive hybrid MLIs is the five-level active NPC (5L-ANPC) topology, which has been successfully introduced into the industry by ABB Ltd for medium-voltage industrial applications up to 6.9 kV [25]. Subsequently, significant efforts have been dedicated to enhancing the 5L-ANPC configuration, with the goal of generating higher voltage levels to reduce filtering requirements, improve system efficiency, and reduce current/voltage stress on power devices. For instance, in [67], a nine-level converter was proposed to enable the filterless operation of a 6-MW grid-connected WT system by cascading a 5L-ANPC converter with a conventional H-bridge. Thanks to the generated nine-level phase voltage (17-level line to line voltage), the converter achieves compliance with the IEC 61000-2-12 and IEEE519 utility standards for voltage and current harmonics with a 4.16kV/33kV transformer, eliminating the necessity for additional passive filters. Eliminating bulky and costly filter requirements for such a level of power considerably reduces the total system cost and increases the efficiency. However, improvements are still needed to reduce the number of components required for this converter, thereby lowering costs and improving converter efficiency. In [60], the authors proposed a nine-level ANPC-based converter with reduced components for grid-connected applications by adding only additional two low frequency switches (LFSs) to the 5L-ANPC. Despite the significant reduction in switch count achieved compared to nine-level topologies, the LFSs must block the full dc-link voltage, which increases the total standing voltage (TSV) of this converter. In addition, three isolated dc-links are used in the three-phase application, adding further cost to the system. Several other topologies have

been presented in the literature in order to develop high-level MLIs with few components and low cost. A comprehensive review of these topologies is provided in Chapter 2. However, most of these topologies lost inherent features of the conventional MLIs, either through the use of switches and/or FCs with higher voltage ratings or through the loss of the ability to utilize a common dc-link in three-phase applications, which has a negative impact on cost, reliability and thus employability of these topologies. Therefore, the motivations and objectives of the first part of this dissertation is to upgrade the hybrid 5L-ANPC to a nine-level topology with reducing the topological complexity, improving the converter efficiency and without increasing the voltage rating of switches or FCs.

As discussed in Section 1.4, MPC demonstrates a strong capability in effectively addressing the complex control problems of MLIs applications, providing notable advantages compared to conventional methods. However, there are still challenges that require efficient and innovative solutions. Considering the online calculations, the high computational burden, especially for MLIs with a large number of levels, is considered one of the major challenges of FCS-MPC. The variable switching frequency, which spreads the harmonic spectrum over a wide range of frequencies and makes the filter design a difficult task for grid-connected applications, and the high steady-state error are also seen as problematic issues of FCS-MPC. While handling multiple objectives is one of the main strengths of FCS-MPC, coordinating weighting factors for achieving acceptable performance across all objectives can indeed be a cumbersome process.

Deadbeat MPC (DB-MPC) is one of the indirect MPC methods that offer a constant switching frequency and reduced steady-state error [68, 69]. It offers the advantage of low computational burden through its direct calculation of the reference voltage that nullifies the current error at the next sample using the system-discrete model. In contrast to FCS-MPC, DB-MPC is usually a single-objective control method. This is an important reason for interpreting the limited application of DB-MPC to MLIs. Another significant challenge associated with MPC (direct and indirect) is the requirement for accurate models. Since MPC is a model-based method by nature, its performance heavily relies on the accuracy of the underlying model used for prediction and control.

Therefore, the motivations and objectives of the second part of this dissertation are to leverage the potential of the FCS-MPC and DB-MPC in addressing the control problem of the MLIs that have limited redundant states. This includes a close investigation of the challenges associated with FCS-MPC and DB-MPC in the context of MLIs, while trying to identify and propose efficient solutions to overcome these challenges.

In general, MLIs are impeded by two interconnected limitations: a high component count and the inherent complexity of control. The root of these challenges lies in the nature and quantity of components employed in MLIs, leading to subsequent issues such as intricate control requirements. These limitations serve as strong motivations to explore and propose innovative topologies that aim to reduce the complexity of both the system's topology and control, addressing the challenges posed by the multiple objective problem.

In summary and driven by the aforementioned discussion, this dissertation is structured into two main parts. The first part focuses on upgrading established topologies to enable nine-level operation, with a specific emphasis on addressing structural complexity and enhancing converter efficiency. The second part is dedicated to tackling the challenges of MPC with MLIs applications, through the proposal of novel MPC-based control methods.

1.6 Dissertation contributions

This dissertation focuses on the investigation of topological structures and control implementations of MLIs applications. All proposed topologies and control methods have been experimentally validated in the laboratory. To facilitate the validation process, a complete test bench has been constructed from scratch, starting at the component level. This involved the use of Infineon's IGBT 1200-kV with the design of suitable gate drivers. The detailed design of the experimental setup can be found in Appendix B. Additionally, a Hardware-In-The-Loop (HIL) setup has been built using the RT Box from Plexim and Microlabbox from dSPACE. All proposed approaches have been validated through tests involving RL load and grid-connected operation. As direct outcomes of this dissertation, eight papers have been published in prestigious IEEE peer-reviewed journals and five papers have been presented at prominent IEEE conferences, showcasing the findings and contributions of this work (see Appendix A). Additionally, several other papers have been published during the duration of the PhD project, although they are not directly related to the specific topic of this dissertation.

The contributions of the dissertation are divided into two main parts. The first part focuses on MLI topologies, and the notable contributions are outlined as

- Comprehensive review of MLI topologies is carried out, covering their topological evolution, notable features and limitations, topologies comparison, modulation techniques, and industrial applications (See Chapter 2).
- A novel hybrid nine-level inverter is proposed as an upgraded version of the well-known 5L-ANPC topology for high-efficiency low- and medium-voltage medium-power applications. Based on switching state redundancies, a voltage control strategy for FCs and dc-link is developed and incorporated into the PWM technique (See Chapter 3).
- A new high-efficiency nine-level T-type converter for grid-connected applications is developed based on the three-level T-type leg, with the optimal modulation method that ensures the balancing of the dc-link and FCs (See Chapter 4).

The second part of the dissertation focuses on exploiting the powerful of MPC in the challenging multi-objective control problem of MLI applications with addressing the common challenges and shortcomings of MPC in this area. The noteworthy contributions in this regard are summarized as

- The current state, challenges and future trends of MPC strategies for MLI applications are presented. The significance of each challenge and the reported effective solutions are reviewed. Moreover, some of the important concepts are experimentally validated through a case study and compared under the same operating conditions to evaluate the performance and highlight their features (See Chapter 5).
- A low computational load FCS-MPC with online parameters estimation is proposed and experimentally validated on the proposed nine-level ANPC topology. This method can handle three control objectives with only one weighting factor, namely, current control, FC balancing, and NP potential stabilization, which reduces the cumbersome effort required for weighting factors coordination. In doing so, an effective dc-link balancing

scheme based on power flow control is proposed and integrated into the FCs control objective. Moreover, this method empowers the converter to operate in different modes under the faulty condition of the bidirectional switch without any structure modification, which guarantees continuous operation of the converter while ensuring the balancing of FCs and dc-link capacitors in all operating modes. The developed method has been experimentally validated for single-phase nine-level converter and can be extended to the three-phase topology (See Chapter 6).

- An improved robust DB-MPC method is proposed and experimentally validated for the FC-based MLIs. Without the need for weighting factors, this DB-MPC method tackles three control goals, which saves the laborious effort of adjusting the weighting factors in the traditional FCS-MPC method. Moreover, to enhance the control robustness, an EKF-based estimator is designed to identify the system parameters online (See Chapter 7).

- To improve the steady-state performance and address the issue of variable switching frequency of FCS-MPC, a dual-vector method with a reduced complexity is proposed. This method notably reduces the computational burden by directly locating the best two vectors without the need for multiple evaluations of the cost function as in the conventional method. Mathematical analyzes were carried out to determine the optimal duration of the selected voltage vectors. While the sequence of the two voltage vectors is identified based on the total harmonic distortion (THD) definition to minimize its value. Compared with standard FCS-MPC, lower steady-state errors, lower THDs, better harmonic distribution, and shorter execution times are achieved (See Chapter 8).

- In order to eliminate the need for weighting factors in the FCS-MPC when dealing with multi-objective problems, a new method based on Lyapunov theory is designed. This Lyapunov-based FCS-MPC method not only addresses the issue of weighting factors but also exhibits enhanced robustness against parameter mismatches compared to the conventional one. The Lyapunov-based method is subjected to a comparative analysis via the experimental implementation with grid-connected operation, where it is compared with a proportional-resonant (PR) controller and other designed MPC methods (See Chapter 9).

Part I

Hybrid Multilevel Inverter Topologies

CHAPTER 2

Multilevel Inverters: Topologies, Modulation and Industrial Applications

This chapter presents a comprehensive review of MLIs, focusing on common dc-link topologies. This review covers the topological evolution, prominent features, topologies comparison, modulation techniques, and industrial application areas. Additionally, future perspectives and recommendations are discussed.

2.1 Classification of MLI topologies

Considering the major evolutionary stages of MLIs, the existing topologies can be categorized into some families, as shown in Fig. 2.1. The first family includes CHB-based topologies and has been reviewed in [59, 70–73]. These converters feature high modularity and an optimal number of power switches for output levels [59]. However, multiple isolated DC sources are required, necessitating the use of bulky isolation transformers or limiting their employability to applications that have several isolated DC sources. In addition, uneven power sharing between the cascaded power cells is one of the common challenges in this family [74, 75]. The second family includes NPC-based topologies such as 3L-NPC and 3L-T^{2}C converters. These converters are characterized by robust power circuits and straightforward protection. However, dc-link balancing is an essential requirement in the control design of these topologies. FC-based topologies use capacitors as clamping components to increase the number of levels, forming an MLI family characterized by high flexibility, high redundancies and fault-tolerant operation. Hybrid MLIs are formed by basic cells of the conventional topologies and, therefore, combine several advantages of classical MLIs with the capability to produce a high number of levels. MMC topologies constitute an MLIs family that represents a breakthrough for HV applications due to its high efficiency and high modularity. However, the control problem of MMC is a challenging task due to raising additional issues like circulating current limitation.

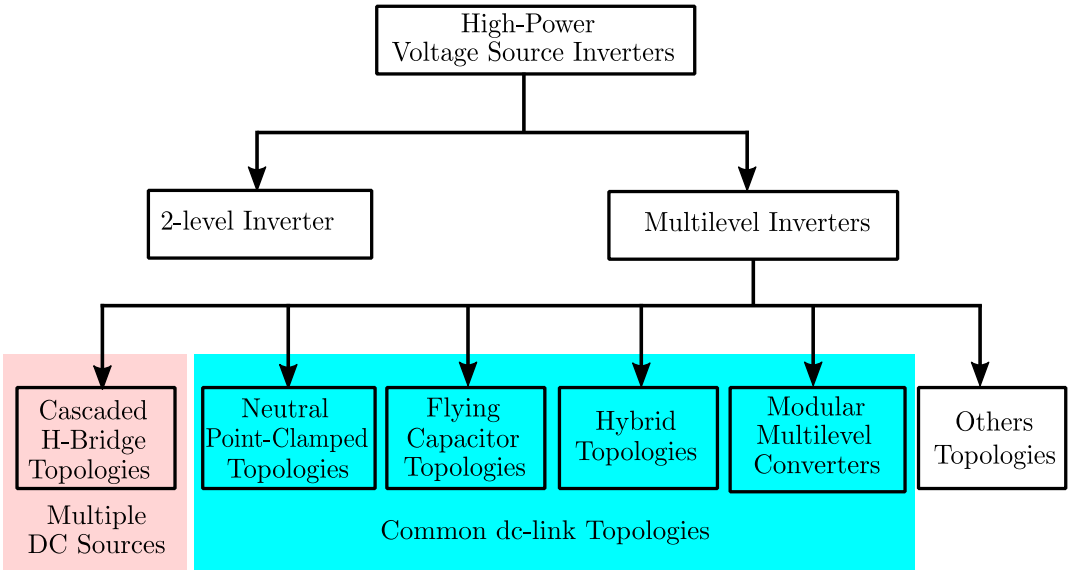


Figure 2.1: Classification of high-power voltage source inverters.

The utilization of a common dc-link voltage source converter (VSC) is an essential requirement for some applications, primarily medium- and high-power/voltage applications such as wind turbine (WT) power conversion systems. This is because providing an additional isolated DC source means the use of a bulky and inefficient transformer in conjunction with a diode bridge rectifier, significantly increasing the size and cost of the system. Furthermore, applications that rely on a back-to-back (BTB) configuration utilize a shared dc-link between the rectification and inversion stages, which necessitates the use of topologies featuring a common dc-link for both stages. In addition, common dc-link MLIs can be fully integrated into power conversion systems where traditional two-level converters are already in operation, without the need for modifications on both the DC and AC side, and with minimal adjustments to the controller design, as only one dc-link voltage needs to be regulated [8]. This explains the prevalence of common dc-link topologies in industrial applications. For instance, for battery-powered automotive industry, the voltage levels are on the rise, therefore, MLIs have been proposed to replace the conventional two-level converters. In doing so, common dc-link topologies are recommended as they fit the application requirements [76]. A plethora of reviews on MLI topologies can be found in the literature [6–8, 70, 73, 77]. However, to date, no comprehensive review article specifically addressing common dc-link topologies has been published yet.

2.2 Common dc-link topologies

2.2.1 NPC category (mid-point clamped)

One of the most widely utilized topologies of MLIs is the neutral-point clamped converter (NPC). The three-level NPC structure is used broadly in various industrial, automotive, and drive applications mostly due to its high performance and simplicity. The structure of a basic three-level NPC inverter is shown in Fig. 2.2. With the basic NPC topology, moving toward a

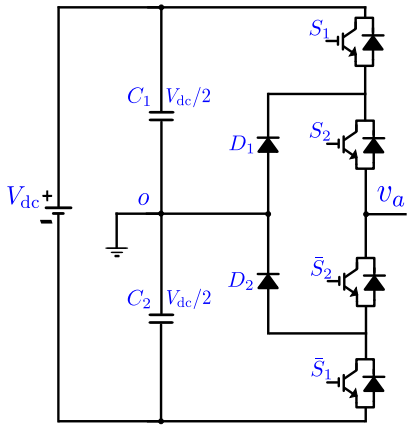


Figure 2.2: One phase-leg of the conventional three-level NPC inverter

larger number of levels is usually not recommended due to control limitations and the considerable increase in the number of clamping diodes [8].

Although the straightforward structure and control of the three-level NPC look promising, several major limitations have led to extensive research on advanced NPC-based topologies to overcome those limitations. A major issue with the three-level NPC structure is the unbalanced loss distribution in the switches of each leg which leads to a drop in the power density due to the unequal maximum junction temperature in the switches [78]. Another limitation is its use in higher-voltage applications due to the high cost of the converter at higher levels. The most famous NPC-based topologies are introduced in this subsection.

2.2.1.1 ANPC converters

The three-level Active NPC (ANPC) structure has been able to address the issue of power loss sharing through the use of two different modulation techniques called modulation patterns I and II. The topology is shown in Fig. 2.3(a) in which the two clamping diodes are replaced with two active switches to control the current flow direction in zero states. Modulation pattern I, also referred to as low-frequency high-frequency (LF-HF), causes most of the switching loss to occur in the outer switches of each leg, while pattern II (HF-LF) moves the switching losses to the inner switches. However, using only one of these patterns for the entire period does not balance the loss completely, so research has looked into ways to use a combination of the two patterns and modify the inverter structure to better balance the loss [78].

Other than the software loss balancing techniques for ANPC converters, hybrid structures propose some power density improvements compared to the basic topology. In hybrid structures, different switch types are exploited where they can minimize the loss [79, 80]. While high-current IGBTs can be used as the inner switches where the majority of conduction loss occurs, wide bandgap MOSFETs can be utilized as the outer/middle switches and withstand switching losses due to their low on/off energy losses.

Higher-level ANPC inverters are also proposed in the literature which will be investigated in detail in Section 2.2.3 on hybrid topologies due to the presence of flying capacitors in their structure.

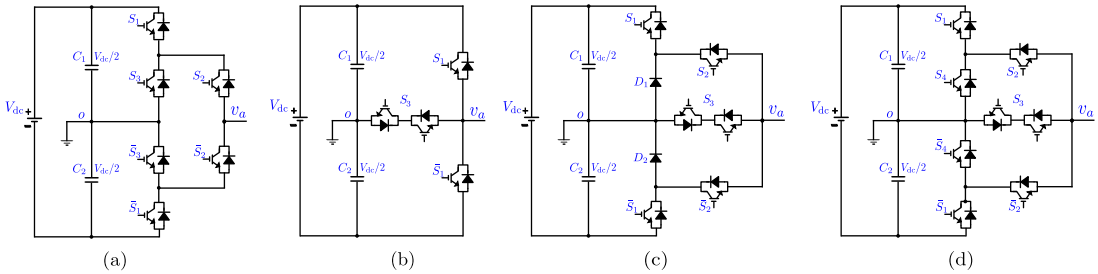


Figure 2.3: One phase-leg of common NPC converters: (a) 3L-ANPC converter, (b) 3L-T^{2}C, (c) 3L-SNPC converter and (d) 3L-ASNPC converter.

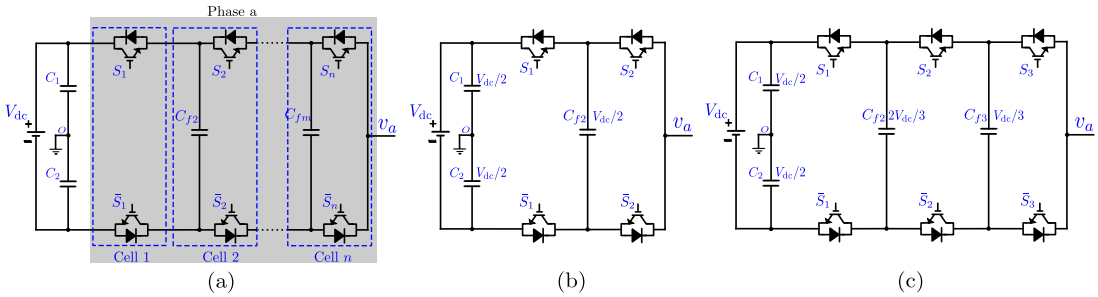


Figure 2.4: One phase-leg of the conventional FC MLI: (a) Generalized n-level topology, (b) 3L-FC converter and (c) 4L-FC converter.

2.2.1.2 T-Type converters

A three-level T-type converter (3L-T^{2}C) is shown in Fig. 2.3(b). A T-type structure benefits from some of the advantages of both two-level and three-level inverters. Simple control implementation, low conduction loss, and reduced component count make it a cost-efficient solution while three-level operation results in better waveform quality compared to the conventional two-level inverters [81]. Moreover, this structure mitigates the issue of unbalanced loss distribution in conventional NPC inverters. However, it is worth mentioning that, unlike conventional NPC and ANPC structures, a T^{2}C does not benefit from voltage stress division which limits its use in high-voltage applications [76].

Although the T^{2}C is mostly used in the three-level configuration, a five-level structure is also proposed. This structure is formed by connecting two 3L-T^{2}C inverters sharing a common dc-link [82]. This topology can effectively increase the output voltage levels to 5, while it suffers from more components count and dc-link voltage stress on all the switches.

T^{2}Cs can be combined with other structures like nested NPC (NNPC) and FC to form hybrid structures [83, 84] which will be discussed in more detail in Section 2.2.3.

2.2.1.3 Stacked and active stacked NPC converter

In another attempt to address the loss distribution issue of the basic NPC converter, a stacked NPC inverter (SNPC) was proposed in [85] as shown in Fig. 2.3(c). Similar to the basic NPC, the converter is utilizing two clamping diodes and the voltage stress on semiconductors is equal to $V_{dc}/2$. With an additional path to the neutral point, made by two back-to-back switches, new PWM strategies are achievable. In [85], these PWM strategies have proven to double the

Table 2.1: Switching states of phase a for the 3L-FC converter ($\downarrow$: discharging, $\uparrow$: charging, $-$: No change).

State	s_1	s_2	v_{ao}	C_f
V_1	1	1	$V_{dc}/2$	$-$
V_2	1	0	0	$\uparrow$
V_3	0	1	0	$\downarrow$
V_4	0	0	$-V_{dc}/2$	$-$

apparent switching frequency and therefore, reduce the switching loss stress on the outer switch.

An improvement to this topology is proposed in [86] where the two clamping diodes of SNPC are replaced with two active switches. The structure is shown in Fig. 2.3(d). The addition of active switches increases the degrees of freedom in achieving the zero-state and therefore, enables a better distribution of the switching losses. By using this topology, the average switching frequency of the power devices has been reduced to half which improves the efficiency and power density of the inverter.

2.2.1.4 Other NPC-based topologies

NPC-based converter topologies that are commonly found in the market are designed to operate at voltage levels between 2.3-4.16 kV. However, these topologies require significant changes in order to be able to handle higher operating voltages, such as those above 6.6 kV. Voltage balancing and control complexity, cost, and fault-tolerance issues are the major limiting factors for moving to higher voltages with a basic NPC-based inverter. In [87], a new power converter, the series-connected multilevel converter (SCMC), is proposed for medium-voltage high-power applications. The five-level operation is achieved by using two series-connected three-level NPC converter modules in each phase.

2.2.2 FC category

This category includes the topologies that employ FCs without a clamped neutral point and, accordingly, do not bring the issue of dc-link balancing. In these topologies, FCs are used to replace the dc-sources while generating voltage levels. In general, thanks to the modularity, this family has the capability to generate relatively higher levels compared to the NPC family. Moreover, flexibility, fault-tolerant operation, and improved loss sharing between switches are prominent features of these topologies. However, FCs voltage control, pre-charging of capacitors during the start-up process and the large number of employed capacitors are primary challenges associated with this category [10, 88, 89].

The conventional n-cell FC-MLI is composed of $2n$ active switches and $n-1$ FCs to generate $n+1$ levels per phase voltage, as shown in Fig. 2.4(a). For cell-i ($i \in \{1, 2, ..n\}$), two complementary switches ($S_i, \bar{S}_i$) and one FC C_{fi} are used. The exception is cell-1, which has the main dc-link instead of an FC. To produce $n+1$ levels, the voltage V_{fi} of C_{fi} is determined as

$$V_{fi} = \frac{n+1-i}{n} V_{dc} \tag{2.1}$$

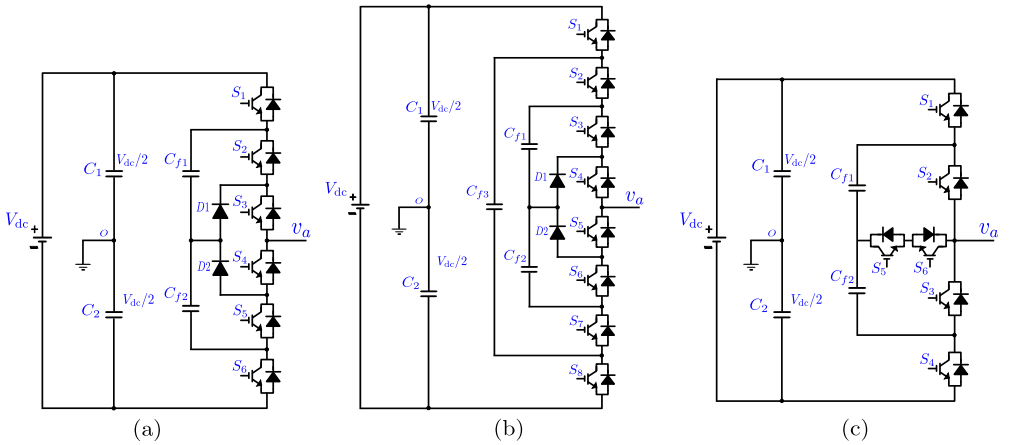


Figure 2.5: One phase-leg of common NNPC converters: (a) 4L-NNPC converter, (b) 5L-NNPC converter and (c) T-type 4L-NNPC converter.

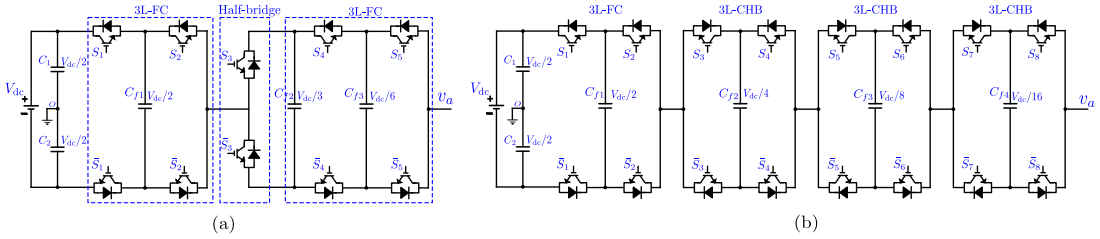


Figure 2.6: Common high-level FC cascaded topologies: (a) 7L cascaded FC converter and (b) 17L cascaded FC converter.

A phase leg of the conventional 3L-FC (2-cell) and 4L-FC (3-cell) converter is shown in Figs. 2.4(b) and 2.4(c), respectively. According to (2.1), the ratio between the DC voltage source and the FCs voltages is $1:\frac{1}{2}$ in the 3L-FC and $1:\frac{2}{3}:\frac{1}{3}$ in the 4L-FC converter. The switch states of the 3L-FC converter are given in Table 2.1, where there are four switching states to create three levels in phase voltage. The redundancies available for the zero are exploited to balance the FC at $V_{dc}/2$. The 3L-FC and 4L-FC converters are two mature industrial converters used for electric drives and solar inverters [8].

Several topologies have been derived from the conventional FC-MLI topology to increase the number of voltage levels and/or reduce the required components. One promising topology in this category is the four-level nested NPC (4L-NNPC) presented for MV applications (2.4-7.2 kV) [90], as shown in Fig. 2.5(a). Similar to the conventional 4L-FC, the 4L-NNPC converter requires six active switches with a blocking voltage of $V_{dc}/3$ and two FCs per phase-leg. The main advantage of this topology is that it limits the sustained voltage of the two FCs to $V_{dc}/3$ instead of $V_{dc}/3$ and $2V_{dc}/3$ in the 4L-FC. However, the 4L-NNPC uses two additional passive diodes. Using an additional cell consisting of two switches and one FC, the 4L-NNPC has been upgraded to the 5L-NNPC converter in [91], as depicted in Fig. 2.5(b). To generate five levels from the 5L-NNPC converter, the two FCs C_{f1}, C_{f2} are balanced at $V_{dc}/4$ and C_{f3} is balanced at $3V_{dc}/4$ by the available redundant states. Later in [92], the 4L-NNPC in Fig. 2.5(a) has been operated as a 5L converter without adding any additional passive or active components by balancing C_{f1}, C_{f2} at $V_{dc}/4$ instead of $V_{dc}/3$ in the 4L operation. In doing so, model predictive

control (MPC) was adopted to achieve the FCs balance due to the lack of redundant states in the 5L operation mode. However, the voltage stress is not equally distributed among all switches under the 5L operation, where S_1 and S_6 are subjected to double the voltage stress $(V_{dc}/2)$ compared to other switches.

Later, a new T-type 4L-NNPC converter has been proposed in [93] to eliminate the use of clamping diodes, as shown in Fig. 2.5(c), where only six active switches and two FCs are used in each phase-leg. The operation of this converter is similar to the 4L-NNPC converter as it has the same number of switching states with the same charge/discharge effects on the two FCs. Subsequently, the operation of the T-type 4L-NNPC as a 5L converter with MPC was reported in [84] using switches of different voltage ratings.

Another way to increase the output levels in this category was proposed in [94], where a 7L converter was formed by cascading two units of the conventional 3L-FC with a half-bridge leg, as shown in Fig. 2.6(a). The FCs are balanced by exploiting the pole redundant states. Moreover, this converter can operate with zero CMV up to the modulation index $M < 0.86$. In [95], a 17L was constructed by cascading a 3L FC unit with three CHB units, as shown in Fig. 2.6(b). One prominent advantage of this converter is the ability to continue operation with a lower number of levels in the event of a CHB unit failure, improving the reliability of the conversion system.

2.2.3 Hybrid MLIs (NPC+FC)

Hybrid MLIs (HMLIs) combine multiple fundamental topologies to make use of their respective advantages, while overcoming some of their limitations. Predominantly, hybrid topologies can improve the voltage balancing capabilities for both dc-link and FCs and the power loss distribution across switches, while reducing the number of required active and passive components when compared to NPC and FC topologies [96]. In this section, hybrid topologies which are particularly characterized by featuring both dc-link clamping and FCs as well as a common dc-link are considered. The HMLIs are categorized into the following groups: 1) neutral-point clamped HMLIs, 2) multi-point clamped HMLIs and lastly 3) cascaded HMLIs.

2.2.3.1 Neutral-point clamped HMLIs

This subsection presents hybrid multilevel converter topologies which are derived by combining fundamental NPC topologies with FCs. The HMLIs in this category are characterized by clamping to a single dc-link midpoint, which acts as a neutral-point, whereas topologies clamping to multiple dc-link points are presented in the next subsection.

One of the most well-known neutral-point clamped HMLIs is the hybrid five-level active NPC (5L-ANPC), which is derived from connecting a three-level ANPC with a FC power cell connected in series as shown in Fig. 2.7(a) [24]. Whereas the three-level ANPC can only clamp to three different voltage levels, i.e. $\pm 0.5V_{dc}$ and 0 (V_{dc} being the total dc-link voltage), the FC enables the generation of two additional voltage levels $\pm 0.25V_{dc}$. To achieve this, the voltage across the FC needs to be balanced at $0.25V_{dc}$ and can then be summed on the dc-link capacitor voltages. For example, a voltage level of $+0.25V_{dc}$ can be generated by switching on the switches S_1, S_5 and S_8. The same voltage level can also be generated by turning on switches S_3, S_6 and S_7. This redundancy of switching states makes it possible to balance the FC at its

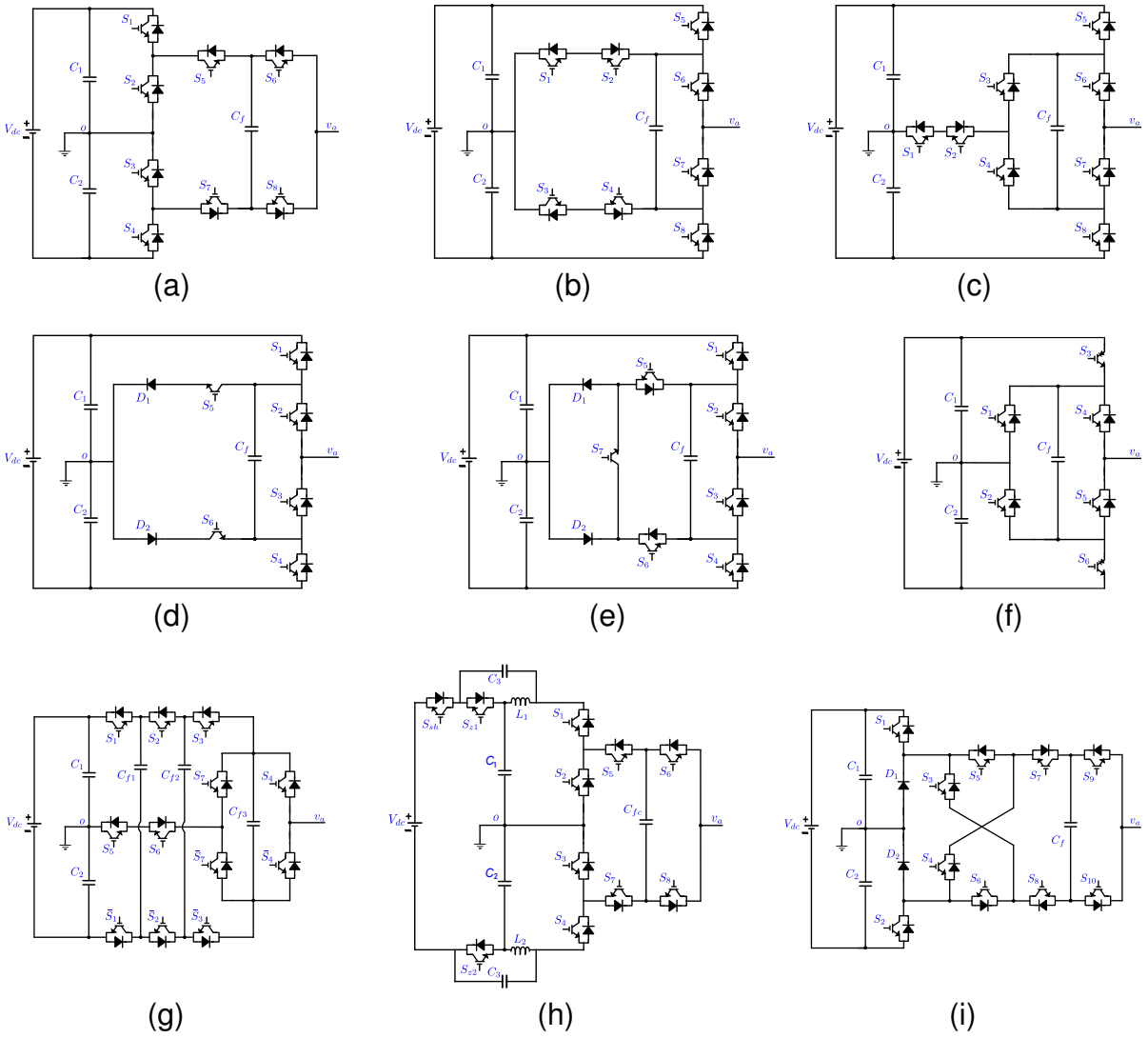


Figure 2.7: 5L-ANPC topologies. (a) 5L-ANPC Type I [24]. (b) 5L-ANPC Type II [97]. (c) 5L-ANPC Type III [98]. (d) Six-switch 5L-ANPC [99]. (e) Seven-switch 5L-ANPC [100]. (f) Six-switch 5L-ANPC with bidirectional switches [101]. (g) 5L-ANPC with auxiliary commutation branches [102]. (h) 5L-ANPC Z-Source Inverter [103]. (i) 5L-ANPC with cross-connected switches [104].

nominal value. As an additional benefit, it also leads to an even power loss distribution among the switching devices [105].

The topology is composed of eight switches, where switches S_1, S_2, S_3 and S_4 have a maximum voltage stress of $0.5V_{dc}$, while switches S_5, S_6, S_7 and S_8 have a maximum voltage stress of $0.25V_{dc}$. The maximum voltage stress on the switches can be reduced by connecting multiple lower rating switches in series, however this approach introduces dynamic voltage sharing issues, which necessitates the implementation of additional control circuitry [106]. For this reason, the usage of switches with different ratings is a widely adopted alternative strategy.

As the topology has a high number of average switches in the current path, its conduction

losses are relatively high at low-voltage applications, making this topology more suitable for medium- and high-voltage applications. Its low cost, volume and control complexity have led to commercially available products for various applications, one of the first being the medium-voltage drive ACS 2000 by ABB rated for voltages up to 6.9 kV [25].

There are two other conventional variants of the 5L-ANPC [97, 98], as shown in Figs. 2.7(b) and 2.7(c), which have the same number of power switches and capacitors, but differ in the number of gate drivers, voltage rating of the switches, total standing voltage (TSV) of switches and number of switches in conduction paths. The 5L-ANPC Type II reduces conduction losses, but because of the higher maximum voltage stress on the switches it is better suited for low voltage applications. The 5L-ANPC Type III has a reduced TSV, but also has a higher maximum switch voltage. In this subsection, prominent HMLIs derived from these three conventional 5L-ANPC converters are presented, grouped by their number of output levels.

In [99] a reduced switch count five-level ANPC is derived from the conventional 5L-ANPC Type II as shown in Fig. 2.7(d). Targeting photovoltaic grid-connected applications where output current and grid voltage are usually in phase, the topology removes some reactive current paths in order to reduce the total number of active switches from eight to six. Two additional discrete diodes are still required, however for the inner switches S_5 and S_6 no antiparallel diodes are required, allowing for a further reduction of the system cost [99]. The topology also poses lower conduction losses when compared to the conventional 5L-ANPC Type I, however it suffers from a higher voltage ripple at lower power factors, as the FC voltage drops under the reactive power condition. The HMLI presented in [100] improves reactive power operation capabilities by adding a seventh switch to the aforementioned six-switch 5L-ANPC as depicted in Fig. 2.7(e), offering similar efficiencies as conventional ANPC topologies under a high power factor.

Another six-switch variant of the 5L-ANPC Type II, shown in Fig. 2.7(f), uses bidirectional switches to increase its output voltage to unity gain, which is double the relative output voltage when compared to the conventional 5L-ANPC converters [101]. Targeting general-purpose applications, this topology features a similar efficiency as the previously presented six-switch 5L-ANPC from [99], but, in contrast, is able to operate at any power factor. Furthermore, the boosted output voltage can eliminate the need for a dc-dc front-end boost converter. However, a significant disadvantage is the high voltage rating for the FC, which is balanced at the full dc-link voltage V_{dc}, increasing the overall system voume and cost. Furthermore, the outer switches S_3 and S_6 require higher current ratings than the conventional 5L-ANPC topologies as they are burdened by both the capacitor charging current and the load current. [101]

In [102] a new topology is derived from the conventional 5L-ANPC Type III by adding two auxiliary capacitors in order to eliminate the need of additional control circuitry for series connected switches, as shown in Fig. 2.7(g).

Various converters based on the 5L-ANPC have been proposed in literature for their voltage-boosting capabilities. One such variation involves the inclusion of a Z-source network, as reported in [103], which eliminates the need for an additional boost converter, as depicted in Fig. 2.7(h). Another variation, discussed in [104], utilizes cross-connected switches to achieve the same outcome, as illustrated in Fig. 2.7(i).

The conventional 5L-ANPC Type I can also be generalized to produce a higher number of levels by cascading additional FC power cells as show in Fig. 2.8(a) [24]. This increases the voltage stress on clamping switches, which is usually dealt with by connecting multiple switches

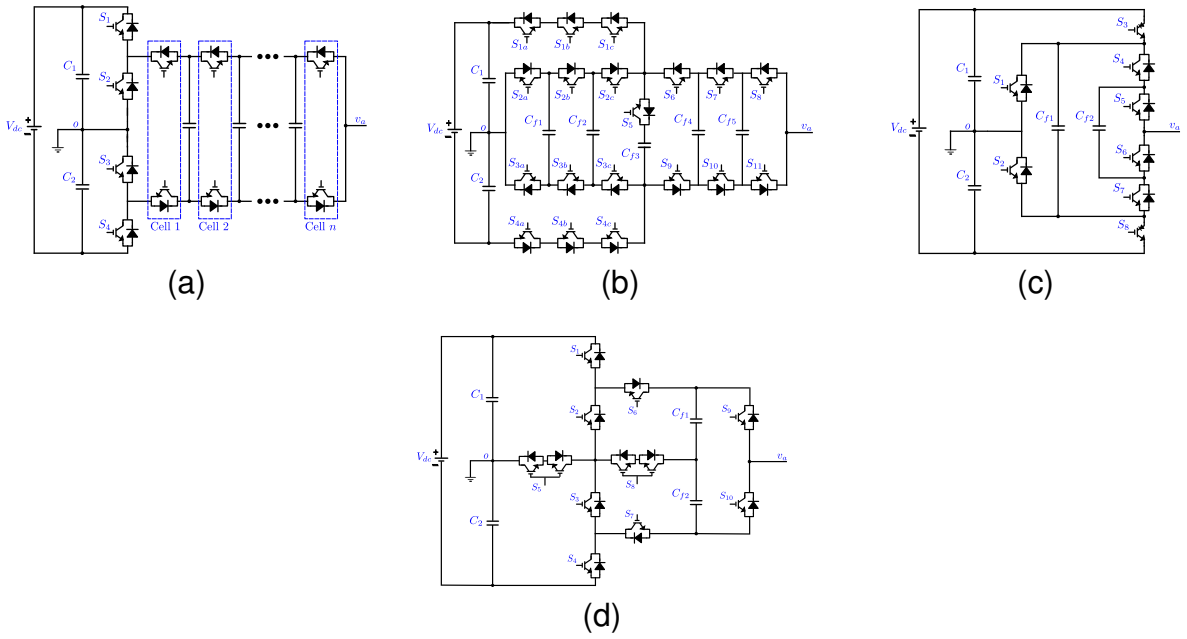


Figure 2.8: Higher level ANPC topologies. (a) Generalized n-level ANPC Type I [24]. (b) 7L-ANPC with aux. commutation branches [107]. (c) 7L-8S-ANPC, based on 5L-6S-ANPC [108]. (d) 7L/9L/11L-Boost-ANPC [64].

in series. With the goal of eliminating the problem of dynamic voltage balancing for these series switches in the generalized topology, a seven-level ANPC with auxiliary commutation branches is presented in [107], as shown in Fig. 2.8(b). In [108], a nested FC cell is added to the six-switch 5L-ANPC in [109] to produce a seven-level output, as shown in Fig. 2.8(c). The seven-level T-type ANPC presented in [64] and shown in Fig. 2.8(d) provides boosting capabilities and can be extended to produce nine or eleven output levels.

2.2.3.2 Multi-point clamped HMLIs

The hybrid topologies reviewed so far have had only one dc-link midpoint, however, there also exist some HMLIs that clamp to multiple dc-link points. An early example of this is the P2 converter introduced in [110] and shown in Fig. 2.9(a), which is a scalable topology deriving its name from the basic two-level FC cell used. Its main advantage is the automatic voltage balancing capability without requiring additional circuitry for both FCs and dc-link capacitors. At the same time, this topology can still be operated for both active and reactive power conversion. Furthermore, all switching devices, diodes and capacitors have the same voltage rating of $1/(N_{\text{level}}-1)$ times the total dc-link voltage. Despite these advantages, this topology requires a large number of switching devices and capacitors, increasing its cost significantly.

Two other multi-point clamped HMLIs, shown in Figs. 2.9(b) and 2.9(c), achieve a reduction of the total device count while maintaining FC voltage balancing capabilities [111, 112]. However, both topologies are limited by their ability of balancing dc-link capacitors, either through a limited operational range or by requiring an auxiliary circuit. At the same time, they still require a relatively high number of capacitors when compared to the ANPC topologies previously

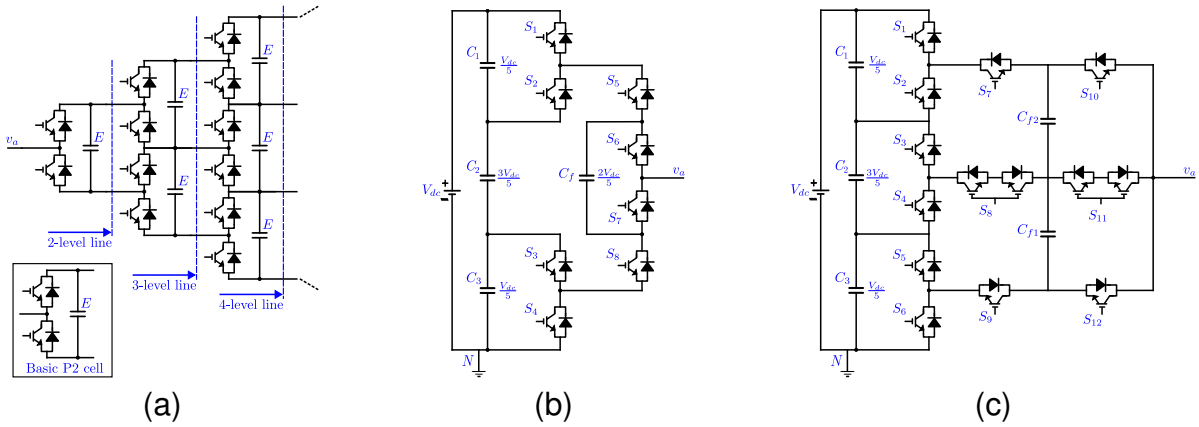


Figure 2.9: Multi-point clamped topologies. (a) General P2 converter [110]. (b) 6L multi-point clamped converter [111]. (c) 7L multi-point clamped converter [112].

presented. In [123], a novel hybrid generalized topology featuring multiple dc-link clamping points is presented. This converter serves as a foundation for deriving various existing and emerging topologies. However, the task of achieving a balanced dc-link is challenging.

2.2.3.3 Cascaded HMLIs

Another possible categorization of HMLIs is to consider those topologies which are derived by cascading one or more types of fundamental cells in parallel or series. Basic cells are typically FC and H-bridge (HB) cells, but can also include more complex cells such as a cross-connected FC cell [96, 122]. The cascaded approach can improve FC voltage balancing characteristics as well as fault-tolerance of the HMLI [96].

A common class of cascaded HMLIs combines a NPC basic cell with a full HB cell in series. Some topologies, such as those in [124] and [125], connect both output phase legs to the HB cell to increase the number of output levels, however this eliminates the possibility of using a common dc-link in three-phase systems as there no longer is a common neutral point. Therefore, within this review only those cascaded HMLIs using a FC-based HB cell are further considered.

An early HMLI using this approach is the converter proposed in [113], connecting a three-level NPC cell with a FC-based HB cell in series, as shown in Fig. 2.10(a). This topology features a boosted output and can produce up to nine levels, depending on the chosen ratio of FC voltage to dc-link voltage. However, a higher number of output levels eliminates redundant switching states and thus only seven-levels are used to maintain FC voltage balancing capabilities. By using a three-level ANPC cell instead of the NPC, as shown in Fig. 2.10(b), Pulikanti *et al.* improve the loss distribution among switching devices in [114]. In another variation, shown in Fig. 2.10(c), a three-level T-type is cascaded with HB unit to form the seven-level HMLI proposed in [115], resulting in an improved efficiency for low-voltage applications, due to reduced conduction losses, when compared to the NPC. The HMLI presented in [116] and shown in Fig. 2.10(d) cascades a three-level FC cell to the previous topology to increase the number of output levels to thirteen.

Another possibility of increasing the number of output levels is to use a higher-level NPC cell. The HMLI proposed by [67] and depicted in Fig. 2.10(e) uses a conventional 5L-ANPC

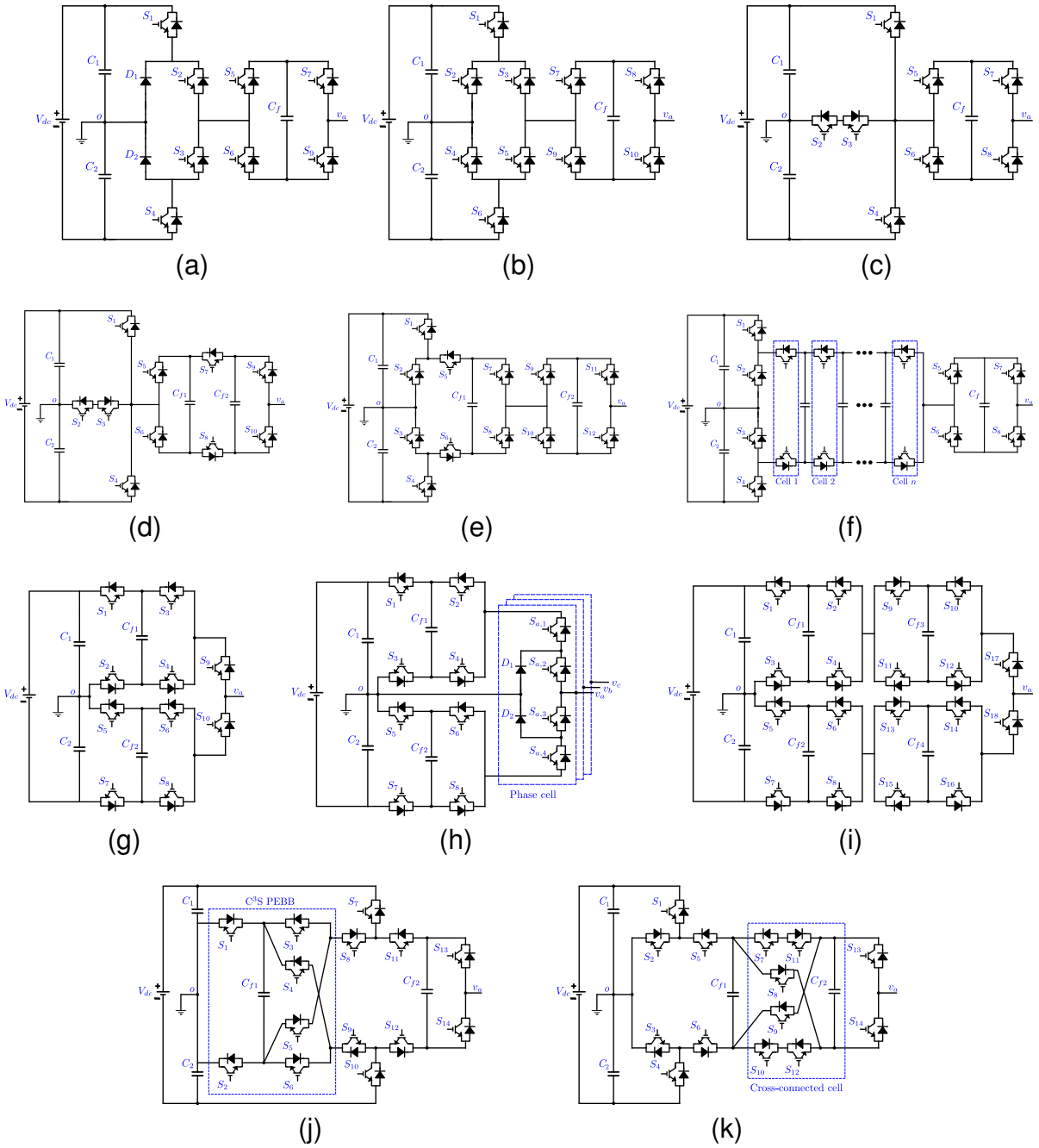


Figure 2.10: Cascaded HMLI topologies. (a) 7L cascaded 3L-NPC with HB in series [113]. (b) 7L/9L cascaded 3L-ANPC with HB in series [114]. (c) 5L/7L cascaded T-type with HB in series [115]. (d) 13L cascaded T-type ANPC with HB in series [116]. (e) 9L cascaded 5L-ANPC with HB in series [67]. (f) Generalized cascaded n-level ANPC with HB in series [117]. (g) 5L cascaded 3L-FC converter [118]. (h) 5L cascaded 3L-FC converter with 3L-NPC [119]. (i) 9L cascaded FC-HB converter [120]. (j) 7L cascaded C3S 5L-ANPC converter [121]. (k) 9L cascaded converter with cross-connected intermediate-level (CCIL) [122].

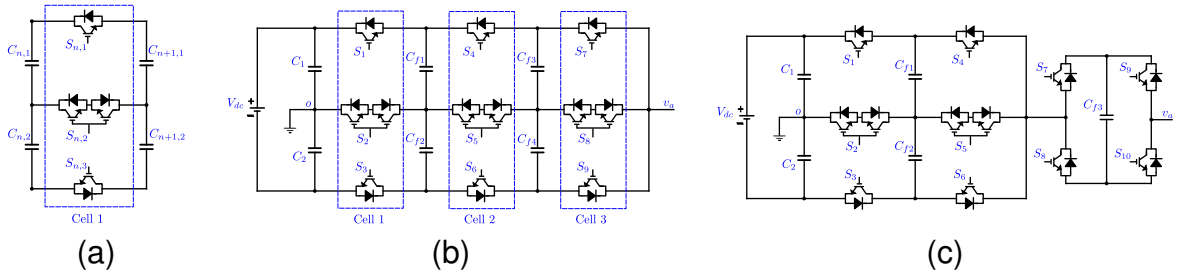


Figure 2.11: Cascaded HMLI topologies based on the Stacked Multicell (SM). (a) Basic cell of the stacked multicell converter [23]. (b) Stacked multicell converter [23]. (c) 9L cascaded SM-HB converter [126].

as the NPC cell and can produce nine levels while retaining redundant switching states for FC voltage balancing. A generalized topology is presented in [117] where a generalized ANPC with n cells is cascaded with a HB cell in series as in Fig. 2.10(f) to produce a total of $4n + 1$ levels.

The cascaded HMLIs discussed so far only used NPC-based cells and HB cells, however other types of basic cells can be used as well. For instance in [118] two parallel FC cells are cascaded with a two-level selector cell in series as shown in Fig. 2.10(g) to produce a dual FC five-level converter. In [119], Karthik and Loganathan modify this topology to reduce the component count in a three-phase converter by sharing the two FC cells along all three phases and using a three-level NPC as a selector cell in each phase, as shown in Fig. 2.10(h). In [120], another modification of the dual FC five-level converter with nine output levels is presented. This is achieved by inserting HB cells in between each of the parallel FC cells and the two-level selector switch as depicted in Fig. 2.10(i). Other cascaded HMLIs combine ANPC and HB cells with a cross-connected FC cell in a seven- and nine-level converter [121, 122]. The seven- and nine-level converters are shown in Figs. 2.10(j) and 2.10(k), respectively.

Lastly the stacked multicell converter (SMC) can also be considered a type of cascaded HMLI, as it is derived by cascading a basic cell both in parallel and in series [23, 127]. Fig. 2.11(a) illustrates the basic cell for a dual-stack multicell converter. A stacked multicell converter with n such basic cells cascaded in series can produce $2n + 1$ output levels, for example Fig. 2.11(b) shows a seven-level SMC with three cells in series. The main advantages of this topology are its high modularity and high number of redundant states. However, compared to other hybrid topologies the SMC requires a larger number of FCs, which not only increases system volume and cost, but also reduces its reliability [96].

The stacked multicell can also be cascaded with other fundamental topologies, for instance in [126] a five-level SMC is cascaded with a HB cell, as shown in Fig. 2.11(c), to produce nine output levels. Compared to the original SMC, fewer FCs are required, while the voltage across the FCs in the SMC cell are balanced at $V_{dc}/4$ and the FC in the HB cell at only $V_{dc}/8$. Proposed for IM drive operation, the topology can also increase the number of output levels to eleven with the goal of increasing the linear modulation range.

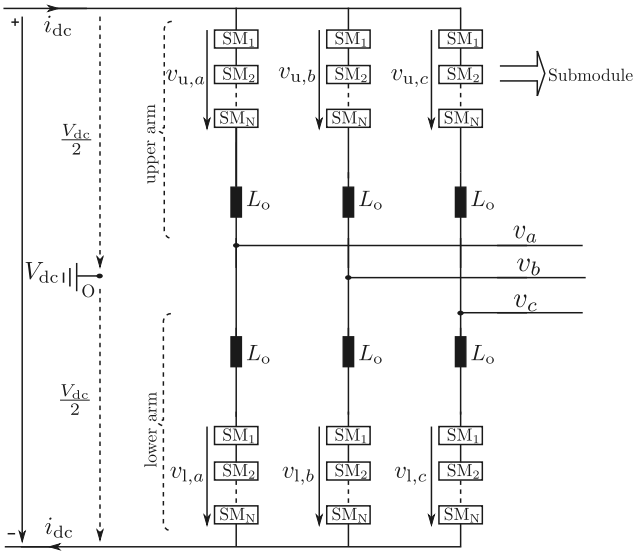


Figure 2.12: Basic structure of a three-phase MMC.

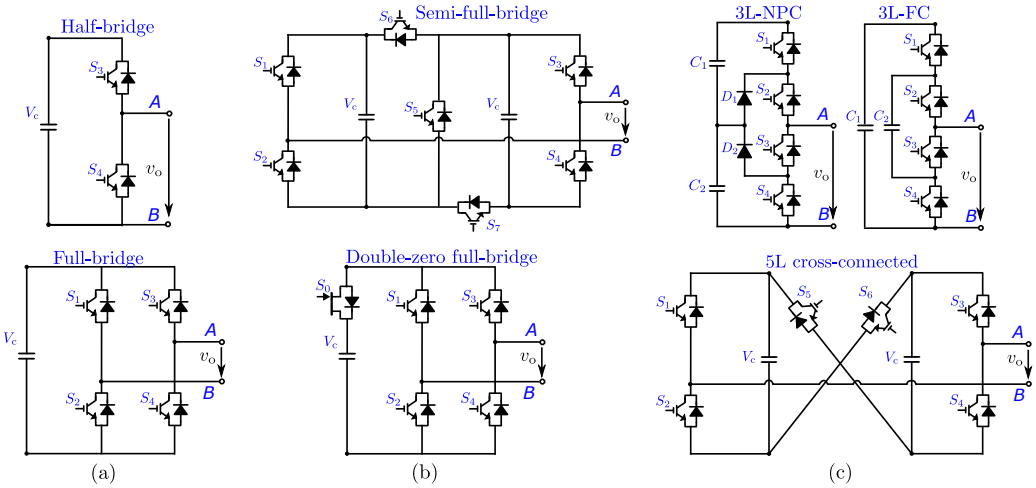


Figure 2.13: Common SM configurations: (a) Basic topologies for SMs, (b) Advanced full-bridge SMs and (c) Multilevel SMs.

2.2.4 MMC category

The modular multilevel converter (MMC) was originally proposed in 2001 in a German utility model and a German patent by Siemens Company and Prof. Marquardt [22, 128]. Later it was introduced to academia by Prof. Marquardt in 2002 [129, 130]. Since then, the MMC has drawn attention among researchers and become the most promising converter topology for medium and high voltage applications due to its high efficiency, low harmonic distortion, high modularity and scalability [131], [132]. A basic structure of a three-phase MMC is shown in Fig. 2.12. The three-phase MMC has three legs, and each phase-leg is divided into two halves, called the upper arm (represented by subscript “u") and the lower arm (represented by subscript “l"). Each arm consists of N series-connected submodules (SMs) and an arm inductor. The arm inductor L_o is used to limit $\frac{di}{dt}$ in the arm currents.

Table 2.2: Quantitative comparison of common three-level topologies.

Topology	N_{US}	N_{BS}	N_{D}	N_{DC}	N_{FC}	V_{MB}	V_{TS}	V_{OP}
3L-NPC [19]	4	0	2	2	0	0.5	2	0.5
3L-FC [20]	4	0	0	2	1	0.5	2	0.5
3L-T^{2}C [12]	2	1	0	2	0	1	3	0.5

2.2.4.1 Basic topologies for SMs

The most popular and widely used SMs in MMC are half and full bridges, as shown in Fig. 2.13(a). The half-bridge SM consists of two IGBTs and one capacitor. The output voltage v_o of the half-bridge SM has two voltage levels, i.e., "0" (S_1 off, S_2 on) and "V_c" (S_1 on, S_2 off). Depending on the combination of different voltage levels of all the SMs in one leg, the phase output voltage varies from -$\frac{V_{\text{dc}}}{2}$ to $\frac{V_{\text{dc}}}{2}$. Due to the simple construction, the half-bridge SM is most commonly used in commercial applications such as MMC-HVDC system [133]. Another topology of the SM is the full bridge, also referred to as an H-bridge converter. In the full-bridge SM, the power capacitors can be connected to the terminal at either polarity, hence it can provide three voltage levels, i.e., "$-V_c$", "0" and "V_c".

2.2.4.2 Advanced full-bridge SMs

In addition to the basic SMs, some advanced full-bridge SMs are introduced, such as semi-full-bridge SM [134] and double-zero full-bridge SM [135, 136]. As shown in Fig. 2.13(b), the semi-full-bridge SM contains two capacitors which can be connected in series or in parallel, hence it can provide four voltage levels, i.e., "$-V_c$", "0", "V_c" and "$2V_c$". Double-zero full-bridge SM, shown in Fig. 2.13(b), is another advanced SM which combines Si IGBT and SiC MOSFET. With the additional SiC switch, both the conduction and switching power losses are reduced.

2.2.4.3 Multilevel SMs

The performance of the SMs can be further improved by using multilevel structure [137]. In multilevel SMs, there are more redundancy switching states in MMC, which significantly improve the controllability of SM capacitor voltages. The structure of three-level NPC SM is shown in Fig. 2.13(c). The three-level NPC MMC has lower semiconductor losses than the full-bridge SM but higher than the half-bridge SM [138]. Besides, the loss is not evenly distributed between the devices, and this SM needs additional voltage balance control. Hence, from the manufacturing and control perspective, the NPC SM is not an attractive solution for MMCs. Another three-level SM is the flying capacitor (FC) SM, as shown in Fig. 2.13(c). This FC SM has similar semiconductor losses with the half-bridge SM and lower loss than the full-bridge SM. Fig. 2.13(c) shows the five-level cross-connected SM which consists of two half-bridge SMs and two extra IGBTs with their anti-parallel diodes [139]. This topology provides five-level quadrant operation and DC fault current limitation.

Table 2.3: Qualitative comparison of common three-level topologies.

Topology	Advantages	Disadvantages
3L-NPC [19]	Simple structure and modulation; equalized voltage blocking; good dynamic response; high efficiency	Unequal loss distribution
3L-FC [20]	Modular structure; fault-tolerance	Complexity of FC voltage balancing
3L-T^{2}C [12]	Simple structure and low losses; no FCs	Higher switch blocking voltages

2.3 Comparison of common dc-link topologies

This section compares a selection of the topologies presented in the previous sections based on both quantitative and qualitative factors. The topologies are compared based on the number of output levels, where three, five, seven, and nine-level topologies are considered.

The evaluated quantitative factors include the semiconductor and capacitor count, required voltage ratings and boost factor, as these factors affect the converters characteristics significantly. For instance, a large switch count requires the implementation of a large number of drivers and increases the modulation complexity and failure rates. Limiting the switch count, however, can reduce the number of redundant states which would otherwise be constructive towards FC voltage balancing, loss distribution, and post-fault reconfiguration.

Similarly, the number of voltage sensors and complexity of voltage balancing algorithms increase with the number of FCs employed. Inverters with natural voltage balancing, however, can significantly reduce the complexity of FC voltage balancing algorithms and the computational load. In general, FCs drastically influence the volume and weight of the inverter, thus decreasing the power density as well as increasing the failure rates which is particularly undesirable in transportation electrification applications and the integrated motor drive configuration [76]. More than two dc-link capacitors will cause similar issues.

Another factor is the maximum switch blocking voltage, which limits topologies for high-voltage application. A high TSV, on the other hand, exacerbates a converters cost. Lastly, converters which have a structure feasible to be constructed from previously manufactured modules have an advantage in terms of industrial applicability.

In order to find an optimal balance between these factors, recently developed topologies follow an application-oriented approach, where the performance of a topology is optimized for the required application voltage and power levels, size, cost, control complexity, loss distribution, reliability and modularity.

For the quantitative comparison, the following parameters are defined: number of unidirectional switches (N_{US}), number of bidirectional switches (N_{BS}), number of diodes (N_{D}), number of dc-link capacitors (N_{DC}), number of flying capacitors (N_{FC}), and phase peak voltage in per unit respective to the dc-link voltage (V_{OP}). In addition, the maximum switch blocking voltage (V_{MB}) and the total standing voltage (V_{TS}) are calculated in all topologies for the same peak-to-peak value of the output phase voltage ($2V_{\mathrm{OP}}$).

Per-phase quantities are considered except for the number of common dc-link capacitors. Although the comparison factors provide an estimated overall cost factor, a qualitative assessment

is nonetheless instrumental in determining performance regarding specific applications.

2.3.1 3L Converters

Three-level converters have seen extensive commercial adoption, with the 3L-NPC [19] being the most popular variant. The 3L-FC [20] and 3L-T^{2}C [12] offer two alternatives that eliminate the need for clamping diodes and flying capacitors, respectively. A comparison of these three-level topologies based on quantitative factors is given in Table 2.2. The qualitative assessment of the three-level topologies is presented in Table 2.3.

2.3.2 5L Converters

The quantitative and qualitative comparisons for selected five-level topologies are presented in Table 2.4 and Table 2.5 respectively. Five-level topologies offer a good balance between performance cost and complexity for several applications and consequently five-level topologies are popular among researchers. The topologies proposed in [101] and [104] have unity dc-link utilization, leading to a potentially increased efficiency or requiring half the original dc-link voltage for meeting the same load voltage requirement. The topologies in [97–100] have higher peak blocking voltages, thus rendering their high voltage applications difficult. Conversely, the lower peak blocking voltages of the topologies in [19, 20, 102] make them preferable for grid-forming, HVDC, FACTS and other high-voltage applications. High number of FCs in [20, 102] will require more sensors and complex balancing schemes. Lower switch count in [84] can be economical but also detrimental in the form of reduced redundant states. Two FCs are used in [119] across all three-phase legs, providing the advantage of simple sensing and balancing control with minimizing the stored energy.

Table 2.4: Quantitative comparison of common five-level topologies.

Topology	N_{US}	N_{BS}	N_{D}	N_{DC}	N_{FC}	V_{MB}	V_{TS}	V_{OP}
5L-NPC [19]	8	0	6	4	0	0.25	2	0.5
5L-FC [20]	8	0	0	2	3	0.25	2	0.5
5L-NNPC [84]	4	1	0	2	0	0.5	2.5	0.5
5L-ANPC Type I [24]	8	0	0	2	1	0.5	3	0.5
5L-ANPC Type-II [97]	4	2	0	2	1	0.75	3.5	0.5
5L-ANPC Type-III [98]	6	1	0	2	1	0.75	3	0.5
5L-6S-ANPC [99]	6	0	2	2	1	0.75	3.5	0.5
5L-7S-ANPC [100]	7	0	2	2	1	0.75	3.75	0.5
5L-6S-ANPCB [101]	4	2	0	2	1	0.5	2.5	1
5L-ANPC-aux [102]	12	0	0	2	3	0.25	3	0.5
5L-ANPC-CCS [104]	10	0	2	2	1	0.25	3	1
Generalized ANPC [140, 141]	8	1	0	2	2	0.5	3.5	0.5
Cascaded FC [118]	10	0	0	2	2	0.5	3	0.5
Cascaded FC-NPC [119]	6.67	0	2	2	0.67	0.5	2.67	0.5

Table 2.5: Qualitative comparison of common five-level topologies.

Topology	Advantages	Disadvantages
5L-NPC [19]	Simple structure and modulation; equalized voltage blocking; good dynamic response; high efficiency	Unequal loss distribution; more dc-link capacitors
5L-FC [20]	Low peak blocking voltage; lack of clamping diodes; modular structure; fault-tolerance	Capacitor balancing issues; high switch and capacitor count
5L-NNPC [84]	Low component count; low TSV	No redundant states; balancing issues
5L-ANPC Type I [24]	Simple structure; hybrid modulation applicable for lower switching losses, lower harmonics and natural capacitor voltage balancing	Unequal device ratings
5L-ANPC Type II [97]	Low switch count; lower conduction losses compared to Type-I 5L-ANPC	High peak blocking voltage; high TSV; capacitor balancing issues at low power factor; unequal switch utilization
5L-ANPC Type III [98]	High efficiency at high modulation index	High peak blocking voltage; low efficiency at low modulation index
5L-6S-ANPC [99]	Low switch count; optimized performance at high power factor	High peak blocking voltage; limited voltage balancing capabilities at low power factors
5L-7S-ANPC [100]	Improved reactive power capability compared to 6S-5L-ANPC	High peak blocking voltage; limited voltage balancing capabilities at low power factors
5L-6S-ANPCB [101]	Unity gain output; better utilization of dc-link	Requires two reverse blocking switches, high current stress of two switches
5L-ANPC-aux [102]	Low peak blocking voltage; capacitors have snubber-like behavior, thus reducing semiconductor overvoltages; diminished capacitor sizes	High switch and FC count
5L-ANPC CCS [104]	Unity gain output; natural FC balancing	Larger sum of voltage and current stresses; high FCs size
Generalized ANPC [140, 141]	High number of redundant states; fault-tolerance capabilities through post-fault reconfiguration; wide modulation index operation	High switch and capacitor count for 5L operation
Cascaded FC [118]	Even loss distribution; solved transient voltage balancing issues	High active switch count
Cascaded FC-NPC [119]	Minimized energy stored in FC; fault-tolerant operation	High number of conducting switches per level; high conduction loss

2.3.3 7L Converters

Table 2.6 and Table 2.7 give the quantitative and comparative assessment of seven-level topologies. Topologies described in [108], [64], [114] and [115] perform better in terms of dc-link voltage utilization. The FC count in the 7L-FC limits their feasibility as the sensor requirements and balancing complexities will be sizeable [20]. The double-midpoint ANPC [112] employs three dc-link capacitors leading to balancing complexities. The boost-ANPC topology in [64] has a dc-link utilization of 1.5 with the downside of the charging inrush current and increasing the current stress of the switches.

Table 2.6: Quantitative comparison of common seven-level topologies.

Topology	N_{US}	N_{BS}	N_{D}	N_{DC}	N_{FC}	V_{MB}	V_{TS}	V_{OP}
7L-FC [20]	10	0	0	2	3	0.167	2	0.5
7L-ANPC-aux [107]	18	0	1	2	5	0.167	3	0.5
7L-8S-ANPC [108]	8	0	0	2	2	0.5	2.5	1
Boost-ANPC [64]	7	1	0	2	1	0.33	2.67	1.5
Generalized ANPC [140]	8	1	0	2	2	0.5	3.33	0.5
Double-midpoint ANPC [112]	10	2	0	3	2	0.33	4	0.5
Cascaded HB-ANPC [114]	10	0	0	2	1	0.33	2.67	0.75
Cascaded T-type HB [115]	6	1	0	2	1	0.33	2.67	0.75

2.3.4 9L Converters

Nine-level topologies can operate with reduced filter size requirements relative to lower-level topologies while meeting the relevant harmonic standards. Table 2.8 and Table 2.9 describe the quantitative and comparative assessment of the topologies. The classical 9L-NPC [19] and 9L-FC [20] topologies have severe challenges because of higher switch and capacitor count. The split-capacitor unity-gain ANPC [143] has unity gain dc-link utilization. The high maximum blocking voltage of the T-ANPC [142] and the total blocking voltages of generalized series HB-ANPC [120] is undesirable for high-voltage applications. The FC-CHB topology [120] is capable of post-fault operation which is vital for reliability-critical applications, however, the high FC count of the cascaded has a negative impact on the control complexity and power density.

2.4 Modulation Methods

A classification of the major control techniques for MLIs is shown in Fig. 2.14. While some control techniques such as direct torque control (DTC) and MPC have implicit modulators, other techniques need an independent modulator stage to generate the inverter pulses based on the output of the controller and the operating conditions of the inverter. As with the two-level converter, the cascaded control structure usually consists of outer and inner control stages in addition to the modulator block. Although the inner and outer loops are similar in the two-level and MLI topologies, the modulator stage needs to be adapted as the number of levels

Table 2.7: Qualitative comparison of common seven-level topologies.

Topology	Advantages	Disadvantages
7L-FC [20]	Redundant switching states; low maximum blocking voltage; fault-tolerance	High FCs and switch count
7L-ANPC- aux [107]	Resolves issue of dynamic voltage sharing in series switches and multilevel voltage jumping of phase output voltages	Increased commutation times, high number of FCs and required sensors, and complexity of deadtime compensation algorithm
7L-8S-ANPC [108]	Unity gain output; better utilization of dc-link	Control requirement for capacitor balancing, high current stress of two switches
Boost-ANPC [64]	Boosted dc-link voltage utilization	Charging operation creates significant pulsating current; capacitor voltage ripple, high number of conducting switches increases conduction losses
Generalized ANPC [140]	Ample redundant states; high efficiency	Relatively high number of switches for 7L operation
Double-midpoint ANPC [112]	Low switch voltage stress	High device and capacitor count; complex dc-link balancing
Cascaded HB-ANPC [114]	Relatively high dc-link voltage utilization; FC voltage balancing achievable at higher modulation indices for inductive dominant loads; fundamental frequency modulation possible	High TSV, relatively high size of FC
Cascaded T-type HB [115]	Relatively high dc-link voltage utilization; low number of switches	Complexity of voltage balancing algorithm

Table 2.8: Quantitative comparison of common nine-level topologies.

Topology	N_{US}	N_{BS}	N_{D}	N_{DC}	N_{FC}	V_{MB}	V_{TS}	V_{OP}
T-ANPC [142]	8	1	0	2	2	0.75	3	0.5
split-capacitor unity-gain ANPC [143]	8	1	4	2	2	0.5	2.75	1
CCIL converter [122]	10	2	0	2	2	0.5	3.75	0.5
9L-SMC [23]	8	4	0	2	6	0.25	3	0.5
Series HB-ANPC [67]	12	0	0	2	2	0.5	3.5	0.5
Cascaded FC-CHB [120]	18	0	0	2	4	0.5	4	0.5
Cascaded SM-HB [126]	8	2	0	2	3	0.5	3.5	0.5

Table 2.9: Qualitative comparison of common nine-level topologies.

Topology	Advantages	Disadvantages
T-ANPC [142]	Low device count	High peak voltage stresses on devices
Split-capacitor unity-gain ANPC [143]	Unity dc-link voltage utilization; capacitor voltage self-balancing	Four clamping diodes required, high conduction losses, high current stress on switches due to capacitor charging
CCIL converter [122]	Ample redundant switching states; simple capacitor voltage balancing mechanism implementation for non-boosting configuration	Addition control and device complexity for boosting configuration
9L-SMC [23]	Ample redundant switching states; high modularity; low-voltage switches and TSV	High number of switches and FCs; high number of conducting switches per level
Series HB-ANPC [67]	Redundant states for balancing FC voltages; operation feasible at all power factors through full modulation index range	High number of conducting switches per level utilization
Cascaded FC-CHB [120]	Fault-tolerance; high modularity, low-voltage switches	Complex capacitor voltage balancing control
Cascaded SM-HB [126]	High dc-link utilization; redundant states	Capacitor balancing at unity power factor

goes higher. In this section, a review of the most popular modulators is presented. A general classification of the modulation techniques for MLIs is shown in Fig. 2.15

2.4.1 Carrier-based PWM techniques

The most straightforward modulation techniques for MLIs are carrier-based PWM (CB-PWM) techniques. In their most well-known form, level-shifted PWM (LS-PWM) and phase-shifted PWM (PS-PWM) have been constantly used in various applications ranging from industrial to automotive applications. LS-SPWM can be further classified into Phase-disposition PWM (PD-PWM) and phase-opposition-disposition PWM (POD-PWM) [144]. In a comparison between these two techniques, the LS-SPWM shows a better output THD with similar operating conditions while suffering from unequal switch utilization. This issue and potential solutions are discussed in detail in [145].

Several modifications have been proposed in the literature for these well-known carrier-based modulators to address their control limitations. In [57], the voltage balancing issue of the FC inverter is addressed by symmetrically arranging the carrier signals in each fundamental period. In [146], the voltage oscillations in low-frequency operation are mitigated at the cost of increased switching frequency by having two modulating signals for each of the converter three phases. Also, the maximum achievable amplitude of the output waveform is improved. In another study [93], a modified PWM technique is used for the NNPC inverter structure in which

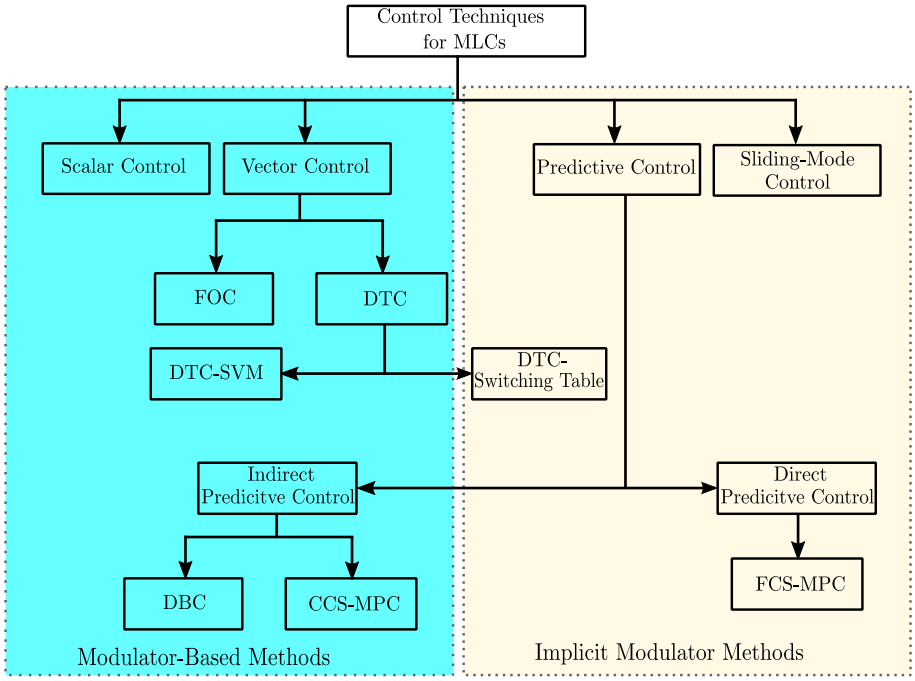


Figure 2.14: Common control techniques of MLIs

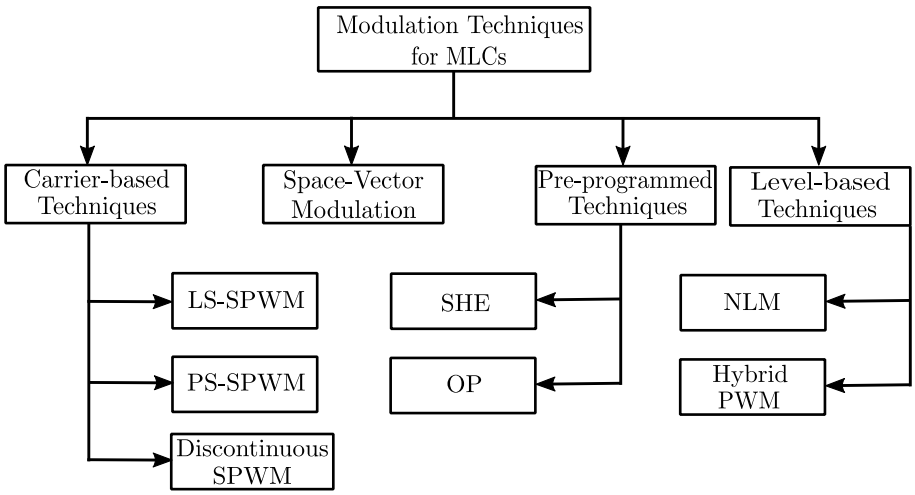


Figure 2.15: Common modulation techniques in MLIs

the voltage of the FC is ensured to remain in the required range.

In addition to the sinusoidal PWM techniques, discontinuous PWM (DPWM) techniques are also extended to multilevel structures, offering significant advantages in terms of inverter power loss. This modulating technique avoids switching events when the switch currents are at the peak in their periods. Based on the study in [64], with a switching frequency of 10 kHz, the total power loss of the inverter can be reduced by 10-20% based on the modulation index. However, a slight increase in the THD value of the load current is the downside of the DPWM. Another drawback of this modulation scheme is the voltage balancing issue due to limited switching events at peak currents. This issue is addressed for an NPC inverter in [147] by using different switching patterns based on the operating point of the inverter in terms of modulation index and

output waveform frequency.

Finally, hybrid PWM methods, in which continuous and discontinuous PWM schemes are used together to take advantage of both low THD and low switching losses can be beneficial. The interval that each method is being used determines the trade-off between the two control objectives of the high-quality output waveform and low switching losses.

2.4.2 Space vector modulation techniques

Space vector modulation (SVM) has a superior performance compared with other modulation techniques when it comes to parameters such as voltage balancing, common mode voltage (CMV) reduction, low-harmonic output,dc-link utilization, and transient response [144]. In addition, the complexity of the technique is acceptable when used in three-level inverters. In fact, SVM is the most used modulating technique in applications that require fast dynamic response such as traction applications. However, the main drawback of this technique arises when the number of inverter levels goes higher. The number of available voltage vectors increases from 27 to 125 when moving from a three-level inverter to a five-level structure. Generally, there exists n^3 combination of switching states in an n-level inverter [148].

The implementation of the SVM usually includes several steps. First, using the output of the control stage, the sector that the reference vector lies within is specified by coordinate transformation. Then, the switching times are calculated and the vectors that will be applied are determined. Mapping to two-level SVM techniques can be used to determine the duration of each vector. Finally, the switching sequence will be determined in order to achieve equal switching loss, minimum THD, and minimum voltage imbalance [149].

The additional flexibility in selecting the optimal vector in the SVM scheme addresses many issues in the MLIs that were investigated in the prior sections. Mitigating the fluctuations in the NP potential of NPC-based inverters or the voltage imbalance in FC-based inverters can be accomplished by removing the medium vectors in the space vector diagram (SVD) and introducing virtual vectors in virtual SVM (VSVM) [144, 150]. Another consequence of the added flexibility and redundant vectors in SVM is the capability of the modulator to remove the vectors that cause larger CMV.

As a result of the increased complexity of the controller with SVM scheme in MLIs, many recent studies in the literature have dealt with proposing methods to simplify the modulator. In [149], a generalized method is proposed for MLIs with any number of levels in which a reverse mapping technique from two-level inverter structure is exploited which effectively generates the vectors and pulses for the switches. This scheme has eliminated the need for an additional look-up table. The look-up tables can put a considerable burden on the memory. Similar mapping methods are presented in other studies that can be extended to any number of levels [148].

2.4.3 Pre-programmed schemes

The selective harmonic elimination (SHE) modulation scheme and its variant, optimal pulse pattern (OPP), apply the switching transitions at certain pre-programmed angles in order to eliminate certain harmonics from the output waveform [151]. The optimum firing angles in

the SHE method is usually driven by solving the harmonic elimination equations using either numerical or intelligent algorithms.

Although SHE method can effectively eliminate low-order harmonics, the overall output THD still remains at high values due to the low effective switching frequency. SHE method is mainly interesting at high-power, high-voltage applications with MMC inverters that operate at low switching frequencies [152].

The low switching frequency in SHE results in high voltage fluctuations on the capacitors or the NP which makes it unattractive for applications that require a high power density with small capacitors. Also, the voltage balancing techniques proposed for the SHE are usually unable to perform at all power factor conditions. In [151], a phase shift is applied to the original firing angles to extend the NP voltage balancing to all power factors.

2.4.4 Level-based schemes

The nearest level modulation (NLM), which is the main level-based modulation scheme, share some characteristics with the SHE method [153]. Similar to SHE, NLM has the advantage of low switching frequency which makes it suitable for high-power applications which use slower switching devices. On the downside, similar to SHE, they have a poorer output waveform quality and a slower dynamic response when compared to SPWM and SVM techniques. However, unlike SHE, NLM method does not require trigger angle calculations. Instead, at each sampling time, the required number of upper and lower inserted submodules are simply calculated using the reference voltage and a rounding function. Therefore, it benefits from a higher simplicity which makes it a suitable modulation method for high-level MMC inverters in high-voltage applications in which the large number of levels can improve the THD [153].

Some studies have focused on improving the characteristics of the conventional NLM scheme. In [153], the number of output levels has been approximately doubled so the method is applicable to medium-voltage applications. However, this level-increased NLM scheme leads to a higher value of peak-to-peak circulating current. This issue is addressed in [154], in which a deadbeat control is applied to suppress the circulating harmonic currents.

Windowed PWM (WPWM) is another hybrid modulation technique proposed in [155] that combines the NLM and sinusoidal PWM techniques to benefit from the advantages of both techniques in low-voltage applications. The modulation switches between NLM and SPWM in different intervals based on the operating conditions of the MLI.

2.5 Industrial applications

Nowadays, many common dc-link (NPC, T3, ANPC, FC) and multiple dc-source (CHB) multilevel converter topologies have been increasingly made available in the market to meet the industrial demand for high-power delivery and overcome the voltage/current rating limitation of switches. Historically, CHB inverters are characterized by their modularity, fault tolerance, and ability to generate a high number of voltage levels by cascading cells. However, the requirement of multiple isolated DC sources (rectifier+transformer from the industry point of view) limits their applicability for a vast range of power ratings. Indeed, CHB inverters are mostly employed in high-power applications (ranging from hundreds of kilowatts to megawatts) where there are

Table 2.10: Common industrial MLI switch modules.

Company	Module Topology	Voltage Rating	Current Rating	Applications
Vincotech [156]	NPC	1200/1500V	30 to 1800A	Drives Solar Inverters UPS
Vincotech [157]	T3	650/1200V	25 to 1800A	Drives Solar Inverters UPS
Vincotech [158]	ANPC	1200/1500V	150/300/600A	Solar Inverters
Vincotech [159]	FC	1200V	200A	Drives Solar Inverters UPS
Fuji Electric [160]	T3	600/900/1200V	50 to 600A	Drives Power Conditioners UPS
Semikron [161]	NPC	650/1200V	20 to 600A	Wind Turbine Converters Solar Inverters UPS
Semikron [161]	T3	650/1200V	50 to 600A	Wind Turbine Converters Solar Inverters UPS
Infineon [162]	NPC	650/1200V	30 to 400A	High-speed Drives Solar Inverters UPS
Infineon [162]	T3	650/1200V	15 to 600A	High-speed Drives Solar Inverters UPS

Table 2.11: Common dc-link MLIs in industry.

Company	Product Series	Topology	V/I/P Rating	Applications
Toshiba	T300MVi	NPC	6600V/391A	Drive
Toshiba		MMC	250kV/1200A	HVDC
ABB	ACS6000	NPC	3-3.3kV	Drive
ABB	ACS2000	ANPC	6kV/800kW	Drive
Siemens	SINAMICS GH150	MMC	4-13.8kV	Drive
Schneider Electric	Altivar 1260	NPC	4.16kV	Drive

no available components for such ratings. On the other side, common dc-link topologies are characterized by the employment of a single DC source making them a good alternative in various applications such as 3-phase industrial systems. Indeed, they can be employed in many configurations such as 3-Leg 3-Wire, 3-Leg 4-Wire, and 4-Leg 4-Wire in motor drives, PV inverters, fast DC chargers, etc. Recently, Vincotech, Semikron, Infineon, and Fuji Electric companies have manufactured switch units for higher efficiency and reduced size ANPC, NPC, and T3 (Table 2.10) inverters by combining many IGBTs and diodes. Vincotech has also developed other modules like FC and H6.5 for various applications such as PV inverters, drives, UPS, and pumps. In terms of medium voltage applications, FC inverters have been used by Alstom Industry and ALSTOM DRIVES and CONTROLS LTD for the control of synchronous and asynchronous machines of a few megawatts [163]. Moreover, some European locomotives have been using FC inverters to adapt to specific voltages and frequencies of the different European railway networks (1.5-kVDC, 25-kV/50Hz, 15-kV/16Hz or 3-kVDC). This adaptation feature makes possible the reduction of the size and cost of the used components. In HVDC applications, MMC topologies are getting an increased interest where they have been used by SIEMENS for the realization of an HVDC transmission system (320kV/2000MVA) between France and Spain [164]. Nowadays, industries are more interested in using MLIs for high and

medium power ratings where 3-phase topologies should be used. It is almost impractical to use topologies with multiple isolated DC sources. Therefore, MLIs with common DC bus have been paid an increased interest in high power applications (pumps, conveyors, fans, traction systems). However, one should note that the increase of active/passive components count will affect the size and cost of the power converter, which is highly undesirable. Thus, market players should find a compromise between the cost, voltage balancing, size, reliability, manufacturing, etc. For instance, Schneider Electric has been using a 3L-NPC for motor drives and 4L-FC for UPS applications, while Toshiba has been employing the 3L-NPC and 3L/5L PWM converters in high-power drive applications. Recently, Huawei has revealed the employment of the 5L-MLI technology in their data centers. Some of the industrial common dc-link MLI products are listed in Table 2.11.

2.6 Discussion and summary

MLIs are getting significant attention from industry and play an important role in the new generation of power converters. However, one of the main barriers to the widespread use of MLIs in the industry is design complexity. Although a higher number of voltage levels reduces inherently the harmonic content and reduces the size and losses of output filters, it requires a higher number of switches, auxiliary capacitors, and consequently more gate drivers and complex voltage balancing techniques. Moreover, capacitors are considered points of failure in addition to their significant contribution to the reduction of the reliability and lifetime of the converter. Thus, there should be a trade-off between the high performance and reliability of MLIs. Currently, three-level and five-level converters are considered matured and widely developed/manufactured by companies for many applications. Thus, taking into account that industries are interested in simplicity and high performance for their next generation of power electronic converters and based on the review study performed in this chapter, the future research and development challenges could be listed as follows:

1. Developing 5L+ topologies with a reduced component count,
2. Developing bidirectional common dc-link converter topologies for grid-connected and stand-alone modes of operations,
3. Reducing the complexity of controllers by proposing new switching strategies with integrated voltage balancing,
4. Increasing efficiency, improving power density, and reducing losses.

In summary, this chapter presented a comprehensive review of common dc-link MLIs, including their topological evolution, features, comparison of different topologies, modulation techniques, and potential application areas. The findings of this chapter reveal that common dc-link topologies are the dominant choice in industrial applications due to their versatility and compatibility with different power conversion systems. The study demonstrated that common dc-link MLIs have significant potential for further development and implementation. However, there is still a need for further research in areas such as cost-effectiveness, efficiency, fault-tolerant operation and reliability to fully realize their potential.

CHAPTER 3

A Nine-Level Split-Capacitor ANPC Converter and Its Optimal Modulation Technique

This chapter proposes a novel hybrid nine-level inverter as an upgraded version of the commercialized 5L-ANPC topology for high-efficiency low- and medium-voltage medium-power applications. Section 3.2 describes the derivation, description and operating principles of the proposed topology. The FCs charging/discharging process and developed modulation method are explained in Section 3.3. Section 3.4 presents the derivation of the mathematical relationship to determine the capacitance of the FCs and modulation index limitations. Power loss analysis is presented in Section 3.5. The simulation studies are conducted in Section 3.6. The experimental implementation, performance evaluation and discussion of the results are presented in Section 3.7. Finally, the summary of the chapter is given in Section 3.8.

3.1 Introduction

The generalized structure of the ANPC topology is shown in Fig. 3.1 for the three variants. For seven-level operation, ten active switches and two FCs are required, while for nine-level operation, twelve active switches and three FCs are included. Despite the practical possibility of the 7L- and 9L-ANPC implementation when higher power quality is required, it is industrially desirable to further reduce the required components, and hence cost and control. Several ANPC-based topologies have been proposed with reduced components. The first attempt to upgrade the 5L-ANPC was proposed in [67] for wind turbine grid-connected applications. Nine levels can be deduced from this topology by connecting a 5L-ANPC with H-bridge unit.

In [108], a 7L-ANPC inverter with boosting capability was proposed using only eight switches and two diodes to block the reverse current path of two switches. The main drawback of this topology is that one of the FCs should be rated at the full dc-link voltage, which significantly increases the converter volume and cost. A nine-level modified ANPC topology with reduced switches count was presented in [60] by adding only two switches to the 5L-ANPC

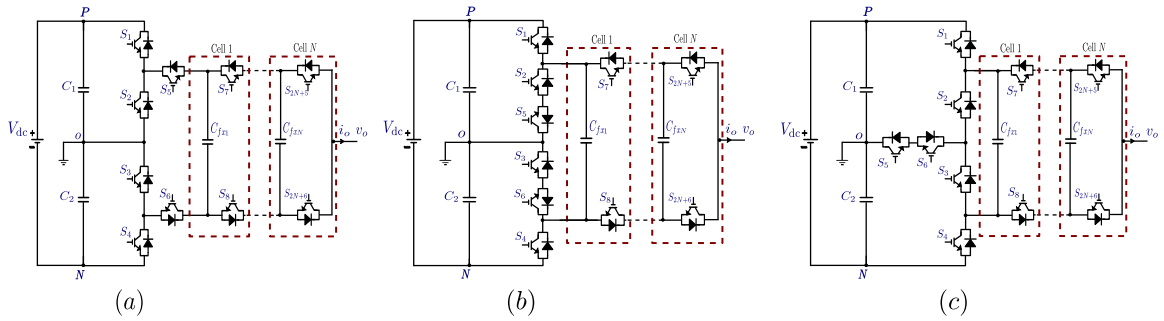


Figure 3.1: Generalized structure of the conventional 5L-ANPC: (a) variant I. (b) variant II. (c) variant III.

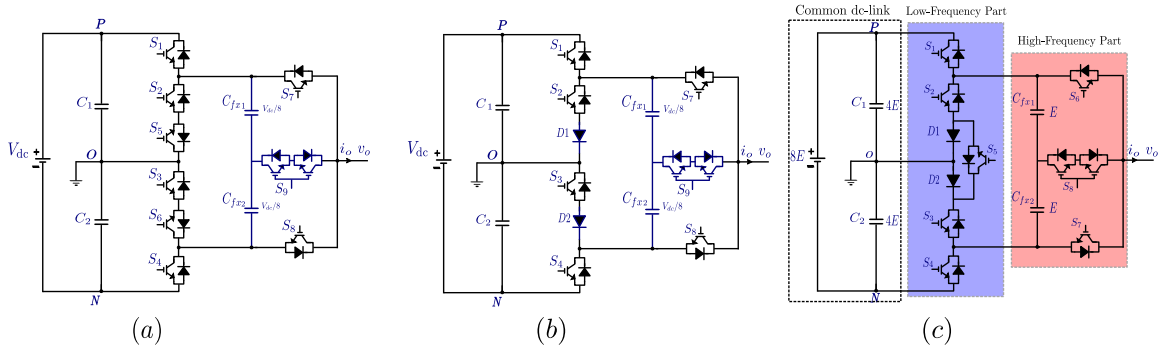


Figure 3.2: Derivation of the 9L-SC-ANPC inverter: (a) modification 1. (b) modification 2. (c) proposed 9L-SC-ANPC inverter.

with a blocking voltage equal to the full dc-link. In addition to the high total standing voltage (TSV) of this topology, the dc-link cannot be shared in the three-phase operation, which creates additional costs for three-phase applications. In [122], a nine-level inverter with a single capacitor was developed, which consists of a 5L-ANPC inverter with two cross-connected switches. Despite the reduction in passive components in this topology, complex control techniques are required for FC and NP regulations and also the maximum modulation index is limited to 0.91 [122]. Several other ANPC-based topologies have been presented in the literature in order to develop high-level MLIs with few components and low cost [64–66]. However, most of these topologies lost inherent features of the ANPC topology, either through the use of switches and/or FCs with higher voltage ratings or through the loss of the ability to utilize a common dc-link in three-phase applications, which has a negative impact on cost, reliability and thus employability of these topologies.

The impetus here is to upgrade the conventional 5L-ANPC to a nine-level topology with reducing the topological complexity and control implementation and without increasing the voltage rating of switches or FCs. Based on the above-mentioned analysis, challenges and advantages of ANPC-based topologies, a novel nine-level split-capacitor ANPC (9L-SC-ANPC) inverter is proposed. Compared with the other 9L-ANPC inverters, the proposed topology not only reduces the number of power devices and capacitors but also the nominal voltage of the FCs, thereby reducing the converter volume and cost. To generate the desired voltage levels and simultaneously balance the FCs and NP, a modulation method based on phase-disposition PWM

(PD-PWM) is developed for the proposed inverter exploiting the existing redundant states with the ability to operate properly under different operating conditions of modulation index and power factor.

3.2 Proposed Nine-level Split-Capacitor ANPC

3.2.1 Derivation of the 9L-SC-ANPC inverter

To generate a five-level output voltage with the 5L-ANPC, the FC should be balanced at one-quarter of the dc-link voltage. The generated levels are $\pm V_{\text{dc}}/2$, $\pm V_{\text{dc}}/4$ and 0. One important advantage of this topology is the availability of three redundant states. Two of them generate $\pm V_{\text{dc}}/4$ and are typically used for FC and NP balancing, which in turn reduces the control complexity. While the third redundant state is available for zero level generation and can be used for switching frequency reduction [24].

The objective of this chapter is to generate a higher number of levels without adding a high number of power devices or capacitors as required in the conventional topology. It is also important to negate a common detriment of most of the recent ANPC-based topologies, which is using high-voltage power devices or FCs. Keeping that in mind and considering the 5L-ANPC variant II, the first refinement is made by replacing the FC with two series-connected capacitors and one four-quadrant switch, which can be realized by connecting two switches in series as shown in Fig. 3.2a. The two FCs form a single auxiliary dc-link rated at $V_{\text{dc}}/4$, i.e. each capacitor should be stabilized at $V_{\text{dc}}/8$. With this modification, nine levels can be produced from this configuration with keeping the redundant switching states, which is an inherent feature of the conventional 5L-ANPC. The achievable levels with this modification are $\pm V_{\text{dc}}/2$, $\pm 3V_{\text{dc}}/8$, $\pm V_{\text{dc}}/4$, $\pm V_{\text{dc}}/8$, and 0. For simplification and by setting the dc input to $8E$, these levels can be defined as $\pm 4E$, $\pm 3E$, $\pm 2E$, $\pm E$, and 0.

Referring to Fig. 3.2a, S_5 and S_6 are used to prevent the direct parallel connection of the FCs with one of the dc-link capacitors. For illustration, S_5 blocks the current to flow from point O to N directly through FCs when S_4 is ON. Similarly, the direct current path via FCs from P to O is blocked by S_6 when S_1 is ON. By exploiting the modification concept proposed in [99], S_5 and S_6 are replaced by two diodes D_1 and D_2, (see Fig. 3.2b). However, the current path becomes unidirectional, which means only active power can be supplied. To negate this detriment, switch S_5 is connected in parallel with the two diodes to enable a bidirectional flow of the current through point O as shown in Fig. 3.2c. It should be mentioned that S_5 carries current only during low voltage levels and when it is required to supply reactive power. With this modification, two active switches are replaced by two diodes and one low-current low-voltage switch.

The derived inverter has the ability to generate nine voltage levels with only nine active switches, two discrete diodes and two capacitors regulated at $V_{\text{dc}}/8$, while the 9L-ANPC (conventional extension of 5L-ANPC) requires 12 active switches and 3 capacitors regulated at $V_{\text{dc}}/8$, $V_{\text{dc}}/4$, and $3V_{\text{dc}}/8$. In addition, it can cover the operation of conventional 5L-ANPC. The operating principles and analysis of the proposed 9L-SC-ANPC inverter are detailed in the following section.

Table 3.1: Switching table of the 9L-SC-ANPC inverter (−: No effect, ↑: capacitor charging, ↓: capacitor discharging).

										$i_o > 0$		$i_o < 0$	
State	s_1	s_2	s_3	s_4	s_5	s_6	s_7	s_8	v_o	C_{fx1}	C_{fx2}	C_{fx1}	C_{fx2}
V_1	1	0	1	0	0	1	0	0	+4E	−	−	−	−
V_2	1	0	1	0	0	0	0	1	+3E	↑	−	↓	−
V_3	1	0	1	0	0	0	1	0	+2E	↑	↑	↓	↓
V_4	0	0	1	0	1	1	0	0	+2E	↓	↓	↑	↑
V_5	0	0	1	0	1	0	0	1	+E	−	↓	−	↑
V_6	0	0	1	0	1	0	1	0	0	−	−	−	−
V_7	0	1	0	0	1	1	0	0	0	−	−	−	−
V_8	0	1	0	0	1	0	0	1	-E	↑	−	↓	−
V_9	0	1	0	0	1	0	1	0	-2E	↑	↑	↓	↓
V_{10}	0	1	0	1	0	1	0	0	-2E	↓	↓	↑	↑
V_{11}	0	1	0	1	0	0	0	1	-3E	−	↓	−	↑
V_{12}	0	1	0	1	0	0	1	0	-4E	−	−	−	−

3.2.2 Topology description and operating principles

One phase leg of the 9L-SC-ANPC inverter is shown in Fig. 3.2c. The dc-link is constituted by two capacitors C_1 and C_2, with a voltage of $4E$ each. The auxiliary dc-link is formed by two FCs C_{fx1} and C_{fx2}, whose voltages have to be maintained at E for each capacitor, where $x \in \{a, b, c\}$ denotes the respective phase. The switching states of the 9L-SC-ANPC inverter with their corresponding voltages and effects on the FCs are listed in Table 3.1. The switching function s_i ($i = \{1, 2, 3, .., 8\}$) of switch S_i can be defined as

$$s_i = \begin{cases} 1, & \text{if } S_i \text{ is ON} \\ 0, & \text{if } S_i \text{ is OFF.} \end{cases} \tag{3.1}$$

The current paths for the obtainable nine levels for one phase leg are shown in Fig. 3.3. Note that the green dashed line indicates the active current path while the red dashed line indicates the reactive current. Since both FCs are forming a single auxiliary DC-link, they can be charged or discharged simultaneously with the same redundant state. Twelve states are provided and labeled by V_1 to V_{12}. Three levels have redundant states: ($+2E$: V_3 and V_4), (0: V_6 and V_7), and ($-2E$: V_9 and V_{10}).

The switches can be divided into three sets based on their complementary operation: {S_1, S_4, S_5}, {S_2, S_3}, and {S_6, S_7, S_8}. Note that the first and second sets operate at a low frequency, while the third set has higher switching frequencies. The voltage stresses of switches S_1, S_2, S_3, S_4, S_5, S_6 and S_7 are the same as in the 5L-ANPC variant II, where the blocking voltages are $0.75V_{\text{dc}}$ for S_1 and S_4, $0.5V_{\text{dc}}$ for S_2 and S_3, and $0.25V_{\text{dc}}$ for S_5, S_6 and S_7. The four-quadrant switch S_8 handles only voltage stresses of $V_{\text{dc}}/8$ but in both directions ($\pm V_{\text{dc}}/8$), while S_8 in the 5L-ANPC has to withstand a voltage stress of $0.25V_{\text{dc}}$ [99]. Accordingly, the TSV of the proposed 9L-SC-ANPC inverter is the same as that of the conventional 5L-ANPC variant II with a value of $3.5V_{\text{dc}}$. According to the operation of the 9L-SC-ANPC inverter, the blocked voltages of the switches for each state are shown in Fig. 3.4. Similar to the 5L-ANPC variant

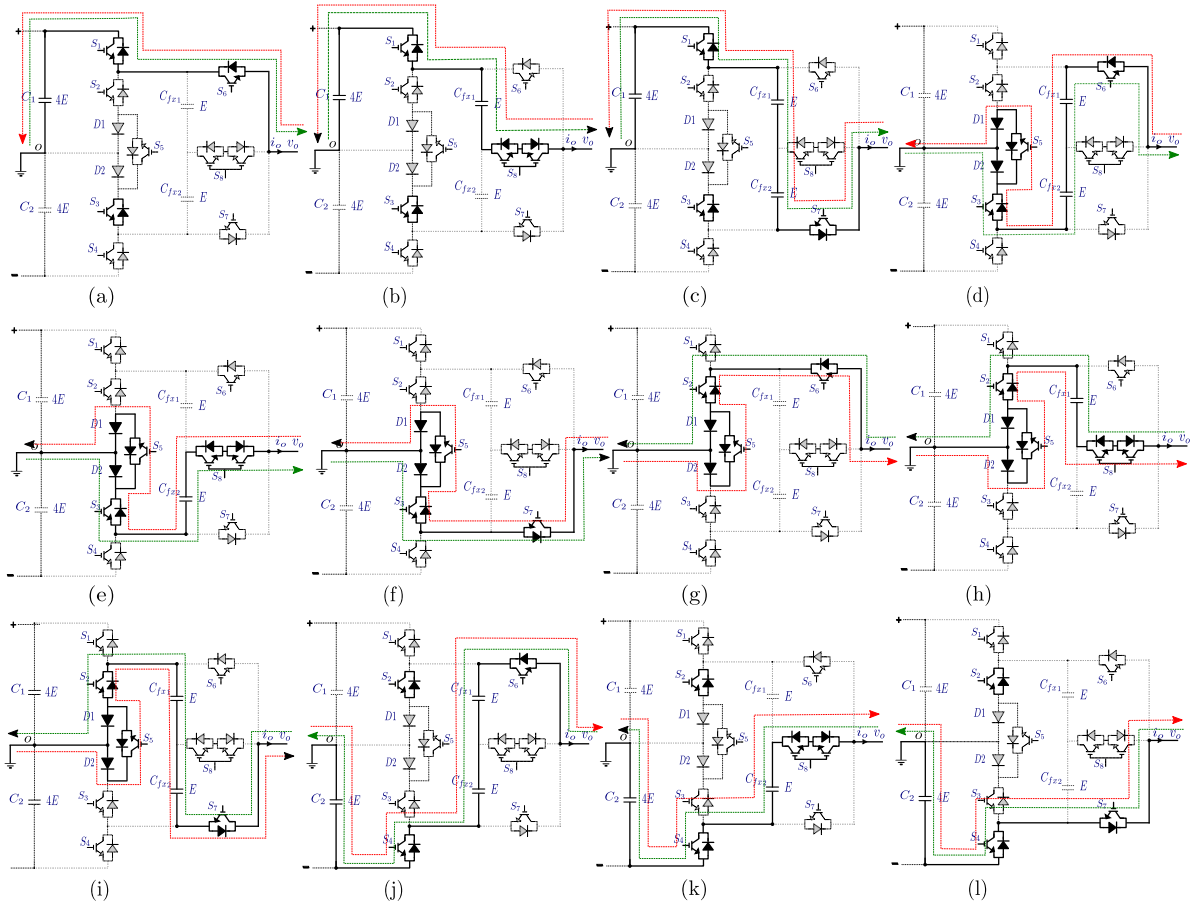


Figure 3.3: Active and reactive current paths of the 9L-SC-ANPC inverter during all switching states. (a) State V_1. (b) State V_2. (c) State V_3. (d) State V_4. (e) State V_5. (f) State V_6. (g) State V_7. (h) State V_8. (i) State V_9. (j) State V_{10}. (k) State V_{10}. (l) State V_{12}.

II, the switches of high voltage ratings are operated at a low switching frequency, while those of low voltage ratings have higher switching frequency, which has a positive impact on the loss distribution among the switches.

From Table 3.1, one can observe two important aspects. First, the redundant states of levels $+2E$ and $-2E$ have an opposite impact on the FCs. Second, for each redundant state, the effects on the two FCs are the same, charging or discharging. Based on these two key observations, the balancing of the FCs and NP can be achieved as detailed in Section 3.3. In doing so, the output current i_o and the actual value of the auxiliary dc-link (two FCs) are required to identify the proper state. For instance, for level $+2E$, if the FCs voltage V_{fx} is higher than its reference V_{fx}^* and i_o positive, then state V_4 is selected to discharge the FCs. In addition, NP balancing is also taken into account by adjusting the reference voltages of the FCs. The active voltage balancing method is integrated into the adopted PD-PWM strategy without using additional conventional or advanced controllers.

The extension of the proposed 9L-SC-ANPC inverter can be realized by adding extension units to each phase legs, comprising of one auxiliary dc-link, two active switches and one four-quadrant switch. The generalized structure of the proposed topology for n-level operation is

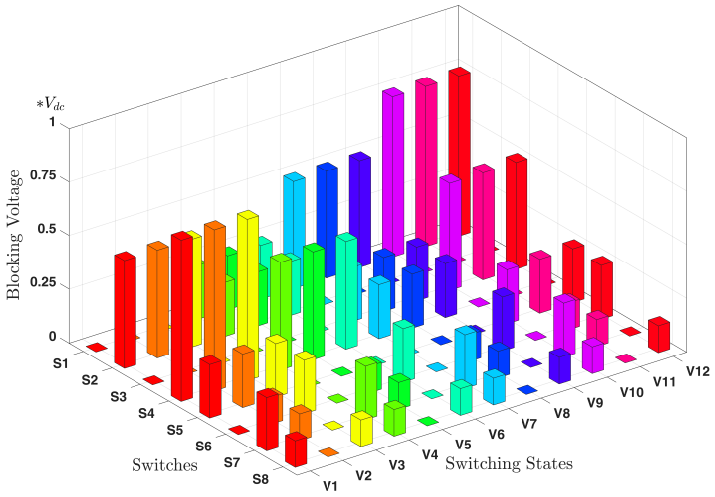


Figure 3.4: Blocking voltage of the active switches during the switching states.

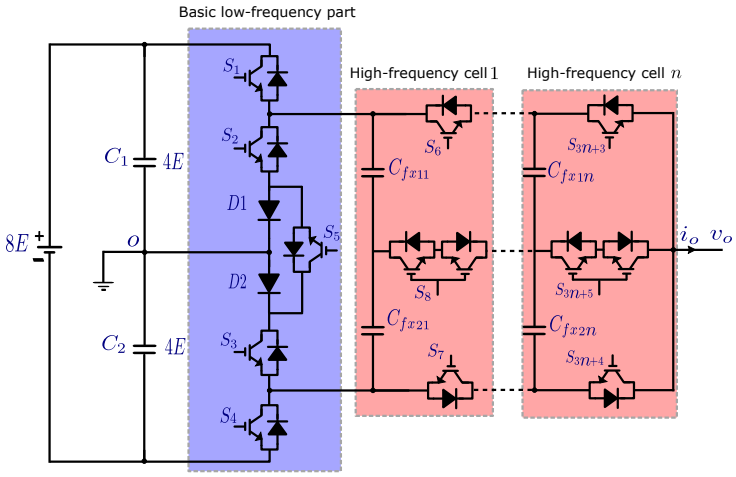


Figure 3.5: Generalized structure of the proposed topology for n-level operation.

shown in Fig. 3.5. For n extension units, the number of voltage levels N_{level}, active switches considering the four-quadrant switch as two switches N_{sw}, and FCs N_{FC} are determined as follows

$$N_{\text{level}} = 2^{n+2} + 1,\ N_{\text{sw}} = 4n + 5,\ N_{\text{FCs}} = 2n. \tag{3.2}$$

The voltage of the FCs in unit $i = \{1, 2, ..., n\}$ is given by

$$V_{fx1i} = V_{fx2i} = \frac{V_{\text{dc}}}{2^{i+2}}. \tag{3.3}$$

3.2.3 Conventional 5L-ANPC operating mode

One important feature of the proposed 9L-SC-ANPC inverter is the ability to cover the operation mode of the well-known 5L-ANPC without requiring any structural modification, which

enhances the functionality of the 9L-SC-ANPC inverter. Additionally, the proposed inverter can continuously operate with a lower number of levels (5L, 7L) even if there is a fault in the four-quadrant switch. In this case, the FCs are seen as one capacitor with a value half of C_{fx1} or C_{fx2}. The transition from 9L to 5L operation is achievable without a transient time because the auxiliary dc-link is still regulated to the same value, i.e. $\frac{V_{\text{dc}}}{4} = 2E$, and the produced levels are $\pm 4E$, $\pm 2E$, and 0. The 7L operation is also attainable with this topology, however, the auxiliary dc-link voltage should be changed to $V_{\text{dc}}/6$, which needs a set-point change and transient time for the FCs stabilization at the new reference voltage.

3.3 Modulation strategy for 9L-SC-ANPC inverter

3.3.1 FCs voltage balancing

The analysis of the charging and discharging process of FCs is first carried out in order to design an efficient balancing control. For the sake of simplification, Fig. 3.6 shows a typical staircase nine-level waveform with the charged/discharged FCs for each voltage level. As it can be observed, i_o flows through the auxiliary dc-link (one or two FCs) during the levels $\pm E$, $\pm 2E$, and $\pm 3E$. Assuming a quarter symmetry output voltage as shown in Fig. 3.6 and considering a positive output current i_o as in Fig. 3.2c, the charge variation ΔQ_{fx1} and ΔQ_{fx2} over a complete sinusoidal cycle of C_{fx1} and C_{fx2}, respectively, is expressed as

$$\left.\begin{aligned}\Delta Q_{fx1} &= \Delta Q_{fx1}^{2E} + \Delta Q_{fx1}^{3E} + \Delta Q_{fx1}^{-E} + \Delta Q_{fx1}^{-2E} \\ &= k_1 \textstyle\int_{\alpha_2}^{\alpha_3} i_o \,\mathrm{d}t + k_1 \int_{\pi-\alpha_3}^{\pi-\alpha_2} i_o \,\mathrm{d}t + \\ &\quad 2 \textstyle\int_{\alpha_3}^{\alpha_4} i_o \,\mathrm{d}t + 2 \int_{\pi+\alpha_1}^{\pi+\alpha_2} i_o \,\mathrm{d}t + \\ &\quad k_2 \textstyle\int_{\pi+\alpha_2}^{\pi+\alpha_3} i_o \,\mathrm{d}t + k_2 \int_{2\pi-\alpha_3}^{2\pi-\alpha_2} i_o \,\mathrm{d}t,\end{aligned}\right\} \tag{3.4}$$

and

$$\left.\begin{aligned}\Delta Q_{fx2} &= \Delta Q_{fx2}^{2E} + \Delta Q_{fx2}^{E} + \Delta Q_{fx2}^{-3E} + \Delta Q_{fx2}^{-2E} \\ &= k_1 \textstyle\int_{\alpha_2}^{\alpha_3} i_o \,\mathrm{d}t + k_1 \int_{\pi-\alpha_3}^{\pi-\alpha_2} i_o \,\mathrm{d}t - \\ &\quad 2 \textstyle\int_{\alpha_1}^{\alpha_2} i_o \,\mathrm{d}t - 2 \int_{\pi+\alpha_3}^{\pi+\alpha_4} i_o \,\mathrm{d}t + \\ &\quad k_2 \textstyle\int_{\pi+\alpha_2}^{\pi+\alpha_3} i_o \,\mathrm{d}t + k_2 \int_{2\pi-\alpha_3}^{2\pi-\alpha_2} i_o \,\mathrm{d}t,\end{aligned}\right\} \tag{3.5}$$

where k_1, $k_2 \in \{1, -1\}$ are introduced to identify the considered state for levels that have redundancies ($\pm 2E$), they are defined as

$$k_1 = \begin{cases} 1, \text{ if } V_3 \text{ is selected,} \\ -1, \text{ if } V_4 \text{ is selected,} \end{cases} \tag{3.6}$$

$$k_2 = \begin{cases} 1, \text{ if } V_9 \text{ is selected,} \\ -1, \text{ if } V_{10} \text{ is selected.} \end{cases} \tag{3.7}$$

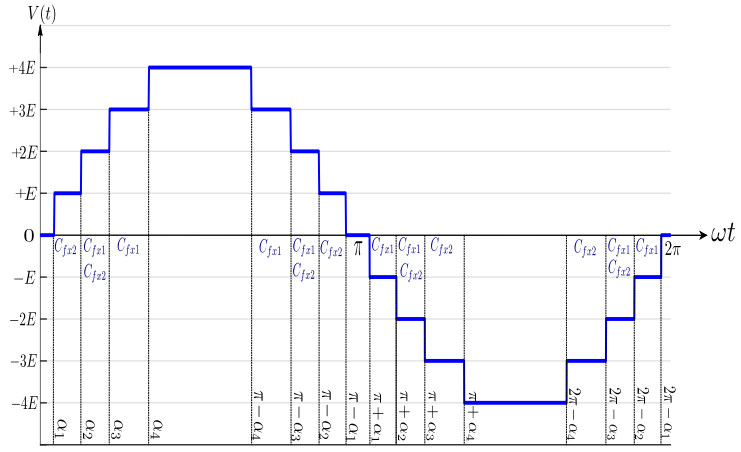


Figure 3.6: Typical staircase nine-level voltage with the charging/discharging capacitors.

From (3.4) and (3.5), it can be observed that the charge variations during $\pm 2E$ of C_{fx1} (ΔQ_{fx1}^{2E}, ΔQ_{fx1}^{-2E}) and C_{fx1} (ΔQ_{fx2}^{2E}, ΔQ_{fx2}^{-2E}) are identical. In addition, for a symmetric current i_o, one can conclude that

$$\left.\begin{aligned} \int_{\alpha_1}^{\alpha_2} i_o \, \mathrm{d}t &= -\int_{\pi+\alpha_1}^{\pi+\alpha_2} i_o \, \mathrm{d}t, \\ \int_{\alpha_3}^{\alpha_4} i_o \, \mathrm{d}t &= -\int_{\pi+\alpha_3}^{\pi+\alpha_4} i_o \, \mathrm{d}t. \end{aligned}\right\} \tag{3.8}$$

By comparing (3.4) and (3.5) while considering (3.8), it can be concluded that over an entire sinusoidal cycle, the charge variation of C_{fx1} and C_{fx2} is the same. Assuming unity PF for the sake of clarification, Fig. 3.7 shows the impact of each state on the FCs, charge difference $(\Delta Q_{fx1} - \Delta Q_{fx2})$ for each level, and the total charge variation for a complete cycle. It is clear that the total charge difference $(\Delta Q_{fx1} - \Delta Q_{fx2})$ over a complete cycle is 0. Also, the figure depicts the evolution of the auxiliary dc-link voltage V_{fx} during the fundamental cycle, where there are four cases according to the values of k_1 and k_2. Accordingly, V_{fx1} and V_{fx2} can be regulated by controlling the auxiliary dc-link voltage V_{fx} because C_{fx1} and C_{fx2} can be inherently balanced. For fixed modulation index, (i.e. fixed α_1, α_2, α_3, and α_4), the FCs charge can be adjusted by k_1 and k_2 based on the selected states according to (3.6) and (3.7).

As mentioned earlier and illustrated in Table 3.1, redundant switching states are available for levels $\pm 2E$ and 0. The zero-level redundant states have no effect on the charging/discharging process of the FCs and thus are used to reduce the current stress of switch S_5 as described later Section 3.3.3. While the redundant states of $\pm 2E$ have an opposite impact on the FCs, they are, therefore, exploited to achieve voltage balancing of the FCs. After sensing V_{fx} and based on the sign of i_o, the appropriate switching states of $\pm 2E$ are identified. Taking $+2E$ as an example, when V_{fx} is lower than its reference ($2E$), V_3 is selected for a positive i_o and V_4 is selected for a negative i_o to charge the auxiliary dc-link. The same concept is applied for $-2E$. To determine the proper switching redundant states, the deviation of V_{fx} from its reference V_{fx}^* is calculated as

$$\Delta V_{fx} = V_{fx}^* - V_{fx}. \tag{3.9}$$

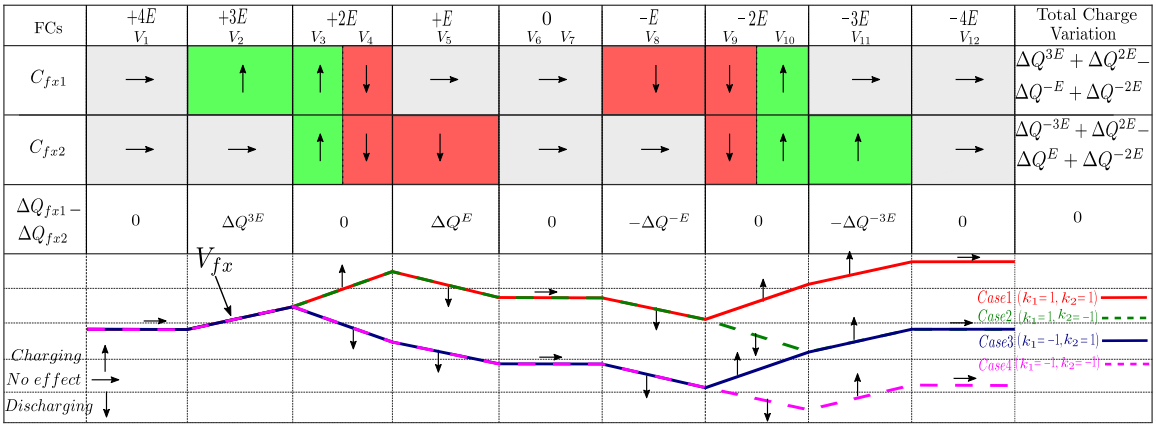


Figure 3.7: Charge variation of C_{fx1} and C_{fx1} over a complete sinusoidal cycle.

A Boolean function $f(y)$ is introduced and defined as

$$f(y)=\begin{cases}1, & \text{if } y\geq 0\\ 0, & \text{if } y<0.\end{cases} \tag{3.10}$$

Considering (3.10), ΔV_{fx} and i_o can be expressed as

$$f(\Delta V_{fx})=\begin{cases}1, & \text{if } \Delta V_{fx}\geq 0\\ 0, & \text{if } \Delta V_{fx}<0,\end{cases} \tag{3.11}$$

and

$$f(i_o)=\begin{cases}1, & \text{if } i_o\geq 0\\ 0, & \text{if } i_o<0.\end{cases} \tag{3.12}$$

Based on (3.11) and (3.12), the proper states of $+2E$ and $-2E$ are given as

$$\left.\begin{aligned}V_{2E}&=V_4[f(\Delta V_{fx})\oplus f(i_o)]+V_3[f(\Delta V_{fx})\odot f(i_o)],\\ V_{-2E}&=V_{10}[f(\Delta V_{fx})\oplus f(i_o)]+V_9[f(\Delta V_{fx})\odot f(i_o)].\end{aligned}\right\} \tag{3.13}$$

where $\oplus$ and $\odot$ refer to the XOR and XNOR logic operations, respectively. The Boolean output of $\oplus$ is true (1) only when an odd number of inputs are true, while the Boolean output of $\odot$ is true only when an even number of inputs are true.

3.3.2 NP Balancing

Although NP balancing of ANPC-based topologies is easier to be realized compared to NPC topologies, it is considered an essential issue in the design of the control system. Inspired by the approach proposed in [165] for the 5L-ANPC converter, an effective NP balancing method is developed for the proposed 9L-SC-ANPC inverter. The designed NP potential control can be used for FC-based reduced-switch MLIs when the redundant states are insufficient to achieve both FCs and dc-Link balancing.

Figure 3.8 illustrates the power flow of the 9L-SC-ANPC inverter for a complete sinusoidal cycle. During the positive half-cycle, the load is supplied by the upper capacitor C_1 of the main dc-link and the auxiliary dc-link (FCs). Similarly, C_2 and FCs supply the load during the negative half-cycle. For a symmetric i_o, The power flow must fulfil

$$P_1 + P_{fxp} = P_2 + P_{fxn}, \tag{3.14}$$

where P_1 and P_2 are the power supplied to the load by C_1 in the positive half-cycle and C_2 in the negative half-cycle, respectively. P_{fxp} and P_{fxn} are the powers provided by FCs during positive and negative half-cycle, respectively. For single-phase operation, the total power P_{c1} provided by C_1 and P_{c2} by C_2 can be expressed as

$$P_{c1} = P_1 + P_{1fx} \text{ and } P_{c2} = P_2 + P_{2fx}, \tag{3.15}$$

where P_{1fx} and P_{2fx} are the powers supplied to the FCs by C_1 and C_2, respectively. As can be concluded from (3.15), the total power provided by C_1 and C_2 can be controlled by regulating the power delivered to the FCs. This can be realized by adjusting the reference value V_{fx}^* of the FCs. Hence, NP balancing can be achieved. For illustration, when $V_{c1} > V_{c2}$, V_{fx}^* should be increased in the positive half cycle to draw more energy from C_1 and decreased in the negative half-cycle to reduce the amount of energy given by C_2. As a result, the energy provided by C_1 will be more than that provided by C_2, which leads to a decrease in V_{c1} and an increase in V_{c2}. Similarly, when $V_{c1} < V_{c2}$, V_{fx}^* is decreased in the positive half cycle and increased in the negative one. Thus, less power will be provided by C_1 and more will be provided by C_2. Based on this concept, V_{fx}^* is calculated every half-cycle according to V_{c1} and V_{c2} as follows:

$$\left.\begin{aligned} V_{fx,P}^* &= 2E + k(4E - V_{c2}), \\ V_{fx,N}^* &= 2E + k(4E - V_{c1}), \end{aligned}\right\} \tag{3.16}$$

where $V_{fx,P}^*$ and $V_{fx,N}^*$ are the FCs references in the positive and negative half-cycle, respectively. k is a weighting factor to adjust the two control objectives (FCs and NP balancing) and is determined by trial and error. It is commonly in the range from 0 to 1. The higher the k-value, the higher the NP balancing priority over FCs control and vice versa.

3.3.3 Selection of zero-level redundancy states

As mentioned before, the redundant zero-level states V_6 and V_7 have no effect on the FCs and thus cannot be taken into account in the voltage balancing scheme. By observing the current path of the states V_6 and V_7 in Fig. 3.3(f) and (g), one can notice that for V_6, i_o passes through two active switches S_3 and S_7 and diode D_2 when i_o is positive. While there are three active switches S_3, S_5 and S_7 and diode D_1 in the current path when i_o is negative. For V_7, and in contrast to V_6, there are three switches S_2, S_5 and S_6 and diode D_2 in the current path for positive i_o, compared to two switches S_2 and S_6 and diode D_1 for negative i_o. Accordingly, to reduce conduction losses, V_6 should be selected for positive i_o and V_7 for the negative i_o. By doing so, no current passes through S_5 for the zero-level states. For other levels, S_5 carries current only when reactive power is required and the conduction period is limited only by the reactive power period. Which means that for unity power factor (PF), S_5 is not required and for

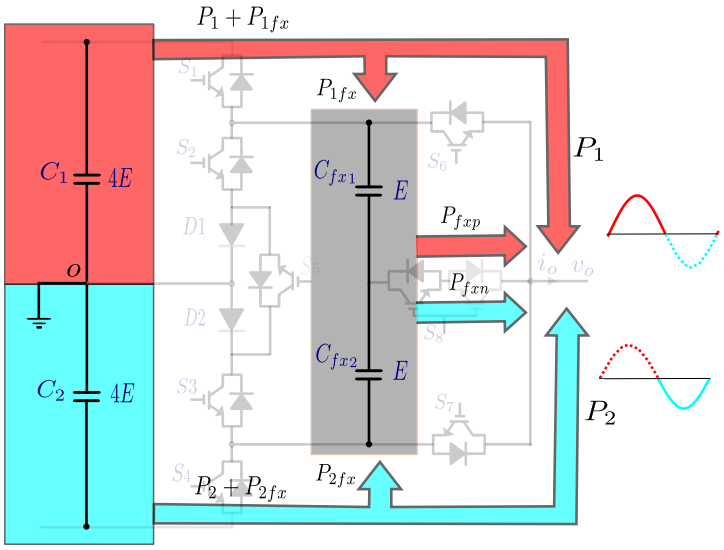


Figure 3.8: Power flow interaction during a complete sinusoidal cycle of the proposed 9L-SC-ANPC inverter.

reactive power operation, a low current-rated switch can be used. It is worth mentioning that, no current flows through the body diode of S_5 under all operating conditions. The flowchart of the FCs and NP balancing control scheme and the zero-level state's selection for the proposed 9L-SC-ANPC inverter is shown in Fig. 3.9. The implementation is integrated into a PD-PWM technique as described in the following subsection.

3.3.4 PD-PWM Design for 9L-SC-ANPC inverter

Among the different modulation schemes, the PD-PWM technique is considered in this work due to its better harmonic profile for single-phase applications [166]. Fig. 3.10 illustrates the PWM waveforms of the 9L-SC-ANPC inverter. A reactive power operation is considered to investigate the proposed control under different operating conditions, which distinctly cover unity PF operation. By comparing nine in-phase carrier signals with a reference sinusoidal waveform, the level region can be identified. The proper switching state for each level is selected according to the proposed control approach as illustrated in Fig. 3.9. Based on the polarity of the modulation signal and i_o, the sinusoidal cycle can be divided into four regions as shown in Fig. 3.10, two reactive regions and two active regions.

Region 1 $(R1)$ ***from*** 0 ***to*** t_1

In this region, the modulation signal is positive and i_o is negative, so the inverter is supplying reactive power. Based on the modulation signal and carriers, v_o is varying between 0 and $+E$. For zero-level, V_7 is selected to reduce the conducting switches in the current path because i_o is negative. For $+E$, V_5 is selected as there is no redundancy available for this level.

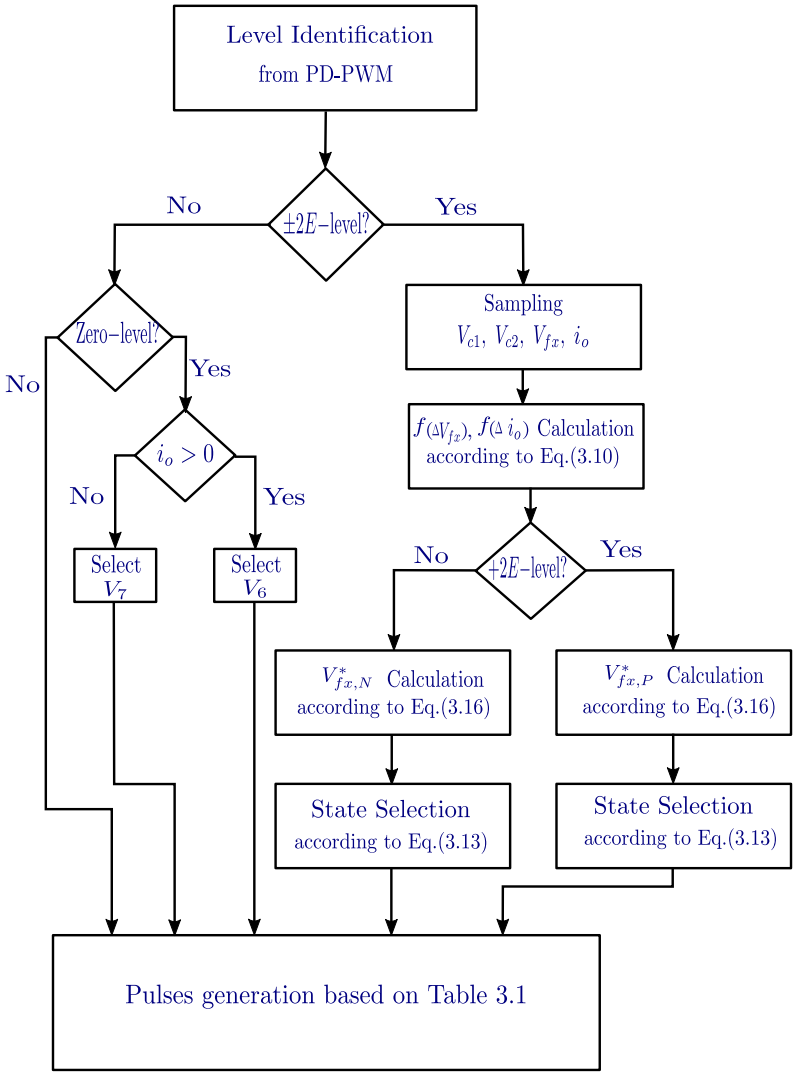


Figure 3.9: Flowchart of the designed balancing algorithm for the 9L-SC-ANPC inverter.

Region 2 $(R2)$ ***from*** t_1 ***to*** $\frac{\pi}{\omega}$

In this region , the inverter is supplying active power as the modulation waveform and i_o are positive. v_o is varying between 0, $+E$, $+2E$, $+3E$, and $+4E$ based on the intersection zone of the modulation and carrier signals as shown in Fig. 3.10. For the zero-level, V_6 is chosen in this region as i_o is positive. For $+2E$, V_3 or V_4 is selected based on the balancing algorithm. For $+E$, $+3E$, and $+4E$, states V_5, V_2, and V_1 are considered, respectively.

Region 3 $(R3)$ ***from*** $\frac{\pi}{\omega}$ ***to*** t_8

The inverter is providing reactive power in this region as the modulation signal is negative and i_o is positive. v_o is varying between 0 and $-E$. For the zero-level, V_6 is selected; while, for $-E$, V_8 is chosen.

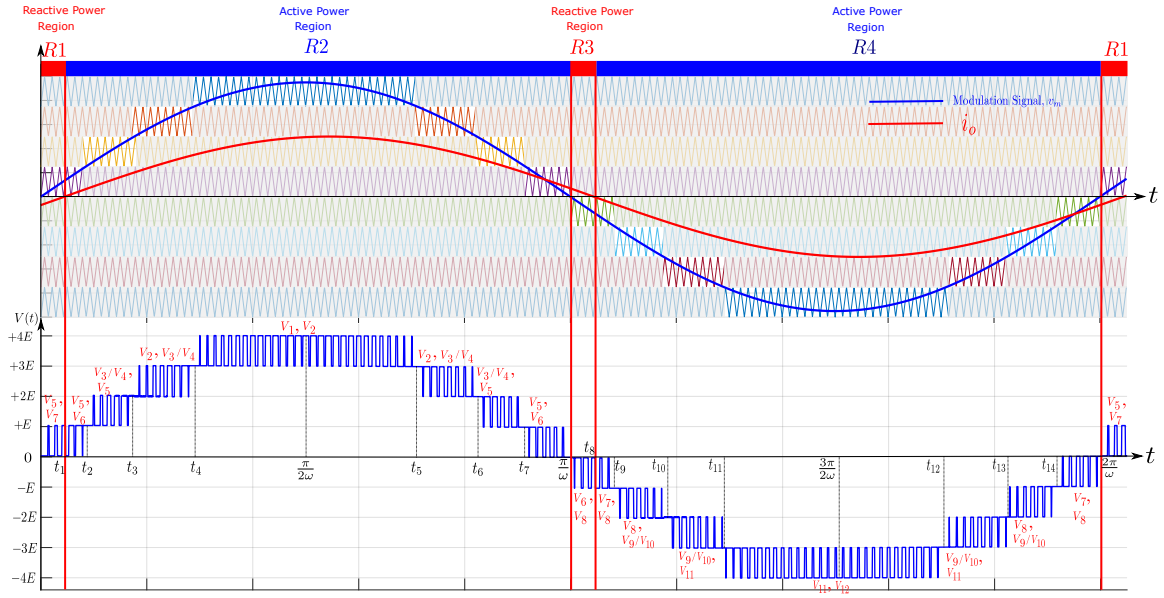


Figure 3.10: PD-PWM strategy for the proposed 9L-SC-ANPC inverter.

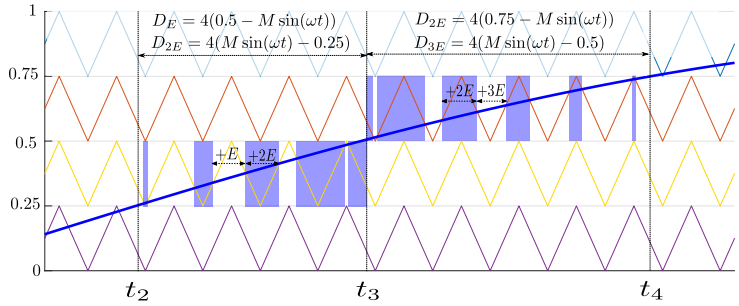


Figure 3.11: +2E-level generation by PD-PWM strategy.

Region 4 $(R4)$ ***from*** t_8 ***to*** $\frac{2\pi}{\omega}$

Both the modulation signal and i_o are negative in this region, so the 9L-SC-ANPC inverter is delivering active power. The inverter is generating 0, $-E$, $-2E$, $-3E$, and $-4E$ according to the comparison with the carrier signals. V_7 is chosen for the zero-level as i_o is negative. V_8, V_{11}, and V_{12} are applied for $-E$, $-3E$, and $-4E$, respectively. While for $-2E$, the switching state V_9 or V_{10} is selected according to the FCs and NP balancing algorithm.

3.4 FCs values selection and modulation index limitations

3.4.1 FCs values selection

An important aspect of FC-based MLIs is the selection of proper FC values to limit the voltage ripple V_r to an acceptable range. For the proposed 9L-SC-ANPC inverter with its developed PD-PWM-based modulation strategy, the FCs values are determined as a function of the desired voltage ripple assuming that the output voltage and current are sinusoidal waveforms. Taking

Table 3.2: Duty cycles of levels during positive-half cycle for PD-PWM.

Period	Duty Cycle
$t_0 \rightarrow t_2$	$D_0 = 4(0.25 - M \cdot \sin(\omega t))$
$(0 \rightarrow \frac{1}{\omega} \cdot \arcsin \frac{1}{4M})$	$D_E = 4M \cdot \sin(\omega t)$
$t_2 \rightarrow t_3$	$D_E = 4(0.5 - M \cdot \sin(\omega t))$
$(\frac{1}{\omega} \cdot \arcsin \frac{1}{4M} \rightarrow \frac{1}{\omega} \cdot \arcsin \frac{1}{2M})$	$D_{2E} = 4(M \cdot \sin(\omega t) - 0.25)$
$t_3 \rightarrow t_4$	$D_{2E} = 4(0.75 - M \cdot \sin(\omega t))$
$(\frac{1}{\omega} \cdot \arcsin \frac{1}{2M} \rightarrow \frac{1}{\omega} \cdot \arcsin \frac{3}{4M})$	$D_{2E} = 4(M \cdot \sin(\omega t) - 0.5)$
$t_4 \rightarrow \frac{\pi}{2\omega}$	$D_{3E} = 4(1 - M \cdot \sin(\omega t))$
$(\frac{1}{\omega} \cdot \arcsin \frac{3}{4M} \rightarrow \frac{\pi}{2\omega})$	$D_{4E} = 4(M \cdot \sin(\omega t) - 0.75)$

this assumption into account, the charge variation during a time period from t_a to t_b can be written as

$$\Delta Q = \int_{t_a}^{t_b} i_o \, \mathrm{d}t = \frac{V_{\mathrm{dc}}}{2|Z|} \int_{t_a}^{t_b} M \cdot \sin(\omega t + \phi) \, \mathrm{d}t, \tag{3.17}$$

where $|Z|$ is the value of the load impedance and ϕ is the power factor angle. Based on the operation of the 9L-SC-ANPC inverter, the ΔQ_{fx1} over an entire sinusoidal cycle is obtained by (3.4). To calculate ΔQ_{fx1}^{2E}, it is required to determine the active time of the level $+2E$ during its generation period. As shown in Fig. 3.10, $+2E$ is produced in periods from t_2 to t_3 and t_3 to t_4. The generation of $+2E$ is acting as an ascending sinusoidal function in the first period and descending function through the second, see Fig.3.11. Consequently, the duty cycle D_{2E} of $+2E$ during its generation period can be calculated as

$$D_{2E} = \begin{cases} 4(M \cdot \sin(\omega t) - 0.25), & \text{for } t_2 \leq t \leq t_3, \\ 4(0.75 - M \cdot \sin(\omega t)), & \text{for } t_3 \leq t \leq t_4. \end{cases} \tag{3.18}$$

Similarly, the duty cycles of the voltage levels during the positive half-cycle are given in Table 3.2. Accordingly and based on (3.17), ΔQ_{fx1}^{2E} can be calculated as

$$\begin{aligned} \Delta Q_{fx1}^{2E} = \tfrac{V_{\mathrm{dc}}}{2|Z|} \big[& k_1 \textstyle\int_{t_2}^{t_3} 4(M \cdot \sin(\omega t) - 0.25)(M \cdot \sin(\omega t + \phi)) \, \mathrm{d}t + \\ & k_1 \textstyle\int_{t_3}^{t_4} 4(0.75 - M \cdot \sin(\omega t))(M \cdot \sin(\omega t + \phi)) \, \mathrm{d}t + \\ & k_1 \textstyle\int_{t_5}^{t_6} 4(0.75 - M \cdot \sin(\omega t))(M \cdot \sin(\omega t + \phi)) \, \mathrm{d}t + \\ & k_1 \textstyle\int_{t_6}^{t_7} 4(M \cdot \sin(\omega t) - 0.25)(M \cdot \sin(\omega t + \phi)) \, \mathrm{d}t \big]. \end{aligned} \tag{3.19}$$

Similarly, the charge variation of level $+3E$ and $-E$ are given as follows:

$$\begin{aligned} \Delta Q_{fx1}^{3E} = \tfrac{V_{\mathrm{dc}}}{2|Z|} \big[& 2 \textstyle\int_{t_3}^{t_4} 4(M \cdot \sin(\omega t) - 0.5)(M \cdot \sin(\omega t + \phi)) \, \mathrm{d}t \\ & + 2 \textstyle\int_{t_4}^{\frac{\pi}{2\omega}} 4(1 - M \cdot \sin(\omega t))(M \cdot \sin(\omega t + \phi)) \, \mathrm{d}t \big], \end{aligned} \tag{3.20}$$

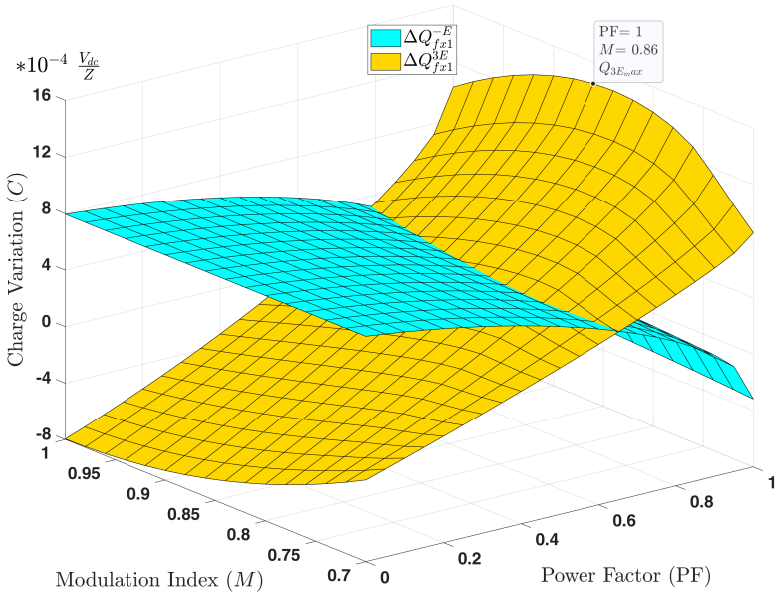


Figure 3.12: C_{fx1} charge during levels $-E$ and $+3E$.

and

$$\Delta Q_{fx1}^{-E} = \frac{V_{\text{dc}}}{2|Z|}\Big[2\int_{\frac{\pi}{\omega}}^{t_9}(-4M\cdot\sin(\omega t))(M\cdot\sin(\omega t+\phi))\,\mathrm{d}t+ \\ 2\int_{t_9}^{t_{10}}4(0.5+M\cdot\sin(\omega t))(M\cdot\sin(\omega t+\phi))\,\mathrm{d}t\Big]. \tag{3.21}$$

Basically, the minimum capacitance for a given V_r is determined based on the maximum change in charge of the capacitor. Back to (3.19), ΔQ_{fx1}^{2E} and ΔQ_{fx1}^{-2E} can be balanced (or minimized) by adjusting k_1 and k_2 for every switching instant T_s. whereas ΔQ_{fx1}^{3E} and ΔQ_{fx1}^{-E} have no redundancies and their values depend on M and PF. To investigate their values and find out which one has a greater value to be considered for the capacitor design, Fig. 3.12 shows ΔQ_{fx1}^{3E} and ΔQ_{fx1}^{-E} as a function of M and PF according to. (3.20) and. (3.21) at $\omega = 100\pi$. Note that the time limits of the integrals are given in Table 3.2.

It can be seen from Fig. 3.12 that $\Delta Q_{fx1}^{3E} > \Delta Q_{fx1}^{-E}$ for high PF values and vice versa for low PF. Also, ΔQ_{fx1}^{-E} reaches its maximum at $M = 1$ and PF = 0, while ΔQ_{fx1}^{3E} has a maximum value at $M = 0.86$ and PF = 1. Since $\max(\Delta Q_{fx1}^{3E}) > \max(\Delta Q_{fx1}^{-E})$, ΔQ_{fx1}^{3E} is considered for capacitance selection.

The total charge variation $\Delta Q_{fx1}^{t\_3E}$ during the period of $+3E$ from t_3 to $\pi/2$ is given as

$$\Delta Q_{fx1}^{t\_3E} = \frac{V_{\text{dc}}}{2|Z|}\Big[2\int_{t_3}^{t_4}4(M\cdot\sin(\omega t)-0.5)(M\cdot\sin(\omega t+\phi))\,\mathrm{d}t+ \\ 2\int_{t_4}^{\frac{\pi}{2\omega}}4(1-M\cdot\sin(\omega t))(M\cdot\sin(\omega t+\phi))\,\mathrm{d}t+ \\ k_1\int_{t_3}^{t_4}4(0.75-M\cdot\sin(\omega t))(M\cdot\sin(\omega t+\phi))\,\mathrm{d}t+ \\ k_1\int_{t_5}^{t_6}4(0.75-M\cdot\sin(\omega t))(M\cdot\sin(\omega t+\phi))\,\mathrm{d}t\Big]. \tag{3.22}$$

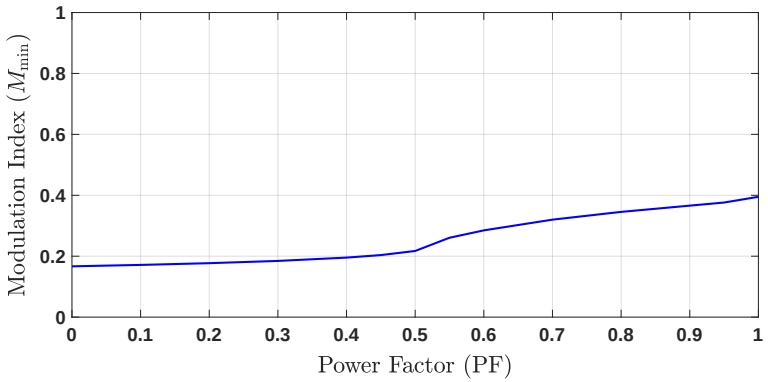


Figure 3.13: Variation of $M_{\min}$ versus PF

The amount of charge resulted from $+2E$ (t_3 to t_4 and t_5 to t_6) in. (3.22) is supposed to reduce $\Delta Q_{fx1}^{t\_3E}$ by exploiting the redundancy state available for $+2E$, therefore, k_1 is set to -1. To find $\max(\Delta Q_{fx1}^{t\_3E})$, M and PF are set to 0.86 and 1 in (3.22), which yields

$$\max(\Delta Q_{fx1}^{t\_3E}) = 0.336\frac{V_{\text{dc}}}{\omega \cdot |Z|}. \tag{3.23}$$

Consequently, the capacitance value is finally given by

$$C_{fx1} = C_{fx2} \approx \frac{\max(\Delta Q_{fx1}^{t\_3E})}{V_r} = 0.336\frac{V_{\text{dc}}}{\omega \cdot |Z| \cdot V_r}. \tag{3.24}$$

As a function of the peak current value I_p as, (3.24) can be written as

$$C_{fx1} = C_{fx2} = 0.672\frac{I_p}{\omega \cdot V_r}. \tag{3.25}$$

3.4.2 Modulation index limitations

From FCs balancing point of view, the operation of 9L-SC-ANPC inverter should generate $\pm 2E$ for a period of time at least that ensures the balance of the FCs. To generate $\pm 2E$, M must be greater than 0.25, as shown in Fig. 3.10. To determine the minimum modulation index $M_{\min}$ for FC balancing, the inverter is assumed to be operated at $0.25 < M < 0.5$. Presuming a quarter-symmetry waveform, the change of the total charge Q_t of the auxiliary DC link is expressed as

$$\begin{aligned}\Delta Q_t = \tfrac{V_{\text{dc}}}{2|Z|}\big[\textstyle\int_0^{t_2}(4M \cdot \sin(\omega t))(M \cdot \sin(\omega t + \phi))\, \mathrm{d}t + \\ \textstyle\int_{t_2}^{\frac{\pi}{2\omega}} 4(0.5 - M \cdot \sin(\omega t))(M \cdot \sin(\omega t + \phi))\, \mathrm{d}t + \\ 2k_1 \textstyle\int_{t_2}^{\frac{\pi}{2\omega}} 4(M \cdot \sin(\omega t) - 0.25)(M \cdot \sin(\omega t + \phi))\, \mathrm{d}t\big].\end{aligned} \tag{3.26}$$

Note that the charge resulted from $\pm 2E$ is multiplied by 2 as i_o passes through the two FCs during these levels while for $\pm E$, i_o flows only through one FC. To find $M_{\min}$, the amount of

charge resulted from $\pm E$ has to be equal to that resulted from $\pm 2E$ irrespective of the polarity as the polarity can be adjusted by using the redundancies of $\pm 2E$ ($k_1 \in \{1, -1\}$). In doing so, (3.26) is rewritten as

$$\begin{aligned} &\Big| \textstyle\int_{t_0}^{t_2} (4M_{\text{min}} \cdot \sin(\omega t))(M_{\text{min}} \cdot \sin(\omega t + \phi))\, \mathrm{d}t + \\ &\textstyle\int_{t_2}^{\frac{\pi}{2\omega}} 4(0.5 - M_{\text{min}} \cdot \sin(\omega t))(M_{\text{min}} \cdot \sin(\omega t + \phi))\, \mathrm{d}t \Big| = \\ &\Big| 2 \textstyle\int_{t_2}^{\frac{\pi}{2\omega}} 4(M_{\text{min}} \cdot \sin(\omega t) - 0.25)(M_{\text{min}} \cdot \sin(\omega t + \phi))\, \mathrm{d}t \Big|. \end{aligned} \tag{3.27}$$

By solving (3.27) at different values of PF, M_{min} can be calculated, as shown in Fig. 3.13. It can be seen that the maximum value of M_{min} is 0.395 at PF = 1. This limitation does not have a negative effect on the usability of the inverter, as the proposed inverter is targeted to be a potential candidate for renewable energy grid-connected applications, which typically operate at $M > 0.5$. In addition, an effective solution is proposed in the next chapter to enable converter operation at lower modulation indices, as presented in Section 4.3.

3.5 Power loss analysis

The proposed 9L-SC-ANPC is modeled in PLECS to evaluate the power losses and efficiency under various operating conditions. A 10-kW single-phase system is considered in the analysis with $V_{\text{dc}} = 1$ kV and $f_c = 2$ kHz. A 40-A sinusoidal current source is connected to the inverter as a load. The FF50R12RT4 IGBT and IDP30E65D1 diode switching devices produced by Infineon are employed in the inverter model. The same switching devices are also utilized in the experimental validation. The thermal models of these components are provided by the manufacturer. Fig. 3.14 shows the distribution of the power losses for four operating conditions ($M = 1$ and PF = 1, $M = 1$ and PF = 0.5, $M = 0.5$ and PF = 1, and $M = 0.5$ and PF = 0.5), as the total losses are mainly attributed to the switching and conduction losses [60]. It is clear that the total losses for the four cases are dominated by the conduction losses of the switches. It should be mentioned that S_8^1 and S_8^2 refer to the two power devices of the four-quadrant switch S_8 and have the same loss value for all conditions. Furthermore, thanks to the proposed modulation algorithm (Section 3.3.3), S_5 has no power loss for unity PF operation and has a low value for reactive power operation, which improves the inverter efficiency. From the loss analysis, the efficiency of the 9L-SC-ANPC at $M = 1$ and PF = 1 is 98.99%. The temperature profiles of the switches are obtained by the thermal analysis of the 9L-SC-ANPC inverter in PLECS environment. The results at PF = 1 and $M = 1$ are shown in Fig. 3.15 and are consistent with loss distribution in Fig 3.14.

3.6 Simulation verification

MATLAB/Simulink is used to verify the effectiveness of the proposed 9L-SC-ANPC inverter with the developed PD-PWM strategy. The parameters used in the simulation model are given in Table 3.3.

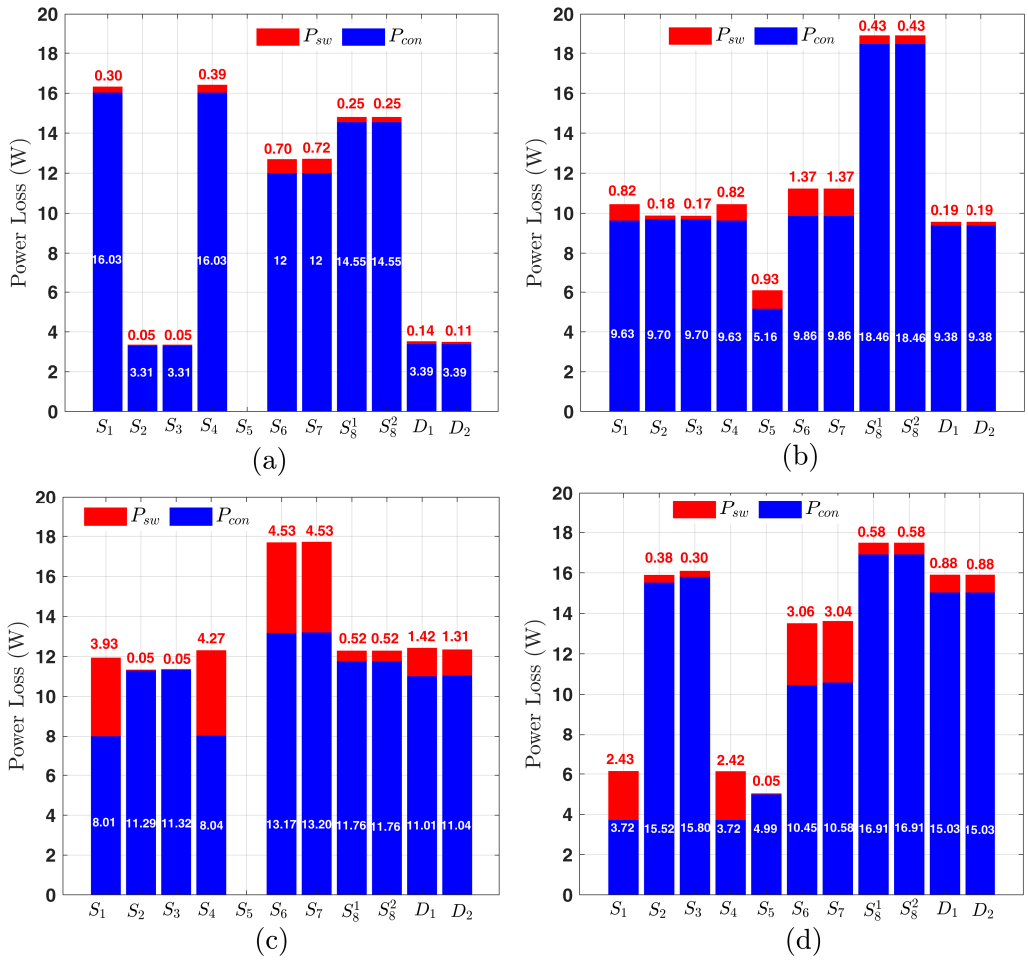


Figure 3.14: Conduction and switching losses of the 9L-SC-ANPC inverter: (a) $M = 1$, PF = 1. (b) $M = 1$, PF = 0.5. (c) $M = 0.5$, PF = 1. (d) $M = 0.5$, PF = 0.5.

Table 3.3: Experimental setup details of the 9L-SC-ANPC inverter.

Parameter	Simulation	Experimental
Input DC source, V_{dc}	400 V	400 V
Line frequency, f_{line}	50 Hz	50 Hz
Carrier frequency, f_c	2 kHz	2 kHz
dc-link capacitors, C_1 and C_2	3300 μF	3300 μF
FCs, C_{fx1} and C_{fx2}	4000 μF	4000 μF

Figure 3.16 shows the steady-state simulation results of v_o, i_o, i_{S5}, V_{c1}, V_{c2}, V_{fx}, V_{fx1}, and V_{fx2} for $Z = 16.9\angle 27.5°\Omega$. It is clear that v_o has nine levels in the sinusoidal cycle, and the dc-link capacitors and FCs are balanced at their references. Thanks to the proper selection of zero-level redundancies, no current flows in S_5 during the zero-level generation, resulting in a low current stress of the switch as clear in the result and reducing the total losses of the inverter. To verify the effectiveness of the FCs balancing method with only one sensor, a mismatch of 10% was made in the FCs ($C_{fx1} = 1.1C_{fx2}$) with different initial voltages by setting C_{fx1} and

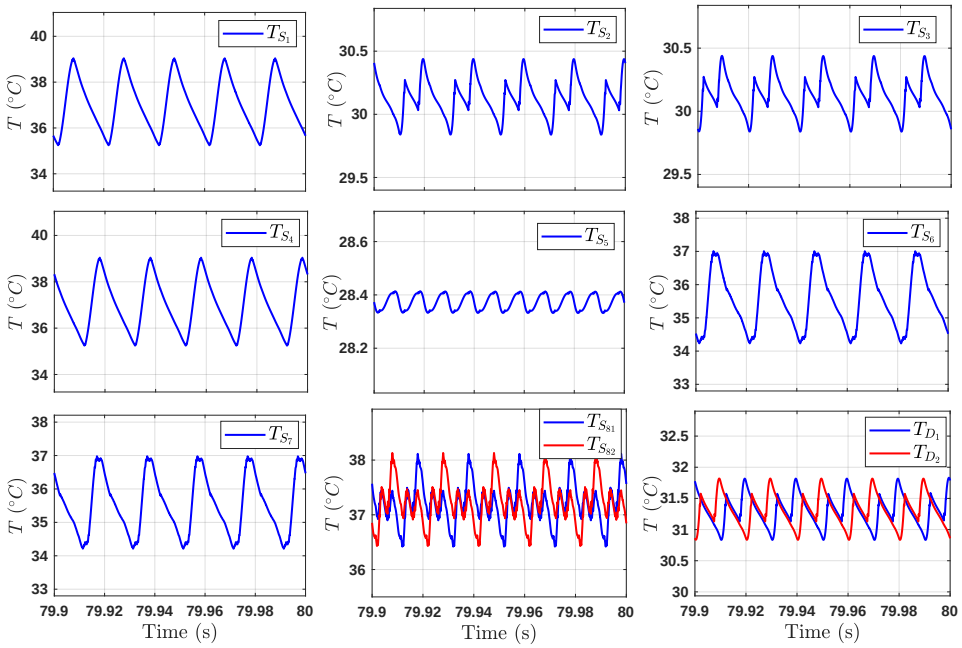


Figure 3.15: Simulated thermal profiles of the power devices with PLECS.

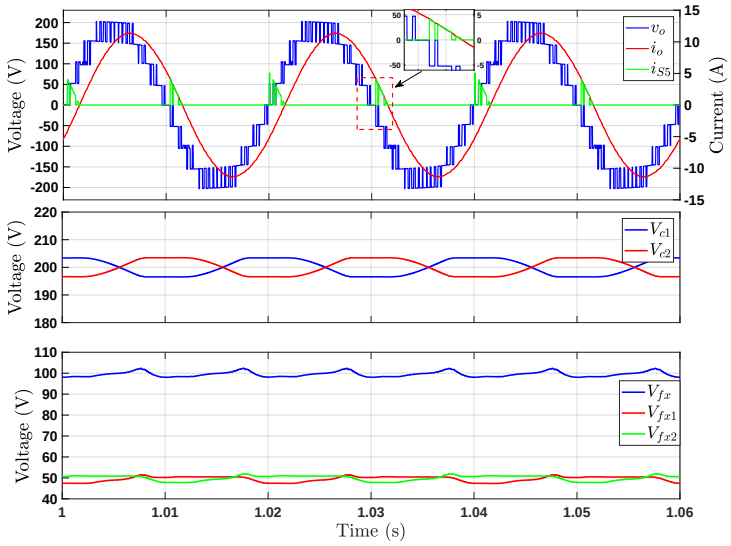


Figure 3.16: Simulation results of the 9L-SC-ANPC inverter for an RL load (PF = 0.89) at steady-state (from top): output voltage, current and current of S_5, voltages of dc-link Capacitors, and FCs voltages.

C_{fx2} to 40 V and 60 V, respectively. Fig. 3.17 shows the simulation results for this case, which prove the ability of the designed balancing method to stabilize the FCs with only one sensor.

The operation of the proposed topology with higher levels is also verified by simulation studies. According to Fig. 3.5, two high-frequency cells $N = 2$ is considered to generate a 17-level output voltage. The number of required components and sustained voltages of the FCs

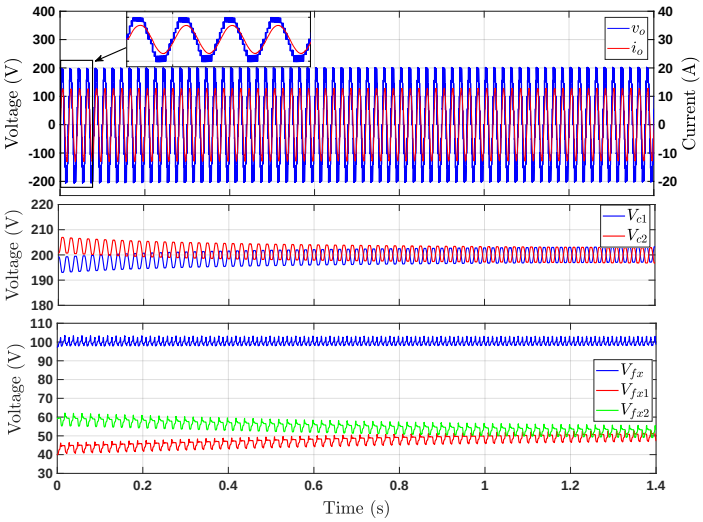


Figure 3.17: Simulation results of the 9L-SC-ANPC inverter at different initial voltages of FCs and 10% mismatch in the capacitors values ($C_{fx1} = 1.1C_{fx2}$) for an RL load (PF = 0.89) (from top): output voltage and current, voltages of dc-link Capacitors, and FCs voltages.

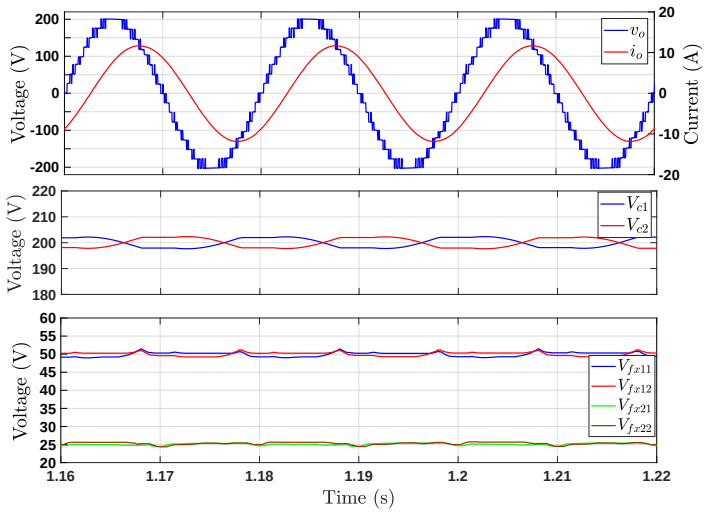


Figure 3.18: Simulation results of the 17L-SC-ANPC inverter at steady-state (from top): output voltage and current, voltages of dc-link Capacitors, and FCs voltages.

are given by (3.2) and (3.3). Fig. 3.18 shows the steady-state simulation results of the 17L-SC-ANPC inverter. As it is clear, v_o has 17 levels in the waveform, and the dc-link capacitors are kept balanced at $V_{\text{dc}}/2$. The voltages of the FCs are stabilized at their reference according to (3.3).

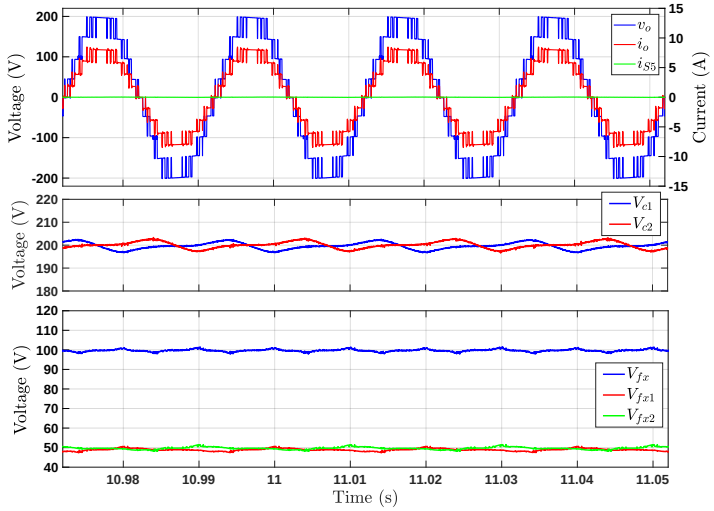


Figure 3.19: Experimental results of the 9L-SC-ANPC inverter for a resistive load (PF = 1) at steady-state (from top): output voltage, current and current of S_5, voltages of dc-link Capacitors, and FCs voltages.

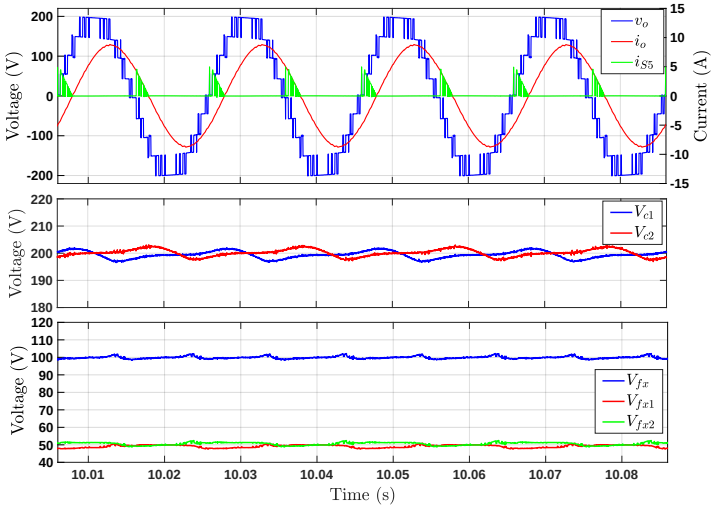


Figure 3.20: Experimental results of the 9L-SC-ANPC inverter for an RL load (PF = 0.89) at steady-state (from top): output voltage, current and current of S_5, voltages of dc-link Capacitors, and FCs voltages.

3.7 Experimental validation

The validation of the proposed inverter with its developed modulation strategy has also been verified on the experimental platform. The details of the experimental setup are given in Appendix B. A dead time of 2 μs is provided by the built-in FPGA in the dSpace Microlabbox. The measured data are plotted in MATLAB after being exported from the dSPACE by controlDesk software. The quality of the figures of this method is higher than that of DSO.

Figure 3.19 shows the steady-state experimental waveforms of v_o, i_o, i_{S5}, V_{c1}, V_{c2}, V_{fx}, V_{fx1}, and V_{fx2} for a resistive load, $Z = 25\angle 0°\Omega$. Nine levels are produced in the output voltage,

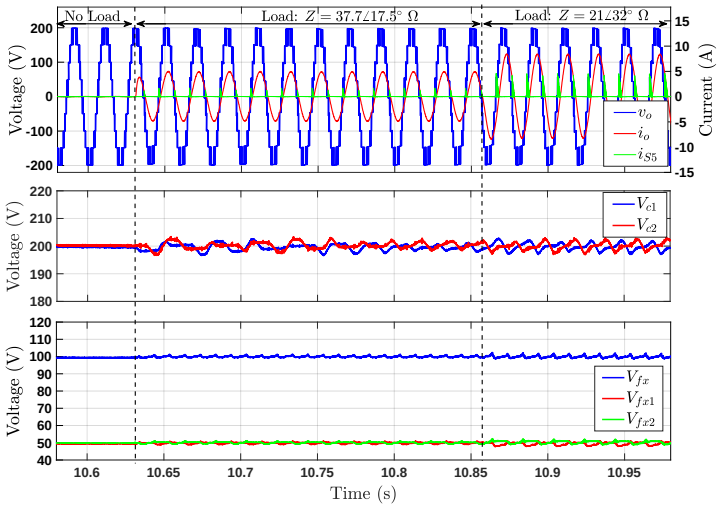


Figure 3.21: Experimental results of the 9L-SC-ANPC inverter for step changes in the load (from top): output voltage, voltages of dc-link Capacitors, and FCs voltages.

resulting in high quality waveforms of the voltage and current. No current flows through S_5 for unity PF operation as shown in Fig. 3.19 and theoretically proven. The dc-link capacitors V_{c1} and V_{c2} are balanced at their reference value $V_{\text{dc}}/2$ with the proposed balancing algorithm. The FC voltages are maintained at their reference $V_{\text{dc}}/8$ with low ripple values and with only one sensor, which is consistent with the theoretical analysis and verifies the effectiveness of the proposed algorithms. The inverter steady-state operation under reactive power operation at PF = 0.89 is shown in Fig. 3.20, $Z = 25\angle 27.5^\circ\Omega$. The dc-link and FCs are balanced, achieving low ripple values. Due to the high-quality waveforms, the THD of v_o is 12.96%, which can be filtered with a small filter. Moreover, the THD of i_o has a very low value of 0.93%. Fig. 3.21 shows the performance of the inverter for step-changes in the load from no load to $Z = 37.7\angle 17.5^\circ\Omega$ and then to $Z = 21\angle 32^\circ\Omega$. It can be seen that the dc-link capacitors are maintained at $V_{\text{dc}}/2$ for all cases with acceptable ripple values. Moreover, the FCs are still stabilized at their references showing a strong balancing performance with only one sensor despite the abrupt changes in the load.

To experimentally investigate the effect of modulation index variation on the output waveforms and the FCs balancing, the performance of the 9L-SC-ANPC inverter is tested under different values of M (0.6, 0.86, and 1). The results are given in Fig. 3.22 for a resistive load $Z = 25\angle 0^\circ\Omega$ and in Fig. 3.23 for a resistive inductive load $Z = 25\angle 27.5^\circ\Omega$. For all cases, the designed PD-PWM with the integrated balancing algorithm shows a good capability in balancing the dc-link and FCs while regulating the output voltage/current. It can be also observed that the ripple in the FC voltages has a maximum value at $M = 0.86$ and PF = 1, which is consistent with the theoretical analysis presented in Section 3.4.1.

For further experimental verifications of the proposed balancing method with only one sensor, a mismatch of 10% was made in the FCs by connecting a parallel capacitor with C_{fx1}, resulting in $C_{fx1} = 1.1C_{fx2}$. The experimental results for this case are shown in Fig. 3.24 for $Z = 25\angle 0^\circ\Omega$. As can be observed, at start-up, the auxiliary dc-link voltage V_{fx} is lower than its reference $V_{\text{dc}}/4$ (100 V), so the redundant states that charge the FCs are selected for $\pm 2E$ (V_3, V_{10} for PF = 1, see Table 3.1). Since the two FCs are simultaneously charged during $\pm 2E$

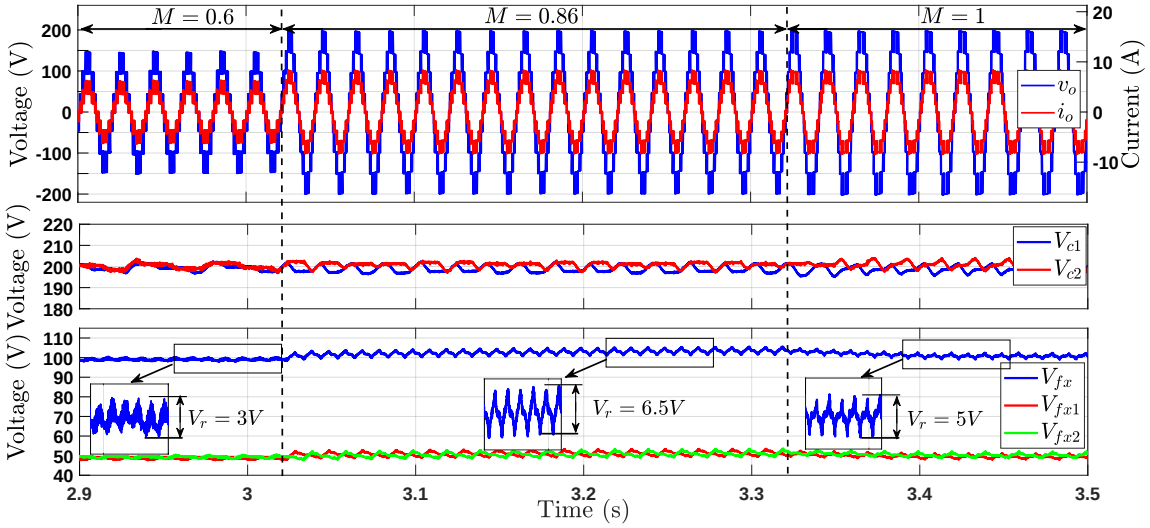


Figure 3.22: Experimental results of the 9L-SC-ANPC inverter for different values of M at PF = 1 (from top): output voltage, current, voltages of dc-link Capacitors, and FCs voltages.

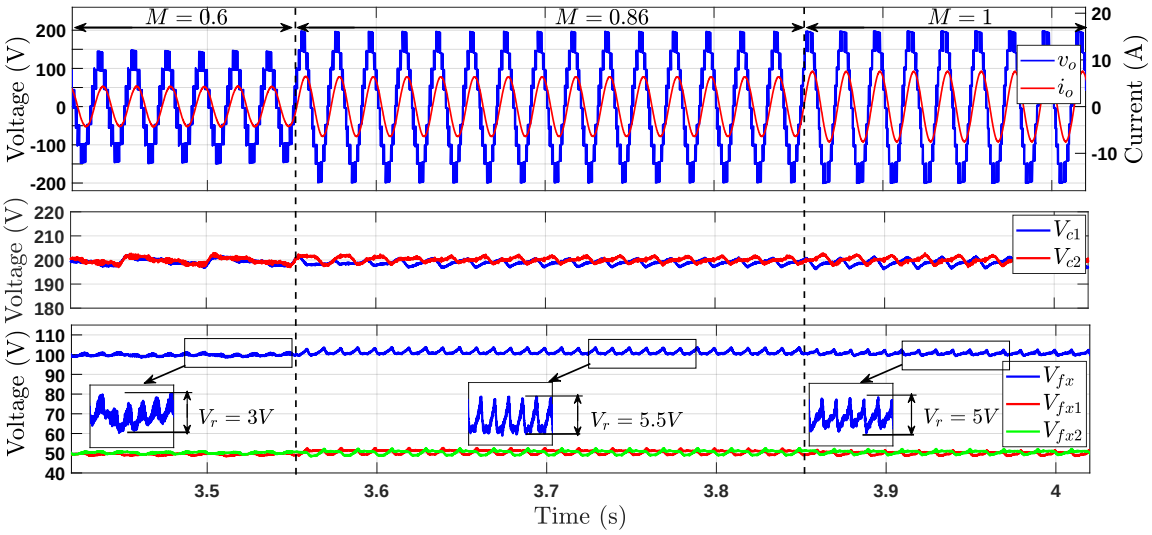


Figure 3.23: Experimental results of the 9L-SC-ANPC inverter for different values of M at PF = 0.89 (from top): output voltage, current, voltages of dc-link Capacitors, and FCs voltages.

with the same current i_o and as $C_{fx1} > C_{fx2}$, the voltage rise of C_{fx2} is higher than that of C_{fx1}. When V_{fx} settles around its reference, the charging or discharging states of $\pm 2E$ can be selected by the algorithm according to (3.11), (3.12), and (3.13). At this time, $V_{fx1} < V_{fx2}$ and both FCs are still charged and discharged with the same current during $\pm 2E$. However, due to $V_{fx1} < V_{fx2}$, the discharging of C_{fx1} during $-E$ will be lower than that of C_{fx2} during $+E$, and also the charging of C_{fx1} during $+3E$ will be higher than that of C_{fx2} during $-3E$, resulting in a gradual increase in V_{fx1} and a gradual decrease in V_{fx2}. This process continues until a voltage balance is reached between the two FCs as shown in Fig. 3.24. It can be also observed from Fig. 3.24 that, due to $C_{fx1} > C_{fx2}$, the voltage ripple V_r of C_{fx1} is slightly lower than that of

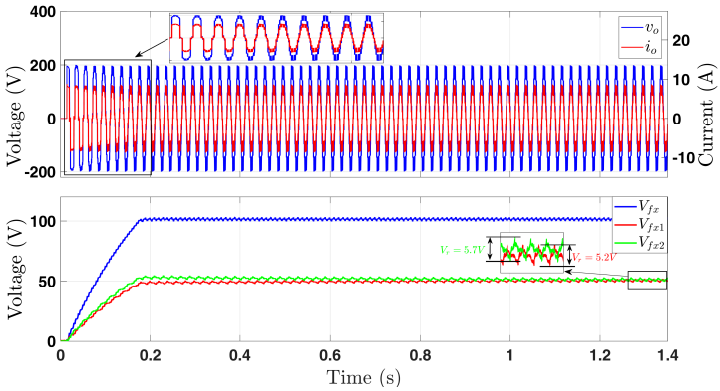


Figure 3.24: Experimental results of the 9L-SC-ANPC inverter for a mismatch of 10% in the FCs for a resistive load (PF = 1), $C_{fx1} = 1.1C_{fx2}$, (from top): output voltage and current, and FCs voltages.

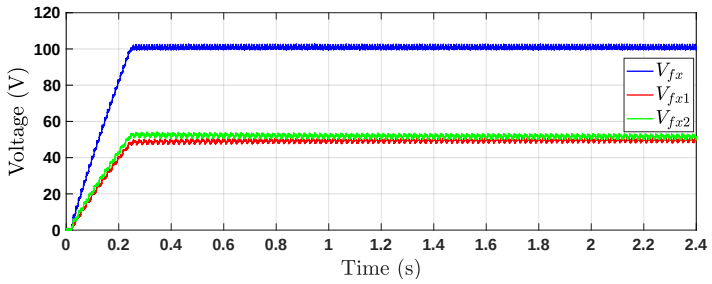


Figure 3.25: Experimental results for FCs voltages of the 9L-SC-ANPC inverter for a mismatch of 10% in the FCs for an RL load (PF = 0.89), $C_{fx1} = 1.1C_{fx2}$.

C_{fx2}. The results are also given for reactive power operation in Fig. 3.25. The operation of the 9L-SC-ANPC inverter with the change of the line frequency is shown in Fig. 3.26 for $M = 1$ and $Z = 25\angle 27.5°\Omega$. The results agree with the derived (3.24), where the ripple of the FCs was reducing with increasing f_{line} from 50 Hz to 100 Hz and, as expected, the ripple of the dc-link is reduced as well. One of the prominent features of the 9L-SC-ANPC inverter is the ability to cover the operation of the well-known 5L-ANPC inverter. In case of fault conditions of the four-quadrant switch S_8, the proposed inverter has the ability to change to the five-level operation as shown in Fig. 3.27. No transient time is required for this change as the FCs are still balanced at the same value and are considered as one FC balanced at $V_{\text{dc}}/4$. Moreover, the proposed inverter can resume its nine-level operation when S_8 is fixed. The THD of v_o in this mode of operation has a value of 27.25% compared to 12.96% in the nine-level operation.

Since the proposed 9L-SC-ANPC inverter is basically an upgrade of the conventional 5L-ANPC inverter, their performances in terms of harmonic spectrum and efficiency are compared experimentally under the same conditions. A prototype of the conventional 5L-ANPC variant I with the same power switch (FF50R12RT4) and 1000 μF FC is used for the comparison. The FC is balanced by the available redundant states and the dc-link is balanced with the same concept used for the proposed 9L-SC-ANPC inverter, Section 3.3.2. Fig. 3.28 shows the steady-state experimental waveforms of v_o, i_o, V_{c1}, V_{c2}, and V_{fx} for $Z = 25\angle 27.5°\Omega$. Fig. 3.29 shows the harmonic spectrum of v_o for the conventional 5L-ANPC and the proposed 9L-SC-ANPC

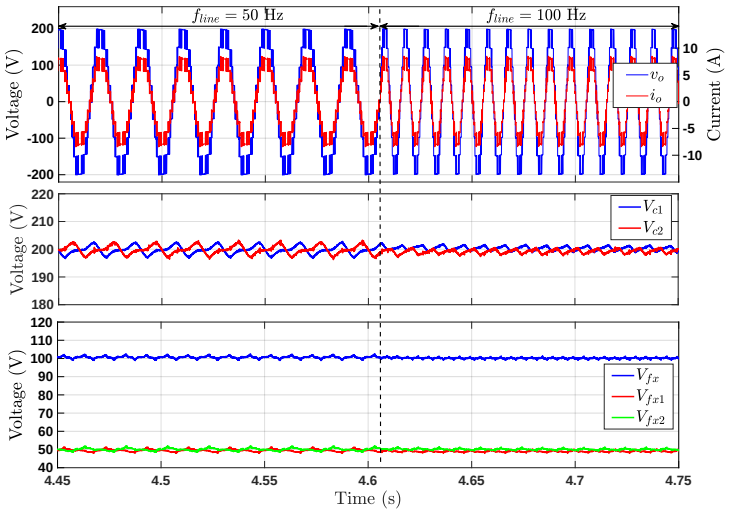


Figure 3.26: Experimental results of the 9L-SC-ANPC inverter for different f_{line} (50 Hz and 100 Hz) (from top): output voltage, current, voltages of dc-link Capacitors, and FCs voltages.

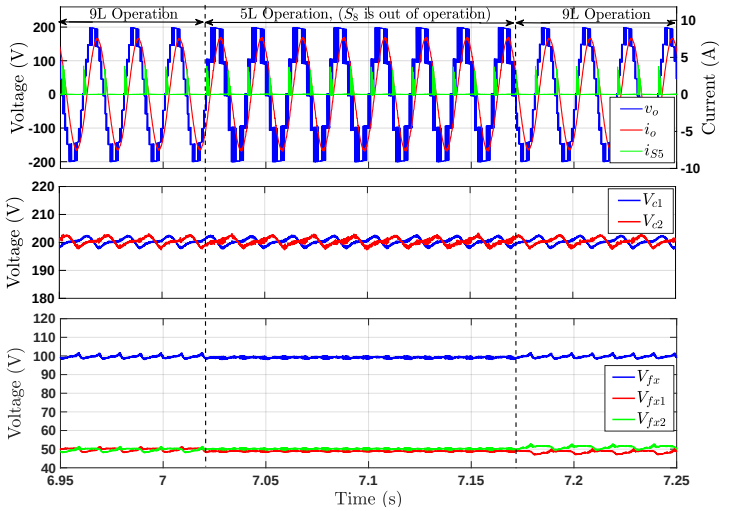


Figure 3.27: Experimental results of the 9L-SC-ANPC inverter in 9L and 5L (fault at S_8) operating modes (from top): output voltage, current and current of S_5, voltages of dc-link Capacitors, and FCs voltages.

inverter. As can be seen, and thanks to the higher number of levels, the proposed topology has a better harmonic profile with a THD of 12.96% compared to 27.25% in the conventional 5L-ANPC inverter, which significantly reduces the filer size. For the same load, the THD of i_o for the proposed and conventional 5L-ANPC inverter was found 0.93% and 2.02%, respectively. Fig. 3.30 depicts the experimental efficiency of the proposed and conventional 5L-ANPC inverter for output power ranging from 0.5 to 2.5-kW. It is clear that the proposed topology has higher efficiency for the whole range with a maximum value of 98.30% at 1-kW output power, while the conventional 5L-ANPC has a maximum efficiency of 97.60% at 0.75-kW output power. The comparison results in terms of the THD of v_o and i_o, and efficiency at 2-kW output power are listed in Table 3.4.

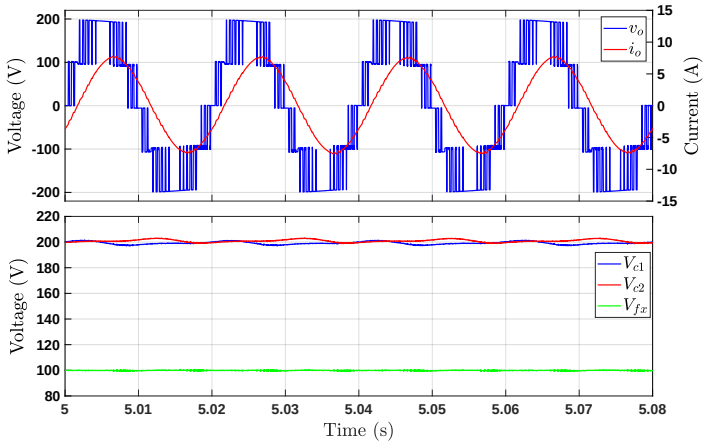


Figure 3.28: Experimental results of the conventional 5L-ANPC inverter for an RL load (PF = 0.89) at steady state (from top): output voltage and current, voltages of dc-link Capacitors, and FC voltage.

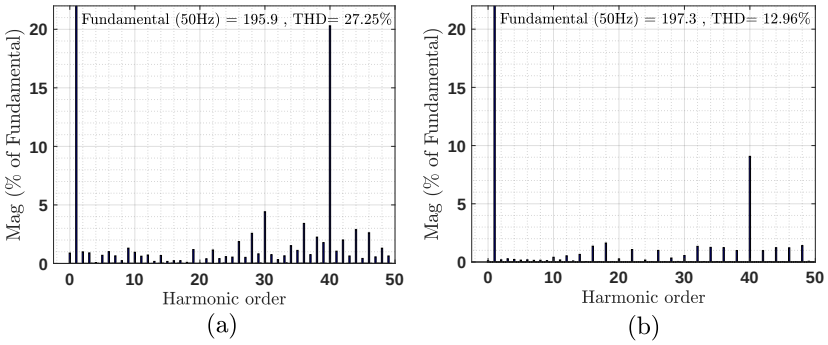


Figure 3.29: Harmonic spectrum of the experimental output voltage: (a) Conventional 5L-ANPC inverter. (b) 9L-SC-ANPC inverter

3.8 Summary

A novel nine-level ANPC-based inverter topology has been proposed in this chapter with low number of active and passive components. The proposed topology has been derived based on the commercially available 5L-ANPC inverter by adding a four-quadrant switch and an FC per phase-leg with reducing the voltage rated of the FCs. Exploiting the redundant states of the inverter, a balancing algorithm is designed for the dc-link and FCs. The developed algorithm has the ability to balance the two FCs with only one sensor, which further reduces the cost of the proposed 9L-SC-ANPC inverter. The designed balancing method has been integrated into the adopted PD-PWM strategy without the necessity for any external controller. Based on the PD-PWM, the mathematical analysis has been carried out to determine the capacitance values of the FCs and modulation index limitations. According to the analyzes and merits of the proposed 9L-SC-ANPC inverter, it is expected to be well appreciated in low- and medium-voltage medium power grid-connected applications. The proposed topology with the balancing strategy has been validated via simulation and experimental results under different operating conditions.

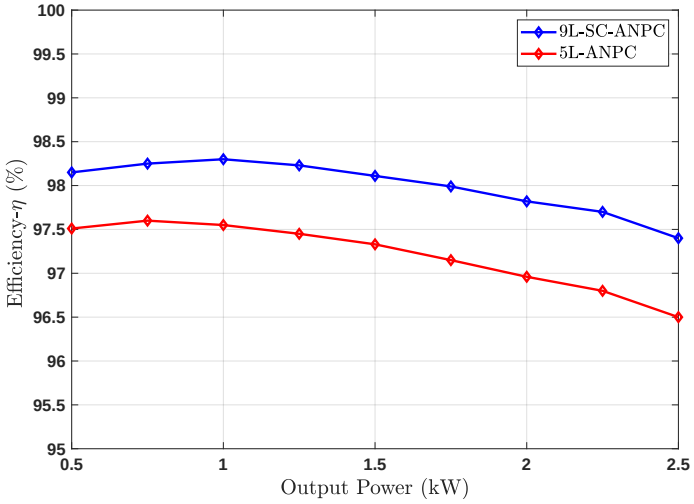


Figure 3.30: Experimental efficiency comparison between the conventional 5L-ANPC inverter and the proposed 9L-SC-ANPC inverter

Table 3.4: Experimental comparison between the conventional 5L-ANPC inverter and the proposed 9L-SC-ANPC inverter.

Parameter	Conventional 5L-ANPC	Proposed 9L-SC-ANPC
THD of v_o	27.25%	12.96%
THD of i_o $Z = 25\angle 27.5°\Omega$	2.02%	0.93%
Efficiency-η @ 2-kW	96.92%	97.83%

The detailed comparison with the conventional and other common dc-link 9L-ANPC inverters is provided in the next chapter. In addition, a simple and effective solution for the minimum modulation index limitation is presented in the next chapter (See chapter 4).

CHAPTER 4

A Nine-Level T-Type Converter for Grid-Connected Distributed Generation

This chapter presents a new high-efficiency nine-level T-type converter (9L-T^{2}C) for grid-connected applications based on the three-level T-type converter (3L-T^{2}C). The description, operation, and modulation of the 9L-T^{2}C are presented in Section 4.2. The operation at low modulation indices is ensured by a simple method as described in Section 4.3. The simulation of a 1-MW three-phase grid-connected 9L-T^{2}C is conducted in the MATLAB/Simulink environment, as described in Section 4.5. The topology with its modulation method has been validated experimentally for standalone and grid-connected operation in Section 4.6. A comprehensive comparison of the 9L-SC-ANPC and the 9L-T^{2}C with other prior-art nine-level topologies is presented in Section 4.7. Finally, Section 4.8 provides the summary of this chapter.

4.1 Introduction

It is of great advantage to implement new high-level topologies using the commercially available power electronics building blocks (PEBBs) without having to reconfigure the conventional structures. Accordingly, the impetus for this work is to develop a nine-level T-type converter (9L-T^{2}C) with its optimal modulation strategy as an upgrade of the 3L-T^{2}C with minimal modifications. The proposed 9L-T^{2}C reduces the topological complexity and control implementation compared to other nine-level converters. The high quality output waveforms, high efficiency, low cost of the proposed converter makes it a competitive candidate for filterless operation of grid-connected DG systems.

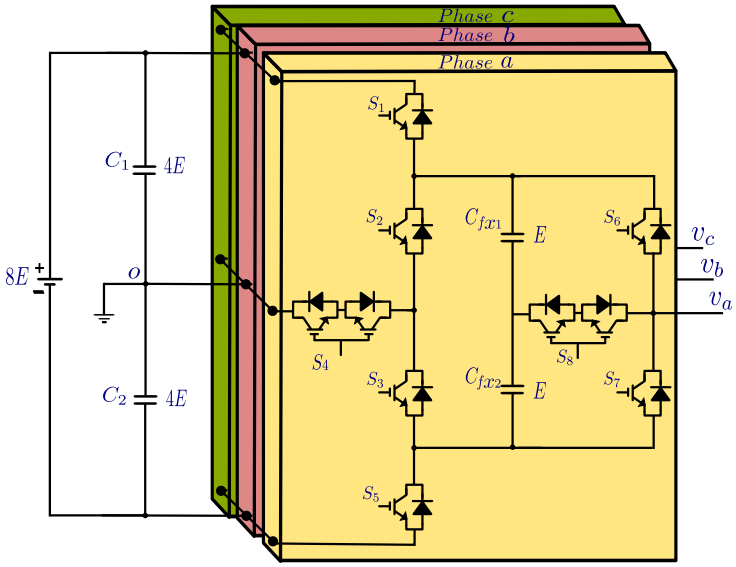


Figure 4.1: Proposed nine-level T-type converter.

4.2 Proposed Nine-level T-Type Converter

4.2.1 Topology description and operation

Figure 4.1 shows the power circuit of the proposed 9L-T^{2}C. Assuming the input voltage $V_{\text{dc}} = 8E$, the dc-link is formed by capacitors C_1 and C_2, with a sustained voltage of $4E$ each. The 9L-T^{2}C is constituted of two 3L-T^{2}C units and two LFSs S_1 and S_5, where the first 3L-T^{2}C unit has switches S_2, S_3 and S_4 and is operated at low switching frequency. While the second unit has switches S_6, S_7 and S_8 and is operated at higher switching frequency. Two FCs C_{fx1} and C_{fx2} are used for each phase-leg, forming one auxiliary dc-link. $x \in \{a, b, c\}$ indicates the corresponding phase. FCs voltages V_{fx1} and V_{fx2} are balanced at $V_{\text{dc}/8}$ (E) to generate nine voltage levels from the converter. Table 4.1 illustrates the available switching states of the 9L-T^{2}C with charging/discharging effects on FCs. The current paths of one phase leg during positive half-cycle are depicted in Fig. 4.2. According to Table 4.1, there are twelve switching states and labeled from V_1 to V_{12}. Three voltage levels $\pm 2E$ and 0 have redundancies as: ($+2E$: V_3 and V_4), (0: V_6 and V_7), and ($-2E$: V_9 and V_{10}). According to the complementary operation, the power devices are grouped into three sets: $\{S_1, S_4, S_5\}$, $\{S_2, S_3\}$, and $\{S_6, S_7, S_8\}$. The first two groups have low switching frequency, whereas the third is operated at higher frequency. Based on the operation of the proposed 9L-T^{2}C, the blocking voltages of power devices in each switching state are given in Fig. 4.3.

Referring to Table 4.1, it can be observed that the available redundancies for levels $\pm 2E$ have an opposite influence on C_{fx1} and C_{fx2}, and also, for each switching state, C_{fx1} and C_{fx2} are simultaneously charged or discharged. The balancing method of FCs is developed based on this key observation. To this end, the auxiliary dc-link voltage V_{fx} and output current i_o are sensed to determine the suitable switching state. For example, considering voltage level $+2E$, if V_{fx} is higher than its reference V_{fx}^* and $i_o \geq 0$, then state V_4 is applied to discharge the two FCs. The NP potential control is designed without the need for further redundant states by controlling the

Table 4.1: Switching states of the 9L-T^{2}C (↑: charge, ↓: discharge, −: No impact).

											$i_o > 0$		$i_o < 0$	
Level	State	s_1	s_2	s_3	s_4	s_5	s_6	s_7	s_8	v_o	C_{fx1}	C_{fx2}	C_{fx1}	C_{fx2}
L_1	V_1	1	0	1	0	0	1	0	0	+4E	−	−	−	−
L_2	V_2	1	0	1	0	0	0	0	1	+3E	↑	−	↓	−
L_3	V_3	1	0	1	0	0	0	1	0	+2E	↑	↑	↓	↓
L_3	V_4	0	0	1	1	0	1	0	0	+2E	↓	↓	↑	↑
L_4	V_5	0	0	1	1	0	0	0	1	+E	−	↓	−	↑
L_5	V_6	0	0	1	1	0	0	1	0	0	−	−	−	−
L_5	V_7	0	1	0	1	0	1	0	0	0	−	−	−	−
L_6	V_8	0	1	0	1	0	0	0	1	-E	↑	−	↓	−
L_7	V_9	0	1	0	1	0	0	1	0	-2E	↑	↑	↓	↓
L_7	V_{10}	0	1	0	0	1	1	0	0	-2E	↓	↓	↑	↑
L_8	V_{11}	0	1	0	0	1	0	0	1	-3E	−	↓	−	↑
L_9	V_{12}	0	1	0	0	1	0	1	0	-4E	−	−	−	−

power flow interaction of the 9L-T^{2}C, as explained in Section 3.3.2. The balance of FCs and dc-link capacitor is incorporated into the designed PD-PWM technique without the need for advanced controllers.

The configuration of the proposed converter for higher levels is depicted in Fig. 4.4. The generated voltage levels N_{level} and required number of power devices N_{sw} and FCs N_{FC} are calculated for a number of extension units N as

$$\left.\begin{aligned} N_{\text{level}} &= 2^{N+2}+1, \\ N_{\text{sw}} &= 4N+5, \\ N_{\text{FCs}} &= 2N. \end{aligned}\right\} \tag{4.1}$$

The FC voltage of each unit $i = \{1, 2, ..., N\}$ can be determined as

$$V_{fx1i} = V_{fx2i} = \frac{V_{\text{dc}}}{2^{i+2}}. \tag{4.2}$$

4.2.2 PD-PWM of the 9L-T^{2}C

Among several modulation strategies, the PD-PWM method is adopted in this work because of its low harmonic contents and low complexity [166]. The block diagram of the PD-PWM and the developed balancing scheme are shown in Fig. 4.5. The FCs and NP balancing method described in the previous chapter for the 9L-SC-ANPC converter is adopted here for the 9L-T^{2}C. As previously mentioned, the available zero-level states have no impact on the FCs and, hence, cannot be involved in the FC balance because no current flows through the FCs through these states. Therefore, the redundant states V_6 and V_7 are used to reduce the switching frequency based on the polarity of the modulation signal v_m. While for the 9L-SC-ANPC, the available

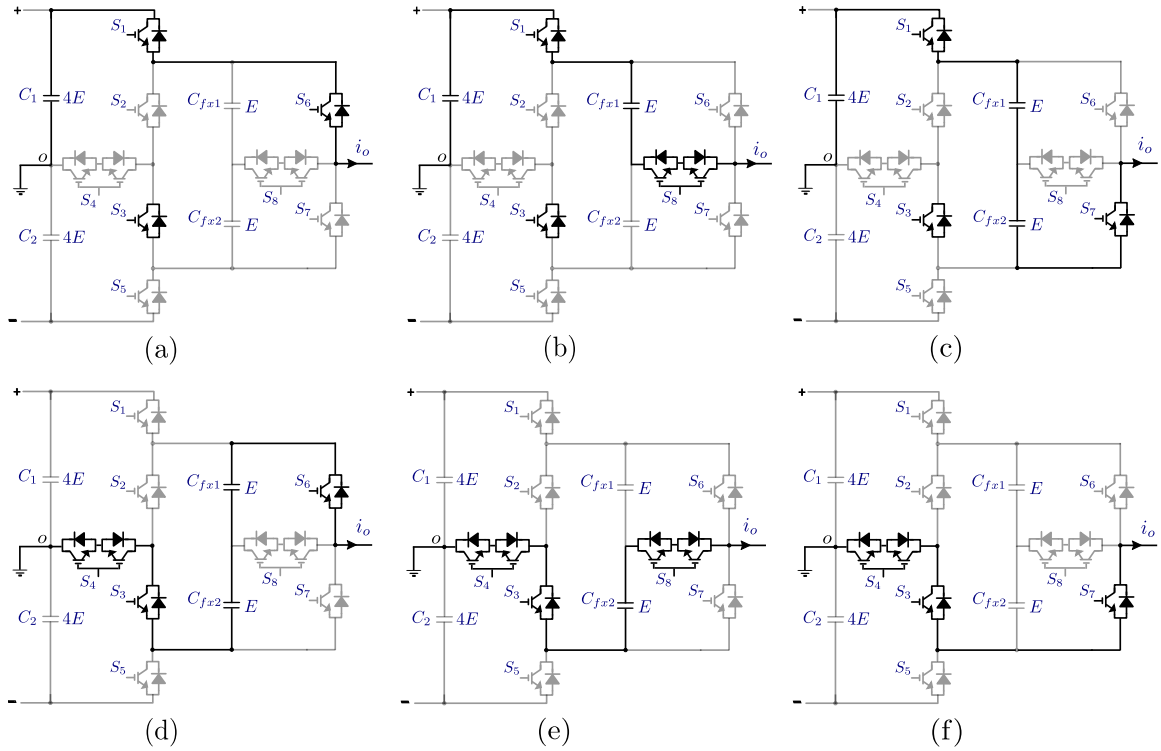


Figure 4.2: Current paths of the 9L-T^{2}C through positive half-cycle. (a) State V_1. (b) State V_2. (c) State V_3. (d) State V_4. (e) State V_5. (f) State V_6.

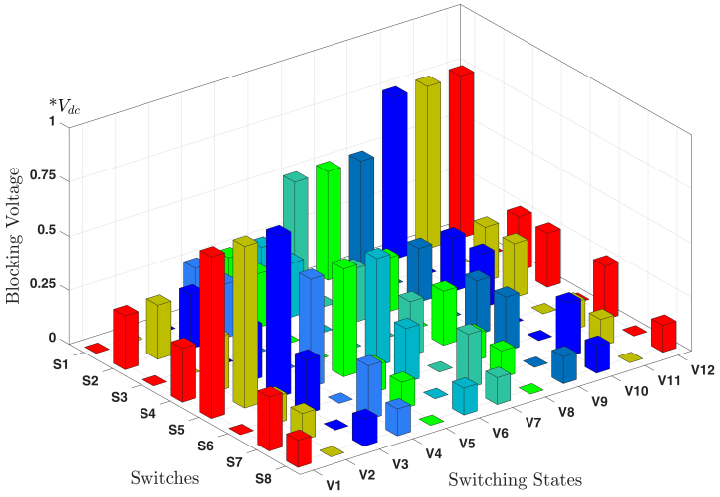


Figure 4.3: Blocking voltage of the power switches.

zero-level states have been exploited to reduce the current stress on S_5, as explained in Section 3.3.3. The flowchart of the balancing control scheme for the proposed 9L-T^{2}C is depicted in Fig. 4.6. Fig. 4.7 shows the PWM waveforms of the 9L-T^{2}C. Reactive power operation case is assumed to illustrate the modulation and capacitor balancing method, which is also applicable for unity PF. As can be seen in Fig. 4.7, the modulation signal v_m is compared with nine in-phase carriers to identify the level region. Then, the switching state of each level is determined

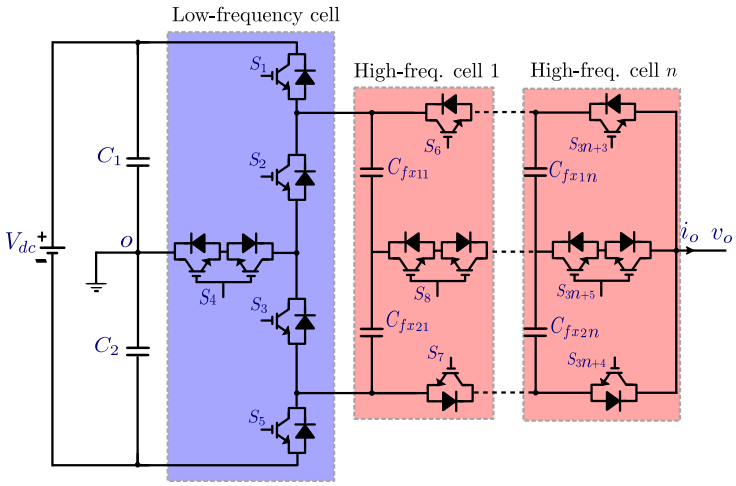


Figure 4.4: Extension of the proposed T-type converter.

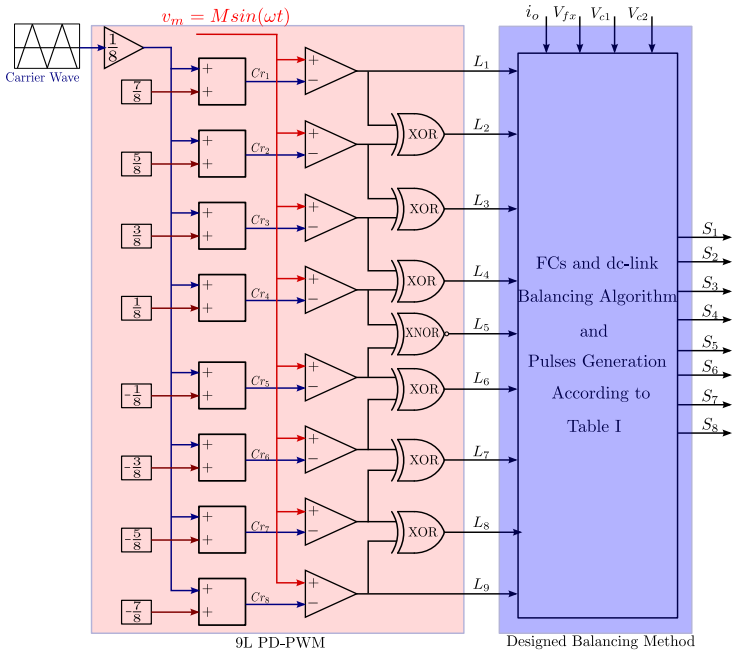


Figure 4.5: Block diagram of the PD-PWM with the developed balancing algorithm.

based on the developed capacitor balance method. Based on v_m and i_o polarity, the fundamental cycle has four regions, two active regions $R2$ and $R4$, and two reactive regions $R1$ and $R3$, as depicted in Fig. 4.7.

4.3 Operation at low modulation indices

Although the 9L-T^{2}C and 9L-SC-ANPC have different structures with different numbers and ratings for power devices, they have the same number of switching vectors with the same charging/discharging effects on the FCs. Consequently, the mathematical analysis and formulation

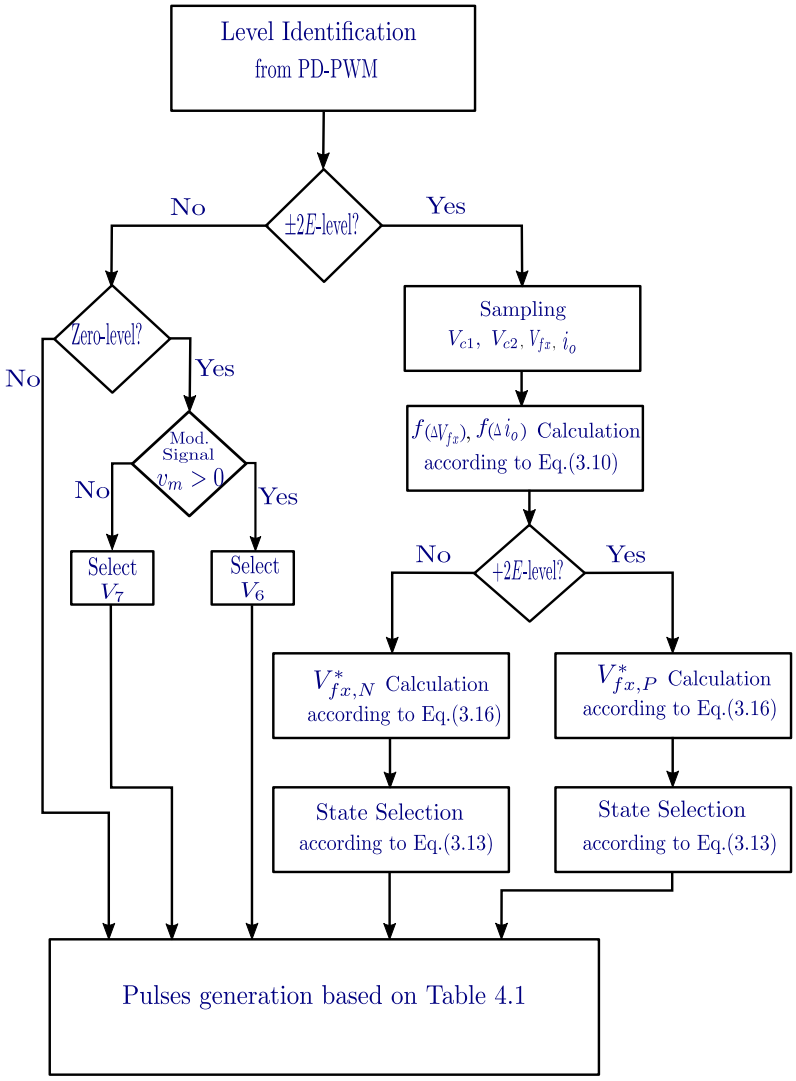


Figure 4.6: Flowchart of the balancing method for the 9L-T^{2}C.

of the FCs sizing presented in Section 3.4.1 for the 9L-SC-ANPC are also applicable to the 9L-T^{2}C. According to the analysis presented in Section 3.4.2, the minimum modulation index with FCs and NP balancing is 0.395.

To ensure proper operation at low values of modulation index ($M < 0.395$) with balancing the FCs and NP potential, the operation is switched to the five-level mode. In this mode, the FCs are seen as one capacitor with a value half of C_{fx1} or C_{fx2}. The transition from nine-level to five-level operation is achievable without a transient time because the auxiliary dc-link is still regulated to the same value, i.e. $\frac{V_{\text{dc}}}{4} = 2E$, and the produced levels are $\pm 4E$, $\pm 2E$, and 0. Fig. 4.8 shows the number of pole levels N_{level} versus M for the two modes of operation. The seven-level operation is also attainable with this topology, however, the auxiliary dc-link voltage should be changed to $V_{\text{dc}}/6$, which needs a set-point change and transient time for the FCs stabilization at the new reference voltage.

To avoid the unstable transition between the nine-level and five-level modes in the case of M oscillation, a hysteresis range is provided as shown in Fig. 4.9. Operating the proposed

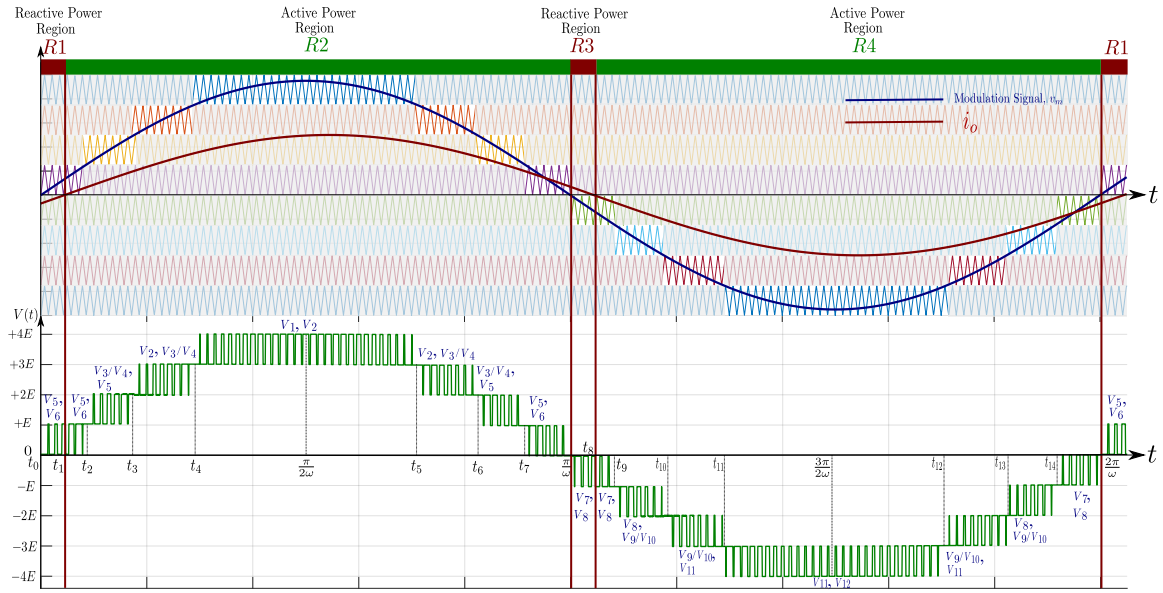


Figure 4.7: Waveforms of PD-PWM for the 9L-T^{2}C.

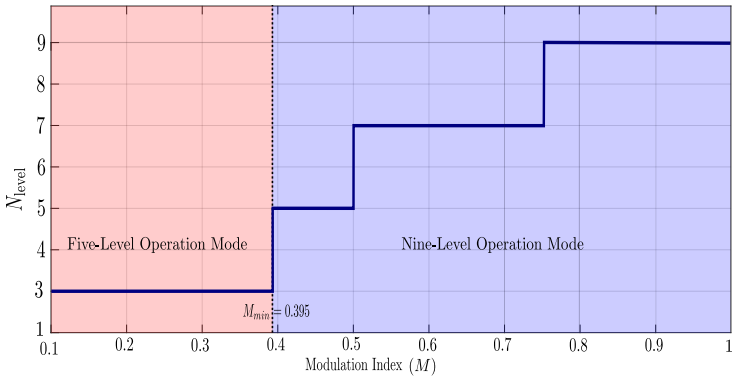


Figure 4.8: N_{level} versus M of the proposed 9L-T^{2}C.

topology at lower voltage levels at $M < 0.395$ does not have a negative impact on the usability of the converter, since at such very low values of M the difference between the nine-level and five-level modes in terms of waveform quality and efficiency is not remarkable.

4.4 Power loss analysis

The 9L-T^{2}C is modeled in PLECS environment to calculate the power losses and efficiency. A single-phase 10-kW model is built with $V_{\text{dc}} = 1$ kV and carrier frequency $f_c = 3$ kHz. The load is represented by an AC current source with 40-A amplitude. FF50R12RT4 IGBT manufactured by Infineon is used as a power device in the PLECS model. The thermal description data of the IGBT used is obtained from Infineon. Fig. 4.10 depicts the conduction and switching losses of the power devices for the 9L-T^{2}C at different values of $M = 1$ and PF. It can be observed that for the four conditions studied, the converter losses are dominated by the conduction losses of the power devices. Note that S_4^1 and S_4^2 denote the switches of the bidirectional switch S_4

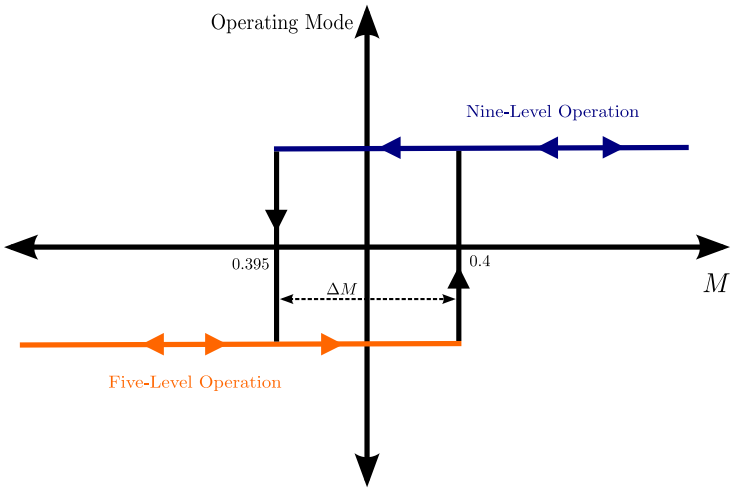


Figure 4.9: Hysteresis band of M.

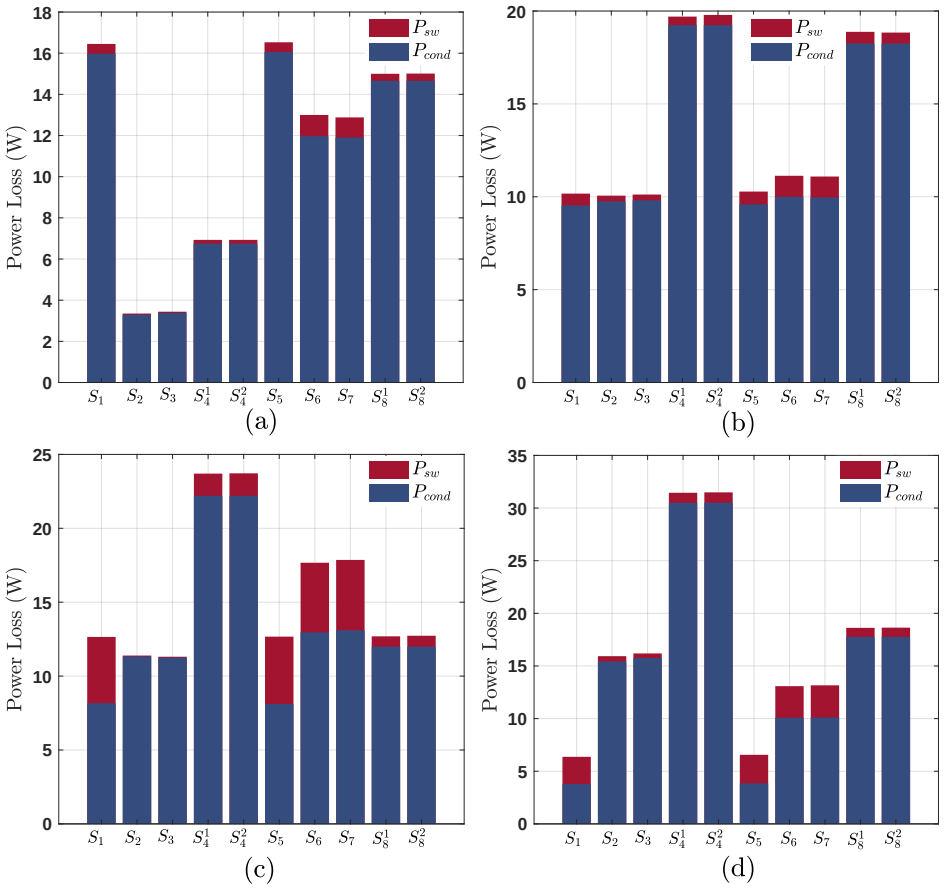


Figure 4.10: Power devices losses of the 9L-T^{2}C: (a) $M = 1$, PF = 1. (b) $M = 1$, PF = 0.5. (c) $M = 0.5$, PF = 1. (d) $M = 0.5$, PF = 0.5.

and, hence, have a similar loss value for all cases. Also, S_8^1 and S_8^1 denote the switches of the bidirectional switch S_8. According to the losses calculation, the efficiency of the proposed

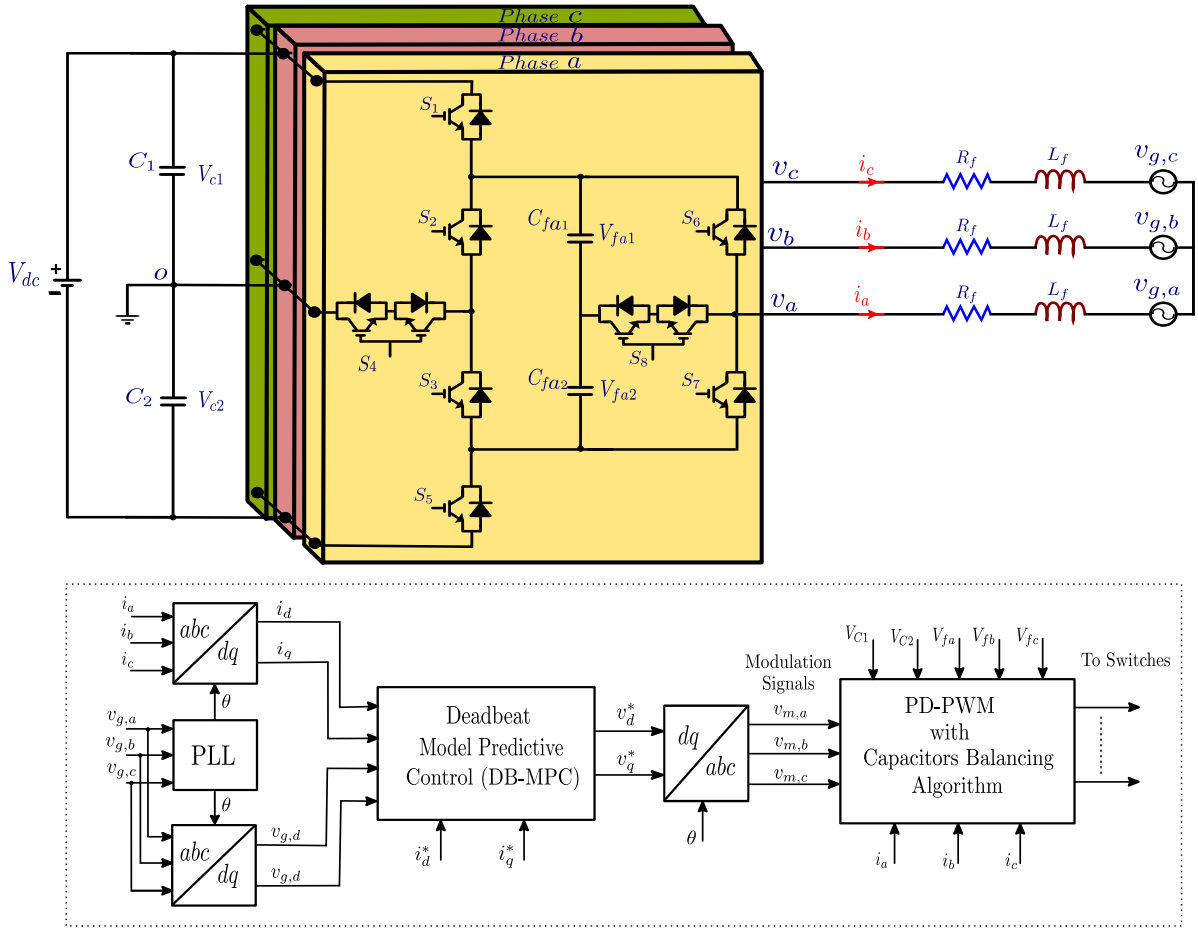


Figure 4.11: Three-phase grid-connected 9L-T^{2}C and its associated control method.

Table 4.2: Parameters of the three-phase 9L-T^{2}C for 1-MVA grid-connected system.

Parameter	Value
dc-link voltage, V_{dc}	6.8 kV
Grid voltage, $V_{g,l-l}$ (line-to-line)	4.16 kV
Line frequency, f_c	50 Hz
Carrier frequency, f_c	2 kHz
Filter resistance and inductance, R_f and L_f	0.1 Ω and 2.5 mH
dc-link capacitors, C_1 and C_2	2.5 mF
FCs, C_{fx1} and C_{fx2}	7 mF
FCs voltage tolerance	60 V

9L-T^{2}C is 98.91% at $M = 1$ and PF = 1.

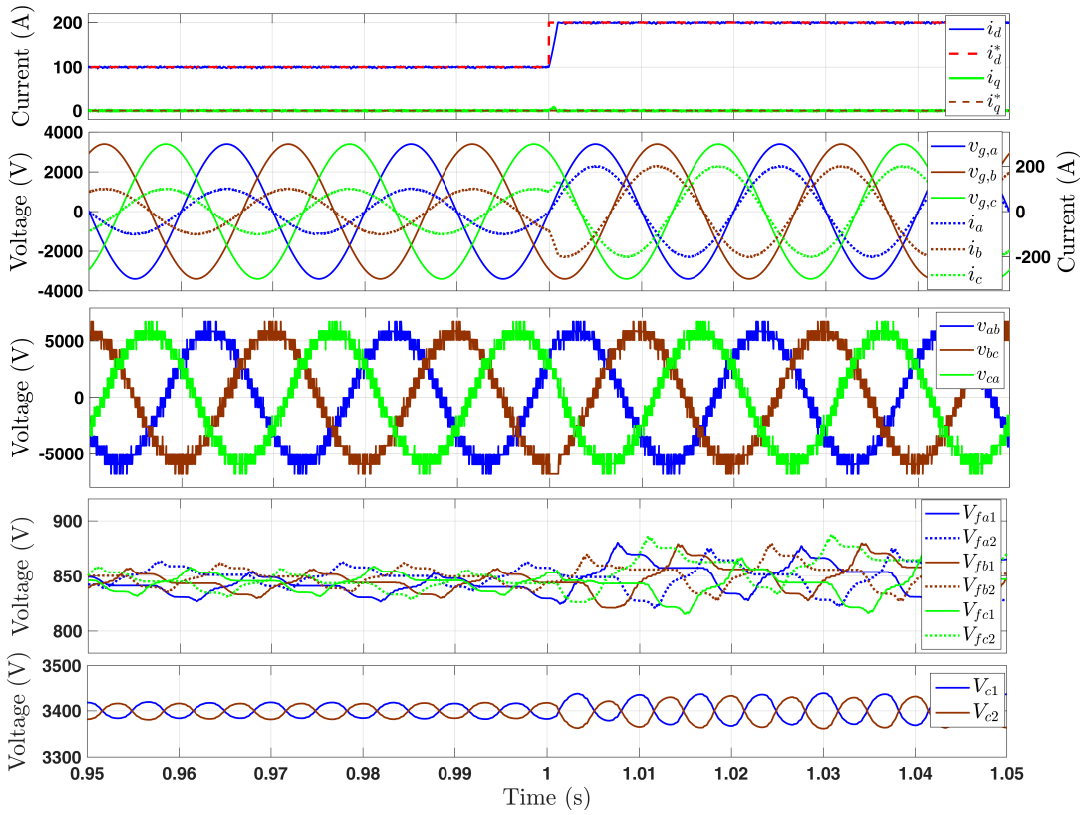


Figure 4.12: Simulation waveforms of the grid-connected 9L-T^{2}C for active power injection (from top): active and reactive current components i_d and i_q, grid voltage and currents, output line-to-line voltages of the 9L-T^{2}C, FCs voltages, and dc-link capacitors voltage.

Table 4.3: Parameters of the single-phase 9L-T^{2}C for simulation and experimental implementation.

Parameter	Value
Input dc-link, V_{dc}	400 V
Line frequency, f_{line}	50 Hz
Carrier frequency, f_c	3 kHz
dc-link capacitors, C_1 and C_2	3.3 mF
FCs, C_{fx1} and C_{fx2}	4 mF
FCs voltage tolerance (PF = 1, $M = 0.86$)	5 V

4.5 Simulation results

The performance of the three-phase grid-connected 9L-T^{2}C is simulated in MATLAB/Simulink environment. The simulation model is built for 1 MVA medium-voltage system with a grid voltage $V_{g,l-l} = 4.16$ kV (line-to-line). The capacitance of the FCs is determined according to (3.25) for a voltage tolerance of 60 V at the worst case (PF = 1, $M = 0.86$). The simulation parameters of the model are given in Table 4.2. The schematic diagram of the grid-connected 9L-T^{2}C with its designed control is shown in Fig. 4.11. A standard dead beat model predictive

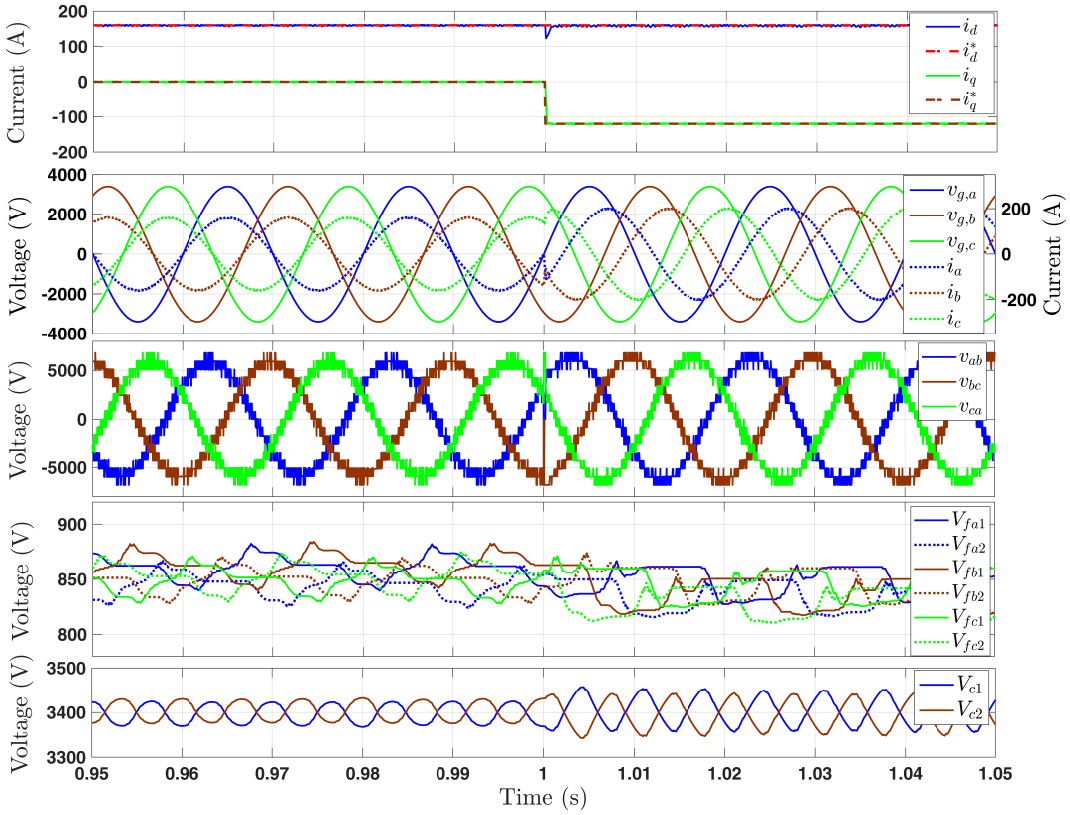


Figure 4.13: Simulation waveforms of the grid-connected 9L-T^{2}C for active and reactive power injection (from top): active and reactive current components i_d and i_q, grid voltage and currents, output line-to-line voltages of the 9L-T^{2}C, FCs voltages, and dc-link capacitors voltage.

control (DB-MPC) is considered to regulate the active and reactive current components of the injected power. The design of the standard DB-MPC for the three-phase grid-connected system is detailed in [167, 168]. The DB-MPC generates the modulation signals ($v_{m,a}$, $v_{m,b}$, $v_{m,c}$) for the PD-PWM, which includes the developed balancing algorithm for the dc-link and FCs, as depicted in Fig. 4.11.

Figure 4.12 shows the simulation results of the grid-connected 9L-T^{2}C for active power operation with a step change in the active reference current $i_{d,ref}$ from 100 A to 200 A at $t = 1$ s and $i_{q,ref} = 0$ A. The output line-to-line voltages of the 9L-T^{2}C has 17 levels in the complete cycle, which results in high-quality voltage and injected current as shown in the results. The FCs are well balanced at their reference ($V_{fx,ref} = V_{\text{dc}}/8 = 850$ V) with only one sensor for each phase-leg. The performance of the 9L-T^{2}C with active and reactive power supply (PF = 0.8) is depicted in Fig. 4.13. In this case $i_{d,ref}$ is set to 160 A with a step change in $i_{q,ref}$ from 0 A to -120 A. The results show the ability of the proposed algorithm to regulate two FCs using one voltage sensor with balancing the dc-link under active and reactive power supply.

The simulation model of the single-phase 9L-T^{2}C is also built in MATLAB/Simulink with the parameters listed in Table 4.3. To validate the developed method for balancing the two FCs with only one sensor, a case study on the dissimilarity of the FCs is examined. In this test, FCs have different initial voltages, where the initial values of V_{fx1} and V_{fx2} are set to 40 V and 60 V, respectively. In addition, there is a mismatch in the capacitance values between

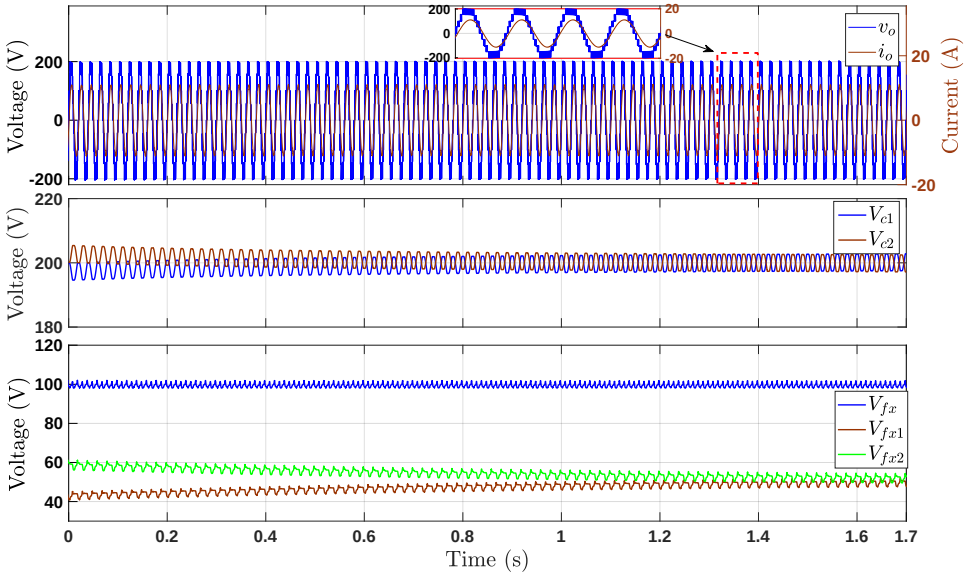


Figure 4.14: Simulation waveforms of the single-phase 9L-T^{2}C with different initial voltages of FCs (V_{fx1}=40 V, V_{fx2}=60 V) and capacitance mismatch (C_{fx1}=1.1C_{fx2}) for stand-alone operation $Z = 17\angle 28.3°\Omega$ (from top): inverter voltage and current, dc-link voltages, and FCs voltages.

the two capacitors, where C_{fx1} is increased by 10% and accordingly C_{fx1}=1.1C_{fx2}. Fig. 4.14 depicts the simulation results for this case study. As it can be seen, at time $t = 0$, $V_{fx1} = 40$ V, $V_{fx2} = 60$ V, and the controlled $V_{fx} = 100$ V. As previously discussed, the levels that affect the charge of C_{fx1} are $\pm 2E$, $+3E$, and $-E$, while for C_{fx2} are $\pm 2E$, $-3E$, and $+E$. The charge variation during $\pm 2E$ is the same for the two FCs as they are charged or discharged with the same current during these levels and, hence, no charge difference between C_{fx1} and C_{fx2} arises during $\pm 2E$. However, since $V_{fx1} < V_{fx2}$, the charge taken from C_{fx1} during $-E$ is less than that taken from C_{fx2} during $+E$. Also, the charge stored in C_{fx1} during $+3E$ is more than that stored in C_{fx2} during $-3E$. The charge difference generated during $\pm E$ and $\pm 3E$ makes V_{fx1} gradually increase and, simultaneously, V_{fx2} gradually decrease, as shown in Fig. 4.14, until balancing is achieved between the FCs. Also, as can be seen, the voltage ripple of V_{fx2} is slightly higher than that of V_{fx1} due to the capacitance mismatch. From this test, it is clear that the balancing of the auxiliary dc-link at $V_{\text{dc}}/4$ is sufficient to stabilize the two FCs at $V_{\text{dc}}/8$ because the two capacitors can naturally achieve equilibrium between each other.

4.6 Experimental results

To demonstrate the feasibility and practicability of the 9L-T^{2}C and its designed PD-PWM method, the experimental prototype of the 9L-T^{2}C is built in the laboratory. As explained before, the redundant states of a single-phase are sufficient to ensure proper operation with balancing the FCs of this phase and the dc-link capacitors. Accordingly, a single-phase implementation is sufficient to validate the proposed topology with the developed modulation strategy. The parameters of the experimental implementation are listed in Table 4.3. For FCs sizing,

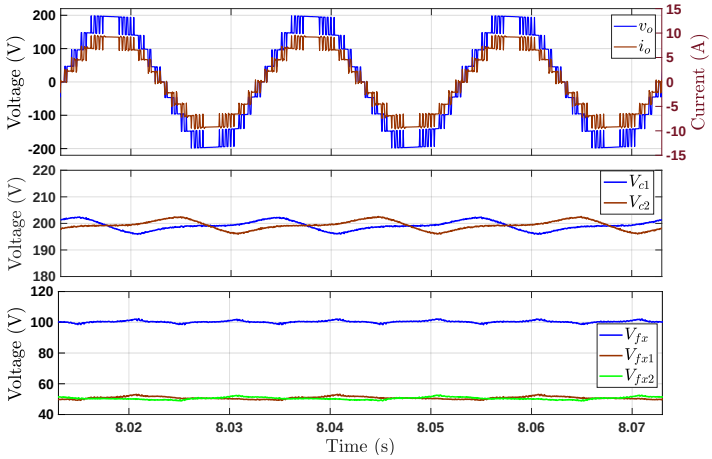


Figure 4.15: Experimental waveforms at steady-state for a resistive load (from top): inverter voltage v_o and current i_o, dc-link V_{c1} and V_{c2}, and FCs voltages V_{fx}, V_{fx1}, and V_{fx2}.

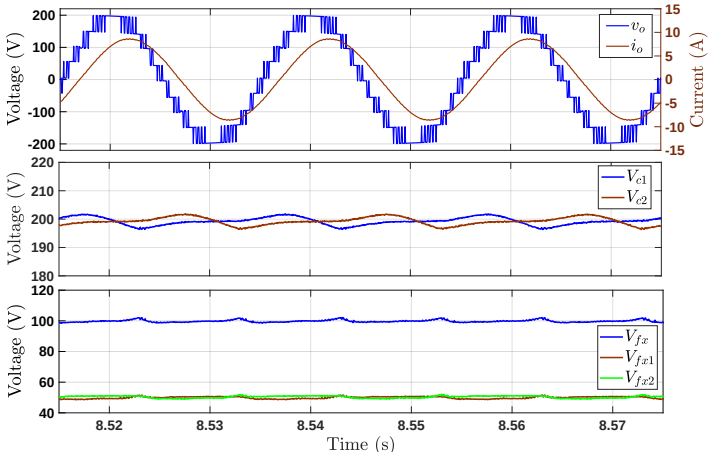


Figure 4.16: Experimental waveforms at steady-state for a resistive-inductive load (from top): inverter voltage v_o and current i_o, dc-link V_{c1} and V_{c2}, and FCs voltages V_{fx}, V_{fx1}, and V_{fx2}.

considering dc-link voltage as 400 V, line frequency as 50 Hz, peak current as 9 A, and FCs voltage tolerance as 5 V at the worst case (PF = 1, M = 0.86), the calculated value of C_{fx1} and C_{fx2} according to (3.24) is 3.9 mF. In the experimental prototype, C_{fx1} and C_{fx2} are chosen as 4 mF. The value of k in (3.16) is tuned at 0.2 and kept constant for all operating conditions.

4.6.1 Stand-alone operation

The experimental waveforms of v_o, i_o, V_{c1}, V_{c2}, V_{fx}, V_{fx1}, and V_{fx2} at steady-state for stand-alone operation $Z = 22\angle 0°\Omega$ are given in Fig. 4.15. As can be seen, v_o has nine levels in the fundamental cycle, which results in high quality waveforms with low harmonic contents of v_o and i_o. The dc-link capacitors are well stabilized at $V_{\text{dc}}/2$ with the developed NP regulation method. Additionally, the voltages of the FCs are balanced at $V_{\text{dc}}/8$ (50 V) using one voltage sensor, which agrees with the mathematical analysis and validates the designed balancing algorithm. The waveforms of the 9L-T^{2}C at P F= 0.88 are depicted in Fig. 4.16, $Z = 22\angle 28.3°\Omega$.

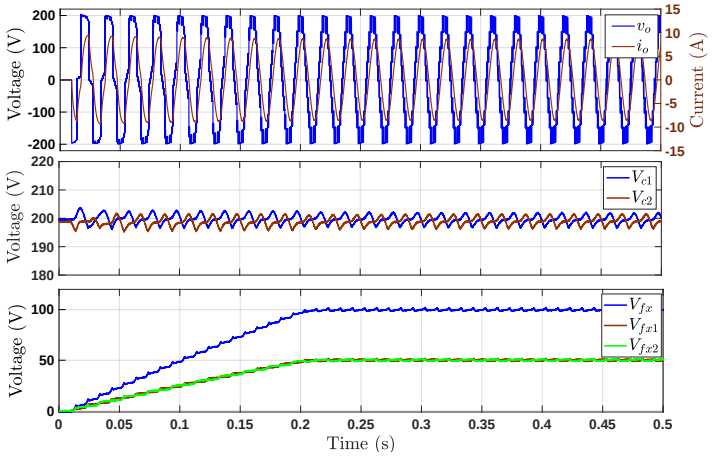


Figure 4.17: Start-up experimental waveforms of the 9L-T^{2}C with a resistive-inductive load (from top): inverter voltage v_o and current i_o, dc-link V_{c1} and V_{c2}, and FCs voltages V_{fx}, V_{fx1}, and V_{fx2}.

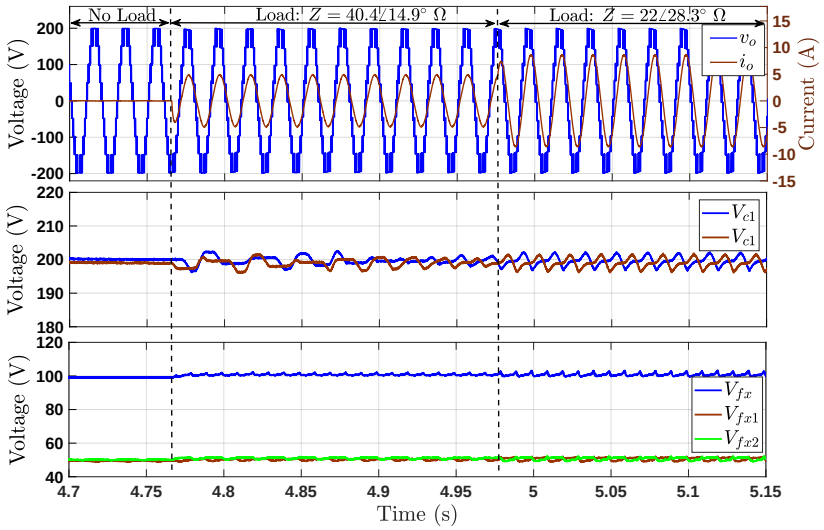


Figure 4.18: Experimental waveforms of the 9L-T^{2}C for load step-changes (from top): inverter voltage v_o and current i_o, dc-link V_{c1} and V_{c2}, and FCs voltages V_{fx}, V_{fx1}, and V_{fx2}.

The FCs and NP potential are strongly controlled with acceptable ripple values. Thanks to the produced high-quality waveforms, the THD of v_o and i_o was found 12.1% and 0.88%, respectively. The start-up process of the 9L-T^{2}C is shown in Fig. 4.17. It can be observed that V_{fx} increases from 0 to its reference $V_{\text{dc}}/4$ (100 V) and, simultaneously, V_{fx1} and V_{fx2} increase from 0 to stabilize at $V_{\text{dc}}/8$ (50 V). The operation of the 9L-T^{2}C with step-changes in the load is depicted in Fig. 4.18, where the load is changed from no load to $Z = 40.4\angle 14.9°\Omega$ and then to $Z = 22\angle 28.3°\Omega$. It is obvious that the NP potential is balanced under all load conditions. Furthermore, the FCs are well controlled showing a strong balancing behavior using only one voltage sensor in spite of the sudden current changes.

To validate the operation of the 9L-T^{2}C and the proposed balancing method with the change

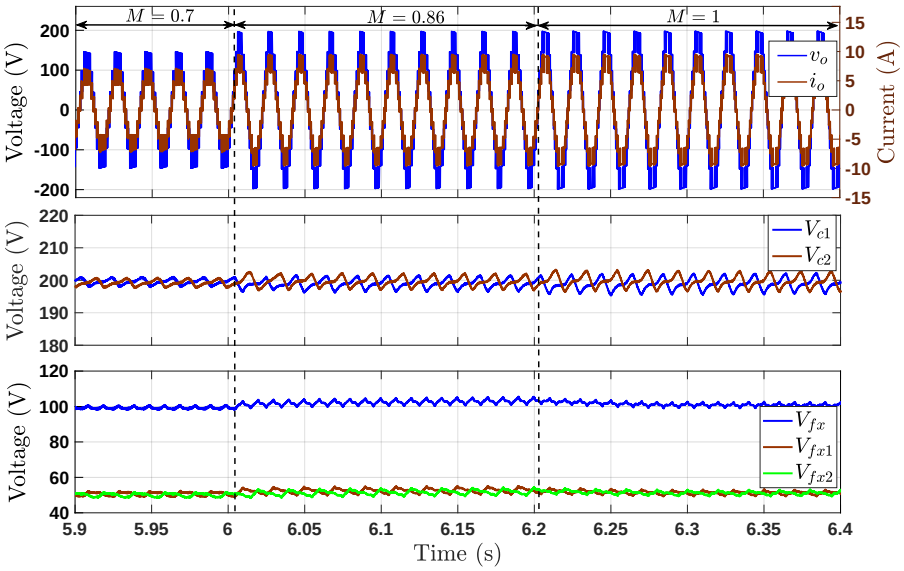


Figure 4.19: Waveforms of the 9L-T^{2}C with changing M at PF = 1 (from top): inverter voltage v_o and current i_o, dc-link V_{c1} and V_{c2}, and FCs voltages V_{fx}, V_{fx1}, and V_{fx2}.

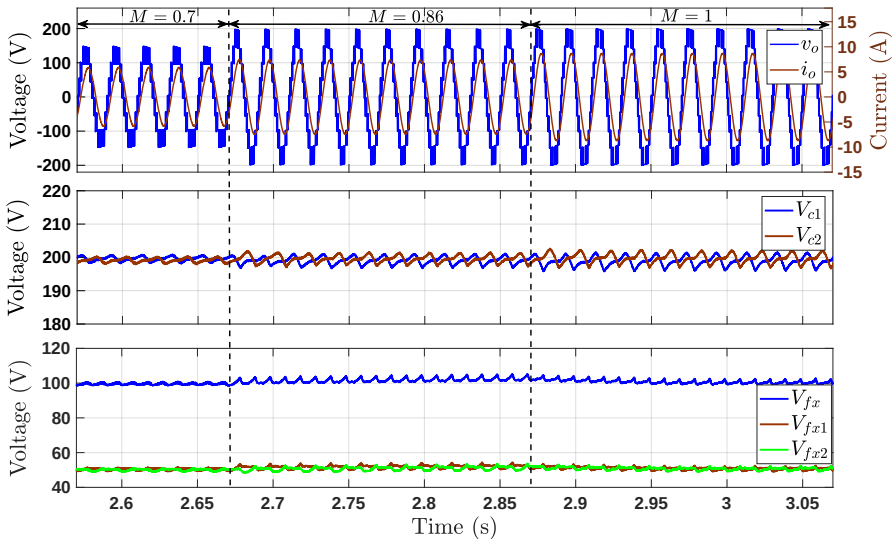


Figure 4.20: Waveforms of the 9L-T^{2}C with changing M at PF = 0.88 (from top): inverter voltage v_o and current i_o, dc-link V_{c1} and V_{c2}, and FCs voltages V_{fx}, V_{fx1}, and V_{fx2}.

in Modulation index M, Fig. 4.19 shows the experimental waveforms at M=0.7, 0.86, and 1 for $Z = 22\angle 0°\Omega$. The results of the same test but with a stand-alone resistive inductive load $Z = 22\angle 28.3°\Omega$ are given in Fig. 4.20. It can be concluded that, with the variation of M, the developed PD-PWM with the capacitors balancing method can stabilize the FCs and NP potential with regulating the voltage/current. In addition, as proved theoretically in Section 3.4, the worst case of the voltage ripple for the FCs is reached at $M = 0.86$ and PF = 1, as can be observed from Fig. 4.19 and Fig. 4.20.

To validate the developed NP potential and FCs balancing method under the FCs dissimilarity

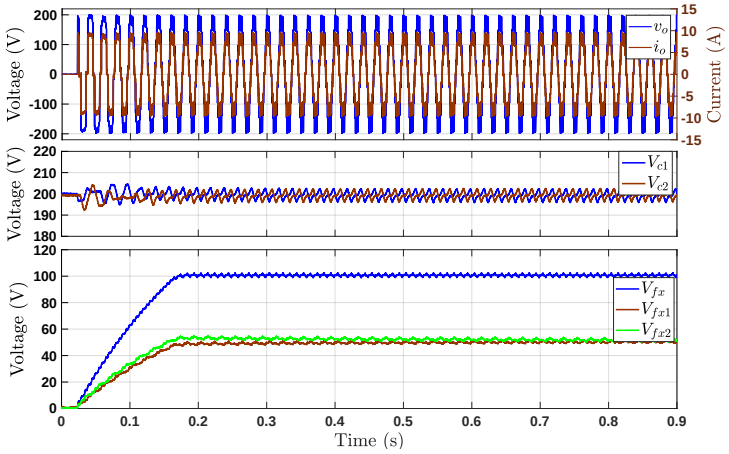


Figure 4.21: Experimental operation with a mismatch of 10% in the FCs, $C_{fx1} = 1.1C_{fx2}$, (from top): inverter voltage v_o and current i_o, dc-link V_{c1} and V_{c2}, and FCs voltages V_{fx}, V_{fx1}, and V_{fx2}.

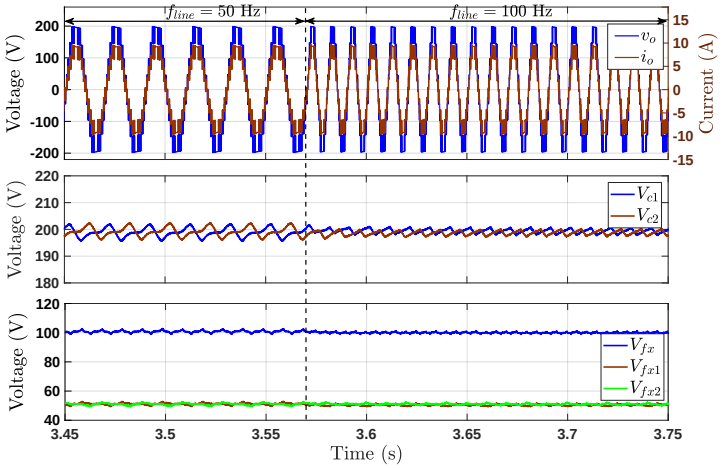


Figure 4.22: Experimental operation with changing f_{line} (from top): inverter voltage v_o and current i_o, dc-link V_{c1} and V_{c2}, and FCs voltages V_{fx}, V_{fx1}, and V_{fx2}.

case, the performance is experimentally investigated with a 10% mismatch in capacitance. The mismatch is realized by connecting an additional capacitor across C_{fx1} to reach the case $C_{fx1} = 1.1C_{fx2}$. Fig. 4.21 shows the experimental waveforms for this test for stand-alone operation at $Z = 22\angle 0°\Omega$. As it is clear from the results, at the beginning, the total voltage of the two FCs V_{fx} is less than the reference value $V_{\text{dc}}/4$, accordingly, the balancing method applies the redundant states that increase V_{fx} during $\pm 2E$ (V_3, V_{10}, see Table 4.1). As the two FCs are concurrently charged with i_o through $\pm 2E$ and because of the capacitance mismatch $C_{fx1} > C_{fx2}$, the increase of C_{fx2} voltage is higher than that of C_{fx1}, as can be observed in Fig. 4.21 during start-up. After V_{fx} reaches $V_{\text{dc}}/4$ (100 V), the redundant state that reduces the deviation of V_{fx} from its reference is applied. At this point, the two FCs have different voltages $V_{fx1} < V_{fx2}$ and, therefore, the charge taken from C_{fx1} during $-E$ is less than that taken from C_{fx2} during $+E$. Also, the charge stored in C_{fx1} during $+3E$ is more than that stored in C_{fx2} during

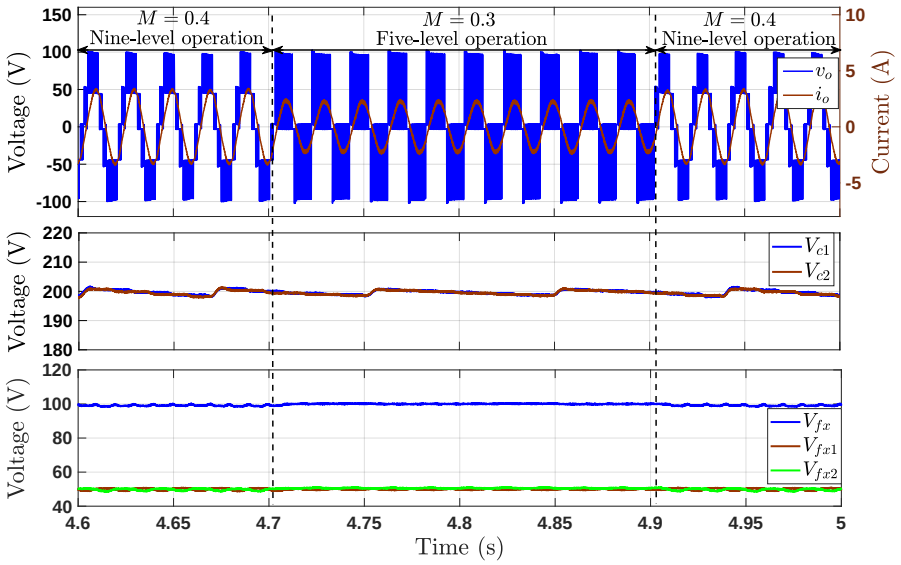


Figure 4.23: Experimental results at low values of M (from top): inverter voltage v_o and current i_o, dc-link V_{c1} and V_{c2}, and FCs voltages V_{fx}, V_{fx1}, and V_{fx2}.

Table 4.4: Grid connection operation parameters.

Parameter	Value
Grig voltage, v_g	120 V (rms)
Grid frequency, f_{line}	50 Hz
Filter inductance, L_f	4 mH
Filter resistance, R_f	0.2 Ω

$-3E$. The charge difference generated during $\pm E$ and $\pm 3E$ makes V_{fx1} gradually increase and, simultaneously, V_{fx2} gradually decrease until equilibrium is realized, as depicted in Fig. 4.21. This case study clearly demonstrates the capability of the proposed scheme to balance two FCs using one voltage sensor, even when there is a dissimilarity between the capacitors. The operation of the 9L-T^{2}C at two different line frequencies (50 Hz and 100 Hz) is illustrated in Fig. 4.22 with $Z = 22\angle 28.3°\Omega$ and $M = 1$. The results are consistent with the capacitance formula (3.24), where the FCs voltage ripple decreases as the line frequency increases.

To validate the operation of the 9L-T^{2}C under low values of M, the performance is investigated at $M = 0.4, 0.3$, and then back to 0.4 as shown in Fig. 4.23. According to the designed PD-PWM strategy, at $M = 0.4$ the converter is operated in the nine-level operation mode and then switched to the five-level mode at $M = 0.3$ to ensure the balancing of the FCs and NP as discussed in Section 4.3. It can be seen that no transient time is required to switch between the two operating modes as the two FCs are still regulated at the same reference and seen as one FC. The generated levels in the five-level mode are $\pm 4E$, $\pm 2E$, and 0. However, only three level ($\pm 2E$, 0) is generated as shown in Fig. 4.23 as the converter is operated at low M (0.3).

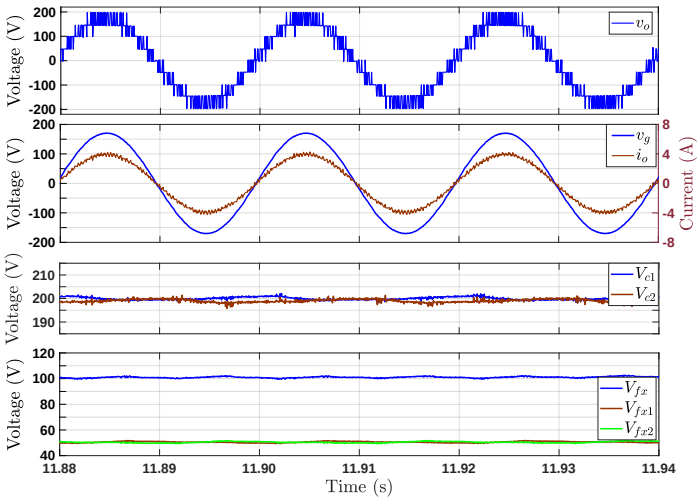


Figure 4.24: Steady-state experimental waveforms of the grid-connected operation for active power injection (PF = 1) (from top): inverter voltage v_o, grid voltage v_g and current i_o, dc-link voltages V_{c1} and V_{c2}, and FCs voltages V_{fx}, V_{fx1}, and V_{fx2}.

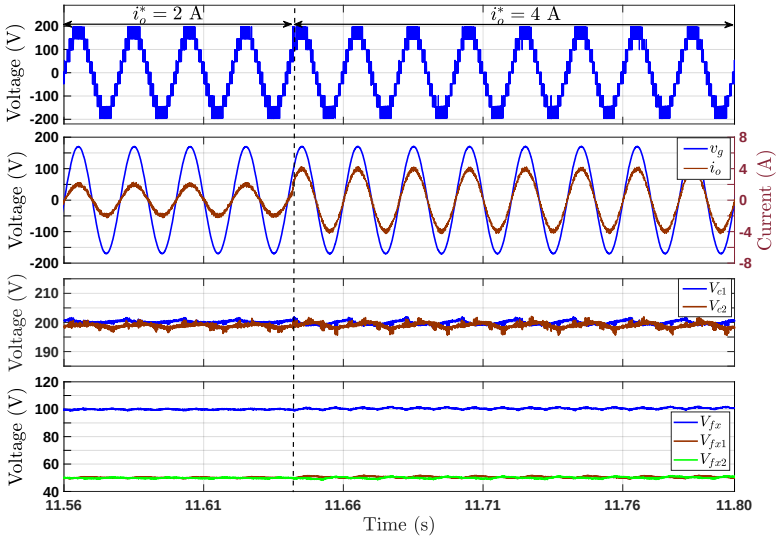


Figure 4.25: Experimental results of the grid-connected operation for active power injection (PF = 1) and step-change in the current (from top): inverter voltage v_o, grid voltage v_g and current i_o, dc-link voltages V_{c1} and V_{c2}, and FCs voltages V_{fx}, V_{fx1}, and V_{fx2}.

4.6.2 Grid-connected operation

To experimentally validate the grid-connected operation of the 9L-T^{2}C with the developed modulation strategy under active and reactive power supply, a standard DB-MPC is designed to generate the modulation signal v_m based on the reference current [167]. The phase angle of the reference current $i_{out,ref}$ is estimated from the grid-voltage using a phase-locked loop (PLL) block, while the amplitude of $i_{out,ref}$ is determined according to the amount of power to be injected. A single-phase four-quadrant voltage/current source, shown in Fig. B.2, is used to

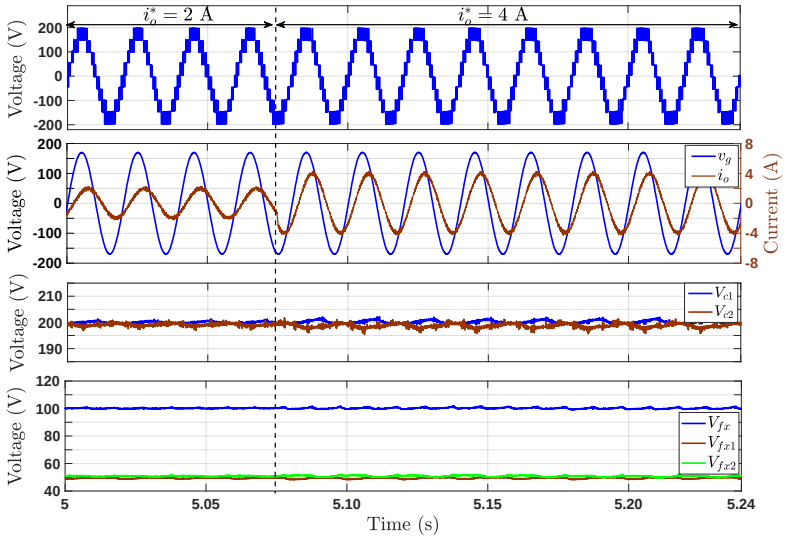


Figure 4.26: Experimental results of the grid-connected operation for active and reactive power injection (PF = 0.77) and step-change in the current (from top): inverter voltage v_o, grid voltage v_g and current i_o, dc-link voltages V_{c1} and V_{c2}, and FCs voltages V_{fx}, V_{fx1}, and V_{fx2}.

represent the grid. The parameters of the grid-connection operation are given in Table 4.4.

The steady-state operation of the 9L-T^{2}C in grid-connected mode with active power injection (PF = 1) is shown in Fig. 4.24. The reference value of i_o is set to 4 A. It can be observed that a nine-level voltage is generated at the output of the 9L-T^{2}C. Grid voltage and the injected current are well synchronized with unity PF operation. The FCs and dc-link capacitors are balanced at their references. Fig. 4.25 shows the experimental results for active power operation (PF = 1) with a step-change in the injected current from 2 A to 4 A. As can be seen, the NP potential and FCs are well stabilized at their references despite the sudden change in i_o. The converter operation under reactive power injection with a step-change in the current is shown in Fig. 4.26, where i_o is lagging the grid voltage v_g by 40° (PF = 0.77). It is clear that the designed modulation strategy is able to achieve the balancing of the NP potential and FCs under active and reactive power supply of the grid-connected operation. In addition, the results confirm the capability of the developed approach to balance two FCs using only one sensor.

4.7 Comparison with other nine-level converters

Several nine-level converters have been reported in the literature and proven to have a good performance in their considered application areas [60, 67, 120, 122, 126, 140, 142, 143, 169–171]. Topologies with boosting capabilities may be considered an appealing choice in some applications areas such as photovoltaic applications [60, 122, 143, 169]. However, these structures typically increase the current and voltage ratings of power devices and/or lose the ability to use a common dc-link for the three-phase implementation, thus reducing their usability in medium voltage high power applications. In addition, these topologies use a relatively larger number of components compared to non-boosting topologies. Therefore, for a fair and realistic evaluation, the 9L-SC-ANPC and 9L-T^2 topologies are compared with other converters that have the same

characteristics, such as nine-level, non-boosting, shared dc-link in the multi-phase implementation, NP-based and suitable for low/medium voltage/power applications. Considering these points, the comparison includes the three conventional variants of the 9L-ANPC as a natural extension of the traditional 5L-ANPC [24, 99] and other recent converters that have the same characteristics and are proven to have high performance in [23, 67, 120, 126, 140, 142].

The comparison is performed for a single-phase leg on the basis of several aspects. First, a quantitative comparison is carried out in terms of the numbers of the required components. Second, the voltage ratings of FCs and their voltage diversity factor (VDF) are investigated. Third, the voltage stress of the switches along with their switching frequency is studied as an indication for the loss distribution between the switches. Fourth, the number of conducting switches per level is compared as a crucial factor for conduction loss and total saturation voltage. Fifth, and finally, the power loss analysis is performed for all considered converters and compared under the same operating conditions. Since the considered converters use a shared dc-link in the three-phase implementation, two capacitors with a voltage of $V_{\text{dc}}/2$ are used for the dc-link, and, hence, this aspect is excluded from the comparison.

4.7.1 Quantitative comparison

The required number of active switches N_{sw}, gate drivers N_{driv}, diodes N_d, and FCs N_{FC} for each topology are listed in Table 4.5. It should be mentioned that two nine-level configurations are proposed in [120] and the considered one in the comparison is the modified reduced switch configuration. As can be seen, the 9L-SC-ANPC converter has the fewest number of active switches (9) with two additional diodes as a substitute of one active switch, as explained in the derivation of this topology. Definitely, two diodes are cheaper than one active switch with its gate driver circuit. The 9L-T^{2}C requires only 10 active switches N_{sw} like the converters reported in [140, 142]. Moreover, if the four-quadrant MOSFET/IGBT is employed, the proposed 9L-SC-ANPC and 9L-T^{2}C will have the fewest number of switches (8). Furthermore, the 9L-T^{2}C and the 9L-SC-ANPC topologies have the fewest number of gate drivers (8) compared to other topologies, which reduces the overall cost of the converter. As in the converters proposed in [67, 140, 142], the 9L-T^{2}C and the 9L-SC-ANPC require two FCs instead of three in the conventional variants and in [120]. In general, it can be concluded that the proposed 9L-SC-ANPC and 9L-T^{2}C topologies have the fewest number of components compared to other ANPC inverters.

4.7.2 FCs Voltages

Indeed, capacitors are considered as one of the weakest components in power electronics converters and negatively affect the lifetime of the system [172]. Therefore, from the reliability point of view, it is important not only to reduce the number of FCs but also reduce their voltage ratings. Besides, reducing the FCs voltage is highly desirable because of its significant impact on the size and cost of the converter. Table 4.5 shows the sustained voltages of the required capacitors for the considered topologies. It can be seen that the 9L-SC-ANPC, 9L-T^{2}C and the topology reported in [140] have the lowest sustained voltages of the FCs, where two capacitors are required to be maintained at $V_{\text{dc}}/8$ (E). To further investigate this important aspect, VDF is considered in the comparison, which can be defined as the sum of FCs voltages calculated in

Table 4.5: Comparison with other common dc-link nine-level converters for single-phase configuration.

Topology	N_{sw}	N_d	N_{driv}	Blocking voltage	TSV	FCs			VDF	FCs sensors	N_{cond}						Efficiency[a] η
						$3V_{dc}/8$	$V_{dc}/4$	$V_{dc}/8$			$\pm 4E$	$\pm 3E$	$\pm 2E$	$\pm E$	0	avg.	
Conventional 9L-ANPC Variant I	12	-	12	$4\times V_{dc}/2$ $8\times V_{dc}/8$	3	1	1	1	0.75	3	5	5	5	5	5	5	97.86%
Conventional 9L-ANPC Variant II	12	-	12	$2\times 5V_{dc}/8$ $2\times V_{dc}/2$ $8\times V_{dc}/8$	3.25	1	1	1	0.75	3	4	4.25	4.5	4.75	5	4.67	98.03%
Conventional 9L-ANPC Variant III	12	-	11	$2\times 5V_{dc}/8$ $2\times 3V_{dc}/8$ $8\times V_{dc}/8$	3	1	1	1	0.75	3	4	4.5	5	5.5	6	4.89	97.87%
Stacked Multicell Converter (SMC) [23]	16	-	16	$8\times V_{dc}/4$ $8\times V_{dc}/8$	3	2	2	2	1.5	6	4	5	6	7	8	5.78	98.12%
[126]	12	-	12	$4\times V_{dc}/2$ $4\times V_{dc}/4$ $4\times V_{dc}/8$	3.5	-	2	1	0.625	3	4	4.67	5	5.33	6	4.89	98%
[140]	10	-	9	$4\times V_{dc}/2$ $4\times V_{dc}/4$ $2\times V_{dc}/8$	3.25	-	-	2	0.25	2	3	4	3	4	3	3.44	98.58%
[67]	12	-	12	$4\times V_{dc}/2$ $4\times V_{dc}/4$ $4\times V_{dc}/8$	3.5	-	1	1	0.375	2	5	5	5	5	5	5	97.75%
[142]	10	-	9	$2\times 3V_{dc}/4$ $4\times V_{dc}/4$ $4\times V_{dc}/8$	3	-	1	1	0.375	2	3	3	4	5	5	3.89	98.57%
[120]	14	-	14	$2\times V_{dc}/2$ $8\times V_{dc}/4$ $4\times V_{dc}/8$	3.5	-	2	1	0.625	3	5	5	5	5	5	5	97.78%
9L-SC-ANPC	9	2	8	$2\times 3V_{dc}/4$ $2\times V_{dc}/2$ $3\times V_{dc}/4$ $2\times V_{dc}/8$	3.5	-	-	2	0.25	1	2	3	2.5^A 3^R	4^A 5^R	3	2.89^A 3.22^R	98.95%
9L-T^{2}C	10	-	8	$2\times 3V_{dc}/4$ $6\times V_{dc}/4$ $2\times V_{dc}/8$	3.25	-	-	2	0.25	1	2	3	3	5	4	3.33	98.91%

[a] Efficiency is determined at $f_c = 3$ kHz, 10-kW single-phase. A: refers to active power operation and R: refers to reactive power operation.

per-unit [60] and expressed as

$$\text{VDF} = \sum_{i=1}^{k} \frac{V_{fxi}}{V_{\text{dc}}},\ k = 1, 2, ..., m, \tag{4.3}$$

where m is the total number of FCs in the converter. The computed VDF values are given in Table 4.5. The 9L-SC-ANPC, 9L-T^{2}C and the converter in [140] have the lowest VDF (0.25), which is a valuable feature compared to other converters.

4.7.3 Blocking voltage and switching frequency of switches

The voltage stress of switches along with their switching frequency is given in Table 4.6. For the 9L-SC-ANPC, 9L-T^{2}C and the converter in [142], S_1 and S_4 should block a voltage of $6E$ compared to $4E$, $5E$ and $5E$ for the conventional ANPC inverter variants I, II and III, respectively. However, this does not mean an increase in the switching losses because their voltage change is only $2E$ when they are switched ON or OFF. In other words, the step change of the blocked voltage is $2E$ as shown in Figs. 3.4 and 4.3 for the 9L-SC-ANPC, 9L-T^{2}C, respectively. S_2 and S_3 in the 9L-SC-ANPC converter have voltage stresses of $4E$, which is

Table 4.6: Blocking voltage and switching frequency of power devices for the considered nine-level inverters (BV: blocked voltage, f_{sw}: switching frequency, H: high, L: low).

Topology	Conventional 9L-ANPC																**9L-SC-ANPC**		**9L-T^{2}C**	
	Variant I		Variant II		Variant III		[126]		[140]		[67]		[142]		[120]					
Switch[a]	BV	f_{sw}	BV	f_{sw}	BV	f_{sw}	BV	f_{sw}	BV	f_{sw}	BV	f_{sw}	BV	f_{sw}	BV	f_{sw}	BV	f_{sw}	BV	f_{sw}
S_1	$4E$	L	$5E$	L	$5E$	L	$4E$	L	$4E$	L	$4E$	L	$6E$	L	$2E$	H	$6E$	L	$6E$	L
S_2	$4E$	L	$4E$	L	$3E$	L	$4E$	L	$4E$	L	$4E$	L	$2E$	L	$2E$	H	$4E$	L	$2E$	L
S_3	$4E$	L	$4E$	L	$3E$	L	$4E$	L	$4E$	L	$4E$	L	$2E$	L	$2E$	H	$4E$	L	$2E$	L
S_4	$4E$	L	$5E$	L	$5E$	L	$4E$	L	$4E$	L	$4E$	L	$6E$	L	$2E$	H	$6E$	L	$\pm 2E$	L
S_5	E	H	E	L	E	L	$2E$	L	$2E$	H	$2E$	H	$2E$	L	$2E$	H	$2E$	L	$6E$	L
S_6	E	H	E	L	E	L	$2E$	L	$2E$	H	$2E$	H	$2E$	L	$2E$	H	$2E$	H	$2E$	H
S_7	E	H	E	H	E	H	$2E$	L	$2E$	H	$2E$	H	E	H	$2E$	H	$2E$	H	$2E$	H
S_8	E	H	E	H	E	H	$2E$	L	$2E$	H	$2E$	H	E	H	$2E$	H	$\pm E(2E)$	H	$\pm E(2E)$	H
S_9	E	H	E	H	E	H	E	H	$\pm E(2E)$	H	E	H	E	H	$4E$	L	-	-	-	-
S_{10}	E	H	E	H	E	H	E	H	-	-	E	H	E	H	$4E$	L	-	-	-	-
S_{11}	E	H	E	H	E	H	E	H	-	-	E	H	-	-	E	H	-	-	-	-
S_{12}	E	H	E	H	E	H	E	H	-	-	E	H	-	-	E	H	-	-	-	-
S_{13}	-	-	-	-	-	-	-	-	-	-	-	-	-	-	E	H	-	-	-	-
S_{14}	-	-	-	-	-	-	-	-	-	-	-		-	-	E	H	-	-	-	-
D_1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	$2E$	L	-	-
D_2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	$2E$	L	-	-

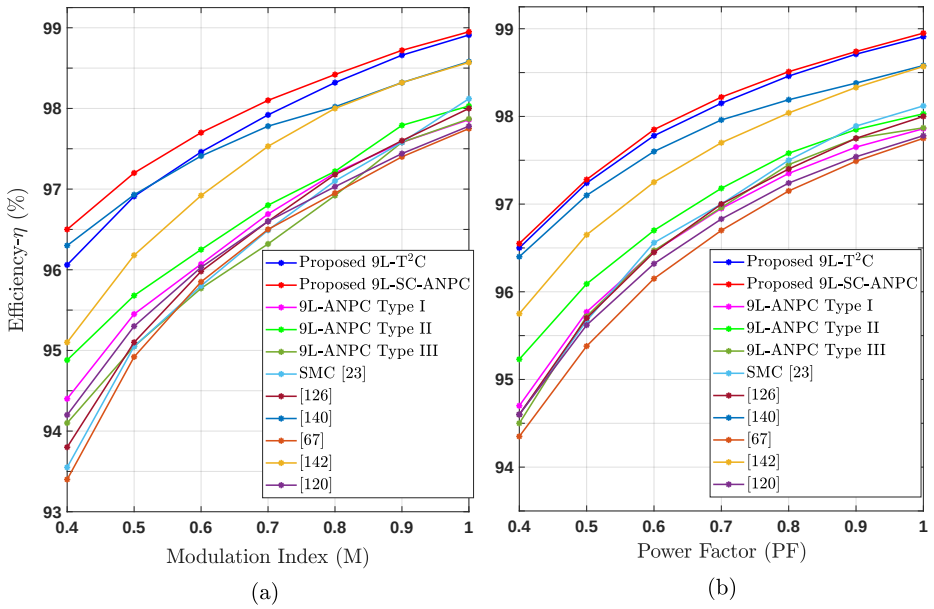
[a]. Switches labels of [67, 120, 126, 140] are different from their original articles.

identical to that in 9L-ANPC variants I and II, and in [67, 126, 140]. The other switches (S_7 to S_{12}) of the three conventional topologies bear voltage stress equal to the voltage level step E. For the 9L-SC-ANPC converter, only S_5 to S_8 exist and bear a voltage stress of $2E$. D_1 and D_2 have a peak inverse voltage (PIV) of $2E$.

It is worth noting that, for all nine-level converters, switches with high voltage stresses are operated at a low switching frequency and switches with low voltage stresses are operated at a high switching frequency, which enhances the switching loss distribution between the switches. S_1 and S_4 in the 9L-SC-ANPC, and S_1 and S_5 in the 9L-T^{2}C are switched at the fundamental frequency f_{line} for a half cycle and operated at sampling frequency f_s only during the transition between V_3 and V_4 as shown in the switching tables (Tables 3.1 and 4.1). S_2 and S_3 are operated at f_{line} for the whole cycle. While the lowest blocking voltage switches S_6, S_7 and S_8 are operated at higher frequency for the whole cycle. It is worth mentioning that for all switches in the proposed 9L-SC-ANPC, 9L-T^{2}C, the maximum voltage change across switches is only $2E$, which has a positive impact on switching loss generation and limits its value per switch to be similar to the conventional topologies. Moreover, the reduced switch count of the 9L-SC-ANPC and 9L-T^{2}C results in lower total switching losses compared to other topologies under consideration.

4.7.4 Number of ON-state switches per level

Conducting power devices directly affect conduction losses and total saturation voltage for each state. For each switching state, all conducting devices carry the same current because only one current path is available. Consequently, for identical switches, the conduction losses can be compared by considering the number of ON-state switches in each level. The average number N_{cond} of ON-state devices for the all nine-level converters is given in Table 4.5. N_{cond} for levels that have redundancies is obtained as the average for those redundant states. For levels that generate higher voltage, i.e. higher current and greater effect on total conduction loss,



(a) (b)

Figure 4.27: Efficiency comparison of the common dc-link nine-level converters: (a) efficiency with modulation index. (b) efficiency with power factor.

N_{cond} is found to be only 2 for $\pm 4E$ and 3 for $\pm 3E$ in the proposed 9L-T^{2}C and 9L-SC-ANPC topologies, which is the least compared to other converters. It should also be noted that N_{cond} in the 9L-SC-ANPC depends on whether the inverter supplies active or reactive power, as described in Section 3.3.3. For active power operation, the 9L-SC-ANPC has an average value of N_{cond} slightly lower than that of the proposed 9L-T^{2}C, while for reactive power operation, both topologies have almost the same value. According to the comparison, it can be concluded that the 9L-T^{2}C and the 9L-SC-ANPC have the lowest N_{cond} and, consequently, the lowest conduction losses compared to the other nine-level converters.

4.7.5 Efficiency Comparison

Power losses and converter efficiency are studied in PLECS environment for all considered topologies for a wide range of M and PF. The analysis are performed at the same parameters for all topologies. Specifically, the parameters used are $V_{\text{dc}} = 1$ kV, $f_c = 3$ kHz, and AC current source with 40-A amplitude (AC load). The estimated efficiency with the change of M at unity PF is shown in Fig. 4.27a, while the efficiency at $M = 1$ and different PF is given in Fig. 4.27b. It is clear that the efficiencies of the proposed 9L-T^{2}C and the 9L-SC-ANPC are the highest under all operating conditions compared to other converters. As can also be observed, the 9L-SC-ANPC inverter has a slightly higher efficiency since it has N_{cond} slightly lower than that of the proposed 9L-T^{2}C, as illustrated in Table 4.5. According to the power loss analysis in PLECS for a 10-kW single-phase structure at f_c = 3 kHz, the efficiency of the 9L-T^{2}C and 9L-SC-ANPC at $M = 1$ and PF = 1 is 98.91% and 98.95%, respectively.

Table 4.7: Cost comparison of nine-level converters for one phase-leg.

Item	Nominal Voltage	Item No. (Package)	Item price*($)	Traditional 9L-ANPC			SMC					
				Type I	Type II	Type III	[23]	[126]	[67]	[120]	**9L-SC-ANPC**	**9L-T^{2}C**
MOSFETS	1200 V	IMW120R045M1 (TO-247)	18.50	-	2	2	-	-	-	-	2	2
	800 V	SPW55N80C3 (TO-247)	15.70	4	2	-	-	4	4	2	2	-
	600 V	IPP60R040C7 (TO-220)	13.70	-	-	2	-	-	-	-	-	-
	500 V	APT56M50L (TO-264)	11.40	-	-	-	8	4	4	8	2	6
		SPI21N50C3 (TO-262)	3.10	-	-	-	-	-	-	-	1	-
	250 V	IRFP4332PBF (TO-247)	5.70	8	8	8	8	4	4	4	2	2
Diode	600 V	IDW50E60 (TO-247)	3.10	-	-	-	-	-	-	-	2	-
Gate drivers	-	HCPL-3120-560E	3.80	12	10	11	16	12	12	14	8	8
Capacitors	500 V	CGS531T500R4L	47.70	1	1	1	2	-	-	-	-	-
	400 V	CGS811T400R4C	42.10	1	1	1	2	2	1	2	-	-
	200 V	DCM162T200EC2A	28.10	1	1	1	2	-	1	1	-	-
	200 V	DCMC742T200DF2B	42.10	-	-	-	-	1	-	-	2	2
Total cost ($)	-	-	-	271.90	269.90	269.70	433.40	303.10	247	310.90	226.50	231.40

*·Prices and part number of the components are referred to https://eu.mouser.com; Unit prices may vary according to market growth and availability.

4.7.6 Cost Comparison

The costs of the considered inverters are calculated for the same case used in the power loss analysis (V_{dc}= 1 kV, nominal power= 10-kW) and are collected in Table 4.7. The voltage ratings of the power switches are determined according to the blocking voltage in Tables 4.5, and 4.6, taking into account a margin of at least 60%. The current ratings are estimated based on the nominal power (10-kW), where all switches have a similar rating except for one low current switch to be used for S_5 in the 9L-SC-ANPC topology, as described in Section 3.3.3. The sizing of the FCs are determined according to their reported formula. It should be mentioned that no data is available about the FCs size for the converters in [140, 142]. Thus, their total costs are not given in Table 4.7. The nominal voltage of the FCs are determined based on their balancing voltage value given in Table 4.5 and the availability in the market, considering a suitable voltage margin. According to Table 4.7, the proposed 9L-T^{2}C and 9L-SC-ANPC have approximately similar costs, lower than other topologies. However, taking into account the FCs sensors, the cost difference compared to other topologies will be more significant.

4.7.7 Case Study: 1-MW wind turbine system

Thanks to the generation of nine levels in the phase voltage (17 levels in line to line voltage), high-quality waveforms are produced, which enables the successful operation of grid-connected DGs while meeting utility criteria of harmonics with low filtering requirements or filterless operation as reported in [67]. For low and medium voltage medium-power grid-connected applications, the reduction or elimination of the filtering requirements significantly reduces the overall cost and improves the efficiency of the power conversion system. A grid-connected 1-MW wind turbine system is considered as a case study to determine the number of components used and their ratings for the three-phase configuration of the proposed and other nine-level inverters under consideration. The system parameters of this case study are; $V_{\text{dc}} = 6.4$ kV, $f_c = 2$ kHz, grid voltage $v_g = 4.16$ kV (line-to-line), and $f_{\text{line}} = 60$ Hz. The required components and their ratings for the considered nine-level inverters are given in Table 4.8. The selection of switches types and ratings is based on various factors, including the blocking voltage of the power device, its switching frequency, and the availability of such components in the market. The adoption of different power devices enables the converter to exploit their individual strengths and opti-

Table 4.8: Required components for different nine-level inverters for 1-MW WT grid-connected system (three-phase configuration).

Topology	Switching devices	Suggested commercial switches	Sustained voltage of FCs	Capacitance relationship	Capacitance at 1-MW	Voltage sensors for FCs
9L-ANPC Variant I	$12 \times 4E$ $24 \times E$	12×5.5 kV (IGCT) 24×1.7 kV (IGBT)	$3 \times 3E$ (2400V) $3 \times 2E$ (1600V) $3 \times E$ (800V)	$\frac{I_p}{V_r \cdot f_c}$	3×0.42 mF 3×0.63 mF 3×1.26 mF	9
9L-ANPC Variant II	$6 \times 5E$ $6 \times 4E$ $24 \times E$	6×6.5 kV (IGCT) 6×5.5 kV (IGCT) 24×1.7 kV (IGBT)	$3 \times 3E$ (2400V) $3 \times 2E$ (1600V) $3 \times E$ (800V)	$\frac{I_p}{V_r \cdot f_c}$	3×0.42 mF 3×0.63 mF 3×1.26 mF	9
9L-ANPC Variant III	$6 \times 5E$ $6 \times 3E$ $24 \times E$	6×6.5 kV (IGCT) 6×5.5 kV (IGCT) 24×1.7 kV (IGBT)	$3 \times 3E$ (2400V) $3 \times 2E$ (1600V) $3 \times E$ (800V)	$\frac{I_p}{V_r \cdot f_c}$	3×0.42 mF 3×0.63 mF 3×1.26 mF	9
SMC [23]	$24 \times 2E$ $24 \times E$	24×3.3 kV (IGCT) 24×1.7 kV (IGBT)	$6 \times 3E$ (2400V) $6 \times 2E$ (1600V) $6 \times E$ (800V)	$\frac{I_p}{V_r \cdot f_c}$	6×0.42 mF 6×0.63 mF 6×1.26 mF	18
[126]	$12 \times 4E$ $12 \times 2E$ $12 \times E$	12×5.5 kV (IGCT) 12×3.3 kV (IGCT) 12×1.7 kV (IGBT)	$6 \times 2E$ (1600V) $3 \times E$ (800V)	$\frac{I_p}{V_r \cdot f_c}$	6×0.63 mF 3×1.26 mF	9
[140]	$12 \times 4E$ $15 \times 2E$	12×5.5 kV (IGCT) 15×3.3 kV (IGBT)	$6 \times E$ (800V)	N/A	N/A	6
[67]	$12 \times 4E$ $12 \times 2E$ $12 \times E$	12×5.5 kV (IGCT) 12×3.3 kV (IGBT) 12×1.7 kV (IGBT)	$3 \times 2E$ (1600V) $3 \times E$ (800V)	$\frac{I_p}{V_r \cdot f_c}$	3×0.63 mF 3×1.26 mF	6
[142]	$6 \times 6E$ $12 \times 2E$ $12 \times E$	6×6.5 kV (IGCT) 12×3.3 kV (IGCT) 12×1.7 kV (IGBT)	$3 \times 2E$ (1600V) $3 \times E$ (800V)	N/A	N/A	6
[120]	$6 \times 4E$ $24 \times 2E$ $12 \times E$	6×5.5 kV (IGCT) 24×3.3 kV (IGBT) 12×1.7 kV (IGBT)	$6 \times 2E$ (1600V) $3 \times E$ (800V)	$\frac{I_p}{V_r \cdot f_c}$	6×0.63 mF 3×1.26 mF	9
9L-SC-ANPC	$6 \times 6E$ $6 \times 4E$ $9 \times 2E$ $6 \times 2E$	6×6.5 kV (IGCT) 6×5.5 kV (IGCT) 9×3.3 kV (IGBT) 6×1.7 kV (IGBT)	$6 \times E$ (800V)	$0.672\frac{I_p}{\omega \cdot V_r}$	6×4.67 mF	3
9L-T^{2}C	$6 \times 6E$ $18 \times 2E$ $6 \times E$	6×6.5 kV (IGCT) 18×3.3 kV (IGBT) 6×1.7 kV (IGBT)	$6 \times E$ (800V)	$0.672\frac{I_p}{\omega \cdot V_r}$	6×4.67 mF	3

mize the cost and size of the converter, which is essential in hybrid structures. Accordingly, integrated gate commutated thyristors (IGCTs) are used for high voltage/current switches with low switching frequency due to their high capabilities and low conduction loss, while insulated gate bipolar transistors (IGBTs) are employed for high switching devices because of their low switching loss. According to Table 4.8, the proposed 9L-SC-ANPC and 9L-T^{2}C have superior performance compared to other topologies in terms of the switches required, the number of FCs and their rated voltages, and the voltage sensors required to balance the FCs. Although the capacitance of FCs is relatively high for the 9L-SC-ANPC and 9L-T^{2}C compared to other topologies, their size and cost are quite acceptable due to their low voltage ratings and number compared to other topologies.

Based on the comparison and performance analysis, the 9L-SC-ANPC and 9L-T^{2}C outperform other common dc-link nine-level converters regarding the required number of active switches, capacitors, FCs voltage ratings, cost, and efficiency. Furthermore, thanks to the developed balancing algorithm, the FCs are stabilized at their reference using a single voltage

sensor in steady-state and dynamic operation, resulting in further reduction in the system cost. Although the capacitance of the FCs in the proposed topologies is relatively large, the volume and cost are still quite acceptable due to their reduced voltage rating compared to most other topologies.

Although the proposed 9L-SC-ANPC and 9L-T^{2}C have different configurations with different numbers and ratings of power devices (active switches and diodes), they have the same number of switching states and their operation is somewhat similar. The 9L-SC-ANPC has a fewer number of switches and slightly better efficiency, however, the 9L-T^{2}C has a lower TSV, as shown in Table 4.5. Also, a salient feature of the 9L-T^{2}C is that it can be easily configured with the commercially available PEBBs, which is desirable from an industry perspective to reduces engineering efforts, testing times, volume, and costs [173].

4.8 Summary

A new nine-level T-type converter has been presented in this chapter with a reduced number of power electronic components. The proposed 9L-T^{2}C can be configured using the commercially available 3L-T^{2}C with two LFSs per phase-leg. Based on the comprehensive comparison performed, the 9L-SC-ANPC and 9L-T^{2}C outperform other common dc-link nine-level converters in terms of the required number of active switches and capacitors, FCs voltage ratings, and efficiency. The dc-link and FCs balancing has been included into the PD-PWM, eliminating the need for an additional controller. The proposed 9L-T^{2}C with the balancing algorithm has been validated for stand-alone and grid-connected operation under different operating conditions through simulation and experimental implementation. A detailed comparison has been conducted. A grid-connected 1-MW wind turbine system is considered as a case study to determine the number of components used and their ratings for the three-phase configuration of the proposed and other nine-level inverters under consideration.

Part II

Model Predictive Control of Hybrid Multilevel Inverters

CHAPTER 5

Model Predictive Control of Multilevel Inverters: Challenges, Recent Advances, and Trends

This chapter provides a detailed overview of the latest advancements reported in the literature for tackling the challenges associated with model predictive control (MPC) in the context of MLI applications. Moreover, some of the important concepts are validated by the experimental implementation and compared with the standard MPC method. This review is organized as follows. Section 5.2 describes the design steps of the finite-control-set MPC (FCS-MPC), considering the grid-connected 5L-ANPC converter as a case study. The importance of each FCS-MPC challenge and the reported effective solutions are provided in Section 5.3. Section 5.4 deals with other popular direct MPC methods, such as Lybanuv-based MPC. Indirect MPC methods for MLIs, including continuous-control-set MPC (CCS-MPC) and deadbeat MPC (DB-MPC), are covered in Section 5.5. A qualitative comparison between the common MPC methods for MLIs is presented in Section 5.6. Finally, the summary is provided in Section 5.7.

5.1 Introduction

MPC has emerged as a promising control method in power electronics, particularly for multi-objective control problems such as MLI applications. In general, any MPC scheme has three key phases, namely the prediction model, cost function, and optimization method. Each phase has relevant issues and limitations that represent research points in the academic community. In this regard, several works have recently been proposed for MLIs applications. Accordingly, and considering the most common MPC methods for MLIs in Fig. 1.5, this chapter aims to discuss the current state of MPC strategies for MLI applications. Through this review, the MPC methods are categorized into two groups, direct MPC (without modulator) and indirect MPC (with modulator). The recent advances of each category are presented and analyzed, focusing on direct MPC as the most applied method for MLI topologies.

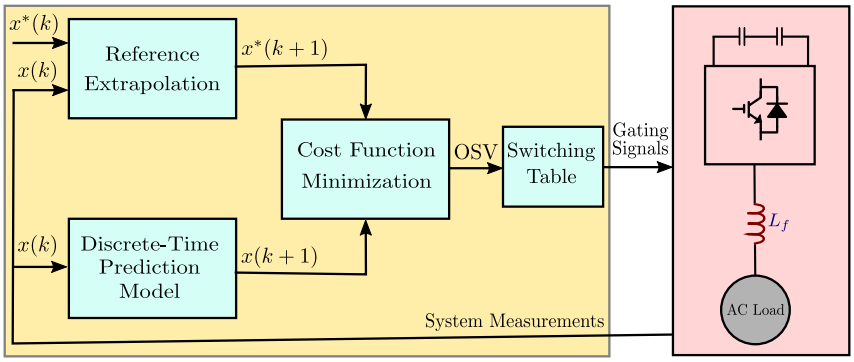


Figure 5.1: Block diagram of standard FCS-MPC.

5.2 Finite control set MPC

Figure 5.1 shows the block diagram of the standard FCS-MPC strategy with a short prediction horizon ($N_p = 1$). The design and operating principles can be summarized in three steps as follows;

1. Constructing a discrete-time prediction model;
2. Design the cost function that includes the control objectives and constraints; and
3. Define and apply the optimal vector that has a minimal cost function through the optimization algorithm.

The analysis presented here is based on the 5L-ANPC inverter connected to the grid, as shown in Fig. 5.2. Besides the primary current tracking objective, FCs balancing and NP potential control are two control targets that need to be considered in the 5L-ANPC inverter. The description and operating principles of the considered case study are presented in [174].

5.2.1 Discrete-time prediction model

The predictive model is considered the core of MPC strategies as it is required to predict the future values of the controlled variable. In addition, the prediction accuracy is an important issue that significantly affects the control performance. Therefore, a time-continuous system model that fully includes the system dynamics should be first built.

Referring to the system shown in Fig. 5.2, the switching states of one leg of the 5L-ANPC inverter are listed in Table 5.1. $x \in \{a, b, c\}$ denotes the respective phase, and the switching function s_{ix} ($i = \{1, 2, 3, 4\}$) of switch S_{ix} is defined as

$$s_{ix} = \begin{cases} 1, & \text{if } S_{ix} \text{ is ON} \\ 0, & \text{if } S_{ix} \text{ is OFF.} \end{cases} \tag{5.1}$$

According to the inverter switching states, the inverter phase-to-neutral voltage v_{xN} can be expressed as

$$v_{xN} = s_{1x}s_{3x}v_{c1} - \bar{s}_{2x}\bar{s}_{3x}v_{c2} + (s_{4x} - s_{3x})v_{fx}, \tag{5.2}$$

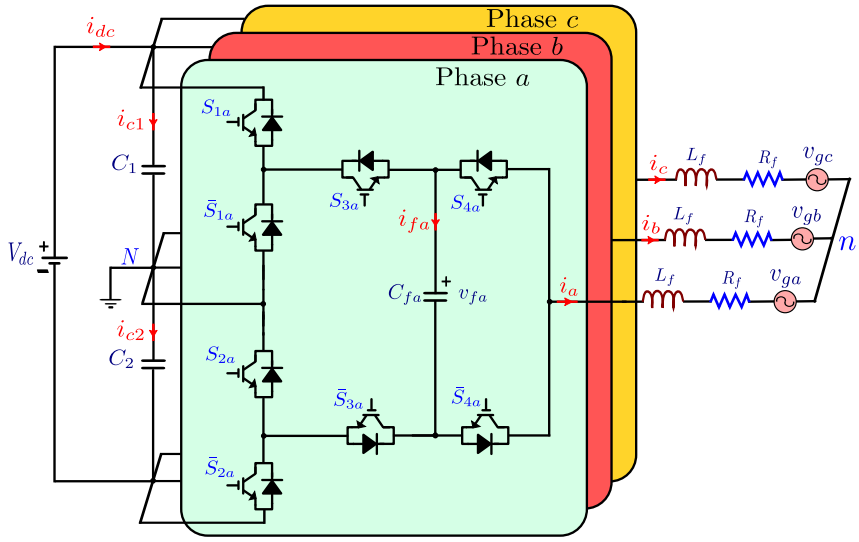


Figure 5.2: Circuit configuration of the grid-connected 5L-ANPC converter.

where v_{c1} and v_{c2} are the dc-link voltages, and v_{fx} is the voltage of the phase capacitor C_{fx}. The dynamic system equations of the three-phase grid-connected system in the abc-frame are expressed as

$$v_{xN} = Ri_x + L\frac{d}{dt}i_x + v_{gx} + v_{nN}, \tag{5.3}$$

where R_f and L_f are the resistance and inductance of the filter, respectively. v_{gx} is the grid voltage and v_{nN} refers to the common-mode voltage. To decouple the control loops, the three-phase system is preferably modeled in a two-dimensional frame, either stationary $\alpha\beta$-frame or rotating dq-frame. In doing so, $\mathbf{x}_{abc} = [x_a\ x_b\ x_c]^T$ is transformed to the $\alpha\beta$-frame as

$$\mathbf{x}_{\alpha\beta} = \mathbf{K}\mathbf{x}_{abc}, \tag{5.4}$$

where $\mathbf{K}$ is the transformation matrix and expressed as

$$\mathbf{K} = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix}. \tag{5.5}$$

Accordingly, the continuous-time model in (5.3) can be written in the $\alpha\beta$-frame as

$$\mathbf{v} = R\mathbf{i} + L\frac{d}{dt}\mathbf{i} + \mathbf{v}_g, \tag{5.6}$$

where $\mathbf{v} = [v_\alpha\ v_\beta]$, $\mathbf{i} = [i_\alpha\ i_\beta]$, and $\mathbf{v}_g = [v_{g\alpha}\ v_{g\beta}]$.

The model of the phase flying capacitor (FC) (C_{fx}) is built based on the inverter states in Table 5.1 as

$$i_{fx} = C_{fx}\frac{d}{dt}v_{fx} = (s_{3x} - s_{4x})i_x, \tag{5.7}$$

where i_{fx} is the current of C_{fx}. Similarly, the dc-link capacitors C_1 and C_2 are modeled as

$$\left.\begin{aligned} i_{c1} &= C_1\tfrac{d}{dt}v_{c1} = i_{dc} - \sum_{x\in\{a,b,c\}} s_{1x}s_{3x}i_x, \\ i_{c2} &= C_2\tfrac{d}{dt}v_{c2} = i_{dc} + \sum_{x\in\{a,b,c\}} \bar{s}_{2x}\bar{s}_{3x}i_x, \end{aligned}\right\} \tag{5.8}$$

Table 5.1: Switching states of phase x of the 5L-ANPC inverter.

State	s_{1x}/s_{2x}	s_{3x}	s_{4x}	v_{xN}	i_{fx}
V_1	1	1	1	$V_{dc}/2$	0
V_2	1	1	0	$V_{dc}/4$	i_x
V_3	1	0	1	$V_{dc}/4$	-i_x
V_4	1	0	0	0	0
V_5	0	1	1	0	0
V_6	0	1	0	$-V_{dc}/4$	i_x
V_7	0	0	1	$-V_{dc}/4$	-i_x
V_8	0	0	0	$-V_{dc}/2$	0

where i_{c1} and i_{c2} are the currents of C_1 and C_2, respectively. For identical dc-link capacitors ($C_1 = C_2 = C$), the dc-link balancing can be formulated as

$$\Delta i_c = C\frac{d}{dt}\Delta v_c = -\sum_{x\in\{a,b,c\}} (s_{1x}s_{3x} + \bar{s}_{2x}\bar{s}_{3x})i_x, \tag{5.9}$$

where $\Delta i_c = i_{c1} - i_{c2}$ and $\Delta v_c = v_{c1} - v_{c2}$.

As previously mentioned, the MPC implementation is based on the discrete-time models. Therefore, after constructing the continuous-time models, a discretization method should be applied. For the discretization procedure, two important aspects should be taken into account [175, Chapter 7]. First, the computational load should be low so as not to add heavy computations to the MPC algorithm. Second, errors resulting from the discretization procedure should be acceptable in order not to negatively affect the modeling accuracy, since the MPC performance is significantly affected by the accuracy of the discrete-time model. Choosing the appropriate discretization can be seen as a trade-off between the first and second aspects, based on the application and control design requirements [38]. In this regard, the discretization methods are divided into three categories: exact, quasi-exact, and approximated methods [176] [175, Chapter 7], as shown in Fig. 5.3. The approximated methods are the most applied in power electronic systems in general and MLIs applications in particular due to their simplicity, straightforward implementation, and low calculation load [177–180].

Forward-Euler, backward-Euler, and bilinear- also known as Tustin- approximations are three common methods that belong to the approximated family, as shown in Fig. 5.3. Table 5.2 shows the derivative approximation using these methods, where T_s is the sample period.

By applying forward-Euler approximation to the system models in (5.6), (5.7), and (5.9), the predicted values $\mathbf{i}(k+1)$, $v_{fx}(k+1)$, and $\Delta v_c(k+1)$ are obtained as

$$\left.\begin{aligned}
&\mathbf{i}(k+1) = (1 - \tfrac{RT_s}{L})\mathbf{i}(k) + \tfrac{T_s}{L}(\mathbf{v}(k) - \mathbf{v}_g(k)),\\
&v_{fx}(k+1) = v_{fx}(k) + \tfrac{T_s}{C_{fx}}(s_{3x} - s_{4x})i_x,\\
&\Delta v_c(k+1) = \Delta v_c(k) - \tfrac{T_s}{C}\sum_{x\in\{a,b,c\}} (s_{1x}s_{3x} + \bar{s}_{2x}\bar{s}_{3x})i_x.
\end{aligned}\right\} \tag{5.10}$$

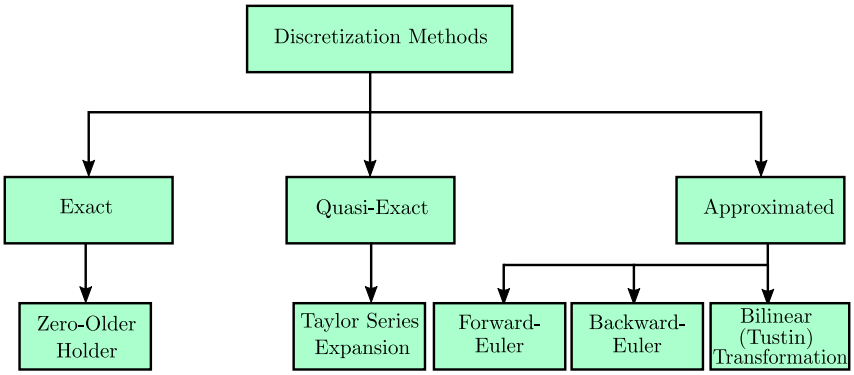


Figure 5.3: Classification discretization methods for MPC.

Table 5.2: Approximated discretization methods.

Method	Formulation
Forward-Euler	$\frac{d}{dt}x(t) = \frac{x(k+1)-x(k)}{T_s}$
Backward-Euler	$\frac{d}{dt}x(t) = \frac{x(k)-x(k-1)}{T_s}$
Bilinear (Tustin)	$\frac{d}{dt}x(t) = \frac{x(k+1)-x(k-1)}{2T_s}$

5.2.2 Cost function formulation

The cost function formulates the MPC optimization problem including all control objectives and, thus, it defines the desired control behavior. The design of the cost function is a challenging task, especially in the multiple objective problems typical in MLIs applications. The issues related to the cost function such as norm, as well as the tuning of the weighting factors, are important research points because of their impact on the performance and stability of the whole system.

The selection of the norm (l) significantly affects the operation of the FCS-MPC [181, 182]. The l_1-norm refers to the sum of absolute values, while the l_2-norm refers to the sum of squared values. Regarding the computational efforts, the l_1-norm requires lower calculations. However, research conducted in [181] showed that the use of l_1-norm can lead to a decrease in performance and closed-loop instability issues. The study found that the FCS-MPC algorithm with the l_1-norm fails to maintain stability during low switching frequency operations, which is an important requirement in high-power high-voltage motor drives, one of the primary applications of MLI topologies. The l_2-norm transforms the optimization problem into a quadratic problem, and the solution to the unconstrained problem can be found by setting the derivative of the cost function to zero, enabling the use of both FCS-MPC with implicit modulator and indirect MPC [176]. For this reason, it is recommended to use the l_2-norm to ensure closed-loop stability, a wide range of switching frequency operations, and low distortion. The design of weighting factors for MLI applications is thoroughly covered in Section 5.3.2

The variables included in the cost function are determined by the MLI topology and the application under consideration. Accordingly, they can be divided into two groups; topology-

related objectives and application-related objectives, as shown in Fig. 1.4.

For the considered case study in Fig 5.2, the dc-link balancing and FC voltage control need to be included to ensure proper operation of the inverter. In addition, current control is considered as an application-related objective. By adopting the l_2-norm, the cost function g can be expressed as

$$g = [\mathbf{i}^*(k+1) - \mathbf{i}(k+1)]^2 + \lambda_1[v^*_{fx}(k+1) - v_{fx}(k+1)]^2 + \lambda_2[\Delta v_c(k+1)]^2, \tag{5.11}$$

where λ_1 and λ_2 are the weighting factors and used to adjust the priority among the control targets. Weighting factors have a great influence on control behaviour and stability. Thus, much research effort has been put into tuning or even eliminating weighting factors, as discussed in Section 5.3.2. $\mathbf{i}^*(k+1)$ in (5.11) is the reference current at $(k+1)^{th}$ sample and is determined by extrapolation methods.

Extrapolation of reference variables is necessary to avoid the delay between the reference and the actual variable, especially when the sampling frequency is not significantly higher than the fundamental frequency. No extrapolation procedure is required in the steady-state operation when the MPC algorithm is designed in the dq-frame as the variables are DC values. However, when the references change, as in transient conditions, a delay arises, bringing the need for an extrapolation method. In this regard, three extrapolation methods are reported, namely discrete-signal generator [175], vector angle extrapolation [175, 177] and Lagrange extrapolation [35, 177, 183]. Discrete-signal generator method is only used when the reference is determined by the user. The other two methods are used when the references are obtained from other control loops. In vector angle extrapolation, the variables must be in polar coordinates form ($re^{j\theta}$), and then a discrete value $N_p\omega T_s$ is added to the angle θ to get the future value, where N_p and ω are the prediction horizon and variable angular frequency, respectively. Since this method is implemented in polar coordinates, it is only applicable to three-phase sinusoidal variables. Lagrange extrapolation is the most commonly used method in MPC because it can be used in single-phase systems and non-sinusoidal quantities. It uses the present and past samples to predict the future value without involving any phase angle calculations. The number of the past samples defines the order of the extrapolation [184]. Adopting a third-order Lagrange extrapolation, $\mathbf{i}^*(k+1)$ in (5.11) is obtained as

$$\mathbf{i}^*(k+1) = 4\mathbf{i}^*(k) - 6\mathbf{i}^*(k-1) + 4\mathbf{i}^*(k-2) - \mathbf{i}^*(k-3). \tag{5.12}$$

5.2.3 Optimal vector identification through the optimization algorithm

Once the discrete-time model is constructed and the optimization problem is formulated via a cost function, an optimization algorithm is applied to identify the optimal control action. Typically, an exhaustive search algorithm (ESA) is used to solve the optimization problem by checking all converter states to find the optimal one. However, in MLI applications, the large number of states leads to a heavy computational burden, resulting in a long sampling period to be used as the optimization problem is solved online. On the other side, in power converter applications, the sample period tends to be short, on the order of tens of microseconds, for high control performance. Accordingly, much effort has been focused on investigating other optimization algorithms, as discussed in Section 5.3.1. With long horizon FCS-MPC, this issue is

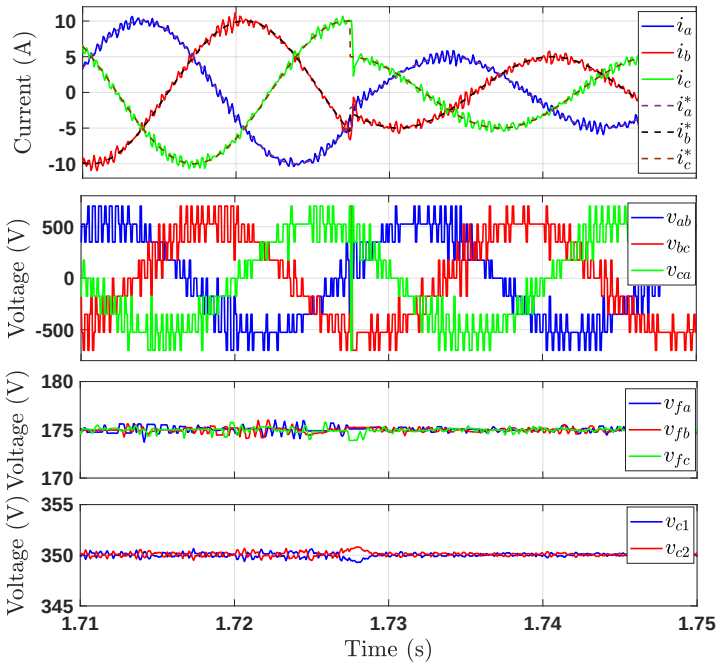


Figure 5.4: HIL results of standard FCS-MPC.

more apparent and, hence, other optimization algorithms are used such as sphere decoding algorithm (SDA) [185]. More details about the implementation of long-horizon MPC are provided in Section 5.3.4.

For the 5L-ANPC inverter, each phase has 8 switching states, as shown in Table 5.1, which means 512 (8^3) states in the three-phase implementation. With the conventional FCS-MPC concept using ESA and a horizon of one, it is required to carry out 512 $\times$ predictions for the controlled variables according to (5.10) and 512 $\times$ cost function evaluation according to (5.11) per each control sampling period T_s. Note that the number of calculations increases exponentially as the prediction horizon increases.

The implementation of the conventional FCS-MPC for the case study considered in Fig. 5.2 is verified by a hardware-in-the-loop (HIL) implementation. The system parameters are given in Table 5.3. Fig. 5.4 shows the HIL results for a step-change in the reference current from 10 A to 5 A. As it is clear, the three control objectives considered in the cost function are well achieved. The grid currents follow the reference with high dynamic performance. The FCs C_{fa}, C_{fb}, and C_{fc} are stabilized at its reference $V_{dc}/4 = 175$ V. In addition, the voltages of the dc-link capacitors are well balanced.

A review of recent advancements in FCS-MPC for MLIs shows that a majority of the published studies focus on addressing one or more of the following challenges;

1. Computational burden reduction;
2. Weighting factors design or elimination;
3. Fixed switching frequency operation; and
4. Long horizon MPC.

Table 5.3: System parameters of the HIL implementation.

Parameter	Value
dc-link, V_{dc}	700 V
Grid voltage, $v_{g,l-l}$	380 V (rms)
Grid frequency, f_f	50 Hz
Filter resistance, R_f	0.1 Ω
Filter inductance, L_f	10 mH
dc-link capacitors, C_1 and C_2	2000 μF
FC, C_f	1000 μF
Sampling time, T_s	100 μs

The advances and improvements related to these issues are discussed in the following section.

5.3 FCS-MPC: challenges and recent advances

5.3.1 Computational Burden Reduction

In FCS-MPC, the optimization problem needs to be solved online. In the case of MLIs in particular, this leads to a high computational load due to the large number of converter states, necessitating the use of a long sampling period, which is undesirable in power electronics applications. Several solutions have been presented to reduce the computational load to realize a successful practical implementation using the standard digital platforms.

Many works have been proposed to reduce the complexity of FCS-MPC for three-phase MLIs. The first attempt was reported in [186] for the 5L-CHB inverter. In this work, the reduction of the computational load is realized in two steps. First, by eliminating the redundant states that produce high common-mode voltages, reducing converter states from 125 to 61 switching states. Second, assuming that the optimal voltage vector is adjacent to that previously applied, only seven vectors are evaluated in each sample. Accordingly, for each different vector, a list of the closest seven vectors is defined off-line and stored in a database. Despite the reduction of the online calculations and acceptable steady-state performance, this method suffers from poor dynamic performance and requires significant memory space to store the LUTs.

An interesting approach was presented in [187], where the current control objective is represented by the converter voltage in the cost function. For illustration, the cost function in (5.11) is rewritten as

$$g = [\mathbf{v}^*(k) - \mathbf{v}(k)]^2 + \lambda_1[v^*_{fx}(k+1) - v_{fx}(k+1)]^2 + \lambda_2[\Delta v_c(k+1)]^2, \tag{5.13}$$

where the reference voltage $\mathbf{v}^*(k)$ is calculated from the system model using the deadbeat concept. Taking the grid-connected system in Fig. 5.2 as an example, $\mathbf{v}^*(k)$ is obtained as

$$\mathbf{v}^*(k) = R\mathbf{i}(k) + L\frac{\mathbf{i}^*(k+1) - \mathbf{i}(k)}{T_s} + \mathbf{v}_g(k). \tag{5.14}$$

This method replaces the computational burden of current predictions with only one voltage reference estimation, hence it is called single-predictive FCS-MPC. Considering the 5L ANPC

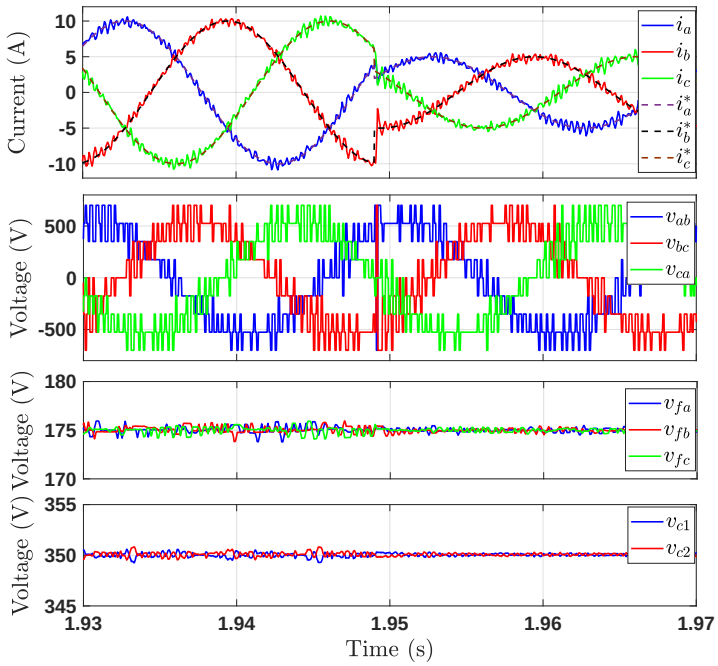


Figure 5.5: HIL results of voltage vector-based FCS-MPC.

inverter, the single-predictive FCS-MPC saves $512\times$ current predictions by estimating $\mathbf{v}^*(k)$ according to (5.14) only once per sample. However, the predictions of the other variables (e.g. FCs and dc-link voltages) are still required for all converter states. This concept has been the basis for several developed low-complexity FCS-MPC methods. These FCS-MPC methods which are based on reference voltage estimation are also referred to as voltage-based FCS-MPC because the cost function is expressed by a voltage as given in (5.13) rather than the current in the traditional method [188]. The HIL results of the voltage-based FCS-MPC for the grid-connected 5L-ANPC converter are shown in Fig. 5.5. The implementation is carried out with the same system parameters in Table 5.3. As can be observed, the results are very similar to those of the standard FCS-MPC in Fig. 5.4, demonstrating the ability of the voltage-based FCS-MPC to identify the optimal state as in the standard method.

The computing effort has been further reduced in [187] by dividing the space vector (SV) diagram into six sectors and only evaluating the vectors of one sector based on the reference voltage location. In [188], the SV diagram of the 5L-CHB inverter is divided into 96 triangle regions. After calculating $\mathbf{v}^*$, one triangle is located based on the magnitude and angle of $\mathbf{v}^*$. Although the evaluated vectors are reduced to three, many calculations are performed offline and stored in LUTs tables, which requires a large storage space. The authors in [189] reduced the number of evaluated vectors from 27 to only 3 for the 3L T-type inverter by dividing the SV diagram into 24 triangular regions. Moreover, dc-link balancing is realized by exploiting the redundant states without the need for capacitor voltage predictions or weighting factors. However, determining the appropriate triangle is not an easy task and requires storage for LUTs. An S-algorithm is proposed in [190] to locate the closest vector to the reference voltage for the 3L-NPC converter. In this method, three imaginary axes denoted as S_1, S_2 and S_3 are added to the SV diagram and the coordinates of the reference voltage with respect to these axes are determined using analytical formulations. Once the reference voltage positions are

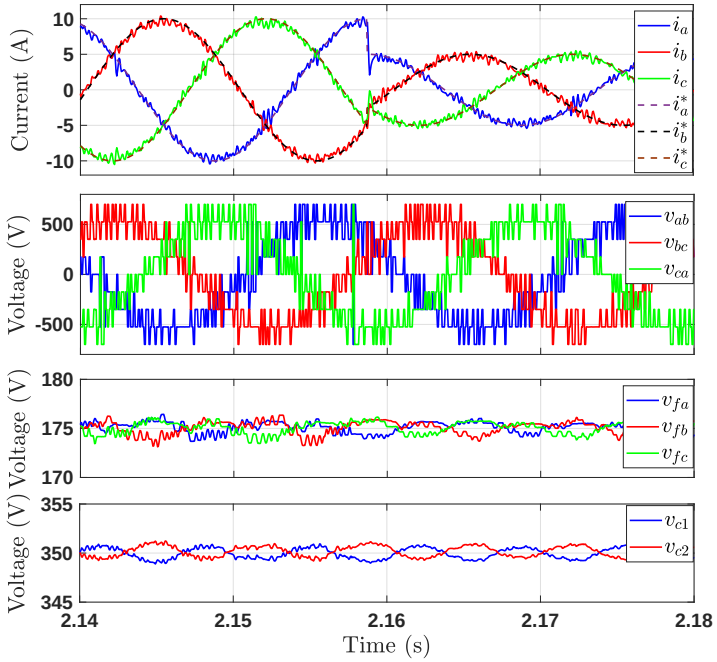


Figure 5.6: HIL results of approximated model-based FCS-MPC.

identified, the optimal vector can be located. The S-algorithm can be applied to higher-level topologies. However, the other control objectives such as dc-link and FCs balancing can only be achieved using the redundant states, which is a limitation for MLI topologies with an insufficient number of redundant states. Voltage-based FCS-MPC has been the basis for other developed computationally efficient algorithms for various MLI topologies [191–195].

Another reduction concept of the FCS-MPC for three-phase MLIs is reported in [196]. The idea of this work is to neglect the correlation between the control objectives of the three phases. Considering the system model in (5.3), the CMV is assumed to be zero $V_{nN} = 0$, resulting in

$$v_{xN} \approx Ri_x + L\frac{d}{dt}i_x + v_{gx}, \tag{5.15}$$

With this approximation, the variables of each phase are controlled independently, reducing the total number of converter states from N_{st}^3 to $3 \times N_{st}$, where N_{st} is the number of switching states of the single-phase leg. However, all redundant states resulting from the correlation of the three phases are ignored, which negatively affects the control performance. Applying this model-approximated FCS-MPC to the 5L-ANPC in Fig. 5.2, the number of evaluated converter states is reduced from 512 to 24. The results of the approximated-model FCS-MPC are depicted in Fig. 5.6. Despite the reduction in computation, the control performance has been degraded compared to the standard FCS-MPC in Fig. 5.4. Lower tracking quality and higher voltage ripples in the FCs and dc-link are observed in this method. This is due to the approximation in the system model, which led to ignoring the redundancies of the three-phase converter.

To compare the calculation load, six prior-art methods are implemented on dSPACE Microlabbox for the grid-connected 5L-ANPC converter. The implemented methods are the conventional scheme, single-predictive and six-sector FCS-MPC methods presented in [187], computationally efficient FCS-MPC presented in [188], S-algorithm method reported in [190] and

Table 5.4: Execution time of reduced-computational burden FCS-MPC schemes on dSPACE Microlabbox.

Method	MPC Algorithm	Total Time
Conventional FCS-MPC	16 µs	35 µs
Single-predictive FCS-MPC	14.5 µs	33.4 µs
Six-sector FCS-MPC	4.12 µs	23 µs
Computationally-efficient FCS-MPC	1.22 µs	20.2 µs
S-Algorithm FCS-MPC	1.15 µs	20.14 µs
Model-approximated FCS-MPC	1.08 µs	20 µs

model-approximated FCS-MPC proposed in [196]. The execution times are measured from ControlDesk software using a *turnaround* variable. Table 5.4 lists the execution times required for the implemented methods, demonstrating the feasibility of computation reduction.

For the single-phase MLIs, only few works have been presented in the literature. In [197], the computational effort of the single-phase 3L-NPC converter has been reduced by avoiding the cost function evaluation. However, in contrast to the standard FCS-MPC, complex analyzes are performed to solve the optimization issue. Additionally, NP balancing is not included in the MPC method, thus, a PID controller is utilized, which complicates the overall control and inserts the issue of PI tuning. A computationally-efficient FCS-MPC for a 4L hybrid H-bridge MLI is presented in [50]. In this approach, only 16 states are evaluated instead of 64 vectors of the standard MPC. However, neglecting 48 states caused the MLI to lose one of its features, the high number of redundancies, that can be exploited to realize better FCs balance or to minimize the switching frequency. Additionally, due to redundancy elimination, two power switches do not carry current with this MPC method, which adversely affects the loss sharing between the power devices. Other computationally efficient FCS-MPC methods have been proposed for single-phase MLIs in [198, 199].

5.3.2 Weighting factors design or elimination

Weighting factors (WFs) directly influence the control performance, particularly in MLIs, where multiple control objectives need to be addressed. Several approaches have been proposed to design WFs, which can be categorized into three categories, as depicted in Fig. 5.7.

5.3.2.1 Weighting Factors Optimization

The optimization of WFs is a very challenging task for cost functions with multiple objectives that are in conflict or cannot be unified. Several approaches have been proposed for tuning the WFs of FCS-MPC [200–206].

The WFs optimization mainly utilizes the heuristic algorithm [200–202] and artificial neural network (ANN) [203–205] to search the global optimal WFs for the cost function of FCS-MPC. The concept of heuristic method for searching the optimal WFs of FCS-MPC is presented in Fig. 5.8. The heuristic methods such as genetic algorithm (GA) [200, 201] and particle swarm optimization (PSO) [202] are employed to find the optimal combination of WFs ($\lambda_1 \cdots$

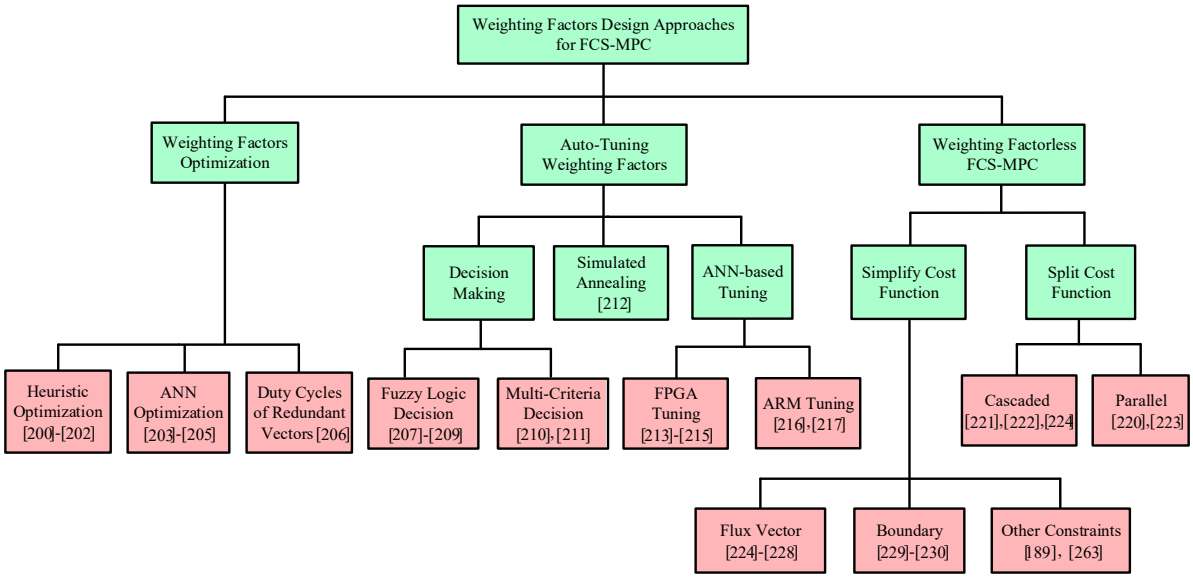


Figure 5.7: Classification of weighting factors design for FCS-MPC.

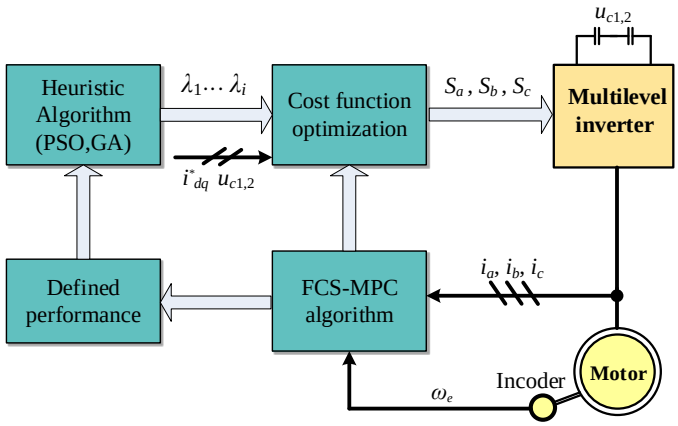


Figure 5.8: Concept of heuristic algorithm for optimizing weighting factors.

λ_i), according to the predefined performance. The heuristic optimization can accurately find the optimal WFs of FCS-MPC for achieving the defined performance. As for ANN based optimization, Fig. 5.9 depicts the block diagram of ANN optimization for the WFs. In Fig. 5.9, the ANN based method firstly generates the dataset from simulations. Then, the dataset is classified into training set and validation set to train and evaluate ANN. After ANN is trained, it is applied to predict the WFs according to the corresponding performance metrics.

In summary, the off-line optimization of WFs neither imposes the computation burden nor deteriorates the dynamic performance of FCS-MPC. However, those approaches fail to be robust to the system parameters mismatch and the WFs should be manually adjusted instead of automatically tuning.

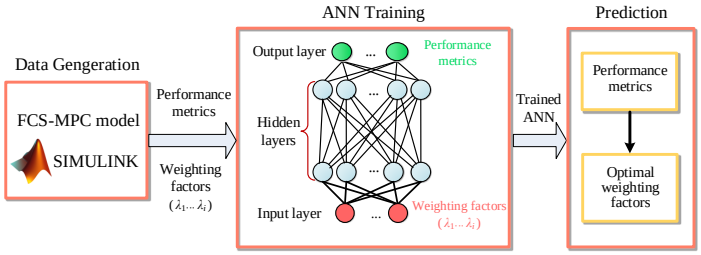


Figure 5.9: Block diagram of ANN optimization for the weighting factors.

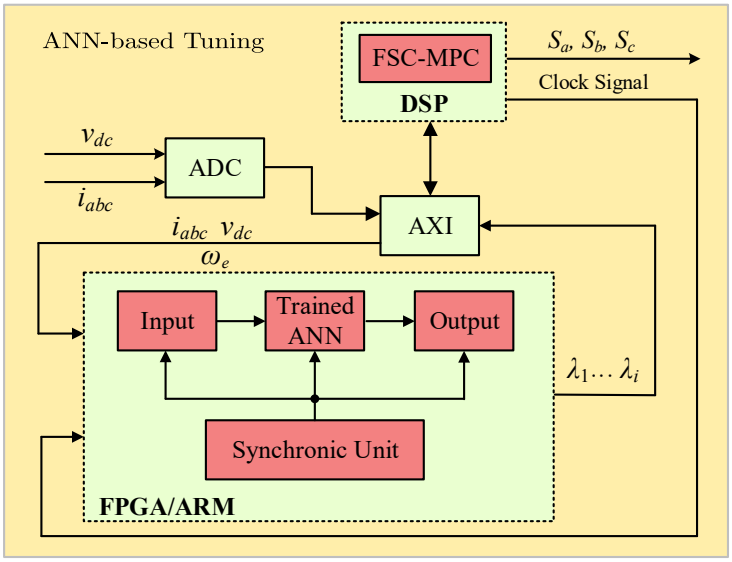


Figure 5.10: Procedure of ANN-based tuning of weighting factors.

5.3.2.2 Auto-Tuning Weighting Factors

With respect to the auto-turning of WFs, it is mainly realized by decision making [207–211], simulated annealing [212] and ANN-based tuning [213–217].

Both the fuzzy logic decision making [208, 209] and multi-criteria decision [210, 211] can be employed to replace the standard selection stage of the cost function. As a result, the WF selection is avoided, and a simple selection scheme is obtained. The fuzzy logic decision making is designed to be the switching state selector for FCS-MPC in induction motor drives [207, 209] and direct matrix converter [208]. Besides, the fuzzy logic decision making can promote the design of the FCS-MPC state selector to be feasible for MLIs. The decision making avoids the WFs selection and it is much suitable for MLI systems. Nevertheless, it increases the computation demand and fails to tackle the problem of preference absence among the criteria of decision making.

The intelligent algorithm simulated annealing in [212] is implemented into an FPGA and searches the optimal combination of WFs to minimize the cost functions. The process of ANN-based auto-turning is presented in Fig. 5.10. The information of sensors (V_{dc}, i_{abc} and ω_e) is transmitted into the input layer of the trained ANN in FPGA/ARM, where the ANN is trained by simulation data. Then, the ANN outputs the WFs for FCS-MPC and the clock signal is

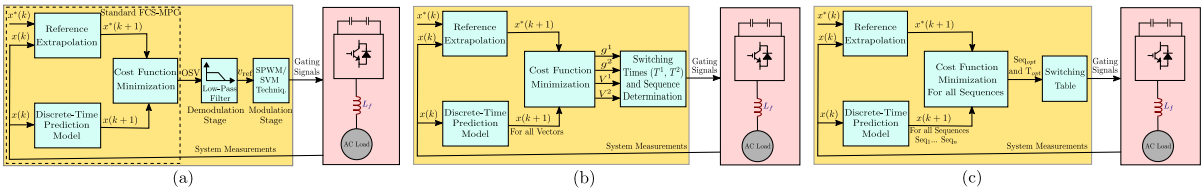


Figure 5.11: Most common FCS-MPC methods with fixed switching frequency: (a) Hybrid FCS-MPC [218], (b) Modulated MPC [52] and (c) Optimal Switching Sequence MPC [219].

transmitted into the synchronic unit to update the trained ANN, where the AXI is the agreement of control bus. Through the ANN-based tuning of WFs, FCS-MPC achieved the robust controlling for a DC-DC boost converter [213], low switching frequency for modular multilevel converter [214], constant switching of better dynamical response for 2L voltage source inverters [215], better dynamic response for 3L-NPC inverter [216] and better reliability for 7L modified packed U-cell (MPUC) active rectifier [217].

In conclusion, the auto-tuning of WFs via intelligent algorithm not only avoids the WFs selection but also enhances the control performance of FCS-MPC. It should be mentioned that the performance of intelligent algorithm is limited to the logic resources of FPGA/ARM.

5.3.2.3 Weighting Factorless FCS-MPC

Since the tuning of WFs is quite cumbersome, the weighting factorless MPC becomes a very attractive solution. The reported methods to avoid the use of WFs can be roughly categorized as split the cost function and simplify the cost function.

Split the cost function is quite intuitive and easy for implementation, where the control objectives are optimized with independent cost functions. Split the cost function is frequently adopted for predictive torque control to eliminate the flux weights, as seen in [220–223]. The cost function for torque and flux magnitude were processed in sequential or by parallel. However, this method may lead the algorithm to be even complex, and it should take care that improper design will deteriorate the performance compared to the FCS-MPC with original cost function [182]. In [224], a cascaded MPC method was proposed for 3L-ANPC inverter drives. In this method, the reference tracking, neutral point potential balance and the losses distribution were achieved in sequential, and each stage adopts an independent cost function without WF.

Simplify the cost function usually adopts the extra constraints based on the specific optimization targets to reduce the terms. For predictive torque control, the most common way is to convert the tracking for torque and flux magnitude into the stator flux vector tracking, which can be quite similar to the predictive current control [224–228]. To achieve the multiple control objectives without WFs, the boundary-based method can be a very effective way. In [229,230], the trajectories of torque, flux magnitude and neutral point potential are extrapolated with a set of input sequences. The candidate voltage vector sequences can maintain three control objectives within their boundaries for the given prediction horizon, separately. Then, the cost function only needs to penalize the commutation times, and the sequence with the lowest switch transition is selected. Thus, the low switching frequency operation can be achieved simultaneously.

5.3.3 Fixed switching frequency MPC

One of the main features of FCS-MPC is that it does not use a modulator to generate the switching pulses for MLIs. This results in a high dynamic performance on one side and, on the other side, a degraded performance in steady-state compared to PWM-based methods. Because in FCS-MPC, only one vector is applied during the whole control period T_s, producing higher ripples in the waveform. Due to the variable switching frequency, FCS-MPC produces a wide harmonic spectrum [231] and, as a result, complicates the filter design.

An early solution to the variable switching frequency issue is the hybrid FCS-MPC (HFCS-MPC) [218]. This technique uses a low-pass filter as a demodulation stage after the standard FCS-MPC to remove the high-frequency components, as shown in Fig. 5.11a. Then, the output of the low-pass filter is modulated by a SPWM or SVM modulation stage. This approach is intuitive and practical and does not increase the computational load. However, the dynamic and steady-state performance is degraded compared to the standard FCS-MPC. In addition, it necessitates the use of an external modulator.

Another effective approach for this matter is the modulated MPC (M2PC) [52], Fig. 5.11b. This method simulates the behaviour of the PWM technique by introducing the concept of variable switching time and applying two vectors (or more) during the control cycle T_s. The implementation of the M2PC for MLIs was first presented in [52] for a 7L-CHB converter. The duration times of the vectors are determined to be inversely proportional to their corresponding cost function values. M2PC has been applied to different MLI topologies in different applications, such as NPC converter in grid-connected applications [232] and CHB converter in STATCOM [233]. Another method is the model predictive pulse pattern control (MP3C). This method is used to reduce harmonic distortion or remove specified harmonics, which are calculated offline at that instant of time [45, 234].

Optimal Switching Sequence MPC (OSS-MPC) is another efficient fixed switching frequency technique that was first applied to MLIs in [219] for grid-connected NPC converter. The concept of approach is to divide the converter states into a limited number of sequences (Seq_1 to Seq_n). The optimal sequence (Seq_{opt}) is identified by optimizing the cost function for all sequences, as shown in Fig. 5.11c. This method has a better steady-state performance with an improved harmonic spectrum compared to conventional FCS-MPC. However, the computational effort is higher and the design of the switching sequences is a challenging task for MLIs, especially for three-phase implementation. The application of this method with a NP potential control as a second control target for a full-bridge NPC converter is presented in [197, 235]. A similar method is reported in [236] for T-type converter by applying three vectors per control cycle. In addition, NP potential control is achieved exploiting the converter redundancies, eliminating the use of a weighting factor. However, the cost function is formulated with the estimated voltage, increasing control sensitivity to model parameters.

5.3.4 Long-horizon FCS-MPC

By adopting a short prediction horizon ($N_p = 1$) for MLIs, the FCS-MPC problem can be solved online with exhaustive enumeration [237] and with the methods detailed in Section 5.3.1. This relates to the formulation derived in Sections 5.2 and 5.3. However, it has been proven that employing FCS-MPC with long prediction horizons can improve the control performance and

result in notable improvements under steady-state operating conditions [238, 239].

In particular, when MLIs are the targeted applications, long horizons strongly impact the closed-loop performance [240–242]. A long prediction horizon enables the controller to make better educated decisions because the evolution of the system state is computed over a longer time interval into the future. According to the study presented in [243, 244] for an MV grid-tied 3L-NPC converter with an LCL filter, extending the prediction horizon from 2 to 10 steps reduces the total demand distortion (TDD) of the grid current by 9% at $T_s = 150$ μs at a switching frequency $f_{\text{sw,avg}} = 400$ Hz. Similar benefits hold over the whole frequency range.

However, the computational complexity increases exponentially as the prediction horizon increases. [182, 245]. Therefore, practical realization of real-time implementation of FCS-MPC with long prediction horizons is not trivial [176]. This challenge becomes more acute in applications of MLIs due to the large number of converter states. Thus, adopting an exhaustive enumeration criteria is computationally unfeasible when considering real-time implementation onto industrial embedded hardware [176].

To reduce the computational load without sacrificing the optimality of the solution, methods that rely on dedicated optimization algorithms, such as branch-and-bound [185], and non-trivial prediction horizon formulations, such as move blocking strategies [245], event-based horizons [45] and prediction with extrapolation or interpolation [230, 246–248], should be considered. Several improvements have been proposed regarding these methods to reduce the computational complexity and with that facilitate the real-time implementation of the long-horizon MPC [243, 249–252]. Another common approach is to limit the search space, i.e., to reduce the number of candidate solutions to be considered adopting one of the methods denoted in Section 5.3.1.

5.4 Lyapunov-Based Direct MPC

The Lyapunov direct method has been widely employed in the development of controllers for power electronic applications. In this section, recent research integrating Lyapunov theory with FCS-MPC is highlighted. Lyapunov-based MPC (MPC) is used to improve system stability for bridge converters [253–255], multilevel converters [217, 256, 257], and drive applications [258–262].

In [256], a gain-free Lyapunov-based MPC is presented for nested neutral-point clamped converters. A finite set of control candidates is generated after eliminating the states that make the Lyapunov function non-definite negative. Since the application of the shortlisted control input candidates does not result in an appropriate output state, duty cycle control is also incorporated into the control system. In addition, the cost function of the MPC is designed using fuzzy logic-based multi-objective optimization. Although the controller achieves satisfactory steady-state error, fast response, and lower average switching frequency compared to classical MPC, its complex design compromises the inherent simplicity, which is a key advantage of MPC.

For the seven packed u-cell (PUC7) converter [263, 264], the cost function of the classical FCS-MPC is replaced by a Lyapunov-based cost function that eliminates the need for gain tuning and avoids the requirement for additional adjustments and/or controllers. The inhomogeneous terms of the cost function are lumped after eliminating the common term thanks to the

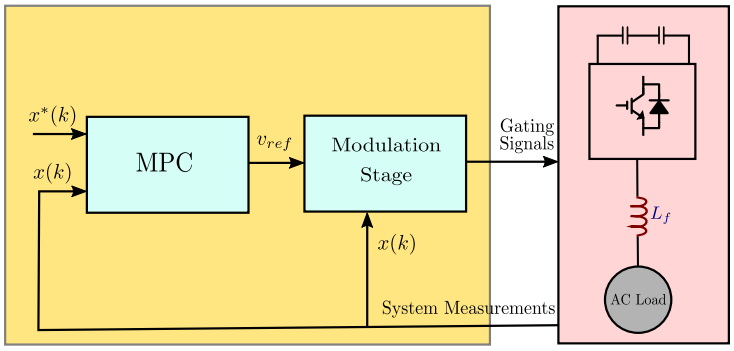


Figure 5.12: Block diagram of indirect MPC.

direct Lyapunov method. Similar research has used the same design concept for PUC7 rectifiers [264], T-type rectifiers [254, 265], interleaved neutral-point clamped converters [257], and three-phase four-arm modular multilevel converters [266].

5.5 Indirect MPC for Multilevel Inverters

In contrast to direct MPC methods, where control and modulation take place in one computational stage, indirect MPC solves these problems in a sequential manner. Hence, indirect MPC computes the control action, e.g., the modulating signal or the duty ratio, which is subsequently fed into a modulator for generation of the switching commands, offering the advantage of constant switching frequency operation. The block diagram of indirect MPC is shown in Fig. 5.12. Indirect MPC methods mask the switching nature of the power converter by considering averaged dynamics. In doing so, the optimization variable is a real-valued vector and the feasible set of the optimization problem underlying indirect MPC a continuous set. This gives rise to the category of indirect MPC methods that are referred to as CCS-MPC.

5.5.1 Continuous control set MPC

Owing to the real-valued optimization variable and the convexity of the feasible set, the optimization problem underlying CCS-MPC is typically formulated as an unconstrained or constrained QP [267]. Solving the former MPC problem is straightforward as there exists an analytical solution [268]. As a result, the state-feedback control law can be easily computed offline, which greatly simplifies the real-time implementation of such a control strategy.

With regards to CCS-MPC as a constrained QP, even though the complexity of the optimization problem is higher than that of the unconstrained QP, its computational load is still relatively modest, especially when comparing with FCS-MPC. This is particularly true for MLIs as the computational complexity of CCS-MPC is almost independent of the number of voltage levels, whereas that of FCS-MPC increases exponentially. The above reason, along with the existence of several off-the-self solvers for QPs, facilitate the real-time implementation of CCS-MPC for MLIs [53, 54, 244, 269–272].

5.5.2 Deadbeat MPC

Deadbeat MPC (DB-MPC) techniques typically use a discretized model of the system to compute the required control actions for a fast transient and zero steady-state error [154, 273, 274]. DB-MPC significantly reduces the computational load by directly calculating the reference voltage that nullifies the current error at the next sample using the system-discrete model. Then, a modulation stage is used to generate the pulses for switches. Unlike CCS-MPC, DB-MPC does not require intricate mathematical formulations. Nevertheless, it has the limitation of being unable to process multiple targets during the calculation of reference voltage, as per its conventional concept. Despite this limitation, handling multiple objectives during the modulation stage remains possible, given the presence of redundant states within the converter being considered.

DB-MPC has been adopted in motor drives with conventional two-level inverters [275–277], achieving a fast dynamic performance as with FCS-MPC. In addition, compared to FCS-MPC, a much lower computational load is required for DB-MPC because there is no need for switching states evaluation, cost function optimization, or weighting factors tuning. Moreover, thanks to the presence of the modulation stage, improved steady-state behavior has been achieved with a fixed switching frequency. Despite the attractive features of DB-MPC, few works have been reported in the literature on the application of this method to MLIs.

A DB-MPC combined with a nearest level modulation approach was proposed in [154], to reduce the circulating current in MMC applications. The suggested control strategy presented a high ability of managing large steady-state circulating current harmonics, superior dynamic performance, while granting the rejection of AC disturbances. Moreover, a dual-objective DB-MPC technique was applied to control a single-phase MMC (minimize the circulating current and track the sinusoidal output current reference) in [278] by governing the upper and lower arm voltages. The authors in [68] developed a DB-MPC for controlling permanent magnet synchronous motors (PMSM) supplied by a 3L-NPC inverter. To improve the robustness of this approach, the saturation effects of the PMSM were taken into account. In [279], three DB-based MPC methods are reported for three-phase 3L-NPC to reduce the computational efforts of the traditional FCS-MPC. The three schemes depend on calculating the reference voltage using the DB concept to nullify the current error at the next sample. However, cost function optimization and weighting factor tuning are still required. In addition, the switching frequency was not constant, bringing again some of the shortcomings of the traditional FCS-MPC.

Modeling accuracy is quite significant in DB-MPC since the future decision is based solely on the calculated reference voltage, which is estimated according to the system parameters. To address the system parameters mismatch and uncertainties, several estimation approaches have been reported in the literature. In [280], a discrete-time disturbance observer is presented and incorporated into the DB-MPC for a five-phase PMSM to address the machine parameter variation issue. The authors in [275] investigated the performance of the traditional DB-MPC for PMSM under system parameters mismatch. Accordingly, an observer based on the sliding mode exponential law was developed to predict the stator currents and track the disturbances resulting from parameter variations.

5.6 Comparison of MPC Methods

In this section, a brief qualitative comparison between the common MPC methods for MLIs is presented and summarized in Table 5.5. The classic proportional–integral (PI) controller in conjunction with a PWM stage is also included in the comparison [29, 281]. The evaluation encompasses various metrics, including computational burden, design complexity, capability to accommodate multiple control objectives, efforts required for tuning weighting factors and controller gains, switching frequency, sensitivity to parameter mismatches, steady-state performance, and dynamic performance.

Simplicity of design and ability to easily include multiple objectives are obvious advantages of conventional FCS-MPC, however, the need for a weighting factor for each objective with the accompanying tuning efforts is a challenge in this scheme. Also, the variable switching frequency makes this method not recommended for grid-connected applications due to the difficulty of the filter design. Long-horizon MPC can achieve better steady-state performance, however, The computational burden increases exponentially as the number of prediction steps N_p increases.

Lyapunov-based MPC is a type of controller that uses a discrete form of the derivative of the positive Lyapunov cost function to ensure system stability and robustness. It is similar to conventional FCS-MPC with optimized weights, achieved by canceling the common term of the errors. However, it is not easy for systems with multiple constraints and objectives.

M2PC and OSS-MPC are two approaches aimed at enhancing the steady-state performance of the conventional FCS-MPC and operating at a fixed switching frequency. However, while offering these advantages, these approaches introduce additional calculation loads and deviate from the design simplicity inherent in the traditional method.

Indirect MPC, in its version of CCS-MPC, has the advantages of FCS-MPC, such as the ability to handle multiple objectives and explicit system constraints in a straightforward manner. At the same time, the inherent disadvantages appear in this derivative as well. Hence, the existence of multiple weighting factors—which can be more than in FCS-MPC due to the presence of slack variables—can complicate the controller tuning. Nevertheless, since CCS-MPC is formulated as a QP its computational complexity can be relatively modest, even when a long horizon is employed, while the presence of a dedicated modulator results in a fixed switching frequency. These advantages make CCS-MPC particularly attractive for a wide range of applications, such as grid-connected converters or applications where higher switching frequencies are required.

DB-MPC exhibits excellent steady-state performance and constant switching frequency, similar to that of a linear PI controller, as both methods employ a modulation stage. However, effectively addressing multiple objectives can be challenging, although it can be achieved to some extent by leveraging the available redundant states of the MLI topology within the modulation stage.While the DB-MPC has high dynamic performance and avoids the problematic tuning associated with the classical PI controller, one drawback is its high sensitivity to model parameters mismatch. MPC has demonstrated a high capability to handle the challenging multi-objective control problems of MLI applications with easy implementation, simplicity, and high dynamic performance. Although tremendous progress has been achieved over the last decade, MPC still has some challenges that represent open research topics.

Table 5.5: Assessment of most common MPC methods for MLIs.

Method	Computational Burden	Design Complexity	Multiobjectives Handling	Gains/Weighting Factors	Explicit Modulator	Switching Frequency	Parameter Robustness	Steady-state Performance	Dynamic Performance
Conventional FCS-MPC	✓	✓✓	✓✓	✗✗	Not required	Variable	✗	✗	✓
Long-Horizon FCS-MPC	✗	✓	✓✓	✗	Not required	Variable	✗✗	✓	✓
Lyapunov MPC	✓	✓✓	✗✗	✓✓	Not required	Variable	✓	✗	✓
MP2C	✗	✓	✓✓	✗✗	Not required	Fixed	✗	✓	✓
OSS-MPC	✗✗	✗✗	✓✓	✗✗	Not required	Fixed	✗	✓✓	✓✓
CCS-MPC	✓	✓	✓✓	✗✗	required	Fixed	✗	✓✓	✓
Deadbeat MPC	✓✓	✓✓	✗✗	N/A	required	Fixed	✗✗	✓✓	✓
Classic PI-PWM	✓✓	✓	✗✗	✗✗	required	Fixed	✓✓	✓✓	✗✗

* Scaled from best (✓✓) to worst (✗✗).

5.7 Discussion and summary

MPC has demonstrated a high capability to handle the challenging multi-objective control problems of MLI applications with easy implementation, simplicity, and high dynamic performance. Although tremendous progress has been achieved over the last decade, MPC still has some challenges that represent open research topics.

Several works have been reported to reduce the computational efforts of direct MPC for MLI applications. However, most of them rely on offline calculations and stored LUTs, which require high storage space. In addition, some computationally-efficient schemes suffer from a significant deterioration in the performance and/or increased complexity compared to the conventional method. Therefore, reducing calculations without degrading control performance or without storing numerous LUTs is still an open research point, especially for high-level MLIs ($N_{\text{level}} \geq 5$). Solving this research question will bring tangible benefits from the industry perspective because this will allow the practical implementation at high sampling frequencies with inexpensive commercial microprocessors.

With multiple-vectors MPC, the heavy computational problem becomes more severe since it is the most computationally demanding subset of direct MPC [282]. During the optimization process, not only the voltage vectors of all switching sequences are evaluated, but also the dwell time of vectors in the optimal sequence is determined. There is some incipient work to mitigate the acute computational complexity with MLIs [283]. However, most of the existing research is limited to 3L topologies. Therefore, the extension of multiple-vectors MPC to higher-level topologies requires further investigation with addressing the related issues.

Moreover, being a multi-objective control technique, the performance of the MPC approach depends mainly on the tedious and time-consuming task of tuning the objectives' WFs to determine their priorities in the control decision. In this regard, MPC without WFs for MLIs can eliminate the complex tuning process, but more research should be devoted to how to avoid the suboptimal problems. Compared with the MPC with a regular cost function, it should be proved that weighting factorless MPC is able to provide the same or even better control performance.

In summary, this chapter presented the fundamentals, operating principles and technical challenges of the MPC for MLIs, focusing on FCS-MPC as the most popular approach for MLIs. The advances and effective solutions to each challenge have been discussed. Some prominent concepts have been experimentally validated on the grid-connected 5L-ANPC inverter and compared to evaluate their performance.

CHAPTER 6

Low-complexity Robust FCS-MPC for FC-based MLI with Different Levels Modes

This chapter presents two improved FCS-MPC algorithms for FC-based MLIs to reduce computational burden and weighting factor design efforts and to enhance control robustness. Section 6.2 presents the mathematical modeling of the considered system. The conventional FCS-MPC method is designed in Section 6.3. The first proposed FCS-MPC method is explained in Section 6.4, while the second proposed low-complexity FCS-MPC method is presented in Section 6.5. The experimental validation, performance assessment, comparison and results discussion are provided in Section 6.6. Finally, Section 6.7 provides the summary of the chapter.

6.1 Introduction

Conventional control methods are the most widely used control techniques in industrial power conversion systems, however, they have some problematic issues such as difficulty to deal with nonlinearities and constraints, parameter tuning problems, and poor dynamic behavior [38]. Furthermore, multi-objectives control problems are considered to be challenging tasks with the traditional methods such as carrier-based PWM (CB-PWM) or SVPWM. As an example, for FC-based MLIs, it is required to regulate the output current and, simultaneously, achieve the balancing of the FCs and NP potential. In addition, although the hybrid MLI topologies have clear superiority in terms of required passive/active components, efficiency and cost compared to conventional ones, a common challenge of these topologies is the low number of redundant states due to reducing the number of power devices. This issue makes FCs balancing challenging and increases the capacitor size for PWM-based control schemes when the balancing algorithm relies on converter redundancies.

As discussed in Chapter 5, MPC has demonstrated a high capability to handle the challenging multi-objective control problems of MLI applications with easy implementation. FCS-MPC, as the most popular MPC schemes, has distinct merits such as fast dynamic response, simplicity,

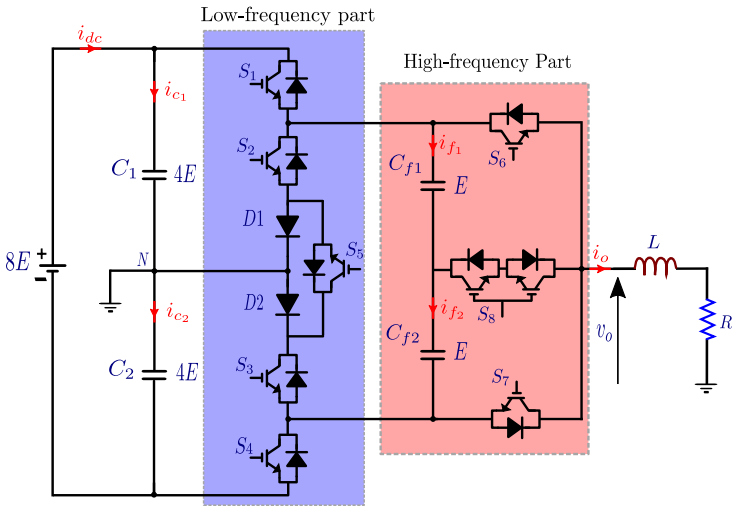


Figure 6.1: Circuit structure of the SC-ANPC inverter.

ability to handle multiple control objectives and constraints [38]. However, as described in the previous chapter, there are still some challenges when it comes to MLI applications, such as high computational burden, tuning of weighting factors and high dependency on the model accuracy.

Motivated by these issues, this chapter proposes a low-complexity FCS-MPC with online parameters estimation for FC-based MLIs. The proposed FCS-MPC method can be applied to different single-phase MLIs. The main advantages of this method are as follows:

1. The computational load of the proposed MPC method has been significantly reduced compared to conventional FCS-MPC, firstly by eliminating the computational load required for current prediction and secondly by halving the number of FCs voltage predictions and cost function evaluations,

2. Three control objectives are achieved with only one weighting factor, further reducing control complexity by eliminating the cumbersome effort of coordinating the weighting factors. Moreover, this method gets rid of the calculation efforts required for the voltage predictions of the dc-link capacitors, and

3. The proposed FCS-MPC ensures continuous operation of the considered converter in the faulty case of the bidirectional switch with a lower number of voltage levels (five or seven), while ensuring the balancing of FCs and NP in all cases.

6.2 System modelling

The circuit configuration of the single-phase SC-ANPC inverter is shown in Fig. 6.1. The dynamic voltage equation of the system is expressed as

$$v_o = Ri_o + L\frac{di_o}{dt}, \tag{6.1}$$

where v_o and i_o are the inverter output voltage and current, respectively, L is the filter inductance, and R is the load resistance. Assuming ideal switches operation and according to the switching states of the inverter given in Table 3.1, v_o can be expressed as

$$v_o = s_1 V_{c1} - s_4 V_{c2} + s_a V_{f1} + s_b V_{f2}, \tag{6.2}$$

where V_{c1} and V_{c2} are the voltages of the dc-link capacitors C_1 and C_2. V_{f1} and V_{f2} are the voltages of FCs C_{f1} and C_{f1}, receptively. s_a, and s_b are new variables used to simplify the analysis and are expressed as

$$s_a = s_4 + s_6 - S_1 - S_2, \; s_b = s_3 + s_4 - s_1 - s_7. \tag{6.3}$$

Concerning the FCs, the continuous-time model can be derived as

$$\left.\begin{aligned} i_{cf1} = C_{f1}\tfrac{dV_{f1}}{dt} = -s_a i_o, \\ i_{cf2} = C_{f2}\tfrac{dV_{f2}}{dt} = -s_b i_o, \end{aligned}\right\} \tag{6.4}$$

where i_{f1} and i_{f2} are the current of the FCs C_{f1} and C_{f1}, respectively. Similarly, the model of the dc-link capacitors is obtained as

$$\left.\begin{aligned} i_{c1} = C_1\tfrac{dV_{c1}}{dt} = i_{dc} - s_1 i_o, \\ i_{c2} = C_2\tfrac{dV_{c2}}{dt} = i_{dc} + s_4 i_o, \end{aligned}\right\} \tag{6.5}$$

where i_{c1} and i_{c2} are the currents of C_1 and C_2, respectively. i_{dc} represents the input dc current. Assuming equal capacitance $C_1 = C_2 = C$, the dc-link voltage balancing can be represented by

$$\Delta i_c = C\frac{d\Delta V_c}{dt}, \tag{6.6}$$

where $\Delta V_c = V_{c1} - V_{c2}$ is the dc-link voltage difference and $\Delta i_c = i_{c1} - i_{c2}$ is the current difference and obtained, from (6.5), as

$$\Delta i_c = -(s_1 + s_4) i_o. \tag{6.7}$$

6.3 Conventional FCS-MPC

The traditional FCS-MPC is described in this section for the conventional operation of the converter as a 9L inverter. Three control objectives are considered in the FCS-MPC algorithm: 1) current tracking i_o, 2) FCs voltage regulation V_{f1} and V_{f2}, and 3) NP potential control. To build the discrete-time model of i_o, forward Euler discretization method [176] is adopted to the continuous system model (6.1), which gives

$$i_o(k+1) = (1 - \frac{RT_s}{L}) i_o(k) + \frac{T_s}{L} v_o(k), \tag{6.8}$$

where $i_o(k+1)$ refers to the predicted current at $(k+1)^{th}$ sample and T_s refers to the sampling period. By discretizing (6.2), $v_o(k)$ is given as

$$v_o(k) = s_1 V_{c1}(k) - s_4 V_{c2}(k) + s_a V_{f1}(k) + s_b V_{f2}(k). \tag{6.9}$$

Similarly, the discrete-time model of FCs (6.5) and dc-link (6.6) can be obtained as

$$\left.\begin{array}{l} V_{f1}(k+1) = V_{f1}(k) - \frac{T_s s_a}{C_{f1}} i_o(k), \\ V_{f2}(k+1) = V_{f2}(k) - \frac{T_s s_b}{C_{f2}} i_o(k), \end{array}\right\} \tag{6.10}$$

$$\Delta V_c(k+1) = \Delta V_c(k) - \frac{(s_1(k) + s_4(k))T_s}{C} i_o(k). \tag{6.11}$$

By adopting the l_2-norm [181], the cost function g is designed as

$$\begin{array}{l} g = [i_o^*(k+1) - i_o(k+1)]^2 + \lambda_1 [V_f^*(k+1) - V_{f1}(k+1)]^2 \\ \lambda_1 [V_f^*(k+1) - V_{f2}(k+1)]^2 + \lambda_2 [\Delta V_c(k+1)]^2, \end{array} \tag{6.12}$$

where λ_1 and λ_2 are the weighting factors used to adjust the priority of the control objectives. $i_o^*(k+1)$ is the reference current at $(k+1)^{th}$ sample and is obtained by using Lagrange extrapolation [175]. As described earlier, the FCs are maintained at $V_{dc}/8$ (E) to generate nine voltage levels, hence, $V_f^*(k+1) = V_f^*(k) = V_{dc}/8$. Commonly, the tuning of the weighting factor is realized by trial and error based on performance indicators [284].

According to the conventional FCS-MPC and the number of the converter states, it is required to carry out $12\times$ current predictions, $12\times$ FCs voltages predictions, $12\times$ dc-link voltage predictions, and $12\times$ cost function calculations each control cycle T_s, which is considered a heavy computational load. In addition, the tuning procedure of the weighting factors is non-trivial and requires several simulations and experimental tests with complex numerical models [284].

6.4 Proposed FCS-MPC for different operation modes and online parameters estimation

6.4.1 NP balancing

As illustrated in Table 3.1, the 9L-SC-ANPC inverter has redundant states for levels 0 and $\pm 2E$. Only the redundancies available for $\pm 2E$ can be employed in the capacitors balancing as the zero-level has no effect on the FCs nor on the dc-link capacitors. Accordingly and as a result of the reduction of the power devices compared to other common dc-link nine-level inverters, the available redundant states are not sufficient to achieve a weighting factorless FCS-MPC with three control objectives, current tracking, FCs, and dc-link balancing as reported in [50].

In conventional FCS-MPC, three control objectives require three terms in the cost function with two weighting factors, as shown in (6.12). Coordinating two weighting factors to achieve acceptable performance in terms of control objectives is a cumbersome process. In this work, two control objectives are represented by one term in the cost function according to the power flow of the 9L-SC-ANPC inverter. Consequently, only one weighting factor is required. This is

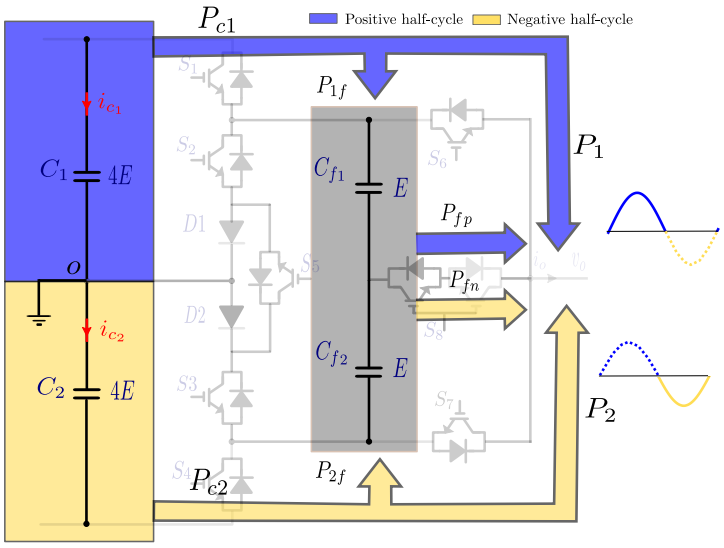


Figure 6.2: Power exchange for an entire cycle of the single-phase SC-ANPC converter.

Table 6.1: dc-link capacitors currents.

State	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_9	V_{10}	V_{11}	V_{12}
v_o	+4E	+3E	+2E	+2E	+E	0	0	-E	-2E	-2E	-3E	-4E
i_{c1}	$-i_o$	$-i_o$	$-i_o$	0	0	0	0	0	0	0	0	0
i_{c2}	0	0	0	0	0	0	0	0	0	$-i_o$	$-i_o$	$-i_o$

realized by adapting the concept presented in Section 3.3.2 to eliminate a weighting factor by integrating the dc-link balance into the FCs control objective.

To this end, the power supplied by the dc-link capacitors to the FCs and the ac side is first analyzed. Table 6.1 shows the dc-link currents i_{c1} and i_{c2} during the switching states. It is clear that the upper capacitor C_1 is involved in transferring power from the dc side to the FCs and the ac load only during the positive half-cycle for switching states V_1, V_2, and V_3. While C_2 takes over the power feed in the negative half-cycle for states V_{10}, V_{11}, and V_{12}. The FCs feed the load in states V_4 and V_5 in the positive half-cycle and states V_8 and V_9 in the negative one, since FCs act as intermediaries for transferring power from the dc-link to the ac side. Fig. 6.2 depicts the power exchange in the inverter during an entire power cycle. The power flow diagram is represented in Fig. 6.3. Assuming symmetrical operation, the equation of the power flow is written as

$$P_1 + P_{fp} = P_2 + P_{fn}, \tag{6.13}$$

where P_1 and P_2 represent the powers provided by C_1 during the first half-cycle and C_2 during the second half-cycle, respectively. P_{fp} and P_{fn} represent the powers supplied by C_{f1} and C_{f2} in the positive and negative half-cycles, respectively. According to the power flow shown in Fig. 6.2, the total power P_{c1} provided by C_1 and P_{c2} by C_2 are given as

$$P_{c1} = P_1 + P_{1f} \text{ and } P_{c2} = P_2 + P_{2f}, \tag{6.14}$$

where P_{1f} and P_{2f} refer to the powers supplied to the FCs by C_1 in the positive half-cycle and C_2 in the negative half-cycle, respectively. As it is clear from (6.14), the total power provided

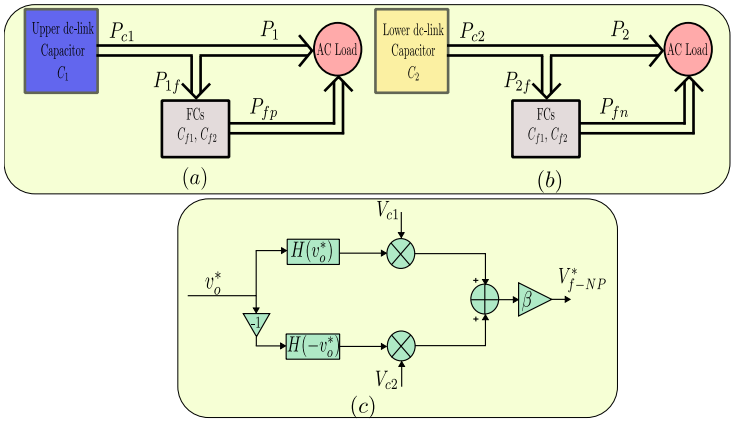


Figure 6.3: Power flow diagram and FCs reference generator: (a) power flow during positive half-cycle, (b) power flow during negative half-cycle, and (c) FCs reference voltage generator.

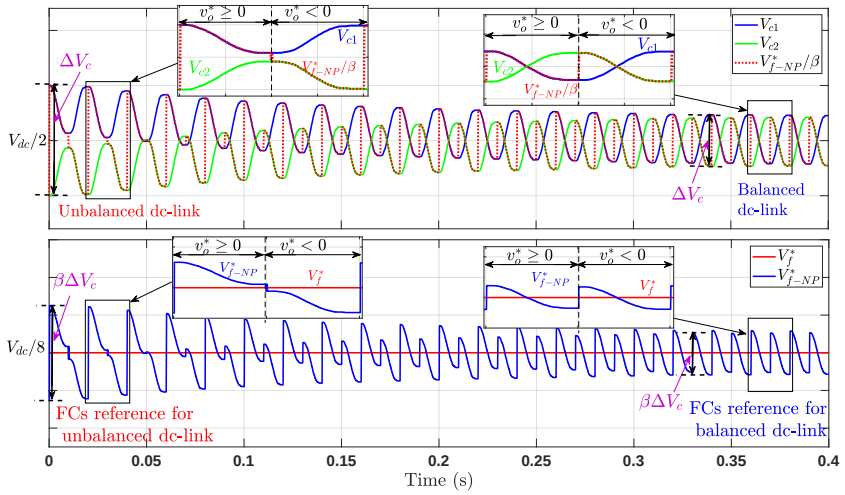


Figure 6.4: FCs reference voltage estimation based on dc-link voltages.

by C_1 and C_2 can be controlled by regulating the power delivered to the FCs P_{1f} and P_{2f}, respectively. Accordingly, V_{c1} and V_{c2} can be controlled. For illustration, assume unbalanced dc-link with V_{c1}>V_{c2} as in Fig. 6.4. To reduce the voltage deviation and realize the balance, the reference voltage of the FCs is increased in the positive half-cycle to increase P_{1f} and reduced in the negative half-cycle to reduce P_{2f}. Consequently, the energy given by C_1 will be higher than that given by C_2 ($P_{c1} > P_{c2}$), which forces V_{c1} to decrease and V_{c2} to increase. By the same way, if $V_{c1} < V_{c2}$, FCs reference voltage is reduced in the first half-cycle and increased in the second one. Note that, to avoid cumulative increases/decreases in the FCs voltage, the power flow of the FCs over a complete cycle must fulfil

$$P_{1f} + P_{2f} = P_{fp} + P_{fn}. \tag{6.15}$$

According to the previous analysis, the reference voltage of the FCs including the NP bal-

ancing V^*_{f-NP} is estimated according to V_{c1} and V_{c2} as

$$V^*_{f-NP} = \begin{cases} \beta V_{c1}, \text{ if } v^*_o \geq 0, \\ \beta V_{c2}, \text{ if } v^*_o < 0, \end{cases} \tag{6.16}$$

where β is a factor that determines the ratio of the nominal reference voltage between the FCs and dc-link capacitors. As previously discussed, for the 9L-SC-ANPC, C_1 and C_2 should be balanced at $4E$ while C_{f1} and C_{f2} are balanced at E, and accordingly, $\beta = E/4E = 0.25$. The generation of the FCs reference voltage is represented in Fig. 6.3c, where H refers to the Heaviside step function [285].

Although this method can achieve NP balance regardless of modulation index or power factor, the voltage ripples of the FCs are affected by the ripples in the dc-link capacitors, since V^*_{f-NP} is estimated based on V_{c1} and V_{c2}. As shown in Fig. 6.4, the peak-to-peak value of V^*_{f-NP} is equal to $\beta\Delta V_c$ and, accordingly, the FCs actual ripples ΔV_f follows the relationship $\Delta V_f \geq \beta\Delta V_c$. If the inverter has redundant states for all levels with opposite impact on FCs, which is not the case for the considered converter, ΔV_f can be limited to $\beta\Delta V_c$. Otherwise, $\Delta V_f > \beta\Delta V_c$. However, this limitation is acceptable because it produces per-unit voltage ripples in the FCs that are equal to or slightly higher than the per-unit ripples in the dc-link (based on the availability of redundancies).

Considering the estimated V^*_{f-NP}, the cost function of the conventional method in (6.12) is simplified as

$$\begin{aligned} g = &[i^*_o(k+1) - i_o(k+1)]^2 + \lambda[V^*_{f-NP}(k+1) - V_{f1}(k+1)]^2 \\ &\lambda[V^*_{f-NP}(k+1) - V_{f2}(k+1)]^2. \end{aligned} \tag{6.17}$$

According to (6.17), only one weighting factor λ is used to realize the three objectives. Moreover, no prediction for the dc-link voltage is required.

6.4.2 Different operation modes

In this section, the conventional control algorithm is improved to enable the SC-ANPC to operate in different modes in the normal state or in case of a faulty bidirectional switch (S_8). The developed FCS-MPC allows the considered converter to generate nine levels in the normal state and seven or five levels in the faulty state. The continuous operation is ensured by regulating the FCs at the new reference value according to the new operation mode, exploiting the available switching states in the faulty case. As discussed before, twelve switching states are available in the normal nine-level operation and are employed in the control design to achieve the three control objectives. Whereas in the faulty case, four switching states are eliminated and only eight states are available as shown in Table 6.2 like the conventional 5L-ANPC converter [24]. In this case, the two FCs (C_{f1}, C_{f2}) are seen as one capacitor ($C_f = C_{f1}/2$) and should be maintained at a new reference according to the desired operation mode of the converter. In this state,FC model is described as

$$i_{Cf} = C_f \frac{dV_f}{dt} = -s_a i_o, \tag{6.18}$$

where $V_f = V_{f1} + V_{f2}$. Adopting forward Euler method, $V_f(k+1)$ is obtained as follows

$$V_f(k+1) = V_f(k) - \frac{T_s s_a}{C_f} i_o(k). \tag{6.19}$$

Table 6.2: Available switching states in the faulty case of the four-quadrant power device S_8.

State	s_1	s_2	s_3	s_4	s_5	s_6	s_7	v_o
$V1$	1	0	1	0	0	1	0	$V_{dc}/2$
$V2$	1	0	1	0	0	0	1	$V_{dc}/2 - V_f$
$V3$	0	0	1	0	1	1	0	V_f
$V4$	0	0	1	0	1	0	1	0
$V5$	0	1	0	0	1	1	0	0
$V6$	0	1	0	0	1	0	1	$-V_f$
$V7$	0	1	0	1	0	1	0	$-V_{dc}/2 + V_f$
$V8$	0	1	0	1	0	0	1	$-V_{dc}/2$

Table 6.3: Switching Table for seven-level operation of the SC-ANPC.

State	s_1	s_2	s_3	s_4	s_5	s_6	s_7	v_o
$V1$	1	0	1	0	0	1	0	$V_{dc}/2$
$V2$	1	0	1	0	0	0	1	$V_{dc}/3$
$V3$	0	0	1	0	1	1	0	$V_{dc}/6$
$V4$	0	0	1	0	1	0	1	0
$V5$	0	1	0	0	1	1	0	0
$V6$	0	1	0	0	1	0	1	$-V_{dc}/6$
$V7$	0	1	0	1	0	1	0	$-V_{dc}/3$
$V8$	0	1	0	1	0	0	1	$-V_{dc}/2$

6.4.2.1 Switching to seven-level mode

To generate seven levels from the SC-ANPC, the reference voltage of the FC is modified as

$$V_f^* = V_{f1}^* + V_{f2}^* = V_{dc}/6. \tag{6.20}$$

According to Table 6.2 and the calculated reference from (6.20), the obtainable levels are $\pm V_{dc}/2$, $\pm V_{dc}/3$, $\pm V_{dc}/6$, and 0. To take the dc-link balancing into account, V_f^* obtained by (6.20) is replaced by V_{f-NP}^* in (6.16) with β=1/3. Accordingly, the modified cost function can be expressed as

$$g = [i_o^*(k+1) - i_o(k+1)]^2 + \lambda[V_{f-NP}^*(k+1) - V_f(k+1)]^2. \tag{6.21}$$

The switching states and corresponding generated levels in this mode are given in Table 6.3.

6.4.2.2 Switching to five-level mode

To produce five voltage levels from the SC-ANPC, the modified reference value of the FCs is set according to (6.22).

$$V_f^* = V_{f1}^* + V_{f2}^* = V_{dc}/4. \tag{6.22}$$

Accordingly, β is set to 1/2 in (6.16) to estimate V_{f-NP}^* and the cost function is the same as (6.21). The generated levels are $\pm V_{dc}/2$, $\pm V_{dc}/4$, and 0. The converter is operating in this

Table 6.4: Switching Table for five-level operation of the SC-ANPC.

State	s_1	s_2	s_3	s_4	s_5	s_6	s_7	v_o
$V1$	1	0	1	0	0	1	0	$V_{dc}/2$
$V2$	1	0	1	0	0	0	1	$V_{dc}/4$
$V3$	0	0	1	0	1	1	0	$V_{dc}/4$
$V4$	0	0	1	0	1	0	1	0
$V5$	0	1	0	0	1	1	0	0
$V6$	0	1	0	0	1	0	1	$-V_{dc}/4$
$V7$	0	1	0	1	0	1	0	$-V_{dc}/4$
$V8$	0	1	0	1	0	0	1	$-V_{dc}/2$

mode as the traditional popular 5L-ANPC [25], where five levels are generated from eight states with the availability of redundant states for levels $\pm V_{dc}/4$, having an opposite impact on the FC. The converter states for the five-level operation mode are given in Table 6.4.

6.4.3 Extended Kalman filter design

Since the MPC is a model-based control method, its performance and stability crucially depend on the accuracy of the system modelling [286]. In [287], authors presented an analytic approach to investigate the effect of the parameters uncertainties on the FCS-MPC. This study showed that a slight mismatch in the system parameters due to temperature, aging and/or varying the operating conditions may lead to prediction errors and, hence, improper selection of the converter vector, which negatively affects the stability or degrades the control performance. To address this issue, an online identification method is designed based on Extended Kalman filter (EKF) to estimate the system parameters (R, L). In addition, the inverter output current is estimated using the designed EKF to reject the measurement noise.

To construct the system model for the online parameters estimator, the nonlinear discretized state-space model is required. The state-space system representation including disturbances can be written as

$$\begin{aligned} \dot{x} &= \mathbf{A}x + \mathbf{B}u + w, \\ y &= \mathbf{C}x + \mathbf{D}u + v, \end{aligned} \tag{6.23}$$

where $x = (i_o,\ R,\ L)^T$, $u = v_o$, and $y = i_o$. $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$, and $\mathbf{D}$ refer to system matrices. w and v are the system uncertainties and measurement noise, respectively. The covariance matrices of w and v are denoted by Q and R, respectively, and are tuned by particle swarm optimization (PSO) [288]. According to the considered system in Fig. 6.1 and referring to (6.1), $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$, and $\mathbf{D}$ are written as

$$\mathbf{A} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \mathbf{B} = \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix}, \mathbf{C} = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}, \mathbf{D} = 0. \tag{6.24}$$

To discretize the system model, forward Euler approximation is employed for (6.23) which

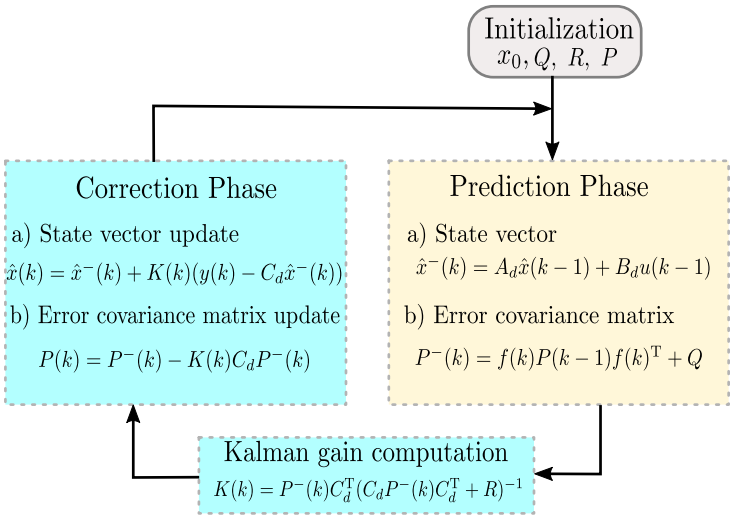


Figure 6.5: Flowchart of the EKF-based parameters estimator.

gives

$$\begin{aligned} x(k+1) &= \mathbf{A}_d x(k) + \mathbf{B}_d u(k) + w(k), \\ y(k) &= \mathbf{C}_d x(k) + \mathbf{D}_d u(k) + v(k), \end{aligned} \tag{6.25}$$

where $\mathbf{A_d}$, $\mathbf{B_d}$, $\mathbf{C_d}$, $\mathbf{D_d}$ are expressed as

$$\mathbf{A_d} = \begin{bmatrix} 1 - \frac{T_s R_t}{L_t} & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}, \mathbf{B_d} = \begin{bmatrix} \frac{T_s}{L_t} \\ 0 \\ 0 \end{bmatrix}, \mathbf{C_d} = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}, \mathbf{D_d} = 0. \tag{6.26}$$

The implementation of the EKF algorithm is depicted in Fig. 6.5 and can be summarized in steps as follows

1. Initialization of state vector $x_0 = x(0)$ and covariance matrices Q and R.
2. Prediction phase
   (a) State prediction $\hat{x}^-(k)$,

$$\hat{x}^-(k) = \mathbf{A}_d\hat{x}(k-1) + \mathbf{B}_d u(k-1), \tag{6.27}$$

   (b) Error covariance matrix prediction $\mathbf{P}^-(\mathbf{k})$,

$$\mathbf{P}^-(k) = J(k)\mathbf{P}(k-1)f(k)^{\mathrm{T}} + \mathbf{Q}, \tag{6.28}$$

   where $J(k)$ is the Jacobian matrix and written as

$$J(k) = \frac{\partial}{\partial x}(\mathbf{A}_d x(k) + \mathbf{B}_d u(k))|_{\hat{x}^-(k)}. \tag{6.29}$$

   According to the system model, $J(k)$ is expressed as

$$J(x) = \begin{bmatrix} 1 - \frac{T_s R}{L} & \frac{-T_s}{L} i_o & \frac{T_s R}{L^2} i_o - \frac{T_s}{L^2} v_o \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{6.30}$$

3. Kalman gain $\mathbf{K(k)}$ computation,

$$\mathbf{K}(k) = \mathbf{P}^{-}(k)\mathbf{C}_d^{\mathrm{T}}(\mathbf{C}_d\mathbf{P}^{-}(k)\mathbf{C}_d^{\mathrm{T}} + \mathbf{R})^{-1}. \tag{6.31}$$

4. Correction phase using measurements

   (a) State vector update,

$$\hat{x}(k) = \hat{x}^{-}(k) + \mathbf{K}(k)(y(k) - \mathbf{C}_d\hat{x}^{-}(k)), \tag{6.32}$$

   (b) Error covariance matrix,

$$\mathbf{P(k)} = \mathbf{P}^{-}\mathbf{(k)} - \mathbf{K(k)C_dP}^{-}\mathbf{(k)}. \tag{6.33}$$

5. Go to step 2.

6.5 Proposed low-complexity FCS-MPC for different operation modes and online parameters estimation

According to the conventional FCS-MPC, for a converter with a number of states N_{st}, it is required per control cycle to carry out $N_{st}\times$ predictions for all variables under control and $N_{st}\times$ cost function calculations, which can be considered a heavy computational load, especially for high-level converters. As a result, the algorithm is time-consuming, resulting in a long sample period to be used which generate a high steady-state error and negatively affects the harmonic spectrum of the waveforms. For these reasons, a computationally-efficient FC-MPC is developed in this section for the 9L-SC-ANPC converter and can be applied for any single-phase converter.

The first objective of the control system is to achieve a high current tracking quality, i.e. to determine the converter state that makes i_o follow its reference i_o^* at the $(k+1)$th instant. Considering the deadbeat control concept by replacing $i_o(k+1)$ with its reference $i_o^*(k+1)$ in (6.8), the reference voltage of the converter v_o^* can be determined as

$$v_o^*(k) = Ri_o(k) + L\frac{i_o^*(k+1) - i_o(k)}{T_s}. \tag{6.34}$$

Depending on v_o^* and the required operating mode, the undesired switching states of the SC-ANPC converter can be excluded as follows.

6.5.0.1 Nine-level operation of SC-ANPC

As shown in Table 3.1, the converter in the normal operation has 12 states (V_1 to V_{12}). The converter states V can be divided into two sets as follow

$$V = \begin{cases} V_p = \{V_1, V_2, V_3, V_4, V_5, V_6\}, \text{ if } v_o^*(k) \geq 0 \\ V_n = \{V_7, V_8, V_9, V_{10}, V_{11}, V_{12}\}, \text{ if } v_o^*(k) < 0. \end{cases} \tag{6.35}$$

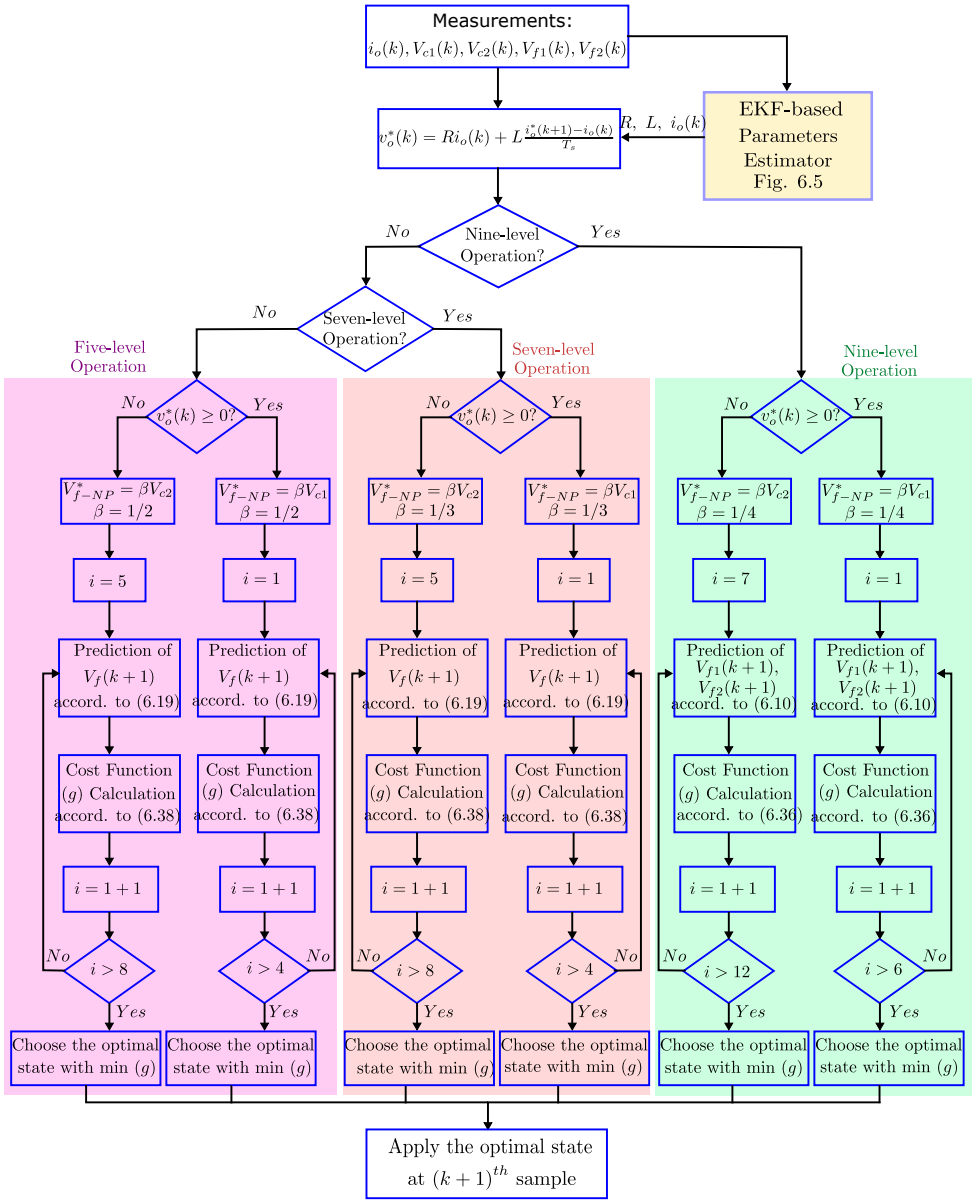


Figure 6.6: Flowchart of the proposed low-complexity FCS-MPC.

Consequently, the FCs voltages predictions (6.10) are carried out for only V_p or V_n based on v_o^*. The modified cost function is expressed as

$$g = [v_o^*(k) - v_o(k)]^2 + \lambda_s[V_{f-NP}^*(k+1) - V_{f1}(k+1)]^2 + \lambda_s[V_{f-NP}^*(k+1) - V_{f2}(k+1)]^2, \tag{6.36}$$

Accordingly, no current predictions are required and the FCs voltages calculations are halved. Moreover, the cost function evaluations are carried out for only the considered 6 vectors. While for the conventional FCS-MPC, it is required per T_s to perform $12\times$ current predictions (6.8), $12\times$ FCs voltages predictions (6.10), and $12\times$ cost function calculations (6.12). Since the cost function is represented in voltage instead of current, it is noted as voltage-based MPC method.

Table 6.5: Experimental system parameters.

Parameter	Value
dc-link voltage, V_{dc}	400 V
Fundamental frequency, f_{line}	50 Hz
Load resistance, R	22 Ω
Filter inductance, L	6 mH
dc-link capacitors, C_1 and C_2	3300 μF
FCs, C_{f1} and C_{f2}	4000 μF
Sampling time, T_s	50 μs

6.5.1 seven- and five-level operation of SC-ANPC

The SC-ANPC converter has 8 states in these operating modes as in Table 6.3. Accordingly, the converter states are divided as

$$V = \begin{cases} V_p = \{V_1, V_2, V_3, V_4, \}, \text{ if } v_o^*(k) \geq 0 \\ V_n = \{V_5, V_6, V_7, V_8\}, \text{ if } v_o^*(k) < 0. \end{cases} \tag{6.37}$$

Similarly, the cost function is written as

$$g = [v_o^*(k) - v_o(k)]^2 + \lambda_s[V_{f-NP}^*(k+1) - V_f(k+1)]^2. \tag{6.38}$$

The NP balancing, FCs model, and online parameters estimator design are the same as the proposed FCS-MPC method in Section 6.4. The flowchart of the proposed low-complexity FCS-MPC is shown in Fig. 6.6.

6.6 Experimental validation

The designed MPC algorithms have been experimentally validated to evaluate their performance. The delay time compensation method proposed in [289] is considered for the three MPC methods. The system parameters used are listed in Table 6.5. The three implemented MPC algorithms are defined as:
Algorithm I: Conventional FCS-MPC method for nine-level operation, presented in Section 6.3,
Algorithm II: Proposed FCS-MPC for different operation modes and online parameters estimation, presented in Section 6.4,
Algorithm III: Proposed low-complexity FCS-MPC for different operation modes and online parameters estimation, presented in Section 6.5.

Several experimental testes are carried out for the three applied FCS-MPC methods. To compare the performance of the MPC methods, the weighting factors λ_1 and λ_2 of algorithm I in (6.12), λ of algorithm II in (6.17), and λ_s of algorithm III in (6.36) should first be tuned. For a meaningful and fair comparison between the MPC methods, the weighting factors are tuned to give the same voltage ripple in terms of the capacitors balancing and, accordingly, the performance can be compared considering the primary control objective, which is the current tracking. The tuning process is performed at the same operating conditions given in Table 6.5

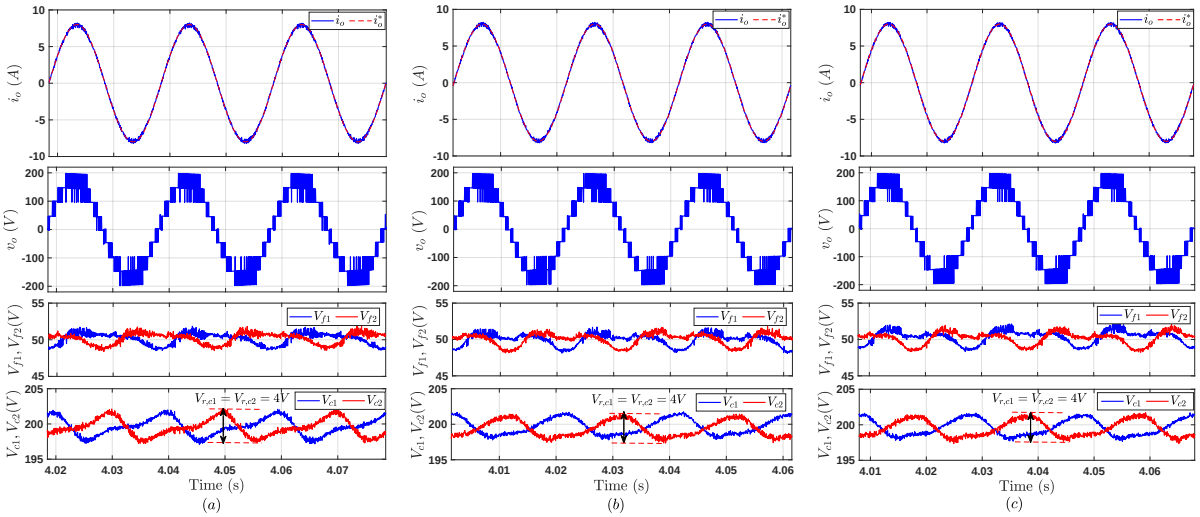


Figure 6.7: Steady-state experimental waveforms in the nine-level mode: (a) Algorithm I, (b) Algorithm II, and (c) Algorithm III.

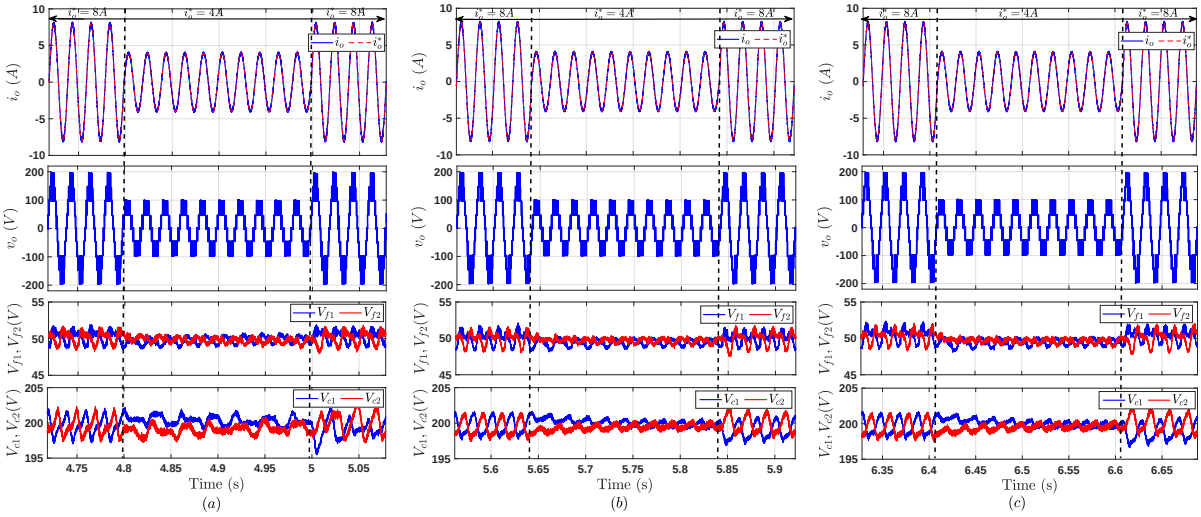


Figure 6.8: Experimental transient performance for a step-change in i_o^*: (a) Algorithm I, (b) Algorithm II, and (c) Algorithm III.

and with a reference current amplitude of 8 A. A voltage ripple of 3 V (6%) in the FCs and 4 V (2%) in the dc-link capacitors are selected and the corresponding λ_1, λ_2, λ and λ_s were found 0.3, 0.08, 0.15 and 2700, receptively.

6.6.1 Steady-state and dynamic performance for nine-level operation

Figure 6.7 depicts the experimental steady-state load current i_o, output voltage v_o, FCs voltages V_{f1}, V_{f2}, and voltages of the dc-link capacitors V_{c1}, V_{c2} for the three MPC methods. The amplitude of i_o^* is 8 A. As it can be seen for the three control methods, i_o follows its reference i_o^* with a high tracking quality. v_o has nine levels in the cycle, which leads to high-quality waveforms with low harmonic contents of v_o and i_o. The voltages of the FCs are well stabilized at their

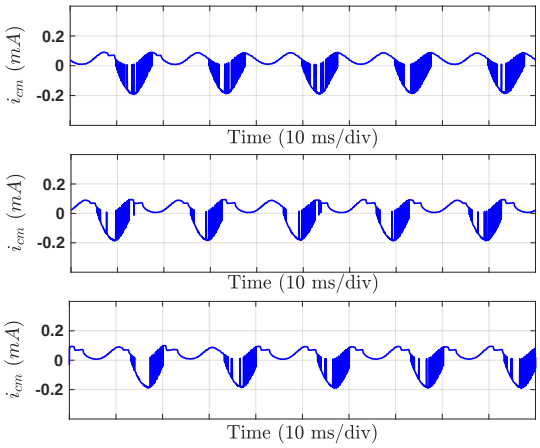


Figure 6.9: Leakage current, from top: Algorithm I, Algorithm II, and Algorithm III.

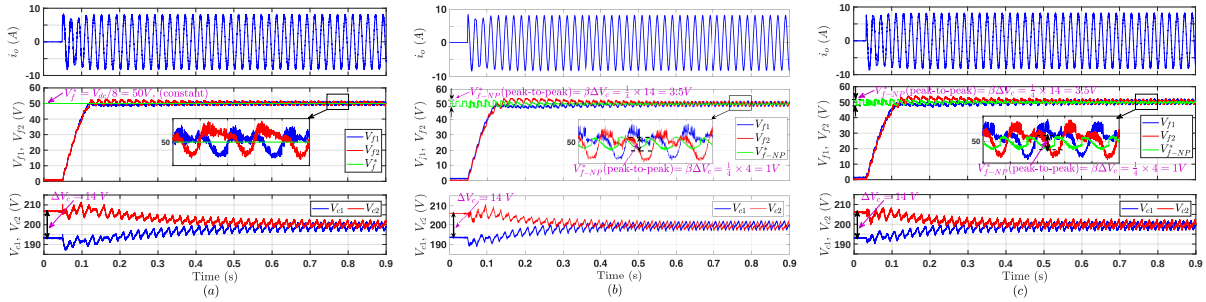


Figure 6.10: Experimental results for start-up process with a mismatch in the dc-link capacitors: (a) Algorithm I, (b) Algorithm II, and (c) Algorithm III.

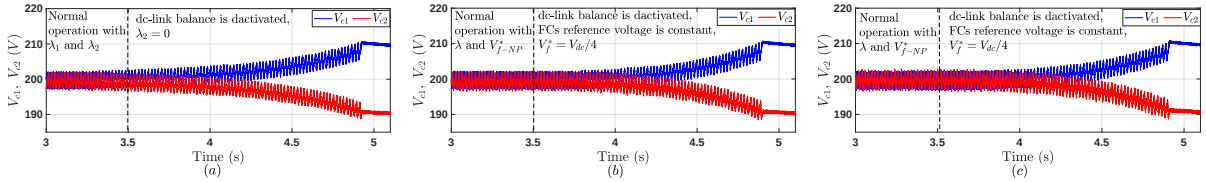


Figure 6.11: Experimental results for dc-link balance deactivation: (a) Algorithm I, (b) Algorithm II, and (c) Algorithm III.

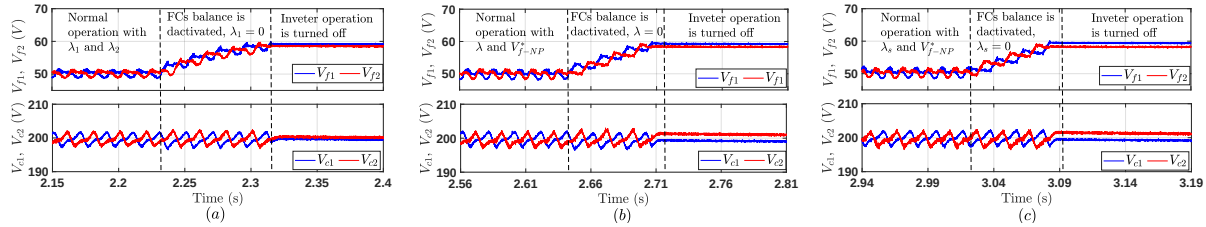


Figure 6.12: Experimental results for FCs balance deactivation: (a) Algorithm I, (b) Algorithm II, and (c) Algorithm III.

reference level $V_{dc}/8$ with a voltage ripple of 3 V and the dc-link capacitors are well balanced

Table 6.6: Steady-state experimental comparison for nine-level operation without parameters mismatch.

Method	Tuned Parameters	e_i	THD$_i$	DC current Injected % i_o	THD$_v$	$i_{cm}(mA)$	f_s[Hz]
Algorithm I	λ_1,λ_2	1.49%	2.45%	0.1%	22.20%	< 0.2	2200
Algorithm II	λ	1.32%	2.20%	0.08%	22.08%	< 0.2	1887
Algorithm III	λ_s	1.28%	2.13%	0.07%	21.02%	< 0.2	1882

with a voltage ripple of 4 V (2%). The comparison of steady-state experimental operation in the nine-level mode is summarized in Table 6.6. Several performance indicators are considered in the comparison, which are the mean absolute reference tracking error of the current e_i, total harmonic distortions of i_o (THD$_i$), injected dc current, total harmonic distortions of v_o (THD$_v$), and average switching frequency f_s. e_i is used as an indicator for the tracking quality and is calculated according to its definition in [29]. From Table 6.6, it is obvious that the three MPC algorithms have high tracking quality with very low tracking error e_i, low harmonic contents for i_o and v_o, and low switching frequency. The injected dc current as a percentage of the rated current is very low for the three methods ($\leq 0.1\%$) and meets the all harmonic standards discussed in [290]. Algorithms II and III have slightly better performance indicators and it can be interpreted that the online parameters estimator can detect the slight variations in the system parameters R and L during the operation, while for algorithm I, the model parameters are assumed to be constant. The transient behavior of the MPC algorithms is examined by varying i_o^* from 8 A to 4 A and again back to 8 A, as depicted in Fig. 6.8. It can be observed that i_o tracks i_o^* with a fast and robust transient performance for all MPC methods. The results confirm the ability of the MPC methods to achieve a stable balancing of the FCs and dc-link capacitors with one weighting factor besides the primary current tracking objective.

Common-mode voltage (CMV) is an important issue in various applications such as grid-connected transformerless PV system. The varying CMV excites the resonant circuit formed by the filter inductance and the parasitic stray capacitors, resulting in leakage current i_{cm}. This current flows through the parasitic capacitor and may cause safety issues, increase the THD of current, and negatively affect system efficiency. The general formulation of the CMV with two filters (L_1, L_2) is written as [290]

$$v_{cm} = \frac{v_{An} + v_{Bn}}{2} + \frac{(v_{An} - v_{Bn})(L_2 - L_1)}{2(L_1 + L_2)}, \tag{6.39}$$

where v_{An} and v_{Bn} refer to the voltages of the output inverter terminals with respect to the negative point of the dc-link. Referring to the considered system in Fig. 6.1 with only L_1 ($L_2 = 0$), v_{cm} is determined as

$$v_{cm} = \frac{v_{An} + v_{Bn}}{2} - \frac{v_{An} - v_{Bn}}{2} = v_{Bn} = V_{c2}. \tag{6.40}$$

The amplitude and frequency spectrum of v_{cm} as well as the value of the parasitic capacitance (C_P) mainly determine the value of i_{cm}. Fig. 6.9 shows the leakage current of the 9L-SC-ANPC under the three MPC methods with C_P= 100 nF. As can be observed, the conventional and two proposed MPC methods have a similar waveform of i_{cm} with a peak value of less than 0.2 mA.

Table 6.7: Steady-state experimental comparison for nine-level operation with a mismatch in R, ($\Delta R = -33.3\%$).

Method	e_i	THD$_i$	THD$_v$
Algorithm I	2.75%	2.15%	25.30%
Algorithm II	1.11%	1.77%	25%
Algorithm III	1.09%	1.75%	24.50%

Table 6.8: Steady-state experimental comparison for nine-level operation with a mismatch in L, ($\Delta L = -60\%$).

Method	e_i	THD$_i$	THD$_v$
Algorithm I	10.75%	19.60%	85.52%
Algorithm II	3.12%	4.64%	17.70%
Algorithm III	3.34%	4.96%	18.92%

Table 6.9: Steady-state experimental comparison for nine-level operation with noise injected into the measured current.

Method	e_i	THD$_i$	THD$_v$
Algorithm I	4.62%	3.82%	32.58%
Algorithm II	2.81%	2.41%	23.10%
Algorithm III	2.74%	2.40%	22.10%

6.6.2 FCs and dc-link balancing evaluation

To further validate the balancing approach of the FCs and dc-link capacitors, the operation is experimentally investigated under abnormal conditions. A capacitance mismatch of 10% was made in the dc-link by connecting a parallel capacitor across C_1, resulting in $C_1 = 1.1C_2$. The experimental results of the converter start-up under this condition are depicted in Fig. 6.10. As can be seen, for the three MPC methods, the two dc-link capacitors have different initial voltages before the start of the inverter operation due to the capacitance mismatch. With start-up, V_{c1} and V_{c2} come close to each other to stabilize at their reference $V_{dc}/2$ despite the capacitance mismatch and the different initial voltages. Also, the FCs voltages V_{f1} and V_{f2} increase from 0 V to settle at their reference value $V_{dc}/8$ (50 V). For the conventional MPC method, the control objectives are achieved by representing them separately in the cost function with two weighting factors. Therefore, the reference voltage of FCs is constant (50 V) as shown in Fig. 6.10a. While for algorithms II and III, as explained in Section 6.4.1, the reference voltage of FCs V^*_{f-NP} is estimated in such a way that the dc-link balance balance is achieved. Fig. 6.10 shows the estimated V^*_{f-NP} based on V_{c1} and V_{c2} starting with an unbalanced dc-link until the balanced operation is reached, which is consistent with the analysis in Fig. 6.4. As can be observed, Algorithms II and III can achieve the balance, even with a mismatch in the dc-link capacitors, in a shorter time compared to the conventional method.

Figure 6.11 shows the experimental results for dc-link balance deactivation. At t = 3.5 s, the dc-link balance target is disabled in the traditional method by setting λ_2= 0 and disabled in Algorithms II and III by setting the FCs reference to its constant nominal value ($V_{dc}/8$).

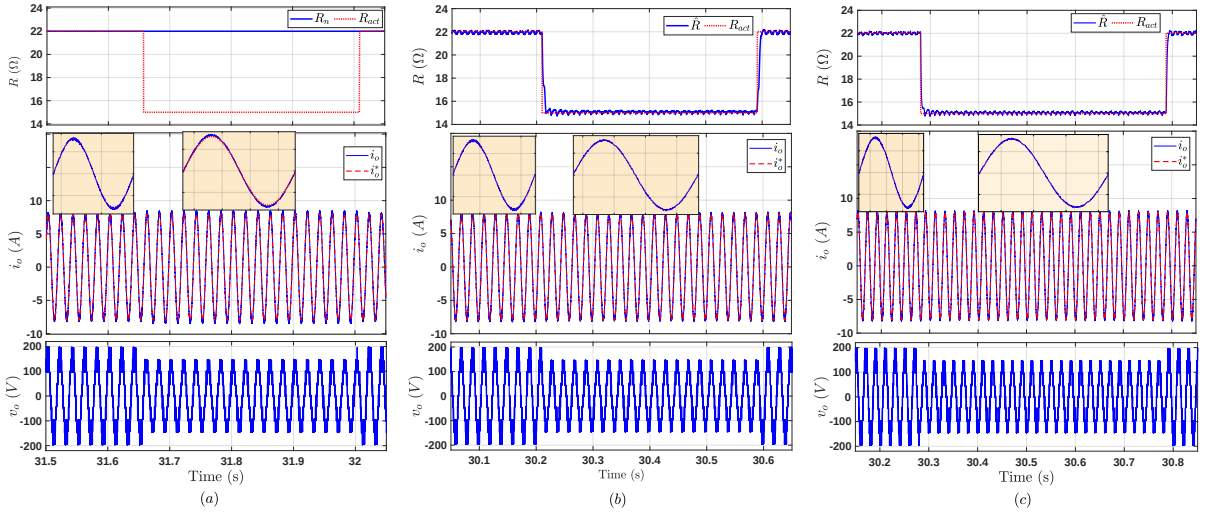


Figure 6.13: Experimental results with a mismatch in the load resistance R: (a) Algorithm I, (b) Algorithm II, and (c) Algorithm III.

As depicted, the difference between V_{c1} and V_{c2} increases until it reaches 20 V, and then the controller turns off the converter operation. The converter operation with FCs deactivation is shown in Fig. 6.12. The FCs control target is disabled by setting λ_1, λ, and λ_s to zero in algorithms I, II and III, respectively. As it is clear, after deactivating the FCs balancing, V_{f1} and V_{f2} rapidly deviate from their reference until the deviation reaches 10 V and then the controller turns off the inverter to protect the FCs from overvoltage damage, which proves the feasibility of the FCs balance for the three MPC methods.

The experimental results in Figs. 6.10, 6.11, and 6.12 confirm the ability of the proposed MPC method to achieve a stable balancing of the FCs and dc-link capacitors besides the primary current tracking objective with only one weighting factor in the normal and abnormal operations, which reduces the cumbersome effort required for weighting factor tuning.

6.6.3 Parameters mismatch and measurement noises

In this test, the control performance is studied under the variation of the real system parameters to investigate the robustness of the system. For Algorithm I, the nominal values of the system parameters R_n and L_n are considered in the system model and assumed to be constant. Whereas for algorithms II and III, the estimated parameters $\hat{R}$ and $\hat{L}$ provided by the EKF-based estimator are considered in the system model. The variation percentage of the system parameters ΔR and ΔL can be calculated as

$$\begin{aligned} \Delta R &= \frac{R_{act}-R_n}{R_n} \times 100, \\ \Delta L &= \frac{L_{act}-L_n}{L_n} \times 100, \end{aligned} \tag{6.41}$$

where R_{act} and L_{act} are the actual values of the real system. Fig. 6.13 shows the control performance for a step-change of -33.3% in the actual load resistance, where R_{act} is changed from 22 Ω to 14.7 Ω and then back to 22 Ω. It can be observed from the results that algorithms II and III can estimate the actual values of the system parameters with fast dynamic response, and as a result, improved current tracking performance is achieved with high-quality waveforms. While

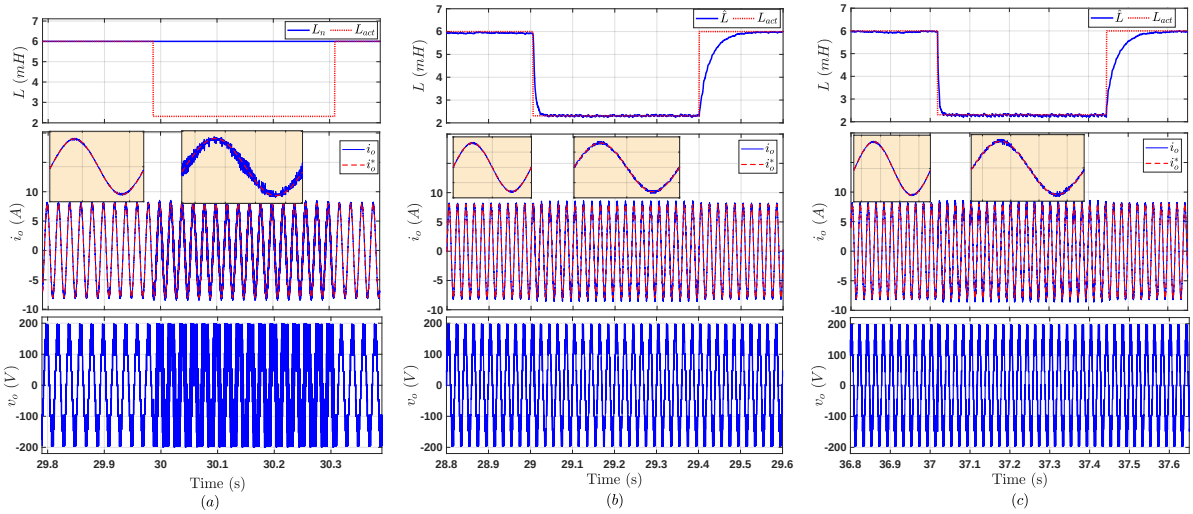


Figure 6.14: Experimental results for a mismatch in the filter inductance L: (a) Algorithm I, (b) Algorithm II, and (c) Algorithm III.

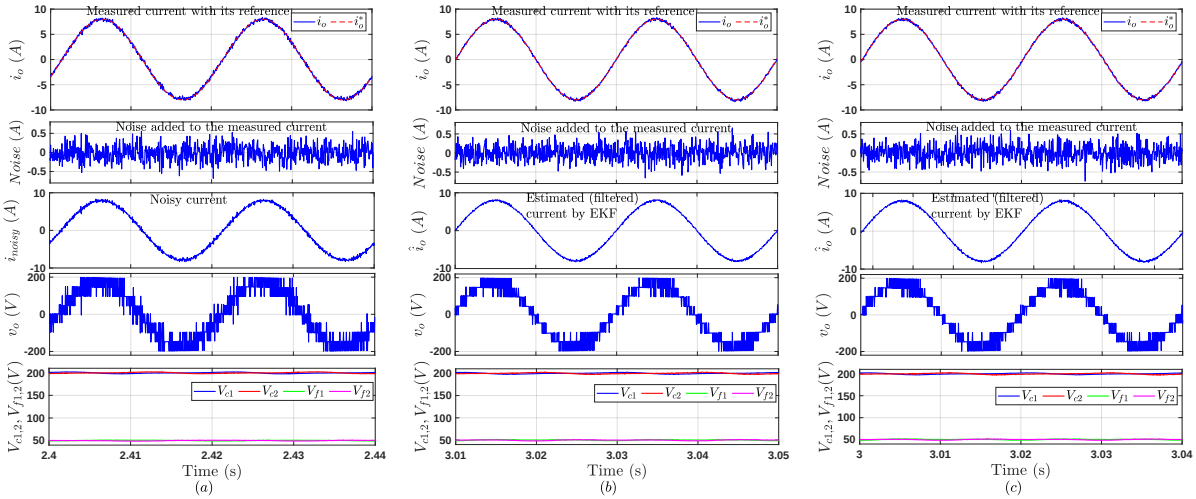


Figure 6.15: Experimental results with noise injection into the measured current: (a) Algorithm I, (b) Algorithm II, and (c) Algorithm III.

the load resistance mismatch has a negative impact on the steady-state error of the current control. The steady-state experimental comparison for this case is given in Table 6.7. Similarly, the performance is investigated for a step-change of -60% in the actual system inductance, where L_{act} is changed from 6 mH to 2.4 mH and then back to 6 mH, and the results for this case are shown in Fig. 6.14. As can be seen, $\hat{L}$ follows L_{act} with low steady-state error for algorithms II and III. Algorithm I has high values current ripples and distorted current and voltage waveform. The results of this test are summarized in Table 6.8. The performance indicators e_i, THD$_i$, and THD$_v$ were found 10.75%, 19.60%, and 85.52%, respectively, while algorithms II and III have much lower values of these parameters as given in Table 6.8. Also, it is obvious that the control performance reacts more sensitively to the system inductance than to the resistance.

Table 6.10: Execution time comparison of the experimental implementation.

Method	MPC Code	EKF Code	Additional Time for Auxiliary Tasks	Total Time
Algorithm I	5.4 μs	-	5.9 μs	11.3 μs
Algorithm II	5.2 μs	4.1 μs	5.9 μs	15.2 μs
Algorithm III	2.7 μs	4.1 μs	5.9 μs	12.7 μs

Table 6.11: Steady-state experimental comparison for Different levels operation Modes.

Method	Operation Mode	e_i	THD$_i$	THD$_v$
Algorithm II	Nine-level	1.32%	2.20%	22.08%
	Seven-level	1.94%	3.29%	32.37%
	Five-level	2.10%	3.40%	34.60%
Algorithm III	Nine-level	1.28%	2.13%	21.02%
	Seven-level	1.86%	3.20%	31.70%
	Five-level	2.10%	3.40%	34.14%

To investigate the filtering capability of the designed EKF and the control performance under noise injection, white noise is added to the measured current as shown in Fig. 6.15. In the conventional MPC method, the noisy current (i_{noisy}) degrades the control performance, resulting in higher harmonic contents in the inverter current and voltage, as depicted in Fig. 6.15a. Whereas for algorithms II and III, i_{noisy} is filtered by the EKF and the estimated current i_o^* is inputted to the control, resulting in better control performance with much lower harmonic contents of i_o and v_o. The results of this test are summarized in Table 6.9, which verifies the practicability of the developed MPC methods under noise injection.

6.6.4 Execution time

To compare the computational burden of the designed MPC methods, the execution time is considered as a performance indicator in the comparison. The three algorithms are implemented on the same real-time controller (dSPACE Microlabbox). The total execution time of each method is measured from the controlDesk software using *turnaroundTime* variable in the task info tab. The execution time of algorithm parts can also be measured from controlDesk via *atomic subsystems*. Table 6.10 shows the execution times for the three MPC algorithms. Thanks to the achieved computational reduction of algorithm III compared to the other two method, the MPC code has the minimum execution time 2.7 μs, achieving a reduction percentage of 50% compared to algorithm I and 48% compared to algorithm II. Since algorithm I has no parameter estimator, it has the minimum total execution time, 11.3 μs compared to 15.2 μs and 12.7 μs for algorithms II and III, respectively.

6.6.5 Different levels operation modes

In this section, experimental tests are performed to verify the effectiveness of the proposed algorithms II and III to continue converter operation with lower voltage levels even in the event

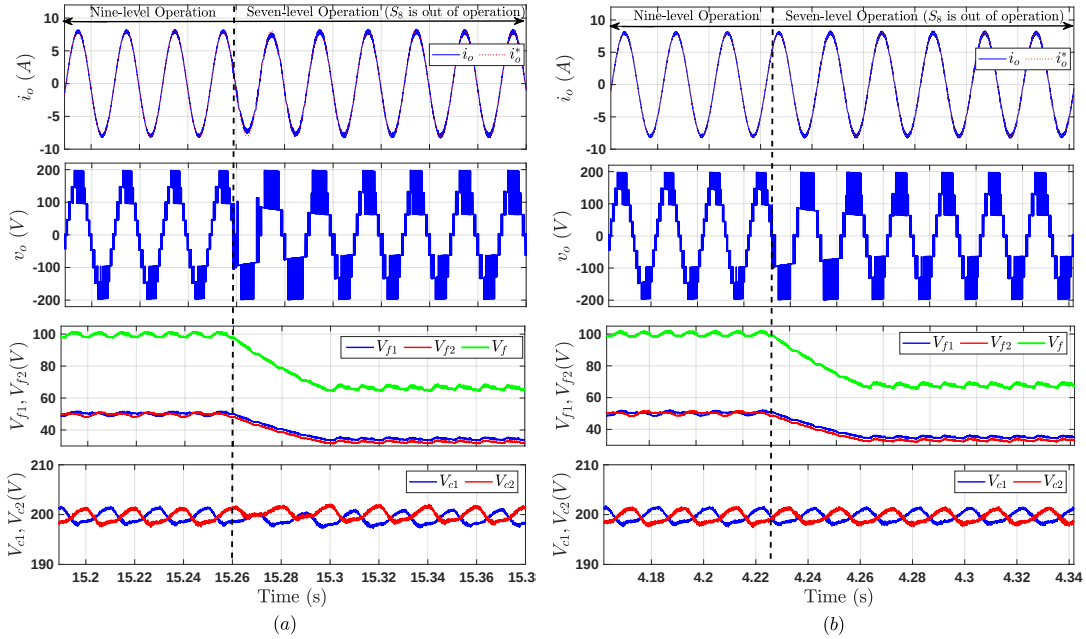


Figure 6.16: Experimental waveforms for switching to seven-level mode: (a) Algorithm II and (b) Algorithm III.

of a failure in the four-quadrant switch S_8. i_o^* is set to 8 A in all operating modes.

6.6.5.1 Switching between nine- and seven-level modes

Fig. 6.16 shows the waveforms of i_o, v_o, V_{f1}, V_{f2}, V_{c1}, and V_{c2} for switching the operation to the seven-level mode. As it can be seen, at a certain time, the operation is switched from the conventional case as a nine-level inverter to the seven-level mode. For the two proposed MPC methods, the transition is realized with a fast transient performance and the two FCs are seen as one capacitor C_f maintained at its modified reference $V_{dc}/6$ (66.7 V). The dc-link capacitors are also strongly balanced in all conditions.

6.6.5.2 Switching between nine- and five-level modes

Fig. 6.17 depicts the experimental waveforms for switching the converter operation to five-level mode. No transition time is required for the switching process as the reference value of the FC is the same as in the normal nine-level operation, as clear in the results.

The experimental performance of the proposed algorithms II and III in the three operating modes (nine-, seven-, and five-level mode) are summarized in Table 6.11. Three control objectives are realized in all cases with one weighting factor. It is clear from the results that better control performance is achieved with increasing levels, however, the control performance is acceptable in all operating modes.

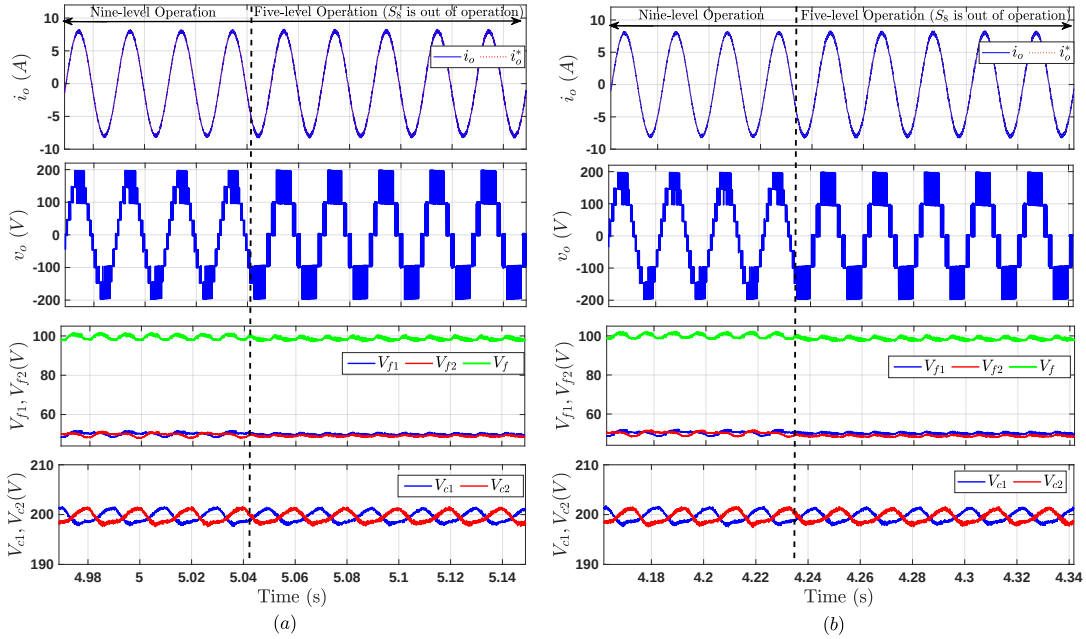


Figure 6.17: Experimental waveforms for switching to five-level mode: (a) Algorithm II and (b) Algorithm III.

6.7 Summary

In this chapter, two improved FCS-MPC algorithms have been presented and compared with the conventional method for hybrid FC-based topology with low active and passive components. The mathematical analysis, prediction models and cost function design have been described. Only one weighting factor is used to realize three control objectives under all operating conditions, which saves the cumbersome effort required to coordinate the weighting factors. The proposed FCS-MPC methods have addressed the parameter mismatch problem by designing an EKF-based parameter estimator. The developed algorithms empower the 9L-SC-ANPC to operate as a seven- or five-level inverter in the normal state or in case of a faulty bidirectional switch. According to the desired mode of operation, the proposed algorithms regulate the FCs voltages. Moreover, the number of iterations required to identify the optimal vector is significantly reduced, which in turn reduces the execution time of the MPC code as demonstrated by the experimental implementation. The feasibility and practicability of the proposed FCS-MPC methods have been verified through experimental implementation.

However, the designed MPC methods in this chapter have variable switching frequency as the conventional FCS-MPC, which will be addressed in Chapter 8. In addition, one weighting factor is still required; therefore, a Lyapanov-based weighting factorless MPC method is proposed in Chapter 9.

CHAPTER 7

Enhanced Robust Deadbeat Predictive Control for Nine-level FC-Based Converter

This chapter presents the design and experimental implementation of a robust DB-MPC for FC-based MLIs. The designed DB-MPC method is described in Section 7.2. The experimental implementation, results and performance evaluations are presented in Section 7.3. The summary of the chapter is given in Section 7.4.

7.1 Introduction

Continuous control set MPC (CCS-MPC) and deadbeat MPC (DB-MPC) are two different types of MPC that offer a constant switching frequency and reduced steady-state error [68, 69]. The first method requires complex mathematical formulations and a digital platform with high computing power, and in some cases solving the control problem offline is inevitable. While DB-MPC significantly reduces the computational load by directly calculating the reference voltage that nullifies the current error at the next sample using the system-discrete model. Then, a modulation stage is used to generate the pulses for switches. DB-MPC cannot process multiple targets during the reference voltage calculation. However, handling multiple objectives is still possible during the modulation stage and is subject to the availability of the redundant states of the converter under consideration.

Influenced by the challenges discussed in Chapter 5 (see Section 5.5.2), an improved DB-MPC method for FC-based MLIs is proposed in this chapter, addressing the issues of traditional FCS-MPC such as high computational load, variable switching frequency, weighting factors tuning, and control sensitivity to parameter mismatch. The improved DB-MPC method includes several advantages. Firstly, it introduces a multi-objective low-complexity DB-MPC technique, simultaneously addressing current control, FCs balancing, and NP potential control. Secondly, the method incorporates an online parameters estimator utilizing EKF, contributing to the control performance's robustness. Additionally, the method guarantees continuous op-

eration of the 9L-SC-ANPC inverter even in the event of a four-quadrant switch failure. The method is experimentally validated on a single-phase 9L-SC-ANPC inverter. However, the extension of the method to three-phase implementation is straightforward.

7.2 Proposed DB-MPC

Multiple goals handling is one of the distinct features of the traditional FCS-MPC. On the other hand, DB-MPC is usually a single-objective control method. This is an important reason for interpreting the limited application of DB-MPC to MLIs as the control problem of MLIs is typically a multi-objective task. Fortunately, handling several targets in DB-MPC is still possible in the modulation stage if there are sufficient redundancies in the inverter states. However, the MLIs with a reduced number of switches are always accompanied by a reduction in the redundant states, which limits the number of variables that can be controlled. In this regard, MLIs are divided into three types; non-redundant, semi-redundant and redundant converters [291]. Due to the significant reduction in power devices, the considered 9L-SC-ANPC can be classified as a semi-redundant topology since the redundancies are available for only $\pm 2E$ and 0. Accordingly, the available redundancies are not sufficient to balance both FCs and NP potential with the conventional concept. Thus, the prime current tracking objective is realized from the conventional DB-MPC concept and FCs balancing is realized by exploiting the redundancies. Whereas the dc-link capacitors are stabilized through the power flow control in the converter without requiring further redundancies, as described later.

Referring to Fig. 6.1 and by adopting Euler method, the system equation in (6.1) is written as follows

$$v_o(k) = Ri_o(k) + L\frac{i_o(k+1) - i_o(k)}{T_s}. \tag{7.1}$$

As discussed before, the first control objective is current tracking, which means generating the inverter voltage that causes i_o to follow i_o^* at $(k+1)^{th}$ sample. To this end, $i_o(k+1)$ in (7.1) is replaced by $i_o^*(k+1)$ to get the inverter reference voltage $v_o^*(k)$ as follow

$$v_o^*(k) = Ri_o(k) + L\frac{i_o^*(k+1) - i_o(k)}{T_s}. \tag{7.2}$$

Note that $i_o^*(k+1)$ is obtained from Lagrange extrapolation as in the traditional FCS-MPC. Then, the calculated $v_o^*(k)$ is inputted to the carrier-based PD-PWM stage to generate the pulses.

7.2.1 Control of FCs and NP potential

As discussed in Chapter 3, there are redundant states for levels $\pm 2E$ that can be exploited to realize the FCs balancing. As the number of redundant states is limited and based on the voltage deviation of each capacitor, the priority should be first identified. In doing so, the priority P is determined as

$$P = \begin{cases} 1, \text{ if } |\Delta V_{f1}(k)| > |\Delta V_{f2}(k)|, \\ 0, \text{ if } |\Delta V_{f1}(k)| < |\Delta V_{f2}(k)|, \end{cases} \tag{7.3}$$

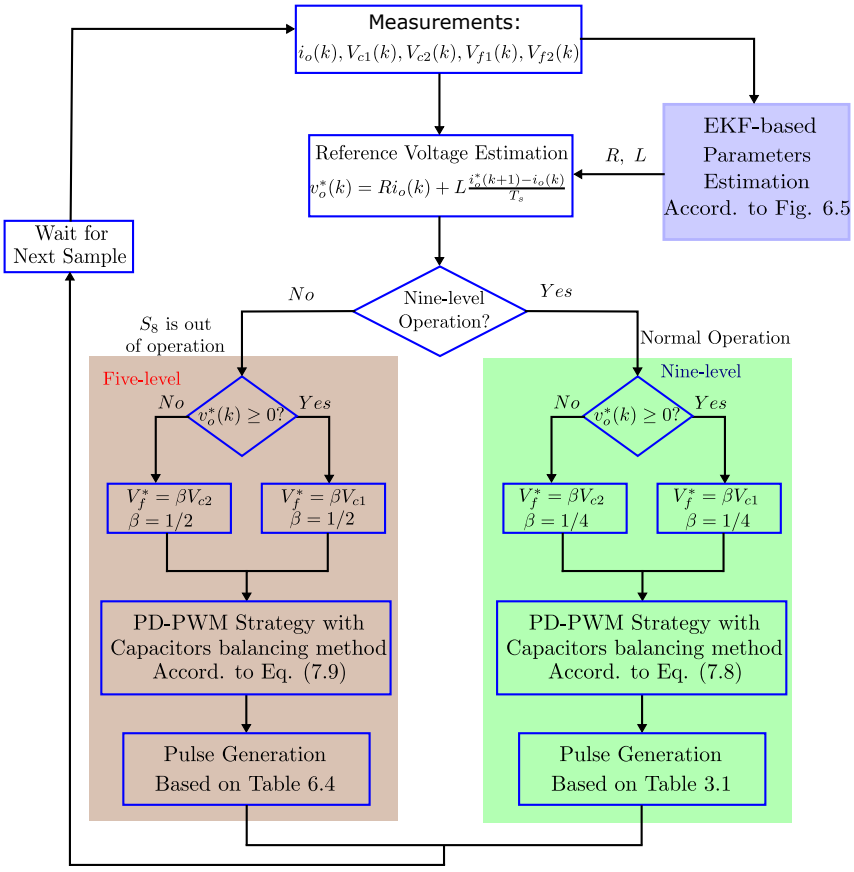


Figure 7.1: Flowchart of the proposed DB-MPC method.

where $\Delta V_{f1}(k)$ and $\Delta V_{f2}(k)$ are the voltage deviations of C_{f1} and C_{f2}, respectively, and are calculated as

$$\Delta V_{f1}(k) = V_f^*(k) - V_{f1}(k), \quad \Delta V_{f2}(k) = V_f^*(k) - V_{f2}(k). \tag{7.4}$$

Assuming that C_{f1} has priority (P=1) and the inverter is generating voltage level $+2E$, switching state V_3 or V_4 should be applied based on the polarity of the $\Delta V_{f1}(k)$ and $i_o(k)$. For example, if $V_{f1}(k)$ is lower than its reference V_f^* ($\Delta V_{f1}(k) > 0$), V_3 is applied for $i_o(k) \geq 0$ and V_4 is applied for $i_o(k) < 0$ to charge the capacitor and increase its voltage. To this end, a Heaviside function $H(y)$ is defined as

$$H(y) = \begin{cases} 1, & \text{if } y \geq 0 \\ 0, & \text{if } y < 0. \end{cases} \tag{7.5}$$

According to (7.5), $f(\Delta V_{fi})$ is given as

$$H(\Delta V_{fi}) = \begin{cases} 1, & \text{if } \Delta V_{fi}(k) \geq 0 \\ 0, & \text{if } \Delta V_{fi}(k) < 0, \end{cases} \tag{7.6}$$

where $i = \{1, 2\}$ represent the FC number. Similarly, $f(i_o)$ is written as

$$H(i_o) = \begin{cases} 1, & \text{if } i_o(k) \geq 0 \\ 0, & \text{if } i_o(k) < 0. \end{cases} \tag{7.7}$$

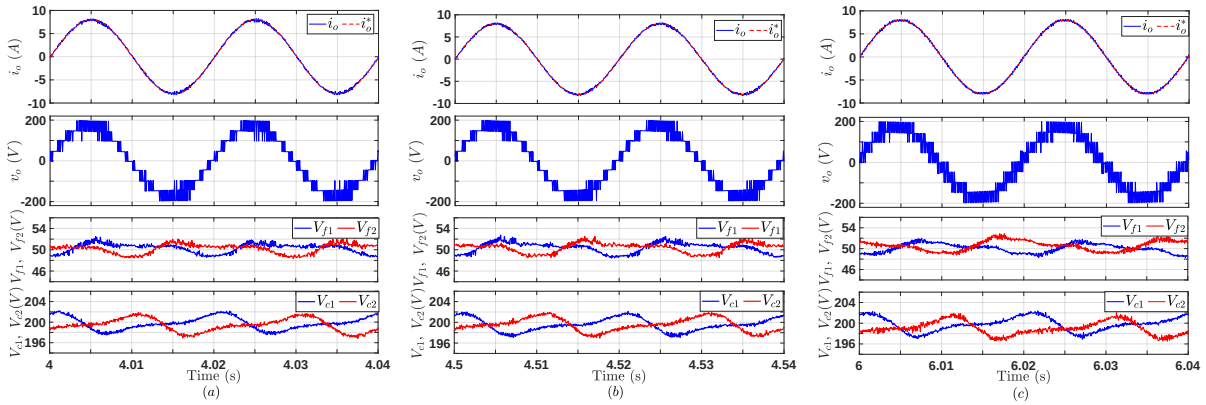


Figure 7.2: Experimental waveforms: (a) Traditional FCS-MPC, (b) Single-predictive FCS-MPC, and (c) Proposed DB-MPC.

Hence, the state of $\pm 2E$ to be applied is selected as

$$\left.\begin{aligned} V_{2E} &= P\{V_4[H(\Delta V_{f1}) \oplus H(i_o)] + V_3[H(\Delta V_{f1}) \odot H(i_o)]\} + \\ &\quad \bar{P}\{V_4[H(\Delta V_{f2}) \oplus H(i_o)] + V_3[H(\Delta V_{f2}) \odot H(i_o)]\}, \\ V_{-2E} &= P\{V_{10}[H(\Delta V_{f1}) \oplus H(i_o)] + V_9[H(\Delta V_{f1}) \odot H(i_o)]\} + \\ &\quad \bar{P}\{V_{10}[H(\Delta V_{f2}) \oplus H(i_o)] + V_9[H(\Delta V_{f2}) \odot H(i_o)]\}. \end{aligned}\right\} \tag{7.8}$$

where $\oplus$ and $\odot$ represent the logical operations XOR and XNOR, respectively. Equation (7.8) defines the appropriate switching state that reduces the voltage deviation of the FCs based on the direction of i_o and the actual FCs voltages. First, after sensing $V_{f1}(k)$ and $V_{f2}(k)$, the priority is determined based on $\Delta V_{f1}(k)$ and $\Delta V_{f2}(k)$ according to (7.3). Then, taking $+2E$ as an example and assume that the FC with the priority has a voltage lower than its reference ($\Delta V_{fi} > 0$), V_3 is applied if $i_o(k) \geq 0$ and V_4 is applied if $i_o(k) < 0$ to charge this FC, as shown in Table 3.1. The same concept is valid for $-2E$. For the operation in the five-level mode, the redundant states of $\pm 2E$ in Table 6.4 can be identified as

$$\left.\begin{aligned} V_{2E} &= V_3[f(\Delta V_f) \oplus f(i_o)] + V_2[f(\Delta V_f) \odot f(i_o)] \\ V_{-2E} &= V_7[f(\Delta V_f) \oplus f(i_o)] + V_6[f(\Delta V_f) \odot f(i_o)]. \end{aligned}\right\} \tag{7.9}$$

Since hybrid MLIs have a limited number of redundant states due to the reduction in the used components, the available redundancies are not sufficient to achieve NP potential control in addition to balancing the FCs, especially the single-phase operation. Therefore, the same method proposed in Chapter 6 with FCS-MPC to integrate the NP balance in FCs control objective is used here (See Section 6.4.1). The flowchart of the designed DB-MPC method is shown in Fig. 7.1.

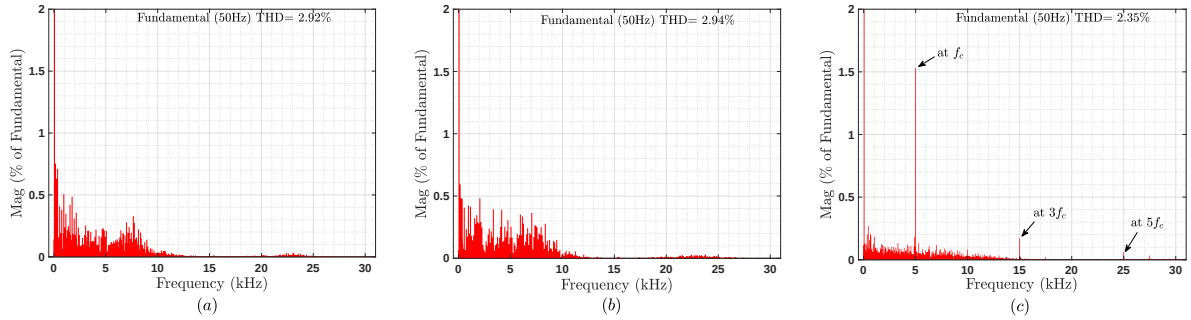


Figure 7.3: Harmonic spectrum of output current: (a) Traditional FCS-MPC, (b) Single-predictive FCS-MPC, and (c) Proposed DB-MPC.

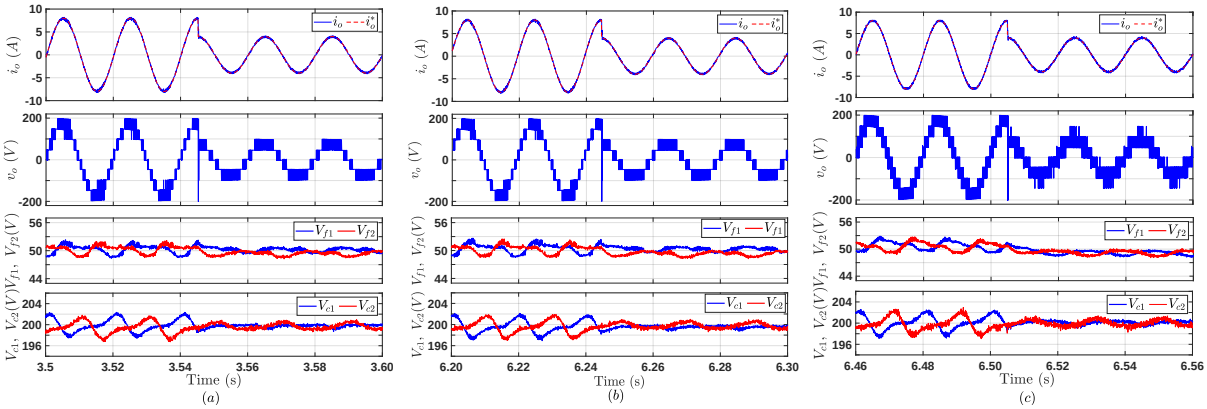


Figure 7.4: Experimental results for current step-change (8 A to 4 A): (a) Traditional FCS-MPC, (b) Single-predictive FCS-MPC, and (c) Proposed DB-MPC.

7.3 Experimental results

For the experimental validation, three distinct MPC methods are experimentally implemented and compared under the same operating conditions, which are defined as follows.
The first method is the conventional FCS-MPC algorithm. The second method is the single-predictive FCS-MPC. This method is first proposed in [187] for the conventional two-level converter and the 3L-NPC converter to eliminate the computational load required for the current prediction in FCS-MPC. Due to its high performance and low computational load, this concept is then applied to various converter topologies such as the 5L-ANPC inverter in [51] and the 3L T-type converter in [236]. To eliminate the calculation efforts required for the current prediction in this approach, the reference voltage that obliges i_o to follow i_o^* at $(k+1)^{th}$ sample is estimated by (7.2). Then, the current tracking objective is expressed in terms of voltage instead of current. Accordingly, the cost function in (6.12) of the conventional FCS-MPC is modified as follows:

$$\begin{aligned} g = [v_o^*(k) - v_o(k)]^2 + \lambda_{v1}[V_f^*(k+1) - V_{f1}(k+1)]^2 \\ \lambda_{v1}[V_f^*(k+1) - V_{f2}(k+1)]^2 + \lambda_{v2}[\Delta V_c(k+1)]^2, \end{aligned} \tag{7.10}$$

where λ_{v1} and λ_{v2} are two weighting factors. Note that instead of 12 $\times$ current predictions in traditional FCS-MPC, this method estimates the reference voltage only once per sample, so it is

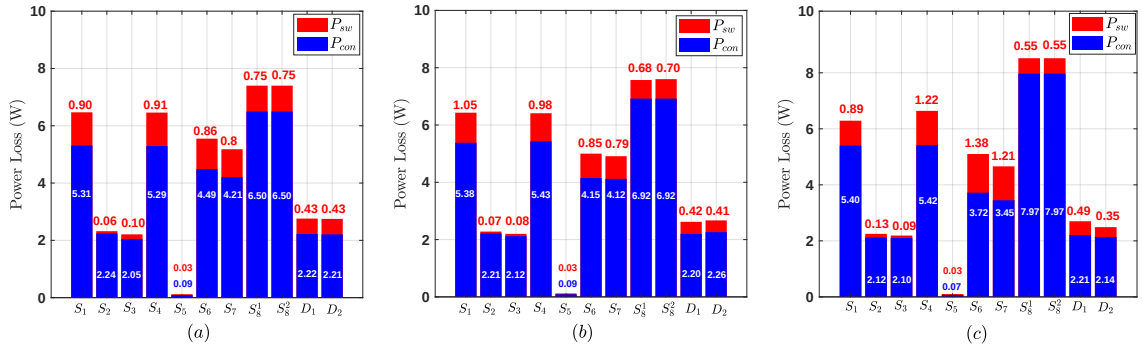


Figure 7.5: Conduction and switching losses of switches: (a) Traditional FCS-MPC, (b) Single-predictive FCS-MPC, and (c) Proposed DB-MPC.

called single-predictive FCS-MPC. However, it is still required to perform 12 $\times$ predictions for the FCs and dc-link voltages and 12 $\times$ cost function evaluation. The third implemented method is the designed DB-MPC in this chapter.

As previously discussed, the weighting factors λ_1 and λ_2 in traditional FCS-MPC and λ_{v1} and λ_{v2} in single-predictive FCS-MPC should be first tuned. For a fair and meaningful comparison with multiple control objectives, λ_1, λ_2, λ_{v1}, and λ_{v2} are tuned to give the same voltage ripples in the FCs and dc-link as in the DB-MPC method. Subsequently, the comparison can be assessed in terms of the current tracking as a prime control target. Considering the experimental parameters given in Table 6.5 and i_o^*=8 A, λ_1, λ_2, λ_{v1}, and λ_{v2} are determined by trial and errors and found to be 0.25, 0.06, 2700, and 450, respectively. Under these values, the three MPC methods have voltage tolerances of 3.5 V and 5 V in FCs and dc-link capacitors, respectively.

7.3.1 Steady-state and dynamic operation at nominal system parameters

For a fair comparison, the same average switching frequency f_s should be adopted for the MPC methods under consideration [29]. f_s of the 9L-SC-ANPC converter is calculated as

$$f_s = \frac{\sum_{i=1}^{8} f_{si}}{8}, \tag{7.11}$$

where f_{si} is the average switching frequency of switch S_i, with $i \in \{1, 2, 3, 4, 5, 6, 7, 8\}$, and is calculated based on the number of commutations n_{si} in the period T_c as $f_{si} = n_{si}/T_c$ [236]. The proposed DB-MPC method is validated experimentally at T_s= 50 μs and carrier frequency f_c= 5 kHz. According to (7.11), f_s of the DB-MPC is found to be 2 kHz. For the traditional and single-predictive FCS-MPC methods, a sampling period T_s of 65 μs is chosen to result in the same average switching frequency, f_s= 2 kHz. Fig. 7.2 shows the experimental steady-state waveforms for the three methods at i_o^*= 8 A. The plotted waveforms, from top to bottom, are reference i_o^* and measured i_o currents, inverter voltage v_o, FCs measured voltages V_{f1} and V_{f2}, and dc-link measured voltages V_{c1} and V_{c2}. As it is clear for the three MPC schemes, i_o tracks i_o^* with high performance. v_o has nine steps in the fundamental cycle, reducing the voltage harmonic contents. The three MPC methods have balanced FCs with voltage ripples of 3.5 V. In addition, the capacitors of the dc-link are balanced with voltage ripples of 5 V. The spectrum of the current harmonics is shown in Fig. 7.3. As can be seen, all MPC methods have

Table 7.1: Performance comparison at steady-state operation with nominal system parameters R and L.

Method	e_i	THD$_i$	THD$_v$	f_s
Traditional FCS-MPC	1.86%	2.92%	22.10%	2 kHz
Single-predictive FCS-MPC	1.88%	2.94%	22.05%	2 kHz
Proposed DB-MPC	1.61%	2.35%	23.44%	2 kHz

very low THDs, valued at 2.92%, 2.94%, and 2.35% for the traditional, single-predictive FCS-MPC, and the proposed DB-MPC, respectively. However, the harmonics in the traditional and single-predictive FCS-MPC methods are distributed over a wide frequency range, making filter design for grid-tied applications a challenging task. In contrast, for the DB-MPC method, the harmonics are concentrated at the carrier switching frequency and its multiples (f_c, $3f_c$, $5f_c$). For a clear and supported performance assessment, Table 7.1 lists three performance indicators for all methods, which are the mean absolute current error e_i [29] and the total harmonic distortion THD$_i$ and THD$_v$ of i_o and v_o, respectively. According to Table 7.1, the developed DB-MPC method has better values in terms of e_i and THD$_i$. To examine the transient operation, Fig. 7.4 depicts the waveforms for a sudden change in i_o^* (from 8 A, 50 Hz to 4 A, 50 Hz). From the results, all MPC schemes have a fast dynamic response and a very effective FCs and NP balancing.

A 5-kW single-phase model of the considered inverter is built in the PLECS software tool to evaluate the efficiency and investigate the power loss distribution among the power devices under the MPC methods. The analysis is performed with V_{dc}= 1 kV and i_o^*= 20 A. The same power switches utilized in the experimental implementation are adopted in PLECS simulation, where FF50R12RT4 IGBT and IDP30E65D1 diode manufactured by *Infineon* are utilized with the thermal and losses description provided by the manufacturer. The resulting switching P_{sw} and conduction P_{con} losses are given in Fig. 7.5. Note that the four-quadrant switch S_8 consists of two power devices, denoted as S_8^1 and S_8^2. From Fig. 7.5, one can observe that the conduction losses of the power devices are much higher than the switching losses in all MPC schemes. In addition, the three MPC schemes have a very similar loss distribution, which can be interpreted as operating at the same average switching frequency. According to the loss analysis under the same conditions, the efficiency of the traditional, single-predictive FCS-MPC, and the DB-MPC is 98.93%, 98.91%, and 98.90%, respectively. An important observation from the power loss analysis is that the four-quadrant switch has the highest power loss compared to other switches, where S_8^1 and S_8^2 have about 32% of the total losses in the 9L-SC-ANPC inverter. This confirms the feasibility of the suggested DB-MPC strategy to ensure converter operation under the failure condition of the four-quadrant switch.

7.3.2 Operation under parameter mismatch and EKF-based estimation

In this test, the robustness and the estimating ability of the EKF-based estimator with variations in parameters R and L are investigated. For the traditional and single-predictive FCS-MPC, the system model assumes constant parameters equal to the nominal values R_n and L_n. While for the proposed DB-MPC, the model parameters used in the control algorithm are estimated using the designed EKF-based estimator and denoted as $\hat{R}$ and $\hat{L}$. Fig. 7.6 shows the experimental re-

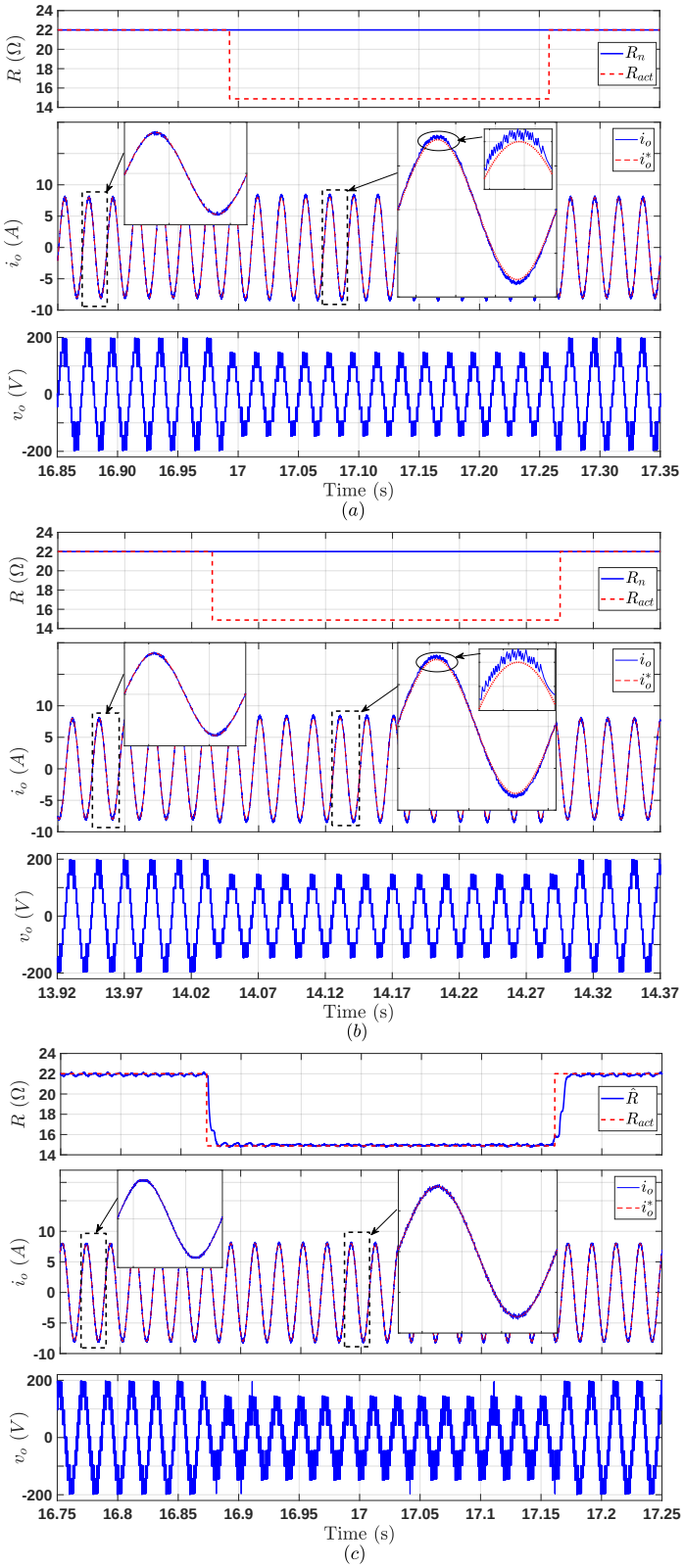


Figure 7.6: Experimental results for a mismatch in R: (a) Traditional FCS-MPC, (b) Single-predictive FCS-MPC, and (c) Proposed DB-MPC.

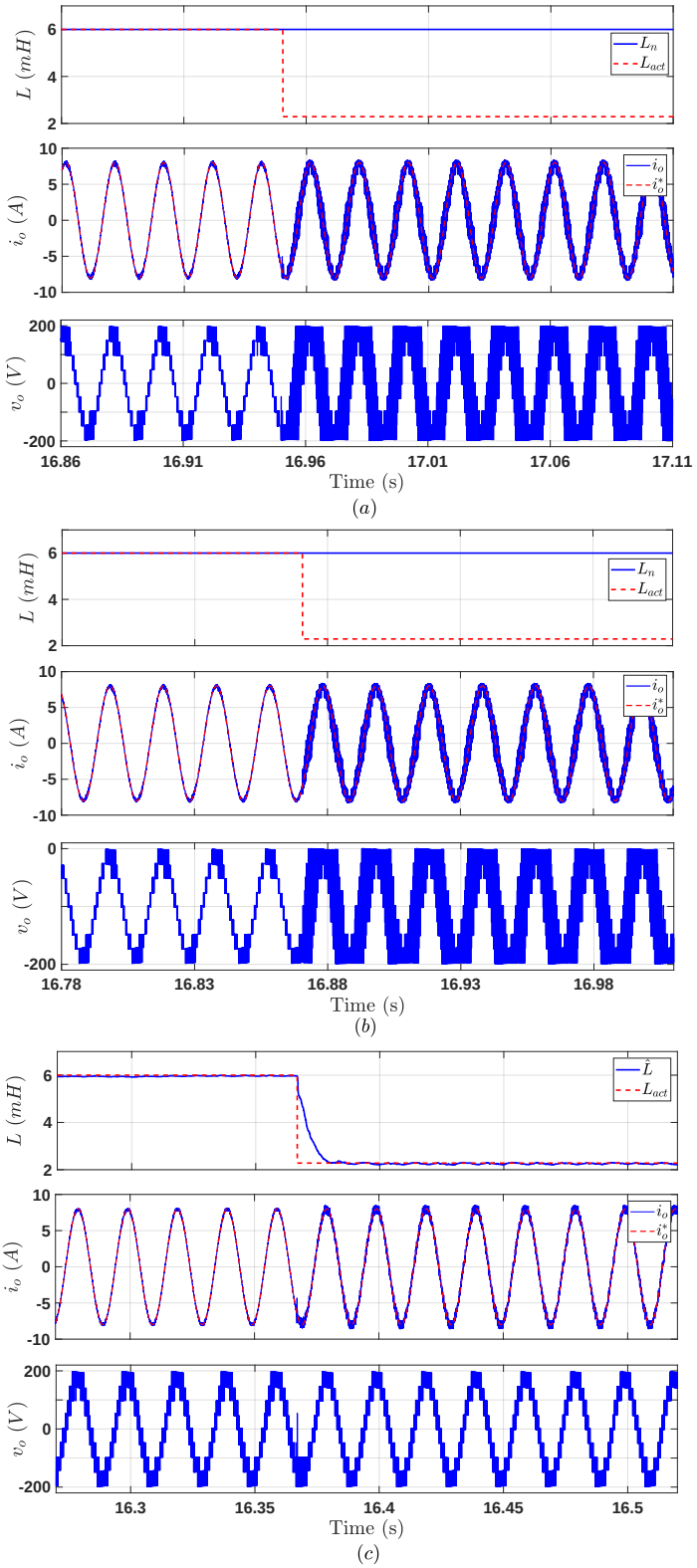


Figure 7.7: Experimental results for a mismatch in filter inductance L: (a) Traditional FCS-MPC, (b) Single-predictive FCS-MPC, and (c) Proposed DB-MPC.

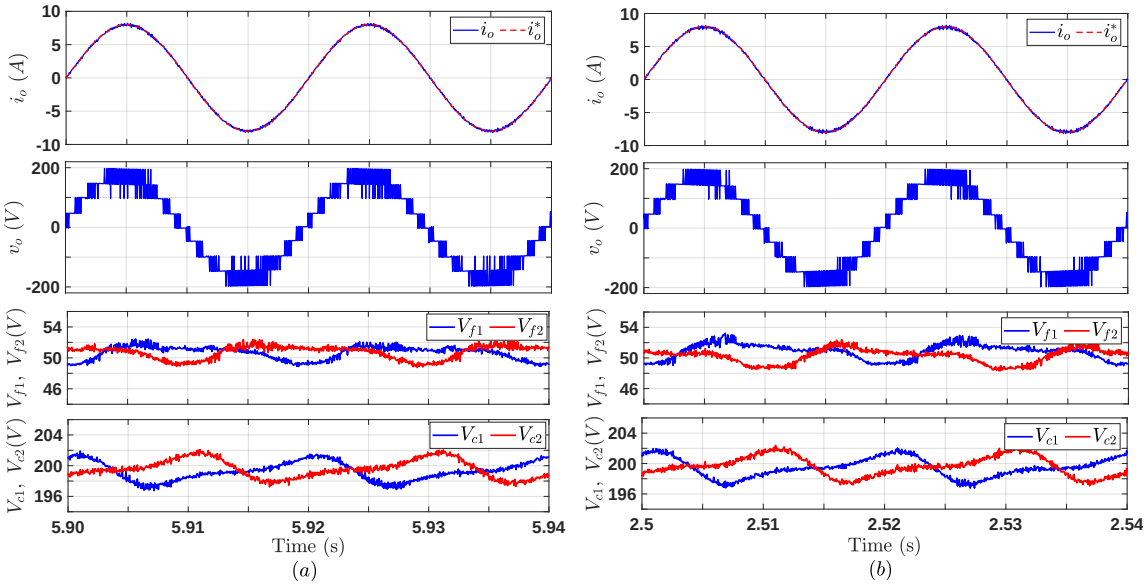


Figure 7.8: Experimental waveforms at T_s=50μs: (a) Traditional FCS-MPC, and (b) Single-predictive FCS-MPC.

Table 7.2: Performance comparison with a mismatch of -33.33% in R.

Method	e_i	THD$_i$	THD$_v$
Traditional FCS-MPC	3.23%	2.56%	25.50%
Single-predictive FCS-MPC	3.43%	2.67%	25.90%
Proposed DB-MPC	1.59%	2.30%	26.75%

sults for the change of the real system resistance between the nominal value (22 Ω) and another value (14.7 Ω), with a change percentage of 33.3%. As can be observed, for the proposed DB-MPC, the estimated resistance $\hat{R}$ follows the actual value $\hat{R}$ with a fast dynamic response and very low steady-state error. As a result, the control has high tracking quality in terms of current control despite the significant change in R_{act}. While for other FCS-MPC methods, due to the mismatch between R_{act} and R_n, a steady-state error is observed in the current. The control performance in this case in terms of e_i, THD$_i$ and THD$_v$ is summarized in Table 7.2. The control performance with filter inductance variation is depicted in Fig. 7.7, where L_{act} is varied from 6 mH to 2.4 mH ($\Delta L = -60\%$). As can be seen, the designed EKF-based estimator can accurately estimate the actual filter inductance, resulting in an acceptable control performance even with a -60% reduction in the filter inductance. For FCS-MPC, very high ripples are observed in the current and also the inverter voltage is highly distorted. The considered performance indicators are summarized in Table 7.3, which shows a clear superiority of the proposed DB-MPC over traditional and single-predictive FCS-MPC methods.

7.3.3 Performance evaluation at the same control period T_s

As discussed in Section 7.3.1, The performance of the MPC methods is compared at the same average switching frequency f_s, which necessitated the implementation of the traditional and

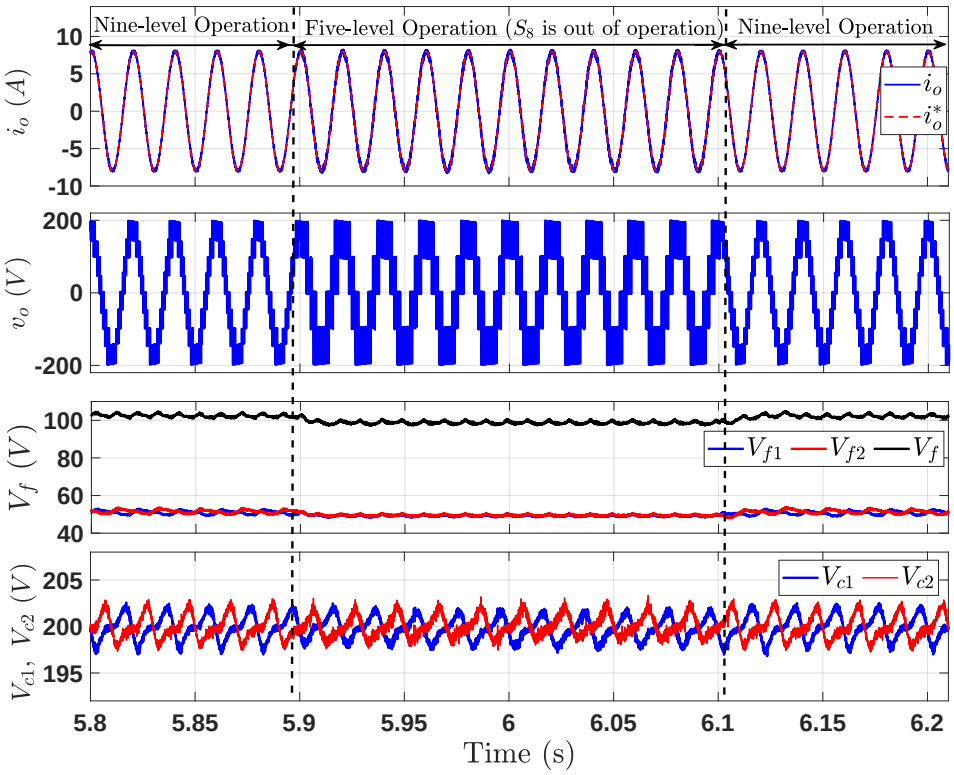


Figure 7.9: Experimental results of the proposed DB-MPC with a failure in the four-quadrant switch S_8.

Table 7.3: Performance comparison with a mismatch of -60% in L.

Method	e_i	THD$_i$	THD$_v$
Traditional FCS-MPC	15.63%	28.16%	90.87%
Single-predictive FCS-MPC	17.82%	29.95%	91.87%
Proposed DB-MPC	3.92%	4.97%	20.30%

Table 7.4: Performance comparison at the same control period, $T_s = 50$ μs.

Method	Tuned Parameters	e_i	THD$_i$	THD$_v$	f_s
Traditional FCS-MPC	λ_1, λ_2	1.57%	2.42%	22.52%	2.35 kHz
Single-predictive FCS-MPC	λ_{v1}, λ_{v2}	1.62%	2.46%	22.18%	2.35 kHz
Proposed DB-MPC	-	1.61%	2.35%	23.44%	2 kHz

single predictive FCS-MPC methods at $T_s = 65$ μs to get f_s= 2 kHz as in the proposed DB-MPC method. In this section, the performance is compared at the same control period by experimentally implementing the traditional and single-predictive FCS-MPC methods at $T_s = 50$ μs. Fig. 7.8 shows the experimental waveforms of the FCS-MPC methods at $T_s = 50$ μs. The comparison between all MPC methods, in this case, is summarized in Table 7.4. Accordingly, all MPC strategies have almost similar values concerning the tracking error e_i, THD$_i$, and THD$_v$.

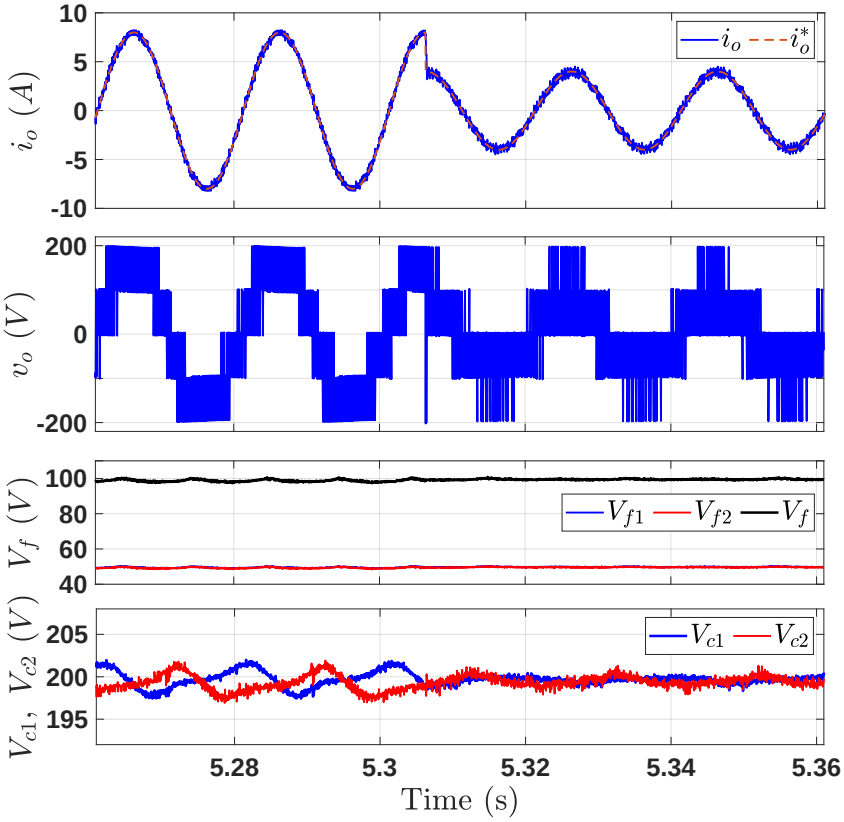


Figure 7.10: Experimental waveforms of the proposed DB-MPC in the five-level mode (open-circuit failure in S_8) with a current step-change.

Table 7.5: Execution time of the traditional and proposed DB-MPC.

Method	Control Algorithm	EKF Algorithm	Time of Auxiliary Tasks	Total Time
Traditional FCS-MPC	5.40 μs	-	5.90 μs	11.30 μs
Single-predictive FCS-MPC	5.10 μs	-	5.90 μs	11 μs
Proposed DB-MPC	1.10 μs	4.10 μs	5.90 μs	11.10 μs

Nevertheless, in contrast to DB-MPC, the harmonics in FCS-MPC methods are distributed over a wide frequency range, complicating the filter design, as previously discussed. In addition, the average switching frequency f_s of the two FCS-MPC methods is increased by 17.5%, 2.35 kHz compared to 2 kHz in the proposed DB-MPC method. No weighting factors are required in the proposed DB-MPC method. In contrast, two weighting factors are used in the FCS-MPC methods. Estimating the weighting factor is non-trivial and one of the ongoing research topics. Complex numerical models are usually required by performing numerous experiments and simulations under different operating conditions [215].

7.3.4 Execution time

Computational load is one of the issues of MPC-based methods. To investigate this aspect, the execution times of traditional FCS-MPC and DB-MPC are measured on the same digital platform (dSPACE Microlabbox). The total required time for the implementation is monitored from ControlDesk by *turnaroundTime* variable. In addition, the time required to execute algorithm sub-parts is also measured through *atomic subsystems*. The measured times of the three MPC methods are listed in Table 7.5. Accordingly, the suggested DB-MPC has a much shorter time for MPC code compared to FCS-MPC, where DB-MPC requires only 1.1 μs compared to 5.1 μs for the single-predictive FCS-MPC and 5.4 μs for traditional FCS-MPC. The reduction is achieved because, unlike FCS-MPC, neither current, FCs and dc-link voltage predictions nor cost function optimization are required. Although the designed EKF-based estimator is integrated into the proposed DB-MPC, the total execution time is still lower than the traditional method, where 11.1 μs is required for the whole developed DB-MPC method compared to 11.3 μs for traditional FCS-MPC.

7.3.5 Operation under the failure of the four-quadrant switch S_8

As theoretically discussed, with the proposed DB-MPC, the 9L-SC-SNPC can continue to operate even in a failure condition of the four-quarter switch S_8. In this test, the operation is experimentally verified with an open-circuit fault in S_8. Fig. 7.9 shows the experimental results for this case. As can be seen, in normal operation, the inverter produces a nine-level voltage waveform, and when a fault occurred in S_8, the 9L-SC-ANPC was directly changed to the five-level mode with no transient time because the FCs were still stabilized at the same voltage. C_{f1} and C_{f2} are seen as on capacitor with a voltage V_f balanced at $V_{dc}/4$ (100 V). It is also clear that the dc-link capacitors are well balanced in all cases. The operation is also experimentally validated in the five-level mode with a step-change in i_o^* from 8 A to 4 A in Fig. 7.10. The results prove the ability of the proposed DB-MPC with the 9L-SC-ANPC topology to operate with a faulty state of S_8 in steady-state and dynamic operation. As expected, due to the reduction of the voltage levels to five, an increase is observed in the tracking errors and harmonic contents compared to the nine-level normal operation, where e_i, THD$_i$ and THD$_v$ were found to be 3.10%, 4.25% and 35.10%.

7.4 Summary

In this chapter, an improved robust DB-MPC method was designed. This method has been applied to single-phase FC-based MLIs and can be extended to three-phase inverters in a straightforward manner. From the experimental results, the advantages of the designed DB-MPC are summarized as follows:

1. Like the FCS-MPC, the designed DB-MPC addresses multiple control goals; current control, FCs balance and NP potential control. Moreover, unlike FCS-MPC, no weighting factors are required, saving the cumbersome effort required to tune the weighting factors;

2. Thanks to the designed EKF-based estimator, the proposed method has better robustness compared to the traditional FCS-MPC;

3. Like the traditional FCS-MPC at the nominal system parameters, the proposed DB-MPC has high tracking quality and an effective balance of FCs and NP in steady-state and dynamic operation;

4. Comparing with FCS-MPC, the developed DB-MPC has a lower calculation burden;

5. The proposed DB-MPC scheme allows the 9L-SC-ANPC to continue operating with the generation of five levels in the open-circuit failure condition of the four-quadrant switch, improving the fault tolerance of the inverter.

Since the FCs balancing is realized using the available redundancies in PWM-based schemes, the operation at low line frequencies is limited with the DB-MPC method due to the low number of redundant vectors hybrid MLIs. Therefore, this issue is addressed in the next chapter by proposing a dual-vector MPC method that improves the balancing and reduces the size of the FCs.

CHAPTER 8

Low-Complexity Dual-Vector Model Predictive Control for Single-Phase Hybrid MLIs

This chapter proposes a dual-vector FCS-MPC method for constant switching frequency operation and better FCs control. Mathematical analyzes have been carried out to determine the optimal duration of the selected voltage vectors in Section 8.2.2. The sequence of the two voltage vectors is identified based on the total harmonic distortion (THD) definition to minimize its value in Section 8.2.3. Compared with standard FCS-MPC, lower steady-state errors, lower THDs, better harmonic distribution, and shorter execution times are achieved. The proposed MPC method is validated in Section 8.3, and the chapter summary is given in Section 8.4.

8.1 Introduction

Due to the lack of a modulator stage in the conventional FCS-MPC, only one voltage vector is applied during the entire control cycle, resulting in a high steady-state error and variable switching frequency. The latter results in a wide harmonic spectrum and, hence, complicates the filter design. One effective approach for this issue is the modulated MPC (M2PC). The adoption of the M2PC for single-phase MLCs was first proposed in [52] for a seven-level CHB inverter. This method considers the modulation stage as part of the optimization process. Two vectors are applied at each control period with their durations setting inversely proportional to the values of the cost function. To reduce the switching frequency in this method, the previous vector is selected as the first one in the next sample, while the second is identified from the cost function evaluation. Although the control performance is improved compared to conventional MPC, only the current tracking is considered as a control objective in this work. The MPC concept based on the optimal switching sequence (OSS) is proposed for the first time in [219] for single-phase NPC converters. The idea behind this approach is to divide the available states of the converter into a lower number of sets, four sets with three vectors in each one for the NPC converter. Then, the corresponding times of the vectors in each set are determined considering the current

slope method. The optimal sequence is finally identified by evaluating the cost function for all combinations. This method achieves a high tracking quality with an improved harmonic spectrum, but the computational effort is high and the design of the switching sequence is a complex task for high-level MLCs. The adoption of this approach, taking into account the dc-link balancing as an additional control objective for single-phase NPC converter, is reported in [197, 235]. A similar FCS-MPC algorithm is described in [236] for single-phase T-type MLC by applying three vectors for each control period. Furthermore, dc-link balancing is realized by exploiting the availability of redundant states, eliminating the need for a weighting factor. However, the cost function is evaluated in terms of the estimated reference voltage, which increases the control sensitivity of the control to system parameters. Two double-vector FCS-MPC algorithms are presented in [51] for single-phase five-level ANPC inverter. The first method determines the application times of the vectors based on the cost function while the second adopts the current slope concept. Three control objectives are well achieved, current tracking, dc-link balancing and stabilization of the FCs. However, this method is based on Lyapunov function, which causes the FCS-MPC to lose the advantage of simplicity.

Motivated by the discussed problematic issues of the classic FCS-MPC, this chapter proposes a computationally-efficient dual-vector FCS-MPC for FC-based MLIs. The developed MPC scheme is applied to single-phase 9L-SC-ANPC converter as a case study. The main contributions of this chapter can be summarized as follows:

1. The computational burden of the FCS-MPC has been significantly reduced by directly locating the best two vectors without the need for multiple evaluations of the cost function as in the conventional algorithm, while achieving a high tracking quality of the current and a strong balancing of the dc-link and FC,

2. Better steady-state performance with fixed switching frequency and an improved harmonic spectrum is realized.

3. Operation at low output frequencies with improved FC balance is realized, and

4. Low steady-state error and better harmonic spectrum are realized with two vector application. The sequence of the two voltage vectors is identified based on the THD definition to minimize its value. Mathematical analyzes were carried out to determine the optimal duration of the applied voltage vectors.

It is worth mentioning that the NP of the dc-link is balanced here using the method presented in Chapter 6 (See Section 6.4.1).

8.2 Proposed FCS-MPC

8.2.1 Double-vector selection

The primary control goal of the algorithm is to realize a current control, i.e. to identify the switching vector that forces i_o to track i_o^* at $(k+1)^{th}$ sample. Exploiting the deadbeat basic concept, the reference voltage $v_o^*(k)$ can be estimated by substituting $i_o(k+1)$ with its reference

Table 8.1: Switching vectors of the 9L-SC-ANPC converter (↓: discharging, ↑: charging, −: No change).

Switching State SW	Voltage Vector V	s_1	s_2	s_3	s_4	s_5	s_6	s_7	s_8	v_o	$i_o > 0$		$i_o < 0$	
											C_{f1}	C_{f2}	C_{f1}	C_{f2}
1	1	0	1	0	1	0	0	1	0	-4E	−	−	−	−
2	2	0	1	0	1	0	0	0	1	-3E	−	↓	−	↑
3	3	0	1	0	1	0	1	0	0	-2E	↓	↓	↑	↑
4	3	0	1	0	0	1	0	1	0	-2E	↑	↑	↓	↓
5	4	0	1	0	0	1	0	0	1	-E	↑	−	↓	−
6	5	0	1	0	0	1	1	0	0	0	−	−	−	−
7	5	0	0	1	0	1	0	1	0	0	−	−	−	−
8	6	0	0	1	0	1	0	0	1	+E	−	↓	−	↑
9	7	0	0	1	0	1	1	0	0	+2E	↓	↓	↑	↑
10	7	1	0	1	0	0	0	1	0	+2E	↑	↑	↓	↓
11	8	1	0	1	0	0	0	0	1	+3E	↑	−	↓	−
12	9	1	0	1	0	0	1	0	0	+4E	−	−	−	−

$i_o^*(k+1)$ in (6.1) as

$$v_o^*(k) = Ri_o(k) + L\frac{i_o^*(k+1) - i_o(k+1)}{T_s}. \tag{8.1}$$

Based on v_o^*, the optimal switching states from the current control point of view can be located. In doing so, mathematical relationships are derived in order to directly determine the switching states that correspond to a given converter voltage v_o. Table 8.1 lists the converter output voltage v_o, converter vector V and switching state SW of the 9L-SC-ANPC converter. In general, one can find a relationship between V and v_o for any single-phase MLC as follows

$$V = \frac{v_o}{E} + k_0, \tag{8.2}$$

where k_0 is a parameter that is calculated based on the number of level N as $k_0 = (N+1)/2$. For the considered 9L-SC-ANPC, $k_0 = (9+1)/2 = 5$. To determine which SWs correspond to a particular V, one can write this relationship as

$$\text{SW}_1 = V + k_1,\ \text{SW}_2 = V + k_2,\ ...\text{SW}_n = V + k_n, \tag{8.3}$$

where SW_1, SW_2, ...SW_n are the redundant states that generate the same voltage vector V. n is the maximum number of redundant states per level. k_1, k_2, ..k_n are parameters that are used to locate the available redundant states. For single-phase 9L-SC-ANPC, $n = 2$, k_1 and k_2 are determined as

$$\left.\begin{aligned} k_1 &= \text{round}(0.25|V-3| + |V-3|), \\ k_2 &= \text{round}(0.25|V-2| + |V-2|). \end{aligned}\right\} \tag{8.4}$$

Referring to (8.1), the calculated v_o^* is a continuous value while the converter voltage v_o is discrete as $v_o \in \{\pm 4E, \pm 3E, \pm 2E, \pm E, 0\}$. To allocate the nearest converter vectors V^x and

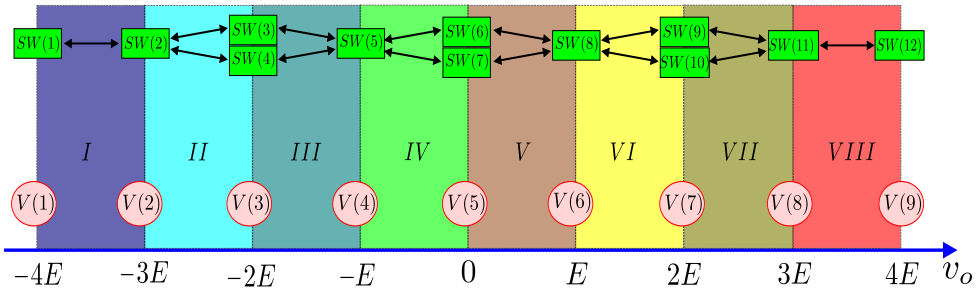


Figure 8.1: Voltage vectors of the single-phase 9L-SC-ANPC converter.

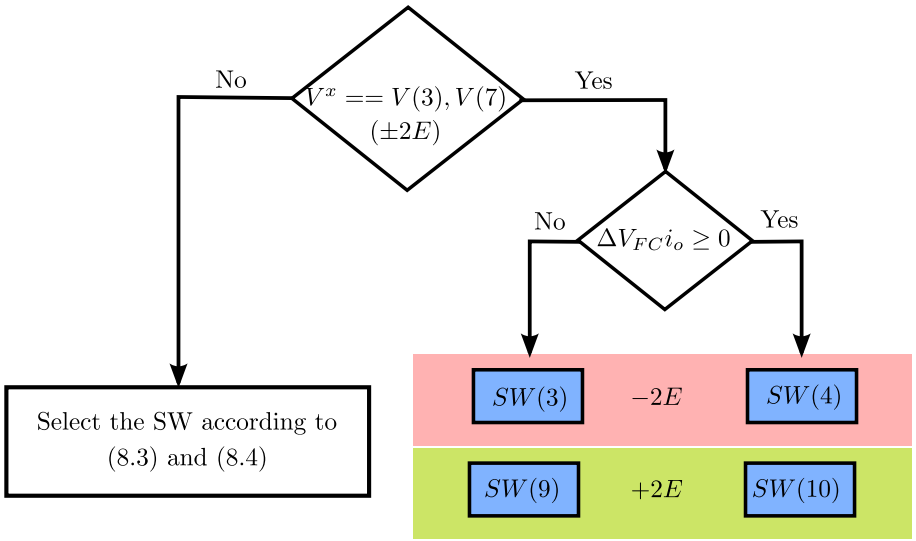


Figure 8.2: Redundancy selection for FCs balancing of the 9L-SC-ANPC converter.

V^y with taking into account the dual vector application, (8.2) is rewritten as

$$\left.\begin{aligned} V^x &= \text{ceil}(\tfrac{v_o^*}{E}) + k_0, \\ V^y &= \text{floor}(\tfrac{v_o^*}{E}) + k_0. \end{aligned}\right\} \tag{8.5}$$

The redundant states for V^x and V^y are calculated with (8.3) and (8.4). Fig. 8.1 illustrates the voltage vectors of the single-phase 9L-SC-ANPC inverter. Eight zones (from I to $VIII$) are formed based on the inverter voltage vectors. Only one region is considered based on the estimated v_o^* as in (8.1). For example, if v_o^* is in zone III, the appropriate vectors will be $V(3)$ and $V(4)$ then their corresponding SWs will be located for each vector based on the previous analysis.

8.2.2 FCs balancing

The FCs balancing in the proposed FCS-MPC is achieved in two steps, first by exploiting the available redundancy of a given V and second by modulating the duration times of the two applied vectors V^x and V^y.

The first stage is realized based on the actual values of FCs voltages and the direction of i_o. Referring to Table 8.1, there are two main key observations. First, the redundancies of $+2E$ and $-2E$ have an opposite effect on the FCs charging/discharging. Second, the influence on the two FCs C_{f1} and C_{f2} are the same during these redundant states. According to that, the proper switching state for FCs balancing can be selected. In doing so, the voltage deviation of the two FCs is calculated as

$$\Delta V_{fc} = 2V_f^* - (V_{f1} + V_{f2}). \tag{8.6}$$

Based on ΔV_{fc} and the output current i_o, the suitable state is chosen to balance the FCs. For illustration, for level $+2E$, if ΔV_{fc} is positive, the state that will charge the FCs should be chosen, which means SW(10) is selected for $i_o > 0$ and SW(9) is selected for $i_o < 0$. Fig. 8.2 shows the selection process of the redundant states of V^x. After selecting the proper state for V^x and V^y, the control objectives are evaluated in terms of the two vectors to determine the optimal duration times of V^x and V^y that minimize the control errors. Considering (8.1), the rate of change of i_o for vectors V^x and V^y can be expressed as

$$\left.\begin{aligned} f_{iV^x} &= \tfrac{d}{dt} i_o\big|_{V^x} = \tfrac{1}{L}(v_{o,V^x} - Ri_o), \\ f_{iV^y} &= \tfrac{d}{dt} i_o\big|_{V^y} = \tfrac{1}{L}(v_{o,V^y} - Ri_o). \end{aligned}\right\} \tag{8.7}$$

The predicted current $i_o(k+1)$ can be expressed as

$$i_o(k+1) = i_o(k) + f_{iV^x} T_x + f_{iV^y} T_y,\ T_x + T_y = T_s. \tag{8.8}$$

where T_x and T_y are the application times of V^x and V^y, respectively. Similarly, the rate of change of V_{f1} and V_{f2} for V^x can be obtained as

$$\left.\begin{aligned} f_{f1V^x} &= \tfrac{d}{dt} V_{f1}\big|_{V^x} = \tfrac{i_{f1,V^x}}{C_{f1}}, \\ f_{f2V^x} &= \tfrac{d}{dt} V_{f2}\big|_{V^x} = \tfrac{i_{f2,V^x}}{C_{f2}}. \end{aligned}\right\} \tag{8.9}$$

Accordingly, $V_{f1}(k+1)$ and $V_{f2}(k+1)$ are given as

$$\left.\begin{aligned} V_{f1}(k+1) &= V_{f1}(k) + f_{f1V^x} T_x + f_{f1V^y} T_y, \\ V_{f2}(k+1) &= V_{f2}(k) + f_{f2V^x} T_x + f_{f2V^y} T_y. \end{aligned}\right\} \tag{8.10}$$

Subsequently, the cost function is formulated as

$$\begin{aligned} g = {} & [i_o^*(k+1) - i_o(k+1)]^2 + \lambda[V_f^*(k+1) - V_{f1}(k+1)]^2 \\ & + \lambda[V_f^*(k+1) - V_{f2}(k+1)]^2. \end{aligned} \tag{8.11}$$

To obtain the optimal T_x and T_y, a partial derivative is performed for (8.11), i.e.,

$$\frac{\partial g}{\partial T_x} = 0. \tag{8.12}$$

By substituting (8.8) and (8.10) into (8.11) and performing the partial derivative in (8.12), T_x and T_y can be obtained as

$$\left.\begin{aligned} T_x &= \tfrac{A}{B}, \quad 0 \le T_x \le T_s, \\ T_y &= T_s - T_x, \; 0 \le T_y \le T_s, \end{aligned}\right\} \tag{8.13}$$

where A and B are expressed as

$$\left.\begin{aligned} A &= f_{iV^x} i_o^*(k+1) + \lambda f_{f1V^x} V_f^*(k+1) + \lambda f_{f2V^x} V_f^*(k+1) \\ &- f_{iV^x} i_o(k) - \lambda f_{f1V^x} V_{f1}(k) - \lambda f_{f2V^x} V_{f2}(k) - f_{iV^x} f_{iV^y} T_s \\ &- \lambda f_{f1V^x} f_{f1V^y} T_s - \lambda f_{f2V^x} f_{f2V^y} T_s, \\ B &= {f_{iV^x}}^2 + \lambda {f_{f1V^x}}^2 + \lambda {f_{f2V^x}}^2 - f_{iV^x} f_{iV^y} - \lambda f_{f1V^x} f_{f1V^y} \\ &- \lambda f_{f2V^x} f_{f2V^y}. \end{aligned}\right\} \tag{8.14}$$

8.2.3 Voltage vector sequence

After defining the two vectors to be used and calculating the duration times based on the control objectives, the optimal vector sequence is determined taking into account the THD and the mean absolute reference tracking error e_{i_o} of i_o as performance indicators for the current control.

Assuming a sinusoidal i_o^*, the THD can be expressed as

$$\text{THD} = \frac{\sqrt{\frac{1}{T}\int_0^T (i_o^* - i_o)^2 dt}}{i_{orms}^*}, \tag{8.15}$$

where i_{orms}^* is the rms value of i_o^*. Also, e_{i_o} is calculated as

$$e_{i_o} = \frac{\frac{1}{m}\sum_1^m |i_o^* - i_o|}{I_o^*}, \tag{8.16}$$

where m is a given number of samples used for e_{i_o} calculation. I_o^* is the amplitude of i_o^*. From (8.15) and (8.16), it is clear that the values of the THD and e_{i_o} mainly depend on the area $S = \int |i_o^* - i_o|\, dt$ enclosed by i_o and i_o^*. Accordingly, the voltage sequence that minimizes S should be selected. Recalling (8.7), the current changes Δi_{oV_x}, Δi_{oV_y} resulting from the application of V^x and V^y with the durations T_x and T_y, respectively, can be obtained as

$$\left.\begin{aligned} \Delta i_{oV^x} &= f_{iV^x} T_x = \tfrac{1}{L}(v_{o,V^x} - R i_o) T_x, \\ \Delta i_{oV^y} &= f_{iV^y} T_x = \tfrac{1}{L}(v_{o,V^y} - R i_o) T_y. \end{aligned}\right\} \tag{8.17}$$

The actual current tracking error $i_{err}(k)$ is calculated as

$$i_{err}(k) = i_o^*(k) - i_o(k). \tag{8.18}$$

Fig. 8.3 shows the current trajectories for four cases as follows:

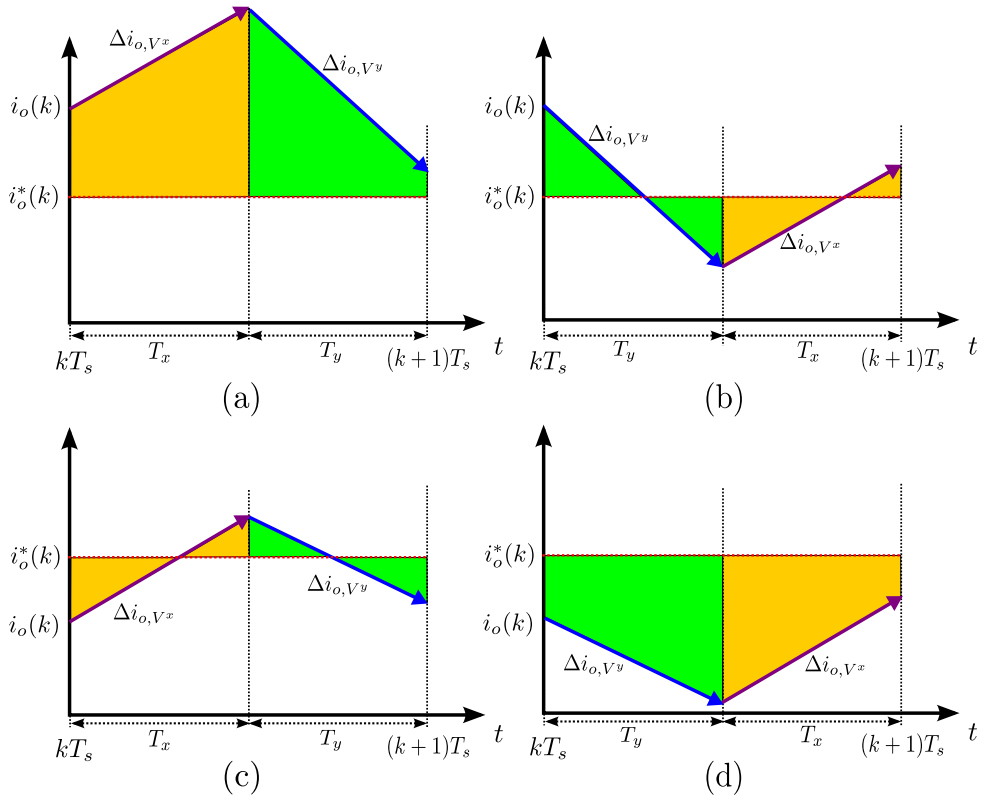


Figure 8.3: Current trajectories for different vector sequences: (a) $i_{err}(k) < 0$ with a vector sequence $\{V^x, V^y\}$. (b) $i_{err}(k) < 0$ with a vector sequence $\{V^y, V^x\}$. (c) $i_{err}(k) > 0$ with a vector sequence $\{V^x, V^y\}$. (d) $i_{err}(k) > 0$ with a vector sequence $\{V^y, V^x\}$.

Table 8.2: Voltage sequence selection.

$i_{err}(k)$	f_{iV^x}	f_{iV^y}	Optimal sequence
+	+	+	$\{V^x, V^y\}$
	+	-	
	-	-	
-	+	+	$\{V^y, V^x\}$
	+	-	
	-	-	

a) $i_{err}(k) < 0$ with a vector sequence $\{V^x, V^y\}$,

b) $i_{err}(k) < 0$ with a vector sequence $\{V^y, V^x\}$,

c) $i_{err}(k) > 0$ with a vector sequence $\{V^x, V^y\}$,

d) $i_{err}(k) > 0$ with a vector sequence $\{V^y, V^x\}$.

It should be noted that V^x is generated from the ceiling function of v_o^* as in (8.5), which will result in choosing the vector that leads to $v_o > v_o^*$, while V^y is produced from the floor function of v_o^* as in (8.5), producing $v_o < v_o^*$. Accordingly, the condition $f_{iV^x} > f_{iV^y}$, i.e. the current

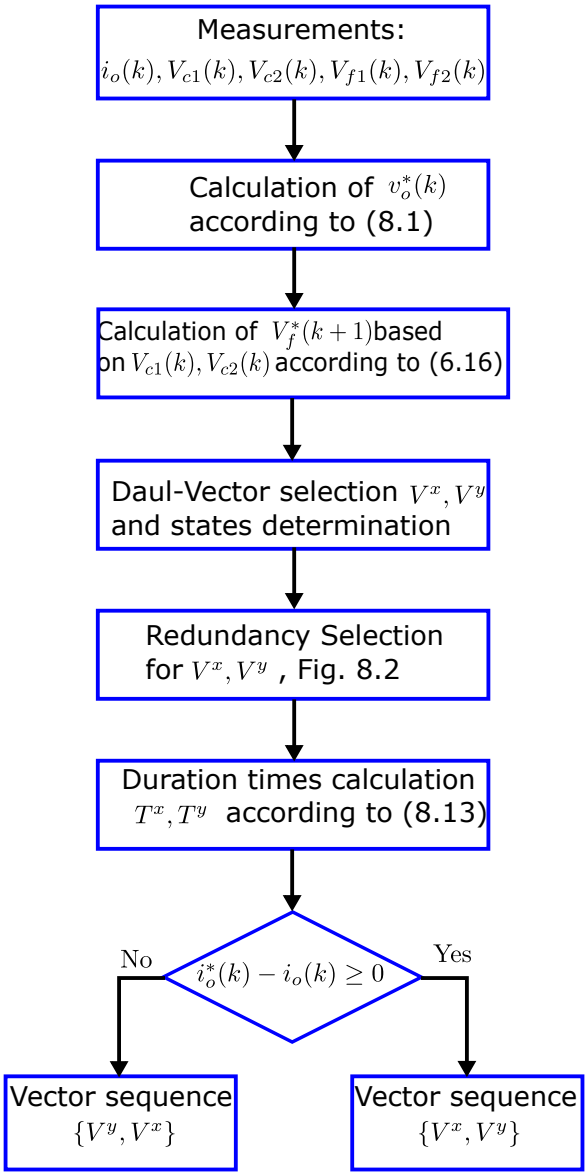


Figure 8.4: Flowchart of the proposed FCS-MPC.

slope of V^x is larger than that of V^y, will always be valid. The considered case in Fig. 8.3 is $f_{iV^x} > 0$ and $f_{iV^y} < 0$.

Referring to Fig. 8.3, It can be observed that for $i_{err} < 0$, the vector sequence $\{V^y, V^x\}$ (Fig. 8.3b) has a smaller enclosed area S during T_s compared to the sequence $\{V^x, V^y\}$ (Fig. 8.3a). While for $i_{err} > 0$, the vector sequence $\{V^x, V^y\}$ (Fig. 8.3c) has a smaller S compared to the sequence $\{V^y, V^x\}$ (Fig. 8.3d). The optimal vector sequence for all possibilities is given in Table 8.2. Fig. 8.4 shows the flowchart of the conventional and proposed FCS-MPC. The proposed FCS-MPC can be summarized in the following steps:

1. Calculation of the voltage reference v_o^* according to (8.1);

2. Selection of the two vectors V^x and V^y and locating the switching states SWs^x for V^x and SWs^y for V^y according to (8.3) and (8.5);

3. Calculation of the reference voltage V_f^* of FCs based on V_{c1} and V_{c2} as in (6.16);

4. Selection of the proper state SW^x and SW^y from the available redundancies based on the FCs actual voltages, Fig. 8.2;

5. Calculation of the optimal duration times of V^x and V^y according to (8.13); and

6. Selection of the voltage vector sequence to minimize THD and e_{i_o}, Table 8.2.

Accordingly, the proposed FCS-MPC requires only $1\times$ voltage reference calculation instead of $12\times$ current predictions, $12\times$ FCs voltage predictions and $12\times$ dc-link voltage predictions in the conventional algorithm. Moreover, the optimal voltage vectors are identified using simple equations without the need for several evaluations of the cost function. The application times of the dual-vector are determined from direct equations. The dc-link balancing is implemented by integrating the algorithm into the FCs balancing without the need for multiple voltage predictions, which saves an additional weighting factor in the cost function and thus the required cumbersome procedure in the tuning process as in the conventional method. Therefore, the computational efforts are considerably reduced in the developed FCS-MPC. In addition, a fixed switching frequency and an improved harmonic spectrum are realized through the use of the dual-vector application.

8.3 Experimental validation

The proposed dual-vector MPC method is experimentally validated in this section. The MPC algorithms are implemented on a DS1202 dSPACE Microlabbox, while the switching sequence with a dead time of 2 μs is generated using the built-in DS1302 FPGA board. For synchronization, the FPGA board generates the interrupt signal to the processor at the sampling frequency $f_s = 1/T_s$. Then the processor board executes the MPC algorithm and provides the selected vectors with their corresponding duration periods to the FPGA board to generate the pulses for switches. The main system parameters are given in Table 6.5 with a different sampling period to be here $T_s = 100\mu s$, corresponding to sampling frequency $f_s = 10$ kHz. The inverter output voltage and current are captured using Oscilloscope DPO-2024 with a sampling rate of 62.5 kHz.

Several experimental testes are carried out to verify the effectiveness of the proposed MPC method. To compare the performance with the conventional algorithm, the weighting factors λ_1, λ_2 of the conventional method in (6.12), and λ of the proposed MPC algorithm in (8.13) are first adjusted. The weighting factors of the two MPC methods are selected to produce the same voltage ripples regarding the FCs and dc-link balance. Consequently, the performance comparison can be carried out regarding the first goal (current control). λ_1, λ_2 of the conventional method, and λ of the proposed dual-vector MPC method are adjusted by trial and errors to give a voltage ripple of 3.5 V in the FCs C_{f1}, C_{f2} and 5 V in capacitors C_1, C_2. The values of λ_1, λ_2 and λ were found to be 0.3, 0.07, and 0.06, respectively, for a reference current amplitude of 8 A.

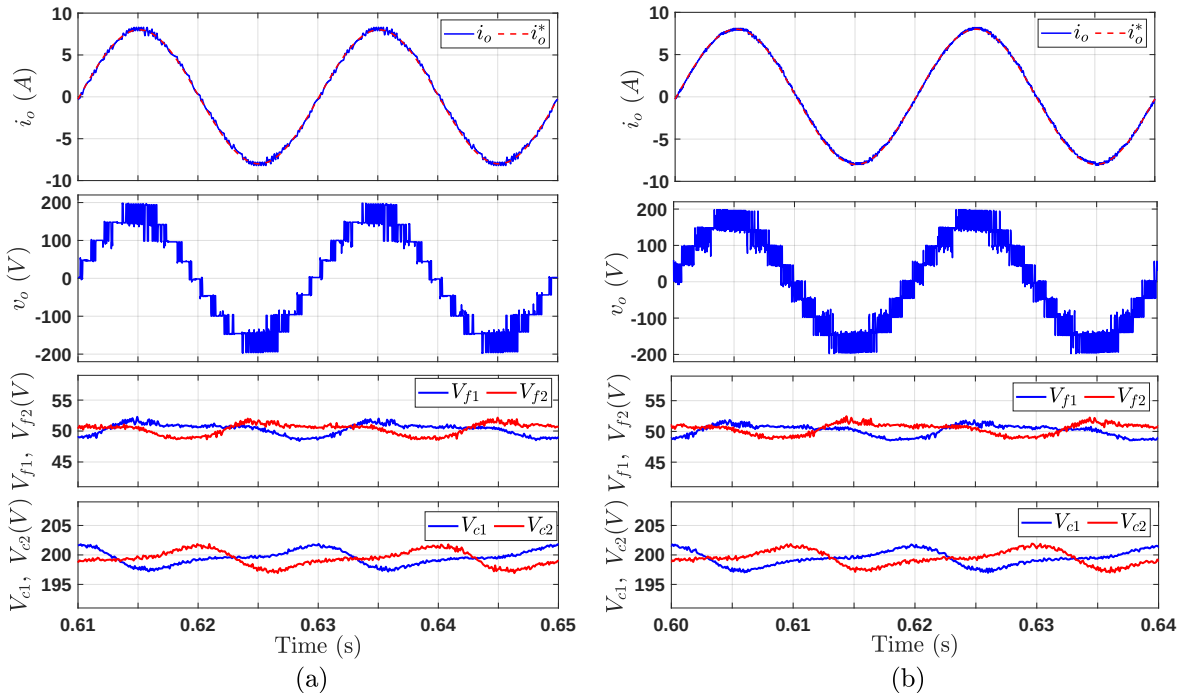


Figure 8.5: Experimental results at steady-state: (a) Conventional FCS-MPC and (b) Proposed FCS-MPC.

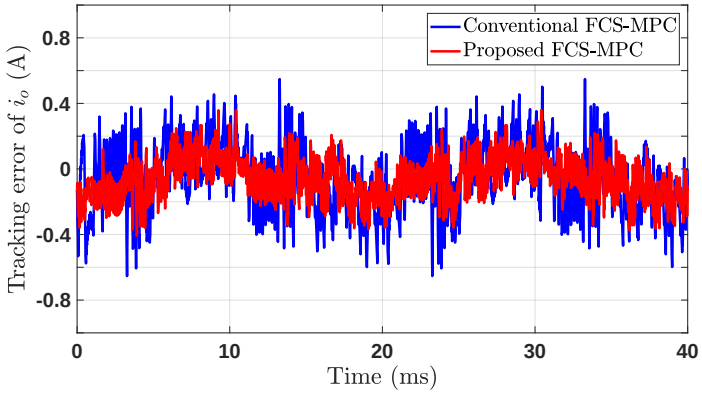


Figure 8.6: Current tracking error at $i_o^* = 8$ A.

8.3.1 Steady-state and transient operation

The experimental results of i_o, v_o, V_{f1}, V_{f2}, V_{c1}, and V_{c2} for the conventional and proposed MPC algorithms at i_o^*= 8 A are depicted in Fig. 8.5. It is clear that for two MPC schemes, i_o tracks the reference current i_o^* with high control performance. The 9L-SC-ANPC converter generates nine levels in the output voltage, improving the quality of v_o and i_o. Also, FCs C_{f1} and C_{f2} are balanced the reference value ($V_{dc}/8$= 50 V), as clear from V_{f1} and V_{f2} in the results. Furthermore, the NP potential is well controlled, as can be observed from V_{c1}, and V_{c2} waveforms. As selected by the weighting factors for the two MPC methods, the voltage

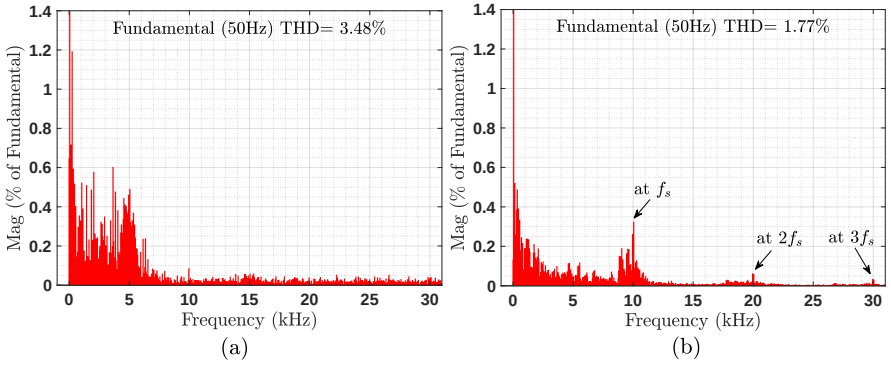


Figure 8.7: Harmonic spectrum of i_o: (a) Conventional FCS-MPC and (b) Proposed FCS-MPC.

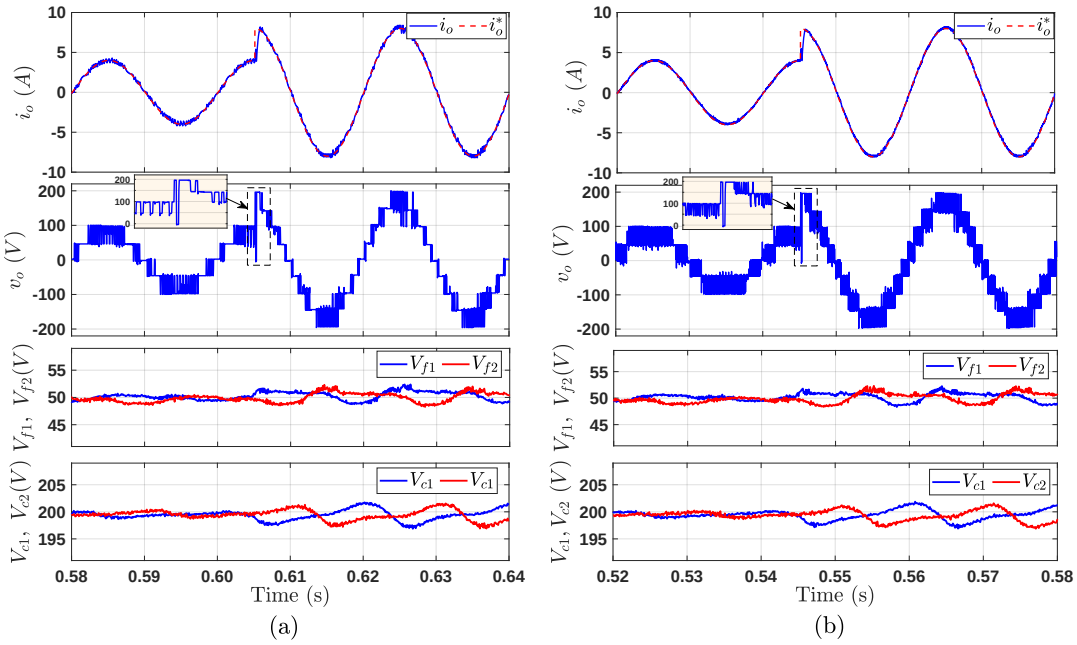


Figure 8.8: Experimental transient performance for a step-change in i_o: (a) Conventional FCS-MPC and (b) Proposed FCS-MPC.

ripples in the FCs and dc-link are 3.5 and 5 V, respectively. Fig. 8.6 depicts the instantaneous tracking error $(i_o^* - i_o)$ for the two MPC methods. It is clear that the proposed control algorithm has a better tracking behavior over the complete sinusoidal cycle. Thanks to the dual vector implementation, the proposed FCS-MPC not only has lower harmonic content, but also better harmonic distribution as shown in the harmonic spectrum of i_o in Fig. 8.7. In contrast to the conventional FCS-MPC, for the proposed MPC method the harmonics are concentrated around the sampling frequency and its multiples, which simplifies the filter design for grid-connected applications. The comparison of steady-state experimental operation is given in Table 8.3. The total harmonic distortion of output voltage and current (THD_v, THD_i), mean absolute current tracking error e_i, and average switching frequency f_{sw} are adopted as indicators to evaluate the performance. From the comparison in Table 8.3, it is clear that the proposed FCS-MPC algorithm has a very high tracking quality and low current harmonic contents, where e_i and THD_i are 1.35% and 1.77%, respectively, compared to 2.60% and 3.48% for the conventional

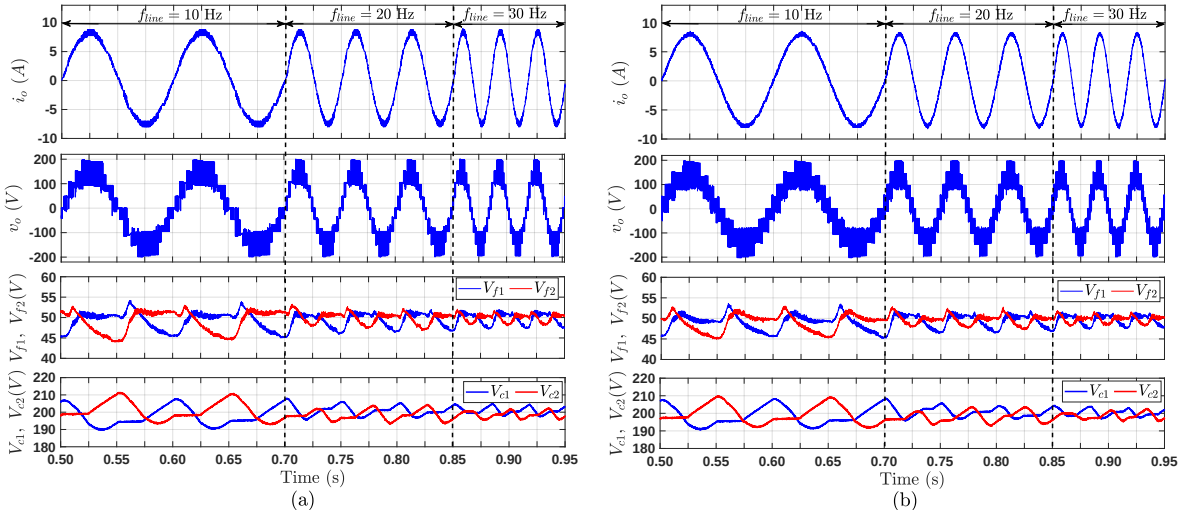


Figure 8.9: Experimental results at low output frequencies: (a) Conventional FCS-MPC and (b) Proposed FCS-MPC.

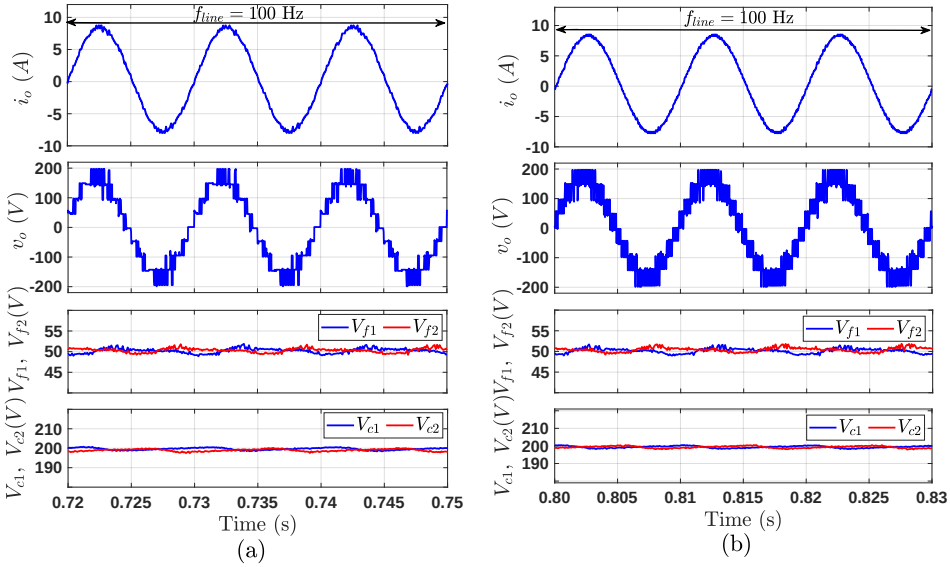


Figure 8.10: Experimental results at high output frequency, f_{line}=100 Hz: (a) Conventional FCS-MPC and (b) Proposed FCS-MPC.

method. Due to the application of two vectors during the control cycle, the proposed MPC method has a higher switching frequency compared to the conventional FCS-MPC, where f_{sw} is 1.28 kHz and 3 kHz for the conventional and proposed method, respectively.

The dynamic performance of the two MPC methods is investigated by changing i_o^* from 4 A to 8 A, as shown in Fig. 8.8. It is obvious that i_o follows i_o^* in the two algorithms, achieving fast dynamic performance. Moreover, the dc-link and FCs are kept stabilized at the references.

Operation at low output frequencies with the traditional PWM-based method is limited for the 9L-SC-ANPC inverter as discussed in Chapter 3 due to the inherent lack of sufficient redundant switching states. FCS-MPC provides more freedom to exploit the switching states

Table 8.3: Steady-state experimental comparison.

Method	e_i	THD$_i$	THD$_v$	f_{sw}
Conventional FCS-MPC	2.60%	3.48%	20.12%	1.28 kHz
Proposed FCS-MPC	1.35%	1.77%	20.89%	3 kHz

to control the voltages of FCs. To investigate this issue, the operation of the 9L-SC-ANPC inverter at low output frequencies under the conventional and proposed MPC methods is examined. Fig. 8.9 shows the performance at output frequency f_{line}= 10, 20, and 30 Hz. As it is clear, the dual-vector MPC method has better performance in terms of the tracking quality and FCs voltage ripples. This is due to the application of two vectors per control cycle with the optimal intervals. FCs balancing is realized by firstly exploiting the redundant states of each selected vector and secondly by modulating the application times of the optimal vectors, as described in Section 8.2.2. For conventional FCS-MPC, THD$_i$ is 5.12%, 4.81%, and 4.19% at f_{line}= 10, 20, and 30 Hz, respectively. While the proposed method has much better values, where THD$_i$ is 3.25%, 2.92%, and 2.64% at f_{line}= 10, 20, and 30 Hz, respectively. The operation at high output frequency (f_{line}= 100 Hz) is depicted in Fig 8.10. Both MPC methods have better performance with increasing f_{line}. However, the proposed MPC method is still superior in all control objectives.

The power losses of power converters mainly relate to conduction losses and switching losses. The power losses of the 9L-SC-ANPC inverter are evaluated under the designed MPC methods via PLECS Blockset in MATLAB/Simulink environment using loss models of the power switches. A 5-kW single-phase model is built with V_{dc}= 1 kV, i_o^*= 20 A, 50 Hz. The power switches of the experimental prototype are employed in the loss calculation, where IGBT FF50R12RT4 and power diode IDP30E65D1 are employed with the loss models provided by the manufacturer (*Infineon*). Fig. 8.11 shows the conduction and switching losses for the conventional and proposed MPC methods. As can be seen, the overall losses are dominated by conduction losses. In addition, the switching losses under the proposed MPC scheme are higher compared to the conventional method due to the increase in the average switching frequency, as illustrated in Table 8.3. However, this does not affect the efficiency of the inverter notably, since the total losses are dominated by the conduction losses. From the loss estimation, the efficiency is found to be 98.94% and 98.81% for conventional and proposed MPC schemes, respectively.

8.3.2 NP and FCs balancing evaluations

In order to further verify the effectiveness of the developed FCs and NP balancing method, the control performance is experimentally studied under abnormal operations. An additional capacitor is connected in parallel across C_1 to create a 10% mismatch between the two dc-link capacitors, leading to $C_1 = 1.1C_2$. The experimental waveforms for the operation in this case are shown in Fig. 8.12. As a result of the capacitance mismatch, the initial voltages of C_1 and C_2 are different, as can be observed in Fig. 8.12. With the starting of the converter operation, the difference between V_{c1} and V_{c2} decreases to realize the NP balance. Despite having a capacitance mismatch of 10% and a voltage difference of about 12 V, the proposed method achieved the NP balance like the conventional MPC scheme. In addition, V_{f1} and V_{f2} rise from 0 V to stabilize at the reference voltage $V_{dc}/8$ (50 V). Fig. 8.13 shows the start-up

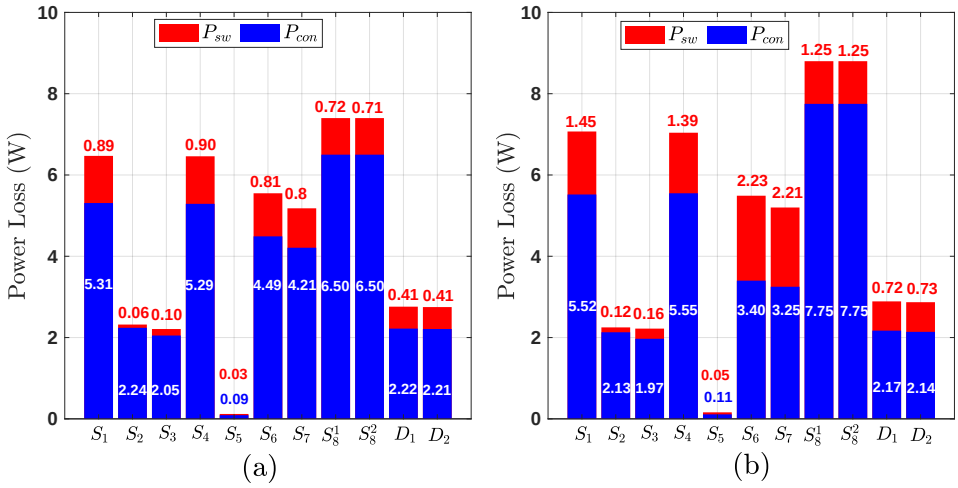


Figure 8.11: Power losses distribution: (a) Conventional FCS-MPC and (b) Proposed FCS-MPC.

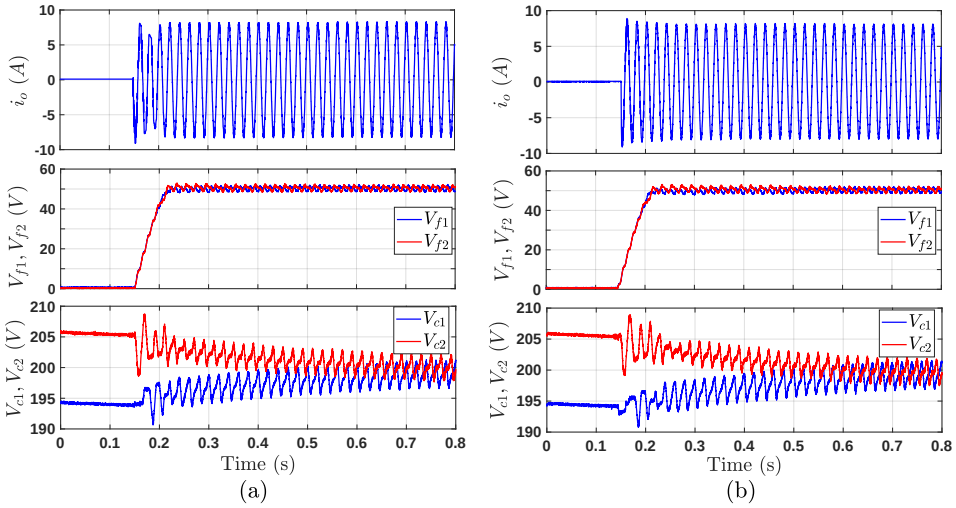


Figure 8.12: Experimental waveforms at start-up with capacitance mismatch ($C_1 = 1.1C_2$) and different initial voltages: (a) Conventional FCS-MPC and (b) Proposed FCS-MPC.

for another anomalous condition, where a mismatch was made in the FCs, resulting in $C_{f1} = 1.1C_{f2}$. From the results, it can be concluded that the proposed dual-vector MPC scheme can ensure balanced operations with only one weighting factor even under capacitance mismatch or different initial conditions, like the standard FCS-MPC with two weighting factors.

To further investigate the FCs balancing under the proposed and conventional MPC methods, the performance is studied under a wide range of operating conditions. e_i and THD_i are monitored as performance indicators for the primary current control objective, while FCs voltage ripple ΔV_f is measured as a performance indicator for the FCs balancing target. It should be mentioned that the voltage ripple of the dc-link capacitors is kept constant at 5 V under all operating conditions for the conventional and proposed methods. Fig. 8.14a shows the variation of e_i, THD_i and ΔV_f in the conventional FCS-MPC method for changing λ_1 in (6.12) from 10^{-1} to

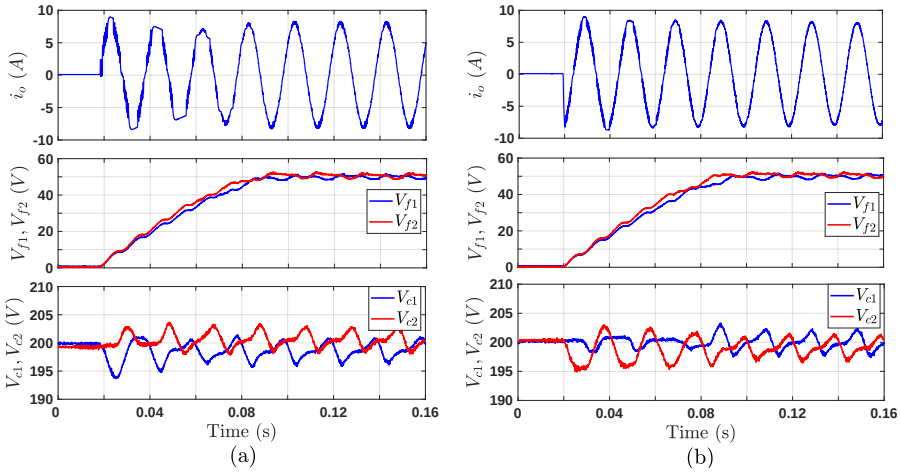


Figure 8.13: Experimental waveforms at start-up with a mismatch in the FCs: (a) Conventional FCS-MPC and (b) Proposed FCS-MPC.

10^1. For $\lambda_1 < 10^{-1}$, the FCs are not balanced, while for $\lambda_1 > 10^1$, the current is out of control. In contrast, the proposed MPC method achieves all control objectives at all values of λ in (8.14) with very acceptable values of performance indicators, as shown in Fig. 8.14b. However, optimal performance is observed for $0.04 < \lambda < 1$. This is because the weighting factor λ in the proposed MPC method only influences the application times (T^x, T^y) of the selected vectors (V^x, V^y). As discussed before, V^x and V^y are the closest vectors to the reference voltage v^* estimated based on $i_o^*(k+1)$, as given by (8.1) and (8.5), which ensures the realization of the current tracking goal even at high values of λ. While, for very low values of λ or $\lambda = 0$, the FCs are balanced with the redundant states, as illustrated in Fig. 8.2.

The trade-off between e_i and ΔV_f for the conventional and proposed methods is given in Fig. 8.14c. The results show a clear superiority of the proposed method, where for acceptable tracking quality ($e_i < 2.8$), the conventional FCS-MPC experiences higher voltage ripples compared to the dual-vector FCS-MPC algorithm. Similarly, the tradeoff between THD_i and ΔV_f is shown in Fig. 8.14d, confirming the ability of the proposed method to improve the FCs balance compared to conventional FCS-MPC. This improvement resulted from applying two vectors with the appropriate redundant states per sample and adjusting the intervals of the vectors as an additional degree of freedom.

8.3.3 Computational burden

To evaluate the calculation load of the proposed and conventional MPC schemes, the execution time is measured and compared. The two MPC methods are implemented on dSPACE Microlabbox as a rapid control prototyping (RCP) platform. The total time required for the implementation of an algorithm is determined by *turnaroundTime* variable in controlDesk software. In addition, the time required to execute a part of an algorithm can be measured through *atomic subsystems*. Table 8.4 gives the measured execution times of the conventional and proposed MPC methods. Basically, the execution times of multi-vector methods are expected to be relatively high compared to the conventional one-vector FCS-MPC due to the computational

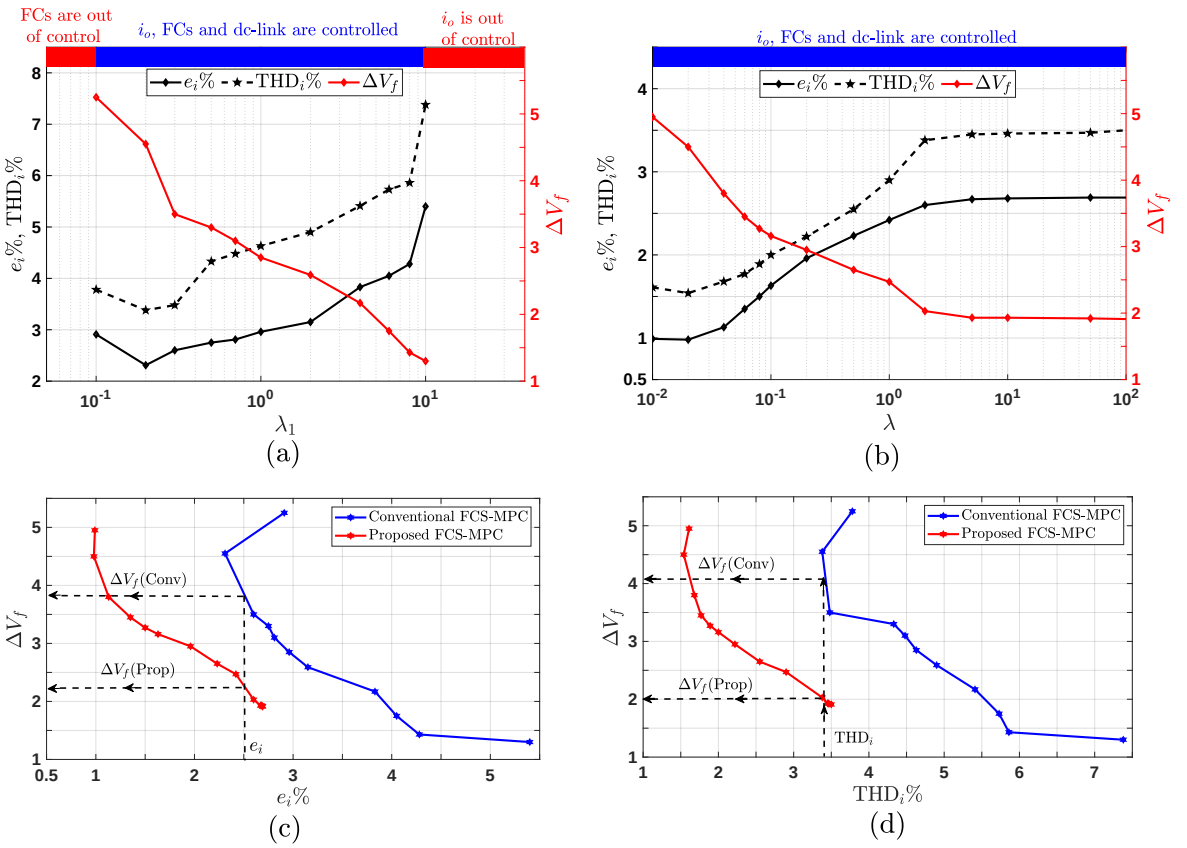


Figure 8.14: Trade-off between the control objectives: (a) e_i, THD$_i$, and ΔV_f versus λ_1 for conventional FCS-MPC, (b) e_i, THD$_i$, and ΔV_f versus λ for proposed FCS-MPC, (c) Trade-off between e_i and ΔV_f and (d) Trade-off between THD$_i$ and ΔV_f.

Table 8.4: Required execution times on dSPACE Microlabbox.

Algorithm	MPC Code	Additional Time for Auxiliary Tasks	Total Time
Conventional FCS-MPC	5.4 μs	5.9 μs	11.3 μs
Proposed FCS-MPC	3.9 μs	5.9 μs	9.8 μs

effort required to identify vectors and calculate their corresponding application periods. However, due to the achieved reduction in the calculations as discussed in Section 8.2, the MPC code of the proposed method has an execution time of 3.9 μs compared to 5.4 μs for the conventional scheme, achieving a reduction by 28%. In addition, it is expected that the reduction will be more significant when the two methods are implemented on platforms with lower computing power. As illustrated in Table 8.4, the total time required to execute the proposed and conventional MPC algorithms are 9.8 μs and 11.3 μs, respectively.

8.3.4 Performance evaluation at the same switching frequency

According to the performance of the two MPC schemes at the same sampling frequency $f_s = 10$ kHz, the average switching frequency f_{sw} was found to be 1.28 kHz and 3 kHz for the conven-

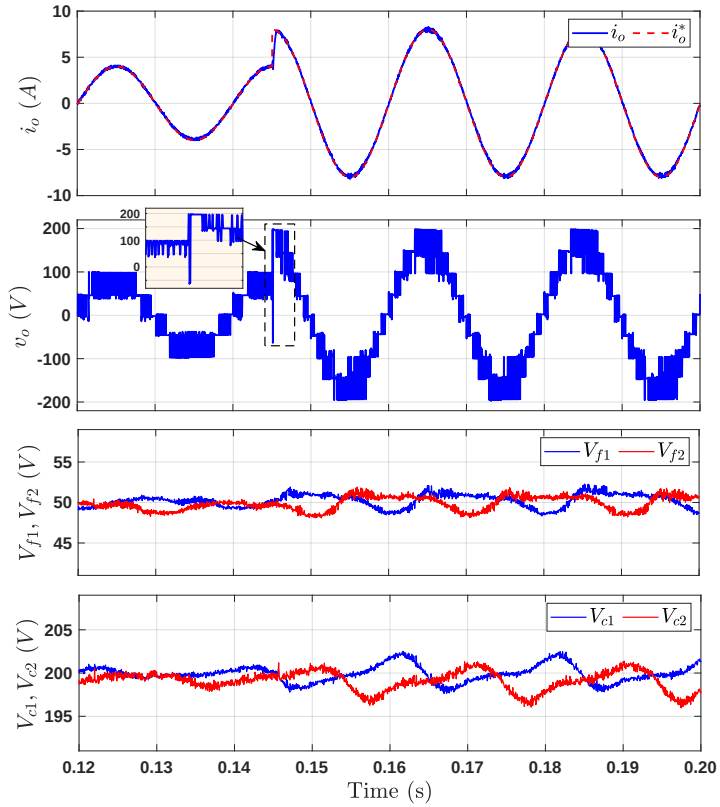


Figure 8.15: Experimental results of the conventional FCS-MPC method at 26 kHz sampling frequency.

tional and proposed MPC methods, respectively, as shown in Table 8.3. For a fair comparison, the same average switching frequency should be considered. To this end, the sampling frequency of the conventional method is increased to be 26 kHz to give an average switching frequency of 3 kHz as the proposed dual-vector scheme. It is worth mentioning that, for an impartial comparison, the weighting factors of the conventional method have been retuned in this case to give the same voltage ripples as the proposed MPC method in terms of FCs and dc-link capacitors. Fig. 8.15 shows the experimental results of the standard MPC method at $f_s = 26$ kHz for changing i_o^* from 4 A to 8 A. It can be observed that the dc-link capacitors and FCs are well balanced with voltage ripples of about 5 V and 3.5 V, respectively, at $i_o = 8$ A. Moreover, i_o has a better tracking behavior compared to the performance at $f_s = 10$ kHz in Fig. 8.5. The current harmonic spectrum at $i_o = 8$ A is shown in Fig. 8.16, where the THD_i has been reduced to 1.79%. The comparison with the proposed MPC method at the same average switching frequency (3 kHz) and $i_o^* = 8$ A is summarized in Table 8.3. According to the comparison at the same average switching frequency, both MPC schemes have almost similar performance regarding tracking quality and THD of i_o and v_o. However, the proposed dual-vector MPC scheme has a better harmonic distribution as can be seen in Fig. 8.7b when compared to Fig. 8.16. Moreover, the proposed algorithm has a lower execution time as a result of reducing the computational burden. It is worth noting that in order for the conventional method to provide a high performance like the proposed method, a very high sampling frequency is required, which necessitate the use of an RCP platform with high computing power, increasing the system cost.

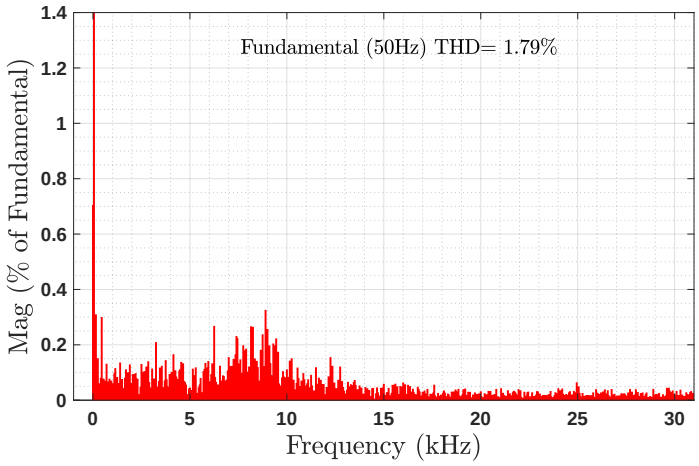


Figure 8.16: Current harmonic spectrum of the conventional FCS-MPC at 26 kHz sampling frequency.

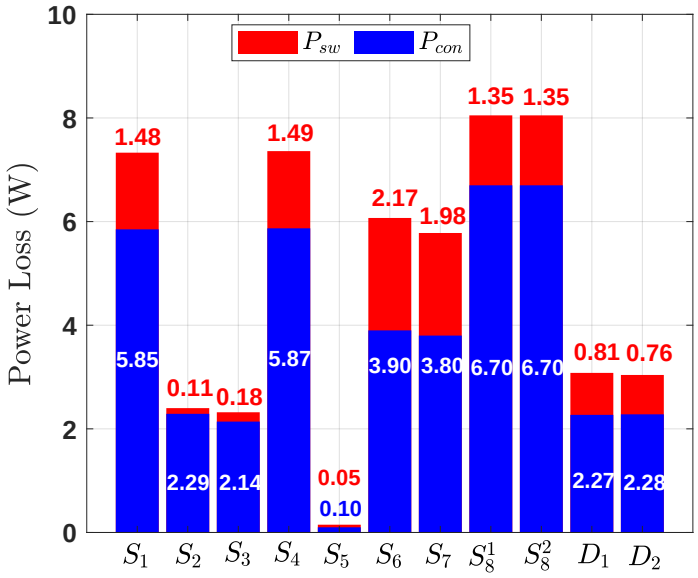


Figure 8.17: Power losses distribution of the conventional FCS-MPC at 26 kHz sampling frequency.

The conduction and switching losses under conventional FCS-MPC at $f_s = 26$ kHz are given in Fig. 8.17. Compared to Fig. 8.11a, an increase in the switching losses can be observed due to the increase in the average switching frequency. The calculated efficiency under these operating conditions is 98.79%. Accordingly, it can be concluded that the proposed MPC method still has better performance in terms of tracking quality, harmonic content, filter design and execution time.

Table 8.5: Steady-state experimental comparison at the same average switching frequency (3 kHz).

Method	f_s	e_i	THD$_i$	THD$_v$	f_{sw}
Conventional FCS-MPC	26 kHz	1.30%	1.79%	22.31%	3 kHz
Proposed FCS-MPC	10 kHz	1.35%	1.77%	20.89%	3 kHz

Table 8.6: Steady-state experimental comparison with a mismatch in the model inductance L.

Method	Performance Indicator	ΔL				
		+30%	+10%	0%	-10%	-30%
Conventional FCS-MPC	THD$_i$	3.20%	3.37%	3.48%	3.91%	4.72%
	e_i	2.29%	2.40%	2.60%	2.82%	3.61%
Proposed FCS-MPC	THD$_i$	1.58%	1.71%	1.77%	2.49%	3.30%
	e_i	1.55%	1.39%	1.35%	1.45%	2.31%

8.3.5 Control sensitivity to parameters mismatch

To investigate the control robustness, the performance is experimentally examined with the variation of the actual filter inductance L_{act} while the MPC algorithm still adopts the nominal value L_n. The variation percentage of the inductance ΔL is expressed as

$$\Delta L = \frac{L_{act} - L_n}{L_n} \cdot 100, \tag{8.19}$$

Table 8.6 lists the measured THD$_i$ and e_i at five different values of L_{act}, varying from $0.7L_n$ to $1.3L_n$. This test is carried out with the system parameters given in Table 6.5 and at $i_o^* = 8$ A. According to Table 8.6, it is obvious that, for the conventional and proposed MPC strategies, THD$_i$ decreases with increasing L_{act} and vice versa. Furthermore, the proposed MPC algorithm has lower values of THD$_i$ and e_i compared to the conventional method in all cases. In addition, with the variation of ΔL within $\pm 10\%$, the control performance demonstrates less sensitivity to ΔL. Considering that the variation limits of L_{act} are likely within $\pm 10\%$ [236], the control performance of the conventional and proposed FCS-MPC methods shows low sensitivity and acceptable performance for inductance variations.

8.4 Summary

In this chapter, a reduced-complexity dual-vector FCS-MPC has been proposed. According to the theoretical analysis and experimental findings, the following points are concluded

1. Compared to the conventional FCS-MPC, the proposed MPC method has a lower computational load and therefore a shorter execution time, despite the application of two vectors per control cycle T_s;

2. The proposed scheme can handle three control goals with a single weighting factor by integrating the NP potential into the FCs balancing objective. This concept can be used for any FC-based MLCs, which further reduces the control complexity;

3. Both conventional and proposed MPC methods can accurately track the reference current while achieving strong balancing of the dc-link and FCs. However, at the same sampling frequency, the proposed scheme exhibits better tracking quality, lower THD, and improved harmonic distribution;

4. At low output frequencies, the proposed MPC strategy has better performance in terms of FCs balancing and current tracking;

5. At the same average switching frequency, both MPC methods have almost similar performance. However, the proposed dual-vector MPC scheme has a better harmonic distribution, which simplifies filter design; and

6. Both MPC methods show low sensitivity and acceptable performance for inductance variations within $\pm 30\%$.

CHAPTER 9

Multi-Objective Control of Hybrid MLI: A Robust and Gain-Free MPC Method

In this chapter, a Lyapunov-based FCS-MPC strategy is presented, which simultaneously addresses three control objectives, namely, current control, FCs balancing and NP control, without the need for the laborious tuning process of weighting factors commonly required in traditional FCS-MPC method. The developed method is applied to a 9L-T^{2}C as a case study. The design steps of the proposed MPC method are presented in Section 9.4. For the sake of a fair comparison, the conventional PR controller is designed for the considered grid-connected system, as discussed in Section 9.5. The performance of the proposed method, along with other MPC methods, is experimentally verified for grid-connected operation under several conditions in Section 9.6. Finally, the summary of the chapter is given in Section 9.7.

9.1 Introduction

Addressing multiple objectives is a notable advantage of FCS-MPC. However, achieving satisfactory performance for all objectives through the coordination of weighting factors can be a complex task [284]. Therefore, the weighting factorless MPC is considered an attractive solution. In doing so, a technique called split cost function is often employed [220, 221]. This approach optimizes control objectives using independent cost functions, which is intuitive and easy to implement. However, implementing this method may increase algorithm complexity, and careful design is necessary to avoid performance degradation compared to the classic cost function in FCS-MPC [182]. Considering the 3L-ANPC inverter, a cascaded MPC method was proposed in [224]. This scheme achieves reference tracking, neutral point control, and losses distribution sequentially, with each stage utilizing an independent cost function without weighting factors.

Simplify the cost function is another approach commonly used for weighting factorless MPC. This method involves incorporating additional constraints based on the optimization goals to

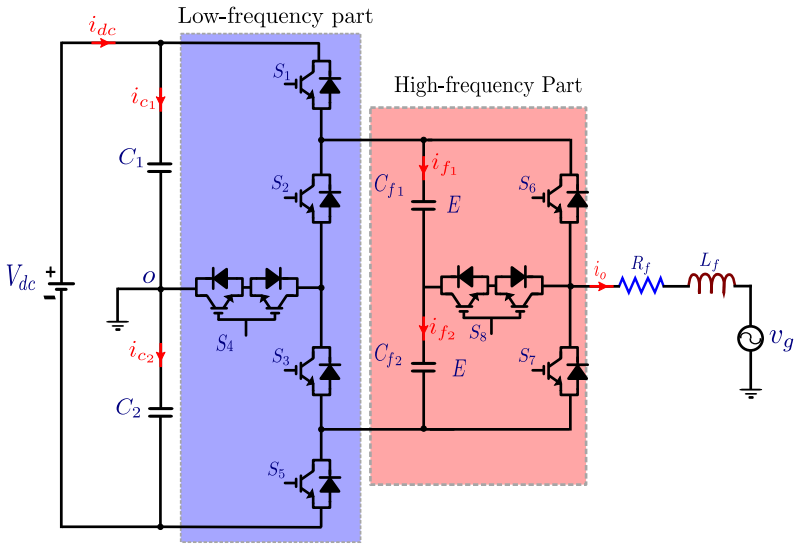


Figure 9.1: Power circuit of the grid-connected 9L-T^{2}C topology.

minimize the number of terms. In [229, 230], the torque, flux magnitude, and neutral point control were extrapolated using a set of input sequences. Candidate vector sequences were selected to ensure that the three objectives remained within their predefined boundaries for the given prediction horizon. Consequently, the cost function only needed to define the commutation times. Authors in [292] introduced a boundary with current error extrapolation, where the cost function defined the vector that has the longest duration within the boundary. However, employing a long-horizon may pose a challenge due to increased computational load.

In this chapter, a gain-free Lyapunov-based MPC method is designed for the 9L-T^{2}C, as an example of the hybrid MLIs with a multi-objective challenging control problem. The performance of the proposed controller is competitive with the conventional FCS-MPC, with the added advantage that no gain tuning is required. It is worth noting that the proposed controller has superior performance in cases where there is a mismatch in the filter inductance. The proposed method is subjected to a comparative analysis via the experimental implementation in grid-connected operation, where it is compared with a proportional-resonant (PR) controller and other MPC methods presented in previous chapters. This analysis reveals the advantages of the proposed method, including eliminating the need for gains or weighting factors, improved robustness, and effective control of the FCs.

9.2 System modeling

According to Fig. 9.1, the system equation is written as

$$v_o = R_f i_o + L_f \frac{di_o}{dt} + v_g, \tag{9.1}$$

where v_o and i_o represent the converter output voltage and current, respectively. v_g is the grid voltage. The filter resistance and inductance are denoted by R_f and L_f, respectively. Under the assumption of ideal switches, v_o is mathematically represented as

$$v_o = s_1 V_{c1} - s_5 V_{c2} + s_a V_{f1} + s_b V_{f2}, \tag{9.2}$$

In (9.2), the voltages of the dc-link capacitors C_1 and C_2 are represented by V_{c1} and V_{c2}, respectively. Additionally, V_{f1} and V_{f2} denote the voltages of the FCs C_{f1} and C_{f2}, respectively. To simplify the analysis, s_a, and s_b are introduced and mathematically represented as

$$s_a = s_5 + s_6 - s_1 - s_2,\ s_b = s_3 + s_5 - s_1 - s_7. \tag{9.3}$$

When considering the FCs, the continuous-time model is represented as

$$\left.\begin{aligned} i_{cf1} &= C_{f1}\tfrac{dV_{f1}}{dt} = -s_a i_o, \\ i_{cf2} &= C_{f2}\tfrac{dV_{f2}}{dt} = -s_b i_o. \end{aligned}\right\} \tag{9.4}$$

In (9.4), the current of the flying capacitors C_{f1} and C_{f2} are depicted by i_{f1} and i_{f2}, respectively. In a similar manner, the model for the dc-link is derived as

$$\left.\begin{aligned} i_{c1} &= C_1\tfrac{dV_{c1}}{dt} = i_{dc} - s_1 i_o, \\ i_{c2} &= C_2\tfrac{dV_{c2}}{dt} = i_{dc} + s_5 i_o, \end{aligned}\right\} \tag{9.5}$$

where i_{c1} and i_{c2} are the currents of the dc-link capacitors and i_{dc} denotes the dc source current, as shown in Fig. 9.1. With the assumption that $C_1 = C_2 = C$, the dc-link equation can be formulated as

$$\Delta i_c = C\frac{d\Delta V_c}{dt}, \tag{9.6}$$

In (9.6), the difference in voltage between the dc-link capacitors is represented by $\Delta V_c = V_{c1} - V_{c2}$, and the difference in current is denoted by $\Delta i_c = i_{c1} - i_{c2}$, which can be obtained as

$$\Delta i_c = -(s_1 + s_5) i_o. \tag{9.7}$$

9.3 Conventional FCS-MPC for grid-connected operation

The main task of the power inverter is to inject a low distorted current into the grid through the grid-connected operation. To accomplish this, it is essential to regulate the FCs voltages, and the NP potential to ensure proper operation of the converter.

By employing forward-Euler approximation method to the system models presented in (9.1), (9.4), and (9.6), the system variables at $(k+1)^{th}$ can be predicted as

$$i_o(k+1) = (1 - \frac{RT_s}{L}) i_o(k) + \frac{T_s}{L}(v_o(k) - v_g(k)), \tag{9.8}$$

$$\left.\begin{aligned} V_{f1}(k+1) &= V_{f1}(k) - \tfrac{T_s s_a(k)}{C_{f1}} i_o(k), \\ V_{f2}(k+1) &= V_{f2}(k) - \tfrac{T_s s_b(k)}{C_{f2}} i_o(k), \end{aligned}\right\} \tag{9.9}$$

$$\Delta V_c(k+1) = \Delta V_c(k) - \frac{(s_1(k) + s_5(k))T_s}{C} i_o(k), \tag{9.10}$$

where T_s is the sampling period. Based on the control objectives, one may define the system errors as

$$\begin{aligned} e_1 &= i_o - i_o^*, \\ e_2 &= V_{f1} - V_f^*, \\ e_3 &= V_{f2} - V_f^*, \\ e_4 &= V_{c1} - V_{c2} = \Delta V_c, \end{aligned} \tag{9.11}$$

where V_f^* is the reference voltage of the FCs and should be regulated at $E = V_{dc}/8$ in order to generate nine output voltage levels. Additionally, i_o^* represents the grid current reference generated to be in phase with the grid voltage for active power injection. Therefore, to achieve the aforementioned tasks and maintain these errors at their minimum values, a conventional FCS-MPC controller suggests the following cost function

$$g{=}e_1(k{+}1)^2 + \lambda_1 e_2(k{+}1)^2{+}\lambda_1 e_3(k{+}1)^2{+}\lambda_2 e_4(k{+}1)^2, \tag{9.12}$$

where λ_1 and λ_2 are design parameters that require tuning. The tuning is done as per the designer's preference prioritizing one term over the other. For example, when λ_1 is selected to be higher than λ_2, this implies that the error in the FCs voltages is more important than the voltage difference at the neutral point. The process of tuning the weighting factors is a challenging task that necessitates multiple simulations and experimental tests involving intricate numerical models [284]. In the following subsection, Lyapunov-based FCS-MPC is proposed to overcome this issue and eliminate the parameter tuning.

9.4 Lyapunov-based MPC

For Lyapunov-based MPC, the first step in the design is to define a positive definite cost function (called Lyapunov function) as

$$J_{\mathrm{L}} = \frac{1}{2}e_1^2 + \frac{1}{2}\gamma_1 e_2^2 + \frac{1}{2}\gamma_1 e_3^2 + \frac{1}{2}\gamma_2 e_4^2, \tag{9.13}$$

where γ_1 and γ_2 are positive gains used in the Lyapunov cost function. This cost function is positive definite (i.e. $J_{\mathrm{L}} > 0$) for all error values at all times. The system under control, represented by (9.1), (9.4) and (9.6), controlled by a control input derived based on the cost function in (9.13) will be globally stable if the derivative of (9.13) is negative. Therefore the derivative of the cost function in (9.13) is found as

$$\frac{dJ_{\mathrm{L}}}{dt} = e_1\frac{de_1}{dt} + \gamma_1 e_2\frac{de_2}{dt} + \gamma_1 e_3\frac{de_3}{dt} + \gamma_2 e_4\frac{de_4}{dt}. \tag{9.14}$$

Taking into account the system models represented by (9.1), (9.4), (9.6), and (9.7), the error derivatives in (9.14) can be derived as

$$\begin{aligned}
\frac{de_1}{dt} &= \frac{1}{L_f}\left(v_o - v_g - R_f i_o\right) - \frac{di_o^*}{dt},\\
\frac{de_2}{dt} &= \frac{dV_{f1}}{dt} = \frac{-1}{C_{f1}} s_a i_o,\\
\frac{de_3}{dt} &= \frac{dV_{f2}}{dt} = \frac{-1}{C_{f2}} s_b i_o,\\
\frac{de_4}{dt} &= \frac{dV_{c1}}{dt} - \frac{dV_{c_2}}{dt} = \frac{-1}{C}\left(s_1 + s_5\right) i_o.
\end{aligned} \tag{9.15}$$

Substituting (9.15) into (9.14), the derivative of the cost function can be written as

$$\begin{aligned}
\frac{dJ_{\mathrm{L}}}{dt} = e_1 &\left(\frac{1}{L_f}\left(v_o - v_g - R_f i_o\right) - \frac{di_o^*}{dt}\right) + \gamma_1 e_2 \left(\frac{-1}{C_{f_1}} s_a i_o\right)\\
&+ \gamma_1 e_3 \left(\frac{-1}{C_{f_2}} s_b i_o\right) + \gamma_2 e_4 \left(\frac{-1}{C}\left(s_1 + s_5\right) i_o\right).
\end{aligned} \tag{9.16}$$

Considering the mathematical expression of v_o in (9.2), $\frac{dJ_{\mathrm{L}}}{dt}$ is written as

$$\begin{aligned}
\frac{dJ_{\mathrm{L}}}{dt} = e_1 &\left(\frac{1}{L_f}\left(s_1 V_{c1} - s_5 V_{c2} + s_a V_{f1} + s_b V_{f2} - v_g - R_f i_o\right) - \frac{di_o^*}{dt}\right)\\
&+ \gamma_1 e_2 \left(\frac{-1}{C_{f_1}} s_a i_o\right) + \gamma_1 e_3 \left(\frac{-1}{C_{f_2}} s_b i_o\right) + \gamma_2 e_4 \left(\frac{-1}{C}\left(s_1 + s_5\right) i_o\right).
\end{aligned} \tag{9.17}$$

In order to represent the system mathematical equations using the system reference and error values, not the actual values, the measured values in (9.17) are substituted by the references and the errors defined in (9.11). By doing so, (9.17) is modified to

$$\begin{aligned}
\frac{dJ_{\mathrm{L}}}{dt} = e_1 &\left(\frac{1}{L_f}\left(s_1(e_4 + V_{c2}) - s_5 V_{c2} + s_a(e_2 + V_f^*) + s_b(e_3 + V_f^*)\right.\right.\\
&\left.\left. - v_g - R_f(e_1 + i_o^*)\right) - \frac{di_o^*}{dt}\right) + \gamma_1 e_2 \left(\frac{-1}{C_{f_1}} s_a (e_1 + i_o^*)\right)\\
&+ \gamma_1 e_3 \left(\frac{-1}{C_{f_2}} s_b (e_1 + i_o^*)\right) + \gamma_2 e_4 \left(\frac{-1}{C}\left(s_1 + s_5\right)(e_1 + i_o^*)\right).
\end{aligned} \tag{9.18}$$

By rearranging (9.18), the resulting equation yields the following common error terms:

$$s_a e_1 e_2 \left(\frac{1}{L_f} - \frac{\gamma_1}{C_{f_1}}\right), s_b e_1 e_3 \left(\frac{1}{L_f} - \frac{\gamma_1}{C_{f_2}}\right), \text{ and } s_1 e_1 e_4 \left(\frac{1}{L_f} - \frac{\gamma_2}{C}\right).$$

In a steady state, assuming small error values, these terms have a negligible effect on the cost function value and thus eliminating them would have the following advantages:

- Simplifies the calculation burden: the final cost function will have a lower number of multiplications and additions.

- Reduces the average switching frequency: as the controller will not need to switch at every small change in the state errors.
- Gain free cost function: selecting the gains as in (9.19) will eliminate the gain tuning.

To eliminate the terms that have multiplied errors (e_1e_2, e_1e_3, e_1e_4) for calculations reduction and errors decoupling [263], γ_1 and γ_2 are selected as

$$\gamma_1 = \frac{C_{f_1}}{L_f},\ \gamma_2 = \frac{C}{L_f}. \tag{9.19}$$

Substituting (9.19) into (9.18) gives

$$\frac{dJ_L}{dt} = \frac{1}{L_f}\left\{\begin{array}{l} e_1\left\{\left(s_1 - s_5\right)V_{c2} + \left(s_a + s_b\right)V_f^* - v_g - R_f e_1\right\} \\ - i_o^*\left\{s_a e_2 + s_b e_3 + \left(s_1 + s_5\right)e_4 + R_f e_1\right\} \\ - s_5 e_1 e_4 - L_f e_1 \dfrac{di_o^*}{dt} \end{array}\right\} \tag{9.20}$$

As the FCS-MPC controller looks for the least value of the cost function, the term $1/L_f$ can be eliminated from the cost function without any complications. The main contribution of this method lies in having a gain-free cost function and the explanation of this gain elimination comes from the fact that we are obtaining a cost function that eliminates the common error terms.

Lyapunov control theorem states that for a positive definite cost function, as the one in (9.13), the respective control system will be stable if the derivative of that cost function is negative. Therefore, if the derivative of the error cost function in (9.21) is shown to be negative all the time, then the controlled system will be stable.

The derivative of the Lyapunov cost function, hereafter referred to as the cost function, can be at $(k+1)^{th}$ sample as

$$\begin{aligned} \frac{dJ_L}{dt}(k+1) &= e_1(k+1)\left\{\left(s_1(k) - s_5(k)\right)V_{c2}(k)\ + \left(s_a(k) + s_b(k)\right)V_f^*(k+1) - v_g(k) - R_f e_1(k+1)\right\} \\ &- i_o^*(k+1)\left\{s_a(k)e_2(k+1) + s_b(k)e_3(k+1)\ + \left(s_1(k) + s_5(k)\right)e_4(k+1) + R_f e_1(k+1)\right\} \\ &- s_5 e_1(k+1)e_4(k+1) - L_f e_1(k+1)\frac{i_o^*(k+1) - i_o^*(k)}{T_s} \end{aligned} \tag{9.21}$$

The system errors at $(k+1)^{th}$ sample in (9.21) are calculated according to the predicted variables in (9.8), (9.9), and (9.10). During each sampling period, the controller evaluates the derivative of the Lyapunov function in (9.21) at the future sample for each valid control input among the finite converter states. It then selects the control input that yields the smallest value of dJ_L/dt. By applying the Lyapunov stability criterion, the stability of the power inverter system can be assessed using the obtained value of dJ_L/dt. Since there is a finite set of inputs, it is sufficient to demonstrate that there exists at least one input that makes the cost function negative in order to establish system stability.

9.5 Proportional-Resonant controller design

The implementation of the proportional-resonant (PR) controller offers the opportunity to enhance the performance of converter reference tracking and effectively addresses the well-known

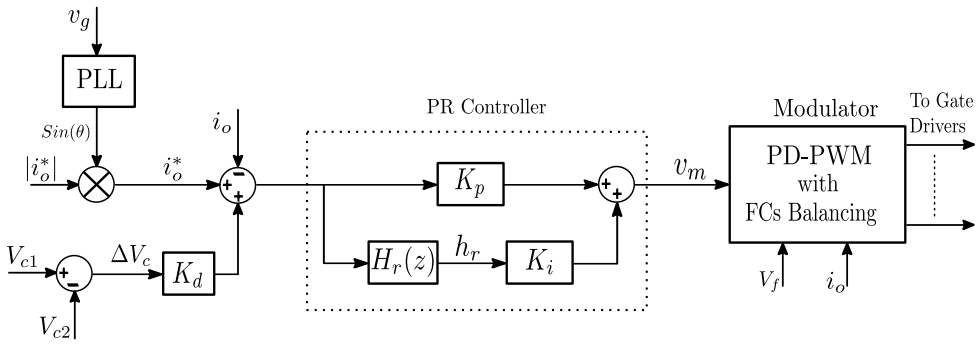


Figure 9.2: Block diagram of the PR controller with PWM.

Table 9.1: Parameters values of the PR controller.

Parameter	Value	Parameter	Value
K_p	0.315	K_i	109.70
a_0	1	a_1	-2
a_2	1	b_0	4.712×10^{-4}
b_1	-4.712×10^{-4}	b_2	0

deficiencies, such as the presence of steady-state error in single-phase systems, typically associated with conventional PI controllers [293]. The block diagram of the PR current controller for the single-phase grid-connected 9L-T^{2}C is shown in Fig. 9.2. The balancing of the NP potential is achieved through the implementation of a proportional controller with a gain K_d, which incorporates the feedforward of the dc-link voltages, as detailed in [294]. The FCs balancing with classic PWM-based controllers is commonly realized by exploiting the redundant states within the modulation stage. While this approach streamlines the design of the control system, its effectiveness relies on the presence of redundancies. Accordingly, C_{f1} and C_{f2} in the 9L-T^{2}C are stabilized at their references with the balancing algorithm presented in Chapter 7.

The design procedure of the PR current controller follows the guidelines outlined in [295] for single-phase grid-connected inverters. The PR controller comprises a proportional gain K_p combined with a resonant path, as shown in Fig. 9.2. The resonant path involves the resonant gain K_i and the resonant filter, represented in the z-domain transfer function $H_r(z)$ as

$$H_r(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}}, \tag{9.22}$$

where a_k and b_k are real values. In the process of designing the digital PR controller, the task involves determining the appropriate values for K_p, K_i, a_0, a_1, a_2, b_0, b_1, and b_2. According to the system parameters, given in Table 9.2, and the analytical equations provided in [295], the parameters of the PR current controller are given in Table 9.1. The design incorporates a resonant frequency (f_r) of 50 Hz with a resonant bandwidth of 1.5 Hz and a damping factor (ξ) of 0.95.

Table 9.2: System Parameters for Grid-connected Operation.

Parameter	Value
dc voltage, V_{dc}	400 V
Grid voltage, V_g	120 V (rms)
Line frequency, f_{line}	50 Hz
Resistance, R_f	3 Ω
Filter inductance, L_f	6 mH
dc-link capacitors, C_1 and C_2	3.3 mF
FCs, C_{f1} and C_{f2}	2 mF

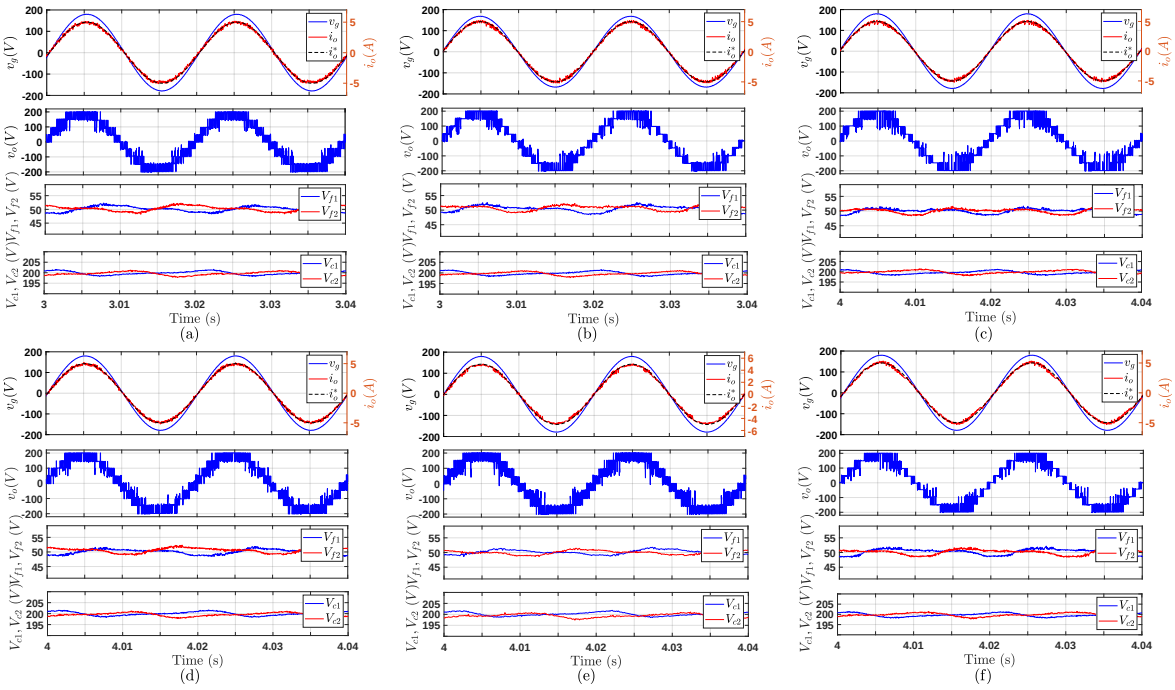


Figure 9.3: Experimental results at steady-state for grid-connected operation: (a) Classic PR controller with PWM, (b) Conventional FCS-MPC, (c) Low-complexity voltage-based MPC, (d) Enhanced DB-MPC, (e) Low-complexity Dual-Vector MPC and (f) Proposed LMPC.

9.6 Experimental results

The performance of the LMPC is experimentally validated for grid-connected operation and compared with other common control methods. The comparison includes classic PR controller and various MPC methods, namely conventional FCS-MPC, low-complexity voltage-based MPC described in Chapter 6, enhanced DB-MPC outlined in Chapter 7, and dual-vector MPC presented in Chapter 8. The system parameters utilized in the experimental implementation are presented in Table 9.2.

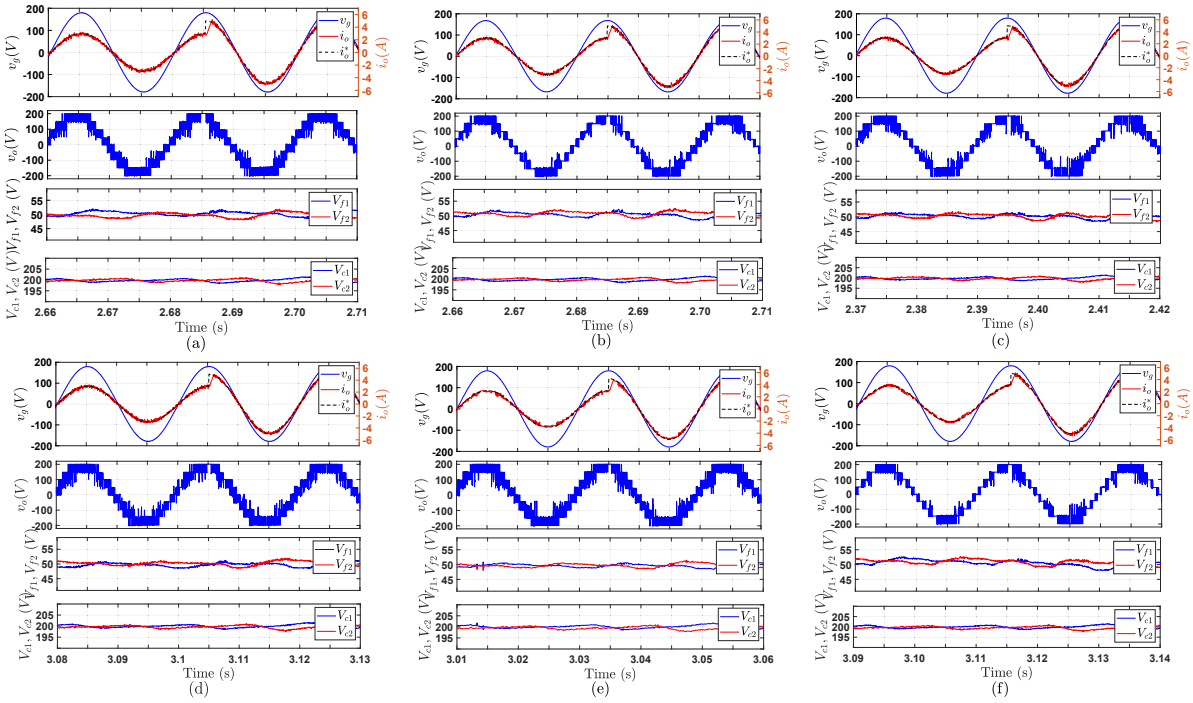


Figure 9.4: Experimental results for grid-connected operation at step-change in i_o^*: (a) Classic PR controller with PWM, (b) Conventional FCS-MPC, (c) Low-complexity voltage-based MPC, (d) Enhanced DB-MPC, (e) Low-complexity Dual-Vector MPC and (f) Proposed LMPC.

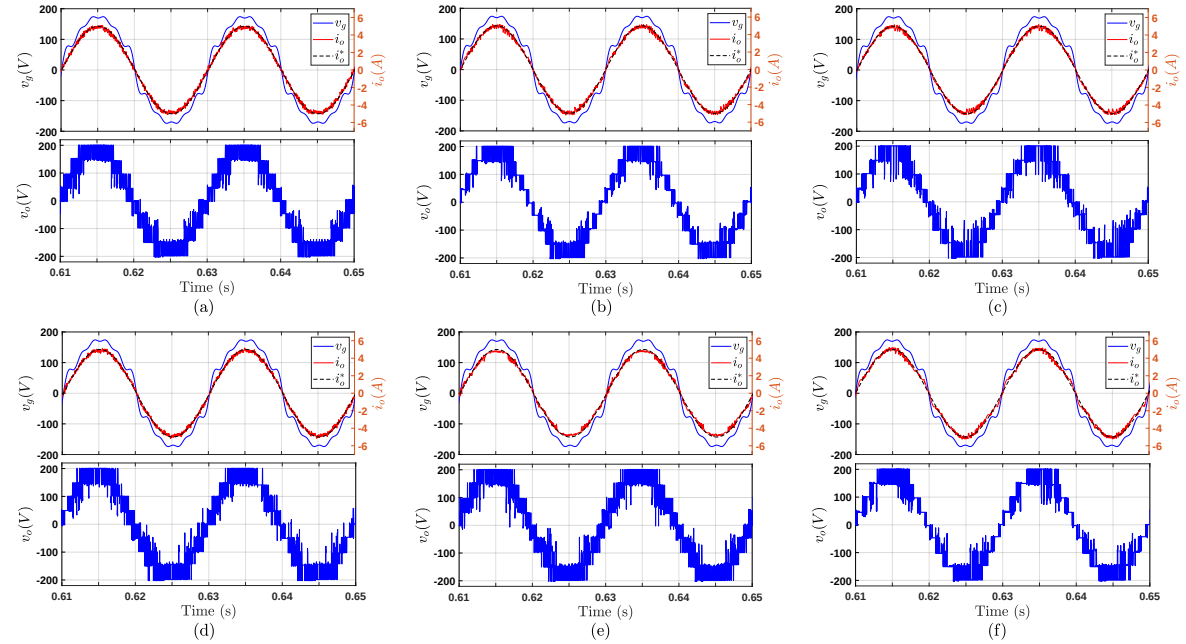


Figure 9.5: Experimental results for grid-connected operation with distorted grid voltage: (a) Classic PR controller with PWM, (b) Conventional FCS-MPC, (c) Low-complexity voltage-based MPC, (d) Enhanced DB-MPC, (e) Low-complexity Dual-Vector MPC and (f) Proposed LMPC.

Table 9.3: Assessment of most common MPC methods for MLIs.

Method	Tuned Parameters	e_i	THD$_i$	THD$_v$	ΔV_f	ΔV_c	$f_{\text{sw,avg}}$	Carrier Freq. f_c	Sampling Period T_s	Execution Time
PR Control	K_p, K_i, a_k, b_k	2.19%	3.56%	22.62%	4 V	4 V	2.02 kHz	6 kHz	50 μs	10.3 μs
FCS-MPC	λ_1,λ_2	1.83%	3%	21.39%	3.25 V	4 V	1.97 kHz	-	50 μs	11.3 μs
Voltage-based MPC	λ	1.90%	3.12%	22.18%	3.25V	4 V	1.93 kHz	-	50 μs	12.7 μs^*
Enhanced DB-MPC	-	2.01%	3.20%	23.56%	4 V	4 V	2.08 kHz	6 kHz	50 μs	11.1 μs^*
Dual-vector MPC	λ	2.60%	3.84%	21.56%	2.5 V	4 V	2.20 kHz	-	100 μs	9.8 μs
LMPC	-	2.30%	3.70%	19.14%	3.25 V	4 V	1.92 kHz	-	50 μs	11.4 μs

* The total time includes the execution time of the EKF-based parameters estimator, which has been developed as part of these methods.

9.6.1 Steady-state and transient operation

Fig. 9.3 illustrates the experimental results of the LMPC and other control methods at $i_o^* = 5$ A. The gains and controller parameters of the PR method are tuned as in Table 9.1 according to the system parameters. The weighting factors λ_1 and λ_2 of the conventional MPC and λ in voltage-based and dual-vector MPC schemes are adjusted to obtain acceptable performance in terms of all control objectives at the considered operating conditions. All methods employ a sampling period of 50μs, except for the dual-vector method, which utilizes a sampling period of 100μs. The purpose of this adjustment is to ensure a switching frequency comparable to the other methods. The dual-vector method applies two vectors per sample, different from the conventional MPC concept, which utilizes only one vector. As shown in Fig. 9.3, all methods demonstrate excellent tracking quality and efficient balancing for the FCs and NP. The performance is compared using various indicators, namely, the mean absolute tracking error of the current e_i, the total harmonic distortion (THD) of v_o and i_o, voltage ripples of the FCs and dc-link capacitors, the average switching frequency $f_{\text{sw,avg}}$, and the execution time, as summarized in Table 9.3.

In terms of current control and waveform quality, all methods exhibit comparable and high performance. However, it is worth noting that the dual-vector method displays slightly lower tracking quality, which can be attributed to its implementation at twice the sampling period compared to the other methods. Despite this, the dual-vector method excels in FCs control, effectively limiting the ripples to 2.5 V. The LMPC method demonstrates acceptable performance across all objectives while achieving a minimum average switching frequency. A key advantage of this method lies in the elimination of weighting factors and the associated tuning efforts. The DB-MPC method, similar to the LMPC method, does not incorporate weighting factors. However, it is important to note that the FCs balance in the DB-MPC method can only be achieved through the use of redundant states in the modulation stage, similar to the PR control method. As a consequence, this reliance on redundant states leads to a higher ripple in the FCs, reaching up to 4V.

The transient operation of the methods is verified and illustrated in Fig. 9.4. A step change is applied to the desired current i_o^*, transitioning from 3 A to 5 A. The results reveal that all methods exhibit commendable dynamic performance. Nevertheless, it is important to highlight that the MPC-based methods inherently possess superior dynamic performance compared to the other approaches.

Table 9.4: Comparison at a -60% mismatch in the filter inductance L.

Method	e_i	THD_i	THD_v
PR Control	3.53%	5.37%	18.11%
FCS-MPC	11.81%	21.10%	88.50%
LMPC	4.50%	7.67%	25.82%

9.6.2 Performance evaluation with a distorted grid voltage

To investigate the performance of the controller under distorted grid voltage conditions, a 5% amplitude from the 3rd harmonic to the 11th harmonic is introduced to the grid voltage, as described by

$$v_g(t) = \sqrt{2}v_g \sin(\omega_e t) + 0.05 \sum_{h=3,5,..}^{11} \sqrt{2}v_g \sin(h\omega_e t). \tag{9.23}$$

The experimental results of this test are presented in Fig. 9.5. It is evident that the grid voltage exhibits significant distortion in this scenario. However, even in the face of this challenging condition, the gain-free LMPC method, along with the other methods under consideration, demonstrates stable operation. Furthermore, they successfully achieve the desired unity power factor (PF) operation.

9.6.3 Performance evaluation with parameter mismatch

As predictive control is a model-based strategy, its performance is highly dependent on parameters uncertainty. To investigate this issue, the actual filter inductance was reduced from 6 mH to 2.4 mH, representing a mismatch of -60%. This change in parameter value simulates uncertainty in the system model and allows for an evaluation of the robustness of the MPC method under such conditions. In order to avoid potential safety concerns arising from this significant mismatch in grid connection, the test is conducted using a stand-alone load with a resistance of $R = 22\ \Omega$. This case study is carried out for the classic PR controller, conventional MPC, and the LMPC. The results of this experiment are presented in Fig. 9.6, which illustrate a clear superiority of the PR controller as it does not rely on the system model. In addition, the LMPC demonstrates satisfactory performance even under a substantial mismatch of -60% in the filter inductance. In contrast, the conventional MPC method exhibits a significant deterioration in performance, particularly with regards to current tracking and the harmonics of the output voltage. The performance indicators of this case study are provided in Table 9.4, which demonstrate the effectiveness of the LMPC scheme as a robust control method, while also avoiding the use of weighting factors. Based on the analyses and the experimental results, a qualitative comparison is carried out among all methods and summarized in Table 9.5

9.7 Summary

In this chapter, a Lyapunov-based MPC method was designed to address the challenge of weighting factors tuning in multi-objective control problems. The results demonstrated that

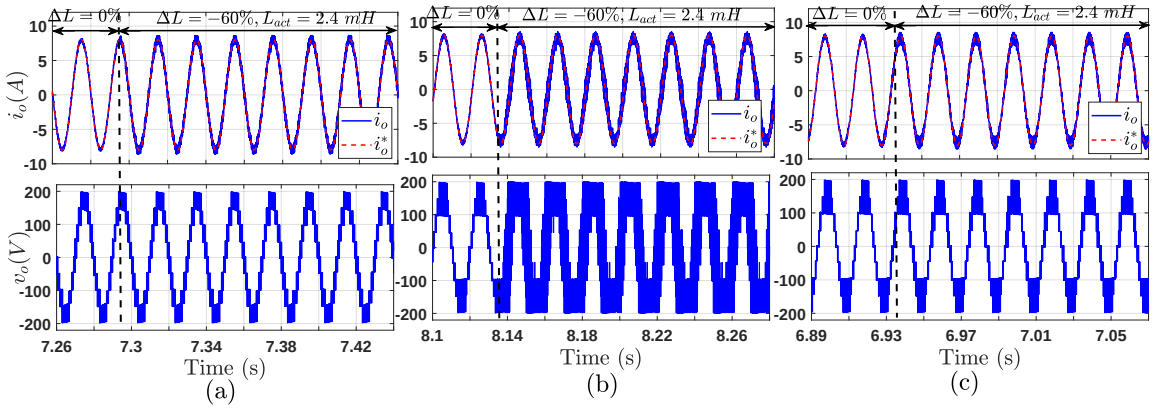


Figure 9.6: Experimental results for a -60% mismatch in the filter inductance with standalone load: (a) Classic PR controller with PWM, (b) Conventional FCS-MPC and (c) LMPC.

Table 9.5: Qualitative assessment of the control methods.

Method	Design Complexity	Gains/Weight. Factors	Explicit Modulator	Switching Freq.	Parameter Robustness	Steady-state Performance	Dynamic Performance	FCs Balance
Classic PR-PWM	✗✗	✗✗	Yes	Fixed	✓✓	✓✓	✗	✗✗
Classic FCS-MPC	✓✓	✗✗	No	Variable	✗	✓	✓✓	✓
Voltage-based MPC	✓	✓	No	Variable	✓	✓	✓✓	✓
Enhanced DB-MPC	✓	✓✓	Yes	Fixed	✓	✓✓	✓	✗✗
Dual-vector MPC	✓	✓	No	Fixed	✗	✓✓	✓✓	✓✓
Proposed LMPC	✓✓	✓✓	No	Variable	✓	✓	✓✓	✓

* Scaled from best (✓✓) to worst (✗✗).

the developed MPC method exhibits high performance in all control objectives, similar to the conventional method. Furthermore, the presented scheme has better robustness to parameter mismatch than the conventional MPC. The proposed scheme has been validated experimentally under different operating conditions. A comparative analysis is performed, comparing the proposed method with the PR controller and other state-of-the-art MPC methods, showcasing the proposed method's advantages. These advantages include eliminating gains or weighting factors, improved robustness, and effective control of the FCs. The research demonstrates the effectiveness of the proposed method in addressing the multi-objective control problem of FC-based converters.

CHAPTER 10

Conclusion and Future Outlook

This dissertation has focused on the topological structures and advanced control methods for MLIs applications. As an attempt to upgrade the well-established hybrid five-level topologies, like the commercial 5L-ANPC, two high-efficiency nine-level hybrid topologies have been developed. The proposed control methods have been implemented on the developed topologies, serving as an illustrative example of hybrid FC-based MLIs characterized by a limited number of redundant states. All designed control schemes have been experimentally validated with an RL load and grid-connected operation by constructing an experimental setup and HIL system in the laboratory, as discussed in Appendix B. Nevertheless, the methods proposed in this dissertation can be applied to other MLIs with some modifications according to the operation and structure of the considered topology.

10.1 Conclusion

The work conducted in this dissertation can be summarized as follows:

- In chapter 2, a comprehensive review of common dc-link MLIs has been conducted. This review includes the analysis of topological evolution, features, a comparison of different topologies, modulation techniques, and potential application areas. The findings of this chapter reveal that common dc-link topologies are the dominant choice in industrial applications due to their versatility and compatibility with different power conversion systems. Moreover, the review highlights the fact that most commercialized MLIs utilize common dc-link topologies. In addition, it has been demonstrated that there is still a need for further research in areas such as cost-effectiveness, efficiency, fault-tolerant operation and reliability to fully realize their potential.

- In chapter 3, a novel nine-level ANPC-based inverter topology has been proposed in this chapter with low number of active and passive components. The proposed topology has

been derived based on the commercially available 5L-ANPC inverter by adding a four-quadrant switch and an FC per phase-leg with reducing the voltage rated of the FCs. Exploiting the redundant states of the inverter, a balancing algorithm is designed for the dc-link and FCs. The developed algorithm has the ability to balance the two FCs with only one sensor, which further reduces the cost of the proposed 9L-SC-ANPC inverter. The designed balancing method has been integrated into the adopted PD-PWM strategy without the necessity for any external controller. Based on the PD-PWM, the mathematical analysis has been carried out to determine the capacitance values of the FCs and modulation index limitations. According to the analyzes and merits of the proposed 9L-SC-ANPC inverter, it is expected to be well appreciated in low- and medium-voltage medium power grid-connected applications.

- In chapter 4, A new nine-level T-type converter (9L-T^{2}C) has been presented in this chapter with a reduced number of power electronic components. The proposed converter can be configured using the commercially available 3L-T^{2}C with two LFSs per phase-leg. The proposed 9L-T^{2}C with the balancing algorithm has been validated for stand-alone and grid-connected operation under different operating conditions through simulation and experimental implementation. The operation at low values of modulation index ($M < 0.395$) for the 9L-SC-ANPC and 9L-T^{2}C has been addressed in this chapter with a simple way without transients or issues in the balancing of the FCs and NP potential.

  Based on the comparison and performance analysis, the 9L-SC-ANPC and 9L-T^{2}C outperform other common dc-link nine-level converters regarding the required number of active switches, capacitors, FCs voltage ratings, cost, and efficiency. Furthermore, thanks to the developed balancing algorithm, the FCs are stabilized at their reference using a single voltage sensor in steady-state and dynamic operation, resulting in further reduction in the system cost. Although the capacitance of the FCs in the proposed topologies is relatively large, the volume and cost are still quite acceptable due to their reduced voltage rating compared to most other topologies.

  Although the proposed 9L-SC-ANPC and 9L-T^{2}C have different configurations with different numbers and ratings of power devices (active switches and diodes), they have the same number of switching states and their operation is somewhat similar. The 9L-SC-ANPC has a fewer number of switches and slightly better efficiency, however, the 9L-T^{2}C has a lower TSV. Also, a salient feature of the 9L-T^{2}C is that it can be easily configured with the commercially available PEBBs, which is desirable from an industry perspective to reduces engineering efforts, testing times, volume, and costs.

- In chapter 5, the fundamentals, operating principles and technical challenges of the MPC for MLIs have been presented, focusing on FCS-MPC as the most popular approach for MLIs. The advances and effective solutions to each challenge have been discussed. Some prominent concepts have been validated and compared to evaluate their performance. Finally, the ongoing research points and future trends have been presented.

  MPC has demonstrated a high capability to handle the challenging multi-objective control problems of MLI applications with easy implementation, simplicity, and high dynamic performance. Although tremendous progress has been achieved over the last decade,

MPC still has some challenges that represent open research topics such as high computational burden for high number of levels ($N_{\text{level}} > 3$), weighting factors design, variable switching frequency operation of direct MPC, and sensitivity to model accuracy and parameters mismatch.

- In chapter 6, two improved FCS-MPC algorithms have been presented and implemented on the 9L-SC-ANPC. The mathematical analysis, prediction models and cost function design have been described. Only one weighting factor is used to realize three control objectives under all operating conditions, which saves the cumbersome effort required to coordinate the weighting factors. This is achieved by regulating the power flow between the dc-link capacitors and FC in the converter. Moreover, this method gets rid of the calculation efforts required for the voltage predictions of the dc-link capacitors.

  The proposed FCS-MPC methods in this chapter have addressed the parameter mismatch problem by designing an EKF-based parameter estimator. The developed algorithms empower the 9L-SC-ANPC converter to operate as a seven- or five-level inverter in the normal state or in the open-circuit fault condition of the bidirectional switch. According to the desired mode of operation, the proposed algorithms regulate the FCs voltages. Moreover, the number of iterations required to identify the optimal vector is significantly reduced, which, in turn, reduces the execution time of the MPC code as demonstrated by the experimental implementation. The feasibility and practicability of the proposed FCS-MPC methods have been verified through experimental implementation.

- In chapter 7, an improved robust DB-MPC method has been developed and applied to the single-phase 9L-SC-ANPC converter. The proposed method is suitable for single-phase ANPC-based MLIs. From the theoretical investigations and experimental results, the advantages of the proposed DB-MPC are summarized as follows:

  1. Like the FCS-MPC, the proposed DB-MPC addresses multiple control goals; current control, FCs balance and NP potential control. Moreover, unlike FCS-MPC, a constant switching frequency is achieved and no weighting factors are required, which saves the cumbersome effort required to adjust the weighting factors;
  2. Thanks to the designed EKF-based estimator, the proposed method has better robustness compared to the traditional FCS-MPC;
  3. Like the traditional FCS-MPC at the nominal system parameters, the proposed DB-MPC has high tracking quality and an effective balance of FCs and NP in steady-state and dynamic operation; and
  4. Comparing with FCS-MPC, the developed DB-MPC has a lower calculation burden;

- In chapter 8, a reduced-complexity dual-vector FCS-MPC has been proposed for FC-based MLIs. This method significantly reduces the computational burden by directly locating the two best vectors without requiring multiple evaluations of the cost function. Mathematical analyses have been performed to determine the optimal duration of the selected voltage vectors. While the sequence of two voltage vectors is determined based on the THD definition to reduce its value. From this chapter, the following points are concluded

1. Compared to the conventional FCS-MPC, the proposed MPC method has a lower computational load and therefore a shorter execution time, despite the application of two vectors per control cycle T_s;
2. Using the same concept proposed in chapter 6, The proposed scheme can handle three control goals with a single weighting factor;
3. Both conventional and proposed MPC methods can accurately track the reference current while achieving strong balancing of the dc-link and FCs. However, at the same sampling frequency, the proposed scheme exhibits better tracking quality, lower THD, and improved harmonic distribution;
4. At low output frequencies, the proposed MPC strategy has better performance in terms of FCs balancing and current tracking;
5. At the same average switching frequency, both MPC methods have almost similar performance. However, the proposed dual-vector MPC scheme has a better harmonic distribution, which simplifies filter design; and
6. Both MPC methods show low sensitivity and acceptable performance for inductance variations within $\pm 30\%$.

- In chapter 9, a Lyapunov-based MPC method has been proposed to realize weighting factorless cost function in multi-objective control problems. The results demonstrated that the developed MPC method exhibits high performance in all control objectives, similar to the conventional method. Furthermore, the presented scheme has better robustness to parameter mismatch than the conventional MPC. A comparative analysis is performed, comparing the proposed Lyapunov-based MPC with the PR controller and other proposed MPC methods in this dissertation, showcasing the advantages of the proposed method. These advantages include eliminating gains or weighting factors, improved robustness, and effective control of the FCs. The classic PR controller and all developed MPC methods have been experimentally compared for grid-connected operation in this chapter.

10.2 Future outlook

Currently, three-level and five-level topologies are considered matured and widely developed/manufactured by companies for many applications. As industries seek higher efficiency and improved power density in the next generation of power electronic converters, and based on the work done in this dissertation, the future research directions could be listed as follows:

- Optimization of the design of MLIs taking into account the recent advances in power device technologies. Exploiting the available variety in the wide-bandgap devices such as SiC and GaN power devices can reduce the cost of the topology and improve the power density and efficiency of the MLIs.

- Proposing novel voltage balancing strategies/external pre-charging circuits to reduce the capacitors size and voltage ripples,

- Although the operation of the 9L-SC-ANPC and 9L-T^{2}C is ensured under the faulty case of the four-quadrant switch S_8, it is suggested to investigate the operation under the fault conditions of other power switches in future work. In addition, the operation at low line frequencies with PWM-based techniques is recommended to be considered with ensuring the FCs and dc-link balance.

- The proposed MPC methods in this dissertation have been applied on single-phase nine-level inverters. However, the concepts can be adapted to the three-phase system. A future work of the three-phase implementation is recommended.

- All designed MPC schemes in this work consider a short prediction-horizon $(N_p = 1)$. The long-horizon MPC is suggested for better steady-state and stability performance. However, the implementation of long-horizon direct MPC for MLIs exacerbates the challenge of computational burden, necessitating the exploration of strategies to mitigate the extensive calculation efforts.

- Weighting factorless sequential MPC for MLIs can eliminate the complex tuning process, but more research should be devoted to how to avoid the suboptimal problems. Compared with the MPC with a regular cost function, it should be proved that weighting factorless-MPC is able to provide the same or even better control performance.

- Due to a larger number of components, the control algorithms for MLIs have to also focus on the reliability of the components. Especially the FCS-MPC has a lot of freedom in the cost-function design to include objectives that can improve the reliability of the MLIs, something that is not very straightforward for conventional linear control algorithms. The challenge here lies in finding the optimum stress distribution of the components (both the semiconductor devices and capacitors) that will ensure the longest lifetime of the converter.

APPENDIX A

List of publications

A.1 Journal papers

The following Journal papers are mainly related to the doctoral research topic and have been published as outcomes of this work.

1. **I. Harbi**, M. Ahmed, C. M. Hackl, R. Kennel and M. Abdelrahem, "A Nine-Level Split-Capacitor Active-Neutral-Point-Clamped Inverter and Its Optimal Modulation Technique", *IEEE Transactions on Power Electronics*, vol. 37, no. 7, pp. 8045-8064, July 2022.

2. **I. Harbi**, M. Ahmed, J. Rodriguez, R. Kennel and M. Abdelrahem, "A Nine-Level T-Type Converter for Grid-Connected Distributed Generation", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 5, pp. 5904-5920, October 2022.

3. **I. Harbi**, M. Ahmed, J. Rodriguez, R. Kennel and M. Abdelrahem, "Low-Complexity Finite Set Model Predictive Control for Split-Capacitor ANPC Inverter With Different Levels Modes and Online Model Update", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 1, pp. 506-522, February 2023.

4. **I. Harbi**, M. Ahmed, C. M. Hackl, J. Rodriguez, R. Kennel and M. Abdelrahem, "Low-Complexity Dual-Vector Model Predictive Control for Single-Phase Nine-Level ANPC-Based Converter", *IEEE Transactions on Power Electronics*, vol. 38, no. 3, pp. 2956-2971, March 2023.

5. **I. Harbi**, M. Ahmed, M. L. Heldwein, R. Kennel and M. Abdelrahem, "Enhanced Fault-Tolerant Robust Deadbeat Predictive Control for Nine-Level ANPC-Based Converter", *IEEE Access*, vol. 10, pp. 108492-108505, October 2022.

6. **I. Harbi**, et al., "Model Predictive Control of Multilevel Inverters: Challenges, Recent Advances, and Trends", *IEEE Transactions on Power Electronics*, vol. 38, no. 9, pp. 10845-10868, September 2023.

7. **I. Harbi**, et al., "Common DC-Link Multilevel Converters: Topologies, Control and Industrial Applications", *IEEE Open Journal of Power Electronics*, vol. 4, pp. 512-538, July 2023.

8. **I. Harbi**, M. Abdelrahem, M. Ahmed, and R. Kennel, "Reduced-complexity model predictive control with online parameter assessment for a grid-connected single-phase multilevel inverter", *Sustainability*, vol. 12, no. 19, pp. 7997, September 2020.

9. **I. Harbi**, Hamza Makhamreh, M. Ahmed, J. Rodriguez, R. Kennel and M. Abdelrahem, "Multi-Objective Control of Nine-Level T-Type Converter: A Robust and Gain-Free MPC Method", *IEEE Transactions on Industrial Electronics*, Submitted, 2023.

The following Journal papers have been published during the doctoral studies at TUM. However, these are not directly linked to the dissertation.

10. M. Ahmed, **I. Harbi**, R. Kennel, J. Rodriguez and M. Abdelrahem, "Model-Based Maximum Power Point Tracking Algorithm With Constant Power Generation Capability and Fast DC-Link Dynamics for Two-Stage PV Systems", *IEEE Access*, vol. 10, pp. 48551-48568, May 2022.

11. M. Ahmed, **I. Harbi**, C. M. Hackl, R. Kennel, J. Rodriguez and M. Abdelrahem, "Maximum power point tracking-based model predictive control with reduced sensor count for PV applications", *IET Renewable Power Generation*, early access, doi.org/10.1049/rpg2.12535.

12. M. Ahmed, **I. Harbi**, R. Kennel and M. Abdelrahem, "Direct Power Control Based on Dead-Beat Function and Extended Kalman Filter for PV Systems", *in Journal of Modern Power Systems and Clean Energy*, early access, doi: 10.35833/MPCE.2021.000793.

13. M. Ahmed, **I. Harbi**, R. Kennel, J. Rodriguez and M. Abdelrahem, "An improved photovoltaic maximum power point tracking technique-based model predictive control for fast atmospheric conditions", *Alexandria Engineering Journal*, vol. 63, pp. 613-624, December 2022.

14. M. Ahmed, **I. Harbi**, R. Kennel and M. Abdelrahem, "Maximum Power Point Tracking Implementation under Partial Shading Conditions Using Low-Cost Photovoltaic Emulator", *Eng*, vol. 3, no. 4, pp. 424-438, October 2022.

15. M. Ahmed, **I. Harbi**, R. Kennel, J. Rodriguez and M. Abdelrahem, "Evaluation of the Main Control Strategies for Grid-Connected PV Systems", *Sustainability*, vol. 14, no. 18, pp. 11142, September 2022.

16. M. Ahmed, **I. Harbi**, R. Kennel, M. L. Heldwein, J. Rodriguez and M. Abdelrahem, "Performance Evaluation of PV Model-Based Maximum Power Point Tracking Techniques", *Electronics*, vol. 11, no. 16, pp. 2563, August 2022.

17. M. Ahmed, **I. Harbi**, R. Kennel, J. Rodriguez and M. Abdelrahem, "Maximum Power Point Tracking-Based Model Predictive Control for Photovoltaic Systems: Investigation and New Perspective", *Sensors*, vol. 22, no. 8, pp. 3069, April 2022.

18. M. Ahmed, M. Abdelrahem, A. Farhan, **I. Harbi**, and R. Kennel, "DC-link sensorless control strategy for grid-connected PV systems", *Electrical Engineering*, vol. 103, no. 1, pp. 2345–2355, February 2021.

19. M. Ahmed, **I. Harbi**, R. Kennel and M. Abdelrahem, "Predictive Fixed Switching Maximum Power Point Tracking Algorithm with Dual Adaptive Step-Size for PV Systems", *Electronics*, vol. 10, no. 24, pp. 3109, Dec. 2021.

20. M. Ahmed, **I. Harbi**, R. Kennel and M. Abdelrahem, "Dual-mode power operation for grid-connected PV systems with adaptive DC-link controller", *Arabian Journal for Science and Engineering*, vol. 47, no. 1, pp. 2893–2907, July . 2021.

21. M. Ahmed, M. Abdelrahem, **I. Harbi** and R. Kennel, "An adaptive model-based MPPT technique with drift-avoidance for grid-connected PV systems", *Energies*, vol. 13, no. 24, pp. 6656, December 2020.

A.2 Conference papers

The following conference papers are mainly related to the doctoral research topic and have been published as outcomes of this work.

1. **I. Harbi**, M. Abdelrahem, M. Ahmed, R. Kennel and J. Rodriguez, "Finite Set Model Predictive Control for Split-Capacitor Active-Neutral-Point-Clamped Inverter with Different Voltage Levels Operating Modes", *in IEEE International Conference on Predictive Control of Electrical Drives and Power Electronics (PRECEDE 2021)*, Jinan, China, 20-22 Nov. 2021, pp. 167-172.

2. **I. Harbi**, M. Abdelrahem, M. Aref, M. Ahmed and R. Kennel, "Computationally Efficient FCS-MPC for Single-Phase Five-Level ANPC Inverter", *in the 22^{nd} International Middle East Power Systems Conference (MEPCON 2021)*, Assiut, Egypt, 14-16 Dec. 2021, pp. 643-647.

3. **I. Harbi**, M. Abdelrahem, M. Ahmed and R. Kennel, "Weighting Factorless Reduced-Complexity FS-MPC for Modified Packed U-Cell Inverter Topology", *in proceedings of International Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM 2021)*, Nuremberg, Germany, 03-07 May 2021, pp. 1-8.

4. **I. Harbi**, M. Abdelrahem, R. Kennel and C. M. Hackl, "Simplified Model Predictive Current Control for Single-Phase Multilevel Inverter", *in the 46^{th} Annual Conference of the IEEE Industrial Electronics Society (IECON 2020)*, Singapore, 18-21 Oct. 2020, pp. 3079-3084.

5. **I. Harbi**, M. Abdelrahem, M. Ahmed and R. Kennel, "Model Predictive Control with Switching Frequency Minimization for Modified Packed U-cell Inverter", *in the 5th IEEE Workshop on the Electronic Grid (eGRID 2020)*, Aachen, Germany, 02-04 Nov. 2020, pp. 1-5.

6. **I. Harbi**, Hamza Makhamreh, M. Ahmed, M. Abdelrahem, M. L. Heldwein, J. Rodriguez and R. Kennel, "Multi-Objective Control of Nine-Level ANPC Converters: A Robust and Gain-Free MPC Method", *in IEEE International Conference on Predictive Control of Electrical Drives and Power Electronics (PRECEDE 2023)*, Wuhan, China, 16-19 Jun. 2023, pp. 51-67.

7. **I. Harbi**, M. Ahmed, M. Abdelrahem, J. Rodriguez and R. Kennel, "Low Modulation Index Operation of a Nine-Level T-Type Converter", *in IEEE International Future Energy Electronics Conference (IFEEC 2023)*, Sydney, Australia, 20-23 November 2023, pp. 493-497.

The following conference papers have been carried out during the doctoral studies at TUM. However, these are not directly linked to the dissertation.

8. M. Abdelrahem, M. S. Bin Arif, **I. Harbi**, M. Ahmed and R. Kennel, "Model Predictive Control for 17-Levels Inverter in PV systems", *in proceedings of International Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM 2022)*, Nuremberg, Germany, 10-12 May 2022, pp. 1-6.

9. M. Ahmed, M. Abdelrahem, **I. Harbi** and R. Kennel, "Predictive Model-based Maximum Power Point Tracking Technique for PV Applications with Reduced Sensor Count", *in proceedings of International Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM 2021)*, Nuremberg, Germany, 03-07 May 2021, pp. 1-6.

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A.3 Awards

1. **Best paper award**, received from the 2023 IEEE International Conference on Predictive Control of Electrical Drives and Power Electronics (PRECEDE 2023), Wuhan, China, for the paper entitled “Multi-Objective Control of Nine-Level ANPC Converters: A Robust and Gain-Free MPC Method”.

APPENDIX B

Test Benches

The test benches utilized to validate the work has been constructed in the laboratory of the Chair of High-Power Converter Systems at the Technical University of Munich. These test benches includes power electronic converters and a real-time control system. Furthermore, a Hardware-in-the-loop system has been built to validate some MPC methods on different topologies, namely the three-phase 5L-ANPC in grid-connected operation.

B.1 Experimental setup of the 9L-SC-ANPC and 9L-T^{2}C topologies

The experimental setup used to validate the proposed topologies and the developed MPC methods is shown in Fig. B.1. The validation of the proposed 9L-SC-ANPC and 9L-T^{2}C topologies with its developed PWM-based strategy has been verified on the experimental platform. Fig. B.2 shows the experimental prototype of the nine-level topologies. The system parameters and hardware components used in the experimental validation are given in Table B.1. Other operating system parameters are changed according to the control method and the investigated point. Therefore, these parameters are given in the respective chapter in the thesis at the beginning of the experimental results section. The dSpace Microlabbox has been used as a real-time controller. A dead time of 2 μs is provided by the built-in FPGA in the dSpace Microlabbox. The measured data are plotted in MATLAB after being exported from the dSPACE by controlDesk software. The quality of the figures of this method is higher than that of DSO. However, for some control methods like dual-vector MPC, the measurements are captured with high sampling frequency using Oscilloscope DPO-2024 with a sampling rate of 62.5 kHz.

The main components of the system are shown in Fig. B.2. The complete test bench has been constructed from scratch, starting at the component level. This involved the use of 1200-kV Infineon's IGBT module with the design of suitable gate drivers, as shown in Fig. B.3. High-performance, fully isolated, multi-channel, current and voltage sensor boards (USM-3IV Taraz)

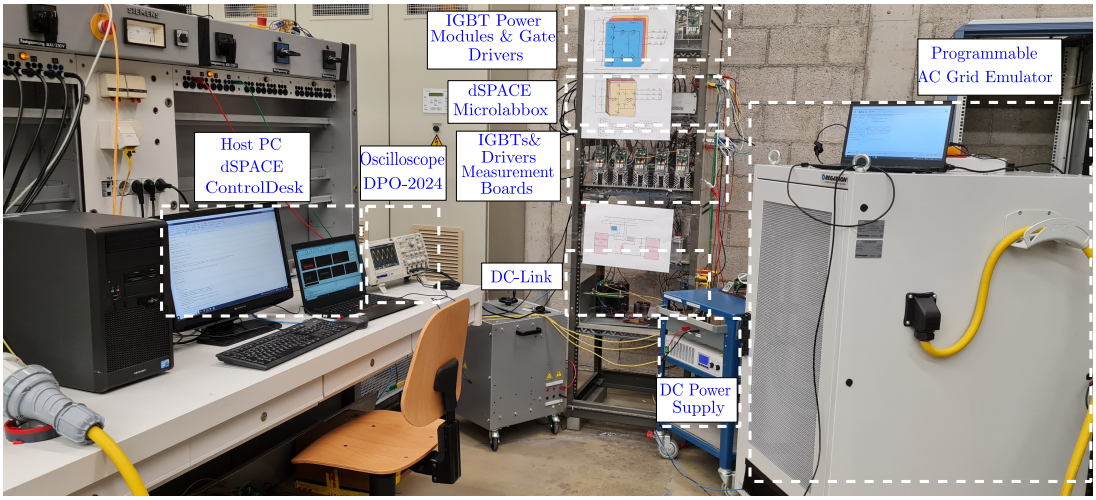

Figure B.1: Experimental setup in the laboratory.

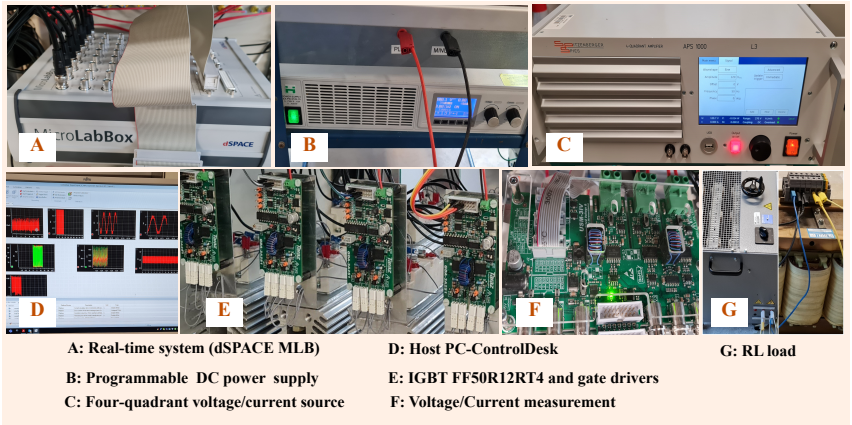

Figure B.2: Main Components of the setup.

are used to measure the system voltages and currents. Each board has the capability to measure

Table B.1: Experimental setup details.

Parameter	Experimental
Input DC source, V_{dc}	400 V
Line frequency, f_{line}	50 Hz
dc-link capacitors, C_1 and C_2	3300 μF
Hardware components	
Power switch, IGBT	FF50R12RT4
Power Diode	IDP30E65D1
Gate driver	GDA-3A2S1
Measurements board	USM-3IV Taraz
dc power supply	EA-PSI 8720-15
Controller	dSPACE Microlabbox

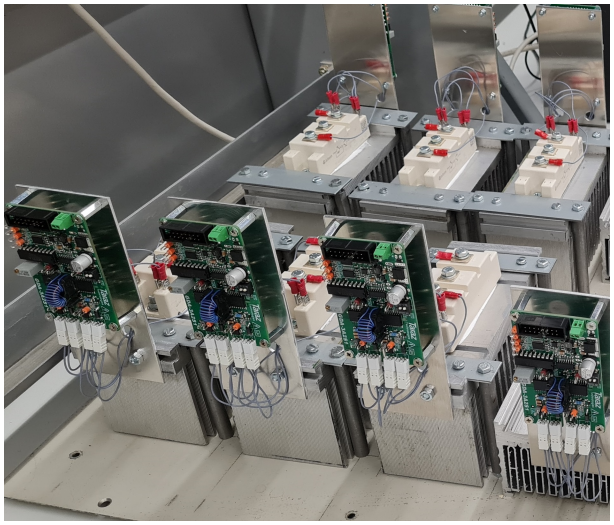

Figure B.3: IGBT modules with gate drivers.

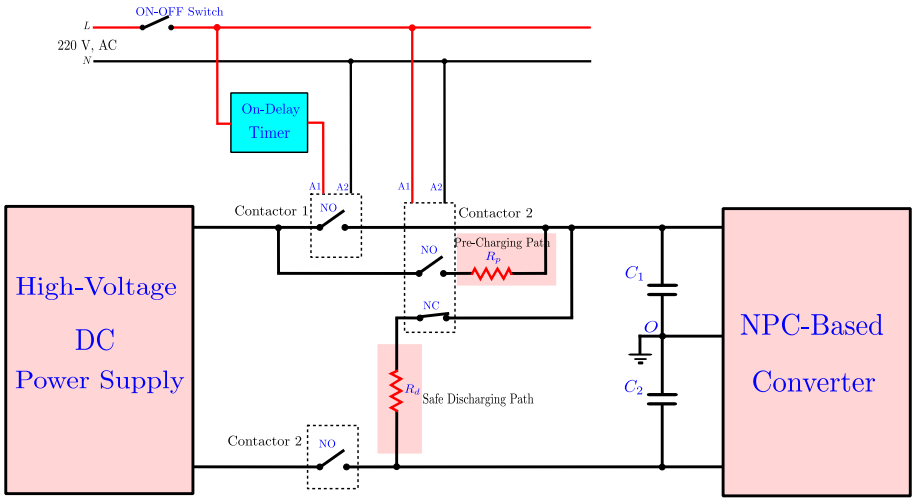

Figure B.4: Precharging of the dc-link for NPC-based topologies.

three voltages and three currents. The voltage range is ± 1 kV, and the current range is ± 100 A, which can be reduced by having many turns across the current sensor. A four-quadrant voltage/current source, shown in Fig. B.1, is used as the AC grid.

The inclusion of a precharging circuit for the dc-link is necessary for the safe and reliable operation. Fig. B.4 shows the schematic of the used precharging circuit. This circuit gradually charges the dc-link capacitors to the DC source voltage before the main power switches are enabled through resistor R_p. By gradually increasing the voltage, the precharging circuit prevents sudden inrush currents that could cause significant stress on capacitors. After sufficient time, as specified on the delay timer, conductor 1 is ON bypassing the precharging resistor. The same circuit is used for the safe discharging of the dc-link through resistor R_d, after the inverter switches are turned off.

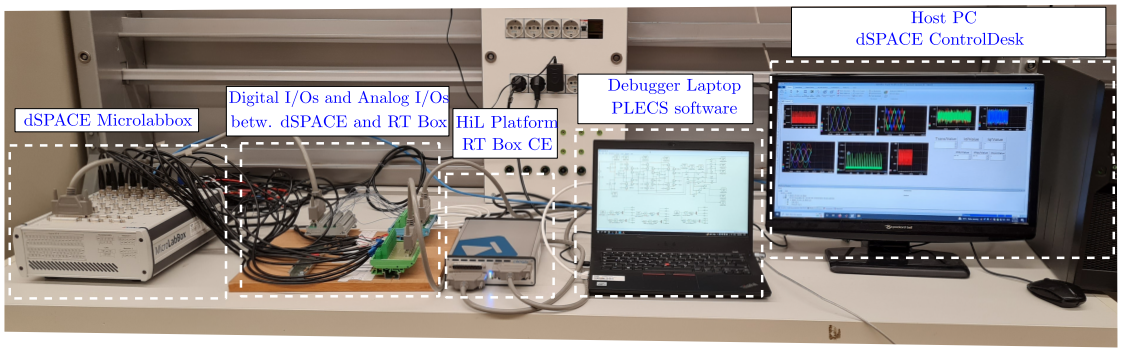

Figure B.5: Hardware-in-the-loop setup.

Table B.2: System parameters of the HIL implementation for grid-connected three-phase 5L-ANPC inverter.

Parameter	Value
dc-link, V_{dc}	700 V
Grid voltage, $v_{g,l-l}$	380 V (rms)
Grid frequency, f_f	50 Hz
Filter resistance, R_f	0.1 Ω
Filter inductance, L_f	10 mH
dc-link capacitors, C_1 and C_2	2000 μF
FC, C_f	1000 μF
Sampling time, T_s	100 μs

B.2 Hardware-in-the-loop system

The controller HIL setup has been built using the RT Box from Plexim as a real-time simulator for the power part of the system (5L-ANPC inverter and the grid). Microlabbox from dSPACE is used as a digital platform for the control implementation. The HIL setup is shown in Fig. B.5. The system parameters for this validation are given in Table. B.2. Several MPC methods are implemented on this system to be compared at the same operating parameters, as explained in Chapter 5.

APPENDIX C

List of symbols and abbreviations

C.1 List of symbols

$\mathbb{N}, \mathbb{R}, \mathbb{C}$	Sets of natural, real and complex numbers
$\boldsymbol{x}$	Real valued (state) vector
$\boldsymbol{u}$	Input vector
$\boldsymbol{y}$	Output vector
$\boldsymbol{A}$	State matrix
$\boldsymbol{B}$	Input matrix
$\boldsymbol{C}$	Output matrix
v_m	Modulation signal
t	Time (continuous)
k	Current Sample (discrete)
$\frac{d}{dt}$	Time derivation
T_s	Sampling time
f_s	Sampling frequency
f_{line}	Line frequency
f_c	Carrier frequency
f_{sw}	Switching frequency
$f_{\text{sw,avg}}$	Average switching frequency
g	Cost function
J_L	Lyapunov function
abc	Natural three-phase reference frame
$\alpha\beta$	Stationary two-phase reference frame
dq	Synchronously rotating two-phase reference frame
$\boldsymbol{T}_C$	Clarke transformation
$\boldsymbol{T}_P(\phi)$	Park transformation

ω_e	Frequency of the grid voltage
ϕ_e	Electrical position of the grid voltage
i_o	Inverter output current
i_o^*	Inverter reference current
v_o	Inverter output voltage
v_o^*	Inverter reference voltage
V_{dc}	dc-link voltage
i_{dc}	Input current of the dc-link
C_1, C_2	dc-link capacitors
V_{c1}, V_{c2}	Voltages of the dc-link capacitors
i_{c1}, i_{c2}	Currents of the dc-link capacitors
C_{f1}, C_{f2}	Flying capacitors
V_{f1}, V_{f2}	Voltages of the FCs
i_{f1}, i_{f2}	Currents of the FCs
V_f^*	Reference voltage of the FCs
$V_{f,P}^*$	Reference voltage of the FCs in the positive half-cycle
$V_{f,N}^*$	Reference voltage of the FCs in the negative half-cycle
$V_{f-\text{NP}}^*$	Reference voltage of the FCs including NP balancing
V_r	Voltage ripple of a capacitor (peak-to-peak)
P_{c1}	Total power supplied by the upper capacitor C_1 of the dc-link
P_{c2}	Total power supplied by the lower capacitor C_2 of the dc-link
P_1	Power supplied by C_1 to the load in the positive half-cycle
P_2	Power supplied by C_2 to the load in the negative half-cycle
P_{1f}	Power supplied by C_1 to the FCs in the positive half-cycle
P_{2f}	Power supplied by C_2 to the FCs in the negative half-cycle
P_{fp}	Power supplied by the FCs to the load in the positive half-cycle
P_{fn}	Power supplied by the FCs to the load in the negative half-cycle
n	Number of extension units
N_{level}	Number of voltage levels
N_{st}	Number of converter states
N_{sw}	Number of active switches
N_{driv}	Number of gate drivers
N_d	Number of diodes
N_{FCs}	Number of FCs
M	Modulation index
M_{min}	Minimum modulation index
ΔQ_{fx1}	Charge variation of C_{fx1} during a complete sinusoidal cycle
ΔQ_{fx2}	Charge variation of C_{fx2} during a complete sinusoidal cycle
$\Delta Q_{\text{fx1}}^{3E}$, $\Delta Q_{\text{fx1}}^{2E}$, $\Delta Q_{\text{fx1}}^{-E}$, $\Delta Q_{\text{fx1}}^{-2E}$	Charge variation of C_{fx1} during levels $3E$, $2E$, $-E$ and $-2E$
$\Delta Q_{\text{fx2}}^{2E}$, $\Delta Q_{\text{fx2}}^{E}$, $\Delta Q_{\text{fx2}}^{-2E}$, $\Delta Q_{\text{fx2}}^{-3E}$	Charge variation of C_{fx2} during levels $2E$, E, $-2E$ and $-3E$
Z	Load impedance
ϕ	Power factor angle
R, L	Total resistance and inductance of filter and load
R_f, L_f	Resistance and inductance of the output filter
$\boldsymbol{v}_g$	Grid voltage

λ, λ_s, λ_1, λ_2	Weighting factors
γ_1, γ_2	Positive gains of Lyapunov cost function
K_p	Proportional gain of the PR controller
K_i	Resonant gain of the PR controller

C.2 List of abbreviations

AC	Alternating current
DC	Direct current
WTS	Wind turbine system
PEBB	Power electronics building block
VC	Vector control
PC	Model predictive control
FCS-MPC	Finite-control-set model predictive control
CCS-MPC	Continuous-control-set model predictive control
LMPC	Lyapunov-based model predictive control
DMPC	Direct model predictive control
DB-MPC	Deadbeat model predictive control
EKF	Extended Kalman filter
WF	Weighting factor
RES	Renewable energy source
BTB	Back-to-back
MPPT	Maximum power point tracking
VSC	Voltage source converter
IGBT	Insulated gate bipolar transistors
PWM	Pulse width modulation
SVM	space vector modulation
FOC	Field-oriented control
VOC	Voltage-oriented control
THD	Total harmonic distortion
TDD	Total demand distortion
DSP	Digital signal processing
FPGA	Field programmable gate array
DTC	Direct torque control
DPC	Direct power control
P&O	Perturb and Observe
PLL	Phase-locked loop
VV	Voltage vector
SSE	Steady-state error
OPP	Optimized pulse pattern
M^2PC	modulated model predictive control
MLC	Multilevel converter
MLI	Multilevel inverter
BV	Blocking voltage
DG	Distributed generation
FC	Flying capacitor
NPC	Neutral point clamped
CHB	Cascaded H-bridge
ANPC	Active neutral point clamped

NP	Neutral point
LFS	Low-frequency switch
PF	Power factor
PMSG	Permanent magnet synchronous generator
PUC	Packed U-cell converter
MPUC	Modified packed U-cell converter

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