Electronic Circuits for High Bit Rate Digital Fiber Optic Communication Systems

JOHANN GRUBER, PETER MARTEN, REINHARD PETSCHACHER, AND PETER RUSSER

Abstract—**This paper describes electronic components for digital fiber optic transmitters and receivers with bit rates from several hundred Mbits/s up into the Gbits/s range. In particular, drivers and multiplexers suitable for direct laser modulation were developed for use in the transmitter units. A laser light output control circuit for independent stabilization of the minimum and peak to peak laser light output levels is described. A demultiplexer and clock regenerator circuit was developed for optical receivers. All high speed components were realized in thin film hybrid integrated technology using silicon bipolar transistors, Schottky diodes and step recovery diodes.**

1. INTRODUCTION

As a result of progress in injection laser and optical fiber technologies, high bit rate fiber optic communication links will become feasible within the next few years. Length×bandwidth products of 1 GHz km have already been achieved with graded index multimode fibers [1]. Even higher bandwidths are obtainable with single mode fibers which exhibit a pulse dispersion of 80 ps per kilometer fiber length and per nanometer spectral width of the optical signal at the wavelength of GaAs injection lasers [2]. Fiber attenuation values below 5 dB/km are obtainable with silica material. Modern GaAs injection lasers have a cw lifetime of several 10 000 hours and a direct modulation capability of up to 2 Gbits/s [3-6]. The spectral width of multimode injection lasers ranges between 1 and 3 nm whereas monomode injection lasers have a spectral width below 0.1 Å. In addition, silicon avalanche photodiodes exhibit a cutoff frequency of 3 GHz and a gain-bandwidth product of 250 GHz [7]. The present stage of development of optical components therefore allows laboratory experiments to be carried out with gigabit rate optical transmission in fiber optic links several kilometers long [8-10].

The need for suitable electronic components arises from the desire to utilize the high bandwidth capability of the above-mentioned optical components. High bit rate electronic circuit design currently makes use of silicon bipolar transistors, GaAs MESFET's, Gunn effect digital devices, Schottky diodes and step recovery diodes as the amplifying and switching devices [11-22]. This paper describes electronic components for fiber optic communication transmitters and receivers capable of bit rates from several hundred Mbits/s to over 1 Gbit/s. The aim of our work was to develop a set of electronic components which would allow maximum flexibility in later system design. We used silicon bipolar transistors as the active devices for bit rates up to 1 Gbit/s, and step recovery diodes for pulse amplification at bit rates of 1 Gbit/s and higher. The use of silicon bipolar transistors facilitates the construction of digital circuits with a lower voltage swing but with a sufficient noise margin. Furthermore, compatibility can be achieved with monolithic integrated ECL circuits.

In the next section a bipolar transistor driver for direct injection laser modulation is described. The third section deals with a control circuit for stabilizing the laser light output against the influences of temperature variation and laser degradation, and in the next two sections, multiplexers with transistors and step recovery diodes are considered, both suitable for direct laser modulation. The sixth section describes an ECL gate suitable for Gbit/s application, and the final section deals with a demultiplexer and clock regenerator circuit.

Most of the circuits were realized using hybrid integrated thin film technology with chip components on alumina substrates. In some cases resistors were also realized using tantalum nitride thin film technology. The chips were mounted on the substrate with a conductive epoxy compound. Connections to the semiconductor chip components were made by thermal compression bonding. Alumina substrates with a completely gold layered bottom surface were used. This bottom surface was used as the ground plane. Through connections to the ground plane were formed, by 0.45 mm, ultrasonically drilled holes plugged with gold wire.

2. THE LASER DRIVER

A hybrid integrated laser driver using bipolar transistors has been developed for direct modulation of injection lasers with high bit rate PCM signals. GaAs double heterostructure injection lasers usually have threshold currents of up to a few hundred milliamperes. Once above threshold, wellbehaved lasers exhibit an approximately linear dependence of light output power on current with a slope of approximately 0.15-0.3 mW/mA. For high bit rate direct modulation, injection lasers must be biased up to threshold in order to avoid a delay between the modulation current pulse and the light output pulse [3]. Control of the bias current and the modulation amplitude must be possible since the threshold current as well as the slope of the light output characteristic may change over long periods of operation. Laser diodes have a low impedance above

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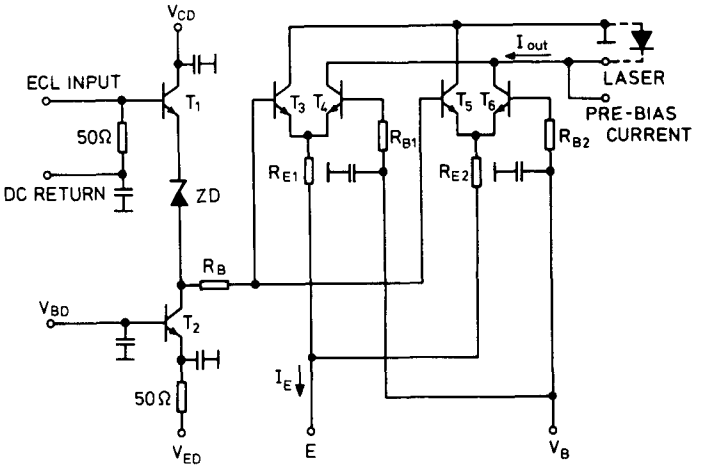

Fig. 1. Circuit diagram of the laser driver.

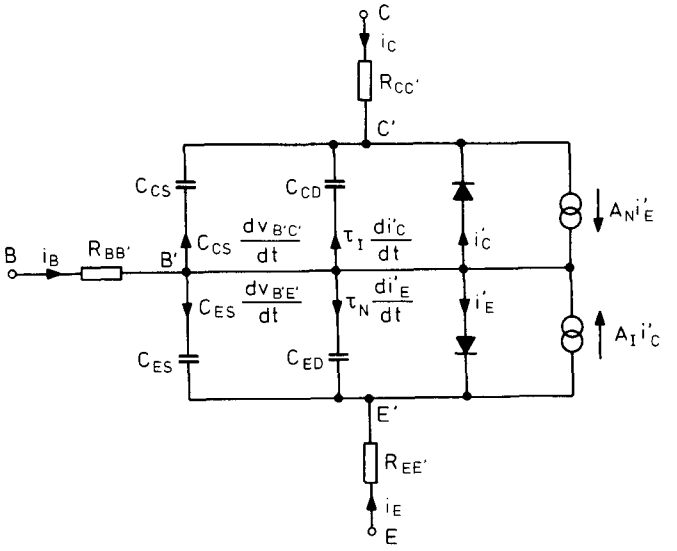

Fig. 2. Modified Ebers-Moll bipolar transistor model.

threshold which is determined mainly by the bulk resistance and the bonding wire inductance. The laser driver should therefore be a high impedance current source.

All these requirements are best filled by a differential amplifier constructed with bipolar transistors. Fig. 1 shows the circuit diagram of the laser driver which consists of an input stage and two differential amplifiers connected in parallel. A 50 Ω input impedance is obtained using emitter follower T_1 and the 50 Ω resistor parallel to the input. T_2 acts as a current source and Zener diode ZD shifts the signal baseline so that the input can be driven from standard ECL levels. Two paralleled differential amplifiers ($T_3 \cdots T_6$) deliver a sufficient modulation current amplitude. The emitter resistors R_{E1}, R_{E2} ensure equal current distribution between the two differential amplifiers. The input current is controlled by a dc control current I_E fed to the differential amplifiers. Due to the limiting behavior of the differential amplifiers, the output current amplitude is independent of the output signal amplitude and has a faster rise time.

The complete laser driver was simulated with a non-linear circuit analysis program in order to optimize the circuit [23]. The transistors were represented by the modified Ebers-Moll model shown in Fig. 2. The dependence of the non-linear depletion layer capacitance on applied voltage, the base transit time (and hence the diffusion capacitance) and the base spreading resistance were determined from pulse transmission and reflection measurements [24]. Both measurements and the subsequent parameter evaluations were carried out on a digital processing oscilloscope fitted with a time domain reflectometer unit. In addition, inductances resulting from the thin film layout configuration, the bonding wires, and the resistor and capacitor series inductances were measured and taken into consideration by the circuit simulation.

In order to check the transistor model, a computer simulation of a single differential amplifier was performed and compared with measurements made on a hybrid integrated test circuit (Fig. 3). When operated with a low impedance load resistor (2 Ω), the unavoidable stray inductances and transistor capacitances may cause pulse overshoot and sometimes even instability. This tendency is increased by the series inductance

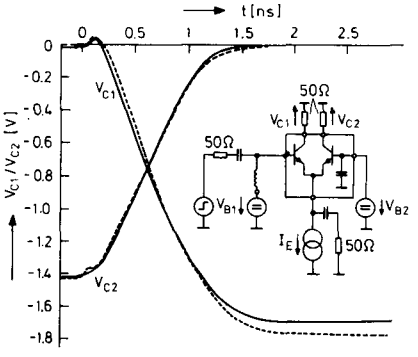

Fig. 3. Measured (- - -) and calculated (—) output voltage transient of a differential amplifier test structure. Bipolar transistors with 3.5 GHz cutoff frequency were used.

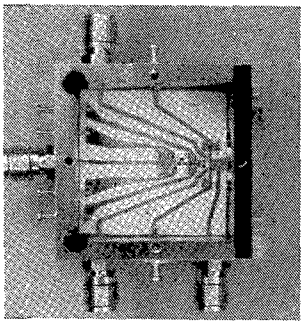

Fig. 4. Photograph of the laser driver.

of the load. To overcome these difficulties, damping resistors R_{B1}, R_{B2} and, in some cases R_B, were inserted. Various driver stages with different transistor types for different maximum output currents and different rise times have been developed. Fig. 4 shows a photograph of the laser driver assembled on a 1″ × 1″ alumina substrate. The resistors were realized by tantalum nitride films with a 50 Ω sheet resistance. In this version, the Zener diode was replaced by four transistor base emitter diodes.

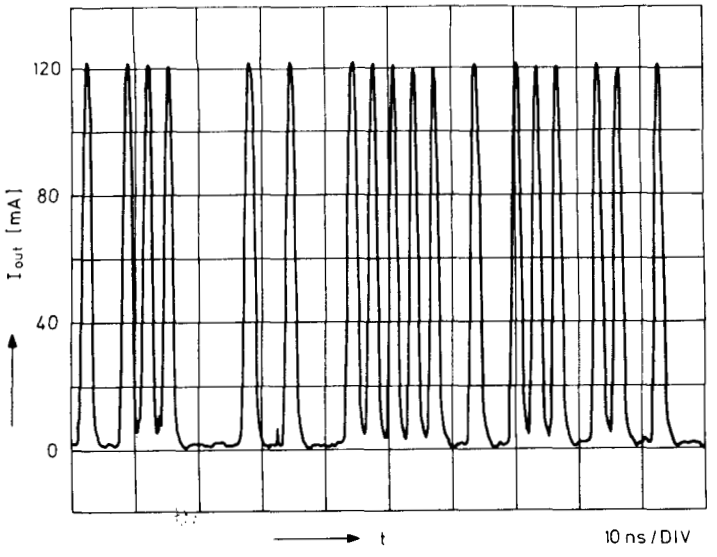

Fig. 5. Output current waveform of the laser driver for a 300 Mbit/s RZ signal (f_T = 5 GHz).

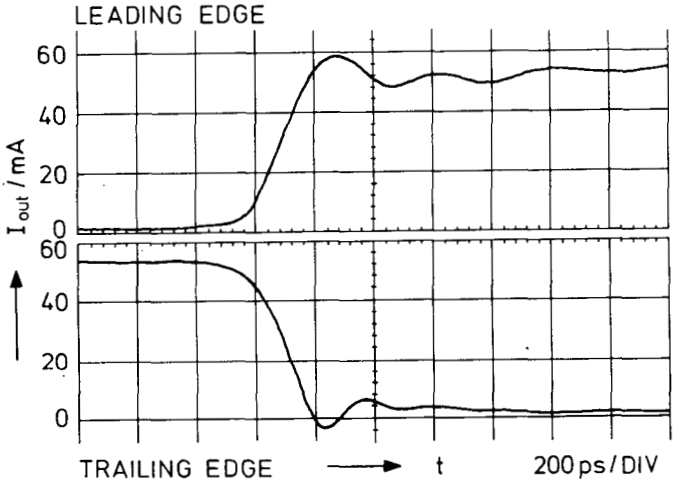

Fig. 6. Switching characteristics of the laser driver using bipolar transistors with f_T = 8 GHz. The Switching 10 to 90 percent switching time is 200 ps.

The amplifiers were terminated with a 2 Ω disk resistor in order to measure the output current waveform. Fig. 5 shows the output waveform of a driver stage modulated with a 300 Mbit/s signal. Medium power microwave transistors with a 5 GHz cutoff frequency were used in the differential amplifiers yielding maximum output amplitude of 120 mA and switching times under 500 ps. When fitted with subnanosecond switching transistors with an 8 GHz cutoff frequency, switching times under 200 ps (between 10 and 90 percent) were achieved with a 50 mA output pulse amplitude. Fig. 6 shows the switching characteristics of this driver measured with an input step pulse having a 400 ps rise time. This example shows the pulse forming capability even for short transition times. An injection laser modulation experiment with a 1 Gbit/s PCM return to zero signal has been performed using this driver. Fig. 7a shows the detected light output signal measured for a 118 mA bias current and 25 mA modulation amplitude. The driver output current waveform at maximum modulation amplitude (60 mA) is shown in Fig. 7b. An AEG-Telefunken $GaAl_{1-x}As$ double heterostructure injection laser with ion implanted stripe geometry (I_{th} = 108 mA) was used. The power consumption of the laser drivers depends on the modulation amplitude. At maximum modulation amplitude it is 1 W for the driver version with 120 mA maximum amplitude and 0.5 W for the high speed version in Figs. 6 and 7 with 60 mA maximum modulation amplitude.

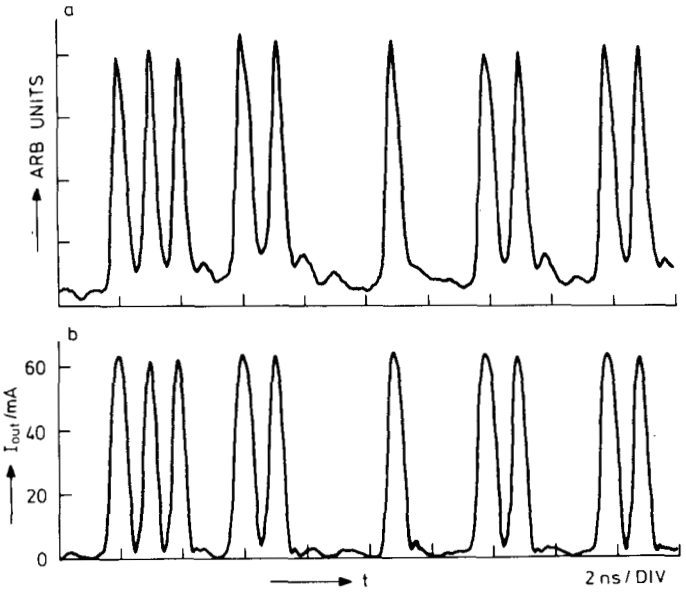

Fig. 7. Direct modulation of a $Ga_xAl_{1-x}As$ injection laser by the laser driver with 1 Gbit/s RZ-signal. a) Detected light output signal. b) Driver output current waveform at maximum modulation amplitude.

3. THE LASER CONTROL CIRCUIT

The function of the laser control circuit is to stabilize the laser light output signal against the influences of temperature changes and degradation during long periods of operation. Both the laser threshold current and the slope of the light output power versus injection current characteristic may change. It is necessary however, to keep the modulation amplitude of the optical output signal constant to ensure a constant signal level at the receiver. Furthermore, the laser must be dc biased slightly above threshold. If the bias is too low, this yields bit pattern dependent modulation distortions [3], whereas an excessive bias level enhances the shot noise in the receiver and also increases the laser degradation rate. All requirements are met by a control circuit which controls the dc laser bias current and the modulation current amplitude. This circuit stabilizes the temporal minimum output level and the modulation amplitude of the light output power. Fig. 8 shows the basic circuit diagram of the laser control circuit. A similar circuit has already been proposed by Epworth [25]. The light output of the laser diode LD is monitored by the PIN photo diode PD. This is accomplished by optically coupling the photo diode to the rear face of the laser diode LD. Tapping the outgoing optical fiber with a trans-

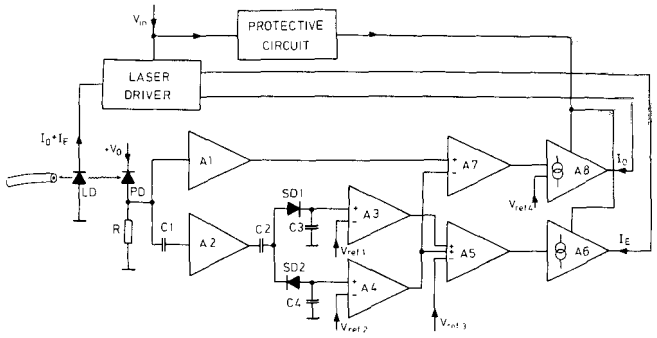

Fig. 8. Basic circuit diagram of the laser control circuit.

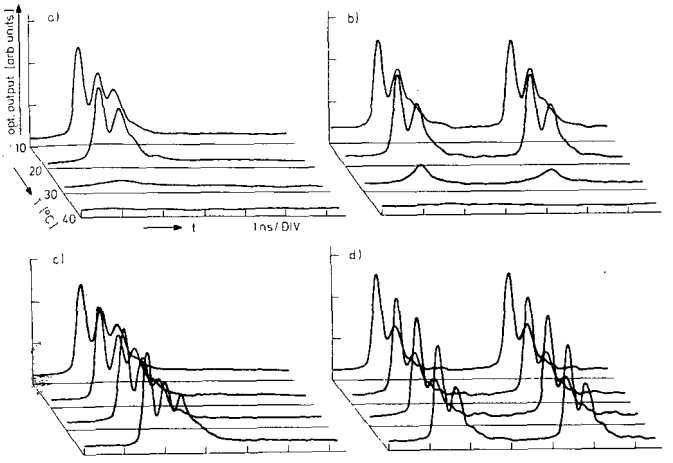

Fig. 9. Laser modulation with 280 Mbits/s at temperatures between 10° and 40° centigrade without (a, b) and with (c, d) level control. No optical output signal occurred without level control at 40°C. A single "1"-bit within a 16 bit frame (a, c), and all bits set to "1" (b, d).

parent photodiode is also possible [26]. The photo diode PD is reverse biased in order to obtain a low junction capacity. The electrical output signal of the photo diode PD is then fed into the low drift dc amplifier A1 and also into the broadband ac amplifier A2. The output signal of A1 is proportional to the temporal mean value P_{av} of the laser light output power. The ac part of the monitoring signal is peak detected after amplification by A2. The positive peak detector is formed by Schottky diode SD1 and capacitor C3, the negative peak detector consists of SD2 and C4. The reference voltages V_{ref1} and V_{ref2} are supplied by voltage divider networks which compensate for the temperature dependence of SD_1, SD_2 and the subsequent amplifiers A3 and A4. Since the dc part of the monitoring signal has been removed by C1, A2, and C2, the output signal of A3 is proportional to $(P_{max} - P_{av})$ and the output signal of A4 is proportional to $(P_{av} - P_{min})$, where P_{max} and P_{min} are the maximum and minimum laser light output powers within a certain interval of time. The sum signal, proportional to $(P_{max} - P_{min})$ is formed in A5 and compared with the reference voltage V_{ref3}. The desired value of $(P_{max} - P_{min})$ is set up with V_{ref3}. The amplifier A6 has a current source output and controls the dc current I_E fed to the differential amplifiers of the laser driver. In this way the modulation amplitude is controlled. The difference between the output signals of A1 and A4 is formed in amplifier A7 in order to generate the bias control signal. The output voltage of A7, which is proportional to P_{min}, is compared with the reference voltage V_{ref4} in A8. The amplifier A8 also has a current source output and supplies the dc laser bias current I_o which can be adjusted via V_{ref4}.

The operation of the control circuit is independent of the "0"-"1" probability ratio of the PCM laser modulation signal. Identical transient behavior of the narrow-band amplifiers A1, A3 and A4 ensures correct functioning of the control circuit even when the "0"-"1" probability ratio changes rapidly with time. The control circuit also contains a protective circuit which can switch off the output currents of A6 and A8. When the transmitter supply voltage is switched on, the protective circuit generates a 50 ms switch-on delay of I_o and I_E in order to guarantee correct operation of the control circuit at the time when the laser is switched on. Furthermore, the protective circuit switches off I_o and I_E if no modulation pulse occurs in a time interval longer than 50 μs. The switch-on process is made sufficiently slow to avoid an overshoot of I_o and I_E. During normal operation of the transmitter, time intervals of 50 μs without modulation pulses do not occur and the protective circuit will not disturb the transmission.

The control circuit was built up on a PC-board. A1 is a dc amplifier with 1 μV/°C offset voltage drift whereas A2 consists of four cascaded broadband amplifiers with 44 dB total gain. The amplifiers A6 and A8 consist of operational amplifiers with additional Darlington output stages, operated as current sources by means of series feedback in the usual way. The output currents I_E and I_o are gated from the protective circuit via additional bipolar Darlington transistor switches. The control circuit was dimensioned with an open-loop gain of 80 and for a settling time of 100 ms.

Measurements with 280 Mbit/s RZ-PCM signals were performed with a continuous bit stream and a single "1"-bit within a 16-bit frame. Fig. 9 shows the detected laser light output measured at different temperatures between 10° and 40° centigrade with and without light output control. An AEG-Telefunken low mesa stripe geometry $Ga_xAl_{1-x}As$ double heterostructure injection laser was used in the experiment. Considerable suppression of the temperature dependence of the laser light output signal was achieved with the control circuit. We measured P_{min} and $(P_{max} - P_{min})$ using a digital processing oscilloscope which was calibrated by comparing the calculated mean value of the PIN diode output with mean power measurements made with a calibrated photo-element. The results are listed in table 1. A slight decrease of optical output power at 10° possibly is due to wet laser end faces.

4. THE TRANSISTOR MULTIPLEXER

A transistor multiplexer, suitable for direct laser modulation, has been developed in order to multiplex four parallel bit streams into a single 1 Gbit/s signal. The circuit, shown in Fig. 10 is based on a circuit given by White [27] and consists of four differential amplifier units with their outputs connected in parallel. Each of the four differential amplifier units consists of three differential amplifiers connected in parallel. A 250 Mbit/s signal is applied to each of the input terminals

TABLE 1
TEMPERATURE T DEPENDENCE OF THRESHOLD CURRENT I_{th}, BIAS CURRENT I_O, AMPLITUDE CONTROL CURRENT I_E, MINIMUM OPTICAL OUTPUT POWER P_{min} AND PEAK TO PEAK VALUE OF THE OPTICAL POWER $(P_{max} - P_{min})$

T(°C)	I_{th}(mA)	I_0(mA)			I_E(mA)			P_{min}(mW)				$P_{max} - P_{min}$ (mW)			
		a,b	c	d	a,b	c	d	a	b	c	d	a	b	c	d
10	179	190	190	173	50	50	74	0.87	1.35	0.87	0.83	8.09	7.88	8.15	8.85
15	180	190	188	169	50	52	78	0.56	1.03	0.85	0.84	8.34	7.90	7.94	8.80
20	185	190	196	175	50	54	81	0.62	0.88	0.83	0.81	6.73	7.46	8.23	8.81
30	202	190	204	178	50	59	97	0.56	0.76	0.83	0.81	0.60	1.72	8.33	9.06
40	220	190	227	206	50	58	87	—	—	0.82	0.83	—	—	8.41	8.66

Note: The measurements were performed with fixed I_O and I_E (a, b) values and with level control (c, d); for a single "1"-bit within a 16 bit frame (a, c) and for all bits set to "1" (b, d).
- No output.

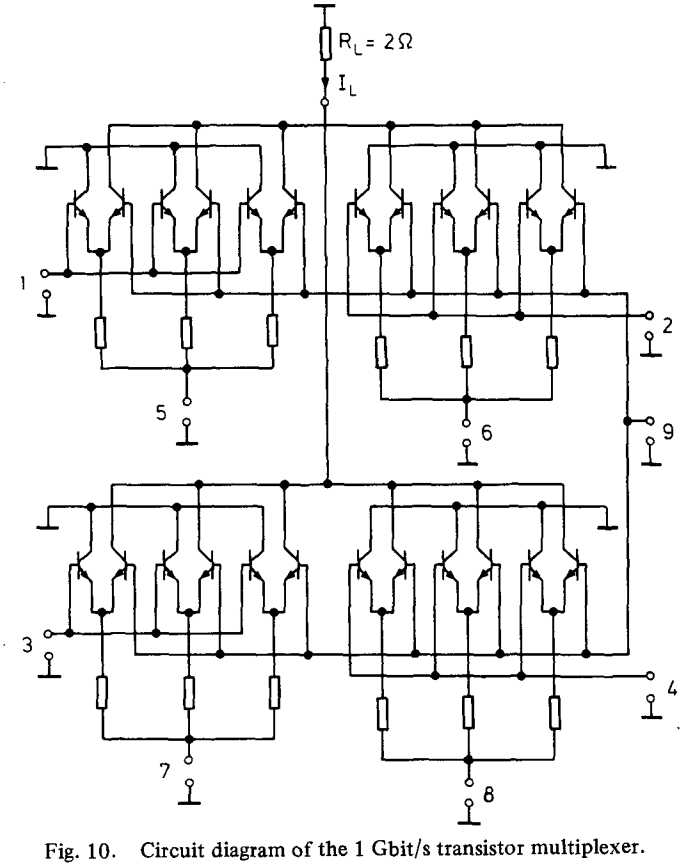

Fig. 10. Circuit diagram of the 1 Gbit/s transistor multiplexer.

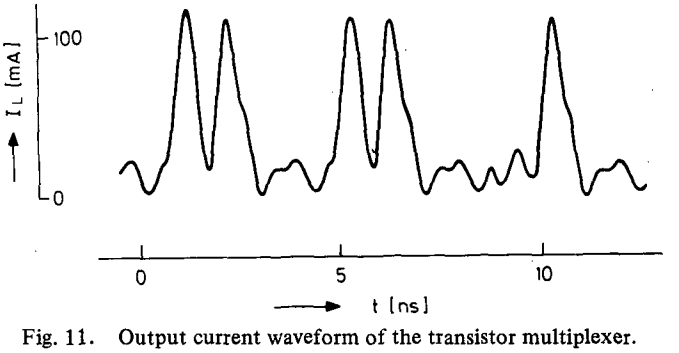

Fig. 11. Output current waveform of the transistor multiplexer.

1···4. In addition, periodic 250 MHz pulse trains, consisting of narrow pulses with negative polarity are applied to terminals 5···8. The pulse trains at terminals 5···8 have a mutual delay of 1 ns and sequentially gate the four differential amplifiers. The PCM signals applied to the input terminals 1···4 are synchronous to the gating pulses and are also mutually shifted by one nanosecond in order to ensure the proper phase relationship to the associated gating pulse train. The 1 Gbit/s multiplexer was implemented on a 1" × 1" alumina substrate using transistors with a cutoff frequency of 3.5 GHz. 1 Gbit/s RZ signals with 150 mA maximum amplitude can be generated by this transistor multiplexer. Fig. 11 shows the waveform of the output signal current measured across a 2 Ω load resistor. The gating pulse trains were generated by a single step recovery diode pulse former followed by a 1:4 power divider. A dc bias current can be added in the same way as in the single differential amplifier. Amplitude control can be achieved by varying the gating pulse train amplitudes.

5. THE STEP RECOVERY DIODE MULTIPLEXER

The step recovery diode multiplexer described in this section combines four parallel bit streams into one PCM signal and provides an output amplitude sufficient to drive an injection laser. The multiplexer consists of four step recovery diode amplifiers paralleled at the output.

First we shall briefly discuss the principle of operation of step recovery diode pulse amplifiers. The utilization of the charge storage effect in semiconductor junction diodes for pulse amplifications was first proposed more than 20 years ago

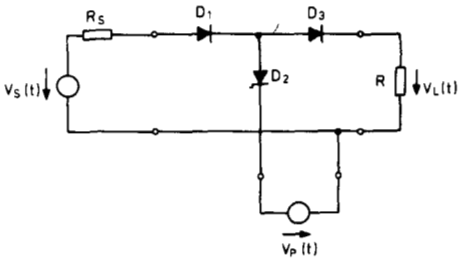

Fig. 12. Basic circuit diagram of the step recovery diode amplifier.

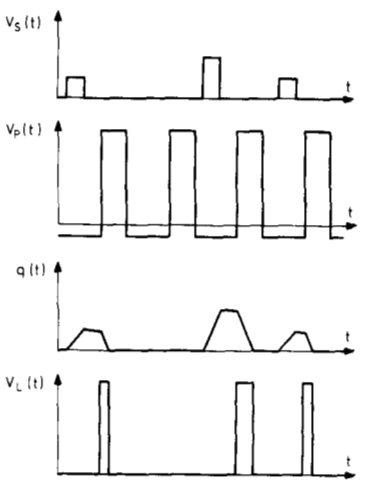

Fig. 13. Ideal signal waveforms in the step recovery diode amplifier.

[28, 29]. The application of this principle to the development of subnanosecond pulse amplifiers became feasible with the availability of modern step recovery diodes [18-20]. Fig. 12 shows the basic circuit diagram of the step recovery diode amplifier. D_2 is a step recovery diode, and D_1 and D_3 are Schottky diodes. R_S is the source impedance, $V_S(t)$ is the open circuit voltage of the source, $V_P(t)$ is the pump voltage, and $V_L(t)$ is the output voltage appearing across the load resistor R_L. Fig. 13 shows the ideal signal waveforms in the step recovery diode amplifier. The step recovery diode D_2 is charged by the input voltage pulses $V_S(t)$ supplied by the signal source. During the input pulses the charge $q(t)$ of the step recovery diode D_2 increases. After the end of the input pulse $q(t)$ only decreases slightly due to the finite recombination lifetime which is of the order of 50 ns in D_2. Thereafter the charge in D_2 is removed by a reverse polarity pump pulse. During the pump pulse a discharge current flows through D_2, D_3 and R_L. As soon as the positive charge in D_2 is fully removed, this diode switches off within a time of approximately 100 ps. The pump voltage source $V_P(t)$ supplies a periodic pulse train which is slightly negative between the pump pulses. Consequently, the input pulses arriving between the pump pulses pass through D_2 and not D_3.

The output pulse area is proportional to the input pulse area. With increasing pump pulse amplitude the output pulse amplitude increases and the output pulse width decreases. Although the charge amplification factor is smaller than 1, the output current amplitude can be considerably higher than the input current amplitude if the output pulse width is smaller

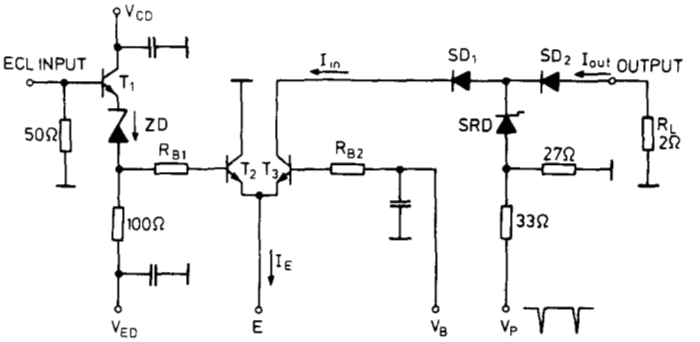

Fig. 14. Circuit diagram of the step recovery diode amplifier with transistor preamplifier.

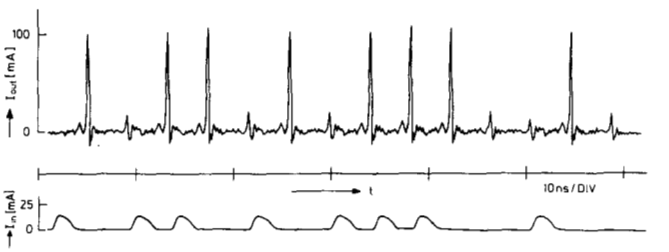

Fig. 15. Signal waveforms of I_{in} and I_{out} in the circuit depicted in Fig. 14.

than the input pulse width. However, voltage amplification and therefore also power amplification can be achieved by appropriate choice of the pump voltage and R_L. The reader may compare the step recovery diode amplifier with a common base bipolar transistor amplifier. D_2 acts like the emitter-base diode during the charge process and like the base-collector diode during the discharge process. The step recovery diode amplifier is well suited for pulse regeneration applications, since the timing of the output pulses depends on the pump pulses, and since pulse narrowing is possible.

Fig. 14 shows the circuit diagram of a step recovery diode amplifier with a transistor preamplifier. A 50 Ω input resistance and level shifting (by ZD) for ECL compatibility is achieved by the first stage (T_1). In the second stage (T_2, T_3) the amplitude of the input current I_{in}, and hence the amplitude of I_{out} are controlled by the impressed dc current I_E. Amplification of a 250 Mbit/s PCM signal has been measured. Fig. 15 shows the output signal of the driver stage and the output signal of the step recovery diode amplifier, the latter measured across a 2 Ω load resistor. The output current pulse amplitude is 100 mA, the pulse halfwidth is 200 ps. The pump signal voltage V_P is supplied by a step recovery diode pulse generator with a 15 V open circuit pulse amplitude and 400 ps pulse halfwidth. Due to pulse narrowing in the step recovery diode amplifier, the output amplitude of 100 mA is achieved with an I_{in} pulse amplitude of only 13 mA.

Due to the small output pulse width, a multiplexer can be simply realized by parallel connection of a number of step recovery diode amplifiers. Fig. 16 shows the circuit diagram of such a multiplexer. Fig. 17 shows the ideal signal waveforms in the multiplexer. $V_{S1} \cdots V_{S4}$ are the input signals, $V_{P1} \cdots V_{P4}$ are the pulsed pump signals for the four step recovery diode

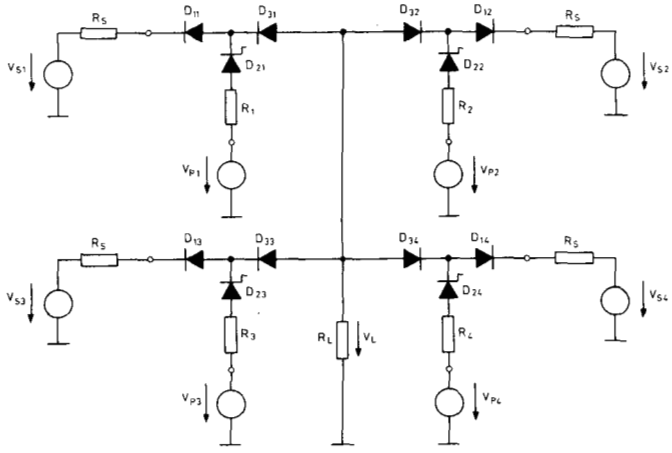

Fig. 16. Circuit diagram of the step recovery diode multiplexer.

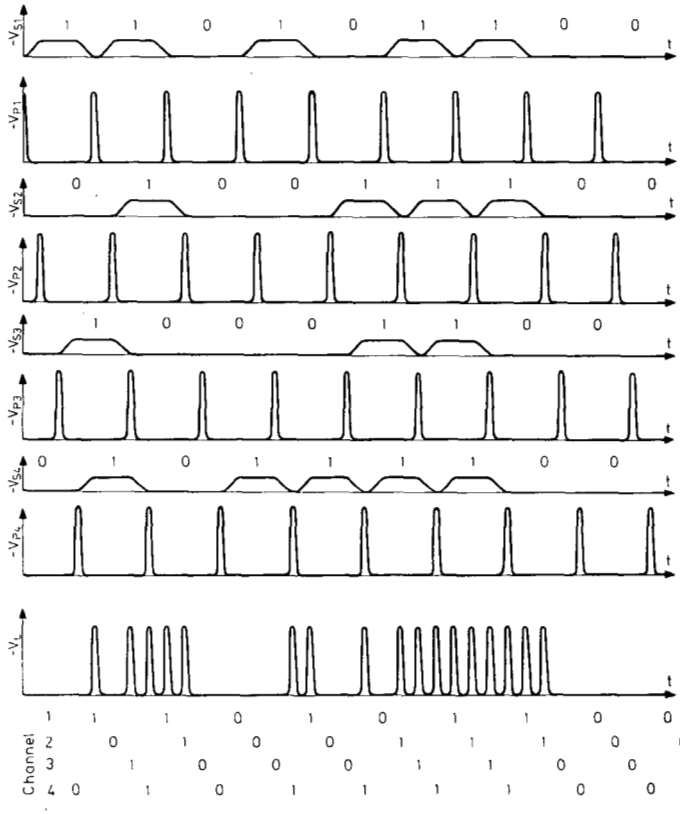

Fig. 17. Ideal signal waveforms in the step recovery diode multiplexer.

amplifiers. Signal and pump voltages for the four step recovery diode amplifiers are mutually shifted by a quarter input clock interval. The output Schottky diodes $D_{31} \cdots D_{34}$ act as an OR gate. The matching of the pump voltage lines is improved by the resistors $R_1 \cdots R_4$. The multiplexer was realized in hybrid integrated thin film technology on a $1'' \times 1''$ alumina substrate. Fig. 18 shows a photograph of the multiplexer. The performance of the multiplexer was measured for pulse rates between 1 Gbit/s and 3.3 Gbits/s. Fig. 19 shows the experimental results for 1 Gbit/s RZ-multiplexing, Fig. 20 for 3.3 Gbits/s NRZ-multiplexing. The pump signals for the multiplexer were derived from a single step recovery diode pulse generator using a power divider and coaxial delay lines.

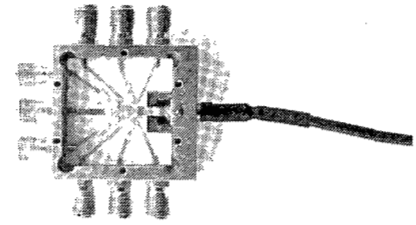

Fig. 18. Photograph of the step recovery diode multiplexer.

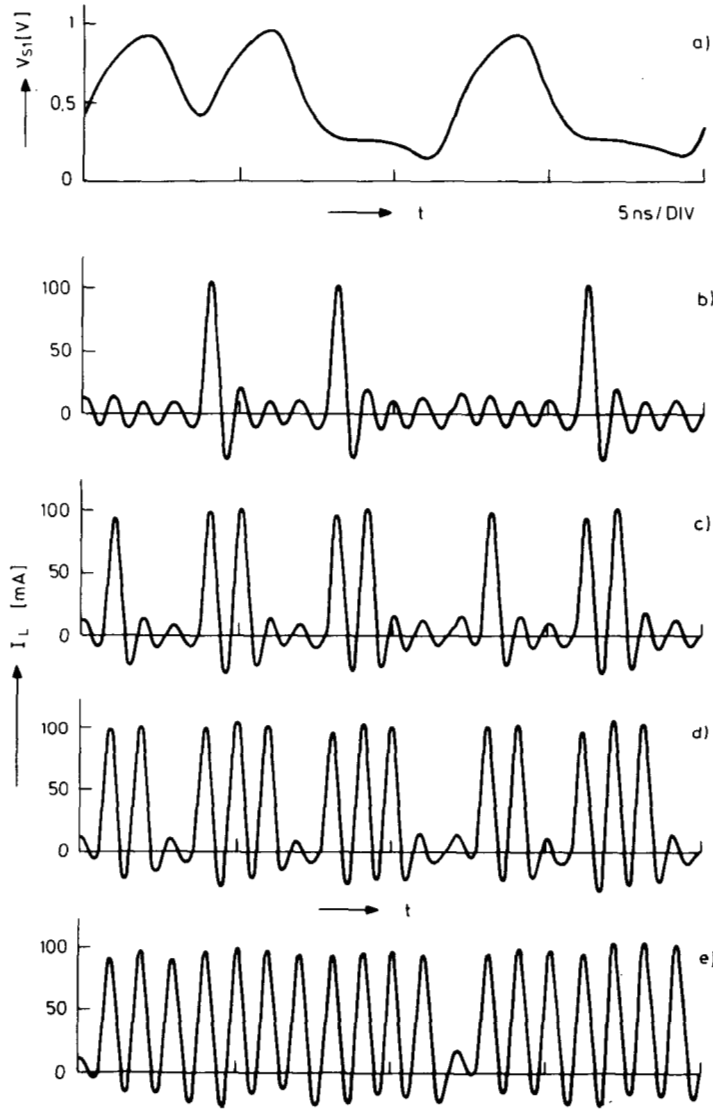

Fig. 19. Signal waveforms of the 1 Gbit/s step recovery diode multiplexer. a) Bit pattern generator monitoring signal at channel 1. b) to e) Output current waveforms for different stationary levels applied to the other three input channels.

6. THE ECL GATE

An ECL OR gate in thin film hybrid integrated technology was realized for Gbit/s applications. Fig. 21 shows the circuit diagram of the gate. The principle of operation is the same as in monolithic integrated ECL circuits. High speed switching transistors with a cutoff frequency of 8 GHz (T_1 to T_3) and 6 GHz (T_4) were used. The hybrid integrated ECL gate is fully

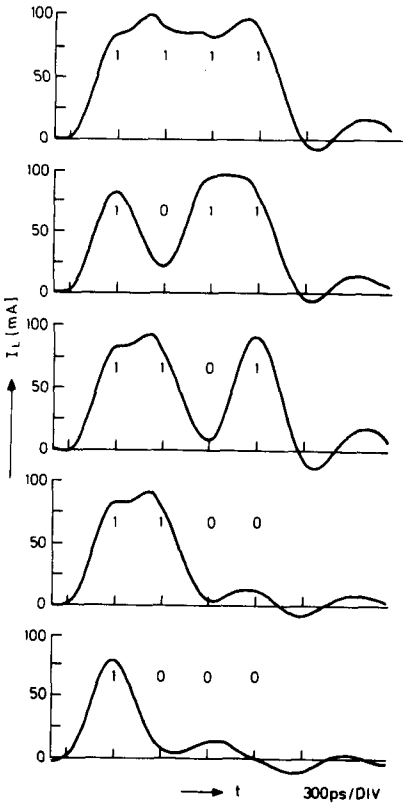

Fig. 20. Output signal waveforms of the step recovery diode multiplexer operated at 3.3 Gbits/s for different bit patterns.

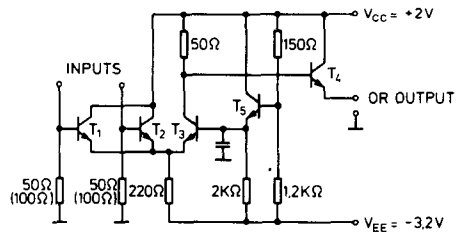

Fig. 21. Circuit diagram of the hybrid ECL OR gate.

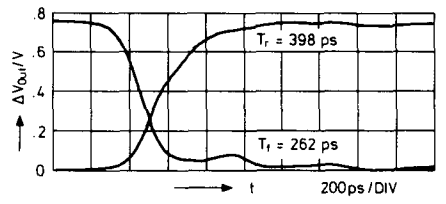

Fig. 22. Switching characteristics of the ECL OR gate.

compatible with conventional monolithic ECL circuits with respect to the logic levels and supply voltages. The use of the two supply voltages +2 V and −3.2 V allows the use of a 50 Ω output load termination. The output swing is greater than 0.7 V with a low level smaller than 0.35 V and a high level greater than 1.05 V. Fig. 22 shows the switching characteristic of a gate with 50 Ω input pull-down resistors. The 10 to 90 percent rise time is less than 400 ps and the fall time less than 270 ps. The total power consumption of the gate is 150 mW.

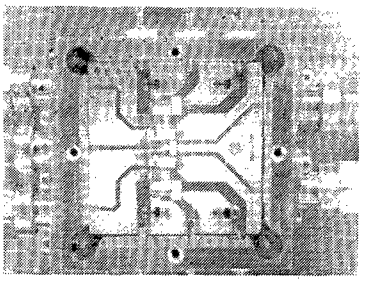

Fig. 23. Photograph of a hybrid integrated dual OR gate.

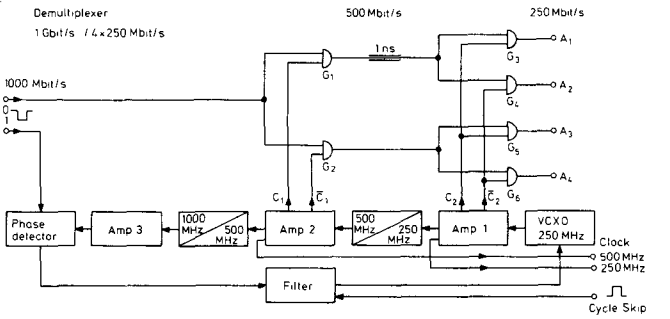

Fig. 24. Basic circuit diagram of the demultiplexer and clock regenerator circuit.

Fig. 23 shows a photograph of a dual OR gate mounted on a 1″ × 1″ alumina substrate.

7. THE DEMULTIPLEXER AND CLOCK REGENERATOR CIRCUIT

A demultiplexer for 1 Gbit/s input signals was realized using the hybrid integrated ECL gates described in the preceding section. The multiplexer is combined with a PLL clock regeneration circuit which provides all clock signals needed in the multiplexer.

Fig. 24 shows the basic circuit diagram of the demultiplexer and clock regenerator circuit. The demultiplexing is performed in two stages: in the first stage the 1 Gbit/s input signal is gated by two 500 MHz clock signals C_1 and $\bar{C}_1$ with opposite phases. The input channel is thus demultiplexed into two parallel 500 Mbit/s channels. A 1 ns delay line in the upper 500 Mbit/s channel removes the time shift between the output channels of the first demultiplexer stage. In the second stage the demultiplexing into four 250 Mbit/s channels is performed by gating with two 250 MHz clock signals C_2 and $\bar{C}_2$ of opposite phases. Negative logic is used in the demultiplexer so that the logic AND operations in the demultiplexer can be performed by the OR gates. In the first stage a dual OR gate with 50 Ω input pull-down resistors is used in which the PCM signal inputs to the two gates are internally connected. The OR gates in the second demultiplexer stage have 100 Ω input pull-down resistors in order to allow the gate outputs of the first stage to drive two gate inputs in parallel. 50 Ω coaxial transmission lines were used to interconnect the gates in the first stage and 100 Ω transmission lines were used in the second stage. Since all transmission lines are correctly terminated at their output ends, delay equalization is easily obtained by an appropriate choice of the line length.

A second order phase locked loop is used for clock regeneration [30]. Second order phase-locked loops are advantageous for clock extraction when compared with resonant circuits since they yield low static as well as low dynamic phase errors [31]. Furthermore, we decided to use a VCXO as the local oscillator since a phase-locked loop with a low noise bandwidth can then be realized. The VCXO operates at 250 MHz and has a maximum relative tuning range of $\pm 10^{-4}$. The clock signals at 250 MHz, 500 MHz and 1 GHz are derived from a chain of clock amplifiers and passive frequency doublers. The phases of the 1 GHz clock signal and the 1 Gbit/s input signal are compared in the phase detector. The VCXO control is derived via an active filter from the phase detector output.

Each of the clock amplifiers 1 and 2 consists of two differential amplifiers with an emitter follower output which are driven by a common emitter follower input stage. One of these differential amplifiers generates the two anti-phase clock signals to drive the demultiplexer gates, whereas the other differential amplifier drives the subsequent frequency doubler and also provides a clock output for external signal processing. Using a linear circuit analysis program, the gain of each amplifier was adjusted in order to obtain power levels appropriate for optimum operation of the subsequent frequency doubler and the demultiplexer gates. The amplifiers are designed for high bandwidth in order to minimize the frequency dependence of the phase shift. The clock amplifier 2, for example, exhibits a power gain of 12.5 dB a 3 dB bandwidth of 550 MHz, and has a peak-to-peak output voltage of 2.4 V for a 1 dB gain compression. Such a high output voltage level allows short gating time intervals to be obtained in the demultiplexer by appropriately positioning the clock voltage dc level with respect to the gate threshold voltage. The clock amplifiers 1 and 2 were realized in hybrid integrated thin film technology. All other elements in the phase locked loop are commercially available microwave components.

A Schottky diode double balanced mixer is used as the phase detector since it provides a high bandwidth and a low offset voltage drift. The phase detector is suitable for RZ-PCM input signals. Preliminary nonlinear signal processing would be necessary for NRZ signals. The phase detector gain factor is proportional to the number of "1" bits per unit of time. A phase detector gain factor $K_d = 40$ mV/rad has been measured with a PCM input signal with a 200 mV pulse amplitude and equal probability of "0" and "1" bits. The power of the 1 GHz spectral line of this signal is -16 dBm.

Fig. 25 shows the basic circuit diagram of the active lead-lag type loop filter. The filter is characterized by its dc gain $A = R_3/R_1$ and by the two time constants $\tau_1 = R_1C$ and $\tau_2 = R_2C$. The VCXO gain measured with respect to the 1 GHz output of the frequency doubler cascade is 12.5×10^4 rad/Vs. Choosing $A = 2200$ yields a dc loop gain $K_v = K_0K_dA = 1.1 \times 10^7 s^{-1}$. Since the tuning range of the VCXO is limited to a maximum frequency deviation of $\Delta f_{max} = \pm 100$ kHz, the calculated maximum steady state phase error is [30]

$$\Theta_{v\,max} = \frac{2\pi\Delta f_{max}}{K_v} = \pm 5.7 \times 10^{-2} \text{ rad.} \tag{1}$$

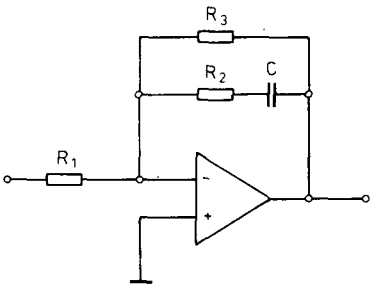

Fig. 25. Circuit diagram of the active lead-lag type loop filter.

The natural loop frequency ω_n and the damping factor ξ are given by

$$\omega_n = \sqrt{K_0K_d/\tau_1} \tag{2}$$

$$\xi = \omega_n\tau_2/2. \tag{3}$$

The damping factor was set to $\xi = 5$ since high gain second order phase-locked loops with high ξ values yield a low jitter accumulation in long repeater chains. The loop noise bandwidth

$$B_L = \frac{\omega_n}{2}\left(\xi + \frac{1}{4\xi}\right) \tag{4}$$

is then $B_L \doteq 2.5\ \omega_n$. For high gain second order PLLs Richman's formula [32] yields the pull-in range

$$\Delta f_P = \pm \frac{1}{\pi}\sqrt{\xi\omega_nK_v}. \tag{5}$$

For a pull-in range $\Delta f_P = \pm 100$ kHz, a natural frequency $\omega_n = 1.79 \times 10^3 s^{-1}$ corresponding to $B_L = 4.49$ kHz is obtained. The approximate formula for the time T_P required for the PLL to lock in is

$$T_P \doteq (2\pi\Delta f)^2/2\xi\omega_n{}^3 \tag{6}$$

for frequency deviations Δf equal to about half the pull-in range. For $\Delta f = 50$ kHz we find that $T_P = 1.71$ s. The hold-in range is given by

$$\Delta f_H = \pm K_v/2\pi. \tag{7}$$

The minimum dc loop gain for which the loop holds lock within $\Delta f_H = \pm 100$ kHz is $K_v = 6.28 \times 10^5 s^{-1}$. This dc loop gain necessary for hold-in is lower by a factor 5.71×10^{-2} relative to the dc loop gain for pull-in. Since K_v is proportional to the amplitude of the 1 GHz spectral line of the PCM signal, a -40.9 dBm 1 GHz spectral line in the PCM input signal is sufficient to hold the PLL locked. This corresponds to a mark probability of 1:35 in the PCM signal. We note that for this lower bit density the damping factor decreases to $\xi = 1.19$ yielding higher jitter accumulation in a repeater chain.

Fig. 26 shows the calculated and measured hold-in and acquisition range of the PLL as a function of the power of the

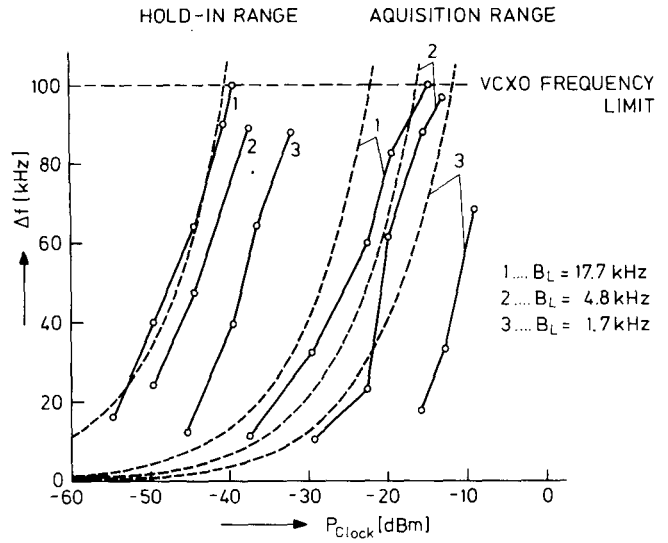

Fig. 26. Calculated (- - -) and measured (—) hold-in and acquisition range of the PLL.

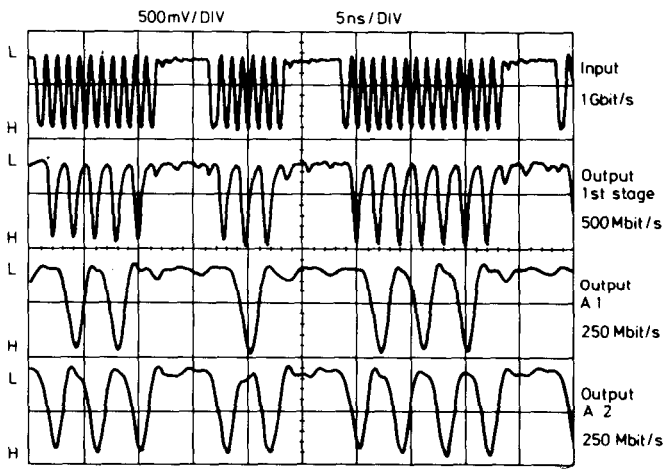

Fig. 27. Demultiplexer signal waveforms.

1 GHz spectral line of the data signal. The power of the 1 GHz spectral line is proportional to the number of "1"-bits per unit of time. For the measurements the spectral power level of the clock signal was set by the mark density of the PCM word and was measured with the microwave spectrometer. Contrary to the calculated behavior, the measured hold-in range decreases with decreasing loop bandwidth. A phase jitter of the input PCM signal is assumed to be the reason for this deviation.

Fig. 27 shows the measured demultiplexer signal waveforms. To achieve word synchronization during subsequent signal processing, the four demultiplexed PCM signals can be shifted from one output to the next by adding a short pulse to the filter output.

CONCLUSION

We have shown that the electronic components required for digital fiber optic transmitters and receivers can be realized with silicon bipolar transistors and silicon diodes for bit rates in the gigabits/s range. Circuit concepts with uncritical dependence on the active component parameters and on temperature were preferred. In many cases monolithic integration will be feasible if large circuit quantities are required.

The present state of bipolar transistor broadband amplifier development also makes front end design at gigabit/s rates feasible.

It is our opinion that in future fiber optic communication systems for bit rates up to 1 Gbit/s, bipolar transistors will dominate.

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