DEMULTIPLEXER USING FAST HYBRID INTEGRATED ECL-GATES FOR 1 GBIT/S PCM SIGNALS

Reinhard Petschacher and Peter Russer

ABSTRACT
This paper describes a demultiplexer combined with a clock regenerator for 1 Gbit/s PCM signals. The demultiplexer divides the incoming signal into four parallel 250 Mbit/s channels using fast hybrid integrated ECL-gates with rise time of less than 400 ps. All clock signals needed to drive these gates are extracted from the input signal by a phase locked loop using two frequency doubler stages between the local oscillator and the phase detector. Since the logic levels and supply voltages of the hybrid integrated ECL-gates are fully compatible with those of monolithic integrated ECL circuits, such ECL-circuits can be directly connected to the outputs of the demultiplexer.

INTRODUCTION

By using lasers as optical transmitters and glass fibres as the transmission medium, it will be possible in the future to transmit PCM information at bit rates of about 1 Gbit/s over distances of several kilometers [1,2]. In order to handle these high transmission rates, it has been necessary to develop suitable high-speed digital circuits. We have already developed a multiplexer [3] and several laser driver stages [4] capable of operating in the Gbit/s range, and in this paper we report the development of a demultiplexer and clock regenerator circuit for use in a receiver operating at 1 Gbit/s. The demultiplexer divides the incoming 1 Gbit/s signal into four 250 Mbit/s channels and is constructed with ECL-gates interconnected by coaxial transmission lines. It is advantageous to use such components in series-to-parallel converters operating at transmission rates of over 500 Mbit/s since very fast ECL-gates can be constructed in hybrid integrated technology, and the necessary delay lines can be simply constructed using the transmission lines. Series-to-parallel converters using similar components but different circuit configurations have already been described by Hanke [5].

In this work, all clock signals required to drive the demultiplexer are extracted from the input signal by a phase locked loop. The PLL system exhibits the advantages of very low dynamic and static phase error when compared with clock regeneration using a resonant circuit [6]. By using a VCXO in the high gain PLL it is possible to match the loop characteristics to the requirements of the transmission system over a wide range.

Dipl.-Ing. R. Petschacher, Dipl.-Ing, Dr. techn. Peter Russer
AEG-TELEFUNKEN, Forschungsinstitut
Elisabethenstraße 3
D-7900 Ulm, W.-Germany

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CIRCUIT OUTLINE

Fig. 1 shows the block diagram of the complete circuit. Fast hybrid integrated thin film ECL-OR gates are used in the demultiplexer. Since negative logic is applied, the gates provide logic AND output functions. In the first demultiplexer stage, the gates G_1 and G_2 are driven by two 500 MHz clock signals with opposite phases (C_1, $\overline{C}_1$) in order to split the input signal into two 500 Mbit/s bit streams. In a second stage they are further divided into four 250 Mbit/s channels by the second row of gates (G_3 to G_6). All clock signals are provided by the phase locked loop. The PLL local oscillator operates at 250 MHz while the clock and the input signal phases are compared at 1 GHz by a double balanced mixer. There is a chain of passiv frequency doublers and amplifiers between the local oscillator and the phase detector. Each of the clock amplifiers 1 and 2 consists of two differential amplifiers which are driven by a common input stage. One of these differential amplifiers generates the anti-phase clock signals, whilst the other drives the frequency doubler and provides a clock output for external signal processing. The clock outputs are connected to the gates by coaxial transmission lines the lengths of which are selected to ensure correct phasing of the clock and data signals at the gate inputs. In the first demultiplexer stage 50Ω transmission lines are used and the gate inputs are terminated with 50Ω resistors. The input resistance of the second row of gates (G_3 to G_6)is made 100Ω in order to allow the gate outputs of the first stage and the outputs of amp. 1 to drive two gate inputs in parallel. The output lines of both the front gates and the clock amplifier 1 are split into two 100Ω transmission lines in order to match the two stages. The output of G_1 is delayed compared with the output of G_2 by 1 ns to obtain equal phase of the two 500 Mbit/s data signals at the inputs of the second stage. The PLL is closed by feeding the phase detector output back to the VCXO through an active filter. Apart from the clock amplifiers 1 and 2 which are constructed in hybrid integrated thin film technology, and the active loop filter which is built up using an operational amplifier, all the components in the PLL are commercially available microwave parts.

THIN FILM COMPONENTS

The ECL-gates and the clock amplifiers 1 and 2 have been realized using thin film techniques with chip components on alumina substrates. The chips were mounted on the substrate with a conducting epoxy compound. Contact to the base and emitter of the transistors was made by thermal compression bonding. Through connections to the underside ground plane were formed by 0.45 mm ultrasonically drilled holes plugged with gold wire.

Fig. 2 shows the circuit of the ECL-OR gate. High speed switching transistors with a transit frequency of 8 GHz (T_1 to T_3) and 6 GHz (T_4) were used. Supply voltages of +2 V and -3,2 V were used so that the input and output transmission lines could be simply terminated to ground with 50Ω loads. Table 1 shows the electrical specifications. Supply voltages as well as logic levels are fully compatible with those of monlithic integrated ECL series. As mentioned

before, the input resistor is either 50Ω or 100Ω . Fig. 3 shows the switching characteristics of a gate with a 50Ω input resistance working into a 50Ω load. Switching times (10 to 90 percent) of T_R = 398 ps and T_F = 268 ps were measured.
The input stage of the clock amplifiers 1 and 2 is an emitter-follower which drives two parallel differential amplifiers. There are also emitter-followers at the outputs in order to achieve a low output inpedance. Using a linear circuit analysis program each amplifier gain was adjusted in order to obtain output power levels appropriate for optimum operation of the following frequency doubler and the demultiplexer gates. The amplifiers are designed as broadband components. Amp. 2 for example exhibits a power gain of 12.5 dB, for a 3 dB bandwith of 550 MHz and a 1 dB gain compression at an output voltage of 2.4 V_{ss}. The d. c. level of the demultiplexer clock signals is adjusted so that the gates are only opened by the negative half wave.

THE PHASE LOCKED LOOP

The phase locked loop is of the second order type and contains an active lag-lead filter. The loop parameters were evaluated after [7] for a d. c. phase detector gain of 40 mV/rad. This corresponds to the applied test signal whicb was a 128 bit pattern with equal numbers of "1" and "0" levels and a pulse amplitude of 200 mV. The spectral power of this signal at the 1 GHz clock frequency was -16 dBm. The d. c. loop gain is about $10^7/_s$ which yields a static phase error of less than 1 degree. Because the lag-lead filter has two independent time constants, the natural frequency and damping can be chosen independently. In order to obtain low jitter accumulation in a long chain of clock regeneration circuits, the damping constant was set to $\zeta = 5$ [6] . Hence the choice of the natural frequency determines the loop noise bandwith as well as the acquisition range. Fig. 4 shows the measured acquisition and hold in range plotted against the input spectral power of the 1 GHz clock frequency with the noise bandwidth as the parameter. The signal applied to the input of the phase detector was a 1 Gbit/s RZ bit pattern with a repetition rate of 3.9 MHz and a pulse amplitude of 200 mV. The tuning range of the VCXO limited the hold in and acquisition range to ± 100 KHz. The loop noise bandwith was therefore chosen to be 17.7 kHz so that the maximum acquisition range of ± 100 KHz was achieved at P_{Clock} = -16 dBm, which was the 1 GHz spectral power of the test signal as mentioned above. Once locked the PLL holds even when the spectral power decreases to -40 dBm.

DEMULTIPLEXER OPERATION

The complete circuit was tested by driving it with a 1 Gbit/s RZ signal from a 1 GHz pulse generator gated by a 250 Mbit/s PCM word generator. The oscillograms in Fig. 5 show the input signal, the 500 Mbit/s bit stream at the output of G_1 and the two subsequent 250 Mbit/s output signals at A_1 and A_2. To achieve word syncronization during further signal processing, the four demultiplexed PCM signals can be shifted from one output to the next by adding a pulse of 80 µs duration and 1 V amplitude to the PLL filter output. This forces the loop to skip one cycle so that the clock

frame is shifted against the input signal by 1 ns. Pulse shaping as well as RZ-NRZ conversion and other signal processing may be performed by monolithic integrated ECL-circuits which can be directly connected to the demultiplexer outputs.

SUMMARY
A demultiplexer for transmission rates of about 1 Gbit/s can be built up with high speed ECL-gates in a very simple circuit configuration when the various clock signals which are needed to drive the gates are directly available from the clock regenerator circuit. This is possible by the use of a PLL with twofold frequency doubling between local oscillator and phase detector. Beside the availability of all clock signals this PLL offers a further advantage since the local oscillator which operates at the lowest clock frequency can be a highly stable crystal oscillator. This allows the PLL to meet the requirements of the transmission system over a wide range.
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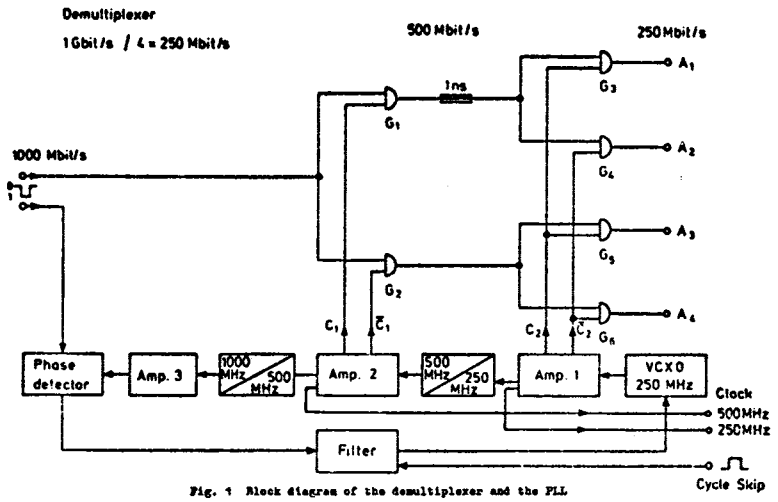

Fig. 1 Block diagram of the demultiplexer and the PLL

Fig. 1
Blockdiagram of demultiplexer and PLL

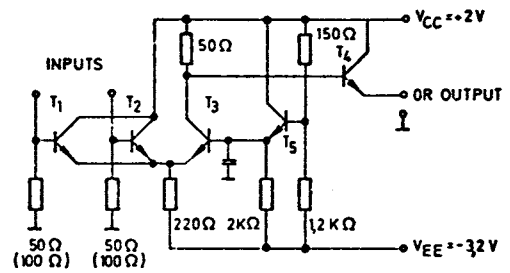

Fig. 2 Circuit of ECL-OR gate

Supply Voltage	+2V, -3.2V
Power Consumption	150 mW
Logic Levels: L	< 0.35V
H	> 1.05V
ΔV_{out}	> 0.7 V
$\Delta V_{in,min}$	0.6 V
T_R, T_F	< 400ps (R_i=50Ω)

Table 1 Electrical specifications of hybrid integrated ECL-OR gates

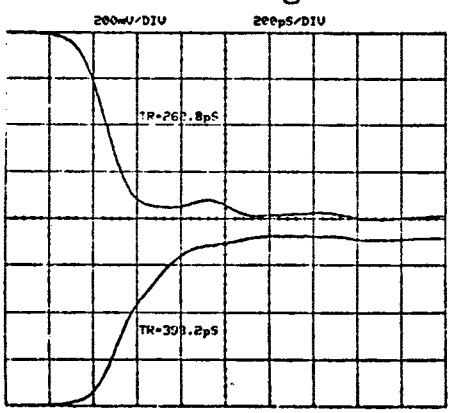

Fig. 3 Switching characteristic of ECL-OR gate

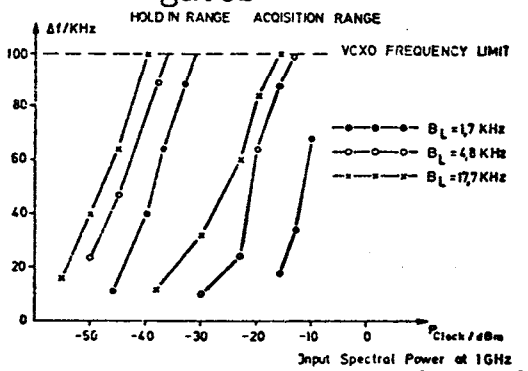

Fig. 4 Measured hold in and acquisition behaviour of the PLL

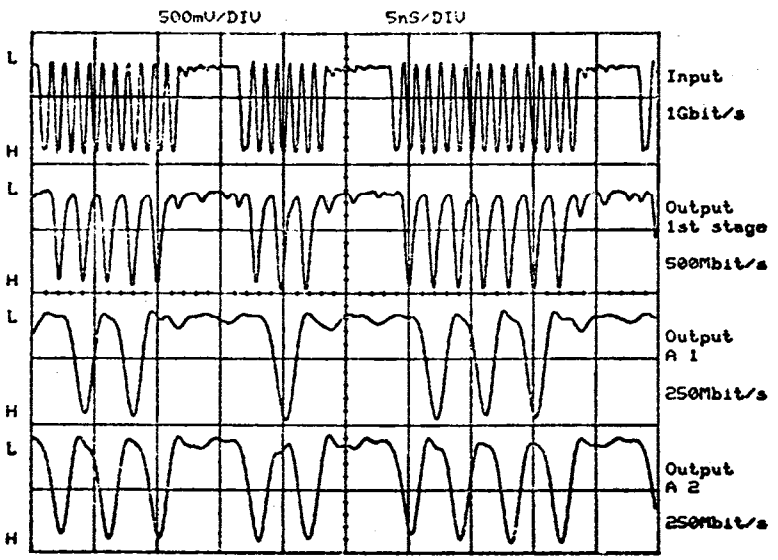

Fig. 5
Demultiplexer signal waveforms