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Fakultät für Elektrotechnik und Informationstechnik
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Design of a fully CMOS compatible Mechanical Stress Sensor

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Vollständiger Abdruck der von der Fakultät für Elektrotechnik und Informationstechnik der Technischen Universität München zur Erlangung des akademischen Grades eines

Doktor-Ingenieurs

genehmigten Dissertation.

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Prüfer der Dissertation:

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Die Dissertation wurde am 26.06.2020 bei der Technischen Universität München eingereicht und durch die Fakultät für Elektrotechnik und Informationstechnik am 08.02.2021 angenommen.

"If I have seen further than others,
it is by standing upon the shoulders of giants."

Isaac Newton

Abstract

This thesis summarizes research and development results of the cooperative project between Technical University of Munich and Texas Instruments Freising on the next generation sensors systems for evaluation of mechanical stress within integrated circuits (ICs) and beyond.

The project was motivated by an increasing need for inexpensive, highly integrated, yet accurate sensing systems that allow to measure mechanical force and stress for industrial automation (i.e. predictive maintenance), modern robotic systems, medical applications, and in general for reliability enhancement of ICs.

By addressing these needs, a novel sensing concept for separation of two stress components (in x- and y-direction) was developed. The concept for sensing elements utilizes n-well resistors, available in every standard CMOS process and is based on physical dependencies of the piezoresistive theory. Besides the stress sensing elements, the system also includes readout electronics with an integrated analog front-end and $\Delta\Sigma$ modulator to provide the measured signal in the digital domain.

The complete system was fabricated in Texas Instruments 130 nm standard CMOS technology with 7 distributed stress sensors per die to determine the two-dimensional impact of stress gradients over and even beyond the chip area. The system was optimized for small area and low power consumption with the readout electronics taking 1.07 x 0.43 mm^2 and consuming 357 μW (when active).

Due to a combination of analog and digital temperature compensation, the sensor system can operate in the widest stress range from -100 MPa to 360 MPa and achieves a resolution of 175 kPa. Also because undesired effects (like non-linearity, mismatch in stress sensitivity, etc.) are predominately tied to silicon material properties, the sensor system is rather stable over process variations during manufacturing and complex recalibration procedures should be unnecessary for volume production.

Summarizing, the system can compensate for large temperature drift, requires less area, and its significantly lower power consumption with advanced functionality enables a much wider field of applications.

Zusammenfassung

Diese Arbeit fasst die Forschungs- und Entwicklungsergebnisse des Kooperationsprojekts zwischen der Technischen Universität München und Texas Instruments Freising über die Sensorsysteme der nächsten Generation zur Bewertung mechanischer Beanspruchungen innerhalb von integrierten Schaltungen und darüber hinaus zusammen.

Das Projekt wurde durch den zunehmenden Bedarf an kostengünstigen, hoch integrierten, dennoch präzisen Sensoren für industrielle Automatisierung (d. h. vorausschauende Wartung), moderne Robotersysteme, medizinische Anwendungen und allgemein zur Verbesserung der Zuverlässigkeit von ICs, mit denen mechanische Kräfte und Spannung gemessen werden können.

Durch die Berücksichtigung dieser Bedürfnisse wurde ein neues Sensorkonzept zur Trennung zweier Spannungskomponenten (in x- und y-Richtung) entwickelt. Das Konzept verwendet n-Wannen-Widerstände, die in jedem CMOS-Standardprozess verfügbar sind und basiert sich auf physikalische Abhängigkeiten der piezoresistiven Theorie. Neben den Messelementen enthält das System auch Ausleseelektronik mit einem integrierten Analog Front-End und $\Delta\Sigma$-Modulator zur Bereitstellung des gemessenen Signals in digitaler Form.

Das komplette System wurde in einem 130-nm-CMOS-Standardprozess von Texas Instruments mit 7 verteilten Spannungssensoren pro Chip zur Bestimmung der zweidimensionalen Einflüsse von Spannungsgradienten im und sogar auerhalb des Chipbereichs hergestellt. Das System ist für kleine Flächen und geringen Energieverbrauch optimiert. Die Ausleseelektronik benötigt eine Fläche von 1,07 x 0,43 mm^2 und verbraucht 357 μW (wenn aktiv).

Aufgrund einer Kombination aus analoger und digitaler Temperaturkompensation kann das Sensorsystem im breitesten Stressbereich von -100 MPa bis 360 MPa betrieben werden und erreicht eine Auflösung von 175 kPa. Auch weil unerwünschte Effekte (wie Nichtlinearität, Unterschied in der Spannungsempfindlichkeit usw.) überwiegend an Siliziummaterial gebunden sind, ist das Sensorsystem über Prozessschwankungen während der Herstellung ziemlich stabil und komplexe Kalibrierungsverfahren sollen für die Volumenproduktion nicht erforderlich sein.

Zusammenfassend kann das System große Temperaturschankungen ausgleichen, benötigt weniger Fläche und deutlich geringerer Stromverbrauch mit der erweiterten Funktionalität ermöglicht ein viel breiteres Anwendungsfeld.

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Chapter 1

Introduction

In emerging applications such as health monitoring, industrial automation and modern robotics there is an increasing need for inexpensive, highly integrated, yet accurate mechanical stress sensing systems that can measure weight, deformation, and structural details of goods and equipment.

As in any other sensor system, the information in form of a physical quantity is extracted by suitable sensing elements and converted into analog or digital signals, dependent on the final application.

First strain sensitive elements were reported by William Thomson (Lord Kelvin) in 1856 [1]. In his experiment, the difference in resistances of copper and iron wires were measured by stretching them with a weight using a modified Wheatstone bridge. Later in 1932, the first directional dependent conductivity was presented by Mildred Allen's measurements of single crystals of bismuth, antimony, cadmium, zinc and tin under strain [2–5]. Based on her work, a tensor formulation for the general homogeneous mechanical stress on the electrical resistance of single crystals was developed by P. W. Bridgman [6, 7].

Leveraging the well-known benefits of CMOS (Complementary Metal Oxide Semiconductor) technology, namely the large-scale production of cost-efficient and feature-rich solutions, semiconductor based strain gauges were promising candidates for the next generation stress sensors. In 1954, Smith reported the first measurements of exceptionally high shear stress sensitivity (compared to metals) of silicon and germanium based sensing elements [8].

Nowadays, semiconductor based sensor systems are widely used in different aspects of our life. Especially, MEMS (Microelectromechanical Systems) have gained popularity in many applications as automotive (crash detection and stability control), biomedical (activity monitoring), consumer electronics (cameras lens stabilization, cellular phones), robotics (environment sensing), structural health monitoring, etc. [9].

To support the mentioned applications and also to make sensor systems more reliable over the whole time of operation, in this work, we present a fully-integrated CMOS

stress sensor that simultaneously exhibits wide dynamic range, low-power consumption, robust over-temperature performance (post-calibration), and resilience to process variation.

Moreover, the sensor system is designed to measure both magnitude and angle of mechanical stress. By combining these desirable features we are targeting two main applications: on-chip sensors for evaluation of mechanical stress and general purpose stress sensors for predictive maintenance (Industry 4.0) and other Internet of Things (IoT) use cases (like e.g. electronic skin).

1.1 On-Chip Stress Sensor for Evaluation of Mechanical Stress

Conventional microelectronic packages are assembled from three main components: silicon die, leadframe and mold compound that are shown in Fig. 1.1. Due to different coefficient of thermal expansion (CTE) of the components, the microelectronic packages generate large mechanical stress on the semiconductor chip [10–12]. This can be explained by the fact that the die with lowest CTE is attached to the leadframe and covered by mold compound with higher CTE at elevated temperatures. After cooling down to the room temperature, the package generates compressive stress on the top surface of the die. Another significant contribution can come from hygroscopic swelling of the mold compound [10–12], which can absorb ambient moisture and reduce the compressive stress.

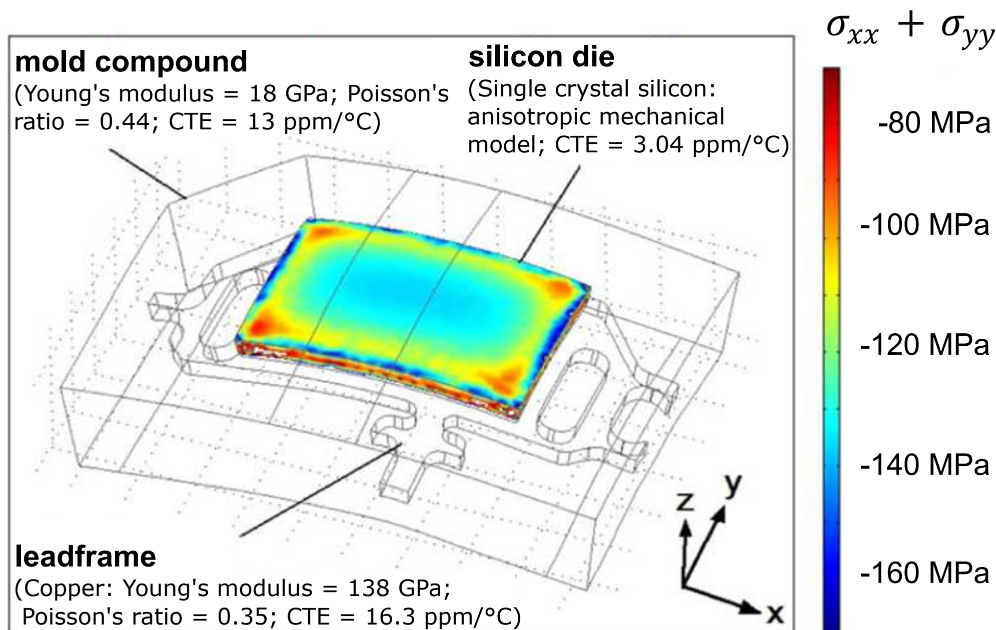

Figure 1.1: Components of a conventional microelectronic package: leadframe, mold compound, silicon die (all have different CTEs) (PG-SSO-4-1) [12].

The generated mechanical stress has an influence on properties of semiconductor devices and can be decisive for designing sensitive IC components. Especially system components that rely on absolute values of semiconductor devices (e.g. resistance, capacitance, base-emitter voltage, etc.) can be strongly affected by mechanical stress. A prime example of such system components is a bandgap voltage reference that can be found in almost any autonomous system.

The main idea of a conventional bandgap reference is a combination of two complementary signals with positive and negative temperature coefficients. The complementary to absolute temperature signal is usually generated from the base-emitter voltage of a bipolar transistor that depends on mechanical stress. This dependence can be a limitation for precision systems.

Another example for a device relying on absolute value of a semiconductor device is a RC oscillator, where both the resistance R and the capacitance C can depend on mechanical stress. Even devices, where the main parameters depend on ratio between the values (e.g. current mirrors, opamps) can have second order dependence on mechanical stress due to residual offset caused by mismatch.

Since conventional microelectronic packages have a laminar structure, the stress on the chip is dominated by two in-plane normal stress components σ_{xx} and σ_{yy}. Other stress components as shear stresses and out-of-plane normal stress σ_{zz} can appear at the perimeter and at the corners of the die. As an example, Fig. 1.2 illustrates the distributions of the sum of in-plane normal stresses $\sigma_{xx} + \sigma_{yy}$ and the in-plane stress shear stress τ_{xy} in a PG-SSO-4-1 package at 20° C.

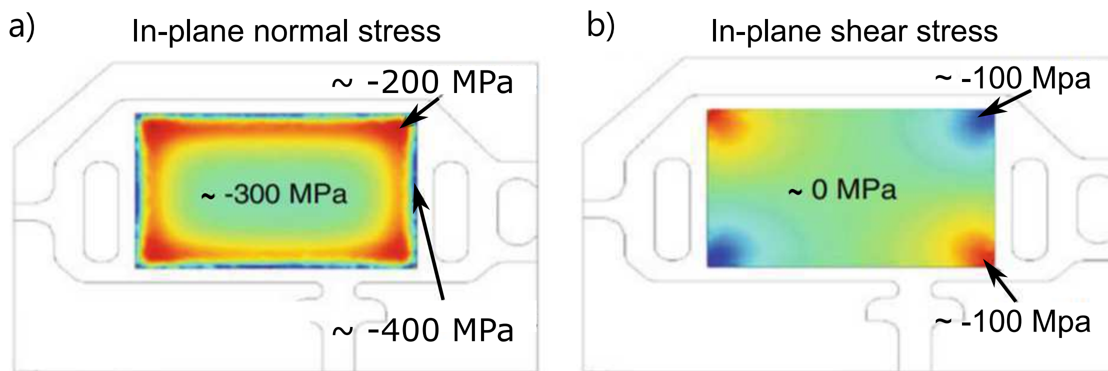

Figure 1.2: Typical stress pattern of a) In-plane normal stesses $\sigma_{xx} + \sigma_{yy}$ and b) In-plane shear stress τ_{xy} (PG-SSO-4-1) [11].

As can be seen, the sum of normal stresses in the center of the die is approximately -300 MPa that indicates that the stress in x- and y-directions is compressive. In contrast to in-plane normal stresses, the shear stress becomes more significant at the die corners. Therefore, the edges as well as the corners of a silicon die are typically avoided or even forbidden for sensitive analog circuits (e.g. for bandgap voltage references). Consequently, the shear stress can mostly be neglected in practical considerations. Hence, for evaluation of mechanical stress in packages, the stress sensor should be able to measure the stress components in x- and y-direction separately.

Conventional CMOS implementations typically utilize piezo-transducer rosettes and achieve directional response by combining n- and p-type diffusion resistors or MOSFETs [13, 14]. However, mismatch of these complementary devices, particularly over temperature, results in limited stress measurement accuracy and other forms of errors that are difficult to compensate via simple calibration.

In the solution proposed here, all primary sensing elements are implemented using n-well resistors whose behaviors track process and temperature variations. Thus, simple analog and digital compensation techniques can be applied to correct for undesired parameter variation over temperature. The inclusion of auxiliary p-type elements then allows for independent extraction of stress angle quadrant information without limiting the accuracy of the system. A prototype of the integrated stress sensor and corresponding interface circuits consisting of on-chip references, AFE, $\Sigma\Delta$ Modulator, etc., has been realized in a standard 130 nm CMOS technology with no sensor specific process modifications.

1.2 Prototype for Industry 4.0 Applications

The sensor system developed in this work can also be used for other applications: the sensor can be attached to a target surface for evaluation of mechanical stress, bending moment and deflection of that surface.

As an example, the sensor can be attached to the rotor of a wind power mill to capture associated forces in both magnitude and angle for estimation of a material fatigue to undertake the necessary measures in advance (predictive maintenance).

Such systems are particularly relevant for Industry 4.0 with a high level of technological process automation, where predictive maintenance can ensure a continuous production flow. The information of the sensor system (e.g. attached to an engine) can be periodically analyzed to determine the next necessary maintenance time.

A prototype of the sensor system is shown in Fig. 1.3, comprising a flexible PCB, the test chip itself, a microcontroller, and other components for power-management.

Die-on-board (or chip-on-board) assembly was used such that the sensor is mechanically coupled to the PCB: the entire system can then be further attached onto a secondary target surface to measure that surface's stress via deformation of the flexible board.

Also shown in the photo are a battery holder for self-sufficient operation and a near-field communication (NFC) antenna embedded into the outer perimeter of the PCB (for transfer of aggregated data). Alternatively, the system offers an I^2C interface for direct bus communication between multiple distributed sensors arranged in an array for the measurement and extrapolation of mechanical forces over a larger sensing area.

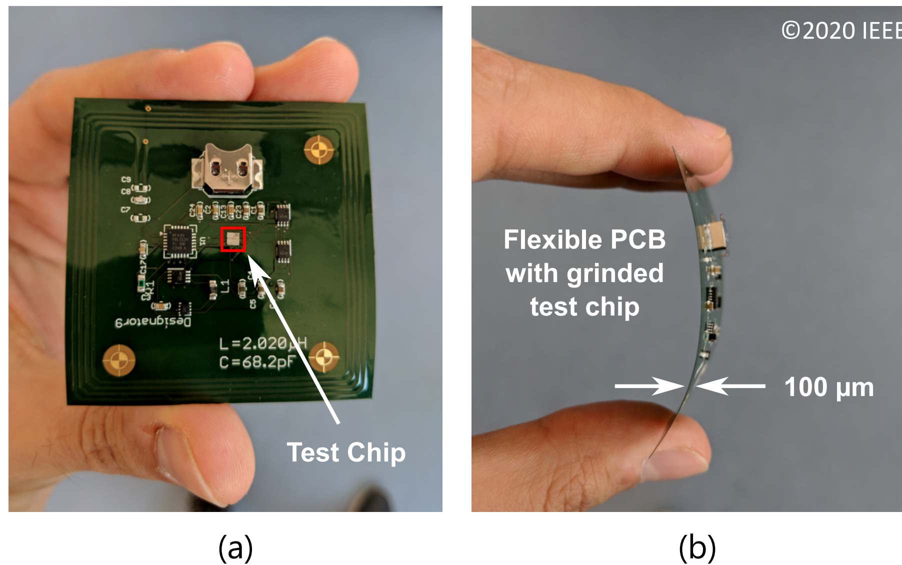

Figure 1.3: Application example of mechanical stress sensor on a flexible PCB: (a) top view of NFC based system and (b) section view with grinded test chip.

1.3 Thesis's Organization

This thesis gives a detailed overview on the challenges and solutions during the development of the sensor system. A theoretical background needed for understanding the concepts behind the piezoresistive sensing elements is provided in Chapter 2. It should help the reader to understand the relationships between mechanical stress, strain and pressure and also give an insight into the stress effect in crystalline silicon by introducing the Miller indices and the piezoresistive effect.

The sensing elements and later the whole system, in this work, are tested by custom built measurement setups. Cantilever-based and four-point bending techniques were used therefor. The development of the measurement setups are presented in Chapter 3: first a mathematical model is introduced and later a 3D CAD Model is shown that was used for fabrication of the setups. At the end an error analysis is performed to estimate the overall accuracy of the both setups.

The main novelty of this work is the design of new types of sensing elements that can measure mechanical stress components in two separate dimensions (e.g. x- and y-direction). The development of the new stress sensing concepts and implementation of primary and auxiliary elements are presented in Chapter 4. The Chapter also includes the theory behind the reference element and how its temperature behavior can be optimized in a standard CMOS technology without process modifications.

The readout electronics were designed under consideration of unique specifications for the new sensing elements. The system was optimized for low power consumption and small area applications. Chapter 5 gives a detailed overview of the designed AFE and the on-chip temperature sensor with corresponding multiplexers. The reader can also find arguments for selection of a proper ADC and reference for the

sensor system. Also, there is information on how the individual component were integrated into the sensor system.

A test chip with the sensing elements and readout electronics was fabricated in a standard 130 nm CMOS technology. This chip was used for testing, evaluation, and validation of noise, stress sensing performance, and evaluation of temperature dependence of measured signals in the digital domain. The measurement results with compensation for non-ideal behavior of the signals can be found in Chapter 6. Finally, a conclusion with a short outlook is given in Chapter 7.

Chapter 2

Theory

This chapter gives an overview on physical quantities (stress, pressure and strain) that are relevant for further discussions in this work. Since the sensor system is designed in a silicon based standard CMOS technology, the effect of mechanical stress in crystalline silicon (especially the piezoresistive theory) is described.

2.1 Mechanical Stress

Mechanical stress is defined as a force per unit area on the surface of a differential cube and is measured in units of pascals (Pa). Since the stress across any surface depends on the orientation of that surface, the stress cannot be described by a single vector. The Cauchy Stress Tensor σ is normally used to represent the stress state with a 3 x 3 matrix with nine components

$$\sigma = \begin{pmatrix} \sigma_{xx} & \tau_{xy} & \tau_{xz} \\ \tau_{yx} & \sigma_{yy} & \tau_{yz} \\ \tau_{zx} & \tau_{zy} & \sigma_{zz} \end{pmatrix}$$

As shown in Fig. 2.1, the components can be divided in three normal stresses σ_{xx}, σ_{yy}, σ_{zz}, where the force acts perpendicular to the surface and six shear stresses τ_{xy}, τ_{xz}, τ_{yz}, τ_{yx}, τ_{zx}, τ_{zy} with forces along the face areas. The indices of two elements indicate the direction of the force and the orientation of the surface. Because of static equilibrium requirements, the stress tensor is always symmetric: $\tau_{xy} = \tau_{yx}$, $\tau_{xz} = \tau_{zx}$, $\tau_{yz} = \tau_{zy}$ and therefore contains only six independent components [15].

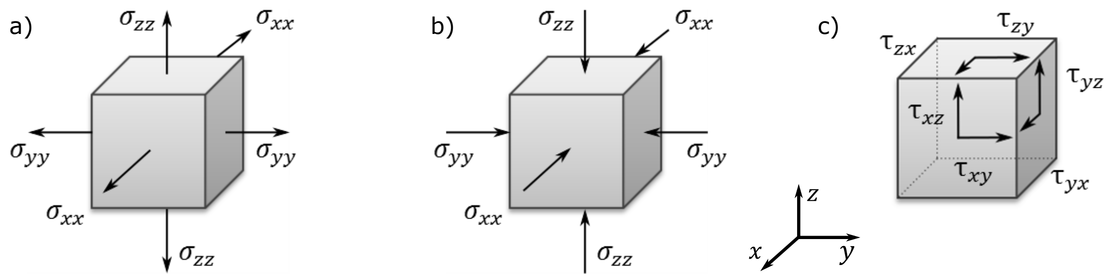

Figure 2.1: Types of mechanical stress: a) Tensile normal stress b) Compressive normal stress c) Shear stress.

2.2 Pressure

Pressure, in contrast to stress, is a scalar quantity expressing the force applied perpendicular to the surface of a differential cube. In general, pressure is a positive quantity and measured in the same units as stress, namely Pa. In other words, pressure can be considered as a special (simplified) case of mechanical stress.

2.3 Strain

Strain is a dimensionless quantity that describes the state of deformation in a solid body. Similarly to the stress, the strain state ε is given by a symmetric 3 x 3 tensor

$$\varepsilon = \begin{pmatrix} \varepsilon_{xx} & \varepsilon_{xy} & \varepsilon_{xz} \\ \varepsilon_{yx} & \varepsilon_{yy} & \varepsilon_{yz} \\ \varepsilon_{zx} & \varepsilon_{zy} & \varepsilon_{zz} \end{pmatrix},$$

where the normal strains ε_{xx}, ε_{yy}, ε_{zz} are defined as the ratio of total deformation to the initial dimension of the body in the direction of consideration (x, y or z). The shear strains ε_{xy}, ε_{xz}, ε_{yz}, etc. represent the tangent caused by the change of angle undergoing a deformation. Fig. 2.2 shows a 2D-section of the differential cube under normal and shear strains.

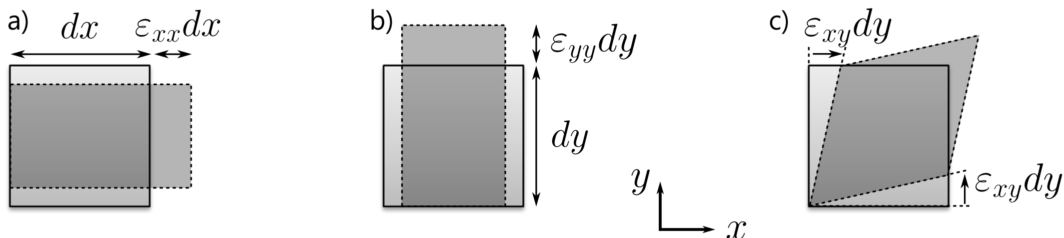

Figure 2.2: Types of mechanical strain: a) Normal strain in x-direction b) Normal strain in y-direction c) Shear strain.

The relation between strain and stress can be expressed by Hooke's law, provided that the stress is below the elastic limit (max. stress or force before the onset of permanent deformation). In this case, the stress tensor has the linear dependence on the strain tensor

$$\sigma = C\varepsilon, \tag{2.1}$$

where C represents a fourth-order elasticity tensor. Similarly, the dependence between strain and stress can be give by

$$\varepsilon = S\sigma, \tag{2.2}$$

with S representing the compliances. Summarized we say that the stress is caused by internal forces in a solid body and the strain, in turn, is the result of the stress.

2.4 Stress effect in crystalline silicon

Mechanical stress alters the band structure of silicon by deforming the crystal structure and changing the atomic distances. This leads to a mobility change of charge carriers (electrons and holes). Also stress sensitivity of semiconductor devices can strongly depend on their orientation to crystal axes. This fact can be explained by bandgap energy models with charge carriers mobility in crystalline silicon under stress [16]. To specify different directions in crystalline structures, the Miller indices are used, as shown in Fig. 2.3. The direction index in square brackets denotes a vector normal to a plane, the plane itself is described by the index in round brackets. The crystallographic direction can be determined or set during the fabrication of silicon wafers. Since a (001) surface wafer has several advantages over other wafer planes in terms of defects in later IC production, the (001) silicon surface is most used in the industry [17].

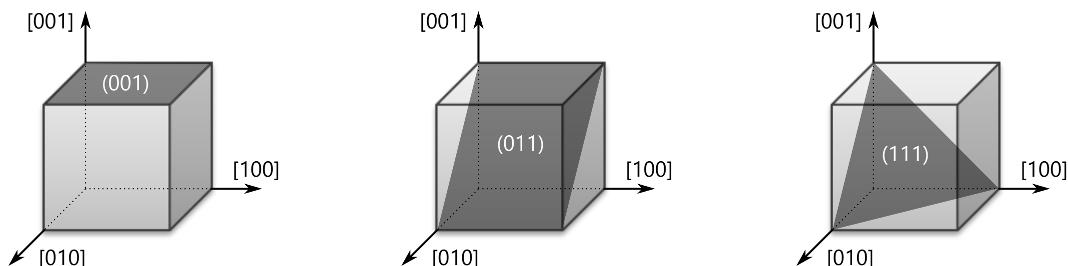

Figure 2.3: Miller indices and commonly employed silicon crystal planes.

Fig. 2.4 shows the main crystal axes of an (001) p-type wafer. Depending on the wafer processing technology, the orientation of a silicon die and thereby the orientation of IC devices are aligned along one of the main crystal axes. For the design of the stress sensor in this work, the silicon wafer with the notch (used for visual indication of the wafer orientation) oriented along the direction [110] is used.

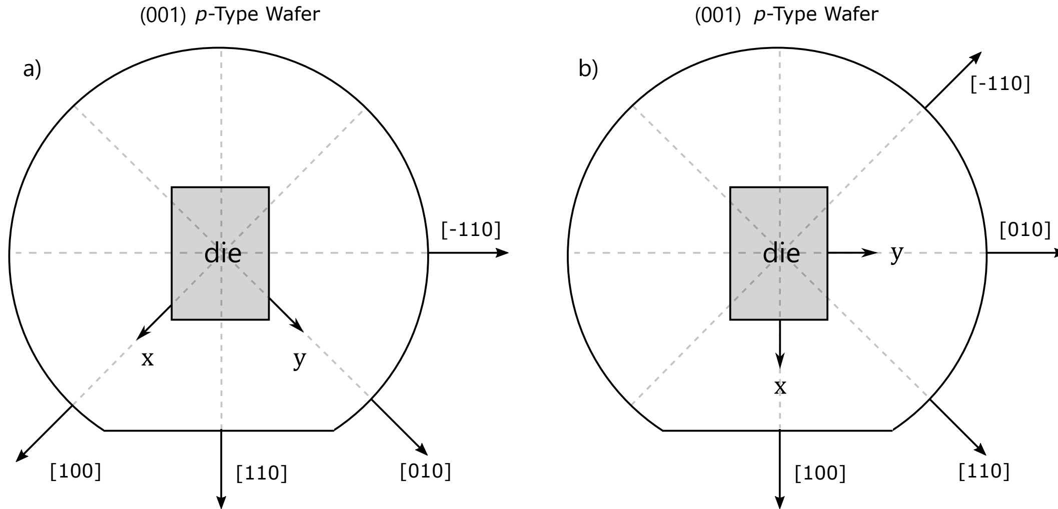

Figure 2.4: Miller indices and defined coordinate system on a (100)-silicon wafer with the notch oriented along a) the direction [110] and b) the direction [100].

2.5 Piezoresistive effect

The resistance of a regular material with the length L, width W, and thickness t can be expressed as

$$R = \frac{\rho}{t}\frac{L}{W}, \tag{2.3}$$

where ρ is the resistivity that for a semiconductor material can be estimated as

$$\rho = \frac{1}{qn\mu}, \tag{2.4}$$

with the elementary charge q, the charge density n, and the mobility μ. Since the mobility of electrons and holes in a silicon device has anisotropic (directionally dependent) response to the stress, the overall resistance change also depends on the stress orientation and consequently, the alignment of the device relative to the main crystal axes.

The sensitivity of a silicon resistor to the stress is represented by piezoresistive coefficients $(\pi_{11}, \pi_{12}, \pi_{44})$ and can be determined with the test configuration proposed by C. S. Smith [8]. As shown in Fig. 2.5, two configurations are required to specify the longitudinal π_{11} and transverse π_{12} piezoresistive coefficients of a device under test (DUT) to the stress along [100] and additional two configuration for π_{44} along [110] direction. Similarly, the coefficients for MOSFETs (piezo-MOS effect), as well as for bipolar devices (piezojunction effect) can be determined using the same test configuration.

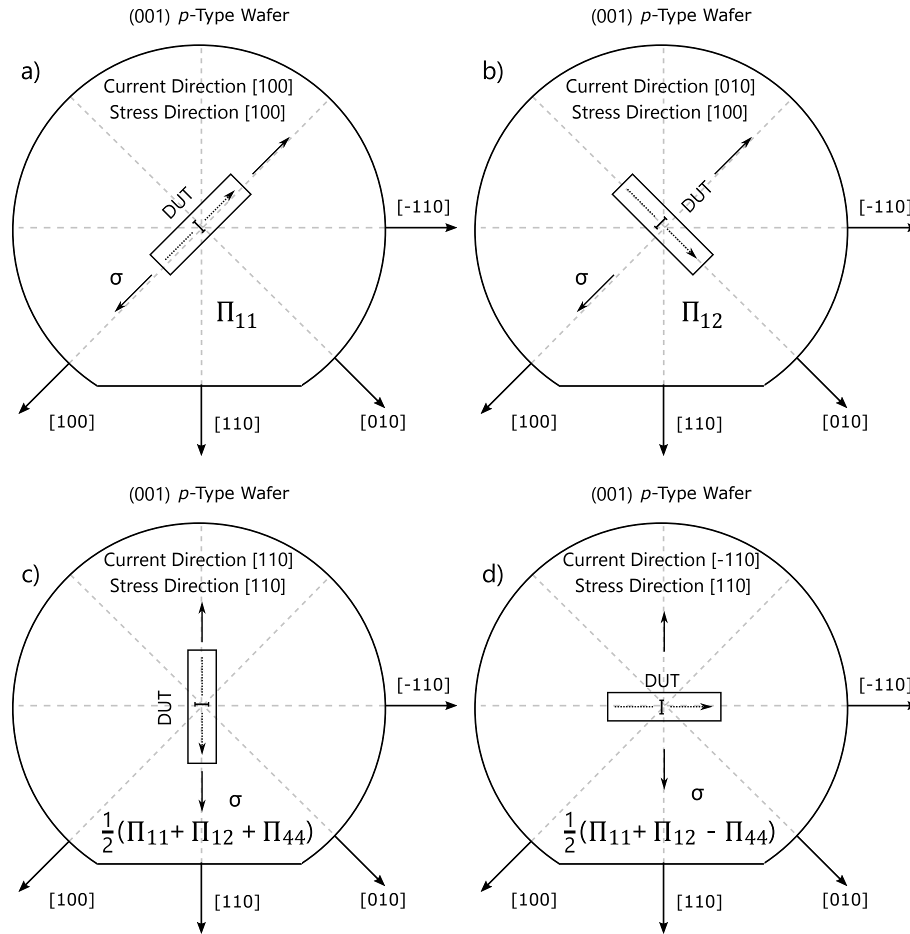

Figure 2.5: Smith's test configuration for determination of piezoresistive coefficients for DUTs oriented along the main crystal axes. Arrangements a) and c) are also defined as longitudinal and b) and d) transverse to the stress direction.

The relation between mechanical stress and resistivity of silicon in a crystallographic coordinate system, with ρ_0 being a nominal resistivity, is given as [18]

$$\begin{pmatrix} \rho_{[100],[100]} \\ \rho_{[010],[010]} \\ \rho_{[001],[001]} \\ \rho_{[100],[010]} \\ \rho_{[100],[001]} \\ \rho_{[010],[001]} \end{pmatrix} = \begin{pmatrix} \rho_0 \\ \rho_0 \\ \rho_0 \\ 0 \\ 0 \\ 0 \end{pmatrix} + \rho_0 \begin{pmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{pmatrix} \cdot \begin{pmatrix} \sigma_{[100],[100]} \\ \sigma_{[010],[010]} \\ \sigma_{[001],[001]} \\ \sigma_{[100],[010]} \\ \sigma_{[100],[001]} \\ \sigma_{[010],[001]} \end{pmatrix} \quad (2.5)$$

The notation in the crystallographic coordinate system is useful for cases in which the device and mechanical stress are oriented along the main crystal axes. For the 2D case, where the device and mechanical stress are oriented in an arbitrary direction, the coordinate transformation by Euler's angles can be used [15].

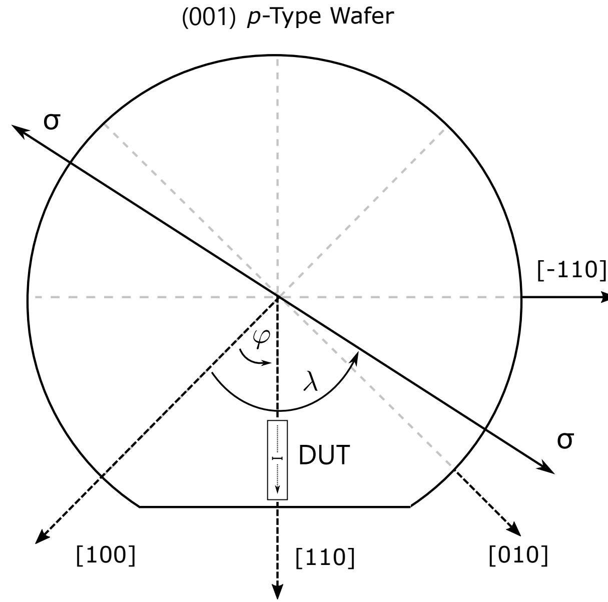

Figure 2.6: Angles between alignment of a resistor and orientation of an uniaxial stress σ relative to [100] direction on a (001) p-Type Wafer.

Thus, the relation between the uniaxial stress and the silicon resistance can be expressed as [15]

$$\frac{\Delta\rho}{\rho} = \frac{\rho - \rho_0}{\rho_0} = \Bigg[\pi_{11}(\frac{1}{2} + \frac{1}{2}\cos(2\varphi)\cos(2\lambda)) + \pi_{12}(\frac{1}{2} - \frac{1}{2}\cos(2\varphi)\cos(2\lambda)) + \pi_{44}(\frac{1}{2}\sin(2\varphi)sin(2\lambda))\Bigg]\sigma, \tag{2.6}$$

where φ and λ are the angle between a silicon resistor and the orientation of an uniaxial stress, relative to [100] crystal direction, respectively. The alignments of the silicon resistor and the uniaxial stress are illustrated in Fig. 2.6.

Assuming that $\lambda = 0$ (stress is oriented along [100] direction), the matrix coefficient from equation 2.5 can be give as [18]

$$\Pi_{ij} = \begin{pmatrix} \pi_{11} - \frac{1}{2}\pi_0\sin^2(2\varphi) & \pi_{12} & \pi_{12} & 0 & 0 & -\frac{1}{2}\pi_0\sin(4\varphi) \\ \pi_{11} + \frac{1}{2}\pi_0\sin^2(2\varphi) & \pi_{11} & \pi_{12} & 0 & 0 & \frac{1}{2}\pi_0\sin(4\varphi) \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ -\frac{1}{4}\pi_0\sin(4\varphi) & \frac{1}{2}\pi_0\sin(4\varphi) & 0 & 0 & 0 & \pi_{44} + \pi_0\sin^2(2\varphi) \end{pmatrix}, \tag{2.7}$$

were

$$\pi_0 = \pi_{11} - \pi_{12} - \pi_{44}. \tag{2.8}$$

The response of both n- and p-type resistors to mechanical stress at constant stress value of 100 MPa and different stress angles are shown in Fig. 2.7 and Fig. 2.8, respectively.

It can be seen that the highest stress sensitivity for n-type resistors can be achieved for [100] and [010] oriented devices. The p-type resistors exhibit the highest stress sensitivity for [110] and [-110] orientations.

Table 2.1 shows the stress sensitivity of silicon devices available in a standard CMOS technology. The values of the devices were found in literature [9,19,20] and give first order piezoresistive coefficients of n- and p-type resistors, lateral bipolar transistors, and MOSFETs.

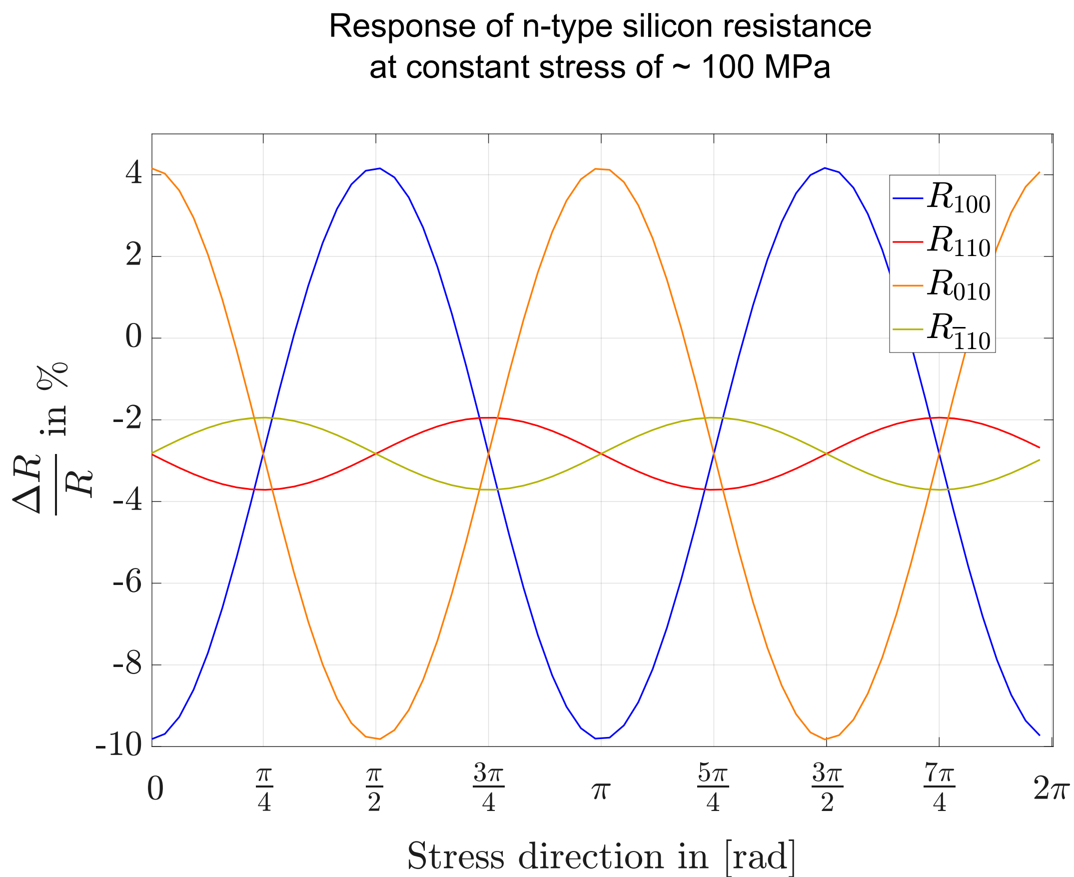

Figure 2.7: Response of n-type resistors oriented in [100], [110], [010], [-110] at constant stress of 100 MPa and different stress angles from 0 to 2π.

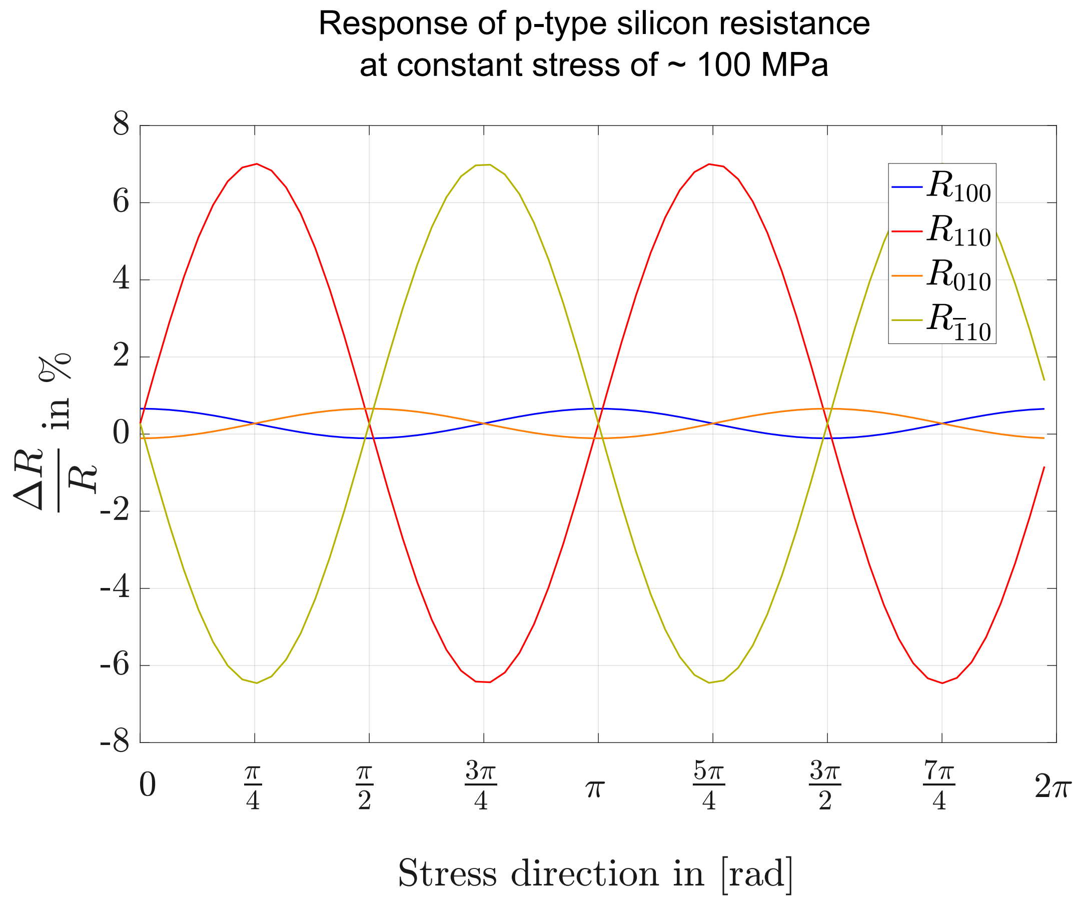

Figure 2.8: Response of p-type resistors oriented in [100], [110], [010], [-110] at constant stress of 100 MPa and different stress angles from 0 to 2π.

Table 2.1: Stress sensitivity of devices in standard CMOS technologies.

Stress Sensitivity (% / 100MPa)					
Stress & Device Current Orientation	Resistor		Bipolar Transistor	CMOS Transistor	
	N-Type	P-Type	Lateral pnp transistor	N-Type	P-Type
Stress along <100> Current along <100> (Π_{11})	-10.2	0.66	1.16	-4.7	-1.5
Stress along <100> Current along <010> (Π_{12})	5.34	-0.11	1.16	-2.2	0.9
Stress along <110> Current along <110> $\frac{1}{2}(\Pi_{11} + \Pi_{12} + \Pi_{44})$	-3.16	7.18	6.47	-3.2	7.1
Stress along <110> Current along <-110> $\frac{1}{2}(\Pi_{11} + \Pi_{12} - \Pi_{44})$	-1.76	-6.63	-3.88	-1.5	-3.2

Chapter 3

Experimental Setups

In order to qualify a stress measurement system, a mechanical setup is needed to impose a known and defined stress onto the chip. Beside applying well defined stress values, there is an additional requirement for the measurement setup of this project, namely: the stress values should be applied at different stress angles. There are various existing options to bend a piece of silicon, e.g. cantilever beam bending, three-point bending, and four-point bending [21, 22].

The measurement setup shown in [15] utilizes the cantilever beam bending that allows to apply stress values through a micrometer screw, controlled by a stepper motor. Therefore, the setup can be partially automated for applying different stress values and for measurements over temperature. However, to be able to apply mechanical stress at different angels, the silicon wafer has to be sawn at a certain direction or angle relative to its notch. It means that for every new stress direction, an additional silicon beam is needed. Another disadvantage of the setup is that for measurements over temperature, the coefficients of thermal expansion (CTE) of mechanical apparatus (e.g. micrometer screw) should be low or at least known to determine the error caused by temperature changes.

Another widely-used bending technique is four-point bending that was implemented in [23–26] and in many other related works. The mechanical stress is applied by using inner and output supports, where the device under test (DUT) is located between the inner supports. In contrast to the cantilever technique, mechanical stress between the inner supports is equally distributed (same stress values). This allows to simultaneously measure and characterize multiple DUTs at the same stress values, without considering displacement of the individual DUTs. This effects will be discussed in more detail in the following sections.

The measurement setup in [23, 24] is based on bending of silicon beams (similar to cantilever technique) and would require multiple beams for applying mechanical stress in different directions. However, in context of [23, 24], this was not necessary for the evaluation of the test chip, due to specific application for measuring of shear and normal stress in x-direction only (orthodontic brackets).

In [22,25], the stress is applied directly to a silicon wafer, which is attached between inner and outer supports. Thus, the setup allows to align the wafer in a desired direction and apply stress values without sawing the wafer. Also, the whole wafer (all DUTs) can be characterized at once, which makes it suitable for high volume stress measurements. The drawback of the setup is the non-uniform distribution of the stress values along the inner supports due to the round shape of the wafer. This leads to lower accuracy measurements (compared to the cantilever technique) if the stress gradients are not considered.

In our project the cantilever and the four-point bending techniques were used to first of all characterize already existing devices in a 130 nm technology, later on the designed sensing and reference elements and finally the complete stress sensor system with all the required system components. The cantilever technique is used for measurements, where higher stress magnitude values are required (e.g. for extraction of piezoresistive coefficients) and the four-point bending for characterization of the sensor system at stress angels with higher granularity but lower magnitude accuracy.

In this chapter, we will describe the main considerations in the design and implementation of the measurement setups for applying well-defined stress values at certain angles.

3.1 Measurement Setup for Applying Uniaxial Mechanical Stress

For characterization of silicon devices and proof of the proposed concept, an accurate mechanical apparatus for applying well-defined values of the mechanical stress is needed. Moreover, to extract the piezoresistive coefficients (Π_{11}, Π_{12} and Π_{44}), the mechanical stress needs to be applied in the main four crystallographic directions ([100], [010], [110], [-110]). Once the piezoresistive coefficients are measured, the response of semiconductor devices to any stress angles can be calculated by using equation 2.6. To perform the measurements with the mentioned specifications, the cantilever technique is used, shown in Fig 3.1.

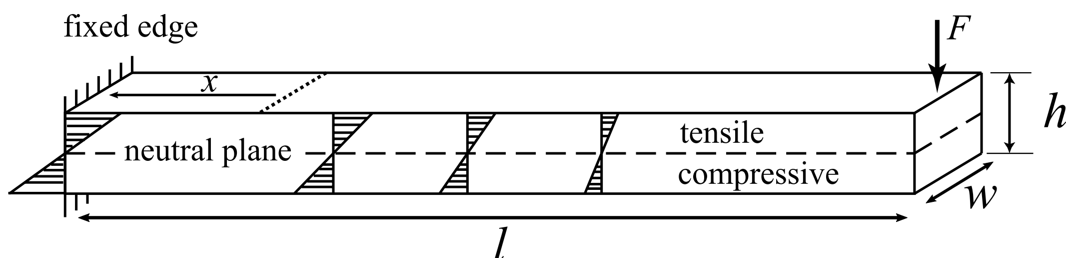

Figure 3.1: Cantilever Technique for applying well defined stress values [27].

For this method, a fixed cantilever beam made of a single-crystal silicon is bend by applying a defined force at the free end. If the applied force F and the beam length

l, width w and thickness h are known, the stress at a distance x from the fixed edge can be calculated as [27]

$$\sigma = \frac{6 \cdot F}{w \cdot h^2}(l - x) \tag{3.1}$$

Depending on the location of the test chip regarding the neutral plane of the beam, the stress can be tensile or compressive. The force F can be generated by placing weights with mass m on the free end of the beam

$$F = m \cdot g, \tag{3.2}$$

where g is the gravitational acceleration of earth. In contrast to [15], the concept of our measurement setup relies on generation of mechanical stress by applying weights and has an advantage of measurement results being stable over temperature. Thus, the generated stress, as can be seen from equation 3.1, only depends on the geometrical dimension of the silicon beam and the applied force.

The dimensions of the beam can be well controlled by modern silicon wafer processing machines or can be measured afterwards (for every silicon beam). The drawback of our setup is the complexity of automation (i.e. different weights should be applied automatically).

Silicon beams with desired dimensions can be sawn directly from wafers. After that the thickness of the processed beams is measured. It can be seen from equation 3.1 that accurate measurements are needed, since the stress depends quadratically on the thickness of the beam. In order be able to apply the stress along the main crystal axes, wafer pieces containing the test chip need to be sawn in four different directions, as shown in Fig. 3.2.

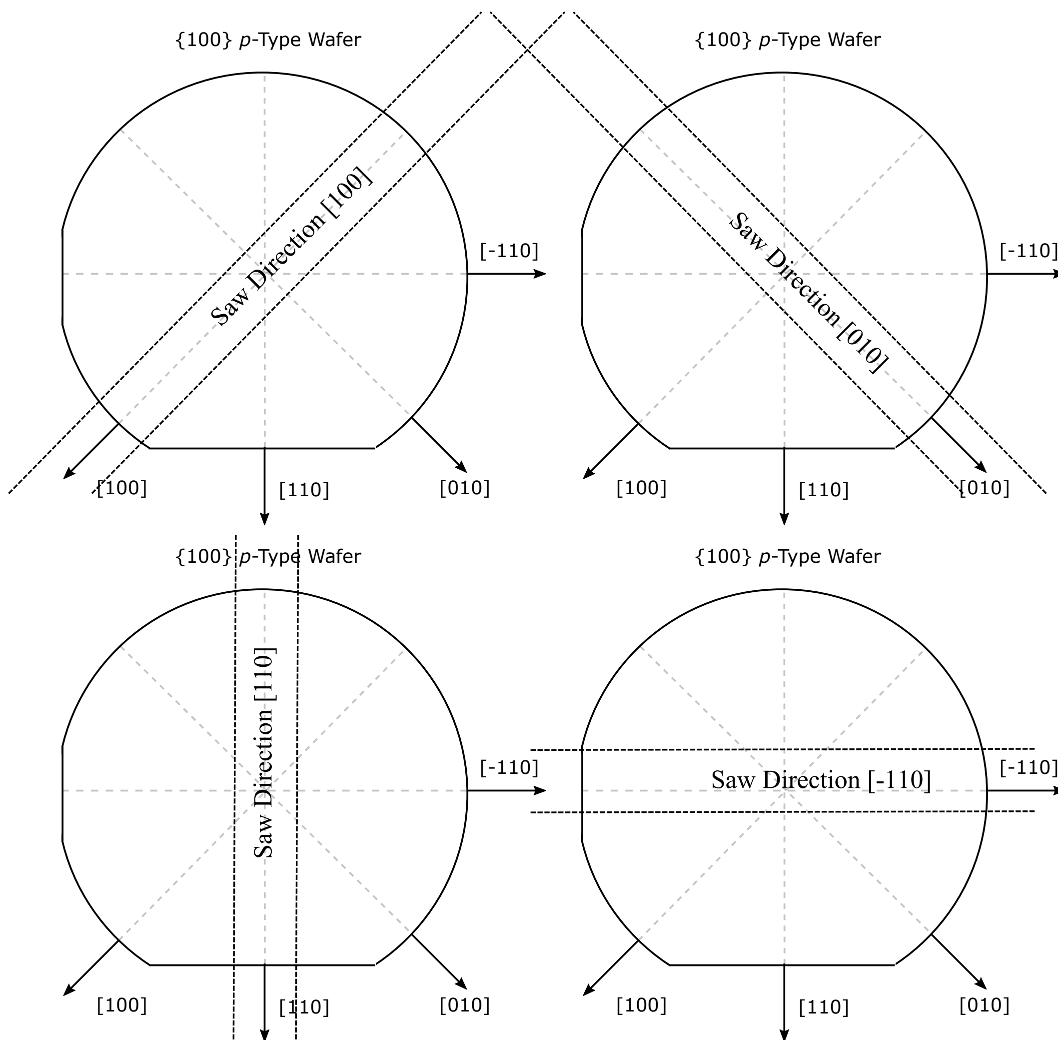

Figure 3.2: Saw directions along the main crystal axes [100], [010], [110] and [-110] for extraction of the piezoresistive coefficients.

Implementation of Measurement Setup

As a first approach to determine physical dimensions required for the measurement setup, a 3D CAD Model of a mechanical apparatus was developed. The setup should fit into conventional temperature chambers, so that it can be used for stress and temperature measurements. The concept shown in Fig. 3.3 presupposes that a test chip on the silicon beam has a wire-bondable surface.

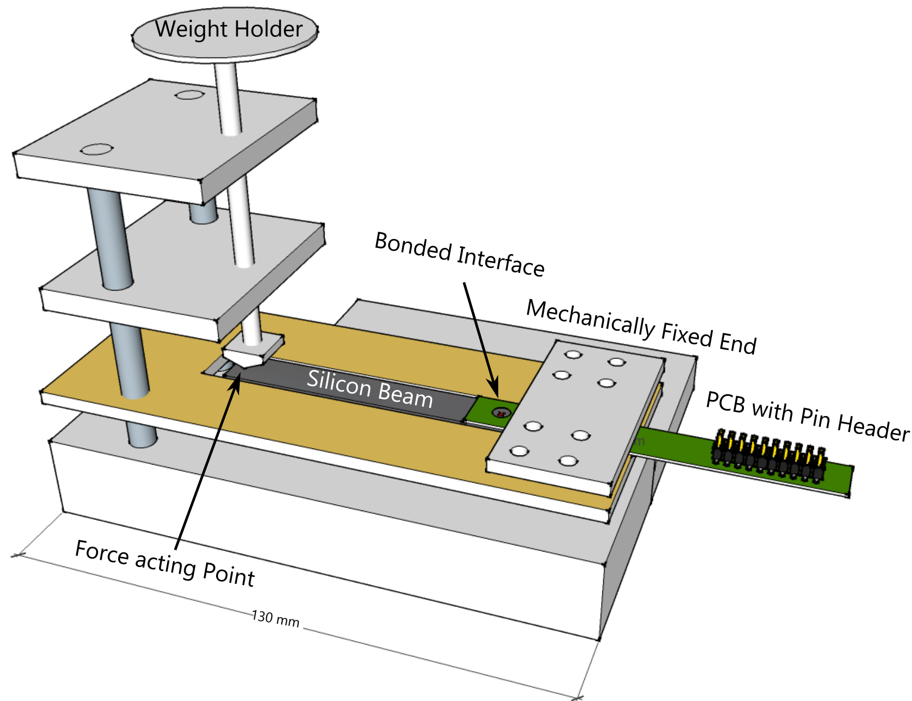

Figure 3.3: 3D Model of the mechanical apparatus for applying well-defined stress values.

The beams are obtained by sawing the silicon wafer in 10 cm by 1 cm strips with an accuracy of ± 50 μm. These dimensions were selected to reduce the relative error caused by sawing tolerances. To further increase the accuracy of the sawn silicon beams, every test chip has a cross-indicator (see Fig. 3.4) that is used as a coordinate origin during the sawing process.

The interface between the test chip on the beam and measurement equipment is established by wire bonding on a printed circuit board (PCB). For this purpose a test chip with an area of 2x2 mm^2 and with 60 available bondpads was designed. This allows to measure multiple devices on a single test chip. However, it was not possible to bond all pads at once (due to geometry issues). Therefore, the test chip was divided into three columns with 20 pads for bonding. Every column is bonded to a single PCB and requires a separate silicon beam.

A die-attach glue was used to keep the beam and the PCB together during wire bonding. It is important to mention that the PCB is glued only at the beam edge,

where it will be mechanically fixed in any case and does not contribute to the stress distribution along the silicon beam.

Fig. 3.5 shows the configuration that allows the PCB to stay undeflected during stress measurements. Otherwise the PCB will affect the overall stress distribution along the beam and cause unexpected deviation from equation 3.1.

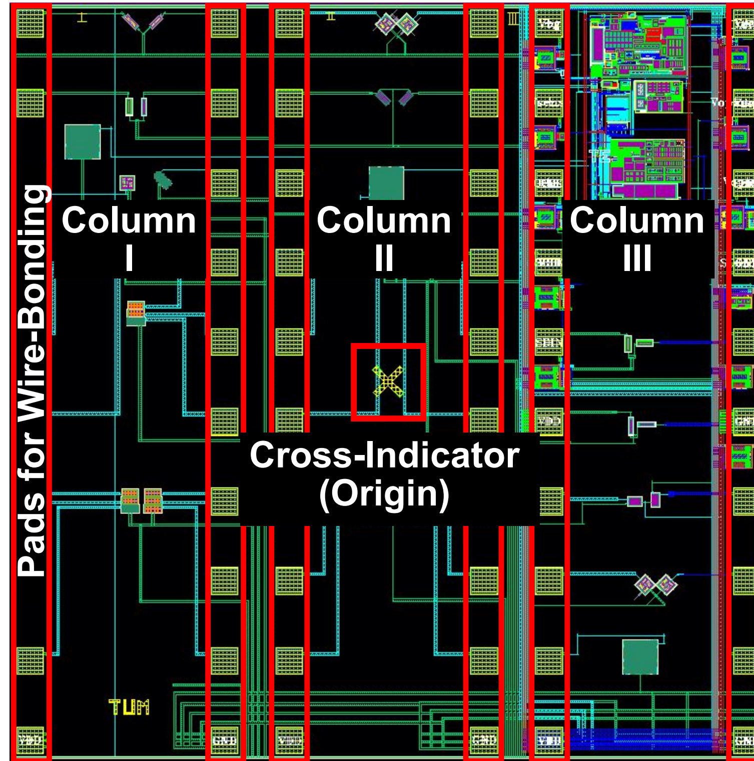

Figure 3.4: Layout of a test chip with an indicator for sawing process and three columns for test structures with overall 60 bonding pads.

Another important aspect for the wire-bonding is the loop parameters of the wire, especially the loop height that should be high enough to sustain deflections within measurement limits of the silicon beam. Also the pads on the PCB should be laid out to have sufficient space during wire bonding. Fig. 3.6 shows processed silicon beams and PCBs for wire bonding, as well as s bonding plan and bonded test structures.

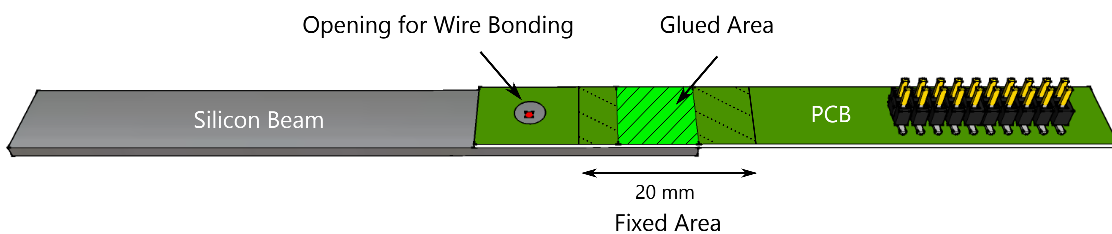

Figure 3.5: Configuration of silicon beam and PCB for wire bonding.

The mechanical apparatus was made of aluminum alloys (except of the weight holder) by using a Computerized Numerical Control (CNC) milling machine with an accuracy of ± 50 μm. The weight holder is realized from a PVC-based rod to reduce its empty weight of ≈ 18.43 g that determines the minimum applicable mechanical stress of ≈ 10.86 MPa (after zero stress).

The temperature and stress measurements have shown that the weight holder can sustain the temperatures from - 50° to 125° and stress values up to 400 MPa.

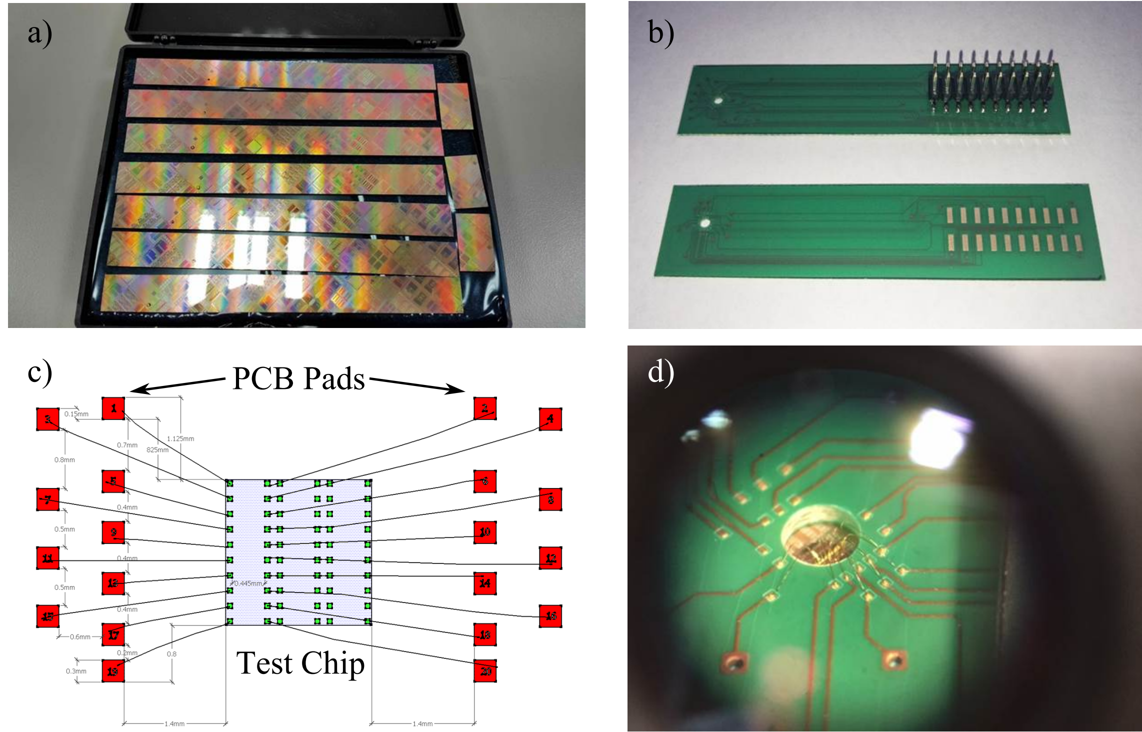

Figure 3.6: Components for wire bonding. a) Processed silicon beams with 10 cm length and 1 cm width. b) PCBs with opening for wire bonding and pin header. c) Bonding plan for test chip. d) Bonded test structures.

To be able to switch between different silicon beams, each beam is attached to a test module, which can be easily screwed onto the mechanical apparatus, as shown in Fig. 3.7.

The resulting inaccuracies of the measurement setup with respect to the equation 3.1 can be given as:

$$\begin{aligned} l &= 65 \text{ mm} \pm 50 \text{ um} \\ w &= 10 \text{ mm} \pm 50 \text{ um} \\ h &= 0.774 \text{ mm} \pm 10 \text{ um} \\ x &= 5 \text{ mm} \pm 1 \text{ mm} \end{aligned} \tag{3.3}$$

The accruing relative errors of the stress values can be calculated by inserting the maximum deviations to equation 3.1:

$$\begin{aligned} \Delta\sigma/\sigma_0(\Delta l) &= \sigma/\sigma_0(l+\Delta l, w, h, x) \approx 0.83\% \\ \Delta\sigma/\sigma_0(\Delta w) &= \sigma/\sigma_0(l, w+\Delta w, h, x) \approx 0.5\% \\ \Delta\sigma/\sigma_0(\Delta h) &= \sigma/\sigma_0(l, w, h+\Delta h, x) \approx 2.64\% \\ \Delta\sigma/\sigma_0(\Delta x) &= \sigma/\sigma_0(l, w, h, x+\Delta x) \approx 1.67\% \end{aligned} \tag{3.4}$$

The overall inaccuracy of the measurement setup results in approximately ± 5.6 MPa in the range of ± 100 MPa, which is 5.6% relative error. This tolerance is obtained by summation of the absolute values of the individual error components. It can be seen that the largest error component arises from the error of the height h of the silicon beam, as a result of quadratic dependence in the equation. This error can be reduced by measuring the thickness of the silicon beam or by dicing the wafer. In general post-processing measurements of the silicon beam and of the mechanical apparatus will result in significantly higher accuracy of the setup.

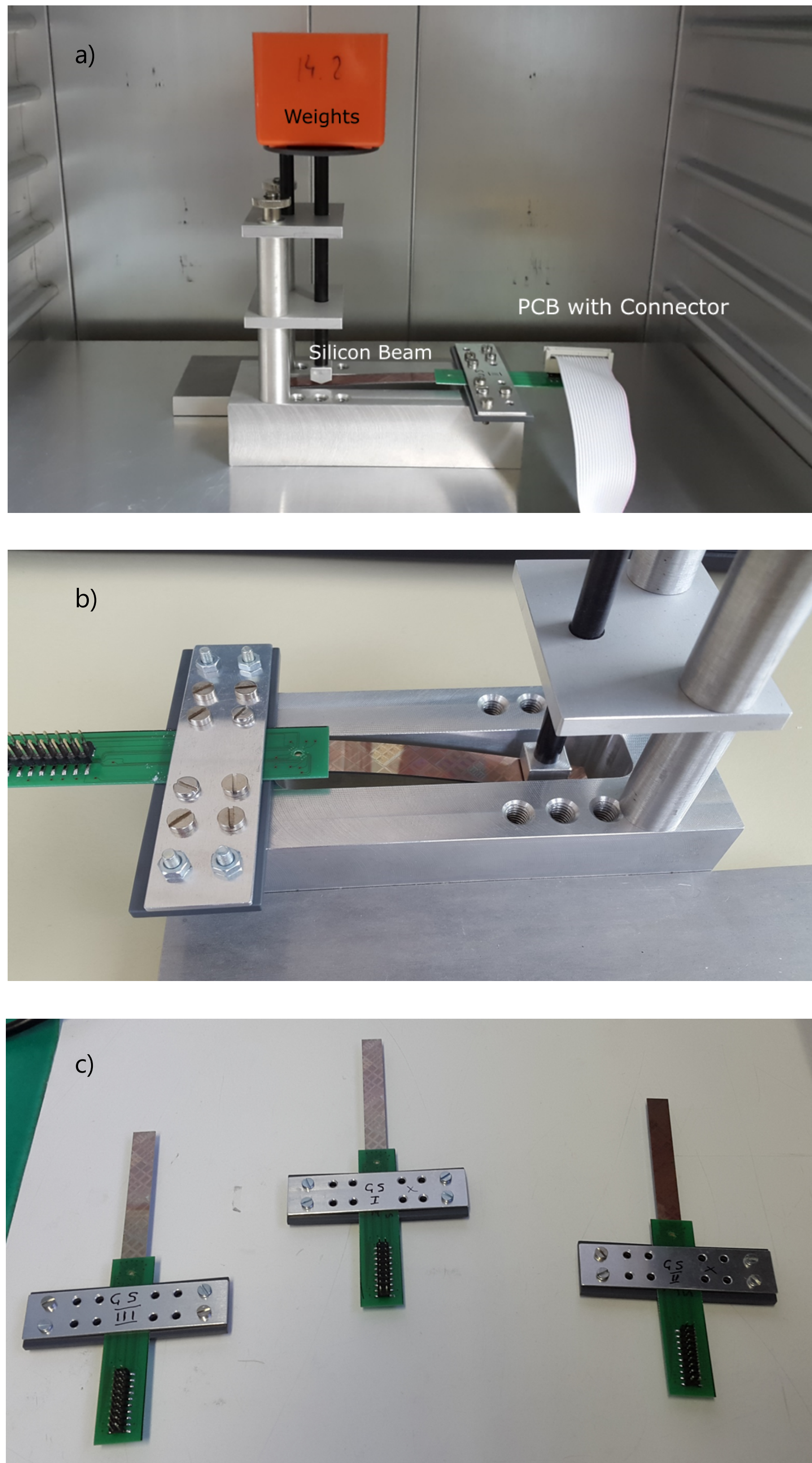

Figure 3.7: Measurement setup for mechanical stress sensors. a) Mechanical apparatus connected to measurement equipment. b) Mechanical apparatus under load of appr. 600 g, which corresponds to a stress of 360 MPa. c) Test modules with silicon beams.

3.2 Measurement Setup with Adjustable Angle of Applied Mechanical Stress

The four-point bending method, shown in Fig. 3.8, has the feature that the surface stress of a bent strip is constant between the inner two supports. That constant surface stress σ relates to the external force F according to

$$\sigma = \frac{3\alpha F L}{b h^2}, \tag{3.5}$$

with a geometry related constant α, the distance between the outer supports L, the width of the beam b, and the thickness (height) of the beam h.

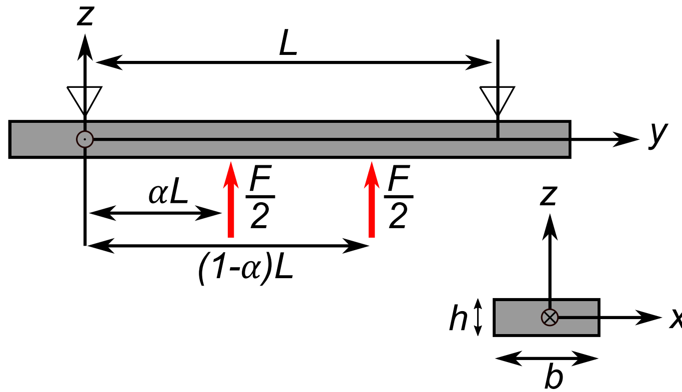

Figure 3.8: Mechanical four-point bending measurement setup: schematic representation of four-point bending setup.

The constant stress is advantageous in our case, because it ensures that the on-chip stress is independent of the position of the chip as long as it lies between the inner supports. Moreover, it ensures that the imposed external stress is constant over the whole chip area; hence, we know that large deviations measured within the chip are caused by setup-independent factors such as integrated nearby structures and packaging.

Implementation of Measurement Setup

Similar to the previous implementation, a 3D CAD Model was created to estimate the required dimensions for the setup (see Fig. 3.9). In order to fit into the temperature chamber of our institute (50 cm x 50 cm x 40 cm), it was decided to work with smaller pieces of silicon rather than taking a whole wafer that in our case has dimensions of 300 mm. Therefore a silicon piece with a 5 x 5 cm^2 square shape was sawn from the wafer.

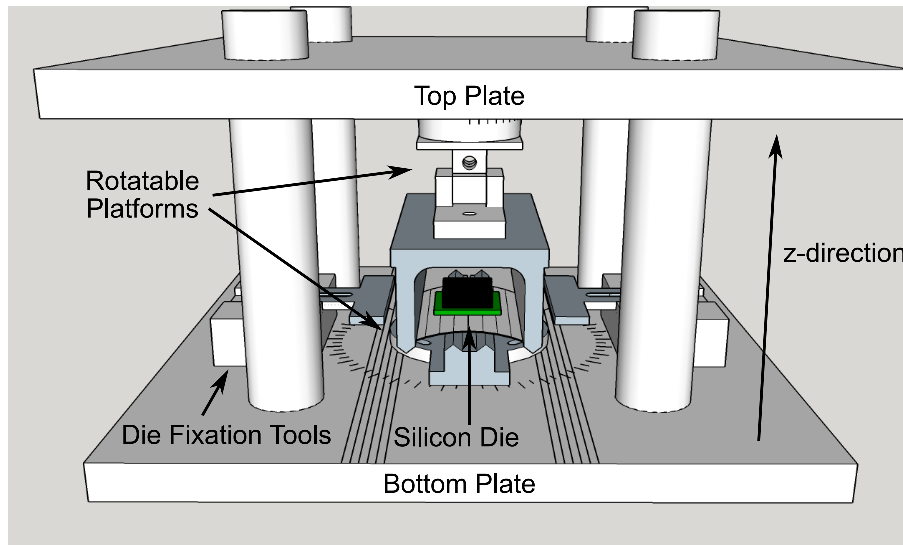

Figure 3.9: 3D Model of four-point bending mechanical apparatus with adjustable angle of applied mechanical stress.

For adjustable angel of applied stress, the outer and inner supports are fixed on two rotatable platforms that are placed between two plates; the top plate is movable in z-direction. Therefore, four rods and linear ball bearings are used to minimize any friction (in z-direction) and keep the top plate stable without wobbling.

The interface between the square-shaped silicon die was also established with wire bonding and the PCB with opening, as it was discussed in section 3.1. Due to the geometrical peculiarity, the setup is capable of applying only one type of stress values after bonding (tensile or compressive).

Unlike, the measurement setup for uniaxial stress, where the silicon beam can be flipped, the silicon peace of the four-point bending technique has to be oriented with the test chip surface showing to the top plate. Fig. 3.10(a) depicts a photography of our measurement setup for tensile stress configuration. The device under test (DUT) can be manually placed at a free angle and calibrated weights are used to impose stress according to equation 3.5. Fig. 3.10(b) also contains a photograph of a built-in DUT measured at an angle of 30°.

Another consideration that has to be taken during the 3D design, is the empty weight of the top plate with the rotatable platform. The empty weight was resulting in a stress value higher than 100 MPa and was not suitable for characterization of the test structures at lower stress values. Therefore a counterweight system was implemented with diverter pulleys and a crane to redirect the forces and compensate the empty weight of the weight holder. The complete implementation of the four-point measurement setup is shown in Fig. 3.11.

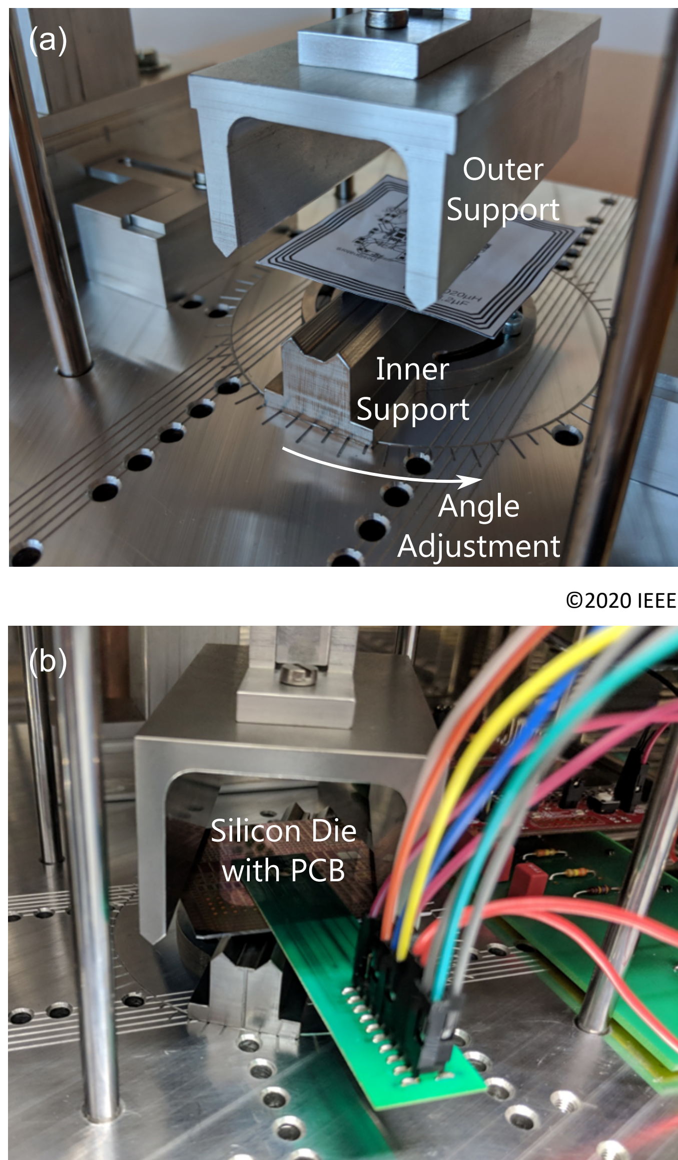

Figure 3.10: Mechanical four-point bending measurement setup: (a) photograph with outer and inner supports for tensile stress configuration, and (b) with DUT during measurements.

Considering the inaccuracies of CNC milling machine, the error analysis for the four-point bending can be given by using equation 3.5:

$$\begin{aligned} \Delta\sigma/\sigma_0(\Delta L) &= \sigma/\sigma_0(L+\Delta L, b, h, \alpha) \approx 0.14\% \\ \Delta\sigma/\sigma_0(\Delta b) &= \sigma/\sigma_0(L, b+\Delta b, h, \alpha) \approx 0.1\% \\ \Delta\sigma/\sigma_0(\Delta h) &= \sigma/\sigma_0(L, b, h+\Delta h, \alpha) \approx 2.54\% \\ \Delta\sigma/\sigma_0(\Delta \alpha) &= \sigma/\sigma_0(L+\Delta L, b, h, +\Delta\alpha) \approx 0.02\% \end{aligned} \tag{3.6}$$

The overall accuracy is 5% in stress magnitude limited by wafer thickness precision, and 3° in stress angle limited by accuracy of manual alignment of the DUT.

Also it should be mentioned that errors resulting from the square shape of the DUT are considered to have a negligible effect on the overall accuracy (from discussions with colleagues at Texas Instruments and the Technical University of Munich). To determine the percentage of the error more precisely, finite element method simulations are necessary, which were not performed in this project.

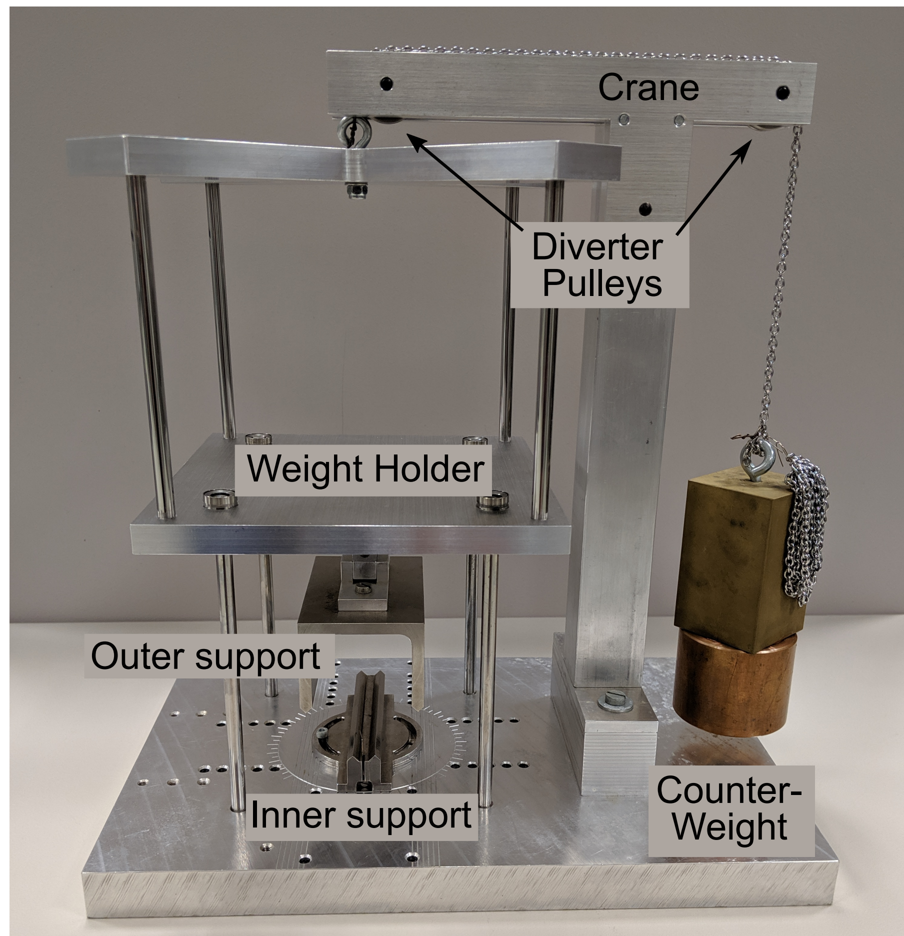

Figure 3.11: Mechanical four-point bending measurement setup with counterweight system for compensation of empty weight of the weight holder.

Chapter 4

Design of Stress Sensor

Modern sensor systems provide information about physical quantities in analog or digital form, depending on the final application. To extract the physical properties from the environment, various types of sensing elements can be used that respond to the change of desired quantity by changing their electrical properties (e.g. resistance).

Ideally, the sensing elements should respond only to the changes of the desired physical quantity while exhibiting relatively high sensitivity. The response should be linear to simplify the signal post-processing, so that it can also be realized with analog circuits. Moreover, for industrial and also for consumer applications, the manufacturing materials and complexity have to be affordable and the cost low for a high volume production.

In the last decades, CMOS has been the leading technology and offers versatility as well as cost efficiency in production of ICs. Therefore, there is a tendency towards integration of all system components including sensing elements and readout electronics into the same silicon chip. Even if the sensing elements cannot be integrated into the chip, the required readout electronics are mostly fabricated in CMOS technology.

A relatively high mechanical stress sensitivity (conductivity change with deformation) of semiconductor devices were published in [28]. A stress sensitivity of 50 times higher than by conventional metal strain gauges (sensing elements for strain measurements) were reported, making semiconductor devices highly suitable for the sensing of mechanical stress.

Unfortunately, due to the property of semiconductor materials, the stress sensing elements respond also to other physical quantities, e.g. temperature [29]. The dependence of stress sensitivity Π along with the resistivity ρ on temperature effects for various doping concentrations were presented in [30]. Moreover, it was reported that the temperature dependence of the stress sensitivity decreases with increasing doping concentration and that the higher doping concentration, in turn, leads to lower stress sensitivity [30].

The nonlinearity effects for strain values higher than 1% (relative to deformation) were shown in [31] by quantifying the second and third piezoresistive coefficients.

To compensate the mentioned nonidealities of semiconductor based piezoresistive sensing elements, various stress sensing concepts, utilizing different circuit techniques and also other methods as signal post-processing are used. There are numerous sensing concepts, optimized for specific applications and therefore for sensing a certain stress component that are explained in the following subsections.

Sensing Difference in Normal Stresses ($\sigma_{xx} - \sigma_{yy}$)

When the difference of normal stress components in x- and y-direction needs to be measured, the use of the Wheatstone bridge can be advantageous [32]. The sensing elements can be aligned in longitudinal (current flow in the direction of stress) and in transverse (current flow perpendicular to stress direction) configurations, building the full Wheatstone bridge with diagonally placed longitudinal and transverse sensing elements. Thus, for an applied stress, the sensitivity of the longitudinal elements is inversely proportional to the sensitivity of the transverse elements that allows to achieve relatively high differential sensitivity ($\sigma_{xx} - \sigma_{yy}$) and leads to a better signal to noise performance [33].

Another benefit that can be achieved by using the Wheatstone bridge is the temperature compensation (in first order) of the differential voltage between the left and right branches of the bridge that relies on ratios between the similar temperature dependence of the sensing elements.

Fig. 4.1(a) shows a schematic implementation of the Wheatstone bridge for sensing the difference of the normal stress components. For the defined coordinate system with x along [110] and y along [-110] crystallographic directions, a pair of two orthogonal p-type resistors is oriented in the [110] and [-110] directions, building the full bridge configuration.

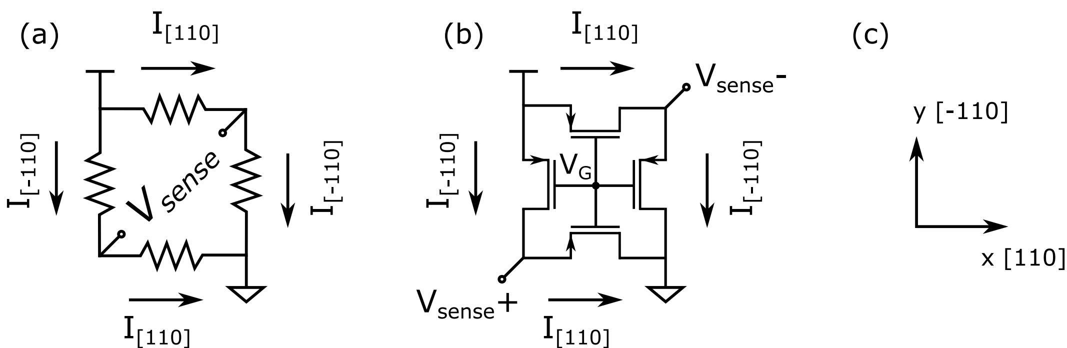

Figure 4.1: Schematic of sensing elements in the Wheatstone bridge configuration for measuring the difference of in-plane normal stresses ($\sigma_{xx} - \sigma_{yy}$): (a) Implementation with p-type resistors, (b) Implementation with PMOS transistors and (c) Definition of the coordinate system.

The sensitivity of the differential voltage V_{sense} depends on the piezoresistive coefficient Π_{44} and can be given as

$$\Delta V_{sense} \propto \Pi_{44}^{\mathrm{p}}(\sigma_{xx} - \sigma_{yy}) \tag{4.1}$$

It should be mentioned that the sensor can be implemented with n- or p-type resistors but the sensitivity of the p-type sensor is higher due to piezoresistive coefficient $\Pi_{44}^{\mathrm{p}} \approx 13.8$ %/100 MPa, compared to $\Pi_{44}^{\mathrm{n}} \approx$ -1.36 %/100 MPa (see Table 2.1). Therefore the p-type resistors are more preferable for the Wheatstone bridge in this case.

Beside p-well and PSD (P-doped Source Drain) resistors, the Wheatstone bridge can also be implemented with MOS transistors that allow to have higher channel resistance with smaller device dimensions, compared with conventional diffusion resistors. Moreover, the high channel resistance leads to a lower power consumption [34].

The MOSFETs are operated in strong inversion and saturation regions therefor. The schematic implementation of the Wheatstone bridge with PMOS transistors for sensing the difference between the in-plane normal stresses are shown in Fig. 4.1(b). The gate contacts of the MOS transistors are connected together and can be used as a switch by applying V_{DD} or V_{SS} voltages for enabling or disabling the sensor.

The disadvantages of the MOSFET based bridges is the higher dependence on process variations due to transistor parameters (e.g. threshold voltage V_{th}, transistor gain factor β) and higher noise due to the device complexity [34].

In some cases, the use of mechanical stress dependent currents might be necessary. The current mirror configuration, as shown in Fig. 4.2, can be used to sense the difference of the normal stress components, similar to the Wheatstone bridge.

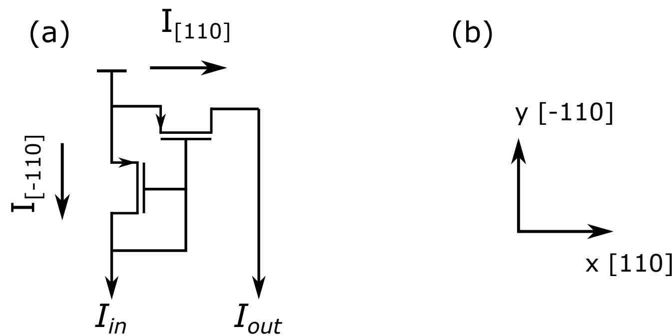

Figure 4.2: Schematic of sensing elements in current mirror configuration for measuring the difference of in-plane normal stresses ($\sigma_{xx} - \sigma_{yy}$): (a) Implementation with PMOS transistors and (b) Definition of the coordinate system.

The orthogonally aligned PMOS transistors respond differently to the normal stresses that can be measured through the difference between the currents I_{in} and I_{out}

$$\Delta I = I_{in} - I_{out} \propto \Pi^{\mathrm{p}}_{44}(\sigma_{xx} - \sigma_{yy}) \tag{4.2}$$

Ideally, if no stress is applied, the currents are identical and any temperature changes result in a common mode response.

Sensing Shear Stress (σ_{xy})

For sensing the in-plane shear stress, n-type resistors oriented along the [100] and [010] wafer directions can be used. Analogously to the sensing the stresses in direction of current, the Wheatstone bridge configuration provides various advantages mentioned in the previous section. Fig. 4.3 illustrates an implementation of a bridge with n-type resistors as well as with NMOS transistors.

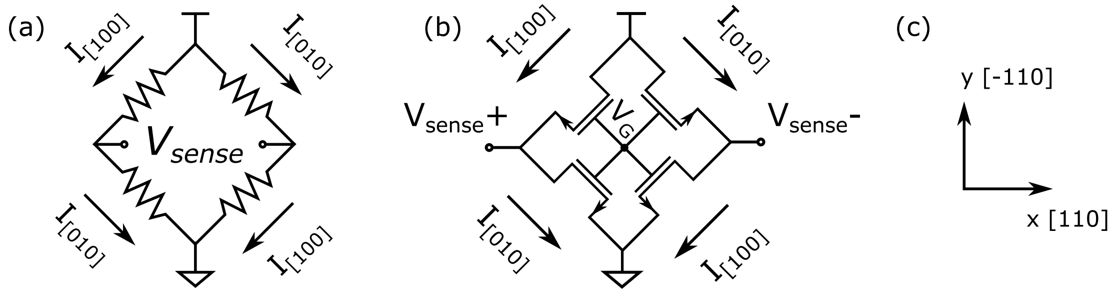

Figure 4.3: Schematic of sensing elements in Wheatstone bridge configuration for measuring the in-plane shear stress σ_{xy}: (a) Implementation with n-type resistors, (b) Implementation with NMOS transistors and (c) Definition of the coordinate system.

The sensitivity of both configurations depends on the difference $(\Pi_{11} - \Pi_{12})$ and can be expressed as follows

$$\Delta V_{sense} \propto (\Pi^{\mathrm{n}}_{11} - \Pi^{\mathrm{n}}_{12})\sigma_{xy} \tag{4.3}$$

For the n-type based configuration the sensitivity of the difference $(\Pi^{\mathrm{n}}_{11} - \Pi^{\mathrm{n}}_{12}) \approx$ -15.6 %/100 MPa and for the p-type $(\Pi^{\mathrm{p}}_{11} - \Pi^{\mathrm{p}}_{12}) \approx 0.77$ %/100 MPa, making the n-type configuration more suitable option.

The schematic with NMOS transistors is shown in Fig. 4.4, for current mode stress sensing. The resulting stress sensitivity can be given as

$$\Delta I = I_{in} - I_{out} \propto (\Pi^{\mathrm{n}}_{11} - \Pi^{\mathrm{n}}_{12})\sigma_{xy} \tag{4.4}$$

Sensing Sum of Normal Stresses ($\sigma_{xx} + \sigma_{yy}$)

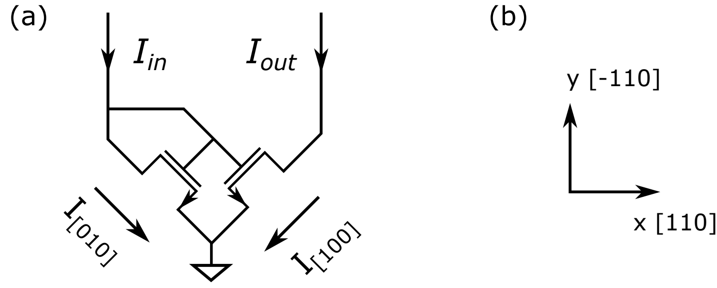

Figure 4.4: Schematic of sensing elements in current mirror configuration for measuring the in-plane shear stress σ_{xy}: (a) Implementation with NMOS transistors and (b) Definition of the coordinate system.

In some applications (e..g for compensation of stress effects in IC packages), it is required to sense the sum of the in-plane normal stresses. In [11], it was shown that orthogonally aligned n-type resistors respond to the sum of the in-plane normal stress components. Fig. 4.5 illustrates the schematic configuration of the resistor and NMOS based sensors. The sensing elements can be connected in series (or parallel) with the resulting sensitivity shown below

$$\Delta V_{sense} \propto \frac{\Pi_{11}^{\mathrm{n}} + \Pi_{12}^{\mathrm{n}}}{2}(\sigma_{xx} + \sigma_{yy}) \tag{4.5}$$

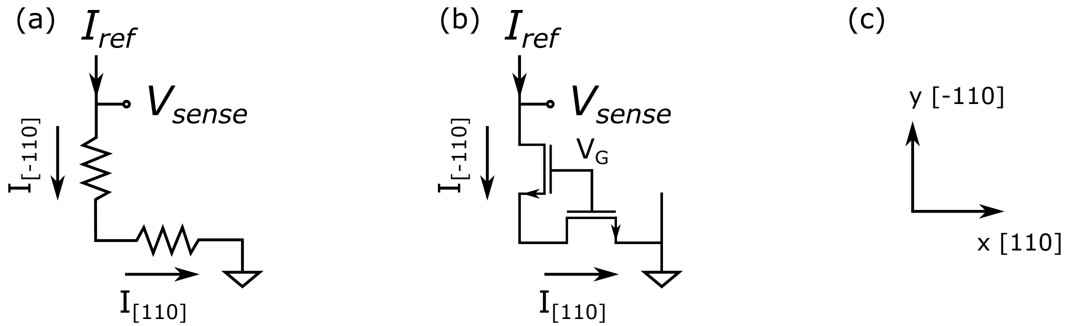

Figure 4.5: Schematic of sensing elements for measuring the sum of in-plane normal stresses $(\sigma_{xx} + \sigma_{yy})$: (a) Implementation with n-type resistors, (b) Implementation with NMOS transistors and (c) Definition of the coordinate system.

Since the stress is extracted directly from the absolute voltage V_{sense}, the temperature dependence and other undesired parameters need to be compensated with analog or digital circuit techniques, so that V_{sense} responds only to the stress change. In [10], an n-well device was proposed that has similar temperature dependence as the sensing resistors and can be used as a reference by implementing an analog front-end.

Sensing Magnitude and Angle of In-Plane Stress

In the applications, where several types of stress components (e.g. shear, normal stresses) need to be detected, separate sensors (resistor configurations) for measuring a certain, distinct stress component can be used. The angle and the magnitude of the stress can be then extracted from the separate measured stress components. The disadvantage of such systems is the utilization of both p-type and n-type resistor based sensors, that have high (uncorrelated) dependence on process variations.

In [35], a multidimensional stress sensor with the active region consisting of n-well in p-doped substrate was proposed. The sensor has eight side contacts C_{1-8} in octagonal alignment and one middle contact C_M. The structure of the sensor is shown in Fig. 4.6.

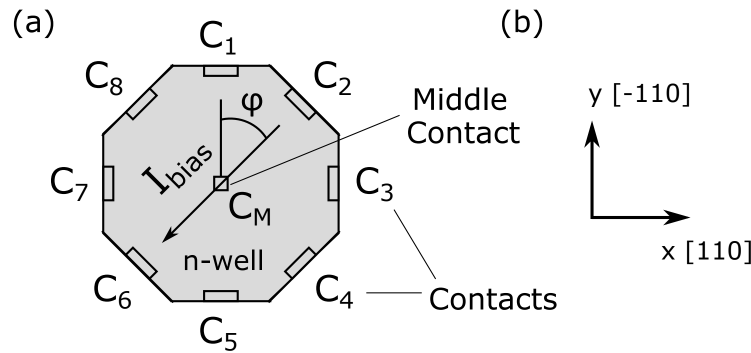

Figure 4.6: Schematic of sensing elements for measuring difference of in-plane normal stresses ($\sigma_{xx} - \sigma_{yy}$): (a) Implementation with p-type resistors, (b) Implementation with PMOS transistors and (c) Definition of the coordinate system.

During the operation of the sensor, two opposite contacts (e.g. C_1 and C_5) are selected to apply the bias current I_{bias}. The middle contact C_M can be connected to a fixed potential for more symmetrical operation of the device. Due to the octagonal shape of the sensor, the angle of the applied current φ, can be switched in 45° angular steps. For a certain applied current direction, two voltages are measured: the parallel voltage $V_{\parallel}$ and the orthogonal voltage $V_{\perp}$ to the current direction. The stress dependence of the voltages $V_{\parallel}$ and $V_{\perp}$ with respect to the current angle φ can be expressed as

$$\begin{aligned}\Delta V_{\parallel}(\varphi) \propto (\Pi^{n}_{11} - \Pi^{n}_{12})\sigma_{xy}\sin(2\phi) + \frac{1}{2}\Pi^{n}_{44}(\sigma_{xx} - \sigma_{yy})\cos(2\phi) \\ + \frac{1}{2}(\Pi^{n}_{11} + \Pi^{n}_{12})(\sigma_{xx} + \sigma_{yy})\end{aligned} \tag{4.6}$$

$$\Delta V_{\perp}(\varphi) \propto (\Pi^{n}_{11} - \Pi^{n}_{12})\sigma_{xy}\cos(2\phi) - \frac{1}{2}\Pi^{n}_{44}(\sigma_{xx} - \sigma_{yy})\sin(2\phi) \tag{4.7}$$

The combination of voltages $V_{\parallel}(\varphi)$ and $V_{\perp}(\varphi)$ for the eight current directions (φ = 45°× n, n = 0 - 7), allows to extract and separate the in-plane stress components σ_{xx}, σ_{yy} and σ_{xy}, but requires more complex signal conditioning.

4.1 Proposed Sensing Concept

As mentioned in Chapter 2, the resistive properties of silicon vary under application of stress (σ) and can be quantified by a set of piezoresistive coefficients (Π_{11}, Π_{12} and Π_{44}) providing sensitivity for each crystalline direction. In many applications, the in-plane normal stress components are of primary interest. For example, due to planar structure of silicon dies in ICs, mechanical stress caused by packaging consists mainly of x- and y-components, close to the center of the die. Therefore, most sensitive system components (bandgap references, etc.) should be places in the middle of the die (see Chapter 1).

By neglecting the out-of-plane normal stress, the 3D stress state consisting of nine components can be simplified to a "plane stress problem" with two normal stress components only [36]. For the 2D case, n-well resistors placed along a main crystal axis, i.e. [100] and [010] still have sensitivity to both σ_{100} (σ_{xx}) and σ_{010} (σ_{yy}) stress components; their total resistance can be expressed as

$$\begin{aligned} R_{[100]} &= R_0(1 + \Pi_{11} \cdot \sigma_{100} + \Pi_{12} \cdot \sigma_{010}) \\ R_{[010]} &= R_0(1 + \Pi_{12} \cdot \sigma_{100} + \Pi_{11} \cdot \sigma_{010}) \\ R_{[001]} &= R_0(1 + \Pi_{12} \cdot \sigma_{100} + \Pi_{12} \cdot \sigma_{010}), \end{aligned} \tag{4.8}$$

where R_0 is the nominal resistor value without stress.

Similarly, if the stress is applied in the [110] or [-110] direction, the equation can be given as

$$\begin{aligned} R_{[110]} &= R_0(1 + \frac{1}{2}(\Pi_{11} + \Pi_{12} + \Pi_{44}) \cdot \sigma_{[110]}) \\ R_{[-110]} &= R_0(1 + \frac{1}{2}(\Pi_{11} + \Pi_{12} - \Pi_{44}) \cdot \sigma_{[-110]}) \end{aligned} \tag{4.9}$$

These equations result from the simplification of equation 2.5. Therefore, R_{xx} as proposed in Fig. 4.7(a) is composed of two orthogonal resistors ($R_{[100]}$ and $R_{[010]}$) in series such that the unwanted y-component is rejected. This scheme is possible because of the physical dependence ($\Pi_{11} \approx -2\Pi_{12}$) [38] and requires proper sizing of the resistance ratio R_{100}/R_{010} for cancellation (with $\sigma_{xx} = \sigma_{100}$ and $\sigma_{yy} = \sigma_{010}$)

$$\begin{aligned} R_{xx} \approx 2R_{[100]} + R_{[010]} = \\ R_0(3 + (2\Pi_{11} + \Pi_{12}) \cdot \sigma_{xx} + (2\Pi_{12} + \Pi_{11}) \cdot \sigma_{yy}) \approx \\ 3R_0(1 - \Pi_{12}) \cdot \sigma_{xx} \end{aligned} \tag{4.10}$$

Similarly, R_{yy} shown in Fig. 4.7(b), reacts only to y-component stress

$$R_{yy} \approx R_{[100]} + 2R_{[010]} \approx 3R_0(1 - \Pi_{12}) \cdot \sigma_{yy} \tag{4.11}$$

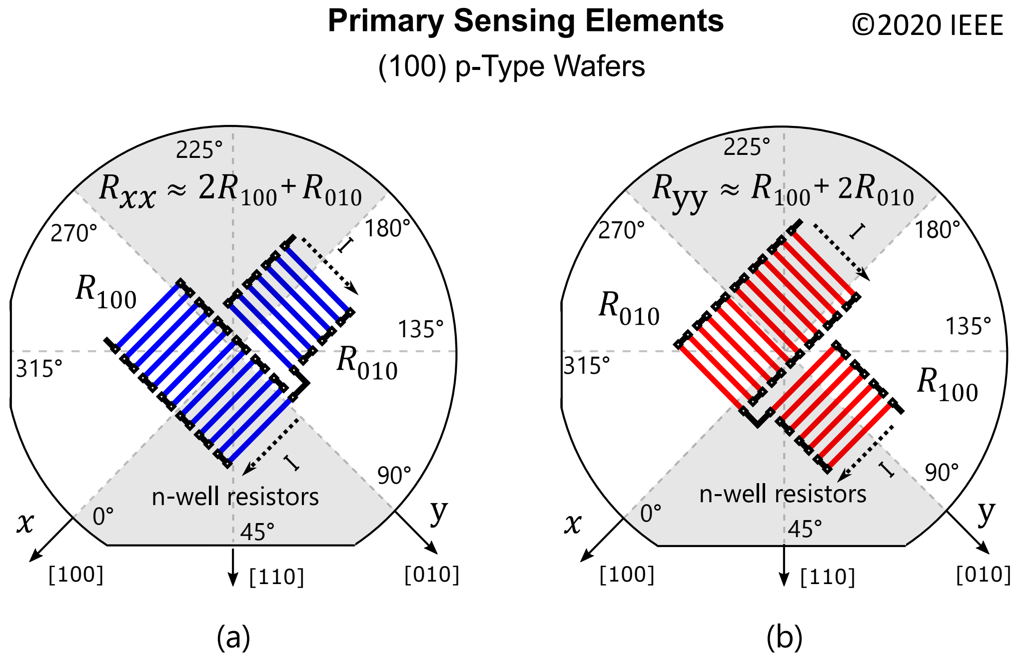

Figure 4.7: The primary sensing elements: (a) Resistor configuration of R_{xx} (x-direction sensitive element), (b) Resistor configuration of R_{yy} (y-direction sensitive element).

As can be seen from equations 4.10 and 4.11, if the resistor ratios are well matched, both configurations R_{xx} and R_{yy} have the same sensitivity to their corresponding x- or y-stress component, namely $3R_0(1 - \Pi_{12})$. For example, if we take the value for n-type resistor from Table 2.1, the resulting sensitivity of both elements will be approximately -5%/100MPa. The use of two equally sensitive n-well sensors (R_{xx} and R_{yy}) allows for 2D spatial resolution with extraction of both stress magnitude and angle.

The experimental response of primary sensing elements versus mechanical stress angle and amplitude can be seen in Fig. 4.8(a) and (b), respectively. As shown, sensed resistor deviations for R_{xx} and R_{yy} are equivalent values at 45° and 135° angles, implying that quadrant operation is ambiguous. It is equivalent to say that stress forces applied along the [110] or [-110] directions are indistinguishable.

An auxiliary sensing element R_Q is required to discern between the first and second quadrants {0 to 90°} and {90 to 180°} where the two n-well sensors output a nearly zero differential signal. R_Q consists of two p-type resistors oriented along the [110] and [-110] directions connected in differential mode, as shown in Fig. 4.9(a). For this task, as can be seen in Fig. 4.9(b), only simple detection of the sign of ΔR/R change is required.

We have also included additional elements for sensing the shear stress, but the measurement setup was not designed to generate any shear stress. Therefore, we could not provide any shear stress results at the time of measurement.

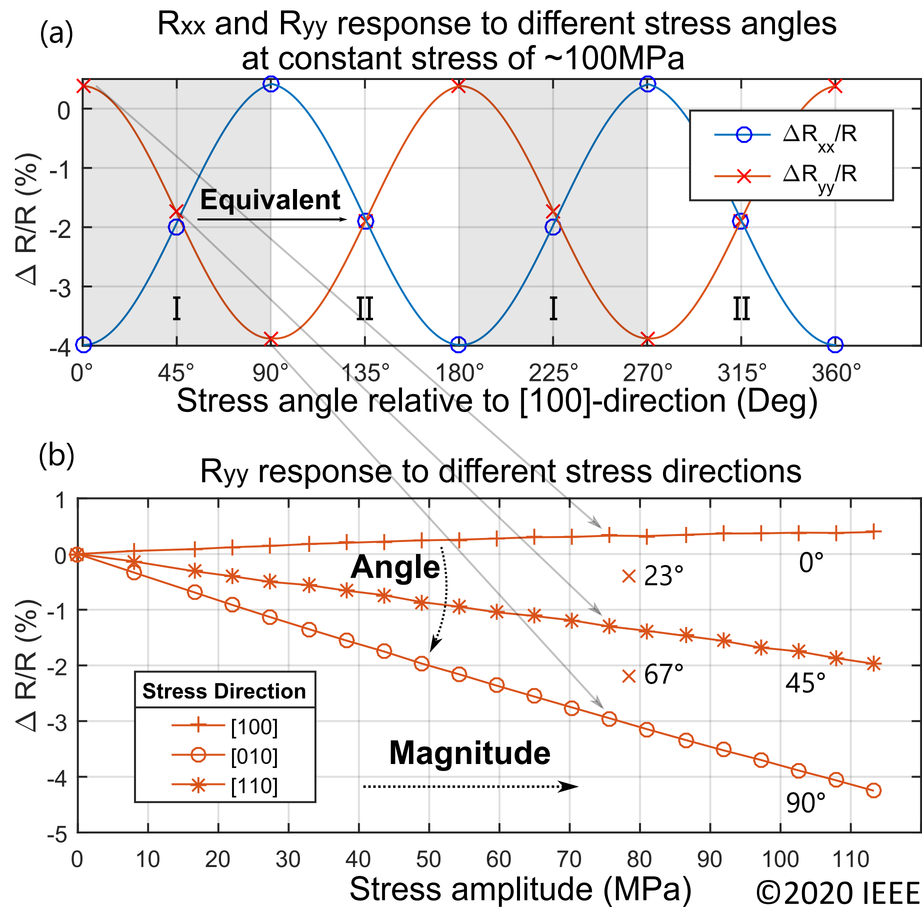

Figure 4.8: Concept of the stress sensing with experimental measurement results: (a) response of primary sensing elements to different stress angles at a constant stress magnitude of 100MPa and (b) response of R_{yy} to stress amplitude and angle.

4.2 Implementation of Sensing Elements

Stress sensitivity is essentially the gain factor (similar meaning as for an amplifier) relating physical stress and a corresponding output variable (i.e. ΔR/R). One of the most important aspects when choosing a sensing element is how its stress sensitivity varies over doping concentration N (more specifically, N_A for p-type or N_D for n-type). If this variation is high, then the sensing elements in every chip would need to be calibrated in a well-controlled manner, thus adding complexity and cost. To avoid this problem, the doping concentration should be in a range where the sensitivity is minimally dependent on process variation.

In order to characterize these dependencies the p-Factor was introduced in [37]. As shown in Fig. 4.10, the p-Factor describing stress sensitivity vs. doping concentration is given for n-type and p-type silicon and for various temperatures.

The stress sensitivity for a certain doping concentration and temperature can be obtained by multiplying the piezoresistive coefficients by the p-Factor. It can be

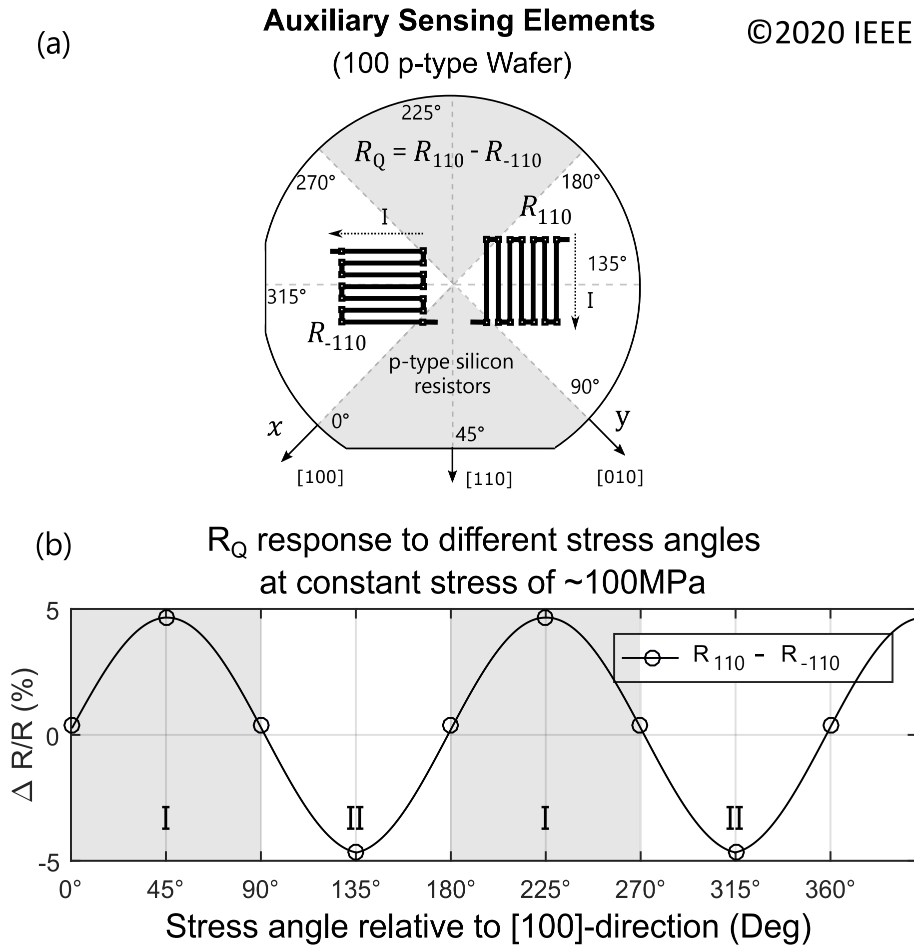

Figure 4.9: Concept of determination of quadrants: (a) resistor configuration of auxiliary sensing elements and (b) response of auxiliary sensing elements to different stress angles.

seen that for doping concentrations below 10^{18}cm^{-3} (nearly flat portions of curves, labeled as constant region), the stress sensitivity of n-type silicon resistors is less dependent on the variation of doping concentration.

The disadvantage of lower doping concentration is a higher temperature dependence of stress sensitivity, as can also be seen in the figure by differing p-factor values at different temperatures (the various curves are far apart). However, the over-temperature behavior in the constant region is largely disconnected from N (i.e. the various curves are flat) and can be compensated by measuring the temperature and correspondingly scaling the stress sensitivity.

Since n-well and n-doped source drain (NSD) regions are an integral part of CMOS transistors, there is no need for extra mask layers for implementation of primary sensing elements. Usually, the doping concentration of an n-well is much lower than that of the NSD region. Therefore, n-well resistors were preferred as primary sensing elements (its associated p-Factor values are in the constant region).

On the other hand, the variation of stress sensitivity for auxiliary sensing elements

doesnt affect the overall accuracy of the stress sensor, and the p-doped drain source (PSD) resistors were preferred due to area and resistor value considerations.

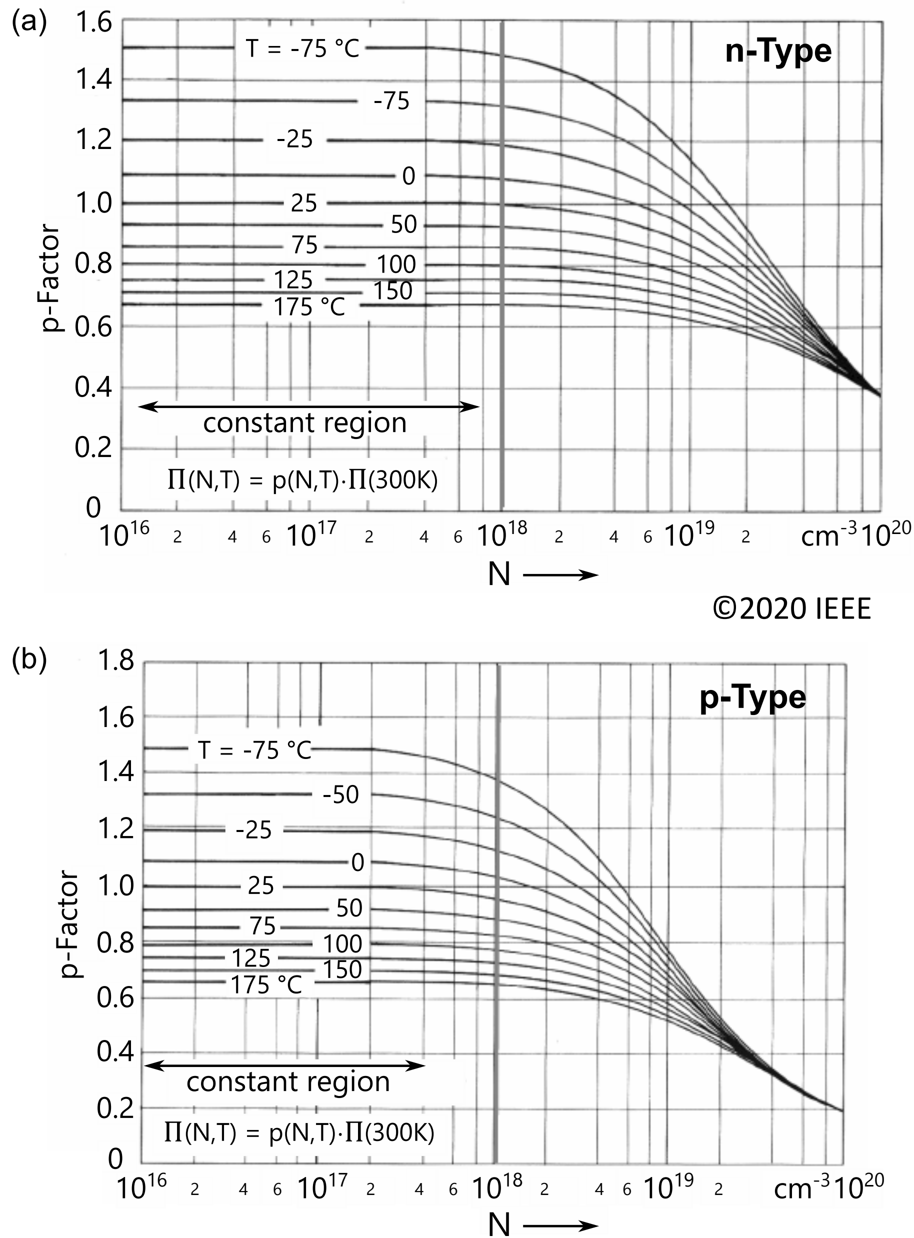

Figure 4.10: p-Factor as a function of doping concentration and temperature. The stress sensitivity of (a) n-Type and (b) p-Type resistors are calculated by multiplying the p-Factor to piezoresistive coefficients determined at 300K (data extracted from [37]).

4.3 Implementation of Reference Elements

Temperature effects arising from n-well resistive behavior are shown in Fig. 4.11(a). As proposed in [10], for analog[1] cancellation of this behavior a reference resistor R_{ref} with similar temperature dependence but reduced stress sensitivity (by a factor of ≈10x relative to R_{xx} and R_{yy}) was designed.

R_{ref} is used to generate an inversely proportional temperature dependent current. This current is then forced through each resistive sensing element, illustrated in Fig. 4.11(b) for a single sense resistance R_{sense}, resulting in a first-order temperature compensated common-mode voltage across the sensing resistors (≈750 mV in this design). The reduced voltage variation over temperature increases the dynamic range of the system (operation always takes place near the following ADCs optimum input range).

Proper (stress-insensitive) implementation of R_{ref} is an important consideration for the proposed system. The method applied here relies on the undesired stress components being canceled using a combination of orthogonal resistive elements whose net sensitivity is essentially nulled. As shown in Fig. 4.12(a) and (b), this is accomplished by mixing vertical and lateral current streamlines in the n-well structure to have similar doping and therefore temperature dependence.

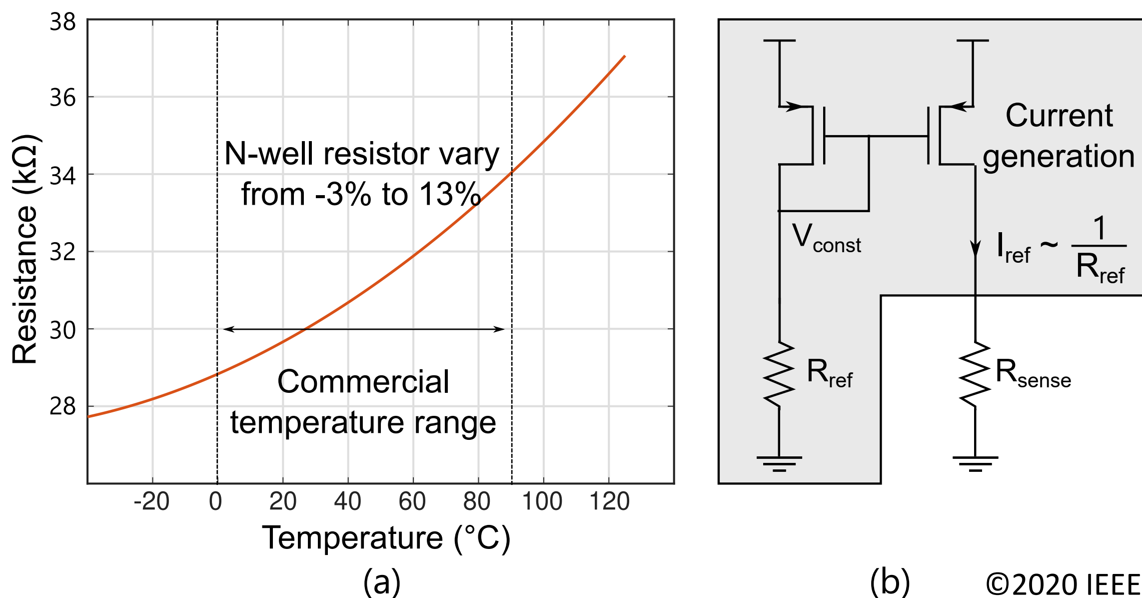

Figure 4.11: Concept of reference elements: (a) temperature behavior of n-well can be compensated by applying (b) current with inverse temperature dependence of the reference.

It can be seen from equation 4.8 that vertical resistor $R_{[001]}$ exhibits equal sensitivity to both stress components, namely $R_0(1 + \Pi_{12}(\sigma_{xx} + \sigma_{yy}))$. This dependence was compensated by using the same physical dependence ($\Pi_{11} \approx -2\Pi_{12}$) that was used

[1] As opposed to additional digital techniques, to be described in Section VI

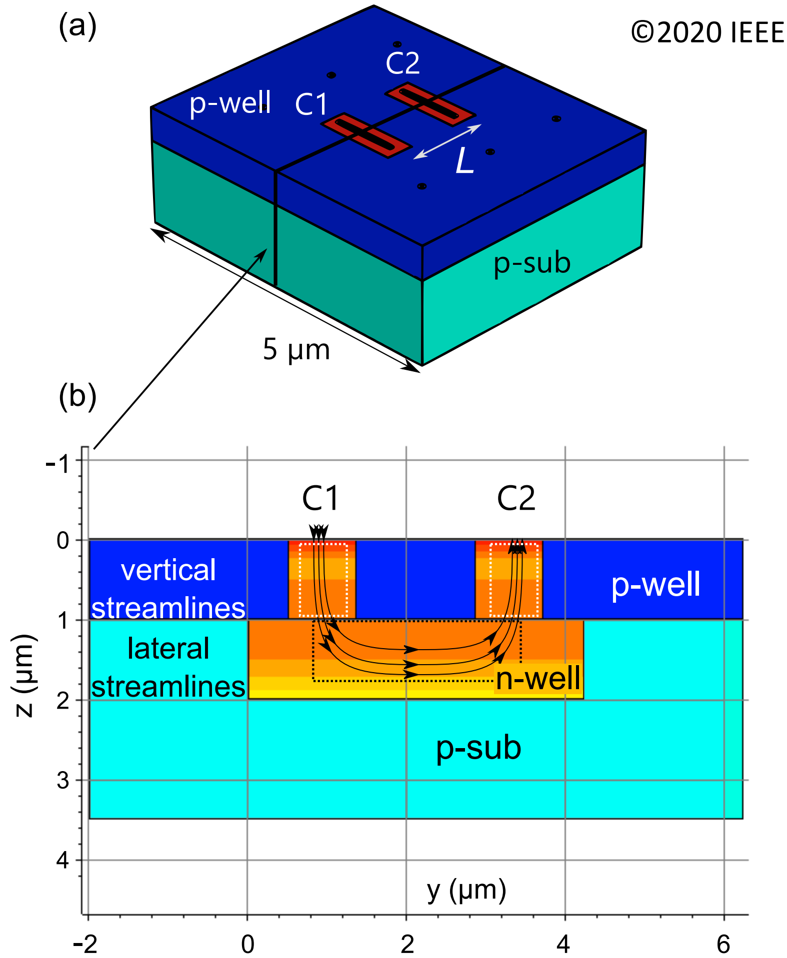

Figure 4.12: Implementation of the reference elements: (a) 3-D view of reference element and (b) section view of the reference resistor with vertical and lateral current streamlines in an n-well structure.

for rejection of undesired x- or y-component stress in our sensing elements. Since the vertical current components exhibit positive stress sensitivity $\Pi_{12} \approx 5.34\%/100\text{MPa}$ for lightly doped n-type resistors (see Table 2.1), the sensitivity of lateral current streamlines has to be negative when positive stress is applied. Moreover, the sensitivity of lateral streamlines has to be equal to both stress components without angular dependency. To fulfill all mentioned requirements, two orthogonal structures (one oriented along the [110] and the other along [-110] direction) shown in Fig. 4.12(a) were connected in series.

Thus, the total sensitivity of the reference resistor R_{ref}, consisting of lateral and vertical current streamlines can be calculated as follows

$$
\begin{aligned}
R_{ref} &= L \cdot [R_{[110]} + R_{[-110]}] + R_{[001]} \\
&= L \cdot [R_0(1 + \frac{1}{2}(\Pi_{11} + \Pi_{12} + \Pi_{44}) \cdot \sigma_{[110]}) \\
&\quad + R_0(1 + \frac{1}{2}(\Pi_{11} + \Pi_{12} - \Pi_{44}) \cdot \sigma_{[-110]})] \\
&\quad + R_0(1 + \Pi_{12}(\sigma_{[100]} + \sigma_{[010]})) \\
&= L \cdot R_0[2 + (\Pi_{11} + \Pi_{12})(\sigma_{[110]} + \sigma_{[-110]})] \\
&\quad + R_0(1 + \Pi_{12}(\sigma_{[100]} + \sigma_{[010]})),
\end{aligned}
\tag{4.12}
$$

with L being the distance between the contacts C1 and C2 (see Fig. 4.12(a)).

Using the coordinate transformation from [39], we can express $\sigma_{[110]}$, $\sigma_{[-110]}$ as a function of $\sigma_{[100]}$ and $\sigma_{[010]}$

$$
\begin{aligned}
\sigma_{[110]} &= \frac{1}{2}(\sigma_{[100]} + \sigma_{[010]}) \\
\sigma_{[-110]} &= \frac{1}{2}(\sigma_{[100]} + \sigma_{[010]})
\end{aligned}
\tag{4.13}
$$

As can be seen from equation 4.13, the sum of $\sigma_{[110]}$ and $\sigma_{[-110]}$ is equal to the sum of $\sigma_{[100]}$ and $\sigma_{[010]}$, showing that the sum of any orthogonal stress components (in 2-D case) has the same sensitivity to any stress angles.

By substituting $(\sigma_{[110]} + \sigma_{[-110]})$ in equation 4.12, the sensitivity of R_{ref} can be expressed as a function of $(\sigma_{[100]} + \sigma_{[010]})$ only

$$
\begin{aligned}
R_{ref} &= L \cdot R_0[2 + (\Pi_{11} + \Pi_{12})(\sigma_{[100]} + \sigma_{[010]})] \\
&\quad + R_0(1 + \Pi_{12}(\sigma_{[100]} + \sigma_{[010]})) \\
&= R_0[1 + 2L + (L(\Pi_{11} + \Pi_{12}) + \Pi_{12})(\sigma_{[100]} + \sigma_{[010]})]
\end{aligned}
\tag{4.14}
$$

Considering the physical dependence $(\Pi_{11} \approx -2\Pi_{12})$, we can derive following equation

$$
\begin{aligned}
R_{ref} &= R_0[1 + 2L + (L(-\Pi_{12}) + \Pi_{12})(\sigma_{[100]} + \sigma_{[010]})] \\
&= R_0[1 + 2L + (L(-\Pi_{12}) + \Pi_{12})(\sigma_{xx} + \sigma_{yy})]
\end{aligned}
\tag{4.15}
$$

Ideally, if the resistances for vertical and lateral components are the same, L should be equal to 0. In other cases L can be adjusted to reject the stress dependence of R_{ref}. Fig. 4.13 shows the stress sensitivity of the reference elements in the main four crystallographic directions.

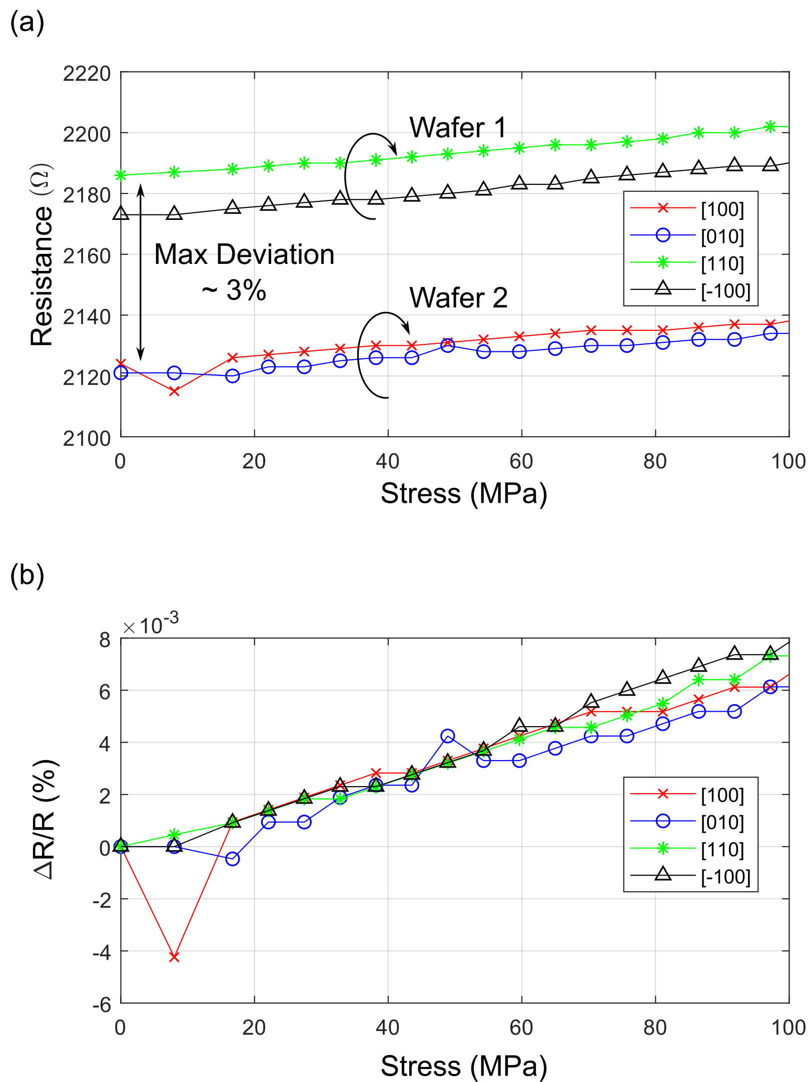

Figure 4.13: Stress sensitivity of the reference element: (a) absolute resistance change (b) relative resistance change over applied tensile mechanical stress in the [100], [010], [110] and [-110] directions (four different reference elements from two wafers).

Since stress sensitivity is only a weak function of doping concentration N (owing to p-Factor flatness), process variations have a minimal influence on sensor performance.

As can be seen in Fig. 4.13(a), the absolute values of reference elements from two different wafers are on average approximately 2.15 kΩ and vary by max. 3%. However, for reasonable statistical confidence, more measurements from different wafers and devices are required. The relative resistance change also for devices from two different wafers and for the main crystallographic orientation is shown in Fig. 4.13(b). It can be seen that the reference elements respond similarly to the tensile stress with the sensitivity on average of 0.7%/100 MPa, which is 5.7x reduced stress sensitivity compared to sensing elements. Since the resulting response of the reference element has a positive sensitivity, it can be further reduced by increasing the length L be-

tween the contacts of R_{ref}. By increasing L, the negative components of the stress sensitivity will increase as shown in equation 4.15. This compensation scheme is very similar to temperature compensation of a bandgap reference, where proportional to absolute temperature (PTAT) is mixed with complementary to absolute temperature (CTAT) component. Fig. 4.14 illustrates the layout of the reference elements for three different lengths L and shows the corresponding stress sensitivities. The increase of the length by approximately 50 % results in approximately 30 % reduction of the stress sensitivity.

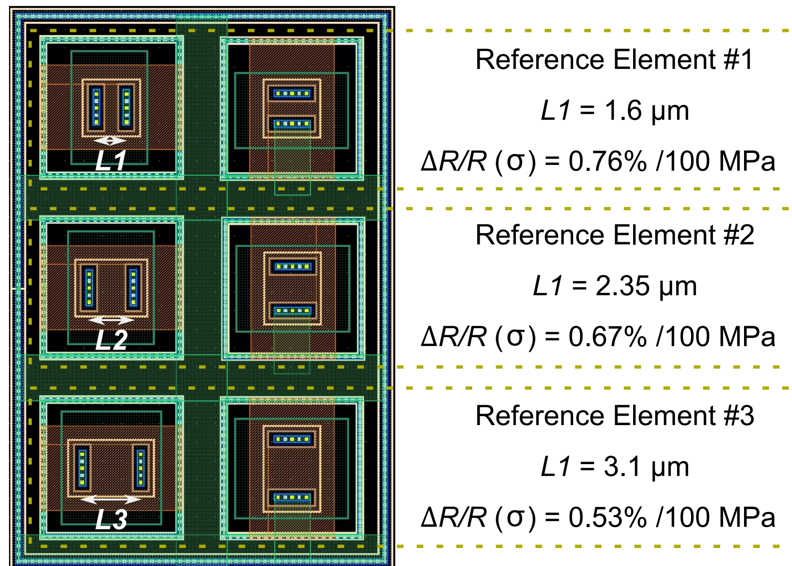

Figure 4.14: Layout of the reference elements for three different lengths (L_1, L_2 and L_3) with corresponding stress sensitivities.

This concept can be used not only for design of reference elements but also for design of sensing elements with a certain stress sensitivity that can be adjusted with the dimensions of the device (L).

Another aspect that should be considered by designing the reference element is the variation of the doping concentration (N) over the depth of the n-well structure that can affect the overall temperature behavior of the device. This might cause a mismatch between temperature coefficients of sensing and reference elements and the main purpose of using the reference resistor (same temperature dependence and 0 stress sensitivity) will not be fulfilled. Fig. 4.15 depicts the temperature behavior of R_{sense} in comparison to R_{ref} with the three lengths (L_1, L_2, L_3).

In all three cases, the temperature behavior of reference elements distinguishes from "target" behavior of the sensing element. However, if the length L is increased, the difference in temperature behavior between R_{sense} and R_{ref} becomes smaller, resulting in a more stable temperature dependence of the circuit shown in Fig. 4.11(b).

It should be noted that the dependencies between L and temperature behavior of R_{ref} might be different in other CMOS technologies. In our case, the increase of L

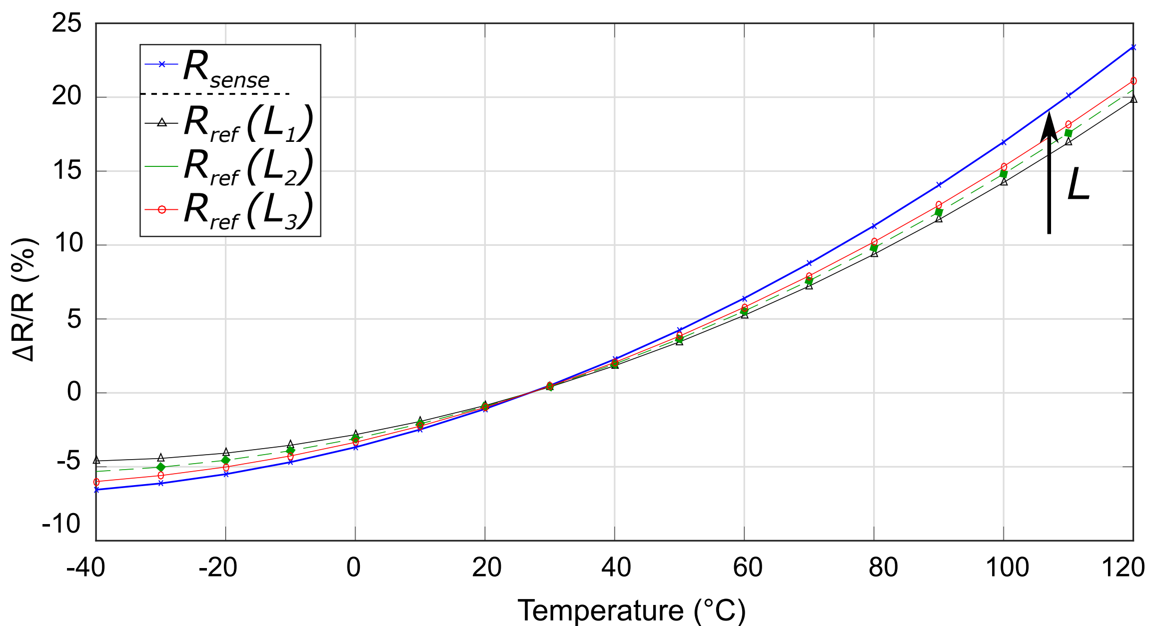

Figure 4.15: Temperature behavior of the sensing elements R_{sense} (target) and the reference elements R_{ref} for the three lengths (L_1, L_2 and L_3).

was optimal for matching of temperature coefficients as well as for reduction of the stress sensitivity of the reference element.

4.4 Behavioral Models for Simulation

For a circuit-level system design, there is a need for simplified behavioral models of sensing and reference elements that can be integrated in analog or/and mixed-signal simulation environment. The models can be written e.g. with Verlog-A language for Cadence Virtuoso or similar simulation tool. The experimental results from previous section, where the stress sensitivity and temperature dependence were measured of the sensing and subsequently of the reference elements, can be used for extraction of the necessary coefficients for the modeling.

Since the sensing elements are conventional n-well resistors without any modifications (except the alignments), the existing process design kit (PDK) n-well model was used. The stress sensitivity that is not usually included in PDK was modeled as additional voltage drop V_Δ on top of the absolute voltage V_0 of the n-well resistor for x- and y-directions

$$\begin{aligned} V(\sigma_{xx}) &= V_0 + V_\Delta = I \cdot R_0 + I \cdot R_0(\Pi_{12} \cdot \sigma_{xx}) \\ V(\sigma_{yy}) &= V_0 + V_\Delta = I \cdot R_0 + I \cdot R_0(\Pi_{12} \cdot \sigma_{yy}) \end{aligned} \tag{4.16}$$

This modeling technique allows to take advantage of the existing PDK device that usually has advanced models for process variations (corner simulations) and can also

be used for mismatch simulations.

Due to the novelty of the reference resistor (not a PDK device) and uncertainty of the n-well depth, the dependence of the stress sensitivity Π_{ref} and also the first order temperature coefficient TC_1 and second order coefficient TC_2 on L were unknown. To determine these dependencies for any lengths L (within reasonable dimensions) of the device, stress sensitivity and temperature measurements for three different lengths L were performed. The measured data points allow to extract the necessary coefficients and set up following equations

$$\begin{aligned} \Pi_{ref}(L) &= C_{21}L^2 + C_{11}L + C_{01} \\ TC_1(L) &= C_{22}L^2 + C_{12}L + C_{02} \\ TC_2(L) &= C_{23}L^2 + C_{13}L + C_{03} \end{aligned} \tag{4.17}$$

The coefficients C_{21}, C_{11} and C_{01} were extracted with curve fitting from measurements over mechanical stress at L_1, L_2 and L_3. Additional coefficients can be extracted for second or higher order fitting to cover wider stress ranges if necessary.

Similarly, the coefficients C_{22}, C_{12}, C_{02} for TC_1 and C_{23}, C_{13}, C_{03} for TC_2 were extracted from temperature measurements. Here we decided to extract the second order coefficients for wider temperature ranges (from -40°C to 120°C).

The final model of the reference resistor can be given dependent on mechanical stress, temperature and length as follows

$$\begin{aligned} R_{ref}(\sigma, T, L) = R_0 \cdot [1 + \Pi_{ref}(L) \cdot \sigma] \cdot [1 + TC_2(L) \cdot T_p^2 + TC_1(L) \cdot T_p], \\ \text{with } T_p = T - 27°C \end{aligned} \tag{4.18}$$

4.5 Final Layout of the Stress Sensor

A proper design of the sensor layout is of high importance, especially the impact of the mismatch and doping concentration gradients can be significantly reduced by using special layout techniques. Since our sensing concept relies on matching of orthogonal n-well resistors, R_{xx} and R_{yy} are divided each into six elements (resistor fingers). Thus, the elements can be aligned to have a common center and the gradients of doping concentration are compensated at a first approximation. R_{xx} is laid out with two fingers oriented in the [010] direction and residual four fingers along the [100] direction. By following this procedure, R_{yy} is interdigitated, so that both sensing resistors are exposed to the similar process conditions and are well matched. To further improve the matching performance of the sensor, dummy resistors were placed at the outside regions of the sensing resistors to minimize differences in the physical structures of the matched devices in production.

Also it is a good practice to isolate sensitive devices from (noisy) switching circuit blocks by using guard rings. For our devices a combination of n- and p-wells are used to build a ”strong barrier” against undesired signals.

Fig. 4.16 shows the final layout of the stress sensor with implemented techniques that are mentioned above. Each stress sensor has its own reference resistors for generation of the reference current I_{ref} and integrated p-type resistors with sensing elements allow to measure magnitude and angle of mechanical stress. The close placement of the reference and sensing resistors ensures optimal parameter tracking over process variations, reducing overall temperature behavior deviation. The sensor is 70 x 70 μm^2 and designed to achieve the common mode voltage of 750 mV in nominal conditions. This voltage was considered to be suitable for low power consumption and still to be sufficient for a wide dynamic range of the system. The dimensions of the sensor can vary depending on specification for power consumption, system accuracy and the CMOS technology.

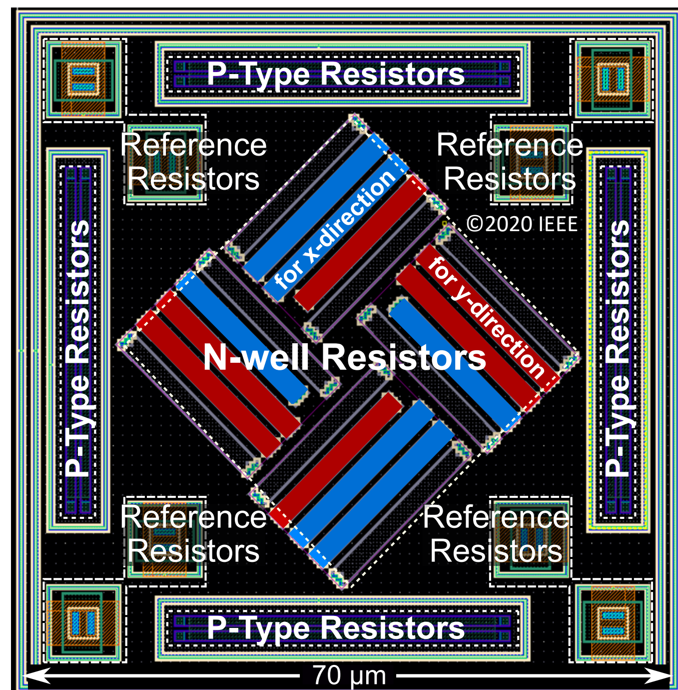

Figure 4.16: Common centroid layout with the guard rings of the stress sensor with built-in reference and p-type resistors for magnitude and angle measurements.

Chapter 5

Readout Electronics

The main purpose of readout electronics is to detect and convert a desired (physical) signal to analog or digital domain for further use. Depending on the final application of the sensor, the specifications and requirements for the readout electronics can be different, ranging from the system architecture to dimensioning of individual devices and circuit components.

As in any other technical design discipline, there is always a trade-off between the key parameters of the system (e.g. speed, power consumption, area, noise performance, accuracy, precision, etc.). The specifications and requirements set the priority between these parameters that allow to optimize the system for a certain application.

The readout electronics usually consists of an analog front-end (AFE) that can be considered as a main part of the signal conditioning in the analog domain. The first overview of the AFE circuits (Wheatstone bridge, current mirror configurations) are presented in Chapter 4. Furthermore, reference signals are required for the proper functionality of the system that can be generated with bandgap references in combination with Low-Dropout Regulators (LDOs) and voltage buffers.

If the analog signal needs to be converted to a digital form, the system includes an Analog-to-Digital Converter (ADC) with Digital Signal Processor (DSP) or Micro-Controller Unit (MCU) for additional signal conditioning in the digital domain.

To be able to select between different modes of the system (e.g. sensing of the shear stress or the normal stresses) or to control the power management (duty cycle operation, selection of the low power mode), a digital signal control is used in modern sensor systems.

In the following we will give an overview of commonly used readout electronics for the sensing elements presented in Chapter 4.

In [40], readout electronics for measuring of 32 MOSFET-based stress sensors is presented. The AFE of the system consists of a Wheatstone bridge with a Programmable Gain Amplifier (PGA) for the gain setting (between 100 and 700) and a multiplexer at the input of the PGA for selecting between the 32 stress sensors.

The sensor system also contains an 8-bit ADC with a DSP that can address all sensors and preform digital signal conditioning (low-pass filtering). The system is optimized for measuring the difference between the normal stresses ($\sigma_{xx} - \sigma_{yy}$) and the shear stress σ_{xy} and can be used for the evaluation of the stress effects during fabrication and packaging.

A comparable readout architecture was presented in [41], for measuring the mechanical stress in orthodontic brackets. The sensor system can also measure the difference of the in-plane normal stresses ($\sigma_{xx} - \sigma_{yy}$), as well as the shear stress σ_{xy}. The AFE utilizes a Wheatstone bridge with a Differential Difference Amplifier (DDA) with automatic gain selection, instead of using a conventional instrumentation amplifier. The advantage of using a DDA is better offset and linearity performance, and the automatic gain selection offers a high sensor resolution.

In [33], a readout system for low noise and low frequency detection of the stress signals was presented. The limitation of the system operating at low frequencies is mainly determined by the 1/f noise (flicker noise), generated by references, amplifier stages and finally by the piezoresistive sensing elements.

To overcome this limitation, a modulation-demodulation system was used. Therefore, a Wheatstone bridge is exited with a sinusoidal signal that modulates the stress dependent signal to frequencies higher than the corner frequency (the frequency, where the noise power of the 1/f noise and white noise is equal) and after amplification, the system filters the undesired frequency ranges out, with the subsequent demodulation.

For current mode stress sensing in [42], an integrator (implemented with a two stage Miller opamp), in combination with a track-and-hold stage, serves as the AFE of the system. The low pass filter behavior of the integrator reduces the noise and other circuit components do not (in first order) contribute to stress signal.

A relaxation oscillator based readout circuit for resistive sensors was demonstrated in [43]. The system differs from other topologies by its robustness to circuit component nonidealities as offset voltage, gain variation of opamps, mismatch in the values of the reference voltages.

In [44] a resistance-to-delay and in [45] a resistance-to-frequency conversion with readout electronics were implemented, respectively.

5.1 General Design Considerations

Based on the final applications of our stress sensor (mentioned in Chapter 1), the readout of the sensor system should be implemented in Texas Instruments 130 nm standard CMOS technology and operate with low power consumption. Also for IoT applications, the small area requirements are essential for the sensor system.

Moreover, the readout electronics have to operate with multiple stress sensors, distributed over the chip area for measuring the local absolute stress values and stress

gradients. The magnitude of the minimum detectable stress signal should be smaller than 200 kPa and all required signals should be provided in digital form.

Also, it was agreed to limit the bandwidth of interest from 0.5 Hz to 7.5 kHz. This limitation allows to minimize the noise power spectrum by filtering out the noise components outside the bandwidth, while still be able to measure semi-static and dynamic stress changes for wider fields of applications.

The system can be supplied with power by a battery and should operate within the voltage ranges from 1.8 V to 3.3 V. The sensor system contains switching circuits and therefore, power supply rejection ratio (PSRR) has to be higher than 90 dB to suppress variations of the supply voltage.

In the following sections, we will show the design steps for the implemented system blocks that can be used for any other standard CMOS technology. Since the parameters of Texas Instruments technology is under non-disclosure agreement, we will demonstrate the equations, used during the design, without giving concrete values or numbers of sensitive information.

5.2 Analog Front-End

DC-Analysis

The AFE was designed for the stress sensor described in Chapter 4. The equivalent schematic representation of the stress sensor is shown in Fig. 5.1. As can be seen, the sensing and reference resistances vary from each other and require proper current values to achieve a certain common mode voltage.

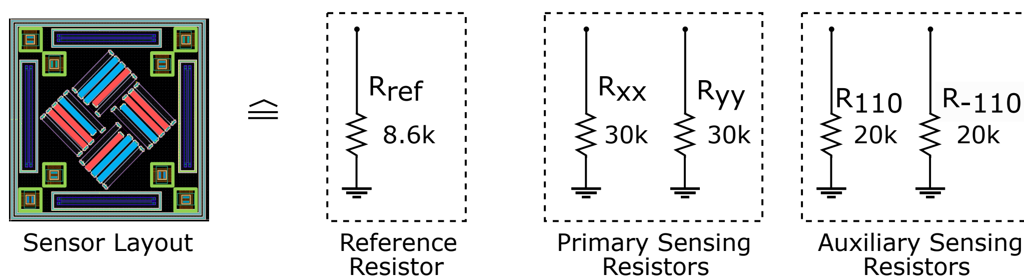

Figure 5.1: Layout of the stress sensor with equivalent schematic representation of reference, primary and auxiliary resistors.

After considering several system architectures, it was decided to set the common mode voltage across the sensing resistors to 750 mV. This voltage allows us to use different ADCs and makes the sensor more integrable to other system environments.

Therefore, the current for primary sensing resistors I_{pr} can calculated as

$$I_{pr} = \frac{750 \text{ mV}}{30 \text{ k}\Omega} = 25 \ \mu\text{A}, \tag{5.1}$$

and the current for auxiliary sensing resistors I_{aux} can be give as

$$I_{aux} = \frac{750 \text{ mV}}{20 \text{ k}\Omega} = 37.5 \ \mu\text{A}. \tag{5.2}$$

These current values are valid for the ideal case, where the resistors show always the same values for all conditions. The real integrated resistors vary over process conditions from device to device and from wafer to wafer, resulting in an offset between the ideal and the real common mode voltage. Therefore an area efficient concept is needed to compensate the resulting offset voltage. Fig. 5.2 demonstrates a simplified schematic of the AFE that is used in our sensor system.

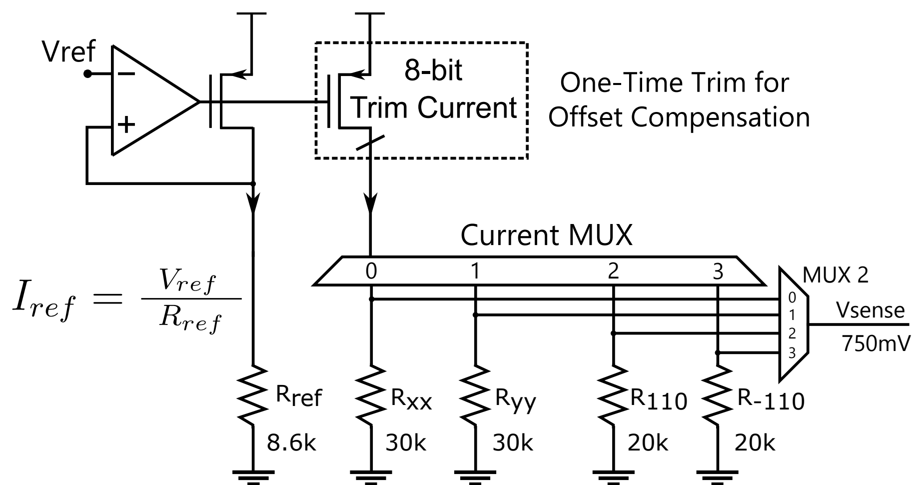

Figure 5.2: Schematic of AFE with trimmable opamp-based voltage to current converter and multiplexers for resistor selection.

An opamp-based voltage to current converter is implemented to generate the current with inverse temperature dependence of the (ideally non-stress sensitive) reference resistor. The generated current is mirrored with PMOS transistors and applied to the sensing resistors. This architecture allows to individually trim every sensing element with a single trimming circuitry that will be discussed in the following sections.

The dependence between reference voltage V_{ref_pr} for the primary sensing elements at the negative input of the opamp and the currents I_{pr} can be calculated as follows

$$V_{ref_pr} = I_{pr} \cdot R_{ref} = 215\text{mV}. \tag{5.3}$$

Similarly, V_{ref_aux} depends on the current I_{aux}

$$V_{ref_aux} = I_{aux} \cdot R_{ref} = 322.5\text{mV}. \tag{5.4}$$

From the equations above, we can determine the input voltage range of the opamp and hence, decide about the type of the input differential pair. Since, V_{ref_pf} is close to the ground potential, PMOS transistors are more suitable choice than NMOS ones. Even for PMOS differential pair, the resulting voltage levels can be too low to keep the transistors of the opamp first stage in saturation region. For certain conditions (temperature, process variations), the input differential pair can fall out of the saturation region and therefore, V_{ref_pr} and V_{ref_aux} were increased to 430 mV and 645 mV, respectively.

This was achieved by setting the mirror ratio to 2x

$$\begin{aligned} V_{ref_pr} &= 2 \cdot I_{pr} \cdot R_{ref} = 430 \text{ mV}, \\ V_{ref_aux} &= 2 \cdot I_{aux} \cdot R_{ref} = 645 \text{ mV}. \end{aligned} \tag{5.5}$$

As a result, I_{ref_pr} and I_{ref_aux} should be equal to 50 μA and 75 μA, respectively. To be able to trim the common mode voltage, additional current branches were used that can be digitally switched on or off. The 8-bit trimming circuitry was implemented to cover the variation range from -30 % to 30 % of the reference current I_{ref}. This range covers minimum and maximum of possible resistance variations over process conditions and therefore ensures that V_{sense} can be trimmed to nominal voltage of 750 mV. The simplified schematic of the trimming circuit is shown in Fig. 5.3. The ideal switches, shown in the Figure, are implemented as inverters with PMOS and NMOS transistors.

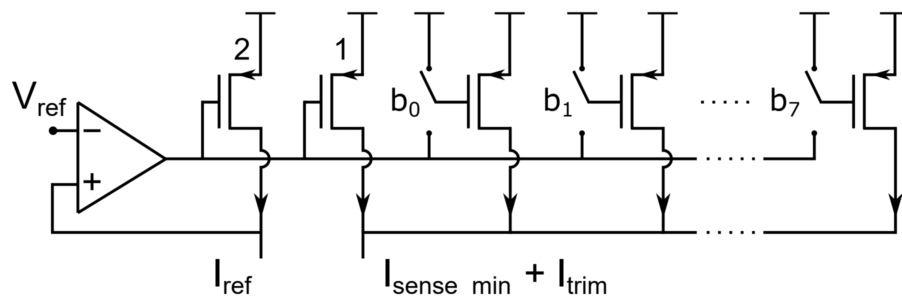

Figure 5.3: Simplified schematic of the trimming circuit for the AFE. A digital control can vary bit0 to bit7 to trim the mirrored current.

The functionality of the trimming circuit is shown in Fig. 5.4. The AFE was simulated with sensing and reference resistors over process corners (Nominal, Strong, Weak, SkewNP, SkewPN) to determine the maximum spread before and after trimming. As can be seen, the offset before trimming was reduced down to 1 mV and V_{sense} is approximately 750 mV for all process corners.

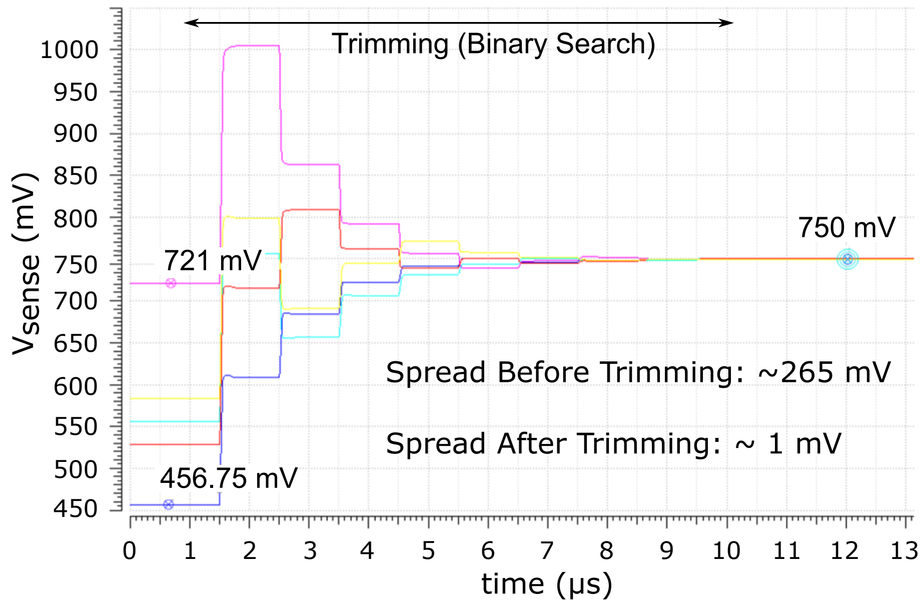

Figure 5.4: Functionality of trimming circuit over process corners: Nominal, Strong, Weak, SkewNP and SkewPN (simulation results).

AC-Analysis

After setting the operating point of the AFE, a small signal analysis can be performed to estimate the behavior of the system over supply voltage variation or power supply rejection ratio (PSRR). Since the sensor can be powered by a battery and the voltage can vary over a wide range, the PSRR should be higher than 90 dB. This requirement was set after discussions with system engineers of Texas Instruments.

As a first step we will consider the opamp-based V-I converter shown in Fig. 5.5. Since $R_{ref} << r_o$ of the PMOS transistors, we can neglect the output impedance r_o and give the following equations

$$\begin{aligned} V_{op} &= A \cdot (V_{FB} - V_{ref}), \\ V_{GS} &= V_{op} - V_{DD}, \end{aligned} \tag{5.6}$$

where V_{op} is the output voltage of the opamp, A is the open loop gain, V_{FB} is the voltage across the reference resistors R_{ref} and V_{GS} being the gate-source voltage of the PMOS transistor.

The following equations express the dependence between the gain of the opamp A and the transconductance of the PMOS transitor g_m

$$\begin{aligned} V_{FB} - V_{DD} &= -R_{ref} \cdot g_m \cdot V_{GS}, \\ &= -R_{ref} \cdot g_m \cdot (V_{op} - V_{DD}), \\ &= -R_{ref} \cdot g_m \cdot A \cdot (V_{FB} - V_{ref}). \end{aligned} \tag{5.7}$$

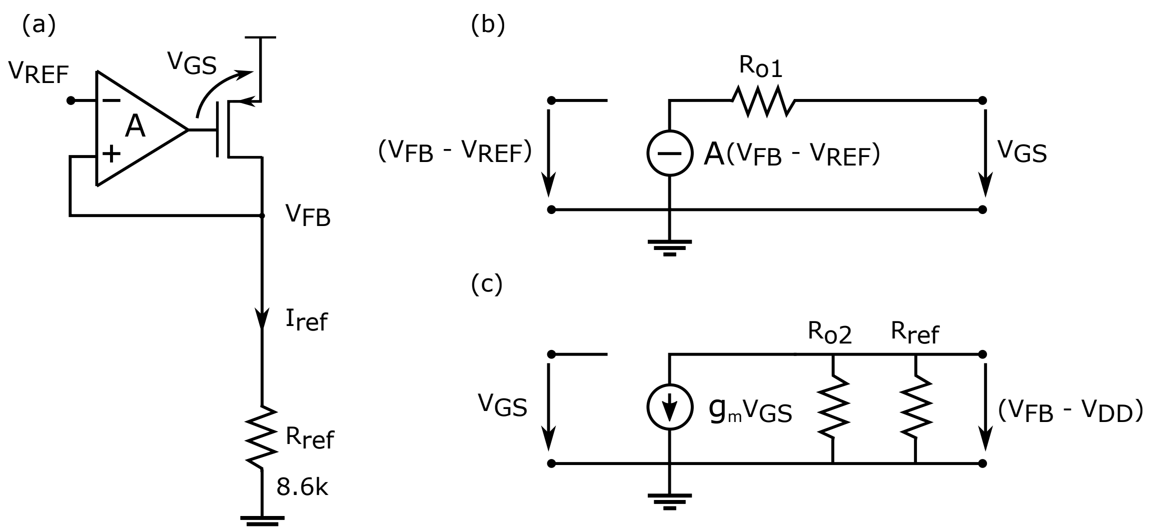

Figure 5.5: Representation of voltage to current converter: a) simplified schematic, b) small signal equivalent circuit of opamp and c) small signal equivalent circuit of output stage with PMOS transistor and reference resistor.

In small signal analysis, all constant voltages can be considered as grounded and therefore the equation 5.7 simplifies to

$$\begin{aligned} V_{FB} - V_{DD} &= -R_{ref} \cdot g_m \cdot A \cdot V_{FB}, \\ V_{FB}(1 + g_m \cdot R_{ref} \cdot A) &= V_{DD}. \end{aligned} \tag{5.8}$$

From equation 5.8, we can derive the equation for PSRR of the system

$$\frac{\Delta V_{DD}}{\Delta V_{FB}} = (1 + g_m \cdot R_{ref} \cdot A). \tag{5.9}$$

From the equation above, we can see that higher PSRR can be achieved by increasing the g_m and the opamp gain A. In order to not disclose the confidential technology parameters of Texas Instruments process, we will assume that $g_m \cdot R_{ref}$ can be maximum 25 dB. From here, we can calculate the opamp gain that is required to achieve the PSRR of 90 dB, namely: $A > 65$ dB. With this specification we can chose a suitable topology for the opamp.

Topology Selection

A single stage differential amplifier has an advantage of design simplicity and there is no need for frequency compensation (single pole system). The drawback of the single stage opamp is a relatively low open loop gain (depending on technology, usualy < 50 dB). As a solution, telescopic cascode operational transconductance amplifiers (OTA) can be used to achieve higher gain by increasing the output impedance with cascode transistors. The problem with the telescopic OTA is the limited input and output voltage range. There are four transistors connected in series that should operate in saturation region and therefore require certain voltage conditions that limit the input and output range.

Therefore, a single-stage folded cascode OTA was selected as the final topology, shown in Fig. 5.6. By using the cascode transistors, a DC gain of ≈ 86 dB was achieved. The biasing network generates the required voltages for current mirrors and cascode transistors by utilizing the gate-source voltage of diode connected transistors. This approach allows to establish a robust operating poing over technology process variations.

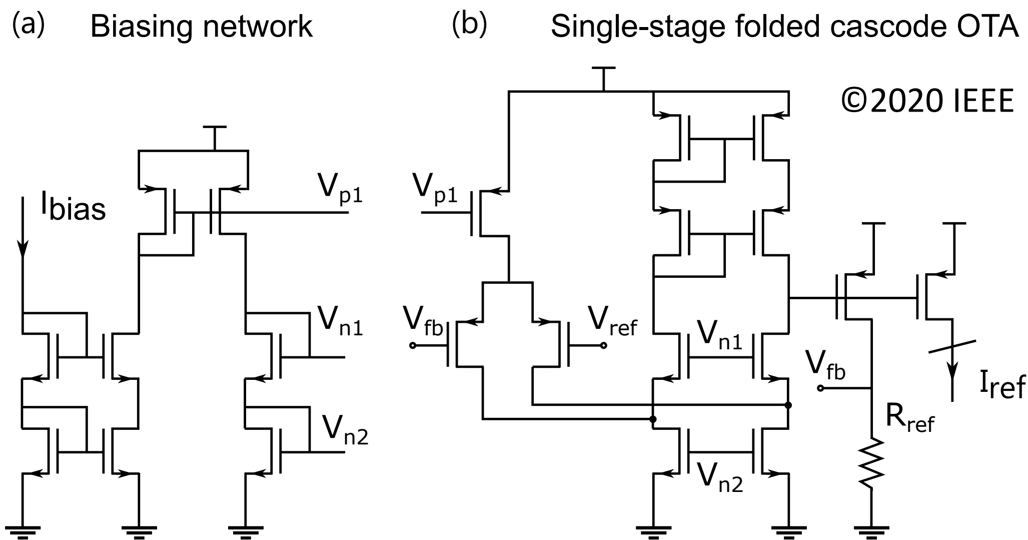

Figure 5.6: Transistor level implementation of analog front-end consisting of (a) biasing network, (b) one-stage folded cascode OTA.

Offset minimization

An offset voltage of an opamp results due to doping variations and non-idealities of a photomask during the IC fabrication. These non-idealities lead to mismatch between transistor pairs followed by asymmetric current flows and voltage drops. One can consider an opamp with offset as an ideal one with a voltage source connected in series at one of the input terminals. This voltage source is also called input referred offset voltage (commonly named as offset voltage). The offset voltage can vary over temperature and mechanical stress and thus corrupt the signal that needs to be measured.

To minimize the input referred offset voltage V_{off}, $g_{m,i}$ of the input differential pair was made large by increasing the width-to-length ratio (W/L) of the transistors. Also $g_{m,m}$ of current mirror transistors was made small by selecting larger length of transistors. The dependence between the offset voltage and the transconductances can be expressed as [46]

$$V_{off} \sim \frac{g_{m,m}}{g_{m,i}} \tag{5.10}$$

Noise Considerations

Noise is a random signal that cannot be predicted from its past values. There are different types of noise and for our system design we will consider the dominant types of noise, namely: white (thermal) and 1/f (flicker) noise.

There are different approaches for noise optimization on device as well as on system level. On system level, white noise can be reduced by using averaging techniques or filtering. The 1/f noise can be reduced by implementing modulation, chopping and auto-zeroing techniques [47]. Most of these techniques require higher bandwidth and therefore higher power consumption.

On device level, noise components can be optimized by properly sizing of transistors with highest noise contribution in the system. Similar to the offset voltage, the overall noise of the system can also be referred to its input. A simplified model of CMOS transistors for low and moderate frequencies can be given as [46]

$$V_{n,in}^2 = 4kT\gamma\frac{1}{g_m} + \frac{K}{WLC_{ox}} \cdot \frac{1}{f}, \tag{5.11}$$

with $V_{n,in}^2$ being input referred noise, γ bias- and technology-dependent coefficient (usually 2/3 for long-channel transistors) and K flicker noise coefficient. The first term of the equation is related with white noise of the effective channel resistance that depends on W/L ratio and can be reduced by increasing the g_m of the transistor. The second term represents 1/f noise and can be optimized by changing the overall size of the device W·L.

The mentioned methodologies for offset and noise reduction have been applied during the design of the folded-cascode OTA and also all the other system components. It should be mentioned that optimization of the noise on device level leads to a trade-off between offset, noise and the area of the final circuitry. As a main goal being, the small area and low power consumption, the transistor length and width have been kept smaller that 50 μm.

The frequency response of the folded-cascode OTA is shown in Fig. 5.7. As can be seen, the DC gain of $\approx$ 86 dB, unity gain frequency of $\approx$ 141 kHz and phase margin of $\approx$ 80° have been achieved.

Considering the AC analysis, due to the high gain of the OTA, the calculated PSRR of the AFE is higher than 110 dB.

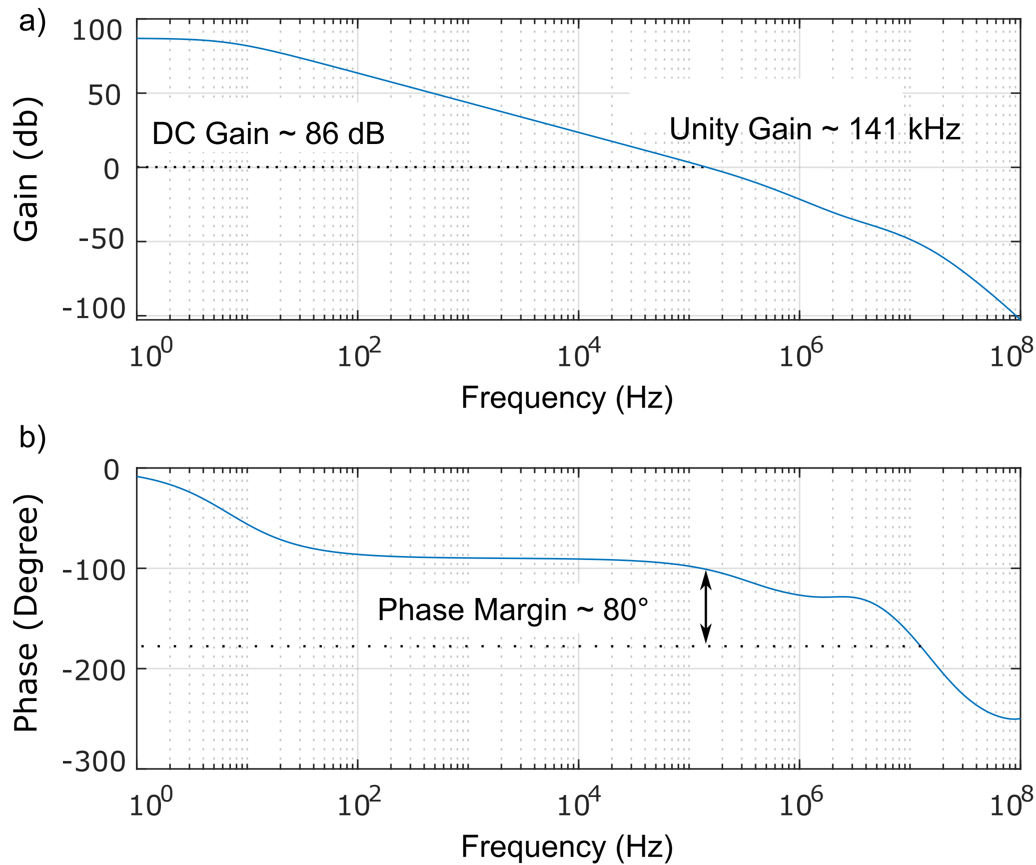

Figure 5.7: Bode plot of the implemented folded cascode OTA (simulation results): (a) Gain in dB over frequency and (b) Phase in degree over frequency.

5.3 Analog-to-Digital Converter

ADC Type Selection

An Analog-to-Digital Converter (ADC) can be seen as a bridge between analog and digital signal domains and is therefore one of the key system components that determines the system resolution, accuracy and speed (bandwidth).

In general, there are two types of ADCs: sampling (or nyquist) and integrating (or oversampling) converters [48].

Sampling converters provide a digital level of an analog signal with a single sample. One of the simplest sampling converters is the flash ADC that mainly consists of a resistive reference circuit and comparators for each voltage level. Once the amplitude of an input signal reaches a reference voltage, the comparator switches its output from "LOW" to "HIGH". A flash ADC requires 2^n - 1 comparators for n-bit conversion, making it impractical (in terms of area and power consumption) for high precision applications.

The most commonly used type of sampling converter is Successive Approximation Register (SAR) ADC. The concept behind the SAR ADC is the binary search algo-

rithm that compares an input signal level with a digital output by utilizing a single comparator and a Digital-to-Analog Converter (DAC).

Integration or oversampling ADCs make use of a higher Oversampling Ratio (OSR) that allows to minimize the quantization error (noise) and thus, maximize the Signal-to-Noise Ratio (SNR).

The most commonly used representative of oversampling converters is a Sigma-Delta ($\Delta\Sigma$) ADC that utilizes noise shaping and oversampling to increase the SNR. We will discuss about a $\Delta\Sigma$ ADC (architecture and theory) in more detail in following sections.

Depending on the final application, designers have many options on how to select the most suitable ADC for certain specification sets. As shown in Fig. 5.8, the selection usually includes considerations about speed (sampling rate) and resolution of an analog signal that should be converted to digital domain.

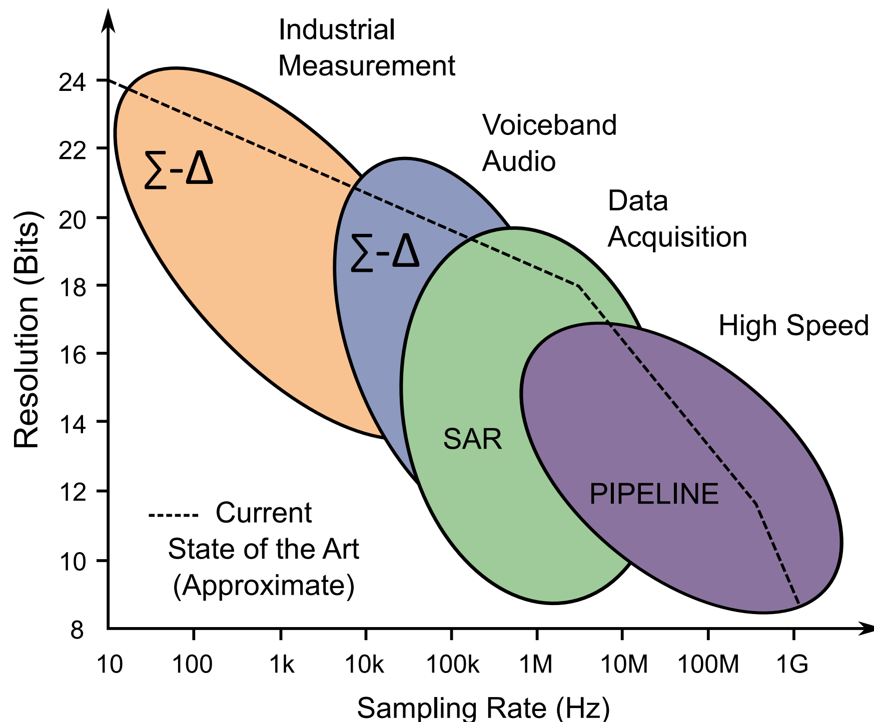

Figure 5.8: ADC architectures, applications, resolution, and sampling rates [49].

For low and moderate frequencies (up to $\approx$ 100 kHz), a $\Delta\Sigma$ ADC might be a suitable choice due to multiple advantages that will be discussed in the following subsections.

For the mechanical stress sensor in this work, a first order fully-differential $\Delta\Sigma$ Modulator with capacitive input mode was used. The $\Delta\Sigma$ ADC was provided by Texas Instruments and therefore we will describe general concepts without giving any specific parameters or specifications of the ADC due to confidentiality reasons.

Theory behind Sigma-Delta Modulator

To understand the working principle of $\Delta\Sigma$ Modulator, we need to consider two fundamental concepts: oversampling and noise shaping. These concepts can be applied not only in ADCs but also in DACs.

First, we will consider an ADC without oversampling, as shown in Fig. 5.9(a). In this scenario, a sine wave signal with a certain frequency is applied at the input of the ADC. The ADC samples the signal with a frequency f_s that should be at least two times higher than the frequency of the input signal (sine wave). This conditions originates from Nyquist-Shannon sampling theorem that is a fundamental bridge between continuous-time and discrete-time signals. According to the theorem, a finite continuous time signal can be reconstructed if the condition of sampling rate (sampling frequency) is fulfilled.

Every real ADC has a finite number of bits or digital states that determine the resolution of the ADC. After converting an analog signal with infinite number of analog states, the output signal of the ADC contains a so called quantization noise that can be seen as information loss in digital domain. The power spectrum of the input signal and the quantization noise are shown in Fig. 5.9(b).

The quantization noise is assumed to have constant average noise power floor or with other word being white noise. This common assumption of the quantization noise being independent of frequency is only approximately exact, because of some correlation between the input signal and the quantization error. Especially, the periodic signals can generate periodic quantization noise. However, this assumption is suitable and commonly used for approximation of the SNR of an oversampling converter [50].

The height of the average of the quantization noise power can be give as [50]

$$k_x = (\frac{\Delta}{\sqrt{12}}) \cdot \sqrt{\frac{1}{f_s}}, \tag{5.12}$$

with Δ being 1 LSB or one step between two subsequent quantization values. Therefore, the noise power of quantization noise P_e can be calculated as follows

$$P_e = \int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} S_e^2(f)\ df = \int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} k_x^2(f)\ df = k_x^2 f_s = \frac{\Delta^2}{12}. \tag{5.13}$$

The power of a sine wave signal with maximum amplitude equals to

$$P_s = \left(\frac{\Delta \cdot 2^N}{2\sqrt{2}}\right)^2 = \frac{\Delta^2 \cdot 2^N}{4}. \tag{5.14}$$

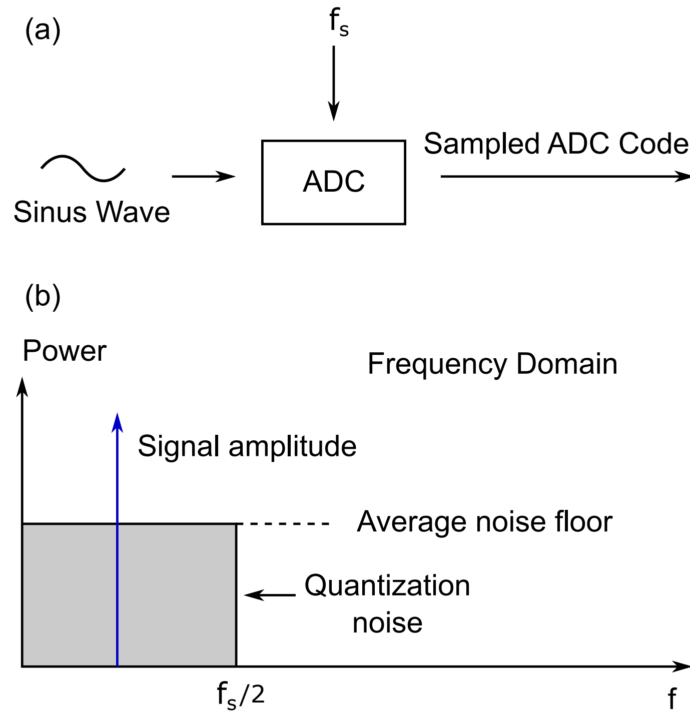

Figure 5.9: Nyquist mode ADC: (a) Block diagram of sampling procedure, (b) frequency spectrum of the sampled signal and quantization noise.

For a sine wave input signal, the maximum SNR depending on number of ADC bits N can be calculated as

$$SNR = 10 \cdot lg\left(\frac{P_s}{P_e}\right) = 10 \cdot log\left(2^{2N} \cdot \frac{3}{2}\right) = (6.02N + 1.76)\ \text{dB}. \qquad (5.15)$$

If the input signal is being oversampled with the resulting frequency of $OSR \times f_s$, k_x becomes lower by $\sqrt{OSR}$, as illustrated in Fig. 5.10. For a signal with a bandwidth f_0, the OSR is defined as

$$OSR = \frac{f_s}{2f_0}. \qquad (5.16)$$

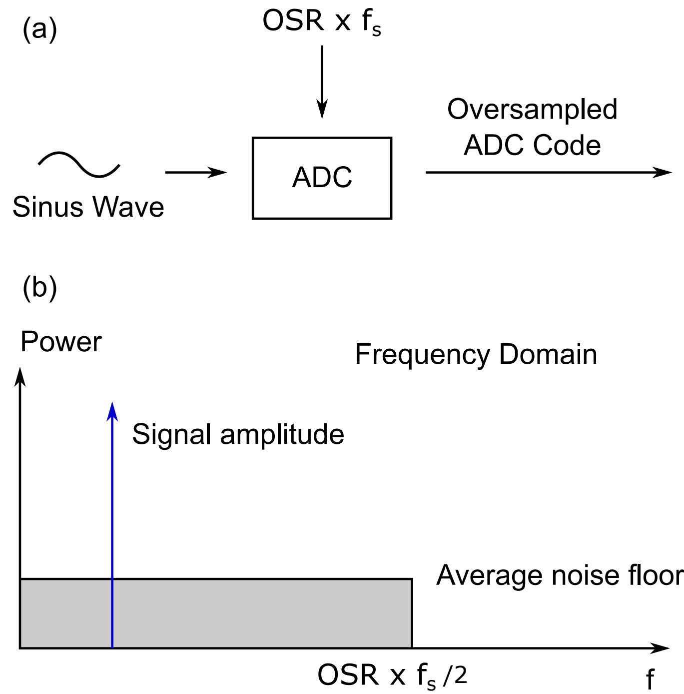

Figure 5.10: Oversampling mode ADC: (a) Block diagram of sampling procedure, (b) frequency spectrum of the sampled signal and quantization noise.

The oversampling itself doesn't improvement the SNR, since the noise power of quantization noise (area under the average noise floor) remains the same

$$P_e = \int_{-OSR\cdot\frac{f_s}{2}}^{OSR\cdot\frac{f_s}{2}} k_x^2(f)\ df = k_x^2 f_s \cdot OSR = \left((\frac{\Delta}{\sqrt{12}}) \sqrt{\frac{1}{OSR \cdot f_s}} \right)^2 f_s \cdot OSR = \frac{\Delta^2}{12}. \tag{5.17}$$

To improve the SNR, a digital low-pass filter with cutoff frequency f_c is used. A large part of quantization noise and other higher frequency undesired signals (for example coming from system clock) are filtered out after f_c. This is demonstrated in Fig. 5.11. If we set $f_c = f_s/2$, the SNR depending on the OSR can be derived as follows

$$P_e = \int_{-f_c}^{f_c} k_x^2(f)\ df = \int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} k_x^2(f)\ df = k_x^2 f_s = \left((\frac{\Delta}{\sqrt{12}}) \sqrt{\frac{1}{OSR \cdot f_s}} \right)^2 f_s = \frac{\Delta^2}{12} \frac{1}{OSR}, \tag{5.18}$$

$$SNR = 10 \cdot lg \left(\frac{P_s}{P_e} \right) = (6.02N + 1.76 + 10 \cdot lg(OSR))\ \text{dB}. \tag{5.19}$$

From the equation above, we can see that the SNR can be largely improved if the OSR is high enough. Every time the OSR increased by factor of 2, the SNR increases by 3 dB or equivalent 0.5 bits/octave.

As an example, if we need to improve the SNR by 60 dB, the OSR should be equal to 10^6. Such a high OSR requires very high sampling frequency compared to input signal bandwidth and therefore leads to higher power consumption.

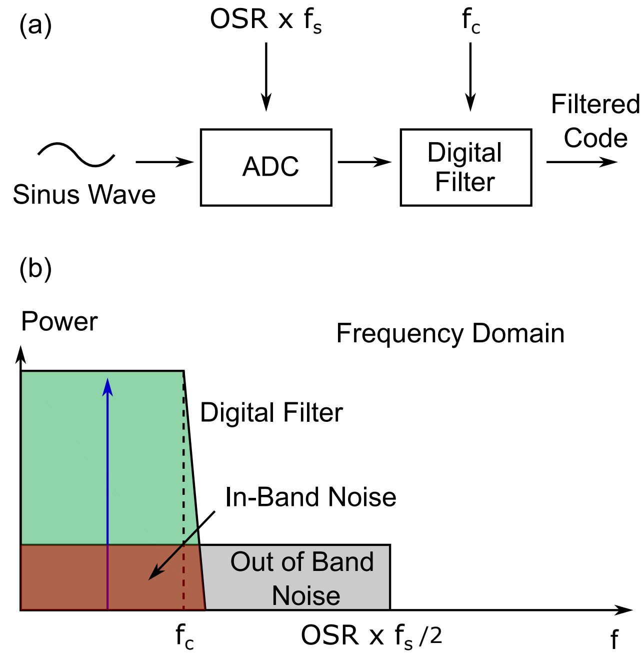

Figure 5.11: Oversampling mode ADC with digital filtering: (a) Block diagram of sampling procedure, (b) frequency spectrum of the sampled signal with in-band and out of band quantization noise.

A further improvement of the SNR can be achieved by using the oversampling with noise shaping concept. The idea behind noise shaping is to shift the in-band quantization noise to higher frequencies by performing low-pass filtering on the signal and high-pass filtering on the quantization noise. This is usually implemented with an integrator and a feedback loop. Depending on the order of the integrator, noise shaping can be more effective and therefore a higher SNR can be achieved. The disadvantage of the higher order modulators are increased system complexity due to required additional circuit components. A possible implementation of the architecture will be discussed in the following sections.

Oversampling with noise shaping of $\Delta\Sigma$ Modulator is shown in Fig. 5.12. The quantization noise power of the first order $\Delta\Sigma$ Modulator can be given as follows [50]

$$P_e = \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_0}{f_s}\right)^3 = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3. \tag{5.20}$$

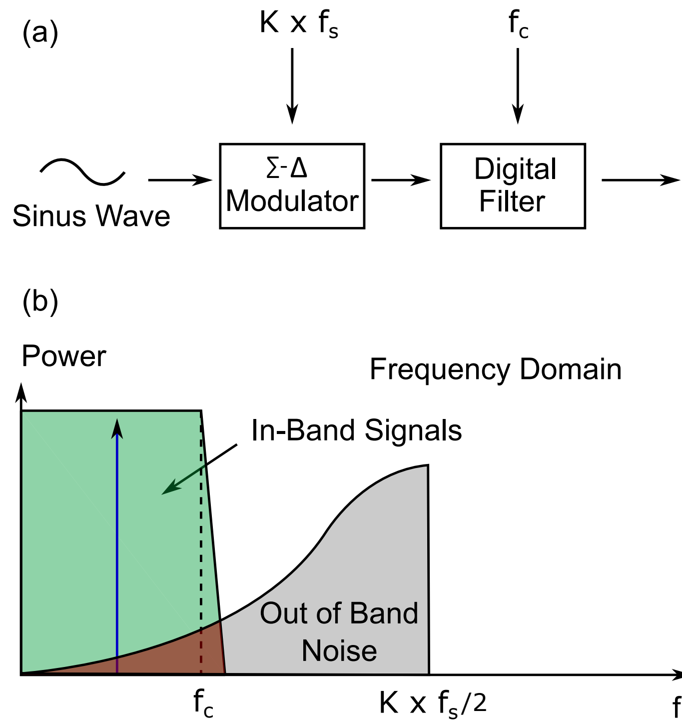

Figure 5.12: ΔΣ Modulator with digital filtering: (a) Block diagram of sampling procedure, (b) frequency spectrum of the sampled signal with in-band and out of band quantization noise.

The maximum SNR is now given by

$$SNR = 10 \cdot lg\left(\frac{P_s}{P_e}\right) = (6.02N + 1.76 - 5.17 + 30 \cdot lg(OSR))\text{ dB}. \tag{5.21}$$

The first-order noise shaping allows to improve the SNR by 9 dB, if the OSR is doubled, or gain an equivalent improvement of 1.5 bits/octave.

Sigma-Delta Architecture

A first-order ΔΣ Modulator with 1-bit quantizer (a single comparator) was used in the stress sensor system of this work. The use of 1-bit quatizer (N = 1) simplifies the circuit and also the requirement for linearity of the quantizer is not an issue. Fig. 5.13 shows a simplified block diagram of the ΔΣ Modulator that was provided by Texas Instruments.

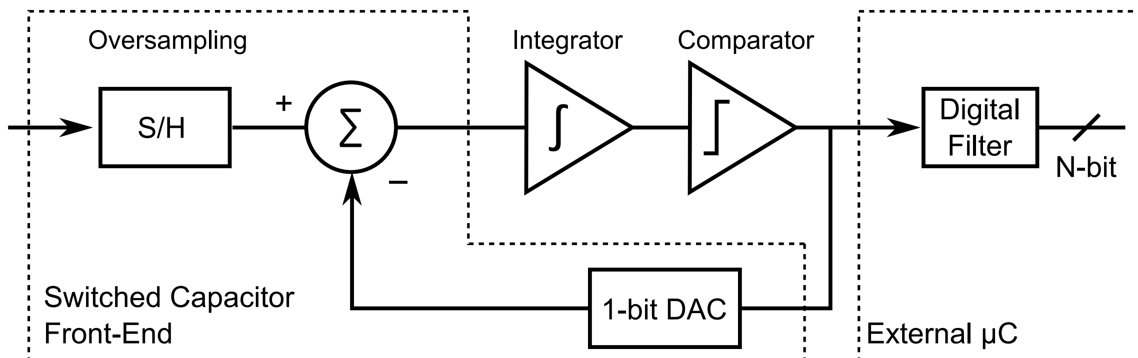

Figure 5.13: Simplified block diagram of SD-Modulator.

The front-end of the system is implement with switched capacitor circuits with digitally adjustable gain of 2x, 4x, 8x, 16x. With the adjustable gain, a small magnitude analog signal can be amplified and converted with high resolution of the modulator.

The $\Delta\Sigma$ Modulator has a fully-differential input that allows to convert positive and also negative mechanical stress values from negative to positive reference voltage V_{ADC_REF}. Also the capacitive input mode allows to sample an analog signal directly from the AFE of the stress sensor and perform summation and subtraction of the analog signals. Another advantage of the $\Delta\Sigma$ Modulator is: once the analog signal is sampled, the noise is mainly determined by kT/C ratio.

During the integration phase of the $\Delta\Sigma$ modulator, it was decided to perform all digital operations as filtering and decimation with an external microcontroller (μC). The use of an external μC gives several advantages as flexibility during testing and evaluation of stress measurements. For instance, the $\Delta\Sigma$ can be optimized for low frequency applications by increasing the number of samples (OSR) and changing the cut-off frequency of the digital filter without any modification of the system architecture.

The μC was also responsible for clock and digital control signal generation, for trimming, and adjusting of gain and selection of certain stress sensing elements. For these tasks a low power 16-bit MSP430 μC was used.

5.4 References

As it was discussed in previous sections, the AFE and the $\Delta\Sigma$ modulator require reference voltages and bias currents. Since all analog system signals are generated and rely on the accuracy of the reference signals, a suitable design and selection of reference blocks are decisive for overall accuracy and corresponding resolution of the sensor system.

Bandgap Voltage Reference

The reference voltages and currents should be ideally constant over temperature, humidity and in our case especially over mechanical stress. A bandgap voltage reference is usually used to generate the reference signals. Depending on the architecture and the order of compensation, bandgap references can have very low temperature dependence.

The temperature compensation is achieved by mixing two analog signals (can be voltages or currents) with a Proportional To Absolute Temperature behavior (PTAT) and a Complementary To Absolute Temperature behavior (CTAT). Bandgap references typically have a Temperature Coefficients (TCs) of 25 to 50 ppm/°C [51].

The CTAT signal is usually generated from a base-emitter voltage V_{BE} by applying a constant current to a diode connected bipolar transistor, as shown in Fig. 5.14(a). V_{BE} is given as follows

$$V_{BE} = \frac{kT}{q} \cdot ln(\frac{I_C}{I_S}), \tag{5.22}$$

with k being the Boltzmann constant, q the elementary charge, I_C collector and I_S saturation currents of a bipolar transistor.

The temperature dependence of V_{BE} can be approximated as [46]

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)\frac{kT}{q} - \frac{E_g}{q}}{T}, \tag{5.23}$$

where Eg ≈ 1.12 eV is the bandgap energy of silicon and m ≈ 2/3 is a parameter depending on the doping level. Fig. 5.14(b) illustrates temperature dependence of V_{BE} for three different currents (5μA, 50μA, 500μA). The slopes of the lines at the temperature of 300 K is ≈ -1.5 mV/K.

To achieve a temperature stable (constant) voltage at the output of a bandgap reference, a positive temperature dependent signal is needed. The PTAT can be generated by measuring the difference ΔV_{BE} between two base-emitter voltages of the bipolar transistors, as shown in Fig. 5.15(a). ΔV_{BE} can be given as follows

$$\begin{aligned} \Delta V_{BE} = V_{BE1} - V_{BE2} &= \frac{kT}{q} \cdot ln(\frac{nI_c}{I_s}) - \frac{kT}{q} \cdot ln(\frac{I_c}{I_s}) \\ &= \frac{kT}{q} ln(n), \end{aligned} \tag{5.24}$$

with n being the ratio between current of the left and right branches of Fig. 5.15(a). Also in Fig 5.15(b) is shown the behavior of ΔV_{BE} over temperature for four different ratios n = 25, 50, 75, 100.

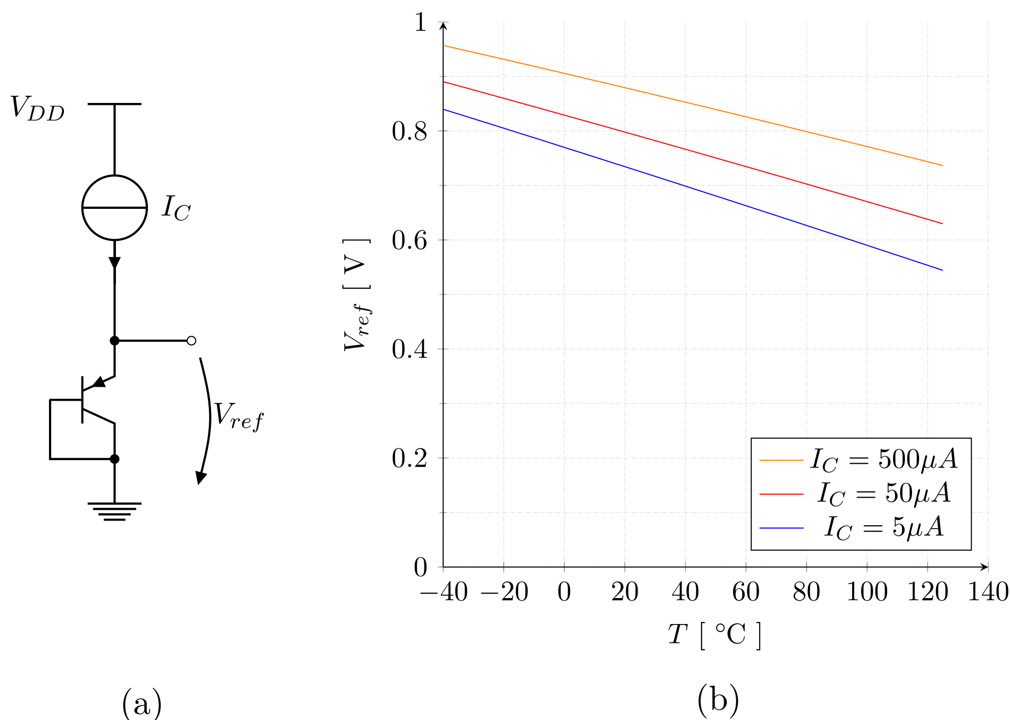

Figure 5.14: CTAT signal for a bandgap reference: (a) circuit for V_{BE} generation and (b) V_{BE} over temperature behavior [52].

Now, the temperature stable reference voltage V_{ref} can be generated by combination of CTAT and PTAT signals with a proper scaled ratio n

$$V_{ref} = V_{BE} + \frac{kT}{q} \cdot ln(n). \tag{5.25}$$

In order to achieve a minimal temperature dependence of V_{ref}, the ratio n should be approximately 17 and therefore the resulting voltage is around 1.2 V. In conventional bandgap references, the ratio n is much smaller (usually < 10) for better marching performance and the minimization of temperature dependence is achieved by using a scale factor β:

$$V_{ref} = V_{BE} + \beta \cdot \frac{kT}{q} \cdot ln(n). \tag{5.26}$$

V_{BE} and ΔV_{BE} can be generated with both types of bipolar transistors: NPN and PNP types and both types are well suited for temperature compensation (PTAT + CTAT). However NPN transistors have higher mechanical stress dependence as their counterparts. In bipolar transistors, the saturation current I_S is the dominant stress dependent component and has direct impact on V_{BE}. In Fig. 5.16, the stress dependence of both bipolar transistor types are shown.

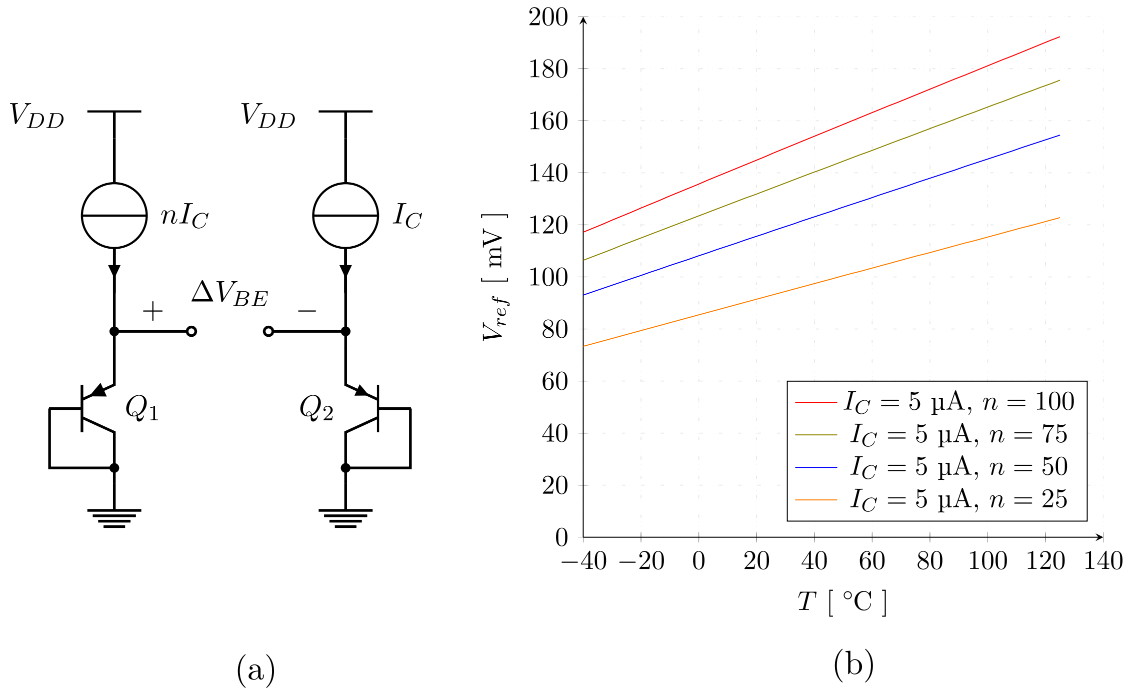

Figure 5.15: PTAT signal for a bandgap reference: (a) circuit for ΔV_{BE} generation and (b) ΔV_{BE} over temperature behavior [52].

The change of V_{BE} has only effect on the first term (CTAT components) of the equation 5.26. Since the generation of PTAT relies on ratio between the saturation currents I_S, the stress dependence of PTAT cancels out (first order).

Considering the points made above, to reduce the overall stress dependence of bandgap reference voltage V_{ref}, PNP type bipolar transistors are better choice.

In our system a standard Broakaw bandgap, built with PNP transistors was used. The bandgap reference has two output signals: V_{ref} with a temperature coefficient of 50 ppm/°C and a PTAT current source that was used as a biasing current for other circuit blocks.

To start up the bandgap reference, a Power On Reset (POR) circuit block is used that ensures that the systems begins its operation from a known state.

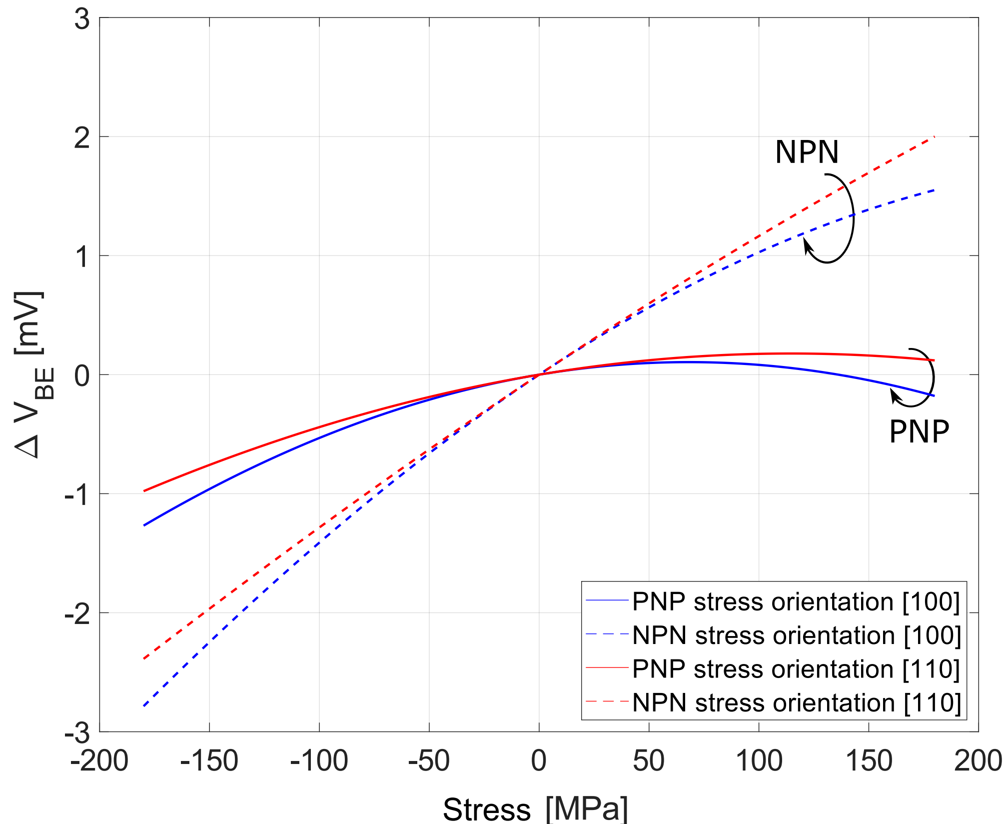

Figure 5.16: Mechanical stress dependence of PNP and NPN bipolar transistors for the crystallographic directions [100] and [110] [15].

Voltage Divider

As it was discussed in previous chapters, the AFE and the ΔΣ Modulator require different reference voltage levels. To generate the required voltages, a voltage divider shown in Fig. 5.17 was implemented. Since the output of the bandgap reference has a very high output impedance and therefore cannot be directly connected to the resistors, an opamp-based voltage follower was used.

The opamp has a high input and low output impedance, acting as a buffer between the bandgap reference and the resistor string. The resistor values were optimized to get minimal noise and simultaneously low power consumption by reducing the current flowing through the resistors.

Voltage Buffers

The ΔΣ Modulator requires two reference voltages: V_{ADC} and V_{buf} that are connected to the switched capacitor circuit (sample and hold). It means that during the sampling one of the reference voltages, the others are directly affected (cross sensitivity), causing a disturbance of the sampled signals. To reduce the cross sensitivity, additional opamp-based buffers with decoupling capacitors are used. The

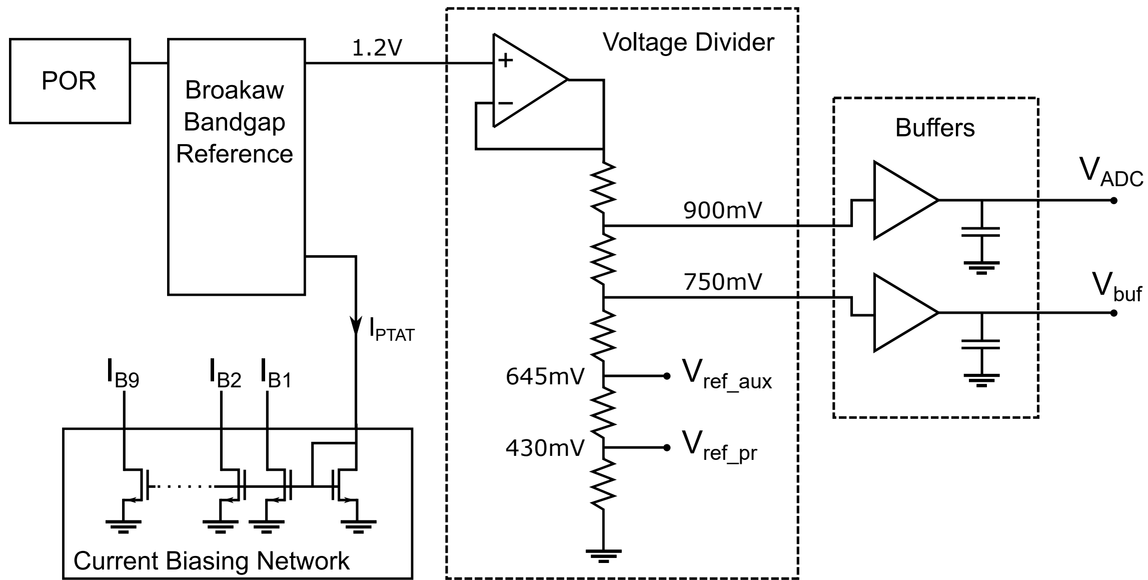

Figure 5.17: Reference circuit blocks and a biasing network for the stress sensor system. Illustrated buffers are needed to reduce the cross sensitivity caused by the sample and hold circuit of the ΔΣ Modulator.

main specification for the buffers is sufficient slew rate so that the reference voltages are settled before the next sampling phase.

The reference voltages for the AFE V_{ref_aux} and V_{ref_pr} are connected to the high impedance input of the OTA (MOSFET-based differential input pair), shown in Fig. 5.2 and therefore, additional buffers are not needed.

Biasing Network

Many of the circuit blocks (as opamps, comparators, buffers) require a biasing current to establish a stable operating point. For this task, the PTAT current I_{PTAT}, generated by the bandgap reference is used. I_{PTAT} partially compensates the CTAT behavior of the threshold voltage V_{th} of CMOS transistors and therefore, leads to more stable operating point.

The output device of the bandgap reference that provides I_{PTAT} is a PMOS device and hence, a NMOS current mirror is used to distribute the biasing currents.

5.5 Temperature Sensor

The temperature sensor in our sensor system is designed to separate the temperature dependence of the stress sensing elements (discussed in Chapter 4) from mechanical stress. Since the sensing elements are implemented with n-well resistors that exhibit relatively high temperature dependence, the analog temperature compensation with the reference resistor R_{ref} might be not sufficient. Thus, the temperature sensor can be used to measure the on-chip temperature and compensate the undesired dependence in the digital domain.

For this task, a PTAT voltage ΔV_{BE} is generated by using PNP bipolar transistors, as it was discussed in the section above. A current mirror with the ratio $n = 1 : 8$ is used to bias the bipolar transistors and generate the stress independent (first order) voltage ΔV_{BE}.

ΔV_{BE} is applied to the input of the $\Delta\Sigma$ Modulator through the multiplexer MUX1 that allows to switch between the temperature and the stress sensor, as shown in Fig. 5.18.

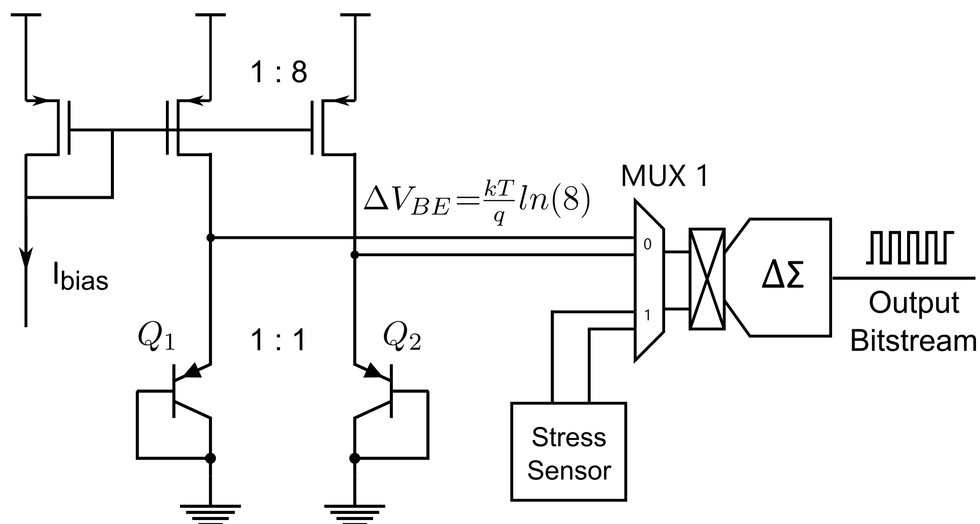

Figure 5.18: Simplified schematic of the temperature sensor implemented with PNP bipolar transistors. The PTAT voltage ΔV_{BE} is in first order stress independent due to cancellation of saturation currents I_S.

The adjustable gain of the $\Delta\Sigma$ Modulator allows to amplify the sensing voltage and achieve a higher resolution by utilizing the wider dynamic range of the ADC. The temperature compensation of the system will be discussed in Chapter 6.

5.6 Multiplexers

The current and voltage multiplexers are designed to have minimal stress contribution in the signal path, noting that stress only appreciably impacts the on-resistance of these devices. Transmission gates are used for selection of signals between the temperature and the stress sensor, as shown in Fig. 5.19(a). The transmission-gate devices only impact the charging time-constant with respect to the effective sampling capacitance of the following ΔΣ modulator stage. To minimize the on-resistance of NMOS and PMOS transistors, the W/L ratio was maximized by using the minimum L and large W with several transistor fingers and multipliers.

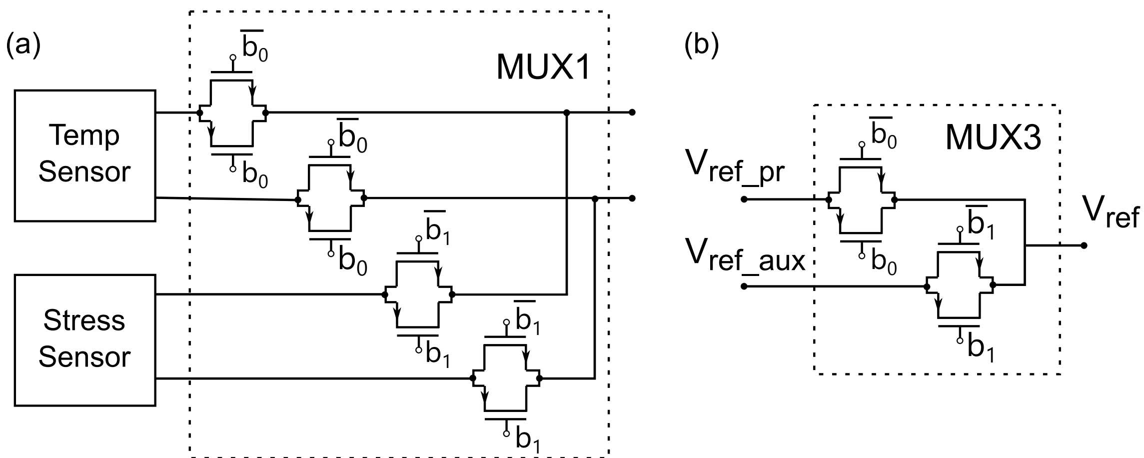

Figure 5.19: Multiplexer implementation of the stress sensor system for selection of: (a) the temperature or the stress sensor and (b) the reference voltages V_{ref_pr} and V_{ref_aux}.

Similarly, the multiplexer for selecting between V_{ref_pr} and V_{ref_aux}, shown in Fig. 5.19 (b) is realized with transmission gates. Since the output of MUX3 is connected to the input of the OTA with high input impedance, there is no high constant current flowing trough the transmission gate devices. Still, the on-resistance of the transistors has to be minimized to reduce white noise.

For selection between the sensing resistors (e.g. R_{xx} and R_{yy}), the reference current I_{ref} has to be redirected to the desired sensing resistor. For this purpose, PMOS transistors are used as shown in Fig. 5.20. To pass the current to a sensing resistor (e.g. R_{xx}), only one PMOS is active (b_0 has to be "LOW") and the other transistors are turned off. The current reaching R_{xx}, etc. is not a function of the PMOS switch on-resistance and V_{sense} is then sampled via MUX2 in a sequential manner and digitized by the ΔΣ modulator.

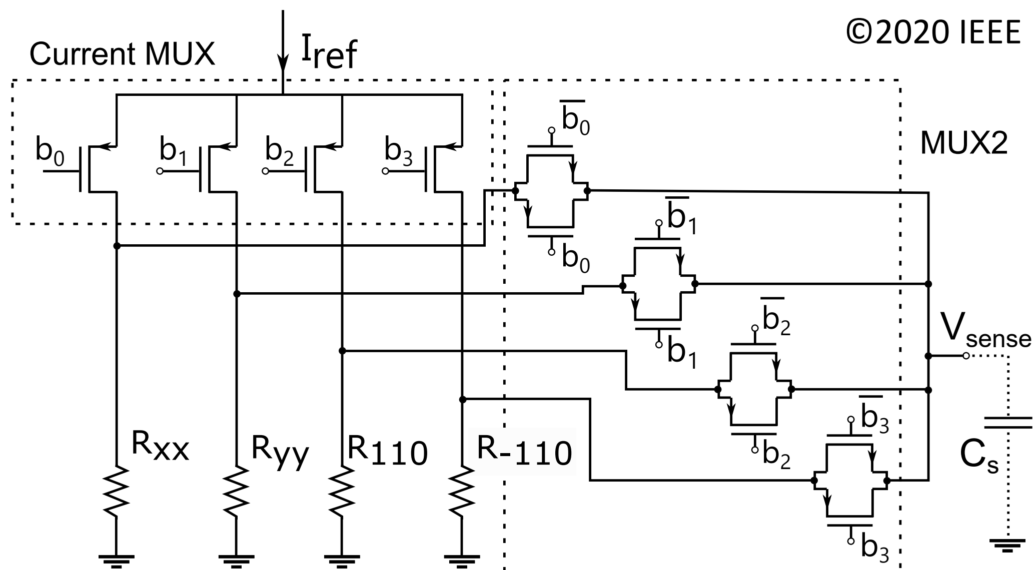

Figure 5.20: Multiplexer implementation of the stress sensor system for selection of a sensing element.

5.7 Interface to Microcontroller

As it was mentioned in previous sections, an external 16-bit ultra low power μC was utilized to provide digital control signals, e.g. for trimming of V_{sense} and for selection of the stress or the temperature sensor. Also the μC was used to perform digital signal conditioning of the bitstream generated by the $\Delta\Sigma$ Modulator.

Since the sensor system requires around 50 control signals for multiplexers, trimming the bandgap and current reference etc., a Serial Input Parallel Output (SIPO) circuit block was necessary. Therefore, a shift register with capture and hold mode was designed by using master-slave flipflops.

The architecture of the shift register is shown in Fig. 5.21 and has following input and output digital signals:

- DIN for serial input data.
- SCLK for input clock.
- BIT0, BIT1, etc. output bits.
- CLRZ for clearing the output bits of the shift register and starting from a known state (should be triggered at the beginning of an initialization).
- CCLK allows to keep the output bits stable until the next DIN is shifted (should be triggered at the end of an initialization).

The initialization of the shift register with following stress sensing is shown in Fig. 5.22. The control signals for the shift register are generated by the μC. After initialization, the $\Delta\Sigma$ modulator provides bitstream that is captured and processed by the μC.

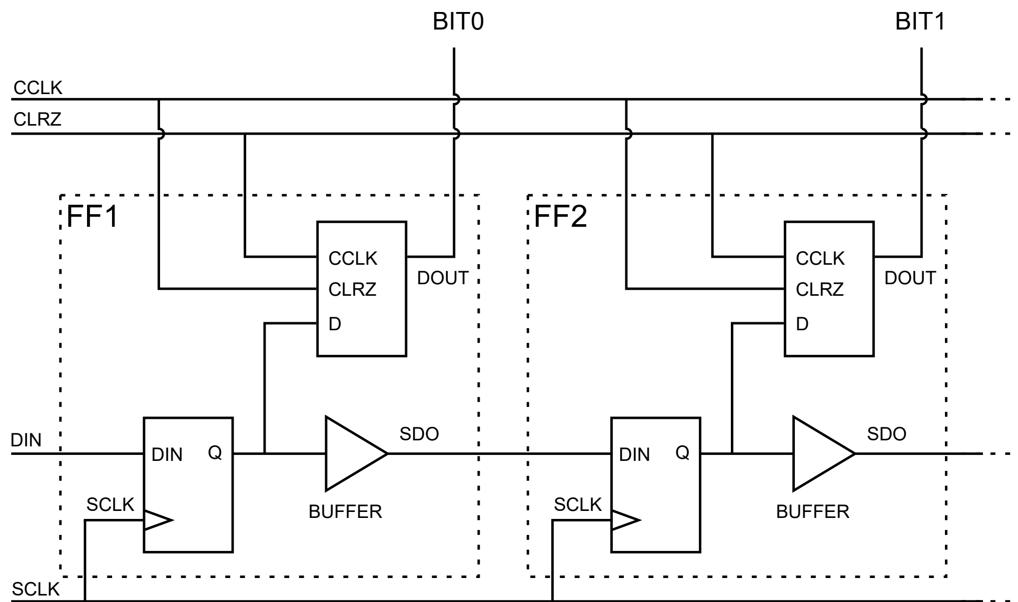

Figure 5.21: Shift register with capture and hold mode for generation of digital control bits to the stress sensor system.

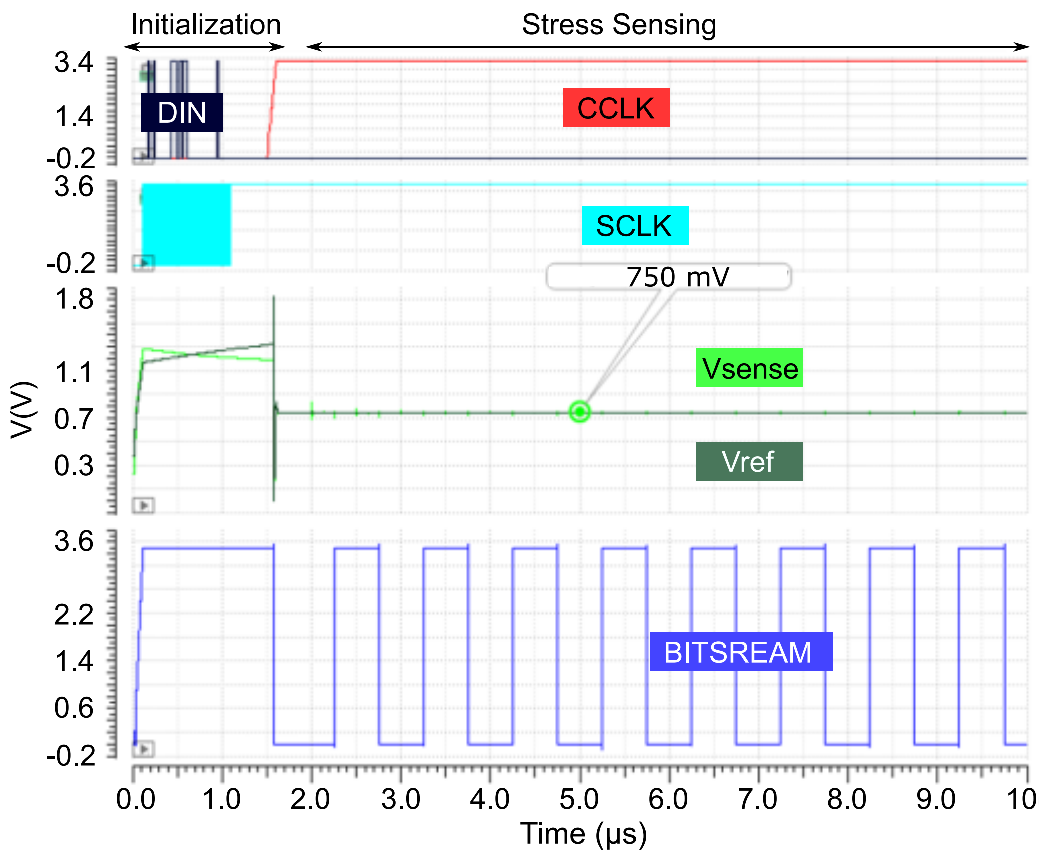

Figure 5.22: Transient simulation of the shift register input signals with output bitstream of the $\Delta\Sigma$ modulator.

5.8 Complete Sensor System

After verification of individual components in Cadence Analog Design Environment, they were integrated into the sensor system with the sensing and reference elements. Multiple simulations were performed to evaluate the system functionality under different temperature, process and mismatch conditions.

A simplified schematic of the readout electronics with the stress sensors for the temperature compensated stress measurement system is illustrated in Fig. 5.23.

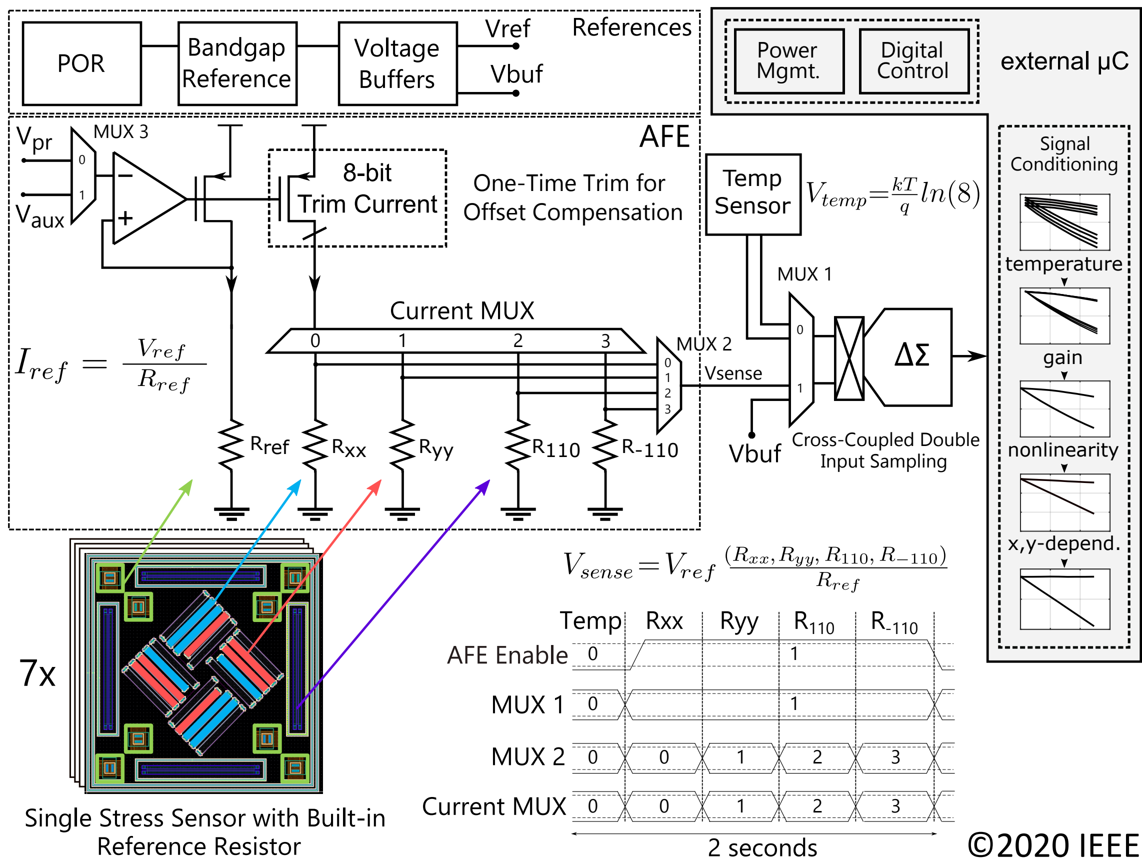

Figure 5.23: System overview: a simplified diagram of readout electronics and the resulting voltage at the output of AFE with corresponding sensing procedure.

The layout of the system was designed following standard layout rules to increase matching performance (e.g. interdigitated and common centriod layout techniques), also to minimize critical parasitic resistance (e.g. wire resistance to ground potential) and capacitance.

The analog ground was separated from the digital one to reduce the cross coupling effects caused by switching circuit blocks. A star-connected ground wiring was performed to the most sensitive circuit parts (e.g. stress sensing elements). The critical analog signals were shielded to reduce the coupling effects.

The complete system was fabricated on a 2 x 2 mm^2 130 nm standard CMOS test chip, the readout electronics taking 1.07 x 0.43 mm^2, with 7 distributed stress sensors

per die to determine the two-dimensional impact of stress gradients over and even beyond the chip area. The fabricated test chip is shown in Fig. 5.24.

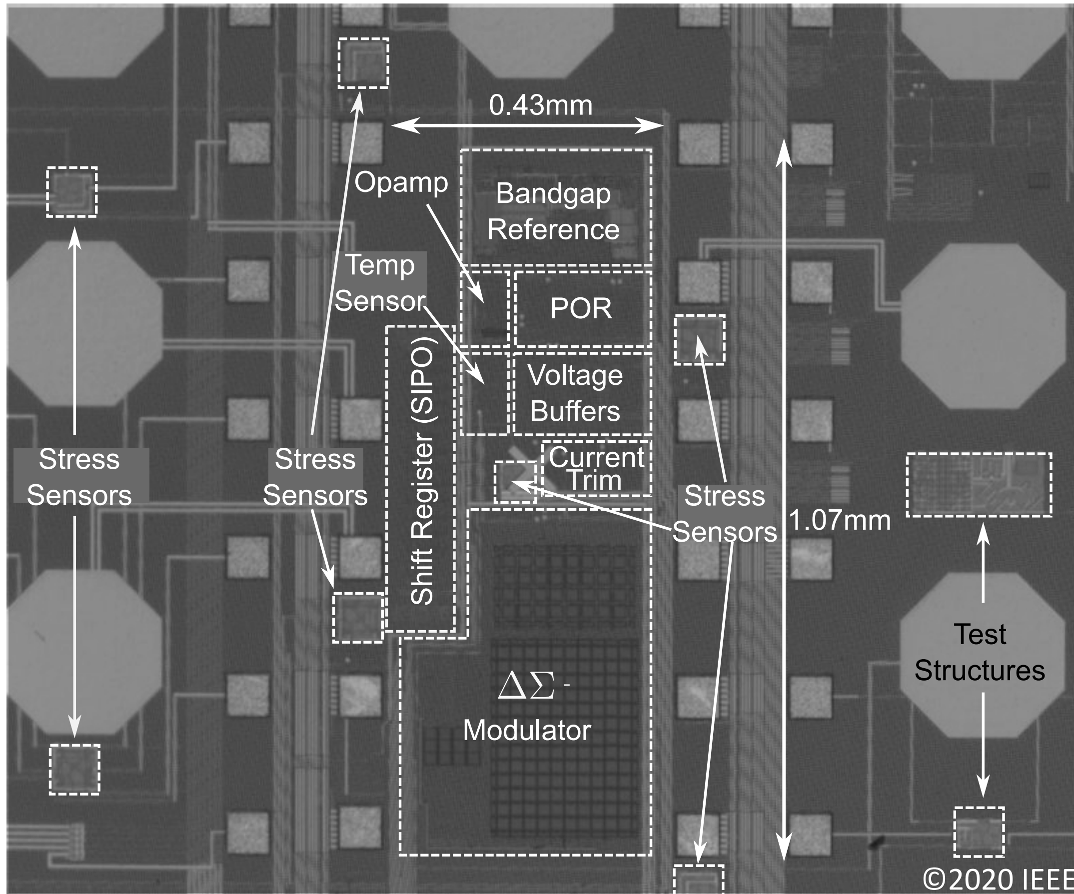

Figure 5.24: Micrograph of the test chip with seven distributed stress sensors and the complete readout electronics.

Chapter 6

Testing and Evaluation

This chapter gives an overview of experimental measurements that were performed to test and evaluate the performance of the stress sensor system regarding noise, mechanical stress sensitivity and temperature dependence.

During the testing, the external μC was connected to a computer via USB that allowed to control and capture digital signals and import them to Matlab for further evaluation. Some of the analog signals (e.g. bandgap reference voltage, AFE output voltage, system current consumption etc.) were observed directly with a Keithley Sourcemeter.

6.1 Noise Analysis

The main limitation of the system in terms of resolution is 1/f-noise resulting from internal references and other circuitry. This was determined through simulation of the simplified system during the design phase, as illustrated in the provided noise power-spectral density plot of Fig. 6.1 with a flicker-noise corner of approximately 10kHz but desired system operation from 0.5Hz to 7.5kHz.

This behavior was confirmed experimentally by evaluating the raw ADC output without applied stress and at constant temperature, as shown in Fig. 6.2 after removal of offset. In this case, 30720 samples were captured over a 2 second time interval ($f_s \approx$15.3kHz) and averaged to form a single measurement, of which 150 were taken for reasonable statistical confidence. The one-sigma variation is 47μV (compared to 25μV in simulation, within expected levels of deviation) which corresponds to a 175kPa stress level, which is essentially the resolution of the system.

It should be mentioned that noise/offset reduction techniques, such as chopping or autozeroing, could have been directly applied in the AFE. These techniques are known to increase system complexity and/or power consumption and, with energy-efficiency as a primary goal, were not implemented in this prototype.

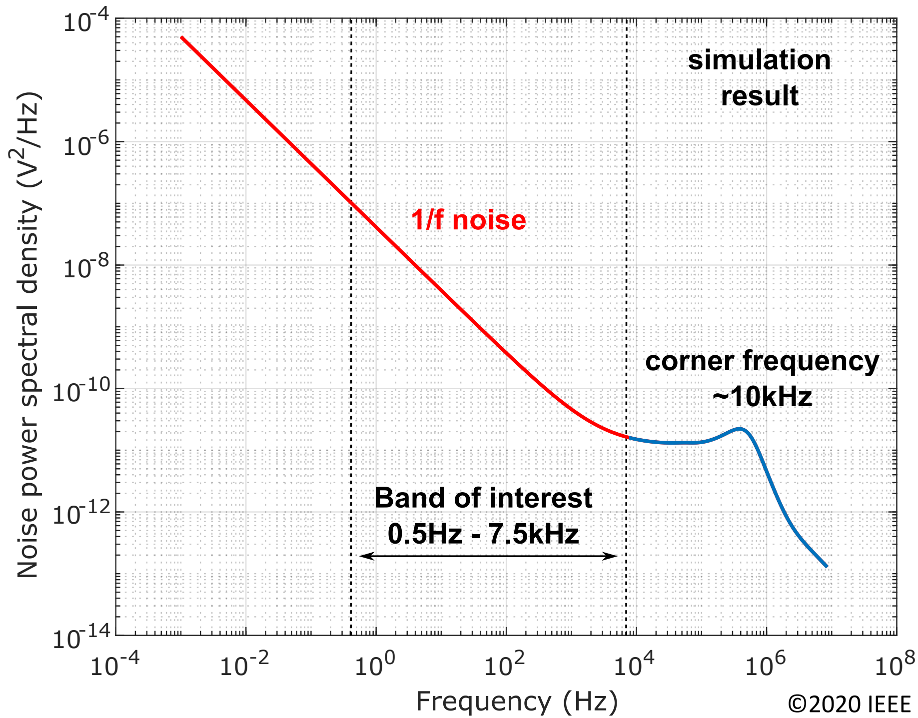

Figure 6.1: Simulated noise power spectral density of the simplified analog part of the system without ADC.

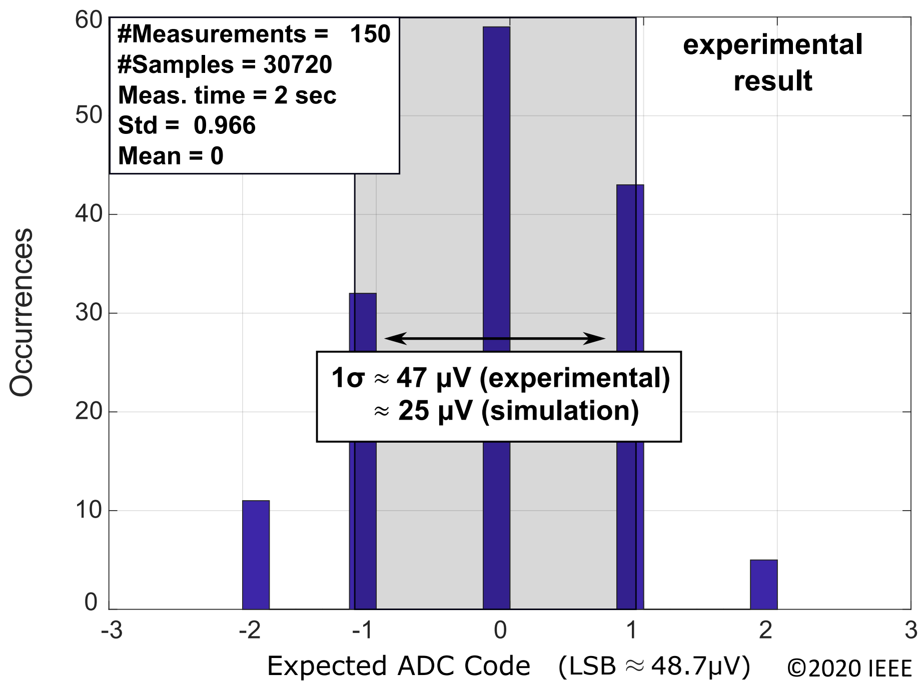

Figure 6.2: Histogram of the ADC Code at 0 stress with an interval of 2 seconds and 150 measurements of the complete system.

6.2 Mechanical Stress and Temperature Dependence

Since the system has an analog first order temperature compensation, additional digital-based temperature compensation doesn't require use of high accuracy temperature information, thus relaxing the specifications for the temperature sensor. During active sensing (2sec) the on-chip system components consume 203μA but are designed for duty-cycled applications, where all of the integrated components can be turned off. A single external 16-bit low-power microcontroller (μC) is used for flexibility of testing and combining the outputs of several such test-chips while also applying simple to implement but effective digital error correction schemes; a potential future on-chip integration of this digital functionality should require only well-established design techniques.

V_{sense} stress signals, even before digital correction, already exhibit a high sensitivity of approximately 30 mV/100 MPa with a low temperature dependence of approximately 165 μV/°C. To demonstrate system functionality, mechanical stress from 0 to 250 MPa was applied at four different temperatures (at 5°C, 30°C, 60°C, and 90°C) in x-direction. As can be seen in Fig. 6.3, before any digital compensation, V_{sense} contains unwanted y-sensitivity, a residual temperature dependent drift, and is non-linear.

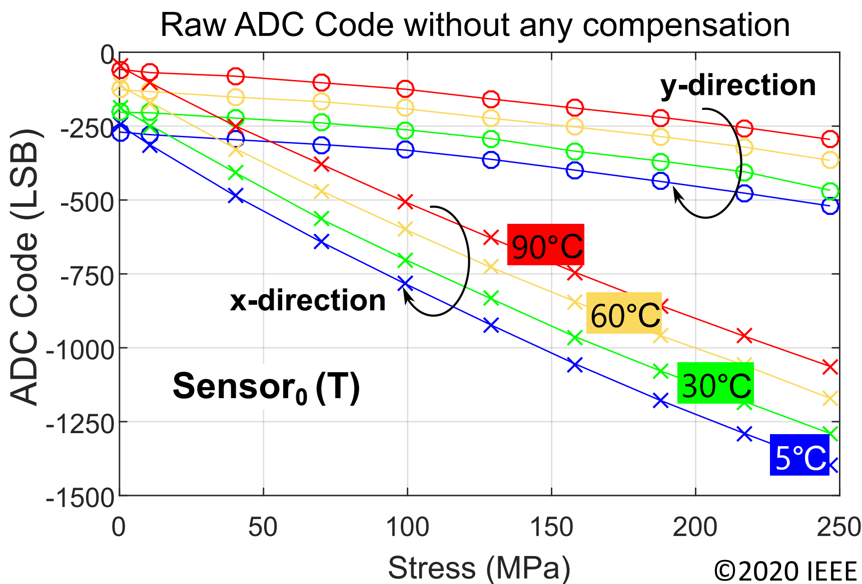

Figure 6.3: Measured ADC code of selected Sensor$_0$ without any compensation over mechanical stress at 5°C, 30°C, 60°C, 90°C.

To counteract all unwanted behaviors, three main forms of correction are to be applied, specifically: (1) offset as a function of temperature, (2) stress sensitivity (or gain) as a function of temperature, and (3) stress sensitivity as a function of stress (non-linearity).

Temperature Dependent Offset Compensation

Digital correction, via the μC, begins by setting the 8-bit current trim such that the unstressed V_{sense} level is biased to 750 mV by choosing the nearest ADC code close to 0 LSB. The remaining non-zero ADC code represents residual offset V_{RES} and is to be corrected digitally. Additional temperature dependent offset $V_{OFF}(T)$ is then extracted using a two-point temperature measurement (also without stress) while utilizing the on-chip BJT temperature reference, as illustrated in Fig. 6.4, resulting in a simple temperature coefficient TC_O (slope of $V_{sense}(T)$).

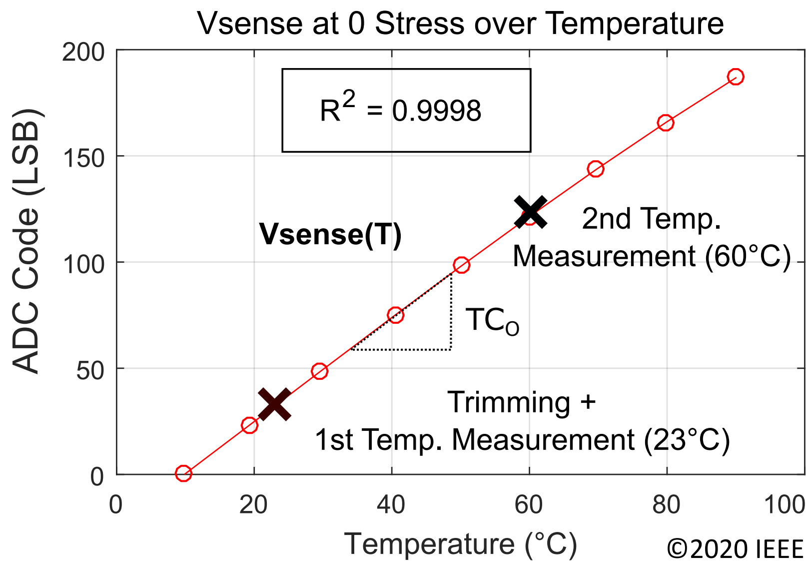

Figure 6.4: Measured ADC code of selected Sensor_0 without applied stress over temperature (residual temperature dependence).

The temperature dependence and residual offset after trimming of V_{sense} can be approximated, e.g. by a polynomial that allows to reproduce a certain value of V_{sense} for a corresponding temperature. The accuracy of the reproduced values depends on the degree of a polynomial (wider temperature ranges would require additional temperature measurements). In our case, V_{sense} exhibits almost a linear response in the temperature range from 5° C to 90° C. Therefore, a first order polynomial approximation was used

$$V_{OFF}(T) = TC_O \cdot (T - T_0) + V_{RES}, \tag{6.1}$$

with T_0 being the room temperature (23 °C). The reproduced value of $V_{OFF}(T)$ is subtracted from V_{sense}, resulting in a temperature compensated voltage V_{TCO}

$$V_{TCO} = V_{sense}(T) - V_{OFF}(T). \tag{6.2}$$

Temperature Dependent Sensitivity Compensation

After correcting for all offset sources (collectively representing the first form of correction), the raw curves from Fig. 6.3 appear as those in Fig. 6.5. Note that the offset correction values extracted from the x-curves were also directly applied to the y-curves. The unwanted y-sensitivity remains and a temperature dependent stress sensitivity is visible in the x-direction (the 4 curves at different temperatures have different slopes and thus different gains).

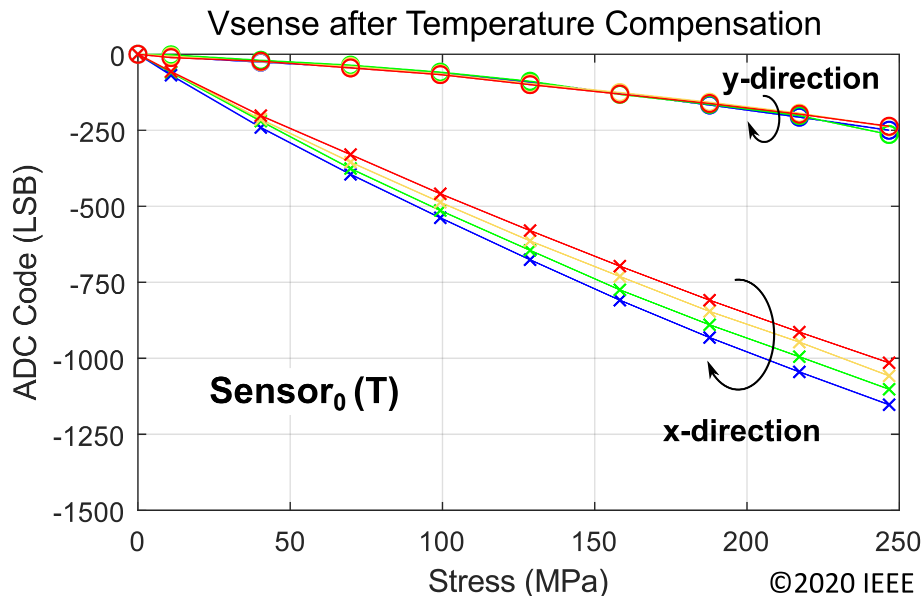

Figure 6.5: Compensated ADC Codes of selected Sensor$_0$ for temperature dependent offset TC_O (by using on-chip temperature sensor).

The sensitivity variation over temperature is end-point corrected by extracting the related error and applying a temperature dependent scale-factor TC_G (corrects gain as function of temperature). For this purpose, a second order polynomial with three gain coefficients GC_1, GC_2 and GC_3 was used due to a nonlinear behavior of the stress sensitivity over temperature (the gain coefficients were extracted with Matlab Curve Fitting Toolbox). The temperature dependence of TC_G can be expressed as

$$TC_G(T) = GC_1 \cdot (T - T_0)^2 + GC_2 \cdot (T - T_0) + GC_3. \tag{6.3}$$

Now, the temperature compensated voltage V_{TCO} is scaled by $TC_G(T)$

$$V_{TCG} = TC_G(T) \cdot V_{TCO}. \tag{6.4}$$

Once this (the second form of) correction is applied to the curves of Fig. 6.5, with this correction, all of which exhibit nearly identical over-stress behavior, as can be seen in Fig. 6.6.

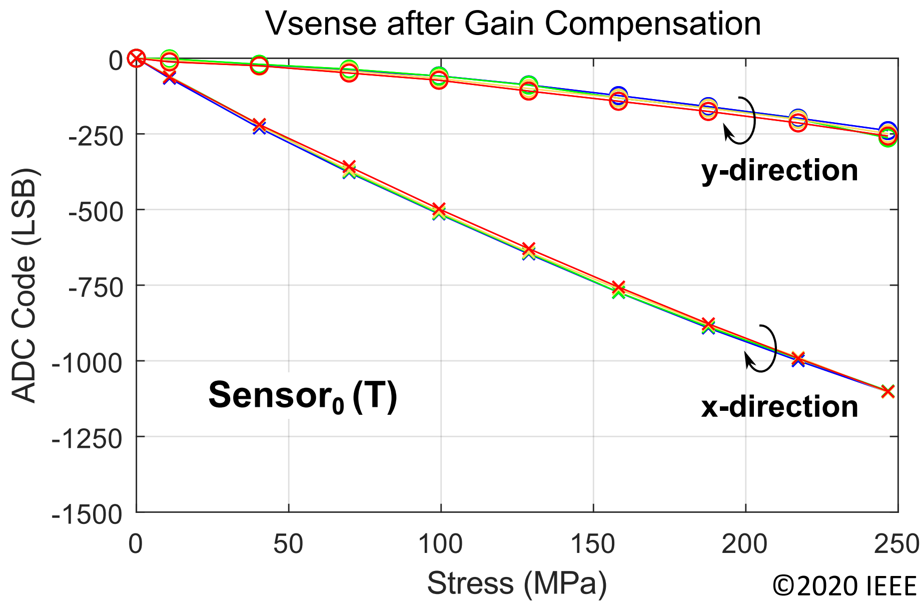

Figure 6.6: Compensated ADC Codes of selected Sensor_0 for temperature dependent offset TC_O and temperature dependent stress sensitivity TC_G.

Nonlinearity Compensation

All non-negligible remaining error is attributed to nonlinearity in R_{100} and R_{010} resistances, which is then extracted and corrected using two simple quadratic equations at one temperature (the third form of correction), one for x and one for y.

Depending on the stress value, the ratio R_{100}/R_{010} (needed for compensation of y-direction sensitivity) changes and this leads to x/y-leakage. The nonlinearity of both resistances are shown in Fig. 6.7.

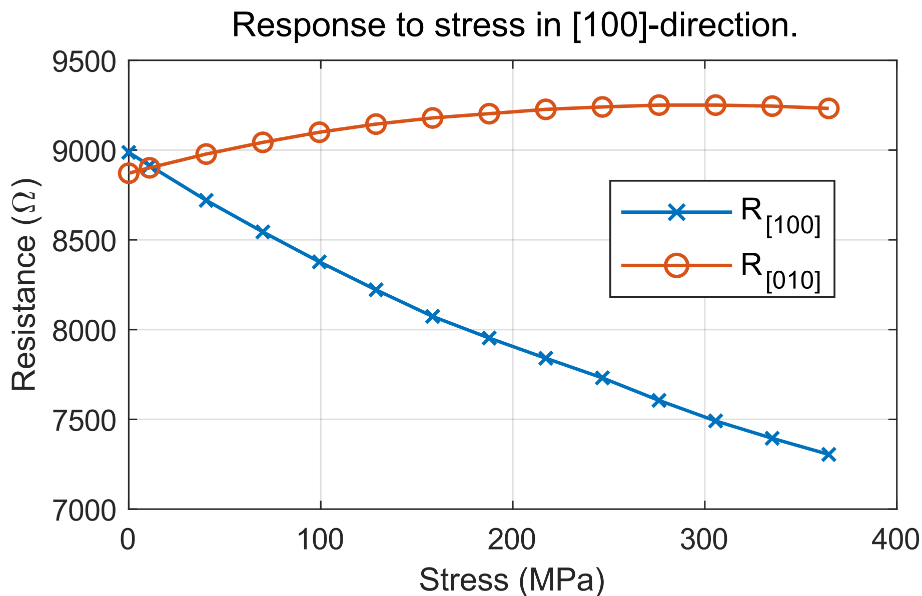

Figure 6.7: Response of n-well R_{100} and R_{010} resistances to the stress in [100]-direction from 0 to 360 MPa.

For compensation of the resulting nonlinearity of Sensor_0, the response of the x- and y-direction sensing elements were fitted with nonlinearity coefficients (NC) to ideal lines (x-fit and y-fit), as shown in Fig. 6.8.

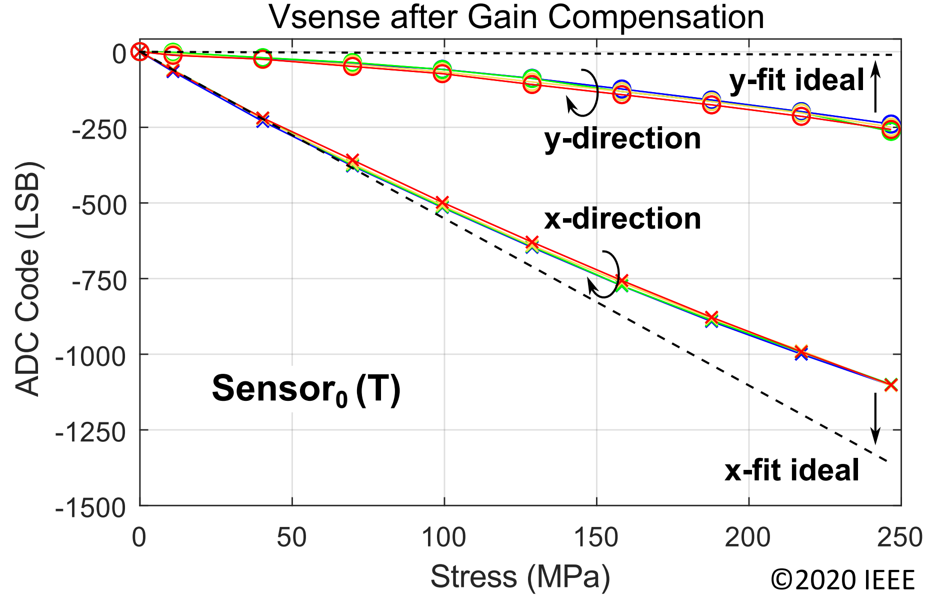

Figure 6.8: Compensated ADC Codes of selected Sensor_0 for temperature dependent offset TC_O and temperature dependent stress sensitivity TC_G with ideal response to x- and y-direction stress (dashed lines).

These extracted nonlinearity coefficients (NC) are referred to as NC_{1x} and NC_{2x} for R_{xx} (and NC_{1y} and NC_{2y} for R_{yy}). Hence, the compensated stress values $V_{NC}(\sigma_x)$ and $V_{NC}(\sigma_y)$ can be calculated as follows

$$\begin{aligned} V_{NC}(\sigma_x) &= \frac{-NC_{1x} - \sqrt{NC_{1x}^2 + 4 \cdot NC_{2x} \cdot \sigma_x}}{2 \cdot NC_{2x}}, \\ V_{NC}(\sigma_y) &= \frac{-NC_{1y} - \sqrt{NC_{1y}^2 + 4 \cdot NC_{2y} \cdot \sigma_y}}{2 \cdot NC_{2y}}. \end{aligned} \tag{6.5}$$

Note that σ_x and σ_y are the output signals from the sensing elements R_{xx} and R_{yy}. Also it should be mentioned that the nonlinearity coefficients (NC) are valid only if the stress is applied in x- or y-direction. For other stress angels, the coefficients have to be altered, since the nonlinearity also depends on angle of the applied stress. For this task, an angle and stress dependent nonlinearity coefficients can be extracted, similarly to the compensation method demonstrated above. In our sensor system, the angle dependent nonlinearity coefficients were not extracted, because the measurement setup was not available at the time of measurement.

The resulting corrected output vs. stress curves for the stress in x- and y-directions are shown in Fig. 6.9, exhibiting a nearly linear response and minimal deviation over temperature.

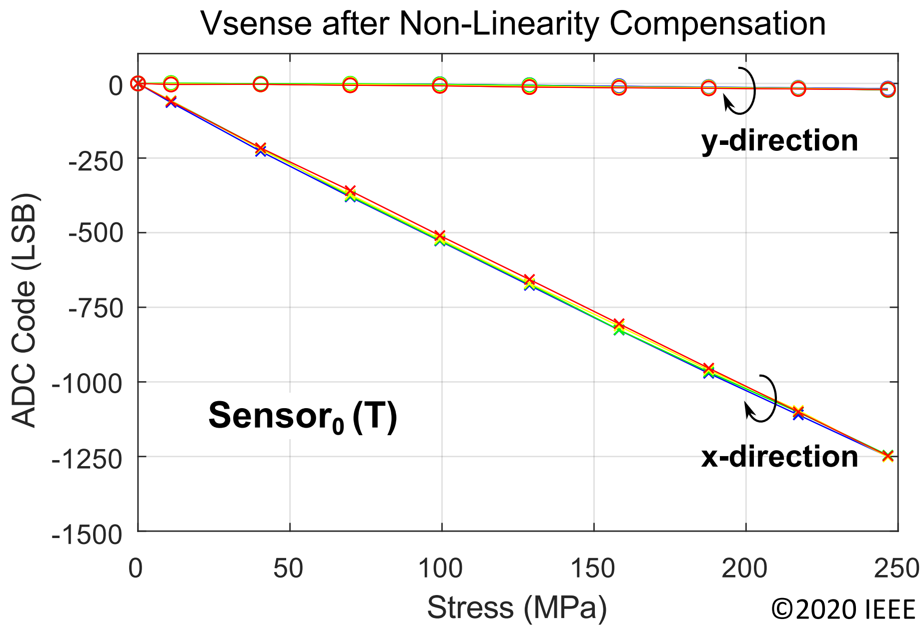

Figure 6.9: Compensated ADC Codes of selected Sensor$_0$ for temperature dependent offset TC_O, temperature dependent stress sensitivity TC_G and non-linearities NCs in x- and y-directions.

6.3 Validation

To support the validity of the trimming and compensation methodologies, Fig. 6.10 shows post-corrected results for 3 sensors (from two different wafers) overlaid and for a wider range of applied tensile stress levels, up to 360 MPa.

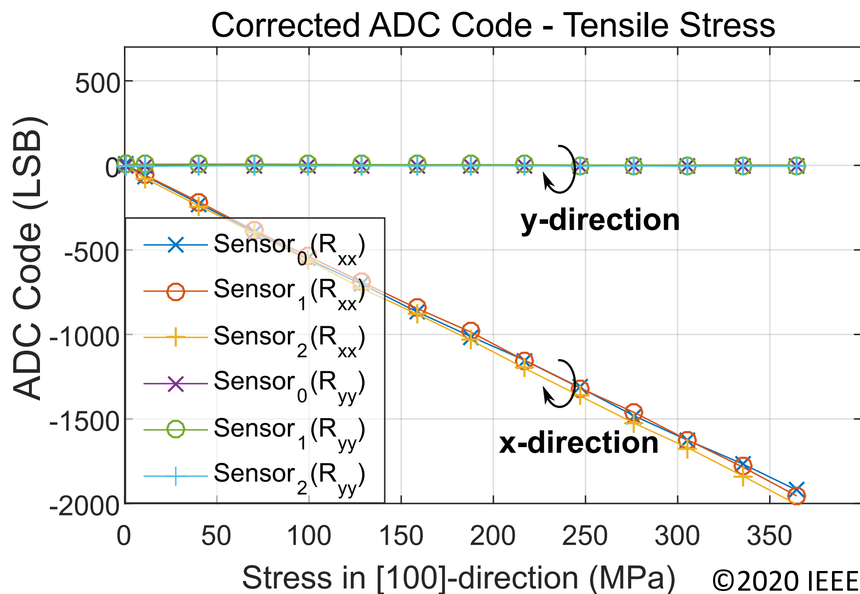

Figure 6.10: Compensated ADC Codes of Sensor$_0$, Sensor$_1$ and Sensor$_2$ (from different wafer) for extended tensile stress range.

Provided in Fig. 6.11 is a similar set of measurements for compressive stress, for up to -100MPa. $Sensor_0$ and $Sensor_1$ are two sensors from different locations on the same die and $Sensor_2$ from a completely different wafer and also at a different location on a die; in all cases post-corrected results are alike.

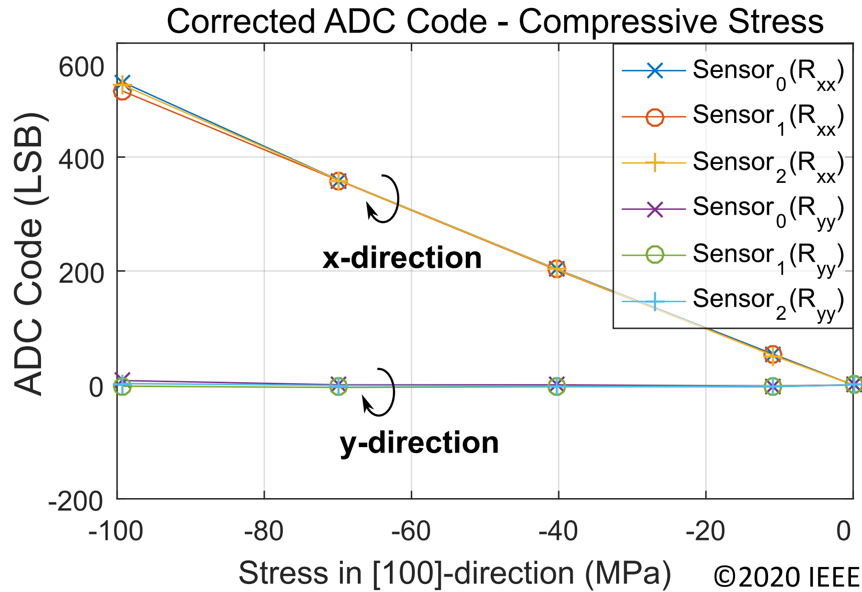

Figure 6.11: Compensated ADC Codes of $Sensor_0$, $Sensor_1$ and $Sensor_2$ (from different wafer) for compressive stress.

For mechanical stress applied in the [110] and [-110] directions, where quadrant is otherwise ambiguous, Fig. 6.12 and Fig. 6.13 show the post-corrected responses of primary and auxiliary (no need for correction) sensing elements, respectively.

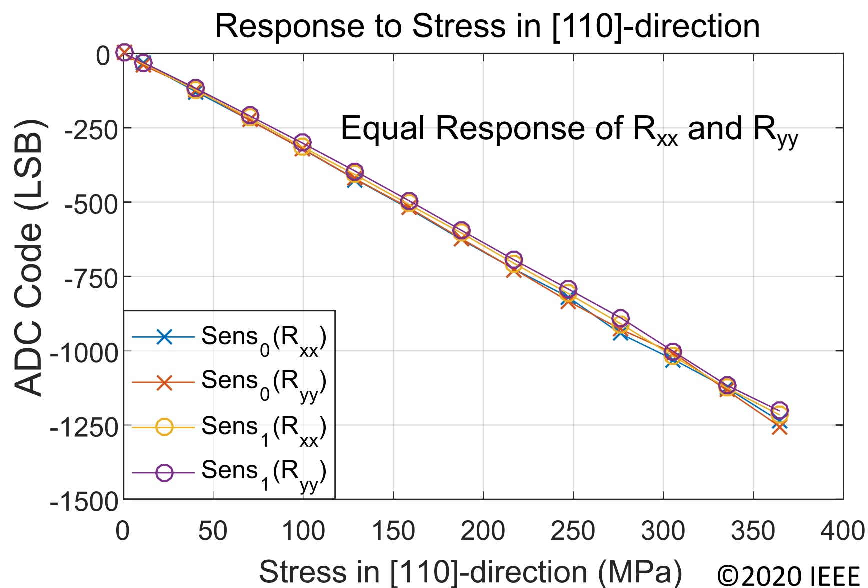

Figure 6.12: Compensated ADC Codes of $Sensor_0$ and $Sensor_1$ for applied mechanical stress in [110]-direction (response of primary sensing elements R_{xx} and R_{yy}).

It can be seen that while R_{xx} and R_{yy} provide outputs that are indistinguishable, quadrant detection can be extracted from the sign of the response in Fig. 6.13.

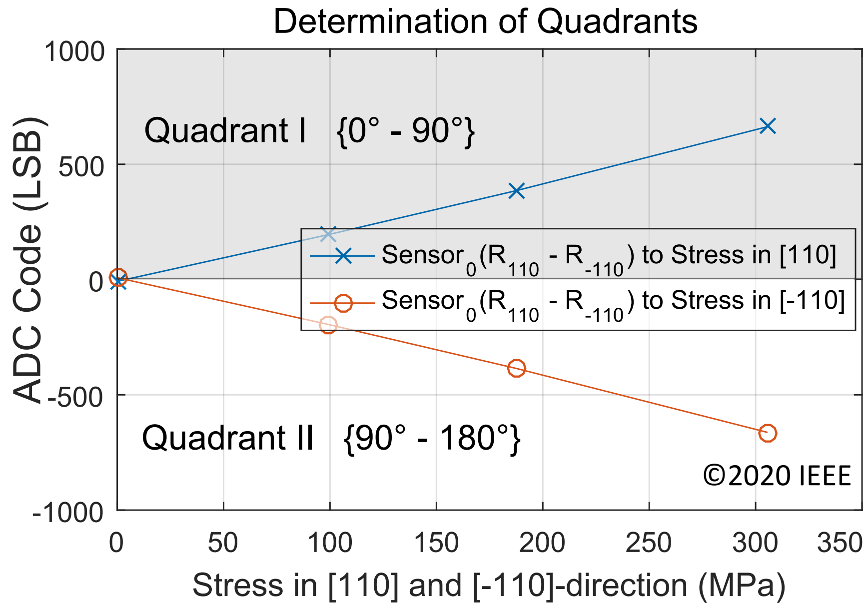

Figure 6.13: Compensated ADC Codes of $Sensor_0$ for applied stress in [110]- and [-110]-directions (response of auxiliary sensing elements R_Q).

Residual Errors

Once all calibrations have been applied, the residual error in the x-direction for tensile stress is shown in Fig. 6.14. The NC values extracted from $Sensor_0$ (wafer #1) were directly applied to $Sensor_1$ (second device from wafer #1) and $Sensor_2$ (from wafer #2). With comparison to the gain of $Sensor_0$, the gain errors for $Sensor_1$ and $Sensor_2$ are +0.3% and -2.7%, respectively. After accounting for gain error and using a best-fit line, residual non-linearity error values (INL) for $Sensor_0$, $Sensor_1$, and $Sensor_2$, are -20 LSB, -35 LSB, and -25 LSB, respectively.

Fig. 6.14 also includes a plot of residual offset error (drift) for R_{xx} and R_{yy} of $Sensor_0$ over temperature (red dashed curves) after all compensations applied at zero stress. Since V_{sense} is not completely linear over temperature, as shown in Fig. 6.4, the first order (linear) compensation results in a residual error that increases at higher temperature, between -20 and +5 LSBs, but both directional components exhibit similar behavior. The overall sensor performance and the measured residual errors are listed for convenience in Table 6.1.

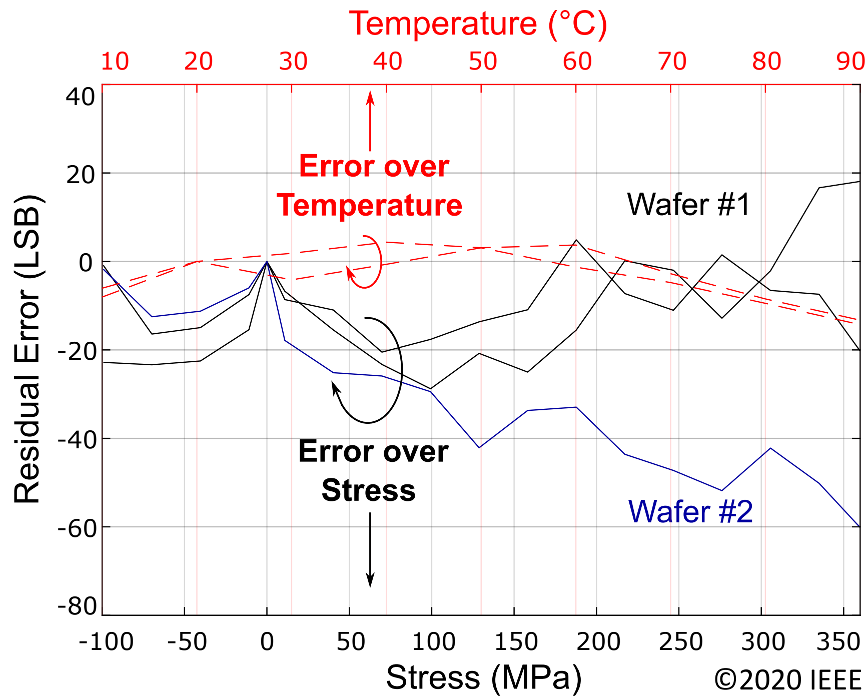

Figure 6.14: Residual error after compensation (in LSBs) for tensile stress in the x-direction and over temperature with zero applied stress (offset drift) for both x- and y-directions (red dashed lines).

Table 6.1: Summary of stess sensor performance and residual errors.

Process	130 nm CMOS
Sensor	n-doped R and p-doped R
Stress Range (measured)	-100 MPa to 360 MPa
Resolution	175kPa (11 bit)
Temperature Range	5°C to 90°C
Temperature Compensation	analog and digital
Angle resolution	±3° limited by measurment setup
Silicon Area	0.46 mm^2 without digital
Power Consumption (analog)	357 uW (without duty-cycling)
Stress Sensors	7
Gain Error (max measured)	2.7 %
Non-linearity error (max measured)	35 LSB
Error over Temperature (max measured)	25 LSB

Chapter 7

Conclusion and Outlook

The stress sensor in this work was developed within a cooperative project between Technical University of Munich and Texas Instruments Freising. The main motivation of the project was to build an on-chip stress sensor for validation of mechanical stress in IC packages and beyond. Hence, there were made specifications for dynamic range, resolution, power consumption and operating temperature range. Also one of the fundamental specifications for the sensor was the ability to separate two stress components in x- and y-direction.

Therefore, a new stress sensing concept was developed that utilizes a combination of n-well resistors for rejection of the unwanted stress components. The concept is based on fundamental dependencies of piezoresistive theory and can be applied in a standard CMOS technology without sensor specific process modifications.

Based on publication of [10], a reference element with similar temperature behavior as sensing resistor, but significantly reduced stress sensitivity was designed utilizing n-well and p-well standard technology components. It was experimentally shown that the temperature and stress dependence of such reference element can be modified by changing certain dimensions of the device.

Two measurement setups were implemented to test the new sensing concept over wide stress ranges and different stress angels. For this purpose, two 3D models were designed of cantilever-based and four-point bending techniques, which were later implemented by the mechanical facility of Technical University of Munich.

Both bending techniques generate mechanical stress on a test device by means of precise weights. This method allows to generate a constant stress over various temperature ranges that is crucial for testing the system in a temperature chamber (separation of mechanical stress from temperature effects).

The readout electronics was designed in the same technology by targeting small area and low power consumption. A special AFE with analog temperature compensation and wide current range trimming ability (that can be used for several stress sensor) was developed.

The combination of $\Delta\Sigma$ ADC with an external μC allows to convert an analog signal

to digital domain and perform there required signal conditioning steps (e.g. digital offset trimming, as well as temperature and nonlinearity compensation).

Several key points for the trim/correction scheme should be emphasized. First, correction of offset (without needing to apply stress) requires a two-temperature trim for each individual sensor; it is recommendable to do this at the wafer level. Simple (not over temperature) offset can be corrected for each packaged device, if necessary. Secondly, as far as the authors have seen (and supported by measurement, to date) stress sensitivity (gain) as a function of temperature should only require extraction of TC_G once, for a given design. These coefficients could then be applied to all devices collectively on any wafer or any lot within normal corner deviations. Thirdly, the NC values for correcting non-linearity would also only be extracted once for a given design and then applied to all devices produced (similar to TC_G).

The points made above are based on the theoretical concepts behind the sensor's function (namely the behavior of stress sensitivity over doping concentration, see Chapter 4.2) and are supported by the provided output signals in Chapter 6.3, recalling that it uses unique offset vs. temperature correction trims (TC_O) but general TC_G and NC values as extracted from a single sensor (applied to all other sensors). In other words, the first form of correction (for offset) must be applied uniquely to every sensor produced but the second and third forms of corrections can be applied blindly to all subsequent devices and can be hardcoded into the final sensor implementations for mass production, at least for specific applications requiring only relaxed sensor accuracy.

It should be mentioned that only two wafers were available for experimental measurements of the sensor system. Therefore, additional statistical data is necessary to further support these assertions. Especially, wafers from different process lots can give the necessary information about critical sensor parameters (e.g. temperature dependence, gain error and nonlinearity) over process variations.

Additionally, the specified temperature range has the potential to be extended further by the use of higher order temperature coefficients which, however, require more measurements over temperature. We also expect that the proposed concept should be compatible with advanced technology nodes beyond 130nm, including those employing strained silicon technologies: unlike the associated MOS transistors, n-well resistors are not strained.

As it was mentioned in Chapter 4.1, the sensor system also includes elements for sensing of shear stress. These sensing elements were not tested during the project due to the measurement setup that was not able to generate shear stress at the time of measurement. Therefore, additional measurement are needed to characterize the sensor system over shear stress. The shear stress sensing element can further extend the application range.

Table 6.1 provides an overview of the sensor performance by showing it operates in the widest stress range (-100 MPa to 360 MPa) and achieves a resolution of 175 kPa. To further improve the resolution of the system, chopping or other modulation techniques are required to reduce 1/f-noise. For example, the reference voltage V_{ref}

of the AFE (see Chapter 5.2), can be modulated. This would shift the desired signal to higher frequencies beyond the 1/f-noise corner frequency of the system.

Summarizing the system performance, in contrast to prior art, the sensor system developed in this work can compensate for large temperature drift, requires less area, and its significantly lower power consumption enables a much wider field of applications.

On-Chip Stress Sensor for Evaluation of Mechanical Stress

The sensor system is designed for on-chip validation of mechanical stress that allows to analyze different types of IC packages in terms mechanical stress under various environment conditions. Distributed sensing element in ICs can also provide information about local absolute stress values, as well as stress gradients between the sensing elements.

The sensor system can also be used for compensation of mechanical stress in systems, where the stress dependency cannot be sufficiently reduced by conventional design methods (e.g. suitable IC package selection, utilization of PNP bipolar transistors instead of NPN, location of sensitive circuits in the middle of a die, etc.). The proposed sensing elements allow to implement analog as well as digital compensation of mechanical stress in ICs.

For this purpose, the critical signal that requires compensation should be tested under mechanical stress. Based on the stress sensitivity of the critical signal, the output signal of the proposed AFE can be scaled to cancel the stress dependence.

Prototype for Industry 4.0 Applications

The prototype presented in this work comprises a flexible 100 μm PCB with a grinded test chip and a μC for digital signal processing. The idea behind the system: the prototype can be attached to a target surface and can measure its bending and deflection under external mechanical stress.

The system has a significant potential to be used in a broad range of applications due to its simplicity of attachment (can be glued or otherwise). However, it is necessary to analyze which portion of mechanical stress is measurable with the test chip and the dynamic range has to be adjusted accordingly.

The prototype can also be used to measure dynamic stress changes. Such system can be used to measure accelerations in certain frequency ranges (limited by the test chip or the prototype configuration). Therefore, a new measurement setup is necessary that can generate mechanical stress at different frequencies.

Nomenclature

Acronyms

ADC	Analog-to-Digital Converter
AFE	Analog Front-End
CAD	Computer-Aided Design
CMOS	Complementary Metal Oxide Semiconductor
CNC	Computerized Numerical Control
CTAT	Complementary to Absolute Temperature
CTE	Coefficient of Thermal Expansion
DAC	Digital-to-Analog Converter
DDA	Dierential Dierence Amplier
DUT	Device under Test
DSP	Digital Signal Processor
IC	Integrated Circuit
INL	Integral Nonlinearity
IoT	Internet of Things
I^{2}C	Inter-Integrated Circuit
LDO	Low-Dropout Regulator
MCU	Microcontroller Unit
MEMS	Microelectromechanical Systems
MOS	MetalOxideSemiconductor
MOSFET	MetalOxideSemiconductor Field-Effect Transistor
MUX	Multiplexer
NC	Nonlinearity Coefficients

NMOS n-channel MOSFET

NFC Near Field Communication

NSD N-doped Source Drain

LSB Least Significant Bit

OPAMP Operational Ampliers

OSR Oversampling Ratio

OTA Operational Transconductance Ampliers

PCB Printed Circuit Board

PGA Programmable Gain Amplier

PDK Process Design Kit

PMOS p-channel MOSFET

POR Power-on Reset

PVC Polyvinyl Chloride

PSD P-doped Source Drain

PSSR Power Supply Rejection Ratio

PTAT Proportional to Absolute Temperature

SAR Successive Approximation Register

SIPO Serial Input Parallel Output

SNR Signal-to-Noise Ratio

TC Temperature Coefficient

USB Universal Serial Bus

Formula Symbols

A	open-loop gain
E_g	bandgap energy of silicon
ε	mechanical strain
F	mechanical force
f	frequency
f_0	signal frequency (bandwidth)
f_s	sampling frequency
g	earth acceleration
k	Boltzmann constant
k_x	average height of quantization noise
m	mass
μ	electron or hole mobility
N	doping concentration
n	charge density
g_m	transistor transconductance
P_e	quantization noise power
P_s	input signal power
Π_{ref}	stress sensitivity of R_{ref}
π	piezoresistive coefficient
q	elementary charge
R_0	nominal resistance

R_{ref}	reference resistor or resistance
R_{sense}	sensing resistor or resistance
ρ	electrical resistivity
σ	mechanical stress
σ_{xx}	normal stress in x-direction
σ_{yy}	normal stress in y-direction
τ	shear stress
T_0	reference temperature (27 °C)
TC_G	gain correction factor
V_0	absolute voltage
$V_{\parallel}$	parallel voltage
$V_{\perp}$	orthogonal voltage
V_{BE}	base-emitter voltage
V_{DD}	positive supply voltage
V_{Δ}	voltage change or drop
V_{FB}	voltage across Rref
V_{GS}	transistor gate-source voltage
V_{NC}	nonlinearity compensated voltage
V_n	input referred noise
V_{ref}	reference voltage
V_{res}	residual offset
V_{off}, V_{OFF}	offset voltage
V_{op}	opamp output voltage

V_{SS}	negative supply voltage
V_{sense}	sensing voltage
V_{TCG}	temperature and gain compensated voltage
V_{TCO}	temperature compensated voltage
V_{th}	transistor threshold voltage
W/L	ration between width and length of a transistor

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Acknowledgements

I would like to express my special thanks and gratitude to my supervisor Prof. Dr.-Ing. Ralf Brederlow, for his confidence and providing guidance through each stage of the project.

I guess I will never forget our discussions at Texas Instruments and later at Technical University of Munich, where I learned a lot of technical concepts and ideas which were fundamental while writing this thesis and certainly will help in my future career.

I thank Prof. Dr. Doris Schmitt-Landsiedel for great opportunity to work on this project and my referee Prof. Dr.-Ing. Roland Thewes for his assistance during my final steps towards the doctorate.

I am particularly grateful for the assistance and guidance given by Tobias Fritz and Dr. Ernst Müllner, without they precious contribution, this dissertation would not have been possible.

I owe my deepest gratitude to my colleague Dr. Christopher M. Dougherty for his willingness to help at any time of the project.

Also, I would like to thank Raj Aggarwal for technology advices and for providing wafers, Rush Carol Ann, Vinod Rai, Gururaj Bankapur, Vishal Gore for helping with layout design, Anton Bauer and Christian Kellner for supporting me with silicon beam sawing and wire bonding and all my other colleagues for their suggestions and assistance.

I had the support and encouragement of my friend Dr. Eugen Egel and have greatly benefited from our fruitful discussions.

Last but not least, I want to thank my parents for their love and care.