Lehrstuhl für Elektrische Antriebssysteme und Leistungselektronik
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Extending the Power and Dynamic Performance of a Power Electronic Hardware-in-the-Loop System through "Inverter Cumulation"

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To my family.

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Munich, in June 2016
Guangye Si

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CHAPTER 1

Introduction

Power electronics systems (PES) have been widely used in industry as effective means of power processing, and played a more important role in most electric power applications. Power semiconductor devices, as the basis of power electronics systems, are always the technical bottleneck because of the semiconductors' physical limitation. In the past several decades, various devices such as thyristor, bipolar junction transistor (BJT), metal-oxide-semiconductor field effect transistor (MOSFET), gate-turn-off thyristor (GTO), integrated gate-commutated thyristor (IGCT) and insulated gate bipolar transistor (IGBT) were developed one after another. After the 1990s, because of good power capability, ease of control and reduced cost, MOSFET and IGBT dominated the power switch market. Although every kind of device has its shortcomings and advantages at the same time, in most industrial conditions one could always realize the required PES with a single type of the semiconductor device. There can be various kinds of requirements for a power processing system, but in general the following aspects are viewed as two most important characteristics of the PES.

- High power processing capability.
- High dynamic response ability.

Most common industry applications have demands for only one of the two aspects above mentioned. For example, the high power high voltage converter system has no excessive requirements to the dynamic response and system switching frequency, due to the relative longer system time constant and aim of switching losses reduction. On the other hand, however applications like switching mode power supplies require very high switching speeds in order to reduce the weight of the necessary magnetic components and increase the power density. Moreover, for the recent high speed and precise servo motor drives, fast dynamic response is also very important. Fortunately, either high power low switching devices or high dynamic low power components are available on the current power electronics device market.

Recently and owing to its intrinsic superiority to the software based simulation, the Hardware -in-the-Loop (HiL) system has got in the focus of researchers. Especially by using power elec-

tronics converters, HiL has a possibility to include real power transfer in the previous signal-based traditional simulation. This new simulation technology named as Power-Hardware-in-the-Loop (PHiL) increases the reliability and reality by adding the physical nature of energy in the simulation process. However, due to the high power rating and large bandwidth of emulation objects, PHiL systems require high power capability and high dynamic response ability *simultaneously*. Therefore, using only a single type of current semiconductor and circuit topology, it is difficult or even impossible to construct a system with such characteristics. How to extend the performance of the PES based on the market-available devices becomes the key issue of PHiL researcher. As mentioned before, because of its physical limitations, every type of semiconductor device has its own weakness which could be the strength of another device. Naturally, a superimposition of characteristics of various devices can be a good solution for the performance extending requirements. Magnetically coupling of several identical or different inverters in various topologies, which will be termed here as *Inverter Cumulation*, is believed to be an effective means to the PHiL, and is the main contribution of this dissertation.

Several successful attempts of *inverter cumulation* have been done at the institute, and two PHiL emulators were developed based on these cumulation systems:

- *Virtual Machine* which emulates the electrical behaviours of various different induction machines.
- *Virtual Grid* which emulates the normal, transient, harmonics, and fault conditions of the utility grid.

The two corresponding *inverter cumulation* topologies are:

- Magnetic-parallel coupling of identical inverters.
- Magnetic-series coupling of different inverters.

During the initial phase of my Ph.D. work, I performed the experimental part of the first project. After that, I focused on the second project which goes beyond the topology of the *virtual machine*. This dissertation mainly documents theoretical analysis and experimental results of these two projects, and is organized as follows: The next chapter gives an overview of two important power semiconductor devices (IGBT and MOSFET) and the principle of the two level voltage source inverter and the 3-phase voltage/current system in order to give the reader the necessary theoretical background. In chapter 3 the first attempt of *inverter cumulation* — magnetic-parallel coupling of identical IGBT inverters are introduced. Based on this inverter cumulation system, a PHiL emulator — *virtual machine* is realized, and it emulates its terminal voltages as real as the back EMF of an induction motor. Chapter 4 firstly introduces the original idea of series-magnetic cumulation topology. However, the experimental failure of the original idea forces one to make a deeper theoretical analysis of the problem. Based on the analysis, the switching frequency components of the inverter must be filtered out before the coupling inductor. At the end, the final modified topology is shown. From the topology point of view, the cumulation system has two units which identically have one VSI with an LC output-filter. Therefore, the control strategy of the whole system is in fact the output voltage control of the LC filter. In chapter 5, several different control methodologies are discussed. The last chapter explains the implementation of the prototype test bench, and then demonstrates the obtained

experimental results to verify the performance of the inverter system and functionality of the PHiL grid emulator. Finally, conclusions and discussions are made and an outlook to future works is given.

CHAPTER 2

Background

This chapter first provides a brief overview of the two most popular power electronics switches. Furthermore, the working principle of the basic two-level inverter system and the mathematical representation of the 3-phase system in synchronous frame are described.

2.1 Power semiconductor devices

The invention of the thyristor or silicon controlled rectifier (SCR) at General Electric (G.E.), in 1956 is viewed as the start era of modern power electronics devices. As the heart of power electronics systems, the performance of power semiconductor devices is continuously improving along with the reduction of their cost, which decreased to less than half in the past century. The desire to have an efficient, reliable and cost-effective design, leads to the engineers requirements to use ideal switches in converters. A ideal switch must have the following characteristics:

- No limit on current ratings (forward or reverse current) when the device is in the on-state;
- No limit on voltage ratings (forward or reverse blocking voltage) when device is in the off-state;
- Zero conduction drop;
- Zero leakage current;
- Instant switching (zero rise and fall times)

Although it is not realistic to have all these features, the industry has moved step by step in this direction. At the same time, PE engineers always try to investigate new circuit topologies to overcome the drawbacks of power semiconductor devices. In the following, a very brief introduction of several representative devices is given in the sequence of their invention time.

The detailed physical structure, working principle, switching characteristics, and driver design etc. are out of the scope of this thesis.

2.1.1 Thyristor-type devices and power BJT

A thyristor is a three-terminal device which has four layers of alternating p-type and n-type material. It is essentially a three-junction pnpn device where pnp- and npn-component transistors are connected in a regenerative feedback mode. Thyristors can be switched into conduction mode by a short gate current pulse, and the gate signal is not required after the device is conducting. Due to the high voltage and current ratings, thyristors are typically used at the large energy levels in power condition circuits. However, one loses the control capability of turning off the devices once they are conducting. Thus thyristors are most used for the phase control of the line voltage in a line commutation mode.

GTOs (Gate Turn-off Thyristor) like conventional thyristors can be turned on by applying a positive gate signal to its gate terminal during forward block condition, but they are designed to be able to turn-off by applying a negative gate signal. This turn-off capability of a GTO is due to heavily interdigitated gate-emitter geometry that permits diversion of the pnp collector current by the gate thus breaking the the pnp-npn regenerative feedback effect [1]. One drawback of GTOs is the poor current gain which is normally below than 5. Moreover, the blocking capability requires thick n-base regions to support the high electric filed, which results in an excessive amount of carriers to remove — large turn-off current tail. Therefore, the GTOs are normally used at conditions with switching frequency around several hundred hertz. The IGCT, Integrated Gate Commutated Thyristor, which is a minor modification of the GTO, is designed and manufactured so that it always has a low-loss n-buffer region between the n-base and p-emitter. The IGCT device package is designed to result in a very low parasitic inductance and is integrated with a specially designed gate-drive circuit. The gate drive contains all the necessary di/dt and dv/dt protection; the only connections required are a low-voltage power supply for the gate drive and an optical signal for controlling the gate. The specially designed gate drive and ring-gate package circuit allows the IGCT to be operated without a snubber circuit, and to switch with a higher anode di/dt than a similar GTO [2].

Power BJT (Bipolar Junction Transistor) has the same structure and working principle as the conventional bipolar junction transistor. But unlike the signal level devices which take the current gain, linearity, frequency response and noises etc. into consideration, its main characteristics are high block voltage, high current rating and better switching performance. A power BJT has three layers of either pnp or npn which form two pn junctions, but npn type transistors are more common to make a Darlington connection. Unlike thyristors, BJTs require a continuous gate-controlled current. Thus the most difficult design aspects to overcome are the base drive circuitry which must generate high and prolonged input currents. Due to minority carriers being removed by the negative gate current entirely and quickly, power BJTs are able to be switched (several kHz) much faster than the thyristor-type devices. However, compared with the new technology of MOSFETs and IGBTs, they are considerably slower, and exhibit long turn-on and turn-off times. Although lower input capacitance and saturation voltage are their advantages, the voltage-controlled devices like MOSFETs and IGBTs are now better alternatives than BJTs.

2.1.2 Power MOSFET

Power MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) are voltage-controlled semiconductor devices, which means their drive circuit is simpler and requires smaller power compared with the current-controlled power electronics switches. Moreover, unlike the BJT, and since only majority carriers contribute to the current flow, the MOSFET surpasses all other devices in switching speed. However, the MOSFET has no latching current capability, thus the gate source voltage must be maintained. The on-state resistance $r_{DS(on)}$ increases rapidly with the device blocking voltage rating. Because of this, the voltage rating of a MOSFET is lower, and it is typically used in applications with a power range below 10kW.

Various types and structures of MOSFETs are available on the market. By means of doping profiles, there are n-channel and p-channel MOSFETs, however n-channel devices are more commonly used. As shown in Figure 2.1, a MOSFET has three terminals (source, drain and gate) and a four-layer structure. When a positive voltage is applied across the drain and source, the MOSFET is in the off-state if the gate and source are in the same potential $V_{\text{GS}} = 0$, and no channel is established in the p-base region. In order to assure the blocking capability, lower doping in the n-drift region is necessary.

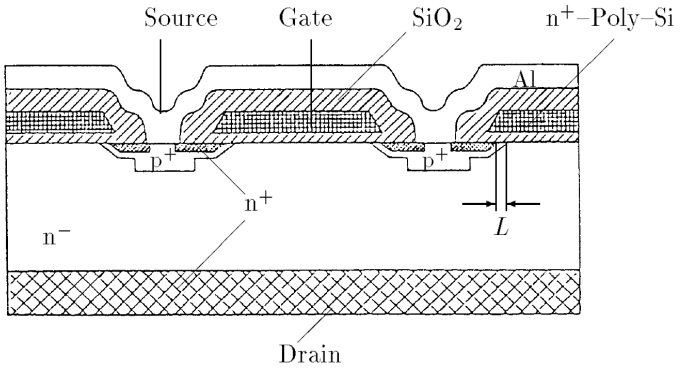


Figure 2.1: Vertical cross-section structure of a MOSFET

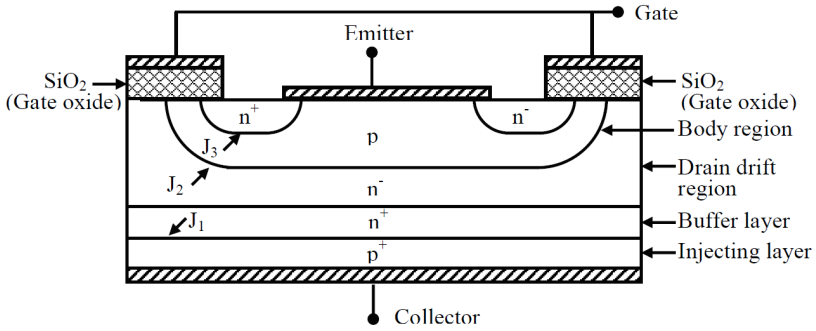
As the gate terminal is isolated from the body by a layer of silicon dioxide (gate oxide), there can be no gate injection current. However, a positive V_{GS} will generate an electric field which repels the majority of carrier holes from the interface region of the p-type and thus exposes the negatively charged acceptors. When the density of free electrons is bigger than the holes, the p-type layer is converted to an n-type layer which is termed inversion layer. Because of this inversion layer, a path or channel between the n^+ drain and source is generated, which permits the conducting of the device. This ability to modify the conductivity type of the semiconductor immediately beneath the gate insulator by means of an applied voltage or electric field is named field effect [3].

The key for modern power electronics is higher and higher switching. The size and weight of the passive components which serve as the output filter of the power converters can decrease dramatically as the result of the increase in the switching frequency. For this reason, MOSFETs are used extensively in switching mode power supply (SMPS), resonant mode power supply and high speed motor drives, etc. Therefore, MOSFETs replace BJTs and several other devices developed before in the small power range application quickly, and they still have a very high

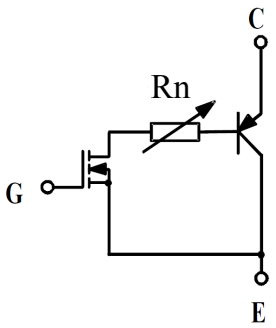
market share. However, as illustrated before, its on-state resistance increases dramatically with increased blocking voltage, hence conduction losses become too high. Thus MOSFETs are limited to a power range of several kilo watts.

2.1.3 IGBT

As mentioned before, the power BJT has a lower on-state resistance especially in devices with a larger blocking voltage, but because of the long switching time, especially during turn-off, they can only be used in low switching applications. On the other hand, the MOSFETs are the fastest switching devices, but they have high conduction losses as a result of the large on-state resistance especially when the blocking voltages are higher. IGBTs (Insulated Gate Bipolar Transistor) are the new attempts which combine BJTs and MOSFETs monolithically on the same silicon wafer and hence have the superior advantages of both types of devices. The structure of an IGBT is shown in Figure 2.2(a). Compared to the structure of a MOSFET,



(a) Vertical cross-section structure of IGBT



(b) Equivalent circuit

Figure 2.2: Structrue of an IGBT and its simplified equivalent circuit

the IGBT has an additional p^+ layer at its collector terminal. This layer forms a pn junction J_1, which injects minority carriers into what would appear to be the drain drift region of the vertical MOSFET. The conductivity of the drain-drift region is modulated by the injection of minority carriers, and since the conduction resistance of the drift region is what dominates the on-state resistance of the MOSFET, hence this conductivity modulation will significantly increase the current-carrying capabilities of the IGBT. The rest of the IGBT structure is basically a MOSFET.

As explained previously, an inversion layer also forms beneath the gate of the IGBT, which shorts the n^- drift region and the n^+ source region exactly as in a MOSFET. An electron current which flows through this inversion layer causes substantial a hole injection from the p^+ which is superior to the MOSFET. The p^+ layer of the collector, the drift n^- layer and the p region constitute a BJT with a wide base region and hence small current gain. From this description, the IGBT is modelled as a Darlington circuit with the pnp BJT as the main transistor and the MOSFET driver device (shown in Figure 2.2(b)).

IGBTs have on-state voltage and current densities comparable to a power BJT with a higher switching frequency. Although they exhibit fast turn-on times, their turn-off times are slower

than a MOSFET because of the current fall time. The current tail limits the IGBT operating frequency and there is a trade off between the on-state losses and faster switching times. However, IGBTs have considerably higher voltage and current ratings than MOSFETs. IGBTs and MOSFETs are still the two most popular switching devices in power electronics, and their characteristics complement each other in some aspects.

2.1.4 The practical switch

Every power semiconductor device developed in the past has its advantages and shortcomings at the same time. Although the new devices always show more superiorities to the previous ones, no device is an ideal switch capable of satisfying all the requirements in every working condition. A practical switch has the following switching and conduction characteristics:

- Limited power handling capabilities.
- Limited switching frequency.
- Finite on-state and off-state resistances.
- Conduction losses and switching losses.

Selecting the most appropriate device for a given application is always a challenging task. It requires the power electronics engineers to have the knowledge about the device's characteristics, unique features and engineering design. Among the various characteristics, the power rating and dynamic response or switching speed are the two most important aspects which determine a final choice of device for a specific application under specific working conditions. Based on the previous introduction, Figure 2.3 shows an approximate power and switching frequency characteristics of the most common power semiconductor devices.

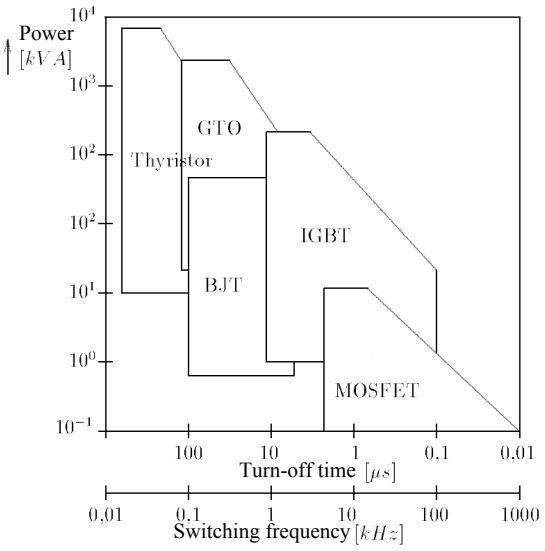


Figure 2.3: Power vs switching frequency characteristics of power devices [4]

As can be seen from the figure, in the high power range, GTOs/IGCTs and thyristors are comparable, however due to the turn-off control capability and faster switching, GTOs/IGCTs

replace the thyristors in these applications of this power range. IGBTs have a comparable power range with BJTs, and a little smaller power rating than GTOs, but higher dynamic response than both of them. Therefore, the BJT is not a competitive solution for applications in this range. IGBTs dominate in the medium power rating and dynamic response industrial applications. The MOSFET has the highest the switching frequency than all the other devices. Although it has a lower blocking voltage and hence a smaller power rating, the MOSFET is the only capable candidate which can handle switching frequencies above 100kHz.

Due to the physical limitation of each power device, no single type of semiconductor switch can cover all the power electronics systems with a whole range of power and dynamics. But power electronics engineers can always find an appropriate device for their designs, because power and dynamics are not simultaneous requirements of the most industrial conditions. The system with high power and high dynamics is however desired in some special cases like PHiL explained before. A solid understanding of the current market available devices is the basis for investigating a possible solution.

2.2 The Two-level voltage source inverter and three-phase systems

The two-level voltage source inverter is the basic circuit of the DC-AC power electronics system. Due to its simplicity and functionality, it plays the most important role in motor control, UPS systems and other grid-connected energy convention systems. As shown in Figure 2.4, each phase of the inverter has two switches S_{x1} and S_{x2} which are IGBTs in this case. By

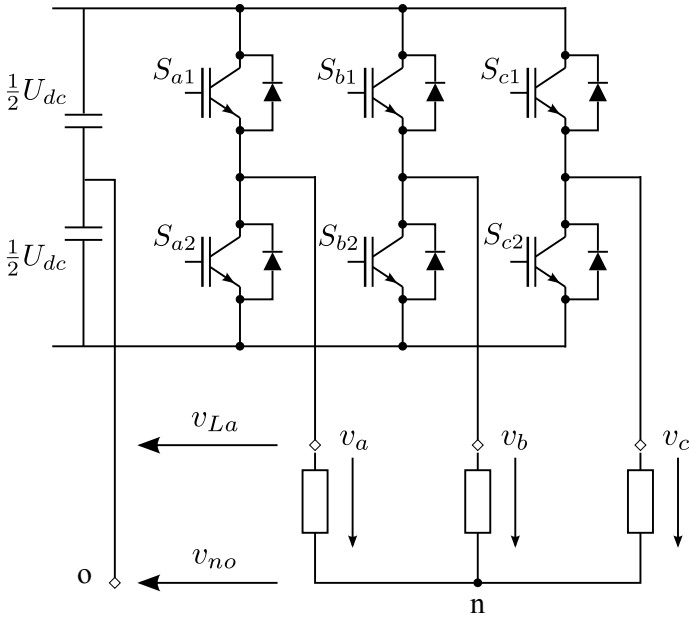


Figure 2.4: Three-phase two-level inverter

activating either the upper switch or the lower switch during each switching period, the output line voltage v_{Lx} is modulated with alternative potentials ether $\frac{1}{2}U_{\mathrm{dc}}$ or $-\frac{1}{2}U_{\mathrm{dc}}$. Simultaneous

on of both switches is strictly forbidden, as this would lead to a short circuit of the DC-link. Both switches in the *off* state leads to an undefined potential at the output terminal, and breaks the current continuous flowing loop which is dangerous under a heavy inductive load condition. Therefore, the allowed switching states are shown in Table 2.1. The neutral point voltage v_{no} is the common voltage of the three-phase system.

Table 2.1: Switching states and output voltages of a two-level inverter leg x

S_x	S_{x1}	S_{x2}	v_{out}
1	1	0	$0.5V_{\text{dc}}$
-1	0	1	$-0.5V_{\text{dc}}$

$$v_{no} = \frac{1}{3}(v_{La} + v_{Lb} + v_{Lc}) \tag{2.1}$$

The phase voltage $v_x(x \subset abc)$ can be calculated as follows:

$$v_x = v_{Lx} - v_{no} \tag{2.2}$$

2.2.1 Mathematical representation of the three-phase system

The aim of the inverter is supplying a sinusoidal symmetrical three-phase voltage to the load system. Therefore, the phase voltages can be described as follows:

$$v_a = U \cdot \sin(\omega \cdot t) \tag{2.3}$$

$$v_b = U \cdot \sin(\omega \cdot t + \frac{2\pi}{3}) \tag{2.4}$$

$$v_b = U \cdot \sin(\omega \cdot t + \frac{4\pi}{3}) \tag{2.5}$$

They can be represented by a three-axis coordinate system as shown in Figure 2.5, but the three-axis a, b and c are not linearly independent of each other [4]. The space vector representation decouples the reference system and transforms a three-phase system into a two-dimensional coordinate system. The space vector is defined as the following equation:

$$\boldsymbol{x}_s = x_a + \boldsymbol{a} \cdot x_b + \boldsymbol{a}^2 \cdot x_c \tag{2.6}$$

$$\boldsymbol{a} = e^{j \cdot \frac{2\pi}{3}} \tag{2.7}$$

The space vector $\boldsymbol{x}_s$ can be split into α and β components in the above mentioned two-dimensional static coordinate system.

$$\boldsymbol{x}_s = x_\alpha + j \cdot x_\beta \tag{2.8}$$

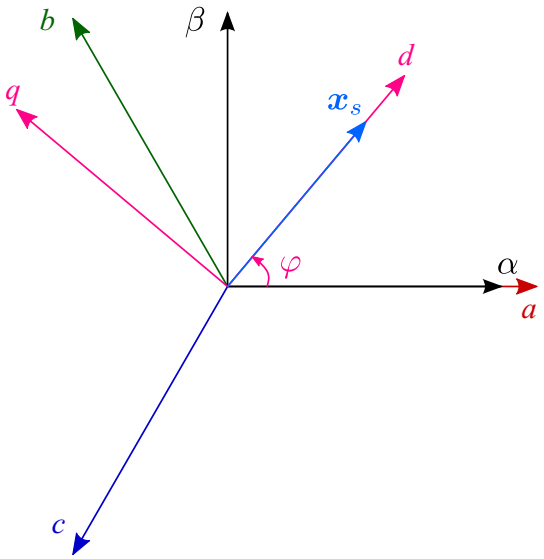


Figure 2.5: Reference systems

By substituting equation 2.8 into 2.6, the transformation can be written in the form

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \boldsymbol{T}_c \cdot \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{2.9}$$

$$\boldsymbol{T}_c = \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{2.10}$$

Equation 2.10 is commonly named as the Clarke transformation operator. The reverse transformation can be calculated in the form

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \boldsymbol{T}_c^{-1} \cdot \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{2.11}$$

$$\boldsymbol{T}_c^{-1} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{2.12}$$

By applying the Clarke transformation, one can decouple the 3-phase non-independent time-various variables into two independent $\alpha\beta$ components. However, in many industrial applications, conventional PI controllers can only compensate DC errors. The space vector $\boldsymbol{x}_s$ in the stationary frame is still a rotary vector, hence its two dimensional components are still time various variables. Therefore all the variables should be transformed as a DC vector in a synchronous *dq*-frame (as shown in Fig. 2.5) which rotates with the same frequency ω as the space vector $\boldsymbol{x}_s$. Normally the the *d*-axis is aligned with the space vector, and the transformation is named as Park transformation which is described by the following equations:

$$\varphi = \omega \cdot t \tag{2.13}$$

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \boldsymbol{T}_p \cdot \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{2.14}$$

$$\boldsymbol{T}_p = \begin{bmatrix} \cos(\varphi) & \sin(\varphi) \\ -\sin(\varphi) & \cos(\varphi) \end{bmatrix} \tag{2.15}$$

The reverse Park transformation from *dq* to $\alpha\beta$ is:

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \boldsymbol{T}_p^{-1} \cdot \begin{bmatrix} x_d \\ x_q \end{bmatrix} \tag{2.16}$$

$$\boldsymbol{T}_p^{-1} = \begin{bmatrix} \cos(\varphi) & -\sin(\varphi) \\ \sin(\varphi) & \cos(\varphi) \end{bmatrix} \tag{2.17}$$

As explained previously, each leg of the two-level inverter has two switching states, so in sum there are 2^3 switching states for a 3 phase inverter. By applying the space vector equation 2.6 to all these switching states, one can get the space vector diagram of the voltage source inverter as shown in Figure 2.6.

$$v_{Lx} = s_x \cdot \frac{1}{2} V_{dc} \tag{2.18}$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \boldsymbol{T}_c \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \boldsymbol{T}_c \cdot \begin{bmatrix} v_{La} - v_{no} \\ v_{Lb} - v_{no} \\ v_{Lc} - v_{no} \end{bmatrix} = \boldsymbol{T}_c \cdot \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} \cdot \frac{1}{2} V_{dc} + \mathbf{0} \tag{2.19}$$

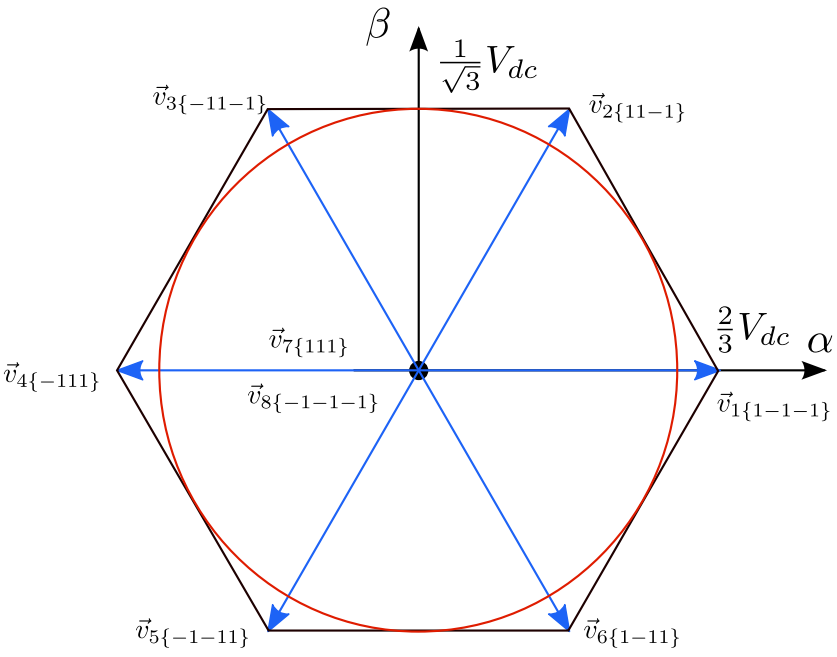


Figure 2.6: Space vector diagram of a 2-level voltage source inverter

As shown in the figure, the red circuit orbit with the amplitude of $\frac{1}{\sqrt{3}}V_{dc}$ coincides with the highest allowable reference value for a linear modulation, which can be located within a hexagon that is constructed from the six active vectors with length $\frac{2}{3}V_{dc}$.

2.2.2 Pulse width modulation of the voltage source inverter

In modern power electronics systems, pulse width modulations (PWM) are widely used to drive the power switches in *on/off* switch mode operation, and in which the modulator ensures the average voltage (per sample interval) equals the user defined average reference value [5]. The two best-known PWM technologies are the triangular carrier-based sinusoidal PWM (SPWM) and the space vector modulation (SVM) [6]. A detailed review of PWM in power converters is beyond the scope of this thesis. In the following, only brief introductions of the working principles of the two above mentioned PWMs are presented to the readers who are not familiar with this issue.

Sinusoidal PWM is based on a triangular carrier signal. The three phase voltage reference signals v_a^*, v_b^*, v_c^* are compared with the common carrier, then the gate signals of the inverter are generated based on the logical signals of the comparison. Typically, if the reference voltage v_x^* is bigger than the carrier, a positive logical signal is generated, and the upper switch of x leg is activated; and the lower switch is switched on when the v_x^* is smaller than the carrier. As shown

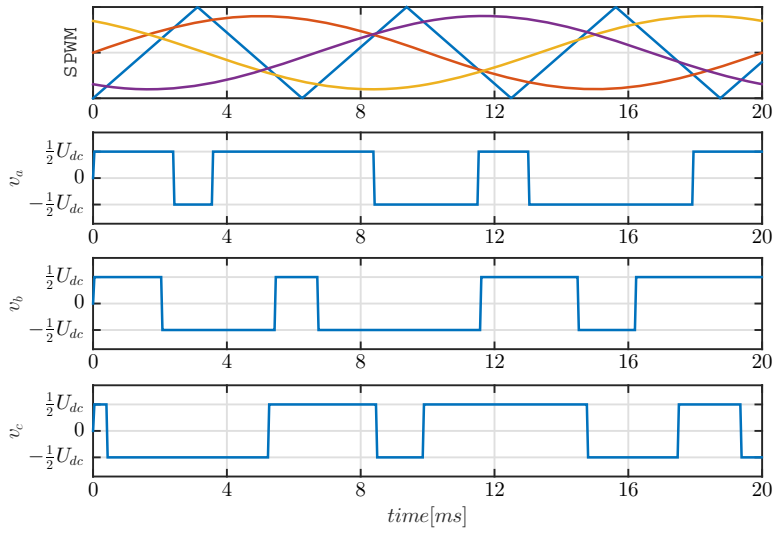


Figure 2.7: Basic waveforms of carrier-based sinusoidal pulse width modulation

in Figure 2.7, the waveforms of the reference voltage signals are compared with a sawtooth carrier, and output phase voltage of each leg alternates with the values of either $\frac{1}{2}U_{\text{dc}}$ or $-\frac{1}{2}U_{\text{dc}}$.

The other popular modulation scheme is the *space vector modulation*. It is directly based on the space vector defined in Equation 2.6. On the space vector diagram, a desired voltage waveform is a trajectory of the reference space vector's end. In each short switching time interval Δt, one average vector is used as the modulation reference as shown in the figure 2.8. This average reference vector is approximated by activating the two adjacent voltage-vectors and the zero-vector for suitable durations. By analysing the example case shown in Figure 2.8, the following equations explain the principle of the SVM.

$$\vec{\boldsymbol{v}}_{ref} \cdot \Delta t = \vec{\boldsymbol{v}}_1 \cdot t_1 + \vec{\boldsymbol{v}}_2 \cdot t_2 + \vec{\boldsymbol{v}}_{7/8} \cdot t_0 \tag{2.20}$$

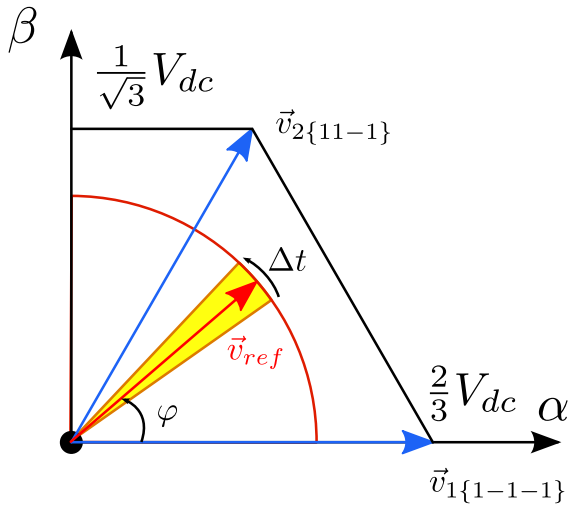


Figure 2.8: Space vector modulation of a 2-level voltage source inverter

$$\beta - axis: \quad |\vec{\boldsymbol{v}}_{ref}| \sin(\varphi) \cdot \Delta t = \frac{1}{\sqrt{3}} V_{dc} \cdot t_2 \tag{2.21a}$$

$$\alpha - axis: \quad |\vec{\boldsymbol{v}}_{ref}| \cos(\varphi) \cdot \Delta t = \frac{1}{\sqrt{3}} V_{dc} \cdot (2t_1 + t_2) \tag{2.21b}$$

where t_1, t_2 and t_0 are the activating time of the space vector $\vec{\boldsymbol{v}}_1$, $\vec{\boldsymbol{v}}_2$ and the zero vector $\vec{\boldsymbol{v}}_{7/8}$

$$\Delta t = t_1 + t_2 + t_0 \tag{2.22}$$

By solving Equation 2.21 and 2.22, one can get the time interval of t_1, t_2 and t_0.

2.3 Summary

In this chapter, a brief overview of the different power semiconductor switches is given first. Due to the superior characteristics and better performance, IGBT and MOSFET are two complimentary devices which are widely used in high power and high dynamic applications respectively. However, as a result of physical limitation, no single type of device can satisfy every performance requirement with one circuit topology. The following part explains the basic principle of the two-level voltage source inverter and the space vector presentation of the three-phase system. These all serve as the basic background of this dissertation.

CHAPTER 3

First attempt of *Inverter Cumulation* and *Virtual Machine*

As explained in the chapter before, a power electronics system with high power rating and high dynamic response results in excessive requirements on the power semiconductor devices. In the past, high power and high dynamics have not been two simultaneously expected characteristics in industrial application. However, due to the quick development of the Power Hardware-in-the-Loop (PHiL) system, a power conversion system which delivers enough power and exhibits wide bandwidth is highly demanded. The *Inverter Cumulation* is defined as:
Interconnection (parallel, series and cascade) of identical or different voltage source inverters via magnetic or galvanic coupling.
The *inverter cumulation* is believed to be an effective approach to extend the power and dynamic performance of a power electronics system. In the past we tried various circuit topologies. As I did several experimental and documentary work on it, and due to the importance of further extending the project, this chapter presents the first attempt of our *inverter cumulation* and the PHiL emulator *Virtual Machine* [7] based on this topology.

3.1 Problem formulation

In order to prevent early failures in commercial products, a power inverter test (burn-in test) is an important issue before the delivery of customers application. Generally, the manufacturer of power inverters for drive applications has to use a multitude of different electrical machine units (as shown in Fig. 3.1) to emulate the industrial applications as close as possible to the reality. But in most of the cases the inverter under test (IUT) is only connected to a machine under no load condition, for the sake of financial benefit and production time reduction. Thus the inverter operates just for a short time during acceleration and deceleration at maximum power. Obviously, this procedure, which is actually more stressful for the electric machine than for the IUT, does not properly emulate typical operating conditions of the inverter. The direct

consequence is a severe lack of pertinence of the results gained from the tests. In fact, a PHiL

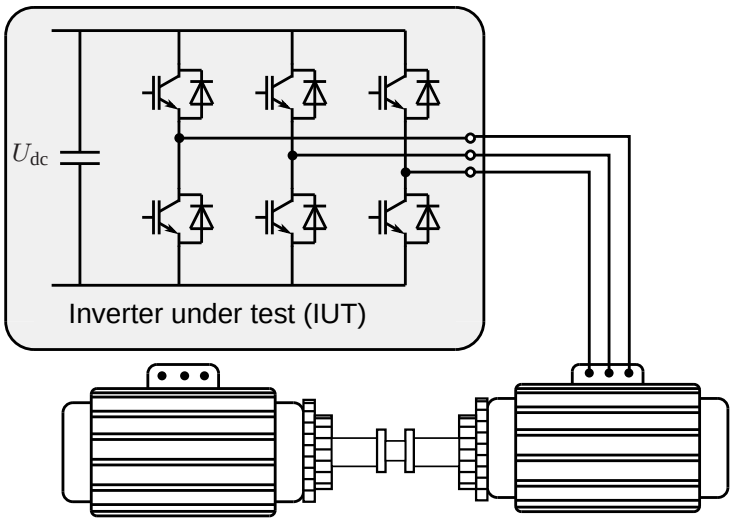


Figure 3.1: Schematic diagram of a conventional test bench for testing power drive inverters

emulator can be substituted for the real machine in inverter testing applications. These motor emulators basically include a power amplifier controlled by a real-time computer to emulate the electrical behaviour of a real motor. Various topologies have been proposed as *Virtual Machine* in the last several years [8–14]. They generally comprise of a back-to-back converter as a power amplifier, allowing energy to be fed back to the grid and hence, increasing the efficiency of the test bench appreciably. The detailed comparison of different topologies is out of the scope of this dissertation. In the following section, the overview topology of our *virtual machine* and the special performance requirements of the emulator power stage is illustrated.

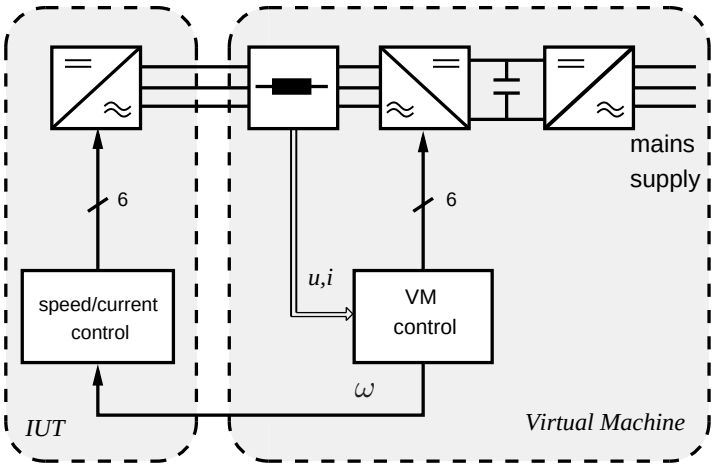


Figure 3.2: Schematic of the proposed test bench topology.

As shown in Figure 3.2, beside the IUT, the VM features a power unit with an active front end for the purpose of energy savings as well as a DSP-based Real Time System (RTS) and

inductive elements allowing the coupling with the IUT. Line currents between the IUT and the VM are measured and sampled by the RTS. Using a machine model, which will be described in later sections, the corresponding value of the back electromotive force (EMF) and the rotor speed are computed. While the back-EMF is then modulated by the power unit, three binary signals are generated from the speed value like the ones of a incremental encoder and passed to the IUT.

3.1.1 Performance requirements of the power electronics system of the VM

An essential requirement to the VM is the possibility of testing the IUT under any of its operating conditions. This especially includes overload tests. For this reason, the performance of the VM has to be slightly greater than the IUT. In practice, an increase of the DC link voltage of 20 to 50V turns out to be sufficient. Therefore, with respect to the power level, the converter inside the VM can be of the same type as the IUT, since the voltage increase stays within the tolerance margins of most industrial inverters. In this case, only an adjustment of the control parameters is needed. Furthermore, using a common inverter instead of a specifically designed system is economically advantageous.

On the other hand, as is well known, switched power sources generate output voltage waveforms with great amounts of parasitic harmonics. Such parasitic harmonics will hence appear in the back-EMF waveform generated by the VM, and special care has to be taken so that they do not alter the behavior of the IUT. However, the coupling inductors between the VM and the IUT will act like low-pass filters and remove the upper harmonic range from the currents flowing through the IUT. Since these currents (and not the back-EMF) are used as control variables by the IUT, choosing a switching frequency high enough will alleviate the adverse effect of switching harmonics.

In fact, owing to the physical limitations of semiconductor devices, doubling or tripling the switching frequency of an industrial inverter is relatively arduous to realize. An effective means of overcoming this difficulty while still using standard commercial products is connecting several inverters in parallel on the same DC link and activating them sequentially, as described in the next section.

3.2 Magnetically paralleled *inverter cumulation* system

In order to build a system which satisfies all the requirements of the VM with standard market available devices, the power stage is a *inverter cumulation* system which is composed of five identical IGBT inverters which are magnetically coupled and sequentially switched. By doing this, the overall system switching frequency is five times higher than each single inverter. As mentioned in Chapter 2, IGBTs are capable of handling high power with a moderate switching frequency. The presented *inverter cumulation* system is believed to increase the system modulation frequency meanwhile keep switching speed within the limitation of each device. This section presents the working principle and the realized test bench in detail.

3.2.1 Sequential switching

Sequential switching, often improperly referred to as *interleaved switching*, is a switching scheme for parallel-connected power semiconductor devices, in which they are switched on and off one after the other but never simultaneously [15, 16]. On the contrary, *interleaved switching* makes use of concurrent operation of parallel devices [15–22].

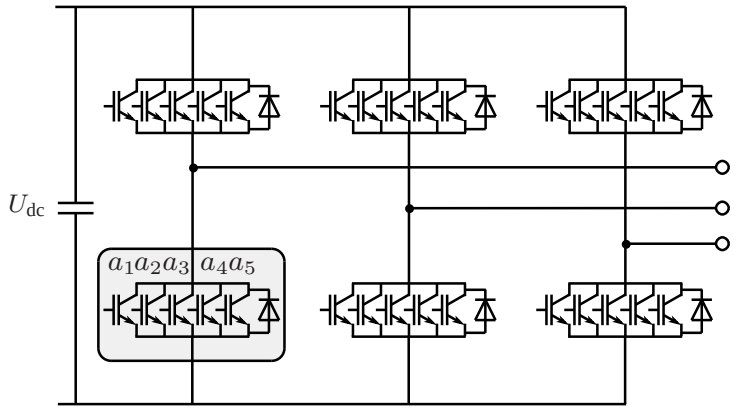


Figure 3.3: Sequential switching of parallel power semiconductor devices in a voltage source inverter.

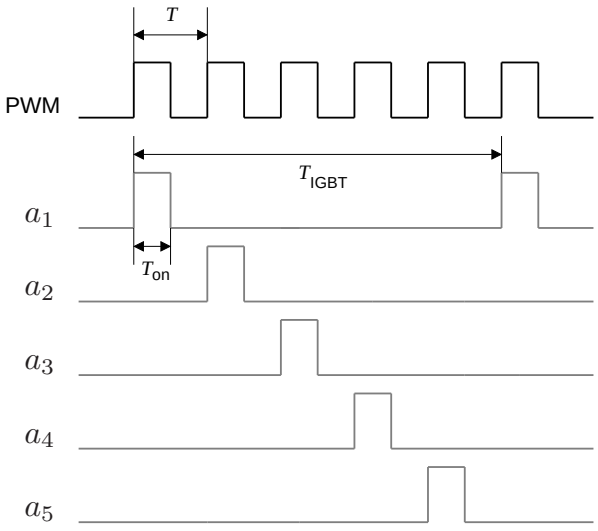


Figure 3.4: Example of sequential switching pulse sequence for power devices connected in parallel.

Sequential switching, as used in the VM, allows to distribute switching and conduction losses among several IGBTs instead of only one. In this way, it is possible to increase the power capability of a system as well as its modulation frequency f_{PWM} without exceeding the maximum ratings of the individual devices. Fig. 3.3 illustrates the concept with a three phase voltage source inverter in which usual IGBTs have been replaced by arrays of five switches connected

in parallel together with a single freewheeling diode (Fig. 3.3). Fig. 3.4 shows a typical pulse pattern for such an array (dead time of upper and lower switches not represented). The PWM signal is not directly transferred to the IGBTs but is split into five couples of signals numbered from 1 to 5. The first signal of couple i is sent to IGBT a_i while the second is used to activate IGBT a_i'. In this example, sequential switching reduces the switching frequency of each power device to a fifth of the PWM frequency, and the maximum switch-on period $T_{\text{on,max}} = T$ of each semiconductor is limited to a fifth of the switching period T_{IGBT}.

Nevertheless, in this configuration, the separate freeweeling diodes would have to carry the whole phase current. In order not to overload them while increasing the switching frequency, a slight modified design based on standard IGBT modules with integrated freeweeling diodes is considered in the following part. However, this approach also raises a few serious challenges, which are discussed next.

3.2.2 Necessity of a magnetic freewheeling control

While sequential switching of IGBTs is easy to implement, the freeweeling diodes are a matter of concern, as they cannot be switched actively. If no particular care is taken, all diodes of a half bridge may conduct during freeweeling operation. Ideally, the diodes should have the same characteristics and share the load current equally. In practice, the physical properties of electrical components show discrepancies. Consequently, the diode with the lowest internal resistance will carry the major part of the load current and heat up more than the others. The negative temperature coefficient makes the current flowing through the component increase. This process continues until its possible destruction.

An effective approach to overcoming this problem, known as *magnetic freeweeling control* and described in detail in [23], [24] and [25], is summarized in the following. It provides a means of switching the freewheeling diodes sequentially, in the same order as the IGBTs by using a magnetic element. The principle of this concept is exemplified in Figure 3.5.

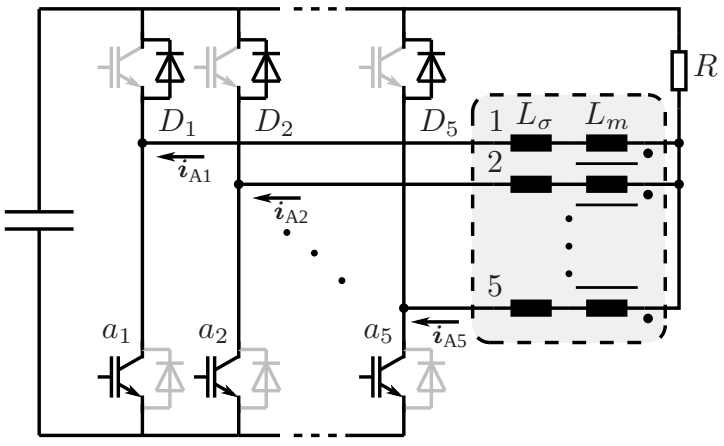


Figure 3.5: Example circuit of magnetic freewheeling control.

In Figure 3.5, five standard IGBT half bridge modules are connected in parallel. Each half bridge output is connected to a coil terminal of the 5-phase coupling inductor shown in the shaded box and assigned a number from 1 to 5. The coils are wound on the same magnetic core

and exhibit a main inductance L_m and a leakage inductance L_σ. The power switches a_1, a_1', ..., a_5, a_5' are activated sequentially according to the pulse sequence shown in figure 3.4. The diodes D_1', D_2', ..., D_5' are expected to conduct the freewheeling current while the current in phase A, i_A, is flowing out of the coupling inductor, i.e. is positive according to figure 3.5. In fact, the coupling inductor is the key component of the freewheeling control strategy. For the sake of clarity, its behaviour and not its design is to be described first.

Assuming a positive phase current i_A and a PWM pattern according to Figure 3.4, IGBT a_1 is activated by the first PWM pulse. The load current i_{A1} starts flowing through IGBT a_1 and coil 1. After turning off a_1, i_{A1} decreases with a slope equal to $\Delta i_{\mathrm{A1}}/\Delta t$, generating a voltage drop across coil 1 given by:

$$\begin{aligned} \Delta u &= \Delta u_m + \Delta u_\sigma \\ &= L_m \frac{\Delta i_{\mathrm{A1}}}{\Delta t} + L_\sigma \frac{\Delta i_{\mathrm{A1}}}{\Delta t}. \end{aligned} \tag{3.1}$$

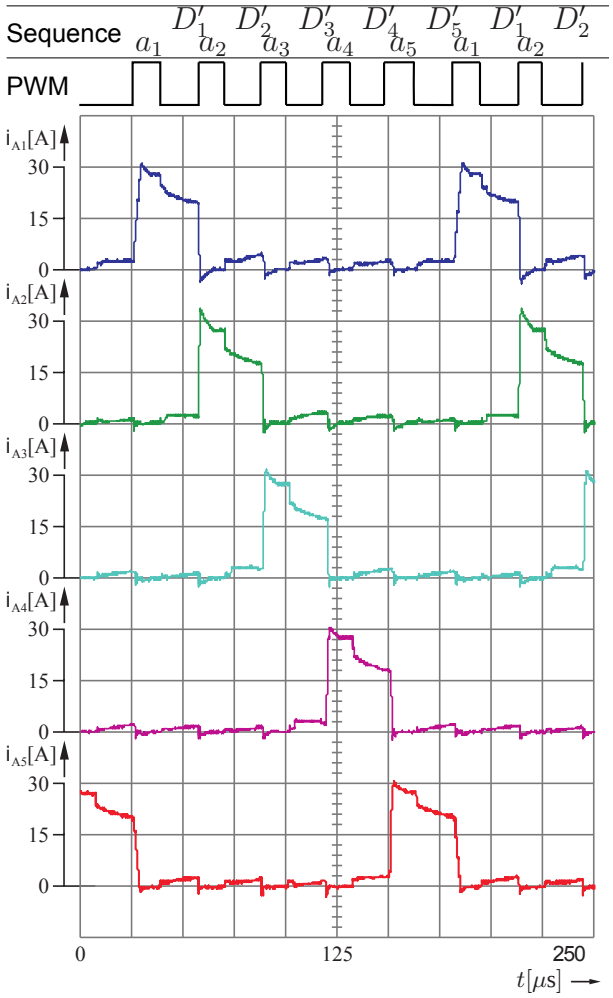
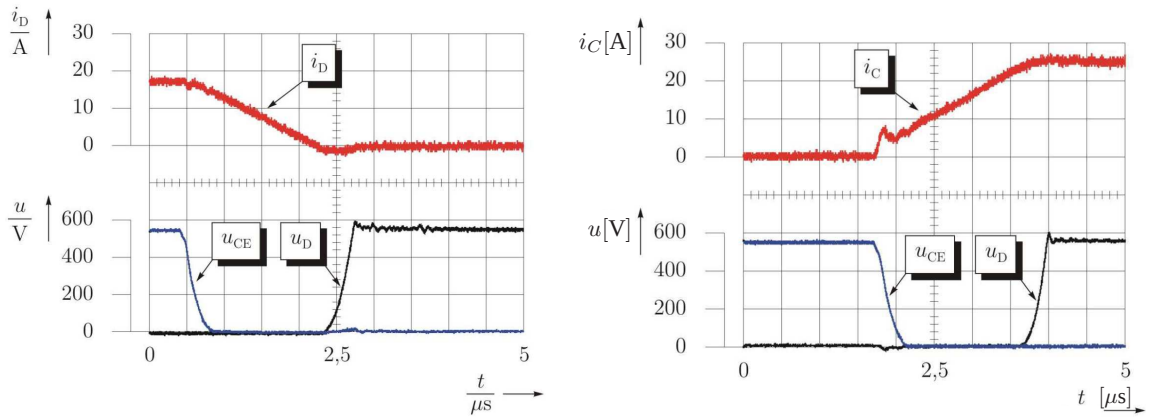


Figure 3.6: Experimental current waves obtained from the VM test bench.

Δu activates the freewheeling diode D_1'. Properly chosen values of main and leakage inductances ensure that the freewheeling current mainly remains in coil 1. In fact, the choice of

suitable values for these parameters is a crucial issue and will be discussed in detail in the coming subsection. After the dead time, IGBT a_1' is not switched on by the high level transition of its gate signal and the positive load current continues flowing through diode D_1'. Since all coils are wound around the same magnetic core, as soon as the second PWM pulse switches on IGBT a_2, the current commutates from D_1' IGBT to a_2, due to the influence of the main inductance L_m of the coils. After the commutation, IGBT a_2 conducts the full load current, which now flows through the second coil. The same process repeats in the other meshes, when turning on or off the corresponding IGBTs.

The proper operation of the coupling inductor has been verified experimentally. Figure 3.6 presents the current waveforms obtained with the PWM pattern previously considered and a positive load current. The PWM frequency is 16kHz, which reduces the switching frequency of an individual IGBT to 3.2kHz. Within a switching cycle, each current waveform exhibits a main and four small current pulses. During the first part of each main pulse, the upper IGBT of the related half bridge is active and conducts the load current. After the falling edge of the PWM signal, the freewheeling diode of the same half bridge takes over and conducts the current until the next IGBT is turned on. According to the results in figure 3.6, it turns out that, during



(a) Turn-off process of a freewheeling diode in sequential switching operation mode

(b) Turn-on process of an IGBT in sequential switching operation mode

Figure 3.7: Soft switching of diode and IGBT during the commutation process under sequential switching operation mode

every PWM period, a small part of the load current also flows through inverters which should normally not be active. This results from the voltage across the mutual inductance Δu_m existing in every coil simultaneously as a consequence of the transformer effect. This is the reason why four small current pulses can be observed in every current waveform. However, since they do not contribute much to the switching or conducting losses, they are of no concern.

Furthermore, the proposed freeweeling control scheme makes the turn-off process of the diode and the turn-on of the IGBT independent of each other. The coupling inductor limits the current variation $\Delta i/\Delta t$, thus reducing the reverse recovery current of the diode. During the commutation, an IGBT switches on at zero current (see Figure 3.7) and its current then rises with the same slope as the diode current decreases. As the total voltage drop is shared in the same proportion between the two coupling inductances involved, the voltage of the IGBT and

diode are zero during the switching process. This phenomenon, known as *soft switching*, leads to a further decrease of the switching losses.

As mentioned, in the case of five IGBTs connected in parallel, the turn-on time of every power electronics component is limited to a fifth of the switching period T_{IGBT}, reducing its conduction losses over this time interval. Decreasing conduction and switching losses at the same time allows the power capability and modulation frequency f_{PWM} of the system to be further increased without exceeding the maximum power ratings of the individual power electronic devices.

Despite rising material costs due to the additional components, these advantages make sequential switching attractive for projects with low piece numbers and sustained development efforts and justifies its use in the frame of the presented project. However, a solution involving standard two level voltage source inverters (VSIs) rather than a specific design would be preferable in case of the VM, since it should remain flexible and hence, its structure independent of the power range of IUTs used.

3.2.3 Parallel cumulation of voltage source inverters

In the previous section, five IGBT inverter legs are parallel magnetically coupled under the help of *magnetic freeweeling control*, and are sequentially switched with a switching frequency of fifth of the overall modulation frequency. For the same purpose, the possibility of coupling VSIs in parallel by means of the aforementioned magnetic freeweeling control scheme has been examined using an experimental rig involving 5 standard three-phase VSIs. The half-bridge outputs of the five inverters were connected together according to the schematic diagram shown in Figure 3.8. To do so, a separate coupling inductor following the same design as in the previous configuration was used for each phase A, B and C (shaded boxes in Figure 3.8).

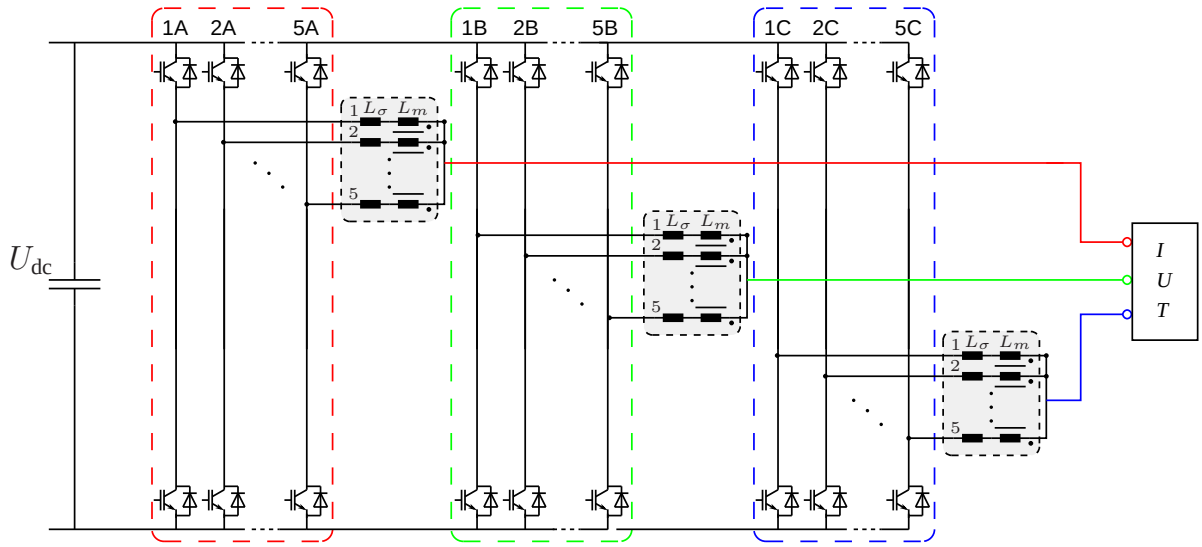


Figure 3.8: A simplified power stage structure of a sequential-switched 3-phase VSI.

In order to verify the proper operation of the system described in Figure 3.8 and assess the benefits arising from sequentially switching inverters connected in parallel in terms of energy

loss reduction, thermal investigations were carried out. More precisely, the array of inverters was first operated at a PWM frequency $f_{\text{PWM}} = 24\text{kHz}$ and at 10% overcurrent during 16 minutes. After that, the PWM frequency was increased to $f_{\text{PWM}} = 40\text{kHz}$, making the switching frequency of each IGBT equal to $f_{\text{S}} = 8\text{kHz}$, i.e. its rated switching frequency. The blue curve

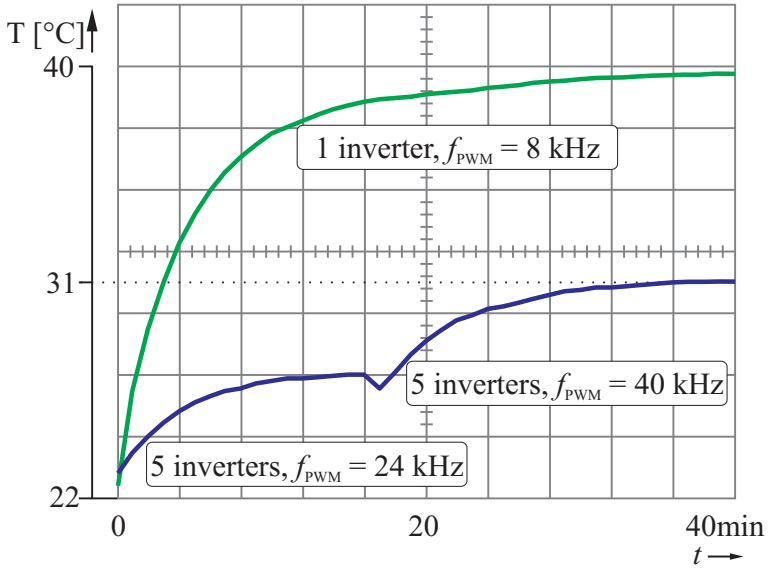


Figure 3.9: Measured temperature of the cooling fins in normal and sequential switching mode.

in the diagram in Figure 3.9 shows the evolution of the temperature measured on the heat-sink of an inverter. On the other hand, the green curve represents the temperature of a single inverter operated at rated current and nominal switching frequency $f_{\text{S}} = f_{\text{PWM}} = 8\text{kHz}$. Owing to the diagram, a significant amount of energy is saved thanks to reduced conduction losses and soft switching in the inverter array, even at 40kHz. This validates the approach of using standard VSIs coupled magnetically and switched sequentially for the power stage of the VM.

3.2.4 Coupling inductor design

The coupling inductor is the key component of the magnetic freewheeling control. It performs two main functions: the sequential switching of freewheeling diodes and the current commutation between separate inverters. As described previously, the main inductance L_m guarantees the current commutation and supports the sequential switching of freewheeling diodes. Unfortunately, it also causes parasitic small current pulses in other branches at the same time (see Figure 3.6). Therefore, an optimal value of L_m has to be found. On the other hand, as the leakage inductance L_σ primarily allows the load current to flow through a single freewheeling diode, a fairly high value of L_σ is required to improve the sequential switching performance and compensate for the side effect caused by L_m.

As described in Figure 3.10, the magnetic flux generated by the three coils wrapped around a ferromagnetic E-core pair can be split into a main flux ϕ_m and a leakage flux ϕ_σ. Magnetic field lines belonging to the main flux ϕ_m form loops within the core, while lines leading to the leakage flux ϕ_σ are located in the non-ferromagnetic materials constituting the winding window. In the case exemplified in Figure 3.10, the three coils exhibit their own leakage flux referred to

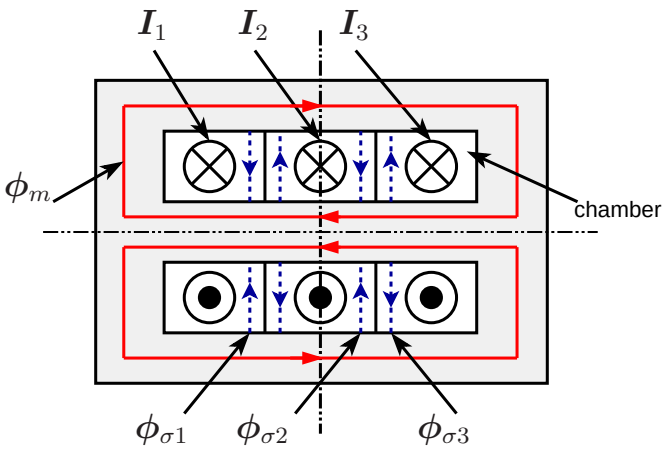
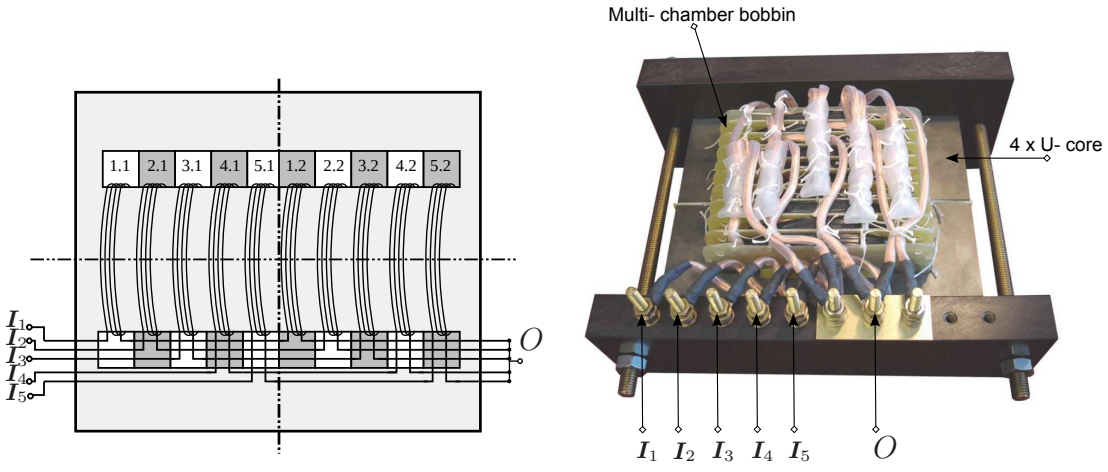


Figure 3.10: Schematic diagram of magnetic field loops in an E-core.

as $\phi_{\sigma i}$ ($i \in \{1, 2, 3\}$). As can be seen, leakage field lines of two neighbouring coils oppose each other, thereby weakening the leakage inductance of the coils. In order to attenuate this effect, a wide winding window allowing for sufficient distance between each coil is required. Moreover, according to [25], by using a special-designed multi-chamber bobbin with each coil wound in a different chamber, the interactions between them can be further weakened.

On the other hand, the spacial distance between coils and magnetic core strongly influences the value of the leakage inductance. Therefore, the distance between every coil and the distance of each coil to the magnetic core should be kept constant, as far as possible. The winding arrangement exemplified in figure 3.10, however, is not a good choice, because coil 2 has a larger distance to the core than coils 1 and 3. Discrepancies in leakage inductances as a consequence of this effect will have an adverse influence on the magnetic freewheeling control.



(a) Schematic representation of the windings in the coupling inductor

(b) Prototype of the coupling inductor

Figure 3.11: Winding arrangement of the coupling inductor

In order to alleviate this drawback, each coil is divided into two sub-coils connected in series

and wound in two separate chambers (see Figure 3.11(a)). By doing this, the average spacial distance between the coils and the magnetic core is approximately identical. In the particular case of the coupling inductor depicted in Figure 3.11(b), the width of the winding window was increased by using U-cores instead of a pair of E-cores. In practice, several configurations were tested in an iterative process until the desired freeweeling behaviour was achieved. Unfortunately, no systematic design guidelines could be found.

3.3 *Virtual machine*

The previous section mainly focused on hardware issues arising from the need for a high-performance power stage to satisfy the requirements of the VM (see Figure 3.8). However, since the VM has to mimic the electrical behaviour of a real motor at its terminals, a proper model allowing the RTS to control the power stage accordingly has to be designed.

3.3.1 Inverted machine model

As stated at the beginning, the VM should not attempt to enforce the phase currents since this would lead to conflicts with the current controller inside the IUT. For this reason, the model discussed in the following uses the phase currents as input quantities and computes the back-EMF which would be generated by a real asynchronous machine through which these currents would flow. The calculated back-EMF is then modulated by the power stage.

Using the notations introduced in [26], the voltage equations of an induction motor in stator coordinates are: (all symbols below are listed in Appendix A.1.

$$u_s^s = r_s \boldsymbol{i}_s^s + \frac{d\boldsymbol{\psi}_s^s}{d\tau} \tag{3.2a}$$

$$0 = r_r \boldsymbol{i}_r^s + \frac{d\boldsymbol{\psi}_r^s}{d\tau} + j\omega\boldsymbol{\psi}_r^s, \tag{3.2b}$$

and the flux linkage equations are:

$$\boldsymbol{\psi}_s^s = l_s \boldsymbol{i}_{\boldsymbol{s}}^s + l_h \boldsymbol{i}_{\boldsymbol{r}}^s \tag{3.3a}$$

$$\boldsymbol{\psi}_r^s = l_r \boldsymbol{i}_{\boldsymbol{r}}^s + l_h \boldsymbol{i}_{\boldsymbol{s}}^s. \tag{3.3b}$$

Rewriting the voltage equations with stator current $\boldsymbol{i}_s$ and rotor flux $\boldsymbol{\psi}_r$ as state variables yields

$$\tau_r \frac{d\boldsymbol{\psi}_r^s}{d\tau} + \boldsymbol{\psi}_r^s = l_h \boldsymbol{i}_s^s + j\omega\tau_r \boldsymbol{\psi}_r^s \tag{3.4a}$$

$$\tau_\sigma' \frac{d\boldsymbol{i}_s^s}{d\tau} + \boldsymbol{i}_s^s = \frac{k_r}{r_\sigma}\left(\frac{1}{\tau_r} - j\omega\right)\boldsymbol{\psi}_r^s + \frac{1}{r_\sigma}\boldsymbol{u}_s, \tag{3.4b}$$

where $r_\sigma = r_s + k_r^2 r_r$ and $\tau_\sigma' = \sigma l_s / r_\sigma$. Solving (3.4b) for $\boldsymbol{u}_s^s$ leads to the following relationship:

$$\boldsymbol{u}_s^s = r_\sigma \boldsymbol{i}_s^s + \sigma l_s \frac{d\boldsymbol{i}_s^s}{d\tau} + \underline{\underline{\frac{k_r}{\tau_r}\left(j\omega\tau_r - 1\right)\boldsymbol{\psi}_r^s}}. \tag{3.5}$$

Equation (3.5) can be represented by the equivalent circuit shown in Figure 3.12, while the underlined term in (3.5) corresponds to the back-EMF $\boldsymbol{u}_{ir}$:

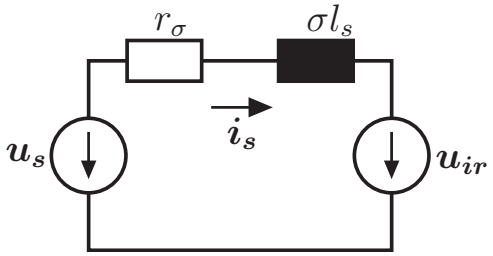


Figure 3.12: Equivalent circuit of an induction motor in stator coordinates.

$$\boldsymbol{u}_{ir} = \frac{k_r}{\tau_r}\left(j\omega\tau_r - 1)\right)\boldsymbol{\psi}_r^s. \tag{3.6}$$

In order to calculate the mechanical angular velocity ω, the mechanical equations (3.7) and (3.8) have to be added.

$$T_e = k_r \cdot \mid \boldsymbol{\psi}_r \times \boldsymbol{i}_s \mid \tag{3.7}$$

$$\tau_m \frac{d\omega}{d\tau} = T_e - T_L \tag{3.8}$$

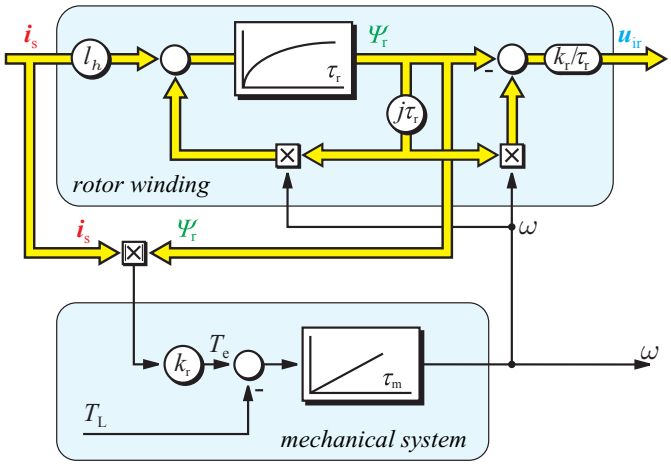


Figure 3.13: Current based machine model for evaluating the back-EMF and the angular velocity of the *virtual machine*.

The relationships between physical quantities gained from the previous equations are represented graphically in a block diagram in Figure 3.13. The stator current $\boldsymbol{i}_s$ leads to a rotor flux

ψ_r which, depending on the angular velocity ω, results in a back-EMF $\boldsymbol{u}_{ir}$. Owing to (3.4b), the current dynamics directly depend on the equivalent leakage inductance σl_s, which is, in the considered case, the inductance of the coupling inductor described in the previous section. According to equation (3.8), the angular velocity depends on a load torque T_L, which is actually an input quantity of the model. This offers the possibility of emulating arbitrary load conditions for the IUT. As will be demonstrated experimentally in the next section, this approach is able to represent the characteristics of a real machine.

3.4 *Inverter cumulation* implementation and *virtual machine* experimental verification

Based on the theoretical analysis of the previous section, a detailed schematic overview of the experimental rig built to test the proper operation of the *virtual machine* is shown in Figure 3.14.

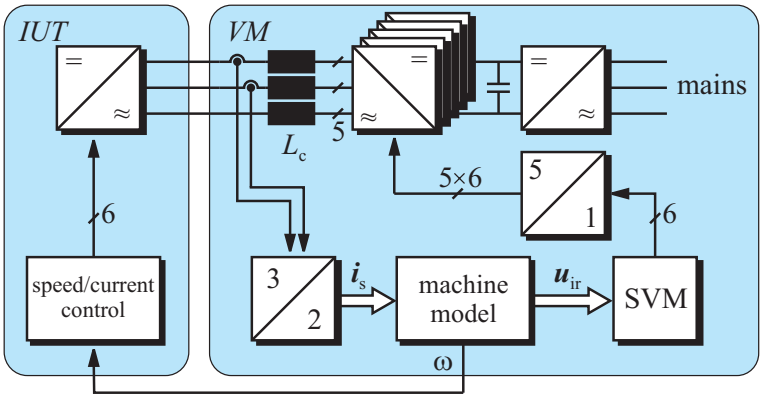


Figure 3.14: Overview of the components constituting the test bench of the VM.

It consists of five industrial standard 14kVA two-level VSIs switched sequentially and connected in parallel using three coupling inductors like the one depicted in Figure 3.5. The rated switching frequency of each inverter is $f_S = f_{PWM} = 8$kHz. The real-time algorithm of the machine model is implemented on a Digital Signal Processor (DSP). The model parameters can be set by means of a PC user interface (Figure 3.15). While the phase current measurements are sampled by the DSP, the load torque of the VM model can directly be modified during tests to emulate load steps. The back-EMF for each phase is available at a specific output pin of the DSP as a PWM voltage signal which is then distributed to the various inverters by an FPGA. The angular velocity, also computed by the DSP, is passed to a second FPGA emulating an incremental encoder. The delivered signals comply with the incremental encoder interface's standards (see Figure 3.16). Finally, as can be seen in Figure 3.17, the IUT used for testing the emulator is of the same type as the parallel connected inverters of the VM. It includes a field oriented controller.

The parameters of the induction machine emulated by the VM during the tests are listed in Table 3.1.

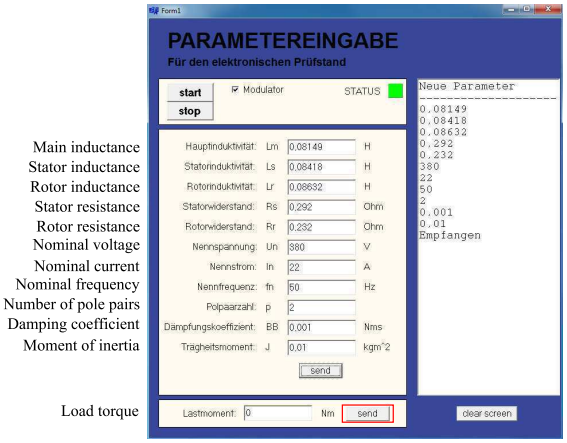


Figure 3.15: PC user interface for parametrizing the VM.

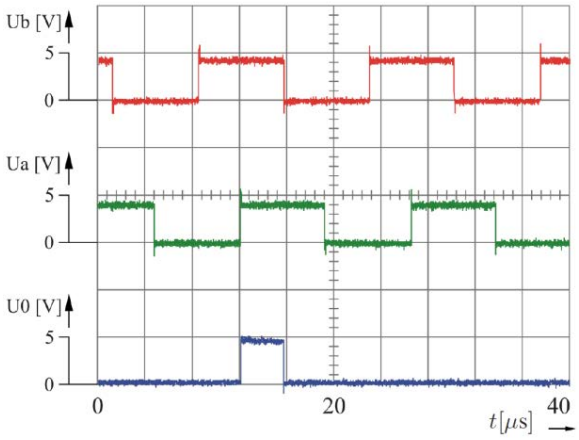


Figure 3.16: Signals delivered by the encoder emulator.

Table 3.1: Parameters of The *virtual machine*

$U_\mathrm{n} = 380\mathrm{V}$	$I_\mathrm{n} = 22\mathrm{A}$
$R_\mathrm{s} = 292\mathrm{m}\Omega$	$R_\mathrm{r} = 232\mathrm{m}\Omega$
$L_\mathrm{s} = 84.18\mathrm{mH}$	$L_\mathrm{r} = 86.36\mathrm{mH}$
$L_\mathrm{h} = 81.49\mathrm{mH}$	$f_\mathrm{n} = 50\mathrm{Hz}$
$J = 0.01\mathrm{kgm}^2$	$p = 2$

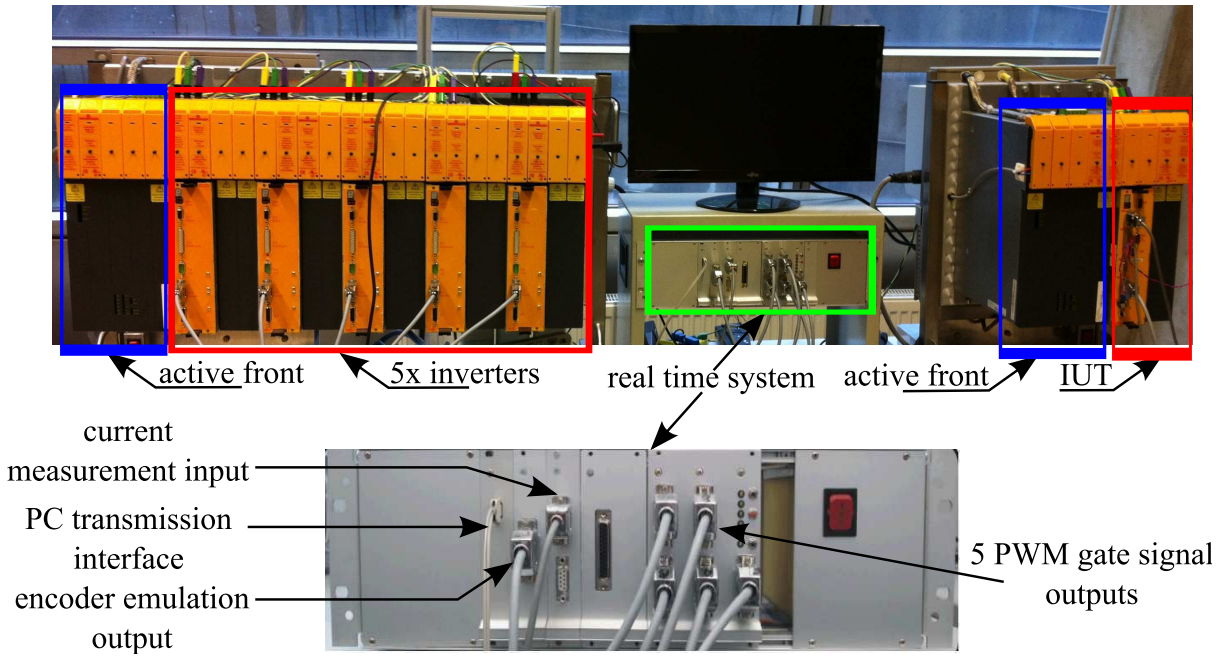


Figure 3.17: Experimental setup of the proposed motor emulator.

Figure 3.18 shows the evolution of stator currents, back-EMF, rotor flux linkage and angular velocity during a slow acceleration process from standstill to nominal speed under no load, when the IUT is operated in speed control mode. The field oriented controller of the IUT enforces speed and current, while keeping the amplitude of the rotor flux constant. As the actual speed increases up to nominal speed, the back-EMF also rises and reaches its nominal value. Fig. 3.19 depicts the results of a speed step from standstill to rated speed. These results are entirely consistent with the behaviour of a real asynchronous machine. As expected from acceleration tests, the IUT delivers its nominal current only during the short acceleration phase and hence, cannot be tested properly without load.

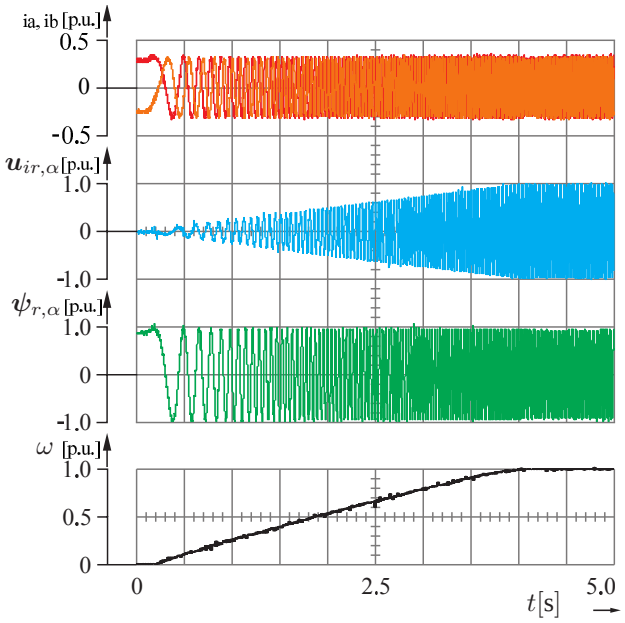


Figure 3.18: Stator currents, back-EMF, rotor flux linkage and angular velocity when accelerating from standstill to nominal speed.

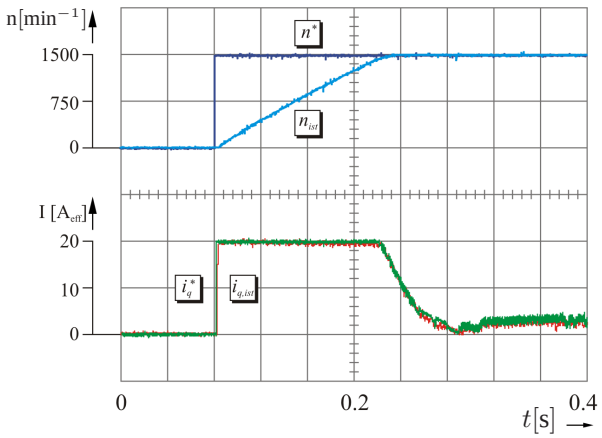


Figure 3.19: Reference and actual values of speed and q current component resulting from a speed step from standstill to rated speed at no load.

The diagram in Figure 3.20 displays the evolution of angular velocity and q current while applying a load step with an amplitude equal to 75% of the rated load torque at nominal speed. At time $t = 0.08s$, the load torque step is emulated by the VM. The speed controller of the IUT reacts with a current i_q to counteract the resistive torque and keep the speed constant. Therefore, the possibility of emulating mechanical energy transfers with the VM enables to test the IUT under realistic operating conditions.

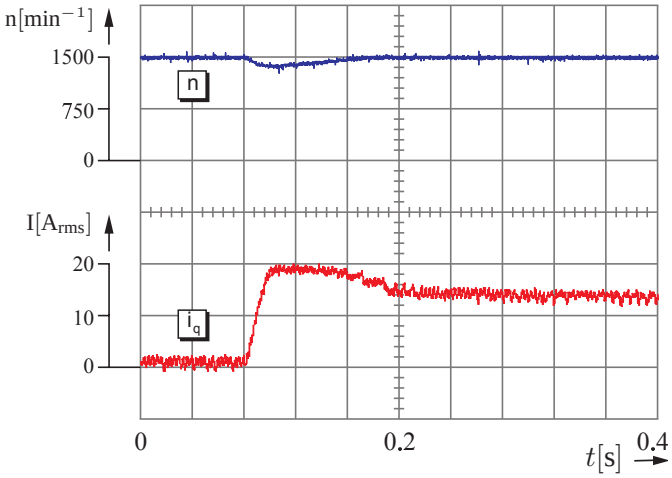


Figure 3.20: Load step of 75% rated torque at nominal speed.

Figure 3.21 shows the ability of the VM to operate not only at rated flux amplitude but also in the flux weakening region. As expected, the current controller of the IUT keeps the d current constant at its nominal values as long as the speed reference does not exceed its rated value. However, when the speed reference is increased beyond this threshold, the rotor flux has to be reduced to limit the back-EMF.

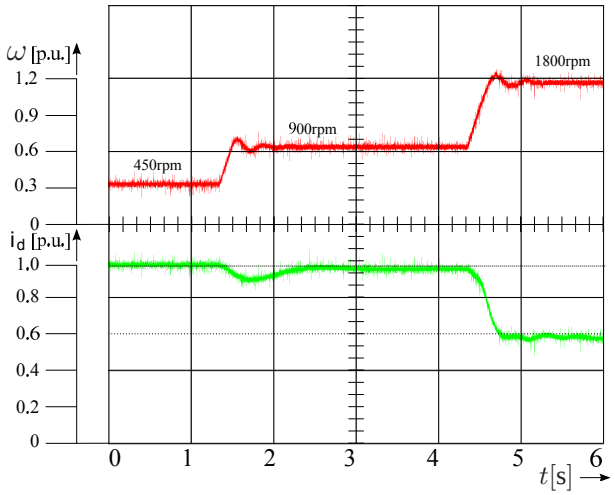


Figure 3.21: Evolution of d current and angular speed at constant flux and in the flux weakening region.

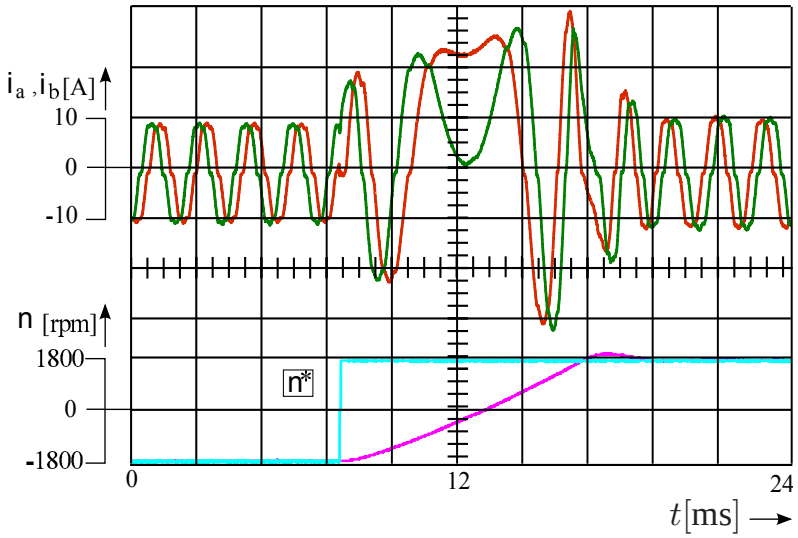


Figure 3.22: Evolution of the stator current and the angular velocity during a speed reversal from -120% to 120% of the nominal speed.

Figure 3.22 displays the evolution of the stator currents of the VM during a speed reversal from -120% to 120% of the nominal speed. Again, the results are absolutly consistent with the behaviour of a real motor.

3.5 Summary

The investigations carried out with the motor emulator presented in this chapter attest to the possibility of a magnetically coupled *inverter cumulation* system. This method does not only allow increasing the overall system modulation frequency but also leads to an appreciable reduction in overall losses since power electronics devices exhibit a soft switching behaviour under these circumstances. Experimental results show that the performance of fiver inverters cumulated in parallel in terms of power and dynamics are sufficient to realize an efficient power hardware-in-the-loop emulator of induction motor.

A crucial feature of the *Virtual Machine* is its ability to be operated with an IUT working with a field oriented controller. This has been made possible by using a model computing the back-EMF as a result of the currents enforced by the IUT. Doing so, the electrical behaviour of the VM is in perfect agreement with the one of a real machine. Furthermore, mechanical torque steps can be reproduced, allowing the IUT to be tested under almost every possible operating conditions.

Thanks to its simplicity and flexibility, the *Virtual Machine* provides an interesting alternative to expensive HiL emulators for testing power inverters. It is particularly suitable for Small and Medium Enterprises manufacturing inverters and seeking for an affordable way of testing their products.

As discussed at the beginning of this chapter, *inverter cumulation* is parallel, series and cas-

cade interconnection of identical or different inverters, which can extend the system overall performance. The success of the project *virtual machine* inspires us to explore deeper in the field of *inverter cumulation* by going beyond the cumulation topology. The new idea and project are going to be presented in the following chapter.

CHAPTER 4

Introducting series magnetic-coupling of inverters with different characteristics

As illustrated in chapter 2, for the most industrial applications, there is a certain suitable power semiconductor which satisfies all the performance requirements. However, the situation is different when taking the power hardware-in-the-loop system into account. A specific example is the power grid emulator which requires a high power rating **and** high dynamic response power electronics system.

4.1 Power grid emulator

The increasing use of complex grid-connected technological components in safety-critical applications like public transportation or distributed power systems requires a precise evaluation of the reliability and robustness of these equipment during their development. Direct on-field tests of high power systems are generally not possible. A conventional method of getting around this problem consists in using software-based simulation to analyse the behaviour of the electric equipment under test (EUT) under normal and transient operation conditions of the grid. However, signal-level simulation is not able to perfectly reproduce every detail of a physical phenomenon.

A grid emulator is a controllable AC power source which is capable of reproducing not only the grid's behaviour under normal operation conditions but also during transient operation. Therefore, it emulates the power grid with the real power transfer, and thus reproduces the real physical environment for the equipment under test. It is believed to be a better solution for factory inspection of the grid-connected industrial applications.

It is very important for a grid emulator to generate several typical fault behaviours to test the reliability and robustness of the EUT. These faults include under-voltage, voltage interruption, frequency variations, unbalance voltage, voltage harmonics, spikes and noise. In Figure 4.4-4.6 several simulation results are shown.

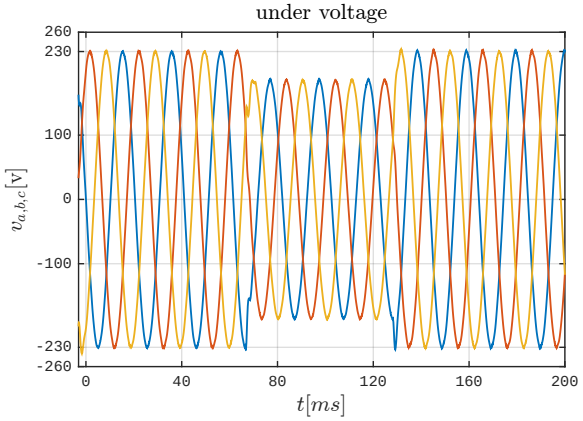


Figure 4.1: 20% under voltage fault for 60ms.

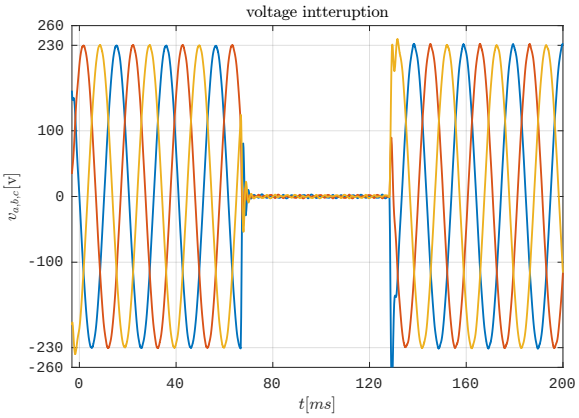


Figure 4.2: 0v voltage intteruption for 60ms

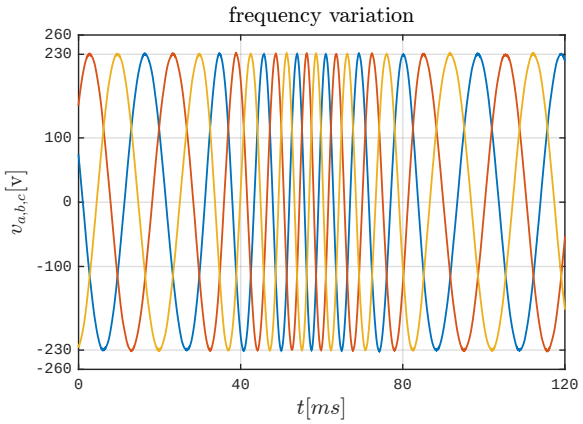


Figure 4.3: Frequency variation fault in 40ms

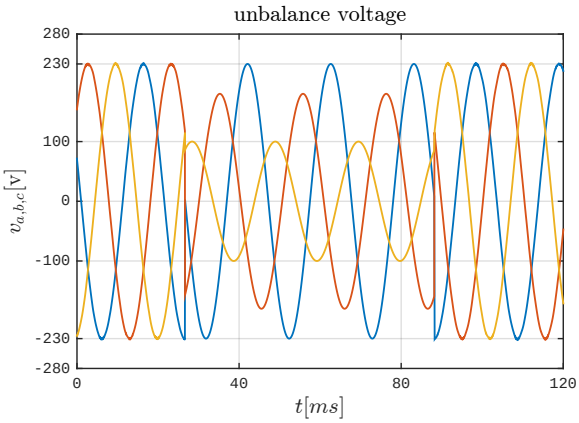


Figure 4.4: Voltage unbalance fault($v_a = 230\text{v}, v_b = 170\text{v}, v_c = 100\text{v}$)

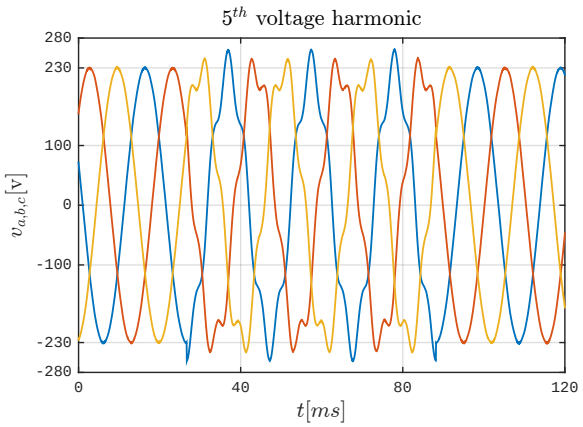


Figure 4.5: 5^{th} harmonic superimposition.

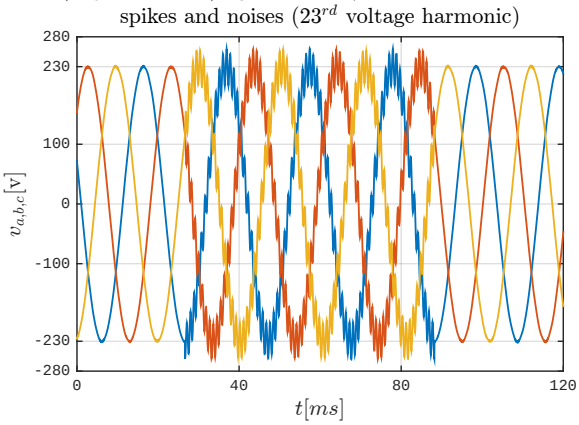


Figure 4.6: Very high order harmonic superimposition — noises and spikes

The four different types of grid emulators used in past are amplifier-based, transformer-based, generator-based and thyristor-controlled-reactor-based(TCR) [27]. The first grid emulator amplifies the desired signals generated by a waveform generator to the required power level. It can emulate all the typical grid faults, but due to the high amplifier cost it is very expensive. The transformer-based grid emulator can only generate voltage waves with different amplitudes, therefore it is not able to emulate frequency variation and harmonic superimposition [28]. The working principle of the third type of emulators is clear and self-explained. By controlling the working condition of the generator, different amplitudes of the output voltage waves are produced. However, by taking the cost, weight and size of the generator into account, it is not an efficient solution [29]. The TCR is able to change its branch impedance by controlling the firing angles of the thyristors. Due to this variation of impedance, the load voltage can be changed [30]. But this produces losses on the impedance, and the control algorithm of the thyristor is strongly dependent on the whole system parameters.

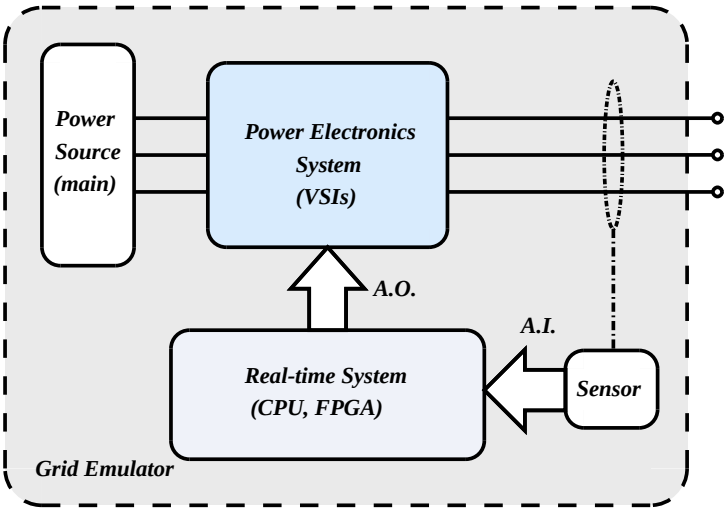


Figure 4.7: Basic schematic of a power converter based grid emulator system.

Due to the fast development of power electronics systems during last several decades, the voltage source inverters (VSI) based system is becoming a very competitive realization method of the grid emulator. The principle diagram of the whole system is shown in Figure 4.7. It includes VSIs (switching-mode power electronic amplifier), a real-time control system and analog-signal (voltage and current) sensors. A mathematical model of the power grid is implemented inside the real-time controller, and the switching-mode power electronic amplifier is modulated according to this model to generate desired voltage signals.

4.1.1 Challenges of voltage source inverter system based grid emulator

Firstly, the most important requirement of a power grid emulator is to be capable of supplying sufficient power to the grid-connected equipment. It naturally depends on the power rating of the applications, but should be as large as possible. Therefore a higher power power electronics device is necessary.

Secondly, the output voltages of a voltage source inverter are pulses with finite potentials under the PWM modulation method. It only ensures that the average voltage per switching interval equals the user defined reference value. For that reason, a shorter switching interval always results in a better quality of the output voltage. However, a shorter switching interval means a faster switching frequency, and the switching frequency is normally set to several ten times higher than the fundamental frequency. If the grid emulator only controls the 50Hz component, the switching frequency of the VSIs system is around several kHz. In this case, it is not a big problem for the modern power electronics devices and processor-based real-time controller. However, for the high order harmonics emulation (Figure 4.6), if one still wants to keep the same ratio of f_s/f_1, then the switching frequency increases easily more than 50kHz. It becomes critical for the switching components to survive with the desired high power ratings.

Taking both aspects mentioned above into account, the high power and high dynamics response are the two simultaneous desired characteristics of the grid emulator. As illustrated in Chapter 2, power and dynamics are two mutual exclusive characteristics for the power semiconductor device manufacturing. However, as shown in Figure 2.3, there is always a solution of either high power or high switching device. For example, the IGBT and MOSFET devices are respectively used in these two different occasions. Due to the physical limitations of the semiconductor, high power and high switching devices are technically difficult or impossible to produce as the result of this bottleneck. Therefore, it is really challenging to construct such a system with both of these characteristics by using any one of the current market-available devices.

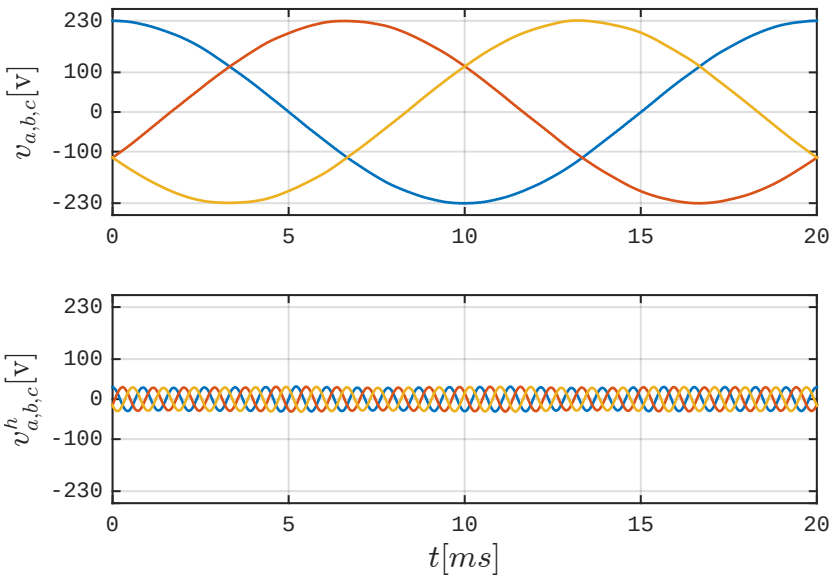


Figure 4.8: Fundamental and harmonic components separation.

Before searching for a solution to this problem, it is better to examine the requirements of the grid emulator in detail. The most critical point is the high order harmonics emulation. The emulator is supposed to control not only the 50Hz fundamental high power signal but also the harmonics whose frequencies are several ten times higher than the fundamental frequency. By separating the harmonic component from the fundamental wave, Figure 4.6 can be re-plotted as

Figure 4.8. As can be seen from the result, the high order harmonic emulation is composed of the high power fundamental 50Hz component and high frequency low amplitude signal.

Based on the analysis above and the different strengths of IGBT and MOSFET power switching devices, an idea is developed naturally. The emulation of the high power fundamental behavior can easily be realized by using a commercial high power inverter with low switching frequency semiconductors (e.g. IGBT). On the other hand, a low power inverter (e.g. MOSFET) showing high dynamics generates high order harmonics behavior .

4.2 Original idea of series magnetic-coupling of inverters with different characteristics

The original idea comes from the applications of a dynamic voltage restorer (DVR) [31–33], the purpose of which is to protect sensitive loads from the effects of grid voltage disturbance, and a series active filter (AF) [34], used to compensate the voltage harmonics distortion generated by the non-linear load. The principle topologies of both are quite similar, which is shown in Figure 4.9. An auxiliary converter based power convention system which is magnetically-series connected in between the power grid and the load is modulated to inject desired voltages into the grid and the load.

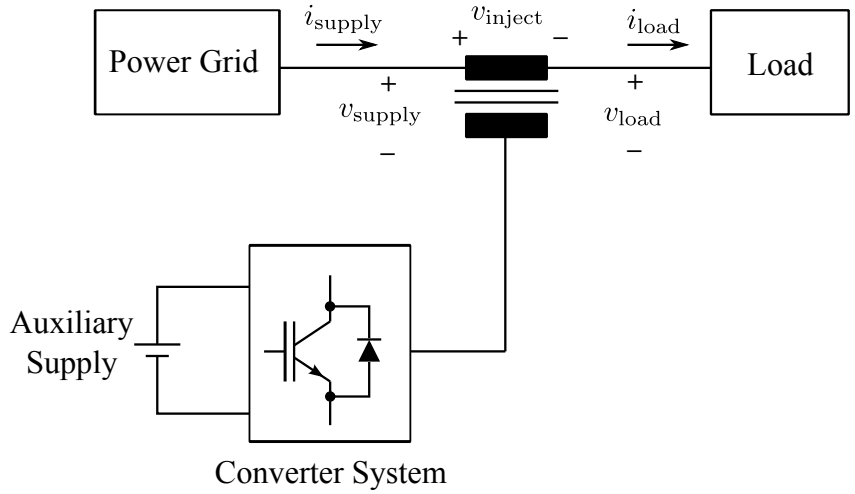


Figure 4.9: Principle topology of the dynamic voltage restorer (DVR) and series active filter.

By using the coupling inductor, the converter-generated voltages are superimposed on the grid fundamental waves. It naturally inspires a solution to our problem illustrated in Section 4.1.1. As mentioned above, realizing a hardware emulation system with a single type of standard power electronic device is particularly challenging. However, on the one hand, high power inverters with a low switching frequency are common products (e.g. IGBT) on the market, and, on the other hand, low power inverters with high dynamic behavior could also be easily constructed with standard market-available power electronic devices (e.g. MOSFET). Moreover, the desired emulation fault waves (voltage and current) of utility grid spikes and noises can be split into two categories:

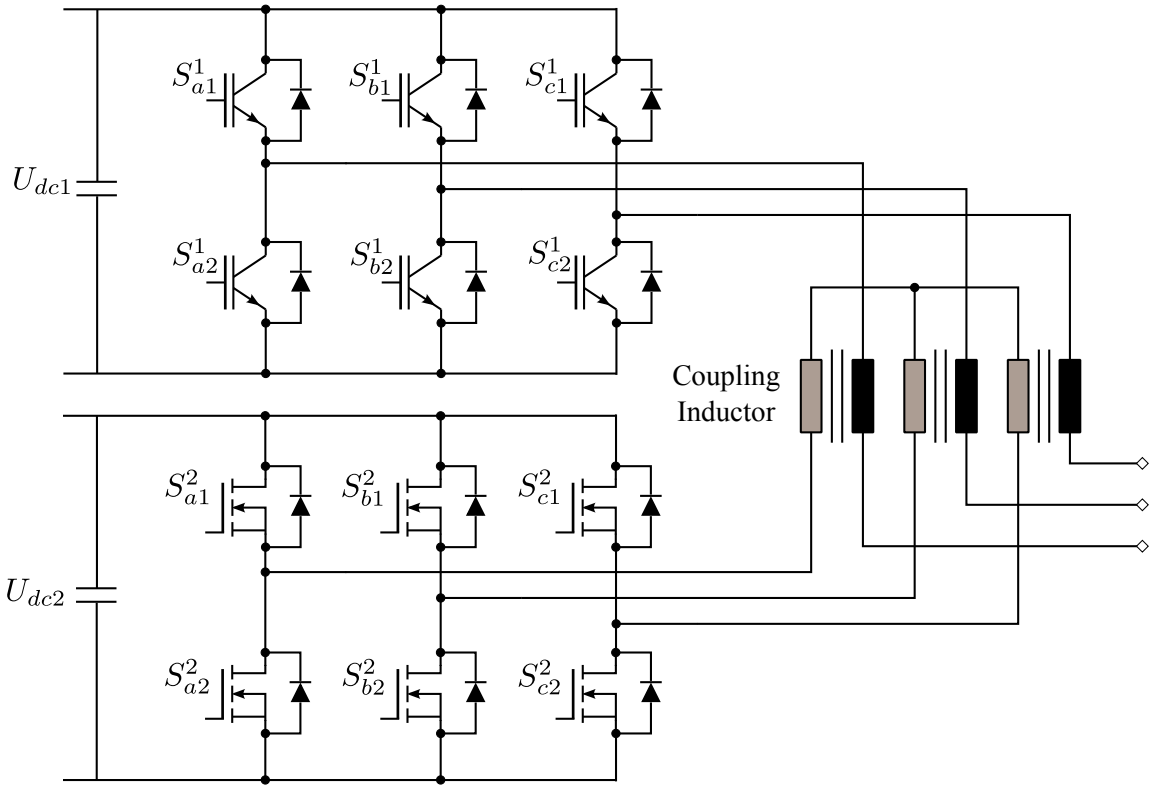


Figure 4.10: Original topology schematic of series magnetic-coupling inverters.

1. high power but low frequency fundamental component.
2. low amplitude but high order harmonic component.

Therefore, by using two cumulated inverters with complete different characteristics (shown in Table 4.1) to generate the above mentioned two waves respectively, and superimposing them together afterwards via a magnetic coupling inductor, a good solution for a high power and high dynamic response amplifier of a PHiL application is reached. Figure 4.10 shows the original topology schematic of the concept of series magnetic-coupling inverters.

Table 4.1: Electrical Specifications of The Inverter Cumulation System

	IGBT Inverter 1	MOSFET Inverter 2
U_{dc}[V]	580	50
f_{s}[kHz]	8	50
f_1[Hz]	50	1250
$V_{\text{ph,max}}$[V]	110	25

Since the power amplifier of the PHiL emulates the behavior of a utility grid, a high-quality sinusoidal output of the system is required. However, the most common used PWM modulated switch-mode converter suffers from massive switching component distortion at its output terminal (as shown in figure 2.7). Therefore, in order to eliminate this problem, an output filter

for the PWM inverter is very important for the final realization of the grid emulator. The output filter of the inverter will be discussed in detail in the later section of this chapter. As shown in the figure below, the first attempt of a grid emulator is implemented. Before moving forward, the next section will show the problems of this topology.

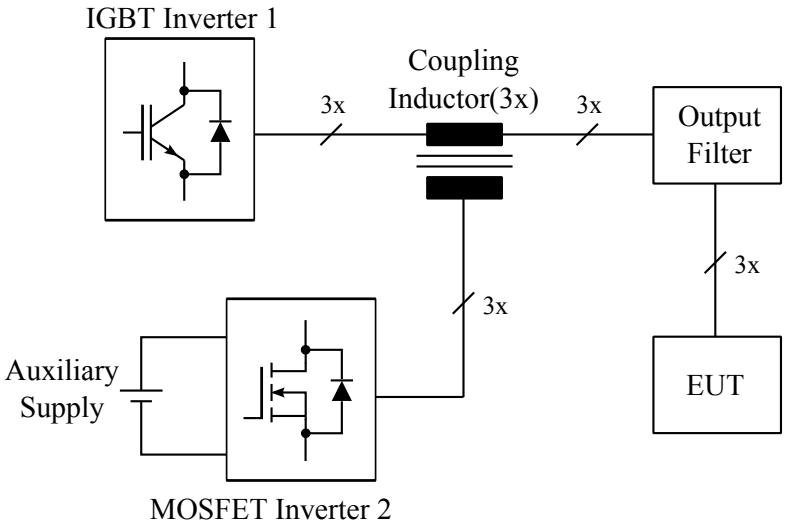


Figure 4.11: First attempt of the grid emulator.

4.3 Failure of the first attempt series *inverter cumulation* system and modified topology

If one compares the topology shown by Figure 4.11 with traditional applications like a dynamic voltage restorer (Figure 4.9), it is obvious that they are quite similar, except that an IGBT inverter replaces the power grid in the first case. The idea is clear and straightforward. The IGBT inverter is used to emulate the fundamental behavior of a utility grid.

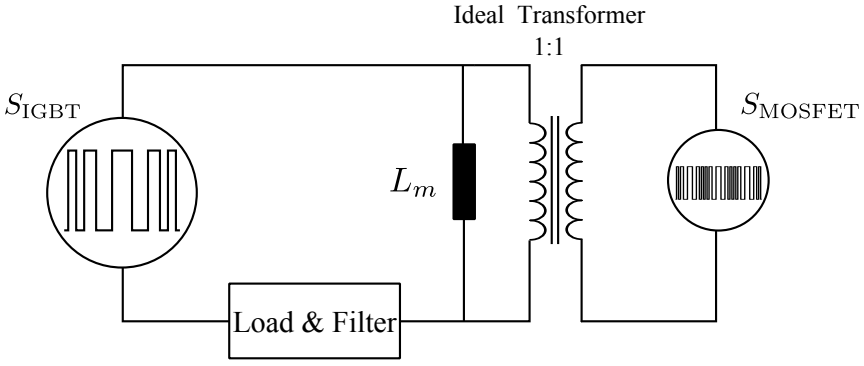


Figure 4.12: Single phase equivalent circuit of the inverter cumulation system.

A simplified single phase equivalent circuit is shown Figure 4.12. The coupling inductor is represented as an ideal 1:1 transformer with a magnetic inductance L_m in parallel. All the

other stray inductance and winding resistance are neglected for a simplified analysis. The IGBT and MOSFET inverters are represented by two pulse voltage sources. The functionality of the MOSFET inverter is easy to observe. The coupling inductor is able to transfer the high order harmonic waves from the secondary to the primary winding where the magnetic inductance L_m cannot be neglected. Because of the superposition principle, the voltage of the load and filter is the combined effect of both voltage sources S_{IGBT} and voltage across the magnetic inductance v_{L_m}.

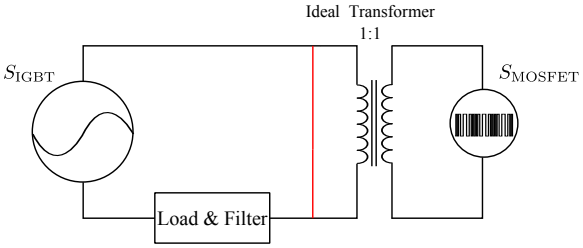


Figure 4.13: Fundamental component model of the equivalent circuit.

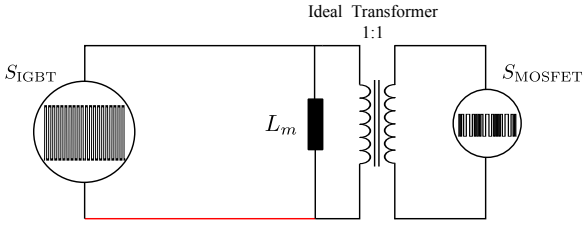


Figure 4.14: Switching component model of the equivalent circuit.

However, due to the smaller voltage and power ratings of the MOSFET inverter, it becomes very critical to ensure that it works without any danger (over-voltage risk) from the IGBT inverter in any operation mode. Because there are various frequency components in the circuit, it is better to discuss them respectively. As discussed before, the output waves of the voltage source inverter are PWM pulses which are composed of fundamental wave and switching-frequency range components. For the fundamental frequency wave, the frequency ω is only 50Hz, the impedance of ωL_m is negligible compared with the load and viewed as short-circuit (shown as in Figure 4.13). Therefore, the fundamental wave of the IGBT inverter has no interference to the MOSFET inverter.

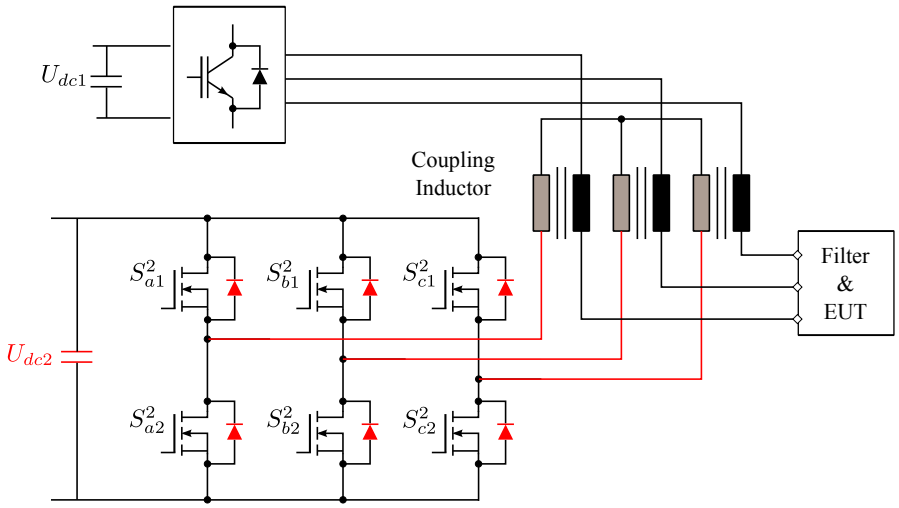
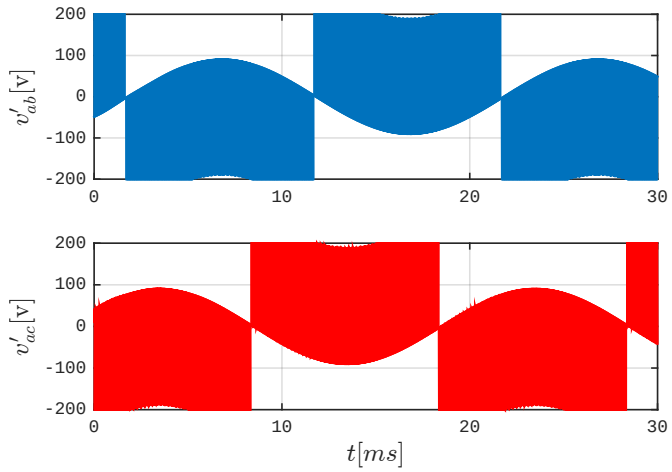


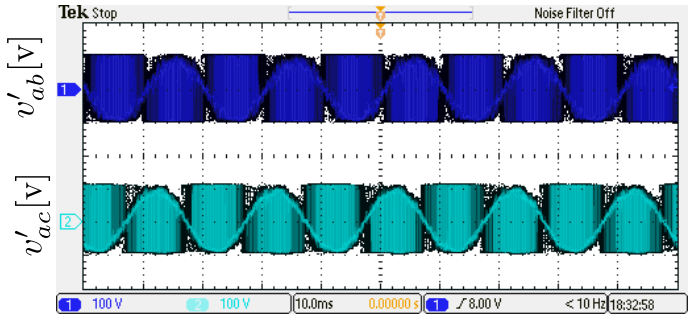
Figure 4.15: The MOSFET inverter acts like a rectifier.

But when it comes to the switching-frequency components, the situation becomes totally dif-

ferent. The impedance of $\omega_{sw} L_m$ increases dramatically to a huge value, and the load becomes negligible in this case. Therefore the circuit topology is changed to the form shown in Figure 4.14. Unfortunately, the ideal transformer reflects this high voltage and frequency components to the MOSFET inverter side. This is very hazardous for the inverter with a lower voltage rating! If the line to line voltage is bigger than the DC-link voltage, the inverter acts as a diode rectifier even if all the switches are disabled, and the DC-link will be quickly charged up beyond the voltage rating of the power stage (Figure 4.15). This effect results in a serious failure of the additional power source of the MOSFET inverter and the functionality of whole grid emulator.



(a) simulation



(b) experiment

Figure 4.16: Secondary terminal voltages of the coupling inductor.

At the initial phase of this project, several experiments were carried out based on this first version topology because of carelessness of this issue, and the power supply of the MOSFET inverter was seriously damaged. The following simulation and experimental results verify the theoretical analysis above. The IGBT inverter is controlled to generate 100V sinusoidal phase voltage. The voltage waves v'_{ab}, v'_{ac} measured at the secondary winding terminals of the coupling inductor are shown in Figure 4.16. The experimental and simulation results showed good agreements. Due to the limited measure range of the voltage probe, the signal information beyond 100V is missing. However, it is still clear that the coupling inductor transfers all the high frequency and voltage components to the secondary sides, and it actually acts as a low-pass L-filter in front of the EUT and filters. It is clear to see that there is a low frequency envelope

which is the compensation of the fundamental signals passed to the downstream circuit. Figure 4.17 explains this phenomena graphically.

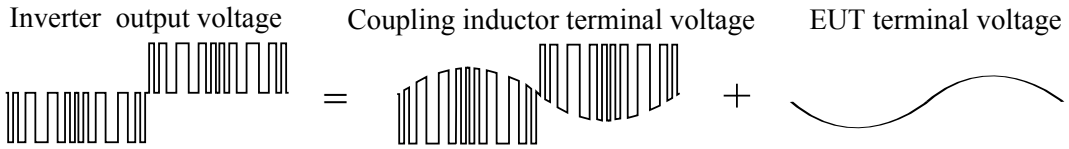


Figure 4.17: Voltage signals split.

All the analysis above reveals a truth: the coupling inductor reproduces the high voltage high frequency components of the IGBT high power inverter at the terminals of the low voltage MOSFET inverter, and due to this interference the MOSFET inverter acts as a diode rectifier which charges up the DC-link quickly beyond the withstand value. Therefore, the switching-frequency range components of the inverter output voltage will cause serious problems. This is the key difference between the DVR or AF applications and our proposed grid emulator.

After understanding the reasons for the first failure, the solution of this problem is easy to find out. It is very important to attenuate all the high frequency components before supplying to the coupling inductor. Therefore, output filters should be added in front of the coupling inductor instead of after it. The modified grid emulator topology is shown in Figure 4.18.

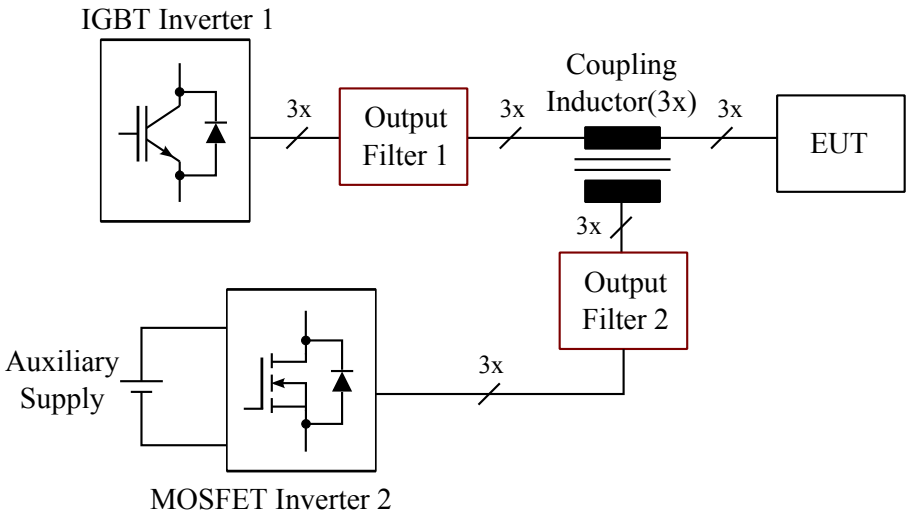
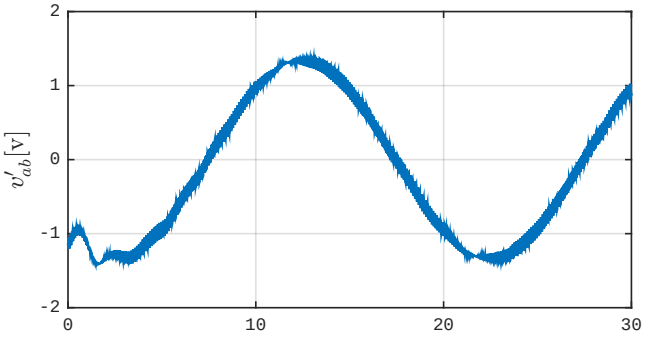


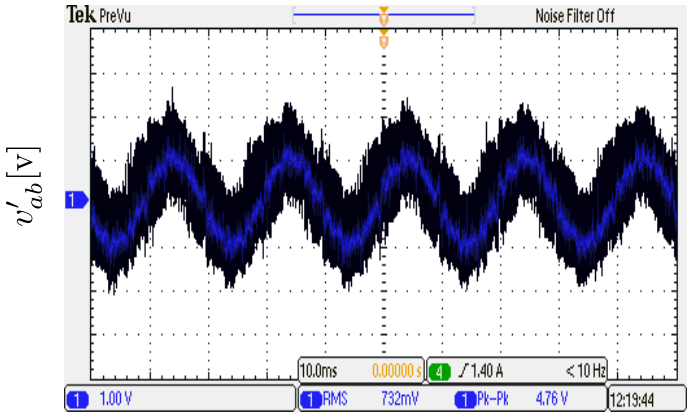
Figure 4.18: Topology of the series magnetic cumulation of inverters with different characteristics.

Two low-pass filters are used to attenuate the switching-components of both inverters. In this case, the coupling inductor is mainly used to couple the fundamental components of the two inverters. Because the fundamental frequency of the MOSFET inverter is several ten times higher than 50Hz, it is better to use the frequency difference to design the coupling inductor which is more sensitive or functional to the frequency components of the MOSFET inverter. In other words, the coupling inductor should be more efficient to transfer the MOSFET inverter frequency components to the IGBT inverter side. On the contrary, the 50Hz components of the IGBT inverter should interfere with the MOSFET side as less as possible. In order to avoid

the previous damage of the MOSFET inverter DC-link, the same simulation and experiment were done, and the result is shown in Figure 4.19. As can be seen, the 50Hz component has a very low amplitude (around 1V), and is caused by the winding resistance and the magnetic resistance of the coupling inductor. And the high frequency component is attenuated to a small amplitude after the output filters. By doing these, the MOSFET inverter should be safe during the operation. But this is still not the full story for the protection of it, because only steady states are considered so far.



(a) simulation



(b) experiment

Figure 4.19: Secondary terminal voltages of the coupling inductor (modified topology.)

The start-up, fault trip and fast transient of the IGBT inverter with high di/dt will be amplified by the coupling inductor L_m, and a secondary voltage with high dv/dt which results in a severe working condition for the MOSFET inverter. Moreover, ideally, with respect to the IGBT inverter, the coupling inductor operates as a current transformer. The primary side is in series with the output terminal, therefore under load condition, an uninterrupted current continuously magnetizes the core of the coupling inductor. The secondary side must maintain a continuous current path to balance the primary magneto motive force (MMF), otherwise an open-circuit secondary winding generates substantial voltage.

As shown in Figure 4.20, the protection approaches are explained as following:

- Fast diode prevents the reverse current to the DC source. Power zener diode buffers the DC-link voltage of MOSFET inverter.

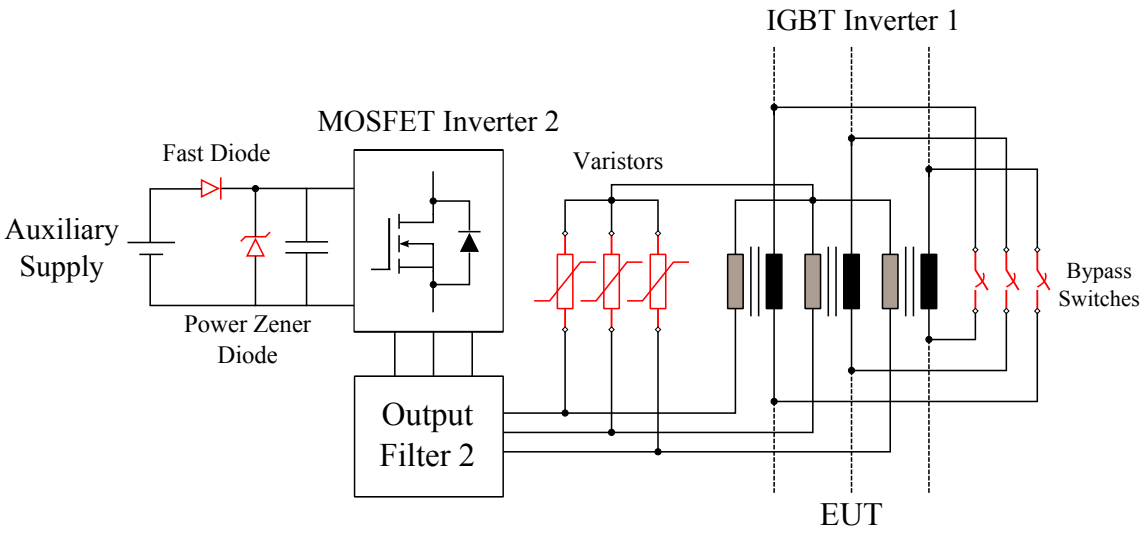


Figure 4.20: Protection circuits of the MOSFET inverter.

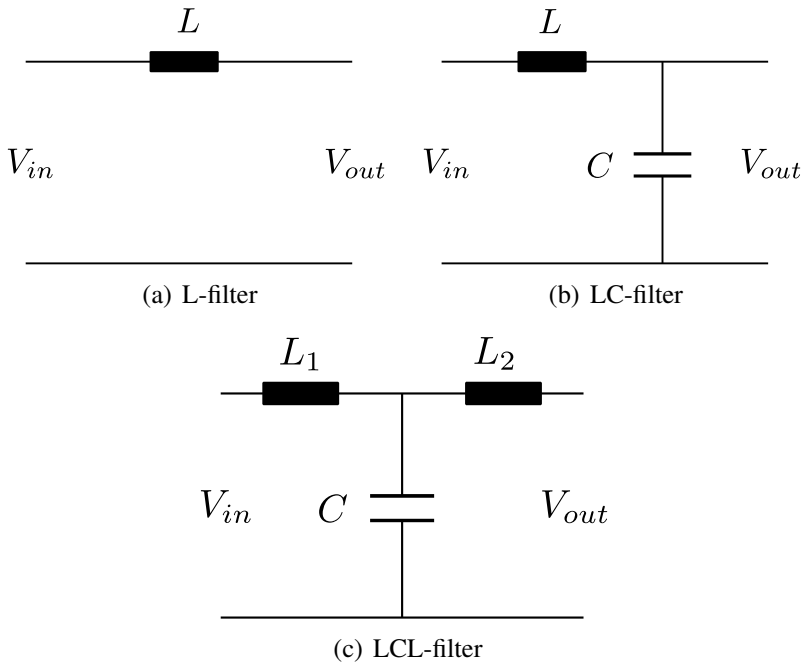
- Varistors clamp the transient over voltage of the coupling inductor.
- During the start or stop transient of the IGBT inverter, switches by-pass the coupling inductor.
- In order to maintain a continuous current path, the MOSFET inverter is always switched to the NULL state during standby.

4.4 Output filter of the voltage source inverter

Based on the previous discussion, it is very important to attenuate the high frequency components in the output voltage of a PWM inverter by using an output filter. This section investigates the output filter topologies, design approaches and operation stability in detail. The passive harmonic output filter is widely used in the grid connected inverters to reduce voltage harmonics and current distortions. The output voltage and current waves of a PWM modulated inverter have various kinds of harmonics:

- Low frequency harmonics,
- Switching frequency harmonics,
- High frequency harmonics.

Each category harmonic must be sufficiently and appropriately attenuated [35]. The proposed grid emulator is supposed to behave as a sinusoidal AC controllable voltage source. The harmonics generated by the PWM inverter have to be attenuated exactly like the grid-connected converter. Therefore, the passive output filter used as the interface of distributed generation application will be adopted also for this grid emulator project. There are three main filter topologies: L, LC and LCL filter which are shown in Figure 4.21



(a) L-filter (b) LC-filter

(c) LCL-filter

Figure 4.21: Three main existing harmonic filter topologies.

The first order L-filter attenuates the input wave with a slope of -20dB/decade over the whole frequency range. It is the simplest current filter topology of a grid connected voltage source inverter. Because of the moderate attenuation capability of the first order L-filter, the switching frequency of the overall system should be very high, in order to achieve a satisfactory harmonic rejection. However, if taking the complexity of the control algorithm and dynamic response into account, an L-filter is still a good solution as a current harmonic filter for the distributed energy generation applications like wind and solar power converter systems.

An LC second order filter exhibits a better -40dB/decade attenuation compared to the L-filter. A shunt capacitor is added at the output terminals, the capacitor voltage is the output voltage of the filter system. Therefore an LC-filter is widely used in the UPS applications which require output voltage control and harmonics rejection since the shunt capacitor and the series inductor have a resonant effect. The resonant frequency is calculated by

$$\omega_{res} = \sqrt{\frac{1}{LC}}. \tag{4.1}$$

The value of inductance and capacitance must be well designed to achieve a good attenuation of switching frequency components, and meanwhile avoid the instability of the system due to the resonance of a two order system. Furthermore, the shunt capacitor consumes more reactive power compared to the L-filter. Due to the close relevance of proposed grid emulator, the modelling and design procedures will be discussed later.

An LCL filter give the best performance for switching harmonics attenuation in three topologies. The current distortion and reactive power is low. Due to the -60dB/decade attenuation slope, lower switching frequency and less energy stored can be achieved. The resonating fre-

quency of an LCL-filter is expressed by

$$\omega_{res} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C}}. \tag{4.2}$$

However, on the other hand, a relative lower dynamic response and more complex control algorithm are naturally the side effects in addition to the higher cost and more complicated parameters design. It is difficult or impossible for a grid-connect application to comply with IEEE standard 519 without an LCL-filter.

4.4.1 LC-filter

Modelling

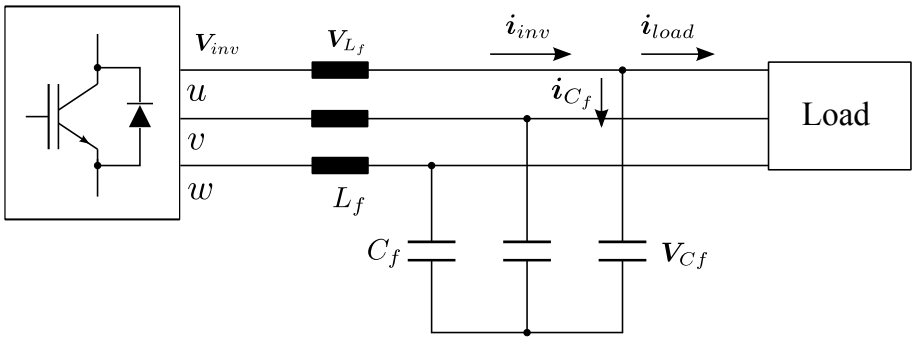


Figure 4.22: LC output filter of a three phase voltage source inverter.

The circuit of a three-phase voltage source inverter with an LC output filter is shown in Figure 4.22. The LC filter can be described by the following equations:

$$\boldsymbol{i}_{C_f} = C_f \frac{d\boldsymbol{V}_{C_f}}{dt}, \tag{4.3}$$

$$\boldsymbol{V}_{L_f} = L_f \frac{d\boldsymbol{i}_{inv}}{dt}, \tag{4.4}$$

$$\boldsymbol{V}_{L_f} = \boldsymbol{V}_{inv} - \boldsymbol{V}_{C_f}, \tag{4.5}$$

$$\boldsymbol{i}_{C_f} = \boldsymbol{i}_{inv} - \boldsymbol{i}_{load}. \tag{4.6}$$

where $\boldsymbol{V}_k = [V_{ku}, V_{kv}, V_{kw}]$, $(k \in \{L_f, C_f, inv\})$; $\boldsymbol{i}_j = [i_{ju}, i_{jv}, i_{jw}]$, $(j \in \{inv, C_f, load\})$. For the controller design, the system is better described by the state space equations as following:

$$\begin{cases} \dot{\boldsymbol{x}} &= \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} \\ \boldsymbol{y} &= \boldsymbol{C}\boldsymbol{x} + \boldsymbol{D}\boldsymbol{u} \end{cases} \tag{4.7}$$

with $\boldsymbol{x} = \begin{bmatrix} \boldsymbol{V}_{C_f} \\ \boldsymbol{i}_{inv} \end{bmatrix}$, $\boldsymbol{u} = \begin{bmatrix} \boldsymbol{V}_{inv} \\ \boldsymbol{i}_{load} \end{bmatrix}$, $\boldsymbol{y} = \boldsymbol{V}_{C_f}$

and $\boldsymbol{A} = \begin{bmatrix} 0 & \frac{1}{C_f} \\ -\frac{1}{L_f} & 0 \end{bmatrix}, \boldsymbol{B} = \begin{bmatrix} 0 & -\frac{1}{C_f} \\ \frac{1}{L_f} & 0 \end{bmatrix}, \boldsymbol{C} = \begin{bmatrix} \mathbf{1} & \mathbf{0} \end{bmatrix}, \boldsymbol{D} = \begin{bmatrix} \mathbf{0} & \mathbf{0} \end{bmatrix}.$

The transfer function $G_{V_{inv} \to V_{C_f}}$ of the LC circuit without load can be expressed as follows:

$$G_{V_{inv} \to V_{C_f}} = \frac{V_{C_f}(s)}{V_{inv}(s)}\bigg|_{i_L=0} = \frac{1}{s^2 L_f C_f + 1}. \tag{4.8}$$

Design

The design approach of the LC-filter basically follows procedures according to [36].

- In order to damp the switching ripple to only 1% which is -40dB, the cut-off frequency is set to the tenth of the fundamental frequency.
- On the other hand, the resonance frequency should be kept as far as possible from the fundamental frequency and low order harmonic components, thus avoiding the resonance problem.

Table 4.2: Parameter of the LC filters

Parameter	IGBT Inverter 1	MOSFET Inverter 2
$L_f\,[mH]$	3.2	0.3
$C_f\,[\mu F]$	30	4.5
$\omega_{res}\,[kHz]$	0.51	4.33

4.5 Final topology of the series magnetic inverter cumulation system

The previous section discussed the typical standard output low pass filter of a power electronic converter system. It brings insight into the technical solutions of the switching components attenuation. With this knowledge, the final topology of the inverter cumulation system based on Figure 4.18 can be completed.

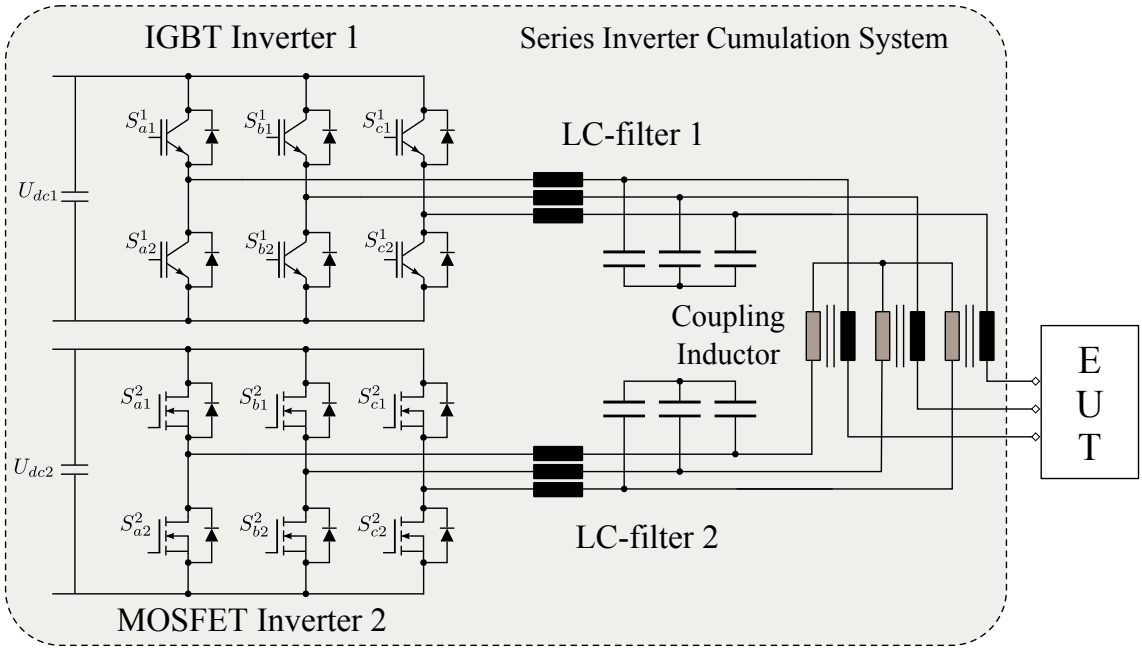


Figure 4.23: Final topology of the series inverter cumulation system.

The LC filter shows a good capability of the output capacitor voltage control, therefore as a programmable AC source emulator, the series-magnetic inverters cumulations system adopts the LC filter as an output filter topology. The final topology is shown in Figure 4.23. The auxiliary circuits like the protection circuit of the MOSFET inverter etc. are not shown in this figure. It is easy to find that the two inverters have different electrical characteristics but the same circuit topology — VSI with LC output filter which is exactly same with the uninterrupted power supply (UPS). As a result, the control algorithm of both inverters could be identical and referred to the UPS output voltage control. However, due to the different switching frequencies of the two inverters, the controllers are implemented on a CPU and an FPGA respectively. As illustrated previously, the MOSFET inverter is supposed to be switched over 50kHz, which is not possible with a normal processor-based controller. This will be discussed in the later chapter.

In this chapter, the original topology is shown. Secondly, the reason behind the damage of the MOSFET inverter is explained. Then the solution for this problem is found and the final topology is derived at the end.

CHAPTER 5

Control strategy of a voltage source inverter with LC output filter

As discussed in the previous chapter, the basic component of the series coupling inverter cumulation system is the voltage source inverter with the LC output filter which is widely used in many industrial applications e.g. UPS and DVR. The system actually has two UPS systems with totally different working conditions. However, for the control strategy design, the same method can be adopted to both systems. This chapter will discuss various voltage control strategies of VSI with LC filter. The cascade multi-loop control in synchronous rotating frame will be presented firstly. Later on, the better performed multi-loop controller in stationary frame is introduced. Besides, due to the light damping of the LC filter itself, the passive and active damping methods are implemented. Last but not least, owing to its superiority (instinct stability, systematic optimization etc.), a linear quadratic controller for the proposed grid emulator is introduced.

5.1 Synchronous rotating frame (SRF) voltage control of the VSI with LC filter

At the initial phase of the controller design, for simplicity, the three-phase system variables are transformed from the stationary abc coordinate to the synchronous dq frame. By doing this transformation, all the ac quantities are converted into DC components on the d and q axis, therefore the conventional PI controllers are capable of tracking the reference signals with zero steady state error. The original idea was introduced in [37] and [38].

By applying the Clarke and Park transformation operators (Equation 2.10 and 2.15) to the state space equation 4.7 of the LC filter, the mathematical model in synchronous frame is derived as follows:

$$\boldsymbol{T_p T_c \dot{x}} = \boldsymbol{A T_p T_c x} + \boldsymbol{B T_p T_c u}. \tag{5.1}$$

with $\boldsymbol{x} = \begin{bmatrix} \boldsymbol{V}_{C_f} \\ \boldsymbol{i}_{inv} \end{bmatrix}$, $\boldsymbol{u} = \begin{bmatrix} \boldsymbol{V}_{inv} \\ \boldsymbol{i}_{load} \end{bmatrix}$, $\boldsymbol{y} = \boldsymbol{V}_{C_f}$

and $\boldsymbol{A} = \begin{bmatrix} 0 & \frac{1}{C_f} \\ -\frac{1}{L_f} & 0 \end{bmatrix}$, $\boldsymbol{B} = \begin{bmatrix} 0 & -\frac{1}{C_f} \\ \frac{1}{L_f} & 0 \end{bmatrix}$, $\boldsymbol{C} = \begin{bmatrix} \mathbf{1} & \mathbf{0} \end{bmatrix}$, $\boldsymbol{D} = \begin{bmatrix} \mathbf{0} & \mathbf{0} \end{bmatrix}$.

The equations of the capacitor voltage V_{C_f} and inverter current i_{inv} in dq frame are expressed as follows

$$\frac{d}{dt}\begin{bmatrix} V_{C_f}^q \\ V_{C_f}^d \end{bmatrix} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}\begin{bmatrix} V_{C_f}^q \\ V_{C_f}^d \end{bmatrix} + \frac{1}{C_f}\begin{bmatrix} i_{inv}^q - i_{load}^q \\ i_{inv}^d - i_{load}^d \end{bmatrix} \tag{5.2}$$

$$\frac{d}{dt}\begin{bmatrix} i_{inv}^q \\ i_{inv}^d \end{bmatrix} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}\begin{bmatrix} i_{inv}^q \\ i_{inv}^d \end{bmatrix} + \frac{1}{L_f}\begin{bmatrix} V_{inv}^q - V_{C_f}^q \\ V_{inv}^d - V_{C_f}^d \end{bmatrix} \tag{5.3}$$

It is quite obvious that state variables have the cross-coupling due to the matrix shown in Equation 5.4.

$$\begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \tag{5.4}$$

Where ω is the fundamental angular frequency of the output capacitor voltage.
Based on the aforementioned analysis, the block diagram of the LC plant is shown in Figure 5.1.

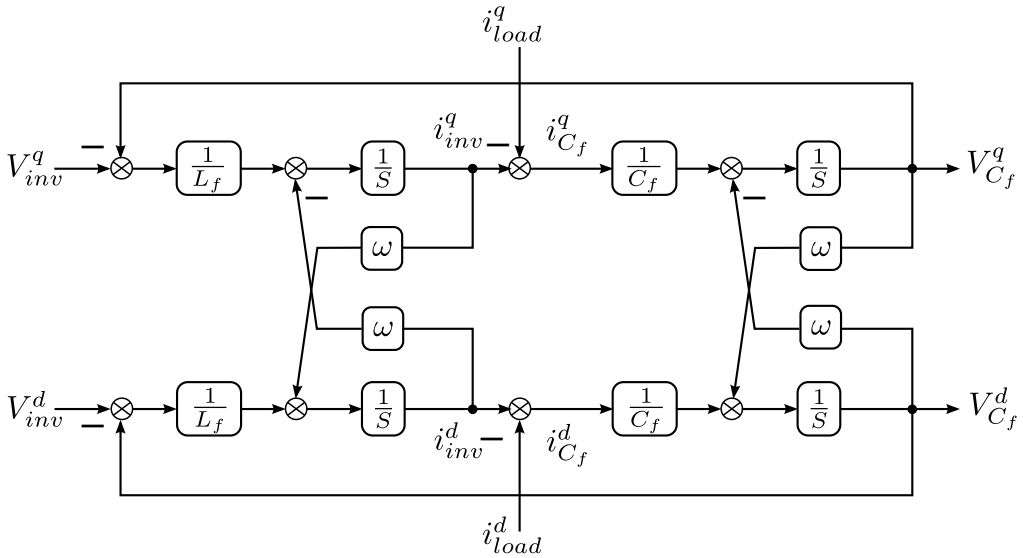


Figure 5.1: Blok diagram of the LC filter plant.

The SRF multi-loop controller has an outer capacitor voltage V_{C_f} feedback loop, the inner feedback loop is an inductor current i_{inv}. In the following subsection, this conventional strategy will be discussed in detail. All the controllers are designed to have decoupling between the dq axes, good reference tracking ability, system overall stability and load disturbance rejection.

5.1.1 Minor-loop inductor current feedback

The inductor currents are sensed and fed back to the controller as the inner current control loop. The control system is decoupled by the items of $\omega C_f V_{C_f}^d$, $-\omega C_f V_{C_f}^q$, $\omega L_f i_{inv}^d$ and $-\omega L_f i_{inv}^q$. The load currents are also sensed and fed back to the controller to achieve the load disturbance rejection. The block diagram of the controller and plant is shown in Figure 5.2.

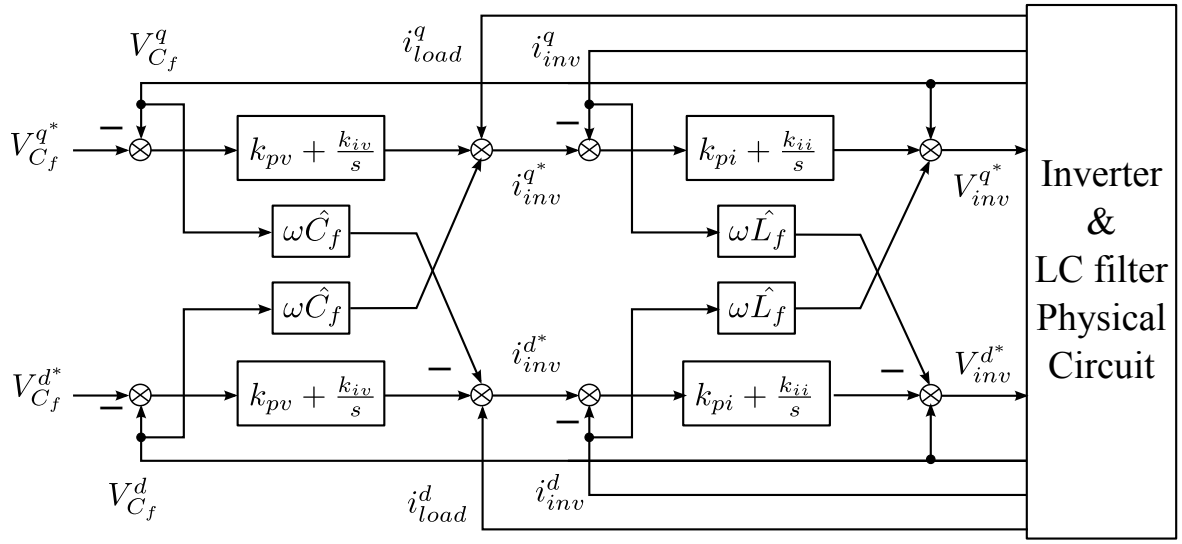


Figure 5.2: LC filter multi-loop controller with inner inductor current feedback.

All cross-coupling terms are assumed to be decoupled in the final control system [39]. Therefore, the system can be decoupled into two total independent subsystems with identical transfer function. In the following analysis, it is sufficient to investigate only the characteristics of the system on q-axis, and the situation of the d-axis follows the same way vice versa. The decoupled close-loop block diagram of the controller and plant is shown in Figure 5.3.

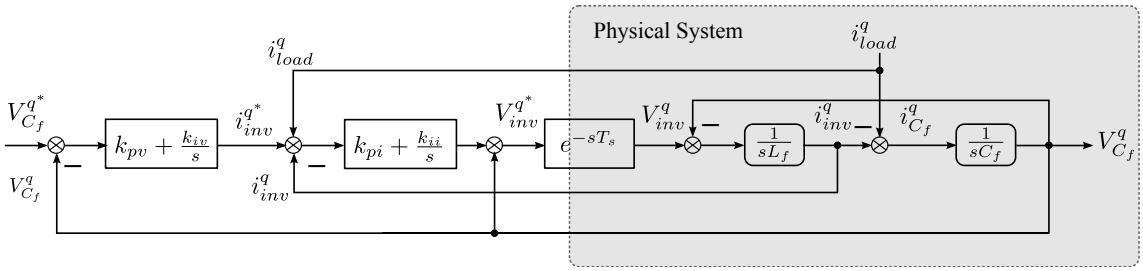
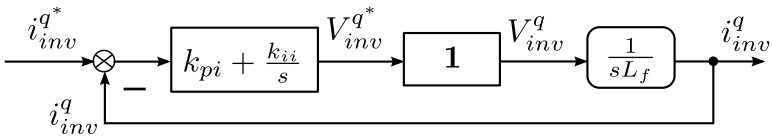


Figure 5.3: Decoupled closed loop block diagram of the LC filter with cascade PI controller (only on q aixs).

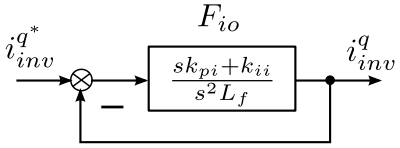
The inverter dead-time, analogue signals sensing and controller calculation delay can be approximated by a first-order inertia element:

$$e^{-sT_s} \approx \frac{1}{1+sT_s} \approx 1 \tag{5.5}$$

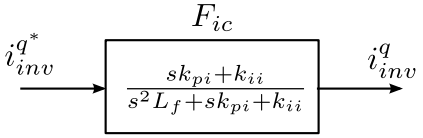
As mentioned in [6], the delay time constant is in the range $(1.5)/2f_s$ to $1/f_s$. Here one chooses the worst case of the $1/f_s$. It is good to analyse the inner current loop first. As the switching frequency of the inverter system is high, the time constant of the delay element T_s is very small. Therefore, for the simplicity of controller design, it is reasonable to view the inverter system as a unit element.



(a) Inner inductor current control loop.



(b) Open loop transfer function of the current loop



(c) Closed loop transfer function of the current loop

Figure 5.4: Block diagrm of the current controller.

The minor current loop block diagram is shown in Figure 5.4. The plant transfer function is a single integrating element $\frac{1}{sL_f}$, a simple proportional controller can achieve zero steady state error for a step reference. An integrator has actually negligible effect when the current loop gain is big enough, and it will cause oscillations when the damping ratio of the closed loop is too small.

$$F_{io} = \frac{sk_{pi} + k_{ii}}{s^2 L_f} \tag{5.6}$$

$$F_{ic} = \frac{sk_{pi} + k_{ii}}{s^2 L_f + sk_{pi} + k_{ii}} \tag{5.7}$$

The steady state error of the controller is calculated by:

$$\Delta i_{inv}^{q} = i_{inv}^{q*} - F_{io}\Delta i_{inv}^{q} \tag{5.8}$$

$$\Delta i_{inv}^{q} = \frac{i_{inv}^{q*}}{1 + F_{io}} \tag{5.9}$$

The steady state response of a step input reference is:

$$\lim_{s\to 0} \frac{\Delta i_{inv}^{q}}{1 + F_{io}} \cdot s = \lim_{s\to 0} \frac{s \cdot \frac{k}{s}}{1 + F_{io}} = \lim_{s\to 0} \frac{k}{1 + F_{io}} = 0 \implies \lim_{s\to 0} F_{io} = \inf \tag{5.10}$$

As mentioned before, the control plant has an integrating component $\frac{1}{sL_f}$, if only a proportional controller is used, the open loop transfer function is:

$$F_{io} = \frac{k_{pi}}{L_f} \cdot \frac{1}{s} = \frac{1}{sT_o} \tag{5.11}$$

with $T_o = \frac{L_f}{k_{pi}}$. It satisfies the Equation 5.10 in any case. The closed loop transfer function is a first order lag element whose response time can be adjusted by the controller gain to as fast as desired.

$$F_{ic} = \frac{F_{io}}{1 + F_{io}} = \frac{1}{1 + sT_o} \tag{5.12}$$

As a rule of thumb, the setting time $t_{set} = 3T_o$, therefore the proportional gain of the controller can be calculated by:

$$k_{pi} = \frac{L_f}{3t_{set}} \tag{5.13}$$

The first order lag element is always stable, the only pole $-\frac{1}{T_o}$ is on the left side of the imaginary axis of s-plane. And the step input response has no over-shoot and can be as fast as required. It is a good choice to use only a P controller instead of a PI controller. But it is a very ideal case that to model the plant by only an integrating component.

Moreover, it is also important to achieve zero steady state error for a ramp reference tracking, if the system is desired to emulate typical grid short circuit fault and recovery. The steady state response of a ramp input reference is:

$$\lim_{s\to 0} \frac{\Delta i^q_{inv}}{1 + F_{io}} \cdot s = \lim_{s\to 0} \frac{s \cdot \frac{k}{s^2}}{1 + F_{io}} = \lim_{s\to 0} \frac{k}{s + sF_{io}} = 0 \implies \lim_{s\to 0} sF_{io} = \inf \tag{5.14}$$

Therefore, a PI-controller is viewed as a necessary solution for the system. Looking closely at the close-loop transfer function of the system with the PI-controller (shown in Equation 5.7, it is a second order system with an additional zero. It can be rewritten into the standard form as:

$$F_{ic} = \frac{\omega_n^2(s + z)}{z(s^2 + 2\xi\omega_n s + \omega_n^2)} \tag{5.15}$$

with $\omega_n = \sqrt{\frac{k_{ii}}{L_f}}$, $\xi = \frac{k_{pi}}{2\sqrt{k_{ii}L_f}}$, $z = \frac{k_{ii}}{k_{pi}} = \frac{\omega_n}{2\xi}$. It can be split into two parts as presented by the following equation:

$$F_{ic} = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} + \frac{s}{z}\frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{5.16}$$

The dominate effect of the transfer function is a standard second order system. It is well known that there is an optimal value for the damping ratio:

$$\xi = \frac{1}{\sqrt{2}} \approx 0.707 \tag{5.17}$$

The system time constant T is defined by:

$$T = \frac{1}{2\xi\omega_n} = \frac{1}{\sqrt{2}\omega_n} \tag{5.18}$$

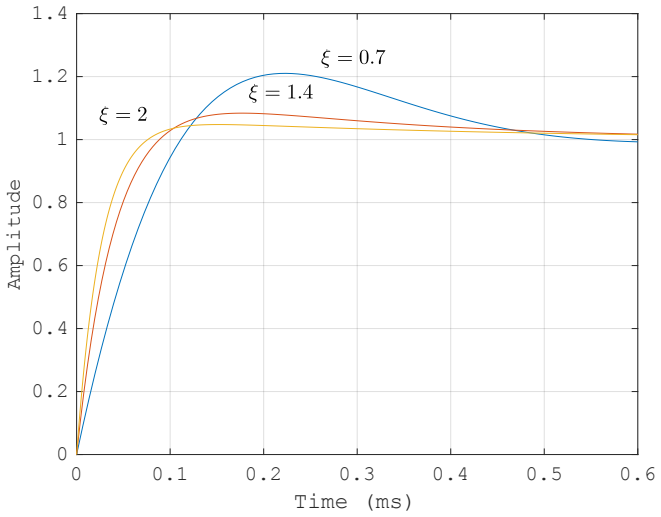
The settling time t_{set} of a step input is calculated by the rule of thumb equation as:

$$t_{set}(5\%) = 4.14T \approx \frac{3}{\omega_n} \tag{5.19}$$

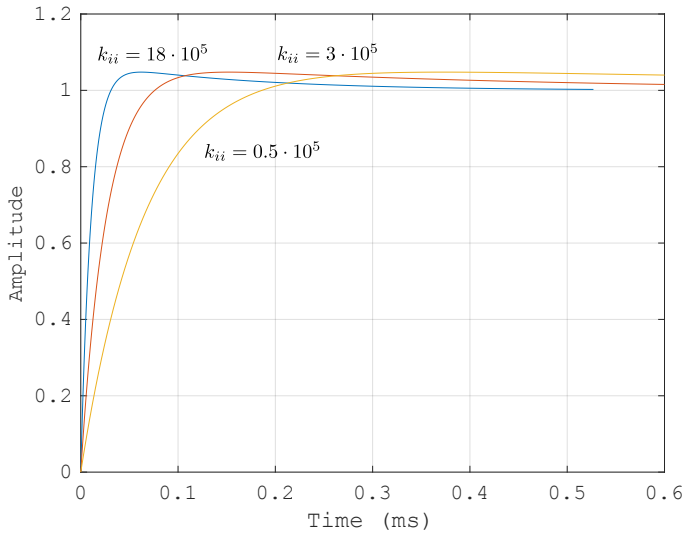
Based on Equation 5.19, one can start to design the parameters of the PI-controller.

$$\omega_n = \sqrt{\frac{k_{ii}}{L_f}} = \frac{3}{t_{set}} \Rightarrow \underline{k_{ii} = \frac{9L_f}{t_{set}^2}} \tag{5.20}$$

$$\xi = \frac{k_{pi}}{2\sqrt{k_{ii}L_f}} \approx 0.707 \Rightarrow \underline{k_{pi} = 2\xi\sqrt{k_{ii}L_f}} \tag{5.21}$$



(a) Different responses by changing the damping ratio ξ. ($k_{ii} = 3 \times 10^5$)



(b) Different responses by changing the integrating gain k_{ii}. ($\xi = 2$)

Figure 5.5: Step response of the inner current loop ($L_f = 3mH$).

Based on the analysis in the text book, the additional zero will cause more oscillations. Therefore, the final overall system response would not be as optimal as the standard second order

system if we set the damping ratio to $\xi = 0.707$. As the consequence of the additional zero, the open loop frequency response and the step input response are investigated to find the new optimal damping ratio.

Initially, the requirements of the dynamic are set as following: the settling time $t_{set} = 0.3ms$, the maximal overshoot $\sigma\% = 5\%$. According to the Equation 5.20, one can get the value of integrator gain as following:

$$k_{ii} = \frac{9L_f}{t_{set}^2} = \frac{9 * 3 * 10^{-3}}{9 * 10^{-8}} = 3 * 10^5 \tag{5.22}$$

However, as shown by Figure 5.5(a), the response overshoot σ is more than 20%. This is the side effect of the additional zero of the system. Therefore, in order to satisfy the required overshoot, new optimal value of ξ has to be found. Based on

$$\sigma\% = e^{-\frac{\xi\pi}{\sqrt{1-\xi^2}}}, \tag{5.23}$$

it is clear that, the overshoot decreases with the increasing damping ratio ξ. According to Figure 5.5(a), when one increases the $\xi = 2$, the system $\sigma\%$ is below 5%. Thus the new optimal value of the damping ratio is set to 2.

Figure 5.5(b) shows that the system settling time is determined only by the integrating gain k_{ii}, when ξ is fixed. The settling time t_s is decreased by increasing k_{ii}. The dynamic behaviour stays almost the same between different curves. When one gets the value of the k_{ii} and ξ, the k_{pi} can be simply calculated by:

$$k_{pi} = 2\xi\sqrt{k_{ii}L_f} = 2 * 2 * 30 = 120. \tag{5.24}$$

The optimal transfer function of the inner current loop can be expressed by the following:

$$F_{ic} = \frac{120s + 3 * 10^5}{0.003s^2 + 120s + 3 * 10^5} \tag{5.25}$$

5.1.2 Major-loop capacitor voltage feedback

After tuning the inner current controller, the transfer function of the inner loop is derived in Equation 5.25. Neglecting the time delay, the inner current loop can be viewed as a unit block. By doing this, the voltage loop controller can be analysed by the new derived block diagram shown in Figure 5.6. However, it requires that the dynamics of the outer voltage controller to be much slower than the inner current controller. In other words, the settling time of the current controller should be much faster than the voltage loop. For the proposed design, the settling time of the voltage controller is $3ms$ which is 10 times longer.
By observing the voltage and current control loops, they have the same structure. The only difference is the parameter of the physical system. Based on the LC filter parameters in Table 4.2, the filter capacitor is $30\mu F$.

Firstly, we assume the disturbance i_{load}^q is zero, then the transfer function $V_{C_f}^q(s)/V_{C_f}^{q*}(s)$ is:

$$F_{vc} = \frac{sk_{pv} + k_{iv}}{s^2C_f + sk_{pv} + k_{iv}} \tag{5.26}$$

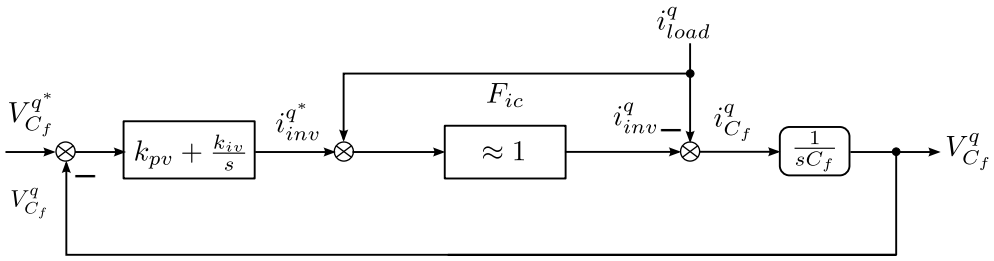


Figure 5.6: Voltage controller block diagram (only in q aixs).

Based on the same tuning process with the current control loop, the k_{pv} and k_{pi} will be calculated by the following equations. The settling time is extended as $t_{set} = 3ms$, but the damping ratio is kept same as $\xi = 2$.

$$k_{iv} = \frac{9C_f}{t_{set}^2} = \frac{9 * 30 * 10^{-6}}{9 * 10^{-6}} = 30 \tag{5.27}$$

$$k_{pv} = 2\xi\sqrt{k_{iv}C_f} = 2 * 2 * 0.03 = 0.12 \tag{5.28}$$

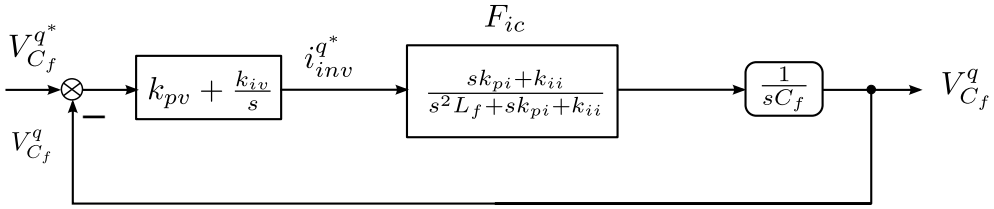


Figure 5.7: Voltage controller and inner current loop block diagram under no disturbance situation (only in q aixs).

Now we replace the inner current loop unit block with its derived closed loop transfer function shown in Equation 5.25, the final block diagram of the whole system is shown in Figure 5.7 (disturbance is still neglected). The final open and closed loop transfer functions are calculated as the following:

$$F_o = \frac{s^2k_{pv}k_{pi} + s(k_{pv}k_{ii} + k_{pi}k_{iv}) + k_{iv}k_{ii}}{s^4C_fL_f + s^3C_fk_{pi} + s^2C_fk_{ii}} \tag{5.29}$$

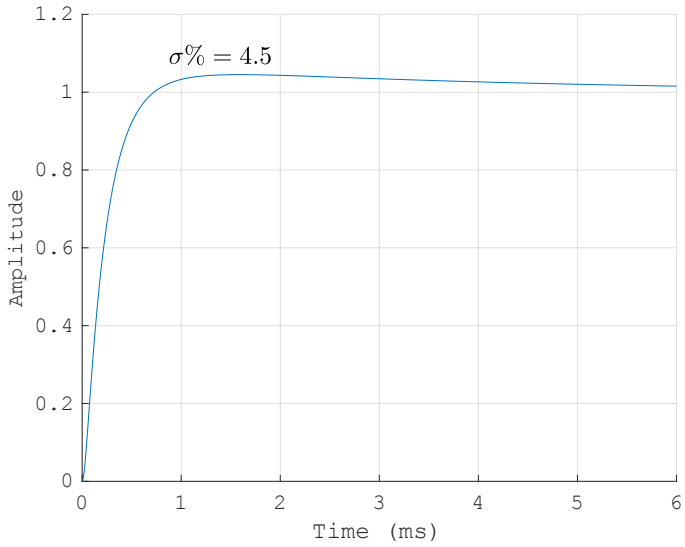
$$F_c = \frac{s^2k_{pv}k_{pi} + s(k_{pv}k_{ii} + k_{pi}k_{iv}) + k_{iv}k_{ii}}{s^4C_fL_f + s^3C_fk_{pi} + s^2(C_fk_{ii} + k_{pv}k_{pi}) + s(k_{pv}k_{ii} + k_{pi}k_{iv}) + k_{iv}k_{ii}} \tag{5.30}$$

with $C_f = 30\mu F, k_{pv} = 0.12, k_{iv} = 30, k_{pi} = 120, k_{ii} = 3 * 10^5$, they can be reformed as:

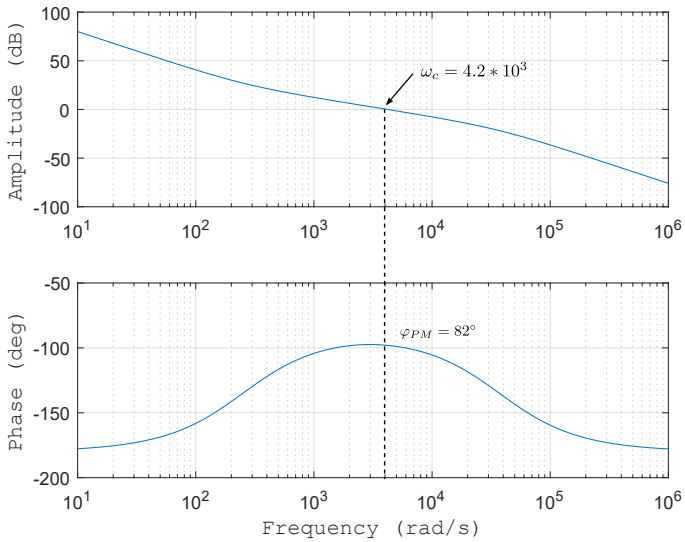
$$F_o = \frac{14.4s^2 + 3.96 * 10^4s + 9 * 10^6}{9 * 10^{-8}s^4 + 3.6 * 10^{-3}s^3 + 9s^2} \tag{5.31}$$

$$F_c = \frac{14.4s^2 + 3.96 * 10^4s + 9 * 10^6}{9 * 10^{-8}s^4 + 3.6 * 10^{-3}s^3 + 23.4s^2 + 3.96 * 10^4s + 9 * 10^6} \tag{5.32}$$

Based on the obtained final transfer function, the overall system characteristics have to be checked. The step response is shown in Figure 5.8(a). As shown in figure 5.8(a), the step response



(a) Step response of voltage controller.



(b) Bode plot of voltage controller.

Figure 5.8: Performance of voltage controller.

of the system described by equation 5.32 has an overshoot $\sigma\% = 4.5$, and the settling time (3%) is around the $3ms$. According to its bode plot, the controller has a cut-off frequency $\omega_c = 4200rad/s$ and phase margin $\varphi_{PM} = 82°$ which is very close to its max value $82.6°$. Therefore the controller design fulfills all the requirements, and has an optimal performance.

5.1.3 Load current rejection

The load current is the disturbance of the system, and it is assumed to be '0' for the previous analysis. A good control system of the grid emulator should also have a good load rejection capability. In this subsection, the effect of the load current is discussed first and then the com-

pensation method is presented.

Firstly, let us assume that there is no feed forward compensation of the load current. The block diagram is shown in Figure 5.9. The closed-loop transfer function is:

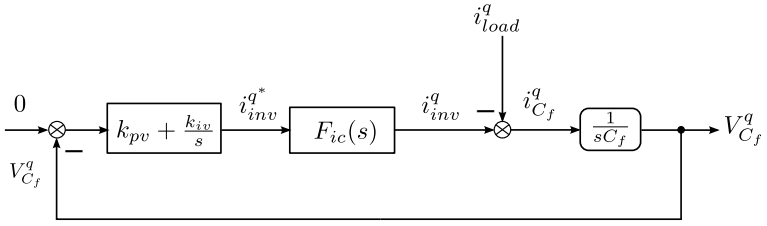


Figure 5.9: System block diagram when the disturbence is only input.

$$\frac{\Delta V^q_{C_f}(s)}{\Delta i^q_{load}(s)} = \frac{-W_2(s)}{1 + W_1(s)W_2(s)}, \tag{5.33}$$

where

$$W_1(s) = (k_{pv} + \frac{k_{iv}}{s}) \cdot F_{ic}(s), \tag{5.34}$$

$$W_2(s) = \frac{1}{sC_f}. \tag{5.35}$$

The steady state error of a step input $\Delta i^q_{load}(s) = \frac{k}{s}$ is calculated as following:

$$e_{ss} = \lim_{s\to 0} \Delta i^q_{inv} \cdot s \cdot \frac{-W_2(s)}{1 + W_1(s)W_2(s)} = 0 \tag{5.36}$$

However, as explained before, it is important to consider a ramp input $\Delta i^q_{load}(s) = \frac{k}{s^2}$, the steady state error is:

$$e_{ss} = \lim_{s\to 0} \Delta i^q_{inv} \cdot s \cdot \frac{-W_2(s)}{1 + W_1(s)W_2(s)} = \frac{k}{30} \tag{5.37}$$

In order to eliminate this problem, a more sophisticated compensation method should be used if a zero steady state error is strictly required for both step and ramp load disturbances.

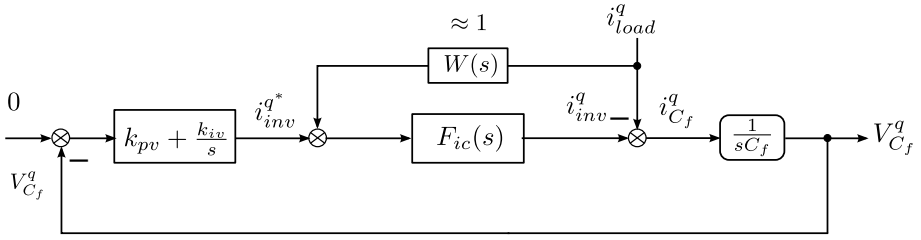


Figure 5.10: System block diagram with disturbence compensation.

From Figure 5.10 one can derive following equation:

$$\frac{V^q_{C_f}(s)}{i^q_{load}(s)} = \frac{W_2(s)[W(s)F_{ic}(s) - 1]}{1 + W_2(s)W_1(s)} = 0 \tag{5.38}$$

thus

$$W(s)F_{ic}(s) = 1 \Rightarrow W(s) = \frac{1}{F_{ic}(s)} = \frac{0.003s^2 + 120s + 3 * 10^5}{120s + 3 * 10^5} \tag{5.39}$$

By adopting the load current feed-forward compensator described by Equation 5.39, the stead state error is eliminated. However, because the order of the compensator numerator is higher than that of the denominator, this causes problems for the implementation in the digital controller. But the transfer function can be approximated as a unit block which gives a satisfactory result. In the following, let us assume there is unit feed forward compensation of the load current. This is the case of Figure 5.3. The new closed-loop transfer function is:

$$\frac{V_{C_f}^q(s)}{i_{load}^q(s)} = \frac{W_2(s)(F_{ic}(s) - 1)}{1 + W_1(s)W_2(s)}. \tag{5.40}$$

The new steady state error of a ramp input $\Delta i_{load}^q(s) = \frac{k}{s^2}$ is calculated as following:

$$e_{ss} = \lim_{s \to 0} \frac{k}{s} \cdot \frac{W_2(s)(F_{ic}(s) \cdot 1 - 1)}{1 + W_1(s)W_2(s)} = 0 \tag{5.41}$$

The steady state error in this case is zero, and this fulfills the control requirement of the proposed grid emulator.

In this section, two cascaded PI controllers, and the load feed-forward compensator are designed based on the system dynamic characteristics and frequency response. Zero steady state error is achieved for both input reference tracking and load rejection. The parameters of the PI controllers and compensator are optimized according to the settling time and over-shoot of the input step response.

5.2 Stationary frame voltage control of the VIS with LC filter

Due to the infinite DC gain of the conventional PI controller in synchronous rotation frame, the steady state error can be forced to 0. Moreover, a well tuned PI controller has satisfied the dynamic performance for the voltage control of the proposed grid emulator. However, because of the complicated frame transformation, the necessity of the decoupling network, and the sensitiveness of the frequency variation, the PI controller in dq frame is not convenient. Recently, stationary frame controller (current and voltage regulation) has gotten more attention [40–42] due to its advantages compared to the conventional synchronous PI controller.

5.2.1 Proportional resonant controller in general

Theoretically the synchronous PI-controller can be equivalently transformed to stationary frame. The transfer function of a single phase PI-controller is:

$$G_{DC}(s) = k_p + \frac{k_i}{s}. \tag{5.42}$$

According to [43], it can be transformed to the stationary frame by the following equations:

$$G_{AC}(s) = \frac{1}{2}[G_{DC}(s + j\omega_{res}) + G_{DC}(s - j\omega_{res})], \tag{5.43}$$

$$G_{AC}(s) = k_p + \frac{k_i s}{s^2 + \omega_{res}^2}. \tag{5.44}$$

A positive sequence synchronous dq^+ PI-controller can be derived in stationary frame as:

$$G_{DC}^{dq^+}(s) = \begin{bmatrix} k_p + \frac{k_i}{s} & 0 \\ 0 & k_p + \frac{k_i}{s} \end{bmatrix} \Rightarrow G_{AC}^{\alpha\beta}(s)^+ = \begin{bmatrix} k_p + \frac{k_i s}{s^2+\omega_o^2} & -\frac{k_i \omega_{res}}{s^2+\omega_{res}^2} \\ \frac{k_i \omega_{res}}{s^2+\omega_{res}^2} & k_p + \frac{k_i s}{s^2+\omega_{res}^2} \end{bmatrix}. \tag{5.45}$$

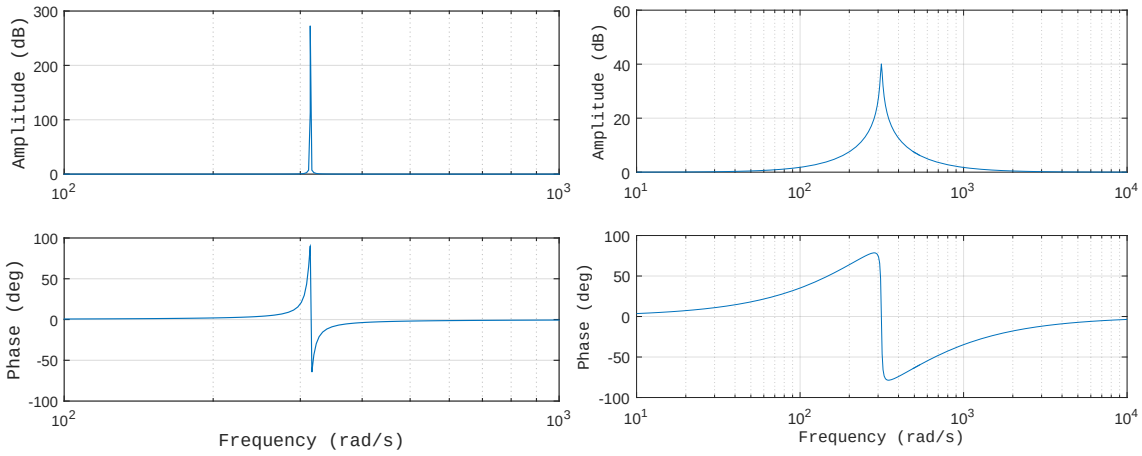
Similarly, the negative sequence synchronous dq^- PI-controller can be derived in stationary frame as:

$$G_{DC}^{dq^-}(s) = \begin{bmatrix} k_p + \frac{k_i}{s} & 0 \\ 0 & k_p + \frac{k_i}{s} \end{bmatrix} \Rightarrow G_{AC}^{\alpha\beta}(s)^- = \begin{bmatrix} k_p + \frac{k_i s}{s^2+\omega_{res}^2} & \frac{k_i \omega_{res}}{s^2+\omega_{res}^2} \\ -\frac{k_i \omega_{res}}{s^2+\omega_{res}^2} & k_p + \frac{k_i s}{s^2+\omega_{res}^2} \end{bmatrix}. \tag{5.46}$$

By observing the above equations, the controller matrix is still complex due to the cross coupling terms between phases. According to [44], by comparing Equations 5.45 and 5.46, it is noticed that the diagonal terms of $G_{AC}^{\alpha\beta}(s)^+$ and $G_{AC}^{\alpha\beta}(s)^-$ are identical, but their non-diagonal terms are opposite in polarity. This inversion of the polarity can be viewed as equivalent to the reversal of rotating direction between the positive and negative sequence synchronous frames. However, if one combines both sequence controllers together, we get the well known and widely used proportional resonant controller [45, 46]. The transfer function of the P+R controller is shown as:

$$G_{PR}^{\alpha\beta}(s) = \begin{bmatrix} k_p + \frac{k_i s}{s^2+\omega_{res}^2} & 0 \\ 0 & k_p + \frac{k_i s}{s^2+\omega_{res}^2} \end{bmatrix}. \tag{5.47}$$

From this equation, it can be seen that the P+R controllers do not require any decoupling networks, neither depend on the sequence control, as a single P+R controller is able to control both positive and negative sequence components [47]. Moreover, the phase angle of the voltage and current system are eliminated.



(a) Orignal form. (b) Practical form.

Figure 5.11: Bode plot of the P+R controller

Figure 5.11(a) shows that the controller has an infinite gain at the resonant frequency ω_{res}, therefore the controller has no phase or magnitude error in the output waves. However, the ideal controller corresponds to a lossless filter network which is physically difficult or impossible to implement due to the component tolerances in analogue systems and finite precision in digital systems [43, 48]. Besides, the controller is so sensitive to the frequency variations, therefore a practical P+R controller expressed below is used as a realistic solution.

$$G_{PR}^{\alpha\beta}(s) = \begin{bmatrix} k_p + \frac{2k_i\omega_c s}{s^2+2\omega_c s+\omega_{res}^2} & 0 \\ 0 & k_p + \frac{2k_i\omega_c s}{s^2+2\omega_c s+\omega_{res}^2} \end{bmatrix} \tag{5.48}$$

where ω_c is the controller cut off frequency. The bode plot of the Equation 5.48 is shown in Figure 5.11(b). By adjusting the cut off frequency ω_c, the controller has a wide bandwidth around the resonant frequency with the cost of reduced resonant peak. A wider bandwidth minimizes the sensitivity to light frequency variation, and the reduced resonant peak is still sufficient for eliminating the steady state error [46]. There are three parameters in the practical P+R controller: k_p regulates the overall gain, k_i adjusts the resonant peak amplitude, and ω_c controls the bandwidth.

Moreover, another big advantage of the P+R controller is selective harmonic control. Related to the proposed grid emulator, in normal operation mode a very low THD fundamental voltage wave is desired, thus low order harmonics (5,7 and 11th) should be compensated (Figure 5.12). When a synchronous frame PI controller is used, multi-frame transforming has to be done, which is complex and probably out of the reach of the digital controller. However, referring to the resonant controller, the multi-harmonic controller is easy to implement without too much calculation burden. Selective harmonic control can be achieved by cascading several resonant blocks (equation 5.49) tuned to resonate at the desired low-order harmonics frequencies.

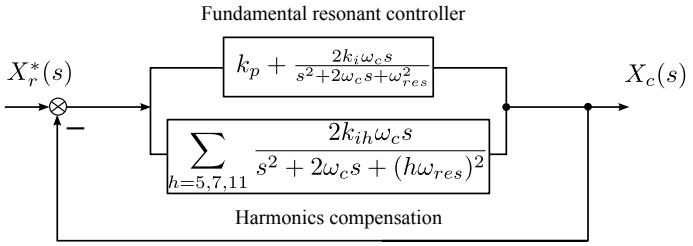


Figure 5.12: P+R with harmonics resonant controller

$$G_h(s) = \sum_{h=5,7,11} \frac{2k_{ih}\omega_c s}{s^2 + 2\omega_c s + (h\omega_{res})^2} \tag{5.49}$$

5.2.2 Multi-loop controller with different minor-loop feedback variables

Related to the proposed power grid emulator, the output voltage of the filter capacitor has to be controlled to track the desired value. A simple single voltage loop with aforementioned P+R controller is capable of achieving the control task. It is cost-effective (no current sensor) and easy to implement, however a trade-off between the controller performance and the system

stability must be made. According to [49] and [50], a larger controller gain is required for better steady and transient performance, but it deteriorates the system stability. Although a feed-forward of reference voltage signals improves the performance, the controller is still subject to serious LC resonance.

A multi-loop strategy has an additional inner current loop which improves the system stability and exhibits good steady and transient performance simultaneously. Therefore, it will be implemented as the controller of the corresponding grid emulator. There are several inner-loop feedback alternatives (inverter current i_{inv} or capacitor current i_{C_f}) which have respective merits and shortcomings [45, 51]. In general, the capacitor current feedback is better for the load rejection, while on the other hand, the inverter current feedback has better LC resonance damping and over current protection ability [49]. Two strategies will be analysed respectively in the following section.

The multi-loop controller with the inner inverter current feedback loop is shown in Figure 5.13 (pahse diagram is shown). Since the steady state error of the inner current loop does not effect the outer voltage loop accuracy, a simple proportional controller is used instead of the complicated PR controller [45]. The sensed output voltage can be positively fed back (output voltage decoupling) to the inner current loop as shown by the doted line. According to [52], by doing this output voltage decoupling, the inner loop could have a higher controller gain and thus a better steady and dynamic performance, and the system is more stable. This is approved by the closed loop transfer function of the inner current loop with and without output voltage decoupling.

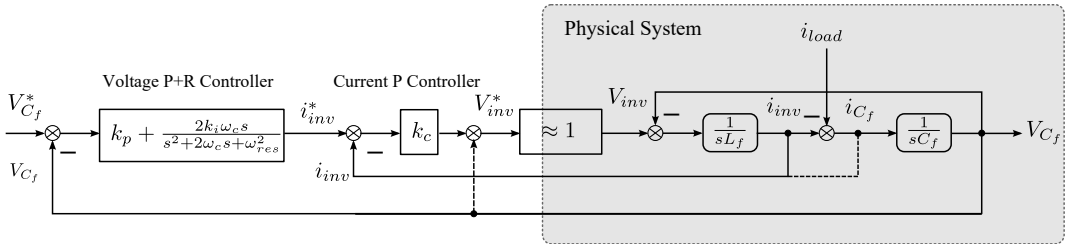


Figure 5.13: Stationary multi-loop controller of the voltage source inverter with LC filter.

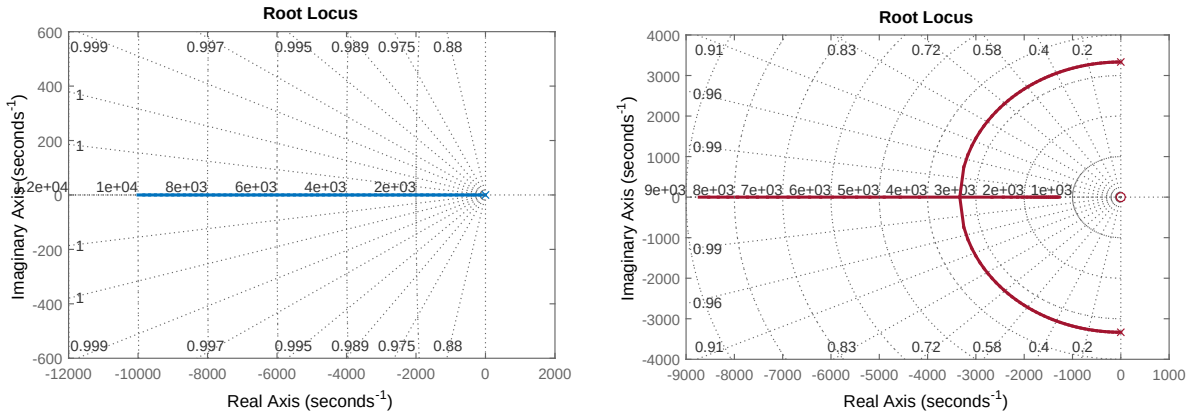
The closed loop transfer function of the inner controller with output voltage decoupling is:

$$G_{i_{inv}\to i^*_{inv}}(s) = \frac{k_c}{L_f s + k_c}, \tag{5.50}$$

and without decoupling is:

$$G'_{i_{inv}\to i^*_{inv}}(s) = \frac{sk_cC_f}{s^2L_fC_f + sk_cC_f + 1}. \tag{5.51}$$

With the output voltage decoupling, the transfer function of the inner current loop is changed from a second order system into a first order system. According to the response characteristics of the first order system, it is always stable and the dynamic performance of a step response could be very fast without any overshoot and oscillation. A larger inner loop controller gain could be possible for the output voltage decoupling case, thus it achieves a robuster and better dynamic performance system. This is approved by the root locus plot of the two transfer Equations 5.50 and 5.51, which are shown in Figure 5.14.



(a) With output voltage decoupling.

(b) Without output voltage decoupling.

Figure 5.14: Root locus of the inner loop when kc in the range of 0 to 30

As discussed previously, either inverter current i_{inv} or capacitor current i_{Cf} can be the inner loop feedback variables. The closed loop transfer function $G_{v_{Cf}\to v^*_{Cf}}(s)$ of both cases is derived in the following.
First the disturbance i_{load} is neglected, and only the effect of the reference v^*_{Cf} is considered.
inverter current feedback

$$G_{v_{Cf}\to v^*_{Cf}}(s)\Big|_{i_{load}=0} = \frac{k_c[k_p s^2 + 2\omega_c(k_p+k_i)s + k_p\omega^2_{res}]}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{5.52}$$

capacitor current feedback

$$G_{v_{Cf}\to v^*_{Cf}}(s)\Big|_{i_{load}=0} = \frac{k_c[k_p s^2 + 2\omega_c(k_p+k_i)s + k_p\omega^2_{res}]}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{5.53}$$

where $a_4 = L_f C_f$, $a_3 = 2\omega_c L_f C_f + k_c C_f$, $a_2 = \omega^2_{res} L_f C_f + 2\omega_c k_c C_f + k_p k_c$,
$a_1 = \omega^2_{res} k_c C_f + 2\omega_c(k_p k_c + k_i k_c)$, $a_0 = k_p k_c \omega^2_{res}$.
By comparing Equations 5.52 and 5.53, it is obvious that the transfer functions of the both feedback variables are exactly the same. In other words, both strategies have the same reference tracking capability. Either inverter or capacitor current inner feedback controller shows no difference under the no load condition.
Second, the reference input v^*_{Cf} is set to 0, and only the effect of disturbance i_{load} is considered. The transfer functions are:
inverter current feedback

$$G_{v_{Cf}\to i_{load}}(s)\Big|_{v^*_{Cf}=0} = -\frac{L_f s^3 + (k_c + 2\omega_c L_f)s^2 + (2\omega_c k_c + L_f\omega^2_{res})s + \omega^2_{res}k_c}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{5.54}$$

capacitor current feedback

$$G_{v_{Cf}\to i_{load}}(s)\Big|_{v^*_{Cf}=0} = -\frac{L_f s^3 + 2\omega_c L_f s^2 + L_f\omega^2_{res}s}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{5.55}$$

By comparing the disturbance rejection transfer function 5.54 and 5.55 of both cases, the differences between two different feedback variables come out. The steady state errors of disturbance current step are calculated as following:

inverter current feedback

$$e_{ss} = \lim_{s\to 0} G_{v_{Cf}\to i_{load}}(s)\big|_{v^*_{Cf}=0} = \frac{\omega^2_{res}k_c}{a_0} = \frac{1}{k_p} \tag{5.56}$$

capacitor current feedback

$$e_{ss} = \lim_{s\to 0} G_{v_{Cf}\to i_{load}}(s)\big|_{v^*_{Cf}=0} = 0 \tag{5.57}$$

Equations 5.56 and 5.57 mathematically illustrated that the capacitor feedback strategy has a zero steady state error for disturbance current step, however the inductor current feedback strategy comparatively deteriorates the load disturbance rejection capability as the result of the steady state error $\frac{1}{k_p}$. As mentioned previously, the inverter current feedback strategy has a benefit of the over current protection, therefore if using the inverter feedback, one compensation method should be used to achieve better disturbance rejection. Similar to the PI controller, the disturbance load current is simply feed forward to the current controller, and it is also named as disturbance current decoupling which is shown in Figure 5.15.

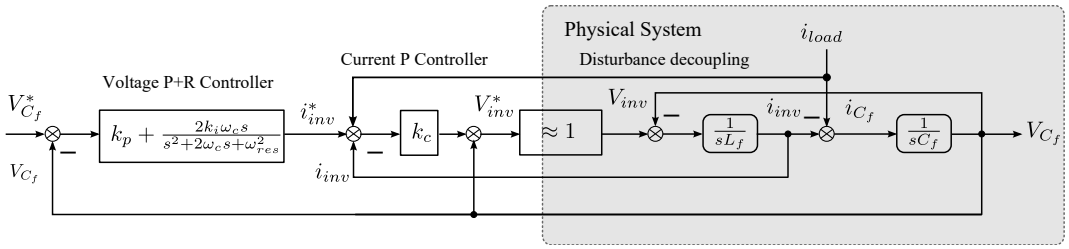


Figure 5.15: Disturbance decoupling of the PR controller.

By doing this, the transfer function of the system is the same as Equation 5.55; thus it has no steady state error for the step response of the disturbance load current.

The tuning process of the multi-loop PR controller is not so systematic, and it is mainly based on the trial and error with the system step response in MATLAB. As the inner current loop has a simple proportional controller, the closed loop transfer function is a first order system which is easily tuned as fast as desired. By using the equation 5.13, the parameter k_c of the inner current controller could be easily calculated with the desired settling time. However, the PR controller has more tuning parameters as k_p, k_i and ω_c, and its optimization is very complicated.

According to [48], k_p controls the cross-frequency of the system, and the higher the proportional gain is the faster the transient response will be. The resonant terms k_i and ω_c mainly influence the resonant frequency, but have very little effect on the cross frequency. The tuning is carried out basically in two steps: first, k_p is chosen so that the transient process has desired settling time and overshoot. Then design the resonant components for the desired steady state and enough phase margin.

5.2.3 Damping methods of the LC circuit resonance

The plant of the LC filter is a low damped second order system, therefore the frequency components which are around the resonance of the LC circuit deteriorate the system stability. In order to solve the resonance problem of the LC plant, two categories of damping methods are introduced in the literature [53–55]: passive and active damping.

The principle of the passive damping is straight forward. By introducing a damping resistor in series or in parallel with the filter inductor or capacitor, the energy of the resonance is absorbed. The four possible positions of the damping resistor are shown in Figure 5.16. The tuning is done with the help of the MATLAB. The closed-loop transfer function of the system is built and its step response is simulated in MATLAB.

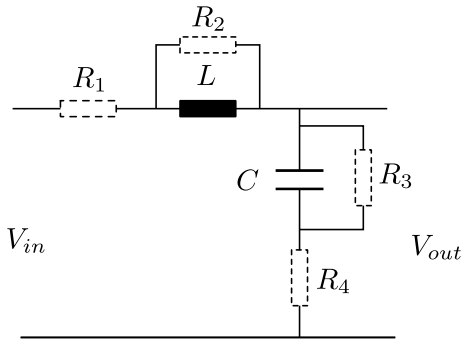
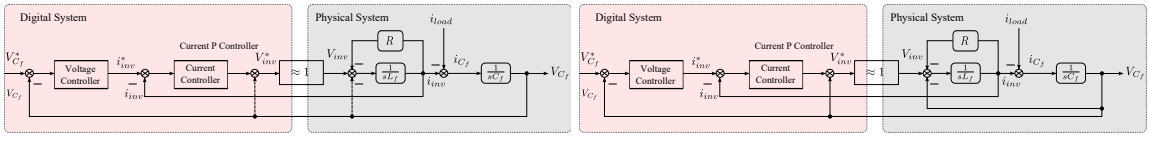


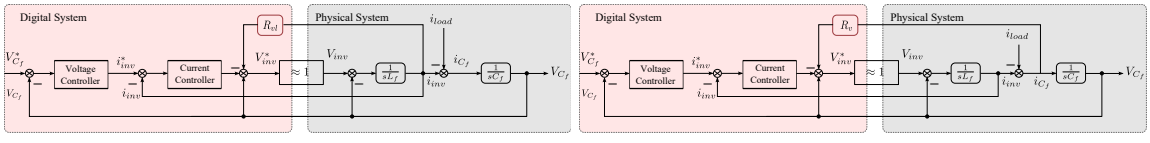
Figure 5.16: The possible positions of the damping resistors.

The passive damping is simple, robust and effective. However, from the efficiency point of view, it is not a reasonable solution due to the losses caused by the additional damping resistors. Therefore, a recently introduced active damping method uses virtual resistors in the digital controller instead of real resistors in the physical circuit. Because the virtual resistor behaves as a compensator which damps the LC resonance effect without producing any losses, active damping is believed as a more effective damping method.



(a) passive damping resistor in series with inductor

(b) passive damping resistor in series with capacitor



(c) active damping virtual resistor in series with inductor

(d) active damping virtual resistor in series with capacitor

Figure 5.17: Passive and active damping of the LC filter

As shown in Figure 5.16, there are four possible positions for the physical damping resistors. Therefore four corresponding virtual resistors can also be digitally implemented to emulate the

behaviours the real resistors. According to [49], for the virtual resistor in parallel with the inductor or capacitor (realized by dividing the inductor or capacitor voltage by the desired virtual resistance), differentiators are required to convert the current signal from the virtual resistor loop output to the voltage signal that can be applied to the PWM modulator in the VSI. However, the differentiator may bring a noise problem as a result of the amplification of the high frequency component in the sensor measured current and voltage signals. In reality, the virtual resistors in series with the inductor or capacitor are the practical solution. The implementation of the virtual resistors is based on the equivalent manipulation of the block diagram with physical resistors. The corresponding implementation is schematically explained in Figure 5.17.

Figure 5.17(a) and 5.17(b) show the control block diagram of the LC filter with passive damping resistors in series with filter inductor and capacitor respectively. Figure 5.17(c) and 5.17(d) are just the manipulation of 5.17(a) and 5.17(b). Therefore the transient and steady state behaviour of the systems before and after manipulation are exactly the same. However, the manipulated block diagram replaces the physical resistor in the plant by the digital feedback gain in the controller.

5.3 State feedback control of the VSI with LC filter

This section discusses another popular control strategy of the VSI with LC filter – state feedback control. This method first requires the state space modelling of the control system. Afterwards by deriving the state feedback gain matrix $\boldsymbol{K}$ based on pole placement or quadratic optimal method, the step response of the controlled system is forced to desired requirements. The section begins with the the general background knowledge of the system modelling and pole placement technique. The following subsection focuses on the quadratic optimal control of the proposed VSI with LC filter system.

5.3.1 General knowledge of state space modelling and pole placement technique

In this subsection, the basic background knowledge of the general state space modelling and pole placement technique is shown. As discussed in literature [56], we consider a multiple-input-multiple-output (MIMO) system described by the following standard space equations:

$$\begin{aligned} \dot{\boldsymbol{x}} &= \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} \\ \boldsymbol{y} &= \boldsymbol{C}\boldsymbol{x} \end{aligned} \tag{5.58}$$

where $\boldsymbol{x}$ is the state vector (n-vector), u is the input vector (r-vector) and y is the output vector (m-vector). $\boldsymbol{A}(n \times n)$, $\boldsymbol{B}(n \times r)$ and $\boldsymbol{C}(m \times n)$ are the system matrices. The control law is expressed by the following equation:

$$\boldsymbol{u} = -\boldsymbol{k}\boldsymbol{x} \tag{5.59}$$

We assume the system is completely state controllable and observable, and $\boldsymbol{u}$ is unconstrained. Firstly, the reference input of the system is considered as zero, the system is also called a regulator system (show as Figure 5.18). If we substitute Equation 5.59 into Equation 5.58, it

gives

$$\begin{aligned} \dot{\boldsymbol{x}}(t) &= (\boldsymbol{A} - \boldsymbol{BK})\boldsymbol{x}(t) \\ \boldsymbol{x}(t) &= e^{(\boldsymbol{A}-\boldsymbol{BK})t}\boldsymbol{x}(0) \end{aligned} \tag{5.60}$$

where $\boldsymbol{x}(0)$ is the initial state. The stability and transient response characteristics are determi-

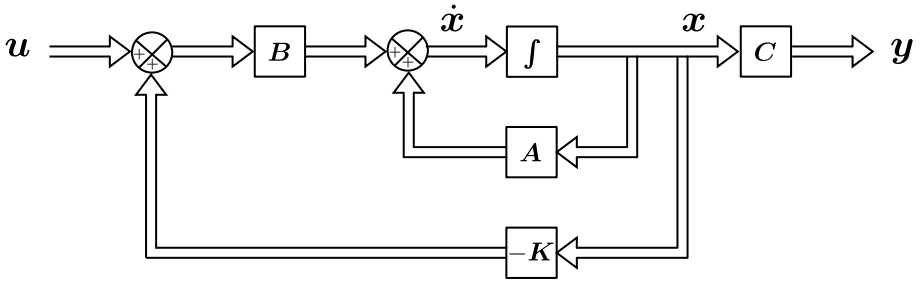


Figure 5.18: Block diagram of the state feedback control of a regulator system.

ned by the eigenvalues of matrix $\boldsymbol{A} - \boldsymbol{BK}$. By properly choosing the matrix $\boldsymbol{k}$, the eigenvalues of the matrix $\boldsymbol{A} - \boldsymbol{BK}$ or the closed-loop poles are placed in the left-half s plane, and the system response can be asymptotically stable and approach $\mathbf{0}$ as t approaches infinity. This problem of choosing the feedback gain matrix $\boldsymbol{k}$, thus placing the closed-loop poles at the desired location is called pole-placement method. It is worth to mention the precondition of the pole-placement method is completely state controllable. In the scope of this dissertation, all the states of the system are assumed controllable and observable without proof.

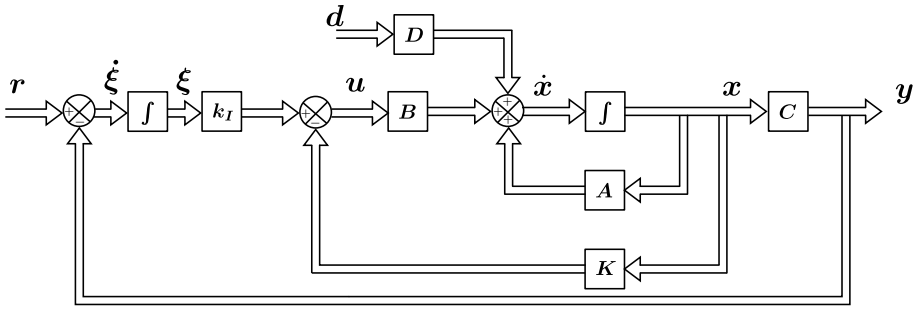


Figure 5.19: Block diagram of the state feedback control of a controller system.

Above we discussed the pole-placement method of a system with no reference input which can be called a regulator system. However, the other more common case which has more importance to the corresponding project is the controller system where the reference input is time varying. It is normally named as controller system according to [56]. The controller system can be divided into two categories – plant with and without integrator. As the relevance to the proposed grid emulator, in the following, only the second category is discussed. In contrast to the regulator system, an integrator is inserted in the feed-forward path between the error comparator and the plant as shown in Figure 5.19.

Based on the block diagram, the new system state space equations are:

$$\begin{aligned} \dot{\boldsymbol{x}} &= \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}u + \boldsymbol{D}\boldsymbol{d} \\ \boldsymbol{y} &= \boldsymbol{C}\boldsymbol{x} \\ \boldsymbol{u} &= -\boldsymbol{K}\boldsymbol{x} + \boldsymbol{k_I}\boldsymbol{\xi} \\ \dot{\boldsymbol{\xi}} &= \boldsymbol{r} - \boldsymbol{y} = \boldsymbol{r} - \boldsymbol{C}\boldsymbol{x} \end{aligned} \tag{5.61}$$

where $\boldsymbol{d}$ is the system disturbance vector, $\boldsymbol{r}$ is the reference vector, $\boldsymbol{\xi}$ is the output of the integrator. Similarly we assume that the system Equation 5.61 is fully controllable and observable. It can be reformulated as the following equation:

$$\begin{bmatrix} \dot{\boldsymbol{x}}(t) \\ \dot{\boldsymbol{\xi}}(t) \end{bmatrix} = \begin{bmatrix} \boldsymbol{A} & \boldsymbol{0} \\ -\boldsymbol{C} & \boldsymbol{0} \end{bmatrix} \begin{bmatrix} \boldsymbol{x}(t) \\ \boldsymbol{\xi}(t) \end{bmatrix} + \begin{bmatrix} \boldsymbol{B} \\ 0 \end{bmatrix} \boldsymbol{u}(t) + \begin{bmatrix} \boldsymbol{D} \\ \boldsymbol{0} \end{bmatrix} \boldsymbol{d}(t) + \begin{bmatrix} \boldsymbol{0} \\ \boldsymbol{1} \end{bmatrix} \boldsymbol{r}(t) \tag{5.62}$$

We also assume the system is asymptotically stable, therefore $\boldsymbol{x}(\infty)$, $\boldsymbol{\xi}(\infty)$, $\boldsymbol{u}(\infty)$ and $\boldsymbol{d}(\infty)$ approach constant values. Then, at steady state $\dot{\boldsymbol{\xi}}(\boldsymbol{t}) = \boldsymbol{0}$, $\boldsymbol{y}(\infty) = \boldsymbol{r}$.

$$\begin{bmatrix} \dot{\boldsymbol{x}}(\infty) \\ \dot{\boldsymbol{\xi}}(\infty) \end{bmatrix} = \begin{bmatrix} \boldsymbol{A} & \boldsymbol{0} \\ -\boldsymbol{C} & \boldsymbol{0} \end{bmatrix} \begin{bmatrix} \boldsymbol{x}(\infty) \\ \boldsymbol{\xi}(\infty) \end{bmatrix} + \begin{bmatrix} \boldsymbol{B} \\ \boldsymbol{0} \end{bmatrix} \boldsymbol{u}(\infty) + \begin{bmatrix} \boldsymbol{D} \\ \boldsymbol{0} \end{bmatrix} \boldsymbol{d}(\infty) + \begin{bmatrix} \boldsymbol{0} \\ \boldsymbol{1} \end{bmatrix} \boldsymbol{r}(\infty) \tag{5.63}$$

For step changing of the reference, $\boldsymbol{r}(\infty) = \boldsymbol{r}(t) = \boldsymbol{r}(t > 0)$. The time constant of the system is normally much slower than the controller period, $\boldsymbol{d}(\infty) = \boldsymbol{d}(t) = \boldsymbol{d}$. By subtracting the above equations, we obtain:

$$\begin{bmatrix} \dot{\boldsymbol{x}}(t) - \dot{\boldsymbol{x}}(\infty) \\ \dot{\boldsymbol{\xi}}(t) - \dot{\boldsymbol{\xi}}(\infty) \end{bmatrix} = \begin{bmatrix} \boldsymbol{A} & \boldsymbol{0} \\ -\boldsymbol{C} & \boldsymbol{0} \end{bmatrix} \begin{bmatrix} \boldsymbol{x}(t) - \boldsymbol{x}(\infty) \\ \boldsymbol{\xi}(t) - \boldsymbol{\xi}(\infty) \end{bmatrix} + \begin{bmatrix} \boldsymbol{B} \\ \boldsymbol{0} \end{bmatrix} [\boldsymbol{u}(t) - \boldsymbol{u}(\infty)] \tag{5.64}$$

We define:

$$\begin{aligned} \boldsymbol{x}_e(t) &= \boldsymbol{x}(t) - \boldsymbol{x}(\infty) \\ \boldsymbol{\xi}_e(t) &= \boldsymbol{\xi}(t) - \boldsymbol{\xi}(\infty) \\ \boldsymbol{u}_e(t) &= \boldsymbol{u}(t) - \boldsymbol{u}(\infty) \end{aligned} \tag{5.65}$$

Then 5.64 can be rewritten as

$$\begin{bmatrix} \dot{\boldsymbol{x}}_e(t) \\ \dot{\boldsymbol{\xi}}_e(t) \end{bmatrix} = \begin{bmatrix} \boldsymbol{A} & \boldsymbol{0} \\ -\boldsymbol{C} & \boldsymbol{0} \end{bmatrix} \begin{bmatrix} \boldsymbol{x}_e(t) \\ \boldsymbol{\xi}_e(t) \end{bmatrix} + \begin{bmatrix} \boldsymbol{B} \\ \boldsymbol{0} \end{bmatrix} \boldsymbol{u}_e(t) \tag{5.66}$$

$$\boldsymbol{u}_e(t) = -\boldsymbol{K}\boldsymbol{x}_e(t) + \boldsymbol{k_I}\boldsymbol{\xi_e(t)} \tag{5.67}$$

Here by defining a new $(n+r)^{th}$ order error vector $\boldsymbol{e}(t)$ and new error system matrix $\hat{\boldsymbol{A}}$, $\hat{\boldsymbol{B}}$ and $\hat{\boldsymbol{K}}$ as following:

$$\boldsymbol{e}(t) = \begin{bmatrix} \boldsymbol{x}_e(t) \\ \boldsymbol{\xi}_e(t) \end{bmatrix}$$

$$\hat{\boldsymbol{A}} = \begin{bmatrix} \boldsymbol{A} & \boldsymbol{0} \\ -\boldsymbol{C} & \boldsymbol{0} \end{bmatrix}, \qquad \hat{\boldsymbol{B}} = \begin{bmatrix} \boldsymbol{B} \\ \boldsymbol{0} \end{bmatrix} \tag{5.68}$$

$$\hat{\boldsymbol{K}} = \begin{bmatrix} \boldsymbol{K} & \vdots - \boldsymbol{k_I} \end{bmatrix}$$

Equation 5.66 and 5.67 can be rewrite as new error state space equation as:

$$\begin{aligned} \dot{\boldsymbol{e}} &= \hat{\boldsymbol{A}}\boldsymbol{e} + \hat{\boldsymbol{B}}\boldsymbol{u}_e \\ \boldsymbol{u}_e &= -\hat{\boldsymbol{K}}\boldsymbol{e} \end{aligned} \tag{5.69}$$

By solving the above equation, it gives the error state expression as:

$$\begin{aligned} \dot{\boldsymbol{e}}(t) &= (\hat{\boldsymbol{A}} - \hat{\boldsymbol{B}}\hat{\boldsymbol{K}})\boldsymbol{e}(t) \\ \boldsymbol{e}(t) &= e^{(\hat{\boldsymbol{A}}-\hat{\boldsymbol{B}}\hat{\boldsymbol{K}})t}\boldsymbol{e}(0) \end{aligned} \tag{5.70}$$

If one compares Equation 5.70 and 5.60, it is easy to notice that they have the same form. Therefore, by adding one integer and one gain block k_i in the reference feed-forward path (Figure 5.19), the new system's error state space controller has the same solution as the regulator system (Figure 5.18). By properly choosing the new state feedback matrix $\hat{\boldsymbol{K}}$, all poles of the closed-loop system can be placed as where the designer desired. By doing this, the system responses of any steady and transient states are controlled as required.

The controllability and observability of the state space system are out the scope of this thesis. Several different kinds of methods of the feedback matrix determination are presented in the literature. Matlab also provides an effective solution for pole-placement problems. Therefore, the computation of a feedback gain matrix is not a difficult problem after choosing the locations of desired closed-loop poles. However, the approach of pole placement strongly relies on the designer's experiences in the root-locus design. Because the system response speed and system control signal energy are two mutual constraints of the poles-placement, it is very hard to optimize the controller design. The following discussed quadratic optimal control determines the desired poles such that it balances between the satisfied response and acceptable control energy.

5.3.2 Linear quadratic optimal controller for the proposed grid emulator

Liner quadratic control as one of the optimal control optimizes the control objectives by minimizing the formulated cost function. In this dissertation, we focus on the control system which has the linear quadratic cost criterion, and the optimization is over an infinite horizon. This so-called infinite horizon linear quadratic controller (LQR) has remarkable superiorities than the common pole-placement strategy. It not only results in instinct closed-loop stability, but also provides a systematic computation of the optimal feedback gain matrix $\boldsymbol{K}$. It results in a unique control law, has reasonably good interpretation for the choice of the design parameters $\boldsymbol{Q}$ and $\boldsymbol{R}$, avoids the need to specify desired pole locations (often chosen without good design reasons), has good transient response, and has better numerical properties than pole placement design. For these reasons, LQR design is often preferred over pole placement in control design practice.

Here we consider the optimal problem of the state space system described as:

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} \tag{5.71}$$

LQR determines the optimal matrix $\boldsymbol{K}$ of the optimal control vector

$$\boldsymbol{u}(t) = \boldsymbol{K}\boldsymbol{x}(t) \tag{5.72}$$

By minimizing the cost function

$$J = \int_0^\infty (\boldsymbol{x}^T \boldsymbol{Q} \boldsymbol{x} + \boldsymbol{u}^T \boldsymbol{R} \boldsymbol{u}) dt \tag{5.73}$$

where $\boldsymbol{Q}$ is a positive-semidefinite Hermitian or real symmetric matrix, and it represents the weight of the state vector away form final value of $\mathbf{0}$. $\boldsymbol{R}$ is a positive-definite Hermitian or real symmetric matrix, and it represents the control effort of regulating the state vector to $\mathbf{0}$. The choice of $\boldsymbol{Q}$ and $\boldsymbol{R}$ reflects the trade-off between the response characteristics of regulating and the expenditure of control energy.

The derivation of the optimal feedback matrix $\boldsymbol{K}$ is out of the scope, and for simplicity the following conclusion is directly presented. Before we get the optimal $\boldsymbol{K}$, a positive-definite matrix $\boldsymbol{P}$ must be solved by the most famous algebraic *Riccati* equation in linear control theory shown as:

$$\boldsymbol{A}^T \boldsymbol{P} + \boldsymbol{P} \boldsymbol{A} - \boldsymbol{P} \boldsymbol{B} \boldsymbol{R}^{-1} \boldsymbol{B}^T \boldsymbol{P} + \boldsymbol{Q} = \mathbf{0} \tag{5.74}$$

After getting the solution of the $\boldsymbol{P}$ from Equation 5.74, the optimal control is give by:

$$\boldsymbol{u}(t) = -\boldsymbol{K} \boldsymbol{x}(t) = -\boldsymbol{R}^{-1} \boldsymbol{B}^T \boldsymbol{P} \boldsymbol{x}(t) \tag{5.75}$$

$$\boldsymbol{K} = -\boldsymbol{R}^{-1} \boldsymbol{B}^T \boldsymbol{P} \tag{5.76}$$

However the computation of the *Riccati* equation is normally very complicated and difficult, MATLAB provides an effective solution for this problem with commands:

$$lqr(\boldsymbol{A}, \boldsymbol{B}, \boldsymbol{Q}, \boldsymbol{R}). \tag{5.77}$$

Regarding to the proposed inverter with an LC-filter system, the state space equations are as:

$$\begin{aligned}
\begin{bmatrix} \dot{V^q_{C_f}}(t) \\ \dot{V^d_{C_f}}(t) \\ \dot{i^q_{inv}}(t) \\ \dot{i^d_{inv}}(t) \end{bmatrix} &= \begin{bmatrix} 0 & -\omega & \frac{1}{C_f} & 0 \\ \omega & 0 & 0 & \frac{1}{C_f} \\ -\frac{1}{L_f} & 0 & 0 & -\omega \\ 0 & -\frac{1}{L_f} & \omega & 0 \end{bmatrix} \begin{bmatrix} V^q_{C_f}(t) \\ V^d_{C_f}(t) \\ i^q_{inv}(t) \\ i^d_{inv}(t) \end{bmatrix} \\
&+ \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{1}{L_f} & 0 \\ 0 & \frac{1}{L_f} \end{bmatrix} \begin{bmatrix} V^q_{inv}(t) \\ V^d_{inv}(t) \end{bmatrix} + \begin{bmatrix} -\frac{1}{C_f} & 0 \\ 0 & -\frac{1}{C_f} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i^q_{load}(t) \\ i^d_{load}(t) \end{bmatrix}
\end{aligned} \tag{5.78}$$

$$\begin{bmatrix} V^q_{C_f}(t) \\ V^d_{C_f}(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V^q_{C_f}(t) \\ V^d_{C_f}(t) \\ i^q_{inv}(t) \\ i^d_{inv}(t) \end{bmatrix} \tag{5.79}$$

By comparing the Equation 5.78 and 5.79 with 5.61, we have:

$\boldsymbol{x} = \begin{bmatrix} V_{C_f}^q(t) & V_{C_f}^d(t) & i_{inv}^q(t) & i_{inv}^q(t) \end{bmatrix}^T$, $\boldsymbol{u} = \begin{bmatrix} V_{inv}^q(t) & V_{inv}^d(t) \end{bmatrix}^T$,
$\boldsymbol{y} = \begin{bmatrix} V_{C_f}^q(t) & V_{C_f}^d(t) \end{bmatrix}^T$, $\boldsymbol{d} = \begin{bmatrix} i_{load}^q(t) & i_{load}^d(t) \end{bmatrix}^T$

and $\boldsymbol{A} = \begin{bmatrix} 0 & -\omega & \frac{1}{C_f} & 0 \\ \omega & 0 & 0 & \frac{1}{C_f} \\ -\frac{1}{L_f} & 0 & 0 & -\omega \\ 0 & -\frac{1}{L_f} & \omega & 0 \end{bmatrix}$, $\boldsymbol{B} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{1}{L_f} & 0 \\ 0 & \frac{1}{L_f} \end{bmatrix}$, $\boldsymbol{C} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}$,

$\boldsymbol{D} = \begin{bmatrix} -\frac{1}{C_f} & 0 \\ 0 & -\frac{1}{C_f} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$.

By substituting into Equation 5.68, we get:

$$\boldsymbol{e}(t) = \begin{bmatrix} V_{C_f}^q(t) \\ V_{C_f}^d(t) \\ i_{inv}^q(t) \\ i_{inv}^d(t) \\ \xi_e^q(t) \\ \xi_e^d(t) \end{bmatrix}, \quad \hat{\boldsymbol{A}} = \begin{bmatrix} 0 & -\omega & \frac{1}{C_f} & 0 & 0 & 0 \\ \omega & 0 & 0 & \frac{1}{C_f} & 0 & 0 \\ -\frac{1}{L_f} & 0 & 0 & -\omega & 0 & 0 \\ 0 & -\frac{1}{L_f} & \omega & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix},$$

$$\hat{\boldsymbol{B}} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{1}{L_f} & 0 \\ 0 & \frac{1}{L_f} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad \hat{\boldsymbol{K}} = \begin{bmatrix} K_v^{qq} & K_v^{qd} & K_i^{qq} & K_i^{qd} & \vdots - k_I^{qq} & -k_I^{qd} \\ K_v^{dd} & K_v^{dq} & K_i^{dd} & K_i^{dq} & \vdots - k_I^{dd} & -k_I^{dq} \end{bmatrix}. \tag{5.80}$$

Before we solve the optimal feedback controller gain, the proper weighting matrix $\boldsymbol{Q}$ and $\boldsymbol{R}$ are only design parameters. As illustrated before, the elements of $\boldsymbol{Q}$ weights the gap of the vector's state and final reference value. Relating to the proposed project, in order to achieve a faster transient response, the weighting factor of ξ_e must be sufficiently large compared with the others. In this problem, the weighting matrices are chosen based on the simulation as follows:

$$\boldsymbol{Q} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 200/C_f & 0 \\ 0 & 0 & 0 & 0 & 0 & 200/C_f \end{bmatrix}, R = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}. \tag{5.81}$$

The MATLAB program of the controller design is shown below.

MATLAB Program of quadratic optimal controller design

```
Lf= 3e-3, w=2pi*50, Cf= 30e-6;
A=[0, -w, 1/Cf, 0, 0, 0; w, 0, 0, 1/Cf, 0, 0; -1/Lf, 0,
0, -w, 0, 0; 0, -1/Lf, w, 0, 0, 0; -1, 0, 0, 0, 0, 0; 0,
-1, 0, 0, 0, 0];
B=[0, 0; 0, 0; 1/L, 0; 0, 1/L; 0, 0; 0, 0], R=[1,0;0,1];
Q=[1,0,0,0,0,0; 0, 1, 0,0,0,0; 0,0,1,0,0,0; 0,0,0,1,0,0;
0,0,0,0, 200/Cf,0;0,0,0,0,0,200/Cf];
K=lqr(A,B,Q,R);
%Program Output--------------------
K= [1.1, 0, 14.6, 0, -2571.6, -231.8; 0, 1.1, 0, 14.6,
231.8, -2571.6];
```

Therefore, the final feedback gain matrix is:

$$\begin{aligned} K_v^{qq} &= K_v^{dd} = 1.1 \\ K_v^{qd} &= K_v^{dq} = 0 \\ K_i^{qq} &= K_i^{dd} = 14.6 \\ K_i^{qd} &= K_i^{dq} = 0 \\ k_I^{qq} &= k_I^{dd} = 2571.6 \\ k_I^{qd} &= -k_I^{dq} = 231.8 \end{aligned} \tag{5.82}$$

The controller will be implemented as shown in Figure 5.20 with all the parameters expressed as Equation 5.82.

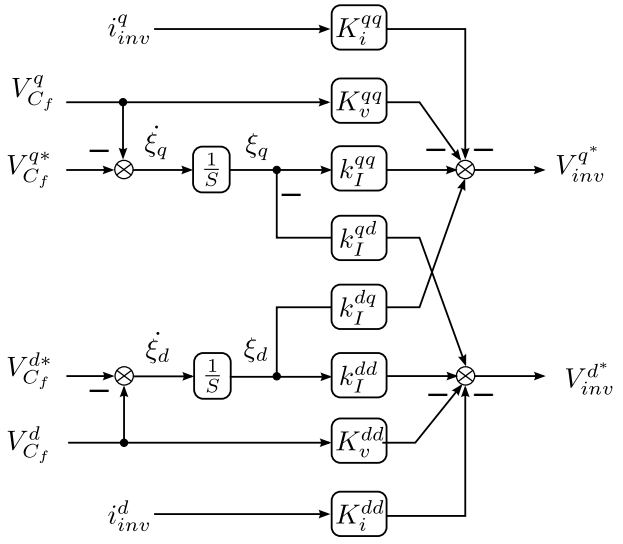


Figure 5.20: Block diagram of the LQR controller in dq frame.

5.4 Discretization the continuous design via transform methods

In the previous sections, all the control strategies are designed based on the analyses of the system in the continuous domain and they have to be transformed into its equivalent discrete forms as a requirement of the modern digital controller relying on the discrete signals. Therefore, it is important to investigate the discretization methods of the pre-designed controller which is represented by its Laplace s-function. This section will illustrate the two main discrete equivalent processes: numerical integration and zero hold equivalent. After gaining enough background knowledge, the discretization of the general form of the PR and the LQR controller will be presented under the help of MATLAB at the end.

5.4.1 Numerical integration discrete equivalent

The numerical integration of the differential equations is very complex itself. The following parts explain only the fundamental concepts and conclusions. We consider a transfer function $H(s)$ as:

$$H(s) = \frac{U(s)}{E(s)} = \frac{a}{s+a} \tag{5.83}$$

according to [57], we can reform it into integral form as following:

$$u(t) = \int_0^t [-au(\tau) + ae(\tau)]d\tau \tag{5.84}$$

$$u(kT) = \int_0^{kT-T} [-au(\tau) + ae(\tau)]d\tau + \int_{kT-T}^{kT} [-au(\tau) + ae(\tau)]d\tau \tag{5.85}$$

$$= u(kT-T) + \left\{ \begin{array}{cc} \textit{area of} & -au(\tau) + ae(\tau) \\ \textit{over} & kT - T \leqslant \tau < kT \end{array} \right. \tag{5.86}$$

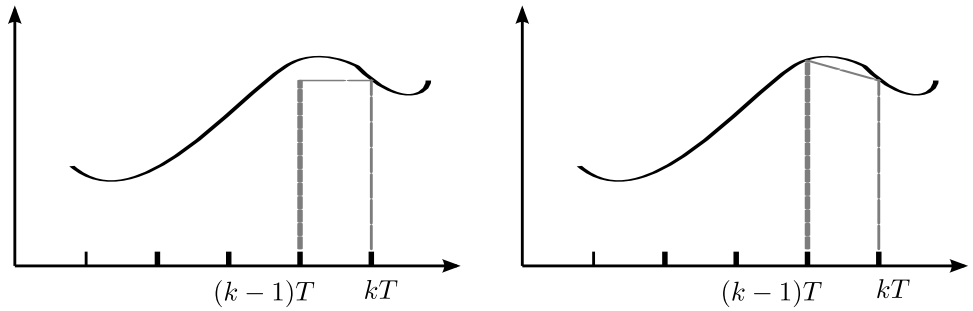
Several different methods have been developed to approximate the incremental area term of Equation 5.86. There are three main strategies: forward rectangular rule, backward rectangular rule and bilinear or trapezoid rule. It is known that, the discrete equivalent by the forward rectangular rule may not always stay stable. Therefore, the forward rule is not recommended. The backward and bilinear rule will be explained in the following and schematically demonstrated by the Figure 5.21

The back rectangular rule follows from taking the amplitude of the approximating rectangle to be the value backward from kT toward $(k-1)T$. The equation of $u(kT)$ approximates as:

$$\begin{aligned} u(kT) &= u(kT-T) + T[-au(kT) + ae(kT)] \\ &= \frac{u(kT-T)}{1+aT} + \frac{aT}{1+aT}e(kT). \end{aligned} \tag{5.87}$$

The z-transform of Equation 5.87 is:

$$\begin{aligned} H_B(z) &= \frac{aTz}{z(1+aT)-1} \\ &= \frac{a}{(z-1)/Tz + a}. \end{aligned} \tag{5.88}$$



(a) Backward rectangular rule (b) Bilinear or trapezoid rule

Figure 5.21: Approximation rules of the incremental area [57].

Similarly, the bilinear approximation takes the trapezoid area of figure 5.21(b). The approximating difference equation is:

$$\begin{aligned} u(kT) &= u(kT-T) + \frac{T}{2}[-au(kT-T) + ae(kT-T) - au(kT) + ae(kT)] \\ &= \frac{1-(aT/2)}{1+(aT/2)}u(kT-T) + \frac{aT/2}{1+aT/2}[e(kT-T) + e(kT)]. \end{aligned} \tag{5.89}$$

again, by applying the z-transform we can get the equation:

$$\begin{aligned} H_T(z) &= \frac{aTz}{z(2+aT) + aT - 2} \\ &= \frac{a}{(2/T)[(z-1)/(z+1) + a}. \end{aligned} \tag{5.90}$$

If one compares Equation 5.83 with 5.88 and 5.90, it can be seen that a discrete transfer function can be obtained from the Laplace transfer function by substitution of an approximation for the frequency variable as shown in the table below. According to Table 5.1, the discretization

Table 5.1: Discrete method

Method	Approximation
Backward	$s \to \frac{z-1}{Tz}$
Bilinear	$s \to \frac{2}{T}\frac{z-1}{z+1}$

method of a continuous controller can be summarized by substitution:

$$H_B(z) = H(s)|_{\frac{z-1}{Tz}} \tag{5.91}$$

$$H_T(z) = H(s)|_{s=\frac{2}{T}\frac{z-1}{z+1}}. \tag{5.92}$$

Equation 5.92 is also called Tustin's method which maps the stable region of the s-plane exactly into the stable region of the z-plane. The stability of the discrete transform is assured. This

method will be used in the aforementioned PR controller. In Matlab, the command below helps to convert the controller transfer function under CAD

$$H(z)_d = c2d(H(s)_c, \quad T_s, \quad 'tustion') \tag{5.93}$$

Where T_s is the sampling frequency of the controller.

5.4.2 Zero order hold equivalent method

The other method is called the hold equivalence and is similar to the signal sampling mechanism. It is based on taking the samples of the signals, extrapolating between samples to form an approximation of the signal. There are several different kinds of the hold techniques, and the most common one is the zero order hold (ZOH) method. In this subsection, the principle of the ZOH will be first illustrated. Later, the discrete equivalent of the continuous sate space expression of the plant will be presented. As the state space feedback control is normally based directly on the direct digital control, it is required to find the discrete equivalent of its continuous plant.

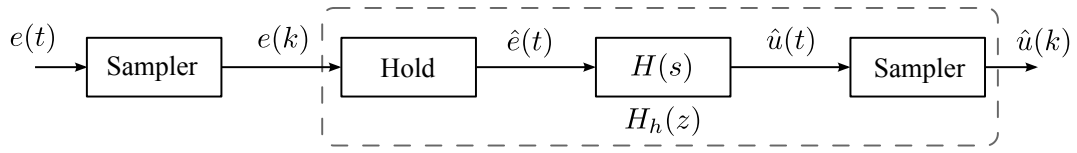


Figure 5.22: Block diagram of the zero order hold discrete equivalent method.

We use Figure 5.22 to explain the principle of the hold equivalent. The input signal $e(t)$ will be sampled as $e(k)$, then held as $\hat{e}(t)$, and passed through $H(s)$ to get $\hat{u}(t)$. The output $\hat{u}(t)$ will be sampled as $\hat{u}(k)$. The discrete equivalent $H_h(z)$ is the combination of the hold, $H(s)$ and the sampler as shown in Figure 5.22. If the holder is a zero order it is called ZOH discrete equivalent. Here, without the derivation, the ZOH discrete equivalent of $H(s)$ is given by

$$H_{h0} = (1 - z^{-1})Z\left\{\frac{H(s)}{s}\right\}. \tag{5.94}$$

Now we pay attention to a linear time invariant state space plant presented as:

$$\begin{cases} \dot{\boldsymbol{x}} &= \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} \\ \boldsymbol{y} &= \boldsymbol{C}\boldsymbol{x} + \boldsymbol{D}\boldsymbol{u} \end{cases} \tag{5.95}$$

according to modern control theory literature, the solution of the Equation 5.95 is:

$$\boldsymbol{x}(t) = e^{\boldsymbol{A}(t-t_0)}\boldsymbol{x}(t_0) + \int_{t_0}^{t} e^{\boldsymbol{A}(t-\tau)}\boldsymbol{B}\boldsymbol{u}(\tau)d\tau. \tag{5.96}$$

if we consider $t_0 = kT, t = (k+1)T$, according to the ZOH rule $\boldsymbol{u}[kT \leqslant t < (k+1)T] = \boldsymbol{u}(kT)$. Then above equation can be rewritten as:

$$\begin{aligned} \boldsymbol{x}[(k+1)T] &= \boldsymbol{\Phi}[(k+1)T - kT]\boldsymbol{x}(kT) + \int_{kT}^{(k+1)T} \boldsymbol{\Phi}[(k+1)T - \tau]\boldsymbol{B}\boldsymbol{u}(\tau)d\tau \\ &= \boldsymbol{\Phi}(T)\boldsymbol{x}(kT) + \int_{kT}^{(k+1)T} \boldsymbol{\Phi}[(k+1)T - \tau]\boldsymbol{B}d\tau\boldsymbol{u}(kT). \end{aligned} \tag{5.97}$$

where $\mathbf{\Phi}(T) = e^{\boldsymbol{A}t}$, we define:

$$\mathbf{\Gamma} = \int_{kT}^{(k+1)T} \mathbf{\Phi}[(k+1)T - \tau]\boldsymbol{B}d\tau. \tag{5.98}$$

if we substitute the $t = (k+1)T - \tau$, the above equation is rewritten as:

$$\mathbf{\Gamma} = \int_{T}^{(0} \mathbf{\Phi}(t)\boldsymbol{B}(-dt) = (\int_{0}^{T} e^{At}dt)\boldsymbol{B}. \tag{5.99}$$

The discrete equivalent of the state space model (equation 5.95) can be described as following:

$$\begin{cases} \boldsymbol{x}(k+1) & = \mathbf{\Phi}\boldsymbol{x}(k) + \mathbf{\Gamma}\boldsymbol{u}(k) \\ \boldsymbol{y}(k) & = \boldsymbol{C}\boldsymbol{x}(k) + \boldsymbol{D}\boldsymbol{u}(k) \end{cases} \tag{5.100}$$

However the calculation of $\mathbf{\Phi}$ and $\mathbf{\Gamma}$ is very complicated and tedious, and normally the discretization is done by the help of the Matlab:

$$sysD = c2d(sysC, T). \tag{5.101}$$

where $sysC$ contains $\boldsymbol{A}, \boldsymbol{B}, \boldsymbol{C}, \boldsymbol{D}$. The above Matlab script transforms $sysC$ to the discrete model $\mathbf{\Phi}, \mathbf{\Gamma}, \boldsymbol{C}, \boldsymbol{D}$ (or $sysD$) with a sample period T.

5.4.3 PR and LQR controller discretization and implementation in real-time system

Now we try to apply the discretization method described before to the designed controller in continuous time domain.

Case 1: PR-controller

Based on the simulation, the final well tuned PR controller is described by the following equation:

$$\frac{v_{error}(s)}{i_{ref}(s)} = k_p + \frac{2k_i\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} = \frac{k_p s^2 + 2\omega_c(k_p + k_i)s + k_p\omega_0^2}{s^2 + 2\omega_c s + \omega_0^2} \tag{5.102}$$

By substituting $k_p = 0.028, k_i = 0.06, \omega_c = 3 * 2\pi, \omega_0 = 50 * 2\pi$, we get

$$\frac{v_{error}(s)}{i_{ref}(s)} = \frac{0.028s^2 + 3.318s + 98700}{s^2 + 37.7s + 98700} \tag{5.103}$$

If the bilinear method is adopted, one can either substitute s by its approximation $\frac{2}{Ts}\frac{z-1}{z+1}$ or use the MATLAB command $c2d(H_c(s), Ts, 'tustion')$. The discrete controller is expressed by the following:

$$\frac{v_{error}(z)}{i_{ref}(z)} = \frac{az^2 - bz + c}{dz^2 - ez + f} \tag{5.104}$$

where $a = 0.112425, b = 0.223978, c = 0.111596, d = 4.005098, e = 7.999229, f = 3.995673$. Based on equation 5.104, the algorithm expressed below will be implemented in the real-time controller.

$$\begin{aligned} i_{ref}(kT_s) &= (a/d)v_{error}(kT_s) - (b/d)v_{error}(kT_s - T_s) \\ &+ (c/d)v_{error}(kT_s - 2T_s) + (e/d)i_{ref}(kT_s - T_s) \\ &- (f/d)i_{ref}(kT_s - 2T_s) \end{aligned} \tag{5.105}$$

Case 2: LQR-controller

In Subsection 5.3.2, the LQR controller is designed based on the system state space equation in the continuous time domain. However, the system signals are discretely sampled by the AD converter of the real-time system, a design based on the continuous model will not work properly due to the sampling and hold mechanism of the digital controller. Therefore, the system state space equation has to be transformed into its discrete form by the ZOH method, then the LQR feedback matrix gain based on this discrete state space system has to be calculated.

According to Subsection 5.4.2, one could calculate the discrete matrix by:

$$\begin{aligned} \boldsymbol{\Phi} &= e^{\boldsymbol{A}T_s} \\ \boldsymbol{\Gamma} &= (\int_0^{T_s} e^{\boldsymbol{A}t} dt)\boldsymbol{B} \end{aligned} \tag{5.106}$$

Or one can use MATLAB to design the discrete controller by using the following program.

MATLAB Program of quadratic optimal controller design

```
Lf= 3e-3, w=2pi*50, Cf= 30e-6, Ts =6.25e-5;;
A=[0, -w, 1/Cf, 0, 0, 0; w, 0, 0, 1/Cf, 0, 0; -1/Lf, 0,
0, -w, 0, 0; 0, -1/Lf, w, 0, 0, 0; -1, 0, 0, 0, 0, 0; 0,
-1, 0, 0, 0, 0];
B=[0, 0; 0, 0; 1/L, 0; 0, 1/L; 0, 0; 0, 0], R=[1,0;0,1];
Q=[1,0,0,0,0,0; 0, 1, 0,0,0,0; 0,0,1,0,0,0; 0,0,0,1,0,0;
0,0,0,0, 200/Cf,0;0,0,0,0,0,200/Cf];
Kd=lqrd(A,B,Q,R, Ts); % discrete-time lqr
%Program Output--------------------
K= [0.8, 0, 13.5, 0.1, -2208.4, -200.1; 0, 0.8, 0.1,
13.5, 200.1, -2208.4;
```

We get the feedback gain matrix $\boldsymbol{K_d}$ based on the discrete state space system as shown below.

$$\begin{aligned} K_v^{qq} &= K_v^{dd} &&= 0.8 \\ K_v^{qd} &= K_v^{dq} &&= 0 \\ K_i^{qq} &= K_i^{dd} &&= 13.5 \\ K_i^{qd} &= K_i^{dq} &&= 0.1 \approx 0 \\ k_I^{qq} &= k_I^{dd} &&= 2208.4 \\ k_I^{qd} &= -k_I^{dq} &&= 200.1 \end{aligned} \tag{5.107}$$

By comparing Equation 5.107 and 5.82, one can clearly notice the differences between the two designs.

5.5 Comparison of aforementioned control strategies

In this chapter, three different controller designs for the grid emulator were presented. The investigation of these different strategies shows the advantages and shortcomings of each case.

Table 5.2: Analytical comparison of three control schemes

	PI	PR	LQR
Operat. frame	dq	$\alpha\beta$	dq
Transfor. calc.	required	no	required
Decoupling net.	required	no	-
Harmonic rejection	bad	good	bad
Sequence control	only positive	positive and negative	only positive
Freq. sensitivity	only fundamental	light frequency variation	only fundamental
Tuning parameters	k_{pv}, k_{iv}, k_{pi}, k_{ii}	k_p, k_i, ω_c, k_c	$\boldsymbol{Q}$
Optimization	-	-	instinct optimization

This section summarizes the characteristics of all controllers, and gives an analytical comparison between them.

The conventional PI controller is simple to implement and easy to understand. It is designed with the frequency response method, and it exhibits a satisfied performance for the system transient and steady state response. However, due to its frequency sensitivity, the PI controller has a very limited harmonic rejection capability. In the case of the nonlinear EUT, the highly distorted currents deteriorate the controller performance. Therefore, the grid emulator can not comply with the voltage standard which requires the THD smaller than 2.5%. In order to solve this problem, selective harmonic compensators have to be implemented. But it requires excessive computational resources for the different frames transformation. Moreover, the decoupling networks are needed for each controller in every frame. Taking all these shortcomings into account, the PI controller is unacceptable.

The PR controller is implemented in the stationary frame. The frame transformation computation and the cross-coupling items are completely eliminated. An effective selective harmonic compensator can be achieved conveniently as shown in figure 5.12. As presented previously, the practical form of the PR controller introduces a new parameter – cut off frequency ω_c, thus the controller has a wider bandwidth around the resonant frequency. This moderates the controller's frequency sensitivity, and improves the THD performance of the grid emulator especially for the nonlinear EUT situation. Moreover, compared with the PI controller, the PR controller has both positive and negative sequence signal control capability, therefore it could be also capable of controlling the unbalanced voltage of the grid emulator. Last but not least, according to [43, 48], for the digital implementation, the P+R controller requires less signal processing, and it is also less sensitive to noise. In the worst case, it costs similar computational resources to that required for a Park transformation. Because of all these advantages, the PR controller is investigated after the PI controller.

The PI and PR controllers both perform well for the control task of the grid emulator. However, their tuning method is very complicated and not so systematic, and the optimization process is normally based on trial and error with the help of the frequency response and MAT-

LAB simulation, which is inaccurate, and very inefficient because of weak purpose and vague criteria. This unsatisfactory aspect is the main reason for investigating further control schemes – linear quadratic regulator (LQR) for the grid emulator. As presented in the previous section, the LQR results in closed-loop stability, and also provides a systematic computation of the optimal feedback gain matrix. In contrast to the PI and PR controller, it gives unique control law, and has reasonably good interpretation for the choice of the matrix $\boldsymbol{Q}$. Although the theory of state space control is difficult to understand, the controller design has to follow the summarized procedures. After modeling the state space equations of the system, the matrix required for the controller design can be directly derived through Equation 5.80. The only tuning parameter is the matrix $\boldsymbol{Q}$, and according to its representative meaning, only two elements for the voltage error in d and q axis should be tuned. The values of the elements are simply increased until the system transient performs a desired process. The LQR controller does not need to sense and feedback the load currents to achieve disturbance rejection. This characteristic saves two expensive current transducers. Therefore, the LQR is the most cost-effective control scheme among the other two.

CHAPTER 6

Final PHiL system realization and experimental verification

In order to validate the function of the proposed PhiL grid emulator, a downscaled 5 kVA PHiL prototype has been constructed. A self-designed real-time system is also implemented to control the *inverter cumulation* system. In this chapter, the real time system and hardware test bench will be presented first. Then the experimental results based on the aforementioned various control algorithms are presented one after the other.

6.1 Hybrid real-time control system

Nowadays, digital control techniques supported by processors (micro-controller or DSP) have replaced the traditional analogue control techniques which rely on discrete hardware components like operational amplifiers etc. DSP controllers are the most popular industrial solutions for many years. In general, all the processor based controllers are either triggered by an external signal or an internal timer generated interruption which forces it to start a new sampling period and then execute a cycle of the control algorithm in a real time. Several different peripheral devices can be integrated depending on the requirements. Normally units like the analogue-to-digital converter (ADC), current and voltage measurements, or PWM generation are very important for the power electronics control system. Besides, the human-machine-interaction (HMI) like digital-to-analogue converters, LCD display and control buttons are necessary to support the functionality of the real-time system. However, there are several drawbacks of the commercial system. Firstly, the high cost and licenses constraints normally cause big problems for universities and technical institutes. The more important limitation is the higher average latency of the processor-based real-time system, which is the consequence of the sequential execution principle.

Thanks to the fast development of the Complex Programmable Logic Devices (CPLDs) and Field Programmable Arrays (FPGAs) in recent years, a quasi-analogue controller became fea-

sible recently [58], especially since FPGAs have more and more logic elements, making them capable of implementing more complex computations than before. The most important feature of the quasi-analogue or quasi-hardware controller compared to the software controller is that the complexity of the computations dominates the amount of hardware resources needed instead of the speed of execution. As it is well known, the time delay of hardware processing is within one or a few clock cycles which is almost negligible compared to the software controller. Furthermore, besides the traditional sequential execution, the hardware implementation can achieve the parallel execution which enables the controller to process different tasks simultaneously. By doing this, the calculation time is dramatically decreased. However, in order to implement the control algorithm on the hardware controller, the complicate VHDL (Very High Speed Integrated Circuit Hardware Description Language) or Verilog language is necessary. The flexible floating-point operation is not possible any more. Instead the more complicated fixed-point computation has to be used. Therefore, as a result of the complex program language, the implementation of the FPGAs controller is very time-consuming, And due to the noncompetitive fixed-point operation, math calculation are very resource-consuming.

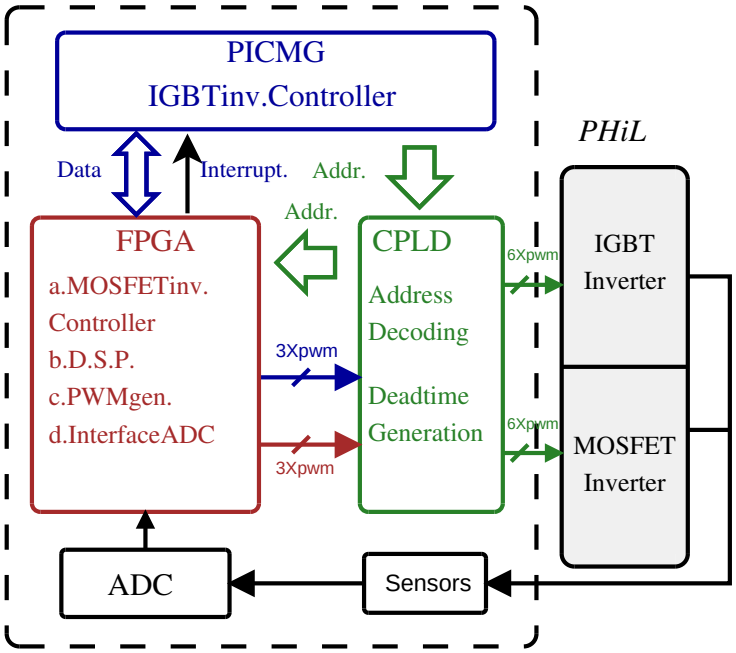


Figure 6.1: Principle diagram of the self-developed FPGA-based real-time system.

As the switching frequency of a MOSFET inverter is above 50kHz, and due to the stringent time constraints and complex control algorithms, it is beyond the capability of a common processor-based controller to control the inverter. In order to implement the control algorithm of the inverter cumulation system, an FPGA-based hybrid real time system with an RTAI-Linux [59] was developed at our institute. In Figure 6.1, the principle schematic shows the three main parts (PICMG main board, FPGA board and CPLD board) of the system. The PICMG main board has a Pentium 4-CPU (3.4GHz). Installed is a Linux based operating system with an RTAI kernel-Patch. The controller of the IGBT inverter is implemented as an interrupt service routine of the CPU which is triggered by the FPGA in real time. The FPGA board

with a Cyclone III FPGA serves as the core element of the system. Its functions include digital signal processing, PWM generation, communication interface with the AD converter and the CPU interrupt generation. Besides, due to the aforementioned ultra fast program execution capability, the MOSFET inverter controller is also implemented in the FPGA. The CPLD takes the response of address decoding of the ISA-Bus of the PICMG main board and the dead time generation for the inverter driver. The above mentioned real-time system combines both the digital and quasi-analogue controller together as a hybrid system, which achieves the control task for the *inverter cumulation* system.

The IGBT inverter controller is implemented in the processor-based controller. The algorithms are programmed as Linux kernel modules which are triggered to execute in real time by an external interrupt from the FPGA. The programming language is C code, and the floating-point math operation is also available. This makes the control solution very flexible and efficient. The MOSFET inverter controller, on the other hand, which requires a fast control cycle period, is programmed by the VHDL in the FPGA. Although the implementation is relatively more complicated than the digital controller, the execution latency requirement is fulfilled.

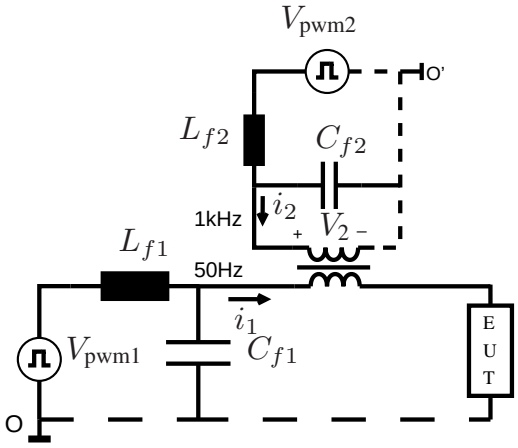
6.2 Prototype test bench of the *inverter cumulation* system

The prototype test bench is shown in Figure 6.2. It consists of an SEW commercial three-phase 5KVA IGBT inverter and a MITSUBISHI low voltage ($V_{DS} = 100V$) MOSFET power module FM200TU. The key issue of the system implementation is the coupling inductor design. The following section will present the system in detail.

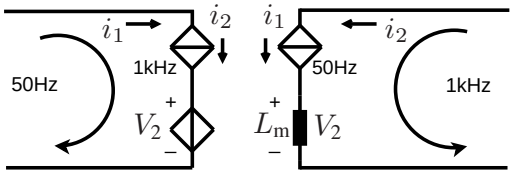
Figure 6.2: Experimental setup of the prototype grid emulator. Upper left: power stage and inductor. Bottom left: coupling inductors and capacitors. Right: Overview of the system.

6.2.1 Magnetic coupling inductor design and implementation

The coupling inductor is the key component of the inverter cumulation system. Ideally, the coupling inductor should inject the high frequency voltage waves generated by the MOSFFET inverter to the IGBT inverter output terminals. However on the other hand, the influence of the IGBT inverter on the MOSFET inverter has to be as minimum as possible. The single phase equivalent diagram is shown in Figure 6.3(a), and for simplification we assume there is no switching component after the LC filter. The criteria of the coupling inductor design is that the magnetic inductance L_m should be negligible to the primary system with low frequency, but has a high p.u. value to the secondary high frequency system. Due to the big difference of power rating and fundamental frequency of the two systems, an appropriate value of L_m is not difficult to find. The coupling inductor is designed by assuming the low frequency (50Hz) component as a DC offset. As shown in Figure 6.3(b), the secondary voltage V_2 and current i_2 are replicated to the primary side, but only the primary current i_1 is reflected to the secondary because of the negligible voltage $V_1 \approx 0$ across L_m.



(a) Single phase equivalent circuit of the proposed *inverter cumulation* system.



(b) Decoupled equivalent primary and secondary circuit of the coupling inductor.

Figure 6.3: Coupling indutor design

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The primary side of the coupling inductor is in series with the system output terminal, therefore the primary current i_1 equals the full rated current of the IGBT inverter. Due to the fundamental frequency of the MOSFET inverter f_{12} is over 20 times of the IGBT inverter f_{11} (50Hz), i_1 could be assumed as a DC offset of the secondary winding of the coupling inductor.

In order to avoid the magnetic saturation effect of the core, the coupling inductor is designed with an air gap. The detailed parameters of the coupling inductor of the 5kW prototype test bench are shown in the Appendix B Table B.1.

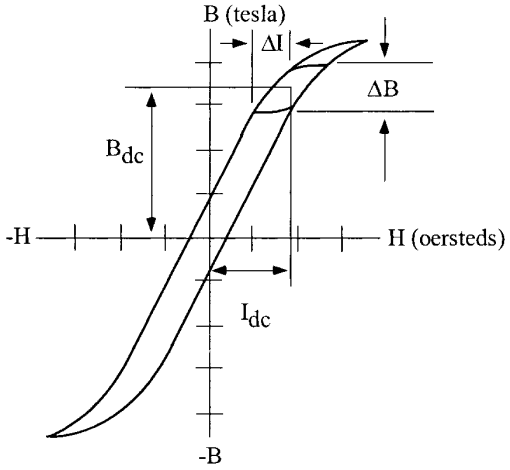


Figure 6.4: BH loop of the coupling inductopr.

The BH loop of the coupling inductor is shown in Figure 6.4. It has one major and one minor loop. The bigger hysteresis loop is produced by the IGBT inverter's low frequency 50Hz sinusoidal current. On the other hand, the MOSFET inverter 1kHz current drives the minor hysteresis loop. The coupling inductor design has to consider the worst saturation case where both major and minor loops reach their maximum value. In other words, the core of the coupling inductor should not be saturated at the worst case.

The first task of the coupling inductor design is choosing the magnetic material and the shape of the core. At the very beginning, the system schematic is designed as in Figure 4.10. The coupling inductors are connected directly to the output terminals of the two inverters. As there are many high frequency switching components, the coupling inductors are originally designed for the high frequency working condition. The main issue of the high frequency magnetic component design is loss minimization. There are two main groups of losses: iron loss and copper loss. The iron loss or the core loss which is caused by the hysteresis and eddy current can be minimized by using the so called soft magnetic material e.g. Ferrite. The copper loss which is dominated by the skin and proximity effect in the high frequency range can be minimized by using the Litz wire. However, the ferrite materials have quite high resistivity but rather low saturation flux density, typically 0.3 T [3]. Litz wires reduce the AC resistance by constituting of many thin, individually insulated, twisted wire strands, but the DC resistance is increased because of the smaller conductor cross sectional area and the copper fill factor k_{Cu} of the Litz wire is below 0.4, due to the insulation and additional space between strands. Therefore, the designers have to compromise the advantages and shortcomings of each technology. As mentioned before, the design of the coupling inductors follows the high operation frequency criteria. The ferret material and Litz wires were chosen at the beginning of the design.

Thanks to the computer aided design software of the magnetic components manufacture (e.g. EPCOS), the tedious mathematically calculations are avoided. The software generates the parameters based on the requirements set by the designers. The software interface of the Ferrite

Magnet Design Tool (version 5.20 EPCOS) is shown in Figure 6.5. The inputs of the software

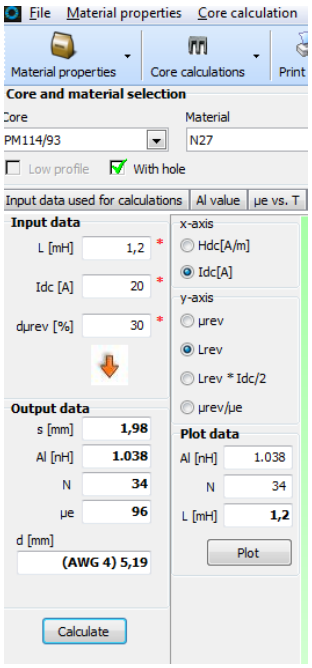


Figure 6.5: Software interface of the inductor design.

are the required the inductance and DC-bias current. After choosing the available core and material, the software will calculate the winding turns, air gap and the maximum wire diameters for you. The tricky point is: how much inductance should be set at the start point? For a coupling inductor, the bigger mutual inductance is better when there is no saturation! However, the core size and winding number will increase to an impractical value. Therefore, there is a limitation of the inductance value. That is determined by the largest core size and the maximum possible winding turns in it. The largest core size is dependent on the manufactures' product range. But when the core size is fixed, the space for the windings is also fixed. The maximum winding number is determined by the diameter of each inductor. The diameter of each wire is strongly dependent on the maximum allowable current density J. According to [60], J is normally in the range of 300-400 A/cm^2. The rated current of the IGBT inverter is 7.5A, therefore as a rule of thumb, it has a reasonable safe margin to set the two times higher current as 15A when designing the inductor. The minimum cross section of the winding wire is calculated by the following:

$$Acu_{min} = I_{dc}/J = \frac{15A}{400A/cm^2} = 3.75mm^2 \tag{6.1}$$

By considering the space in the core and the available litz wire on the market, the final design of the coupling inductor has the winding ratio of 1:1.5. The minimum cross section of the secondary winding is calculated as follows:

$$A'cu_{min} = I_{dc} * 1.5/J = \frac{15A * 1.5}{400A/cm^2} = 5.6mm^2 \tag{6.2}$$

Based on the result above, by checking the litz wire available on the market, the final winding parameters are listed in Table B.2 in the appendix. The MOSFET inverter side winding has

$N_1 = 33$ turns, and the IGBT inverter side winding has $N_2 = 50$ turns. The copper fill factor f_{cu} is calculated as follows:

$$k_{cu} = \frac{1}{2}\frac{Acu_1 * 2N_1 + Acu_2 * 2N_2}{A_n} = \frac{1}{2}\frac{6.28 * 2 * 33 + 3.77 * 2 * 50}{1070} \approx 0.37 \tag{6.3}$$

where $A_n = 1070mm^2$ is the window area of the bobbin of the chosen ferrite core. As illustrated before k_{cu} of the inductor using the litz wire should be smaller than 0.4, therefore the design should have no manufacturing problems. The pictures of the final designed are shown in Figure B.1 in the appendix. The inductors of the MOSFET inverter LC filters follows the same process. By setting the desired inductance and chosen core as the input of the MDT software, the number of winding turns and the air gap are calculated. The detailed parameters information are shown in the Table B.3 in the appendix.

Effects of the high frequency design of the inductor
As explained in Chapter 4, the original topology does not work. The coupling inductors have to be connected after the LC filter instead of the inverter output terminals. Therefore, the most part of the high frequency components are filtered out, thus the coupling inductors are not necessarily designed to withstand them. Does it cause problems, if the previous designed inductors are used?

Using the ferrite core, the inductance is difficult to reach a high value as the consequence of the lower saturation flux density. Furthermore, the cost of the ferrite material is higher. The advantage of the lower hysteresis losses of the ferrite is not obvious in the lower operating frequency. The other characteristic of the high frequency design is the use of the litz wire. As the cross sectional area of each strand gets smaller, the total DC resistance of the winding becomes much higher (more losses and heat) than normal wire. Moreover, the design is bulky and expensive as a consequence of the complicated structure of the litz wire.

However, the desired inductance is still assured. One advantage is that the higher DC resistance of the litz wire winding has a better damping effect of the LC resonance. Therefore, although the final topology does not require a high frequency coupling inductor, the previous manufactured inductors are still used in this case. The functionality of a high frequency design is guaranteed in the lower frequency working conditions. The higher resistance litz wire winding is not efficient from the losses point of view, but it exhibits a better stable operation of the whole system. The cost and manufacture complexity are high, but as the prototype, these issues are not as important as the verification of the functionality.

6.2.2 PHiL emulator hardware realization

The power stage of the emulator are two inverters. The IGBT inverter is a commercial product of the SEW which is ready to plug and play. On the other hand, the MOSFET inverter is a little bit complicated. There is no intelligent power module (IPM) available on the market. As explained before, the switching frequency of the MOSFET inverter is more than 50kHz which requires a high performance (power) driver. In order to avoid the potential failure, a high frequency two-channel-driver '2SC0650P' from 'CONCEPT' is used. An interface board for a three-phase-drive is designed and shown in Figure B.2.

The other topic of the test bench implementation is the analogue signals (voltage and current) sampling. A four-channel current sensor board was designed before at our institute as the peripheral board of the aforementioned real-time Pentium system. However, the previous designed voltage measurement board is only suitable for the DC-link sensing. Therefore, a new designed voltage measurement board shown in Figure B.2 has a 3-channel AC and 1-channel DC voltage sensing capability.

6.3 PHiL introduction and the requirements of the grid emulation

6.3.1 Concept of Power-Hardware-in-the-Loop (PHiL)

No software-based simulation is able to exactly reproduce the behaviour of a system under real operating conditions. This inherent limitation is the result of the finite amount of information which can be carried out by a model [61]. For this reason, performing simulations during the development phase of a complex system can generally not ensure that the end product will actually operate as expected. Furthermore, design faults may not be discovered until the very last stage of the on-the-field testing, which results in considerable costs to fix them.

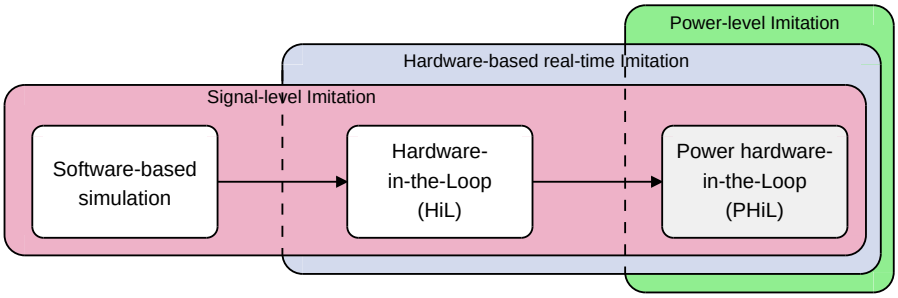


Figure 6.6: Imitation technologies of the real-world system.

The use of real-time emulated environments to assess the correct function and reliability of hardware components is being increasingly recognized as an effective means of overcoming these drawbacks. This innovative method, commonly referred to as Hardware-in-the-Loop (HiL) simulation, involves the technical equipment under test as well as sensors and actuators interacting with a real-time computer system [8]. Usually, the output quantities delivered by the equipment under test are captured by the sensors and processed by the real-time system according to a mathematical model representing the emulated environment. Consequently, control signals are generated for the actuators to behave like the emulated environment, providing the device under test with the corresponding input quantities. This increases the realism of the tests and hence, the significance of the obtained results. In contrast to early HiL schemes involving almost exclusively signal processing systems, modern HiL emulation also features energy transfers. This approach, known as *Power Hardware-in-the-Loop (PHiL)*, involves real energy fluxes in the testing process [62–64]. This characteristic inherent in PHiL systems obviates the need for a specific energy model. This also solves the problem of model inaccuracy since real energy will behave according to its physical properties given by nature.

For these reasons, PHiL constitutes an efficient means of precisely reproducing the behaviour of energy conversion systems, providing access to their physical features and, thus reducing the risk of simulation inaccuracies at same time.

PHiL emulators include a power amplifier (switch mode, generator or linear amplifier) between the real-time system (RTS) and the EUT [63]. Switch mode amplifiers (power electronics converters) are commonly preferred due to their lower cost, higher flexibility, ease of manufacture and despite the fact that the voltage levels at their output terminals is limited to a few discrete values. In consequence, the signal to be amplified has to be approximated by a series of pulses, generally by means of a pulse-width modulator. Although the mean output voltage over one carrier period is fairly equal to the one expected, the modulation produces a significant number of additional frequencies in the spectrum of the output waveform [65]. As a result, the carrier frequency – and hence, the switching frequency of the power electronic components inside the emulator – has to be chosen high enough so that harmonics originating from the modulation do not influence the tested device significantly. Owing to the physical constraints limiting the switching frequency of power electronic devices, this requirement might be difficult to fulfill if the device under test has a large bandwidth.

6.3.2 The technical standards of grid emulation

As the aforementioned power electronics system aims at building up the grid emulator, the performance of the PHiL system should conform to the requirements of the technical standards. The key evaluation criteria of the power grid is the power quality. However, the power quality is a very general concept which is difficult to directly measure and evaluate. By specifying parameters, patterns and limitations, several international and national technical standards play important roles in evaluating the grid quality, and on the test procedures for grid connected devices. The following standards are closely related to the grid emulator system [66]:

- EN 50160 voltage characteristics of the public distribution system
- IEEE 1547 interconnection of distributed resources with electric power systems
- IEC 61000-4-x transient immunity test

Table 6.1: Requirements of power grid

Item	Requirements
Voltage variation	$\pm 1\% U_n$
Frequency variation	± 0.1 Hz
Harmonics distortion	$\mathrm{THD}_v < 2.5\%$

According to [66], all the necessary requirements can be specified to the two categories of phenomena concerning grid voltage: stable and transient state. Table 6.1 summarizes the main requirements of the grid steady state from the standards EN 50160 and IEEE 1547. The standard EN50160 gives the individual harmonic voltages at the supply terminals. It is shown in Table 6.2.

Table 6.2: Values of individual harmonic voltages based on the standard EN 50160

Order h	5	7	11	13	17	19	23	25
Relative voltage (%)	6	5	3.5	3	2	1.5	1.5	1.5

Table 6.3: Disturbances of the power grid

Events	Durations
Sags: 0.1-0.9 pu	instantaneous : 0.5-30 cycles
Interruptions: below 0.1 pu	momentary : 30cycles - 3sec
—	temporary: 3sec - 1min

The standards also define the pattern and parameters of the grid transient behaviours like voltage sags and short interruptions (Table 6.3). The fault ride through (FRT) test is very important for the distributed energy resource (DER) especially wind turbines. Therefore the grid emulator is surpassed to emulate the fault behaviours based on the standard requirements. Figure 6.7 shows the standard fault ride through curve of Germany, which is used as the reference signal for the grid emulator.

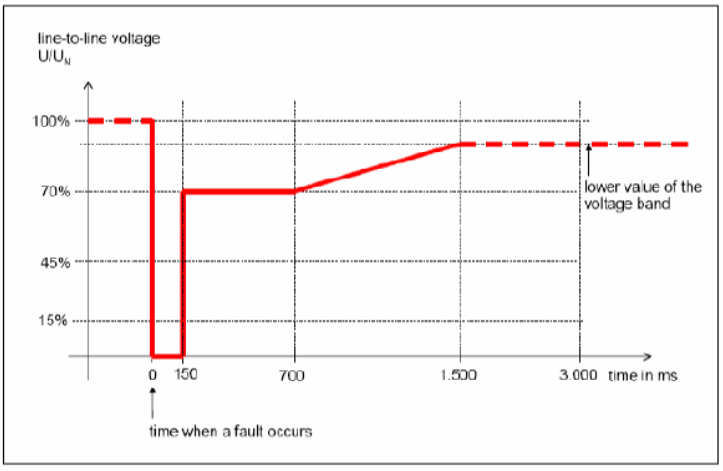


Figure 6.7: Imitation technologies of the real-world system.

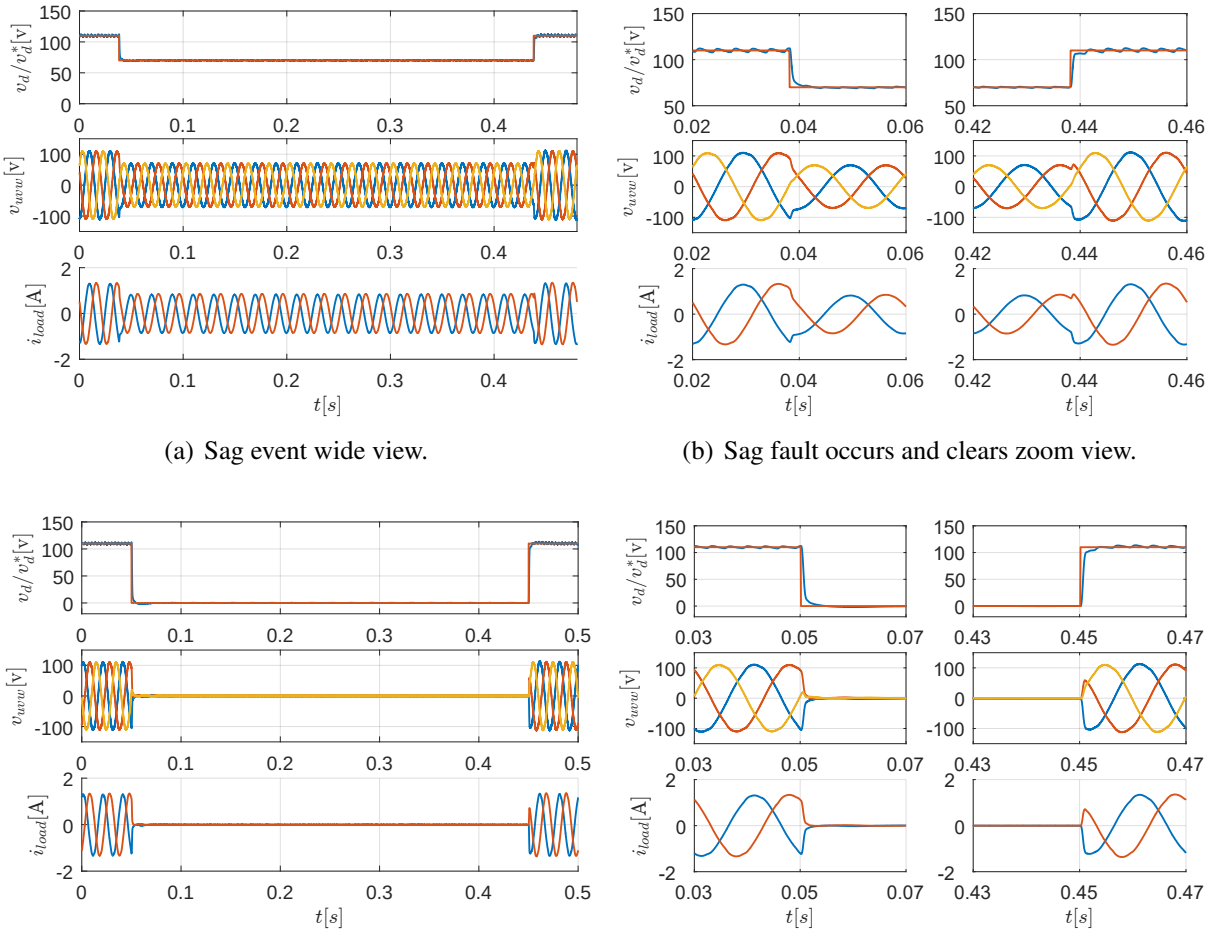
6.4 Experimental verification

In this section, the experimental results obtained from the prototype test-bench are presented in the sequence of aforementioned control algorithm designs in chapter 5. The proposed grid emulator is tested with two different types of EUT. An RL load bank represents the first type of linear user of the power grid, on the other hand a rectifier with resistor emulates the behaviour of the non-linear grid-tied equipment. Several typical behaviours including sag, trip,

frequency variation and low order harmonic programmability are emulated by the grid emulator with respective controller.

6.4.1 Experiments of the grid emulator with multi-loop PI controller

The GE is controlled to generate the 70% rate voltage ($U_r = 110V$) sag and 0% rate voltage trip fault for a time period of 0.4s. The emulation performances are shown in Figure 6.8(a) and 6.8(c). The wide view of the events are on the left hand side, and the zoom view when the event occurs and clears are shown on the right. In order to further investigate the emulated



(a) Sag event wide view.

(b) Sag fault occurs and clears zoom view.

(c) Trip event wide view.

(d) Trip fault occurs and clears zoom view.

Figure 6.8: Linear load sag and trip fault emulation with multi-loop PI-controller.

voltage signal quality, the total harmonic distortion (THD) is calculated by applying the Fast-Fourier Transformation (FFT) to the measured voltage curves. The calculation is based on the geometrical summation of the amplitude of the voltage harmonics V_h normalized to the amplitude of the fundamental voltage V_1.

$$\text{THD}_v = \frac{\sqrt{\sum_{h=2}^{f_s/f_1} \mid V_h \mid^2}}{V_1}\% \tag{6.4}$$

In this dissertation, only the harmonics up to the switching frequency for the THD calculation are considered. Figure 6.9 shows the FFT spectrum (up to 30^{th} harmonic)of the voltage signals. The THD is 2.38% which fulfills the requirements of the voltage standard (THD<2.5%).

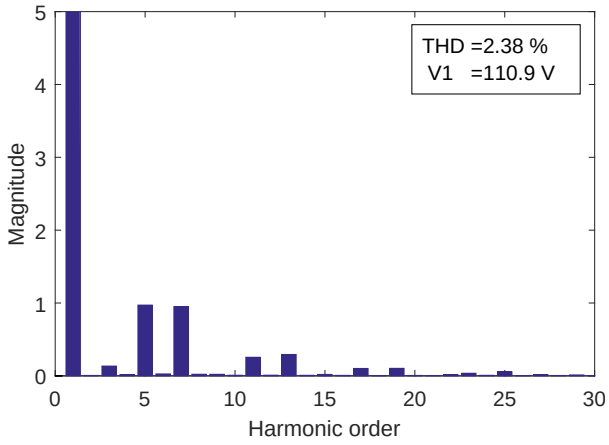


Figure 6.9: FFT spectrum of the voltage signal.

The grid emulator is also able to emulate the frequency variation fault. In order to exaggeratingly show its performance, the fundamental frequency of the voltage is changed from 50Hz to 100Hz and back to 50Hz after 100ms. As discussed in Section 6.3.2, the capability of the fault ride through (FRT) emulation is very important for the device under test such as wind turbine systems. By generating the voltage waves (as Figure 6.7) in a down-scaled time period 500ms, the proposed grid emulator demonstrates its capability of FRT emulation.

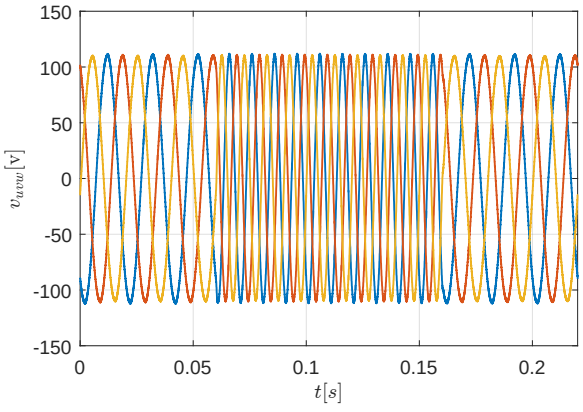


Figure 6.10: Frequency variation fault emulation.

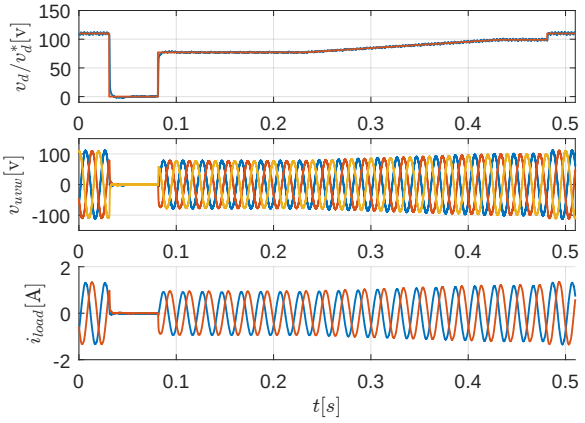
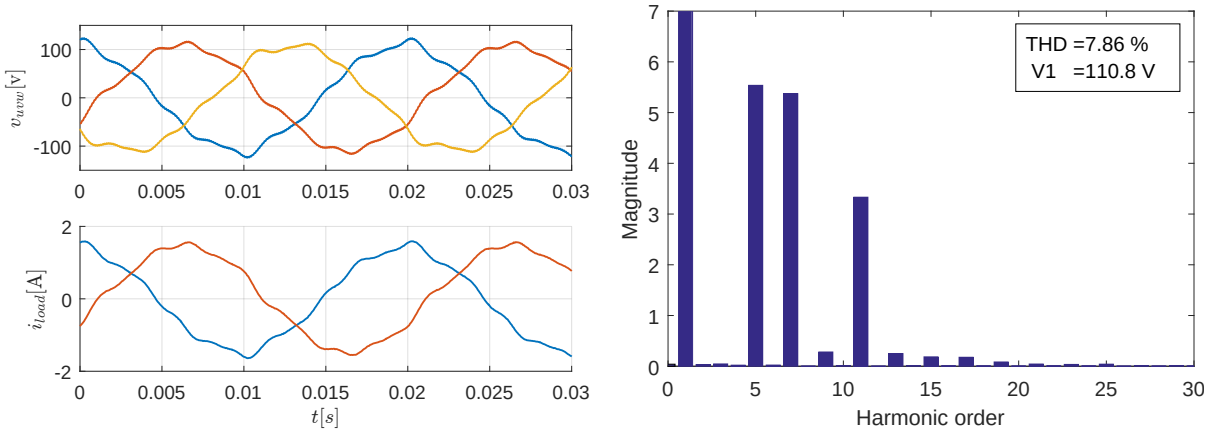


Figure 6.11: Fault ride through emulation.

The low-order harmonics programmability of the grid emulator is demonstrated by Figure 6.12(a). The voltage signal is generated with various harmonics based on the standard as described in Table 6.2. The proposed grid emulator injects three harmonic components (5, 7 and 11) according to the standard and Figure 6.12(b) shows the FFT spectrum of the voltage signals. It is clear to see that the harmonic components $V_5 \approx 5.6\%V_1$, $V_7 \approx 5.4\%V_1$ and $V_{11} \approx 3.3\%V_1$.



(a) Low order harmonics superposition.

(b) FFT spectrum and THD.

Figure 6.12: The low order harmonic programmability of the GE

6.4.2 Grid emulator with P+R-controller under non-linear load condition

As discussed in Section 5.2, compared to the synchronous-frame PI-controller, the P+R controller has several advantages. It is implemented in the stationary $\alpha\beta$-frame without any cross-coupling, therefore the complicated frame transformation and decoupling calculation are all eliminated. Moreover, the practical P+R controller can not only compensate both positive and negative sequence components, but also have the wider bandwidth. These superiorities of the P+R controller enables a better capability of harmonic rejection. As we know, the non-linear load injects various harmonic distortions, and these harmonic components deteriorate the performance of the conventional PI-controller. The P+R controller performs more effectively when the grid emulator supplies a non-linear device under test.

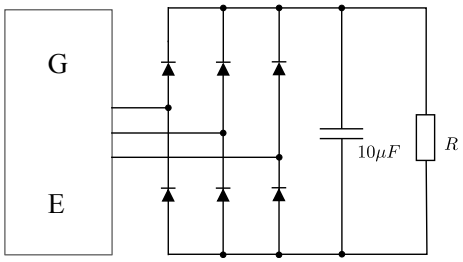
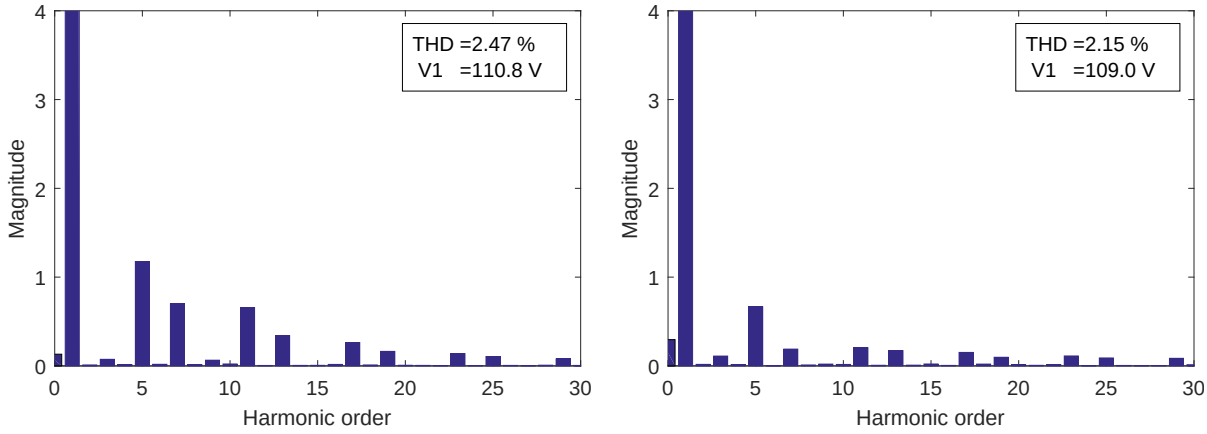


Figure 6.13: Non-linear device under test.

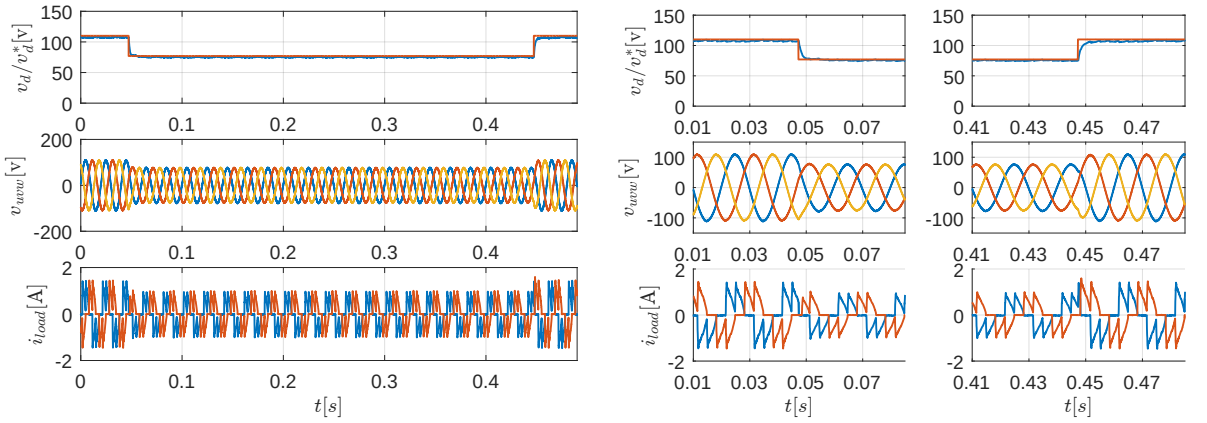
A non-linear load shown in Figure 6.13 is connected to the grid emulator. Both PI and P+R controller are used, and the generated voltage signals are evaluated by their FFT spectrum and THD. From Figure 6.14, it is obvious that the THD of the voltage signals generated by the PI-controller approaches the standard limitation. The P+R controller shows a very effective harmonics rejection ability. Compared to the PI controller, the low order harmonics (5, 7, 11 and 13) are dramatically reduced when using the P+R controller. The THD of the voltage signals is even better than the PI-controller with linear load. Therefore the P+R controller is adopted for the non-linear EUT, and the experimental results are shown in Figure 6.15.



(a) PI-controller.

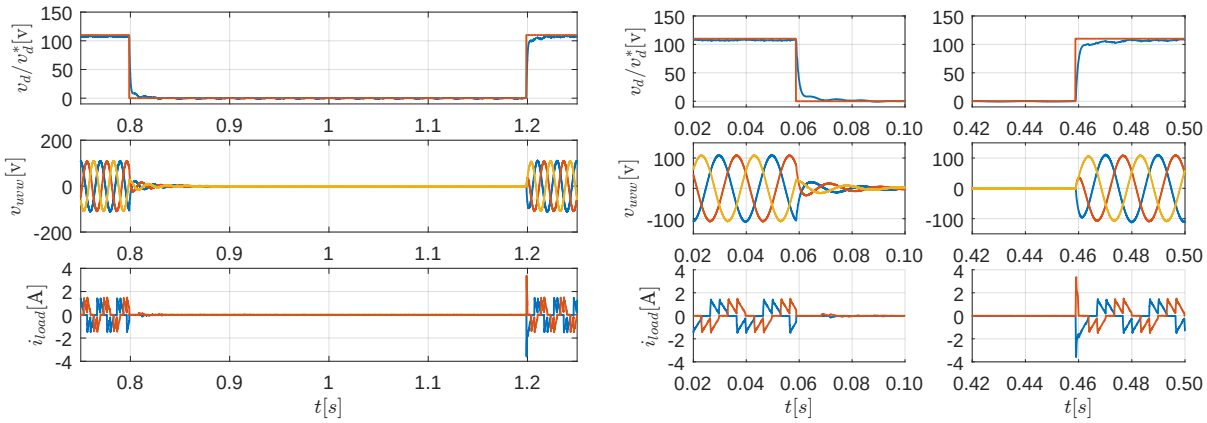
(b) P+R-controller

Figure 6.14: FFT spetrum and THD comparison between PI and P+R controller (Non-linar DUT connected).



(a) Sag event wide view.

(b) Sag event zoom view.



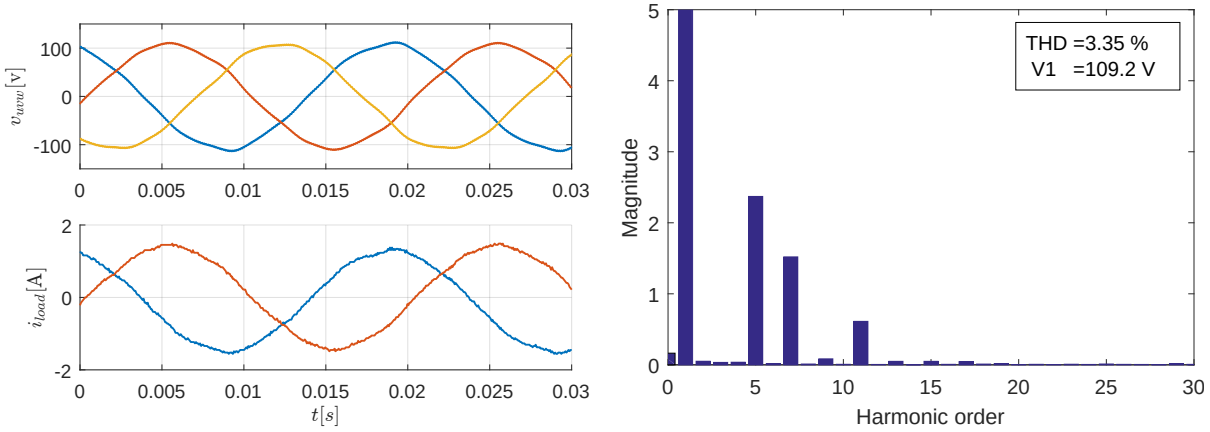
(c) Trip event wide view.

(d) Trip event zoom view.

Figure 6.15: Non-linear load sag and trip fault emulation with stationary fram P+R-controller.

The reference voltage signals of the P+R controller are v_α and v_β in the stationary frame. In Figure 6.15, the v_d and v_d^* are obtained by the transformation of corresponding quantities in the stationary frames. As we could see from Figure 6.15(d), the start current of the positive step response is much higher even with longer settling time compared to the situation with a linear load. The reason is that the DC-link capacitor of the rectifier causes a big inrush current at the positive voltage step. The capacitance of the non-linear load should be limited according to the ability of the power grid emulator. It is reasonable to set it smaller than the capacitance of the LC filter itself. The controller is tuned to have a slower transient process, and the inrush current is controlled within a tolerable range of the system. However, because of the slower response, the voltages oscillate with a small amplitude for several periods after the reference voltage reaches 0 (shown as Figure 6.15(d)).

Although the P+R controller has several advantages compared to the conventional PI-controller, several drawbacks are discussed in the following. The harmonic rejection causes problem for the harmonic programmability of the grid emulator. As shown in Figure 6.16,



(a) Low order harmonics superposition.

(b) FFT spectrum and THD.

Figure 6.16: The low order harmonic programmability of the GE with P+R controller

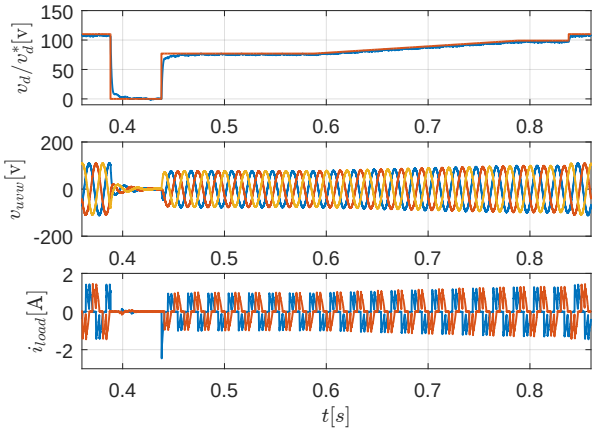
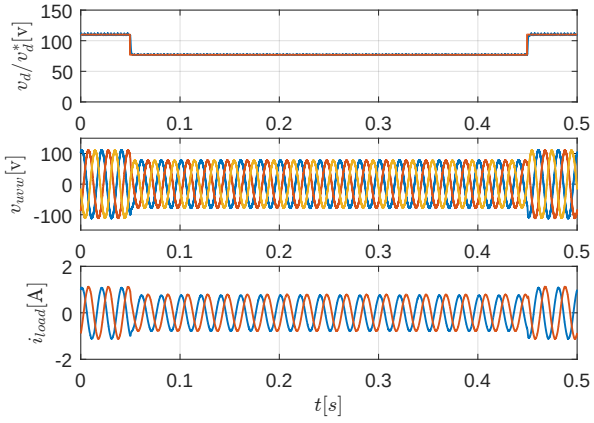


Figure 6.17: Fault ride through emulation under non-linear EUT.

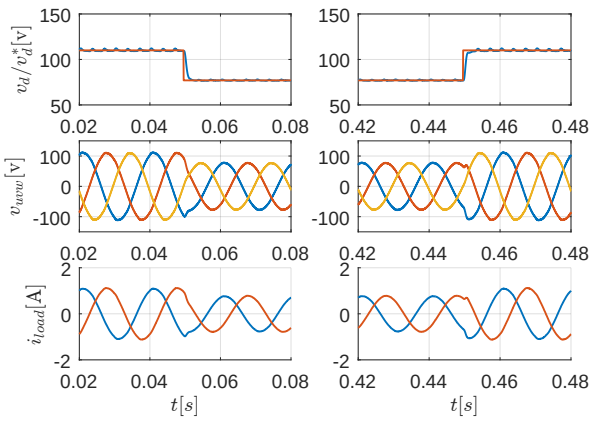
the P+R controller dramatically attenuates the superimposed 5, 7 and 11th order harmonics. Compared to the PI-controller (Figure 6.12(b)), the THD is reduced to 3.35% which is only half of the previous value. All the harmonic components are much lower than the injected value. Moreover, the P+R controller is designed for a specific frequency. The previous frequency variation from 50 to 100 Hz experiment is not suitable for this case. The fault ride through test under non-linear load is shown in Figure 6.17. As discussed before, the inrush current of the rectifier capacitor is quite high at the positive reference step and because of the longer settling time of the controller, the voltages have small amplitude oscillation when the reference signal is 0.

6.4.3 Experimental results of the linear quadratic controller

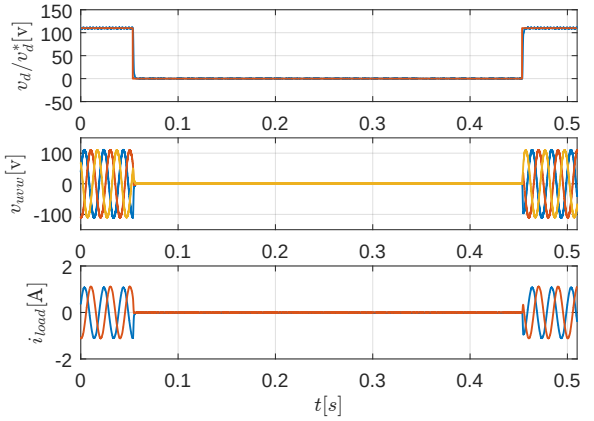
The linear quadratic regulator is one type of state space control. It provides not only the instinct closed-loop stability, but also the optimal transient response. The controller is implemented in the synchronous rotating frame, but the feedback matrix needs only the simplest gain elements. Compared to the previous PI and P+R controller, the LQR shows several superiorities including less implementation effort, instinct stability and optimal performance. In this section,



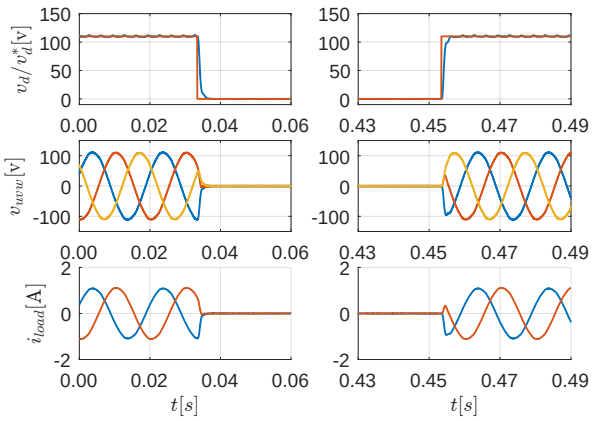
(a) Sag Event wide view.



(b) Sag fault occurs and clear zoom view.



(c) Trip Event wide view.



(d) Trip fault occurs and clear zoom view.

Figure 6.18: Linear load sag and trip fault emulation with LQR controller.

the previous emulation experiments are repeated on the grid emulator controlled by the LQR controller. A linear RL load is connected, the sag and trip faults emulations are shown in Figure 6.18. Compared with the PI controller, both the transient process or steady state of the LQR controller show comparable good performance. The frequency variation and FRT emulation of the LQR controller are shown in Figure 6.19 and 6.20.

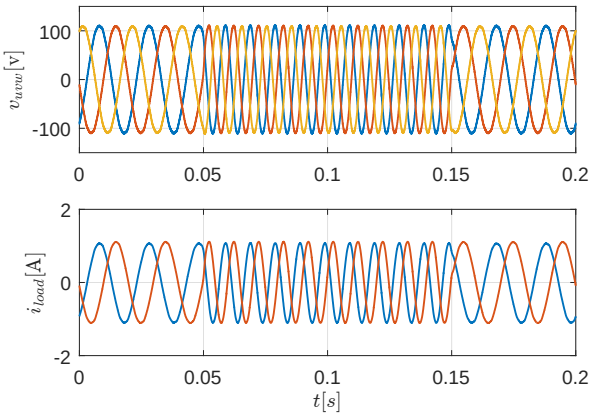


Figure 6.19: Frequency variation fault emulation with LQR controller.

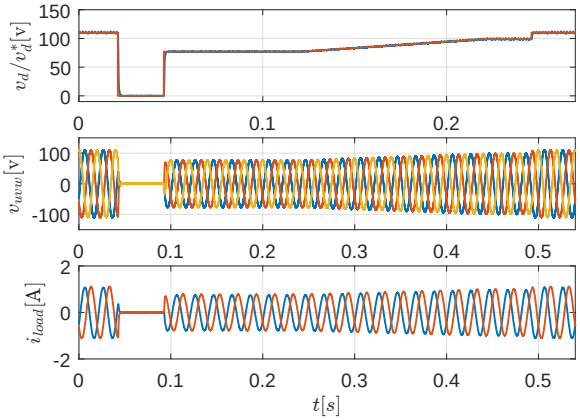


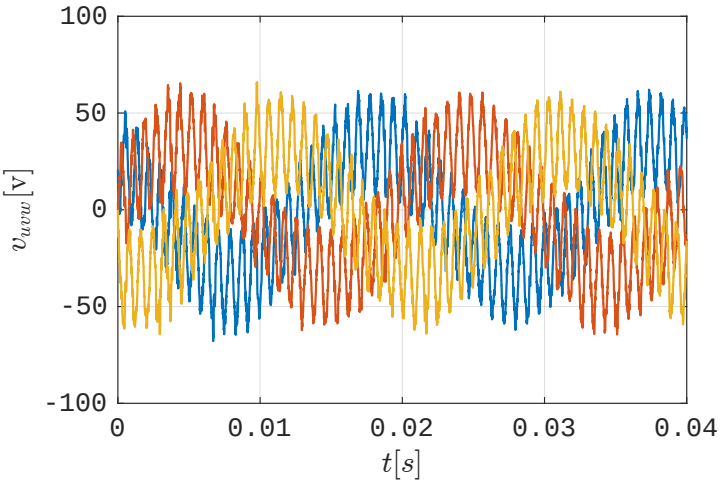
Figure 6.20: Fault ride through emulation with LQR controller.

The experimental results verify the previous discussion. The LQR controller has a systematic optimization process, and it performs as good as the multi-loop PI controller but with much less implementation effort. However it operates in synchronous rotating frame, and frequency sensitivity is still a matter of concern.

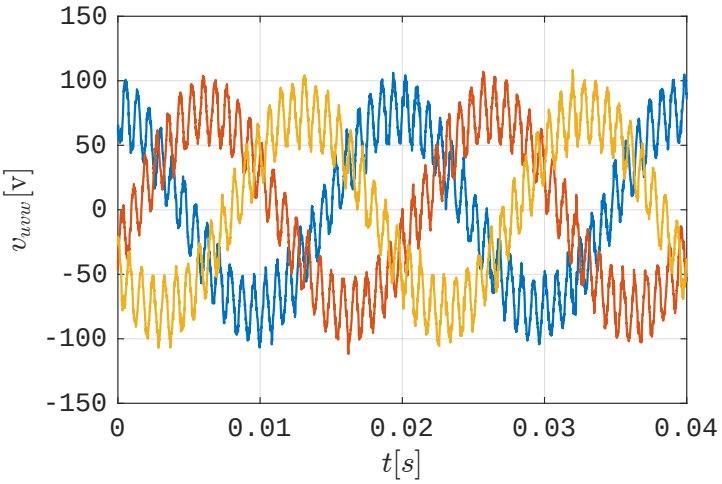
6.4.4 High frequency harmonics injection capability

The IGBT inverter is controlled to emulate the lower harmonics in the power grid. However, as discussed in the previous chapter, the most challenging task of the grid emulator is the high frequency harmonics superimposition. The 13^{th} and higher order harmonic components, which require a much higher switching frequency, are emulated by the FPGA-regulated MOSFET inverter. In order to demonstrate the high-frequency signal superposition performance of the proposed system, the MOSFET inverter produces a 25^{th} harmonic with an exaggerated phase amplitude of 25V. Figure 6.21 shows the three-phase voltages (35V, 70V and 110V) of the RL-load with MOSFET high-frequency injection. The start and stop transient of this high frequency injection can be seen in Figure 6.22(a) and 6.22(b). Moreover, the high frequency harmonics are also capable of being superimposed on all typical fundamental faults (sag, trip and FRT), which are shown in Figure 6.23.

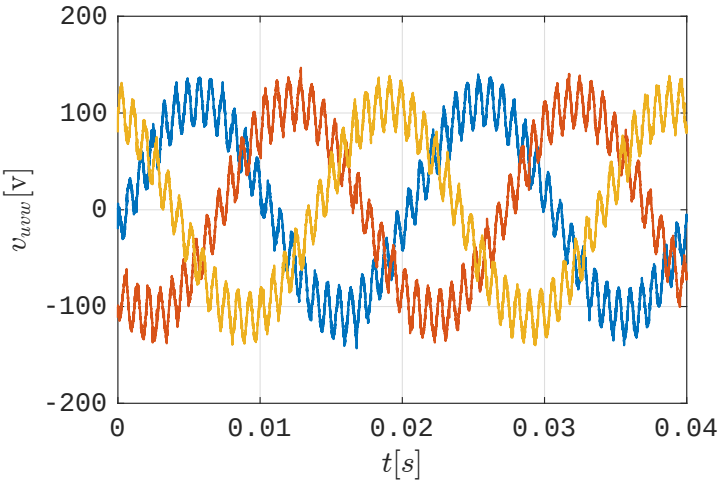
Based on the grid standard, the values of high order harmonics (above 23rd) are relatively small (1.5%). In this case, it seems hard to justify the size of 50V MOSFET inverter. However, the grid emulator is supposed to emulate not only the normal operation but also the special situation for particular scenario. As we know, large amounts of frequency converter drive systems (e.g. AC-DC-AC), non-linear equipment and switch-mode power supply have been widely connected as customers of the power grid. All of these applications cause the high order har-



(a) 35V with HF harmonic.



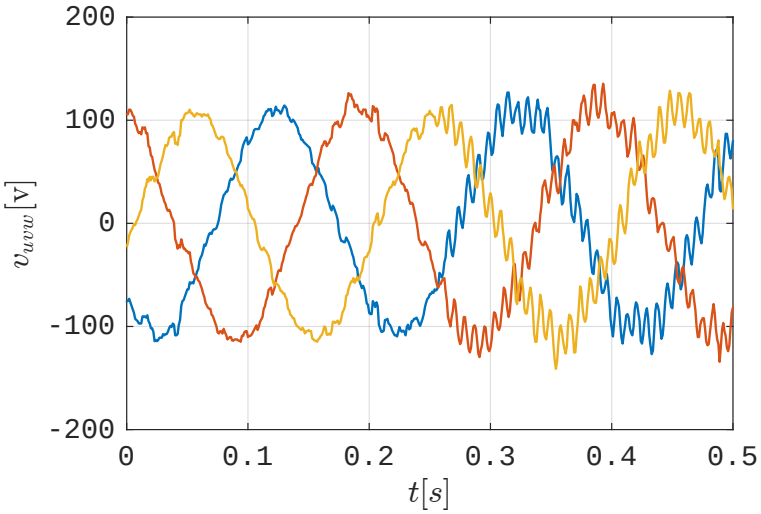
(b) 70V with HF harmonic.



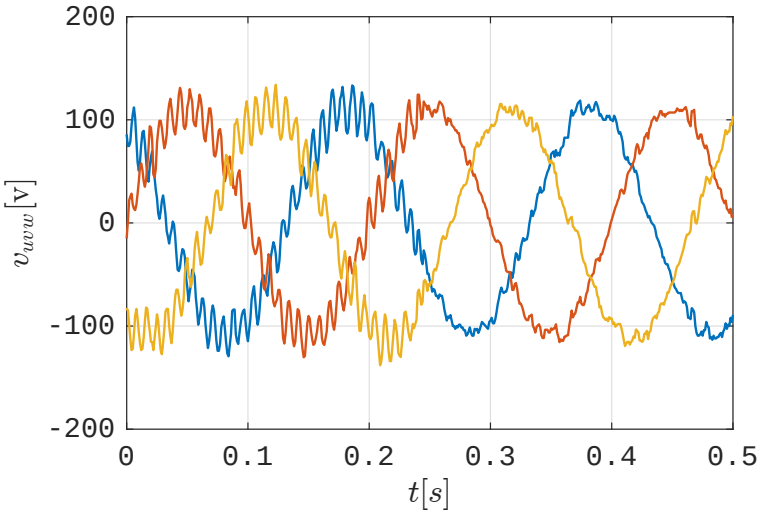
(c) 110V with HF harmonic.

Figure 6.21: HF harmonic injection with different amplitude of fundamental voltages.

monics which affect power quality of grid. Moreover, as the development of micro-grid and the



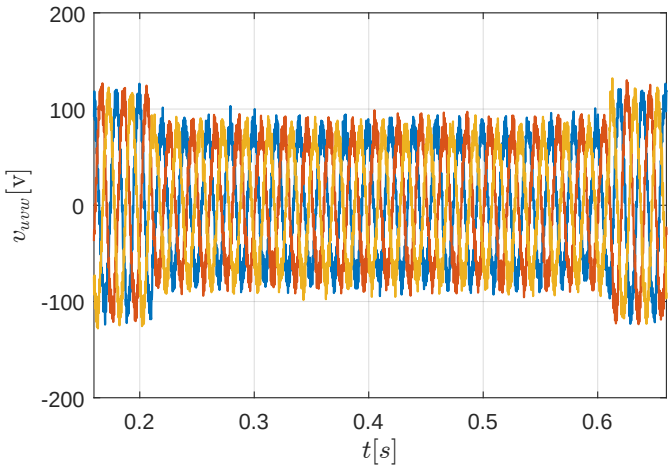
(a) HF harmonic injection start.



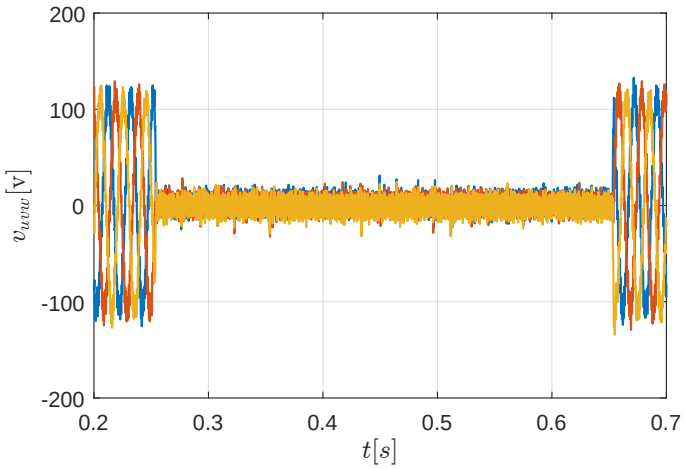
(b) HF harmonic injection stop.

Figure 6.22: HF harmonic injection start and stop transients.

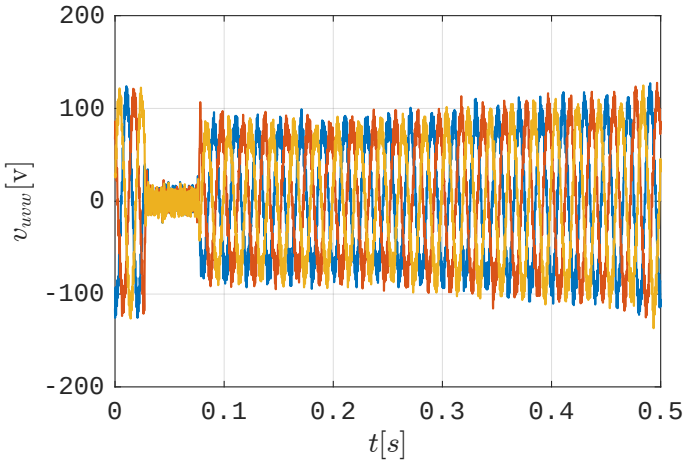
distributed-energy-resources (DER), more and more grid-tied inverters are used. They generate harmonic components around their switching frequency. In case of series-resonant or parallel-resonant of point of common coupling (PCC), these harmonic components will be amplified to ten times of their original value. By taking these special faults emulation into account, the MOSFET inverter with relative higher power rating has a reasonable necessity.



(a) Sag emulation with HF harmonic.



(b) Trip emulation with HF harmonic.



(c) FRT emulation with HF harmonic.

Figure 6.23: Fundamental voltage fault emulation with HF harmonic injection.

6.5 Discussion and further research focus

A downscaled PHiL grid emulator has been realized and tested. The ability of the 'inverter cumulation' concept to handle high power while simultaneously providing highly dynamic responses is validated experimentally. In addition, the encouraging results offer good prospects regarding the production of PHiL grid emulators economically affordable for small and medium enterprises.

6.5.1 Limitations and modifications

However, the proposed grid emulator based on the current topology has several limitations. In the following discussion, the technical reasons of these limitations and possible further improvements are presented item by item. The system has a limited current rating. The 'inverter cumulation' is based on the magnetic coupling components. As we know, all the magnetic material will be saturated when the current is bigger than a certain threshold. A larger inductance and higher saturation threshold are two incompatible characteristics of the inductor design, therefore a trade-off between them must be tolerant during the system design. The DC-link charging of the IGBT and MOSFET inverters are done by the simple diode-rectifier, thus the power flow is non-reversible. The proposed grid emulator is capable of emulating only as a power source instead of a sink. However, the power sink emulation is important to the EUT like grid-connected distributed generation sources (DGS). A possible modification is to replace the diode-rectifier by an active front end (AFE). By means of its back to back topology, the modified grid emulator will be able to work as both power source and sink. Unbalanced voltage faults with zero-sequence components (e.g. single phase fault) can not be emulated by the current system. The proposed topology is a 3-phase 3-wire system. Three phases are not independent with each other, and the system is capable of generating only positive and negative sequence voltages. However the most important single phase short-circuit fault contains positive, negative and zero sequence components which is impossible to emulate by the current system topology. By separating the dc-link and getting its middle point, the system can be modified as a 3-phase 4-wire system which has the ability of single phase fault emulating.

6.5.2 New research focuses of the grid emulator

The proposed grid emulator is able to reproduce the steady state and transient process of grid voltage waveform. Although this is the most important expected capability, it is not the full story of grid emulation. Several challenging research topics have been also focused on by peers worldwide during the development of the proposed project. Therefore, in order to have an overview of the new research trends and possible further improvements of the proposed grid emulator, this subsection presents the three newest aspects – the grid virtual inertia emulation, grid short circuit emulation and DC injection control.

6.5.2.1 Virtual inertia emulation

The power grid is composed of a lot of conventional synchronous generators which have inherent features beneficial to system stability. One big advantage is that the generator shaft inertia

increases the system constant, thus a more stable power-frequency can be achieved. This good characteristic is especially important for a weak grid situation. Aforementioned switching mode inverter based grid emulator has totally different dynamic response behavior, because it has no inertia. The previous experiments are carried out under an assumption – the grid emulator performs as an ideal voltage source. When the load is changing, it supplies the sufficient power with a stiff frequency and a voltage transient. In other words, it is a stiff frequency weak voltage grid emulator. In this situation, as there is no power and frequency droop control, therefore there is no need to have inertia emulation. However, when the grid emulator is supposed to reproduce weak frequency grid behavior, a droop controller with virtual inertia becomes necessary. In the following, a method based on the publication [67] in 2015 is presented and served as a possible further improvement of the proposed grid emulator.

The grid voltage forming controller stays the same as the previously presented multi-loop PI controller. The key of this task is an additional power regulated frequency controller which is determined by the famous virtual swing function shown below.

$$M\frac{d\omega^*}{dt} = P_0 - P - D(\omega^* - \omega_0) \tag{6.5}$$

By solving this equation in the Laplace domain, one can get the expression of the ω^* controller as:

$$\omega^* = \omega_0 - \frac{P - P_0}{Ms + D} \tag{6.6}$$

M is the desired virtual inertia of the emulated weak grid. P_0 is the scheduled output power in the original steady state, and P is the actual output power of the grid emulator when a load step occurs. ω_0 is the nominal frequency which is 50Hz, and ω^* is the new reference frequency of the grid emulator. D is the damping power coefficient which is determined by the primary frequency regulation characteristic expressed by the equation below.

$$\Delta\omega = \omega^* - \omega_0 = -\frac{P - P_0}{D} = -\frac{\Delta P}{D} \tag{6.7}$$

It establishes a droop relationship between the frequency and output power of the grid emulator. Moreover, for a practical implementation, the amplitude of the frequency deviation can be limited by saturation limits shown in Figure 6.24.

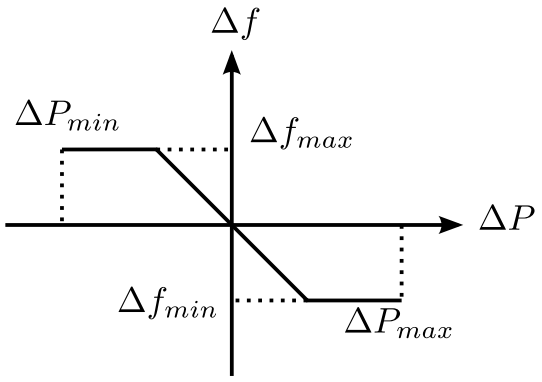


Figure 6.24: Primary frquency regulation charateristic.

As we know, the secondary frequency control can restore the system frequency to nominal value. It is also good to have this good characteristic on the grid emulator. According to [67], this could be realized by a slow-response integral $\frac{K_s}{s}$ term to balance the new scheduled power to the actual power:

$$P_0 = P^* + \Delta P \tag{6.8}$$

where P^* is the previous scheduled output power. Equations 6.6 and 6.8 are schematically illustrated in the overall control scheme in Figure 6.25.

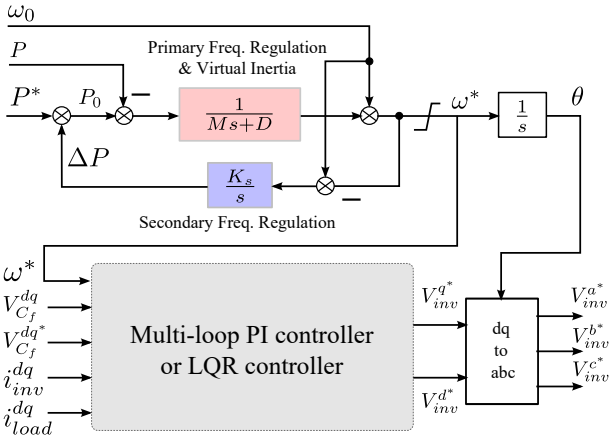


Figure 6.25: Frequency regulation and virtual inertia control of the grid emulator.

6.5.2.2 Short circuit fault emulation

The proposed grid emulator can generate voltage trip faults for the EUT. During this event, the voltage source inverter is controlled to generate a zero voltage vector for the EUT. However, in this case, no current can flow in the circuit, and the EUT can only work in a stop mode. For the short circuit emulation, it not only requires a 0 voltage, but also has to create the actual fault current. The previous topology is not capable of emulating this behavior, and it is really a challenge and new focus. In 2015, according to [68], a short circuit emulation method which uses a shunt connected voltage source inverter was published. The basic idea is explained in the following.

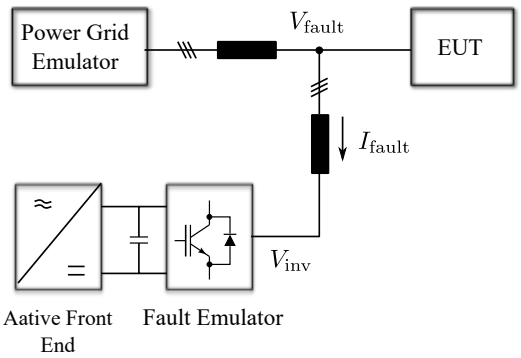


Figure 6.26: Shunt connected short circuit fault emulator.

The basic principle of the short circuit emulation is a ground impedance control of the fault position. The shunt voltage source inverter is controlled to generate the fault voltage as if the shunt ground impedance were connected [68]. By adopting this idea, a modification of the proposed grid emulator is shown in Figure 6.26. This fault emulator is able to generate single-line-to-ground, double-line-to-ground, line-to-line and three-phase fault. The single-line-to-ground fault emulation is presented here, and the others have the same principle but with different current and impedance conditions. The constraint equation is:

$$V^*_{\text{fault}} = Z_{\text{fault}} \cdot I_{\text{fault}} \tag{6.9}$$

where I_{fault} is the sensed phase to ground fault current, Z_{fault} is the emulated grounding impedance, and the V^*_{fault} is the reference voltage of the fault emulator. The block diagram of the controller is shown in flowing.

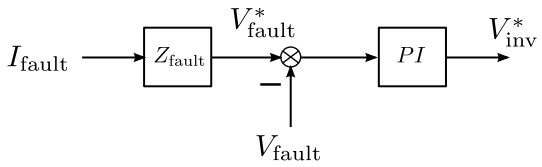


Figure 6.27: Single line to ground fault emulation controller block diagram [68].

For more information on the other fault emulations, in [68] all scenarios are documented. The functionality of this method is approved by simulations and experiments under the working condition with real power grid. Therefore, it is reasonable to believe it will work with the proposed grid emulator.

6.5.2.3 DC-current suppression strategy

The proposed grid emulator produces the ac power from a dc source, and due to the unbalanced modulation, non ideal current sensing etc. it injects excessive amount of DC current into the EUT which is very troublesome. This DC current can distort the magnetization of the transformer, and lead to saturation of all the magnetic components in the EUT. Moreover, it also causes the corrosion of the underground equipment and malfunction of protective equipment [69]. Therefore, the suppression of the DC current is very critical for the functionality of the grid emulator with DC-sensitive EUT.

The simplest elimination method is by connecting a line frequency transformer which is designed to have an ability of withstanding a certain level DC current. However, the line frequency transformer is very bulky, expensive and inefficient from the energy point of view. Another method blocks the DC current by using a capacitor series connected between the grid emulator and EUT, but it not only requires extra cost, but also produces unnecessary losses. In [70], an algorithm which replaces the real capacitor by a virtual capacitor in the controller is presented, but the performance of closed-loop controller of the grid emulator is strongly affected [71]. After investigating several recent publications, a possible modification of the proposed grid emulator based on the method in [72] is presented in Figure 6.28.

Two differential amplifiers with low offset and noise but high CMRR (common-mode refection ratio) are used to sample the line-to-line voltage at the output terminals of the inverter.

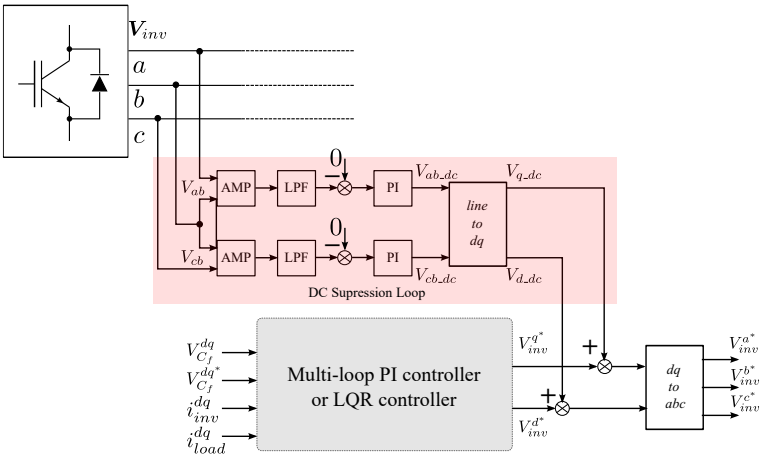


Figure 6.28: DC injection control scheme diagram [68].

Then the DC-components are extracted by the low pass filter, and are regulated to its reference value '0' by the PI controller. After frame transformation, these DC suppression voltage references are superimposed on the control signals of the emulator voltage controller. In [72], this method is used for a grid-connected voltage source inverter with an L filter, and its functionality is approved both by simulation and experimental results. For the proposed grid emulator based on a voltage source inverter with LC output filter, this method is also believed to be a good strategy after a minor modification.

CHAPTER 7

Summary and future work

7.1 Summary

In this dissertation, a new high power rating and high dynamic response power electronics system based on the concept of *inverter cumulation* has been investigated. This high performance system extends the physical limitation of current topologies based on single type market-available power electronics devices. Thus, it serves as an effective means of PHiL systems which have higher requirements for its power convention system. As mentioned in Chapter 1, the core idea of the *inverter cumulation* is that by magnetically coupling different and identical inverters, the final cumulation system accumulates the power and dynamics characteristics from various subunits. The two magnetically coupling methods (magnetic-parallel coupling of identical IGBT inverters and magnetic-series coupling of IGBT and MOSFET inverters) have demonstrated their superior characteristics as the power convention units of two different PHiLs (virtual machine and grid emulator).

The first attempt at the PHiL virtual machine showed success of the parallel coupling inverter modulated by the 'sequential switching' concept. The cumulation concept increases the system overall modulation frequency while keeping the switching frequency of each device within its physical limitation. The virtual machine is controlled to generate the calculated back-emf voltage according to a reverse machine model. From the EUT point of view, virtual machine behaves like a real machine. The two key issues of the virtual machine are: coupling inductor for the sequential switching of the freewheeling diodes and the reverse model of the induction motor.

This work mainly focuses on the second cumulation topology. One high power IGBT inverter is magnetically coupled with another high switching MOSFET inverter. The two inverters operate with totally different characteristics (power, DC-link voltage, switching frequency, fundamental voltage and frequency). Because of the different power rating of the two inverters, it is very critical to ensure the safe operating condition of the smaller power rating sides. The original topology neglected the effect of the high amplitude switching components from the IGBT

inverter, which caused a fatal problem for the MOSFET inverter as a result of its rectifying and recharging working mode. After the first unsuccessful attempt, the author realized that the switching components at the output terminal of the IGBT inverter have to be filtered out. The next key issue of the project is the low pass output filter design and its control. As mentioned before, there are mainly three types of filters: L, LC and LCL filter. Due to the limited filtering effect of the first order L-filter, LC and LCL filters are the two reasonable choices of most industrial applications.

The output of the LC filter is the capacitor voltage, on the other side, the inductor current serves as the output variable of the LCL filter. Choosing a type of filter is determined by the desired output signal. The proposed inverter system is supposed to emulate the behavior of the power grid, therefore the voltage signals generation is the main task. In this case, it performs like a programmable voltage source, thus an LC filter is the right choice. On the other hand, LCL filter is suitable for the system working as a current source.

A later chapter explains the output voltage control of the inverter with an output LC filter. Three different strategies including the conventional synchronous-frame PI controller, recent popular stationary-frame resonant controller and the state space feedback controller are investigated and implemented. The prototype of the proposed *inverter cumulation* system was built. By emulating not only the normal operation, but also the typical fault of the power grid, it demonstrates its high performance as a PHiL grid emulator.

7.2 Outlook

One prospective future work is to investigate new cumulation topologies by going beyond the current coupling method and different inverter topologies. Recently, more and more researchers are focusing on the multilevel inverter in the medium voltage range. There are three main kinds

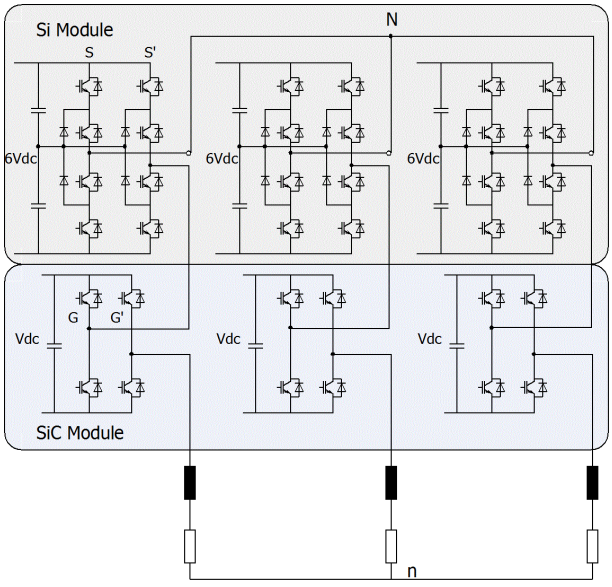


Figure 7.1: New *inverter cumulation* topology.

of multilevel topologies — neutral point clamped (NPC), flying capacitors (FCs) and cascaded

H-bridge (CHB). Among these converter topologies, CHB converters can easily reach higher voltage levels and larger power ratings by standard mature technology components because of its series connection structure of several single phase converters. Unlike the conventional CHB converters, cascading identical single phase inverters with equal dc-link voltage, the hybrid asymmetrical CHB converters combine various different topologies of inverters with unequal DC source voltages. By doing this, the converter can combine the advantages of different topologies, and achieve higher voltage levels with less circuit and control.

The proposed new cumulation topology investigates the possibility of the cascaded coupling of different inverters. Each phase of the system is composed of one Si-based 5-level NPC H-bridge (HV cell) and one SiC-based 3-level H-bridge (LV cell). A 15-level phase output voltage waveform will be synthesized by configuring the dc-bus voltages of the two cells in the ratio of 6:1. The recent fast developed SiC switches are considered as ideal candidates for fast switching applications. However due to the complexity of manufacturing, the cost of the SiC-based power devices is still high. The proposed hybrid topology replaces only the low voltage and fast switching cells by using SiC power switches, which increases the performance of the whole system with a reasonable price at same time. The project aims at investigating the realization of hybrid converter systems and implementation of their advanced control methodologies.

APPENDIX A

List of symbols and abbreviations

A.1 List of symbols

General remark:
The following convention was used for variables:

Scalars are italic letters:	x
Vectors are bold lower case letters:	$\boldsymbol{x}$
Matrices are bold upper case letters:	$\boldsymbol{X}$
References are marked with a star superscript:	x^*

Used symbols:
In the following the most important symbols are listed which are used within this work.

General symbols:

$\boldsymbol{x}$	State vector
$\boldsymbol{u}$	Input vector
$\boldsymbol{y}$	Output vector
$\boldsymbol{A}$	State matrix
$\boldsymbol{B}$	Input matrix
$\boldsymbol{C}$	Output matrix
$\boldsymbol{D}$	Feedthrough matrix
t	Time (continuous)
k	Time (discrete, current sample)
$\frac{\mathrm{d}}{\mathrm{d}t}$	Time derivation
T_s	Sampling time

General electrical variables:

a, b, c	Phases
α, β	Equivalent two-phase coordinates
j	$\sqrt{-1}$
v	Voltage
i	Current
R	Resistor
C	Capacitor
L	Inductor

symbols used in the chapter 3

U_{dc}	DC-link voltage
L_m	Main inductance of coupling inductor
L_σ	Leakage inductance of coupling inductor
$\boldsymbol{\phi}_m$	Main flux of coupling inductor
$\boldsymbol{\phi}_\sigma$	Leakage flux of coupling inductor
r_s	Normalized stator resistance
r_r	Normalized rotor resistance
l_s	Normalized stator inductance
l_r	Normalized rotor inductance
l_h	Normalized magnetizing inductance
k_s	Stator magnetic coupling factor l_h/l_s
k_r	Stator magnetic coupling factor l_h/l_r
σ	Total leakage coefficient $1 - k_s k_r$
$\boldsymbol{\psi}_r$	Normalized rotor flux linkage
$\boldsymbol{u}_s$	Normalized stator voltage
$\boldsymbol{u}_{\text{ir}}$	Normalized induced voltage
ω	Normalized angular velocity of the rotor
τ	Normalized time
τ_r	Normalized rotor time constant l_r/r_r
τ_m	Normalized mechanical time constant
T_L	Load torque
T_e	Electromagnetic torque

symbols used in the chapter 4 and 5

C_f	Filter capacitor
L_f	Filter inductor
V_{C_f}	Voltage of filter capacitor
i_{C_f}	Current of filter capacitor
i_{inv}	Inverter output current
i_{load}	load current
V_{inv}	Inverter output voltage
k_p	Proportional gain of PI controller
k_i	Integration gain of PI controller
ω	Fundamental angular frequency

ω_{res}	Resonant frequency
ω_n	Undamped natural frequency
ω_c	Cut-off or cross frequency
ξ	Damping ration
$\sigma\%$	Maximum overshoot
t_{set}	Setting time
φ_{PM}	Phase margin

A.2 List of abbreviations

AC	Alternating Current
AD	Analog to Digital (converter)
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
DA	Digital to Analog (converter)
DC	Direct Current
DSP	Digital Signal Processor
FPGA	Field Programmable Gate Array
FS	Finite-Set
HDL	Hardware Description Language
HiL	Hardware-in-the-Loop
IGBT	Insulated Gate Bipolar Transistor
LCD	Liquid Crystal Display
LQR	Linear-quadratic regulator
MOSFET	Metall-Oxid-Halbleiter-Feldeffekttransistor
PHiL	Power Hardware-in-the-Loop
PWM	Pulse Width Modulation
RAM	Random Access Memory
RMS	Root Mean Square
RTAI	Real-Time Application Interface
SI	International System of Units
SRF	Synchronous Rotating Frame
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply
VHDL	Very High Speed Integrated Circuit Hardware Description Language

APPENDIX B

Test bench data

B.1 Magnetic components design

B.1.1 Coupling inductor

Table B.1: Parameter of Coupling Inductor

Core	EPCOS PM114/93
Ferrite	N27
L_m (mH)	1.2
Air gap δ (mm)	2
I_{DC} (A)	20
I_{AC} (A)	5
I_{pk} (A)	20

B.1.2 litz wire parameter

Table B.2: Parameter of litz wire

	No.of strands	external diameter	cross section
IGBT inverter side	0.2mm * 120	3mm	$3.77mm^2$
MOSFET inverter side	0.2mm * 200	3.94mm	$6.28mm^2$

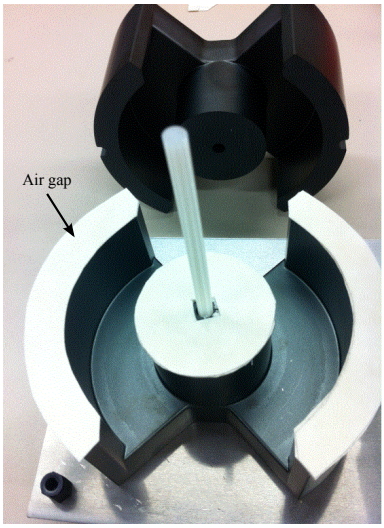
B.1.3 Inductor of LC filter

Table B.3: Parameter of LC filter inductors

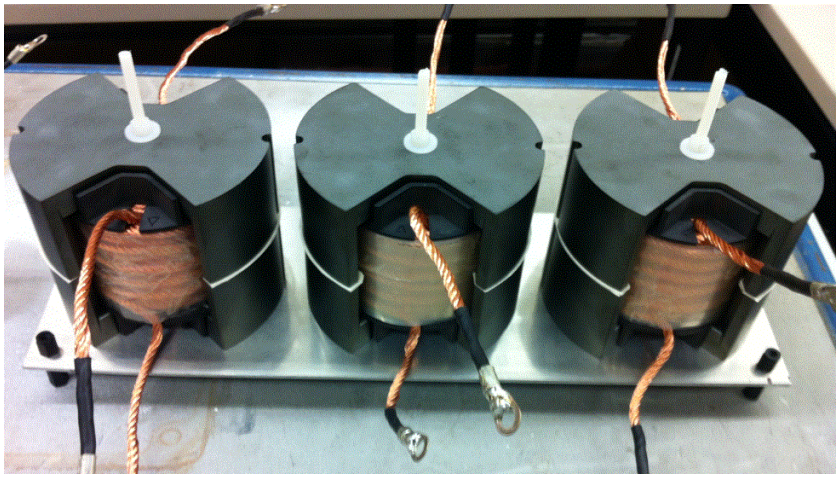
Filter inductor	Inductance	I_{dc}	Turns	Air gap	Core
MOSFET inverter	0.25mH	20A	20	1.2mm	EPCOS PM74/59

B.1.4 Picture of the coupling inductor

(a) Picture of the coupling inductor winding on the bobbin.



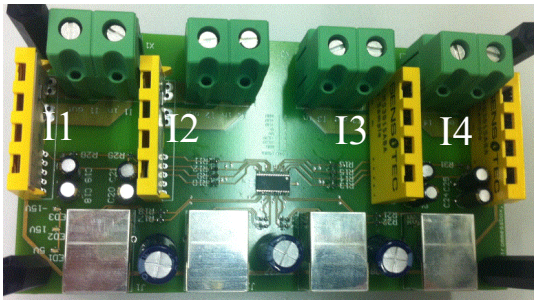
(b) Air gap precise adjustment by the insulated paper.



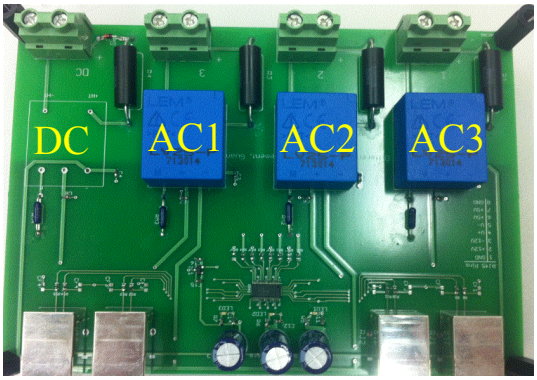
(c) Final three phase coupling inductor.

Figure B.1: Block diagrm of the current controller.

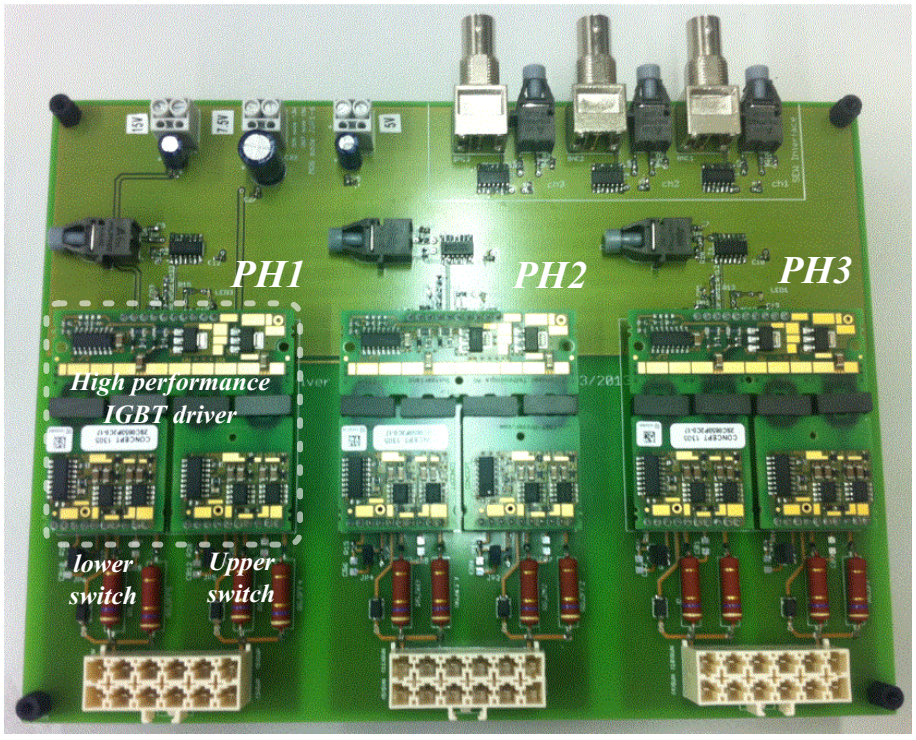
B.2 Picture of driver and measurement boards



(a) Four-channel AC current measurement board.



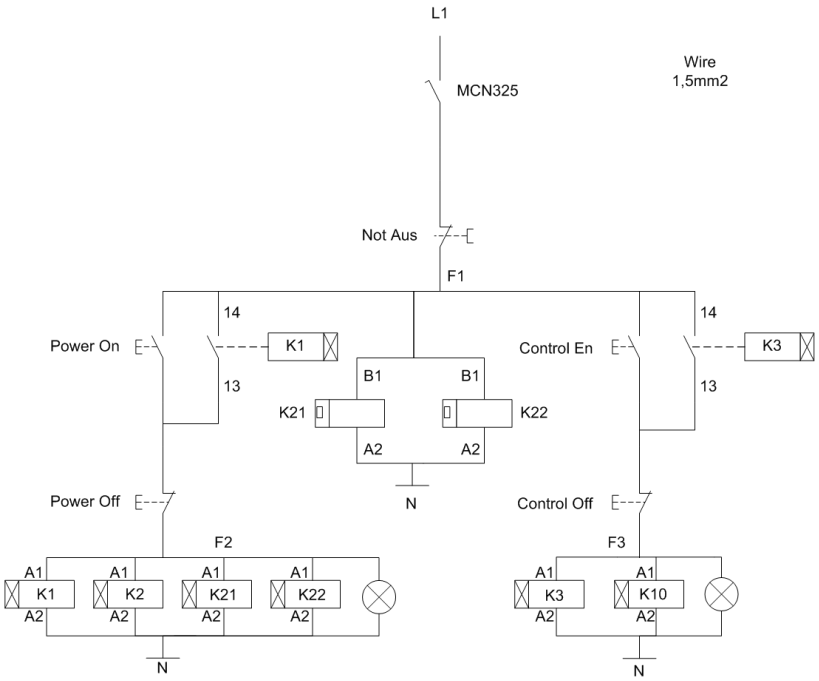
(b) Three-channel AC and one-channel DC voltage measurement board.



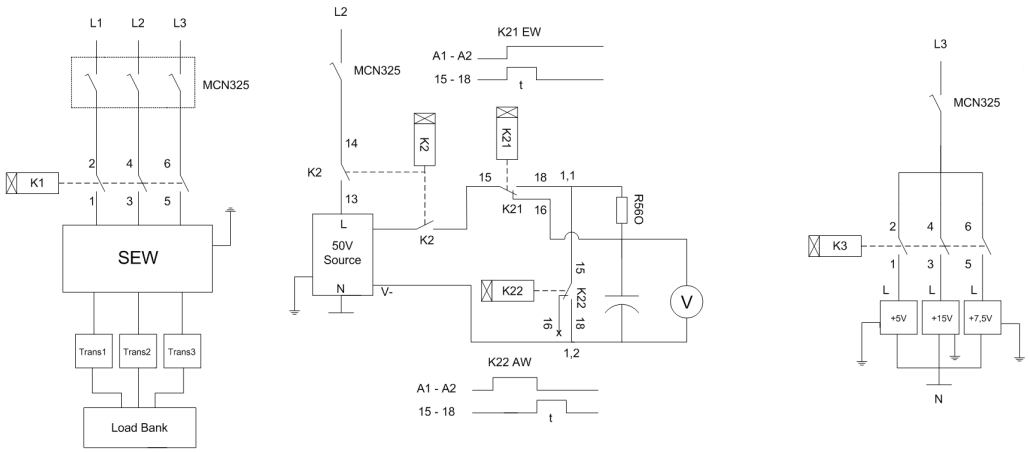
(c) Closed loop transfer function of the current loop

Figure B.2: Block diagrm of the current controller.

B.3 Main wiring diagram of switching test bench cabinet



(a) Four-channel AC current measurement board.



(b) Three-channel AC and one-channel DC voltage measurement board.

Figure B.3: Block diagrm of the current controller.

APPENDIX C

List of publications

C.1 Journal papers

- G. Si, J. Cordier and R. M. Kennel, "Extending the Power Capability With Dynamic Performance of a Power-Hardware-in-the-Loop Application — Power Grid Emulator Using Inverter Cumulation", *Industry Applications, IEEE Transactions on*, vol. 52, no. 4, pp. 3193-3202, July-Aug. 2016.
- G. Si, J. Cordier and R. M. Kennel, "Hardware-in-the-Loop Emulation of Electrical Drives Using Standard Voltage Source Inverters", *EPE Journal*, Vol. 24, No.4, pp. 28-37, 2014.

C.2 Conference papers

- G. Si and R. Kennel, " Switch Mode Converter Based High Performance Power-Hardware-in-the-Loop Grid Emulator", *2nd IEEE Southern Power Electronics Conference (SPEC 2016)*, Auckland, New Zealand, 2016.
- G. Si, Z. Shen, Z. Zhang and R. Kennel, "Investigation of the Limiting Factors of the Dead Time Minimization in a H-bridge IGBT Inverter", *2nd IEEE Southern Power Electronics Conference (SPEC 2016)*, Auckland, New Zealand, 2016.
- G. Si and R. Kennel, "Comparative study of PI controller and quadratic optimal regulator applied for a converter based PHiL grid emulator", *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, Hefei, 2016.
- G. Si, J. Cordier and R. Kennel, "Development of a power-hardware-in-the-loop application — Power grid emulator by using voltage source inverter cumulation", *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015.

- Z. Zhang, F. Wang, G. Si and R. Kennel, "FPGA Based Encoderless Predictive Control of Back-to-Back Power Converter PMSG Wind Turbine Systems with Extended Kalman Filter", *2nd IEEE Southern Power Electronics Conference (SPEC 2016)*, Auckland, New Zealand, 2016.

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