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Design, Modeling and Implementation of Distributed Architectures for Modular Battery Packs

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Abstract

This thesis addresses the design challenges associated with distributed Battery Management Systems (BMSs) by proposing modular electrical architectures and optimized control algorithms.

High power applications such as Electric Vehicles (EVs), Hybrid Electric Vehicles (HEVs), Electrical Energy Storages (EESs) for smart grids, etc., use battery packs made of series-connected Lithium-Ion (Li-Ion) cells due to their superior energy and power densities compared to other rechargeable battery chemistries. In spite of their significant advantages, Li-Ion cells are very sensitive with respect to their operating conditions. Operation outside their defined set of safe operating limits of voltage, current or temperature significantly reduces their lifetime and probably damage them, causing fire or explosion due to thermal runaway. Moreover, the usable capacity or energy output of a series-connected battery pack is affected by variation in charge levels of individual cells. This is caused by manufacturing inhomogeneities and varying temperature distribution along the battery pack. Cell balancing is typically performed to mitigate this issue by equalizing the State-of-Charge (SoC) of individual cells. Conventional cell balancing approaches are *passive*, where the excess energy from cells that are overcharged is dissipated as heat across a switched power resistor. In contrast to this, *active* cell balancing approaches transfer the excess charge from cells with higher SoC to cells with lower SoC, increasing both the energy-efficiency and lifetime of the battery pack. Therefore, in order to maintain safe operating conditions and to increase the usable capacity of a series-connected Li-Ion battery pack, a sophisticated BMS equipped with an energy-efficient active cell balancing architecture is favorable.

State-of-the-art BMS topologies are centralized, having a central master controller monitoring parameters of all individual cells and maintaining them within their safe operating limits. By contrast, decentralization of both hardware and software architectures of the BMS into individual cell-level controllers is emerging and provides significant advantages. With a homogeneous modular electrical architecture, the distributed BMS topologies enable easier integration and reduce time to market of the application. Moreover, by moving the sensing and controlling part closer to the cell, distributed BMSs minimize potential single point of failures that are present in a centralized topology where excessive wiring from each cell to the central master controller reduces the reliability of the system. In addition, decentralization increases the controlling capability of a BMS, thereby enabling efficient implementation of complex active cell balancing architectures.

In spite of the significant advantages offered by distributed BMS topologies, there exist certain design challenges, which need to be addressed. These challenges are grouped into four different abstraction levels, cell-level, balancing-level, communication-level and algorithm-level. (i) At

cell-level, low-power consumption, high accuracy monitoring and control, galvanic isolation of signals and reduced installation volume are some of the key design challenges that have to be considered while designing an efficient architecture for the individual cell-level controllers. (ii) On the balancing-level, modular, homogeneous active cell balancing architectures providing improved charge transfer capabilities with a reduced number of hardware components and control complexity are required for distributed BMS topologies. (iii) At communication-level, an efficient communication topology depending upon the functions of a distributed BMS is required. For instance, a bus-based communication topology provides higher bandwidth, however, local data exchange between neighboring cells also occupy the bus equally and therefore efficient filtering is required. By contrast, a daisy chain communication enables concurrent data exchange but broadcasts become less efficient. (iv) Finally, a new class of algorithms are required that transfer BMS functions from centralized to decentralized topology by considering the capabilities of the underlying electrical architecture and utilizing the potentials of the communication topology.

This thesis addresses the cell-level and balancing-level design challenges that are associated with distributed BMS topologies. For this purpose, (1) a homogeneous electrical architecture of the individual cell-level controllers in a distributed BMS topology is proposed. (2) To address the challenges associated with the balancing abstraction level, several modular active cell balancing architectures satisfying the design requirements of distributed BMSs are proposed. (3) In addition, accurate closed-form analytical models of the active cell balancing process are developed with which optimized design choices and energy-efficient control points of operation are obtained.

Different functions that are performed by all cell-level controllers of a distributed BMS are identified and the necessary modules that are required in each controller for performing these functions are proposed. Suitable design choices for each module are identified and a custom-designed Printed Circuit Board (PCB) realizing the cell-level controller is developed. Each cell-level controller has a high accuracy sensing module for measuring cell parameters, a power supply module enabling low-power consumption, a galvanically isolated communication channel, an active cell balancing controller module and a computational unit for performing complex computations to calculate SoC and State-of-Health (SoH) of the cell. A distributed BMS development platform consisting of five series-connected Li-Ion cells with each cell associated with a cell-level control unit is developed. This development platform is used as a test bed for functional evaluation of different distributed BMS algorithms and verification of active cell balancing architecture. Easy interfaces to external Data Acquisition (DAQ) systems such as oscilloscopes, LabVIEW enable high accuracy measurements of different parameters that are used for model validation purposes.

To address the challenges associated with the balancing-level, this thesis introduces a design methodology for active cell balancing architectures to be implemented in distributed BMS topologies. Based on these design requirements, three modular active cell balancing architectures are proposed in this thesis for efficiently equalizing the charge levels of individual cells in the battery pack. When compared with state-of-the-art approaches, the proposed balancing architectures provide improved charge transfer capabilities with a reduced number of hardware components and control complexity. Switching schemes for performing charge transfer between cells of a battery pack are derived and verified using an automated framework. Moreover,

a hardware implementation of each proposed balancing architecture is developed and their charge transfer capabilities are verified by integrating into the distributed BMS development platform. All design files of both the distributed BMS development platform and the active cell balancing architectures are uploaded in an online repository for easy reproduction by the scientific community for evaluating distributed BMS algorithms.

For evaluating the system-level performance of the proposed modular active cell balancing architectures, this thesis develops a methodology for deriving accurate, closed-form analytical models that can be used to perform fast simulations of the active cell balancing process. The detailed analytical models include the losses involved in the individual parasitic elements present in the circuit components. Moreover, each part of the analytical model is validated with high accuracy measurements taken from the hardware implementation of the proposed active cell balancing architecture. Using the validated analytical model, optimization approaches are proposed in this thesis for improving the energy efficiency of the equalization process. A design space exploration is performed for identifying optimal device combinations for the balancing unit. In addition, optimal control points of operation for each active cell balancing architecture depending upon the charge transfer scenario are identified to further improve the energy efficiency of the equalization process. Case studies performed with the proposed optimization methodologies show that an optimal circuit configuration operated at energy-efficient control points will result in $80\,\%$ less energy dissipation compared to a random choice of circuit components and operating point.

The electrical architectures and the optimized control algorithms proposed in this thesis are necessary for addressing the challenges associated with higher abstraction levels of distributed BMS topologies. For instance, without knowing the electrical architecture and capabilities of the individual cell-level controller, distributed software algorithms cannot be implemented. Moreover, evaluating the optimal communication methodology for a distributed BMS topology is not possible without the knowledge of its electrical feasibility. Efficient equalization strategies cannot be proposed without considering the capabilities and limitations of the underlying electrical architecture of the active cell balancing unit. Moreover, performance evaluation of the strategies are enabled by the closed-form analytical models proposed in this thesis. Therefore, by addressing the challenges that are associated with cell and balancing levels of distributed BMS topologies, this thesis lays the groundwork for finding efficient solutions to the design challenges associated with higher abstraction levels, such as communication and decentralized algorithm of distributed BMS topologies.

Kurzfassung

Diese Thesis schlägt modulare Schaltungsarchitekturen und optimierte Steuerungsalgorithmen vor, um die Designherausforderungen von verteilten Batteriemanagementsystemen (BMS) zu behandeln.

Hochleistungsanwendungen, wie Elektrofahrzeuge oder stationäre elektrische Speicher, vor allem im Kontext von intelligenten Stromnetzen, nutzen Batteriepacks aus seriell verbundenen Lithium-Ionen (Li-Ion) Batteriezellen. Diese Zellchemie ist anderen bezüglich Energie- und Leistungsdichte überlegen, aber sie reagiert sehr empfindlich auf falsche Betriebsbedingungen. Ein Betrieb außerhalb der vorgegebenen Spannungs-, Strom- oder Temperaturgrenzwerte reduziert ihre Lebensdauer signifikant oder führt gar zu unmittelbaren Schäden, Feuer oder Explosion. Zusätzlich sind die verfügbare Kapazität und die mögliche Leistungsabgabe eines derartigen Batteriepacks in Serienverbindung beeinflusst von Änderungen im Ladungszustand der individuellen Zellen. Solche Änderungen können unter anderem hervorgerufen werden durch Inhomogenität aus dem Fertigungsprozess oder ungleichmäßige Temperaturverteilung im Betrieb. Um diesen Umstand zu mildern, wird typischerweise Balancing durchgeführt und der Ladungszustand der individuellen Zellen angeglichen. Konventionelle Balancingansätze sind passiv. Hier wird überschüssige Energie aus den überladenen Zellen über einen schaltbaren Widerstand als Wärme abgeführt. Im Gegensatz dazu transferieren aktive Balancingansätze die überschüssige Ladung von Zellen mit hohem zu Zellen mit niedrigerem Ladungszustand. Dies erhöht sowohl die Energieeffizienz als auch die Lebensdauer des Batteriepacks. Um sichere Betriebsbedingungen zu gewährleisten und die nutzbare Kapazität eines Li-Ion Batteriepacks zu erhöhen, ist daher ein durchdachtes BMS mit effizienter, aktiver Balancingarchitektur vorteilhaft.

Derzeitige BMS Topologien verwenden einen zentralen Mastercontroller, der die Parameter von jeder einzelnen Zelle überwacht und sichere Betriebsbedingungen einhält. Die aufkommende Dezentralisierung von Hardware- und Softwarearchitektur hingegen bietet signifikante Vorteile. Mit homogener, modularer Schaltungsarchitektur ermöglichen verteilte BMS Topologien einfachere Integration und reduzieren die Produkteinführungszeit. Darüber hinaus minimieren verteilte BMS die Fehleranfälligkeit von zentralisierten Topologien, wo übermäßige Verkabelung von jeder Zelle zum Mastercontroller die Verlässlichkeit des Gesamtsystems reduziert. Zusätzlich erhöht Dezentralisierung die Regelungskapazität des Systems und ermöglicht so die effiziente Implementierung von komplexen, aktiven Balancingarchitekturen.

Trotz der signifikanten Vorteile, die verteilte BMS-Topologien bieten, gibt es auch bestimmte Designherausforderungen, die behandelt werden müssen. Diese Herausforderungen fallen in vier verschiedene Abstraktionsebenen: Zellebene, Balancingebene, Kommunikationsebene und Steuerungsebene. (i) Auf der Zellebene zählen geringer Energieverbrauch, hochgenaue Messung

und Steuerung, galvanische Signalisolierung und reduziertes Volumen zu den Schlüsselherausforderungen, die beim Design einer effizienten Architektur für individuelle Zellcontroller beachtet werden müssen. (ii) Auf der Balancingebene werden modulare, homogene Balancingarchitekturen benötigt, die verbesserten Ladungstransfer ermöglichen mit einer kleineren Anzahl von Hardwarekomponenten und einer geringeren Signalkomplexität. (iii) Auf der Kommunikationsebene wird eine effiziente Kommunikationstopologie gebraucht, die von den Funktionen eines verteilten BMS abhängt. Eine Bustopologie beispielsweise stellt höhere Bandbreite zur Verfügung, hat aber den Nachteil, dass lokaler Datenaustausch den gesamten Bus belegt und daher effizientes Filtern erforderlich macht. Im Gegensatz dazu, erlaubt Daisychain-Kommunikation gleichzeitigen Datenaustausch, aber Broadcasts werden schwieriger. (iv) Zuletzt ist eine neue Klasse von Algorithmen erforderlich, die BMS Funktionalität von zentralisierter in dezentralisierte Topologie überführt, indem sie die das Leistungsvermögen der zu Grunde liegenden Schaltungsarchitektur beachtet und die Potenziale der Kommunikationstopologie nutzt.

Diese Thesis behandelt die Designherausforderungen auf der Zell- und der Balancingebene, die mit verteilten BMS Topologien in Zusammenhang stehen. Zu diesem Zweck wird (1) eine homogene Schaltungsarchitektur vorgeschlagen aus individuellen Controllern auf der Zellebene in einer verteilten BMS-Topologie. Für die Herausforderungen, die mit der Balancingebene zusammenhängen, werden (2) mehrere modulare aktive Balancingarchitekturen vorgeschlagen, die die Designanforderungen von verteilten BMS erfüllen. Zusätzlich werden (3) akkurate analytische Modelle aus geschlossenen Ausdrücken entwickelt, mit denen optimierte Designoptionenund energieeffiziente Arbeitspunkte gewonnen werden.

Verschiedene Funktionen, die auf Zell- und Packebene eines verteilten BMS ausgeführt werden, werden identifiziert und die entsprechenden Module, die jeder Zellcontroller benötigt, um diese Funktionen auszuüben, werden vorgeschlagen. Passende Designoptionen für jedes Modul werden identifiziert und eine speziell entworfene Leiterplatte, die den Zellcontroller realisiert, wird entwickelt. Jeder Zellcontroller hat ein hochgenaues Abtastmodul, um die Zellparameter zu messen, ein Stromversorgungsmodul, das einen geringen Stromverbrauch ermöglicht, einen galvanisch isolierten Kommunikationskanal, ein Controllermodul für aktives Balancing und eine Recheneinheit, um komplexe Operationen zur Berechnung von Ladungs- und Gesundheitszustand der Zelle durchzuführen. Eine verteilte BMS-Entwicklungsplattform wird entwickelt, bestehend aus fünf Li-Ion Zellen in Serienschaltung und einem Zellcontroller für jede Zelle. Diese Entwicklungsplattform wird benutzt als Versuchsstand zur funktionalen Evaluierung von verschiedenen BMS-Algorithmen und zur Verifikation der aktiven Balancingarchitektur. Einfache Schnittstellen zu externen Datenerfassungssystemen, wie Oszilloskopen oder LabVIEW, ermöglichen hochgenaue Messungen von unterschiedlichen Parametern, die zur Modellvalidierung verwendet werden.

Um die Herausforderungen auf der Balancingebene anzugehen führt diese Thesis eine Designmethodologie ein für aktive Balancingarchitekturen, die in verteilten BMS-Topologien implementiert werden sollen. Basierend auf diesen Designanforderungen werden in dieser Dissertation drei modulare aktive Balancingarchitekturen vorgeschlagen, um die Ladungsniveaus von individuellen Zellen im Batteriepack auf effiziente Weise anzugleichen. Verglichen mit dem Stand der Technik, liefern diese Architekturen verbesserten Ladungstransfer mit weniger Hardwarekomponenten und reduzierter Signalkomplexität. Schaltsequenzen, die den Ladungstransfer

schließlich durchführen werden präsentiert und mit einem automatisierten Framework verifiziert. Außerdem wird eine Hardware-Implementierung von jeder vorgeschlagenen Balancingarchitektur entwickelt, die anschließend durch Integration in die verteilte BMS-Entwicklungsplattform validiert wird. Alle Designdateien sowohl von der verteilten BMS- Entwicklungsplattform als auch von den aktiven Balancingarchitekturen sind in einem Repository online verfügbar zum Zweck der einfachen Reproduzierbarkeit durch die wissenschaftliche Gemeinschaft und zur Evaluierung von verteilten BMS-Algorithmen.

Um die Performance der vorgeschlagenen modularen aktiven Balancingarchitektur auf Systemebene zu evaluieren entwickelt diese Dissertation eine Methodologie zur Herleitung von genauen, analytischen Modellen, die auf geschlossenen Ausdrücken beruhen. Diese können benutzt werden, um schnelle Simulation des Balancingprozesses durchzuführen. Die detaillierten, analytischen Modelle enthalten die Verluste, die in den parasitären Elementen der Schaltungskomponenten vorhanden sind. Außerdem wird jeder Teil des analytischen Modells validiert durch hochgenaue Messungen an der Hardwareimplementierung der vorgeschlagenen Balancingarchitektur. Unter Benutzung des validierten analytischen Modells werden in dieser Thesis Optimierungsansätze vorgeschlagen, um die Energieeffizienz des Balancingprozesses zu verbessern. Eine Design-Space Exploration wird durchgeführt, um optimale Kombinationen von einzelnen Geräten für die Balancingeinheit zu identifizieren. Zusätzlich werden in Abhängigkeit von dem Ladungstransferszenario optimale Betriebspunkte für die Balancingarchitektur identifiziert, um die Energieeffizienz des Balancingprozesses weiter zu verbessern. Fallstudien mit den vorgeschlagenen Optimierungsmethodologien zeigen, dass eine optimale Schaltungskonfiguration mit energieeffizientem Betriebspunkt in 80% weniger Energiedissipation resultiert verglichen mit einer zufälligen Wahl von Schaltungskomponenten und Betriebspunkt.

Die in dieser Arbeit vorgeschlagenen Schaltungsarchitekturen und optimierten Steueralgorithmen sind notwendig, um die Herausforderungen im Zusammenhang mit höheren Abstraktionsebenen von verteilten BMS-Topologien zu behandeln. Ohne die Schaltungsarchitektur und das Leistungsvermögen des individuellen Controllers auf Zellebene zu kennen, können verteilte Softwarealgorithmen beispielsweise nicht implementiert werden. Außerdem ist es nicht möglich die optimale Kommunikationsmethodologie für eine verteilte BMS-Topologie zu evaluieren ohne Wissen über die elektrische Machbarkeit. Effiziente Balancingstrategien können nicht vorgeschlagen werden ohne die Fähigkeiten und Beschränkungen der zu Grunde liegenden Schaltungsarchitektur zu berücksichtigen. Außerdem wird Performance-Evaluierung von Strategien durch die geschlossenen, analytischen Modelle aus dieser Dissertation möglich gemacht. Durch die Behandlung der Herausforderungen auf Zell- und Balancingebene bildet diese Arbeit die Grundlage, um effiziente Lösungen für die Designherausforderungen, wie Kommunikation und verteilte Algorithmen, auf den höheren Abstraktionsebenen von verteilten BMS-Topologien zu finden.

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1 Introduction

Electrical Energy Storage (EES) is the process of storing electrical energy in other forms such as hydro, kinetic, chemical etc. and using it when required. Electricity produced at low demand periods are stored in an EES system and are then used to complement the base power plants during peak periods. This prevents the fluctuation in electricity prices by avoiding the use of expensive power generation systems during the peak periods of demand. Moreover, with the increasing global pollution level, alternative forms of electricity production using renewable energy resources such as solar or wind are gaining more importance. However, their dependence on environmental conditions make them unpredictable and volatile, in which case EES systems become necessary to store the electrical energy produced during favorable weather conditions. Apart from the power generation and distribution systems, mobile EESs are widely used in emerging technologies like EVs and HEVs, forming a pollution free, sustainable transportation solution alternative to the gasoline powered Internal Combustion Engine (ICE) vehicles.

There are different forms of EES systems available depending upon the specific requirements of each application. For very high power storage, in the range of several MW to few GW, pumped hydro storage can be used, where the electrical energy generated during off peak periods is stored by pumping water from a lower reservoir to an upper reservoir. On the other hand, EES formed by double-layer capacitors also called as *supercapacitors* are mainly used in applications where the stored energy has to be retrieved within short time periods in the range of seconds to minutes. Similarly, the electrical energy generated during the low demand time is used to electrolyze water molecule and the released H_2 is used in a fuel cell EES to support the high demand during peak periods.

Electrochemical EESs in the form of batteries are widely used to store the electrical energy due to their high energy and power density. Higher energy and power density correlates to lower required installation volume for storing the electrical energy. Moreover, batteries can be tailored to meet the specific requirements of the application such as fast charging, longer shelf life, higher

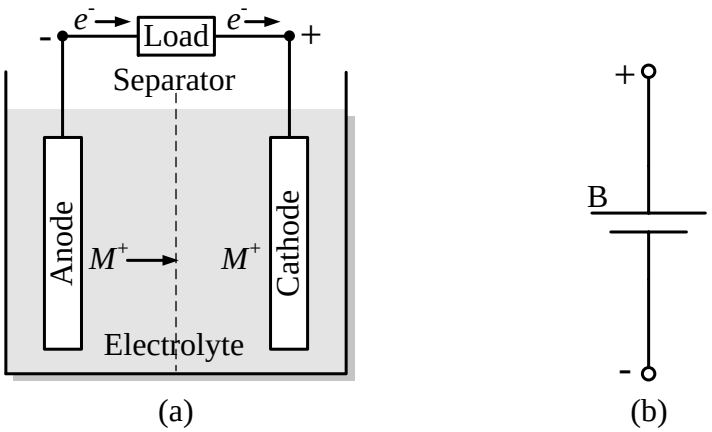


Figure 1.1: Electrochemical cell, the fundamental unit of a battery pack. (a) Shuttle ions (M^+) are oxidized at the anode and move towards the cathode inside the cell. The electrons (e^-) released during this oxidation travels through the outer circuit to power the load. (b) Electrical symbol of the electrochemical cell, which will be used hereafter in this thesis.

power capability or higher energy density. Therefore, they are widely used as EES in the kW and MW power range. In addition, they dominate other technologies in the field of mobile EES such as EVs and HEVs due to their highly compact nature with high specific energy and power.

1.1 Electrochemical Cell and Battery Packs

Batteries are electrochemical storage devices, meaning their chemical reaction is coupled with an electron transfer. In general, batteries are broadly classified into *primary* (non-rechargeable) and *secondary* (rechargeable). The primary, non-rechargeable batteries are designed to be used once and are discarded when the active chemical materials of the battery generating electricity are fully utilized. By contrast, the secondary rechargeable batteries can be charged and discharged multiple times. They perform a reversible chemical reaction, which allows them to store electrical energy (*charging*) and release the stored electrical energy by performing the opposite reactions (*discharging*). In case of EES systems, the secondary rechargeable batteries are preferred since they allow to store (charge) and extract (discharge) the electrical energy without the necessity for replacing the battery itself.

The basic unit of a rechargeable battery is an electrochemical cell, which consists of a positive electrode *cathode*, a negative electrode *anode* and an electrolyte to favor the movement of the charge carries inside the cell as shown in Fig. 1.1a. During discharging, shuttle ions (M^+) are oxidized at the anode side and release electrons (e^-), which travel through the outer circuit to power the load. The oxidized shuttle ions move through the electrolyte to the cathode inside the cell and are reduced by the incoming electrons from the outer circuit. This process is represented

by the following equations:

$$Anode\colon M \rightarrow M^{+} + e^{-} \qquad (Oxidation) \tag{1.1}$$

$$Cathode\colon M^{+} + e^{-} \rightarrow M \qquad (Reduction) \tag{1.2}$$

The opposite reactions take place during charging, facilitating storage of electrical energy in the form of chemical reactions. Fig. 1.1b, shows the electrical equivalent symbol of an electrochemical cell, which will be used hereafter in this thesis to represent a battery cell.

1.1.1 Secondary Rechargeable Batteries

The secondary rechargeable batteries are further classified into different chemistries based on the chemical composition of the anode, cathode and the electrolyte materials used for construction. For example, a Nickel-Metal Hydride (NiMH) secondary rechargeable battery chemistry consists of nickel cathode, a hydrogen absorbing anode and a potassium hydroxide electrolyte. Similarly, the lead-acid battery chemistry is made of Lead-dioxide cathode, a metallic Lead anode and an electrolyte of sulphuric acid solution. Compared to all the secondary rechargeable battery chemistries, the Lithium (Li) based batteries provide superior performance in terms of energy and power densities, since the electrochemical potential of Li is higher compared to other materials. Moreover, the flexibility in designing the cell for high specific energy (Energy cell) or for a high specific power (Power cell) provides a wide range of applications for this type of battery chemistry.

Advantages of Lithium batteries. The Li chemistry based rechargeable cells dominate other secondary cells with their high energy and power densities. Therefore, the cells can be manufactured with smaller size and weight for the same energy and power requirements of the application. Moreover, Li based cells can be manufactured in several form factors and shapes such as cylindrical, prismatic, pouch cells etc., that enables different compact mechanical arrangements for forming battery packs. Li based cells do not exhibit any memory effect (a situation in which the battery loses its energy capacity with repeated charging after partial discharging) which is commonly visible in other secondary rechargeable cells with Nickel (Ni) based chemistry. As a result, they provide a longer cycle life compared to other secondary rechargeable battery chemistries. In addition, superior thermal and chemical stability of Li chemistry enables them to be used for higher discharge current rates without having a risk of thermal runaway. Therefore, they are predominantly used in EVs and HEVs, where high acceleration and regenerative braking currents are typically experienced. In addition, having a high coulombic efficiency (ratio of discharged capacity over charged capacity) and low self discharge rate makes them the market leader in the domain of rechargeable battery chemistries. While several Li chemistry based cells are available, Li-Ion technology is the most preferred cell type for high voltage applications such as EVs, HEVs, stationary EES etc.

1.1.2 High Voltage Battery Packs for Automotive Applications

While high voltage battery packs consisting of Li-Ion cells are used in several applications such as EVs, stationary energy storages for smart grids etc., this thesis primarily focuses on

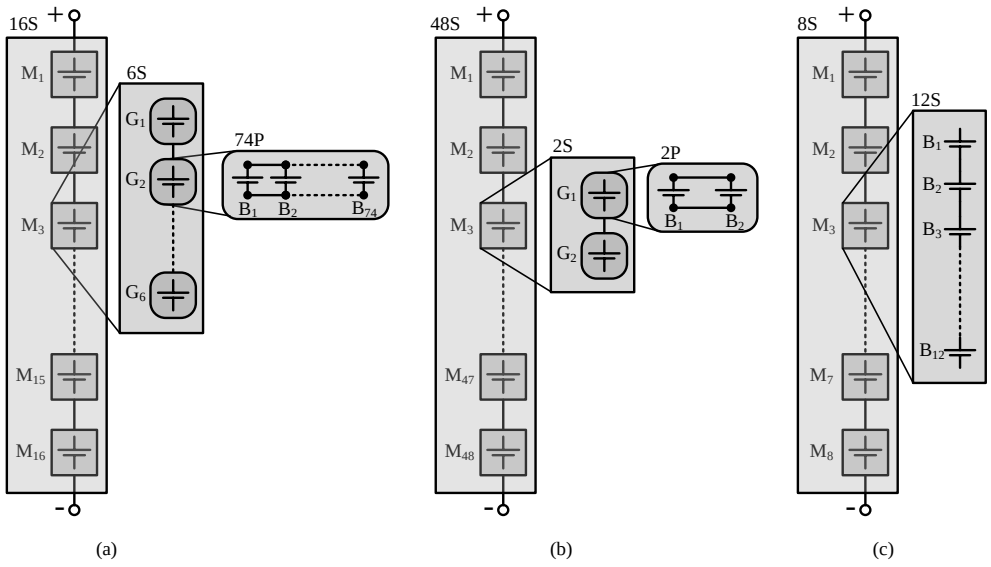


Figure 1.2: High voltage battery packs. (a) Tesla Model-S $85\,\mathrm{kW\,h}$ battery pack, consisting of 96 series-connected modules with 74 parallel-connected individual Li-Ion cells in each module. (b) Nissan leaf battery pack with 96 series-connected modules each having 2 sheet shaped $32{,}5\,\mathrm{A\,h}$ Li-Ion cells in parallel. (c) BMW i3 EV battery pack having 96 series-connected $60\,\mathrm{A\,h}$ cells.

automotive battery packs, since the research work is performed in TUM CREATE, which is a center for electromobility research in Singapore. Moreover, EV battery packs cover a large set of challenges, with their specific requirements of higher energy and power delivery, high capacity storage with reduced volume and weight, stringent monitoring requirements to provide safe operation etc. However, the concepts and technologies proposed in this thesis are suitable for all applications involving high voltage battery packs.

The current capacity of a single Li-Ion cell depends upon the geometry of the cell. For instance, a Li-Ion cell of "18650" form factor ($18\,\mathrm{mm}$ in diameter and $65\,\mathrm{mm}$ length) has typically a capacity in the range of $3\,\mathrm{A\,h}$, whereas the large format pouch cells have a capacity in the range of $60\,\mathrm{A\,h}$. Moreover, the operating voltage of a single Li-Ion cell is in the range of $2{,}7\,\mathrm{V}$ to $4\,\mathrm{V}$. Nevertheless, the voltage and capacity of a single Li-Ion is insufficient to support high power EV and HEV requirements of $450\,\mathrm{V}$ and $200\,\mathrm{A\,h}$. Therefore, battery packs for these high power applications are formed with a number of series and parallel connected individual Li-Ion cells. In order to have a higher current capability, multiple Li-Ion cells are connected in parallel and the required higher operating voltage can be obtained by series-connection of individual cells. For example, by connecting five $3\,\mathrm{A\,h}$ individual Li-Ion cells in parallel results in a total capacity of $15\,\mathrm{A\,h}$ and connecting twelve of these parallel-connected modules in series provides a voltage of $48\,\mathrm{V}$, considering the nominal voltage of each cell is $4\,\mathrm{V}$. This corresponds to an EES of $720\,\mathrm{W\,h}$.

Example high voltage battery packs. The Tesla Model-S full EV consists of a battery pack of $85\,\mathrm{kW\,h}$. It is made up of Panasonic "18650" Li-Ion cells each having a capacity of $3{,}2\,\mathrm{A\,h}$. The battery pack is divided into 16 series-connected modules and each module has six series-

connected groups of 74 parallel-connected individual Li-Ion cells as shown in Fig. 1.2a. The battery pack configuration is represented as 74P6S16S with a total of 7104 individual Li-Ion cells. On the other hand, the battery pack in the Nissan leaf EV is formed by 48 series-connected modules. Each module consists of 4 cells that are configured in 2P2S fashion, 2 series-connected groups and in each group 2 sheet shaped $32{,}5\,\mathrm{A\,h}$ Li-Ion cells are connected in parallel as shown in Fig. 1.2b. The entire battery pack configuration is represented as 2P2S48S. The BMW i3 EV has 12 series-connected $60\,\mathrm{A\,h}$ prismatic Li-Ion cells forming a module and the battery pack consists of 8 modules connected in series represented as 1P12S8S pack configuration as shown in Fig. 1.2c.

1.2 Battery Pack Challenges

The benefits of high energy and power densities offered by Li-Ion cells do not come for free. A comprehensive overview of issues associated with battery packs consisting of Li-Ion cells is provided in [1]. The critical challenges pertaining to high voltage battery packs consisting of multiple series-connected Li-Ion cells are

- Safety and
- Energy-efficiency

Li-Ion cells are very sensitive towards their operating conditions and require tight monitoring of their parameters to maintain safe operation conditions. Furthermore, sophisticated circuit architectures and control methodologies are required to improve the energy-efficiency of the battery pack, which directly translates to improved driving range in terms of EV applications and reduced CO_2 consumption in stationary EES storage systems. A detailed discussion on both of the above mentioned challenges is provided in the following.

1.2.1 Safety

Li-Ion cells have a defined set of safe operating conditions in terms of voltage, current and temperature. Operation outside the specified limits can severely damage the cells reducing their lifetime and possibly cause fire or explosion due to thermal runaway.

Safe operating voltage. The minimum and maximum operating voltage of most Li-Ion cells are in the range of $2{,}7\,\mathrm{V}$ and $4{,}2\,\mathrm{V}$, respectively. Charging a Li-Ion cell with a voltage higher than that specified, causes excessive current flows inside the cell and increases the internal temperature leading to fire or explosion by thermal runaway. Moreover, over-charging leads to a process called *Lithium Plating* that occurs on the anode surface, reducing the freely available lithium ions and result in an irreversible capacity loss. In addition to the capacity loss, lithium plating will also lead to an internal short circuit of the cell causing excessive temperatures that ultimately damage the cell. Similarly, discharging a Li-Ion cell below its minimum threshold voltage (over-discharging) results in a gradual breakdown of the internal cell electrodes, reducing their lifetime. In certain situations, over-discharging releases metallic ions from the electrodes

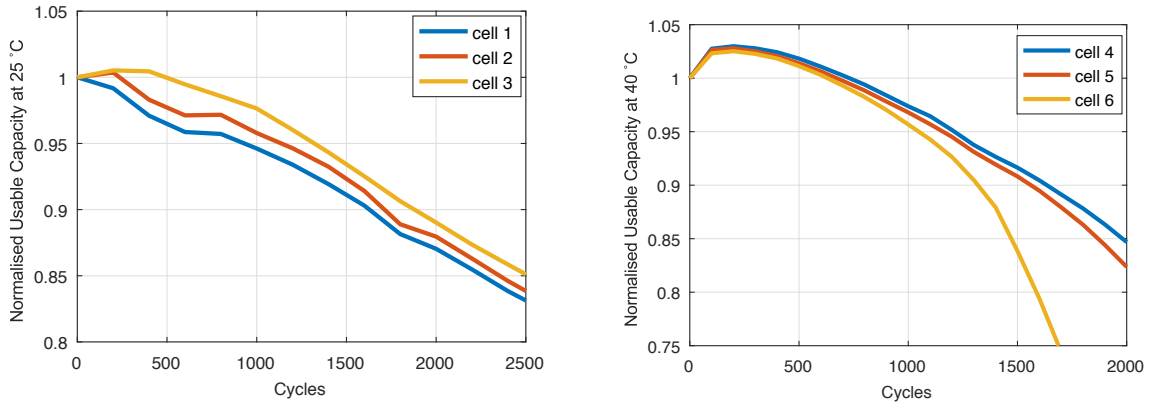
into the electrolytes which can potentially cause internal short circuits between the electrodes of the cell. Therefore, strict operating limitations in terms of cell voltage are required to maintain safe operating conditions.

Safe operating current. The maximum current with which a cell can be charged depends upon the design of the electrodes. With a proper cell design, charging currents as high as 4C are possible, where C signifies the current rate required to charge or discharge the cell in one hour. Nevertheless, charging with high currents (*fast charging*), especially in terms of EV applications, is gaining more importance, since a regular charging of an EV battery pack might take hours. However, increasing the charging current significantly increases the temperature of the cell and if adequate control measures are not taken to regulate the battery pack temperature, the lifetime of the battery pack will significantly be reduced. In certain cases, the cells experience an increased pressure due to charging at a higher current and will start to swell due to generation of gases inside the cell. If provisions to vent out the gases and adequate mechanical clearance between cells in the pack are not provided, it will result in a short circuit situation leading to fire or explosion due to thermal runaway. Likewise, discharging the cell with higher currents results in an inherent capacity loss, due to the *rate capacity effect*, which is defined as the reduction in the battery capacity obtained due to the increased discharge current. Therefore, it is necessary to limit the charging and discharging currents within the safe operating limits, in order to extend the lifetime of the cell and to obtain the maximum output capacity from the cell.

Safe operating temperature. As explained in Section 1.1, an electrochemical cell stores energy in the form of chemical reactions. The rate of these chemical reactions is directly affected by the temperature. With very low temperatures the speed of the chemical reactions is very slow and therefore results in a reduced current carrying capacity, both in terms of charging and discharging. Prolonged operation of the battery pack at reduced temperatures, below $0\,^{\circ}\mathrm{C}$, will result in a premature capacity loss of the battery pack. In contrast to the low temperature operation, increased temperatures will result in catastrophic effects causing fire or explosion. With temperatures over $80\,^{\circ}\mathrm{C}$, the protection layer between the electrolyte and the electrode deforms. This results in an exothermic chemical reaction between the electrolyte and the electrode that further increases the temperature. Temperatures above $110\,^{\circ}\mathrm{C}$ results in the breakdown of the electrolyte material and releases flammable hydrocarbon gases within the cell. If the generated gases are not released safely, the internal pressure of the cell builds up, until a point when the cell structure ruptures and the internal gases release into the atmosphere, catching fire immediately. Therefore, temperature is an important property to be monitored and controlled to ensure the safety and efficiency of the cell.

1.2.2 Energy Output

As shown in Fig. 1.2, battery packs for high power applications such as EVs, HEVs are formed by multiple series-connected Li-Ion cells to achieve the required operating voltage. The usable capacity of a series-connected battery pack is limited by the cell with the minimum SoC compared to other series-connected cells. As explained in Section 1.2.1, Li-Ion cells have strict limits



(a) (b)

Figure 1.3: Capacity degradation of Li-Ion cells with repeated cycling at different temperatures. (a) Three cells from the same manufacturing lot are cycled at $25\,^{\circ}\mathrm{C}$ and (b) at $40\,^{\circ}\mathrm{C}$.

with respect to their operating voltage. Over charging or over discharging a Li-Ion cell above its specified voltage limit will result in the damage of the cell and in some cases leads to fire or explosion due to thermal runaway. Therefore, the discharging or charging process of a series-connected battery pack must stop when any cell in the pack reaches the lower or upper operating thresholds, respectively. In an ideal case all cells forming the battery pack are required to be uniform, thereby reaching the top and bottom threshold limits at the same time enabling to fully utilize the available capacity of the battery pack. However, in reality, there exists certain variations between the cells thus limiting the maximum usable capacity. These variations between cells are primarily attributed to the following reasons.

1.2.2.1 Manufacturing Variances

Cell mismatch due to manufacturing process can range from $1\,\%$ to $10\,\%$ depending upon the quality of manufacturing and the control process [2, 3]. Manufacturing process of individual raw materials required for the cell production are highly mature and therefore considered to be homogeneous. However, the combination of these individual raw materials to form a Li-Ion cell requires several steps and each phase has to be monitored and controlled closely to minimize the variations between each cell. For instance, the active material (anode and cathode) production involves powdering the raw materials and slurry formation by mixing the powdered raw materials of anode and cathode [4]. Having a uniform composition of these powders is critical to minimize the variation in manufactured cells capacity. Uneven particle sizes and shapes will result in different surface areas of the powders which will lead to cells with different capacities. Moreover, variations in the content of active material, composition and physical property of cells will lead to different characteristics of Li-Ion cells [5].

Tiny imperfections in the manufacturing process of Li-Ion cells lead to soft shorts inside the cell, which results in different self-discharge rates of each cell. Studies [6] show that this difference in self-discharge could be in the range of $3\,\%$/month. This difference is cumulative and aggravates with repeated cycling leading to a higher differential SoC between individual cells in

a pack, which results in a reduced usable capacity. Even after manufacturing with tight process control and sorting the cells carefully based on their capacity, imbalances between cells tend to develop with aging and operating temperature. Three Li-Ion cells from the same manufacturing lot are cycled at different operating temperatures to identify the capacity degradation over aging. In one set the temperature was maintained at $25\,^{\circ}\mathrm{C}$ and in other set the operating temperature was kept at $40\,^{\circ}\mathrm{C}$, respectively. The normalized capacity plots are shown in Fig. 1.3. As seen, the normalized capacity of cells differs with cycling and this will result in a reduced usable capacity of the battery pack after certain charge/discharge cycles.

1.2.2.2 Temperature Distribution

The other major source of cell-to-cell variations in a series-connected Li-Ion battery pack is the temperature distribution in the pack. According to Arrhenius law, the speed of chemical reactions doubles with every $10\,^{\circ}\mathrm{C}$ rise in temperature. As a result, each cell will have a varying discharge characteristic if their surrounding temperature is not uniform. Moreover, uneven temperature distribution along the battery pack will lead to mismatch in the internal cell resistances and their self-discharge rates [7]. Li-Ion also experience capacity degradation and reduction in lifetime at higher operating temperatures. For instance in [8], a heat-map of a Li-Ion battery pack is obtained in order to study the variations in temperature at each end of the battery pack. It was observed that the temperature of the cooling air increases by $1{,}3\,^{\circ}\mathrm{C}$ as it crosses each module of cell. As a result there exist a certain difference in temperature between cells that are placed near to the cooling inlet than cells that are placed farther away. In the above-mentioned case study ([8]) this difference in temperature was calculated to be $13\,^{\circ}\mathrm{C}$. This will lead to inhomogeneous discharging of the battery pack, with cells that are placed close to the cooling inlet having higher capacities and cells that are father away will provide a reduced capacity. Moreover, this will also result in unequal aging of the battery pack since cells that experience a higher temperature will age much faster than others.

Furthermore, at higher operating temperatures, unwanted chemical reactions such as phase changes in electrode, active lithium consumption, passive film formation, etc., take place inside a Li-Ion cell, which will eventually lead to capacity degradation [9]. A case study performed in [10] using Sony 18650 Li-Ion cells revealed that the cell lost around $60\,\%$ capacity after 500 cycles at $50\,^{\circ}\mathrm{C}$ and $70\,\%$ at $55\,^{\circ}\mathrm{C}$. Larger differences in operating temperatures along the battery pack will lead to uneven capacity degradation of cells in the pack. Therefore, proper thermal management is required to maintain uniform temperature across the battery pack for obtaining higher usable capacity.

1.2.2.3 Impact of cell-to-cell variations

Due to the above mentioned factors, SoC of individual cells in a series-connected battery pack differs and this variation will impact the usable capacity of the battery pack. To analyze the impact of cell-to-cell variation, consider a battery pack consisting of 4 series-connected Li-Ion cells as shown in Fig. 1.4a. Due to manufacturing variations and temperature distribution, the SoC of cell B^1 is at $70\,\%$ and that of cell B^4 is at $50\,\%$. As soon as a load current is drawn from the battery pack at time 0, the SoC of all cells start to decrease depending upon the load current

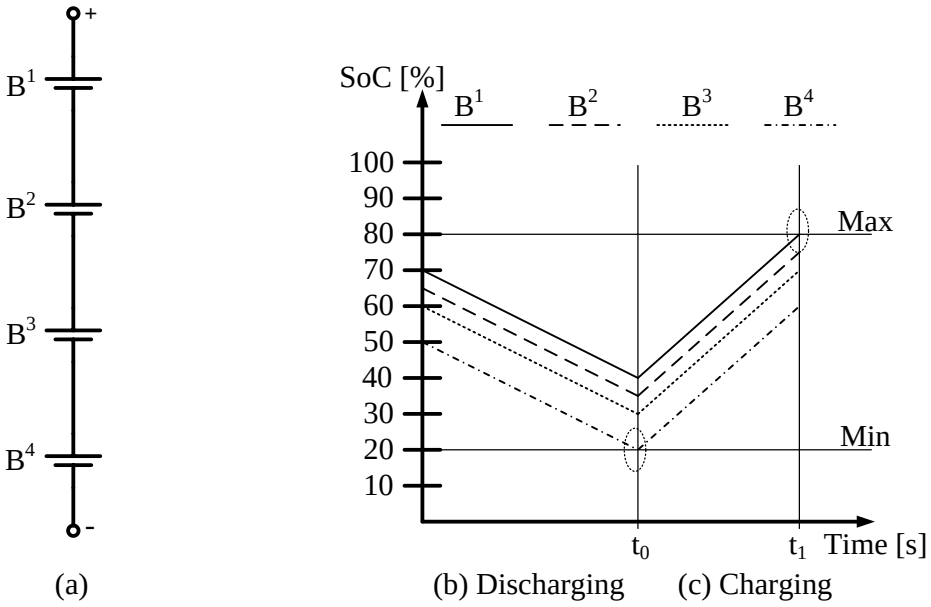


Figure 1.4: Motivating example consisting of four series-connected Li-Ion cells to show the impact of cell-to-cell SoC variations. (b) While discharging, Cell B^4 with a lower SoC compared to others will stop the discharging process as soon as it reaches the bottom threshold value. (c) While charging, Cell B^1 with a higher SoC compared to others will stop the charging process once the top threshold is reached.

value. A series-connected battery pack can only be discharged till the SoC of any cell in the pack reaches the bottom threshold value. In this example, cell B^4 is the weakest cell compared to others and will reach the lower threshold value faster than other cells in the pack. Therefore, once cell B^4 is discharged to the lower threshold value, see Fig. 1.4b, the discharging process has to be stopped. Even though other cells in the pack have active energy stored in them, it cannot be used for discharging since all cells are connected in series and any current flowing out of the pack will deep discharge cell B^4, eventually damaging the cell. As a result, the discharging process of the battery pack has to be stopped at time t_0 (see Fig. 1.4b), with the SoC of cells B^1, B^2, B^3 and B^4 at the end of discharge being $40\,\%$, $35\,\%$, $30\,\%$ and $20\,\%$, respectively, assuming cells B^2 and B^3 start with $65\,\%$ and $60\,\%$ SoC values, respectively.

Once SoC of any cell in the pack has reached the lower threshold value, the BMS notifies the pack is empty and requests for charging. Since all cells are connected in series, the same charging current flows through all of them and their SoC starts to increase depending upon the current value. The charging process continues till any one cell in the pack reaches the top threshold value. In the example here, cell B^1 is the strongest cell and therefore reaches the top SoC threshold earlier than other cells in the pack. Once cell B^1 is fully charged (at time t_1), the charging process has to be stopped (see Fig. 1.4c), even though remaining cells in the pack are not fully charged. This results in a battery pack consisting of cells that are unevenly charged.

Repeated charging and discharging of such an imbalanced battery pack, will result in a situation where the cell with the low SoC value (B^4) stops the discharging process and the BMS requests for charging. Once the charging plug is connected, the cell with a higher SoC value (B^1) will reach the top SoC threshold and the BMS notifies that the battery pack is fully charged. This deviation increases over time and continues as a chain reaction eventually resulting in a situation where the battery pack can no further be discharged (cell B^4 stops discharging) or charged (cell B^1 stops charging). This leads to an unusable battery pack and therefore it is required to equalize the SoC of individual cells in the battery pack in order to fully utilize the usable capacity.

The process of equalizing the SoC of individual cells is referred to as *cell balancing* and it is broadly classified into *passive* and *active*. Passive cell balancing involves dissipation of the excess charge stored in cell(s) with higher SoC across a switched resistor. Even though it is simple to implement and cost-efficient, it is not energy-efficient, since the excess charge in cell(s) is dissipated as heat across the resistor. By contrast, active cell balancing approaches are energy-efficient since they transfer the excess charge from cell(s) with higher SoC to cell(s) with lower SoC using energy storage elements. However, their electrical architecture is highly complex consisting of higher number of switches and require sophisticated high frequency control signals for operation. More details regarding cell balancing and their types are explained in Chapter 4.

1.3 Battery Management System (BMS)

In order to address the above mentioned challenges associated with high voltage battery packs, a sophisticated Battery Management System (BMS) is required to maintain safe operating conditions and to maximize the usable capacity of the battery pack. A definition of basic tasks performed by a BMS as defined in [11] is:

> *The basic task of a BMS is to ensure that optimum use is made of the energy inside the battery in powering the load and that the risk of damage inflicted upon the battery is minimized. This is achieved by monitoring and controlling the battery's charging and discharging process.*

The BMS monitors the parameters such as voltage, current and temperature of individual cells and controls them within their safe operating limits. In addition, the BMS accurately calculates the cell states such as SoC and SoH, which are required to estimate the driving range and lifetime of the battery pack, respectively. Moreover, the BMS controls the cell balancing process for minimizing the cell-to-cell variations within the series-connected battery pack and thereby improves its usable capacity. Following are the key functions performed by a typical BMS of a high voltage battery pack.

Monitoring and control. The BMS has a dedicated sensing module, which accurately measures the required cell parameters such as voltage, current and temperature of each individual cell of the battery pack. In addition, the BMS coordinates with other control units of the application to maintain the safe operating limits of the individual cell parameters. For instance, to regulate the

battery pack temperature, the BMS coordinates with the Heating, Ventilation and Air Conditioning (HVAC) control unit of the application to maintain uniform and safe operating temperatures within the battery pack. Similarly, communication with the charging station enables to prevent over charging and over discharging situations in the battery pack.

Computation. Computation of SoC is an important function of a BMS. SoC is directly related to the stored charge available in the battery pack, which in terms of an EV translates to the possible driving range. In addition to SoC, SoH of a battery pack is also calculated by the BMS. This signifies the ability of the battery pack to accept or deliver requested power. Moreover, accurately estimating the SoH enables timely replacement and in maintenance of used battery pack.

Cell balancing. The usable capacity of the battery pack is improved by performing cell balancing, which involves equalization of SoCs of individual cells in the series-connected battery pack. The BMS determines the SoCs of individual cells through its computational capability and actuates the associated cell balancing modules of the respective cells to perform equalization. In case of passive cell balancing, the BMS controls the amount of charge that is dissipated across the shunt resistor. By contrast, if an active cell balancing methodology is employed, the BMS determines the source and destination cells of the charge transfer pair and generates the necessary high frequency control signals required to transfer charge between them.

1.4 BMS Topologies

Depending upon the hardware and software architecture of the BMS, they are broadly classified into *centralized* and *distributed*. Distributed BMSs are further classified into hierarchical, partially distributed and fully distributed topologies, depending upon their levels of decentralization.

1.4.1 Centralized BMS Topology and Challenges

State-of-the-art BMSs [12], as will be explained in detail in Chapter 3, are centralized in fashion as shown in Fig. 1.5a. A single master controller monitors and maintains all operating parameters of each individual cell of the battery pack. Sensors from individual cells are directly wired to the master controller in which all computations and control functions of the BMS are performed. The main advantage of this approach is its cost effectiveness, since only a single controller is required to manage all cells in the battery pack. Even though the centralized BMS topology is cost effective to implement, there are significant challenges faced by this approach due to the growing complexity of battery packs and a huge demand to reduce the time-to-market especially in terms of EV applications.

1.4.1.1 Modularity and Scalability

The centralized BMS topology has a huge integration effort. For each application, the mechanical layout and thermal design of the battery pack is required to determine the design, sizing and placement of the central controller board. Any changes to the mechanical properties of the battery pack at later design stages, will impact the hardware design of the central controller board. Moreover, the requirements and specifications of the battery pack differs for each application if they use different types of cells. In such cases, using a centralized BMS topology leads to a full redevelopment of the monitoring circuit boards to suit the application requirements. Subsequently, the software design has to be updated according to the new hardware specification for each new application. This leads to an increased time-to-market of the application.

1.4.1.2 Wiring and Control Complexity

With a central master controller monitoring parameters of each individual cells, there exists a huge amount of wiring between cells and the controller. Typically, each cell requires sensors for voltage and temperature, which for a battery pack consisting of 96 series-connected cells results in a total sensor count of 192. Since all cells are connected in series and the same current flows through all of them, a single current sensor is sufficient to measure the battery pack current. Nevertheless, considering a minimum of 2 wires per sensor, a total of 386 individual wires from all cells will be connected to the central master controller. This significantly increases the wiring harness and weight, which in EV and HEV applications directly impacts the driving range. Moreover, the DC potential of each cell along the series string of the battery pack varies and therefore, proper galvanic isolation of signals is required in order to prevent potential short circuits. This vastly increases the complexity and makes debugging difficult at later stages of vehicle maintenance.

From a control perspective, with a central master monitoring and controlling the parameters of all individual cells, it is significantly challenging to implement active cell balancing approaches. As discussed in Section 1.2.2, the usable capacity of the battery pack is improved by performing active cell balancing, where the excess charge from cell(s) with higher SoC are transferred to cell(s) with lower SoC. For this purpose each cell of the battery pack will be associated with an individual active cell balancing unit and depending upon their electrical architecture one or more high frequency control signals are required to transfer charge between cells. Generating all high frequency control signals with the required timing parameters from a central controller and distributing them to each cell is highly challenging and difficult to implement, while still performing other critical functions of the BMS.

1.4.1.3 Reliability

The master controller in the centralized BMS topology represents a potential single point of failure in the system. Any fault in the controller will isolate the battery pack from the application unit and improper isolation in certain scenarios might lead to catastrophic accidents, especially in terms of EVs. Moreover, the excessive wiring from the cell sensors to the master controller in the centralized topology also increase the probability of failures in the system. It is highly

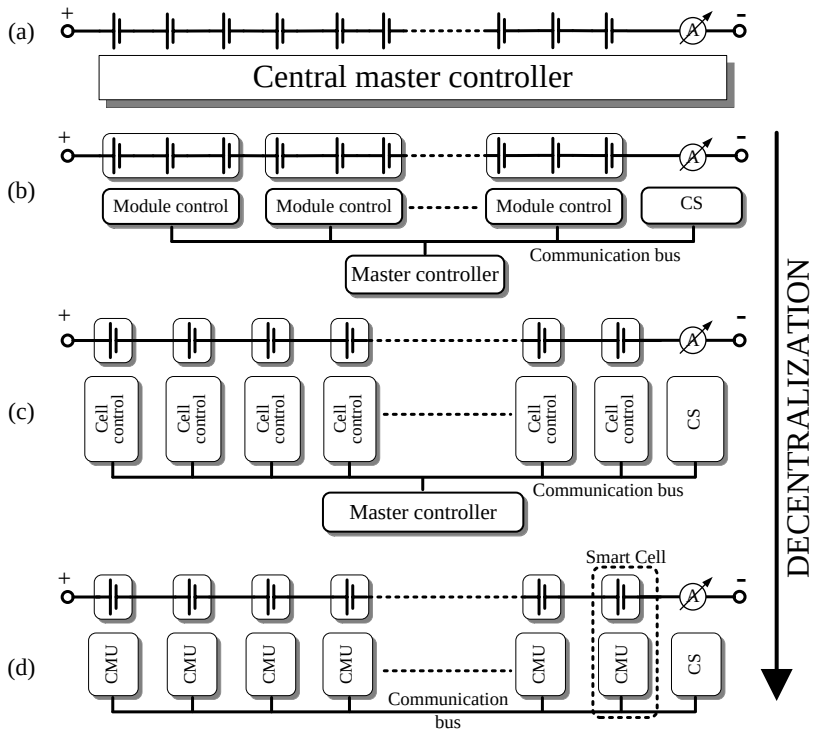


Figure 1.5: BMS topologies. (a) Centralized, (b) Hierarchical, (c) Partially distributed and (d) Fully distributed *smart cells*.

difficult for the central master controller to distinguish between a fault in sensor cable from a fault in the cell. If a signal wire from the sensors of any cell breaks, the master controller will shutdown the application unit by isolating the battery pack.

1.4.2 Distributed BMS Topologies

In order to overcome the above mentioned challenges faced with a centralized BMS topology, distributed BMSs are an emerging alternative. Fig. 1.5 shows the trend towards decentralization of BMS topology in state-of-the-art approaches. Compared to the centralized topology, in [13], a hierarchical system was proposed, which groups 8 to 12 series-connected cells into a module and monitors them with a dedicated slave control unit. These individual slave units are then controlled with a central master controller as shown in Fig. 1.5b. Further decentralization, resulted in a partially distributed BMS topology as shown in Fig. 1.5c, where each individual cell is monitored with a dedicated cell-level control unit and a overall master controller unit to coordinate the individual cell-level controllers. Fig. 1.5d, shows the topology of a fully distributed *smart cell* BMS topology. Each cell in the battery pack is provided with an intelligent monitoring and control unit making the individual battery cells into *smart cells*. Series-connection of multiple *smart cells* forms the battery pack, in which the BMS functions are performed in a fully distributed fashion by employing techniques from the domain of distributing computing.

More details regarding each individual BMS topology is provided in Chapter 3. Even though distributed BMS topologies significantly address the challenges associated with the centralized approach, they require a paradigm shift in their design methodology. Design challenges in distributed BMSs that has to be addressed for an efficient implementation are classified into four levels as follows.

1.4.2.1 Cell-level Design Challenges

Low power consumption is the key design criteria of a distributed BMS controller. Especially, in the case of partially and fully distributed BMSs, where each cell is associated with an individual control unit powered from the respective battery cell, power consumption of the individual controllers must be very low in order not to drain the cell for monitoring purpose itself. Low-power circuit design methodologies and intelligent power management techniques are required to minimize the power consumption of the individual controller. Furthermore, in a series-connected battery pack, the DC potential of each cell varies with respect to the negative terminal of the battery pack. For instance, the voltage across the terminals of cell 2 is $4\,\mathrm{V}$ and $8\,\mathrm{V}$ and that of cell 100 would be $396\,\mathrm{V}$ and $400\,\mathrm{V}$, with respect to the negative terminal of the battery pack, respectively. Since the individual cell controllers are powered directly from their respective battery cells, the ground potential of each controller varies while charging and discharging the pack. As a result, the sensing module in each cell-level controller has to be designed in such a way to overcome the measurement inaccuracies and the common-mode noise introduced by the varying DC potential. Moreover, appropriate galvanic isolation has to be provided for the communication signals between the controllers, in order to prevent potential short circuit situations. Apart from these circuit design challenges, the size and weight of the individual cell-level controller has to be minimized for integration with the cell. Eventually, a system-on-chip solution that can be integrated with the cell is required to minimize the volume and to overcome the integration challenges.

1.4.2.2 Balancing-level Design Challenges

With the decentralization of the BMS topology into modules and individual cell-level control units, efficient implementation of active cell balancing approaches is possible due to the ability to generate the required high frequency control signals locally. However, the challenge now shifts from the controlling perspective of active cell balancing architectures to their electrical architecture design. Distributed BMSs require the underlying active cell balancing architecture to be modularized into individual homogeneous units that can be attached with each cell-level controller. Subsequently, the system-level balancing architecture has to be formed with reduced interconnection between these individual units, in order to maintain the low integration efforts promised by distributed BMS topology. In addition to being modular, the control scheme of the balancing architecture requires to be self-contained, meaning, all required high frequency control signals for transferring charge between cells must be generated independently by the respective controllers without any requirement of synchronization with other controller units.

Apart from the architectural design challenges, fast and accurate models of the active cell balancing architectures are required to facilitate system-level performance analysis through

simulations. Moreover, the analytical models are used to perform design space exploration and optimization of the energy-efficiency of the active cell balancing architecture. On a system-level perspective, having an automated verification methodology such as in [14] and [15], that validates the control scheme of an active cell balancing architecture will rapidly speed-up the design process. Moreover, smart charge transfer algorithms are required to increase the energy-efficiency of the balancing process by fully utilizing the capabilities of the underlying active cell balancing architecture.

1.4.2.3 Communication Design Challenges

Determining an appropriate communication architecture for a distributed BMS is a challenging task. For instance, a bus-based communication architecture achieves higher bandwidth and enables direct communication between the cell-level controllers. However, it requires an isolated power supply for galvanically isolating the communication signals, resulting in an increased current consumption from the battery cell. Moreover, communication between adjacent cell-level controllers equally occupy the bus which requires efficient scheduling and filtering. On the other hand, the power consumption is reduced by using a daisy chain communication architecture, where the cell-level controllers can only communicate to their adjacent units. However, propagating data from the first cell to the last cell in the series chain of the battery pack consumes considerable amount of time, which might not be suitable for certain time critical functions, such as notification of fault in a cell to the entire battery pack. Therefore, an appropriate communication methodology, is required to have a fast and energy-efficient communication between cell-level controllers. Consequently, the top-level distributed algorithms implementing the BMS functions must consider the capabilities of the underlying communication architecture and optimize the management functionality. Moreover, a robust communication architecture is required, to withstand the harsh environments of automotive applications. Furthermore, establishing a secure communication protocol between the individual cell-level controllers is essential for safe operation of the BMS. By enabling encrypted messaging schemes, only the intended recipients of the message can access it. From that perspective, it is mandatory to have a light-weight encryption algorithm such as in [16], that is fast and secure, while at the same time consumes less computational resources and power.

1.4.2.4 Distributed Algorithm Design Challenges

Decentralization of the system architecture requires a paradigm shift from software algorithm perspective, since novel distributed algorithms are required to transform the centralized BMS functions into decentralized. For instance, identifying the topological order of cells in the series string is an important information for both control and maintenance purposes. Compared to the centralized system, where the master controller knows the position of each cell in the battery pack, this information might be difficult to obtain in a fully distributed BMS topology, where each cell has its own individual controller that communicates over a shared bus. Novel approaches for identifying the topological order in a series-connected battery are required compared to [17], where the topological order is obtained using the underlying active cell balancing unit, which might not be possible in certain applications. In addition, the level of monitoring and control

distribution is a key challenge especially in case of partially distributed BMS topology shown in Fig. 1.5c, where both individual cell-level controllers and a master controller are present. Increasing the computations in the cell-level controller requires more computing resources, which needs to be planned in advance and also increases the current consumption from the cell. On the other hand, if all computations are performed by the master controller, it might result in deadline misses or timing violations for certain critical functions. Therefore, an optimum distribution of control is required to maintain the balance between energy consumption from the cell and avoiding deadline misses. Moreover, algorithms used in case of a centralized BMS topology are no longer applicable and a novel methodology is required to transform these centralized BMS functions into distributed algorithms. This transformation gives rise to interesting challenges since the software algorithms must be designed considering the underlying hardware architecture and the communication topology between the individual cell-level controllers.

1.5 Contributions

The contributions of this thesis address the design challenges involved in the cell and balancing levels of distributed BMS topologies explained in Section 1.4.2.1 and 1.4.2.2, respectively. Moreover, the design of the cell-level controller and the modular active cell balancing architectures proposed in this thesis are targeted towards the partially and fully distributed BMS topologies (see Fig. 1.5c and 1.5d), since they cover the largest set of demanding properties.

1.5.1 Cell-level Design

This thesis classifies the functions that are performed in a distributed BMS topology into cell-level and pack-level. Cell-level functions such as sensing, calculating cell SoC, SoH etc., are performed independently by each individual cell-level controllers, without any requirement of communication with other controllers. On the other hand, the pack-level functions such as calculating the pack SoC, power capability, active cell balancing etc., are performed in a distributed fashion by coordination via communication between the individual cell-level controllers. Upon identifying the cell and pack-level functions, this thesis, determines the necessary modules that are required in each individual cell-level controllers, in order to perform these functions in a distributed fashion. Design specifications for each individual module in the cell-level controller are derived satisfying the overall requirements of distributed BMSs.

With the specifications for each module outlined, design choices for individual modules are evaluated and an appropriate option was selected. Implementation of each individual module was performed using commercial off-the-shelf components that are combined in a custom designed Printed Circuit Board (PCB) representing a cell-level controller that can be directly powered from a battery cell. The design of the PCB was focused towards facilitating extensive debugging and obtaining high accuracy measurements. Inputs to each module can be actuated with test signals and their corresponding outputs can be measured separately without involving other modules. This facilitates functional verification of each module and also enables to characterize their performance individually in terms of energy consumption.

The individual cell-level controller boards are combined to form a development platform for distributed BMS topologies. The development platform consists of five series-connected Li-Ion cells along with their individual cell-level controllers. Communication between the individual cell controllers is established using an isolated bus topology through which the functions of a distributed BMS are performed by negotiations between the individual cell controllers. Since the cell level controllers are powered by their respective battery cells, a galvanically isolated communication channel is used to avoid potential short circuits between cells. In addition to the bus-based communication architecture, a daisy chain communication topology between the individual cell-level controllers is also provided. This enables performance comparison of different communication architectures to solve the design challenges in the communication level of distributed BMSs explained in Section 1.4.2.3.

The modular design of the development platform enables easy interfaces with external test equipment and DAQ systems. This facilitates functional verification of different distributed BMS functions and also to obtain high accuracy measurements for model validation purposes. All hardware design files and the firmware of the cell-level controller are uploaded in an online repository [18] and made publicly accessible. This enables easy reproduction of the development platform with minimal integration efforts and facilitate the scientific community in solving the challenges involved in the communication and software algorithm level of distributed BMSs explained in Section 1.4.2.3 and 1.4.2.4, respectively.

1.5.2 Balancing-level Design and Optimization

As discussed in Section 1.4.2.2, decentralization of BMS topology enables efficient implementation of complex active cell balancing approaches. However, existing active cell balancing architectures designed for centralized BMS topology are not suitable for implementation towards distributed BMSs. Therefore, a new class of active cell balancing architectures are required for implementation towards a distributed BMS topology. Towards this perspective, this thesis, derives the guidelines for designing active cell balancing architectures in order to be suitable for distributed BMS topologies.

Design rules of active cell balancing architectures for distributed BMSs are classified into imperative and performance-related design rules. An active cell balancing architecture is suitable for implementation in a distributed BMS only if it satisfies the imperative design requirements. Furthermore, the suitable active cell balancing architectures satisfying the imperative design requirements are evaluated using the performance-related design goals. Based on this design methodology, three different modular active cell balancing architectures are proposed in this thesis and their working principle are explained in detail. All balancing architectures consist of homogeneous units that can be easily integrated with each cell of battery pack. Consequently, with minimal interconnection between the balancing units, a system-level active cell balancing architecture is obtained facilitating charge transfer between cells. In addition to their electrical circuit architecture, control scheme of each active cell balancing for transferring charge between cells are derived and verified using an automated verification framework developed in [15]. Possible charge transfer scenarios of each active cell balancing architecture are explained in detail.

The homogeneous units of the active cell balancing architectures proposed in this thesis are directly controlled by the respective cell-level controller associated with each cell of a battery pack. Isolated gate-drive units are used to isolate the high power MOSFET switches in the active cell balancing architecture from the low power outputs of the cell-level controller. Custom-designed PCB implementation of all proposed active cell balancing architectures are developed using commercial off-the-shelf components. In addition to the balancing part the hardware implementation also consist of monitoring circuitry to measure all relevant parameters pertaining to active cell balancing. Two sets of measurement circuitry are provided with different ground potentials. This allows simultaneous sampling of all relevant parameters by both the individual cell-level controller for feedback control and also using other external DAQ systems such as oscilloscopes or LabVIEW. The hardware implementation can be directly integrated in the distributed BMS development platform discussed in Section 1.5.1 and is used to perform functional verification of the charge transfer capabilities of the proposed active cell balancing architectures. Moreover, with the ability to acquire high accuracy measurements using the hardware implementation accurate validation of the analytical models for the charge transfer process can be performed.

Verifying the system-level functionality and performance evaluation at battery pack level requires multiple instances of the hardware implementation and a complicated laboratory setup. Therefore, minimalistic hardware implementation that can be used to efficiently verify all possible charge transfer scenarios is developed. To analyze the system-level performance of the proposed active cell balancing architectures, a generalized modeling methodology is proposed considering the lower-level circuit details and the losses involved in the parasitic resistances and capacitances present in the circuit components. This generalized model is then adapted to each of the proposed active cell balancing architecture and this enables to calculate their system-level performance. Each part of the analytical model is validated with high accuracy measurements taken from the hardware implementation of the active cell balancing architecture. Using the validated analytical model an algorithm for performing system-level charge transfer simulations is proposed in this thesis.

Using the validated analytical model, optimization approaches for maximizing the energy-efficiency of the active cell balancing architectures with reduced installation space are proposed in this thesis. Components of the active cell balancing architecture (switches and energy storage elements) determine the energy-efficiency and the installation space. Therefore, it is necessary to have optimal choice of circuit components that will provide a higher energy-efficiency at reduced installation space. For this purpose, an efficient design space exploration algorithm is proposed in this thesis using the validated analytical model to identify the optimal choices of circuit components. In addition, for each energy-efficient circuit configuration, their exist an optimal control point of operation that will further improve the energy-efficiency of the equalization process. A case study is performed with commercial variants for each component in the active cell balancing unit using the design space exploration algorithm and Pareto-optimal circuit configurations with energy-efficient control points are identified. A system-level case study performed using the Pareto-optimal design configuration showed that up to $80\,\%$ less energy dissipation could be obtained with optimal circuit configurations operated at energy-efficient control points compared to a random choice of circuit components.

1.6 Publications

1. Swaminathan Narayanaswamy, Sangyoung Park, Sebastian Steinhorst and Samarjit Chakraborty: *Design Automation for Battery Systems*. In Proceedings of International Conference on Computer-Aided Design (ICCAD), 2018.
2. Swaminathan Narayanaswamy, Sangyoung Park, Sebastian Steinhorst and Samarjit Chakraborty: *Multi-Pattern Active Cell Balancing Architecture and Equalization Strategy for Battery Packs*. In Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED), 2018.
3. Alma Pröbstl, Sangyoung Park, Swaminathan Narayanaswamy, Sebastian Steinhorst and Samarjit Chakraborty: *SoH-Aware Active Cell Balancing Strategy for High Power Battery Packs*. In Proceedings of Design, Automation & Test in Europe Conference & Exhibition (DATE), 2018.
4. Alexander Lamprecht, Swaminathan Narayanaswamy and Sebastian Steinhorst: *Improving Fast Charging Efficiency of Reconfigurable Battery Packs*. In Proceedings of Design, Automation & Test in Europe Conference & Exhibition (DATE), 2018.
5. Matthias Kauer, Swaminathan Narayanaswamy, Sebastian Steinhorst and Samarjit Chakraborty: *Rapid Analysis of Active Cell Balancing Circuits*. In IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 36, no. 4, pp. 694-698, 2017.
6. Swaminathan Narayanaswamy, Matthias Kauer, Sebastian Steinhorst, Martin Lukasiewycz and Samarjit Chakraborty: *Modular Active Charge Balancing for Scalable Battery Packs*, In IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 3, pp. 947-987, 2017.
7. Sebastian Steinhorst, Matthias Kauer, Arne Meeuw, Swaminathan Narayanaswamy, Martin Lukasiewycz and Samarjit Chakraborty: *Cyber-Physical Co-Simulation Framework for Smart Cells in Scalable Battery Packs*, In ACM Transactions on Design Automation of Electronic Systems (TODAES), vol. 21, no. 4, pp. 62:1-62:26, 2016.
8. Swaminathan Narayanaswamy, Steffen Schlueter, Sebastian Steinhorst, Martin Lukasiewycz, Samarjit Chakraborty and Harry Ernst Hoster: *On Battery Recovery Effect in Wireless Sensor Nodes*, In ACM Transactions on Design Automation of Electronic Systems (TODAES), vol. 21, no. 4, pp. 60:1-60:25, 2016.
9. Sebastian Steinhorst, Zili Shao, Samarjit Chakraborty, Matthias Kauer, Shuai Li, Martin Lukasiewycz, Swaminathan Narayanaswamy, Muhammad Usman Rafique and Qixin Wang: *Distributed Reconfigurable Battery System Management Architecture*. In Proceedings of 21^{st} Asia and South Pacific Design Automation Conference (ASP-DAC), 2016.
10. Matthias Kauer, Swaminathan Narayanaswamy, Sebastian Steinhorst, Martin Lukasiewycz and Samarjit Chakraborty: *Inductor Optimization for Active Cell Balancing Using Geometric Programming*. In Proceedings of Design, Automation & Test in Europe (DATE), 2015.

11. Matthias Kauer, Swaminathan Narayanaswamy, Sebastian Steinhorst, Martin Lukasiewycz and Samarjit Chakraborty: *Many-to-many Active Cell Balancing Strategy Design*, In Proceedings of 20^{st} Asia and South Pacific Design Automation Conference (ASP-DAC), 2015.
12. Martin Lukasiewycz, Sebastian Steinhorst, Swaminathan Narayanaswamy: *Verification of Balancing Architectures for Modular Batteries*, In Proceedings of International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2014.
13. Sebastian Steinhorst, Martin Lukasiewycz, Swaminathan Narayanaswamy, Matthias Kauer and Samarjit Chakraborty: *Smart cells for Embedded Battery Management*. In Proceedings of International Conference on Cyber-Physical Systems, Networks and Applications (CPSNA), 2014.
14. Swaminathan Narayanaswamy, Sebastian Steinhorst, Martin Lukasiewycz, Matthias Kauer and Samarjit Chakraborty: *Optimal Dimensioning of Active Cell Balancing Architectures*. In Proceedings of Design, Automation & Test in Europe (DATE), 2014.
15. Matthias Kauer, Swaminathan Narayanaswamy, Sebastian Steinhorst, Martin Lukasiewycz and Samarjit Chakraborty: *Modular System-level Architecture for Concurrent Cell Balancing*. In Proceedings of 50^{th} Design Automation Conference (DAC), 2013.

1.7 Organization

The concepts and contributions of this thesis are organized into different chapters as follows. Chapter 2, provides a brief introduction of basic power electronic devices and circuit architectures, that will be extensively used in the remainder of this thesis. Readers familiar with these basic concepts can skip this chapter. In Chapter 3, a detailed analysis of different BMS topologies is provided. Functions and modules required in the cell-level control units of distributed BMSs are identified and their design challenges are discussed. Chapter 4, consolidates the existing literature in cell balancing and derives the design goals of active cell balancing architectures for implementation towards a distributed BMS topology. These two chapters (Chapters 3 and 4) introduce the preliminary concepts in detail and lay the ground work for better understanding of the technical contributions proposed in Chapters 5, 6 and 7, respectively. Moreover, this extended introduction of the basic concepts enables to correctly apprehend the experimental results of the case study performed in Chapter 8 of this thesis. Chapter 5, discusses the generalized modeling methodology of active cell balancing architectures and proposes a system-level simulation algorithm for performance evaluation at battery pack level. Furthermore, using the analytical model optimization approaches for increasing the energy-efficiency of the active cell balancing process are proposed. This thesis proposes three different modular active cell balancing architectures in Chapter 6, satisfying the design requirements of distributed BMS topologies derived in Chapter 4. Working principle, control scheme and possible charge transfer schemes of all proposed balancing architectures are explained in detail. Hardware implementation details of the individual cell-level controller, the proposed active cell balancing architectures and the distributed BMS development platform are presented in Chapter 7. Chapter 8 is the experiments and validation section, where functional verification of the charge transfer capabilities of the proposed active

cell balancing architecture is performed using the hardware implementations. Moreover, the analytical model derived in Chapter 5 are validated with high accuracy measurements made using the hardware implementation. Results of the system-level simulation analysis and the optimization approaches are presented. Finally, in Chapter 9, conclusions and suggestions for future work are provided. Fig. 1.6, shows the organization of the thesis into different chapters along with a short summary of the important points discussed in each chapter.

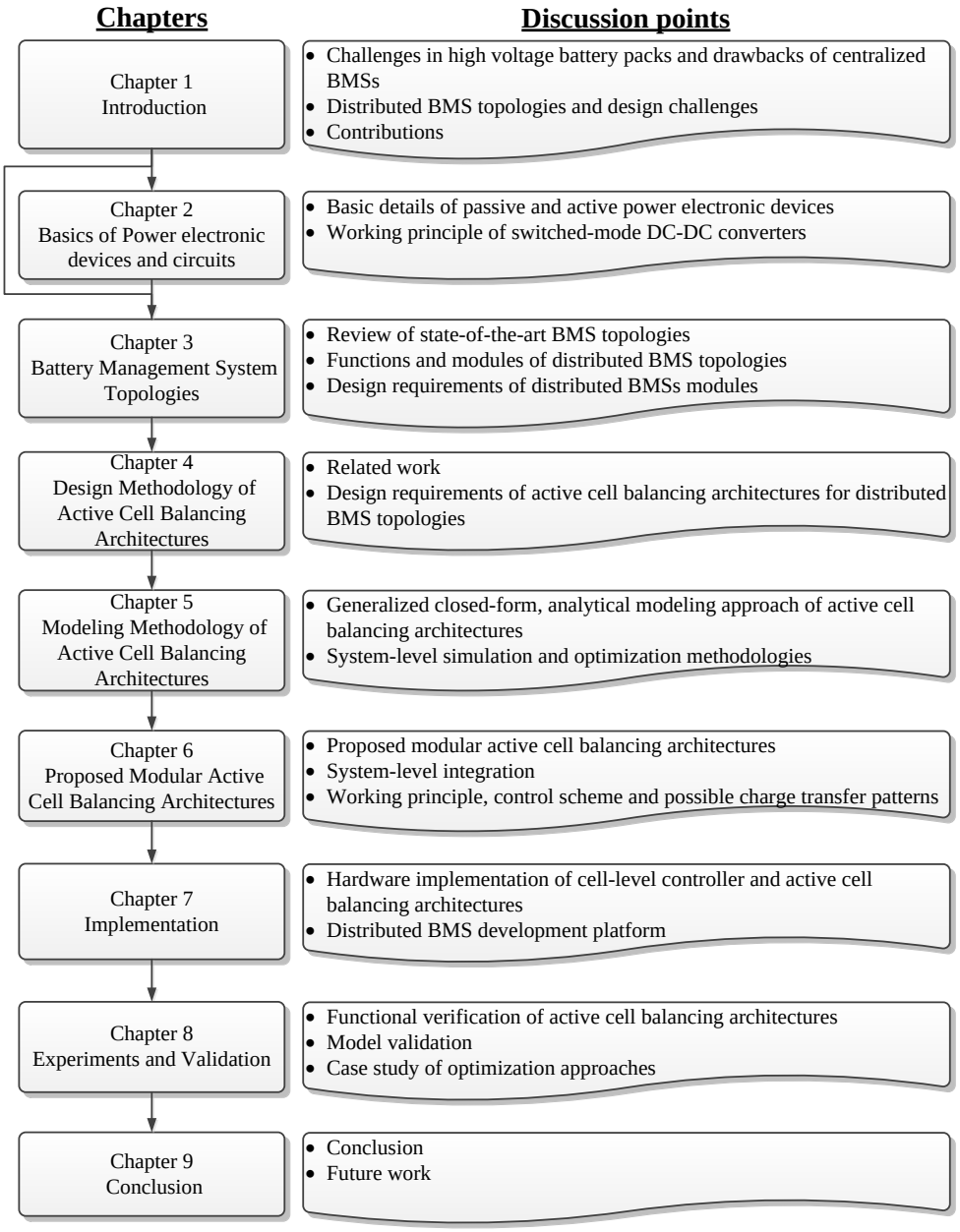


Figure 1.6: Organization of the thesis into different chapters with short summary of points discussed in each chapter.

2

Basics of Power Electronic Devices and Circuits

Transferring charge directly between the series-connected cells of the battery pack is not possible without isolating the main power line due to potential short circuits between cells. Therefore, to equalize the charge level of all cells in a series-connected battery pack, cell balancing using temporary energy storage devices are required. In order to address the balancing-level design challenges associated with the distributed BMS topology explained in Section 1.4.2.2, this thesis proposes several modular active cell balancing architectures in Chapter 6. All proposed modular active cell balancing architectures consist of homogeneous balancing units that exchange charge between the cells through the charge transfer bus as shown in Fig. 2.1. Furthermore, each unit consists of temporary energy storage elements that act as buffers storing charge for a short amount of time and discharge to the respective battery cell in the pack. In addition to the energy storage elements, a switching network formed of power electronic switches is also required to appropriately route the flow of charge from the cell to the energy storage element and vice versa. The active cell balancing circuit architecture formed with the combination of the energy storage elements and the power electronic switches transfers charge between cells based on the working principle of switched-mode DC-DC converters.

In this chapter, different types of power electronic energy storage elements such as inductors, capacitors and transformers along with different power electronic switching devices such as diodes, MOSFETs and Insulated-Gate Bipolar Transistors (IGBTs), which are used in the active cell balancing architectures proposed in this thesis are explained. Moreover, operating principle and features of certain power electronic circuits that are analogous to the working behavior of the active cell balancing architectures proposed in this thesis are briefly outlined. Introduction to these basic concepts facilitates better understanding of the architectures, models and optimization algorithms proposed in this thesis.

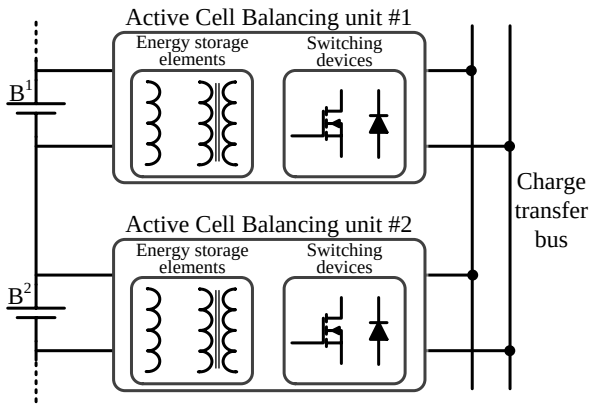


Figure 2.1: System-level active cell balancing architecture consisting of homogeneous modular units exchanging charge over a charge transfer bus. Each unit consists of energy storage elements and switching devices, which operate on the working principle of DC-DC converters.

2.1 Energy Storage Elements

Energy storage element in power electronic circuits are mainly used as temporary buffers for storing energy during a power conversion process. Typically they are of three types, inductors, capacitors and transformers. In this section, a basic overview of each of the energy storage element is provided.

2.1.1 Inductor

Inductors are devices that store electrical energy in the form of magnetic field. They are typically used as energy storage elements in power electronic circuitries that perform AC-DC or DC-DC or DC-AC power conversions. A magnetic flux Φ is generated across a conductor when a current i flows through it and the inductance L of an inductor is defined as the amount of flux created for a given current:

$$L = \frac{\Phi}{i} \tag{2.1}$$

Any current carrying conductor will have a magnetic flux across it and an inductance. But the intensity of the magnetic flux is increased by winding the conductor to a ferromagnetic material such as iron, which is typically called as a core. The current flowing through the conductor can quickly saturate the ferromagnetic core losing the property of inductance. Therefore, typically a small air-gap is provided in an inductor, which stores the electrical energy applied in the form of magnetic flux. According to Faraday's law of induction, a change in the current flowing through the coil induces a change in the magnetic flux which produces a voltage across the coil given by:

$$V = \frac{d\Phi}{dt} = \frac{d(Li)}{dt} = L\frac{di}{dt} \tag{2.2}$$

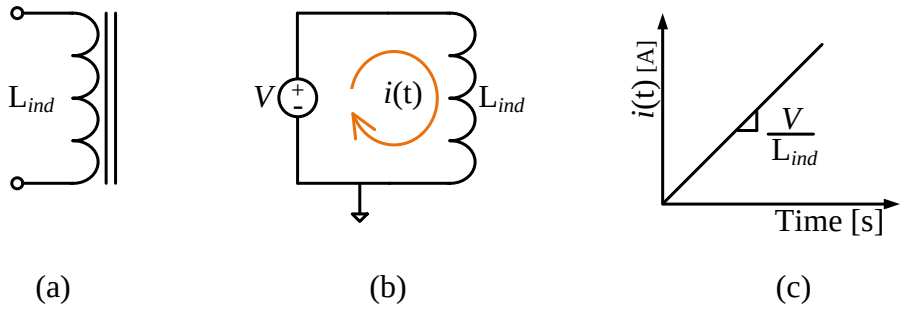


Figure 2.2: (a) Circuit symbol of an inductor. (b) Voltage V applied across an inductor induces a current through the inductor. (c) The current through the inductor increases linearly with a slope of L.

The circuit symbol of an inductor is shown in Fig. 2.2a and the inductance value of the inductor is measured in H, where $1\text{H} = \frac{1\,\text{V s}}{1\,\text{A}}$.

The current through an inductor cannot change simultaneously, while the voltage across it can change instantaneously. If a constant voltage is applied across an inductor as shown in Fig. 2.2b, the current increases in a linear fashion with respect to time as shown in Fig. 2.2c and the slope of the current is inversely proportional to the inductance value of the inductor. Moreover, the applied voltage and the resulting current (I) flowing through an inductor stores an electrical energy in it, which is given by:

$$E = \int_0^I i \cdot L\frac{di}{dt} = L\int_0^I idi = \frac{1}{2}LI^2 \tag{2.3}$$

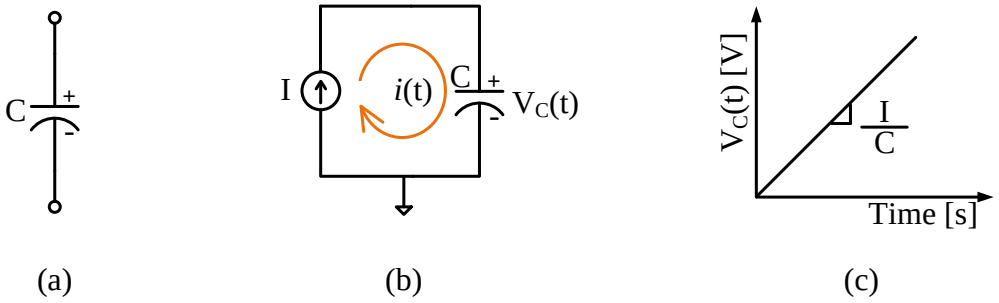
2.1.2 Capacitor

Unlike inductors, capacitors store their energy in the form of electric field. A capacitor consists of two conductive plates that have a dielectric insulator material between them. The capacitance C of a capacitor is measured in F and is given by:

$$C = \frac{\epsilon_r \epsilon_0 \cdot A}{d} \tag{2.4}$$

where ϵ_r is the permitivity of the dielectric material, ϵ_0 is the permitivity of the air, A is the overlapping area of the two conductive plates and d is the separation between the two plates. The electrical symbol of the capacitor is shown in Fig. 2.3a. In contrast to the inductor, where the voltage is a time derivate of current, in capacitors, the voltage is an integral value of the current flowing through it, which is given by:

$$V = \frac{1}{C}\int i(t)dt + V_0 \tag{2.5}$$



(a) (b) (c)

Figure 2.3: (a) Circuit symbol of a capacitor. (b) Current I applied through a capacitor increases its voltage V_C. (c) The voltage across the capacitor increases linearly with the applied current.

where C is the capacitance of the capacitor, V_0 is the initial voltage across the capacitor and i is the current flowing through the capacitor. With a constant current applied across the capacitor as shown in Fig. 2.3b, the voltage of the capacitor increases linearly with time as shown in Fig. 2.3c. Capacitors have the tendency to block DC signals and allow time varying AC signals to pass through them, which finds their application typically as a filter element to smoothen the ripples present in the output of power converters.

Moreover, the current flowing through a capacitor C stores Q amount of charge in it, which is given by:

$$\begin{aligned} \frac{dQ}{dt} &= i \\ dQ &= i \cdot dt \\ \int dQ &= \int C\frac{dV}{dt}dt \\ Q &= CV \end{aligned} \tag{2.6}$$

The energy stored in the capacitor is given by:

$$E = \int_0^V C\frac{dv}{dt}vdt = C\int_0^V vdv = \frac{1}{2}CV^2 \tag{2.7}$$

2.1.3 Transformer

Typically transformers are used in power transmission in an electrical distribution network or used to achieve impedance matching in signal transmission applications. Apart from that, they are also used to provide isolation from input to output in certain power electronic circuits. In this thesis, the energy storage application of the transformer is utilized and therefore the properties related to that are briefly outlined.

A transformer consists of two or more coils wound on a ferromagnetic core. By winding the coils on the same core, a flux generated in one coil due to the flow of current in it, is mutually

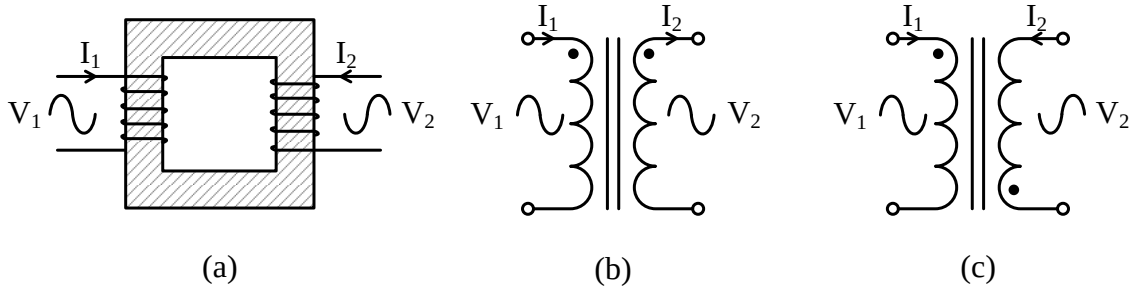


Figure 2.4: (a) Cross-section view of a transformer showing primary and secondary windings. (b) Similar winding directions in both primary and secondary and their dot convention representation. (c) Opposite winding directions between primary and secondary resulting in out of phase voltage and current.

linked to the other coils wound on the core. The mutual linkage mainly depends upon the number of turns (N) of each coil. This mutually linked flux generates a voltage across the coil and an appropriate current flows if the coil is electrically connected to a load device. Fig. 2.4a shows a two-winding transformer wound on a ferromagnetic iron core and its corresponding electrical symbol is shown in Fig. 2.4b. It consists of a primary winding with N_p turns and a secondary winding with N_s turns respectively. A voltage V_1 applied across the primary winding produces a current I_1, which generates a flux Φ in the iron core. The generated flux induces a voltage V_2 across the secondary winding since it is wound on the same core and a current I_2 flows if a load is attached to the secondary winding of the transformer. Therefore, the transformer in general transfers power from one voltage level (primary) to another voltage level (secondary).

In an ideal transformer, the primary and secondary voltages and currents are related to each other by the number of turns as follows.

$$\frac{V_2}{V_1} = \frac{N_s}{N_p} = \frac{I_1}{I_2} = N \tag{2.8}$$

The ratio $\frac{N_s}{N_p}$ is often called as turns ratio N of the transformer. Please note that this thesis adopts the definition of N as the ratio between secondary to primary winding turns to be in line with Simulation Program with Integrated Circuit Emphasis (SPICE) simulations that will be performed in later part of this thesis, whereas, many text books and articles may define N as the ratio between primary and secondary winding turns. A turns ratio $N = 0.1$ means that for each turn of coil in the primary winding there is 0.1 turns in the secondary winding, for example, a transformer having 20 turns of primary winding and $N = 0.1$ will have 2 turns on its secondary winding.

While there are several properties and applications transformers are utilized, this thesis, primarily focuses on using transformer as an energy storage element. Conventional transformers cannot store energy in it since the ferromagnetic core on which the primary and secondary windings are wound does not have an air gap. However, certain transformers have gapped ferromagnetic core to facilitate energy storage and they are primarily used in DC-DC power

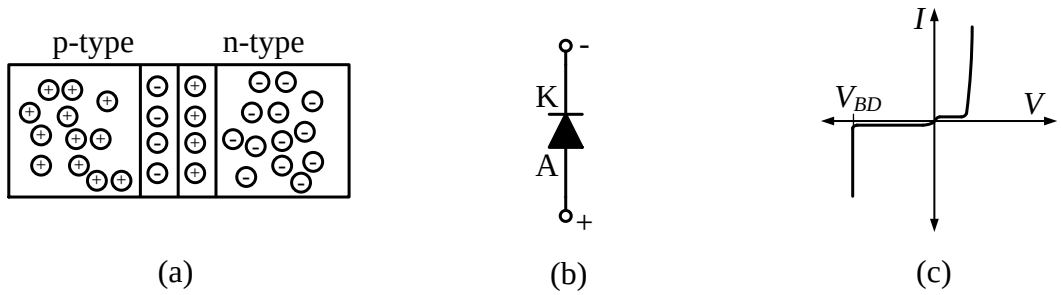


Figure 2.5: (a) Cross section of a power diode showing p-type and n-type semiconductors. (b) Electrical circuit symbol of a power diode. (c) I-V characteristic of a diode showing the increase in current during forward-biased condition and the reverse blocking capability.

conversion, for example in flyback converters. Such transformers with a gapped core are often called as *inductor-transformers*, since their operating principle is closely related to the energy storage property of the inductor with an added benefit of galvanic isolation.

An important property of an inductor-transformer that requires to be explained in order to clearly understand their working principle in later parts of this thesis is the dot convention rule. The dot convention in the electrical symbol of a transformer signifies how the primary and secondary windings are wound on the core. It enables to easily understand the winding polarities of the transformer without looking into the actual construction. If both windings of the transformer are wound in the same direction, that is clockwise or anticlockwise, then the electrical symbol of the transformer will have dots on the primary and secondary winding at the same level as shown in Fig. 2.4b. Consequently, the voltage and the current in both winding will be in phase. On the other hand, if the primary and secondary windings are not wound in the same direction, then their voltages and currents are out of phase and the dots are opposite as shown in Fig. 2.4c.

2.2 Switching Devices

Apart from the energy storage elements, switching devices are an important component of any power electronic converter circuits. While there are many switching devices such as power diodes, power MOSFETs, IGBTs, thyristors, etc. this thesis primarily uses power diodes and power MOSFETs. Therefore, the properties of these devices are explained briefly in this section.

2.2.1 Power Diodes

Power diodes are similar in construction to a normal semiconductor diode having a p-type semiconductor material (positive doped material) fused together with a n-type (negative doped) silicon material as shown in Fig. 2.5a. The prime difference between a power diode and a conventional semiconductor diode is the capability of handling higher currents ($> 1\,\mathrm{A}$). Diodes

are two terminal devices and their electrical circuit symbol is shown in Fig. 2.5b which consist of anode and cathode terminals. They are unidirectional conducting devices meaning the current flows only from anode to cathode when a positive voltage is applied to the anode and conduction in the opposite direction is not possible if the positive voltage is applied to the cathode, until the voltage reaches a certain limit called as break-down voltage. Once this reverse voltage limit is reached, the property of the diode is lost and starts to conduct like a short circuited wire with very low resistance.

With no external voltage, the majority carriers from both P-side and N-side diffuse to form a diffusion barrier. When an external voltage is applied with P-side being positive and N-side being negative, the diode is said to be in forward-biased mode and carries a current once the applied external voltage is higher than the threshold value. The current through the diode is proportional to the applied voltage and is given by

$$I_F = I_S \left[e^{\left(\frac{qV}{kT}\right)} - 1 \right] \tag{2.9}$$

where I_F is the forward-biased current of the diode, I_S is the saturation current, V is the applied voltage, q charge of an electron, k is the Boltzman's constant and T is the temperature. The current flowing through the diode in the forward-biased condition with a voltage V_d across it will result in a power loss given by:

$$P = V_d \cdot I_F \tag{2.10}$$

Now if the applied voltage is in the opposite direction, the diode is said to be in a reverse-biased mode and conducts only small values of leakage current. Operation of the diode in this region is not highly recommended unless the diode is specifically manufactured for that purpose, for example, Schotkky diode. When the reverse-biased voltage is increased beyond a certain value, typically referred to as breakdown voltage V_{BD}, internal destruction of the diode takes place. This breakdown voltage is required to know the voltage blocking capability of the diode in certain power converter applications. Fig. 2.5c shows the I-V characteristic of the diode, where the above explanation is graphically explained. As for this thesis is concerned, individual diode devices are not typically used. However, as will be shown in Section 2.2.2, a power MOSFET switch has an in-built body-diode due to its construction and the operating principle of that body-diode is similar to the normal power diode device explained in this section.

2.2.2 Power MOSFETs

Power MOSFETs are typically used as switching devices in power converters that operate in the range of several kHz to MHz. They are characterized with low *ON*-resistance (R_{DS}) and fast switching speed. A power MOSFET has three terminals *gate* (G), drain (D) and source (S).

Fig 2.6a shows the internal cross section of a power MOSFET device. In the top figure, no external voltage is applied between gate-source and drain-source. The switch is in the *OFF* state and no current flows through it. When a sufficiently high gate-to-source voltage (V_{GS}) is applied to the switch, a conducting channel forms between the drain and source connection as shown in the middle figure in Fig. 2.6a and the switch turns *ON* carrying current, when a sufficient voltage is applied between drain and source terminals (V_{DS}). All power MOSFET switches have

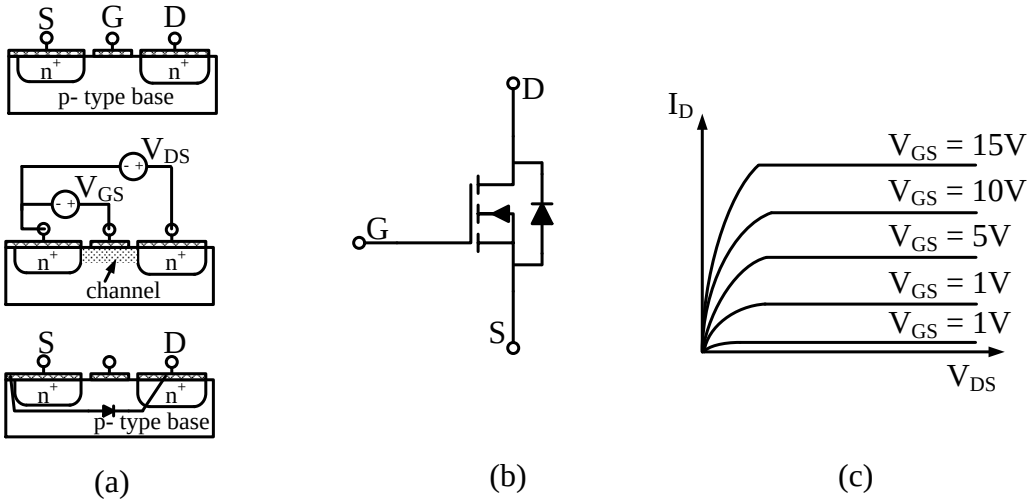


Figure 2.6: Power MOSFET(a) Internal structure, channel formation and parasitic body-diode between drain and source. (b) Electrical circuit symbol of a power MOSFET. (c) Output characteristic of a power MOSFET.

an internal body-diode parallel to the conduction channel by its inherent structure as shown in the bottom figure in Fig. 2.6a. This body-diode comes into conduction when the drain voltage is held negative than the source terminal and carries current in only one direction. Even though the switching times of this body-diode is not very fast, it is generally used in power converters to carry the reverse current.

Fig. 2.6b shows the circuit symbol of a typical N-channel power MOSFET, that is biased with a gate-to-source voltage $V_{\rm GS}$ and drain-to-source voltage $V_{\rm DS}$. Fig. 2.6c shows the I-V characteristic of the N-channel power MOSFET shown in Fig. 2.6b. The drain current ($I_{\rm D}$) is plotted as a function of drain-to-source voltage ($V_{\rm DS}$) for different values of gate-to-source voltages ($V_{\rm GS}$). The conduction channel is formed when $V_{\rm GS}$ exceeds a threshold value $V_{\rm T}$ below which the device is said to be in off state. In the on state, the drain-to-source voltage $V_{\rm DS}$ is roughly proportional to the drain current $I_{\rm D}$. A characteristic feature of the MOSFET when conducting is its drain-to-source ON-resistance ($R_{\rm DS}$). This results in a conduction energy dissipation ($E_{\rm cond}$) when the MOSFET conducts a current $I_{\rm D}$ for time $T_{\rm ON}$ through it and is given by:

$$E_{\rm cond} = I_{\rm D}^2 \cdot R_{\rm DS} \cdot T_{\rm ON} \tag{2.11}$$

In addition, the drain current and the drain-to-source voltage do not change abruptly during the MOSFET switching and therefore results in a certain amount of switching energy dissipation ($E_{\rm sw}$) given by

$$E_{\rm sw} = \frac{1}{2} \cdot I_{\rm D} \cdot V_{\rm DS}\{t_{\rm ON} + t_{\rm OFF}\} + \frac{1}{2} C_{\rm OSS} V_{\rm DS}^2 \tag{2.12}$$

where $t_{\rm ON}$ and $t_{\rm OFF}$ are the times required for the MOSFET to fully conduct the load current once a gate-to-source voltage has applied and the time required for the MOSFET to completely

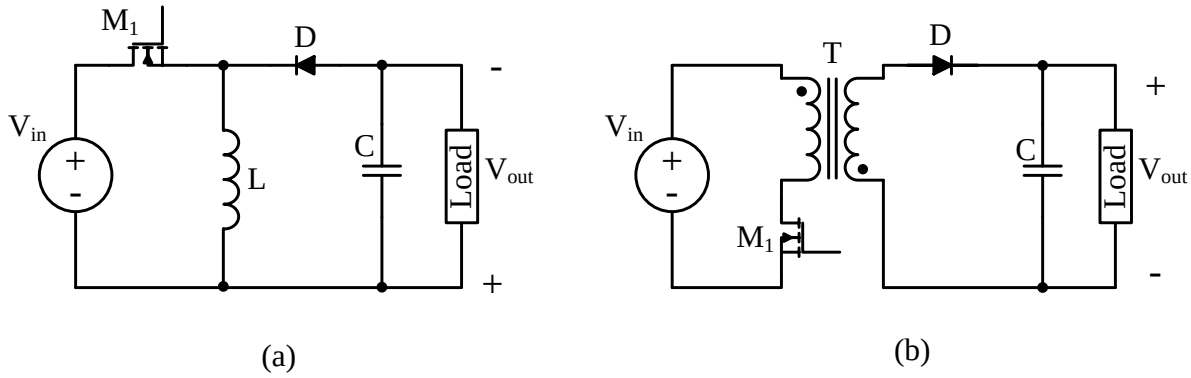


Figure 2.7: Power converter topologies. (a) Buck-boost converter. (b) Flyback type DC-DC converter.

turn off after the gate-to-source voltage is removed, respectively. C_{OSS} is the parasitic output capacitance present between the drain and source terminals of the MOSFET.

2.3 DC-DC Converter

DC-DC converters are a class of power electronic circuits that translate a DC voltage of one level to another. They achieve this by using any one or multiple energy storage devices explained in Section 2.1 in combination with a switching device primarily MOSFET. They are typically used as power supply devices for maintaining a regulated supply voltage in many Integrated Circuit (IC) and embedded system applications. While there are several variants of DC-DC converters available such as buck, boost, forward, SEPIC, Cuk, etc., the active cell balancing architectures that are proposed in this thesis work on the operating principle of buck-boost and flyback type DC-DC converters. Therefore, the operating principle of these two converters are explained briefly in this section.

2.3.1 Buck-boost and Flyback Converter

Buck-boost converters are typically used to obtain a regulated output voltage that can either be lower or higher than the input voltage of the converter. Flyback converters are an isolated version of the buck-boost converter using an inductor-transformer as an energy storage element. Fig. 2.7a and 2.7b shows the typical circuit diagram of the buck-boost and flyback type DC-DC converters topologies, respectively. Operating principle of the buck-boost DC-DC converter is explained in the following. The flyback converter also operates on a similar working principle with the difference being the energy storage element is a transformer instead of an inductor.

Working principle. The operation of the buck-boost type DC-DC converter is divided into two phases, *ON*, top figure of Fig. 2.8a and *OFF*, bottom figure of Fig. 2.8a. The switching process

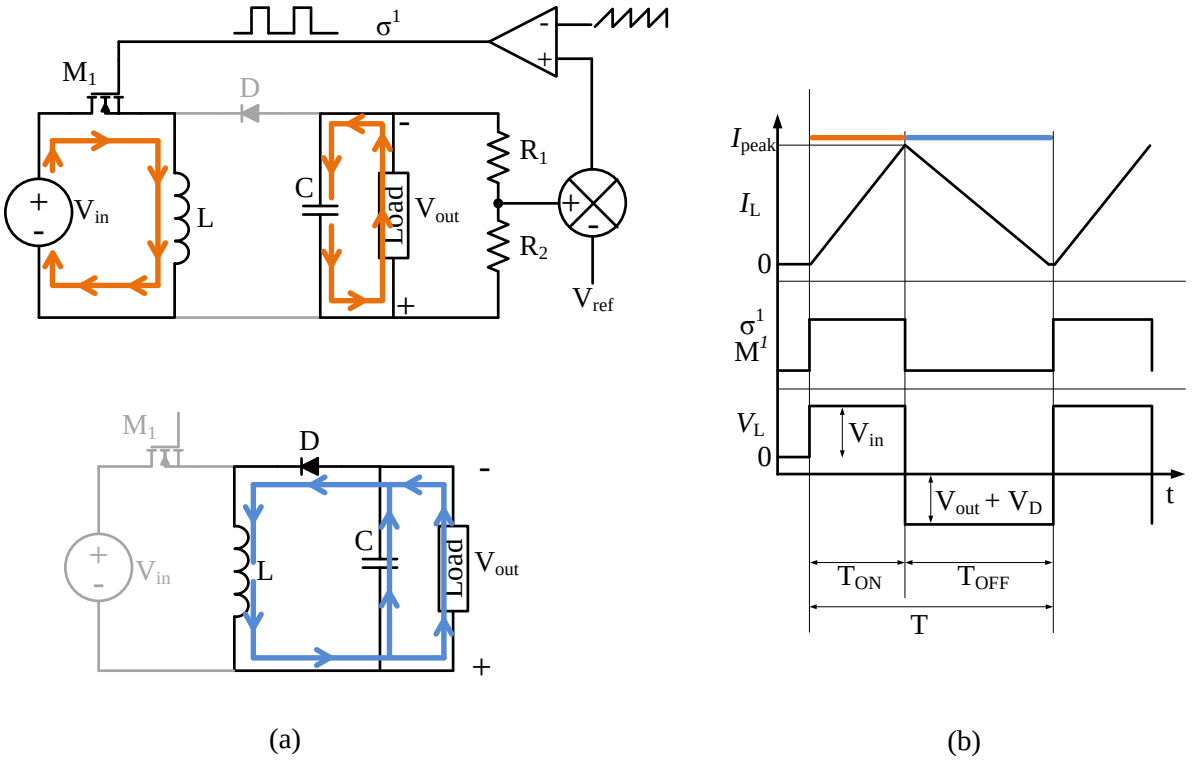


Figure 2.8: Operating principle of buck-boost type DC-DC converter. (a) Two phases of operation and the current flow directions. Part of the circuit that are not utilized are grayed out for better visibility. (b) PWM control signal σ^1 along with the corresponding inductor current and the inductor voltage.

is controlled using a Pulse Width Modulated (PWM) signal σ^1 as shown in Fig. 2.8b. During the *ON* phase, MOSFET M^1 is actuated with the PWM signal σ^1 and the inductor L is charged from the input voltage source V_{in}. The current through the inductor I_{L} increases linearly with the input voltage as shown in Fig. 2.8b. During this phase, diode D is reverse-biased and does not conduct any current. The output voltage is maintained by the filter capacitor C as shown in Fig. 2.8a.

When the MOSFET switch is turned *OFF* after a certain time period T_{ON}, the inductor is disconnected from the input source. As explained in Section 2.1.1, the current through the inductor cannot be interrupted and as a result the voltage across the inductor changes polarity to maintain the flow of inductor current. This change in polarity forward-biases diode D and the inductor starts to discharge the stored energy during the *ON* phase into the load and at the same time charges the output capacitor C as shown in the bottom part of Fig. 2.8a. Output voltage V_{out} is monitored through a resistor-divider network formed by R^1 and R^2 as shown in Fig. 2.8a. This is compared with the desired output voltage (V_{ref}) value in the error amplifier A^1. The error between the output and the desired value is then compared with a triangular signal in Q^1

to generate the desired PWM signal σ^1 for actuating MOSFET M^1. Fig. 2.8b shows the PWM signal σ^1, the inductor current I_{L} and the inductor voltage V_{L} of the buck-boost converter.

2.4 Summary

This chapter provided the fundamental concepts of the energy storage elements and power electronic components that will be extensively used in this thesis. Moreover, operating principles of common DC-DC converter topologies which are used in the active cell balancing architectures proposed in this thesis are explained.

3 Battery Management System Topologies

BMS is a monitoring and controlling system that maintains the battery pack within its safe operating limits and improves its usable capacity by equalizing the charge levels of individual cells in the battery pack. In this chapter, a brief overview of different BMS topologies that are existing in the literature are analyzed. In contrast to the centralized BMSs, distributed BMSs are emerging and their individual variants are explained in detail. Different cell-level and pack-level functions performed in distributed BMS topologies are outlined in Section 3.2.4. Modules that are required in each individual cell-level controller to perform these functions are identified. In Section 3.3, challenges and requirements for each module are discussed and their possible options of implementation are explained.

3.1 Centralized BMS Topology

A centralized BMS topology as discussed in [12] is shown in Fig. 3.1. Here sensors for measuring the voltage, temperature of each individual cell of the battery pack are wired directly to the central master controller. A single current sensor for measuring the pack current is sufficient since all cells are connected in series and the same current flows through all of them. All computations and control decisions of the BMS are performed in the central controller instance. The prime advantage of this topology is its reduced cost, since only a single controller is required to monitor and control all series-connected cells in the battery pack. This approach might be suitable for smaller battery packs consisting of fewer number of cell, however, there are challenges to implement such a centralized system in case of a large battery pack consisting of 100s of series-connected cells typically found in EV applications. For each application, the BMS has to be planned in advance considering the mechanical and electrical interconnections in the battery pack, which leads to an increased time to market of the application. Moreover, the complexity of the system is vastly increased due to the huge amount of wiring involved with connecting

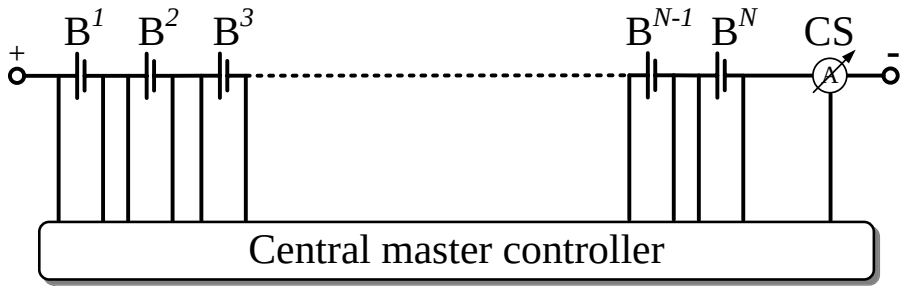


Figure 3.1: Centralized BMS topology, where a single master controller monitors and maintains the parameters of individual cells in a series-connected battery pack.

the individual cell sensor to the master controller. This also increases the probability of failure and thereby reducing the reliability of the system. In addition, all complex high frequency control signals required for active cell balancing has to be generated and distributed from the master controller which makes it challenging to implement. Due to the growing complexity of battery packs with increasing number of cells and the necessity to reduce the time to market, it is therefore beneficial to distribute the hardware and software architectures of the BMS into different abstraction levels as will be explained in the following section.

3.2 Distributed BMS Topologies

Distributed BMSs are an emerging alternative compared to the centralized BMS topologies. A hierarchical BMS topology is proposed in [13] which will be explained in Section 3.2.1, followed by partially decentralized BMSs proposed in [19] and [20] in Section 3.2.2. Section 3.2.3 presents a fully distributed BMS topology that was presented in [21].

3.2.1 Hierarchical BMS

Fig. 3.2 shows a hierarchical BMS topology as proposed in [13]. Here a set of 8 t o 12 cells are grouped to form a module and each module is controlled by a dedicated Module Management Unit (MMU). The MMUs of each module consists of monitoring circuits for cell voltages and temperature of individual cells within the module. Typically, the monitoring part in the MMU has a single Analog to Digital Converter (ADC) and sensors from each cell in the module are alternatively connected to it through a high voltage multiplexer [22]. The MMUs are powered directly from the module of cells and they also control the cell balancing process between cells within the module. All MMUs in the battery pack are controlled by a central Pack Management Unit (PMU) as shown in Fig. 3.2. The MMUs communicate to the PMU through a galvanically-isolated Controller Area Network (CAN) bus and communication between the PMU and other control units of the application is established with an external CAN bus. The PMU reads the data regarding each individual cell from the MMU and calculates the cell states such as SoC, SoH etc. Moreover, the PMU decides the cell balancing pairs for equalization and communicates

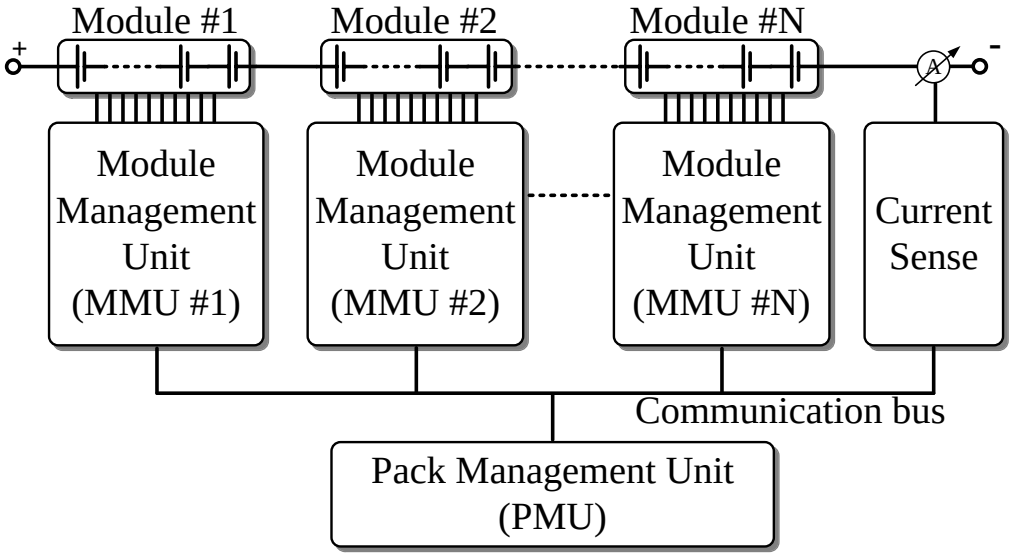


Figure 3.2: Hierarchical BMS topology, where 6 to 8 cells are grouped into a module and monitored with a dedicated MMU and all MMUs are in turn controlled by a single PMU.

this information to the respective MMUs. Subsequently, balancing process is initiated by the corresponding MMUs in order to equalize the charge levels of cells in the pack.

Compared to the centralized BMS topology, wiring harness and complexity is reduced in the hierarchical BMS topology due to the introduction of module controllers. The MMUs can be located closely to their corresponding module in order to minimize the wiring between individual cell sensors to the MMU. Moreover, the communication between MMUs and the PMU is via a shared galvanic bus, further reducing the required wiring harness. However, their exist certain challenges with this approach. Full architectural scalability and modularity is not achieved with this BMS topology, since the MMUs are designed only based on the inputs of number of cells in the module. Their PCB design is affected by the mechanical orientation of the cell module, since the MMUs have to be placed near to the module to reduce the wiring from cells. In terms of reliability, the hierarchical BMS topology performs slightly better than the centralized BMS topology. A break in the sensor to MMU wiring or if any one of the MMU fails, then only that module needs to be isolated from the series string of the battery pack. Moreover, adding new cells to the pack at a later stage of design might be difficult in a hierarchical BMS topology if the MMU is saturated in its controlling capability and in such cases an addition of a single cell will require a new MMU resulting in a higher cost and installation volume.

3.2.2 Partially Distributed BMS

Fig. 3.3a, shows the topology of a partially distributed BMS proposed in [19] and [20]. Here each cell of the battery pack is equipped with a local control unit that is powered from the battery cell and maintains the parameters of the cell within safe operating limits. All cell-level control

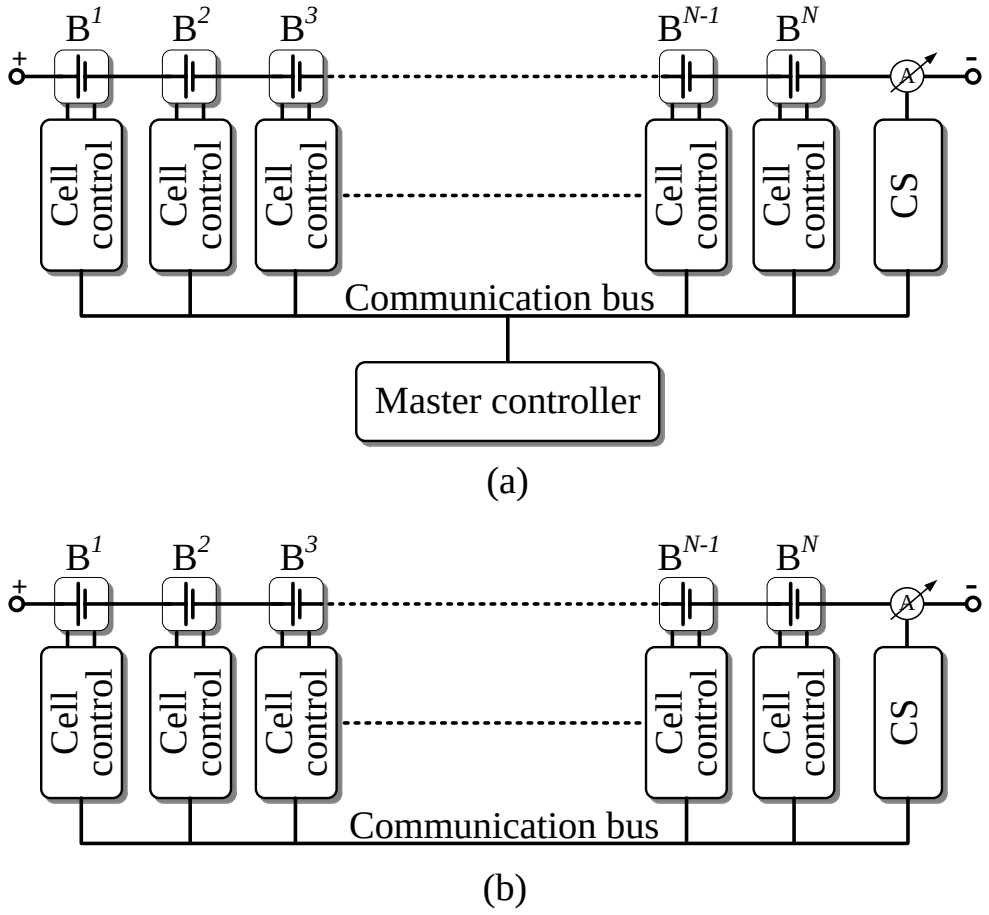


Figure 3.3: (a) Partially distributed BMS topology. (b) Fully distributed BMS topology (*Smart cells*).

units are connected to a central master as shown in Fig. 3.3a, which is similar to the PMU in hierarchical BMSs. All pack-level parameters such as battery pack SoC or SoH are calculated in this central master instance. By brining the monitoring and controlling functionality close to the cell, improved safety is obtained. Moreover, the reliability of the system is increased by minimizing the potential chances of single point of failure. Malfunctioning of an individual cell-level control unit will result in non-availability of a single cell compared to hierarchical BMS where a fault in the MMU results in the failure of an entire module consisting of 8 cells.

3.2.3 Fully Distributed BMS (*Smart cells*)

A fully decentralized BMS topology as proposed in [21] is shown in Fig. 3.3b. Modular, intelligent Cell Management Unit (CMU) in each battery cell monitors and maintains the local parameters of the associated cell within the safe operating limits. The CMU consists of sensing and computation circuitry for accurately calculating the cell states such as SoC, SoH, etc.

			INPUT								
			CELL						PACK		
			Voltage	Temperature	SoC	SoH	Resistance	Balancing current	Pack current	SoC	SoH
OUTPUT	CELL	Calculate: SoC* $\in \mathbb{R}$	✓	✓				✓	✓		
		Calculate: SoH* $\in \mathbb{R}$	✓	✓			✓				
		Calculate: Resistance* $\in \mathbb{R}$	✓						✓		
		Detect: Fault $\in \{0, 1\}$	✓	✓	✓	✓			✓		
		Detect: Over charge or discharge $\in \{0, 1\}$	✓		✓						
	PACK	Calculate: SoC*{min, max} $\in \{\mathbb{R}$x$\mathbb{R}\}$			✓						
		Calculate: SoH* $\in \mathbb{R}$				✓					
		Perform: Balancing $\in \{0, 1\}$	✓		✓			✓		✓	
		Calculate: {max Power, max Time} $\in \mathbb{R}$x$\mathbb{R}$	✓	✓	✓	✓			✓	✓	✓

Table 3.1: Cell-level and pack-level functions of a distributed BMS topology. Inputs specified in the columns are used to calculate cell and pack-level outputs mentioned in the rows. Output of certain functions that are marked with * are used as inputs for calculations in other functions.

Moreover, it also facilitates local generation of complex high frequency control signals that are required for performing charge transfers and therefore enables an efficient implementation of sophisticated balancing architectures. The cell along with the CMU is termed as a *smart cell* and the network of battery pack is formed by interconnection of multiple smart cells in series. Consequently, all system-level functions of battery management are performed in a fully distributed fashion through coordination via communication between smart cells, without requiring a central master controller instance.

3.2.4 Distributed BMS Functions

Table 3.1 provides a comprehensive list of functions that are performed at both cell-level and pack-level in a distributed BMS topology. Inputs to the functions are specified in the columns and the functions along with their outputs are specified in the rows of the table.

Cell-level functions. Cell-level functions are implemented in their respective local control units since these functions are independent of other cells, meaning the status and parameters of other cells in the battery pack are not required to be communicated to implement these cell-level

functions. The inputs required for each function calculation is marked with ✓ along the respective columns in Table 3.1. For example, the function that calculates the SoC of the individual cell requires the cell voltage, temperature, balancing current and pack current as inputs. For calculating the individual cell SoC, the local controller does not require data from other cells in the battery pack. Similar explanation holds for other cell-level functions such as calculation of SoH and resistance, detection of fault, over charge and over discharge conditions. Depending upon the application requirement these functions are executed in a periodic fashion with a definite time interval or as an event driven process, happening once after a certain event has occurred. For example, the voltage sensing, resistance calculation, SoC estimation are executed in a periodic fashion in the local controller, whereas, the fault detection and over charge or over discharge control functions are executed once their corresponding events occur.

Pack-level functions. In contrast to cell-level functions that are independently implemented in each cell-level control unit, pack-level functions are realized in a distributed fashion. Here all individual cell controllers collectively exchange their cell data through the communication channel, to compute the pack parameters in a cooperative manner. They can either be a measured parameter such as voltage, temperature etc. or a computed result of a certain cell-level function such as SoC, SoH etc. Outputs of such cell-level functions that are in turn used as inputs for calculating battery pack-level parameters are marked with a * in Table 3.1. For example, to calculate the minimum and maximum SoC of the battery pack, the individual SoC of each cell has to be communicated to other cells through the communication channel. Depending upon the topology of the communication channel, bus or daisy-chain, the information exchange could either be repeated broadcast messages by each cell or multiple neighbor-only data exchanges, respectively. Cells that have the minimum and maximum SoC compared to other cells represent the minimum and maximum SoC of the battery pack.

3.3 Distributed BMS Modules

Distributed BMSs as explained in Section 3.2.2 have individual cell-level control units that monitor and maintain the parameters of the associated cell within their safe operating limits. Compared to the partially distributed BMS topology shown in Fig. 3.3a, the fully distributed smart cell topology does not have a central master controller as shown in Fig. 3.3b. Nevertheless, the electrical architecture of the cell-level control units of both topologies are identical, with the only difference of having a higher computation power in each cell-level control units in the case of *Smart cells* compared to the partially distributed BMS topology The necessary modules that are required in each cell-level control units of distributed BMS topologies for performing both the cell and pack-level functions described in Table 3.1 is shown in Fig. 3.4 and are explained below.

- **Sensing:** The sensing module is used to measure the cell parameters such as cell voltage, temperature, balancing current and pack current, which are used as inputs for calculating the cell and pack-level functions of the BMS.

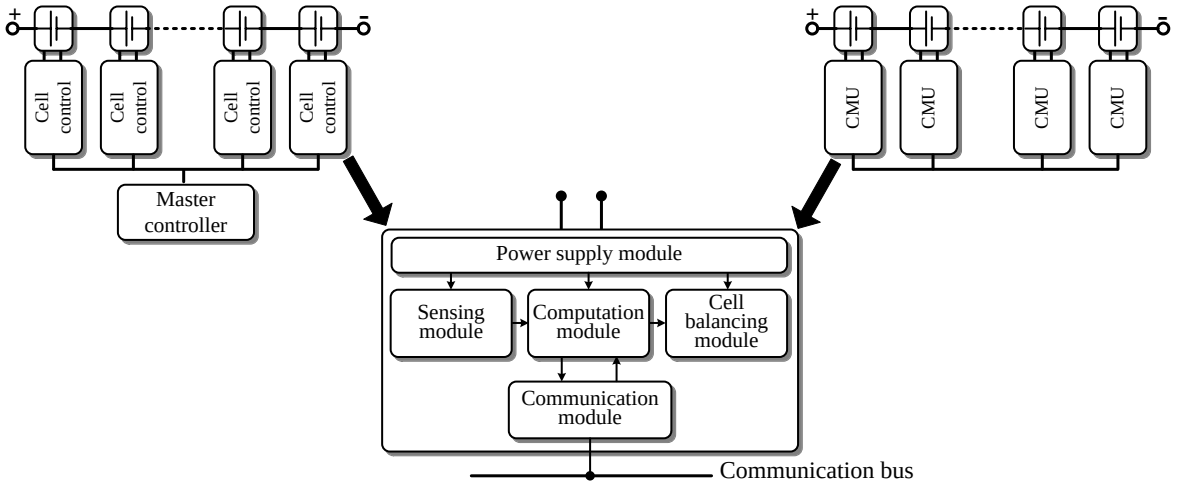


Figure 3.4: Necessary modules in each cell-level control unit of distributed BMS topologies.

- **Computation:** The computation module implements all the cell-level and pack-level functions of the distributed BMS topologies. It takes the measured parameters from the sensing module as inputs for calculating the cell-level functions and the pack-level functions are performed by communicating with other cell-level controllers.

- **Communication:** Data exchange between the individual cell-level controllers or to the master controller is facilitated by the communication module.

- **Cell balancing:** Equalization of individual cell capacities is performed by the cell balancing module to improve the usable capacity of the battery pack.

- **Power supply:** Power supply module provides a constant regulated supply voltage, which is required for efficient functioning of other modules in the cell-level controller unit.

Requirements and design challenges for individual module and their existing possible implementation options are discussed in detail in the following sections.

3.3.1 Sensing Module

The parameters such as voltage, temperature, balancing current and pack current are required to be accurately measured by the cell-level control unit for maintaining safe operation conditions of the battery pack. The required specifications and state-of-the-art approaches for measuring these parameters are explained below.

3.3.1.1 Voltage measurement

The BMS must measure the terminal voltage across each series-connected cell to protect them from being over charged or over discharged. Accurate measurement of cell voltage enables to calculate the cell states such as SoC, SoH, etc.

Challenges and requirements. As shown in Fig. 1.2, battery packs for high voltage applications such as EVs, HEVs etc., consist of multiple series-connected modules, in which each module has cells connected in parallel and series depending upon the required capacity and voltage of the application. The parallel-connected cells are electrically indistinguishable since their terminal voltages are identical, however, the DC voltage level of each series-connected cell varies with respect to the negative terminal of the battery pack. For instance, the voltage across the terminals of cell B^{N-1} in Fig. 3.3a is $4\,\mathrm{V}$ and $8\,\mathrm{V}$ with respect to the negative terminal of the battery pack, whereas, cell B^1 has $396\,\mathrm{V}$ and $400\,\mathrm{V}$ across its terminals with respect to the negative terminal of the battery pack.

The varying DC potentials across the cells in the battery pack makes accurate sensing of the cell potential a challenging task. A high-level of common-mode noise is induced due to this variation in the DC potential of the cells when they are connected in series. The sensing module has to cope with this common-mode noise potential to accurately measure the cell voltage. In addition, since cell-level controllers in the distributed BMSs are powered directly from the monitoring cell itself, the ground potential of the sensing circuitry is not a fixed reference value. Instead the ground potential varies during operation of the battery pack and this results in measurement inaccuracies which the sensing module has to overcome for accurate measurements. Moreover, Li-Ion cells exhibit an extremely flat voltage profile within the usable SoC range of $80\,\%$ to $20\,\%$. Therefore, high resolution measurements in the range of $1\,\mathrm{mV}$ are required to accurately calculate the SoC and SoH of the cell.

Existing approaches. Many methods for measuring the cell potential in a series-connected battery pack are discussed in the literature. For instance, [23] uses resistor-divider network across each cell for measuring the individual cell voltages. Even though this method is cost effective and easier to implement, they suffer from measurement inaccuracies induced by the variation in the resistances due to temperature. Moreover, huge values of high-precision resistors are required to minimize the current through them. Another approach proposed in [24] uses huge mechanical relays for individually measuring the cell potential in a series-connected battery pack. The installation space and cost of this implementation approach is significantly increased due to the bulky relays required for each cell of the battery pack. Alternatively, measuring the voltage of each cell with an isolation amplifier as proposed in [25], requires an additional isolated, high voltage power supply which increases the cost of the system and also the energy consumption from the cell. Cell voltage measurement with operational amplifier as proposed in [26], consists of individual amplifiers that monitor the cell voltages for a module of cells in series. However, for individual cell voltage measurement, the design of the operational amplifier must contain high Common-Mode Rejection Ratio (CMRR) since the power supply voltage from a single cell will be much less compared to a module of series-connected cells. Direct measurement of cell voltages by using an individual ADC for each cell as proposed in [20], provides accurate results and also favors towards on-chip integration.

3.3.1.2 Temperature measurement

Measuring cell temperature is extremely important to maintain safety and improve the performance of the Li-Ion cell. The temperature data is also used by the applications HVAC control unit for maintaining the required operating temperature of the battery pack.

Challenges and requirements. Temperature variation affects the usable capacity obtained from Li-Ion cells. Even though increasing the temperature speeds up the rate of electrochemical reactions inside the cell, resulting in a higher output capacity, temperatures beyond the safety limit will damage the cell and possibly result in fire or explosion due to thermal runaway. Moreover, fast charging (charging with a higher current), especially in the case of EV batteries results in increased temperature fluctuations within the cell and requires high accuracy monitoring and control of the cell temperature to ensure safety of the battery pack. Multiple temperature sensors are required specially for the case of large format pouch cells, where the temperature distribution over the cell surface is non-uniform and therefore, has higher probability of generating localized hot spots. Moreover, temperature profiling of the cell at different current values enables to obtain a heat map explaining the potential hot spots in the cell and also provides an idea for placement of the temperature sensors. In addition, it is also required to closely monitor the inner temperature of the cell, since there exists a certain time delay for the heat generated inside the cell to be sensed at the surface [27]. Varying temperature distribution along the battery pack will result in non-uniform aging of cells and cause imbalances in their capacity. This requires accurate monitoring of temperature over the entire battery pack in order to maintain uniform aging of all cells.

Existing approaches. Several cell temperature measurement techniques are available in literature as explained in [28]. Temperature sensors such as Resistance Temperature Detector (RTD), thermocouples or thermistors are widely used for measuring the surface temperature of the cell [29]. Thermistors and RTD sensors work on the principle that their resistance changes with respect to temperature and measuring the change in resistance helps to calculate the surface temperature of the cell. On the other hand, thermocouple sensors produce a voltage proportional to the temperature that has to be measured. Currently thermistor sensors are most widely used for measuring the surface temperature of the cell due to their simplicity in design and cheaper manufacturing costs [30]. In this context, [31] provides design and implementation details of a monitoring module that can measure up to 12 thermistor sensors with low-power consumption. Alternatively, for measuring the inner temperatures of the cell, special custom made sensors are required that can be attached into the cell during the production phase. In [32–35], special in-situ RTD type temperature measurement sensors are fabricated that can be attached into the inner surface of the cell during the manufacturing phase and the temperature data can be read by the cell-level controllers using methods proposed in [36] and [37]. For measuring the output of both RTD and thermistor type sensors, whose resistance changes according to the temperature, a resistor-divider network is required, where the change in resistance of the sensor will result in an equivalent change in voltage that can be measured using an ADC.

3.3.1.3 Current measurement

Accurate measurement of battery pack current enables to calculate the SoC and SoH values of each cell. In addition to the battery pack current flowing equally in all cells, individual balancing currents per each cell are also required to be monitored for accurate control of cell balancing.

Challenges and requirements. Balancing and the battery pack load currents are the two variables that are required to be measured by the current measurement module. Based on the SoC distribution of the battery pack, the balancing currents of each cell varies. Therefore, each cell requires a dedicated balancing current measurement unit. In addition, depending upon the type of balancing method employed i.e., either passive or active, the measurement requirements of the balancing current changes. For instance, in case of passive balancing approaches, the balancing current is constant and does not require sophisticated high frequency measurements. However, the currents in an active balancing network, changes at very high frequency and therefore close monitoring of the balancing current at a higher sampling rate is required to prevent damage of the components involved in the balancing network. In contrast to the individual balancing current, the battery pack load current is of higher orders of magnitude and is same for all cells, since they are connected in series. Therefore, one high accurate, low-noise, pack current measurement sensor for the entire series-connected battery pack is sufficient. Moreover, for measuring pack currents with very high resolution, dual-range current sensors are employed, where one sensor monitors pack current at a higher range and the other one measures at a lower range.

Existing approaches. A detailed review of different current measurement techniques in automotive applications is provided in [38]. Current transformers [39], which are capable of measuring only AC currents and magneto-resistive sensors [40], which suffer from poor temperature stability and low measurement range are not suitable for battery pack current measurements. In case of balancing current measurement, shunt or series sense resistor techniques are widely used. Here a small value of resistance is placed in series to the measurement current path and the voltage developed across it is directly proportional to the current flowing in the circuit. This technique is suitable for measuring low to medium current values and therefore it is widely used in both passive and active cell balancing approaches. On the other hand, for measuring the battery pack current, which is of higher orders of magnitude than the individual balancing currents, hall effect sensors [41] are typically used. They provide good accuracy and linearity for a wide range of current values.

3.3.2 Computation Module

Computation module is the main processing unit, where the cell and pack-level functions of a distributed BMS listed in Table 3.1 are implemented. Cell parameters such as voltage, temperature, balancing current and pack current that are measured by the sensing module are taken as inputs by the computation module for calculating the cell-level functions. In addition, pack-level BMS functions are computed by communication with other cell-level controllers.

Challenges and requirements. Since the individual cell-level control units are powered directly from the associated cell, low-power processing is the main design objective of the computational module. Power management techniques such as Dynamic Power Management (DPM), Dynamic Voltage and Frequency Scaling (DVFS) etc., are required to be implemented in order to minimize the power consumption from the cell. Moreover, depending upon the application requirement, real-time, high-speed processing is also required, to process hundreds of messages received through the communication channel within a short time frame. Safety-critical applications such as EVs and HEVs, demand additional safety certifications, requiring multi-core computational units performing the same task to ensure system reliability.

In terms of computational requirement, the individual cell-level controllers must be capable of performing high accuracy calculations involving matrix multiplications, divisions and inversions. For instance, to accurately estimate the SoC of a cell [42–44], sophisticated models of the Li-Ion cell are required to be implemented in the computational unit of the individual cell-level controllers. Moreover, the controlling part of the computation module must interact with the cell balancing module to control the switches in the balancing network for charge transfer. For this purpose, several PWM timer modules are needed which can generate complex high frequency control signals that are required for actuating the switches in the active cell balancing module.

Existing approaches. The choice of the computation unit purely depends upon the size and accuracy requirement of the battery pack. For example, a 16-bit Micro Controller Unit (MCU) core could be sufficient for small and medium sized applications such as laptops or electric bikes [45]. However, large volume battery packs consisting of 100's of Li-Ion cells connected in series, require additional computations and safety certifications. Therefore, a computationally powerful, 32-bit, tri-core processors were used [13], in which each function is calculated independently by each core and the combined result is used as the output. In certain situations, Application Specific Integrated Circuits (ASICs) [46], were also developed which combines the required circuit blocks into a single IC thereby reducing the installation space.

3.3.3 Communication Module

Communication between the cell-level controllers and to the master controller is the key for performing the pack-level functions of a distributed BMS topology listed in Table 3.1.

Challenges and requirements. Any fault or out of specification operation of a given cell has to be notified to other cell-level controllers in the battery pack. For this purpose, the communication channel must be reliable and fast allowing broadcast messages. Moreover, to form a battery pack using individual cells associated with localized control units, that from outside, behaves like a conventional battery pack, all cells must know their topological position along the series string. Specifically in the case of the fully distributed *smart cell* topology, without a central master controller, the individual cells must be capable of *self organizing* themselves in the battery pack with a unique ID denoting their position in the series string. For this purpose, the communication channel must also enable self-organization of cells in the battery pack by exchanging their position along the series string, when other hardware methods of neighbor-

identification such as in [17] are not available. Since the individual cell-level controllers are powered directly from their respective battery cells and due to the varying DC potential of each cell in a series-connected battery pack, proper galvanically isolated communication interface is required to avoid short circuits. Therefore, a robust, noise free and reliable communication architecture with minimum wiring harness is required for a distributed BMS topology in order to achieve minimum integration efforts.

Existing approaches. For battery packs with fewer number of cells, a galvanically isolated daisy chain communication topology such as in [47] is sufficient. However, this becomes inefficient if the number of cells in the battery pack increases and if most communication messages are broadcasts. Therefore, a galvanically isolated bus-based communication topology such as in [48], is required for high power battery packs. Alternatively, using the DC power-line cable of the battery pack for communication reduces the amount of wiring compared to the bus or daisy chain communication topologies [49]. However, they suffer from noise in the power-line of the battery pack due to the varying DC potential levels and the fast changing load currents. Approaches using wireless communication [50] are unpredictable in the noisy battery pack environment and are difficult to implement when the battery pack is tightly sealed. Alternatively capacitively coupled data transmission systems as proposed in [51] and [52] can also be considered for applications that require bandwidths in the range of certain kbps.

3.3.4 Cell Balancing Module

The usable capacity of a battery pack and its lifetime is significantly affected by the variation in SoC of individual cells caused by manufacturing differences and varying temperature distribution along the battery pack. Since all cells are connected the charging and discharging thresholds of the battery pack are determined by cells with the highest and lowest SoCs, respectively. As soon as a cell reaches the bottom SoC threshold value the discharging process has to be stopped even though other cells in the battery pack may have active energy stored in them. Similar condition applies during the charging case where any cell reaching the top SoC threshold value stops the charging process even if other cells in the series chain are not fully charged. Repeated charging and discharging of such an unbalanced battery pack results in an unusable battery with certain cells that have active energy stored in them. Therefore, cell balancing is required to increase the usable capacity of the battery pack by equalizing the SoC of individual cells.

Challenges and requirements. Compared to passive balancing approaches, active cell balancing techniques are energy-efficient since the excess charge in cells are redistributed instead of dissipating and are therefore more favorable. The prime requirements of an active cell balancing module to be implemented in a distributed BMS topology are scalability and localized control scheme. The cell balancing module must consist of homogeneous modular blocks that are fixed in design and can be mass produced. The individual balancing modules must be controlled independently by their respective control units, without any requirement for a high frequency synchronization with other cell controllers. Moreover, a simple control scheme reduces the computational effort and minimizes the power consumption from the cell. In addition to being

modular, active cell balancing architectures must provide increased charge transfer capabilities with reduced number of hardware components and control complexity.

Existing approaches. A comprehensive overview of different active cell balancing techniques is provided in [53]. They are classified into inductor-based, capacitor-based and transformer-based approaches depending upon the type of energy storage element used to transfer the excess charge between cells. The capacitor-based active cell balancing architectures such as in [54] and [55] are slow and suffer from the fixed energy loss involved in charging the capacitor directly from the battery cell. On the other hand, multi-winding transformer-based architectures as proposed in [56] and [57] are expensive, require a large installation space and cannot be modularized into individual homogeneous units. By contrast, the inductor-based active cell balancing architectures [15] and [58], are energy-efficient than the capacitor-based approaches and require reduced installation volume compared to transformer-based active cell balancing architectures.

3.3.5 Power Supply Module

Power required for efficient operation of all modules in the cell-level controller is obtained from the power supply module. As explained before, the operating voltage of a Li-Ion cell varies from $4{,}2\,\mathrm{V}$, when it is fully charged, to $2{,}5\,\mathrm{V}$, when it is fully discharged. Even though some modules in the individual cell-level controllers can operate directly with this variation in the cell voltage, other modules require a constant regulated supply for their operation. For instance, the sensing module requires a constant regulated supply voltage to accurately measure the parameters of the cell. In addition, a higher operating supply voltage compared to the terminal voltage of the cell is required for functioning of other modules (cell balancing and communication) in the cell-level controllers. Moreover, powering the computation unit with a constant regulated supply voltage, increases the runtime obtained from the cell compared to directly operating from the cell as shown in [59].

Challenges and requirements. Since the individual cell-level controllers are powered from the respective battery cell itself, low-power consumption is the important goal of a power supply module. In addition, the power supply module must provide the required operating voltage and current for each individual module in the cell-level controller. Furthermore, the power supply module must facilitate the implementation of power management techniques such as DPM, DVFS in order to minimize the power consumption from the battery cell. Moreover, quiescent current drawn from the cell should be minimum in order not to drain the associated battery cell. Therefore, a power supply module providing a low-noise, ripple-free regulated supply voltage is required for efficient functioning of other modules in the cell-level control unit.

Existing approaches. Low Dropout Regulators (LDOs) [60] as a direct power supply from the battery cell is not possible since they can only provide a regulated output that is lower than their input voltage. Moreover, they are energy-inefficient if the difference between the output and input voltage is high. By contrast, switched-mode DC-DC converters using inductors, capacitors or

transformers provide an output voltage both higher or lower than their input voltage [61]. Charge pump based switched-mode DC-DC converters [62] using capacitors to boost the cell voltage, occupy less installation space than their inductor and transformer based counterparts. However, they are limited by their maximum output current capability, which for certain modules in the cell-level controller might not be sufficient. Even though the switched-mode DC-DC converters using transformers [63] have a high output current capability and provide good isolation, their huge size increases the required installation space. On the other hand, the inductor-based, switched-mode DC-DC converters have higher output current capability than charge pumps and occupy reduced installation volume compared to transformer-based approaches. Apart from the type of energy storage elements, the switched-mode DC-DC converters are classified into three basic topologies such as buck (output voltage less than input voltage), boost (output voltage higher than input voltage) and buck-boost (output voltage higher or lower than input voltage).

3.3.6 SoC Estimation

SoC of a cell is defined as the ratio of capacity left in the cell to the capacity of the cell when it is fully charged. It is expressed as a percentage value with $100\,\%$ signifying the cell is fully charged and $0\,\%$ signifies that the cell is empty. SoC estimation is an important task performed by a BMS in order to know the remaining capacity that is left in the pack and how long the pack can continue to provide before it has to be charged. Moreover, accurately estimating the SoC of the cell is necessary to perform active cell balancing, where the charge level of cells are equalized based on their SoC value. In this section, challenges and requirements of accurately estimating the SoC of a cell and of pack in case of a distributed BMS topology is explained in detail. Moreover, existing approaches in the literature for calculating the SoC of the cell are outlined.

Challenges and requirements. Accurate estimation of cell SoC is important to calculate the remaining capacity left in the pack and to perform active cell balancing. For estimating the SoC of individual cells, the cell-level controller in the distributed BMS requires to measure the cell voltage, current (both pack and balancing) and temperature of the cell. These measurements are then used as inputs for a complex model that calculates the SoC of the cell at each time instant. Depending upon the accuracy requirements of the application the complexity of the estimation technique might vary. For instance in low-power applications such as laptops, cell phones, where only fewer number of cells are connected in series, a simple voltage-SoC look-up table might be sufficient for calculating the SoC of the cell. However, for high power and range critical applications such as EVs, HEVs the estimation method will be very complex, involving either coulomb counting, Kalman filtering, extended Kalman filtering, etc. For these applications, the computation module in the cell-level controller of the distributed BMS needs to have a higher computational capability for performing complex mathematical tasks such as matrix multiplication, addition, inversion etc.

Apart from the individual cell SoCs, accurately calculating the pack SoC is also important, since it determines the usable capacity of the battery pack and the driving range that is possible in terms of EV applications. The battery pack SoC is the SoC of cell that is lowest

among all other cells in the series chain. In case of distributed BMSs, where each cell-level controller is capable of only measuring the SoC of associated cell, the pack SoC is computed in a distributed fashion by communication with other cell-level controllers. Naive approach would be each cell-level controller periodically broadcasting the SoC of its associated cell to all other cell-level controllers over the CAN bus. This however, increases both the energy consumption from each cell and also might lead to high level of bus utilization preventing other communication messages from accessing the bus. Intelligent approaches would consider using the neighbor-only communication topology where only the minimum SoC is propagated to the cell-level controllers and in the end the computed pack SoC could be broadcast to all cell-level controllers in the pack. This minimizes the bus utilization and also the energy consumption from the individual cells in the pack. In addition to minimizing the communication payload and energy consumption, the periodicity of estimating the pack SoC is also a crucial aspect to be considered. Slow updates might lead to overestimation of driving range and in some cases might also be catastrophic. On the other hand, a very high periodic updates might consume a lot of energy from all cells and over usage of the communication bus. Moreover, the update period of SoC must also depend upon the current that is drawn from the pack and this has to be real time.

Existing approaches. A detailed overview of several methods of SoC estimation is presented in [64]. The most reliable and simple method for SoC estimation is the discharge test method, which calculates SoC based on a discharge test performed under controlled conditions. However, this is only suitable during initial testing and maintenance times as it is very time consuming. Moreover, it also requires the cell to be removed out of the battery pack [64], which might not be suitable for real-time monitoring and control. Another method uses the integral value of current flowing in and out of the cell to calculate the SoC of the cell known as coulomb counting. Here, the SoC of a cell could be calculated by integrating the current (discharging or charging) over a specified amount of time and adding it with a known initial SoC value. However, measurement errors due to integration and the self-discharge effects of the cell reduces the accuracy of SoC estimation using coulomb counting [65]. Another method of estimating SoC is by means of calculating the Open Circuit Voltage (OCV) of the cell. The SoC of a cell depends upon its OCV and could be calculated using a look-up table. Although, this method is simple and easy to implement, it requires sufficient rest periods between discharge or charge activity, because of the voltage drop developed due to the internal resistance of the cell and therefore, makes it less attractive for continuous monitoring [66]. Fuzzy logic estimations and artificial neural networks for calculating the cell SoC as proposed in [67] and [68], respectively require extensive training data and in particular the data should be from a similar cell chemistry. Analysis and design of the Extended Kalman Filter (EKF) is presented in a series of three papers [42], [43] and [44], where [42] discusses the requirements of the complex methods, [43] proposes a cell model for the EKF algorithm and finally in [44] the proposed EKF method is used to estimate the SoC.

3.4 Summary

A sophisticated BMS is required for monitoring and maintaining safe operating conditions of a Li-Ion battery pack. There exists a clear trend towards decentralization of the BMS topology,

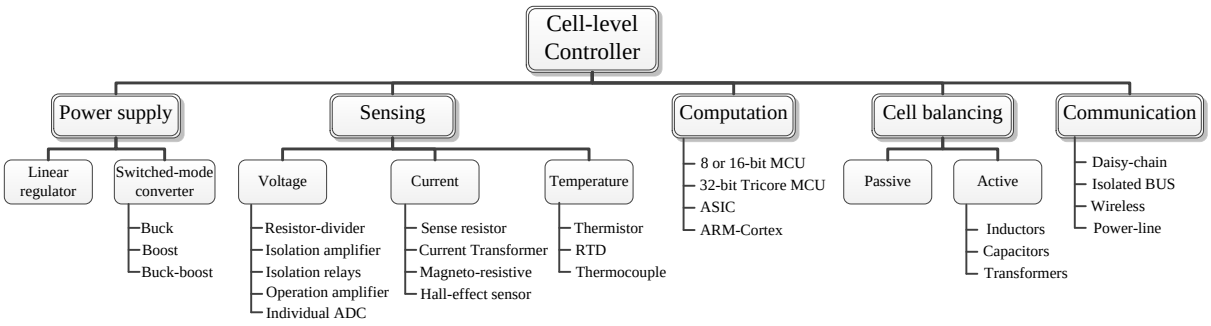


Figure 3.5: Different modules in the individual cell-level control unit and their possible choices of implementation.

which provides significant advantages in terms of higher modularity, reduced wiring complexity, increased safety and reduced integration efforts. In this Chapter, required modules in the cell-level controller of a distributed BMS are identified depending upon the typical functions that are performed on both cell-level and pack-level. Fig. 3.5 summarizes the different modules in the individual cell-level controllers and their existing implementation choices discussed so far in this section. Design challenges and required specifications of each module were discussed in detail along with their existing options. Methods for calculating the SoC of a cell, which is required for performing active cell balancing was also discussed. Later in Chapter 7, implementation details of each module in the cell-level controller is explained in detail.

4

Design Methodology for Active Cell Balancing Architectures

Cell balancing methodology can be broadly classified into either *passive* or *active*. A detailed overview of different existing balancing architectures is provided in Section 4.1. Moreover, the design requirements for cell balancing architectures to be suitable for implementation in a distributed BMS topology are derived in Section 4.2. Based on these design requirements, three novel active cell balancing architectures are proposed in Chapter 6.

4.1 Related Work

In this section, a detailed overview of existing cell balancing approaches is provided and are classified based on the type of the energy storage element used and their charge transfer scenario. A comprehensive overview of existing balancing techniques is provided in [53], [69], [70] and [71]. The process of cell balancing is broadly classified into *passive* and *active* as shown in Fig. 4.1. Furthermore, the *active* balancing approaches are divided into inductor-based, capacitor-based and transformer-based, depending upon the type of energy storage element used to equalize the SoC of individual cells. In addition, the *active* cell balancing architectures are further classified into cell-to-cell, cell-to-pack, pack-to-cell and cell to/from pack topologies, depending upon their charge transfer scenarios.

4.1.1 Passive Cell Balancing

Passive cell balancing involves dissipation of excess energy of an over charged cell across a high power resistor until the SoCs of all cells in the pack are equal. In this approach each cell is attached with a fixed high-power resistor in series with a switch or relay. During charging,

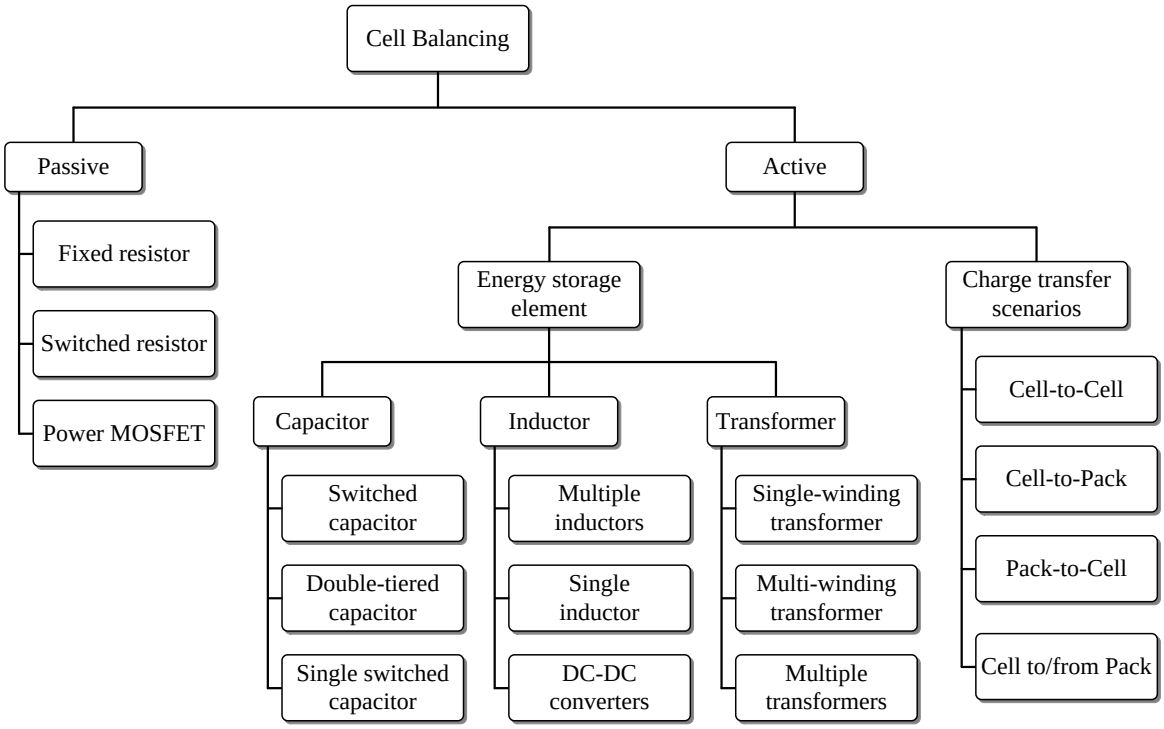


Figure 4.1: Types of cell balancing approaches.

stronger cells that are with a higher SoC value, are discharged through the resistor, such that all cells in the pack attain the top threshold at the same point of time. Since the excess charge is dissipated across the resistor, this approach is fully energy-inefficient and therefore can only be useful during the charging process of the battery pack. The prime advantage of this technique is its ease of implementation and low cost due to reduced number of components. Therefore, it can be used to equalize small volume battery packs such as in E-bikes or laptops. However, the major disadvantage of the passive cell balancing approach is its energy dissipation, especially for range critical applications such as EVs or HEVs that focus to fully utilize the stored capacity of the battery pack. With all charge dissipated across the resistor, the passive balancing approach has an energy-efficiency of $0\,\%$. Passive cell balancing can be implemented by either using a fixed-resistor in series with a switch or relay as proposed in [72] or by using a power MOSFET switch operated in linear-mode as the discharge resistor, see [73].

4.1.2 Active Cell Balancing

In contrast to the energy-inefficient passive balancing approach explained in the previous section, active cell balancing approaches increase the energy-efficiency of the equalization process and thereby improve the usable capacity of the battery pack. Active cell balancing involves transfer of the excess charge from cell(s) with a higher SoC to cell(s) with a lower SoC by using energy storage elements and switches described in Chapter 2. As a result active cell balancing approaches can be used during both charging and discharging process of the battery

pack. Even though the number of components and cost of the system is increased compared to passive balancing approaches, active equalization techniques provide significantly higher energy-efficiency. Active cell balancing approaches are classified depending upon the type of energy storage element used to perform the charge transfer as:

- Capacitor-based
- Inductor-based and
- Transformer-based

4.1.2.1 Capacitor-based Active Cell Balancing

Capacitor-based active cell balancing techniques, use capacitors as an energy storage element to transfer charge from an overcharged cell(s) to an undercharged cell(s). In first step, the balancing capacitor is connected to the cell that has a higher SoC. The balancing capacitor is charged from the cell till its voltage is equal to that of the battery cell. Once fully charged, the balancing capacitor is now connected across the cell with a low SoC. Due to the difference in the voltage, the charge stored in the balancing capacitor is transferred to the cell. By repeatedly connecting and disconnecting the balancing capacitor, charge from cells with high SoC values are transferred to cells with a low SoC value.

No closed loop control is required for maintaining the balancing current, since it is dependent upon the voltage difference between the cell and the capacitor. Therefore, simple control strategy is the key advantage of the capacitor-based balancing architectures. Moreover, the balancing capacitors are small in size and thereby occupy a reduced installation space. However, charging the capacitor directly from a voltage source, such as battery, involves an inherent energy dissipation of $50\,\%$ of the total charge across the parasitic series resistances. Therefore, the capacitor-based approaches can only attain a maximum efficiency of $50\,\%$. Moreover, the speed of equalization is dramatically decreased, especially towards the end of balancing process. Due to progressive equalization, over time, the voltage difference between the strong and weak cell becomes very less. Since the balancing current flowing into the capacitor is proportional to this voltage difference, the speed of balancing is significantly reduced in the capacitor-based approaches. The capacitor based balancing technique can be implemented in three types as

- **Switched Capacitor [54]**: $N-1$ capacitors and $2N$ switches are used to balance a battery pack of N cells. Modular architecture and easier implementation are the key advantages, which otherwise suffers from longer equalization time, since charge transfer can only happen between adjacent cells of the battery pack.
- **Double-tiered switched capacitor [74] and [75]**: With two-levels of capacitors involved, the double-tiered approach is capable of transferring charge between non-adjacent cells. By sacrificing the modularity of the system, the double-tiered switched capacitor technique, reduces the balancing time to quarter compared to that of the switched capacitor balancing approach.

- **Single switched capacitor [76]**: In this method only a single capacitor is used as energy transfer element and each cell is accompanied with a switch network to connect and disconnect the cell with the capacitor. Direct transfer of charge between non-adjacent cells makes this method much faster than both the switched capacitor and double-tiered capacitor balancing system. The disadvantage is that the architecture is not modular and increased number of wires from the switching circuitry to the balancing capacitor.

4.1.2.2 Inductor-based Active Cell Balancing

As the name suggest, this method of active cell balancing involves inductor as its energy storage element. Compared to capacitor-based approaches, which can only attain a maximum of $50\,\%$ energy-efficiency due to charging from the voltage source, inductors can achieve higher energy-efficiencies. Moreover, it is possible to use higher balancing currents with reduced size of inductors, which in turn translates to a lower installation volume. Therefore, the active cell balancing architectures proposed in this thesis are either based on inductors or transformers. The working principle of inductor-based active cell balancing architectures are explained in Chapter 6. Even though the inductor-based approaches are energy-efficient compared to the capacitor-based balancing techniques, they require a highly accurate control scheme to avoid potential short circuits between cells. Moreover, the higher stress involved in the power MOSFET switches in an inductor-based active cell balancing architecture, requires special type of components and increases the cost of the system. Furthermore, operating at very high frequencies, in order to reduce the installation volume, will induce unwanted spikes in the inductor current each time during switching that will affect the Electro-Magnetic Interference (EMI) regulations of the battery pack. Nevertheless, these constraints can be overcome by intelligent design choices, optimized component values, control algorithm and equalization strategies. Therefore inductor-based balancing architectures are more utilized in state-of-the-art approaches compared to other active cell balancing architectures that are based on capacitors and transformers. Existing inductor-based balancing methods are broadly classified into:

- **Multiple inductors [77]**: Being modular with each module consisting of an inductor and two power MOSFET switches, this architecture can be produced in large quantities due to its homogeneity. However, this approach can only transfer charge to their neighboring cells in the pack, reducing the energy-efficiency when the imbalanced cells in the battery pack are farther away in the series-string.

- **Single inductor [78]**: Compared to [77], which uses one inductor per cell module, the balancing architecture proposed in [78] uses a single inductor for the entire pack and has a complex switching network that selectively connects the source and destination cell to the balancing inductor. Even though less number of components are required, this architecture is not modular since each cell module is not homogeneous and also leads to longer equalization time due to lack of concurrent charge transfers between cells.

- **DC-DC converters [79] and [80]**: By using established switched-mode DC-DC converter topologies such as buck-boost, Cuk, etc. for active cell balancing, SoC equalization of

individual cells can be achieved. Increased control complexity is the prime disadvantage of these approaches which make them less attractive for active cell balancing applications.

4.1.2.3 Transformer-based Active Cell Balancing

Typically transformers are either used to obtain isolation or to step-up or down the voltage level in an application. In addition to providing isolation, the transformers in active cell balancing applications are used to store charge from a higher SoC cell(s) and transfer it to cell(s) with lower SoC. Therefore, the construction of these transformers are different compared to the normal transformers used in AC-AC or AC-DC power conversion applications. A typical transformer as explained in Section 2.1.3, cannot store energy in it. Therefore, a small air-gap in the ferromagnetic core of the transformer is provided, which facilitate the device to store charge in the core material. Such transformers are typically referred to as *inductor-transformers*. Most transformer-based active cell balancing approaches work on the operating principle of flyback type DC-DC converters, which will be explained in Chapter 6. Proper isolation ensuring safety of the balancing process and fast equalization speed are the key advantages of transformer-based active cell balancing approaches. However, their size and increased weight remains a challenge to be addressed for modular implementation. Existing transformer-based active balancing architectures can be classified into three types as follows:

- **Single-winding transformer [81] and [82]**: Similar to the single-inductor architecture, this approach uses a single transformer as an energy storage element and employs a switching network to connect the cells that are required to be balanced. Advantages include reduced cost since only a single transformer is required, however, the lack of modularity and concurrency make this approach not suitable for distributed BMS topologies.

- **Multi-winding transformer [83]**: In this method, the primary winding of a custom-made transformer is connected to a module consisting of 8 to 12 cells and the secondary winding is connected to each individual cells. This method can perform faster equalization than the single-winding approach, since it can perform multiple charge transfers simultaneously. However, the major issue with this approach is the custom-made, multi-winding transformer itself, which significantly increases the implementation cost. Moreover, the scalability is a critical issue with this approach, since the single primary winding can only accommodate a maximum of up to 12 cells, beyond which special type of switching MOSFETs are required.

- **Multiple transformers [84]**: In contrast to the single-winding and multi-winding approaches, here, each cell in the module is associated with an individual transformer. The primary of all transformers are connected to their respective cells and their secondary winding is connected across the entire module. Charge can be taken out of single cell and distributed to the entire module and vice versa. Similar to the multi-winding approach, this architecture is also limited to a module of 12 cells thereby lacking scalability for equalization of an entire battery pack.

4.1.3 Classification based on charge transfer scenarios

Apart from categorizing active cell balancing architectures based on the type of energy storage element used, they are also classified based on their charge transfer scenarios as:

- Cell-to-cell
- Cell-to-pack
- Pack-to-cell
- Cell to/from pack

A good overview of these different charge transfer topologies is provided in [85] and [86].

4.1.3.1 Cell-to-cell

Balancing architectures proposed in [77], [54] and [79] fall under this charge transfer topology. Here, charge is transferred from a single source cell to a single destination cell in the battery pack. According to [85], this charge transfer topology provides higher energy-efficiency than other topologies, since the difference in cell voltage between the input and output of the balancing architecture is small compared to other scenarios.

4.1.3.2 Cell-to-pack

Charge from a single source cell is transferred to a module of 8 to 12 series-connected cells. This method of charge transfer might be beneficial during charging of the battery pack, where a single cell with higher SoC can prematurely stop the charging process and quickly distributing its excess charge to other cells enables to fully charge the battery pack. Balancing architectures such as in [87] and [88] fall under the cell to pack charge transfer topology.

4.1.3.3 Pack-to-cell

In the case of pack-to-cell topologies, charge from a module of cells is transferred to a single cell. In contrast to the cell-to-pack topologies, the pack-to-cell charge transfer topology, can be typically used during the discharging process of the battery pack. The discharging threshold is determined by the weak cell in the pack and by transferring charge from the entire module of cells to the weak cell, its SoC is significantly increased.

4.1.3.4 Cell to/from Pack

This is the combination of both cell-to-pack and pack-to-cell topologies, where the charge can be transferred in both directions, from a single cell to the module of cell or vice versa. The associated balancing module is considered bi-directional and overcomes both the individual cell to pack and pack to cell topologies. For instance, [89] and [57] proposes balancing architectures that consist of individual bi-directional active cell balancing units, that can transfer charge from single cell to the module or vice versa.

4.2 Design Requirements for Active Cell Balancing Architectures

Even though their exist certain number of balancing architectures in the literature, not all of them are suitable for implementation towards distributed BMSs. However, they can be employed for a centralized BMSs. For this purpose, this section explains the design requirements for an active cell balancing architecture to be considered as suitable for distributed BMS topologies. Based on these design requirements, three modular active cell balancing architectures are proposed in Chapter 6 of this thesis. The design requirements for active cell balancing architectures to be suitable for distributed BMSs are classified into two types as:

- Imperative design requirements
- Performance-related design requirements

4.2.1 Imperative Design Requirements

The imperative design requirements are the mandatory conditions a balancing architecture must satisfy in order to be suitable for distributed BMS topologies. Further balancing architectures that satisfy these design requirements are then evaluated based on the performance-related design requirements that will be explained in Section 4.2.2. The imperative design requirements of active cell balancing architectures for distributed BMSs are:

- Modularity: Active cell balancing architectures must contain homogeneous modular units enabling easy integration at cell level
- Localized control: Control signals for actuating the switches in each balancing unit must be generated by their respective controllers without a need for high frequency synchronization with other modules.

4.2.1.1 Modularity

As explained in Section 3.2.2, the key advantage of the distributed BMS topology is its modular architecture. Each cell has a homogeneous cell-level intelligent control unit attached to it and the battery pack is formed by interconnecting these individual cells in series. This homogeneity of the hardware and software modules of the cell-level control units provides architectural flexibility enabling battery packs for different capacity and power requirements be easily formed by interconnecting the standardized cell modules without requiring a full redevelopment of the entire BMS for each different application. Therefore, for any balancing architecture to be suitable for distributed BMSs it must contain modular, homogeneous balancing units that can be easily attached to each individual cell of the battery pack. Consequently, these individual balancing units must be capable of being interconnected to form a system-level balancing architecture for an entire battery pack, in order to keep the low integration efforts promised by distributed BMS topologies. As a result, balancing architectures that cannot be modularized into identical units are not applicable for distributed BMSs, even though they might be suitable for a centralized BMS topology.

4.2.1.2 Localized Control

Each active cell balancing architecture consists of an energy storage element and certain number of power MOSFET switches. Depending upon the control scheme of the balancing architecture, one or more switches are required to be actuated with high frequency control signals. Moreover, for certain balancing architectures it is mandatory to have accurate time synchronization between these high frequency control signals in order to avoid potential short circuits between cells. With the trend towards decentralization of the BMS topologies, generation of these complex control signals became feasible, since each cell has its own intelligent control unit. However, in a distributed BMS topology as explained in Section 3.2.2, all individual cell-level control units interact with each other through the common communication channel. Implementing time synchronization between the individual controllers in a distributed BMS topology over the shared communication bus is highly inefficient and increases the energy consumption of the controller that is powered from the cell. Therefore, it is essential to have a synchronization-free control scheme for the active cell balancing architectures, such that all necessary high frequency control signals are generated independently from their respective cell-level control units without requiring synchronization between them.

4.2.2 Performance-related Design Goals

The performance-related design goals are used to evaluate the balancing architectures that satisfy the above mentioned imperative design requirements. The performance-related design goals that evaluate the suitable balancing architectures for distributed BMS topologies are:

- **Non-neighbor balancing:** Ability to transfer charge directly between non-adjacent cells in a battery pack.
- **Percentage of concurrency:** Percentage of simultaneous charge transfers between cells in a pack.
- **Total number of switches:** Total count of MOSFET switches in each individual balancing unit.
- **Number of high frequency switches:** The number of MOSFETs that are actuated by high frequency control signals.
- **Number of high frequency control signals:** Number of high frequency control signals required for a single charge transfer cycle.
- **Charge transfer scenarios:** Different charge transfer scenarios enabled by the balancing architecture.

4.2.2.1 Non-neighbor balancing

Due to uneven temperature distribution along the battery pack, cells that are closer to the cooling inlet will have a higher SoC and cells that are farther away will have a lower SoC. This creates an

imbalanced conditioned between cells that are not adjacent in the series string of the battery pack. Therefore, transferring charge directly between the non-neighboring cells, is always beneficial in terms of energy-efficiency, instead of shuttling the excess charge through all intermediate cells of the charge transfer pair. This is due to the fact that each charge transfer activity using a balancing architecture involves a certain amount of loss, introduced by the parasitic resistances and capacitances that are present in the circuit components. By shuttling the excess charge through all the intermediate cells, we increase the number of charge transfer activity and therefore the energy-efficiency of the balancing process is decreased. Moreover, by performing direct non-neighbor charge transfers, the lifetime of battery pack is also increased, due to the reduced charge/discharge cycles of the intermediate cells, which are not required to be involved in the equalization process. Therefore, in order to increase the efficiency and preserve the lifetime of the battery pack, an active cell balancing architecture must be capable of performing direct non-neighbor charge transfers between cells.

4.2.2.2 Percentage of concurrency

While direct non-neighbor charge transfer increases the energy-efficiency of the balancing process, faster equalization of the battery pack is achieved by performing multiple concurrent charge transfers between cells. By performing concurrent charge transfers between cells, the balancing time required to equalize the entire battery pack is reduced. However, certain balancing approaches, due to their electrical architecture, require the adjacent cells of the charge transfer pair to be in blocking mode, in order to prevent short circuit situation between cells. For instance, during a charge transfer between cell B^2 and B^3, the balancing units associated with cells B^1 and B^4 must be in blocking mode, meaning they cannot perform charge transfers with other cells in the pack. This subsequently reduces the number of simultaneous charge transfers possible in the battery pack, prolonging the overall equalization time. Therefore, balancing architectures that are capable of performing a high number of concurrent charge transfers between cells are favorable for distributed BMS topologies in order to increase the equalization speed.

4.2.2.3 Total number of switches

Apart from the above mentioned performance criterion, active cell balancing architectures are also evaluated based on the number of hardware components that form a single balancing unit. Typically, in order to increase the possible capabilities of a balancing architecture, more number of MOSFET switches or additional interconnections paths are required. This enables to perform non-neighbor balancing or multiple concurrent charge transfers between cells. However, increasing the switch count also increases the cost and installation volume of each balancing unit. More importantly, each switch has a parasitic resistance during conduction and therefore having an increased number of switches will increase the resistance in current flow path, resulting in an increased energy dissipation. Hence, balancing architectures having low number of switches, while still providing improved charge transfer capabilities are more favorable for distributed BMS topologies.

4.2.2.4 Number of high frequency switches

In addition to the total number of switches in each individual unit, an important performance constraint to be evaluated in an active cell balancing architecture is the number of switches that are required to be actuated with high frequency control signals in each balancing unit for performing charge transfer. Typically, power MOSFET switches in active cell balancing architectures are either actuated with a DC *ON* or *OFF* or using a high frequency control signal. Nevertheless, these power MOSFETs require a higher gate-drive actuation voltage compared to the logic-level output of the cell-level controller generating the control signal. Moreover, all MOSFETs in the balancing unit must be actuated with isolated gate-drive units, in order to prevent potential short circuits between cells. While in the case of switches that are actuated with DC signals, the gate-driver for the MOSFET can be realized as photovoltaic units, which generate the required isolated high gate-drive voltage directly from the logic-level output of the cell-level controller. They do not require any additional isolated power supply voltage for their operation. However, these photovoltaic drivers cannot be used for actuating switches with high frequency control signals, because of their relatively slow turn-*ON* and turn-*OFF* times. As a result, switches operated with high frequency control signals require sophisticated high speed gate-drivers powered with an isolated supply voltage, in order to avoid potential short circuit between cells. This results in an increased installation cost, volume and also consumes higher energy from the cell, since the isolated supply voltage is generated from the monitoring cell itself. Therefore, apart from the total switch count, it is beneficial for an active balancing architecture to have a reduced number of switches operated with high frequency control signals.

4.2.2.5 Number of high frequency control signals

Certain switches in each balancing unit are actuated using non-overlapping high frequency control signals, that consist of a series of *ON* pulses followed by *OFF* pulses. Depending upon the control scheme of the balancing architecture, more than one or two high frequency control signals are required to be generated for performing charge transfers. For a balancing architecture to perform direct non-neighbor charge transfer in a self-contained fashion (without requiring high frequency synchronization between controllers), either the number of switches in a balancing unit must be increased or more high frequency control signals are required. Increasing the switch count as discussed earlier will involve additional cost, volume and increased energy consumption due to the requirement of isolated gate-drive units. In addition, generating more high frequency control signals is also not beneficial since it increases the energy consumption from the cell. Since the individual cell-level controllers that are generating these high frequency control signals are directly powered from their respective battery cells, balancing architectures that require an increased number of these high frequency control signals will increase the energy consumption from the cell. Therefore, a balancing architecture that provides an increased charge transfer capability with a reduced number of high frequency control signals is much favored for implementation towards distributed BMS topologies.

4.2.2.6 Charge transfer scenarios

Apart from enabling non-neighbor balancing and higher percentage of concurrency, an active cell balancing architecture must also provide different possible charge transfer patterns as required so forth depending upon the SoC distribution along the battery pack. For example, if only a single cell of a series-connected battery pack has a higher SoC compared to the rest of the cells, it is energy-efficient and faster to transfer the excess energy from the higher SoC to all other cells in the battery pack, instead of transferring it to a single cell. For this scenario, the balancing architecture must enable a cell-to-pack charge transfer capability to achieve higher energy-efficiency. Similarly, if there exist a single weak cell in a battery pack compared to other cells, then transferring charge from all higher SoC cells simultaneously to the weak cell improves the equalization speed of the battery pack and therefore, the balancing architecture should be capable of performing pack-to-cell charge transfers. Moreover, a module-to-module transfer capability further increases the equalization speed and energy-efficiency if the imbalance in a series-connected battery pack are primarily between two modules of cells. Depending upon the SoC distribution over the battery pack, the active cell balancing strategies (will be discussed in Section 5.3.1) choose the optimal transfer scenario for improving both the energy-efficiency and overall equalization time. However, for the balancing strategies to independently choose the transfer scenario, the underlying architecture of the active cell balancing unit must allow different charge transfer patterns. As a result, balancing architectures that enable different charge transfer scenarios provide flexibility for the equalization strategies to choose the transfer pattern that will increase both the energy-efficiency and equalization time of the battery pack.

4.3 Summary

In this chapter, existing cell balancing approaches are discussed in detail. They are classified based on the methodology, type of energy storage elements and charge transfer scenario. Moreover, design requirements for implementing active cell balancing architectures in a distributed BMS topology are derived. Any cell balancing architecture must satisfy the imperative design requirements for implementation towards distributed BMSs. Architectures that satisfy the imperative design goals are further evaluated using the performance-related design goals. Based on these design requirements, three different modular active cell balancing architectures are proposed in Chapter 6 of this thesis.

5 Modeling Active Cell Balancing Architectures

From the design methodology and requirements described in the previous chapter, several modular active cell balancing architectures are proposed in Chapter 6 of this thesis. However, to analyze their performance-benefits on a system-level perspective and to optimize their energy-efficiency, a closed-form, analytical model is required. In this chapter, a generalized modeling methodology for an active cell balancing architecture is derived considering the different losses involved in the circuit components. Using the derived closed-form, analytical model, a methodology for performing system-level simulation analysis is described. Furthermore, optimization algorithms for improving the energy-efficiency of an active cell balancing architecture are proposed.

5.1 Battery Model

There is a huge body of literature proposing models for Li-Ion cells in various levels of complexity. These models are used in several application domains such as battery cell design, performance comparison, circuit design, etc. A good overview of different modeling approaches for Li-Ion cells is provided in [90]. Models of Li-Ion batteries are broadly classified into four types.

5.1.1 Electrochemical Models

Electrochemical models of Li-Ion cell analyze the individual chemical reactions that take place inside the cell. They are highly accurate and model every step of battery process in great detail. Typical application of these electrochemical Li-Ion cell models are in optimization of the physical battery properties such as electrode concentration, porosity to have an efficient design of the battery with significant performance in terms of power and energy capability. Even though they

are highly accurate and provide detailed information regarding Li-Ion battery parameters, they are typically not used in the circuit domain due to their increased complexity and implementation difficulty. Therefore, this thesis, does not consider the electrochemical cell models since they are not typically employed for circuit design and optimization approaches.

5.1.2 Analytical Models

Analytical models analyze the performance of the battery based on empirical equations that govern the ion movement inside the cell. It provides a system-level performance perspective in terms of battery runtime, capacity etc. Several analytical models have been proposed in the literature which range from simple Peukert's law [91] to complex kinetic battery models proposed in [92] and [93]. Even though the complexity is not as high as electrochemical models, these are not useful for circuit optimization approaches, since they do not model the transient voltage behavior of the cell with respect to load current. Rather they focus on determining the overall battery capacity or runtime which will be useful whether the battery can be used as a suitable power supply source for an application or not.

5.1.3 Stochastic Models

Here, the cell behavior is modeled as a stochastic evolution process, consisting of different states through representing the battery capacity. Stochastic models from [94–96] are widely referenced in the literature. They are primarily used for optimizing the communication traffic and work-load pattern of the application that is powered from the battery, in order to increase the effective capacity or runtime of the cell. However, all these models are based on a non validated *recovery effect* phenomenon, which is defined as the increase in effective capacity of the battery by performing a pulse discharge instead of a continuous discharge. Motivated from the fact that lead-acid cells exhibit positive behavior for pulse discharge, these models generalize the specific property of lead-acid cells to all other battery chemistries such as NiMH, Li-Ion etc. By contrast, in [97], through a systematic and exhaustive experimental validation, it was proved that Li-Ion cells do not exhibit any charge recovery effect. Therefore, these models are useful for modeling the electrical behavior of the battery in this thesis.

5.1.4 Electrical Battery Models

In contrast to the above mentioned modeling approaches, electrical models of Li-Ion cells accurately capture the transient voltage behavior of the cell with response to a current input or output, which enables their widespread application in areas such as circuit optimization, time-domain analysis, system-level simulations, etc. They consist of electrical components such as voltage source, resistors and capacitors that model the different phases of the cell voltage. The basic R_{int} electrical model of a Li-Ion cell as shown in [85], consists of a SoC dependent voltage source ($V_{\mathrm{B}}(SoC)$) representing the cell terminal voltage behavior to the SoC of the cell, in series with the internal resistance (R_{B}) of the cell. A piece-wise linear function representing the voltage characteristic of the cell with respect to the SoC is obtained by performing a discharge

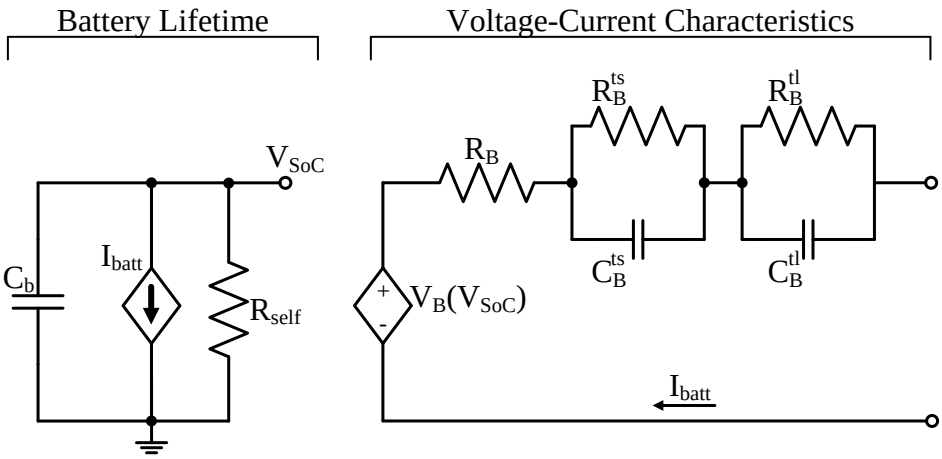


Figure 5.1: Electrical model of a Li-Ion cell as proposed in [99]. Capacitor C_b represents the total capacity and SoC of the cell. The terminal voltage of the cell is modeled by a voltage dependent voltage source in series with the internal resistance of the cell and two *RC*-networks modeling the transient behavior.

experiment at a current rate of $0.1C$ and measuring the cell voltage. However, the R_int model does not include the polarization effects of the Li-Ion cell, which come into place at higher values of discharge currents and therefore are not accurate for all application scenarios [98].

This thesis utilizes a more sophisticated electrical Li-Ion cell model as proposed in [99], that takes into account the different polarization effects. The cell capacity and SoC is represented by a huge capacitor C_B as shown in Fig. 5.1, whose value is calculated based on the rated capacity of the cell as

$$C_\mathrm{B} = 3600 \cdot \text{Capacity} \cdot f_1(\text{Cycle}) \cdot f_2(\text{Temp}) \tag{5.1}$$

where Capacity is the total $\mathrm{A\,h}$ capacity of the cell from the datasheet. The value of C_B also depends upon the cycle number and temperature of the cell through non-linear functions. Current source I_batt represents the load current to the cell. Its sign is positive while discharging and negative while the battery is being charged. The self-discharge phenomenon of the Li-Ion cell is modeled using a huge resistor R_self in parallel to the capacitor C_B as shown in Fig. 5.1. To ease the model validation process and parameter extraction, the dependency on cycle number and temperature can be relaxed as shown in [99]. They show that the modeling accuracy changes only $10\,\%$ for over 300 cycles and they used a temperature chamber to maintain constant temperature throughout the experiments. Moreover, the changes in capacity due to self-discharge of the cell is insignificant in the range of $2\,\%$ to $10\,\%$ over a period of one month and therefore, the impact of this huge resistor is also neglected for model simplification purposes.

The remaining part of the model depicts the terminal voltage behavior of the cell in response to a current input or output. The voltage dependent voltage source $V_\mathrm{B}(SoC)$ models the OCV of the cell. Its value is a non-linear function of the cell SoC, which is voltage across the capacitor C_B. By initializing the voltage across C_B to 1.0 or 0 enables to simulate a fully charged or an empty battery pack, respectively. The terminal response of a Li-Ion cell towards a pulse

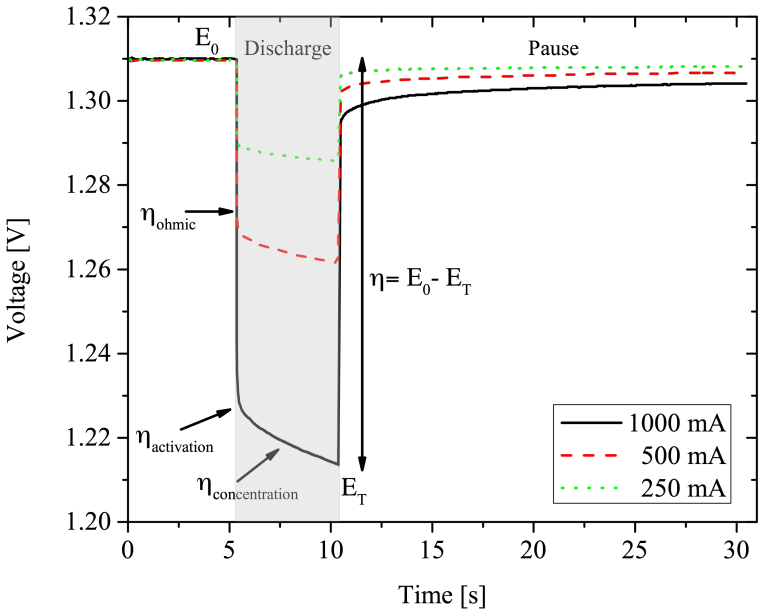


Figure 5.2: Measured terminal voltage response of a Li-Ion cell to an input current pulse.

current load is shown in Fig. 5.2. As soon as the input current is applied, the cell voltage drops immediately due to the internal resistance of the cell R_{B} as shown in Fig. 5.2 and is typically referred to as *ohmic overpotential*. The internal resistance is due to the resistances of electrolyte, electrodes (*Anode* and *Cathode*), current collectors and bonding wires of the cell. The time domain of this voltage drop due to this internal resistance of the cell is in µs range. First non-linear drop in the cell voltage shown in Fig. 5.2, is called as *activation overpotential*, which is due to the electron-transfer resistances of the cell and kinetic hindrance during the charge-transfer reaction. In addition, the cell voltage further drops in a non-linear fashion with respect to the current which is called as *concentration overpotential*, due to the diffusion process involved in the Li-Ion cells. These *activation* and *concentration* overpotentials are modeled using two parallel-connected *RC*-networks $R_{\mathrm{B}}^{\mathrm{ts}}$, $C_{\mathrm{B}}^{\mathrm{ts}}$ and $R_{\mathrm{B}}^{\mathrm{tl}}$, $C_{\mathrm{B}}^{\mathrm{tl}}$, respectively, in the electrical cell model shown in Fig. 5.1. All individual component values R_{B}, $R_{\mathrm{B}}^{\mathrm{ts}}$, $C_{\mathrm{B}}^{\mathrm{ts}}$, $R_{\mathrm{B}}^{\mathrm{tl}}$ and $C_{\mathrm{B}}^{\mathrm{tl}}$ are non-linear functions of the cell SoC and are extracted through experimental results and model fitting methods as shown in [99].

5.1.5 Battery Model for Active Cell Balancing Architectures

In the context of active cell balancing, existing works [14] and [85] use a simplified battery model, that consists of a fixed voltage source in series with the cell resistance. They claim that the variation in the cell voltage is very small over the useful SoC range of $80\,\%$ to $20\,\%$ for a small value of balancing current output or input. However, they do not consider that the balancing can happen during normal discharging operation of battery pack or during charging, in which

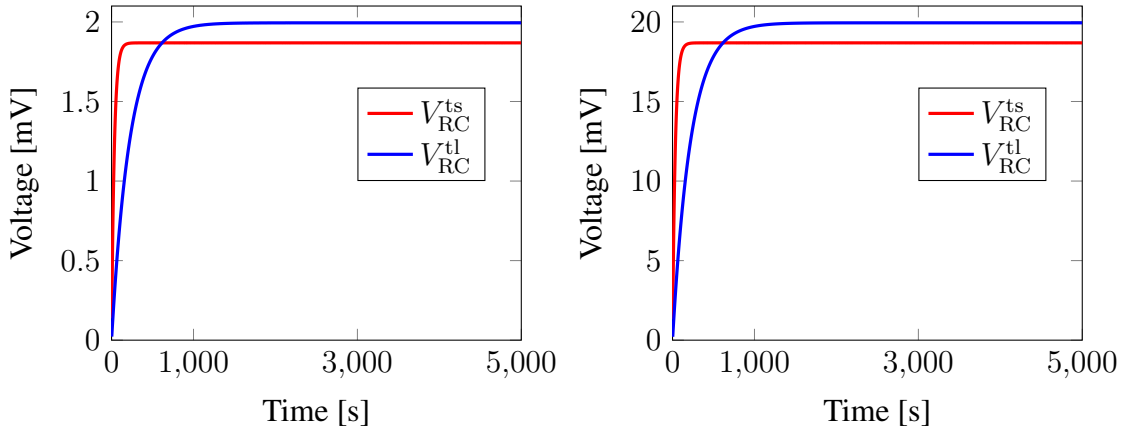


Figure 5.3: Simulated voltages across the *RC*-networks in the cell model shown in Fig. 5.1 (a) for a current pulse of $0.1C$ and (b) for a $1C$ current pulse.

case the Li-Ion cell will experience high amounts of currents, causing significant changes to the cell terminal voltage. Therefore, the voltage drops across the *RC*-networks in the cell model shown in Fig. 5.1 cannot be neglected during all instances. In order to show the impact of these *RC*-networks, a simulation of the cell model shown in Fig. 5.1 is performed using LTspice-IV, with the individual component values calculated from [99], assuming a $60\,\%$ SoC. Figs. 5.3a and 5.3b shows the voltages across the two *RC*-networks for a discharge current of $0.1C$ and $1C$, respectively.

It can be observed that for small values of currents, the capacitors in these *RC*-networks are not charged to a higher value, approximately in the range of $2\,\mathrm{mV}$. However, for higher values of currents, the voltage across these *RC*-networks increase significantly to a value of $200\,\mathrm{mV}$. In addition, the error induced due to ignoring these stages are accumulated over time and affect the calculation of timing parameters for the control signal. Therefore, the effects of these *RC*-networks must be considered while performing system-level analysis and optimization of active cell balancing architectures. Without loss of accuracy, it can be seen that the current drawn from the battery fully charges the capacitors in these *RC*-networks at a certain period of time, after which the voltage across these *RC*-networks remains constant, typically referred to as *steady-state* condition. After reaching *steady-state*, all currents requested from the battery or provided flows through the resistances $R_{\mathrm{B}}^{\mathrm{ts}}$ and $R_{\mathrm{B}}^{\mathrm{tl}}$ of the respective *RC*-networks. It is important to note that the worst-case difference between the cell terminal voltage and the OCV occurs during this *steady-state* condition and accounting the voltage drops at this region ensures high accuracy for system-level simulation. Therefore, the modeling methodology of active cell balancing architectures consider the cell as a voltage source V_{C}, which is influenced by the OCV of the cell and the *steady-state* values of the *RC*-networks as below

$$V_{\mathrm{C}} = \begin{cases} V_{\mathrm{B}} - V_{\mathrm{B}}^{\mathrm{ts}} - V_{\mathrm{B}}^{\mathrm{tl}}, & \text{if discharging} \\ V_{\mathrm{B}} + V_{\mathrm{B}}^{\mathrm{ts}} + V_{\mathrm{B}}^{\mathrm{tl}}, & \text{if charging} \end{cases} \tag{5.2}$$

where $V_{\mathrm{B}}^{\mathrm{ts}}$ and $V_{\mathrm{B}}^{\mathrm{tl}}$ represent the *steady-state* voltages across the *RC*-networks. Depending upon the direction of output current, these voltages add up (if charging) or subtract (if discharging)

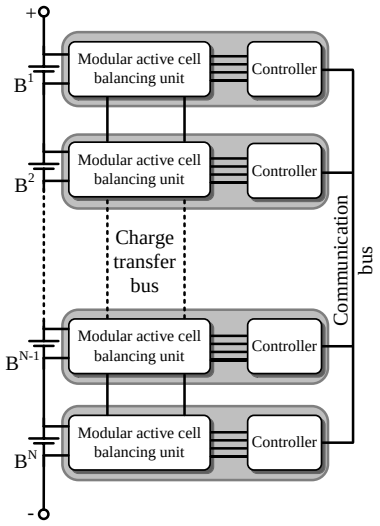


Figure 5.4: System-level representation of active cell balancing architectures. Each cell of a modular battery pack is associated with an individual balancing unit that are controlled by the cell-level controllers and transfer charge between cells through the charge transfer bus.

with the OCV (V_{B}) of the cell, respectively. Please note that the impact due to the internal resistance R_{B} is not considered in Eq. (5.2). However, it is taken into account in the modeling methodology of active cell balancing architectures explained in the following section.

5.2 Modeling Active Cell Balancing Architectures

As discussed in Chapter 4, active cell balancing architectures for distributed BMS topologies must contain homogeneous units attached to each cell and with minimal interconnection form a system-level balancing architecture as shown in Fig. 5.4. Furthermore, the individual balancing units transfer charge between cells through the charge transfer bus as shown in Fig. 5.4. Since capacitors only achieve a maximum energy-efficiency of $50\,\%$ when charged directly from a battery cell, this thesis considers only balancing architectures that use inductors and transformers as an energy storage element. The working principle and the modeling approach for both inductor and transformer-based active cell balancing architectures are similar. Therefore, the generalized modeling approach for inductor-based active cell balancing architecture is explained in the following and the modifications required for the transformer-based approaches is explained in Section 5.2.3. The charge transfer process of both inductor and transformer-based active cell balancing architectures consists of:

- Charging phase (Φ_1)
- Discharging phase (Φ_2)

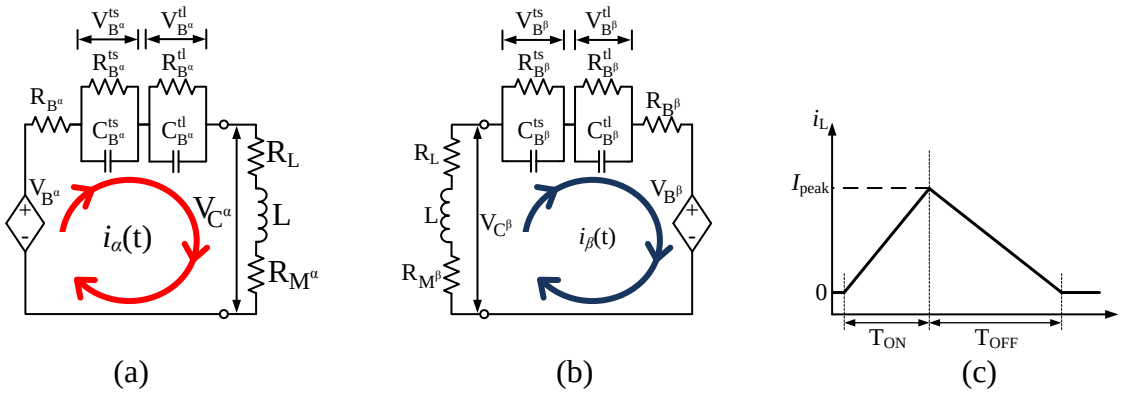


Figure 5.5: Equivalent circuits of the active cell balancing during charge transfer phases. (a) Equivalent circuit during charging phase Φ^1. (b) Equivalent circuit during discharging phase Φ^2. (c) Inductor current during the charge transfer phases.

Subsequently, equivalent circuits of the balancing architecture in these two phases can be generated and modeled individually to obtain a closed-form analytical model for system-level performance analysis.

5.2.1 Charging Phase Φ_1

During the charging phase Φ_1, MOSFETs in the balancing unit associated with the source cell (B^α) of the charge transfer pair are actuated to connect the energy storage element (inductor or transformer) to the cell. Fig. 5.5a shows the equivalent circuit during the charging phase. The current through the inductor increases linearly as shown in Fig. 5.5c. The terminal voltage V_{C^α} of the cell B^α is obtained by Eq. (5.2). The voltage V_L developed across the inductor for a balancing current i_α flowing through it is calculated by:

$$V_L = L\frac{di_\alpha}{dt} \tag{5.3}$$

Moreover, there will be an additional voltage drop due to the parasitic resistances of the individual components present in the charge flow path. During the charging phase, the *ON*-resistances R_{M} of the switches in the balancing unit, parasitic resistances of the energy storage element R_{L} and the internal resistance R_{B^α} of the source cell B^α of the charge transfer pair constitute the overall resistance during the charging phase. These individual resistances can be combined into a single term as:

$$R_\alpha = R_{\mathrm{B}^\alpha} + R_{\mathrm{L}} + R_{\mathrm{M}^\alpha} \tag{5.4}$$

The voltage drop generated across these individual resistances due to the flow of balancing current i_α is then calculated as:

$$V_{R_\alpha} = R_\alpha \cdot i_\alpha \tag{5.5}$$

Now by applying KIRCHHOFF'S voltage law to the equivalent circuit during charging phase shown in Fig. 5.5a results in:

$$V_{\mathrm{C}^\alpha} = V_L + V_{R_\alpha} \tag{5.6}$$

Substituting for V_L and V_{R_α} from Eqns. (5.3) and (5.5) in Eq. (5.6) gives:

$$L\frac{di_\alpha}{dt} + R_\alpha \cdot i_\alpha = V_{\mathrm{C}^\alpha} \tag{5.7}$$

Eq. (5.7) is a first order Ordinary Differential Equation (ODE), which can be solved by method of substitution. Assuming that there was no charge stored in the energy storage element before balancing, the initial value of current is $i_\alpha(0) := 0$. Solving Eq. (5.7) with this initial value gives a time-domain representation of the balancing current as:

$$i_\alpha(t) = \frac{V_{\mathrm{C}^\alpha}}{R_\alpha}\left(1 - e^{\frac{-R_\alpha}{L}t}\right) \tag{5.8}$$

The time taken for the balancing current to reach the peak value I_{peak}, determined by the saturation current limit of the energy storage element, is denoted as T_{ON} as shown in Fig. 5.5c. Solving Eq. (5.8) for $i_\alpha(T_{\mathrm{ON}}) := I_{\mathrm{peak}}$ provides:

$$\begin{aligned}
I_{\mathrm{peak}} &= \frac{V_{C^\alpha}}{R_\alpha}\left(1 - e^{\frac{-R_\alpha}{L}T_{\mathrm{ON}}}\right) \\
I_{\mathrm{peak}} \cdot R_\alpha - V_{\mathrm{C}^\alpha} &= -V_{\mathrm{C}^\alpha} \cdot e^{\frac{-R_\alpha}{L}T_{\mathrm{ON}}} \\
e^{\frac{-R_\alpha}{L}T_{\mathrm{ON}}} &= \frac{V_{\mathrm{C}^\alpha} - I_{\mathrm{peak}} \cdot R_\alpha}{V_{\mathrm{C}^\alpha}} \\
T_{\mathrm{ON}} &= -\frac{L}{R_\alpha} \cdot \ln\left[\frac{V_{\mathrm{C}^\alpha} - R_\alpha \cdot I_{\mathrm{peak}}}{V_{\mathrm{C}^\alpha}}\right]
\end{aligned} \tag{5.9}$$

The amount of charge Q_{tx} that is taken out of the source cell during the time period $0 \leq t \leq T_{\mathrm{ON}}$ is calculated by integrating Eq. (5.8) as:

$$\begin{aligned}
q_\alpha(t) &= \int_0^{T_{\mathrm{ON}}} i_\alpha(t) \cdot dt \\
&= \int_0^{T_{\mathrm{ON}}} \frac{V_{\mathrm{C}^\alpha}}{R_\alpha}\left(1 - e^{\frac{-R_\alpha}{L}t}\right) dt \\
Q_{\mathrm{tx}} &= \frac{V_{\mathrm{C}^\alpha}}{R_\alpha}T_{\mathrm{ON}} - \frac{L \cdot V_{\mathrm{C}^\alpha}}{R_\alpha^2}\left[1 - e^{\frac{-R_\alpha}{L}T_{\mathrm{ON}}}\right]
\end{aligned} \tag{5.10}$$

5.2.2 Discharging Phase Φ_2

The discharging phase Φ_2 involves the transfer of stored energy in the inductor to the destination cell (B^β) of the charge transfer pair as shown in Fig. 5.5b. The inductor current decreases as shown in Fig. 5.5c with a slope determined by the terminal voltage V_{C^β} of the destination cell

obtained by Eq. (5.2). Moreover, the individual resistances on the receiving side can be combined in a similar fashion like Eq. (5.4) as:

$$R_\beta = R_{\mathrm{B}^\beta} + R_\mathrm{L} + R_{\mathrm{M}^\beta} \tag{5.11}$$

A voltage drop V_{R_β} is generated across this resistance due to the flow of discharging current i_β. Applying KIRCHHOFF'S voltage rule to the discharging phase leads to:

$$V_L + V_{R_\beta} + V_{\mathrm{C}^\beta} = 0 \tag{5.12}$$

This gives a first order ODE for the discharging phase as:

$$L\frac{di_\beta}{dt} + R_\beta \cdot i_\beta + V_{\mathrm{C}^\beta} = 0 \tag{5.13}$$

The initial value of the balancing current during discharging phase is the peak value of the current at the end of charging phase $i_\beta(0) := I_\mathrm{peak}$. Solving Eq. (5.13) with this initial value gives a time domain representation of the balancing current during discharging phase as follows:

$$i_\beta(t) = I_\mathrm{peak}\left(e^{\frac{-R_\beta}{L}t}\right) - \frac{V_{\mathrm{C}^\beta}}{R_\beta}\left(1 - e^{\frac{-R_\beta}{L}t}\right) \tag{5.14}$$

With the time domain representation of the discharging current i_β, the time T_OFF required for the inductor to fully discharge its stored energy to the destination cell is calculated by solving Eq. (5.14) by substituting $i_\beta(T_\mathrm{OFF}) = 0$.

$$\begin{aligned}
0 &= I_\mathrm{peak}\left(e^{\frac{-R_\beta}{L}T_\mathrm{OFF}}\right) - \frac{V_{\mathrm{C}^\beta}}{R_\beta}\left(1 - e^{\frac{-R_\beta}{L}T_\mathrm{OFF}}\right) \\
I_\mathrm{peak}\left(e^{\frac{-R_\beta}{L}T_\mathrm{OFF}}\right) &= \frac{V_{\mathrm{C}^\beta}}{R_\beta}\left(1 - e^{\frac{-R_\beta}{L}T_\mathrm{OFF}}\right) \\
\left(I_\mathrm{peak} + \frac{V_{\mathrm{C}^\beta}}{R_\beta}\right)e^{\frac{-R_\beta}{L}T_\mathrm{OFF}} &= \frac{V_{\mathrm{C}^\beta}}{R_\beta} \\
T_\mathrm{OFF} &= \frac{-L}{R_\beta}\ln\left[\frac{V_{\mathrm{C}^\beta}}{V_{\mathrm{C}^\beta} + I_\mathrm{peak}\cdot R_\beta}\right]
\end{aligned} \tag{5.15}$$

Subsequently, the charge (Q_rx) that is received by the destination cell B^β is calculated by integrating Eq. (5.14) for the time period $0 \leq t \leq T_\mathrm{OFF}$ as:

$$\begin{aligned}
q_\beta(t) &= \int_0^{T_\mathrm{OFF}} i_\beta(t)dt \\
&= \int_0^{T_\mathrm{OFF}} I_\mathrm{peak}\left(e^{\frac{-R_\beta}{L}t}\right) - \frac{V_{\mathrm{C}^\beta}}{R_\beta}\left(1 - e^{\frac{-R_\beta}{L}t}\right)dt \\
Q_\mathrm{rx} &= \frac{L}{R_\beta}\left(I_\mathrm{peak} + \frac{V_{\mathrm{C}^\beta}}{R_\beta}\right)\left[1 - e^{\frac{-R_\beta}{L}T_\mathrm{OFF}}\right] - \frac{V_{\mathrm{C}^\beta}}{R_\beta}T_\mathrm{OFF}
\end{aligned} \tag{5.16}$$

5.2.3 Efficiency and Loss Models

In this section, the losses introduced due to the parasitic resistances and capacitances that are present in the components of the active cell balancing unit are outlined. There are typically three types of losses introduced by the circuit components in the balancing architecture. They are:

- Conduction losses
- Switching losses and
- Leakage inductance losses (only for transformer-based balancing architectures)

5.2.3.1 Conduction Losses

Each individual component in the balancing unit has a parasitic internal resistance due to its construction. When a current flows through these parasitic resistances, energy is dissipated across it in the form of heat. This energy dissipation is proportional to the value of the current (I), resistance (R) and the time (T) the current flows through the resistance as:

$$E_{\mathrm{cd}} = I^2 \cdot R \cdot T \tag{5.17}$$

In the case of active cell balancing, the conduction energy dissipation is divided into charging and discharging phases. The equivalent resistances in both phases are derived in Eqns (5.4) and (5.11), respectively. Since the charging and discharging phase models presented in Section 5.2.1 and 5.2.2, respectively, include the impact of these parasitic resistances (R_α and R_β) in their derivation, the overall conduction energy dissipation in one charge transfer cycle is calculated as:

$$\begin{aligned} E^{\mathrm{cd}}_{(\Phi_1,\Phi_2)} &= E_{\mathrm{tx}} - E_{\mathrm{rx}} \\ &= Q_{\mathrm{tx}} \cdot V_{\mathrm{C}^\alpha} - Q_{\mathrm{rx}} \cdot V_{\mathrm{C}^\beta} \end{aligned} \tag{5.18}$$

5.2.3.2 Switching Losses

The switches in the balancing units are realized as power MOSFETs. As explained in Section 2.2.2, power MOSFET switches exhibit two types of energy dissipation. The conduction energy dissipation as explained in the previous section is due to the *ON* resistance between the drain-to-source terminals. In addition, the MOSFET dissipates energy during each switching transition. This energy dissipation is attributed to the non-zero turn-on (t_{ON}) and turn-off (t_{OFF}) delays required for charging and discharging of the input parasitic capacitance C_{ISS}. Moreover, with each switching activity the output parasitic capacitance C_{OSS} has to be discharged, which also adds to the switching energy dissipation. The losses due to each switching activity of the MOSFET as explained in Section 2.2.2 can be calculated by:

$$E^{\mathrm{sw}} = \frac{1}{2} \cdot I_{\mathrm{ds}} \cdot V_{\mathrm{ds}} \{t_{\mathrm{ON}} + t_{\mathrm{OFF}}\} + \frac{1}{2} \cdot C_{\mathrm{OSS}} \cdot V_{\mathrm{ds}}^2 \tag{5.19}$$

Inductor-based balancing architectures. In case of inductor-based active cell balancing architectures, this switching loss is divided into charging (Φ_1) and discharging (Φ_2) phases. During

charging phase, the current through the MOSFET starts to rise slowly from zero as shown in Fig. 5.5c. Therefore, during the turn-*ON* delay time t_{ON}, the current through the MOSFET switch is also zero and as a result no energy is dissipated during these periods. However, during the end of charging phase, the MOSFET switch is turned off with a non-zero current and therefore incurs a switching energy dissipation given by:

$$E_{\Phi_1}^{\mathrm{sw}} = \frac{1}{2} \cdot I_{\mathrm{peak}} \cdot V_{\mathrm{C}^\alpha} \cdot t_{\mathrm{OFF}} + \frac{1}{2} \cdot C_{\mathrm{OSS}} \cdot V_{\mathrm{C}^\alpha}^2 \tag{5.20}$$

Similarly, during the discharging phase Φ_2, the MOSFET switch is turned-*ON*, with the peak current I_{peak} resulting in an energy dissipation calculated as:

$$E_{\Phi_2}^{\mathrm{sw}} = \frac{1}{2} \cdot I_{\mathrm{peak}} \cdot V_{\mathrm{C}^\beta} \cdot t_{\mathrm{ON}} + \frac{1}{2} \cdot C_{\mathrm{OSS}} \cdot V_{\mathrm{C}^\beta}^2 \tag{5.21}$$

The total switching energy dissipation in each charge transfer cycle in an inductor-based active cell balancing architecture is given by:

$$\begin{aligned} E_{\mathrm{sw}(\Phi_1,\Phi_2)}^{\mathrm{Ind}} &= E_{\Phi_1}^{\mathrm{sw}} + E_{\Phi_2}^{\mathrm{sw}} \\ &= \frac{1}{2} \cdot I_{\mathrm{peak}} \cdot \{V_{\mathrm{C}^\alpha} \cdot t_{\mathrm{OFF}} + V_{\mathrm{C}^\beta} \cdot t_{\mathrm{ON}}\} + \frac{1}{2} \cdot C_{\mathrm{OSS}} \cdot \{V_{\mathrm{C}^\alpha}^2 + V_{\mathrm{C}^\beta}^2\} \end{aligned} \tag{5.22}$$

Transformer-based balancing architectures. Even though the conduction energy dissipation for both inductor and transformer based balancing architectures are same, their switching energy dissipation is different. Compared to inductors, transformers have a primary and secondary winding as explained in Section 2.1.3. During charging phase Φ_1, charge from the source cell is stored in the primary winding for time period T_{ON}. The stored charge in the primary is transferred to the secondary winding of the transformer and discharged to the destination cell during the discharging phase Φ_2 for the time period T_{OFF}. The charging phase Φ_1 in transformer-based balancing architectures is similar to inductor-based approaches and therefore, the switching energy dissipation $E_{\Phi_1}^{\mathrm{sw}}$ during the charging phase is the same. However, during discharging phase Φ_2, the current through the secondary winding of the transformer starts to rise from zero to peak value once the primary-secondary energy transfer takes place. As a result, the switching energy dissipation due to the MOSFET turn-*ON* during the discharging phase is zero, since there is no flow of secondary current when the MOSFET is turned *ON*. Similarly, the MOSFET is turned *OFF* with zero current and therefore, the only contribution for the switching energy dissipation during discharging phase Φ_2 is from the MOSFET parasitic output capacitance C_{OSS}. The total switching loss in transformer-based balancing architectures is:

$$E_{\mathrm{sw}(\Phi_1,\Phi_2)}^{\mathrm{Trf}} = \frac{1}{2} \cdot I_{\mathrm{peak}} \cdot V_{\mathrm{C}^\alpha} \cdot t_{\mathrm{OFF}} + \frac{1}{2} \cdot C_{\mathrm{OSS}} \cdot \{V_{\mathrm{C}^\alpha}^2 + V_{\mathrm{C}^\beta}^2\} \tag{5.23}$$

5.2.3.3 Leakage Inductance Losses

The losses due to leakage inductance are specific only to transformer-based active cell balancing architectures. As explained in Section 2.1.3, a transformer has a primary and secondary winding that are wound on the same iron core. For using a transformer in active cell balancing applications,

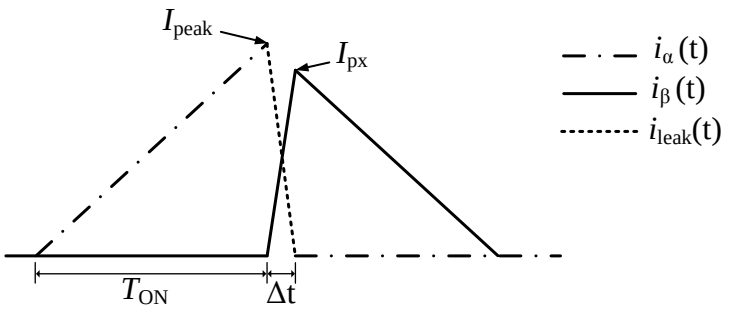


Figure 5.6: Parasitic leakage inductance associated with the primary winding of the transformer delays the primary-secondary energy transfer for a time period Δt. As a result, the initial value of the secondary is reduced to I_{px}.

the core requires to have an air-gap, in which the energy is stored. When the primary winding of the transformer is charged from the source cell during phase Φ_1, it creates a magnetic flux that is linked to the secondary winding through the core of the transformer. Once the discharging phase Φ_2 begins, the primary-secondary energy transfer takes place and the secondary winding current starts to flow discharging the stored energy in the transformer to the destination cell. Not all the energy from the primary is transferred to the secondary winding of the transformer. Some part of magnetic flux generated from the primary winding leaks into the surrounding air and leads to a reduced amount of energy transferred to the secondary winding of the transformer. This unlinked flux from the primary winding is modeled as an additional inductance in series with the primary winding and called as *leakage inductance*.

The balancing current from the source cell during the charging phase Φ_1, charges the leakage inductance to the same peak I_{peak} value of current, in addition to the primary of the transformer. The energy stored in the leakage inductance is not transferred to the secondary winding of the transformer. Instead, the leakage inductance forms a resonant circuit with the parasitic output capacitance C_{OSS} of the MOSFET switch and starts oscillating, thereby discharging the energy as heat into the MOSFET switch. If proper care is not exercised, the voltage due to this oscillation might reach higher values than the MOSFET break-down voltage limit eventually damage the switch. To alleviate this issue, several clamping methods for the leakage inductances such as *RCD*-snubbers, Zener-diode clamping are typically used, see [100], to safely discharge the energy stored in the leakage inductance.

Nevertheless, the energy stored in the leakage inductance of the transformer has to be discharged fully for the primary-secondary energy transfer to take place. The time taken to fully discharge the energy stored in leakage inductance is calculated by [100]

$$\Delta t = \frac{I_{\mathrm{peak}} \cdot L_{\mathrm{leak}}}{V_{\mathrm{clamp}} - V_{\mathrm{LS}} \cdot N} \tag{5.24}$$

where L_{leak} is the leakage inductance value, V_{clamp} is the clamping voltage, V_{LS} is the voltage across the secondary winding of the transformer and N is the turns-ratio of the transformer defined by Eq. (2.8). During this time period Δt, no current flows in the secondary winding as

shown in Fig. 5.6. The current through the secondary winding only starts to flow after this time period Δt and therefore, the initial value of the secondary winding current is not equal to the final value of the primary winding current of the transformer. Instead, the initial value of the secondary current during discharging phase is given by:

$$I_{\mathrm{px}} = I_{\mathrm{peak}} \left[\frac{L_{\mathrm{leak}}}{L \cdot \left(\frac{V_{\mathrm{clamp}}}{V_{\mathrm{LS}} \cdot N} \right) - 1} \right] \tag{5.25}$$

As a result, Eq. (5.14) modeling the balancing current during discharging phase Φ_2, in case of transformer-based balancing architectures is given by

$$i_{\beta}(t) = I_{\mathrm{px}} \left(e^{\frac{-R_{\beta}}{L} t} \right) - \frac{V_{\mathrm{C}^{\beta}}}{R_{\beta}} \left(1 - e^{\frac{-R_{\beta}}{L} t} \right) \tag{5.26}$$

with I_{px} calculated from Eq. (5.25).

5.2.3.4 Energy-efficiency

The energy-efficiency of an active cell balancing architecture is defined as

$$\eta_{(\Phi_1,\Phi_2)} = 1 - \frac{E^{\mathrm{diss}}_{(\Phi_1,\Phi_2)}}{E^{\mathrm{tx}}_{(\Phi_1,\Phi_2)}} \tag{5.27}$$

where E_{diss} is defined as the energy dissipated in the parasitic resistances and capacitances present in the circuit components and E_{tx} is the amount of energy taken out of the source cell of the charge transfer pair. E_{diss} is the total of individual energy dissipations described in Sections 5.2.3.1 to 5.2.3.3.

$$E^{\mathrm{diss}}_{(\Phi_1,\Phi_2)} = \begin{cases} E^{\mathrm{cd}}_{(\Phi_1,\Phi_2)} + E^{\mathrm{Ind}}_{\mathrm{sw}(\Phi_1,\Phi_2)}, & \text{for inductor-based balancing architectures} \\ E^{\mathrm{cd}}_{(\Phi_1,\Phi_2)} + E^{\mathrm{Trf}}_{\mathrm{sw}(\Phi_1,\Phi_2)}, & \text{for transformer-based architectures} \end{cases} \tag{5.28}$$

The energy dissipation due to the leakage inductance in case of transformer-based balancing architectures, is directly included in the calculation of discharging phase current $i_{\beta}(t)$ as shown in Eq. (5.26). Therefore, it is not explicitly mentioned in Eq. (5.28). Furthermore, the amount of energy taken from the source cell is calculated by:

$$E^{\mathrm{tx}}_{(\Phi_1,\Phi_2)} = Q_{\mathrm{tx}} \cdot V_{\mathrm{C}^{\alpha}} \tag{5.29}$$

In the following section, an approach to perform system-level simulation of the balancing process using the above closed-form, analytical model is explained in detail, along with potential scopes for optimization at different levels of abstraction.

5.3 Balancing Strategies and System-level Simulation

In this section, balancing strategies that determine the source and destination cells of a charge transfer pair, depending upon the SoC distribution of the battery pack are discussed. Furthermore, an approach for performing system-level simulation using the analytical closed-form model to evaluate the performance of the active cell balancing architectures that are proposed in Chapter 6 of this thesis is explained.

5.3.1 Active Cell Balancing Strategies

Having an efficient active cell balancing electrical architecture, that minimizes the losses involved in the parasitic resistances, capacitances and inductances present in the circuit components as explained in Section 5.2.3.1 to 5.2.3.3, is imperative. However, the system-level efficiency of the balancing process depends upon the charge exchange patterns between the cells of a series-connected battery pack. For this purpose, it is imperative to have an efficient algorithmic strategy that determines the source and destination cells of the charge transfer pair, in order to maximize the system-level efficiency of the balancing process. Moreover, an active cell balancing strategy also determines the order in which these charge transfers will take place in the battery pack. In addition, the active cell balancing strategies must also consider the capabilities of the underlying hardware architecture of the balancing unit, while determining the charge transfer pairs. For example, as explained in Section 4.2.2.2, performing a higher number of simultaneous charge transfers between cells results in a faster equalization of the battery pack. However, certain active cell balancing architectures might require the adjacent cells of the charge transfer pairs to be in blocking mode, in order to prevent short circuit conditions. This information has to be considered by the active cell balancing strategies while determining the source and destination cells of the charge transfer pairs, such that unsafe charge transfers are not initiated. Therefore, active cell balancing approaches require a hardware/software co-design, where the software algorithms (balancing strategies) determine the optimal charge transfer pair of cells and charge flow directions considering the specific characteristics and capabilities of the underlying hardware architecture of the active cell balancing unit. In the following, the design requirements of active cell balancing strategies for distributed BMS topologies are discussed.

5.3.1.1 Design Requirements of Active Cell Balancing Strategies

Active cell balancing strategies for distributed BMSs must be developed satisfying the following design requirements.

Maximize energy-efficiency. Higher energy-efficiency is the prime advantage of active cell balancing approaches compared to passive techniques. In addition to having an energy-efficient hardware configuration, active cell balancing process requires efficient strategies to determine the source and destination cells of the charge transfer pair. An energy-efficient balancing strategy fully utilizes the capabilities of the underlying hardware architecture. For example, consider a case where charge has to be transferred from cell B^1 to cell B^8 of a series-connected battery pack. If a neighbor-only active cell balancing architecture is used, then the charge has to be shuttled

through all intermediate cells, whereas, using a non-neighbor active cell balancing architecture, direct charge transfers are possible. Moreover, there exists a maximum limit on the number of intermediate cells in case of the non-neighbor balancing architecture. Considering a limit of 4 intermediate cells, i.e., the maximum possible charge transfer distance from cell B^1 is cell B^6, and such a limitation for the above example provides different possibilities of transferring charge from cell B^1 to cell B^8. Different possible combinations of source and destination cells are $B^1 \rightarrow B^4$ and $B^4 \rightarrow B^8$ or $B^1 \rightarrow B^5$ and $B^5 \rightarrow B^8$, etc. However, the efficiency of charge transfer is higher only if it is transferred to a maximum distance as possible and therefore the corresponding active cell balancing strategy has to determine the source and destination cell accordingly to maximize the energy-efficiency of the balancing process. Moreover, a balancing strategy is only energy-efficient if the individual cell SoC and the pack average SoC change monotonously, i.e., a cell cannot be selected as a destination of a charge transfer pair, if it has been chosen as a source cell in earlier transactions.

Minimize equalization time. Apart from increasing the energy-efficiency, active cell balancing strategies must also focus on reducing the equalization time of the battery pack. Increasing the balancing current will reduce the time required for equalization, since large amount of charge can be transferred in each cycle. However, this also increases the energy dissipation across the parasitic resistances, capacitances and inductances involved in the circuit components as discussed in Section 5.2.3.1, 5.2.3.2 and 5.2.3.3, respectively. Therefore, optimal value of balancing current which maximizes the equalization speed and at the same time minimizes the energy dissipation across the parasitic components has to be used. In addition, the equalization speed can be improved by performing multiple simultaneous charge transfers between cells.

Maximize usable capacity. As discussed in Section 1.2.2.3, the discharging or charging process of the battery pack has to be stopped once the SoC of any cell in the pack reaches the minimum or maximum safe operating threshold value, respectively. Failure to do so will result in over-discharging or over-charging faults that might lead to fire or explosion due to thermal runaway. Therefore, in certain situations, it is important for an active cell balancing strategy to focus on improving the critical factors, rather than trying to have an energy-efficient equalization. For instance, the discharging threshold of the battery pack depends upon the cell with the minimum SoC and quickly bringing up the SoC of the cell, when it is near to the lower threshold value, increases the effective usable capacity of the battery pack and thereby the driving range of an EV. Similar conditions apply during charging process, where the SoC of the strong cell (cell with higher SoC than others), has to be reduced quickly, in order to prevent it from reaching the maximum threshold value and thereby allowing to fully charge the remaining cells of the battery pack. Therefore, apart from energy-efficiency, active cell balancing strategies must also focus on improving the usable capacity of the battery pack, in order to prevent cells from reaching the lower or upper threshold limits.

Maximizing lifetime of cells. In the process of increasing the usable capacity of the battery pack by performing active cell balancing, the equalization strategies must also focus on maintaining the SoH of the individual cells of the battery pack. Each balancing activity involves discharging

and charging the source cell and the destination cell of the charge transfer pair, respectively. This effectively increases the charge/discharge cycles of the individual cells and eventually affects their SoH. Even though having an equalized battery at all time instants is beneficial, performing constant equalization affects the SoH of the individual cells and therefore, the balancing process must be appropriately carried out during critical instances. Moreover, cells that have a reduced SoC value compared to other cells are considered as weak and discharging them with the same series current will weaken their capacity compared to the strong cells that have higher SoC values. Therefore, apart from equalization, active cell balancing strategies must reduce the stress experienced by these weaker cells with the help of the associated active cell balancing architecture. Alternatively, the stronger cells in the pack having a higher SoC value must be stressed more to have an uniform aging process of the battery pack.

Minimize communication messages. For the case of fully distributed *smart cell* BMS topology, all functions are carried out through coordination via communication between the individual cell-level controllers. The source and destination cells of the charge transfer pair in such a BMS topology are likewise determined by negotiations between the individual cell-level controllers. Each communication message involves a certain amount of energy drawn from the transmitting cell and the receiving cell. Therefore, the goal of the active cell balancing strategy is to minimize the number of communication messages and thereby reduce the energy dissipation from the cell. For example, in each charge transfer cycle only a small amount of charge (in the range of μC) is transferred and therefore it is not necessary to update the status of the source and destination cells after each cycle. Rather the SoCs of the source and destination cells of the charge transfer pair can be updated by performing millions of such balancing cycles, which minimizes the amount of messages transmitted and reduces the energy consumption from the cell. Moreover, smart SoC estimation algorithms can track the evolution of individual cell SoCs over a balancing process, thereby further minimizing the energy dissipation due to the requirement of communication between the cell-level controllers.

5.3.1.2 Existing Active Cell Balancing Strategies

Several active cell balancing strategies exist in the literature. For example, in [101] and [102] two control optimization algorithms for active cell balancing are proposed. One algorithm focuses on maximizing the effective capacity of the battery pack while the other addresses the issue of balancing the SoCs of the individual cells in the battery pack. Similarly, in [58], two cell balancing strategies, *Slow* and *Fast*, are proposed, which are primarily based on direct non-neighbor charge transfer architectures. *Slow* mainly focuses on performing direct energy-optimal charge transfers rather than exploiting the concurrent charge transfer capabilities of the architecture. Therefore, the energy-efficiency of this balancing strategy is higher while resulting in an increased equalization time. By contrast, the *Fast* strategy, performs multiple concurrent charge transfers between cells, resulting in an increased equalization speed, while compromising a small factor in energy-efficiency. A modified version of the *Slow* strategy for charge transfers between multiple source and destination cells *MMSlow* is proposed in [103]. Furthermore, *MMfind* proposed in [103], groups cells with higher SoCs as a single unit and transfers the excess charge to another group of that have lower SoCs. In [104], four different

active cell balancing strategies, *Below-average*, *Minimum*, *Maximum* and *Minmax*, are proposed for neighbor-only charge transfer architecture, to equalize the SoC of all cells in the battery pack.

5.3.2 System-level Simulation Methodology

Each charge transfer cycle in the balancing process involves a charging phase Φ_1, during which a portion of the excess charge from the source cell is stored in the energy storage element and a discharging phase Φ_2, in which the stored charge in the energy storage element is transferred to the destination cell. Typically, cells in the battery pack have a capacity in the order of several $\mathrm{A\,h}$ and the imbalances in charge levels of cells are in the range of several kC. However, the energy storage element used in the balancing unit has a charge storing capacity in the order of several $\mu\mathrm{C}$ to mC, in order to have a reduced installation volume. For instance, a $60\,\mathrm{A\,h}$ rated capacity battery pack consisting of imbalanced cells with SoCs in the range of $60\,\%$ ($129{,}6\,\mathrm{kC}$) and $50\,\%$ ($108\,\mathrm{kC}$), means a difference in charge of $21{,}6\,\mathrm{kC}$. On the other hand, if an inductance of $100\,\mu\mathrm{H}$ with a maximum current rating of $5\,\mathrm{A}$ is used as an energy storage element in the balancing unit, the maximum amount of charge Q_{tx} that can be transferred from the source cell to the energy storage element in a single charge transfer cycle is approximately equal to $295{,}65\,\mu\mathrm{C}$, calculated using Eq. (5.10) assuming a peak balancing current I_{peak} of $4{,}5\,\mathrm{A}$. Therefore, millions of individual charge transfer cycles comprising of T_{ON} and T_{OFF} are required to fully equalize the SoCs of individual cells in the battery pack. With N being the number of individual charge transfer cycles required to equalize the SoC levels of cells in the battery pack, then the total equalization time T_{B} is calculated as:

$$T_{\mathrm{B}} = N \cdot (T_{\mathrm{ON}} + T_{\mathrm{OFF}}) \tag{5.30}$$

Moreover, the energy metrics calculated in Section 5.2.3.4 is for a single charge transfer cycle and the overall energy-dissipation and transferred energy are calculated as follows:

$$\begin{aligned} E_{\mathrm{diss}}^{\mathrm{Tot}} &= N \cdot E_{\mathrm{diss}}^{\mathrm{PWM}} \\ E_{\mathrm{tx}}^{\mathrm{Tot}} &= N \cdot E_{\mathrm{tx}}^{\mathrm{PWM}} \\ \eta_{\mathrm{eff}}^{\mathrm{Tot}} &= 1 - \frac{E_{\mathrm{diss}}^{\mathrm{Tot}}}{E_{\mathrm{tx}}^{\mathrm{Tot}}} \end{aligned} \tag{5.31}$$

Algorithm 1 shows the methodology for performing system-level simulation of the equalization process. The input array consists of an unbalanced battery pack and the output of the equalization process is an equalized battery pack, where charge levels of all cells are within the tolerable variance value. The balancing simulation is performed until the deviation between the charge level of all cells in the battery pack is within $0{,}1\,\%$ (line 2). Depending upon the balancing strategy, a set of charge transfer pairs $\mathcal{P}$ are identified (line 3) considering the charge distribution of the battery pack and the underlying constraints of the active cell balancing architecture. For each identified pair p in $\mathcal{P}$, times T_{ON}, T_{OFF} are calculated from Eqns. (5.9) and (5.15), respectively, for the specified peak value of the balancing current (line 5). Moreover, the charge that is transferred Q_{tx} and received Q_{rx} for times T_{ON} and T_{OFF} are computed as per Eqns. (5.10) and (5.16), respectively (line 5).

Algorithm 1 System-level charge transfer simulation algorithm.

Input:
Unbalanced charge array Q, macro step size T_M

Output:
Balanced charge array Q

1: $E_{\text{diss}} = 0$, $T_{\text{bal}} = 0$
2: **while** Max(Q) - Min(Q) > $0{,}1\,\%$ **do**
3: Find charge transfer pairs $\mathcal{P}$
4: **for** each pair p in $\mathcal{P}$ **do**
5: Calculate T_{ON}, Q_{tx}, T_{OFF} and Q_{rx} for the desired I_{peak}
6: $N = \frac{T_M}{(T_{\text{ON}}+T_{\text{OFF}})}$
7: Perform transfers in p for N cycles
8: Calculate $E^{\text{cd}}_{(\Phi_1,\Phi_2)}$, $E^{\text{sw}}_{(\Phi_1,\Phi_2)}$ for each charge transfer cycle
9: $E^{\text{Tot}}_{\text{diss}} = N \cdot (E^{\text{cd}}_{(\Phi_1,\Phi_2)} + E^{\text{sw}}_{(\Phi_1,\Phi_2)})$
10: $T_B = N \cdot (T_{\text{ON}} + T_{\text{OFF}})$
11: $E_{\text{diss}} = E_{\text{diss}} + E^{\text{Tot}}_{\text{diss}}$
12: $T_{\text{bal}} = T_{\text{bal}} + T_B$
13: Adjust Q according to transfers
14: **end for**
15: **end while**

Since only a small amount of charge, in the order of µC, is transferred in each cycle, to speed up the simulation process, transfers are performed for a macro step time of T_M. The number of charge transfer cycles N in each macro step time T_M is computed in line 6. With Q_{tx} and Q_{rx}, the conduction ($E^{\text{cd}}_{(\Phi_1,\Phi_2)}$) and switching ($E^{\text{sw}}_{(\Phi_1,\Phi_2)}$) energy dissipations for each charge transfer cycle are calculated from Eqns. (5.18) and (5.22), respectively (line 8). The total energy dissipation and the balancing time are computed by multiplying the energy dissipation and the time for individual charge transfer cycles with N and are added for all charge transfer pairs (lines 11 and 12). The charge values of all cells in the battery pack are adjusted depending upon Q_{tx} and Q_{rx} (line 13). Based on this methodology, a system-level charge transfer simulation is performed in Section 8.3.1 using the proposed balancing architecture in Chapter 6.

5.4 Optimization of Active Cell Balancing Architectures

Using the closed-form, analytical model of the active cell balancing architecture derived in Section 5.2, optimization approaches for improving the performance of the equalization process are proposed in this section.

5.4.1 Optimal Dimensioning

Each active cell balancing module consists of an energy storage element and a switching network made of power MOSFETs. Several variants from commercial off-the-shelf components exist

as implementation choices for the energy storage elements and MOSFETs. Every feasible circuit configuration forming an active cell balancing unit has a significant impact on the performance in terms of energy-efficiency of the equalization process and installation area of the balancing unit. For instance, selecting an inductor with a high value of inductance L reduces the frequency of operation, thereby minimizing the switching energy dissipation across the MOSFET switches. However, a higher inductance value is obtained by winding more number of coils on a magnetic core which increases the installation area and might not be suitable for range-critical applications such as EVs and HEVs. On the other hand, choosing a low value inductor reduces the installation space, however affects the energy-efficiency at smaller values of balancing current due to very high frequency control signals. For example, a $3{,}5\,\mu\mathrm{H}$ inductor requires control signals in the range of $1{,}1\,\mathrm{MHz}$ for balancing with a peak current in the range of $1\,\mathrm{A}$. For this high frequency range, special type of MOSFETs with a lower turn-ON and turn-OFF delay are required. Moreover, the higher operating frequency will eventually result in an increased switching energy dissipation across the parasitic capacitances of the MOSFETs. A similar trade-off exists in the selection process of MOSFET switches for active cell balancing architectures. To minimize the conduction energy-dissipation across the MOSFET the parasitic *ON*-resistance (R_{M}) has to be minimum. This is achieved by increasing the channel width of the MOSFET switch which also results in an increased installation area. Moreover, the higher the size of the MOSFET switch the slower its transient performance and therefore, the turn-*ON* and turn-*OFF* delays are higher. This results in an increased switching energy-dissipation across the MOSFET switch.

5.4.2 Optimal Control

In addition to optimal dimensioning of active cell balancing components, the energy-efficiency of the equalization process can be significantly improved by optimizing the control point of operation. The source and destination cells of a charge transfer pair are identified by the active cell balancing strategies as explained in Section 5.3.1. In addition, the average value of the balancing current, I_{bal} with which the active cell balancing unit operates is predetermined by the equalization strategies depending upon the difference in charge levels between the source and destination cells and the time required to equalize them. While maintaining this average value of balancing current, two modes of operation of an active cell balancing architecture are possible by actuating the MOSFETs with control signals based on Pulse Frequency Modulation (PFM) technique. Depending upon the balancing current through the energy storage element, the operating modes of an active balancing architecture is classified into Discontinuous Transfer Mode (DTM) and Continuous Transfer Mode (CTM). For a given active cell balancing architecture the energy-efficiency for any specific value of the average balancing current can be significantly increased by appropriately choosing its operating point.

For the following explanation of the operating modes please refer to Fig. 5.7. In DTM, during the charging phase controlled by $\sigma^{1}_{\mathrm{DTM}}$, the current through the energy storage element starts from zero and rises until the peak value I_{peak}. During the discharge phase controlled by $\sigma^{2}_{\mathrm{DTM}}$, the current ramps down till zero, thereby transferring all the stored energy into the destination cell. Therefore, in DTM, the balancing current is fully discharged to zero after each charge

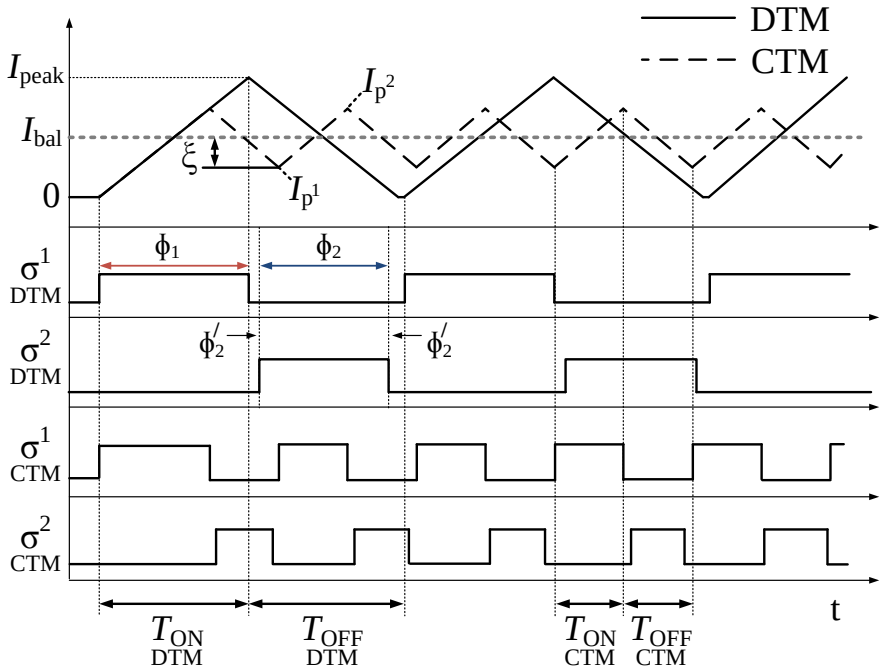


Figure 5.7: DTM and CTM operation of active cell balancing architectures. In DTM, the balancing current is fully discharged to zero after each charge transfer cycle, and in CTM, the balancing current is varied between two fixed points around average.

transfer cycle consisting of Φ_1 and Φ_2 as shown in Fig. 5.7. By contrast, in CTM the balancing current is never discharged to zero after each charge transfer cycle. Instead, the balancing current starts to rise from I_{p^1} to I_{p^2} during σ^1_{CTM} and discharges from I_{p^2} to I_{p^1} during σ^2_{CTM} as shown in Fig. 5.7b. Only during the initial time of σ^1_{CTM}, the current starts to rise from zero to I_{p^2} and similarly the last phase of σ^2_{CTM} where the stored energy is fully discharged to the destination cell. The points I_{p^1} and I_{p^2} are related to the average value of balancing current I_{bal} as

$$I_{p^1} = I_{\mathrm{bal}}(1-\xi) \tag{5.32}$$

$$I_{p^2} = I_{\mathrm{bal}}(1+\xi) \tag{5.33}$$

where ξ is the percentage of fluctuation around the average balancing current I_{bal}.

5.4.2.1 Influence on Energy-efficiency

The energy-efficiency of an active cell balancing architecture for any specific value of average balancing current depends upon the operating modes. For instance, in DTM operation, the peak value I_{peak} for a given average value of balancing current is higher compared to CTM operation as shown in Fig. 5.7. As a result a higher amount of charge (Q_{tx}) is transferred in each step, since the integration area in Fig. 5.7 is larger. Moreover, the switching energy dissipation explained in Section 5.2.3.2 in case of DTM operation is less compared to CTM operation, since the

MOSFETs in the active cell balancing unit are actuated with zero current across them. However, for higher values of average balancing currents, the peak current I_{peak} increases considerably and results in a higher amount of conduction energy dissipation as explained in Section 5.2.3.1. Therefore, a reduced peak value of the balancing current as in CTM is favorable for minimizing the conduction energy dissipation at higher values of balancing currents.

On the other hand, choosing an appropriate operating point ξ in case of CTM operation is also necessary. Even though, the conduction energy dissipation is minimized with low values of ξ, choosing an extremely low value, will result in the operating points I_{p^1} and I_{p^2} being very close to the average value of the balancing current. As a result, less charge is transferred in each cycle and more number of charge transfer cycles are required to equalize the source and destination cells. Moreover, in CTM operation, the MOSFETs in the active cell balancing unit are switched with non-zero currents which results in a higher switching energy-dissipation compared to DTM operation. Therefore, it is necessary to find an optimal control point ξ for each average value of the balancing current that provides an energy-efficient equalization process. For this purpose, the closed-form, analytical model for the charging and discharging phases of the active cell balancing process derived in Sections 5.2 has to be revised considering the DTM and CTM operations.

From Fig. 5.7, the initial value of the balancing current during charging phase in CTM operation is not zero, as assumed in the derivation of I_α in Eq. (5.8). Instead, the charging phase current starts with an initial value of I_{p^1} calculated according to Eq. (5.32). Therefore, the charging phase current in CTM operation is given by:

$$i_\alpha(t) = I_{\mathrm{p}^1}\left(e^{-\frac{R_\alpha}{L}t}\right) + \frac{V_{\mathrm{C}^\alpha}}{R_\alpha}\left(1 - e^{\frac{-R_\alpha}{L}t}\right) \tag{5.34}$$

Similarly, the peak value of the charging phase current in CTM operation is I_{p^2} and subsequently T_{ON} and Q_{tx} for CTM operation are obtained as:

$$T_{\mathrm{ON}} = -\frac{L}{R_\alpha} \cdot \ln\left[\frac{V_{\mathrm{C}^\alpha} - R_\alpha \cdot I_{\mathrm{p}^2}}{V_{\mathrm{C}^\alpha} - R_\alpha \cdot I_{\mathrm{p}^1}}\right] \tag{5.35}$$

$$Q_{\mathrm{tx}} = \frac{L}{R_\alpha}\left(I_{\mathrm{p}^1} - \frac{V_{\mathrm{C}^\alpha}}{R_\alpha}\right)\left[1 - e^{-\frac{R_\alpha}{L}T_{\mathrm{ON}}}\right] + \frac{V_{\mathrm{C}^\alpha}}{R_\alpha}T_{\mathrm{ON}} \tag{5.36}$$

Similar to the charging phase, the discharging phase current, time (T_{OFF}) and charge received (Q_{rx}) also changes for CTM operation as follows:

$$i_\beta(t) = I_{\mathrm{p}^2}\left(e^{-\frac{R_\beta}{L}t}\right) - \frac{V_{\mathrm{C}^\beta}}{R_\beta}\left(1 - e^{-\frac{R_\beta}{L}t}\right) \tag{5.37}$$

$$T_{\mathrm{OFF}} = -\frac{L}{R_\beta} \cdot \ln\left[\frac{V_{\mathrm{C}^\beta} + R_\beta \cdot I_{\mathrm{p}^1}}{V_{\mathrm{C}^\beta} + R_\beta \cdot I_{\mathrm{p}^2}}\right] \tag{5.38}$$

$$Q_{\mathrm{rx}} = \frac{L}{R_\beta}\left(I_{\mathrm{p}^2} + \frac{V_{\mathrm{C}^\beta}}{R_\beta}\right)\left[1 - e^{-\frac{R_\beta}{L}T_{\mathrm{OFF}}}\right] - \frac{V_{\mathrm{C}^\beta}}{R_\beta}T_{\mathrm{OFF}} \tag{5.39}$$

With non-zero initial and final currents during charging and discharging phases, respectively, the switching energy dissipation derived in Eqns. (5.20) and (5.21) has to be modified for CTM operation as:

$$E_{\Phi_1}^{\mathrm{SW}} = \frac{1}{2} \cdot \left(I_{\mathrm{p}^1} \cdot t_{\mathrm{ON}} + I_{\mathrm{p}^2} \cdot t_{\mathrm{OFF}}\right) V_{\mathrm{C}^\alpha} + \frac{1}{2} \cdot C_{\mathrm{OSS}} \cdot V_{\mathrm{C}^\alpha}^2 \tag{5.40}$$

$$E_{\Phi_2}^{\mathrm{SW}} = \frac{1}{2} \cdot \left(I_{\mathrm{p}^2} \cdot t_{\mathrm{ON}} + I_{\mathrm{p}^1} \cdot t_{\mathrm{OFF}}\right) V_{\mathrm{C}^\beta} + \frac{1}{2} \cdot C_{\mathrm{OSS}} \cdot V_{\mathrm{C}^\beta}^2 \tag{5.41}$$

Charging and discharging phase analytical model for DTM operation is derived in Sections. 5.2.1 and 5.2.2.

There is, as shown in this thesis, a significant potential for optimizing the design process of active cell balancing architecture. In the following the design metrics that are used to evaluate a certain component choice for the active cell balancing architecture and the critical parameters of the circuit components that affect the optimization objectives are introduced. Smart techniques to speed up the exploration process are outlined followed by the optimization algorithm that will be used in a case study performed in Section 8.3.2 for finding the optimal circuit configurations for an active cell balancing architecture.

5.4.3 Optimization Goals and Parameters

The design metrics that form the optimization objectives for evaluating the component choices are:

- **Energy dissipation:** Energy dissipated across the parasitic resistances and capacitances present in the circuit components during the charge transfer process.
- **Installation space:** Total area occupied by the components in each homogeneous module of the proposed architecture.
- **Balancing current:** The maximum value of the balancing current supported by the component choices determines the speed of the equalization process.

5.4.3.1 Energy dissipation

As discussed in Section 5.2.3 the two major sources of energy dissipation in an inductor-based active cell balancing architecture are:

- **Conduction losses:** Parasitic internal resistances of the circuit components dissipate heat when a current flows through them.
- **Switching losses:** Each switching activity of a MOSFET switch dissipates certain amount of energy due to the non-zero turn-on and turn-off times required for charging and discharging of the input parasitic capacitance.

Conduction losses. Influence of the parasitic resistances of the individual circuit components are included in the transferred (Q_{tx}) and received charges (Q_{rx}) modeled by Eqns. (5.36) and (5.39), respectively. Therefore, the conduction energy dissipation due to the parasitic resistances

of the circuit components is calculated by Eq. (5.18). The total parasitic resistances for both charging (R_α) and discharging (R_β) phases calculated from Eqns. (5.4) and (5.11), respectively are for a general inductor-based active cell balancing architecture. These equations are required to be modified in order to model the equivalent resistances during the charge transfer phases of the inductor-based active cell balancing architectures proposed in Chapter 6 of this thesis.

Switching losses. Each switching activity of a MOSFET dissipates energy due to charging and discharging of the input parasitic capacitances. For each MOSFET, when a control signal is applied, there is a characteristic delay time t_{ON}, during which the internal resistance of the transistor decreases to reach its specific ON resistance. This t_{ON} delay is caused by the time taken to fully charge the input capacitance of the MOSFET. Similarly, during the OFF period, the transistor does not switch to OFF instantaneously, because of the delay t_{OFF} that is caused by discharging its input capacitance. Moreover, the energy dissipation due to the discharge of the stored charge in the parasitic output capacitance C_{OSS} of the MOSFET during conduction also adds to the switching loss. The switching energy dissipations during both charging and discharging phases are derived in Eqns (5.40) and (5.41), respectively. The total switching energy dissipation is the sum of the individual losses in each phase. The overall energy dissipation during the charge transfer process is the sum of both conduction and switching energy dissipations as given by:

$$E^{\mathrm{tot}}_{(\Phi_1,\Phi_2)} = E^{\mathrm{cd}}_{(\Phi_1,\Phi_2)} + E^{\mathrm{sw}}_{(\Phi_1,\Phi_2)} \tag{5.42}$$

For a given active cell balancing architecture the objective of the optimization approach is to find circuit configurations for which the total energy dissipation is minimum.

5.4.3.2 Installation area

The active cell balancing architectures that are proposed in Chapter 6 of this thesis consist of homogeneous units that are attached with individual cells of the battery pack. Therefore, a reduced installation area of the components forming the homogeneous units of active cell balancing architecture is favorable for integration with the cell. The reduced installation area of the circuit components also ensures that the weight occupied by the PCB implementation of the homogeneous units is also minimum, enabling a higher driving range for EV and HEV applications. Depending upon the functionality of the MOSFET switch, the amount of current carried and the the size of the switch increases. The total area of a single modular unit of our proposed architecture is calculated as the sum of area of the individual components in the balancing unit. Architecture specific details for calculating the installation area of all proposed active cell balancing architectures are discussed in Section 8.3.2.

5.4.3.3 Balancing Current

Balancing current is an important design metric for optimizing the component choices of the active cell balancing architecture. A higher value of the balancing current will enable a faster equalization process of the battery pack. The high equalization speed is extremely important in future scenarios where a higher number of EVs are designed for fast charging applications. Therefore, balancing with a higher current is beneficial in terms of equalization speed. However,

Inductor	Symbol	MOSFET	Symbol	Objectives	Goal
Inductance	L	O/p capacitance	C_{OSS}	Energy dissipation	*Minimize*
Maximum current	I_{L}	Maximum current	I_{M}	Installation area	*Minimize*
Resistance	R_{L}	Resistance	R_{M}	Balancing current	*Maximize*
Area	A_{L}	Area	A_{M}		
		ON delay	t_{ON}		
		OFF delay	t_{OFF}		

Table 5.1: Parameters of the circuit components and the optimization objectives of active cell balancing architectures.

with higher values of balancing current, the energy dissipation across the parasitic resistances of the circuit components also increase. Therefore, the circuit components forming the active cell balancing architecture must be selected such that they allow balancing with a higher value of current while maintaining reduced energy dissipation.

5.4.3.4 Parameters

Table 5.1 lists the critical parameters of the circuit components involved in each module of the active cell balancing architecture that influence the optimization objectives. For instance, a lower inductance value L of the inductor denotes a reduced number of windings and installation area. However, with a reduced inductance, less amount of charge is transferred in each switching cycle and as a result the number of cycles required to equalize the battery pack increases. This eventually results in an increased switching energy dissipation across the MOSFET switches. Similar kind of trade-offs exist for all parameters of the circuit components listed in Table 5.1. In the following section, a framework for identifying optimal device combinations from a set of inductors and MOSFETs that satisfy the optimization objectives listed in Table 5.1 is proposed.

5.4.4 Design Space and Speed-up Techniques

The optimization algorithm performs an exhaustive search over the entire design space to find out the optimal combinations of inductors and MOSFETs. This means simulating the system-level simulation algorithm explained in Section 5.3.2 for each peak value of the balancing current with all available possible combinations of inductors, MOSFETs and control points (ξ). If $I = \{I_1, I_2, ...I_n\}$ is the set of possible peak balancing currents, $L = \{L_1, L_2, ...L_n\}$ is the set of inductors, $M = \{M_1, M_2, ...M_n\}$ is the set of MOSFETs and $\xi = \{\xi_1, \xi_2, ...\xi_n\}$ is the set of control points in CTM operation, then the set of possible circuit configurations that needs to be simulated using Algorithm 1 is:

$$C_c = L \times M \times \xi \tag{5.43}$$

Moreover, certain active cell balancing architectures proposed in Chapter 6 consists of MOSFET switches that are required to carry different values of current and as a result the design space

to be explored increases. Performing the charge transfer simulation using Algorithm 1 for all possible component choices as stated above will involve considerable amount of time. The following methods are adopted to speed up the exploration process.

- Pruning the design space based on the maximum possible current limit
- Architectural symmetry of the balancing modules
- Pruning the design space of slow switching MOSFETs
- Pruning the design space of operating points
- Reducing the simulation space

5.4.4.1 Pruning based on current limit

All components in the active cell balancing unit have a maximum possible current limit beyond which they fail. For instance, operating an inductor at a current above its maximum rated value will lead to saturation, where the inductance property of the inductor is lost and behaves like a wire short-circuiting the battery cell. Similar condition applies for the MOSFETs where operating at a higher current value than the specified maximum range will heat up the device and eventually lead to breakdown. Therefore, all devices must be operated within their maximum possible current limit to ensure safe operation. Filtering the set of combinations C_c based on their rated current and the desired balancing current reduces the component choices in the design space that needs to be optimized for the goals listed in Table 5.1.

5.4.4.2 Architectural symmetry

All proposed active cell balancing architectures consist of homogeneous units. Therefore, an optimal solution for an architecture will not have different components in each module since they all perform the same function. This reduces the possible combinations in the design space of an active cell balancing architecture for an entire battery pack. Furthermore, within each module certain architectural symmetry exists and this can be utilized to further constrain the configuration choices of MOSFETs. For example, MOSFETs that carry the same amount of current or actuated with similar type of control signals can be uniform, i.e. they can all be of the same type. An optimal solution in any case will not have different MOSFET devices for the same type of functionality they perform. This further reduces the number of combinations in the design space that needs to be optimized.

5.4.4.3 Pruning the design space of slow switching MOSFETs

In all balancing units certain MOSFETs are actuated using high frequency control signals for performing charge transfer and there are MOSFETs that are set statically to either *ON* or *OFF*. These statically set MOSFETs will be termed as slow switching MOSFETs in the rest of this thesis. In certain balancing architectures proposed in Chapter 6 of this thesis, there may be more than one type of slow switching MOSFETs due to their different current requirements. As seen

from Section 5.4.3.1, the energy dissipation of an active cell balancing architecture is classified into conduction and switching energy dissipations. While the switching energy dissipation is due to the frequent turn-*ON* and turn-*OFF* activity of the MOSFETs actuated with high frequency control signals, the conduction energy dissipation is mainly due to the parasitic resistances of the circuit components. Since these slow switching MOSFETs are not actuated with high frequency control signals, their main contribution to the energy dissipation metric is the conduction losses due to their parasitic *ON*-resistance. Therefore, initial pruning of the design space of these slow switching MOSFETs could be performed on the basis of their parasitic resistances and installation area to identify the dominated combinations.

5.4.4.4 Pruning design space of operating points

The energy efficiency of an active cell balancing architecture is significantly influenced by its mode of operation. For the same value of average balancing current, the DTM operation will have the inductor current to be fully discharged to zero after each switching cycle, whereas, the CTM operation varies the current through the inductor between two fixed points. The energy dissipation in DTM operation will be higher if the average value of balancing current and the parasitic resistances of components are higher. By contrast, operating in CTM very close to the average value of the balancing current will result in an increased switching energy dissipation due to the higher amount of charge transfer cycles required to equalize the charge difference between cells. Therefore, each circuit configuration of the active cell balancing needs to be evaluated with the set of operating points $\xi = \{\xi_1, \xi_2, ...\xi_n\}$. However, for some configurations of inductors and MOSFETs in the design space, certain values of operating points ξ are not possible. The times T_{ON} and T_{OFF} required by a certain configuration C_{c1} while operating at ξ_p might be less than the turn-*ON* (t_{ON}) and turn-*OFF* (t_{OFF}) delays of the MOSFET switch. In such cases, the configuration C_{c1} cannot be operated at ξ_p and therefore it is not required to evaluate this operating point for the particular configuration. This initial filtering of the design space for each configurations provides additional speed up of the exploration process.

5.4.4.5 Reducing simulation space

Each possible circuit configuration in C_c is evaluated by performing a system-level performance simulation using the Algorithm 1 described in Section 5.3.2. However, this increases the runtime of the exploration process particularly when the design space is considerably large. In contrast to this, for checking whether a configuration C_{c1} will dominate C_{c2} on a system-level scope, it is sufficient to evaluate their performances for a neighbor-only charge transfer case. This is due to the fact that the energy dissipation for a charge transfer between neighboring cells is always less than the energy dissipation for a charge transfer between non-neighboring cells, using the same balancing architecture and circuit configuration due to the increased parasitic resistances in case of non-adjacent charge transfers. In other words, if a configuration C_{c1} dominates C_{c2} on all optimization objectives listed in Table 5.1 for a charge transfer between neighboring cells then it will also dominate C_{c2} in case of a system-level analysis. Therefore, it is sufficient to evaluate all configurations of inductors and MOSFETs for a charge transfer between neighboring cells to identify the Pareto-optimal design configurations of an active cell balancing architecture.

Algorithm 2 Design space pruning and identification of possible design configurations.

Input:

Set of balancing currents $I_{peak} = \{I_1, I_2, ...I_n\}$
Set of inductors $L_{\text{ind}} = \{L_1, L_2, ..., L_n\}$
Set of MOSFETs $M = \{M_1, M_2, ..., M_n\}$
Set of control points $\xi = \{\xi_1, \xi_2, ...\xi_n\}$
Source and destination cell SoCs σ and δ

Output:

Set of possible design configurations C_c

1: **for** all C_c in $I_{peak} \times L_{\text{ind}} \times M \times \xi$ **do**
2: **if** $m \cdot I_L < I_{\text{peak}}$ or $m \cdot I_M < I_{peak}$ or $T_{\text{ON}} < t_{\text{ON}}$ or $T_{\text{OFF}} < t_{\text{OFF}}$ **then**
3: The selected configuration is *infeasible*
4: **else**
5: $E_{\text{diss}} = 0$
6: **while** $\sigma - \delta > 0.1\%$ **do**
7: Calculate Q_{tx} and Q_{rx}
8: Calculate $E^{\text{tot}}_{\Phi_1,\Phi_2}$ for each charge transfer cycle
9: $E_{\text{diss}} = E_{\text{diss}} + E^{\text{tot}}_{\Phi_1,\Phi_2}$
10: Adjust σ and δ according to Q_{tx} and Q_{rx}
11: **end while**
12: $A_{\text{balancing}} = A_{\text{ind}} + A_{\text{MOSFET}}$
13: Add configuration to C_c
14: **end if**
15: **end for**

5.4.5 Optimization Algorithm

The optimization algorithm that implements the design space exploration process along with the speed-up techniques discussed from Section 5.4.4.1 to Section 5.4.4.5 is shown in Algorithm 2. The design space to be explored for optimal circuit configurations is the Cartesian product of I_{peak} (set of balancing currents), L_{ind} (set of inductors), M (set of MOSFETs) that can be operated at several control points in ξ. If the balancing architecture consists of different types of slow switching MOSFETs depending upon their functionality, then the design space is filtered using the technique presented in Section 5.4.4.3. Further filtration of the design space based on the maximum allowable current of each device, symmetry of the balancing architecture and operating points validity as discussed in Sections 5.4.4.1, 5.4.4.2 and 5.4.4.4, respectively are performed in line 2. Any design configuration of inductors and MOSFETs that satisfies these filtering criteria are considered as *infeasible* (line 3) and are not further evaluated. On the other hand, configurations that do not satisfy these criteria can be used in an active cell balancing architecture and requires to be optimized for energy dissipation, installation area and balancing current. The selected configurations are further evaluated for energy dissipation using the closed-form analytical model developed in Chapter 5.

For each configuration, the transferred and received charges for each control point ξ are calculated using Eqns (5.36) and (5.39), respectively. From that the conduction energy dissipation ($E^{\mathrm{cd}}_{(\Phi_1,\Phi_2)}$) and the switching energy dissipation ($E^{\mathrm{sw}}_{(\Phi_1,\Phi_2)}$) for each charge transfer cycle are calculated from Eqns (5.18) and (5.22), respectively. The total energy dissipation, which is the sum of the conduction and switching energy dissipations, is calculated as shown in line 9. The charge levels of the source and destination cells are updated depending upon the transferred and received charges as shown in line 10. These steps are executed until the difference in SoCs of source and destination cells (σ and δ) is less than $0{,}1\,\%$ (line 6). The installation area of a homogeneous active cell balancing module for each configuration is calculated in line 12. The above algorithm finds the energy dissipation and installation area for all feasible combinations of balancing currents, inductors and MOSFETs. From this, Pareto-optimal design points that are not dominated by other configurations for all optimization objectives listed in Table 5.1 are identified. Each configuration is compared with other feasible combinations for dominance in terms of balancing current, energy dissipation and installation area. A circuit configuration C_{c_1} is said to dominate another device choice C_{c_2} if

$$I^{\mathrm{peak}}_{C_{c_1}} > I^{\mathrm{peak}}_{C_{c_2}} \text{ and } E^{\mathrm{diss}}_{C_{c_1}} < E^{\mathrm{diss}}_{C_{c_2}} \text{ and } A_{C_{c_1}} < A_{C_{c_2}}$$

5.4.5.1 Dynamic control

Active cell balancing strategies as discussed in Section 5.3.1 determines the source and destination cells of the charge transfer pair based on the SoC distribution of individual cells in the battery pack. Furthermore, as discussed in the performance-related design goals of an active cell balancing architecture in Section 4.2.2.1, the energy-efficiency of an equalization process is significantly improved by performing direct charge transfer between non-adjacent cells. However, the optimization methodology described above identifies energy-efficient control points of operation for an optimal device choice while performing neighbor-only charge transfers. An optimal operating point for a neighbor-only charge transfer case might not be optimal when the balancing takes place between non-adjacent cells. This is due to the fact that the total parasitic resistances in the charge flow direction increases depending upon the number of cells that are in between the source and destination cells of the charge transfer pair.

Depending upon d, the number of balancing modules that are in between the source and destination cells of the charge transfer pair, the equivalent resistances and the conduction energy dissipation of a circuit configuration changes. Therefore, the optimal control point of operation of an active cell balancing architecture also changes when performing non-neighbor balancing. As a result, finding an optimal control point dynamically depending upon the position of the source and destination cell of the charge transfer pair is mandatory to improve the energy-efficiency of the balancing process. In reality, the designer identifies the optimal circuit configuration of the active cell balancing architecture depending upon his current, energy dissipation and installation area requirements. For each value of d using the identified optimal circuit configuration the total parasitic resistances in each phase of the charge transfer process can be calculated by adding the individual parasitic resistances in the current flow path. Using the simulation methodology presented in Algorithm 1, the optimal control point for each value of d for the specific circuit

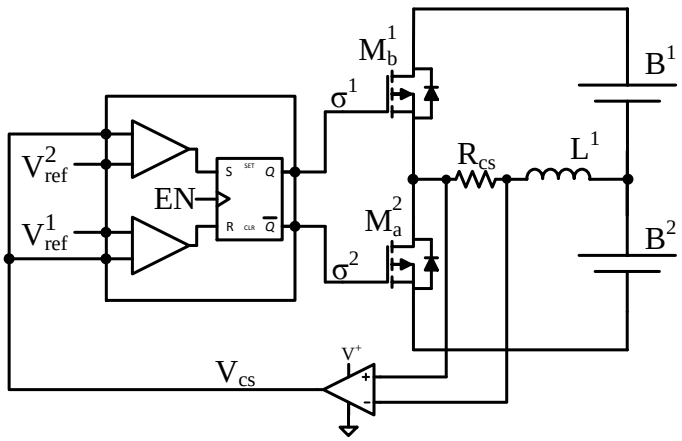


Figure 5.8: Control circuit for maintaining the balancing current through the inductor within the optimal points I_{p^1} and I_{p^2}.

configuration is then calculated in advance and programmed in the individual cell-level controller that generates the necessary control signals for the charge transfer.

While in operation, depending upon the source and destination cells identified by the equalization strategies, the active cell balancing architecture is operated at the appropriate optimal operating point (ξ_p) that is precomputed for each charge transfer pair. The balancing current through the inductor is maintained within I_{p^1} and I_{p^2} by the cell-level controller using the control circuit provided in Fig. 5.8. Series resistor R_{cs} generates a voltage V_{cs} proportional to the balancing current through the inductor, which is amplified by using a Current Sense Amplifier (CSA) as shown in Fig. 5.8. Depending upon the optimal control points I_{p^1} and I_{p^2} reference voltages V^1_{ref} and V^2_{ref} are computed by the cell-level controller. The balancing current measurement V_{cs} is compared with these reference voltages as shown in Fig. 5.8. When V_{cs} is greater than V^1_{ref} the control signal σ^1 is used to actuate MOSFET M^1_a to charge the inductor from the source cell B^α. The stored energy in the inductor is discharged to the destination cell B^β by actuating MOSFET M^1_b with control signal σ^2, when the value of V_{cs} exceeds V^2_{ref} which represents I_{p^2}. The reference voltages V^1_{ref} and V^2_{ref} can be dynamically changed with the help of a Digital to Analog Converter (DAC) converter depending upon the value of d.

5.5 Summary

A generalized modeling methodology of active cell balancing architectures was proposed in this chapter. Sources for energy dissipation and detailed analytical models for energy-efficiency are derived. Based on these analytical models, an approach for performing system-level simulation of active cell balancing process is explained. Optimization approaches for improving the energy-efficiency by optimal dimensioning of components and control policy are proposed.

6

Proposed Modular Active Cell Balancing Architectures

Based on the design requirements of active cell balancing architectures for distributed BMS topologies outlined in Chapter 4, three different modular balancing architectures are proposed in this chapter, using inductors or transformers as energy storage elements. Inductor and transformer based active cell balancing approaches are more preferable compared to capacitor-based active cell balancing architectures, since charging a capacitor directly from a battery will result in $50\,\%$ energy dissipation across its parasitic resistances. All proposed balancing architectures can be modularized into individual homogeneous units that can be attached to each cell and controlled locally by the respective cell-level controllers of the distributed BMS. Operating principle of each of the proposed architecture and their charge transfer patterns are explained in detail. Moreover, control scheme for operating the balancing architectures to perform different charge transfer scenarios are outlined for each of the proposed balancing architecture.

6.1 Isolating Non-neighbor Balancing Architecture

As discussed in Section 4.2.2, if the imbalanced cells are not adjacent in the power line connection of the battery pack, then transferring the excess charge directly between them provides higher energy-efficiency compared to shuttling the excess charge through the intermediate cells. This is due to the fact that each charge transfer activity incurs a certain amount of loss introduced by the parasitic resistances and capacitances present in the circuit components. Moreover, by performing direct charge transfers between non-adjacent cells, SoH of the intermediate cells is preserved by reducing its charge/discharge cycles.

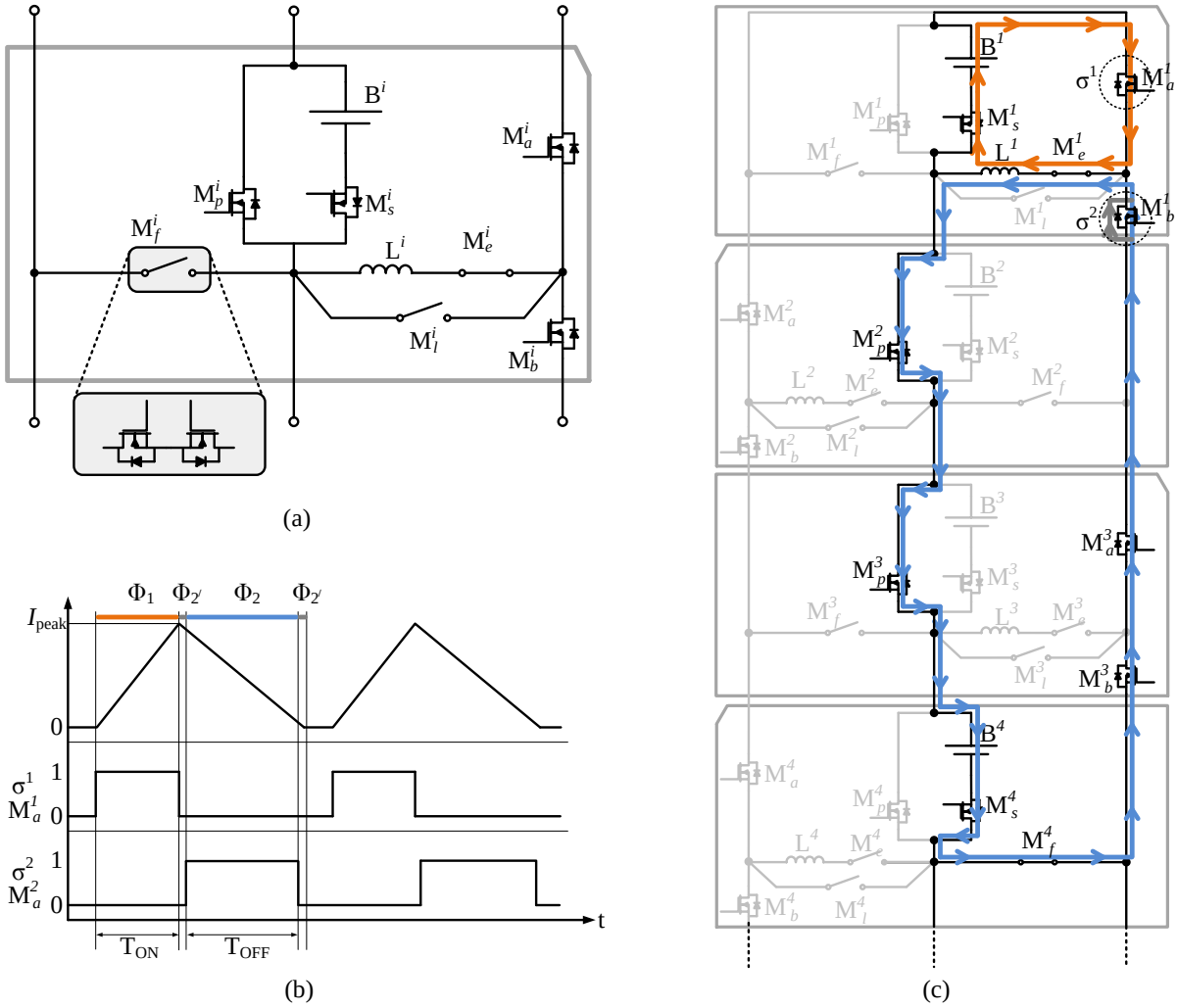


Figure 6.1: Cell-isolating inductor-based active cell balancing architecture. (a) Each homogeneous unit of the proposed active cell balancing architecture consists of 10 MOSFETs and an inductor. (b) Control signals for actuating MOSFETs in the individual balancing unit. (c) System-level representation of the proposed balancing architecture showing an example of direct charge transfer between non adjacent cells ($B^1 \rightarrow B^4$).

6.1.1 Homogeneous Balancing Unit

For enabling such direct charge transfer between non adjacent cells, an isolating non-neighbor active cell balancing architecture is proposed in this thesis. A single modular unit of the proposed active cell balancing architecture is shown in Fig. 6.1a. Each module consists of 10 MOSFET switches and an inductor, which is used as the temporary energy storage element. M_p^i and M_s^i are parallel and series MOSFETs, respectively, that are used to isolate the associated battery cell B^i from the power line and route the balancing current across the cell during non-neighbor balancing. They are high power MOSFETs capable of carrying the entire battery pack current

and have very low *ON*-resistance in the range of $\mathrm{m}\Omega$ to prevent conduction energy dissipation. M_a^i and M_b^i are fast switching MOSFETs actuated with non-overlapping high frequency control signals that enable charge transfer from the source cell to the inductor and from the inductor to the destination cell, respectively. MOSFETs M_e^i, M_f^i and M_l^i are bi-directional switches that are connected in such a way that their internal parasitic body-diodes are blocking each other from conduction. This provides complete isolation and are used to direct the flow of balancing current accordingly. Each cell of a series-connected battery pack is associated with the proposed modular active cell balancing unit and these individual units are interconnected with other units to realize a system-level active cell balancing architecture as shown in Fig. 6.1c.

6.1.2 Working Principle

The proposed inductor-based active cell balancing architecture works on a similar operating principle of buck-boost type DC-DC converters explained in Section 2.3. An example for a direct charge transfer between nonadjacent cells using our proposed active cell balancing architecture is shown in Fig. 6.1c. Here, excess charge from cell B^1 is directly transferred to cell B^4 using the inductor L^1 without involving the intermediate cells B^2 and B^3. For this purpose, during the initialization phase, cells B^2 and B^3 are isolated from the charge flow path by actuating MOSFETs M_p^2, M_p^3 and opening M_s^2 and M_s^3, respectively. Similarly, the bi-directional switches M_e, M_f and M_l in all modules are actuated accordingly, in order to aid the flow of balancing current between B^1 and B^4. Parts of the circuit that are not used during charge transfer process are grayed out in Fig. 6.1c for better visibility. The charge transfer process is controlled by actuating MOSFETs M_a^1 and M_b^1 by non-overlapping control signals σ^1 and σ^2 as shown in Fig. 6.1b.

During the charging phase Φ_1, MOSFET M_a^1 is actuated with signal σ^1 as shown in Fig. 6.1b. The inductor L^1 gets charged from cell B^1 and its current increases linearly as shown in Fig. 6.1b till a peak value I_{peak}, determined by the maximum current limit of the inductor. At time $t = T_{\mathrm{ON}}$, the inductor charging is stopped by opening M_a^1. The current through the inductor cannot be interrupted abruptly due to its inherent property and as a result the voltage across the inductor reverses in order to discharge its stored energy. This polarity reversal of the inductor voltage forward biases the internal parasitic body-diode of MOSFET M_b^1 as shown in Fig. 6.1c. The balancing current through the inductor freewheels over the MOSFET body-diode charging cell B^4, marked as phase Φ_2' in Fig. 6.1b. To minimize the losses incurred by balancing over the body-diode of the MOSFET, M_b^1 is actuated with σ^2 (Fig. 6.1b) to divert the balancing current through the low resistance MOSFET channel path. Likewise, the remaining amount of energy in the inductor is discharged over the body-diode, to prevent the inductor from being charged in the opposite direction. This completes one charge transfer cycle consisting of times T_{ON} and T_{OFF}. The times T_{ON} and T_{OFF} of the control signals σ^1 and σ^2, respectively and the amount of charge transferred Q_{tx} by the source cell and the amount of charge received by the destination cell Q_{rx} for each charge transfer cycle are obtained from the closed-form analytical models derived in Chapter 5.

	States	Description	Switching Configuration						
			M_a^n	M_b^n	M_p^n	M_s^n	M_e^n	M_f^n	M_l^n
1.	$\exists p \in \mathcal{T} : n \in \mathrm{S} \wedge \tilde{n} \in \mathrm{D} \wedge n < \tilde{n}$	Source cell above the destination cell	σ^1	σ^2	0	1	1	0	0
2.	$\exists p \in \mathcal{T} : n \in \mathrm{S} \wedge \tilde{n} \in \mathrm{D} \wedge n > \tilde{n} \wedge \lvert n - \tilde{n} - 1 \rvert \% 2 = 0$	Source cell below the destination cell	0	0	0	1	0	1	0
	$\exists p \in \mathcal{T} : n \in \mathrm{S} \wedge \tilde{n} \in \mathrm{D} \wedge n > \tilde{n} \wedge \lvert n - \tilde{n} - 1 \rvert \% 2 \neq 0$		1	0	0	1	0	0	1
3.	$\exists p \in \mathcal{T} : n \in \mathrm{D} \wedge \tilde{n} \in \mathrm{S} \wedge n < \tilde{n}$	Destination cell above the source cell	σ^2	σ^1	0	1	1	0	0
4.	$\exists p \in \mathcal{T} : n \in \mathrm{D} \wedge \tilde{n} \in \mathrm{S} \wedge n > \tilde{n} \wedge \lvert n - \tilde{n} - 1 \rvert \% 2 = 0$	Destination cell below the source cell	0	0	0	1	0	1	0
	$\exists p \in \mathcal{T} : n \in \mathrm{D} \wedge \tilde{n} \in \mathrm{S} \wedge n > \tilde{n} \wedge \lvert n - \tilde{n} - 1 \rvert \% 2 \neq 0$		1	0	0	1	0	0	1
5.	$\exists p \in \mathcal{T} : n \in d(p) \wedge n \notin \mathrm{S} \wedge \tilde{n} \notin \mathrm{D} \wedge \lvert n \rvert \% 2 = 0$	Forwarding	0	0	1	0	0	0	0
	$\exists p \in \mathcal{T} : n \in d(p) \wedge n \notin \mathrm{S} \wedge \tilde{n} \notin \mathrm{D} \wedge \lvert n \rvert \% 2 \neq 0$		1	1	1	0	0	0	0
6.	$\forall p \in \mathcal{T} : n \notin d(p)$	No charge Transfer	0	0	0	0	0	0	0

Table 6.1: Switching configuration of MOSFETs in the balancing unit for all possible states of the associated cell. 0, 1 means that the MOSFET is statically *OFF* or *ON*, respectively and σ^1, σ^2 means they are controlled by non-overlapping high frequency control signals shown in Fig. 6.1b.

6.1.3 Control Scheme

In this section, control scheme for operating all the MOSFET switches in each module is derived for enabling charge transfer between cells using the proposed active cell balancing architecture. The switching rules for the MOSFETs in the balancing unit depend upon whether the associated battery cell is a source or destination or a cell in between the source and destination cell of a charge transfer pair. The derived switching rules are verified for correctness using a design automation framework developed in [15] in order to avoid potential short circuits between cells.

A battery pack consists of a set of $\mathcal{N} = \{1, ..., N\}$ series-connected cells and each cell $n \in \mathcal{N}$ is associated with an individual balancing unit that has an inductor L^n and a set of MOSFETs $M^n = \{M_a^n, M_b^n, M_p^n, M_s^n, M_e^n, M_f^n, M_l^n\}$. A transfer scenario is defined by $\mathcal{T}$ that consists of multiple charge transfer pairs $p = (\mathrm{S}, \mathrm{D}) \in N$ formed by source cells $\mathrm{S} \subseteq N$ and destination cells $\mathrm{D} \subseteq N$ that are disjoint. Moreover, each transfer pair forms a domain

$$d(p) = \{\min(n | n \in \mathrm{S} \cup \mathrm{D}), .., \max(n | n \in \mathrm{S} \cup \mathrm{D})\}$$

and the domains are disjoint in order to avoid short circuits between cells. Depending upon the transfer scenario $\mathcal{T}$, the switching configuration of each MOSFET is:

$$s(\mathcal{T}, M) \in \{0, 1, \sigma^1, \sigma^2\} \tag{6.1}$$

where 0 represents that the switch is *OFF*, 1 denotes that it is *ON*, σ^1 and σ^2 are non-overlapping control signals shown in Fig. 6.1b.

Table 6.1 presents the switching configuration of MOSFETs in the balancing unit depending upon the state of the associated cell. State 1 represents the case where the source cell of the charge transfer pair is above the destination cell and the corresponding configuration for actuating the MOSFETs in the associated balancing unit is provided. Switching configurations in state 2 applies when the source cell of the charge transfer is below the destination cell. Depending upon the number of cells that are in between the source and destination cells of the charge transfer pair two different sets of switching configuration are applied correspondingly. State 3 applies to the

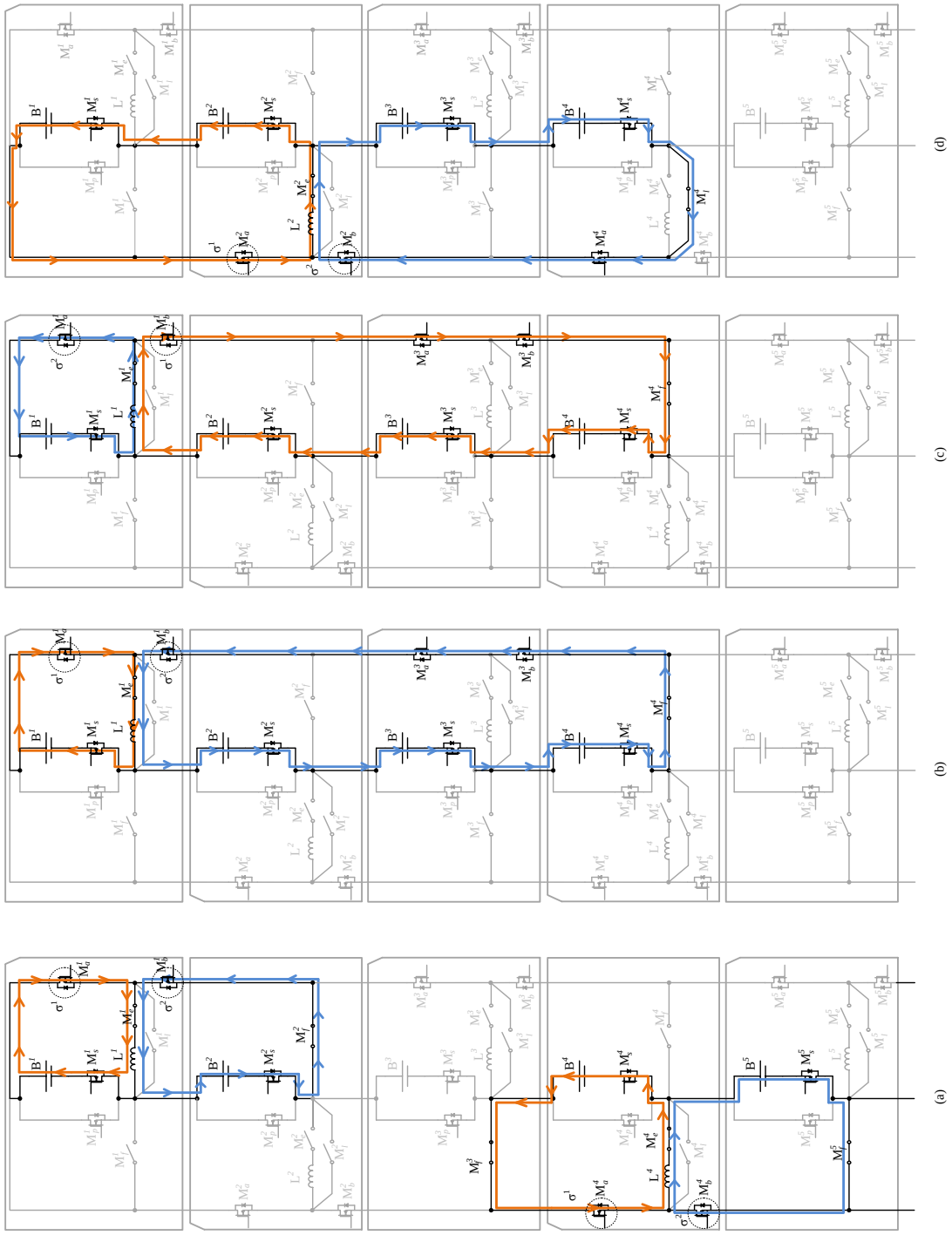


Figure 6.2: Possible charge transfer scenarios of cell-isolating inductor-based active cell balancing architecture.(a) Concurrent charge transfers between $B^1 \rightarrow B^2$ and $B^4 \rightarrow B^5$, while B^3 is in blocking mode. (b) One cell to many cells, $B^1 \rightarrow B^2, B^3, B^4$. (c) Many cells to one, $B^2, B^3, B^4 \rightarrow B^1$. (d) Many cells to many cells, $B^1, B^2 \rightarrow B^3, B^4$.

MOSFETs in the balancing unit associated with the destination cell that is above the source cell of the charge transfer pair. Similarly, if the destination cell is below the source cell two sets of switching configuration for the MOSFETs in the balancing applies depending upon the number of cells that are in between the source and destination cell. State 5 is the switching configuration for MOSFETs in the balancing unit that are associated with the cell that is in between the source and destination cells of the charge transfer pair. Finally, if a cell is not involved in the charge transfer process, the MOSFETs in the respective balancing unit are configured according to State 6.

6.1.4 Possible Charge Transfer Scenarios

In this section, charge transfer scenarios that are possible with the proposed active cell balancing architecture are discussed. Fig 6.2 shows the different charge transfer patterns that can be achieved using the proposed balancing architecture. Fig. 6.2a depicts the concurrent charge transfer feature of the proposed architecture. Here charge from cell B^1 is transferred to cell B^2 and at the same time charge from cell B^4 is transferred to cell B^5. Note that adjacent cells of a charge transfer pair, in this example B^3 and B^6 considering the charge transfer pair is B^4 and B^5, are required to be in blocking mode and cannot take part in another charge transfer process. As a result the maximum percentage of concurrency that is possible with the proposed architecture is limited to $66\,\%$ for a given battery pack. Fig. 6.2b shows the capability of transferring charge from one cell to multiple cells in the battery pack. Here excess charge from cell B^1 is transferred to cells B^2, B^3 and B^4 through inductor L^1. Similarly, the proposed balancing architecture is capable of transferring charge from multiple cells to a single cell in the battery pack. This feature is depicted in Fig. 6.2c, where charge from cells B^2, B^3 and B^4 are transferred to cell B^1. Finally, the proposed balancing architecture also supports charge transfers between groups of cells as shown in Fig. 6.2d, where cells B^1 and B^2 transfer charge to cells B^3 and B^4, respectively.

6.1.5 Advantages and Disadvantages

The proposed active cell balancing architecture consist of only 10 MOSFET switches and is capable of performing direct charge transfers between non-neighboring cells. Compared to existing approaches [77] and [54] which perform charge transfers only between adjacent cells, the proposed architecture increases the energy-efficiency of the charge transfer process. Moreover, the proposed active cell balancing enables multiple charge transfer patterns such as cell-to-cell, cell-to-pack and pack-to-cell as shown in Section 6.1.4. In addition, the cell isolation feature enabled by MOSFET switches M_p^i and M_s^i, allows individual cell to be isolated from the battery pack during malfunctioning. This also prevents overcharging scenarios, where all cells are charged in series with the same current and the individual cells when fully charged can isolate from the power line resulting in an uniform charging of the battery pack. However, the cell isolation switches M_p^i and M_s^i during normal operation incurs high power dissipation due to their non-zero parasitic *ON*-resistance. This power dissipation can be minimized by placing multiple MOSFETs in parallel which eventually reduces their *ON*-resistance and thereby power dissipation. In contrast, the power dissipation across the MOSFETs can also be minimized by

connecting multiple cells in parallel which will reduce the current flowing through individual isolation switches. Since the balancing architecture isolates the intermediate cells to perform charge transfer, equalization cannot be performed when the battery pack is in operation. In order to achieve balancing while the battery pack is charged or discharged either additional spare cells or switches or high frequency control signals are required.

6.2 Parallel-attached Active Cell Balancing Architecture

In order to avoid the high power dissipation across the cell isolation switches explained in the previous section and to enable non-neighbor charge transfer during discharging process of the battery pack, a parallel-attached inductor-based non-neighbor charge transfer architecture is proposed in this section. Each module consists of homogeneous blocks that are attached in parallel to the cells and the system-level architecture is formed by interconnecting these homogeneous units.

6.2.1 Homogeneous Balancing Unit

A single unit of the proposed parallel-attached balancing architecture is shown in Fig. 6.3a. Each block consists of 8 low-power MOSFET switches and an inductor. As shown in Fig. 6.3a the balancing unit is attached in parallel to each cell and therefore the proposed architecture can be used during the discharging process of the battery pack also.

Balancing between cells is facilitated by the charge transfer bus BB^+ and BB^- as shown in Fig. 6.3a. The battery cell is connected alternatively to the charge transfer bus using the power MOSFETs. MOSFETs M_h^i and M_g^i connect the positive and negative terminals of the battery cell to BB^- and BB^+, respectively. By contrast, M_a^i, M_c^i and M_b^i, M_d^i connect the positive and negative terminals of the battery cell to BB^+ and BB^-, respectively. Therefore, these MOSFETs are always actuated with complimentary control signals in order to avoid potential short circuit of the cell. Finally, MOSFETs M_{BB+}^i and M_{BB-}^i enable to isolate the charge transfer bus between the modules, in order to facilitate concurrent charge transfers between cells. Each cell of the battery pack is associated with such a homogeneous unit and they are interconnected through the charge transfer bus to form the system-level active cell balancing architecture as shown in Fig. 6.3c.

6.2.2 Working Principle

Fig. 6.3c shows an example charge transfer between non-adjacent cells B^1 and B^3 using the proposed architecture. For this purpose, certain MOSFETs are actuated with any of the two high frequency complimentary control signals σ^1 and σ^2 as shown in Fig. 6.3b and certain MOSFETs are statically turned *ON* or *OFF* in order to aid the flow of balancing current. Switches that are *OFF* and parts of the circuit that are not used during the charge transfer process are grayed out in Fig. 6.3c for better visibility of the current flow path.

In this example, the inductor in the balancing unit associated with cell B^1 is used for performing the charge transfer. Cell B^3 is connected to the charge transfer bus by actuating

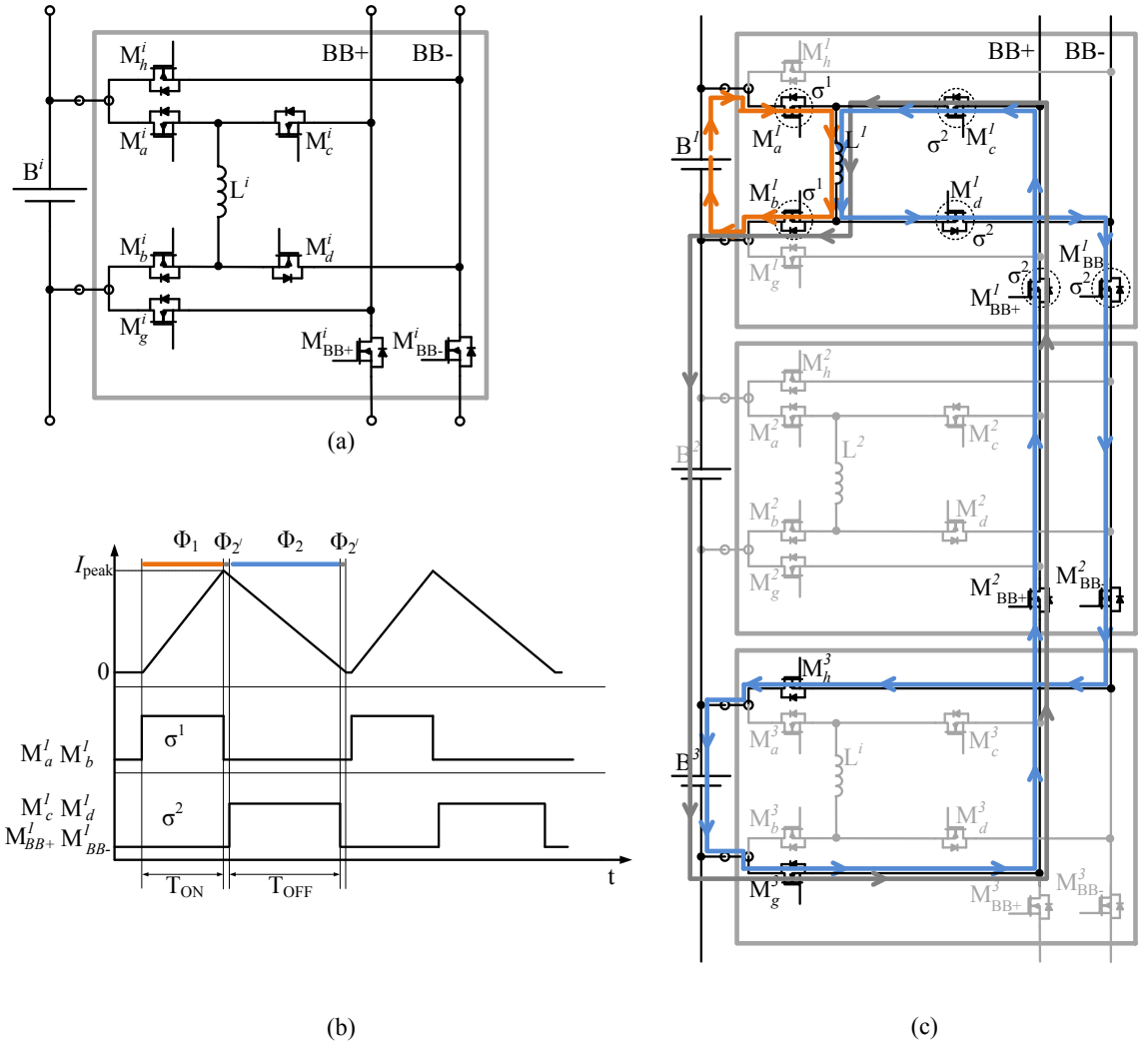


Figure 6.3: Parallel-attached inductor-based active cell balancing architecture. (a) Homogeneous unit of the proposed parallel attached active cell balancing architecture consisting of 8 MOSFET switches and an inductor as energy storage element. (b) Control signals for enabling charge transfer between cells. (c) Example charge transfer from cell B^1 to B^3 using the proposed balancing architecture. Parts of the circuit that are not used are grayed out for better visibility of the balancing current flow direction.

switches M_h^3 and M_g^3, respectively. Rest of the switches in the balancing unit associated with cell B^3 are kept *OFF*. Connection of the charge transfer bus between balancing unit 3 and 1 is enabled by actuating MOSFETs M_{BB+}^2 and M_{BB-}^2, respectively present in the balancing unit associated with cell B^2. All other switches in the balancing unit of cell B^2 are *OFF* to isolate the cell from the charge transfer bus. Once the static switching configuration is set, the charge transfer process is initiated by actuating the corresponding switches with high frequency signals σ^1 to σ^2 shown in Fig. 6.3b.

During the charging phase (Φ_1) of the inductor, MOSFETs M_a^1 and M_b^1 are actuated using σ^1 as shown in Fig. 6.3b. This connects the inductor L^1 to cell B^1 and the current through the inductor starts to rise linearly as shown in Fig. 6.3b. Once M_a^1 and M_b^1 are turned *OFF* at time $t = T_{\mathrm{ON}}$, the inductor current freewheels over the destination cell through the internal body-diode of the MOSFET M_b^1 for the phase Φ_2' as shown in Fig. 6.3b. Once establishing the freewheeling phase, the synchronous charge transfer is triggered by actuating MOSFETs M_c^1, M_d^1, M_{BB+}^1 and M_{BB-}^1 with the control signal σ^2 shown in Fig. 6.3b. Now the inductor starts to discharge its stored energy into the destination cell B^3 for a time period T_{OFF} in phase Φ_2 as shown in Fig. 6.3b. Finally, a single charge transfer cycle is completed by transferring the remaining amount of charge in the inductor through the body diode of M_b^1, in order to prevent reverse charging of the inductor from the destination cell B^3.

6.2.3 Control Scheme

In this section, a detailed control scheme for actuating the MOSFETs in the balancing unit depending on whether the associated battery cell is a source or destination cell of the charge transfer pair is discussed. Each cell $n \in N$ in a battery pack consisting of $N = \{1, 2, ...M\}$ series-connected cell is associated with a balancing unit that has an energy storage element inductor L^n and a set of MOSFETs $M^n = \{M_h^n, M_g^n, M_a^n, M_b^n, M_c^n, M_d^n, M_{BB+}^n, M_{BB-}^n\}$. Each charge transfer scenario defined by $\mathcal{T}$ consisting of pairs $p = (S, D) \in N$ formed by source cells $S \subseteq N$ and destination cell $D \subseteq N$ are disjoint. Moreover, the domains formed by these transfer pairs

$$d(p) = \{\min(n|n \in \mathrm{S} \cup \mathrm{D}), .., \max(n|n \in \mathrm{S} \cup \mathrm{D})\}$$

are also disjoint in order to avoid short circuits between cells. Depending upon the state of the associated battery cell, the actuation signal of each MOSFET in the balancing unit could be any of the following

$$s(\mathcal{T}, M) \in \{0, 1, \sigma^1, \sigma^2\} \tag{6.2}$$

where 0 represents the MOSFET is *OFF*, 1 represents the switch is *ON* and control signals σ^1 and σ^2 are as shown in Fig. 6.3b. Detailed switching rules for each of the MOSFET in the balancing unit depending upon the state of the associated battery cell is shown in Table 6.2. State 1 represents the switching configuration of MOSFETs in the balancing unit associated with the source cell of the charge transfer pair that is above the destination cell. State 2 provides the switching configuration when the associated battery cell is below the destination cell of the charge transfer pair. States 3 and 4 are the switching configuration for balancing units associated with the destination cell of the charge transfer pair that are either above or below the source cell, respectively. State 5 provides switching configuration for cells that are in between the source and destination cell of the charge transfer pair and State 6 is the switching configuration for cells that are not involved in the charge transfer process.

6.2.4 Possible Charge Transfer Scenarios

Fig. 6.4 shows the different charge transfer patterns that are possible with the proposed parallel-attached active cell balancing architecture. Maximum concurrent charge transfers are possible

	States	Description	Switching Configuration							
			M_h^n	M_g^n	M_a^n	M_b^n	M_c^n	M_d^n	M_{BB+}^n	M_{BB-}^n
1.	$\exists p \in \mathcal{T} : n \in \mathrm{S} \wedge \tilde{n} \in \mathrm{D} \wedge n < \tilde{n}$	Source cell above the destination cell	0	0	σ^1	σ^1	σ^2	σ^2	σ^2	σ^2
2.	$\exists p \in \mathcal{T} : n \in \mathrm{S} \wedge \tilde{n} \in \mathrm{D} \wedge n > \tilde{n}$	Source cell below the destination cell	1	1	0	0	0	0	0	0
3.	$\exists p \in \mathcal{T} : n \in \mathrm{D} \wedge \tilde{n} \in \mathrm{S} \wedge n < \tilde{n}$	Destination cell above the source cell	0	0	σ^2	σ^2	σ^1	σ^1	σ^1	σ^1
4.	$\exists p \in \mathcal{T} : n \in \mathrm{D} \wedge \tilde{n} \in \mathrm{S} \wedge n > \tilde{n}$	Destination cell below the source cell	1	1	0	0	0	0	0	0
5.	$\exists p \in \mathcal{T} : n \in d(p) \wedge n \notin \mathrm{S} \wedge \tilde{n} \notin \mathrm{D}$	Forwarding	0	0	0	0	0	0	1	1
6.	$\forall p \in \mathcal{T} : n \notin d(p)$	No charge Transfer	0	0	0	0	0	0	0	0

Table 6.2: Switching configuration of MOSFETs in the balancing unit for all possible states of the associated cell. 0, 1 means that the MOSFET is statically *ON* or *OFF*, respectively and σ^1 and σ^2 mean they are controlled by high frequency control signals shown in Fig. 6.3b.

with the proposed architecture as shown in Fig. 6.4a, where simultaneous charge transfers between cells $B^1 \rightarrow B^2$ and $B^3 \rightarrow B^4$ are shown. Adjacent cells of the charge transfer pair are not required to be in blocking mode with the proposed architecture and therefore $100\,\%$ concurrency is achieved for all transfers between neighboring cells. Furthermore, as shown in Fig. 6.4b, the proposed architecture is capable of transferring charge from a single cell to a group of cells and from many cells to a single cell as shown in Fig. 6.4c. Finally, charge transfers from multiple source to multiple destination cells is also possible with the proposed architecture as shown in Fig. 6.4d.

6.2.5 Advantages and Disadvantages

Compared to the architecture in Section 6.1, the parallel-attached balancing architecture does not require huge power MOSFET switches in the series power line of the battery pack. As a result, balancing can also be performed while the battery pack is in operation. Since the balancing unit is attached in parallel to each cell and it only carries the balancing current, which is in the range of few Amperes. Therefore, the MOSFET switches in each balancing unit can be relatively small compared to the high power MOSFETs used in the power line in case of the cell-isolated balancing architecture. Moreover, as shown in Fig. 6.4a, the proposed architecture does not require the adjacent cells of the charge transfer pair to be in blocking mode. As a result, a maximum percentage of concurrency is achieved with this architecture in comparison to Section 6.1. In addition, the number of MOSFETs required to perform multiple charge transfer patterns for the parallel-attached balancing architecture is 8, which is less than the 11 switches required for the balancing architecture in Section 6.1. However, the only drawback of the proposed architecture is that it requires more number of switches (6 MOSFETs) to be operated with high frequency control signals compared to the balancing architecture in Section 6.1. This results in an increased energy consumption and control complexity, since for each MOSFET that is operated with a high frequency control signal, special type of galvanically-isolated gate drive circuitry with individual power supply is required, which results in an increased installation space, cost and energy consumption from the battery cell.

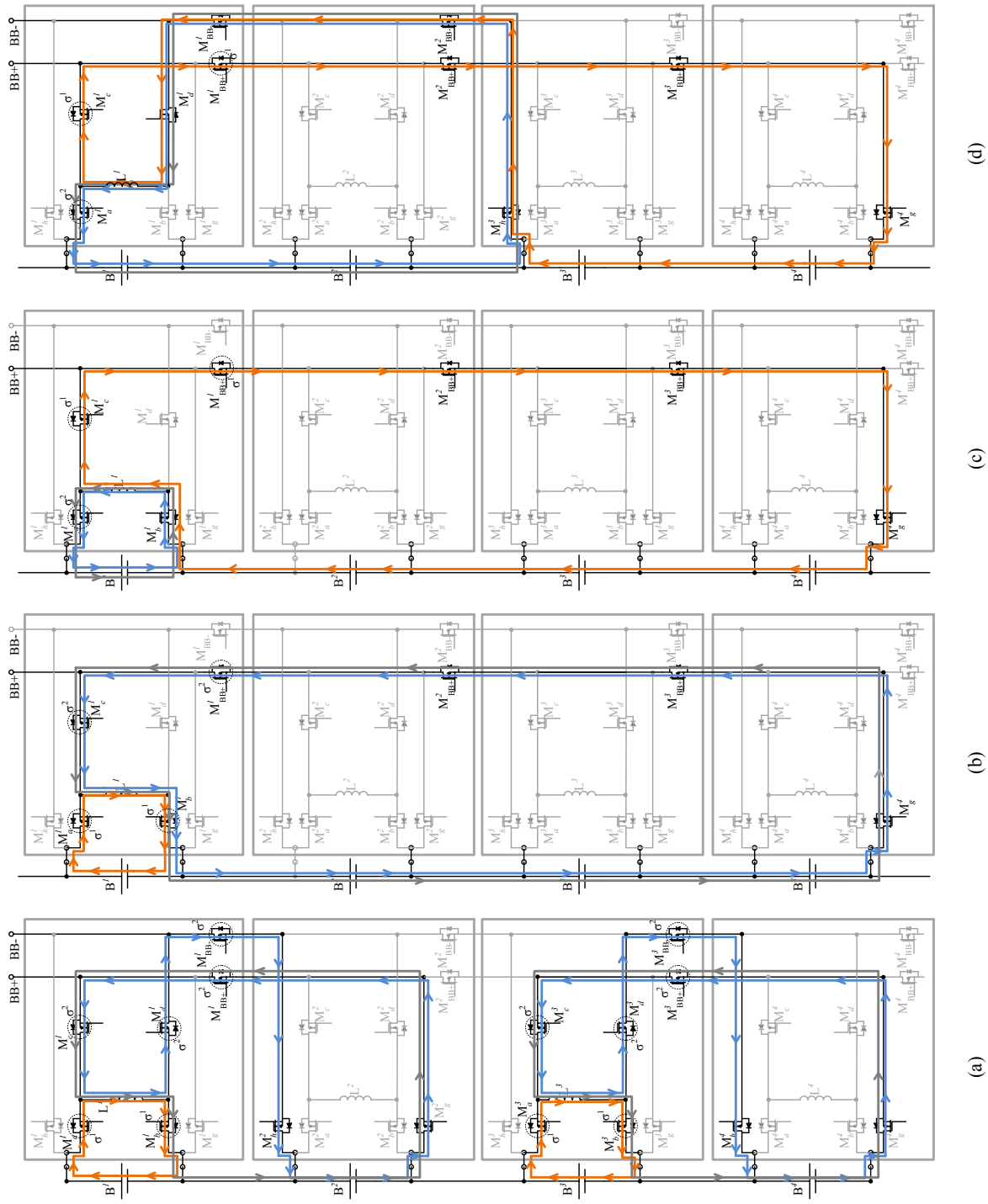


Figure 6.4: Possible charge transfer scenarios of parallel-attached inductor-based active cell balancing architecture. (a) Concurrent charge transfers, $B^1 \rightarrow B^2$ and $B^3 \rightarrow B^4$, at the same time. (b) One cell to many cells, $B^1 \rightarrow B^2, B^3, B^4$. (c) Many cells to one, $B^2, B^3, B^4 \rightarrow B^1$. (d) Many cells to many cells, $B^3, B^4 \rightarrow B^1, B^2$.

6.3 Transformer-based Active Cell Balancing Architecture

In this section, an active cell balancing architecture utilizing transformer as an energy storage element is proposed and analyzed in detail.

6.3.1 Challenges in Inductor-based Active Cell balancing Architecture

Inductors are highly energy-efficient energy storage element compared to capacitors in terms of performing charge transfer between battery cells. Moreover, when compared with transformers they occupy reduced installation space for the same value of balancing current. However, using an inductor for active cell balancing purpose imposes certain design challenges in the electrical architecture perspective of the balancing unit. As explained in Section 2.1.1, the physical property of an inductor does not allow the current to be interrupted or changed instantaneously. By opening the current flow path of an inductor even for a short duration will produce an arc through the surrounding air and this will eventually damage the remaining power MOSFETs in the circuit or result in a thermal runaway situation of the Li-Ion cell when the temperature induced by the arc is high. As a result, any active cell balancing circuit using inductors as energy storage element, always require a closed connection path to be established for the inductor current to flow.

Designing an active cell balancing architecture that performs charge transfers between non-adjacent cells of the battery pack while at the same time maintain a closed-connection path for the inductor current is not a trivial task. Improper connection of the source cell to the inductor or the inductor to the destination cell will result in a short circuit condition. For this purpose, the isolating non-neighbor architecture proposed in Section 6.1, disconnects the series connection of the battery pack to avoid potential short circuits. However, by isolating the power line of the battery pack, balancing during normal operation is not possible. In order to enable non-neighbor balancing without breaking the series connection of the battery pack, additional MOSFETs, more interconnection points and an increased number of high frequency control signals are used by the parallel-attached balancing architecture presented in Section 6.2. However, these options will increase the power consumption from the battery cell since the controllers that generate these high frequency control signals are powered directly from the battery cell. In order to overcome the closed connection path challenges involved in inductor-based active cell balancing architectures, this thesis proposes a transformer-based architecture and utilizes the inherent isolation of the transformer to perform non-neighbor balancing with reduced hardware and control complexity.

6.3.2 Homogeneous Balancing Unit

Fig. 6.5a shows the homogeneous unit of the proposed transformer-based active cell balancing architecture that is associated with each cell of the battery pack. The balancing unit is added as an external connection to the battery cell and does not interfere with the series power line connection of the battery pack. Therefore, the balancing process can take place while the battery pack is in operation (both charging and discharging). Each balancing unit consists of one energy storage transformer (T^1) and eight low power MOSFET switches. The primary

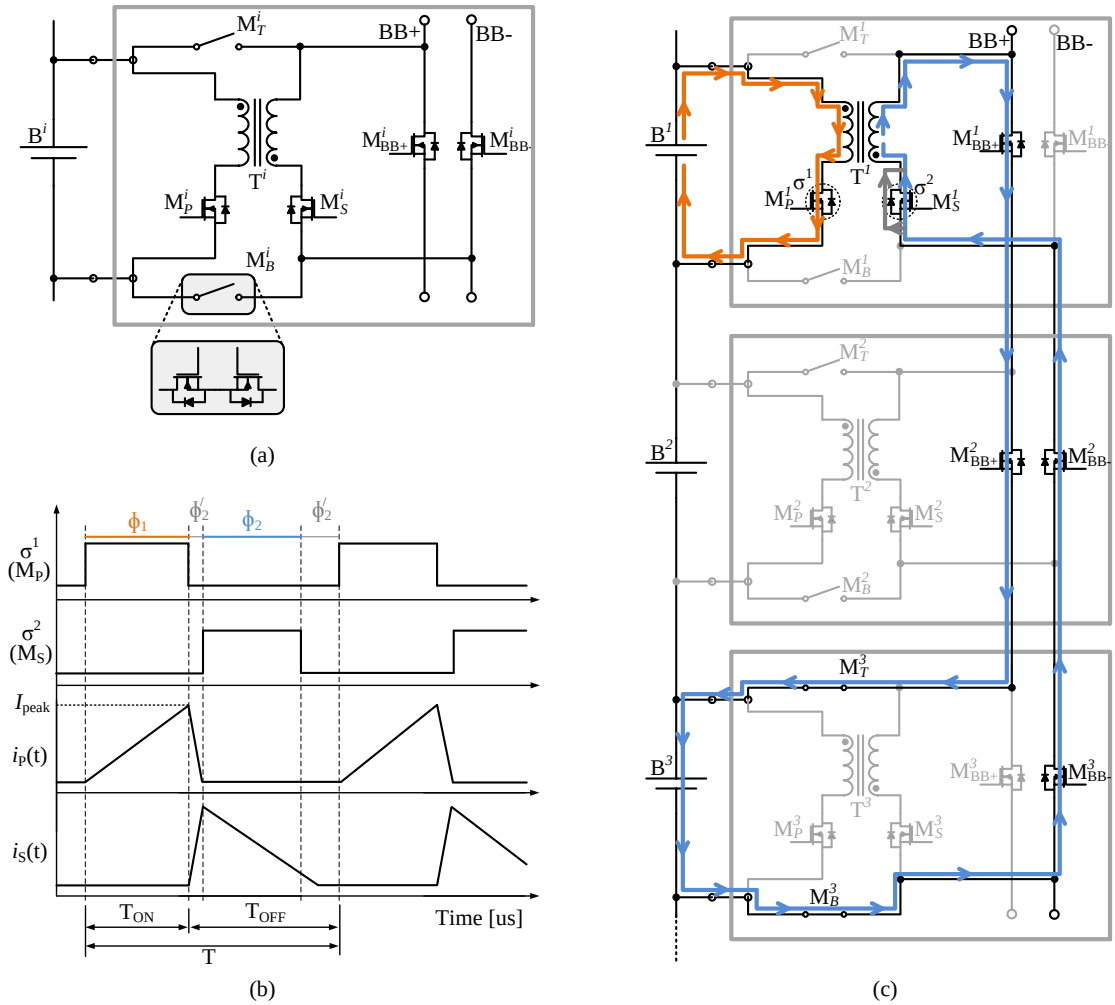


Figure 6.5: Transformer-based active cell balancing architecture. (a)Homogeneous unit of the proposed transformer-based balancing architecture that is associated with each cell of a series-connected battery pack. Each unit consists of one flyback transformer T^1, two switching MOSFETs (M^1_P & M^1_S), top and bottom cell isolation switches (M^1_T & M^1_B), two charge transfer bus isolation MOSFETs ($\mathrm{M}^1_{\mathrm{BB}+}$ & $\mathrm{M}^1_{\mathrm{BB}-}$). BB^+ and BB^- represent the charge transfer bus that connects to the neighboring balancing units.

winding of the transformer is connected to the respective battery cell and the secondary winding is connected to a charge transfer bus (BB^+ and BB^-). Switches M^1_T and M^1_B consist of two low power MOSFET switches that are connected in such a way that their internal body-diodes are blocking each other as shown in Fig. 6.5a and thereby provide complete isolation between the battery cell and the charge transfer bus. MOSFETs $\mathrm{M}^1_{\mathrm{BB}+}$ and $\mathrm{M}^1_{\mathrm{BB}-}$ are used to isolate the charge transfer bus between the modules, thereby allowing to perform concurrent charge transfers. Balancing between cells is enabled by actuating the primary and secondary MOSFET switches (M^1_P and M^1_S) with non-overlapping high frequency control signals shown in Fig. 6.5b,

respectively. Therefore, only two high frequency control signals and switches are required for each module. The rest of the switches in the module are either statically turned *ON* or *OFF* according to the switching rules presented in Section 6.3.4.

Safety of the balancing unit is ensured in the following ways. The energy storage transformer provides an inherent isolation of the battery cell from the charge transfer bus. The only direct connection between the battery cell and the charge transfer bus is via switches $\mathrm{M_T}$ and $\mathrm{M_B}$. Accurate control of these switches is possible, since they are actuated with static signals (*ON* or *OFF*) and do not require any high frequency control. Moreover, to further improve the safety, all switches in the balancing unit are realized as N-type power MOSFETs, that are normally-open and isolate the balancing circuit from the battery pack in case of any failure.

The individual balancing unit shown in Fig. 6.5a is connected with other units to form a homogeneous system-level balancing architecture as shown in Fig. 6.5c. The balancing units are connected to each other through the charge transfer bus in order to exchange charge between cells. Current flow on the charge transfer bus ($\mathrm{BB^+}$, $\mathrm{BB^-}$) is bi-directional, meaning charge could be transferred in both directions, i.e., from a top cell to a bottom cell or vice versa. The charge transfer bus carries balancing currents which are in the range of few Amperes compared to the high magnitude load currents that flow in the main power line of the battery pack. Therefore, thick cables are not required for interconnecting the charge transfer bus of the individual units. Concurrent balancing between battery cells is achieved by isolating the charge transfer bus between the modules, with the help of switches $\mathrm{M_{BB+}}$ and $\mathrm{M_{BB-}}$ associated with each balancing unit.

6.3.3 Working Principle

The proposed balancing architecture works on the same principle of flyback-type DC-DC converters (for a general overview of a flyback DC-DC converter please refer to Chapter 7 of [100]). The transformer used in a flyback DC-DC converter is commonly referred to as an inductor-transformer. Unlike an ideal transformer, the current in an inductor-transformer does not flow simultaneously in both windings, due to the reversed polarity connection of the primary and secondary windings. This is shown in Fig. 6.5a, where the dots (which signifies the polarity of the windings) in the primary and secondary windings of the transformer are opposite to each other. For the following explanation on the working principle of our proposed balancing architecture, please refer to Fig. 6.5c, where cell B^1 transfers its excess charge directly to cell B^3, without involving cell B^2. The control signals required for performing the charge transfer and the corresponding balancing currents on both primary and secondary windings of the transformer are shown in Fig. 6.5b.

For this example, cell B^1 and B^2 are isolated from the charge transfer bus by opening MOSFETs M_T^1, M_B^1 and M_T^2, M_B^2, respectively. By contrast, cell B^3 is connected to the charge transfer bus by actuating M_T^3 and M_B^3, respectively. The charge transfer bus is connected between cells B^1 and B^3 by actuating switches $M_{\mathrm{BB+}}^1$, $M_{\mathrm{BB+}}^2$, $M_{\mathrm{BB-}}^2$ and $M_{\mathrm{BB-}}^3$, respectively. Rest of the switches in the respective balancing modules are turned *OFF* before initiating the charge transfer process. Once the static configuration of switches are set, the charging phase (Φ^1) of the balancing process is initiated by actuating M_P^1 with the control signal σ^1 shown in Fig. 6.5b.

	States	Description	Switching Configuration					
			M_T^n	M_B^n	M_P^n	M_S^n	M_{BB+}^n	M_{BB-}^n
1.	$\exists p \in \mathcal{T} : n \in \mathrm{S} \wedge \tilde{n} \in \mathrm{D} \wedge n < \tilde{n}$	Source cell above the destination cell	0	0	σ^1	σ^2	1	0
2.	$\exists p \in \mathcal{T} : n \in \mathrm{S} \wedge \tilde{n} \in \mathrm{D} \wedge n > \tilde{n}$	Source cell below the destination cell	0	0	σ^1	σ^2	0	1
3.	$\exists p \in \mathcal{T} : n \in \mathrm{D} \wedge \tilde{n} \in \mathrm{S} \wedge n < \tilde{n}$	Destination cell above the source cell	1	1	0	0	1	0
4.	$\exists p \in \mathcal{T} : n \in \mathrm{D} \wedge \tilde{n} \in \mathrm{S} \wedge n > \tilde{n}$	Destination cell below the source cell	1	1	0	0	0	1
5.	$\exists p \in \mathcal{T} : n \in d(p) \wedge n \notin \mathrm{S} \wedge \tilde{n} \notin \mathrm{D}$	Forwarding	0	0	0	0	1	1
6.	$\forall p \in \mathcal{T} : n \notin d(p)$	No charge Transfer	0	0	0	0	0	0

Table 6.3: Switching configuration of MOSFETs in the balancing unit for all possible states of the attached cell. 0, 1 means that the MOSFET is statically *ON* or *OFF* and σ^1, σ^2 means they are controlled by non-overlapping high frequency control signals shown in Fig. 6.5b, respectively.

Excess charge from cell B^1 is stored in the primary winding of the transformer T^1 as shown in Fig. 6.5b, where the primary winding current increases linearly. After a predefined peak current value (I_{peak}) is reached for a time period of T_{ON}, M_P^1 is turned *OFF*.

Due to the property of the transformer, where the current cannot be interrupted instantaneously, the polarity of the voltages across the primary and secondary winding reverses. This polarity reversal causes the internal body-diode of the secondary winding MOSFET M_S^1 to be forward-biased. As a result, the primary-secondary energy transfer takes place and the charge stored in the transformer is discharged to cell B^3 through the secondary winding. This phase is marked as short freewheeling phase Φ_2' in Fig. 6.5b. To minimize the loss involved in balancing over the diode, the discharging phase Φ_2 is initiated by actuating the secondary winding MOSFET M_S^1 by control signal σ^2 as shown in Fig. 6.5b. Now the transformer discharges the stored energy into cell B^3 through the low-resistance MOSFET channel as shown in Fig. 6.5c. Finally, the last remaining amount of charge stored in the transformer is discharged over the body-diode of M_S^1 in order to prevent the transformer being charged from cell B^3. This completes a single charge transfer cycle.

6.3.4 Control Scheme

In this section, control scheme for operating all the MOSFET switches in each module is derived for enabling charge transfer between cells using the proposed active cell balancing architecture. The switching rules for the MOSFETs in the balancing unit depend upon whether the associated battery cell is a source or destination or a cell in between the source and destination cell of a charge transfer pair. The derived switching rules are verified for correctness using a design automation framework developed in [15] in order to avoid potential short circuits between cells.

A battery pack consists of a set of $\mathcal{N} = \{1, 2, ..., N\}$ series-connected cells and each cell $n \in \mathcal{N}$ is associated with an individual balancing unit that has a transformer T^n and a set of MOSFETs $M^n = \{M_T^n, M_B^n, M_P^n, M_S^n, M_{\mathrm{BB+}}^n, M_{\mathrm{BB+}}^n\}$. A transfer scenario is defined by $\mathcal{T}$ that consists of multiple charge transfer pairs $p = (\mathrm{S}, \mathrm{D}) \in N$ formed by source cells $\mathrm{S} \subseteq N$ and destination cells $\mathrm{D} \subseteq N$ that are disjoint. Moreover, each transfer pair forms a domain by

$$d(p) = \{\min(n|n \in \mathrm{S} \cup \mathrm{D}), .., \max(n|n \in \mathrm{S} \cup \mathrm{D})\}$$

and the domains are disjoint in order to avoid short circuits between cells. Depending upon the transfer scenario $\mathcal{T}$, the switching configuration of each MOSFET is:

$$s(\mathcal{T}, M) \in \{0, 1, \sigma^1, \sigma^2\} \tag{6.3}$$

where 0 represents that the switch is *OFF*, 1 denotes that it is *ON*, σ^1 and σ^2 are non-overlapping control signals shown in Fig. 6.5b.

Table 6.3 presents the switching configuration of MOSFETs in the balancing unit depending upon the state of the associated cell. States 1, 2 represent the switch configuration for MOSFETs in the balancing unit that is associated with the source cell of a charge transfer pair. Depending upon the position in the battery string with respect to the destination cell, an appropriate configuration is selected (state 1 if the source cell is above the destination cell and state 2 if it is below in the series string). Similarly, the switching configuration for MOSFETs in the balancing unit of the destination cell is provided in state 3 (when the destination cell is above the source cell in the series string) or 4 (when the destination cell is below the source cell in the battery pack). State 5 is the forwarding mode in which the battery cell is in between the source and destination cells of a charge transfer pair. Finally, state 6 provides configuration of the switches in a balancing unit which is associated with a cell that is not involved in the balancing process.

6.3.5 Possible Charge Transfer Scenarios

Similar to the previously proposed balancing architectures, the transformer-based active cell balancing architecture is also capable of performing multiple charge transfer scenarios as will be explained in this section. Fig. 6.6a shows the maximum concurrent charge transfer capabilities of the proposed architecture. Charge from cell B^1 is transferred to cell B^2 and at the same time B^3 also transfers its excess charge to B^4. The adjacent cells of the charge transfer pair are not required to be in blocking mode as in the case of the cell-isolating balancing architecture proposed in Section 6.1. Fig. 6.6b and 6.6c shows that the proposed transformer-based active cell balancing architecture is capable of transferring charge from a single cell to a group of cells and vice versa, respectively. Finally, it is also possible to balance between one group of cells to other group of cells using the proposed active cell balancing architecture as shown in Fig. 6.6d.

6.3.6 Advantages and Disadvantages

In comparison to the cell-isolating inductor-based active cell balancing architecture presented in Section 6.1, the transformer-based balancing architecture has a reduced number of MOSFET switches and does not required the high power MOSFETs in the series powerline of the battery pack. Moreover, the transformer-based approach requires only two non-overlapping high frequency control signals and MOSFETs and thereby has a reduced energy consumption in comparison to the parallel-attached inductor-based active cell balancing architecture proposed in Section 6.2. This is achieved by utilizing the inherent isolation provided by the transformer and as a result the requirement of closed connection path for the current in the inductor-based balancing architectures is addressed by having two separate windings in the transformer. Even though using transformer simplifies the electrical architecture and control scheme of the charge

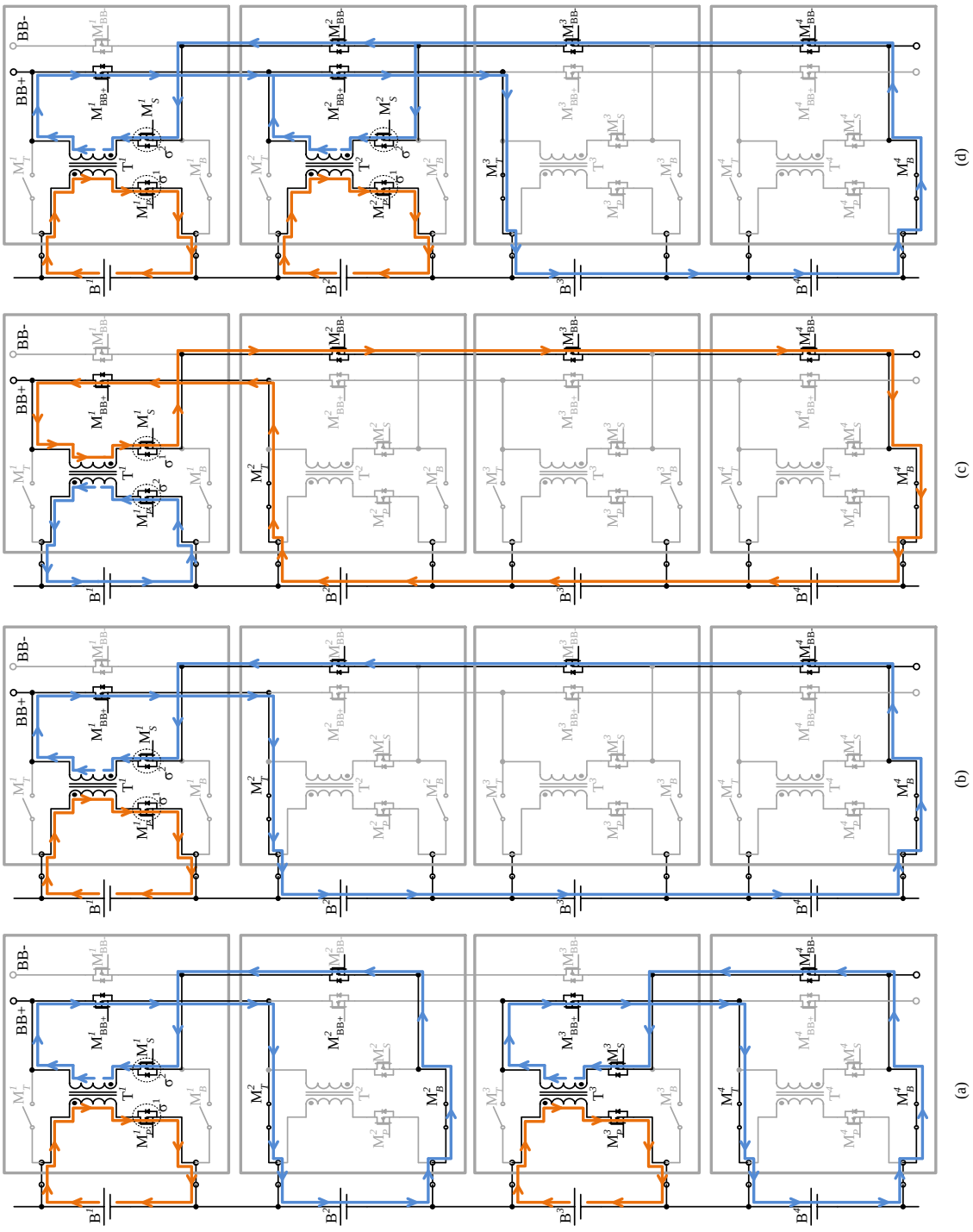


Figure 6.6: Possible charge transfer scenarios of transformer-based active cell balancing architecture. (a) Concurrent charge transfers, $B^1 \rightarrow B^2$ and $B^3 \rightarrow B^4$, at the same time. (b) One cell to many cells, $B^1 \rightarrow B^2, B^3, B^4$. (c) Many cells to one, $B^2, B^3, B^4 \rightarrow B^1$. (d) Many cells to many cells, $B^1, B^2 \rightarrow B^3, B^4$.

balancing process, there exist certain challenges that requires to be addressed for achieving improved energy-efficiency. The installation space required for the transformer in comparison to the inductor for the same value of inductance is higher, since two windings are required in case of the transformer. Moreover, in comparison to the inductor-based approaches transformers exhibit an additional energy dissipation due to the leakage inductance discussed in Section 5.2.3.3. To minimize this effect, proper coupling of primary and secondary winding with adequate sealing is required for avoiding the flux leakage. Therefore, special type of transformers optimized for reduced leakage inductance are required, which will increase the cost of the system.

6.4 Summary

Depending upon the design requirements derived in Chapter 4, three different modular active cell balancing architectures were proposed in this chapter. Each of the proposed architecture can be modularized into homogeneous units that can be attached with each cell and controlled by the respective cell-level controller. Working principle and the control scheme required for actuating the switches in the balancing module for performing charge transfer are derived. Different charge transfer scenarios that are possible with the proposed active cell balancing architectures are explained in detail. In the following chapter, hardware implementation of each of the proposed active cell balancing architecture is developed using commercial off-the-shelf components and integrated into the distributed BMS development platform for functional verification and model validation.

7 Implementation

In this chapter, implementation details of the individual modules in the cell-level controller of the distributed BMS discussed in Section 3.3 is presented. The individual modules are implemented using commercial off-the-shelf components in a custom-designed PCB. Furthermore, hardware implementation of the active cell balancing architectures proposed in Chapter 6 is performed. A modular, reconfigurable development platform for emulating the partially and fully distributed BMS topologies is developed by connecting five Li-Ion in series, each associated with their respective cell-level controllers. This development platform is used as a test bed to perform functional verification and model validation of active cell balancing architectures proposed in this thesis.

7.1 Implementation of Cell-level Controller

In this section, a detailed discussion regarding the implementation of each module in the cell-level controller is discussed. Based on these implementation details a cell-level controller is developed as a custom-designed PCB.

7.1.1 Sensing Module

Parameters such as voltage, balancing current and temperature of the cell are measured using the sensing module.

Voltage measurement. Measuring the cell voltage using an ADC provides high accuracy compared to other methods such as resistor-divider, isolation relays as discussed in Section 3.3.1.1. A single-supply, difference amplifier as shown in Fig. 7.1a calculates the difference between the positive and negative terminals of the cell. The difference amplifier also serves as a buffer for the

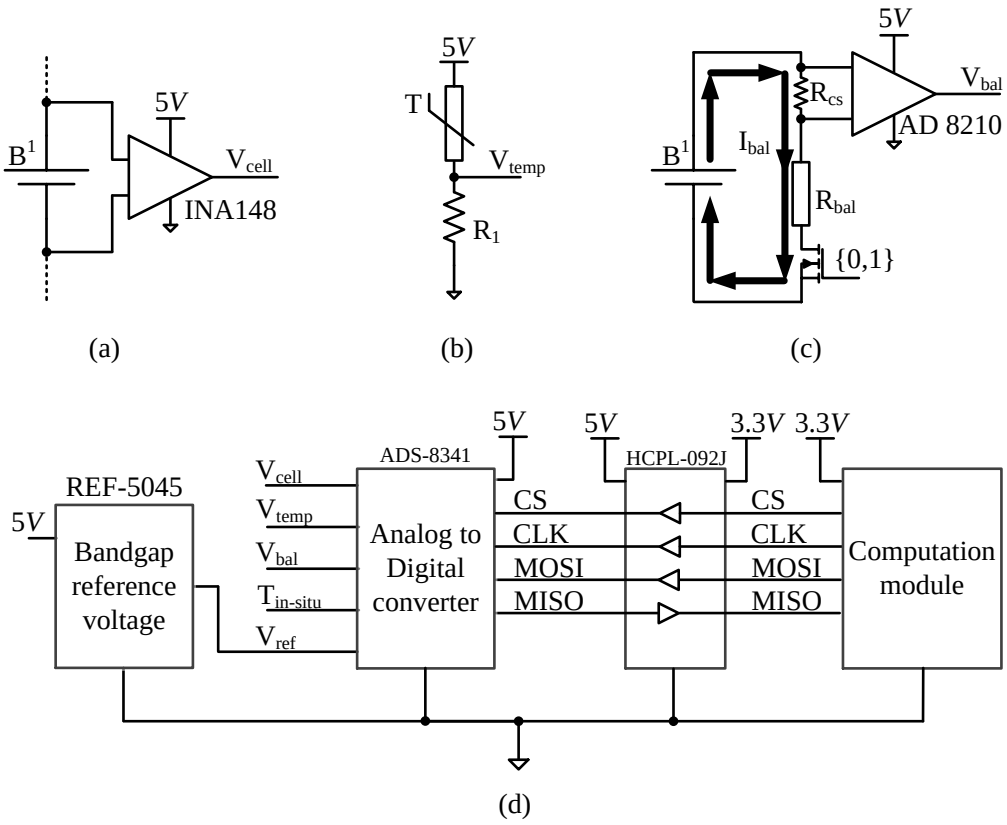


Figure 7.1: Sensing module implementation of the individual cell-level controller. (a) Cell voltage is measured using a single supply difference amplifier and (b) temperature is monitored using thermistor sensor with a resistor-divider network. (c) Balancing currents are measured using a shunt resistor. (d) All analog measurement values are digitized using an ADC and the converted results are provided to the computation module through the digital isolator.

low impedance ADC input channels and prevents them from damage due to high voltage spikes. Output of the difference amplifier is directly provided to an ADC as shown in Fig. 7.1d.

Temperature measurement. The surface temperature of the cell is monitored using a thermistor sensor due to its high accuracy and ease of implementation. The thermistor is connected to a high precision resistor R_1 in series as shown in Fig. 7.1b, whose value is equal to the nominal resistance of the thermistor, at ambient temperature conditions. The thermistor sensor and the series-resistance R_1 forms a resistor-divider network. Temperature changes in the cell causes the resistance of thermistor sensor to vary and this changes the voltage V_{temp}. This is measured using an ADC which directly relates to the temperature of the cell. The inner temperature of the cell requires in-situ mounting of sensors during the production phase and therefore is not shown here. However, depending upon the in-situ temperature sensor, appropriate signal conditioning circuitry to measure the inner temperature of the cell is provided as shown in Fig. 7.1d.

Current measurement. The balancing currents are of lower orders of magnitude compared to the pack current and therefore resistive method is employed as shown in Fig. 7.1c. The voltage developed across this small series-resistance R_{cs} is amplified by a CSA and the analog output voltage, which is a direct indication of the balancing current is measured using the signal processing circuitry shown in Fig. 7.1d. On the other hand, dual range hall effect sensors are used for pack current sensing, where one sensor measures currents at a higher range and the other one provides accurate measurements in the low current range. The balancing current sensors are implemented in all individual cell-level controllers, whereas the pack-level current sensor is implemented as a separate entity with communication capabilities at the negative terminal of the battery pack. The power for operation of the pack-level current sensor is obtained from the adjacent cell module.

Signal conditioning. All analog measurement values are digitized using a high-accuracy, multi-channel ADC as shown in Fig. 7.1d. The reference voltage (V_{ref}) required for the conversion process of the ADC is obtained from a temperature-compensated, band-gap reference voltage generator as shown in Fig. 7.1d. Moreover, the converted digital signals from the ADC are read by the computation module for further processing and computation of cell states such as SoC, SoH, etc. Since the ADC and the computational module are operating at different voltage levels, a digital isolator is used to compensate the varying voltage levels of the signals as shown in Fig. 7.1d. One side of the digital isolator is powered from the same supply as the ADC and the other side with the voltage corresponding to the computational module.

7.1.2 Computation Module

Choosing a computation core for the cell-level controller is the most critical and difficult task. As mentioned in Section 3.3.2, the computational module depends upon the size and accuracy requirements of the application. In order to implement the cell-level and pack-level functions of the BMS listed in Table 3.1 and to meet the safety regulations pertaining to the specific application, a 32-bit, ARM Cortex-M4 MCU architecture from ST Microelectronics family STM32F407 [105] is chosen for implementation. Running at $168\,\mathrm{MHz}$ clock frequency the chosen MCU architecture provides higher computation power for evaluating the cell and pack-level functions of the distributed BMS. Since being a development platform, this high computation power offers flexibility in designing several complex software algorithms for distributed BMSs and verify their functionality. With up to 17 timers available in the core, complex high frequency control signals required for the control of active cell balancing architectures can be efficiently generated. In addition, having 15 possible communication interfaces provides flexibility to independently test and verify different communication topologies for distributed BMSs. Moreover, complex matrix computations for SoC and SoH estimation, which involves matrix multiplications and inversions can be efficiently implemented.

A real-time operating system µC/OS-III [106] runs on the computation MCU, which facilitates the implementation of the cell-level and pack-level functions of the distributed BMSs listed in Table 3.1. The objective of using a real-time operating system is to split each function into different *tasks*, which are then scheduled to run on the MCU depending upon their priority-levels.

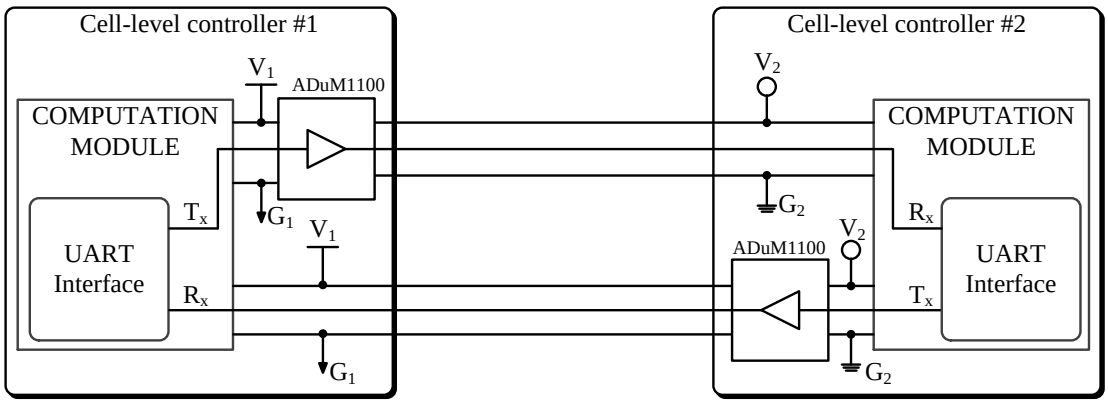


Figure 7.2: Daisy chain communication module of the cell-level controller implemented through UART interface and digital isolators.

The µC/OS-III real-time operating system supports *multi-tasking*, a process of scheduling and switching the MCU between several tasks. This facilitates an application programmer to implement a complex function into multiple modular tasks, that are then periodically executed by the operating system. This not only simplifies the programming implementation but also enables efficient usage of the MCU resources in the computational module. Moreover, the ability to assign priority levels to tasks ensures that safety-critical BMS functions are executed with high priority in a timely manner meeting their deadlines. This would not be possible with other software architectures such as super-loop or hyper-loop. In addition, a real-time operating system also facilitates system-level debugging with efficient usage of available computational resources.

7.1.3 Communication Module

Communication between the cell-level controllers of the distributed BMS is necessary for performing the pack-level functions listed in Table 3.1. As discussed in Section 1.4.2.3, powerline communication interface suffers because of noise generated due to fast switching currents and wireless communication between cell-level controllers are not reliable for safety-critical applications. Therefore, both daisy chain and an isolated bus communication topology are implemented in the development platform for comparing the efficiency.

Daisy chain communication. Communication between neighboring cell-level controllers is established by a daisy chain communication topology implemented using the Universal Asynchronous Receiver Transmitter (UART) serial interface. UART is a two-wire serial data communication topology for which the necessary commands and protocols are provided by the MCU in the computation module. Since each cell-level controllers are powered from the respective battery cells a isolated communication interface is required between the controllers in order to avoid potential short circuits between cells. A digital isolator from Analog Devices family, ADuM1100 is used to provide the required isolation as shown in Fig. 7.2. All $\mathrm{T_x}$ communication line of the serial interface are isolated using the digital isolator, where one side is powered from

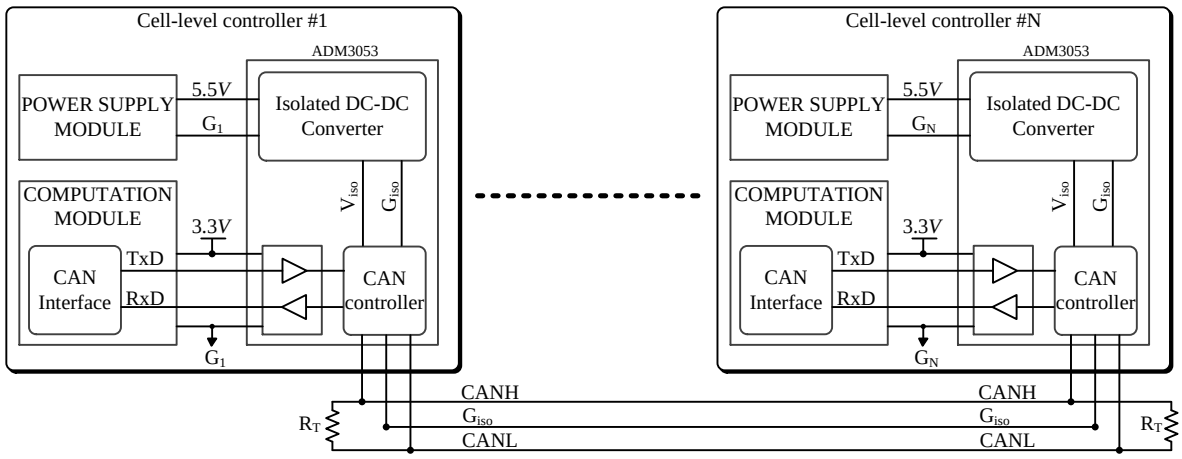


Figure 7.3: Bus communication between cell-level controllers of a distributed BMS is implemented through an isolated CAN.

the transmitting controller and the other end is connected to the power supply of the receiving controller as shown in Fig. 7.2.

Bus communication. In addition to the neighbor-only daisy chain communication interface, a bus communication topology is also provided in the development platform. The bus communication is implemented using an isolated CAN bus as shown in Fig. 7.3. The MCU in the computational module provides the necessary CAN communication control and executes the time-triggered scheduling protocol. Isolated CAN transceivers from Analog Devices, ADM3053, is used to implement the physical layer of the CAN bus. The transceiver has an in-built, DC-DC converter which provides an isolated supply voltage V_{iso} and G_{iso} for the bus. The isolated bus topology is required to avoid short circuit conditions because of the varying DC potentials along the battery pack. Apart from the power supply isolation, the transceivers also isolate the CAN output signals TxD and RxD from the MCU using an in-built digital isolator. Finally, the communication bus is formed by connecting the CANH, CANL and the ground reference G_{iso} of the CAN transceivers in all cell-level controllers and terminating the communication bus on both sides with resistor a R_T as shown in Fig. 7.3, in order to avoid reflections on the bus.

7.1.4 Cell Balancing Module

Three different modular active cell balancing architectures were proposed in Chapter 6 of this thesis. These modular active cell balancing architectures are implemented as a separate entity that can be attached with the battery cell and controlled by the respective cell-level controllers. Implementation details of the individual balancing architectures are explained in detail in Section 7.2. Nevertheless, to investigate system architectures without active cell balancing and to make the cell-level controller a fully functional unit of a distributed BMS, an on board passive balancing technique as shown in Fig. 7.4 is employed. A MOSFET switch M^1 controlled by the computational MCU is connected in series with a high power resistor R_{bal} which is used

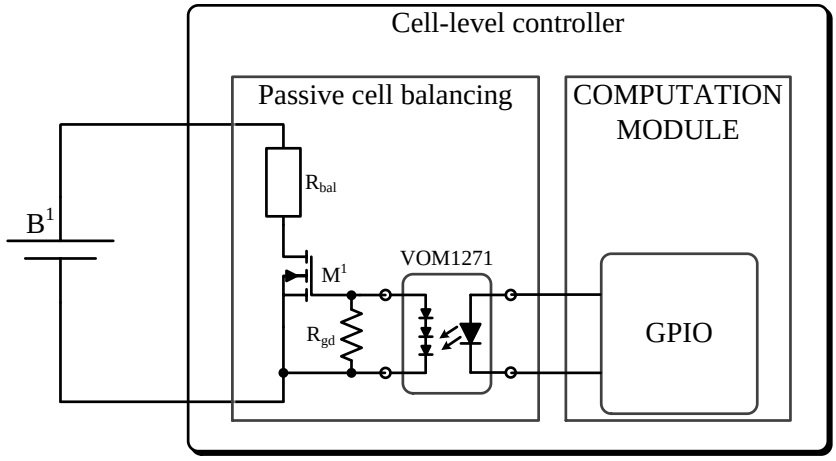


Figure 7.4: Switched-resistor passive balancing technique is employed using the balancing resistor R_{bal} and the power MOSFET M^1. A photovoltaic gate drive unit is used to actuate the high power MOSFET from low voltage MCU in the computation module.

to discharge the excess charge of cells with higher SoC. Since a higher gate drive actuation voltage compared to the logic level output of the MCU is required to turn-*ON* the MOSFET, a photovoltaic MOSFET gate drive unit from Vishay VOM1271 is implemented as shown in Fig. 7.4. Moreover, the photovoltaic driver provides optical isolation for the low voltage MCU output signals from the high voltage battery power line. The photovoltaic driver is an optically isolated MOSFET drive unit which does not require any external power supply to actuate the MOSFET into conduction. It consists of a Light Emitting Diode (LED) at its input which generates light radiation upon applying a DC signal shown in Fig. 7.4. The output of the driver consists of a monolithic integrated photovoltaic generator, which generates the required higher drive voltage for actuating the power MOSFET. Compared to the turn-*ON* time, the turn-*OFF* period of the photovoltaic gate driver is larger, due to its relatively slow discharging current. In order to achieve a fast turn-*OFF* a high value gate discharge resistor R_{gd} is connected to the gate and source terminals which enables quick discharge of the MOSFET input capacitance.

7.1.5 Power Supply Module

Individual modules in the cell-level controller require different supply voltages for their operation. For instance, the computation module requires a supply voltage of $3{,}3\,\mathrm{V}$, whereas, the isolated CAN transceivers in the communication module operate with a supply of $5{,}5\,\mathrm{V}$ as shown in Fig. 7.3. Since the terminal voltage of a Li-Ion cell ranges from $2{,}7\,\mathrm{V}$ to $4{,}2\,\mathrm{V}$, a power supply module is necessary for generating a higher supply voltage and to provide constant regulated power for accurate measurement in sensing module. A two-stage power supply scheme is employed to provide the necessary operating voltage for each module of the cell-level controller as shown in Fig. 7.5.

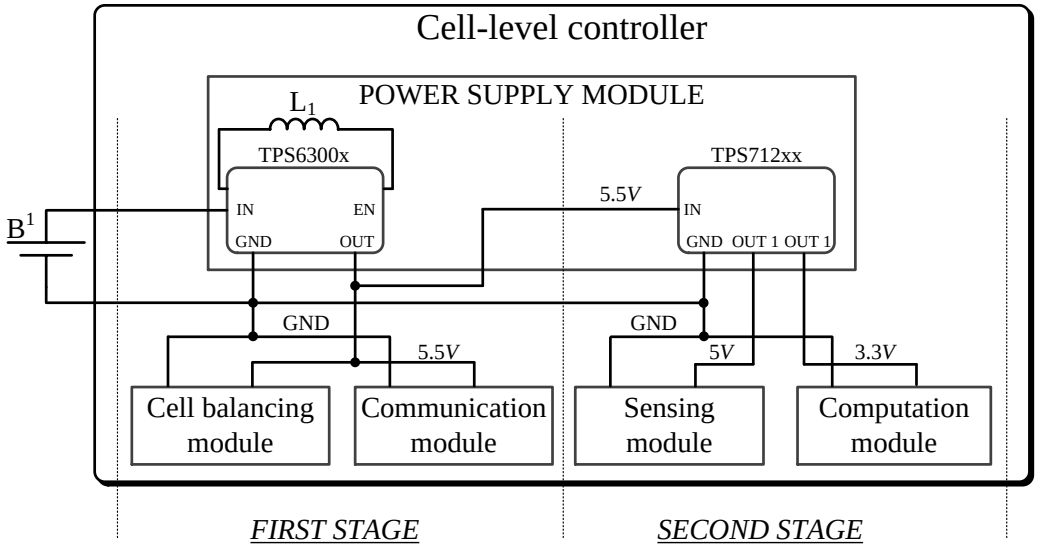
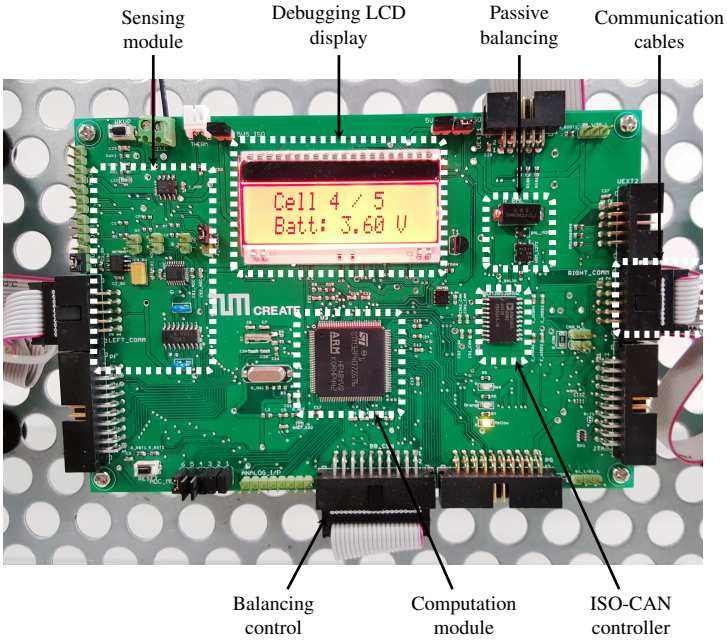


Figure 7.5: In the first stage, the cell voltage is stepped-up by using either a boost or buck-boost type switched-mode DC-DC converter to power the balancing and communication module. The boosted cell voltage is filtered and stepped-down to a lower value in the second stage by using a Low Dropout Regulator (LDO) to obtain a low-noise and ripple free supply voltage for the sensing and computation modules of the CMU.

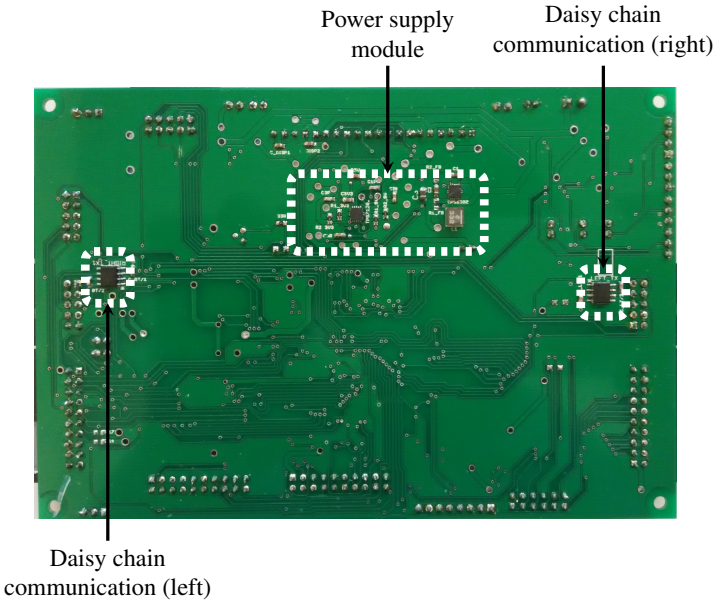
In the first stage the varying cell voltage is boosted to a higher regulated output value of $5{,}5\,\mathrm{V}$ using a buck-boost type DC-DC converter from Texas Instruments TPS6300x. This high voltage power supply is used for actuating the active cell balancing module and the internal DC-DC converter of the isolated CAN transceiver in the communication module shown in Fig. 7.3. However, operating the computation module in the cell-level controller at a high supply voltage results in an increased current consumption. Moreover, the output of the buck-boost type DC-DC converter contains high ripple content, which may not be desirable for sensing module that requires a regulated power supply for performing high accuracy measurements. Therefore, in the second stage, a high-efficiency LDO regulator is used to step-down and filter the output ripples of the first power stage. A dual output LDO from Texas Instruments TPS712xx, which provides a regulated $5\,\mathrm{V}$ and a $3{,}3\,\mathrm{V}$ output is employed. The $5\,\mathrm{V}$ power supply is required for the sensing module and the $3{,}3\,\mathrm{V}$ output power supply is used for powering the computational module of the individual cell-level control unit. The buck-boost type DC-DC converter has an EN pin as shown in Fig. 7.5, which can be utilized for implementing power management techniques such as DPM, DVFS, etc., to minimize the current consumption from the cell.

7.1.6 Cell-level Controller

Fig. 7.6 shows the custom-designed PCB implementation of the cell-level controller. All individual modules of the cell-level controller described from Section 7.1.1 to 7.1.5 are realized using off-the-shelf components on the custom-designed PCB. Each cell of a battery pack is



(a) Top side of cell-level controller board



(b) Bottom side of cell-level controller board

Figure 7.6: Custom-designed implementation of the cell-level controller in a distributed BMS topology. (a) Top side of the controller board showing sensing, computation, CAN communication and passive balancing modules. (b) Bottom side of the controller board consisting of the power supply and the daisy chain communication modules.

associated with an individual cell-level controller that monitors and controls the parameters of the cell within the safe operating limits. Consequently, a distributed BMS is formed by connecting the individual cell-level controllers through the communication channel.

Fig. 7.6a shows the top side of the cell-level controller board. Implementation of sensing, computation, passive balancing and the isolated CAN communication modules are marked. An on board Liquid Crystal Display (LCD) display is also provided for status messages and debugging purposes. Fig. 7.6b shows the bottom side of the custom-design cell-level controller PCB, where the power supply and the daisy chain communication modules are implemented. Functional verification of each module is possible by actuating its inputs with test signals and measuring the corresponding outputs without involving other modules. For example, the sensing module can be functionally verified by applying test signals at its input and the corresponding ADC data can be obtained at the output Serial Peripheral Interface (SPI) port. In addition, external DAQ systems such as oscilloscopes or LabVIEW can be easily interfaced with the cell-level controller facilitating automated data acquisition. Moreover, the isolated CAN bus shall also be tapped and connected to a PC using a suitable adapter. This enables the controllers to be operated using a system-level algorithm that is running on the PC, thereby facilitating Hardware-in-the-loop (HIL) simulation. All hardware design files of the cell-level controller PCB and the MCU firmware are uploaded in an online repository [107] for easy reproduction and evaluation of distributed BMS algorithms. Table 7.1 provides the list of components that are used to implement each module of the cell-level controller shown in Fig. 7.6.

Module	Component	Part number	Manufacturer
Power supply	Buck-boost converter	TPS6300x	Texas Instruments
	LDO	TPS712xx	Texas Instruments
Sensing module	Voltage (Difference amplifier)	INA148	Texas Instruments
	Temperature (Thermistor)	100K6A1A	Betatherm
	Balancing current (Current sense amplifier)	AD8210	Analog Devices
	Digital isolator	HCPL-092J	Avago Technologies
	Bandgap reference	REF5045	Texas Instruments
	Data conversion	ADS8341	Texas Instruments
Cell balancing (Passive)	Switching MOSFET	BUK9Y30	NXP Semiconductors
	Gate-driver	VOM1271	Vishay Semiconductors
Computation	ARM Cortex-M4	STM32F407-ZGT6	STMicroelectronics
Communication	Daisy-chain	ADuM1100	Analog Devices
	Isolated CAN	ADM3053	Analog Devices

Table 7.1: List of commercial off-the-shelf components that are used to implement the modules of the cell-level controller.

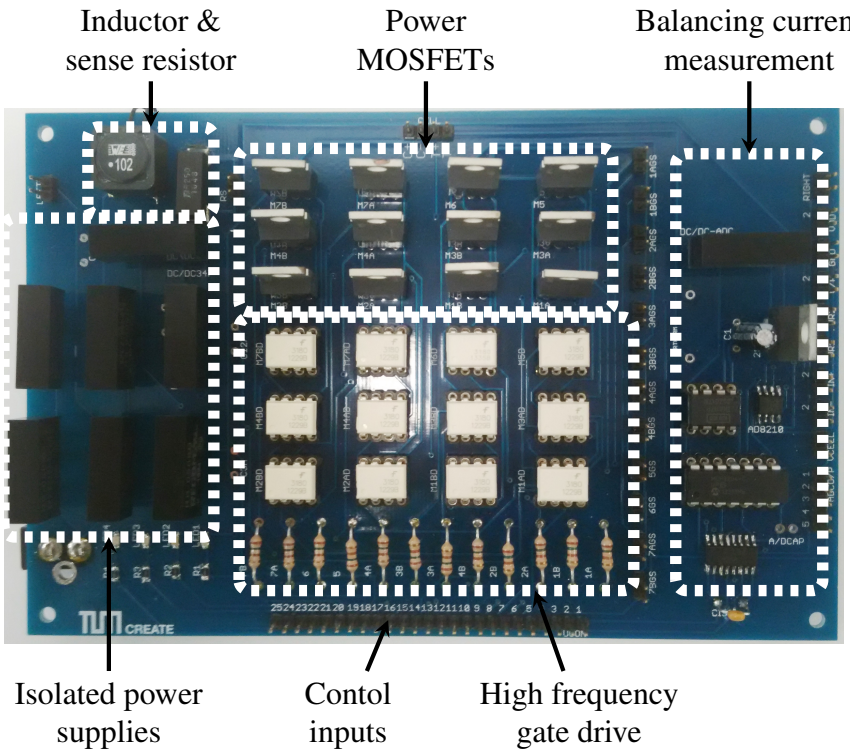


Figure 7.7: Hardware implementation of inductor-based active cell balancing architectures proposed in Chapter 6.

7.2 Implementation of Active Cell Balancing Architectures

In this Section, implementation details of the modular active cell balancing architectures that are proposed in Chapter 6 of this thesis are explained. Custom-designed PCBs for both the inductor-based and transformer-based active cell balancing architectures are developed using commercially available off-the-shelf components.

7.2.1 Inductor-based Active Cell Balancing Architecture

Fig. 7.7 shows the hardware implementation of the inductor-based active cell balancing architectures proposed in Chapter 6. With minor adjustments to the connection scheme of the MOSFETs, the same hardware implementation could be used to emulate both cell-isolating non-neighbor and the parallel-attached non-neighbor inductor-based active cell balancing architectures proposed in Section 6.1 and 6.2, respectively. The battery cell is connected at the top of the board and the control inputs from the computation module for the switching MOSFETs are connected at the bottom as shown in Fig. 7.7. Connections to other balancing units of the application to form a charge transfer bus are also provided on both sides of the PCB as shown in Fig. 7.7. Power MOSFETs from NXP semiconductors model PSMN1R6-30PL with a maximum current capacity of $100\,\mathrm{A}$ are used in the hardware implementation in order to facilitate for balancing with higher currents and also to satisfy the high power requirements of the MOSFETs in the power line of

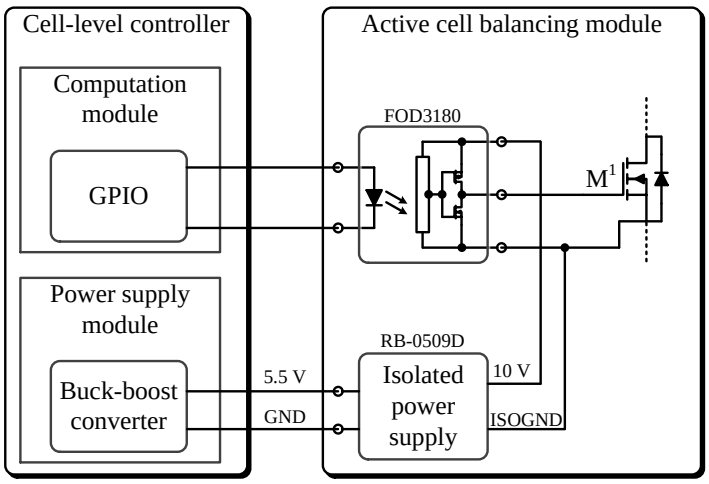


Figure 7.8: High speed gate drive implementation for the power MOSFETs in active cell balancing architectures proposed in Chapter 6. Each MOSFET that is actuated with high frequency control signal consists of a optocoupler based gate drive unit powered with an isolated power supply.

the cell-isolating inductor-based active cell balancing architecture. Moreover, all MOSFETs are provided with high speed gate drive requirement which enables the hardware implementation to be reconfigured for emulating different inductor-based active cell balancing architecture.

High frequency gate drive. Power MOSFETs in the active cell balancing architectures are connected with the power line of the battery pack and therefore they cannot be actuated directly from the computation module. Moreover, the voltage of the control signals from the computation module are in the order of 3 to 5 V which is less compared to the higher gate drive voltage required for actuating the power MOSFETs. Therefore, external gate drive units are required to interface the MOSFETs to the computation module. As shown in Fig. 4.1 gate drive for MOSFETs that are actuated with either *ON* or *OFF* DC signals can be accomplished using a photovoltaic gate drive units. However, the turn-*ON* and turn-*OFF* times of the photovoltaic gate drive components are relatively slow compared to the requirements of the high frequency actuation signals used in active cell balancing purposes that are in the range of $10\,\mathrm{kHz}$ to $100\,\mathrm{kHz}$. Therefore, they cannot be employed as gate drive units for actuating MOSFETs that are actuated with high frequency control signals. As a result, special type of gate drive arrangement is required for actuating MOSFETs that are operated with high frequency control signals.

Fig. 7.8 shows the gate drive arrangement implemented for MOSFET switches that are actuated with high speed control signals. An optocoupler based MOSFET gate drive unit from National Semiconductors FOD3180 is used to boost the low voltage control signals that are generated from the computation module of the cell-level controller. Moreover, the optocoupler gate drive unit isolates the high voltage battery and active cell balancing circuitries from the low voltage computation units. The input stage of the optocoupler gate drive unit consists of a LED which illuminates when a signal is applied at its input. The output stage is formed by a P-type

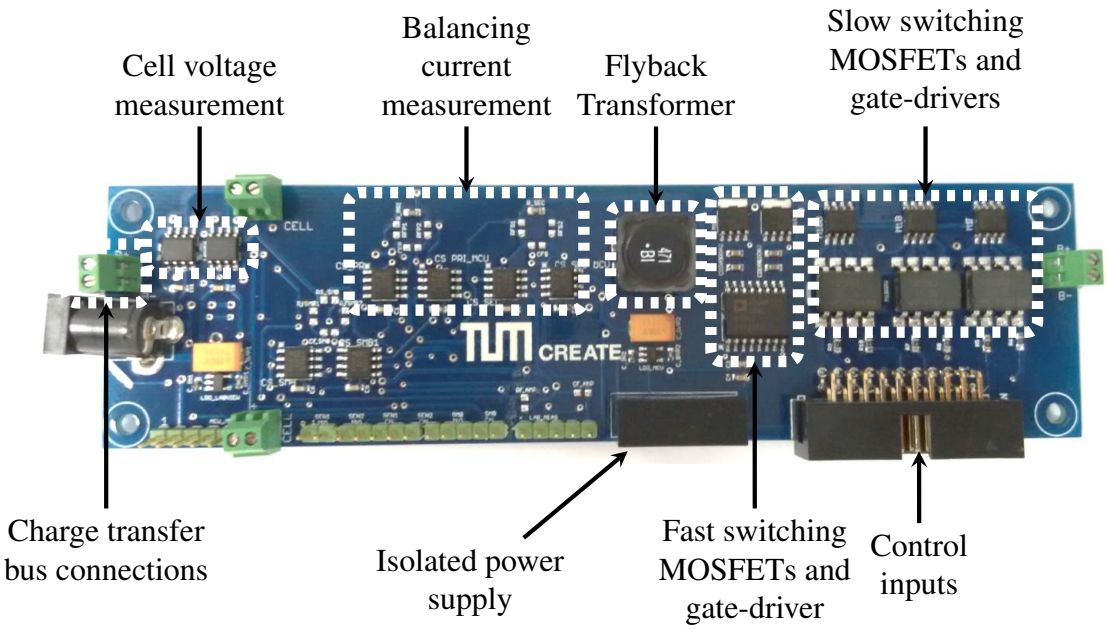


Figure 7.9: Hardware implementation of the transformer-based active cell balancing architecture proposed in Section 6.3.

and N-type phototransitor connected in push-pull arrangement as shown in Fig. 7.8. An isolated power supply unit from RECOM RB-0509D is used to obtain a higher supply voltage required for the optocoupler based MOSFET gate drive unit. This unit is powered from the output of first stage of the power supply module shown in Fig. 7.5. The high frequency control signals from the computation module actuates the input LED of the optocoupler gate drive unit and the illumination created by the LED makes the output phototransistors to conduct. During the *ON* phase of the high frequency control signal, P-type phototransistor (top transistor) conducts to connect the gate of the power MOSFET to the isolated power supply voltage. During the *OFF* phase, N-type phototransitor (bottom transistor) connects the gate of the power MOSFET to the ground in order to turn-*OFF* the MOSFET switch.

7.2.2 Transformer-based Active Cell Balancing Architecture

Fig. 7.9 shows the hardware implementation of the transformer-based active cell balancing architecture proposed in Section 6.3. Each cell of the battery pack is associated with such an active cell balancing unit and controlled by their respective cell-level controller. Control inputs from the computation module are provided on the bottom right of the board. Gate drive implementations are similar to the inductor-based active cell balancing architectures. Moreover, two sets of balancing current measurement circuitry with different power supply and ground potentials are provided. This facilitates continuous monitoring of the balancing currents from both the cell-level controller and from external DAQ systems. Charge transfer bus connections to the other balancing units are provided on both left and right side as shown in Fig. 7.9.

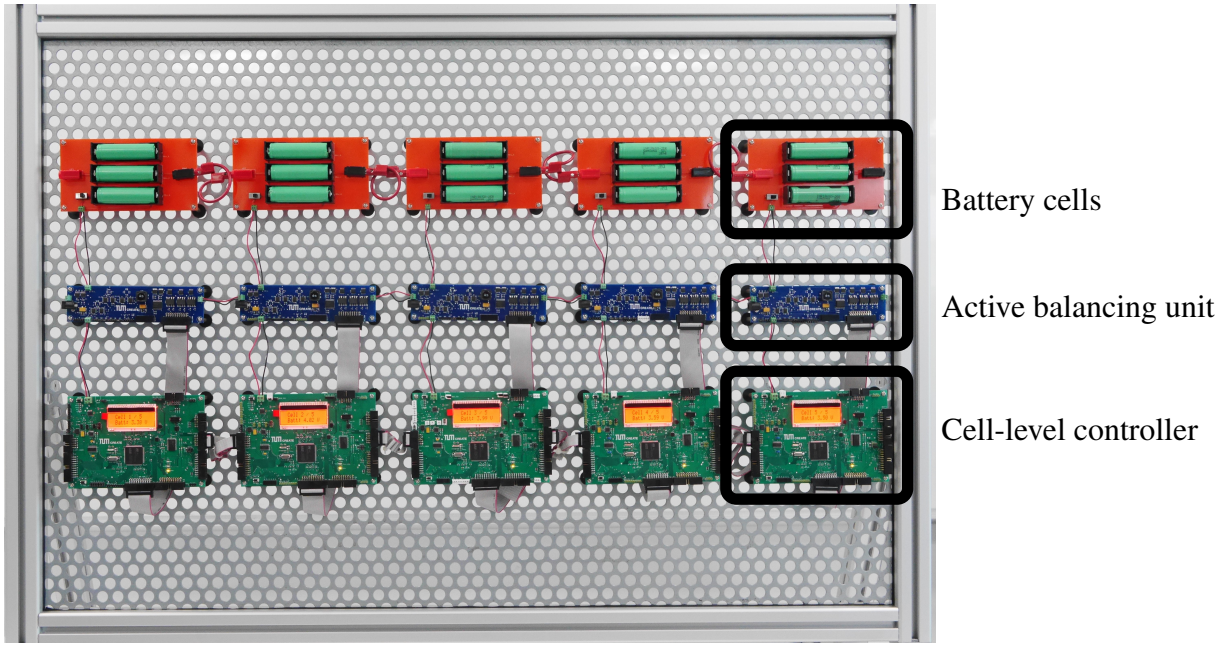


Figure 7.10: A development platform for distributed BMSs consisting of 5 series-connected Li-Ion cells and their respective control units. Each unit consists of 3 parallel-connected Li-Ion cells that is monitored and controlled by the dedicated cell-level controller and individual active cell balancing unit.

7.3 Development Platform for Distributed BMS Topology

In this section, the hardware and software implementation details of a development platform for distributed BMS topologies are explained in detail.

7.3.1 Hardware Platform of Distributed BMS Topology

The hardware implementations of the cell-level controller and the active cell balancing architectures discussed in Sections 7.1 and 7.2, respectively, are combined to form a development platform for distributed BMS topology as shown in Fig. 7.10. It consists of battery cells, active cell balancing unit and cell-level controller boards. Each battery unit in this development platform consists of 3 Samsung $2{,}5\,\mathrm{A\,h}$ capacity Li-Ion cells of 18650 form factor are connected in parallel. For safety purposes the platform uses battery cells with smaller capacity, however, hardware prototypes of the cell-level controllers and the active cell balancing architectures are capable of operating with high capacity battery cells. The power for operation of the cell-level controller and the active cell balancing units is obtained from their respective battery cells. The PCBs of the balancing unit and the cell-level controller unit are larger in size compared to the size of the battery cells in order to allow extensive debugging and measurement capability. Being a development platform it is not fully optimized for size, rather focuses on providing high-level of functional debugging capability for each module and facilitate verification of distributed algorithms. With minor modifications the development platform can be reconfigured to emulate

all distributed BMS topologies explained in Chapter 3. For instance, the cell-level controller on the last leg of the development platform can be configured to function as a master controller controlling the other cell-level controllers in order to emulate a partially distributed BMS topology. Similar reconfigurations are possible with the development platform, where the first four individual cell-level controllers can be modified as MMUs and the last controller board can be configured as the PMU for performing simulations pertaining to hierarchical BMS topology.

Moreover, the development platform can be interfaced with external data logging devices in several ways. For short time data recording, all cell-level controllers of the development platform can be used to stored the measurement data in their internal memory and periodically be read through a Personal Computer (PC). For recording data over a longer time periods, external DAQ devices such as LabVIEW, oscilloscopes can be easily interfaced with the development platform. This provides an opportunity to record multiple important parameters of the battery pack and analyze externally through data processing techniques. Furthermore, the isolated CAN bus implemented in the development platform can be interfaced with a suitable external CAN to USB adapter such as P-CAN [108]. This enables to develop custom-designed applications that can be used for both data recording and passing certain commands to the individual cell-level controllers. As a result, the development platform interfaced to an external PC over the CAN bus enables to perform a HIL simulation for verifying the functionality of distributed algorithms.

7.3.2 Software Platform of Distributed BMS Topology

In this section, details regarding the real-time operating system µC/OS-III that is running on the computation MCU of each cell-level controller is explained. The objective of using a real-time operating system is to implement the functions of the distributed BMS into several *tasks*, which are then scheduled to execute on the MCU depending upon their priority levels. Table 7.12a provides the list of tasks that are currently implemented in the µC/OS-III real-time operating system along with their priority levels. All tasks can be broadly classified into periodic and event-driven tasks. Periodic tasks are executed in a time-triggered manner while the event-driven tasks are performed on occurrence of a certain event.

The µC/OS-III real-time operating system supports multi-tasking, a process of scheduling and switching the computation MCU between several tasks. A *Preemptive*, *priority-based* scheduling algorithm is followed in µC/OS-III, where tasks with higher priority when they are ready-to-run can preempt the execution of low priority tasks. In addition, tasks with equal priority levels are scheduled based on a *round-robin* scheduling algorithm in which case each ready-to-run task of the same priority is executed for a defined time period called as *time quanta*. After the specified *time quanta* the operating system executes the next available ready-to-run task of the same priority level. Fig. 7.12b shows an example timing diagram of the scheduling process in the µC/OS-III real-time operating system. The entire scheduling process is visualized as a state diagram consisting of states representing the status of each task as shown in Fig. 7.11.

Ready state consists of tasks that are ready-to-run on the computation MCU. Depending upon their priority level and the scheduling algorithm they are executed by the MCU and moved to *running* state as shown in Fig. 7.11. If the task moved to the *running* state is an event-driven task and the corresponding event has not occurred, then it will be moved from the *ready* state to

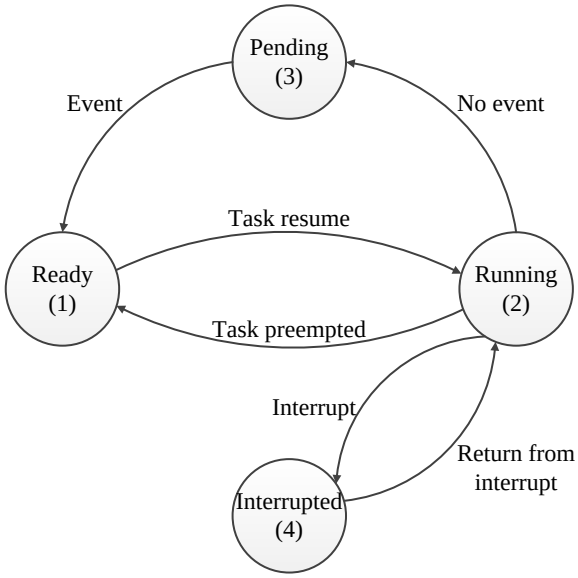


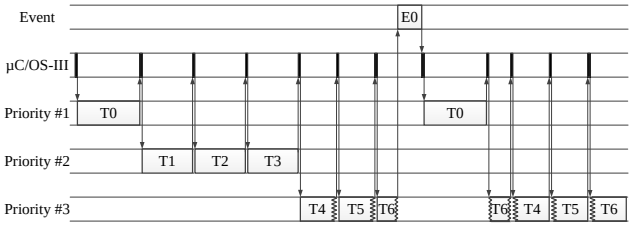
Figure 7.11: State diagram representing the scheduling process of the µC/OS-III real-time operating system used in the computation MCU of the distributed BMS development platform.

the *pending* state, where it waits for the corresponding event to take place. Tasks waiting for an event to occur in the *pending* state does not consume any MCU operation time. Once the corresponding event occurs the task is moved from the *pending* state to the ready state, notifying the operating system. The µC/OS-III real-time operating system checks the priority-level of the newly readied task and preempts the execution of the current task if the newly ready-to-run task is of higher priority. In addition to preemption from higher priority tasks, the task that is currently executing can be preempted by incoming interrupts as shown in Fig. 7.11. Interrupts are always considered as higher priority in µC/OS-III real-time operating system and when an interrupt occurs the task moves from the *running* state to the *interrupted* state. The task is executed after the execution of the Interrupt Service Routine (ISR) that is associated with the specific interrupts.

Fig. 7.12b shows the scheduling process of the µC/OS-III real-time operating system. Tasks with equal priorities are executed for a predefined time period and then the scheduler executes the next ready-to-run task of equal priority. This *round-robing* scheduling process can be seen in Fig. 7.12b, where equal priority tasks $T4$ (*CurrentSampling*), $T5$ (*VoltageAverage*) and $T6$ (*StatusMessage*) do not run for completion once executed. Instead, each task runs for the same amount of time period and then the next equal priority task is executed. This maintains equal resource utilization for all tasks that are at the same priority levels. Preemption from higher priority tasks can stop the execution of the currently running low priority task and the OS shifts the high priority task into *running* state for execution. This is shown in Fig. 7.12b, where the higher priority task $T0$ (*ProcessCANMsg*) gets executed preempting the low priority task $T6$ (*StatusMessage*) as soon as the event $E0$ occurs, which in this case is an incoming CAN message. The preempted low priority task moves to the *ready* state and begins execution from the same point where it was preempted, only after the processing of high-priority task is finished.

Task ID	Task name	Priority	Trigger type
$T0$	*ProcessCANMsg*	1	Event
$T1$	*PackMonitoring*	2	Periodic
$T2$	*ChargeRequesting*	2	Periodic
$T3$	*ChargeAcknowledge*	2	Periodic
$T4$	*CurrentSampling*	3	Periodic
$T5$	*VoltageAverage*	3	Periodic
$T6$	*StatusMessage*	3	Periodic

(a) Tasks of distributed BMSs.



(b) Scheduling algorithm of OS.

Figure 7.12: µC/OS-III real-time operating system timing diagram and tasks. (a) Distributed BMS functions implemented as tasks in the real-time operating system. (b) Timing diagram of the scheduling process of the µC/OS-III real-time operating system.

7.4 Integration Perspective

The individual modules of the cell-level control units can be integrated into a system on chip, with supporting accessory off-chip components in a small PCB. This significantly reduces the time-to-market of a scalable battery pack, where only mechanical integration has to be planned, keeping the electrical and the software architecture fixed by the homogeneous design. Some of the implementation options chosen for each module presented in the previous section, may not be suitable for on-chip integration due to size or increased current consumption. For this purpose an outlook towards integration choices of each module is presented in this section.

Sensing module. The cell voltage is monitored using a difference amplifier as shown in Fig. 7.1a. Low-noise, high gain and high CMRR Complimentary Metal-Oxide Semiconductor (CMOS) implementation of a difference amplifier is possible [109] and hence we can keep the same choice of implementation for the voltage measurement part in the sensing module. The surface temperature of the cell is measured using a thermistor sensor and a resistor-divider as shown in Fig. 7.1b. Depending upon the type of thermistor sensor the resistor-divider network changes and therefore it should be kept as an off-chip component to allow flexibility in choosing different sensors. Even though, integrating the current sense amplifier for measuring balancing currents as shown in Fig. 7.1c is possible [110], the sense resistor should be kept as an off-chip component to prevent the flow of high value balancing currents inside the chip. The entire data conversion part consisting of the ADC, band-gap reference voltage and the digital isolator as shown in Fig. 7.1d can be integrated into a single chip [111].

Computation module. Low-power processing is the key requirement of the computational module in the cell-level controller, which is enabled by using several power management techniques such as DVFS and DPM in the computational module. Moreover, tri-core processing units are required for certification purpose in safety-critical applications such as EVs and HEVs. Therefore, three instances of the computational core must be provided, where all computations

are performed independently in each of the computational element and the combined result is used as output. Certain BMS functions (cell parameters measurement, fault detection) listed in Table 3.1 can be implemented as hard-core fabric using Hardware Descriptive Language (HDL), that enables faster processing and efficient implementation. On the other hand, certain BMS functions (SoC and SoH estimation) which depend upon the application details require configuration at a later stage. Therefore, some reconfigurable, soft-core fabric must be available in the computational module that is capable of running application programs written using a high-level programming language. Apart from the Arithmetic and Logical Unit (ALU), the computational unit must also have the PWM and general-purpose timers for control of active cell balancing and the necessary communication interface.

Communication module. Both daisy chain and a bus communication architecture are required in a distributed BMS topology to efficiently perform all cell and pack-level functions in a timely manner. To obtain isolation for the communication signals in the daisy chain architecture, integrated monolithic transformers providing isolation up to $4\,\mathrm{kV}$ RMS [112] can be employed. Even though the CAN communication interface can be integrated, it consumes high current due to the in-built isolated DC-DC converter. Therefore, alternative form of bus communication topology is required for distributed BMSs. Capacitively coupled data transmission system [51] and [52], with a bandwidth of $250\,\mathrm{kbps}$ could be a preferred for integrating the bus communication architecture. Even though the bandwidth offered by the capacitive solution is lower than the CAN bus ($1\,\mathrm{Mbps}$), having smart algorithms that efficiently use both the daisy-chain and the bus topology will enable to meet the required deadlines for tasks. Moreover, the current consumption of the capacitive based solution is much lower compared to the isolated CAN transceivers, thereby favoring it as an on-chip solution for the bus communication module.

Cell balancing module. For passive balancing currents in the range of $500\,\mathrm{mA}$ the balancing resistor could be integrated into the cell-level controller chip [22]. However, for higher values of balancing currents an external power resistor is required with an external MOSFET switch to limit the flow of higher currents into the chip. By contrast, the active cell balancing architecture proposed in this thesis involve very high currents and therefore, they should be implemented as off chip components. Nevertheless, the gate drive units of slow and fast switching MOSFETs can be integrated into the cell-level controller.

Power supply. A two stage power supply scheme was implemented in the cell-level controller of the distributed BMS shown in Fig. 7.5. This implementation choice was chosen to support the high current requirement of isolated power supplies in the communication and cell balancing modules of the cell-level controller. However, with alternative low-power options for these modules in the integrated version, other choices for power supply module can be utilized to minimize the number of off-chip components. One suitable choice for power supply module would be an integrated charge pump converter [113], which can be used to boost the cell voltage to a sufficient value required for the sensing module and satisfy the current requirements for the communication and balancing modules. In addition, the output of the charge pump converter has

to be regulated with an integrated LDO [114], to obtain a ripple-free, supply voltage for sensing and computation modules of the cell-level controller.

7.5 Summary

In this section, implementation details of the cell-level controller and the proposed active cell balancing architectures were explained in detail. The hardware implementation of the cell-level controller and the active cell balancing architectures are combined to form a distributed BMS development platform. This platform can be reconfigured to emulate different distributed BMS topologies explained in Chapter 3. Moreover, using the development platform functional verification of the proposed active cell balancing architectures is performed in the next chapter. In addition, high accuracy measurements are taken using the hardware implementation of the active cell balancing architectures integrated with the development platform for validating the closed-form analytical model developed in Chapter 5.

8 Experiments and Validation

In this Chapter, experimental validation of the architectures and analytical models presented in this thesis are performed. The different charge transfer scenarios of the proposed active cell balancing architectures in Chapter 6 are functionally verified by integrating their hardware implementations into the distributed BMS development platform presented in Chapter 7. Different sets of high accuracy measurements taken using the hardware implementation of the active cell balancing architectures are used to validate each part of the analytical model presented in Chapter 5. Using the validated analytical model case studies are performed to show the system-level active cell balancing simulation methodology and the effectiveness of the optimization approaches proposed in Sections 5.3.2 and 5.4, respectively.

8.1 Functional Verification of Active Cell Balancing Architectures

The hardware implementation of the modular active cell balancing architectures discussed in Chapter 7 are functionally verified by integrating it with the distributed BMS development platform described in Section 7.3. The cell-level controller associated with each cell of the development platform is programmed with the control scheme of the respective active cell balancing architectures proposed in Chapter 6. It generates the necessary high frequency control signals and the constant DC output signals for actuating the MOSFETs in order to perform charge transfers between cells. Balancing currents and the voltages of the cells are measured by interfacing the development platform to external high accuracy LabVIEW type DAQ system. All charge transfer scenarios of the proposed active cell balancing architectures are verified in the following sections.

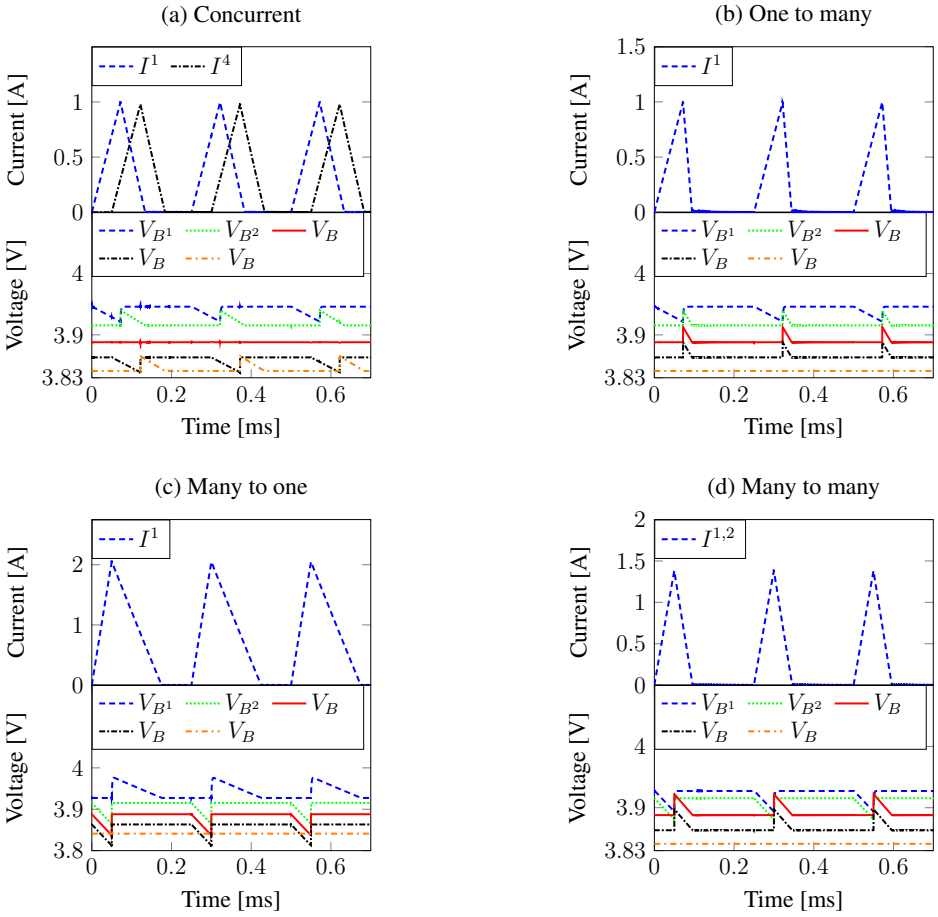


Figure 8.1: Functional verification of the cell-isolating inductor-based active cell balancing architecture. (a) Concurrent charge transfers $B^1 \rightarrow B^2$ and $B^4 \rightarrow B^5$, while B^3 is in idle mode. (b) One to many charge transfer scenario where cell B^1 transfers charge to B^2, B^3 and B^4. (c) Many to one charge transfer example with cells B^2, B^3 and B^4 transferring charge to B^1. (d) B^1 and $B^2 \rightarrow B^3$ and B^4 forms the many to many charge transfer scenario.

8.1.1 Cell-isolating Inductor-based Active Cell Balancing Architecture

Fig. 8.1 shows the functional verification of the possible charge transfer scenarios of the cell-isolating inductor-based active cell balancing architecture proposed in Section 6.1.4. Fig. 8.1a verifies the concurrent charge transfer capability where cell B^1 transfers charge to B^2 and at the same time charge is transferred from cell B^4 to B^5. However, as explained in Section 6.1.4, the cell-isolating inductor-based active cell balancing architecture requires the adjacent cells of the charge transfer pair to be in blocking mode. In this example, cell B^3 is not involved in the charge transfer process in order to avoid potential short circuits between cells. Fig. 8.1b shows the scenario of transferring charge from a single cell (B^1) to a group of cells (B^2, B^3 and B^4). The slope of the inductor discharging current is more steeper than the charging phase as observed from the current waveforms shown in Fig. 8.1b. This is due to the higher voltage across the inductor during the discharging phase formed by the 3 series-connected compared to the voltage

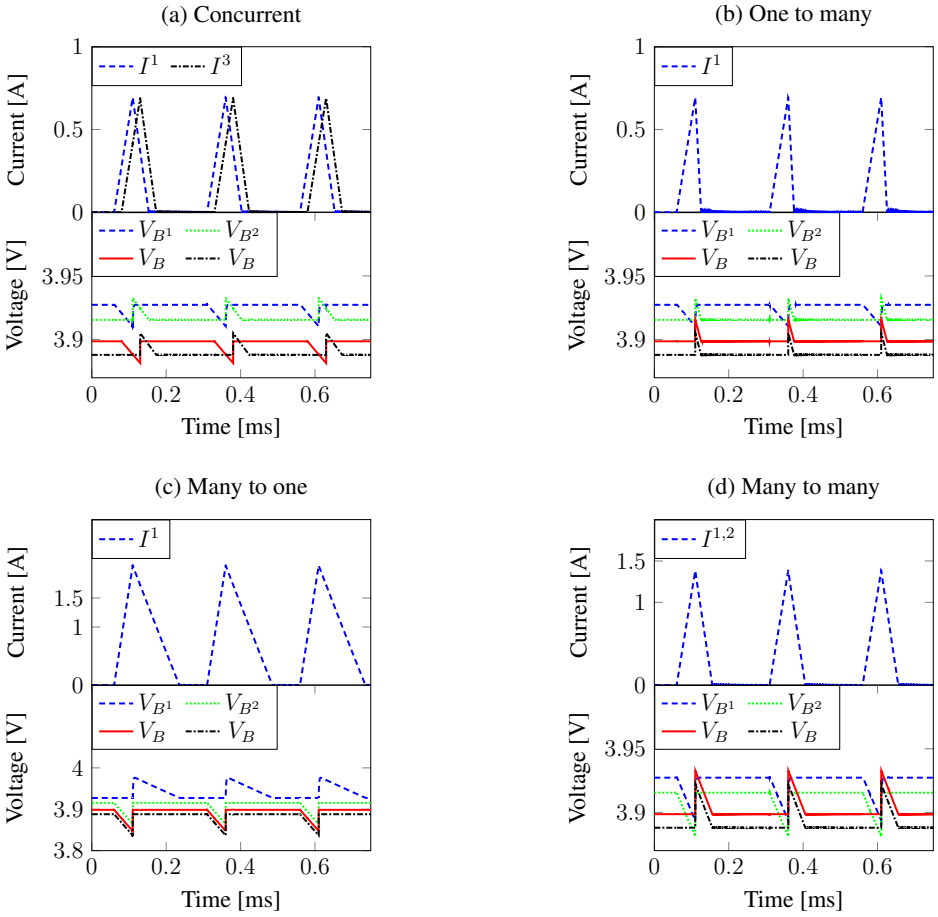


Figure 8.2: Functional verification of the parallel-attached inductor-based active cell balancing architecture. (a) 100 % concurrent charge transfers, $B^1 \rightarrow B^2$ and $B^3 \rightarrow B^4$. (b) One to many charge transfer scenario, $B^1 \rightarrow B^2, B^3$ and B^4. (c) Many to one charge transfer, B^2, B^3 and $B^4 \rightarrow B^1$. (d) B^1, $B^2 \rightarrow B^3$, B^4 shows many to many charge transfer scenario.

of a single cell during the charging phase. Similar observations can be made with Fig. 8.1c, where a higher voltage during charging phase formed by the series connection of B^2, B^3 and B^4 results in a steeper charging of the inductor compared to the discharging phase where the voltage across the inductor is only from cell B^1. Finally, the capability of the proposed balancing architecture to transfer charge from multiple source cells (B^1, B^2) to multiple destination cells (B^3, B^4) as claimed in Section 6.1.4 is verified using the hardware implementation and shown in Fig. 8.1d.

8.1.2 Parallel-attached Inductor-based Active Cell Balancing Architecture

With minor modifications to the connection scheme between the switches and the cell and between the balancing boards, the same hardware implementation shown in Fig. 7.7 can emulate the parallel-attached inductor-based active cell balancing architecture proposed in Section 6.2 of

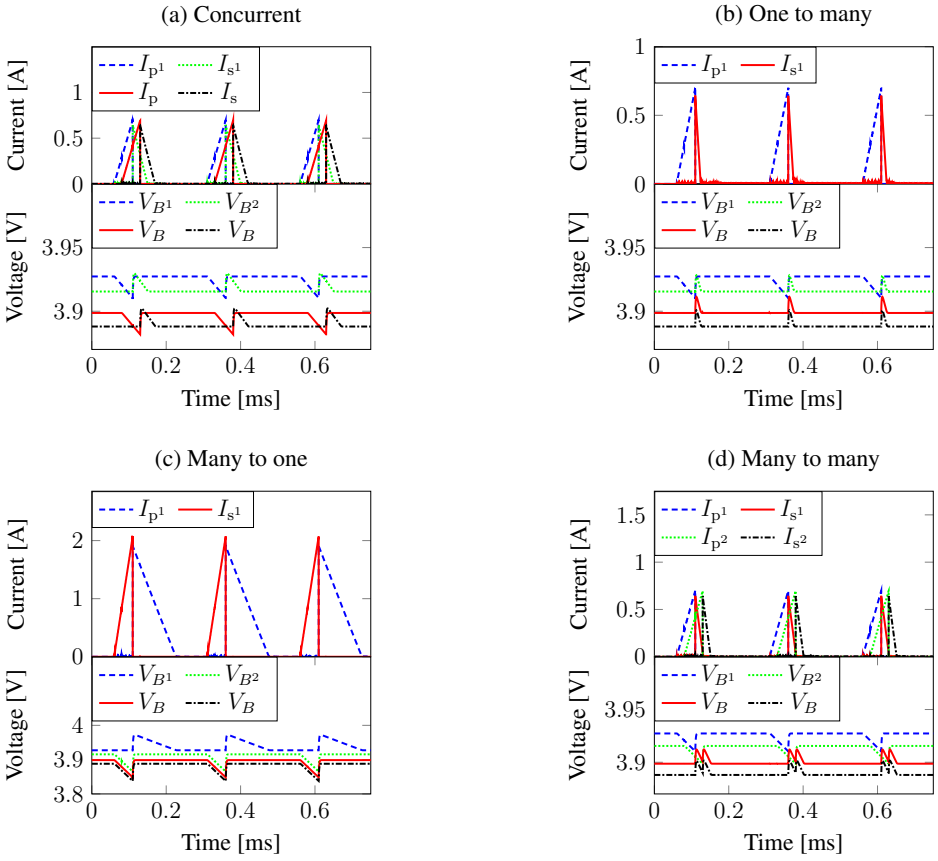


Figure 8.3: Functional verification of the transformer-based active cell balancing architecture. (a) Concurrent, $B^1 \rightarrow B^2$ and $B^3 \rightarrow B^4$. (b) One to many, $B^1 \rightarrow B^2, B^3$ and B^4. (c) Many to one, B^2, B^3 and $B^4 \rightarrow B^1$. (d) $B^1, B^2 \rightarrow B^3, B^4$ the many to many charge transfer scenario.

this thesis. Functional verification of the parallel-attached active cell balancing architecture and its possible charge transfer scenarios described in Section 6.2.4 are evaluated using the distributed BMS development platform. By implementing the control scheme for the MOSFET switches described in Table 6.2 in each cell-level controller all required high frequency control signals and the constant DC signals for performing charge transfer between cells can be generated. The results of the functional verification is shown in Fig. 8.2.

Fig. 8.2a shows the concurrent charge transfer scenario. As described in Section 6.2, unlike the cell-isolating active cell balancing architecture, the parallel-attached inductor-based architecture does not require the adjacent cells of the charge transfer pair to be in blocking mode. As a result, $100\,\%$ concurrent charge transfers are possible with the parallel-attached inductor-based active cell balancing architecture. This is functionally verified in Fig. 8.2a where cell B^1 transfers charge to cell B^2 and at the same time charge can be transferred from cell B^3 to B^4 without any short circuit situations. Fig. 8.2b verifies the one to many charge transfer scenario and Fig. 8.2c verifies the capability of performing many to one charge transfers with the parallel-attached inductor-based active cell balancing architecture. Finally, Fig. 8.2d shows

the many to many charge transfer scenario of the parallel-attached inductor-based active cell balancing architecture verified using the distributed BMS development platform.

8.1.3 Transformer-based Active Cell Balancing Architecture

Finally, the hardware implementation of the transformer-based active cell balancing architecture proposed in Section 6.3 was integrated with distributed BMS development platform for verifying the possible charge transfer scenarios claimed in Section 6.3.5. For this purpose, the cell-level controller associated with each cell in the development platform is programmed with the switching scheme of the transformer-based architecture described in Table 6.1. Depending upon the charge transfer scenario verified appropriate MOSFET switches are actuated by the cell-level controller. Both primary and secondary winding currents of the transformer along with voltage of all cells are measured using LabVIEW DAQ system.

Fig. 8.3 shows the functional verification of the proposed transformer-based active cell balancing architecture. The $100\,\%$ concurrent charge transfer capability of the transformer-based active cell balancing architecture is shown in Fig. 8.3a, where cell B^1 transfers its excess charge to cell B^2 and at the same time charge is transferred from cell B^3 to B^4. Fig. 8.3b and 8.3c verifies the one to many and many to one charge transfer capabilities of the transformer-based active cell balancing architecture claimed in Section 6.3.5. Finally, charge transfer from multiple source cells to multiple destination cells is verified in the development platform and the result is shown in Fig. 8.3d. Note in all graphs, the secondary winding current of the transformer does not start from the same point where the primary winding was fully charged during the charging phase, due to the effect of leakage inductance described in Section 5.2.3.3.

8.2 Model Validation

In addition to the functional verification of the proposed active cell balancing architectures, the closed-form, analytical model of the charge transfer process derived in Chapter 5 is validated using the measurements taken with the hardware implementation. A LabVIEW type DAQ system is integrated with the distributed BMS development platform and different sets of high accuracy measurements are taken for varying values of balancing currents. Each part of the analytical model derived in Section 5.2 is validated using the measurement data.

8.2.1 Balancing Current Model Validation

The balancing current model during charging and discharging phases derived in Sections 5.2.1 and 5.2.2 are validated for both inductor and transformer-based active cell balancing architectures.

8.2.1.1 Inductor-based Active Cell Balancing Architecture

An inductor with an inductance of $22\,\mu\mathrm{H}$ from the product family [115] is implemented in the inductor-based active cell balancing architecture board shown in Fig. 7.7. Peak value of balancing current I_{peak} is chosen to be half the *C*- rate of the battery cells ($3{,}5\,\mathrm{A}$), where 1C

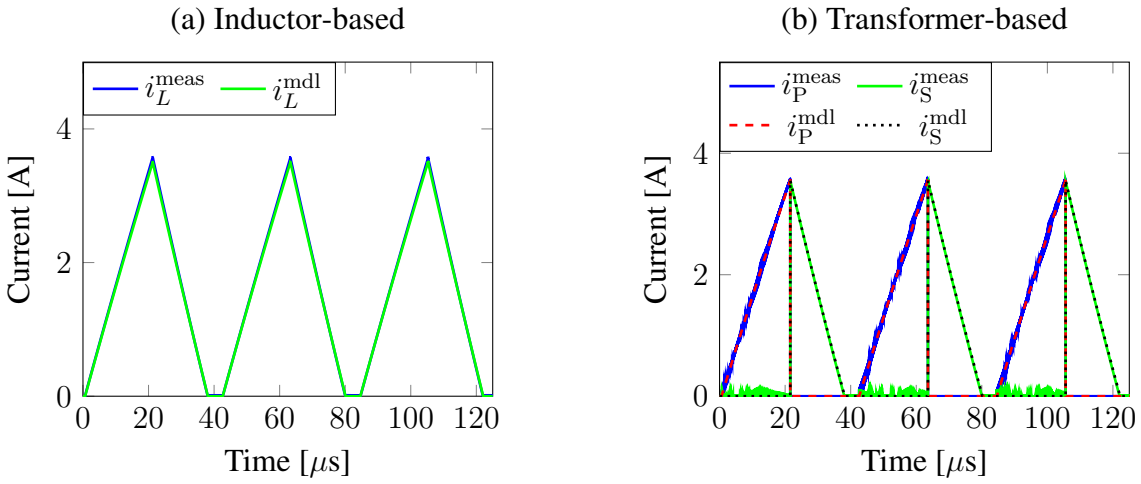


Figure 8.4: Validation of balancing current model of both (a) inductor-based and (b) transformer-based active cell balancing architectures. The measured balancing currents from the hardware implementation agrees well with the closed-form analytical model.

stands for charging and discharging the battery cell in one hour. The times T_{ON} and T_{OFF} of the high frequency control signals σ^1 and σ^2 required to achieve the desired I_{oeak} are calculated based on Eqns. (5.9) and (5.15), respectively. The cell-level controller of the distributed BMS development platform is programmed to generate the necessary high frequency control signals with the calculated timing values. Balancing current through the inductor and the cell voltages are recorded with a high accuracy LabVIEW DAQ system.

The closed-form analytical model derived in Section 5.2 is simulated with the corresponding cell voltages and the balancing currents. Fig. 8.4a shows the measured (i_L^{meas}) balancing current from the hardware implementation of the inductor-based active cell balancing architecture and the balancing current obtained from the closed-form analytical models (i_L^{mdl}) derived in Chapter 5. As seen from Fig. 8.4a the balancing current outputs from the closed-form analytical model matches with the real measurements from the hardware implementation with a maximum relative error of $5\,\%$.

8.2.1.2 Transformer-based Active Cell Balancing Architecture

A flyback transformer with an inductance of $22\,\mu\text{H}$ is chosen for model validation purpose. The hardware implementation of the transformer-based active cell balancing architecture is controlled by the cell-level controller of the distributed BMS development platform. Timing values T_{ON} and T_{OFF} are programmed in the cell-level controller to generate the necessary high frequency control signals σ^1 and σ^2, respectively. High accuracy measurements of both the primary and secondary winding currents of the transformer are made using a LabVIEW DAQ system. Fig. 8.4b shows the result of the charge transfer current model validation of the transformer-based active cell balancing architecture. It can be observed that the closed-form analytical model of the balancing current in the transformer-based active cell balancing architecture agrees well with the measured primary and secondary winding currents with a maximum relative error of $4\,\%$.

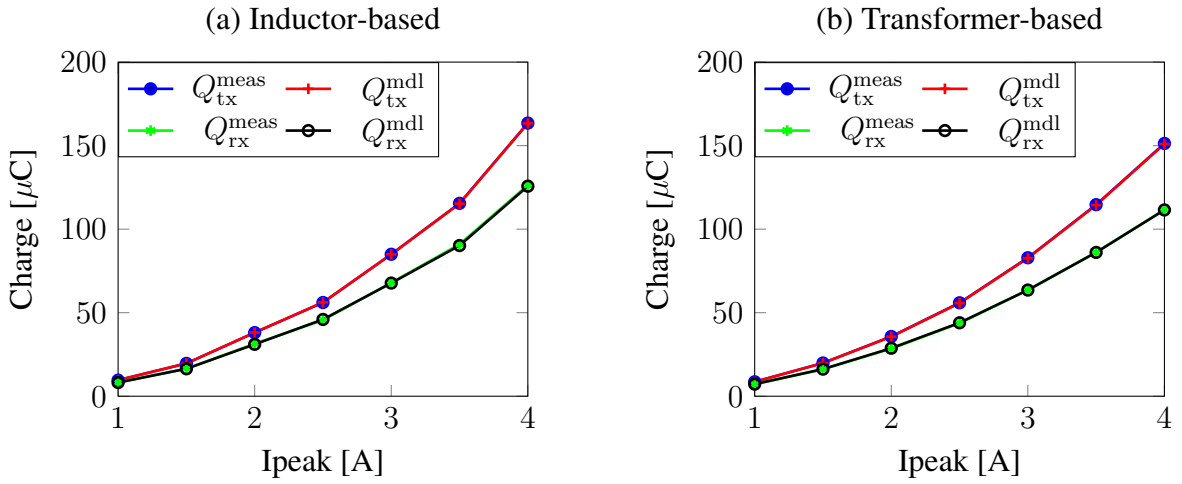


Figure 8.5: Validation of charge transferred and received model of both (a) inductor-based and (b) transformer-based active cell balancing architectures. The measured values from the hardware implementation agrees well with the closed-form analytical model.

8.2.2 Charge Transfer Model Validation

Upon validating the balancing current in both inductor and transformer-based active cell balancing architectures, in this section, validation of the transferred and received charge modeled by Eqns. (5.10) and (5.16), respectively, is performed. For this purpose, multiple charge transfer cycles between the source and destination cells are performed with different peak current values using the hardware implementation of the active cell balancing architectures.

8.2.2.1 Inductor-based Active Cell Balancing Architecture

The hardware implementation of the inductor-based active cell balancing architectures is connected to the distributed BMS development platform. The cell-level controller is programmed with the validated balancing current model for generating the necessary high frequency control signals for performing charge transfers. The peak value of the balancing current is varied in equidistant steps and for each value the cell voltages and the current through the inductor are recorded using a LabVIEW type DAQ system. The measured charge that is transferred $Q_{\mathrm{tx}}^{\mathrm{meas}}$ and received $Q_{\mathrm{rx}}^{\mathrm{meas}}$ for each value of the balancing current is obtained by numerical integration from the measurements. Similarly, the charge transfer model is simulated with the experimental data to obtain $Q_{\mathrm{tx}}^{\mathrm{mdl}}$ and $Q_{\mathrm{rx}}^{\mathrm{mdl}}$ from Eqns. (5.10) and (5.16), respectively. Fig. 8.5a shows the measured and model charge that is transferred and received during the balancing process for each value of peak inductor current. It can be observed that the charge transfer model of the inductor-based active balancing architecture accurately matches with the measurement data with a maximum relative error of $3\,\%$.

8.2.2.2 Transformer-based Active Cell Balancing Architecture

The hardware implementation of the proposed transformer-based active cell balancing architecture is integrated with the distributed BMS development platform for performing charge transfer measurements at different peak current values. The measured charge that is transferred $Q_{\mathrm{tx}}^{\mathrm{meas}}$ and received $Q_{\mathrm{rx}}^{\mathrm{meas}}$ for each peak value of the balancing current is obtained through numerical integration. Fig. 8.5b shows the validation of the charge transfer model, where the measured transferred and received charges agrees well with the modeled transferred and received charges, $Q_{\mathrm{tx}}^{\mathrm{mdl}}$ and $Q_{\mathrm{rx}}^{\mathrm{mdl}}$, respectively. The maximum observed relative error from the model and the measured values is in the range of $4\,\%$. From Fig. 8.5b it can be observed that at higher values of balancing currents, the effect due to leakage inductance of the transformer become more significant. As explained in Section 5.2.3.3, for higher values of peak current the time Δt taken to discharge the energy stored in the leakage inductance increases and this delays the primary-secondary energy transfer, thereby reducing the value of Q_{rx}.

8.3 Case Study

In this section, a case study for the system-level simulation methodology described in Section 5.3.2 is performed using the transformer-based active cell balancing architecture proposed in Section 6.3 of this thesis. Furthermore, the optimal dimensioning and control approaches discussed in Section 5.4 are evaluated using commercial off-the-shelf components and the results are explained in detail.

8.3.1 System-level Simulation

The validated balancing current model and charge transfer model can be used to perform system-level performance analysis of the proposed active cell balancing architecture using Algorithm 1 described in Section 5.3.2. For a case study, the transformer-based active cell balancing architecture proposed in Section 6.3 is utilized. The component values in the active cell balancing architecture are as follows:

The battery pack used in the case study consists of 96 series-connected modules with each module formed by connecting 24 Li-Ion cells of $2{,}5\,\mathrm{A\,h}$ each. SoC of all series-connected modules are randomly initialized around an average value of $45\,\%$ with a variance of 0.02. Balancing strategy *fast* proposed in [58] is used for identifying the set of charge transfer pairs $\mathcal{P}$ in line 3 in Algorithm 1. For each identified pair p in $\mathcal{P}$, the times T_{ON} and T_{OFF} required for achieving the specified I_{peak} value for the above circuit configuration is calculated based on Eqns. (5.9) and (5.15), respectively. Similarly, the transferred (Q_{tx}) and received (Q_{rx}) charges over the time period T_{ON} and T_{OFF} are computed according to Eqns. (5.10) and (5.16), respectively. As explained in Section 5.3.2, the transferred and received charges are small in value compared to the charge levels of Li-Ion cells and therefore transfers are performed in macro cycles. Energy dissipated, both conduction and switching, for each macro step period for all charge transfer pair are computed through the validated analytical models. SoC of all cells are updated after each charge transfer cycle as shown in line 13 in Algorithm 1.

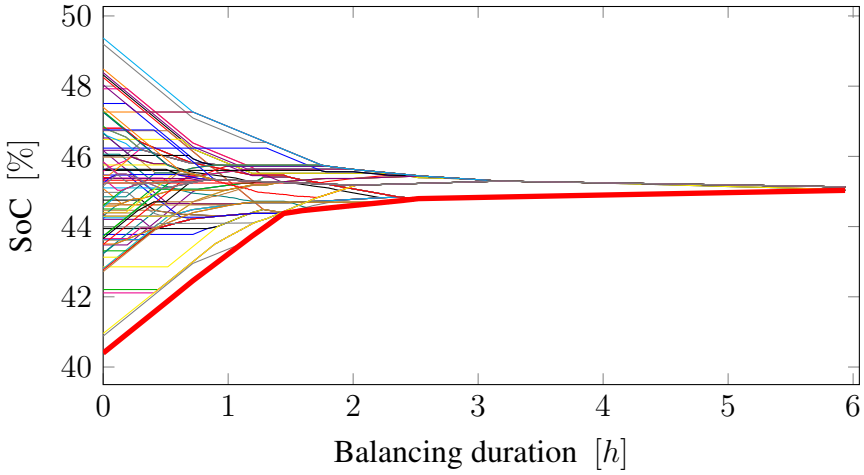


Figure 8.6: SoC evolution of all cells in the battery pack while balancing.

Fig. 8.6 shows the SoC evolution over balancing time for the battery pack considered in this case study. It also shows the evolution of the overall pack SoC (—), which is the minimum SoC value of all cells in the battery pack. The proposed transformer-based active cell balancing architecture using the above circuit configuration, equalizes the SoC of all cells in the battery pack within $6\,\mathrm{h}$. The final pack SoC after equalization is around $44{,}8\,\%$, whereas the initial pack SoC was $40\,\%$.

8.3.2 Optimization Results

In this section, the design space exploration and the control point optimization methodologies for improving the energy-efficiency of an active cell balancing architecture are evaluated for the cell-isolating and parallel-attached inductor-based active cell balancing architectures proposed in Sections 6.1 and 6.2, respectively. As explained in Section 5.4, the design of an active cell balancing architecture is a trade-off between energy-efficiency and the installation area. Smaller values of parasitic resistances of inductors and MOSFETs will result in a higher energy-efficiency. However, for minimizing the parasitic resistances of the inductor, thick winding coils are required which will eventually increase the installation area. Similar trade-off exist for MOSFETs where increased size of the device will have a reduced *ON*-resistance providing higher energy-efficiency. Therefore, the choice of components forming the active cell balancing architecture has to be optimized for providing higher energy-efficiency and at the same time consume a smaller installation space.

The design space that needs to be optimized for the objectives listed in Table 5.1 consists of the following commercial off-the-shelf components

- 100 inductors (L_{ind})
- 25 high power MOSFETs (M_{hp})
- 92 low power MOSFETs (M_{lp})

- 92 switching MOSFETs (M_{sw})
- $I_{peak} = \{1, 2, 3, 4, 5, 6, 7, 8, 9, 10\}$

The SoCs of source and destination cells are initialized with $50\,\%$ to $45\,\%$.

For the case of cell-isolating inductor-based active cell balancing architecture, the design space needs to be additionally pruned to identify the non-dominated slow switching MOSFET combinations as explained in Section 5.4.4.3, since it consists of two high power MOSFETs (M_s^i, M_p^i) in the power-line of the battery pack and six slow switching MOSFETs that are not actuated with high frequency control signals. After pruning the design space of slow switching MOSFETs and using Algorithm 2 to the filtered design space, for all peak current values in I_{peak}, 965,913 total number of possible circuit configurations were identified for the cell-isolating inductor-based active cell balancing architecture. For the case of parallel-attached inductor-based active cell balancing architecture, where all MOSFETs carry the same amount of balancing current, Algorithm 2 with above component set produced 35,548 total number of possible design configurations.

From these combinations Pareto-optimal design points that are not dominated by other configurations for each value of the balancing current are computed. A design configuration C_{c_1} dominates another design configuration C_{c_2} if

$$I_{C_{c_1}}^{\max} > I_{C_{c_2}}^{\max} \text{ and } E_{C_{c_1}}^{\text{diss}} < E_{C_{c_2}}^{\text{diss}} \text{ and } A_{C_{c_1}} < A_{C_{c_2}}$$

Upon applying the above ideology to the set of possible configurations, 855 and 197 total Pareto-optimal design configurations were found for the cell-isolating and parallel-attached inductor-based active cell balancing architectures that are not dominated by other circuit configurations. This is shown in Fig. 8.7a for the cell-isolating inductor-based architecture and Fig. 8.7b for the parallel-attached inductor-based active cell balancing architecture.

Furthermore, as discussed in Section 5.4.5.1, for each Pareto-optimal design point, the optimal control point ξ_p when performing non-neighbor balancing varies depending upon d, the number of balancing modules that are in between the source and destination cells of the charge transfer pair. This is due to the fact that the equivalent parasitic resistance in the charge transfer phases changes depending upon the position of the source and destination cells in the series string of the battery pack. For the case of the inductor-based active cell balancing architectures proposed in Chapter 6 of this thesis, the equivalent resistances during the charge transfer phases depending upon d is shown in Table 8.1.

One design configuration from the set of Pareto-optimal design space is selected to show the improvement in energy-efficiency obtained by dynamically changing the operating point depending upon the position of the source and destination cells of the charge transfer pair. The parameters of the components in the selected Pareto-optimal design point is shown in Table 8.2. The optimal control point ξ_p for charge transfer between adjacent cells using the circuit configuration listed in Table 8.2 at a peak current of $10\,\text{A}$ is 0.2. To identify the control point for non-neighbor balancing, charge transfer simulations are performed using the component values listed in Table 8.2 for equalizing source and destination cells that are initialized with $50\,\%$ and $45\,\%$ SoC, respectively. The distance d representing the number of balancing modules that are in between the source and destination cells of the charge transfer is varied from 0 to 10. For

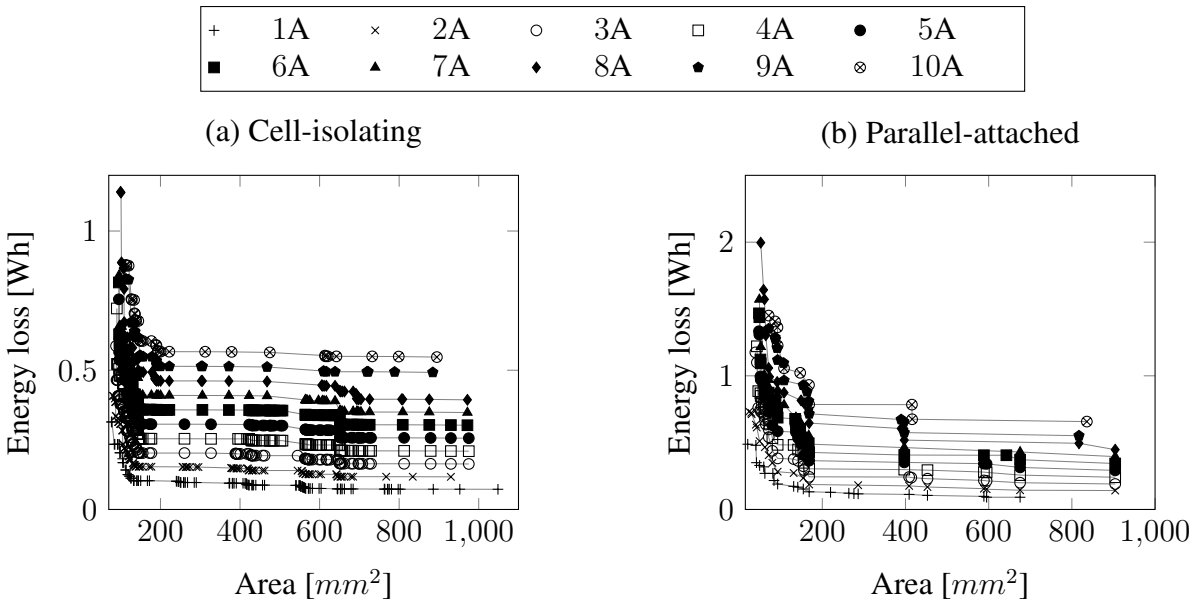


Figure 8.7: (a) Pareto-optimal design configurations for the cell-isolating inductor-based active cell balancing architecture and (b) for parallel-attached inductor-based active cell balancing architecture.

each value of d, the optimal control point is identified and the improvement in energy-efficiency compared to the operating point of neighbor-only case is calculated.

Fig. 8.8 shows the improvement in energy-efficiency obtained with dynamically computing the optimal operating point depending upon the number of balancing modules that are in between the source and destination cells of the charge transfer pair. It can be observed that for smaller values of d, the parasitic resistances contributed by the additional balancing modules in between the charge transfer pair is less and therefore a small amount of improvement in energy-efficiency is obtained. However, when the charge transfer pair of cells are farther apart from each other in the series-chain of the battery pack, the number of balancing modules in between the source and destination cells and consequently the contribution due to the parasitic resistances of the MOSFETs in the current flow path increases. In such cases operating the active cell balancing

	Cell-isolating	Parallel-attached
R_α	$R_{\mathrm{B}^\alpha} + R_{\mathrm{L}} + R_{\mathrm{M_{sw}}} + 2 \cdot R_{\mathrm{M_{lp}}} + R_{\mathrm{M_{hp}}}$	$R_{\mathrm{B}^\alpha} + R_{\mathrm{L}} + 3 \cdot R_{\mathrm{M}}$
R_β	$R_{\mathrm{B}^\beta} + R_{\mathrm{L}} + (d+1) \cdot (R_{\mathrm{M_{hp}}} + R_{\mathrm{M_{sw}}}) + 4 \cdot R_{\mathrm{M_{lp}}}$	$R_{\mathrm{B}^\beta} + R_{\mathrm{L}} + (7 + 2 \cdot d) R_{\mathrm{M}}$

Table 8.1: Equivalent resistances during charge transfer phases of the cell-isolating and parallel-attached inductor-based active cell balancing architectures depending upon d, the number of balancing modules that are in between the source and destination cells of the charge transfer pair.

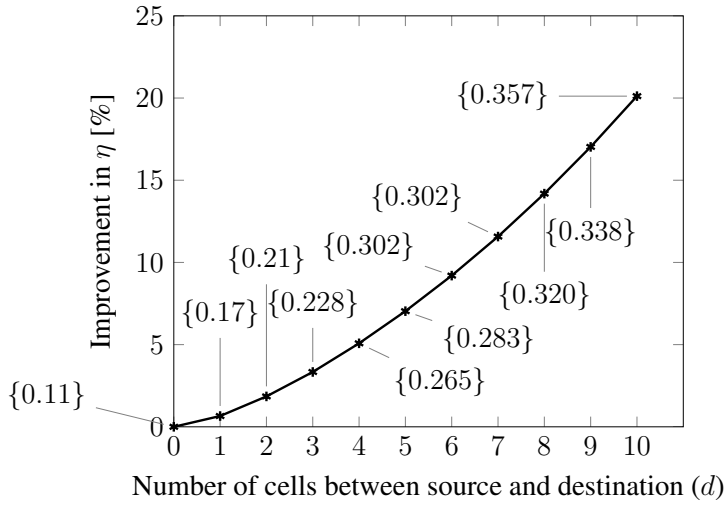


Figure 8.8: Dynamically adjusting the operating point according to the number of balancing modules between the source and destination cells provides a maximum of $22\,\%$ improvement in energy-efficiency compared to operating at the optimal control point for the neighbor-only charge transfer case.

architecture at a fixed control point is no longer energy-efficient. Here, the operating point of the active cell balancing architecture must be computed dynamically based on the number of balancing modules that are in between the source and destination cells. By performing dynamic optimization of the operating point at run time up to $20\,\%$ improvement in energy-efficiency can be obtained compared to operating at fixed control point especially for larger values of d as shown in Fig. 8.8. The system-level impact of the optimal circuit configuration, optimal control point and dynamic optimal control are shown in the following section.

Inductance		High-power MOSFET		Low-power MOSFET		Switching MOSFET	
Parameter	value	Parameter	value	Parameter	value	Parameter	value
Manufacturer	Würth	Manufacturer	NXP	Manufacturer	Vishay	Manufacturer	ON-Semiconductor
Model	7443632200	Model	PSMN0R925YLD	Model	SiA400EDJ	Model	NTMFS4C55NT1G
Resistance	$10{,}65\,\mathrm{m\Omega}$	Resistance	$0{,}85\,\mathrm{m\Omega}$	Resistance	$19\,\mathrm{m\Omega}$	Resistance	$3{,}4\,\mathrm{m\Omega}$
Inductance	$22\,\mu\mathrm{H}$					t_{ON}	$43\,\mathrm{ns}$
						t_{OFF}	$30\,\mathrm{ns}$
						C_{OSS}	$1215\,\mathrm{pF}$

Table 8.2: Component values of a Pareto-optimal design point that is used for the dynamic optimal control point case study.

8.3.3 System-level Impact of Optimal Dimensioning and Control

In this section, a system-level simulation is performed using the algorithm presented in Section 5.3.2 for analyzing the performance improvement obtained by choosing optimal circuit configurations and control point in comparison to a random selection of components. The simulation framework considers 96 series-connected modules and in each module 10 Li-Ion cells with each having a capacity of $2{,}5\,\mathrm{A\,h}$ are connected in parallel. All parallel-connected cells are electrically considered as a single unit and balancing takes place only between modules that are connected in series. SoC of all series-connected modules are initialized randomly around a average value of $57\,\%$ with a variance of 0.02. The initial energy distribution of the battery pack considered for this case study is shown in Fig. 8.9. To equalize the SoC of all cells in the battery pack and to improve its usable capacity the simulation framework considers the parallel-attached inductor-based active cell balancing architecture proposed in Section 6.2 of this thesis.

The equalization process is carried out with two set of component values. An optimal design configuration with reduced energy dissipation and installation area from the Pareto-front of the parallel-attached inductor-based architecture presented in Fig. 8.7b is selected and simulated at its optimal control point. Moreover, dynamic calculation of the operating point depending upon d, the number of balancing modules that are in between the source and destination cells of the charge transfer pair, as explained in Section 5.4.5.1 is implemented in the simulation framework. To show the effectiveness of the proposed optimization approaches, a dominated circuit configuration from the design space of the parallel-attached inductor-based active cell balancing architecture is also selected to simulate the performance characteristics. The component values of the dominated and optimal circuit configurations are listed in Table 8.3. The peak value of the balancing current in the simulation is assumed to be $5\,\mathrm{A}$.

Fast balancing strategy proposed in [58] is used to identify the source and destination cells of the charge transfer pair depending upon the SoC distribution of all cells in the battery pack. The simulation is performed according to Algorithm 1 proposed in Section 5.3.2. In the case of simulation with the Pareto-optimal circuit configuration, for each identified pair of source and destination cells, the equivalent resistance along the charge flow direction is calculated with the expression in Table 8.1. Similarly, the optimal control point for each value of d are computed dynamically as explained in Section 5.4.5.1. With the optimal control point and

Parameter	Pareto-Optimal design choice	Random circuit combination
L	$33\,\mu\mathrm{H}$	$3{,}3\,\mu\mathrm{H}$
R_L, R_M	$2{,}4\,\mathrm{m\Omega}$, $3\,\mathrm{m\Omega}$	$10\,\mathrm{m\Omega}$, $15\,\mathrm{m\Omega}$
t_{ON}, t_{OFF}	$54\,\mathrm{ns}$, $75\,\mathrm{ns}$	$32\,\mathrm{ns}$, $35\,\mathrm{ns}$
C_{OSS}	$800\,\mathrm{pF}$	$260\,\mathrm{pF}$
E_{diss}	$27{,}73\,\mathrm{W\,h}$	$139{,}23\,\mathrm{W\,h}$

Table 8.3: Values of Pareto-optimal design choices and random circuit combinations used in the system-level simulation analysis.

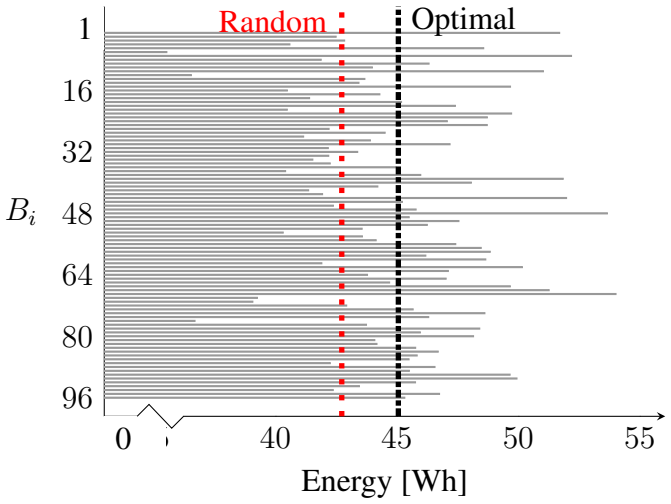


Figure 8.9: Initial energy distribution of a battery pack consisting of 96 series-connected Li-Ion cells considered for the system-level performance evaluation of choosing optimal circuit configurations and control scheme. The final average equalized energy of the battery pack using the Pareto-optimal design point is higher compared to a random design choice.

circuit component values the times T_{ON} and T_{OFF} required for the inductor current to reach points I_{p^2} and I_{p^1} are computed as per the validated model described in Eqns: (5.35) and (5.38). Charge transferred (Q_{tx}) and received (Q_{rx}) are also computed for the time period according to Eqns. (5.36) and (5.39). The energy transferred and dissipated as conduction and switching losses for each charge transfer cycle are computed according to the validated analytical model described in Section 5.2.3. These steps are repeated for all charge transfer pairs identified by the equalization strategy and the process is continued until the deviation in SoC of all modules in the battery pack is within $0{,}1\,\%$.

The vertical bars in Fig. 8.9 are the final average energy stored in the battery pack after equalization using a Pareto-optimal circuit configuration with dynamically computed optimal control point and a random choice of circuit components. It can be observed that choosing an optimal circuit configuration and selecting an energy-efficient control point of operation (.....) increases the average usable energy output of the battery pack compared to a random choice of circuit components (. . .). Table 8.3 shows the total energy dissipation (E_{diss}), which is the sum of conduction and switching energy dissipations over the entire equalization process. This is calculated by adding the individual energy dissipations computed by Eqns. (5.18), (5.40) and (5.41) for each charge transfer cycle, till the overall battery pack is equalized. The optimal choice of circuit components and control algorithm results in $80\,\%$ less energy dissipation compared to a random choice of circuit components and control point.

8.4 Summary

In this chapter, the charge transfer features of all proposed active cell balancing architectures are verified using their hardware implementations. High accuracy measurements taken using

the hardware implementation were used to validate the closed-form analytical model. Using the validated analytical-model a case study was performed to show the effectiveness of the optimization approach proposed in Chapter 5. Optimized circuit components operated at their optimal control points dissipate up to $80\,\%$ less energy compared to a random choice of circuit components.

9 Concluding Remarks

Distributed BMS topologies in comparison with the centralized approaches provide significant advantages such as easier integration, better monitoring and control capability and improved reliability by minimizing potential single point of failures. However, there exist certain design challenges at different abstraction levels of distributed BMS topologies that need to be addressed. This thesis proposed modular, efficient electrical architectures and analytical models that form the groundwork for finding solutions to the design challenges that are associated with higher abstraction levels of distributed BMSs.

9.1 Summary

The contributions of this thesis towards addressing the open design challenges of distributed BMSs are:

- Cell-level controller design and implementation
- Modular active cell balancing architectures
- Analytical modeling and optimization approaches

Cell-level Controller Design. Depending upon the cell-level and pack-level functions performed by a typical distributed BMS, the necessary modules required for each cell-level controller was proposed. This consist of the sensing module for monitoring the cell parameters, power supply module for ensuring low power consumption, active cell balancing module for increasing the usable capacity of the battery pack, galvanically isolated communication module and a high performance computational unit for calculating SoC and SoH of the cell. Specifications for each module was developed and a homogeneous, modular electrical architecture for each module

of the cell-level controller was proposed. Commercial off-the-shelf components satisfying the specification of each module was identified and a custom-designed hardware implementation of the cell-level controller was developed. The hardware implementation is designed in such a way that each module in the cell-level controller can be independently characterized by applying test inputs and their corresponding outputs can be measured without involving other modules of the cell-level controller. A distributed BMS demonstrator platform was developed, which consisted of five series-connected Li-Ion cells each associated with an individual cell-level controller. The demonstrator platform served as a testbed for verifying the cell and pack-level functions of a distributed BMS topology. With the capability to interface different high accuracy DAQ systems, the distributed BMS development platform was used for functional evaluation of the proposed active cell balancing architectures and validation of the developed analytical, closed-form models.

Modular active cell balancing architectures. This thesis proposed three modular active cell balancing architectures that satisfy the design requirements of distributed BMS topologies. All proposed architectures consist of homogeneous balancing units attached to each cell of the battery pack. A system-level active charge transfer architecture was enabled by interconnecting the homogeneous units. The proposed balancing architectures provides improved charge transfer capabilities such as direct non-neighbor balancing, percentage of concurrency, multiple source to destination cells charge transfer which are not typically supported by state-of-the-art modular approaches. Control scheme for actuating the switches in the each homogeneous unit for performing several charge transfer scenarios were derived. Moreover, hardware implementation of all proposed active cell balancing architectures were developed and their functionality and charge transfer patterns were verified by integrating into the distributed BMS development platform. All design files of both the distributed BMS development platform and active cell balancing architecture are uploaded in an online repository and made publicly accessible. This enables easy reproduction of the set-up and provides the necessary starting framework for the scientific community to validate their distributed software algorithms for BMSs.

Analytical models and optiization approaches. The hardware implementations of the active cell balancing architectures developed in this thesis were predominantly used for functional verification of the claimed charge transfer possibilities. To analyze the system-level performance of the proposed active cell balancing architectures, this thesis developed accurate, closed-form analytical models including the parasitic losses present in the individual circuit components. Using the analytical model, a fast, system-level simulation algorithm was proposed for analyzing the performance improvement achieved with the active cell balancing process on a battery pack level. Moreover, high accuracy measurements are made using the hardware implementations of the active cell balancing architectures and each part of the analytical model was validated. Using the validated analytical model optimization approaches for improving the energy-efficiency of the active cell balancing architectures were proposed. An efficient and fast design space exploration was performed in this thesis for optimally selecting the circuit configurations of the active cell balancing architecture that increases the energy-efficiency of the equalization process compared to a random choice of circuit components. In addition, for each optimal circuit configuration of the active cell balancing architectures, energy-efficient control points of

operation depending upon the position of source and destination cells of the charge transfer pair were identified. A system-level case study performed with the optimal circuit configurations and control point indicated that up to $80\,\%$ savings in the energy dissipation could be obtained by optimally selecting the circuit configurations and actuating them at the optimal control point of operation.

9.2 Future Work

While this thesis provides the fundamental electrical architecture of the cell-level controller and proposed multiple modular active cell balancing architectures, there are some challenges to address for further improvements and commercialization.

Integrated cell-level controler. The necessary modules in each cell-level controller were derived and their specifications were drafted in a detailed fashion. However, the implementation at present is performed using commercial off-the-shelf components on a custom-designed PCB. This involves both an increased installation space and weight of the cell-level controller. This might not be suitable for implementation in range limited applications such as EVs, HEVs, etc., where additional weight of the battery pack will significantly affect the driving range achievable with the vehicle. Therefore, a silicon integrated version of the cell-level controller architecture proposed in this thesis is required to satisfy the stringent requirements of mobile EES applications. Moreover, an integrated version can be mass produced and could minimize the application cost of the distributed BMS.

Active cell balancing strategies. While multiple modular, energy-efficient active cell balancing architectures were proposed in this thesis, for maximizing the system-level performance smart equalization algorithms are required. Charge transfers using the proposed modular active cell balancing architectures happens in pair of cells with one or many source and destination cells in each pair. Active cell balancing strategies determine the source and destination cells of the charge transfer pair depending upon the SoC distribution of the battery pack. The goal of the equalization algorithms must be to maximize the available pack capacity and it should fully utilize the capabilities of the underlying hardware architecture of the active cell balancing unit. While there exists several equalization strategies, none of them are optimized for the balancing architectures that are proposed in this thesis. Therefore, an essential future work towards this direction is to proposed equalization algorithms that utilizes the proposed active cell balancing architectures to its fullest extent for improving the energy-efficiency of the balancing process.

Reconfiguration of active cell balancing architectures. As shown in the optimization approaches proposed in this thesis the circuit configurations of the active cell balancing architectures are optimal at a particular value of balancing current. Depending upon the external environment factors, the required balancing current value might change. For example, in case of an EV, it is not required to equalize the battery pack with a higher current value when the vehicle is parked over night. However, if the same battery pack has to be equalized in a fast manner, for example standing over in a traffic light, then the required balancing current is higher.

Therefore, depending upon the external environmental factors the equalization time and accordingly the required balancing current value will change. An active cell balancing architecture with fixed circuit configuration that is optimal for a given balancing current might not provide energy-efficient equalization at a different value of balancing current. Moreover, all proposed active cell balancing architectures in this thesis are capable of performing direct charge transfer between non-adjacent cells in the battery pack. This increases the energy-efficiency in terms of non-neighbor balancing compared to state-of-the-art approaches that can only perform neighbor only charge transfers and equalizes the SoC difference between non-adjacent cells in multiple hops through all intermediate cells. However, when comparing the energy-efficiency of an equalization between adjacent cells, the direct non-neighbor balancing architectures will have a higher energy dissipation compared to the neighbor only approaches due to the increased number of MOSFETs in the current flow path. Therefore, methodology to dynamically change the component parameters depending upon the required balancing current value and reconfiguring the active cell balancing architecture depending upon the charge transfer pair of cells are required for improving the energy-efficiency of the equalization process.

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Abbreviations

ADC Analog to Digital Converter

ALU Arithmetic and Logical Unit

ASIC Application Specific Integrated Circuit

BMS Battery Management System

CAN Controller Area Network

CMOS Complimentary Metal-Oxide Semiconductor

CMRR Common-Mode Rejection Ratio

CMU Cell Management Unit

CSA Current Sense Amplifier

CTM Continuous Transfer Mode

DAC Digital to Analog Converter

DAQ Data Acquisition

DPM Dynamic Power Management

DTM Discontinuous Transfer Mode

DVFS Dynamic Voltage and Frequency Scaling

EES Electrical Energy Storage

EKF Extended Kalman Filter

EMI Electro-Magnetic Interference

EV Electric Vehicle

HDL Hardware Descriptive Language

HEV Hybrid Electric Vehicle

HIL Hardware-in-the-loop

HVAC Heating, Ventilation and Air Conditioning

IC Integrated Circuit

ICE Internal Combustion Engine

IGBT Insulated-Gate Bipolar Transistor

ISR Interrupt Service Routine

LCD Liquid Crystal Display

LDO Low Dropout Regulator

LED Light Emitting Diode

Li Lithium

Li-Ion Lithium-Ion

MCU Micro Controller Unit

MMU Module Management Unit

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

Ni Nickel

NiMH Nickel-Metal Hydride

OCV Open Circuit Voltage

ODE Ordinary Differential Equation

PC Personal Computer

PCB Printed Circuit Board

PFM Pulse Frequency Modulation

PMU Pack Management Unit

PWM Pulse Width Modulated

RTD Resistance Temperature Detector

SoC State-of-Charge

SoH State-of-Health

SPI Serial Peripheral Interface

SPICE Simulation Program with Integrated Circuit Emphasis

UART Universal Asynchronous Receiver Transmitter