Optimal Dimensioning of Active Cell Balancing Architectures

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***Abstract*—This paper presents an approach to optimal dimensioning of active cell balancing architectures, which are of increasing relevance in Electrical Energy Storages (EESs) for Electric Vehicles (EVs) or stationary applications such as smart grids. Active cell balancing equalizes the state of charge of cells within a battery pack via charge transfers, increasing the effective capacity and lifetime. While optimization approaches have been introduced into the design process of several aspects of EESs, active cell balancing architectures have, until now, not been systematically optimized in terms of their components. Therefore, this paper analyzes existing architectures to develop design metrics for energy dissipation, installation volume, and balancing current. Based on these design metrics, a methodology to efficiently obtain Pareto-optimal configurations for a wide range of inductors and transistors at different balancing currents is developed. Our methodology is then applied to a case study, optimizing two state-of-the-art architectures using realistic balancing algorithms. The results give evidence of the applicability of systematic optimization in the domain of cell balancing, leading to higher energy efficiencies with minimized installation space.**

I. Introduction

The demand for efficient, high capacity Electrical Energy Storages (EESs) is increasing continuously, particularly driven by the growing Electric Vehicle (EV) market and stationary EES applications in smart grids which are gaining momentum. For such high power and energy density requirements, Lithium-Ion (Li-Ion) cells are dominating in most applications. This battery chemistry, however, is very sensitive to its operating parameter range. Out-of-specification operation can lead to irreversible damage, that, in the worst case, could result in fire or explosion of the battery pack. Therefore, sophisticated Battery Management Systems (BMSs) monitor and control the battery, maintaining its parameters within a safe operating range.

An important function of the BMS is cell balancing, equalizing the charge values of all cells in the battery pack. In (high voltage) batteries with series topologies of many cells, the overall State of Charge (SoC) is determined by the cell with the lowest charge, as the discharging cannot be continued when the first cell reaches the lower discharging threshold. Conservative state-of-the-art approaches incorporate *passive* cell balancing, where the charge of all cells is reduced to the one of the cell with the lowest charge by dissipating excess charge via a switched resistor. While being widely adopted, this approach is inefficient from an energy perspective.

Energy efficiency is one of the main drivers of modern EES applications. Therefore, *active* cell balancing architectures are emerging which are capable of transferring charge between cells instead of dissipating it. As a result, the energy efficiency and effective capacity of these batteries is significantly increased in comparison to passive cell balancing solutions.

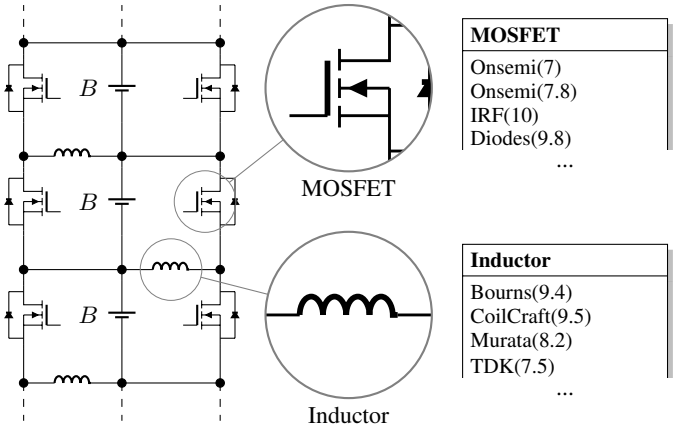

Fig. 1: Active cell balancing circuits are relying on electrical components to transfer the charge between different cells (B). Choosing the appropriate type of transistors and inductors is a challenging task.

While active cell balancing has been scientifically explored from an architectural perspective, it has not yet been investigated from an optimization point of view. Consider the state-of-the-art architecture illustrated in Figure 1. Here, several inductor and Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) variants can be selected for the final circuit design. Every feasible configuration for a certain balancing current will change the energy dissipation and the installation volume of the architecture.

Contributions of the paper. There is, as we will show in this paper, a significant potential for optimization with respect to the introduced design metrics. An optimized design, in turn, results in a higher energy efficiency of the balancing process, hence conserving energy that otherwise would be wasted. For this purpose, we present an approach to optimally dimension active cell balancing architectures.

In particular, we make the following contributions: (1) We analyze two state-of-the-art active cell balancing architectures and develop design metrics for energy dissipation, installation volume, and balancing current. (2) Based on the introduced design metrics, this paper proposes a methodology to evaluate design choices by involving a simulation of the cell balancing algorithms. (3) Finally, we present a case study for which we efficiently obtain Pareto-optimal solutions for two state-of-the-art architectures, using realistic balancing algorithms.

Organization of the paper. The remainder of this paper is organized as follows. Section II discusses related work in the area of cell balancing and optimization approaches for EESs. Two state-of-the-art inductor-based active cell balancing architectures are discussed in Section III in order to develop design metrics in Section IV. Based on these metrics, a design evaluation approach is presented in Section

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V. In Section VI, this approach is applied to the presented state-of-the-art architectures before the paper is concluded in Section VII.

II. Related Work

Several approaches to cell balancing for Li-Ion batteries exist in literature. A comprehensive overview is presented in [1], [2]. Active balancing architectures involving capacitor-based charge transfer [3], [4] suffer from the inherent energy loss that is associated with capacitor charging. While transformers can be applied in active cell balancing [5], such approaches require huge installation space and heavy hardware and are infeasible for applications such as EVs where weight and space are critical. Therefore, inductor-based charge transfer architectures are the most promising group, enabling concurrent charge transfer between neighboring cells in the battery string [6] or, as a further improvement, fast and efficient transfer between non-adjacent cells [7].

While optimization has not been considered in literature in the specific area of cell balancing architectures, in the domain of EVs, approaches to optimization for system-level energy efficiency have been performed from different perspectives, mostly on a high abstraction level. From an embedded systems perspective, the efficiency of charge migration in an Hybrid Electric Vehicle (HEV) is optimized for a battery and supercapacitor EES architecture [8]. In [9], this optimization is further extended involving the BMS. On the other hand, the optimization of charging patterns in order to optimize charging efficiency of EVs is another approach to increase the overall system efficiency [10]. In the domain of stationary hybrid EES, an optimization approach for the control methodology of a charge transfer architecture is presented in [11]. In [12] an optimization of the cycle efficiency of such systems is performed.

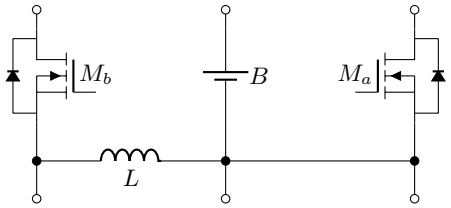
Optimization of circuit parameters has been considered in the electronic circuit domain, where a wide range of approaches has been developed to optimize the circuit performances. In order to enable automated circuit sizing, approaches have optimized performances of integrated circuits such as operational amplifiers and voltage controlled oscillators [13] as well as in the domain of power electronics [14].

Existing approaches to the optimization of EES energy efficiency do not cover the optimal dimensioning of cell balancing circuits. Therefore, in this paper, we will propose an approach to efficiently obtain Pareto-optimal solutions for the multi-objective optimization problem of minimizing the energy dissipation and volume of active cell balancing architectures at different balancing currents. This contributes to further increase the energy efficiency of the EES system architectures for applications in EVs or stationary solutions in smart grids, where, until now, the optimization potential of the cell balancing process has not been considered.

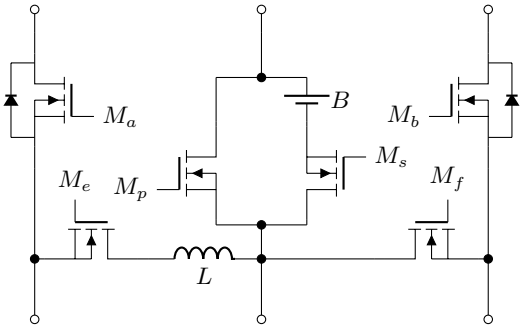
III. Active Cell Balancing Architectures

In this section, the characteristics of two state-of-the-art active cell balancing architectures (see Figure 2) from [6] and [7] will be analyzed. From this analysis, we develop an energy dissipation model in Section IV-A and determine the required installation volume in Section IV-B, which will both be used as optimization objectives in Section VI.

Both architectures rely on inductor-based charge transfer between the series-connected cells of a battery pack. Inductor-based active cell balancing architectures dominate other approaches in terms of energy efficiency and installation space. The architecture presented in [6], in the remainder of this paper referred to as *circuitA*, enables concurrent charge transfers among the cells in a battery pack, but only between adjacent cells. By contrast, the circuit proposed in [7], in the remainder of this paper referred to as *circuitB*, enables concurrent charge transfers also between non-adjacent cells, hence increasing balancing speed and energy efficiency by reducing the number of required balancing steps. In the following, the operating principles of the two architectures will be discussed.



(a) *circuitA*



(b) *circuitB*

Fig. 2: The basic building block of the inductor-based active charge transfer circuit for balancing between adjacent cells (a) and between non-adjacent cells (b).

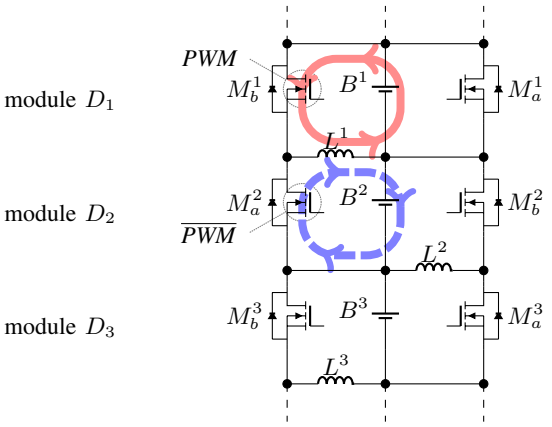


Fig. 3: Example of a charge transfer from module D_1 to D_2 via the inductor L_1.

A. circuitA

The modular non-dissipative current diverter architecture, as proposed in [6], is shown in Figure 2a. It consists of two switches and one inductor per module. The switches are realized by power MOSFETs which are actuated by a Pulse Width Modulation (PWM) signal that is provided by a control circuit. The PWM signal, as illustrated in Figure 4 and further detailed in Section IV-A, consists of times T_{ON} and T_{OFF} during which the charge is transferred from one cell to another.

Please refer to Figure 3 for the following explanation of the charge transfer process from cell B^1 to cell B^2. During T_{ON}, signal *PWM* is high (logical 1) and closes MOSFET M_b^1. Hence, charge from cell B^1 in module D_1 is stored in inductor L^1 with a certain peak balancing current I_{peak}. Similarly, during T_{OFF}, *PWM* is low (logical 0), opening MOSFET M_b^1 and the complementary signal $\overline{PWM}$ is high, closing MOSFET M_a^2. Hence, the stored energy in inductor L_1 is discharged to cell B^2 in module D_2. Note that the balancing current

TABLE I: Properties of inductors and MOSFETs.

Inductor Property	Symbol	MOSFET Property	Symbol
Inductance	L	Output Capacitance	C_{OSS}
Maximum Current	I_{max}	Maximum Current	I_{max}
DC Resistance	R_{ind}	*ON* Resistance	R_{ds}
Volume	$\mathcal{V}_{ind}$	Volume	$\mathcal{V}_M$
		ON delay time	t_{ON}
		OFF delay time	t_{OFF}

I_{peak} is limited by the maximum current I_{max} that the inductor can withstand until it gets saturated. In order to transfer as much charge as possible per PWM pulse, T_{ON} of the PWM signal has to be chosen equal to the time required to fully charge the inductor up to I_{peak}. For a given inductance L, T_{ON} is calculated by:

$$T_{ON} = \frac{L \cdot I_{peak}}{V_1 - V_M} \tag{1}$$

V_1 and V_M are the voltage of the cell in module D_1 by which the inductor is charged and the voltage drop across the MOSFET, respectively.

Similarly, T_{OFF} is the time required to discharge the stored energy in the inductor and is given by:

$$T_{OFF} = \frac{L \cdot I_{peak}}{V_2 + V_M} \tag{2}$$

V_2 is the voltage of cell in module D_2 to which inductor L[1] discharges.

B. circuitB

The architecture *circuitB*, shown in Figure 2b, works based on the same principle of inductor-based active charge transfer as *circuitA*, but with an additional benefit of enabling charge transfers between non-adjacent cells. This feature of the architecture is enabled by the two MOSFETs M_s and M_p, which allow to bypass cells that are on the charge transfer path between two non-adjacent cells. These MOSFETs are high-power devices, because they conduct the entire battery pack current during operation. The architecture also comprises two horizontal switches M_e and M_f, in order to prevent the flow of current in undesired directions, while performing non-adjacent charge transfer. Detailed switching rules for the MOSFETs to transfer charge between any two cells in the battery pack are explained in [7].

The properties of the inductors and MOSFETs that determine the parameters of the inductor-based active cell balancing architectures are listed in Table I. Those properties, that have not been explained in this section, will be discussed in the following Sections IV-A and IV-B.

IV. Design Metrics

In this section, we will introduce three design metrics for active cell balancing architectures:

- The energy dissipation of the charge transfer process that depends on specific circuit parameters (Section IV-A).
- The installation volume of a module of the charge transfer architecture circuit (Section IV-B).
- The balancing current that not only determines the speed of the charge transfer process but also affects the energy dissipation (Section IV-C).

A. Energy dissipation

In the following, the two factors contributing to the energy dissipation of the balancing architectures during operation will be analyzed. The two factors are:

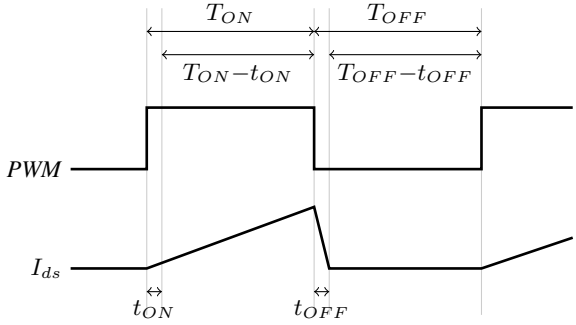


Fig. 4: Illustration of the *ON* and *OFF* phases of a PWM pulse with the respective delays for t_{ON} and t_{OFF} of the drain-source current I_{ds} of a MOSFET switched by the PWM signal.

- Switching energy dissipation, i.e., the energy dissipated per switching that occurs in the MOSFETs controlled by the PWM signal.
- Conduction energy dissipation, i.e., the energy dissipated due to the resistance of the circuit elements on the current path during the charge transfer.

For both factors, we will first characterize the energy dissipation for a single PWM pulse that is illustrated in Figure 4 that consists of an *ON* time T_{ON} and an *OFF* time T_{OFF}. Subsequently, we will present how to calculate the overall energy dissipation for a complete balancing process from the sum of respective energy dissipations per PWM pulse.

Note that, in the remainder of this paper, we will refer to pairs of cells (σ, δ), where σ is the source and δ is the destination of a charge transfer.

Switching energy dissipation for a single PWM pulse. The switching of a MOSFET dissipates energy due to charging and discharging of input and output capacitances of the transistor during its turn-*ON* and turn-*OFF* activity. For each MOSFET, when a PWM pulse is applied, there is a characteristic delay time t_{ON}, during which the internal resistance of the transistor decreases to reach its specific *ON* resistance. This t_{ON} delay is caused by the time taken to fully charge the input capacitance of the MOSFET. Similarly, during the *OFF* period, the transistor does not switch to *OFF* instantaneously, because of the delay t_{OFF} that is caused by discharging its input capacitance.

However, as shown in Figure 4, due to the specific behavior of charging and discharging an inductor in the balancing module, the actual current I_{ds} of the transistor only slowly ramps up to reach I_{peak} at the end of the T_{ON} phase. Hence, for the switching MOSFET in the module that charges the inductor, during t_{ON}, I_{ds} is negligible, while during t_{OFF}, I_{ds} equals I_{peak} and has to be taken into account.

For the switching MOSFET in the module receiving the charge from the inductor, the complementary behavior can be observed. During its t_{ON} time, I_{ds} equals I_{peak}, while during its t_{OFF} time, I_{ds} is negligible. Furthermore, the energy dissipation due to discharging of the output capacitance C_{OSS}, an inherent characteristic of MOSFETs, also has to be taken into account.

Consequently, the overall switching energy $E_{swPWM}^{(\sigma,\delta)}$ dissipated for a single PWM pulse transferring charge between a pair of cells is determined by the charging and discharging of the input capacitance during t_{ON} and t_{OFF}, as well as the discharging of the output capacitance C_{OSS}:

$$\begin{aligned} E_{swPWM}^{(\sigma,\delta)} =& \frac{1}{2} \cdot I_{ds} \cdot (V_{ds,\sigma} \cdot t_{OFF} + V_{ds,\delta} \cdot t_{ON}) \\ &+ \frac{1}{2} \cdot C_{OSS} \cdot (V_{ds,\sigma}^2 + V_{ds,\delta}^2) \end{aligned} \tag{3}$$

Here, I_{ds} is the current flowing through the MOSFET, which, in this case, equals the balancing current I_{peak}. $V_{ds,\sigma}$ is the voltage of the source cell of the charge transfer which equals the voltage across the drain and source terminals of the switching MOSFET. $V_{ds,\delta}$ is the voltage of the destination cell in the module to which the inductor is discharged.

Note that for both balancing architectures, the energy dissipation due to the switching activity is calculated with the same Equation (3), since there is only one active MOSFET switch per module that will be driven by the PWM signal.

Conduction energy dissipation for a single PWM pulse. For any current flowing through a circuit element that has a non-zero resistance, there is a conduction energy dissipation. Therefore, the energy dissipated during the actual charge transfer has to be determined. For this purpose, we have to consider the resistances of the circuit elements through which the current passes in order to calculate the conduction energy dissipation $E^{(\sigma,\delta)}_{condPWM}$ for each PWM pulse of a charge transfer between a pair of cells (σ, δ):

$$E^{(\sigma,\delta)}_{condPWM} = I^2_{bal} \cdot (R_\sigma \cdot (T_{ON} - t_{ON}) + R_\delta \cdot (T_{OFF} - t_{OFF})) \quad (4)$$

Here, we have to distinguish between R_σ as the sum of resistances in the charge transfer path during the *ON* phase of the PWM signal and R_δ as the sum of resistances in the charge transfer path during the *OFF* phase of the PWM signal. I_{bal} is the average current during the charge transfer which equals to $\frac{1}{2} \cdot I_{peak}$ due to the linear behavior of the inductor current flow controlled by the PWM signal. From the T_{ON} and T_{OFF} of the PWM signal, we have to subtract t_{ON} and t_{OFF}, for which the energy dissipation has already been taken into account in $E^{(\sigma,\delta)}_{swPWM}$.

The determination of R_σ and R_δ differs between the two balancing architectures as discussed in the following.

1) Determination of R_σ: For architecture *circuitA*, R_σ is the sum of the *ON* resistance of the switching MOSFET and the resistance of the inductor:

$$R^A_\sigma = R_{M_a} + R_{ind} \quad (5)$$

For architecture *circuitB*, three MOSFETs and one inductor are in the current loop and the value of R_σ is calculated as follows:

$$R^B_\sigma = R_{M_a} + R_{M_e} + R_{ind} + R_{M_s} \quad (6)$$

2) Determination of R_δ: R_δ is the same as R_σ for *circuitA*, because it can only perform charge transfer to a neighboring cell and therefore involves the same inductor and one switching MOSFET of the neighboring module. For *circuitB*, the value of R_δ depends on the distance between the cells of the pair performing a charge transfer and is calculated as follows:

$$R^B_\delta = n_{ind} \cdot R_{ind} + n_{hp} \cdot R_{hp} + n_{lp} \cdot R_{lp} + n_{sw} \cdot R_{sw} \quad (7)$$

Here, n_{ind}, n_{hp}, n_{lp}, n_{sw} are the amount and R_{ind}, R_{hp}, R_{lp}, R_{sw} are the resistances of inductors, high-power MOSFETs (M_s, M_p), low-power horizontal MOSFETs (M_e, M_f) and the switching MOSFETs (M_a, M_b) involved in the charge transfer path, respectively. The values of n_{ind}, n_{hp}, n_{lp}, and n_{sw} are calculated depending on the number of isolated cells, in the following referred to as distance d, present between two cells that are performing the charge transfer as follows.

- $n_{sw} = d + 1$.
- $n_{hp} = d + 1$.
- If the cell that receives charge is the first cell in the series-connected battery string, then the value of $n_{lp} = 1$, otherwise $n_{lp} = 2$.
- If d is an even number, then $n_{ind} = 1$, otherwise $n_{ind} = 2$.

Energy dissipation for a time step $\mathbf{T_M}$. Equation (3) defined the switching energy dissipation and Equation (4) defined the conduction energy dissipation for a pair of cells σ, δ for a single PWM pulse of duration

$$T_{PWM} = T_{ON} + T_{OFF}. \quad (8)$$

For a number n_{PWM} of PWM pulses forming a time step

$$T_M = n_{PWM} \cdot T_{PWM}, \quad (9)$$

the energy dissipation at each PWM pulse during T_M has to be taken into account. Hence, the total energy dissipation $E^{(\sigma,\delta)}_{pair}$ for a time step T_M can be summed up as follows:

$$E^{(\sigma,\delta)}_{pair} = \sum_{i=1}^{n_{PWM}} \left(E^{(\sigma,\delta)}_{swPWM} + E^{(\sigma,\delta)}_{condPWM} \right) \quad (10)$$

We will use Equation (10) in the design evaluation presented in Section V.

B. Volume

The installation volume $\mathcal{V}$ of each module of the cell balancing architectures is determined by the sum of the volume of individual circuit elements forming the module. For the architecture in *circuitA*, there are two switching MOSFETs and one inductor in the module and therefore the installation volume is given by:

$$\mathcal{V}^A = \mathcal{V}_{ind} + 2 \cdot \mathcal{V}_{swM} \quad (11)$$

$\mathcal{V}_{ind}$, $\mathcal{V}_{swM}$ are the volume of the inductor and the switching MOSFET, respectively.

Architecture *circuitB* consists of six MOSFETs and one inductor and the volume is given by:

$$\mathcal{V}^B = \mathcal{V}_{ind} + 2 \cdot \mathcal{V}_{swM} + 2 \cdot \mathcal{V}_{lpM} + 2 \cdot \mathcal{V}_{hpM} \quad (12)$$

$\mathcal{V}_{ind}$ is the volume of the inductor, $\mathcal{V}_{swM}$ is the volume of the switching MOSFETs (M^1_a, M^1_b), $\mathcal{V}_{lpM}$ is the volume of the low-power horizontal MOSFETs (M^1_e, M^1_f), and $\mathcal{V}_{hpM}$ is the volume of the high power isolation MOSFETs (M^1_s, M^1_p), respectively.

C. Balancing Current

The balancing current is another relevant design metric for active cell balancing architectures. A higher peak current capability I_{max} of an inductor leads to a higher average balancing current, as discussed in Section IV-A. This can be deducted from the relation between the average current I_{bal} which equals $\frac{1}{2} \cdot I_{peak}$. As the balancing time is proportional to I_{bal}, a high I_{peak} is desirable from the perspective of balancing speed. However, as seen from Equation (4), the conduction energy is quadratically related to the balancing current, while the balancing time will only decrease linearly.

V. Design Evaluation

To enable an optimization of active cell balancing architectures, it becomes necessary to evaluate a certain circuit design with the presented metrics. For a circuit configuration with specific MOSFET and inductor types, the metrics have to be used to determine the optimization objectives.

In contrast to the selection of the peak current and the determination of the volume, the evaluation of the total energy dissipation for a single circuit design is a challenging task. Here, the specific circuit architecture, balancing algorithm, and energy dissipation metric have to be considered concurrently, which will require an iterative simulation. Performing a complete battery balancing process, Algorithm 1 determines the energy dissipation for a given initial charge distribution within an iterative simulation.

The algorithm considers a given configuration of the cell balancing architecture in terms of MOSFETs, inductors, and peak current I_{peak}. The algorithm simulates the balancing process, starting with a total energy dissipation of 0 (line 1). If the actual peak balancing current I_{peak} cannot be satisfied by an m-ratio of the maximum current limit

Algorithm 1 Computation of the total energy dissipation for a complete battery balancing process for a given circuit design.

Require:
Configuration of MOSFETs and inductors
I_{peak}
Ensure: E_{total}
1: $E_{total} = 0$
2: **if** $m \cdot I_{max} > I_{peak}$ **then**
3: **while** $Var(Q)/avg(Q) > 0.01$ **do**
4: $\mathcal{P}$ = determinePairs(Q)
5: **for** (σ, δ) in $\mathcal{P}$ **do**
6: $E_{total} = E_{total} + E_{pair}^{(\sigma,\delta)}$
7: **end for**
8: Adjust Q according to transfers
9: **end while**
10: **else**
11: Configuration is *infeasible*
12: **end if**

I_{max} of the inductor or MOSFETs, respectively, the current design point can be rejected as infeasible (line 2 and 11). Note that often m is defined at about 70% as a safety-margin. For feasible configurations, the algorithm carries out the balancing process iteratively until the normalized variance of battery cell charge values Q falls under a given threshold (line 3). In each time step, the pairs for (concurrent) charge transfer are determined, depending on the charge values of the cells (line 4). This is done by an algorithm that has to comply with the constraints of the current circuit design, e.g., for *circuitA*, a transfer between non-adjacent cells is not possible. Algorithms that determine the pairs for a transfer are discussed in [7] and will be used in our experimental results. Finally, the value of the total energy dissipation is incremented by the energy that is dissipated during the charge transfer between each pair in one time step (lines 5-7). Note that the voltages can be deduced from the charge values and vice versa. Moreover, the charge of the cells has to be adjusted continuously (line 8) since it has a direct influence on the dissipated energy during a transfer. This calculation of charge values and voltages can be a time-consuming operation as it requires the proper calculation of charge flow and resulting voltage drop which will be necessary in each iteration.

As explained, the determination of the objective of a single circuit design can be very time-consuming, making it necessary to reduce the search space. For this purpose, we constrain the configuration of MOSFETs, taking into account that the modules in *circuitA* and *circuitB* are symmetric, see Figure 2. Thus, we propose to use the same MOSFET for pairs (M_a, M_b), (M_e, M_f), and (M_p, M_s) for each specific circuit. The rationale behind this approach is that these pairs of MOSFETs have the same functionality and, therefore, an optimal solution will not have different devices for a single pair. This enables us to exhaustively explore the search space within a reasonable amount of time as shown in the experimental results.

VI. Experimental Results

For obtaining experimental results, we applied our optimization methodology to *circuitA* and *circuitB*. All our experiments were carried out on an Intel Xeon E5-1620 at 3.60GHz clock frequency and 32GB of RAM. We considered a battery pack of 100 cells that need to be balanced, starting from a randomized voltage per cell following the natural distribution $\mathcal{N}(3.6, 0.05^2)$. We consider three objectives for the circuit optimization: (1) the energy dissipation, (2) the volume, and (3) the peak current.

The search space is defined by the different component types that are chosen. We considered

- 29 inductors for L,
- 11 high-power MOSFETs for M_p and M_s,
- 10 low-power MOSFETs for M_e and M_f, and
- 11 switching MOSFETs for M_a and M_b.

Additionally, we consider I_{peak} currents from 1A to 6A (in a step size of 1A). This results in 732 feasible configurations for *circuitA* and 80114 feasible configurations for *circuitB* after the infeasible solutions are removed where the inductors or MOSFETs, respectively, do not comply with the I_{peak} current. Since a single simulation run of Algorithm 1 for the determination of the energy dissipation can take up to half an hour due to the iterative calculations of the charge flow and voltage drop, it is particularly important to reduce the entire optimization runtime. As a remedy, we propose to do a profiling of the charge transfer pairs $\mathcal{P}$ as well as the resulting charge values Q for each combination of currents and inductors for a given circuit. We propose to assume an average of *ON* resistances of the considered MOSFETs such that the resulting T_{ON} and T_{OFF} values that are determined by Equation (1) and (2), respectively, have only a negligibly small error. Using the resulting profiles for $\mathcal{P}$, Q, T_{ON}, and T_{OFF}, it becomes possible to determine the energy dissipation for each combination of MOSFETs very efficiently. This can be observed in the resulting runtimes where more than 80% of the time is spent on the profiling for the considered circuits. Note that the calculation time for volume is negligibly small while the current as third objective is predefined in steps.

From [7], we used one balancing algorithm for *circuitA* and two different algorithms for *circuitB* (Fast/Slow). For *circuitB*, (Fast) prefers charge transfer between neighboring cells and (Slow) prefers charge transfer between distant cells. The overall runtimes for obtaining the Pareto-optimal solutions were 68h for *circuitA*, 77h for *circuitB* (Fast) and 72h for *circuitB* (Slow). Given the large search space, these runtimes are considered as acceptable, while they can be easily reduced significantly by evaluating many circuit designs in parallel on multiple machines. Although the number of feasible configurations differs a lot between *circuitA* and *circuitB*, the final runtimes do not differ that significantly. This is due to the fact that most time is spent on the profiling, which requires the same amount of runs for both circuits since the same number of inductors and the same peak currents are considered.

The Pareto-fronts for all three circuit variants with a projection of the energy dissipation versus volume is given in Figure 5. Three sample circuit designs from the Pareto-fronts are presented in Table II while the details for the inductors and MOSFETs are given in Table III and Table IV, respectively. These results illustrate the diversity of the design space and the necessity to optimize and choose the right balancing circuit and algorithm concurrently.

TABLE II: Sample circuit designs from the Pareto-front with the types of components and their results of the cell balancing algorithm for *circuitA*, *circuitB* (Fast), and *circuitB* (Slow), respectively.

Circuit architecture **Circuit design**	*circuitA* (P_1)	*circuitB* (Fast) (P_2)	*circuitB* (Slow) (P_3)
Inductor	Murata(8.2)	Coilcraft(9.5)	BOURNS(2.6)
High-power MOSFET	N/A	Infineon(300)	Infineon(180)
Low-power MOSFET	N/A	Infineon(9.3)	IRF(10)
Switching MOSFET	Onsemi(7.8)	Diodes(9.8)	Diodes(9.8)
$\mathbf{E_{total}}$ [Wh]	10.41	5.71	1.91
$\mathcal{V}$ [mm^3]	899.44	814.05	783.77
$\mathbf{I_{peak}}$ [A]	5	6	1
Balancing time [h]	12.5	0.8	23.12

VII. Conclusion

This paper presented an optimization approach for dimensioning of active cell balancing architectures. From the analysis of the characteristics of two state-of-the-art architectures, design metrics were developed for energy dissipation, installation volume, and balancing

TABLE III: Specifications for the inductors from Table II.

Inductor	$\mathbf{L}$ [μH]	$\mathbf{I_{max}}$ [A]	$\mathbf{R_{ind}}$ [mΩ]	$\mathcal{V}_{\mathbf{ind}}$ [mm^3]
Murata(8.2)	2.2	10	8.2	893.04
CoilCraft(9.5)	1.2	9.5	20.5	57.86
Bourns(2.6)	22	2.6	67.5	625

TABLE IV: Specifications for the MOSFETs from Table II.

MOSFET	$\mathbf{I_{max}}$ [A]	$\mathbf{R_{ds}}$ [mΩ]	$\mathcal{V}_{\mathbf{M}}$ [mm^3]	$\mathbf{t_{ON}}$ [ns]	$\mathbf{t_{OFF}}$ [ns]	$\mathbf{C_{OSS}}$ [pF]
Infineon(300)	300	0.4	271	47	186	7200
Infineon(180)	180	0.8	22	59.8	107.4	3800
Infineon(9.3)	9.3	15	54.25	11.1	12.9	450
IRF(10)	10	15.5	4.41	20.8	32.8	260
Onsemi(7.8)	7.8	35	3.2	14	24	116
Diodes(9.8)	9.8	16	52.84	15.4	41.1	158

current. In order to enable evaluation of possible designs with respect to these metrics, an algorithm was presented that combines the energy dissipation metric with a simulation of a battery balancing algorithm. Finally, we presented a case study were Pareto-optimal design points were computed for a wide range of inductors and MOSFETs at different balancing currents. The obtained results clearly show the possible improvement in energy efficiency and installation volume by choosing appropriate design points from the obtained Pareto-front.

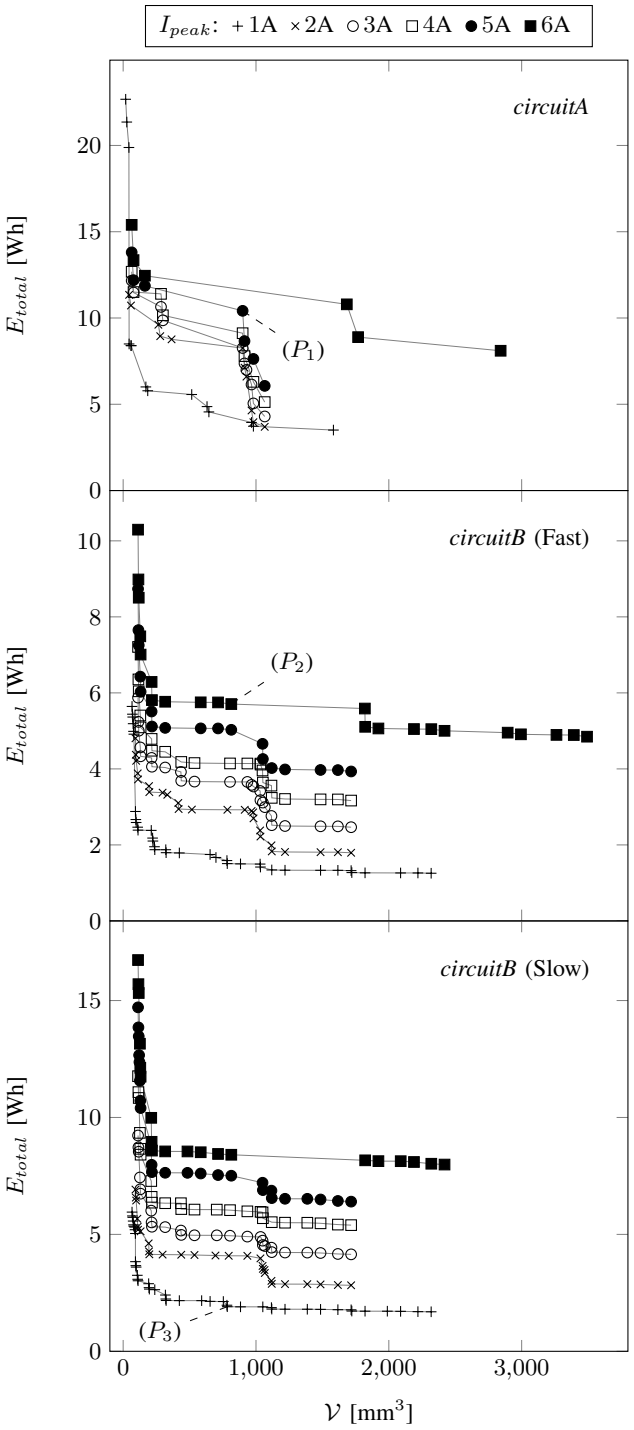


Fig. 5: Pareto-optimal results for *circuitA* and *circuitB* (Fast/Slow). The objectives are the energy dissipation (E_{total}), volume $\mathcal{V}$, and peak current I_{peak}.

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