A study of dielectric breakdown of a half-bridge switching cell with substrate integrated 650 V GaN dies

This paper proposes an ultra-low inductance halfbridge switching cell with substrate integrated 650V GaN bare dies. A vertical parallel-plate waveguide structure with 100µm layer thickness results in a commutation loop inductance of 0.5 nH resulting in a negligible drain-source voltage overshoot in the inductive load standard pulse test. On the other hand reliable circuit operation requires an assessment of the isolation strength of the thin dielectric layer in the main commutation loop, because critical high local electric fields might occur between the pads. Measurements of the dielectric breakdown voltage followed by a statistical failure analysis provide a characteristic life of 14.7 kV and a 10% quantile of 13.5 kV in the Weibull fitted data. This characteristic life depends strongly on the ambient temperature and drops to 4.1 kV at 125°C. Additionally, ageing tests show an increasing in dielectric breakdown voltage after 500 h, 1000 h and 2000 h at 125°C high-temperature storage due to resin densification processes.