Abstract:

The introduction of multicore architectures in embedded systems allows system integrators to locate multiple applications on the same chip. In the context of certification separation of these applications is mandatory. Most current multicore systems have a low core count and programmers have a need for easily utilizable platforms. Therefore, most of the current multicore systems use shared memory architectures based on bus communication. In this paper we discuss several possible architectures for shared memory protection using local and shared MPUs and MMUs for architectures of this type. This analysis includes typical use cases for multicore systems and their compatibility to these architectures. It has a strong focus on the platform’s suitability for mixed-critical workloads with some cores executing safety-critical, hard-real-time applications. This paper proposes a novel shared memory protection unit to efficiently enforce spatial separation of the shared memory among the cores. Preliminary synthesis results are provided along with latency considerations relevant for hard-real-time application.