Application of Nanomagnetic Logic: Co/Pt based Systolic Pattern Matcher

Abstract:
Nanomagnet Logic (NML) is widely considered to be one of the promising for “beyond-CMOS” nanoscale architectures. So far only relatively simple circuits (nanomagnetic logic gates and adders) have been studied experimentally and in simulations. Here we investigate the possibility of building larger-scale computing devices from out-of-plane NML. We designed a systolic pattern matcher circuit that is in principle scalable to arbitrary number of nanomagnets and can match arbitrarily long patterns in an incoming data stream. The design of this systolic architecture for NML makes an important step toward large-scale devices.

Kongress- / Buchtitel:
IEEE Transactions on Nanotechnology, 12, 399-407(2012)

Kongress / Zusatzinformationen:
Madison WI USA, May 22 - 25, 2012

Verlag / Institution:
IEEE Xplore Digital Library

Jahr:
2012

Quartal:
2. Quartal