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Graphenic Carbon: A Novel Material to Improve the Reliability of Metal-Silicon Contacts

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ABSTRACT Contact resistance and thermal degradation of metal-silicon contacts are major challenges in nanoscale CMOS as well as in power device applications. Titanium silicide (TiSi) is commonly used to establish low-barrier height contacts to silicon, in state-of-the-art FinFETs or Schottky diodes. But the metal is known to diffuse into the active region under high current stress, as during an electro-static discharge event. This work shows with a Schottky diode as test vehicle that a carbon–silicon (C–Si) contact has the same low Schottky barrier height as a TiSi–Si junction but is over 100 million times more stable against high current pulses. A Schottky barrier height between 0.36 eV and 0.45 eV can be obtained by a variation of the deposition process. This makes C–Si a promising candidate for future high current density and temperature stable contacts and even for applications that require low contact resistances.

INDEX TERMS Carbon, contact resistance, ESD, FEM, graphene, metal-semiconductor, reliability, Schottky barrier, Schottky diode, silicide, TiSi.

I. INTRODUCTION

Metal to semiconductor contacts are essential elements in integrated and discrete electronic devices. The source and drain contacts to state-of-the-art FinFETs rely on titanium silicide (TiSi) formation [1] and, as predicted by Adusumilli *et al.* [2], future downscaled 3D technologies will be based on titanium (Ti) silicided contacts to preserve functional yield. Recent efforts to reduce the contact resistance to NMOS and PMOS devices also make heavy use of TiSi [3]–[5] as it provides a very low Schottky barrier height (SBH) on silicon, making it also very suitable for Schottky diodes used in zero-barrier mixer applications [6].

Joule heating and electric fields of sufficient magnitude can force metal ions to migrate and diffuse into the underlying semiconductor [7], [8]. This is especially during an electrostatic discharge (ESD) event, when a high current flows through the device causing a degradation of the inherent electrical properties or even leading to a junction burnout and consequently a failure of the device [9], [10].

The power P per volume V (power density) in a conductor during a current pulse of an ESD event leads to joule heating and is given by

$$\frac{P}{V} = j \cdot E = j^2 \cdot \rho, \tag{1}$$

where j is the current density, E is the local electric field and ρ is the electrical resistivity. It is obvious that the magnitude of the applied current density has the strongest influence on the induced damage to the device and hence on its reliability. The pulse can force the diffusion of ions in the substrate or the interface material can undergo a thermal instability changing the electrical properties [7]–[12].

Carbon (C) in its various forms is establishing itself as novel material in the semiconductor research. Previously, graphenic carbon (GC) [13] films have already been used as electrodes in DRAM capacitors [14], as switching material for non-volatile memories [15] and as highly stable membranes [16]. Recent investigations on next-generation interconnects demonstrate that copper (Cu) wires encapsulated by graphene [17] and doped individual multilayer graphene-nanoribbon [18] are very promising in their electrical and reliability properties to improve or replace conventional Cu interconnects. Recently, we demonstrated that carbon-silicon

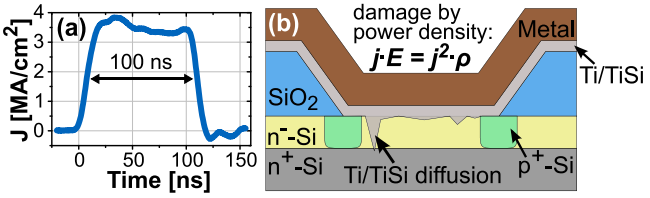

FIGURE 1. **(a) Illustrates a measured waveform of a 100ns current pulse with a rise/fall time of <15 ns and an average current density $j = 3.5$ MA/cm² which was measured with a Tektronix CT-1 current sensor. (b) schematic cross-section of a TiSi-Si Schottky diode where Ti or rather TiSi diffuses into the n⁻-Si epitaxial layer and could even reach the highly doped substrate by the application of a high current pulse.**

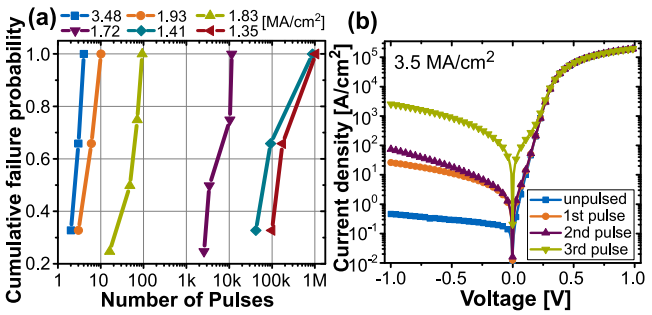

FIGURE 2. **(a) Illustrates the failure probability versus number of current pulses at different current densities for commercial BAT15 diodes with TiSi-Si interface. At least three devices were stressed for a given pulse current density, a pulse width of 100 ns and a duty cycle <0.0001. The failure of the diode was defined when the diode degrades to a reverse current >100 μA @ $V_r = 1$ V. The *J-V* curves in (b) show the degradation of a TiSi diode pulsed with a current density of 3.5 MA/cm² and a width of 100 ns. Every single pulse led to a deterioration of the reverse behavior of the diode and after a third pulse a normal operation is not possible anymore.**

(C-Si) contacts have almost the same electrical properties compared to the well-established TiSi-Si contacts but show a much improved reliability and temperature stability [19]. In this paper, we will discuss these results in much more detail as we review the carbon deposition process and additional results from the simulations. In addition, we show that the barrier height of the C-Si contact can be lowered even more by a variation of the carbon deposition process.

II. SCHOTTKY DIODE TEST VEHICLE

Schottky diodes for high frequency applications are a well-known platform for reliability tests of interface materials. Any changes at the metal-semiconductor junction, forced by an electrical stress or just by temperature, can easily be detected by evaluating the electrical characteristics of the diode [20]–[23]. The reliability of the devices is often tested with a high voltage or current pulse, like shown in Fig. 1(a). The pulse has a width of 100 ns [24] which is similar to the ANSI/ESDA/JEDEC JS-001-2012 Human Body Model [25] and the IEC61000-4-2 test standard [26]. A damaged or deteriorated diode can be identified by monitoring the characteristics of the Schottky diode at a fixed reverse bias. A degradation of the properties shows up as an increased reverse current leakage.

In our experiments we used a vertical Schottky diode structure with an active area of 45.36 μm² to evaluate the impact of a high current pulse on the reliability of the metal-semiconductor interface. The used test vehicle is a BAT15 Schottky diode from Infineon [27], a low SBH diode for mixer and detector applications. In its commercial available version it uses TiSi as the interface material to silicon (TiSi-Si) and consists of a thin n⁻-epitaxial layer with a thickness of 150 nm. This thin layer is very susceptible to degradations in its electrical reverse bias characteristics when contaminations like metal ions enter this epitaxial region. Pulses with high power density can force the diffusion of Ti/TiSi into the epitaxial layer which can short-circuit the diode, like sketched in Fig. 1(b).

III. TISI-SI DIODES RELIABILITY

Commercially available BAT15 Schottky diodes with TiSi-Si junction were pulsed with different current densities j at room temperature and the reliability results are plotted in Fig. 2(a) as a function of the pulse number. The current pulse used has a duty cycle less than 0.0001 and a waveform as shown in Fig. 1(a). This low duty cycle guarantees that the diode can cool down to room temperature after every individual current pulse. The condition of the diode was monitored at a reverse voltage of $V_r = 1$ V and the diode is declared as failed if the reverse current reaches a value of 100 μA (220 A/cm²) as the on/off ratio of the diode is then deteriorated by a factor of more than 500. It is evident from Fig. 2(a) that the maximum number of transient stress pulses depends on the used current density level. For 1.35 MA/cm², which is slightly above the permissible pulse load of 1.21 MA/cm² specified by the manufacturer, the failure probability is spread over a wide range and a wear out of the diodes is observed between 100 k and 1 M events. The probability of a possible damage to the diode is severely increased when higher current densities are applied because the power density is proportional to j^2 (see in (1)). As a consequence, the TiSi-Si junction can only withstand 2 – 4 pulses of 3.5 MA/cm² at 100 ns pulse width.

Fig. 2(b) highlights that even a single 3.5 MA/cm² event can degrade the original behavior of the diode, indicated by the over 100x increase of the reverse current at $V_r = 1$ V. This proves the inter-diffusion of Ti/TiSi within the silicon epitaxial layer. Further pulses incrementally deteriorated the device even more as a metal or silicide filament might be created and the diode is short-circuited after 3 pulses.

IV. GRAPHENIC CARBON-SILICON DIODES

To allow a direct comparison of the C-Si and TiSi-Si diodes, the manufacturer provided BAT15 silicon vehicles with all the same dimensions, dopants and guard ring structure to establish a "metallic contact" to silicon by graphenic carbon (GC), like shown in Fig. 3. The GC was deposited by a chemical vapor deposition (CVD) process which has been described in [28] and [29]. The deposition of the GC can be performed directly on the surface of the substrate, here

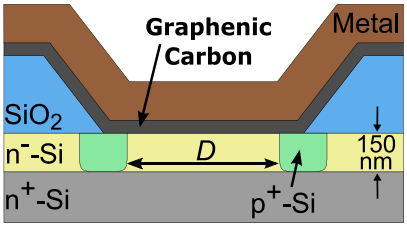

FIGURE 3. **A schematic cross-section of the used Schottky diode with guard ring structure and grapenic carbon as metallic interface material to silicon. The diameter *D* of the active region is 7.6 μm.**

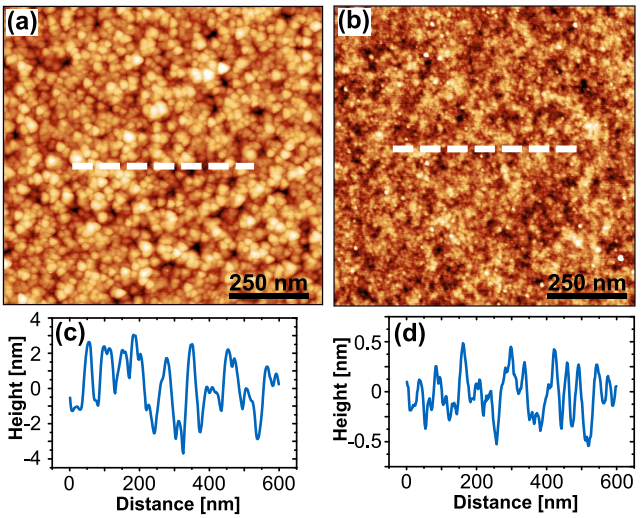

FIGURE 4. **Comparison of the surface roughness and the corresponding height profile of the deposited GC films measured with an AFM. (a,c) show the surface and profile of a GC film grown with a precursor gas flow of 80 sccm. The root-mean-square surface roughness (R_{rms}) is 1.8 nm. The surface and height profile of the GC film which was grown without any flow of the precursor gas is shown in (b,d). The surface is much smoother and has a R_{rms} of just 0.44 nm. A similar roughness can be observed at low gas flow (20 sccm).**

silicon, silicon oxide and silicon nitride, without the need of a catalyst as it would be the case for graphene deposition. GC has a high adhesion to the surface due to formation of strong covalent carbon-silicon bonds [16]. In contrast, transferred graphene [30] has a poor adhesion to the underlying substrate surface and adheres just by van der Waals interaction [31].

The sample substrates were prepared by ultrasonic cleaning in acetone and isopropyl alcohol and completed by a full RCA clean. It is very crucial to have a contamination-free silicon substrate for the reliability tests as every ion or impurity could contribute to a possible degradation of the device. The native oxide on the devices was removed by a dip in a 5 % solution of hydrofluoric acid (HF) to get a clean silicon surface on the BAT15 structure. The HF-dip was done immediately before the deposition of graphenic carbon to receive a pure metal-semiconductor interface afterwards.

Subsequently, the samples were placed in a hot-wall reactor and purged under a hydrogen gas flow (H_2, 99.9999 % purity) of 250 sccm at 0.6 mbar. The samples could be heated up in this hydrogen atmosphere or already in process gas atmosphere. For the latter we used a hydrocarbon precursor gas such as acetylene (C_2H_2, 99.6 % purity) or ethylene (C_2H_4, 99.995 % purity) at a gas flow between 20 sccm and 80 sccm. The gas flow directly influences the deposition rate of the GC (beside temperature, pressure and time) as a low flow increases the residence time of the gas in the reactor which in turn increases the probability for the gas molecules to react on the substrate. The surface roughness is influenced by the gas flow, as illustrated in the atomic force microscope (AFM) measurements in Fig. 4. The images show the relation between precursor gas flow and surface roughness. At low flow rates ($\leq$ 20 sccm) a much smoother surface can be obtained than for higher flow rates like 80 sccm.

The deposition temperature ranged from 850 °C up to 1000 °C while the used precursor gas pressure varied from 10 mbar to 50 mbar. For C_2H_2, we used a deposition temperature of $<$ 900 °C [32] which could lead to a higher content of amorphous hydrogenated carbon [33]. The electrical resistivity of the GC is strongly influenced by the deposition temperature [34], that's why the samples were subsequently annealed for 30 s at 1000 °C to improve the GC resistivity [35]. At higher deposition temperatures ($\leq$ 1000 °C) we used C_2H_4 as precursor gas and didn't perform the additional annealing step. The samples were subsequently cooled down in a H_2 gas flow (250 sccm, 0.6 mbar).

It is very desirable to have a short deposition time as the dopants from the highly doped substrate would otherwise diffuse into the thin low doped epitaxial layer. The diffusion makes this layer even thinner and could change the electrical and reliability properties of the resulting Schottky diode. To prevent this, the deposition time was always kept below 15 min. The final thickness of the grown GC film can be tuned from a few nm up to several μm by changing the process parameters. The thickness was verified with an AFM by measuring the step height at a region where the GC was scratched away.

The layered structure of the graphenic carbon film is nicely seen in the cross-section shown in Fig. 5(a). The cleaved sample reveals the high anisotropy of the carbon growth and that the layers nicely follow the structure of the substrate during the deposition. The existence of a high content of covalent sp^2-bonds from carbon atoms is confirmed by the Raman spectrum in Fig. 5(b): G- and G'-peaks are pronounced and the D-peak is smaller than the G-peak [36]. Consequently, GC has anisotropic material properties leading to an in-plane resistivity $\rho_{\parallel}$ between 1 mΩ·cm and 3 mΩ·cm (determined by four probe method). In the direction perpendicular to the surface it has a resistivity of $\rho_{\perp} = 50$ mΩ·cm. The ratio of up to 50 is quite small compared to highly ordered graphite which has a ratio of almost 750 between the in- and out-of-plane electrical resistivity [37]. The value for the direction perpendicular to the surface was extracted from analyzing samples with varying carbon thickness. The slope of the area-normalized

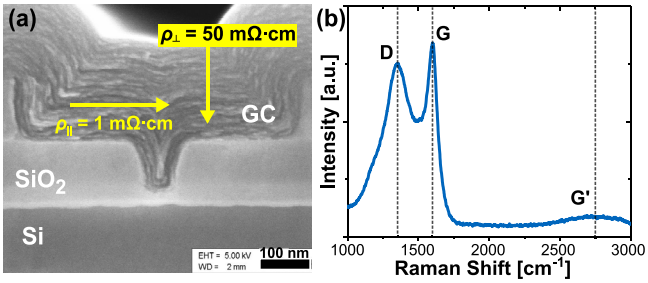

FIGURE 5. The laminar growth of graphenic carbon, which nicely follows the shape of the substrate, is revealed in the cross-section SEM in (a) of a cleaved sample. The layered growth leads to anisotropic electrical resistivity. (b) shows a typical Raman spectrum of the GC film where the D-peak (1348 cm^{-1}), G-peak (1601 cm^{-1}) and G'-peak (2710 cm^{-1}) are marked. An excitation laser wavelength of 532 nm was used.

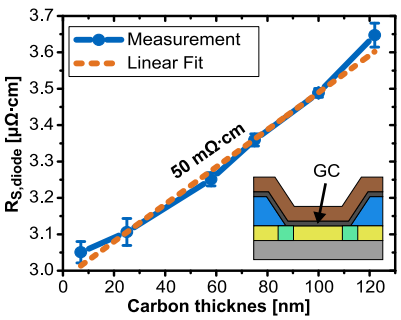

FIGURE 6. The area-normalized series resistance of the C-Si diode $R_{s,diode}$ as a function of the graphenic carbon thickness on the diode with all the same metallization layers on top. The out-of-plane electrical resistivity is extracted to be $\rho_\perp$ = 50 mΩ·cm.

series resistance R_s of C-Si diodes as function of the GC thickness gives the electrical resistivity as plotted in Fig. 6. R_s of the C-Si diode is calculated by fitting the Schottky diode equation for the current density (J) from the thermionic emission theory [38] to the measured current-voltage data in forward direction of the diode. The equation was also used to extract the Schottky barrier height ϕ_B and the ideality factor n:

$$J = \underbrace{A^{**}T^2 \exp\left(-\frac{e\phi_B}{k_B T}\right)}_{=J_0}\left[\exp\left(\frac{e\,(V - JR_s)}{nk_B T}\right) - 1\right]. \qquad (2)$$

J_0 is the saturation current density, A^{**} is the effective Richardson constant, T is the device temperature, e is the elementary charge, k_B is the Boltzmann constant and V is the applied voltage.

The top metallization of the diodes was formed by electron-beam evaporation through a shadow mask onto the GC and consists of a stack of 50 nm of Ti, 1.3 µm of Cu and 40 nm of Au. The thick Cu acts as additional heat sink as well as to prevent current crowding. Finally, the carbon was structured in hydrogen plasma with the metal stack acting as a hard mask where the GC is fully removed at non-covered regions.

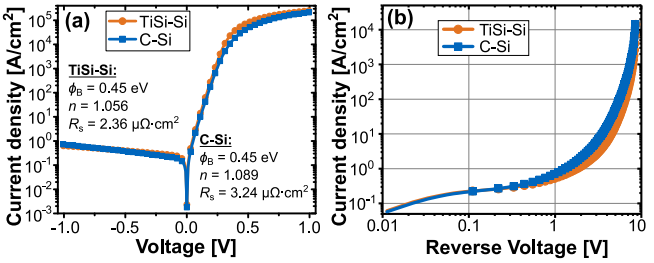

FIGURE 7. (a) Shows a comparison of the dc characteristics of a TiSi-Si (BAT15) and a C-Si diode with a carbon thickness of 58nm. Ideality factor n, SBH ϕ_B and area-normalized series resistance R_s are displayed for the pristine diodes. The SBH is the same for both devices. (b) compares the reverse dc-characteristics of a TiSi-Si and a C-Si diode. The C-Si diode has a lower blocking capability as a reverse leakage current of 220 A/cm^2 (100 µA) is reached at an about 0.6V smaller voltage than for a TiSi diode.

V. CHARACTERISTICS AND RELIABILITY OF C-SI DIODES

The dc-characteristics of the pristine (no current pulse applied) TiSi-Si and C-Si diodes are compared at room temperature in Fig. 7(a). Both diodes have a Schottky barrier height ϕ_B of 0.45 eV and an ideality factors n below 1.1. Only the C-Si diode has a little higher resistance as the 58 nm thick layer of GC adds more series resistance than the TiSi. When the same current pulse is applied to each of the two devices, the diode with the higher resistance should experience even more damage due to the increased joule heating in this case. As shown in Fig. 7(b), the C-Si diode has a slightly higher reverse leakage current than the TiSi diode. At a reverse current of 220 A/cm^2 (100 µA), the C-Si diode has a 0.6 V lower reverse voltage. The exact origin is not yet identified as the two devices have the same SBH. It could be a consequence of the high temperature deposition of the GC as the dopants from substrate might start to diffuse and therefore decrease the thickness of the n$^-$-epitaxial layer.

After the exposure to air for more than one year, the C-Si diode neither showed any deterioration in its electrical characteristics nor a separation of the GC from the substrate. In contrast, exposure to air can degrade the device properties of graphene-silicon Schottky diodes due to the formation of an interfacial layer between graphene and silicon [39].

A graphenic carbon thickness of 28 nm was used to evaluate the impact of 3.5 MA/cm^2 current pulses (100 ns width) on the electrical characteristics. As illustrated in Fig. 8, the C-Si diode can easily endure up to 500 M pulses and is fully functional without showing any reasonable deterioration. In contrast, the TiSi-based diode was short-circuited after 2 – 4 pulses. Interestingly, the C-Si diode has less reverse leakage after 1 M pulses which is even further decreased after 500 M pulses. This might be due to a formation of a thin silicon carbide (SiC) layer at the C-Si interface as the SBH is slightly increased from 0.45 eV to 0.46 eV. A first degradation is observable after 545 M pulses which is attributed to dopant diffusion from the substrate or to the diffusion of the top metallization.

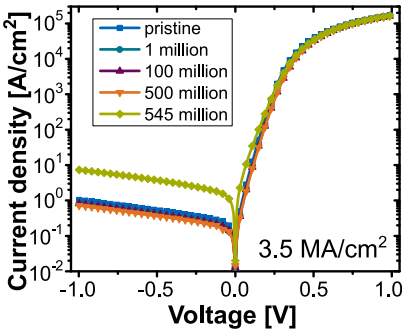

FIGURE 8. The *J-V* curves show the change in the dc-characteristics of a C-Si diode with a 28 nm thick GC after several million current pulses (3.5 MA/cm², 100 ns) were applied. After up to 500 M pulses the electrical behavior is almost not affected. Only a small shift of the SBH of 0.01 eV is observable leading to a lower reverse current. After 545 M pulses the diode starts to degrade as the reverse leakage is increased.

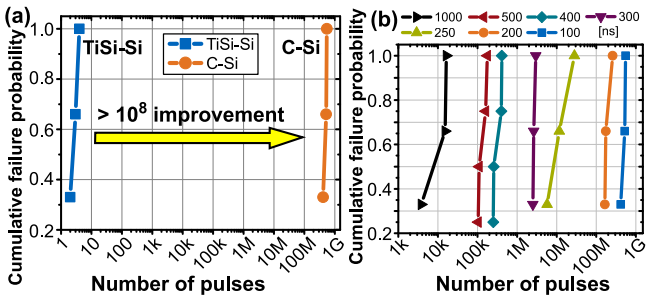

FIGURE 9. (a) Comparison of stress pulse endurance of TiSi-Si (BAT15) and C-Si diodes for a current density of 3.5 MA/cm² and a pulse width of 100 ns. The majority of the diodes are deteriorated below 4 pulses whereas the C-Si diodes can withstand over 100 million more pulses until a wear out is observed. Image (b) shows the failure probability as a function of the number of pulses at different pulse lengths for the C-Si diodes. At least three devices were stressed with a given pulse current density of 3.5 MA/cm² and a duty cycle < 0.0005. The failure of the diode was defined when the diode degrades to a reverse current >100 μA @ V_r = 1V.

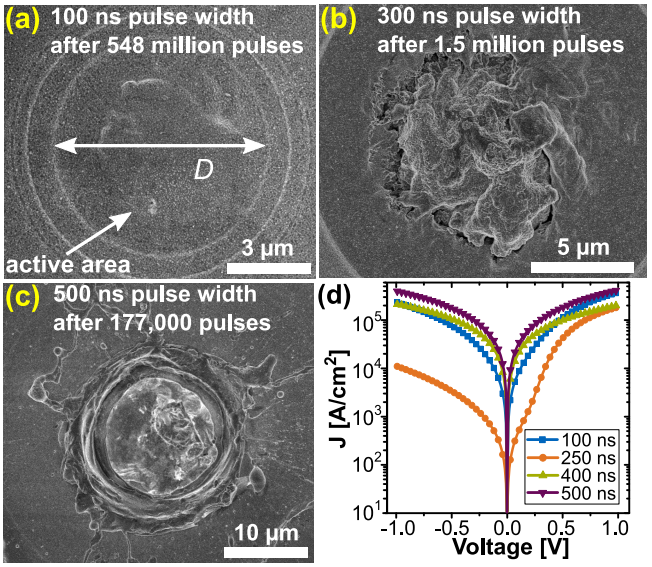

FIGURE 10. SEM image of the top view of C-Si Schottky diodes with Ti/Cu/Au top metallization after the diodes failed. All the devices where stressed with the same current level of 3.5 MA/cm² while only the pulse length was altered. (a) shows a device after 548 million pulses (100ns) where almost no damage in the top metallization is visible. The device in (b) demonstrates the damage of a 300 ns pulse after 1.5 million pulses where the metal even started to melt and piled up. (c) illustrates a sample where the temperature in the copper raised so much during the 500 ns pulses that some kind of volcano was created as molten copper was spit on the periphery and a circular crater was formed. (d) shows *J-V* characteristics of C-Si diodes after they reached the threshold for a failed diode. The diodes show an increased J_0 and consequently a reduced Schottky barrier height ϕ_B.

Fig. 9(a) compares the failure probability of the TiSi-Si (BAT15) and the C-Si diode and shows that the reliability for C-Si diodes range between 420 M and 550 M pulses before a wear out is detected. Under these test conditions, graphenic carbon can enhance the robustness against high current events like ESD by a factor of over 100 million compared to the TiSi diode which underlines the importance of the C-Si contact scheme. The improvement might be attributed to the fact that carbon has a 1,500 times smaller diffusivity in Si than Ti at 950 °C [40], [41]. GC can also act as diffusion barrier for the top metallization as sp^2-bonded carbon is known to be a good diffusion barrier for the Ti and Cu metallization [42], [43].

Fig. 9(b) shows the pulse-count dependent failure probability for increased pulse widths of C-Si diodes tested at the same current pulse density of 3.5 MA/cm². When the pulse width is doubled from 100 ns to 200 ns the total applied energy is also doubled, however the reliability is still extremely high and ranges from 150 M up to 240 M pulses. It is obvious from the graph that a higher pulse width leads to an earlier failure and for a width of 1 μs (10x higher energy) the failure happens between 5 k and 16 k pulses which is still outperforming in terms of reliability compared to the TiSi diode at 100 ns pulse width.

The top metallization of the diode was analyzed by a scanning electron microscope (SEM) to examine how much the surrounding area of the active device region is damaged by pulses with a strength of 3.5 MA/cm² (Fig. 10(a-c)). For a 100 ns pulse, the damage to the top metallization is hardly visible as the event is so short that the heat can hardly spread away from the C-Si interface (Fig. 10(a)). The visible bump may just arise due to the thermo-mechanical stress by the thermal expansion at each pulse cycle. In Fig. 10(b,c), the top metallization is heated to the point that it is even melted and causes a pile-up of the metal. At a pulse width of 500 ns, the metallization starts to create a "volcano" as it spits out molten Cu on the periphery of the diode. Cu has its melting point at 1085 °C [44] and consequently the temperature at the C-Si interface must be much higher. This points out how temperature stable the C-Si contact is because the device could withstand up to 177 k pulses.

Fig. 10(d) reveals that the failed diodes all show the same behavior. They are not open-circuited devices, but they have a strongly increased reverse current with almost linear characteristics, like electrically shorted. This is most probably by a diffusion of the dopants from the substrate towards the

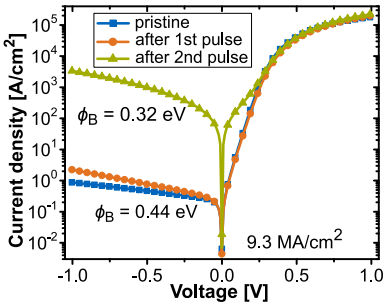

FIGURE 11. ***J-V*** **characteristics of a C-Si diode with a GC thickness of 58nm. After one pulse with a current density of 9.3 MA/cm^2 (100 ns) the diode is fully functional and in its reverse behavior still close to the pristine curve. Only the second pulse is destructive.**

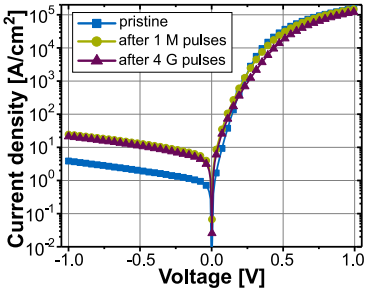

FIGURE 12. **The *J-V* curves show the dc-characteristics of a C-Si diode were the substrate was heated in H_2 atmosphere before the precursor gas was inserted in the reactor. The pristine/unstressed device has a low SBH of 0.41 eV which is decreased to 0.36 eV after the diode was stressed with at least 1 M pulses. The diode is still functional after 4 M pulses without a further deterioration of the reverser leakage but the device gets a degraded series resistance and ideality factor.**

Schottky contact or by a diffusion of the top metallization through the GC.

C-Si diodes with 28 nm and 58 nm thick carbon layers were tested at elevated stress levels with a transmission line pulse (TLP) setup with a 100 ns pulse width and a rise/fall time of about 15 ns. To evaluate the maximum applicable current density, the diode should at least withstand a single pulse event without any strong degradation to still fulfill the acceptable reverse leakage specified for the TiSi-Si BAT15 diode (100 µA @ $V_r = 4$ V).

A maximum applicable current density of 9.3 MA/cm^2 could be identified for the diode with a 58 nm thick carbon film which is an 2.65 times increased current density compared to the endurance tests. This means in consequence that the power density, which is mainly responsible for a possible damage, is increased by a factor of 7 as the current density has a squared dependency (see in (1)). Like shown in Fig. 11, the first pulse is not destructive to the device as the Schottky barrier height, ideality factor and series resistance are barely affected. Only a slightly higher reverse current is observable, but the diode still fulfills the BAT15 specifications. Only the second pulse is destructive to the diode and it completely fails, indicated by the about 500x higher reverse current.

For a C-Si diode with a 28 nm thick GC film a slightly lower maximum applicable current density of 8.0 MA/cm^2 is identified. This implies a power density more than 5 times greater than in the endurance pulse tests shown in Fig. 9. The devices here had the same electrical behavior as the diode shown in Fig. 11 where the first pulse was not destructive, but the second one was. The exact origin of the failure cannot be identified at the moment, although the GC thickness dependency suggests the diffusion of the Ti/Cu top metallization through the GC-layer as a possible cause.

The previously discussed C-Si diodes were all heated up in precursor gas atmosphere. In contrast, when the substrate was heated up in H_2 atmosphere (150 sccm, 0.5 mbar) for 5 min before the precursor gas was inserted in the reactor, we observed C-Si contacts to have SBHs as low as 0.41 eV, like shown in Fig. 12. This diode has a GC thickness of 37 nm, an area-normalized series resistance R_s of 3.85 µΩ·cm^2 and an ideality factor n of 1.18, all slightly higher than for the previous samples. Reliability tests with a current density of 3.5 MA/cm^2 showed that this diode starts to degrade gradually until 1 M pulses were applied. As can be seen in Fig. 12, the SBH was decreased to 0.36 eV, n was increased to 1.75 and R_s is almost unchanged. Interestingly, the C-Si diode, as tested so far, could withstand 4 G pulses without further degradation in the reverse bias characteristics, only R_s was increased by 0.3 µΩ·cm^2 but the diode is still functional. This high pulse number even outperforms our previous results on C-Si diodes [19]. A reason for the improved reliability might be the increased GC thickness of 37 nm which is thicker than the 28 nm from the previously tested device and acts therefore as a better diffusion barrier for the top metallization. In addition, the 37 nm thick GC was deposited at a low precursor gas flow, which led to a reduced surface roughness. This might be another reason for the better reliability as a higher surface roughness can lead to an electrical field enhancement. This in turn could produce localized stress spots with higher power density leading to a higher damage probability.

In order to achieve low specific contact resistances ρ_c the SBH ϕ_B needs to be decreased. This is often achieved by inserting a thin dielectric layer (like TiO_2) between metal and silicon (MIS contact) to de-pin the Fermi level [45]. Unfortunately this approach is not compatible with high temperatures as the contact would increase its resistivity after a mild temperature anneal [46]. The value of the saturation current density J_0 (see in (2)) of a metal-semiconductor (MS) contact is a good indication for the SBH and the obtainable ρ_c as they are inversely proportional ($\rho_c \sim 1/J_0$) [38]. Fig. 13 compares current density plots of C-Si with recent efforts from Yu *et al.* [46] to achieve low ρ_c.

The C-Si diodes with a SBH of 0.45 eV have already a J_0 as high as the MIS contact from Yu *et al.* while the C-Si contact with 0.41 eV and the pulse-annealed contact with 0.36 eV exceed these results. Therefore, GC on Si could be an interesting material combination to create high current and temperature stable contacts.

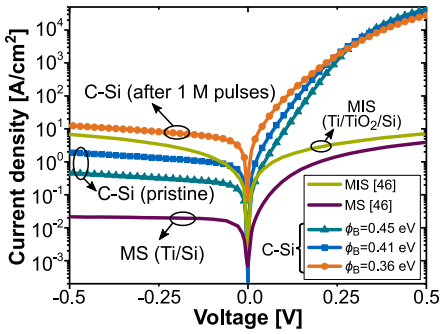

FIGURE 13. Comparison of *J-V* curves of literature values of MS (Ti/Si) and MIS (Ti/TiO_2/Si) with C-Si values on n⁻-Si. The contact resistivity ρ_C is inversely proportional to J_0 which is as high or even higher for pristine C-Si (ϕ_B = 0.41 eV & 0.45 eV) compared to the MS and MIS diode from [46]. The pulse-annealing with 1 M pulses of the C-Si diode with a SBH of 0.41 eV leads to an even lower SBH of 0.36 eV and is consequently much better.

VI. ELECTRO-THERMAL SIMULATIONS

To get a deeper insight to the heat distribution in the diode during the ESD event, coupled time-dependent electro-thermal simulations based on finite element method (FEM) were performed with COMSOL Multiphysics. The geometry of the model is built close to the BAT15 structure with the same dimensions, doping profile and Ti/Cu as top metallization. The Au top layer is neglected here as it is very thin and hence should have no influence on the simulation results. GC or TiSi is used as contact material to Si, whereas GC has a thickness of 30 nm. For simplicity, TiSi is assumed to have a thickness of 0 nm and consequently only Ti is used as the interface material to Si.

Temperature dependent parameters for electrical resistivity, thermal conductivity and heat capacity were used for all materials and based on values reported in [37], [44], and [47]–[51]. If the temperature range of the used parameter is exceeded during the simulations, the values where extrapolated.

The electrical resistivity ρ of silicon depends on the doping level and hence no exact literature values can be used. Instead, it is calculated as a function of the temperature T by

$$\rho\,(T) = \frac{1}{e \cdot \mu\,(T) \cdot n\,(T)}, \tag{3}$$

where e is the elementary charge, n is the mobile charge carrier density (all dopants are ionized and only one charge type is present as a Schottky diode is an unipolar device) and μ is the charge carrier mobility which is modeled according to Arora *et al.* [52]. The charge carrier density in silicon is determined by the doping concentration n_{ext} until a temperature of ∼700 K. At higher temperatures it is dominated by the intrinsic charge density n_i [38] as more and more electron-hole pairs are thermally generated. The relation is expressed by:

$$n\,(T) = n_{ext}\,(T) + n_i\,(T)\,, \tag{4}$$

The temperature dependence of n_i is described after Sze and Ng [38] with

$$n_i\,(T) = 2 \cdot \left(\frac{2\pi k_B T}{h^2}\right)^{3/2} \cdot \left(m_e^* m_h^*\right)^{3/4} \cdot \exp\left(-\frac{E_g\,(T)}{2k_B T}\right), \tag{5}$$

where k_B is Boltzmann constant, h is Planck constant and m_e^* and m_h^* are electron and hole effective masses, respectively.

The band gap E_g in silicon changes also with the temperature and can be expressed by

$$E_g\,(T) = E_g\,(0) - \frac{\alpha T^2}{T + \beta}, \tag{6}$$

where $E_g(0)$, α and β are constants.

The temperature dependent electrical and thermal properties of the used graphenic carbon are strongly influenced by the process conditions and do not have any distinct literature values. Instead, the thermal conductivity and heat capacity of Acheson graphite [44], [47] were used as it is an artificial or rather polycrystalline graphite [37] and it is likely to have thermal properties close to our GC. The electrical resistivity was assumed to have the measured value of ρ_{ref} = 50 mΩ·cm at room temperature (T_{ref} = 300 K). The behavior of the resistivity at higher temperatures was assumed to behave like published data from Pierson [37] and Noyes [51]. For simplicity, these values were assumed for in- and out-of-plane resistivity as the layer is very thin. First, the resistivity decreases, which is different to conventional metals, and between 800 K and 900 K it reaches a minimum with a value ∼75 % of ρ_{ref}. At higher temperatures the resistivity increases again.

The experimentally measured current waveform and density (in average 3.5 MA/cm²) were used in the simulations. The temperature distribution in the C-Si diode near the active region is shown for different time steps in Fig. 14(a-d). At normal operation conditions, low current densities (240 kA/cm²), the diode keeps cool and close to room temperature while the inner part of the active region is heated more. The active area close to the guard ring structure is heated more at high current densities and even a peripheral hot spot is created around the active area which leads to a higher damage probability. This phenomenon is guided by current crowding at the edges of the low doped epitaxial layer, like illustrated in Fig. 14(f) when the device after 5 ns is still at low temperature. This leads to an increased heating of this area and as the silicon becomes more and more intrinsic, the heating is concentrated to this region. The maximum temperature even reaches the melting point of silicon (1685 K [44]) and so the accuracy of the simulation model at this temperature might be affected as the resistivity of molten silicon is dramatically reduced [48] and the exact crystalline behavior is not known. After 100 ns the hotspot in the C-Si diode cooled down to 1550 K as the heat spreads out to the periphery (Fig. 14(d)). The reason is the relative high electrical resistivity of GC that provides not enough current to maintain the hot spot at high temperature.

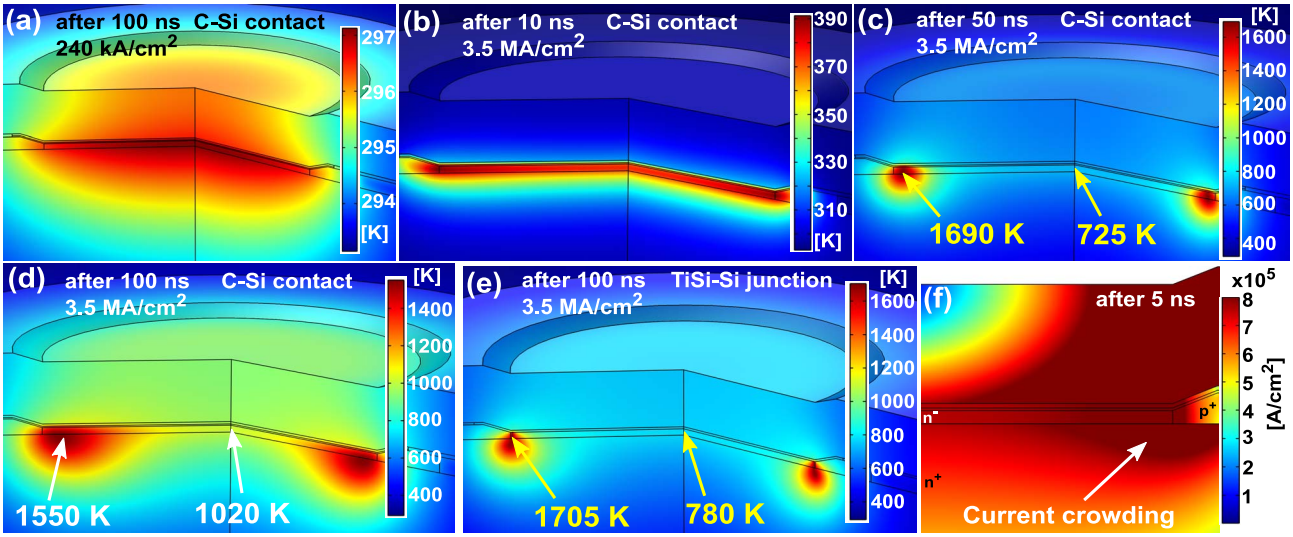

FIGURE 14. **Coupled transient electro-thermal simulations of the used Schottky contacts. Image (a) shows the temperature in the device operated at normal conditions (240 kA/cm^2). (b)-(d) show the temperature distribution in a C-Si diode when stressed with a 3.5 MA/cm^2 current pulse. A peripheral hot-spot is created in the epi-layer during the pulse which spreads out and cools down the hot spot under the melting temperature. In (e) TiSi is used as interface metal but the hot spot doesn't disappear during the pulse. The image in (f) shows that the normalized current density in a cross-section of a C-Si diode. Current crowding at the transition area between epitaxial layer and guard ring is visible.**

Consequently, more current flows to the cooler inner part of the diode and heats this part up.

In the simulation we identified that the exact shape of the temperature dependent resistivity of GC has almost no influence on the temperature distribution and the absolute value in the diode. Even by assuming a temperature independent value with ρ_{ref}, a variation of only $< 10\,\mathrm{K}$ ($< 1\,\%$) in the heat distribution was observed.

This circular hot spot is also formed in case of the TiSi-Si diode but the temperature remains still high after 100 ns (Fig. 14(e)). TiSi or Ti has an about 1000x lower resistivity than carbon and therefore it provides enough current to keep the hot spot at high temperatures, leading to a higher damage probability than a device with GC at the interface. We obtained similar results when we decreased the thickness of the GC layer to 10 nm. The hot filament also didn't disappear as the resistance of the GC film is decreased and hence GC couldn't limit the current to flow through the high temperature outer part anymore. This underlines that a certain minimum GC thickness is needed to have an advantage over the TiSi contact. For a thicker GC layer, the edge region of the diode is also heated more, but the hot spot, as shown in Fig. 14(c), is not formed. This is mainly due to the higher total resistance of the GC film which limits the current through the hot spot.

The concentration of the current at the edges was observed in the real C-Si diode by stressing the diode with a thinner top metallization. Fig. 15 illustrates that a recrystallization of the Cu occurs at the transition region between active area and guard ring, indeed in a circular fashion pointing to a higher temperature at this edge region. Interestingly, the marks here are also visible at regions which are not just in the direct path of the current flow. These results together with

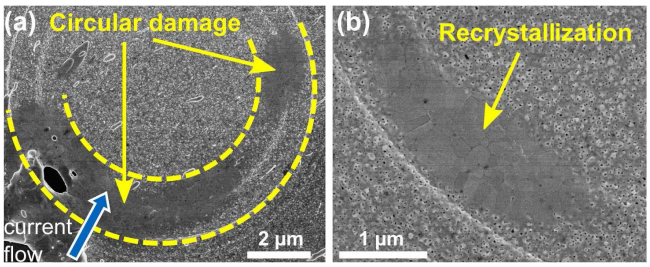

FIGURE 15. **The SEM images show C-Si diodes with thinner metallization after several 3.5 MA/cm^2 pulses were applied. (a) the direct current path from the probe tip to the diode is indicated by the blue arrow. A recrystallization of the top metallization at the transition region between guard ring and active epi region occurs. A damaged region with recrystallized metal is highlighted in (b).**

the previous SEM analysis in Fig. 10(c), where a circular crater was formed in the top metallization, are supported by the results of the FEM simulations. The edge burnout in Schottky diodes at short pulse durations has also been confirmed by Anand *et al.* [53].

VII. CONCLUSION

Due to the material properties of graphenic carbon (GC), the superior reliability of a new C-Si contact compared to a commercial TiSi-Si junction has been demonstrated. In the FEM simulations we identified that a circular hot spot with a temperature close to the silicon melting point is formed at the edge of the diode. This is most likely the main reason for the failure of the device. GC can limit the current through this hot spot and allows the heat to spread away. The exact origin of the failure of the C-Si diodes during the pulse test needs to be evaluated in more detail to enable the examination of the limits of the GC thickness on the reliability. A very thin but

still highly reliable, temperature stable C-Si contact would be a promising candidate for low contact resistance contacts in future semiconductor devices as the barrier height of the C-Si contact can be lowered to 0.41 eV just by changing the process conditions of the GC deposition. A problem might arise due to the high deposition temperature of GC, which might not be compatible with the temperature budget of advanced technology nodes. However, this won't be an issue for power applications with relaxed doping profiles.

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