Technische Universität München

Max-Planck-Institut für Physik (Werner-Heisenberg-Institut)

Development of radiation hard pixel modules employing planar n-in-p silicon sensors with active edges for the ATLAS detector at HL-LHC

Stefano Terzo

Vollständiger Abdruck der von der Fakultät für Physik der Technischen Universität München zur Erlangung des akademischen Grades eines

Doktors der Naturwissenschaften
genehmigten Dissertation.

Vorsitzender: Univ.-Prof. Dr. Alejandro Ibarra
Prüfer der Dissertation:
             1. Hon.-Prof. Dr. Siegfried Bethke
             2. Univ.-Prof. Dr. Stephan Paul

Die Dissertation wurde am 16.09.2015 bei der Technischen Universität München eingereicht und durch die Fakultät für Physik am 09.11.2015 angenommen.

Abstract

ATLAS is one of the two main experiments at LHC with the purpose of investigating the microscopic properties of matter to address the most fundamental questions of particle physics. After the achievements of the first years of running, the potential reach for new discoveries and precise measurements at LHC is being extended by pushing further the energy and luminosity frontiers through three upgrades of the accelerator culminating in the High Luminosity Large Hadron Collider (HL-LHC). To fully profit from the increased luminosity, two main upgrades of the ATLAS inner detector are planned.

The first upgrade was already completed at the beginning of 2015 with the insertion of the IBL, a fourth pixel layer located at just $3.2\,\mathrm{cm}$ from the beam line. The new layer features modules with increased granularity and improved radiation hardness. These include sensors using the 3D technology which is employed for the first time in a high energy physics experiment. In this thesis the properties of these 3D sensors were characterised at beam tests before irradiation and the results used for the validation of the digitisation model implemented in the ATLAS simulation software.

In the second major upgrade, foreseen for 2024, the full inner detector will be replaced by a completely new inner tracker fully made of silicon devices to cope with the high particle density and the harsh radiation environment at the HL-LHC, which during its operational period will deliver $3000\,\mathrm{fb}^{-1}$, almost ten times the integrated luminosity of the full LHC program. The most severe challenges are to be faced by the innermost layers of the pixel detector which will have to withstand a radiation fluence up to $1.4 \times 10^{16}\,\mathrm{n_{eq}/cm^2}$, providing at the same time the maximum possible active area. A novel module concept was developed to fulfil the requirements for the pixel detector at the HL-LHC. This consists of thin planar n-in-p pixel sensors with active or slim edges, connected to the readout chip by a 3D integration concept including the Through Silicon Via technology. Thin sensors are designed to withstand high radiation fluence thanks to their enhanced charge collection efficiency and the possibility of operating at full depletion with moderate voltages. Moreover, the extension of the implantation to the sensor sides, allows to reduce the distance from the last pixel implant to the sensor edge, thus extending the active area up to a full active edge design. The Through Silicon Via technology allows to maximise the active area on the chip by removing the large wire-bond balcony and conveying the signal through the chip itself to the backside. In this thesis different sensor prototypes implementing the technologies described above are investigated before and after irradiation by means of radioactive sources and beam test measurements aiming at the development of a radiation hard four side buttable module for the innermost layers of the ATLAS pixel detector. The results for different sensor thicknesses ranging from 100 to $200\,\mathrm{\mu m}$ are compared with the performance of thicker and thinner sensors, including results from previous analysis. The behaviour at the edge of slim and active edge sensors is investigated and specific studies are presented in view of the future module geometries for the different layers and pseudorapidity regions of the pixel detector. Furthermore, n-in-p sensors were already demonstrated to be a cost effective alternative to the pixel technologies presently employed in ATLAS and are therefore suited to cover large areas in the outer layers for which first prototypes of four chip modules have been developed and characterised.

Keywords: ATLAS, pixel detector, ITk, HL-LHC, n-in-p, thin sensors, slim edges, active edges, radiation damage, IBL, 3D sensors

Contents

Overview

An investigation of novel pixel modules for the ATLAS detector upgrades is presented. The 3D modules employed in the new Insertable B-Layer were measured before irradiation and the results are compared to simulated data. For the ATLAS upgrade at HL-LHC, a novel pixel module concept based on n-in-p planar sensors is presented which combines thin sensors, active edge process and 3D integration using the Through Silicon Via technology. The performance of these technologies is investigated before and after the high irradiation doses expected for the ATLAS pixel detector at HL-LHC.

Chapter 1: The ATLAS experiment at LHC is introduced. Motivations and plans for the upgrade of the accelerator and of the ATLAS detector are discussed.

Chapter 2: The general properties of semiconductor detectors and the main design concepts of pixel detectors relevant for this thesis are explained.

Chapter 3: The design of the present ATLAS pixel modules are described and a novel planar pixel module concept for the ATLAS detector upgrade is presented.

Chapter 4: The experimental methods adopted to obtain the results presented in this thesis are described. The instrumentation is described and the methodology is discussed.

Chapter 5: The characterisation of the 3D pixel technology presently employed in the recently added Insertable B-Layer of ATLAS is discussed. A comparison of experimental and simulated data is presented for the validation of the digitisation model implemented in the ATLAS simulation software.

Chapter 6: The performance of novel n-in-p planar pixel sensors designed for the ATLAS upgrade at HL-LHC are investigated before and after irradiation. The results of different sensor thicknesses, active and slim edge designs are compared. Large area sensors and new pixel layouts are discussed.

Chapter 7: The status of the development of the Through Silicon Via technology is reported.

Chapter 8: A summary of the main results obtained is given, including an outlook on the possible outcome and future objectives of the presented research.

Throughout this thesis natural units $c = \hbar = 1$ are used. Energy, momentum and mass are therefore given in electron-volts (eV). The electric charge is expressed in units of elementary charge (e). The kinematic variables β and γ have their usual relativistic meanings.

1 The ATLAS experiment from LHC to HL-LHC

The Large Hadron Collider (LHC) [1–3], located at the Conseil Européen pour la Recherche Nucléaire (CERN)[1] in Geneva, is presently the largest and most powerful particle accelerator dedicated to high energy physics research. It was built in the $27\,\mathrm{km}$ long underground tunnel between Switzerland and France, which previously hosted the Large Electron Positron collider (LEP). The accelerator is designed for proton-proton collisions up to a centre of mass energy of $\sqrt{s} = 14\,\mathrm{TeV}$ at a maximum nominal luminosity of $10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ and lead ion collisions up to $\sqrt{s} = 1.15\,\mathrm{PeV}$ with a nominal luminosity of $10^{27}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. Two particle beams are collided in four Interaction Points (IPs) along the accelerator ring, where the main experiments, ATLAS[2] [4], ALICE[3] [5], CMS[4] [6], and LHCb[5] [7] are hosted. The ALICE detector is designed to investigate the properties of Quark-Gluon-Plasma in lead ion collisions and the LHCb experiment is dedicated to the study of Charge conjugation and Parity symmetry violation (CP violation) in the b-quark sector. ATLAS and CMS are general purpose experiments using different and complementary technologies to investigate the microscopic properties of fundamental matter. In Section 1.1 the main characteristics of the LHC accelerator complex are described and in Section 1.2 the ATLAS experiment is introduced. The upgrade plans for the accelerator complex and for the ATLAS experiment are then presented and discussed in Section 1.3 and 1.4, respectively.

1.1 The LHC complex

The LHC accelerator complex is illustrated in Figure 1.1. The particle beams are accelerated in subsequent steps by different accelerating machines before being injected into the LHC ring. Protons are obtained ionising a hydrogen gas and are accelerated in bunches inside the LINear ACcelerator (LINAC) 2 to a kinetic energy of $50\,\mathrm{MeV}$. From the LINAC 2 the beam is injected first in the proton synchrotron booster, in which it is accelerated up to $1.4\,\mathrm{GeV}$ and then in the Proton Synchrotron (PS) where it reaches an energy of $25\,\mathrm{GeV}$. From the PS the protons are transferred to the Super proton Synchrotron (SpS) to be accelerated up to $450\,\mathrm{GeV}$ and finally injected into the two beam pipes of the LHC where they circulate in opposite directions until they reach the collision energy. For heavy ion operations, the presently used lead ions are obtained from a source of vaporised lead and accelerated first in the LINAC 3 and then in the Low Energy Ion Ring (LEIR) before being injected into the PS. From there, they follow the same accelerating path as the protons to enter the LHC.

---

[1] `http://cern.ch`
[2] A Toroidal LHC ApparatuS
[3] A Large Ion Collider Experiment
[4] Compact Muon Solenoid
[5] Large Hadron Collider beauty
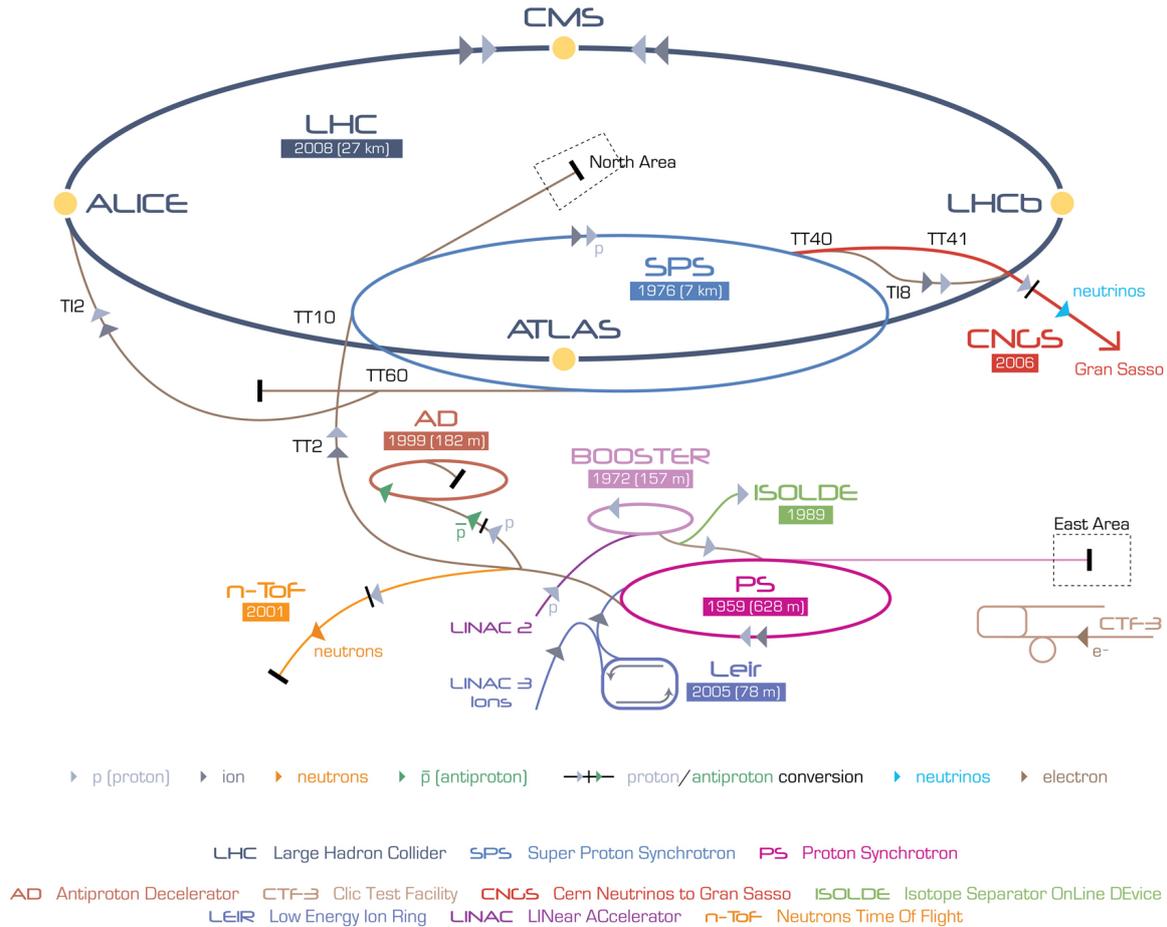
Figure 1.1: The LHC accelerator complex at CERN [8].

1.1.1 Performance

The first collision at the LHC took place in 2010 between two proton beams of 3.5 TeV, the beam energy was then raised to 4 TeV after a first shutdown of the accelerator in 2011, leading to collisions at $\sqrt{s} = 8$ TeV. The centre of mass energy of the collisions is essential to extend the discovery frontier to heavier particles, but is not the only parameter that defines the performance of the accelerator. Especially at hadron colliders, where the quark and gluon interactions give rise to a huge number of different processes, the statistics is a key factor to identify rare decays in the harsh background and even more crucial for subsequent precise measurements of the process characteristics in a reasonable time. This is defined by the luminosity of the collider which is determined by several parameters of the accelerating machine. For the present and the future phases of the LHC, the main beam parameters are summarised in Table 1.1 and discussed in the following.

Luminosity

The luminosity L determines the rate of particle interactions R occurring for a given process cross section σ_{p} according to [1]:

$$R = L\sigma_{\mathrm{p}} \tag{1.1}$$

Table 1.1: Main beam parameters of the LHC before the 2013 shutdown [9] compared with the nominal design parameters and the ones planned for the HL-LHC [10, 11] upgrade for two possible configurations with different bunch spacing.

Parameter Name	Symbol	[Unit]	Run 1	Nominal	HL-LHC	
Bunch spacing	Δt_s	[ns]	50	25	25	50
Protons per bunch	N_{b}	$[10^{11}]$	1.6	1.15	2.2	3.5
Number of bunches	n_{b}	-	1374	2808	2748	1374
Revolution frequency	f_{rev}	[kHz]	11.245	11.245	11.245	11.245
Normalised emittance	ϵ_{N}	$[\mu m]$	2.4	3.75	2.5	3.0
Betatron function at the IP	β^*	[m]	0.6	0.55	0.15	0.15
Piwinski parameter	ϕ	-	0.6	0.65	3.14	2.87
RMS bunch length	σ_{z}	[cm]	≥ 9	7.55	7.55	7.55
RMS beam size at the IP	σ^*	$[\mu m]$	19	16.7	13.6	10.0
Peak luminosity	L_{peak}	$[10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}]$	0.7	1.0	7.18	8.44
Levelled luminosity	L_{level}	$[10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}]$	-	-	5	2.5
Pile up	$\langle\mu\rangle$	[events]	19.5	19	140-200	140-200
Energy	$\sqrt{s}$	[TeV]	8	14	14	14

In a collider, the luminosity is given by the beam intensity I per collision area A which, for a circular machine, assuming Gaussian beam profiles, can be expressed as:

$$L = \frac{I}{A} = \frac{N_{\mathrm{b}}^2 n_{\mathrm{b}} f_{\mathrm{rev}} \gamma}{4\pi \epsilon_{\mathrm{N}} \beta^*} R_\phi \tag{1.2}$$

where n_{b} is the number of bunches, N_{b} is the number of particles per bunch and f_{rev} is the revolution frequency. The collision area of the bunches A is given by the normalised transverse emittance ϵ_{N} and the value of the betatron function at the IP β^*. Furthermore, it depends on a geometric factor R_ϕ which takes into account the collision angle of the bunches [12]. The brightness of the accelerator, defined as $N_{\mathrm{b}}/\epsilon_{\mathrm{N}}$, is mainly limited by the injection chain (booster and PS), while the magnet technology determines the minimum achievable β^*. For the first years of operations, ATLAS recorded an integrated luminosity of $5.08\,\mathrm{fb}^{-1}$ compared to the $5.46\,\mathrm{fb}^{-1}$ delivered by the LHC running with beam energies of $3.5\,\mathrm{TeV}$. After the first shutdown in 2012 the beam energy was increased to $4\,\mathrm{TeV}$ and the accelerator delivered $22.8\,\mathrm{fb}^{-1}$ ($21.3\,\mathrm{fb}^{-1}$ recorded by ATLAS) [13]. Further improvements of the luminosity can be achieved reducing the bunch spacing from the present $50\,\mathrm{ns}$ to $25\,\mathrm{ns}$, without increasing the number of collision events taking place for each bunch crossing (pile-up events).

1.2 The ATLAS experiment

ATLAS is one of the two multi purpose detectors designed to exploit the full potential of the LHC. The main motivation for the design of the ATLAS experiment was the search for the Higgs boson responsable of the symmetry breaking mechanism that gives rise to the different masses of the elementary particles [14–19]. The main breakthrough of the ATLAS and CMS experiments in 2012 was the discovery of a particle which has all the characteristics of the Higgs boson predicted by the Standard Model (SM) theory [20, 21].
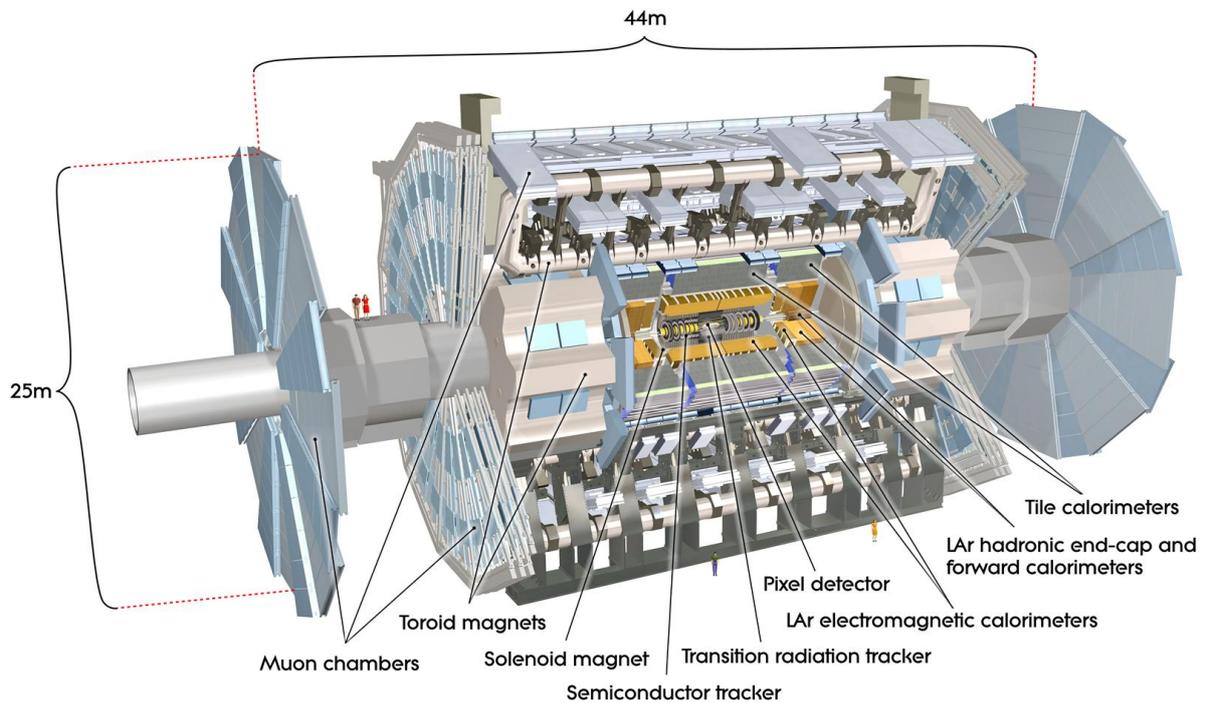
Figure 1.2: The ATLAS detector at the LHC [33].

1.2.1 The ATLAS detector

Most particles investigated at the LHC, such as the Higgs boson, are very heavy and decay immediately after their production. The reconstruction of their invariant masses and the determination of their couplings are obtained though the measurement of their final decay products. The ATLAS detector is a hermetic structure designed to identify and measure the particles originating from proton-proton collisions. It consists of a cylindrical barrel section and two end-caps. Each section is divided into four main sub-detector systems dedicated to the identification of different particles and the determination of their energies and momenta. These are from the inner to the outer part of the detector: the Inner Detector (ID) [22, 23], the electromagnetic calorimeter [24, 25], the hadronic calorimeter [24, 26] and the muon system [27, 28]. The ATLAS detector design is driven by the choice of the superconducting magnet for the muon identification consisting of a large toroidal apparatus [29–31] with an inhomogeneous magnetic field of up to 4 T. An additional central solenoid [29, 32] encloses the ID and creates an almost homogeneous magnetic field of 2 T along the beam direction. The main advantages of this detector design are the large space available for the calorimeter systems and the large level arm provided by the independent magnetic systems, which allows for an excellent muon tracking and trigger performance. As a drawback, both calorimeters are located outside of the central solenoid and their energy resolution is therefore degraded by the large amount of material in front of them.

Inner Detector

The ID is immersed in the magnetic field of the central solenoid and measures the trajectories of charged particles originating from the proton collisions to identify the sign of their electric charges, measure their momenta and reconstruct the decays of short lived particles.

The innermost part of the ID, closest to the IP, is the pixel detector [34, 35] which is composed of four barrel layers (including the recently added Insertable B-Layer (IBL) [36]) and six end-cap disks (three at each side) entirely made of silicon pixel modules. This detector technology provides the highest spacial resolution among the tracking detectors of ATLAS, which is necessary to associate each particle in the final state to the corresponding decay vertex. In particular, in proximity of the IP, this is fundamental to link the decay products to the original proton collision. Moreover, tracking and vertexing performances of the pixel detector are fundamental to distinguish jets of particles originating from different quark flavours. Especially, jets from bottom and charm quarks can be identified measuring the decay of B-mesons (b-tagging) which requires the capability to separate the meson jets from the harsh background and demands high granularity of the tracking devices closer to the IP.

The pixel detector is surrounded by four barrel layers and nine more end-cap disks per side of micro-strip detectors which compose the SemiConductor Tracker (SCT) [37, 38]. The micro-strips are silicon detectors with larger readout structures and consequently reduced spatial resolution and cost with respect to pixel detectors, which make them suitable to cover larger areas at outer radii. The ID is completed by the Transition Radiation Tracker (TRT) [39, 40]. This is composed of straw tubes with 4 mm of diameter filled with a mixture of ionising gas (mostly xenon). Radiation foils and fibres are inserted between the tubes to enable the generation of transition radiation by crossing particles, which allows to distinguish electrons from pions. The ID itself is able to provide a full information about charged particles in the analysis of a physics process and thanks to the fast timing of its detector technologies is essential for pile up rejection.

Electromagnetic calorimeter

The Electromagnetic CALorimeter (ECAL) is a sampling calorimeter composed of accordion shaped layers consisting of Liquid Argon (LAr) as active material and lead plates as absorbers. This structure is designed to stop electrons and photons, measuring at the same time their energy. The barrel part sits just outside of the central solenoid and it is completed by two end-caps in the forward regions of the ATLAS detector.

Hadronic calorimeter

The function of the Hadronic CALorimeter (HCAL) is to stop and determine the energy of jets originated from the quark hadronisation. As the ECAL, this is also a sampling calorimeter which, for the barrel part, consists of iron absorbers and scintillating tiles of polystyrene as sensor material. The end-caps are instead made of copper and tungsten absorbers with LAr active layers.

Muon system

The muon system is the outermost detector of ATLAS with the main task of measuring the momentum of the muons, which can penetrate several metres of material without being stopped

and thus pass through the calorimeters. The barrel part is hosted inside the magnetic field of the toroidal magnet system and consists of two layers of Resistive Plate Chambers (RPCs) used for triggering and of three layers of Monitored Drift Tube (MDT) chambers composed of arrays of drift tubes of 30 mm of diameter for muon tracking. The same tasks are performed in the end-caps by the Thin Gap Chambers (TGCs) and the Cathode Strip Chambers (CSCs) in addition to two disks per side made of MDTs.

1.2.2 Coordinate system

In this thesis, the coordinate system of the ATLAS detector is defined in cylindrical coordinates with the origin at the IP, at the geometrical centre of the detector. The z axis points along the beam line, the azimuth φ is the angle around the z axis and the radial distance from the beam line r. An additional parameter is given by the pseudorapidity η of the particles originating from the primary vertex. This is defined as:

$$\eta = -\log\left(\tan\frac{\theta}{2}\right) \tag{1.3}$$

where θ is the angle between the particle momentum and the z axis. Hence, $\eta = 0$ indicates a particle exiting the IP with direction perpendicular to the beam line, while $\eta = \infty$ is the direction of the beam line. Because of the symmetry of the concepts described in this thesis, the direction of the axis is not relevant. The ATLAS detector ensures a coverage over the entire φ with all its sub-detectors, that are instead differently limited in their pseudorapidity coverage. The muon spectrometer has a coverage of $|\eta| < 2.7$, while the HCAL covers up to $|\eta| < 4.9$ and the ECAL in the forward direction reaches $|\eta| < 3.2$. The original ID was covering $|\eta| < 2.5$ and after the IBL insertion is now reaching $|\eta| < 3.0$.

1.3 The way to the HL-LHC

Before the first Long Shutdown (LS) at the beginning of 2013, the LHC delivered about $30\,\mathrm{fb}^{-1}$ of data operating at $\sqrt{s} = 7\,\mathrm{TeV}$ for the first years and at $\sqrt{s} = 8\,\mathrm{TeV}$ from 2012 [13]. The next phases of the LHC will bring the collider to its nominal centre of mass energy, $\sqrt{s} = 14\,\mathrm{TeV}$, and will further increase the luminosity through a series of upgrades of the accelerating machines culminating in the HL-LHC.

1.3.1 Physics motivations

The increase of energy and luminosity will allow to further investigate the Higgs mechanism for a better understanding of the SM and will extend the potential reach for discoveries of physics Beyond the Standard Model (BSM) [41–43]

Higgs boson

After the Higgs-like boson discovery the main purpose of the ATLAS and CMS experiments is to understand the nature of this new particle. Its mass of about 125 GeV [44], is particularly suited for investigations at the LHC, due to the large number of decays predicted by the SM that could be experimentally reconstructed. The integrated luminosity collected thanks to the upgrades of the accelerator, will allow to determine the spin and CP quantum numbers of this

new particle with an increased significance and obtain precise measurement of its couplings to prove if it is effectively the SM Higgs boson. Moreover, the huge statistics delivered by the HL-LHC that will produce a factor ten more Higgs particles than the entire LHC program, will permit to further probe the symmetry breaking mechanism and check the consistency of the SM by measuring the Higgs self-couplings [42].

Supersymmetry

In the present picture of the SM in which the existence of the Higgs boson is confirmed, it still remains to be explained why its mass is lighter than the Planck mass which defines the length scale for the unification of quantum mechanics and general relativity. One possible answer to this so-called hierarchy problem is given by the Supersymmetry (SUSY) theories [45–49] which predict a symmetric partner for each particle of the SM. In particular, the existence of the super-symmetric partner of the top quark with a mass lower than 1 TeV would cancel the quadratic divergence in the renormalisation of the Higgs mass. At the same time, SUSY can also offer a solution for the dark matter problem of the missing mass in the universe, in which the lightest super-symmetric particle could be a dark matter candidate if its decay into non super-symmetric particles is forbidden. The future energy and luminosity frontiers foreseen with the accelerator upgrades will give access to the potential discovery of SUSY particles or alternatively will extend the constrains for such theories.

Beyond the Standard Model

In addition to the SUSY extensions, a wide range of models provide entirely novel explanations for the still unsolved problems of fundamental physics. Most of the particles and phenomena predicted by these BSM theories foresee the production of cascade decays with final states involving high transverse momentum leptons, photons, jets and missing transverse energy which are in the reach of the LHC. Up to now the LHC experiments were able to set several constrains for these theories, but the increase of the energy and the huge luminosity at the HL-LHC will rise the sensitivity for many different new processes, for example in top anti-top and dilepton resonances [42, 50, 51]. Furthermore the LHC will explore new frontiers never previously reached in particle colliders which could reveal signature of new particles and open the way for completely new BSM theories.

1.3.2 Upgrade schedule

The upgrade schedule of the LHC, shown in Figure 1.3, will require three LS periods in which the accelerator will undergo several upgrades, each one followed by a physics run that will profit from the luminosity and energy improvements.

LS1 - Run 2

The LS1 started in 2013 and was completed in April 2015 with the aim of consolidating the accelerator allowing for collisions at energies close to the design value. After a rework of the interconnections of the accelerator magnets and the replacement of 18 of them, higher currents and thus higher magnetic fields can be achieved. For the following Run 2, the number of protons in the bunches will be reduced to limit the pile up, but at the same time the bunch spacing will be decreased from 50 ns to 25 ns, effectively increasing the luminosity. Moreover, the width of
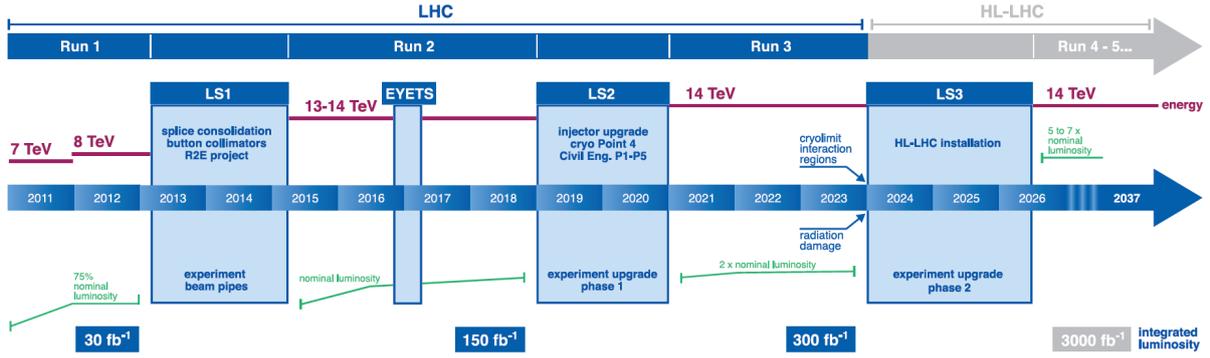
Figure 1.3: The upgrade schedule of the LHC [52].

the beam decreases with the energy rise allowing for a better focus of the beams and therefore leading to an even further increase of the peak luminosity which is expected to exceed the nominal design already after this shutdown. In the first period after the LS1, the LHC will be operated at $\sqrt{s} = 13 \, \text{TeV}$ to eventually reach the design energy of $\sqrt{s} = 14 \, \text{TeV}$ by the end of Run 2.

LS2 - Run 3

Another LS is foreseen to start in 2019 to connect the new LINAC 4 [53] to the LHC complex which will replace the present LINAC 2. At the same time the consolidation of the LHC and its injector chain will allow for an increase of the number of protons per bunch. This second upgrade stage is expected to provide a further increase of the peak luminosity up to $2.5 \times 10^{34} \, \text{cm}^{-2} \, \text{s}^{-1}$ [54].

LS3 - HL-LHC

At the end of the planned LHC program, the statistical improvement of running the accelerator without a significant increase of its luminosity will become minimal, since the time required to half the statistical uncertainties will be more than ten years [41]. Hence, to extend the physics reach and collect the necessary statistics for the precise measurement of rare processes, a major upgrade of the LHC is planned which will provide a substantial increase of the luminosity up to $5–7 \times 10^{34} \, \text{cm}^{-2} \, \text{s}^{-1}$. The aim of this new phase, named HL-LHC, is to collect a total integrated luminosity of $3000 \, \text{fb}^{-1}$ with an average of $200–300 \, \text{fb}^{-1}$ per year to exploit the further discovery potential of the machine in a reasonable operation time of $10–12$ years. To achieve the HL-LHC luminosity goal, a complete upgrade of the injection complex and an improvement of the technology of the magnets will be necessary to reduce the β^* factor and increase the number of protons per bunch while keeping the emittance at the present low value [55]. Several new technologies are presently under study for the HL-LHC which include $11–13 \, \text{T}$ superconducting magnets [56] and high-power superconducting links with zero energy dissipation [57] as well as new superconducting radio-frequency cavities (crab cavities [58, 59]) which allow to reduce the colliding area by rotating the bunches just before their collision. However, the higher pile up and the degradation of the performance of the inner tracker by intense radiation will become a serious limitation at a luminosity higher than $5 \times 10^{34} \, \text{cm}^{-2} \, \text{s}^{-1}$, therefore a controlled reduction

of the peak luminosity (luminosity levelling [60]) is foreseen for the HL-LHC baseline. These upgrades are planned to be implemented during a third long shutdown, LS3, starting in 2024.

1.4 Upgrades of the ATLAS detector

To maintain its capabilities and profit from the increased energy and luminosity of the accelerator up to the end of the HL-LHC program, the ATLAS detector will also require substantial upgrades and consolidations of its sub-detectors. This section gives an overview of the main requirements and planned upgrades of the ATLAS detector focusing mainly on the ID and in particular on the pixel detector which is the topic of this thesis.

1.4.1 Phase 0

During the LS1 an additional pixel layer, the IBL, was introduced in the barrel at a radius of 3.2 cm from the beam line, thus becoming the new innermost layer. The IBL was inserted together with a smaller beam pipe, 2.4 cm of inner radius, replacing the one used in Run 1. The IBL consists of 14 staves with newly designed pixel modules. These employ a new readout chip, the FE-I4 [61], which features a larger area with a reduced pitch and an improved radiation hardness than the former FE-I3 chip [62] used in the original pixel detector. Two different silicon sensor technologies are implemented in the IBL: planar n-in-n and 3D sensors [63]. The higher granularity of these devices will help to maintain and improve the tracking and b-tagging efficiency to deal even with the higher pile up expected for Run 3. Moreover, the IBL will provide compensation for the expected degradation of the original pixel detector due to radiation damage. A more detailed description of the pixel modules employed in the present ATLAS pixel detector is given in Chapter 3. For the cooling of sensors and electronics, a new system with reduced mass and based on CO_2 was implemented.

In the same shutdown period the muon spectrometer was also augmented with the installation of new MDT chambers featuring drift tubes with a smaller diameter, which will improve the detection efficiency at $1.0 < |\eta| < 1.3$, and a new neutron shielding to cope with the higher particle fluence.

1.4.2 Phase I

The next upgrade of the detector is planned during the LS2. This will complete the improvements to withstand the foreseen luminosities well beyond the nominal values [64]. The proposed innovations include the installation of new Muon Small Wheels in the forward regions of the detector. These will be composed of MICROMEGAS micro-pattern gas detectors [65] complemented with small-strip Thin Gap Chambers which will create a redundant system for both tracking and triggering. Moreover, to maintain an effective trigger capability in the higher pile-up regime, a dedicated highly parallel hardware-based track finder [66, 67] will be implemented which makes use of the full pixel detector to provide track information to the Level-2 trigger. Further upgrades of the calorimetry system are also discussed to improve the segmentation in the front and middle ECAL sampling layers and thus increase the background rejection by a better discrimination of electrons and jets.

1.4.3 Phase II

The last planned detector upgrade, heading to the HL-LHC, is foreseen during the LS3 from 2024 to 2026. The number of pile-up events expected at the HL-LHC is 140-200 [11], which is almost five times the one at the nominal luminosity. This will require high occupancy capabilities which cannot be provided by the TRT gas detector technology. Moreover, the performance of the pixel detector and the SCT will be degraded by the accumulated radiation fluence. A replacement of the whole tracker will be thus necessary to face the harsh environment at HL-LHC.

The new Inner Tracker (ITk) is planned to be completely based on silicon sensors and will require high granularity, improved material budget and increased radiation hardness. The current baseline design, shown in Figure 1.4, consists of four pixel and six strip layers in the barrel part and six pixel and and seven strip double-sided disks in each of the two end-caps. A possible alternative, also strongly supported, foresees instead five pixel and four strip layers. To meet the occupancy requirement, the size of the pixel cells for the outer layers of the pixel detector will be reduced to the one of the present IBL, while for the innermost layers an even smaller pixel pitch is planned, which requires the design of a new readout chip [68]. The solutions presently under investigation include square pixels of $(50 \times 50)\,\mu m^2$ pitch or rectangular pixels with a reduced pitch in the φ direction of $(25 \times 100)\,\mu m^2$. In addition, an extension of the η coverage with respect to the baseline design to reach up to $|\eta| = 4$ with the innermost layer and additional end-cap disks is of great interest to fully exploit the physics potential at HL-LHC [69,70]. This extension of the pixel detector increases, for example, the sensitivity for the Higgs production through vector boson fusion which is predicted to be the second largest contribution to the total Higgs production cross section. In this process the Higgs boson is generated by the fusion of two W or Z bosons emitted by the interacting quarks resulting in two opposite forward jets in the final state. The investigation of decay channels such as $pp \rightarrow qqH \rightarrow ZZ^* \rightarrow l^+l^-l^+l^-$ and $pp \rightarrow qqH \rightarrow WW^* \rightarrow l\nu l\nu$ allows to measure with better precision the vector boson coupling to the Higgs boson [71,72]. More challenging physics channels involving the decay of Higgs bosons in b quark pairs, which are suppressed by the large background, become accessible with the huge statistics at HL-LHC. These channels not only have an impact on the precise determination of the Higgs properties such as the Higgs self coupling [73], but their observation could also be an evidence for many BSM theories which for example predict rates of Higgs boson pair production significantly higher than in the SM [71].

B-tagging and lepton identification rely on the impact parameter resolution and two-track separation, and depend critically on the rate of fake tracks. In particular, the reconstruction efficiency for hadrons and electrons is dominated by the interaction with the detector material, due to hard scattering and bremsstrahlung, respectively, resulting in a systematic uncertainty which globally is of the order of $5\,\%$ [74]. The dependance of the reconstruction efficiency on the pile up and ageing of the detector modules should be smaller than this uncertainty. The efficiency of the tracking modules and the minimisation of the dead areas are fundamental to maintain the capabilities for fake track rejection and ensuring a sufficient number of hits, especially in the pixel layers, where are essential to constrain tracks in particular in the core of high energetic jets. The radiation hardness will thus be another huge challenge not only for the chip design, but also for the sensor technology. In the inner layers, the modules will have to withstand an integrated fluence of $1.4 \times 10^{16}\,n_{eq}/cm^2$ within the HL-LHC running period, hence the possibility of replacing the two innermost pixel layers is also under discussion. Moreover, the pixel modules are required to have the largest possible active area since, as for the IBL, they cannot be overlapped along the z-direction. For the outer pixel layers, due to the larger

area to be covered, a cost reduction is required for the module production and assembly, in particular for the sensor technology and the interconnection to the readout chips. The expected fluences and the most relevant requirements for the design of the pixel modules for the different barrel layers and the end-cap disks of the ITk at the HL-LHC are summarised in Table 1.2.
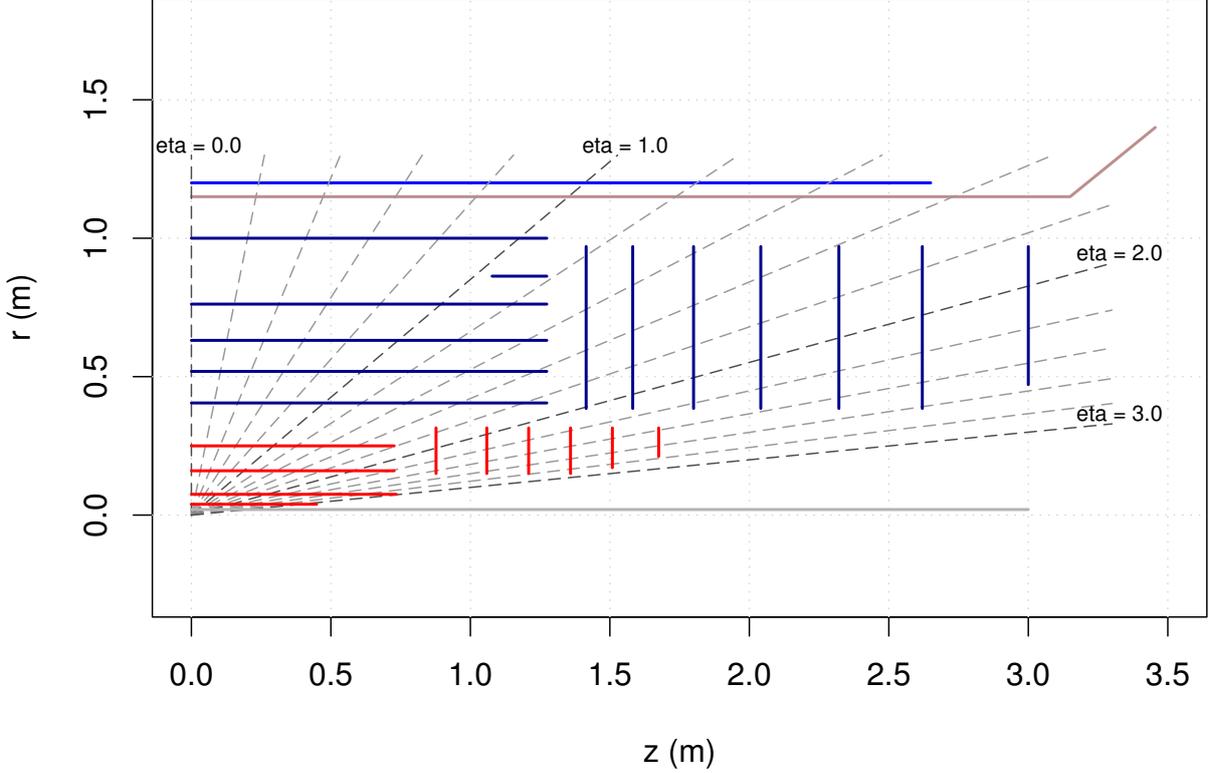

Figure 1.4: The baseline layout of the ITk for the ATLAS Phase II upgrade [75]. The picture shows a quarter of the ITk where the pixel detector layers are represented in red and the silicon strip layers in blue. An alternative scenario includes the extension of the pseudorapidity coverage with the innermost pixel barrel layer up to $|\eta| < 4$ [71].

Table 1.2: Baseline requirements for the different barrel layers and for the end-cap disks of the pixel detector at HL-LHC [75, 76]. The expected maximum fluence is given for an integrated luminosity of $3000\,\mathrm{fb}^{-1}$ [77]. Additional safety factors usually considered for the module design are not applied.

Parameter	Layer 1	Layer 2	Layer 3	Layer 4	End-cap disks
Radial position [mm]	39	78	155	250	-
Maximum fluence [$10^{15}\,\mathrm{n_{eq}/cm^2}$]	14	5.4	3.5	0.9	1.8
Module [chips]	2×1	2×2	2×2	2×2	2×2 or 2×3
Inactive edge [μm]	150	150	500	500	500
Total area [m^2]			5.1		3.1

The trigger system will also be upgraded by implementing a track trigger combining full granularity calorimeter and improved muon trigger coverage. Additional upgrades are planned for the calorimetry systems to ensure their adequate performance in the high radiation environment. These will consist mainly of a replacement of the readout electronics.

2 Semiconductor detectors

Solid state detectors based on semiconductor materials are the state of the art of tracking devices in high energy physics experiments. With respect to gas devices, which are less expensive and therefore employed in the outer parts of the detectors at LHC, solid state detectors represent a very compact solution which guarantees higher granularity and radiation hardness with faster timing. They are therefore particularly suited to be operated close to the IP where the high particle multiplicity per event and the integrated radiation dose are demanding high tracking performance. In this chapter the properties of semiconductor detectors and in particular those of silicon pixel detectors are described. Section 2.1 presents the general characteristics of semiconductors and how they are used for particle detection. In Section 2.2, the effects of radiation damage in silicon sensors is discussed. Finally, Section 2.3 introduces the concept of pixel detector and its design and production for high energy physics applications.

2.1 General properties

The periodic structure of the crystalline lattice in solid materials defines discrete energy levels in which electrons are confined. The highest energetic level which is fully filled with the outer-shell electrons constituting the covalent bondings of the atoms within the crystal, is called valence band, while the next higher energetic level, which may be empty or partially filled, is called conduction band. Depending on the material, these bands may be overlapping or separated by forbidden energy gaps. In the former case the electrons are free to move in the crystalline lattice and the solid is called conductor. In the latter case, instead, the electrons need to acquire enough energy to cross the forbidden gap and reach the conduction band where they can migrate throughout the crystal. Such a material is classified as insulator or semiconductor, depending on the width of the gap between the valence and the conduction band. The probability for an electron to occupy an energy level E at thermodynamic equilibrium is given by the Fermi-Dirac distribution:

$$f_{\mathrm{e}}(E) = \frac{1}{1 + \exp\left(\frac{E - E_{\mathrm{f}}}{k_{\mathrm{B}}T}\right)} \tag{2.1}$$

where k_{B} is the Boltzmann constant, T is the absolute temperature and E_{f} is the Fermi energy, which in an *intrinsic* material, i.e. an ideal pure material without impurities, lies between the energies of the valence E_{V} and conduction E_{C} bands, in the middle of the band gap:

$$E_{\mathrm{f}} \sim \frac{E_{\mathrm{C}} + E_{\mathrm{V}}}{2}. \tag{2.2}$$

Semiconductors are usually defined by a band gap energy E_{g} of less than $3\,\mathrm{eV}$ which allows electrons to have a non negligible probability of occupying a state in the conduction band at room temperature (about $300\,\mathrm{K}$). When one or more electrons are lifted from the valence band to the conduction band, they are free to migrate throughout the crystal and at the same time a vacancy, also called hole, is left in the valence band by each missing electrons which represents a

net positive charge that can also move in the lattice. The resulting resistivity ρ of the material is given by the concentration of electrons in the conduction band n and holes in the valence band p, and their mobilities (μ_e and μ_h) as:

$$\rho = \frac{1}{e(n\mu_e + p\mu_h)} \tag{2.3}$$

Since the detector technology discussed in this thesis is based on silicon, the following sections are mainly focused on the treatment of this material. Silicon is the most common semiconductor material used for charged particle detection since it is available with high purity and offers a good energy resolution with reduced noise at moderate temperatures. It is characterised by a crystalline lattice with a diamond structure and a band gap of $E_g(300\,\mathrm{K})$=1.12 eV. In an intrinsic semiconductor material n is equal to p which for silicon would be of the order of $10^{10}\,\mathrm{cm}^{-3}$ [78]. Commonly available silicon has a non negligible amount of impurities in the crystal, that cannot be avoided, which compromises its bare use as particle detector. Therefore, to define and control its properties, the semiconductor material is doped artificially introducing additional impurities which increase either n or p. In the first case the dopants introduce a energy level in the band gap that is close to the conduction band and are called *donors*, while in the second case they introduce a energy level close to the valence band and are referred to as *acceptors*. In silicon the most commonly used acceptor is boron which has one bonding electron less than the silicon atom in the lattice resulting in a so-called *p-type* silicon. Instead, as donor, phosphorous is commonly used, which provides additional bonding electrons with respect to silicon resulting in a negative charge excess and a so-called *n-type* silicon. In doped silicon, the energy required to move an electron from the valence band to the new acceptor level or from the new donor level to the conduction band is much smaller than E_g and a high current is easily induced by thermal excitation.

2.1.1 The pn-junction

For particle detection a junction of p-type and n-type silicon is used. This is obtained from a single crystal doped with donors and acceptors on two different sides. At the junction of the two regions, due to their different concentration, electrons and holes diffuse from the zones of high concentration to those of low concentration where they recombine with the opposite carriers and create a so-called *depleted region* with $p = n$. As an effect of the recombination a space charge of opposite sign is produced in the depleted region which creates an electric field that diminishes the tendency for further diffusion up to the equilibrium. The potential across the junction can be found solving the Poisson equation:

$$\nabla^2 \phi = -\frac{\rho}{\epsilon} \tag{2.4}$$

where ϵ is the dielectric constant of the medium and ρ is the net charge density. At the junction between the two doping concentrations, the band structure is therefore modified as shown in Figure 2.1. In this configuration the depleted region exhibits a very high resistivity compared to the doped areas and can be used as active area for detection of ionising particles, but only with very poor performance, due to the small *built-in* voltage V_{bi} of about 1 V that is spontaneously created across the junction. Applying a reversed bias voltage V_b to the junction, i.e. a voltage polarized inversely with respect to the intrinsic electric field at the junction, further charge

(a) p-type and n-type silicon
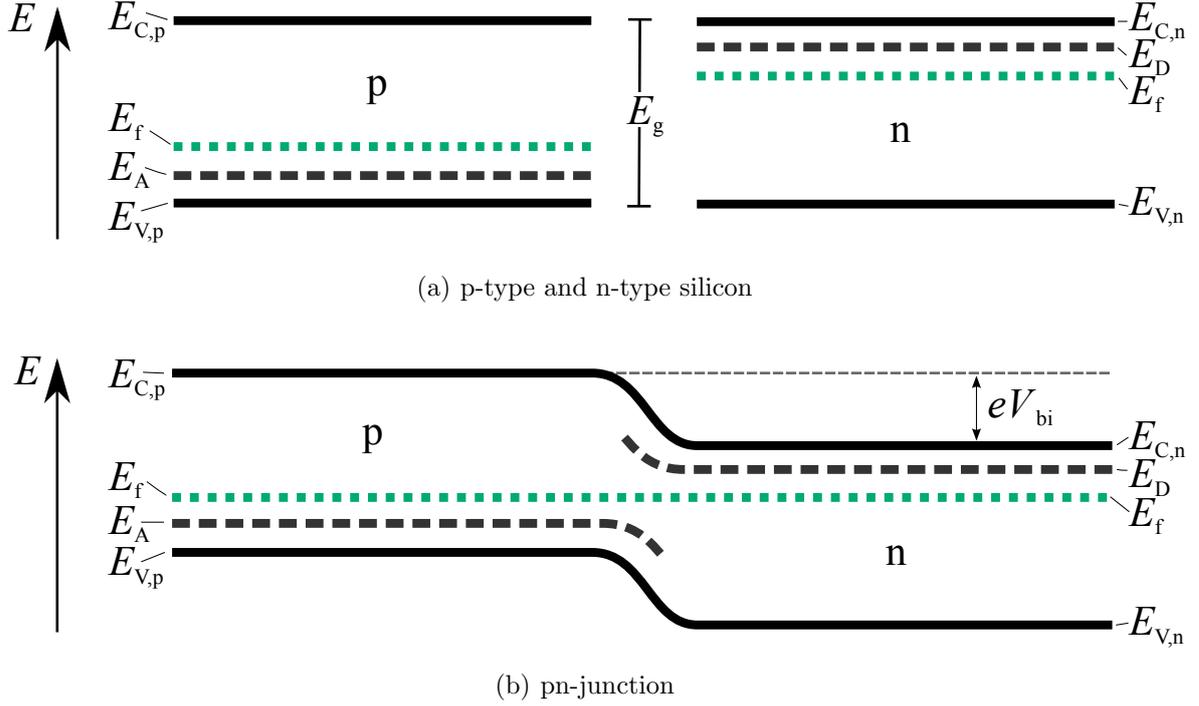
(b) pn-junction

Figure 2.1: Energy levels in the band structure of p-type and n-type silicon before (a) and after (b) the formation of the pn-junction. The energies of the valence (E_V) and the conduction (E_C) bands are drawn together with the Fermi energy (E_f). The symbols E_D and E_A indicate the energy levels introduced by donor and acceptor dopings, respectively. The widths of the energy gap and the energy given by the built-in voltage are indicated by E_g and eV_{bi}, respectively. Image adapted from Ref. [79].

carriers are removed from the doped regions extending the width of the depleted region d_a according to:

$$d_a = \sqrt{\frac{2\epsilon(V_b + V_{bi})}{e}\left(\frac{1}{N_D} + \frac{1}{N_A}\right)} \tag{2.5}$$

where N_D and N_A are the dopant concentrations of donors and acceptors, respectively. Since the pn-junction is usually obtained with a predominant doping concentration and $V_b \gg V_{bi}$, Eq. 2.5 can be simplified as:

$$d_a \cong \sqrt{\frac{2\epsilon V_b}{eN}} \tag{2.6}$$

where N represent the dopant concentration of the side of the junction that has the lower dopant level. The minimum voltage for which the depleted region extends over the entire detector thickness d_b is called *full depletion voltage* V_{fd}. For $V_b > V_{fd}$ the electric field in the depleted region increases by $(V_b - V_{fd})/d_b$ and the detector is said to be *over-depleted*. Since the depleted region is the active area where the produced charge can be detected, the maximum signal for a particle traversing the sensor through its thickness is obtained when the full depletion is reached.

2.1.2 Charge generation

The average number of electron-hole pairs produced in the depleted region of the semiconductor is proportional to the energy transferred to the lattice divided by the average energy necessary to create an electron-hole pair, that in silicon is $3.65\,\mathrm{eV}$ at $300\,\mathrm{K}$. At low energies, photons interact in the semiconductor mainly through the photoelectric effect releasing all their energy in a localised area of the bulk and creating a proportional number of electron-hole pairs. On the other hand, charged particles interact in the depleted region of the semiconductor creating electron-hole pairs along their entire path with a mean energy loss per length transferred to the material, which is described by the Bethe-Bloch equation [80]. While highly ionising particles, such as alpha from radioactive decays, are stopped in the material losing most of their energy at the end of their path, particles that reach their minimum energy loss, so-called Minimum Ionising Particles (MIPs), can pass through the full active thickness of the silicon detector and are those typically measured in high energy physics experiments with tracking devices. For charged particles passing through detectors of moderate thickness, the energy loss is subject to large fluctuations and its probability distribution is described by a Landau-Vavilov distribution for which the Most Probable Value (MPV), indicated with Δ_p, is given by [81, 82]:

$$\Delta_{\mathrm{p}} = \xi \left[\ln\frac{2m_{\mathrm{e}}\beta^2\gamma^2}{I} + \ln\frac{\xi}{I} + 0.200 - \beta^2 + \delta(\beta\gamma) \right] \tag{2.7}$$

where m_{e} is the electron mass, I is the mean excitation energy of the material, $\delta(\beta\gamma)$ is a density effect correction to the ionisation energy loss [83] and $\xi \propto d_{\mathrm{a}}/\beta^2$. The MPV of the Landau-Vavilov distribution therefore depends on the active thickness d_{a} and the particle energy as shown in Figure 2.2.

The long tail of the Landau-Vavilov distribution is given by rare but not negligible high-energy-transfer events in which a γ-ray or a δ-ray is generated. Compared to the MPV, the mean energy loss described by the Bethe-Bloch is very sensitive to these high-energy-transfer collisions with about $90\,\%$ of the events resulting in an energy deposit below this value. The most probable energy loss is, instead, less sensitive to fluctuations and tails of the distribution, it is therefore used to measure the deposited charge.

2.1.3 Signal formation

When a reverse bias voltage is applied to the pn-junction, the electric field E in the detector increases and the electron-hole pairs created in the depleted region drift towards the positive and negative electrodes, respectively, with a velocity given by:

$$v_{\mathrm{e,h}}(E) = \mu_{\mathrm{e,h}}E \tag{2.8}$$

The movement of the charge in the electric field induces a current i on the electrodes which is described by the Shockley-Ramo theorem [84, 85]:

$$i = e\vec{v} \cdot \vec{E}_{\mathrm{w}}. \tag{2.9}$$

Here E_{w} is the *weighting field* which is defined as the negative gradient of the *weighting potential* ϕ_{w} obtained solving the Laplace equation $\nabla^2\phi_{\mathrm{w}} = 0$ with specific boundary conditions. These imply a unit voltage on the electrode for which the charge is calculated and a 0 voltage
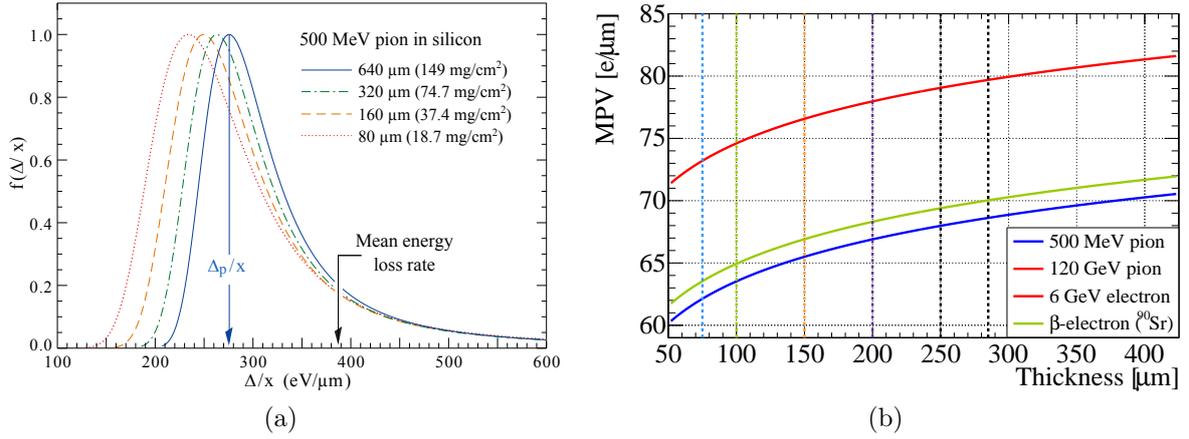
Figure 2.2: Distribution of the energy released by charged particles traversing a silicon sensor and correspondent MPV of electron-hole pairs created as a function of the sensor thickness. (a) shows the Landau-Vavilov distributions obtained for a 500 MeV pion crossing different silicon thicknesses calculated from Eq. 2.7 [81]. (b) shows the MPV of the number of electron-hole pairs created per micron for various particles and energies as a function of the sensor thickness. The curves for electrons with energies of 4 GeV and 120 GeV pions are indicated by the same colour since their difference is insignificant. The vertical lines indicates the most relevant detector thicknesses for this thesis. Image adapted from Ref. [79].

for all the other electrodes. The resulting charge signal Q is obtained integrating this current over the charge collection time $t_c = [t_1; t_2]$ for a charge moving from $\vec{x}_1$ to $\vec{x}_2$:

$$Q = \int_{t_1}^{t_2} i(t)\, dt = e[\phi_w(\vec{x}_1) - \phi_w(\vec{x}_2)] = e\Delta\phi_w. \qquad (2.10)$$

As illustrated in Figure 2.3, the weighting potential in a pad detector, in which the electrode dimensions are larger than the bulk thickness, is a liner function of the distance from the electrode z going from 1 to 0 and thus, the signal at the anode is calculated from Eq. 2.10 as the sum of the contributions of both charge carriers by:

$$Q = -n_q e\left(\frac{z}{d_b} - 1\right) + n_q e\left(\frac{z}{d_b} - 0\right) = n_q e \qquad (2.11)$$

where n_q is the number of electron-hole pairs generated. The first term in Eq. 2.11 is the contribution of holes and the second is the contribution of electrons, hence the signal induced by each charge carrier separately depends on the interaction depth, but the total signal depends only on n_q. In this case, even if the current is not constant in time, because it changes with the electric field, the induced charge is the same for any part of the drift path. As shown in Figure 2.4, this linear approximation of the weighting potential does not hold if the dimension of the electrode become similar or even smaller than the thickness of the detector, as it is generally the case in pixel detectors. For these configurations the region further away from the electrode, where the weighting potential approaches zero, gets larger and, as a result, most of the signal is induced by the charges drifting towards the electrode in the last part of the

their path. As opposite, the contribution of charges drifting away from the electrode becomes negligible. Nevertheless, when all charge carriers reach the electrodes, the integral of the induced current is always equal to the number of electron-hole pairs generated (full collected charge).
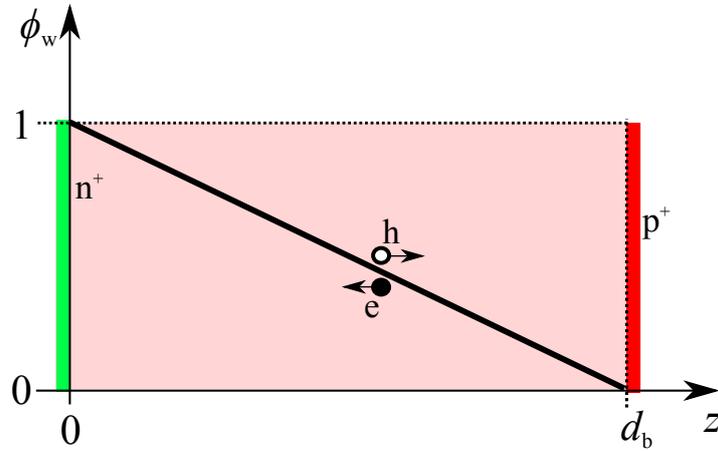

Figure 2.3: Weighting potential as a function of the bulk thickness d_b for a pad detector (electrode dimensions larger than d_b).
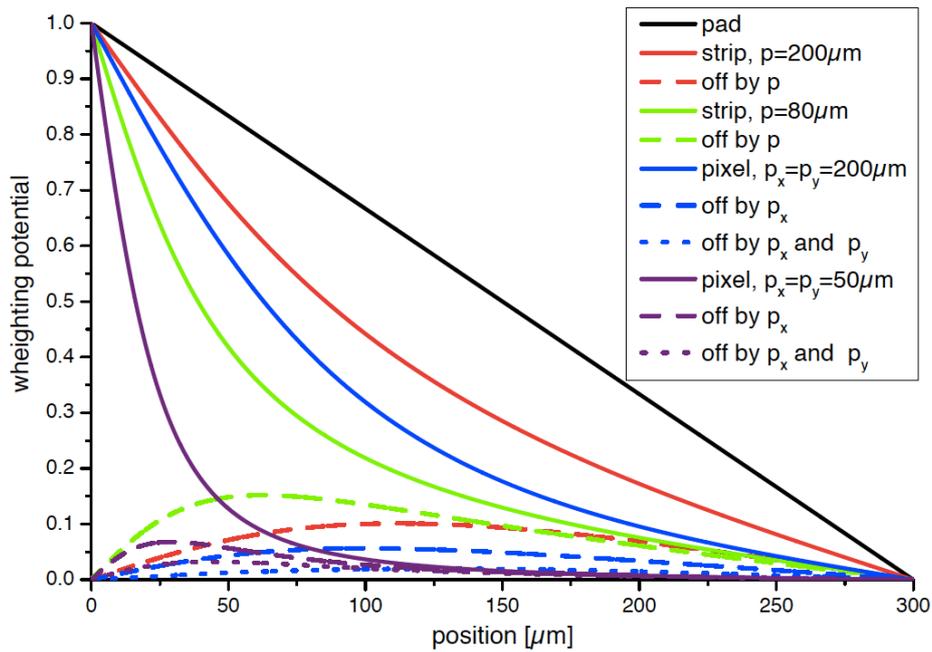

Figure 2.4: Weighting potential for different electrode dimensions as a function of the distance from the electrodes for a $300\,\mu m$ thick sensor. The symbols p_x and p_y indicate the x and y pitches of the pixels and p indicates the pitch of the strips. The weighting potential is calculated in the centre of the electrode (solid lines) and between the electrodes (dashed lines). Image taken from Ref. [86].

Diffusion

During their drift, electrons and holes are also subject to random movements, due to the variation of the carrier concentration within the material, which leads to a diffusion of the charge cloud. After a drift time t_d, the lateral diffusion of the minority carriers σ_D is given by [87]:

$$\sigma_\mathrm{D} = \sqrt{Dt_\mathrm{d}} \tag{2.12}$$

where D is a diffusion constant which depends on the temperature T and on the charge carrier mobility $\mu_\mathrm{e,h}$ as:

$$D = \frac{k_\mathrm{B}T}{e}\mu_\mathrm{e,h} \tag{2.13}$$

Since, according to Eq. 2.8, $t_\mathrm{d} \propto 1/\mu_\mathrm{e,h}$ the effect is equal for electrons and holes. For segmented semiconductors, due to charge diffusion, the induced signal may be spread over several electrodes. In a pixel detector this effect can be used to improve the spatial resolution as discussed in Section 4.5.4, but at the same time it may lead to inefficiencies if the electronics is not able to deal with the smaller signal induced in each pixel.

2.1.4 Leakage current

When the pn-junction is polarised a *leakage current* is also observed which can be divided in *surface current* and *bulk current*. The latter is due to electron-hole pairs thermally generated in the depleted zone and is therefore directly proportional to the depleted volume V. Hence, given Eq 2.6, the contribution of this component rises with $\sqrt{V_\mathrm{b}}$ and saturates when V_fd is reached. In addition, the bulk current I_b has a strong dependence on the temperature T according to:

$$I_\mathrm{b} \propto T^2 \exp\left(-\frac{E_\mathrm{g}}{2k_\mathrm{B}T}\right). \tag{2.14}$$

which could lead to an increase of the leakage current even after full depletion, due to the self heating of the sensor. When the depleted region reaches the wafer surface an additional contribution to the leakage current emerges. This surface current is usually small compared to the bulk current and does not depend on V_b. If, increasing the bias voltage, the electric field at the pn-junction reaches critical values, the charge carriers can gain enough energy to create further electron-hole pairs leading to an avalanche multiplication that causes and exponential increase of the leakage current. This phenomenon is called *breakdown* and defines the operational voltage limit of a sensor. An early breakdown can be due the quality of the processing at the Si-SiO$_2$ interface and edge defects from the dicing inducing high electric field regions. The overall leakage current also contributes to the noise of the detector and can become critical after the sensor irradiation as discussed in Section 2.2.2.

2.2 Radiation damage

Particles penetrating the silicon sensor can also have non-ionising energy loss through scattering with the atoms of the crystalline lattice. A damage can be produced by these interactions both in the silicon bulk and in the interface with the SiO$_2$ layer, deposited on the sensor surface for protection. The resulting defects created in the sensor are classified as *bulk defects* or *surface defects*, respectively. Surface defects create a positive charge density on the sensor surface which attracts electrons leading to a compensation of the doping between the pixel implants.

This has to be taken into account in the sensor design to avoid for example that changes in the oxide influence the detector performance, resulting in a decreased inter-pixel resistance [88].

Bulk defects are instead the main cause of performance deterioration for silicon detectors in high energy physics experiments. These are produced by high energetic particles which interact with the nuclei of the silicon atoms. If the colliding particle transfers an energy larger than 25 eV to the nucleus [89], this can be displaced from its original position in the lattice creating a not reversible defect which can be charged and hence change the electrical properties of the material. As a result of this displacement a vacancy is left in the crystal lattice and the recoiling atom can either move to an interstitial lattice position or travel in the crystal displacing other atoms and creating further point-like defects. In case the transferred energy exceeds 2 keV, the atoms lose most of their energy in a localised area at the end of their path in the lattice, leading to so-called cluster defects [90]. The formation of these complex defects produces new energy states located deeply in the band gap which act as generation and recombination centres.

2.2.1 The NIEL scaling hypothesis

Since neutral and charged hadrons interact differently with the silicon lattice, the resulting bulk defects depend on the radiation type. To obtain an absolute measure of the radiation damage the Non-Ionizing Energy Loss (NIEL) scaling hypothesis is used [91], which assumes a correlation of the amount of displacement damage with the energy transferred in the collision, independently of the particle type or interaction process. Hence, for each particle and energy it is possible to define a *hardness factor k* which scales the displacement-damage integrated over the energy spectrum, to the equivalent one for mono-energetic 1 MeV neutrons. The final measure of the irradiation dose is then given in equivalent fluence of 1 MeV neutrons which would create the same damage:

$$\Phi_{\text{eq}} = k\Phi = k \int \Phi(E) \, \mathrm{d}E \tag{2.15}$$

All measured fluences in this thesis are expressed in 1 MeV equivalent neutrons according to the NIEL hypothesis, therefore in the following the symbol Φ is used as substitute of Φ_{eq}. However, deviation from the NIEL hypothesis were observed for oxygenated silicon [92], hence the irradiation type is always specified for the performed irradiations.

2.2.2 Impact on sensor performance

Bulk defects in reversly biased silicon sensors lead to three main effects: change in doping concentration, leakage current increase and charge trapping.

Doping concentration

Most of the bulk defects induced by radiation behave as acceptors and can change the initial effective doping concentration $N_{\text{eff},0} = N_{\text{D}} - N_{\text{A}}$ of the silicon. The resulting effective doping concentration N_{eff} can be expressed as a function of the fluence according to the following parameterization [93]:

$$N_{\text{eff}}(\Phi) = N_{\text{D}}e^{-c\Phi} - N_{\text{A}} - b\Phi, \tag{2.16}$$

where c is the donor removal constant and b is the acceptor creation rate. While in p-type silicon the exponential term is negligible, since $N_{\text{A}} \gg N_{\text{D}}$, in n-type silicon the acceptor-like
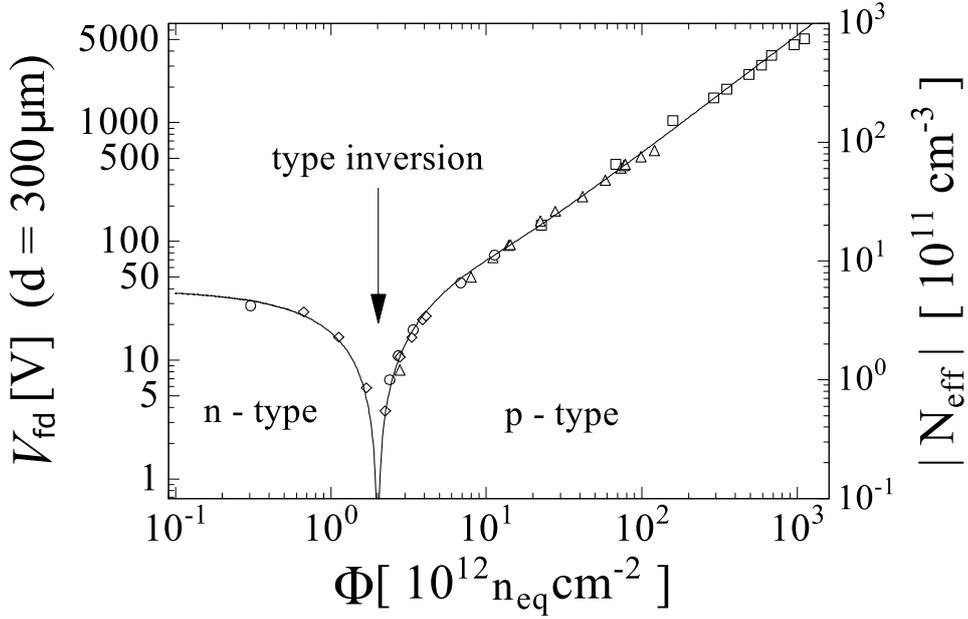
Figure 2.5: Type inversion in the n-type silicon pixels of ATLAS. The effective doping concentration and the corresponding full depletion voltage are shown as a function of the fluence. Image adapted from Ref. [93]

defects can compensate the donor concentration up to the inversion of the bulk into an effective p-type. For the n-in-n pixel sensors of the original ATLAS pixel detector this inversion was observed for fluences around 1–$3 \times 10^{13}\,\mathrm{n_{eq}/cm^2}$, as shown in Figure 2.5.

As a consequence of the rise in the acceptor concentration, the full depletion voltage also increases with the fluence and can be calculated substituting $N \to |N_{\mathrm{eff}}(\Phi)|$ in Eq. 2.6 as:

$$V_{\mathrm{fd}}(\Phi) \cong \frac{e}{2\epsilon}|N_{\mathrm{eff}}(\Phi)|d_{\mathrm{b}}^2 \qquad (2.17)$$

Leakage current increase

Defects which create energy levels close to the middle of the band gap act as generation centres increasing the probability for electrons to be excited into the conduction band. This leads to an increase of the leakage current ΔI generated in the active volume of the semiconductor V which is proportional to the fluence:

$$\frac{\Delta I(\Phi)}{V} = \alpha \Phi \qquad (2.18)$$

Here α is the *current-related damage rate*, which is independent of the initial resistivity of the silicon, the dopant concentrations and the type of irradiation [94]. As discussed in Section 2.1.4, the leakage current in the sensor depends also strongly on the temperature. Hence, after high irradiation doses, the increase of the leakage current can lead to the heating of the sensor and a consequent *thermal runaway* that would destroy the junction. To avoid this effect the detectors need to be properly cooled.

Trapping

Charged defects in the silicon bulk constitute trapping centres which can hold charge carriers during the collection time, thus reducing the signal in the detector. Accordingly, the resulting collected charge Q becomes also a function of the fluence and can be calculated by:

$$Q(\Phi) \cong Q_0 \exp\left(-\frac{t_c}{\tau}\right) \quad \text{with} \quad 1/\tau = \beta_T \Phi \tag{2.19}$$

where Q_0 is the full collected charge (i.e. the signal before irradiation), t_c is the collection time and τ is the trapping time. The latter is a linear function of the fluence with a coefficient β_T that depends on the charge carrier type and also on the particle type (neutron or charge hadrons) used for the irradiation [95]. Even if the effective trapping times for electrons and holes are similar, the collection time for holes is almost three times as large due to their different mobility ($\mu_e=1350\,\text{cm}^2/(\text{V\,s})$ and $\mu_e=480\,\text{cm}^2/(\text{V\,s})$ at $300\,\text{K}$). Hence, due to the configuration of the weighting field discussed in Section 2.1.3, silicon pixel detectors employing electron collecting electrodes have better performance after high irradiation. Trapping becomes the dominant effect for fluences above $10^{15}\,\text{n}_{eq}/\text{cm}^2$ and therefore is expected to be the main limiting factor for pixel sensors at the HL-LHC reducing the Charge Collection Efficiency (CCE) which is defined as the ratio of the collected charge Q to the collected charge Q_0 measured at full depletion before irradiation:

$$\text{CCE} = \frac{Q}{Q_0}. \tag{2.20}$$

2.2.3 Annealing

The previously described point-like and cluster defects created in the silicon bulk by radiation are not static, but they can move freely in the lattice reacting with other defects or impurities and recombining or forming new defect structures. The evolution in time of the defects, known as *annealing*, has a strong dependence on the temperature. The effect of an annealing on the damage rate constant for different temperatures, shown in Figure 2.6, is always beneficial and leads to a consequent decrease of the leakage current. On the other hand, the change of the effective doping concentration with the annealing time, illustrated in Figure 2.7, is characterised by an initial short term beneficial annealing, of the order of few days, and a subsequent long term reverse annealing. These two phases have a direct effect on V_{fd} and therefore on the charge collection for particle detection. In particular, for p-type sensors, V_{fd} decreases during the beneficial annealing and increases again during the reverse annealing. Due to this behaviour, irradiated sensors are usually intentionally kept at room temperature (or higher temperatures) for short and monitored periods of time, but they have to be maintained at temperatures lower than $0\,°\text{C}$ both during storage and operations to avoid a further degradation of their performance.

2.3 Pixel sensors

To obtain an unambiguous two dimensional information of the particle impact point, the electrodes of semiconductor sensors are segmented in several cell structures. If both dimensions of the cells are small (i.e. around $500\,\mu\text{m}$ or less), these are usually called *pixels* and the sensor is called a *pixel sensor*. Planar pixel sensors are produced from an initial lightly doped silicon bulk material with two subsequent heavily doping implantations (n^+ and p^+) on the two
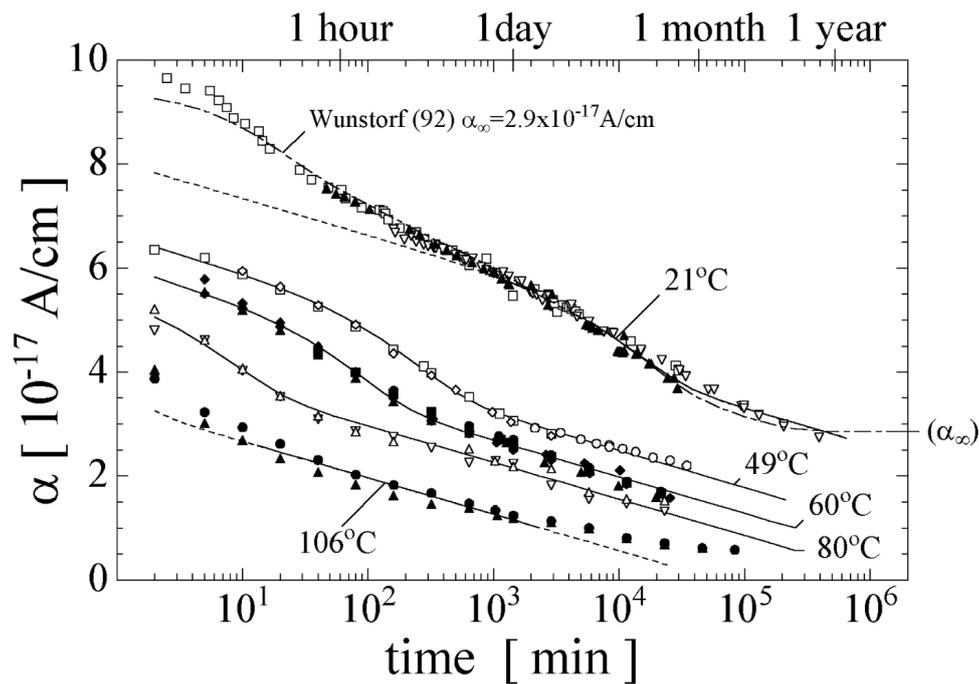
Figure 2.6: Change of the damage rate constant α with the annealing time at different temperatures [94].
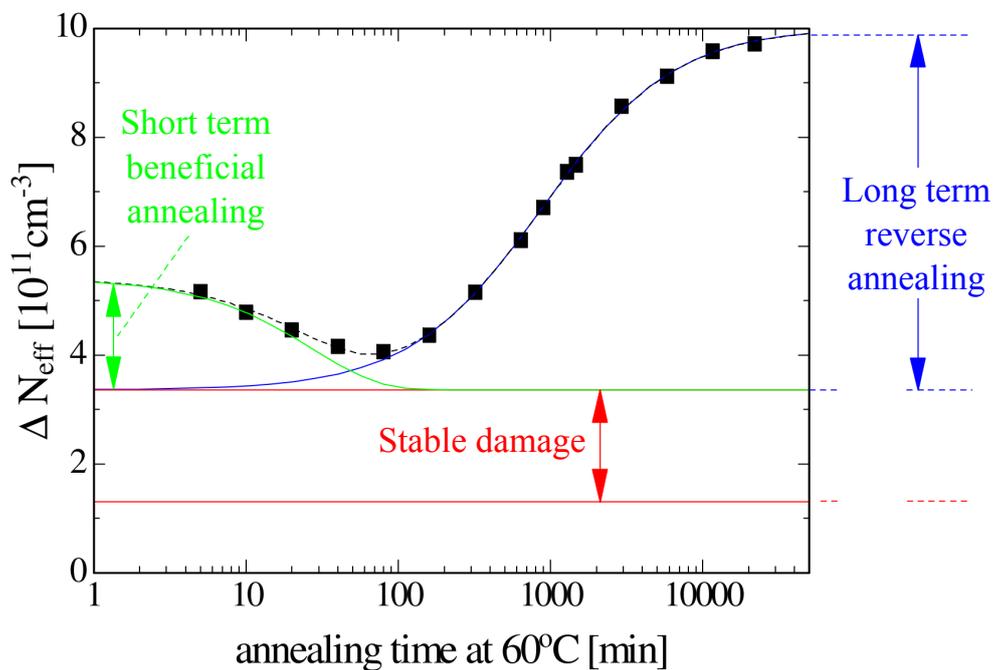

Figure 2.7: Effect of the annealing at $60\,^{\circ}\mathrm{C}$ on the effective doping concentration. On top of a stable damage effect (red), the beneficial annealing is shown in green and the reverse annealing in blue. Image adapted from Ref. [94].

opposite sides, as illustrated in Figure 2.8. First the polished surface of the silicon wafer is covered with a thin layer of SiO_2 and a photolithography mask is used to partially etch this oxide for the subsequent n^+ implantation defining the pixel electrodes. The backside is then implanted with Boron to form an ohmic contact. The implanted ions undergo an annealing step at high temperatures, around $1000\,°C$, to be electrically activated. Successively, silicon nitride and LTO (Low Temperature SiO_2) are deposited on the front side and contacts are formed through these layers to the implants. An aluminium layer is deposited and patterned on the front side, and a passivation layer (usually polyimide or low temperature SiO_2) is applied to isolate and protect the sensor surface.

(a) Thermal oxidation   (b) Photoresist for implant   (c) Developing of the photoresist

(d) Etch oxide for implantation   (e) Implantations   (f) Metallisation
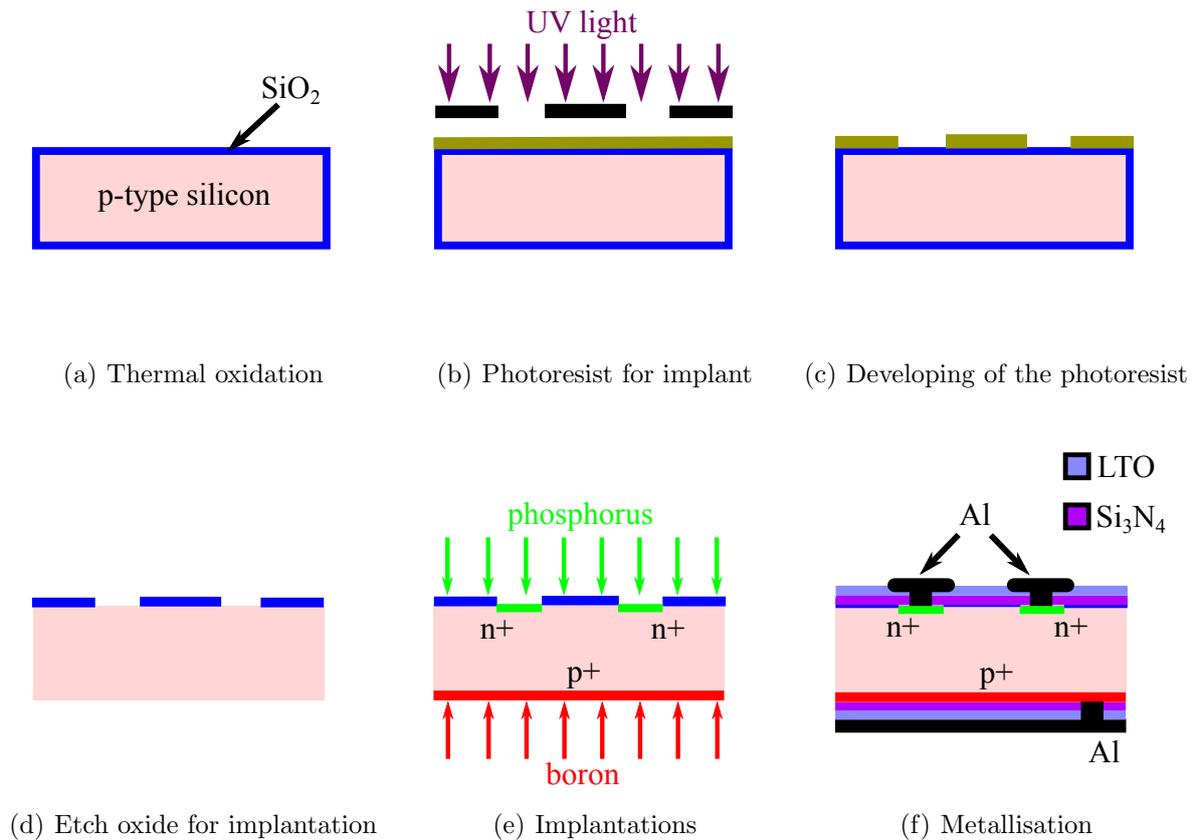
Figure 2.8: Main production steps for a planar n-in-p silicon pixel sensors.

2.3.1 Sensor concepts

Four combinations of substrate and electrode dopings are possible, which can be suitable for different applications. For pixel sensors employing p^+-pixel implants, the signal is mainly generated by the hole drift, due to the higher weighting field close to the electrodes (see Section 2.1.3). Since the mobility of holes in silicon is three times lower than for electrons, these pixel sensor designs are not suitable for high radiation fluences when trapping effects becomes significant. Hence, in high energy physics experiments, where radiation hardness is a fundamental requirement, the pixel sensor technology has to profit from the higher charge

mobility of the electrons using n$^+$-pixel implants. Two configurations, illustrated in Figure 2.9, are thus possible: the so-called *n-in-n* technology, where n$^+$-doped pixels are implanted in an n-type silicon substrate, which is the sensor technology presently used for planar pixel sensors in ATLAS; or the *n-in-p* technology where n$^+$-doped pixels are implanted in a p-type silicon substrate.
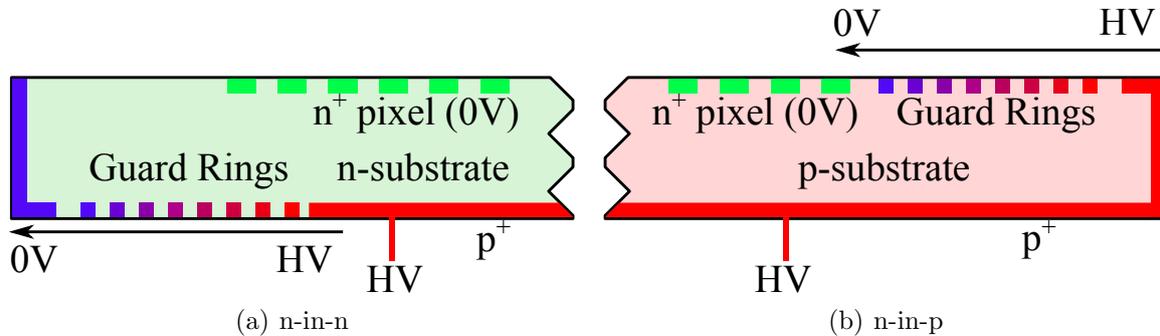
Figure 2.9: Comparison of the n-in-n (a) and n-in-p (b) planar sensor technologies. Image adapted from Ref. [79].

The n-in-n concept

In this configuration the pn-junction is located on the backside. Thus, additional processing steps to pattern the backside are necessary to implement protecting structures around the p$^+$ implantation (see Section 2.3.2). Before irradiation the depletion starts from the backside and until the depleted region reaches the pixel implants, these are shorted together by the conductive bulk. In these conditions, the detector cannot be operated partially depleted. Moreover at full depletion the electric field is lower closer to the segmented side where, instead, the weighting field is higher and the movement of the electrons induces most of the signal. However, since the bulk is n-type, after high radiation fluence this is subject to type inversion and therefore the junction moves to the pixel side and the sensor can be operated even strongly under-depleted.

The n-in-p concept

In n-in-p pixel sensors the pn-junction is located on the pixel implant side and therefore only one single-sided structured processing of the wafer is necessary. This makes this kind of technology potentially cost effective and therefore particularly interesting when large areas, of the order of $1\,\mathrm{m}^2$ or more, need to be covered. Additional advantages of this design are also the starting p-type bulk which is not subject to type inversion and the depletion that always starts from the pixel implant side.

2.3.2 Additional structures

The final pixel sensor is completed by a series of different structures which are described in the following.

Guard rings

The cutting edge of the sensor is conductive due to the damage induced by the mechanical cutting procedure. If the depleted region extends up to this cutting edge, the high electric field causes a sudden increase of the leakage current that leads to the breakdown of the junction. Hence, the edges of the sensors have to be protected with dedicated structures called *guard rings*. These are additional ring implantations around the active area, at the edges of the sensor surface, implemented to ensure a smooth drop of the potential from the pn-junction to the cutting edge. The number and the shape of the guard rings is crucial for the breakdown properties of the sensor. While in n-in-n sensors the guard rings are placed on the backside and the entire edge is therefore kept at ground potential, in n-in-p sensors these are on the pixel implant surface and thus the edge is at the backside potential. In the latter case, for hybrid pixel detectors, the maximum bias voltage that can be applied to the sensor is limited by the risk of sparks between the sensor edge and chip surface that could damage permanently the detector. Possible remedies employ additional insulation layers between sensor and chip.

Biasing structures

In experiments like ATLAS for which a large number of silicon modules is required, a high production yield is a fundamental requirement for limiting the costs. To optimise the module production process and select the best sensors, dedicated biasing structures are implemented which allow to measure the electrical properties of the pixels before interconnection. For the sensors described in this thesis, the *punch through* mechanism is used. All pixels are connected through a common implant around the active area of the sensor, called *bias ring*, and a metal *bias rail*, as shown in Figure 2.10. The connection between the bias rail and the pixel implant is realised with a separate circular implantation (*bias dot*) located within the pixel cell. When the depleted zone encloses both implants, the grounded bias dot and the pixel body at floating potential, which are close but not at contact, the floating implant follows the potential of the grounded one. This effect, called punch through, is used twofold: to ensure a common potential for eventually disconnected pixel cells and, at the same time, to ground all pixels with just one connection allowing the characterisation of the full sensor before interconnection as described in Section 4.3. Since neither the bias dot nor other bias structures are connected to the readout, the signal induced in their proximity is partially lost. To maximise the signal, the size of these structures as well as the distance of the bias dot to the pixel implant has to be reduced as much as possible within the limitations of the production process. Especially after irradiation, due to the decrease of the CCE, these structures can represent a critical area for the inefficiency of the detector.

Inter-pixel isolation

The positive charges of the oxide attract electrons which accumulate between the pixel implants. When n^+ implants are used for the segmented side of the sensor, this electron layer creates a short of all pixels. The three available solutions to this problem are shown in Figure 2.11. The first consists of applying a further p^+ implantation between the n^+ pixels (*p-stop*). This technique requires an additional photolithographic step in the production with a critical alignment procedure needed to avoid the superposition of the two implants. Moreover, after irradiation, since the positive charges in the oxide increment, also the potential difference between p-stop and the pixel increases, resulting in a lower breakdown voltage [96]. The second

(a) Edge   (b) Pixels
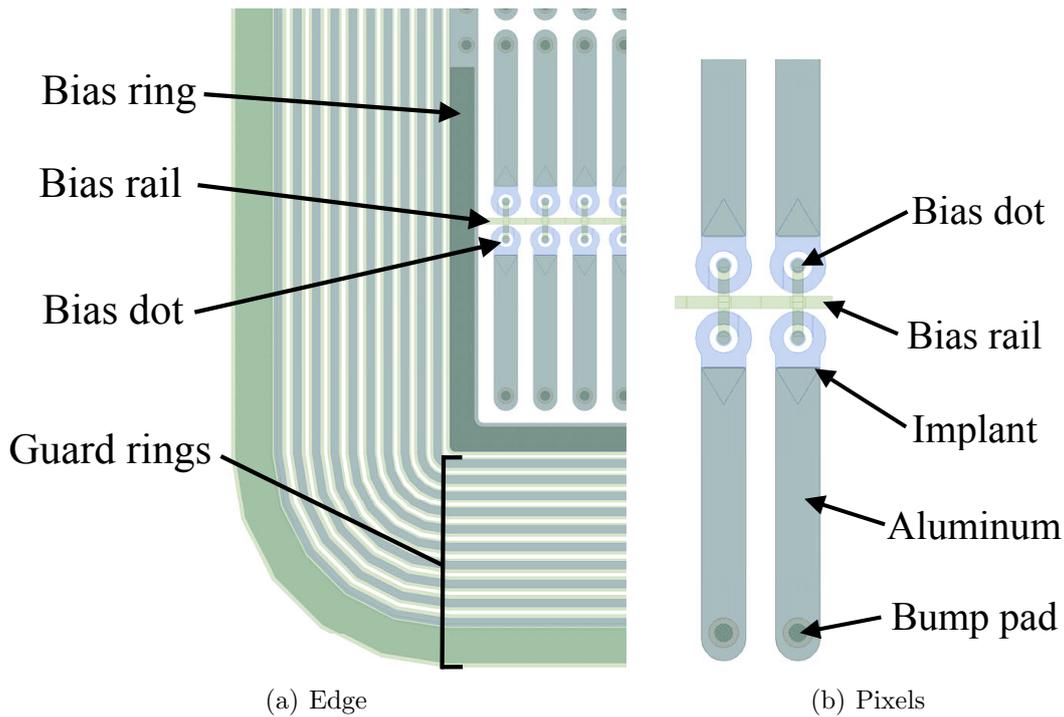
Figure 2.10: Standard layout of a silicon pixel sensor. The edge of the sensor is shown in (a), while (b) shows the structure of the pixel cells in detail. The guard rings and the biasing structures are indicated as well as other main structures of the pixel cell.

solution consists of a low dose of p-implantation, called *p-spray* isolation. The dose is chosen to be low [97] to avoid high electric fields close to the n^+ implants. This solution has several advantages with respect to the p-stop approach: it allows for lower pixel dimensions and it does not require a second mask with the consequent alignment problems. The third solution combines a moderated dose of p-spray with the p-stop approach. Here a region with a higher p-spray dose is created by etching the silicon nitride layer in a narrow line at the centre between the pixel implants, thus allowing more boron ions to reach the silicon bulk.

(a) p-stop   (b) Homogeneous p-spray   (c) Moderated p-spray
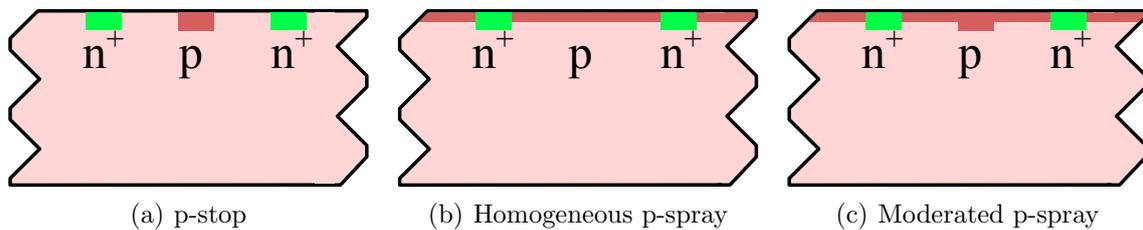
Figure 2.11: Schematics of the inter-pixel isolation techniques for n-in-p sensors [79]. The p-spray, represented in red in (b, c), is implanted on the entire sensor surface including the n^+ implants. For the moderated p-spray approach shown in (c), a narrow region with a higher p-spray dose is created in the centre between two pixel implants by etching of the silicon nitride layer.

2.4 Hybrid pixel detectors

In contrast to monolithic pixel detectors, where part of the electronics are embedded in the sensor, in hybrid pixel detectors the sensor and the chip are produced separately and interconnected through *flip chipping*. This technique consists of small solder *bump bonds* (indium or lead-tin) deposited on the contacts of the readout chip on which the sensor is placed. A reflow solder process is used to melt the bumps and create the electrical connection between each channel of the readout chip and its facing pixel on the sensor. This hybrid pixel technology is very important at hadron colliders since it allows to optimise each of the two detector parts independently to obtain at the same time high spatial resolution, timing precision and, most important for long term operations, radiation hardness.

3 The ATLAS pixel modules

The ATLAS pixel detector consists of four barrel layers. The three outermost layers, together with the six end-cap disks, form the original pixel detector which operated in Run 1. This is composed entirely of FE-I3 silicon planar modules. The new IBL, introduced in the LS1, is instead composed of two kind of modules employing a new readout chip, the FE-I4, and two different silicon sensor technologies. In the central region, up to $|\eta| \sim 2.8$, the staves host n-in-n planar sensors while at $2.8 < |\eta| < 3.0$ the 3D sensor technology is used. This pixel technology is also one of the candidates for the future pixel detector together with thin silicon planar sensors and diamond sensors as stated in the Letter Of Intent (LOI) for the ATLAS Phase II [75]. This chapter is dedicated to the module technologies of present and future upgrades of the ATLAS pixel detector. In the first two sections the characteristics of the readout chips and of the sensor technologies of the original ATLAS pixel detector and of the IBL are described. Section 3.3 presents the new module concept designed at the Max-Planck-Institut für Physik (Werner-Heisenberg-Institut) (MPP) [98, 99] in collaboration with the Halbleiterlabor der Max-Planck-Gesellschaft (MPG HLL) for the ATLAS Phase II at HL-LHC, which is the main subject of the investigations presented in this thesis.

3.1 Readout chips

Two different readout chips, the FE-I3 and the FE-I4, are presently used for pixel modules in the ATLAS detector which are compared in Figure 3.1. The same chips are also used in module prototypes designed for Phase II investigations. Their different characteristics are discussed in the following.

3.1.1 FE-I3

The ATLAS FE-I3 [62] (on the left in Figure 3.1) is a front-end chip produced in a 250 nm Complementary Metal Oxide Semiconductor (CMOS) technology with an active area of $(7.2 \times 10.8)\,\mathrm{mm}^2$ which contains 2880 pixel channels arranged in 160 rows and 18 columns with a pitch of $(50 \times 400)\,\mathrm{\mu m}^2$. Each pixel channel has an analogue and a digital part. In the analog part the charge signal is amplified and compared to a programmable threshold. In the digital part the pixel address and the times when the rising edge and the falling edge of the signal cross the threshold are registered. The pixel columns are connected in pairs to a buffer at the periphery of the chip where the digitised information is transferred and collected. In this area of the chip, called End-Of-Column (EOC), the Time over Threshold (ToT) is calculated and stored in an 8-bit register. The hit data are then matched to the trigger signal and transmitted serially out of the chip. Since the discharge of the feedback current in the analog amplifier is approximately linear, the pulse height is proportional to the ToT, which is thus used to measure the collected charge. Close to the EOC, a series of wire-bond pads provide contacts for powering the analog and the digital parts of the chip and for its communications.
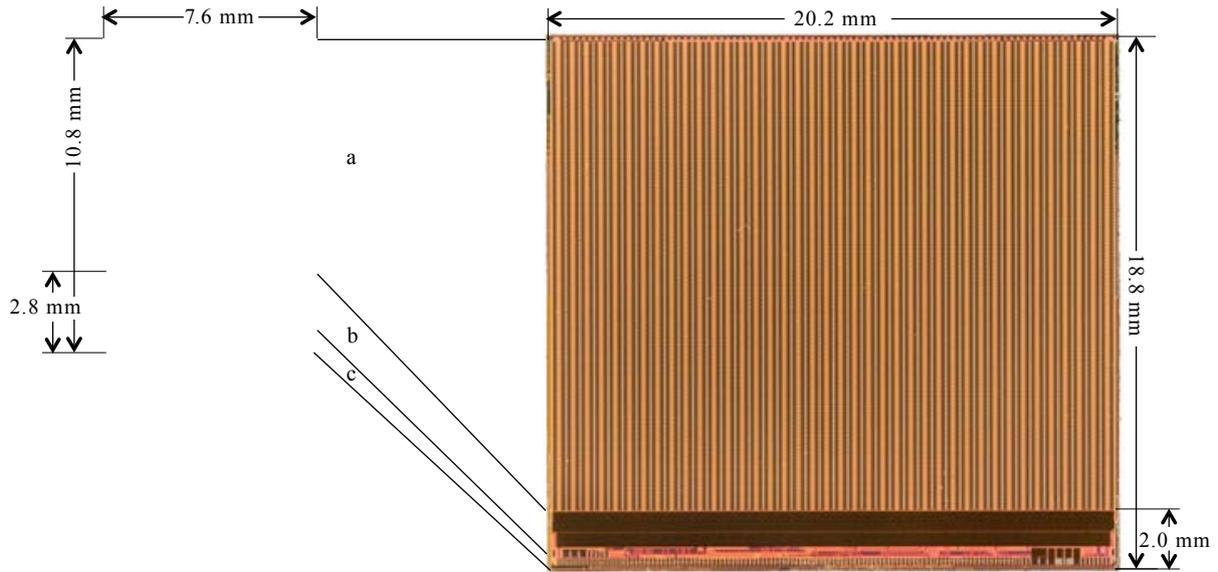
Figure 3.1: The ATLAS readout chips. The three different sections, the pixel active area (a), the EOC (b) and the bonding pads (c) are indicated for the FE-I3 (left) and FE-I4 (right) chips. Image adapted from [100].

To fulfil the ATLAS requirements, the FE-I3 has a clock speed of 25 ns, which matches the nominal LHC frequency, and was designed to be radiation hard up to $10^{15} \, \mathrm{n_{eq}/cm^2}$ [35]. For the calibration of the ToT response and the adjustment of the threshold settings, the chip is provided with an analog injection circuit schematised in Figure 3.2. This allows to inject a test charge up to 100 ke [101] using a single capacitor C_{lo}, or even larger changes, but with worse precision, selecting two capacitors in parallel $C_{\mathrm{lo}} + C_{\mathrm{hi}}$. The specified minimum threshold for the standard ATLAS multi-chip modules is 4 ke, but for single chip modules, lower thresholds, down to 1.5 ke, have also been achieved. Multi-chip modules need an additional Module Controller Chip (MCC) [102] to coordinate the operation of the different chips.
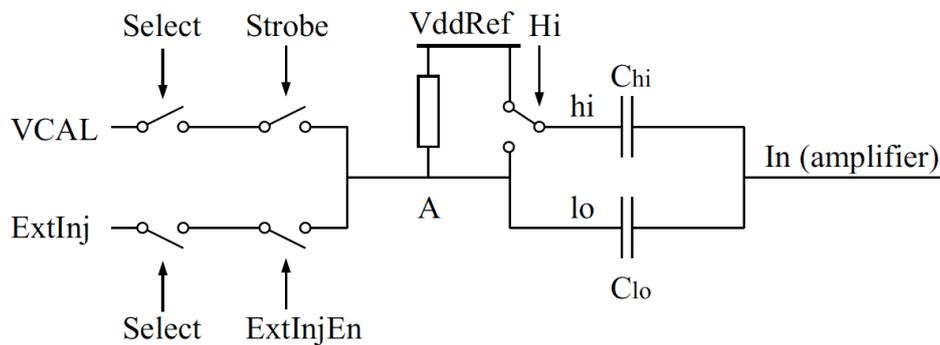
Figure 3.2: The injection circuit (chopper) of the FE-I3 pixels [103].

FE-I2

A previous version of the FE-I3 ATLAS chip, the FE-I2 [104], was also employed on module prototypes used for comparison in this thesis. This chip only differs for minor details from the FE-I3, such as slightly different operational voltages, which are not relevant for the presented results.

3.1.2 FE-I4

The FE-I4 front-end chip [61] was designed to fulfil the requirements for the IBL in terms of radiation hardness, occupancy and rate capabilities. It is produced in the $130\,\text{nm}$ CMOS technology which allows for an improved radiation hardness up to $5 \times 10^{15}\,\text{n}_\text{eq}/\text{cm}^2$ and an optimal power distribution over long columns. The active surface of the chip can be therefore larger than in the FE-I3 allowing to reduce the flip chipping costs and minimise the module overlap close to the beam pipe. The active part of the chip measures $(16.8 \times 20.2)\,\text{mm}^2$ and contains 26880 pixel channels in a matrix of 80 columns by 336 rows. Each pixel has a dimension of $(50 \times 250)\,\text{µm}^2$ and, as for the FE-I3, consists of an analogue and a digital part. The analog part contains the amplifier for the charge signal and the comparator, and is optimised for low power consumption and low noise which allows to set the threshold to values as low as $1\,\text{ke}$ in the case of single chip modules. The digital part is instead shared among four pixels channels. Here, differently from the FE-I3, the hit information is processed in a local buffer where the ToT is computed and stored in a 4-bit register. The trigger signal is also forwarded to this digital block and data are transmitted to the EOC only when in time with the trigger. This structure allows to optimise the bandwidth usage and thus the readout speed for the larger number of channels of the FE-I4 chip with respect to the former FE-I3 chip. In the FE-I4, the EOC is also used to manage the operation of multi-chip modules without the need of a separate MCC. On the side of the chip, protruding from below the sensor, wire-bond pads for communication and powering are implemented. Also this chip version is provided with an analog injection circuit consisting of two capacitors C_lo and C_hi which can be selected singularly or in parallel for a total capacitance value $C_{\text{in}j} = C_\text{hi} + C_\text{lo}$ which is the one usually used for tuning and calibration.

FE-I4A and FE-I4B

Two versions of the FE-I4 chip were designed which are both relevant for this thesis: a first prototype, the FE-I4A, designed and produced for testing purposes, which has been largely used also for characterisation of sensor prototypes; and the final version of the chip, the FE-I4B, presently employed in IBL pixel modules. In the FE-I4A, different circuit configurations were implemented for some of the columns which were subsequently evaluated to define the best solution then adopted in the FE-I4B chip [107]. In particular, a different injection mechanism is used for the columns at the edge of the chip that are therefore frequently masked, due to their problematic tunability and their consequent high noise level. Another difference between the two chips is the possibility to access and measure the value of the injection capacitances on wafer which is implemented in the FE-I4B version of the chip, but not in the FE-I4A version. Additional minor differences are present, which are not relevant for the understanding of the results presented in this thesis, and are therefore omitted. A complete list of changes between the two chip versions can be found in Ref. [106].
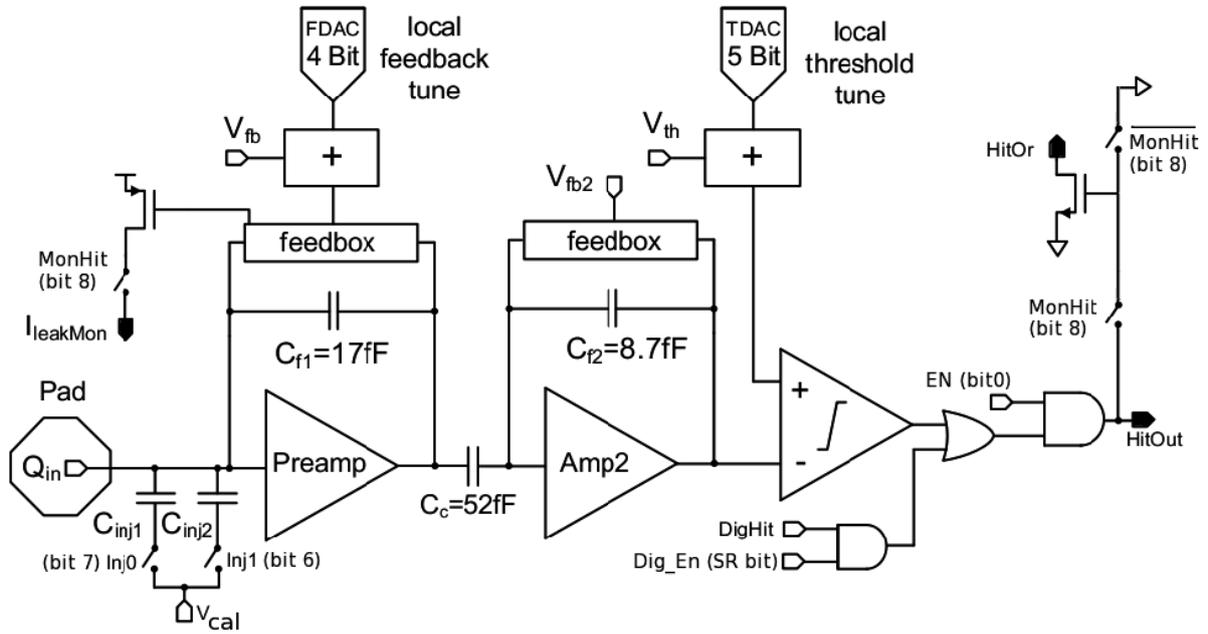
Figure 3.3: The analog circuit of a pixel in the FE-I4 chip [105,106].

3.2 Sensor technologies

Two silicon pixel sensor technologies featuring a different electrode geometry are used in the ATLAS pixel detector: n-in-n planar sensors and n-in-p 3D sensors. In this section the characteristics of both these technologies as implemented in the present ATLAS modules are presented.

3.2.1 Planar sensors

In a planar pixel sensor the electrodes are parallel to the bulk surface and the pixel cell is defined by the size of the implantation on the frontside. This is the most common geometry for pixel sensors and it is largely employed in high energy physics experiments.

The FE-I3 sensors

The pixel modules of the three outer barrel layers of ATLAS, which composed the original pixel detector before the IBL insertion, consist of n-in-n planar silicon sensors with an active thickness of $250\,\mu m$. The bulk is made of oxygenated Float Zone (FZ) silicon and the inter-pixel isolation is obtained with moderated p-spray. The full sensor has a sensitive area of $(16.4 \times 60.4)\,mm^2$ which contains 328×144 pixel cells with a pitch of $(50 \times 400)\,\mu m^2$ (except for 16 columns with pitch of $(50 \times 600)\,\mu m^2$). This arrangement is such that each sensor can be connected to 16 FE-I3 chips. The first and the last 8 rows of pixels at the edge of the sensor are the so-called *ganged* and *inter-ganged pixels*, which are connected in pairs to the same readout channel of the chip. The sensor is provided with a biasing structure that connects all pixels to a common bias ring by employing a bias dot for each cell as described in Section 2.3.2. The potential drop at the sensor edge is controlled through a guard ring structure consisting of 22 rings placed on

the sensor backside. Due to these structures, the dead region between the last pixel implant and the pixel edge is of about d_e=1.1 mm.

The IBL sensors

The same n-in-n planar technology with oxygenated FZ silicon is employed for the pixel sensors in the central part of IBL, but for the reduced bulk thickness of 200 μm. The pixel cells have a smaller pitch of (50×250) μm² and are isolated with moderated p-spray. With respect to the planar sensors of the other layers, the active area at the edge is extended by reducing the guard ring structure on the backside to 12 rings and shifting them under the long side of the pixel implants as shown in Figure 3.4. This results in d_e=200 μm for the columns direction (i.e. the long side of the pixel pitch) and d_e=450 μm in the row direction (i.e. the short side of the pixel pitch). The sensors are designed as double chip sensors with an active size of (16.8×40.9) mm² and are interconnected to two FE-I4 chips. To ensure the necessary space for the guard ring shift and the placement of the two neighbouring chips, two columns at the edge and two columns in the middle of the double chip sensors have a longer pitch of (50×500) μm².
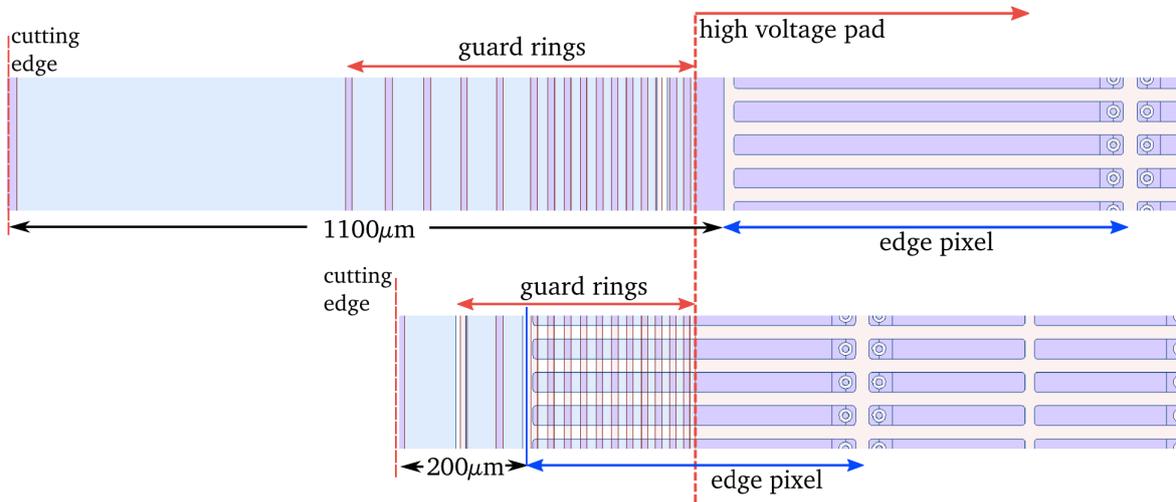
Figure 3.4: Comparison of planar sensor edge designs of the original pixel detector (top) and of IBL (bottom) in which the guard ring reduction and the last pixel implant, on the frontside, above the guard rings, on the backside, lead to an increase of the active area [100].

3.2.2 3D sensors

The 3D concept was first proposed in 1997 by Parker and Kenny [63] and consists of placing the electrodes perpendicular to the pixel surface instead of parallel, as in the case of standard planar sensors. This is realised etching narrow columns trough the active bulk of the silicon and doping them, usually by diffusion. The electric field is generated between the n$^+$ and p$^+$ columns with the collecting electrodes surrounded by the opposite doped electrodes which define the pixel cell. As shown in Figure 3.5, this design allows to decouple the drift length from the active thickness such that the collection distance between the electrodes can be reduced without affecting the charge signal for charged particles crossing the full bulk thickness. The result

is a radiation hard sensor with a low depletion voltage and a high average electric field. The main drawback of this technology is the low production yield due to the complex processing (about 60 % for the IBL production [108]). The column implants can traverse completely or only partially the bulk thickness. While in the former case a particle traversing the sensor orthogonally to its surface through one of the columns, does not produce electron-hole pairs, for partially penetrating columns a small signal can be still obtained in the last part of the active bulk at the end of the column implant.

(a) Planar n-in-n

(b) 3D n-in-p
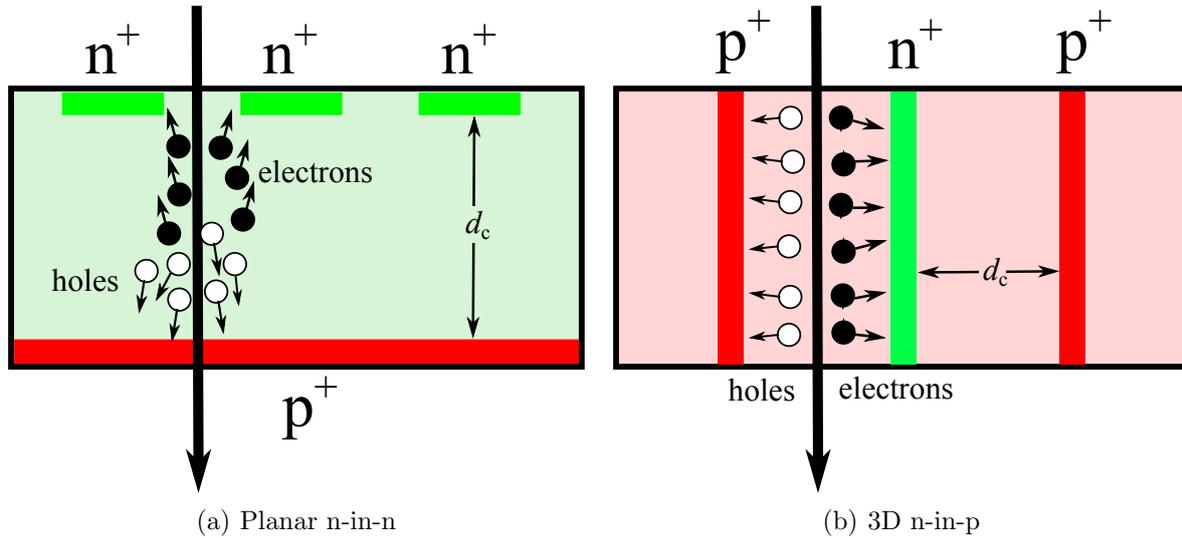
Figure 3.5: Comparison of the design and the charge collection properties of planar (a) and 3D sensors (b). The collection distance is indicated by d_c and is 200 μm for the present n-in-n planar sensors of IBL and about 67 μm for 3D sensors.

In the ATLAS pixel detector, 3D sensors with a 230 μm thick bulk of p-type FZ silicon are employed as single chip sensors in the high-η region of the IBL [109]. The choice of the p-type substrate is preferred to avoid type inversion after high radiation fluence. The pitch of the pixel cells is (50×250) μm^2, matching the geometry of the FE-I4 chip to which the sensors are interconnected. Each pixel cell has the so-called 2E layout consisting of two n$^+$ collecting electrodes surrounded by six p$^+$ columns, leading to a charge collection distance of about 67 μm. Sensors with both partially and fully passing columns are employed which have been fabricated at the Centre Nacional de Microelectrònica (CNM) [110] and at the Fondazione Bruno Kessler (FBK) [111], respectively (see Figure 3.6). For CNM sensors the implants reach a depth of about 200 μm inside the bulk, leaving 30 μm of remaining active length. Another difference between the two designs is the surface isolation between the columns which is obtained by a p-spray layer on both sides for FBK sensors and with p-stops for CNM sensors. Both sensor types have a slim edge design with d_e=200 μm.

3.3 A module concept for Phase II

The HL-LHC upgrade represents a big challenge for silicon pixel detectors. The pixel technology presently implemented in the ATLAS inner detector will be insufficient to cope with the high particle density and the harsh radiation environment expected, thus the development of new

| oxide | metal | passivation |
| p⁻ Si | p⁺ poly-Si | n⁺ poly-Si | p⁺ Si |

(a) CNM

| oxide | metal | passivation |
| p⁻ Si | p⁺ Si | n⁺ Si |

(b) FBK
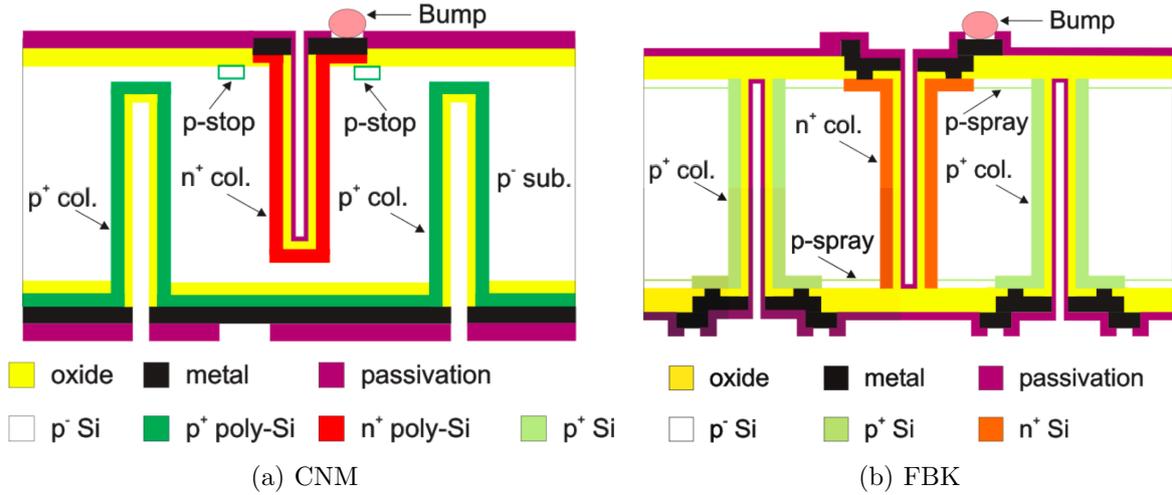
Figure 3.6: The two 3D sensor technologies employed in IBL [100]. (a) shows the CNM design with partially passing column implants and (b) shows the FBK design with fully passing column implants, both sensors are 230 μm thick.

pixel modules is necessary. In addition to occupancy and radiation hardness, the layout of the future pixel detector imposes strict requirements for the module design. The innermost layer will be as close to the beam pipe as the present IBL layer, therefore, the modules cannot overlap in the z direction due to space constraints, and slim edge sensors are an essential requisite to reduce as much as possible the inactive areas. Moreover the full tracker will be made of silicon and a larger area will have to be covered by the outer pixel layers, which demands for a cost-effective module production. Another important specification is a reduced material budget of the full pixel detector structure, including the pixel modules. This is necessary to limit the amount of material in front of the calorimeters, which would degrade their energy resolution, and for improving the tracking performance reducing multiple scattering. In this thesis a novel module concept developed at MPP [98, 99] to fulfil the requirement for the pixel tracker of Phase II is investigated. Differently than the present n-in-n planar pixel sensors, the MPP prototype is based on n-in-p pixels with a thinner bulk between 75 and 150 μm and the implementation of active edges, which together with further innovations on the chip side (Through Silicon Via (TSV) and Solid Liquid Inter-Diffusion (SLID) interconnection), aims at obtaining a four-side buttable module. A comparison with the modules of the present pixel detector is shown in Figure 3.7. The different technologies developed for this concept are described in the following.

3.3.1 The n-in-p planar technology

The use of n-in-p pixel sensors is already foreseen in the LOI for Phase II [75]. This sensor technology represents a potentially cost effective alternative to the present n-in-n planar sensors, since, as discussed in Section 2.3, it requires less processing steps in the production. However, to maintain the cost advantages of the n-in-p technology, given by the single-side processing, the guard rings have to be located on the same side as the pixel implants. The cutting edge of the sensor is therefore not at ground potential, differently than in the n-in-n case. With the increase of the bias voltage, necessary to fully deplete the sensors after irradiation, this configuration

(a) Present ATLAS module

(b) MPP concept
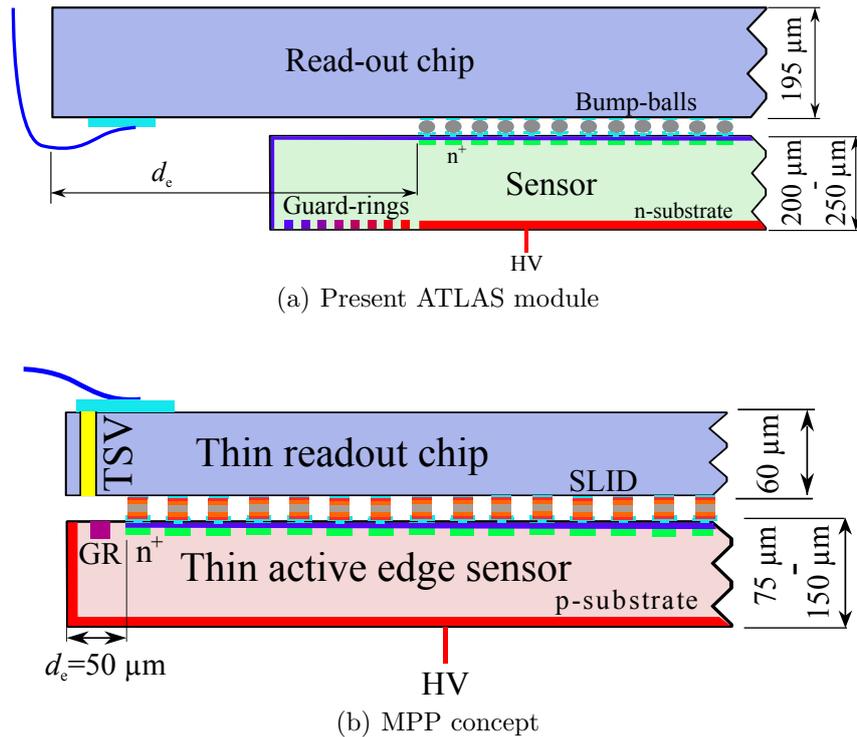
Figure 3.7: Comparison of the planar pixel sensor design presently employed in the pixel detector of ATLAS (a) and the MPP module concept (b). Images adapted from Ref. [79, 97].

may lead to sparks between the edge of the sensor, which is at the backside potential, and the readout chip that is grounded with the pixel implants. To avoid these sparks, which can permanently damage the module, a coating layer of BenzoCycloButene (BCB) or Parylene can be deposited on the sensor surface with the aim of extending the operational voltage of the sensor.

3.3.2 Thin sensors

Thin planar pixel sensors are potentially radiation hard due to the smaller distance between the collecting electrodes which counteracts the trapping effects. Thin sensors achieve the full depletion at lower bias voltage and have therefore a smaller leakage current compared to thicker pixel sensors. On the other hand the active volume at full depletion before irradiation is reduced, hence a charged particle traversing the detector thickness leads to a smaller signal. However, after the high irradiation fluences expected at HL-LHC the configuration of the electric field and the weighting potential in thin sensors is such that the corresponding signal is expected to be enhanced with respect to thicker sensors [97], resulting in a better signal to noise ratio. The higher electric field in thin sensors leads to an increase of the drift velocity of the charge carriers which reduce the collection time. Due to the saturation of the drift velocity, this effect is only relevant up to moderate voltages and is thus especially important in the low field regions of the depleted zone. Also, as the ratio between the pixel pitch and the bulk thickness decreases, the linearity of the weighting field increases and the charge carriers generated further from the pixel implants contribute more to the overall signal before being trapped. Nevertheless, the small

number of electron-hole pairs generated, which is proportional to the depleted thickness, can be a challenge for the electronics. Therefore, a compromise between the initial active thickness and the radiation hardness is necessary.

3.3.3 Slim and active edges

Due to the n-in-p layout, it is no more possible to shift the pixels behind the guard rings, which are on the frontside, to reduce the dead area at the sensor edge as in the IBL planar design (see Section 3.2). Nevertheless, the backside implantation can be extended to the edges of the sensor to create a rectifying junction reducing the defects induced by the cutting. This allows to decrease the number of guard rings and thus considerably shrink the distance between the last pixel implant and the implanted edge. Moreover, since the electric field extends up to the side implantation, the entire edge is in principle fully active in case no bias ring is implemented, which would otherwise act as a collecting electrode.

3.3.4 3D integration

To further increase the active area of the full pixel module a new three dimensional integration concept is under investigation. This consists of replacing the presently used bump bond interconnection with a SLID process and bring the signal to the backside of the chip passing through the chip itself using the TSV technology.

SLID

The SLID interconnection technique developed by the Fraunhofer-Einrichtung für Modulare Festkörper-Technologien (EMFT) [112] consists of a Cu_3Sn alloy which is formed at around $300\,°C$ and has afterwards a melting point around $600\,°C$. This technique has several advantages with respect to the solder bump-bonding process currently used for the ATLAS modules. It allows to reduce the pitch as low as $20\,\mu m$ with arbitrary and different geometries. Moreover, it requires less processing steps with respect to the bump-bonding procedure and is therefore potentially cheaper. However, it needs a good alignment precision of the structures and it does not allow for reworking. An additional drawback is the need for a wafer to wafer or chip to wafer interconnection, while a chip to chip approach that would be more flexible, is not available at the moment. A comparison of the SLID and the bump-bonding process is illustrated in Figure 3.8. The results obtained on the first pixel module prototypes employing this interconnection technique are discussed extensively in Ref. [79, 113].

TSV

The TSV technology allows to convey data and control signals through silicon devices and therefore vertically interconnect together different layers of integrated circuits [115]. In silicon pixel detectors this allows to remove the large balcony outside of the active area of the chip which is used for wire-bond pads, by performing the connection on the backside of the chip. The fixed aspect ratio of the TSV technology results in the need of thinning the read-out chips to achieve a diameter of the vias of a few tents of microns or below. Together with the active edge technology this solution allows to build pixel modules which have in principle a fully sensitive area for particle detection and can be placed near each other without overlapping. A more
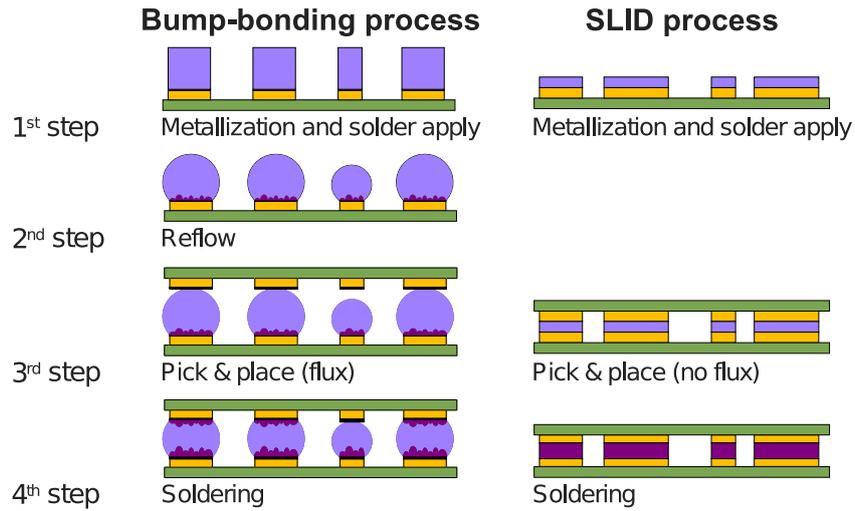
Figure 3.8: Comparison of the standard bump-bonding process (left) and the SLID interconnection technique (right). Image adapted from [114].

detailed description of the TSV process and the first attempts to realise it on FE-I2 devices are presented in Chapter 7.

4 Instrumentation and experimental methods

In this chapter the experimental setups and methods employed to obtain the results presented in this thesis are discussed. In Section 4.1, the data acquisition setups and the readout systems used to operate the pixel modules are described and in Section 4.2 the procedures for the tuning and calibration of the modules are explained. In the following sections the methods employed for the characterisation of the pixel modules are discussed: Section 4.3 and Section 4.4 describe the experimental setups located at MPP and the techniques to measure the electrical characteristics and study the charge collection properties of the sensors; Section 4.5 is instead dedicated to facilities, instrumentation and analysis methods employed to measure the module performance at beam tests. In Section 4.6 tools and algorithms used for simulations are discussed. The different irradiation facilities used to irradiate the modules to high fluences are finally presented in Section 4.7.

4.1 Data acquisition

The readout chain for the characterisation of pixel module prototypes consists of an interface to power and communicate with the front-end chip that is connected to a readout system steered by a computer, which allows for tuning and data taking operations. In this section a description of the different parts of the Data Acquisition (DAQ) systems used in this thesis is given.

4.1.1 Module interfaces

The assembled FE-I4 and FE-I3 modules are wire bonded at MPP to readout interfaces, which provide the necessary connections to match the characteristics of the respective chips. The different Printed Circuit Boards (PCBs) and flex designs adopted for measurements in this thesis are shown in Figure 4.1 and described in the following.

Single chip cards

For the characterisation of single chip modules, three dedicated PCBs, designed by the University of Bonn, allow the readout of FE-I3, FE-I4A and FE-I4B chips, respectively. All these single chip cards have a LEMO[1] connector to provide the bias voltage to the sensor and a KEL[2] connector through which both analog and digital voltages are routed together with the data stream. The FE-I4 single chip cards have in addition the possibility of routing the data stream via an ethernet cable providing analog and digital low voltages for the chip on a separate 8-pin connector. The FE-I4 board gives also the possibility of accessing the injection capacitance of the chip to perform a calibration of the injection circuit after flip chipping as described in Section 4.2.

---

[1] www.lemo.com
[2] www.kel.jp

Four-chip cards

A PCB was designed at the Liverpool University to interface at the same time four FE-I4B chips. It is equipped with a single 8-pin connector on which analog and digital voltages are routed together with the bias voltage for the sensor. The same analog and digital lines are connected to all four FE-I4 chips, while the data stream is accessed separately for each chip through four ethernet connectors. A large cutout in the centre of the PCB is designed to host sensors with different sizes thanks to selectable pitch adapters which bridge the wire bonds from the chips to the pads on the board. No access to measure the injection capacitance of the chip is provided by this PCB. This forces the user to rely on the parameters obtained from the wafer characterisation or, in case these are not available, on the average parameter values of the chip production.

FE-I4 flex

The flex is a two copper layer circuit which offers a simple and compact interface for FE-I4 chips. It was designed in different versions for single or double chip modules, corresponding to the two geometries developed for IBL. Later, this solution was adapted to four chip modules (quad modules). In the configuration used for prototype characterisation, the chips are wire bonded to the flex which takes the signals to a small PCB. This provides just the basic connections for the module operation: a 4-pin connector for analog and digital voltages and a LEMO connector for the bias voltage of the sensor. The data stream is managed via ethernet cables.

4.1.2 Readout systems

For data taking and tuning procedures, the detector board and flexes presented in the previous section can be connected to two different readout systems described in the following.

USBPix

The USBPix [116] is a modular readout system based on a multi-purpose input/output Field-Programmable Gate Array (FPGA) board (Multi-IO board) which was designed at the Bonn University for the ATLAS pixel community. The readout system, shown in Figure 4.2, is completed by dedicated adapter cards which offer the possibility of steering either FE-I3 or FE-I4 chips. The Multi-IO board handles the signal transmission to the chip and provides connections to the computer via the Universal Serial Bus (USB) protocol version 2.0. An external trigger input connection via ethernet or LEMO is also available. Two different adapter cards were used for FE-I3 and FE-I4 single chip modules which are both equipped with a KEL connector and, in the case of the FE-I4, also with an ethernet connector for the data stream and an 8-pin connector for the analog and digital voltages. A different adapter card, the Burn-in card shown in Figure 4.2(b), was instead designed for quad modules providing ethernet connections to handle the data stream of four FE-I4 chips at the same time. All adapter cards can be externally powered to generate analog and digital voltages for the chips [117]. The full system is steered with the STControl software which provides full access to the chip DAC registers as well as different tuning algorithms and test scan procedures with customisable parameters.

(a) FE-I3 single chip   (b) FE-I4A single chip card   (c) FE-I4B single chip card
card

(d) Quad PCB   (e) Quad flex
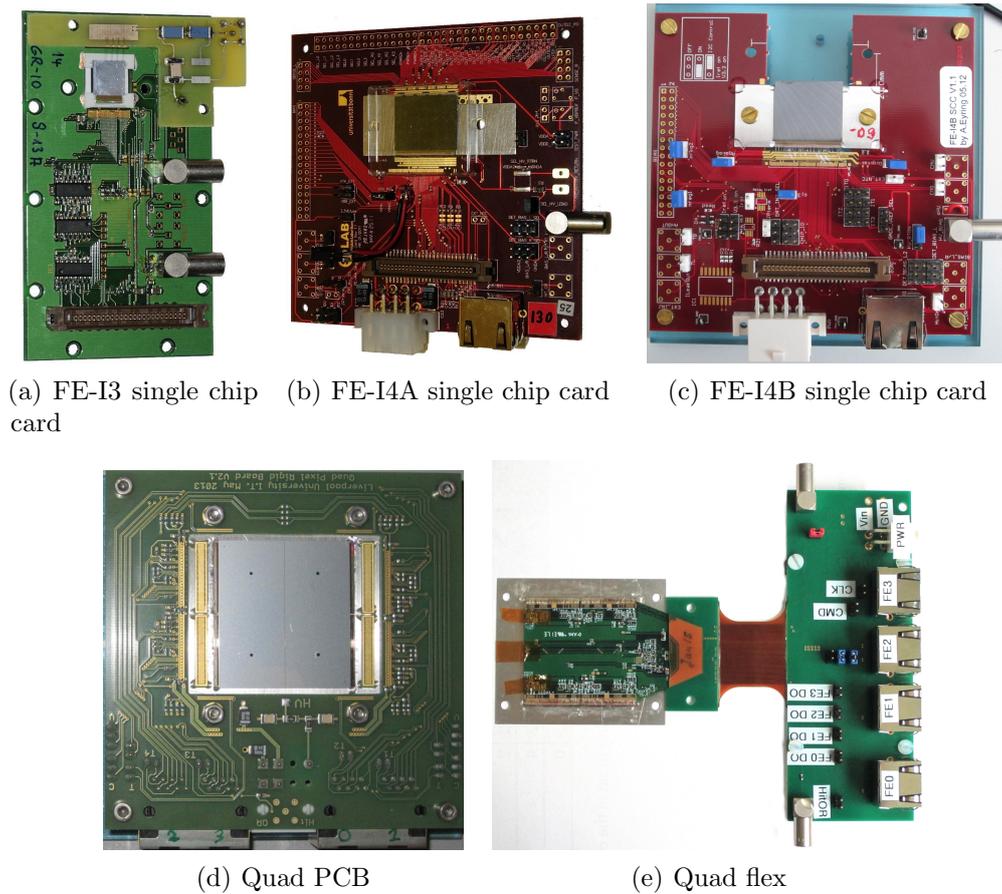
Figure 4.1: The different readout chip interfaces. (a), (b) and (c) show the single chip cards for
the FE-I3, FE-I4A and FE-I4B chips, respectively. The PCB designed in Liverpool
for the quad modules is shown in (d). (e) shows an example of flex designed for
quad modules.

RCE

The Reconfigurable Cluster Element (RCE) system [118] is a DAQ system developed at the
Stanford Linear Accelerator Center (SLAC) for ATLAS pixel development and upgrade ap-
plications. It is based on the Advanced Telecommunication Computing Architecture (ATCA)
which guarantees high speed data handling. The setup for pixel module readout is illustrated in
Figure 4.3. It consists of one or more RCE boards and a Cluster Interconnect Module (CIM)
located in an ATCA create. The CIM offers an ethernet connection to a DAQ computer to
steer the readout system. An external High Speed Input/Output Module (HSIO) is connected
to the RCE via an optical fibre and handles the trigger signals and the data stream of the
pixel modules through an adapter card, which provides the specific connections. The adapter
card used for FE-I4 modules offers ethernet connections to interface to a maximum of eight
chips at the same time. Two different software packages are provided to operate the RCE:
the *calibGUI* that allows for tuning and source scans and the *cosmicGUI* which provides an
interface dedicated to beam test applications.

(a) USBpix system

(b) Burn-in card
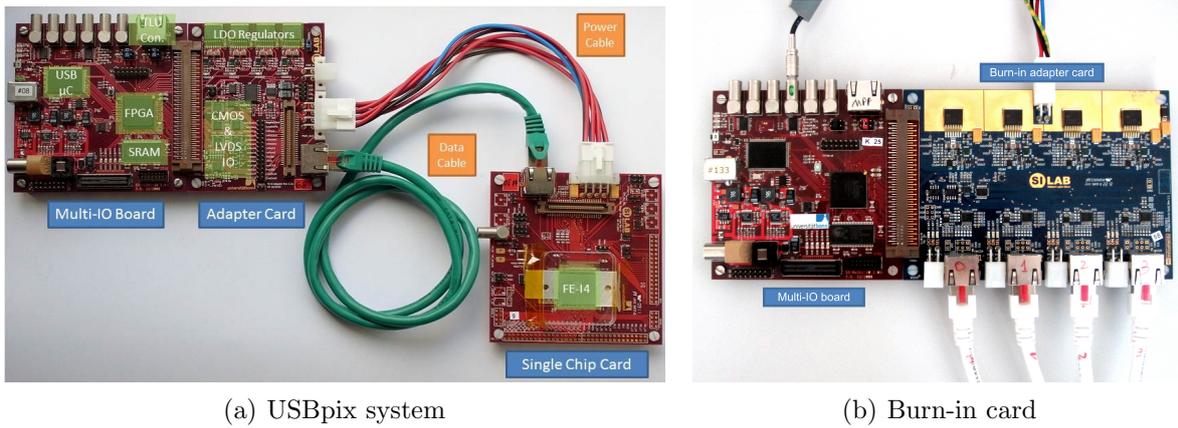
Figure 4.2: The USBpix readout system [116]. A configuration for single chip FE-I4 cards is shown in (a). The Burn-in adapter card is shown in (b).

(a) RCE boards

(b) HSIO + FE-I4 adapter card
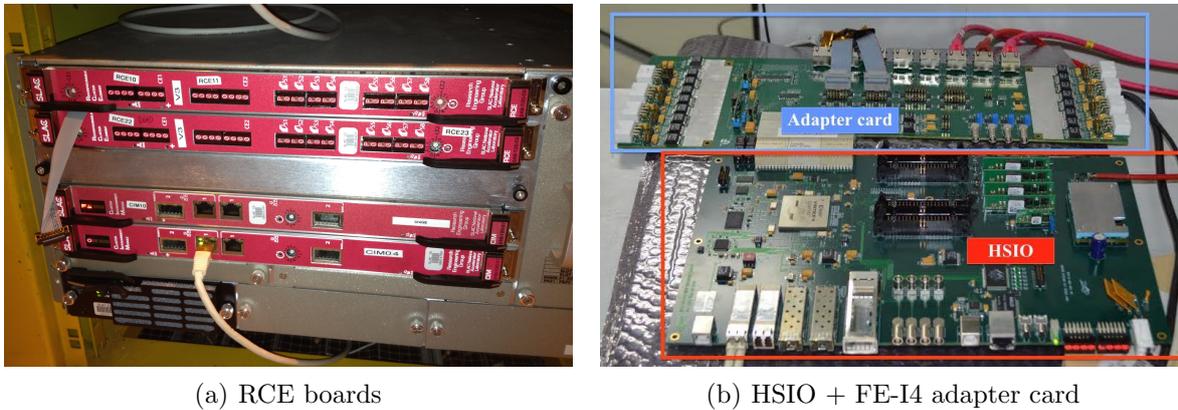
Figure 4.3: The RCE readout system [118]. In (a) the RCE boards and the CIM inside the ATCA crate are shown. (b) shows the HSIO connected to the FE-I4 adapter card.

4.2 Chip tuning

As discussed in Section 3.1, each channel of the chip has a discriminator, which determines a threshold below which the collected charge is not registered. At the same time, the ToT depends on the feedback current of the shaping circuit, which changes the fall time of the signal. Due to production variations over the chip surface, the Digital to Analogue Converter (DAC) settings, which determine threshold and ToT for each pixel, correspond to different values of these parameters. To reduce within reasonable limits their dispersion, the chip needs to be tuned. As shown in Figure 4.4, ToT and threshold are strictly connected and a change of one parameter affects the other, an iterative procedure is therefore needed to achieve a uniform tuning of both parameters at the same time. Similar tuning algorithms are used for the two generations of ATLAS chips and their concepts are independent of the DAQ system, therefore they will be discussed in general terms in this section.
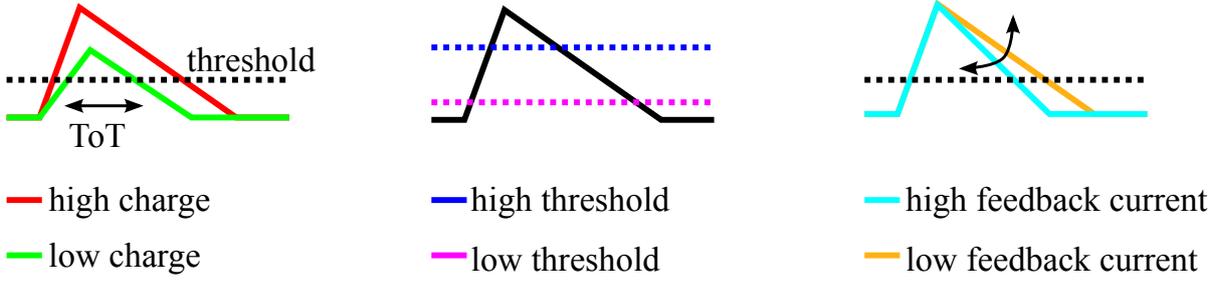
Figure 4.4: Dependance of the preamplifier output signal from the settings of threshold and feedback current. Figure adapted from Ref. [119].

4.2.1 Threshold

The threshold is measured for each pixel by performing a scan over the charge range of the injection circuit. For each scan point the charge is injected multiple times and the percentage of signals detected (occupancy) is recorded. The value of the threshold Q_{thr} is defined by the amount of charge which corresponds to an occupancy of 50 %. Figure 4.5 shows the distribution of a typical threshold measurement for one pixel. To determine the threshold value, this is fitted with a convolution of a step function and a Gaussian distribution which describes the probability of having a signal p for a certain injected charge Q as:

$$p(Q) = \frac{1}{2}\text{Erfc}\left(\frac{Q_{\text{thr}} - Q}{\sqrt{2}\sigma_{\text{noise}}}\right) \tag{4.1}$$

where Erfc is the complementary error function defined as:

$$\text{Erfc}(x) = 2\int_{x}^{\infty} \frac{e^{-y^2}}{\sqrt{\pi}}\,\text{d}y. \tag{4.2}$$

The corresponding noise is defined by σ_{noise}.

   In a pixel detector the threshold is crucial for the particle detection efficiency and the spatial resolution. It has therefore to be adjusted for each pixel to maximise and equalise the efficiency and, at the same time, to avoid fake signals caused by noise in the readout electronics. The aim of a threshold tuning is to achieve the same value of the threshold for each pixel to have a uniform response over the entire module surface. This is possible by changing two digital registers in the chip, GDAC[3] and TDAC, which control the global and local discriminator stages of the chip, respectively. The GDAC sets a common value of the discriminator over the entire chip, it is 5-bit long in the FE-I3 chip and 16-bit long in the FE-I4 chip; the TDAC allows to independently fine tune the threshold of every single pixel and it is 7-bit long in the FE-I3 chip and 5-bit long in the FE-I4 chip. Two different algorithms can be used for tuning these registers. The GDAC TUNE algorithm performs a scan over the charge range of injection circuit and calculates the threshold for each pixel using Eq. 4.1. The GDAC register, for which the average threshold is closest to the target value is selected. As for the GDAC TUNE, also the local TDAC TUNE performs a scan over the full charge range of the injection circuit calculating the threshold of each pixel. If the threshold is lower than the target value, the TDAC register of

---

[3]also called V$_{\text{thin}}$ in the FE-I4 version.
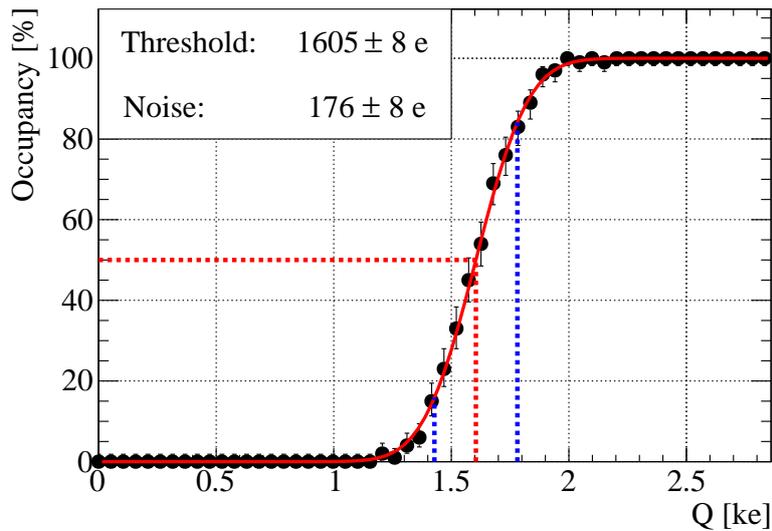
Figure 4.5: Threshold measurement for a single pixel of an FE-I4 chip. The data points are fitted to Eq. 4.1. The red dotted line shows the 50 % occupancy point which defines the threshold value. The noise is defined by the distance between the red and blue dotted lines, which corresponds to one standard deviation of the convoluted Gaussian.

the pixel is increased by a defined step, otherwise it is decreased. This procedure is repeated reducing progressively the step size to converge on the best register value. Fast versions of these algorithms are also implemented in the RCE software and in recent developments of STControl, which injects only the target threshold charge, instead of performing a scan over the full charge range. The measured occupancy of each pixel allows to decide whether the actual threshold was higher or lower than the injected charge and change the register setting accordingly to approach the 50 % occupancy. On one hand this fast algorithm reduces considerably the overall number of injections for each pixel and avoids the fit procedure, allowing to gain a substantial amount of computational time, especially given the high number of channels in the FE-I4 chip. On the other hand it is less robust, in particular for irradiated modules where noisy and inefficient pixels can compromise the assumption made by the occupancy measurement. An example of threshold and noise distributions for a not irradiated FE-I4A module after the described tuning procedure is shown in Figure 4.6.

4.2.2 ToT

As for the threshold also the ToT is tuned through one global register (IFDAC) and one local register for each pixel (FDAC). In this case the target charge is injected into each pixel and a scan over the register range is performed to find the value that gives the closest ToT response to the target. An example of a ToT tuning is shown in Figure 4.7 for an FE-I4 chip.
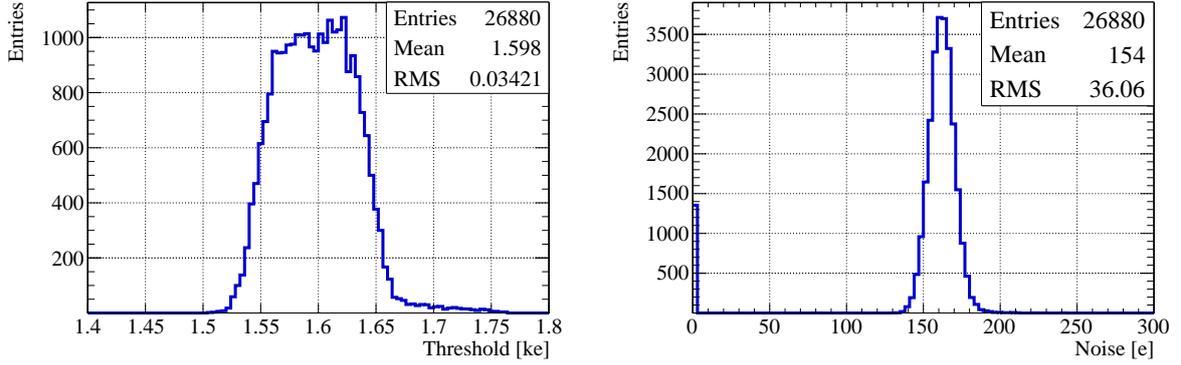
(a) Threshold distribution

(b) Noise distribution
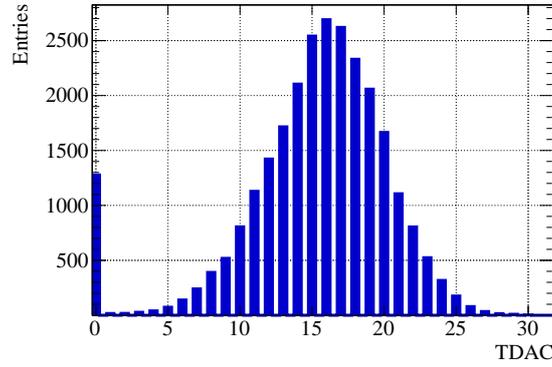
(c) TDAC distribution

Figure 4.6: Threshold and noise distributions of an FE-I4A chip before irradiation. The module was tuned to a target threshold of 1.6 ke. The distributions of the threshold and the corresponding noise are shown in (a) and (b), respectively. (c) shows the distribution of the local TDAC register value. Due to the different injection mechanism implemented for the first and last columns (see Section 3.1.2), these were not tuned.

4.2.3 Injection charge calibration

For an accurate absolute measurement of both ToT and threshold it is essential to know the injected charge with good precision. The absolute tuning of the chip relies on the injection circuit described in Section 3.1 and in particular on the correct measurement of the value of the injection capacitances $C_{\mathrm{inj}} = C_{\mathrm{lo}} + C_{\mathrm{hi}}$ and of the voltage response to the steering register (PlsrDAC). Knowing these two values the corresponding injected charge Q_{inj} can be calculated with the equation:

$$Q_{\mathrm{inj}} = C_{\mathrm{inj}} \cdot V_{\mathrm{cal}} \quad \text{with} \quad V_{\mathrm{cal}} = V_{\mathrm{slope}} \cdot \mathrm{PlsrDAC} + V_{\mathrm{offset}} \tag{4.3}$$

where V_{offset} is a reference potential, which for FE-I3 chips is equal to the analog voltage [120] and for FE-I4 chips is determined interpolating the result of the threshold measurements performed with different injection capacitances. For the FE-I3 chips of the ATLAS production, the value of the injection capacitors and V_{slope} were measured in Bonn at wafer level [121]. A
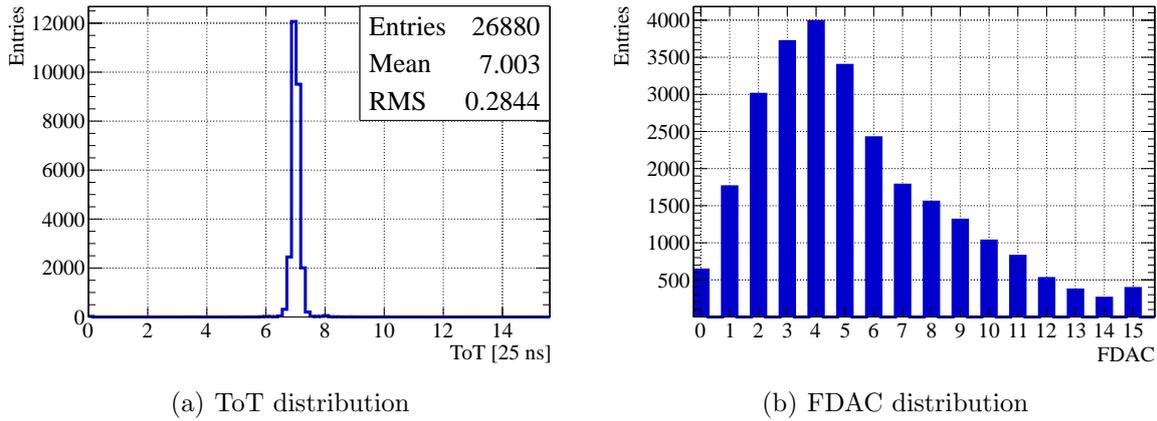
(a) ToT distribution

(b) FDAC distribution

Figure 4.7: ToT distribution of an FE-I4 chip before irradiation. The module was tuned to a target ToT of 7 for an injected charge of 14 ke. The distribution of the pixel response in ToT for the target injected charge of 14 ke is shown in (a). (b) shows the distribution of the local FDAC register.

variation of 5 % was found for the injection capacitance of the tested wafers with an additional difference of 2 % within each wafer and a 5 % variation for the measured slopes. For the injection capacitance of the FE-I4A chips the value obtained from the simulation of the production process is used, since no circuit to measure the injection capacitance is available [122]. On FE-I4B chips, instead, a dedicated circuit is implemented which allows to measure the injection capacitance on chip wafers before interconnections. For the investigations presented in this thesis, FE-I4B chips out of the IBL production were used, for which a spread of the value of the injection capacitance of 4 % was measured [123]. In the FE-I4 chips it is possible to calibrate V_{slope} after interconnection [122]. For each PlsrDAC register setting the voltage across the injection capacitance is measured, and the slope of the distribution is calculated in its linearity region as shown in Figure 4.8.

4.3 IV measurements

A first fundamental quality measure for silicon sensors is the leakage current of the bulk as a function of the bias voltage V_{b}, and its breakdown point V_{bd}. To obtain the maximum signal for charged particles crossing the pixel detector, the sensor bulk needs to be fully depleted. Moreover, increasing V_{b} over the full depletion voltage V_{fd}, the absolute value of the electric field in the depleted region and its uniformity are also incremented, hence the possibility of operating the sensor with $V_{\mathrm{b}} > V_{\mathrm{fd}}$ is a minimum fundamental prerequisite. A characterisation of all sensor structures is performed both before and after irradiation. The leakage current as a function of the applied bias voltage can be measured directly at wafer level, for the sensor designs which implement dedicated bias structures, or otherwise after interconnection to readout chips. In the following the resulting curve will be referred to as IV curve and its properties as IV characteristics. The IV curves of the new productions are measured at wafer level to define V_{bd} of the different structures and select the best candidates for interconnection. The IV curves of the pixel sensors are performed with a probe station. The voltage is applied to the sensor backside through the probe-station chuck, while the bias ring is kept at ground potential by
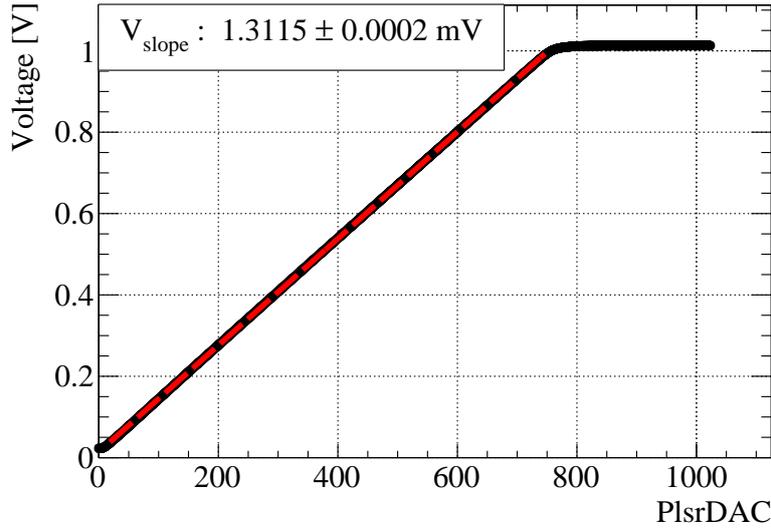
Figure 4.8: Measurement of the injection capacitance slope. The voltage across the injection capacitance is measured as a function of the PlsrDAC register setting. The fit to obtain V_{slope} of the linear part of the distribution is shown in red.

contacting it with a needle through dedicated openings in the SiO_2 passivation layer. The wafers are maintained at stable temperature with a cooling system connected to the chuck. After flip chipping the sensors are measured using the voltage connection of the detector board and are kept at stable temperature inside a climate chamber. For each applied voltage, ten subsequent measurements are performed and the resulting mean and standard deviation are calculated. For pixel sensors designed without bias structures a characterisation before interconnection is not possible and an optimal production yield is therefore essential for large productions.

4.4 Charge collection characterisation

The characterisation of the charge collection properties of the sensors is performed using ^{90}Sr beta electrons triggered by a scintillator placed behind the module as illustrated in Figure 4.9. The decay chain of ^{90}Sr consists of two beta emissions with a characteristic continuous three-body spectrum [81, 124]:

$$^{90}\mathrm{Sr} \quad \rightarrow \quad e^- + \overline{\nu}_e + {}^{90}\mathrm{Y} \quad (t_{1/2} = 28.8\,\mathrm{y}, E_{\mathrm{max}} = 0.546\,\mathrm{MeV}) \tag{4.4}$$

$$^{90}\mathrm{Y} \quad \rightarrow \quad e^- + \overline{\nu}_e + {}^{90}\mathrm{Zr} \quad (t_{1/2} = 2.67\,\mathrm{d}, E_{\mathrm{max}} = 2.280\,\mathrm{MeV}). \tag{4.5}$$
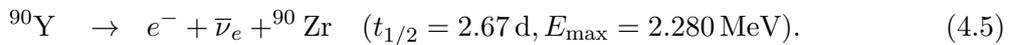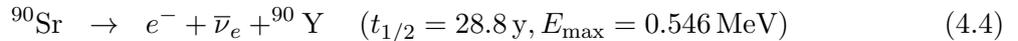
The low energy part of the spectrum is filtered since only electrons with an energy close to 2.280 MeV, which are good representatives of a MIP, pass through the detector thickness and thus can reach the scintillator. The full setup is kept at stable temperature inside the climate chamber. If not differently noted, all charge collection measurements in this thesis were performed at 20 °C for not irradiated modules and at −50 °C for irradiated modules.

A typical charge measurement of the MIP energy loss in a 100 μm thick silicon sensor with FE-I3 and FE-I4 modules is shown in Figure 4.10. The data are fitted to the expected Landau distribution convoluted with a Gaussian distribution, which describes the intrinsic detector
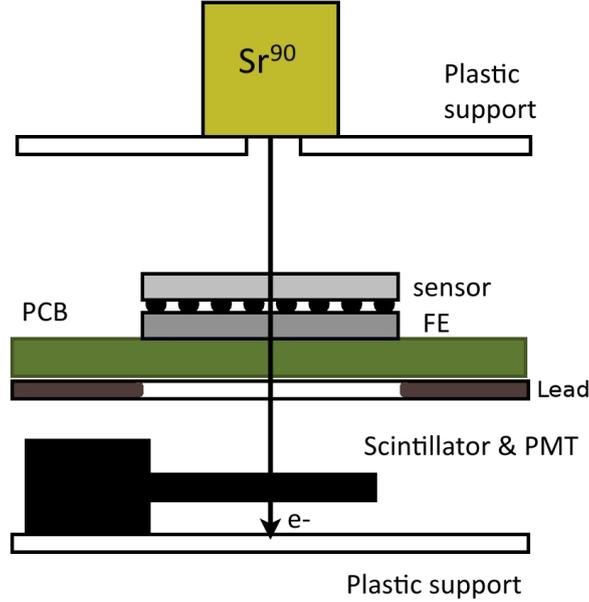
Figure 4.9: Schematics of the experimental setup for charge collection measurements, mounted
          in a climate chamber.

fluctuations and the electronic noise [125]. The Gaussian contribution broadens the shape of
the distribution and increases the MPV with respect to the one of the original Landau. The
MPV of the convoluted Landau distribution is accessible from the fit and offers a measurement
of the charge collection of the sensor which is disentangled from the noise and has only a small
dependency on the fit range. Hence, this value will be implicitly referred to in the following
when stating the measured collected charge. Measurements with γ radioactive sources are
performed in the same setup, but using the internal self-trigger of the chip, since low energy γs
interact with silicon mostly through photoelectric effect releasing all their energy at once and
therefore they do not reach the external trigger system. The internal self-trigger processes and
registers all signals above threshold. It is therefore very sensitive to noisy pixels which could
hinder the readout system. For this reason, after irradiation, noisy channels need to be masked
and the measurement for these modules are in some cases performed for only a sub-sample of
pixels.

4.4.1 ToT to charge calibration

To compare results of different modules the charge measured in ToT is converted to the
correspondent number of electrons. For FE-I3 chips the ToT response after tuning is calibrated
performing a charge injection over the full V_{cal} range for each pixel. The resulting relation
between injected charge Q and ToT is represented by:

$$Q = \frac{\text{ToT} \cdot C - A \cdot B}{A - \text{ToT}} \quad \text{or} \quad \text{ToT} = A\frac{B + Q}{C + Q} \tag{4.6}$$

The fit is performed for each pixel and the three parameters A, B and C are used to convert
the ToT to charge in measurements with external particles. An exemplary ToT to charge

(a) FE-I3   (b) FE-I4
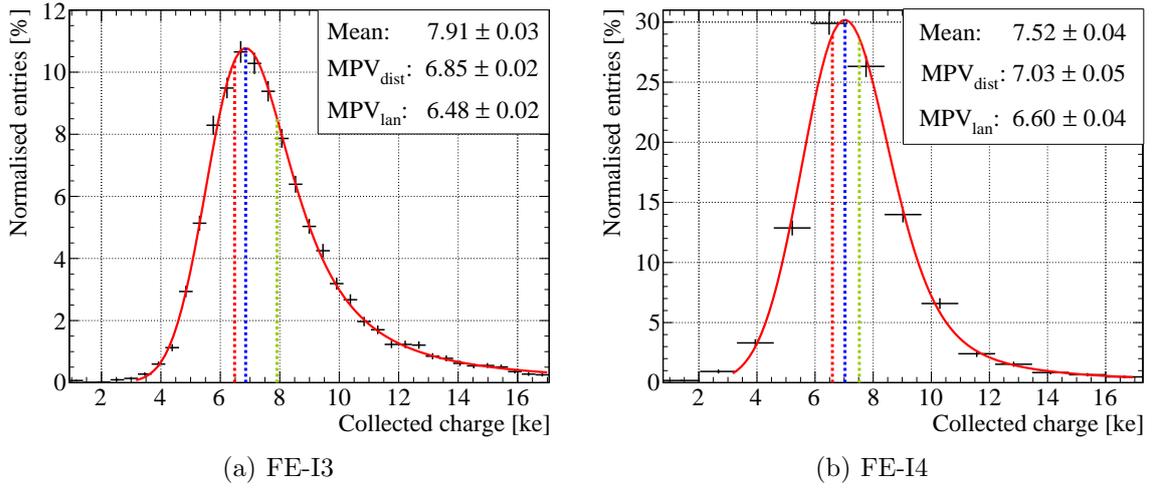
Figure 4.10: Collected charge distribution for MIPs in $100\,\mu$m thick silicon sensors before irradiation. The measurement was performed in (a) with an FE-I3 module tuned to a threshold of $2.5\,$ke, and in (b) with an FE-I4 module tuned to a threshold of $1.6\,$ke. The distribution is fitted with a convolution of a Landau and a Gaussian distribution. The blue and the red dotted lines show the MPV of the full distribution (MPV_{dist}) and of the convoluted Landau (MPV_{lan}), respectively. The green dotted line indicates the mean value. The coarser binning for the FE-I4 module is due to the lower number of bits dedicated to the ToT information with respect to the FE-I3 chip.

distribution obtained for a single pixel and fitted with this empirical function is shown in Figure 4.11(a).

To verify the calibration and eventually correct for further systematic biases [121], radioactive sources with a well defined γ spectrum are used as reference. For FE-I4 chips a reliable ToT to charge calibration pixel by pixel is not yet available, hence a global calibration, which relies on external γ source measurements, is adopted to reduce the uncertainties in the direct conversion of the MPV of the distribution from ToT to charge. The MPV of the convoluted Landau distribution is corrected assuming the linearity of the ToT response close to the target value of the ToT tuning. Figure 4.11(b) shows that the linearity approximation is a good assumption for the average ToT response of FE-I4 pixels within $3\,$ToT from the target values of the tuning. A list of radioactive sources used and their γ energies expected in silicon is presented in Table 4.1. The most energetic γ line of ^{241}Am was used as reference for not irradiated modules employing 150 and $200\,\mu$m thick sensors where a MPV of the charge is expected between 10 and $14\,$ke. For modules employing $100\,\mu$m thick sensors and irradiated modules, for which a charge between 3 and $8\,$ke is expected, the most intense γ peaks of ^{109}Cd are used as reference. Measurements of spectra of these isotopes, performed with FE-I4 chips, are shown in Figure 4.12. The relevant γ peaks are fitted with Gaussian functions. For FE-I3 modules a systematic uncertainty of $7.3\,\%$ is associated to the measured charge, due to the uncertainty on the injection calibration discussed in Section 4.2.3. A total systematic uncertainty of $12\,\%$ is associated to charge collection measurements with FE-I4 modules where the MPV is corrected with γ lines. This uncertainty takes into account the precision in the determination of the γ peaks and the linearity of the

(a) FE-I3

(b) FE-I4
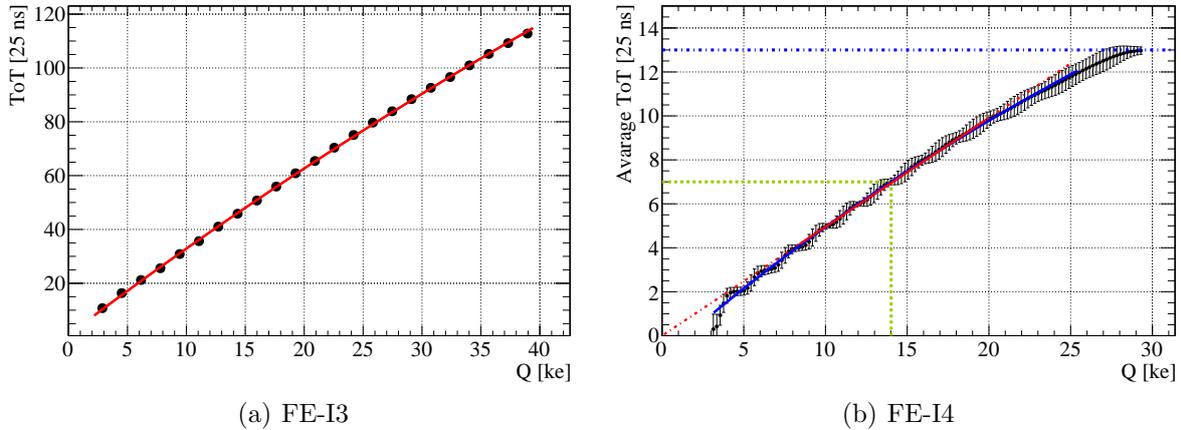
Figure 4.11: ToT to charge calibration. (a) shows the ToT distribution as a function of the injected charge for a single pixel of an FE-I3 chip tuned to a target ToT of 60 for 20 ke. The red line is a fit to the data with Eq. 4.6. (b) shows the average ToT as a function of the injected charge for the pixels of an FE-I4 chip tuned to a target ToT of 7 for 14 ke. The solid blue line is a fit to the data with Eq. 4.6, while the red line is a linear fit to the data (the solid part indicates the fit range around the calibration target). The dotted green lines show the tuning targets and the dotted blue line highlights the upper limit of the ToT range. Both modules were tuned to a threshold of 2.5 ke.

Table 4.1: List of radioactive sources used for the ToT to charge calibration correction. Energies and relative intensities of the most significant lines of the γ spectrum for each nuclide are shown [126]. The γ energies used for calibration are highlighted in purple and green for ^{241}Am and ^{109}Cd, respectively.

Nuclide	γ energy [keV]	Average signal in Si [ke]	Intensity [γs per 100 disint.]
^{241}Am	26.3	7.2	2.3
	59.5	16.3	35.9
^{109}Cd	22.0	6.0	29.2
	22.2	6.1	55.1
	25.0	6.9	15.3
	25.5	7.0	2.7

average ToT response with a conservative approximation. If a correction based on γ sources was not available a conservative systematic uncertainty of 20 % is assumed. A summary of the total systematic uncertainties associated to the collected charge measurements for the different chips is given in Table 4.2.

Table 4.2: Systematic uncertainties associated to the charge collection measurements performed with different readout chips.

Chip	γ correction	Systematic uncertainty [%]
FE-I3	yes	7.3
FE-I4	yes	12
	no	20

For better comparison of the measurements obtained with different sensor thicknesses and readout chips, the analysis of the charge collection with radioactive sources has been restricted to single pixel clusters. This allows to reject the most tilted tracks which have a longer path in the active volume of the sensor and more likely give two pixel clusters. Moreover, when the energy released by the crossing particle is shared between two or more pixels, a lower charge is collected by each pixel which could fall in the non linearity region of the ToT response for FE-I4 chips.
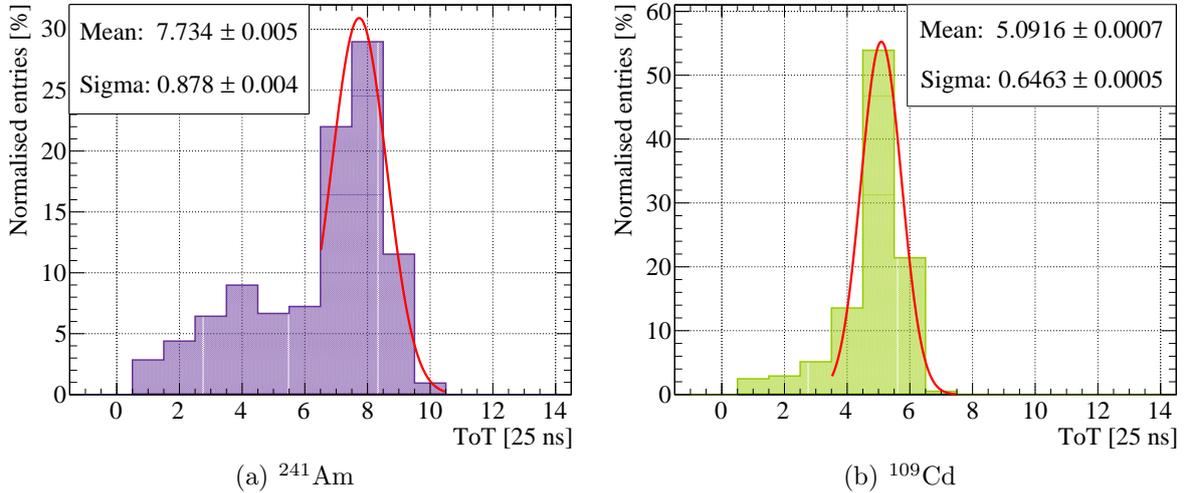
(a) ^{241}Am

(b) ^{109}Cd

Figure 4.12: ToT distribution of the γ spectrum for ^{241}Am (a) and ^{109}Cd (b) measured with FE-I4 modules. For the ^{241}Am data the chip was tuned to 7 ToT for a target charge of 14 ke, while, for ^{109}Cd measurements, a tuning of 6 ToT for a target charge of 6 ke was used. The peaks corresponding to the γ lines highlighted in Table 4.1 are fitted with a Gaussian.

4.5 Beam tests

The final results to define the performance of pixel modules for tracking purposes are obtained in beam test experiments with high energetic particles, producing conditions close to the one expected in high energy physics experiments. Particle beams are provided by dedicated accelerator facilities with well defined characteristics, such as energy and intensity. An array of tracking devices arranged as a telescope is aligned along the beam line and allows to reconstruct the particle trajectories and determine their impact points on the Device Under Tests (DUTs), which are normally placed in the centre of the telescope. The accurate determination of the impact point on the DUT allows to perform precise studies of the detector properties over the pixel cell area. In this chapter the different beam test facilities and telescope setups are presented, and the performed measurements and analysis methods are described.

4.5.1 Beam lines

Particle beams of two facilities were used to obtain the results presented in this thesis. Their characteristics are described in the following.

DESY

The Deutsches Elektronen-Synchrotron (DESY) complex provides a continuous electron or positron beam to three beam test lines with up to 1000 particles per cm^2 per second with an energy up to 6 GeV [127]. The spread of the particle momenta in the beam is around 5 %. The beam is obtained from the DESY II electron/positron synchrotron where bremsstrahlung radiation is generated by a carbon fibre target and converted again into electron and positrons by passing through a metal plate. The preferred particle type is selected with a magnetic dipole which spreads horizontally the particle beam that is then collimated and delivered to the different beam lines. Since the energy of the synchrotron varies with time, the bremsstrahlung edge of the photon spectrum also changes with the cycles of the accelerator, thus, working with higher energies implies lower particle rates. For the presented measurements the current of the magnet was tuned to have a particle energy of 4 GeV, which ensures an optimal compromise with the particle rate.

SpS

The SpS at CERN offers seven beam lines, four of which are dedicated to beam test facilities in the North Area. The proton beam is extracted from the SpS accelerator and directed onto two primary targets serving several beam lines each. Hitting on the targets, protons are converted to pions which then pass through a dipole magnet where their momenta are selected and they are delivered to the different beam lines. For beam lines served by the same target, the momenta and polarities of the beams are strongly correlated. The measurements preformed at this facility were obtained with an energy of either 120 GeV or 180 GeV. To serve the different facilities the beam is delivered in spills lasting from 4.8 to 9.6 seconds with one spill every 14–48 seconds depending on the number of facilities which need the SpS extraction. The maximum number of particles per spill is 2×10^8.

4.5.2 Telescopes

The particle trajectories are reconstructed in beam test experiments using two telescopes based on different pixel detector technologies. For all setups described in the following the DUTs are placed on a movable stage in the middle of the two telescope arms and are protected from the environmental light by a foam box designed at the Dortmund University [128]. This box is also used to provide the necessary cooling to operate irradiated modules. The layout of the cooling box, illustrated in Figure 4.13, consists of two separated areas to host the DUTs and dry ice blocks which provide the cooling. The temperature of each module is monitored close to the sensor. With this setup typical temperatures between -50 and $-40\,°C$ are obtained during operations.
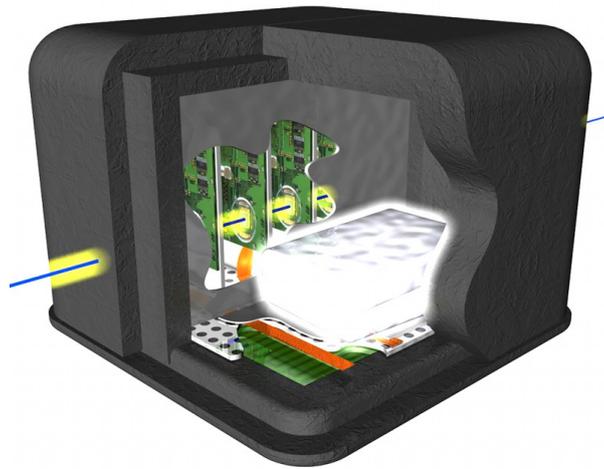
Figure 4.13: The cooling box for beam test measurements designed at the Dortmund University [128].

EUDET

The EUDET beam telescope is composed of six detector planes based on Monolithic Active Pixel Sensors (MAPS) with fast binary readout and zero suppression [129, 130]. These are MIMOSA26 pixel sensors which have 576×1152 square cells with a pitch of $(18.4 \times 18.4)\,\mathrm{\mu m}^2$ and a thickness of only $25\,\mathrm{\mu m}$. The extremely thin sensors make this telescope particularly suitable for tracking of low energy particles, since the pointing resolution is strongly affected by multiple scattering. The readout is triggered by particles crossing four scintillators, two at each end of the telescope. The ideal pointing resolution achievable is about $2\,\mathrm{\mu m}$ [129] with a maximum possible rate of $\sim9\,\mathrm{kHz}$ set by the MIMOSA26 integration time of $115.2\,\mathrm{\mu s}$ [131]. The readout architecture is able to host different modules as DUTs including FE-I3 and FE-I4 modules through the integration of both USBPix and RCE readout systems with the telescope DAQ. Due to the larger integration time of the MIMOSA26 with respect to the ATLAS readout chips, a reference device (usually another FE-I3 or FE-I4 module) is needed in addition to the DUTs to select the in-time tracks. Several replica of the EUDET telescope were produced. Some of these are in use at the DESY beam test facility, while one telescope, ACONITE, is ATLAS propriety and is installed at CERN.

FE-I4 telescope

A telescope based on IBL modules was developed at the University of Geneva to be used at the CERN SpS beam line. It is composed of three IBL FE-I4 pixel planar modules per arm for a total of six tracking planes. Since the shape of the FE-I4 pixel cell is rectangular, the telescope layout alternates horizontal and vertical planes to obtain high resolution measurements in both coordinates. An ideal pointing resolution of 8 and 14 µm in the x and y direction, respectively is estimated in the case of negligible multiple scattering effects. The full telescope system is read out with RCE and presently can host up to two FE-I4 modules as DUTs. The trigger is produced by the first and the last plane in the beam. Thanks to the large surface of the FE-I4 modules and their high clock speed, this telescope is able to fully profit from the beam intensity of the SpS beam lines even up to the HL-LHC rates. Moreover, having only FE-I4 modules ensures a synchronous readout of telescope planes and DUTs without the necessity of a reference plane for time matching.

4.5.3 Track reconstruction

The track reconstruction was performed within the EUTelescope framework [132, 133] and is divided in five main steps: first the trigger informations are decoded, and the pixels with a signal over threshold (hit) are associated to the proper crossing time, defining an event. In the same step, pixels which exhibit an excessive firing frequency are considered noisy and are suppressed. The second step is the clustering, here, for each detector, the adjacent hits in each event are grouped together defining cluster structures from which the coordinates of the particles crossing the device are calculated. In the next step the extrapolated coordinates are transformed into the global reference frame of the telescope according to each plane position and rotation in space. A crucial step of the track reconstruction is the alignment of the telescope and the DUT planes. This is performed in two phases: first the hits on each plane (including the DUTs) are selected and associated to possible tracks. The second phase uses the *Millepede II* [134] package to perform an iterative alignment of all planes with a *Kalman filter* approach [135]. In the last step the hits on the telescope planes are interpolated with a broken-line fit [136] and the crossing coordinates on the DUTs are calculated.

4.5.4 Data analysis

The information on reconstructed tracks is stored together with DUT data for the subsequent analysis which was mainly performed inside the TBmon framework [137]. Here, the data of the DUTs are reprocessed to match the requirements of the different specific analysis: noisy pixels and unresponsive pixels, which include the ones masked during the data taking, are identified and excluded from the analysis; clusters are formed grouping together pixels which are adjacent both in space and time. Tracks that fulfil the quality requirements are selected and by looking at their impact points on DUTs, they are associated to the closest reconstructed cluster within a distance of 1.5 times the pitch of the device in each direction. The data are then ready to be processed for dedicated analysis.

Cluster properties

A signal in multiple pixels can be produced by a single particle crossing perpendicularly to the pixel surface close to the border between two or more cells, due to diffusion of the charge

carriers in the silicon bulk (see Section 2.1.3), or by particles impinging non perpendicularly to the detector surface. Hits belonging to the same event which are close in space and time are assumed to be produced by the same crossing particle and are regarded as clusters. The corresponding cluster size is the number of pixel cells forming the cluster, while the cluster width defines the length in number of pixels in one of the two detector coordinates. For single pixel clusters the geometrical centre of the pixel is the best approximation of the particle crossing coordinates. For clusters with size larger than one, the crossing point can be extrapolated with a better precision by weighting the position of each pixel in the cluster with the respective collected charge. An even more precise measurement of the impact point is possible for clusters with size two, when weighting the charge with the η correction algorithm [138, 139]. In all cases the particle crossing point is defined in the middle of the depleted depth.

Spatial resolution

The intrinsic spatial resolution of a pixel detector can be extrapolated from the residual distribution. A residual is the difference between the crossing position measured by the DUT and the reconstructed impact point of the closest track associated to it. Because of the rectangular shape of the pixel cells the residuals are calculated separately in x and y according to the coordinate systems defined in Figure 4.14. Due to the uniform particle flux, for single pixel clusters the residual distributions are expected to be box shaped, with a smearing at the edges, given by the pointing resolution of the telescope. For clusters with higher pixel multiplicity the resolution is improved with the charge information and the distribution is expected to have a Gaussian shape.

Hit efficiency

The hit efficiency of a given sensor is defined as the ratio of the number of reconstructed tracks associated to a cluster in the DUT to the total number of tracks reconstructed by the telescope crossing the active area of the DUT. Depending on the pointing resolution, it is possible to determine the hit efficiency for the entire module and also for selected structures on its surface. This allows to study the hit efficiency inside the single pixel cells or at the border of the sensors. To collect the necessary statistics for these high resolution measurement, the information of identical structures is accumulated and projected onto one structure. An absolute systematic uncertainty of $0.3\,\%$ is associated to all hit efficiency measurements according to Ref. [140]. Because of the high statistics usually collected at beam tests, this systematic uncertainty is dominating. When a different uncertainty is quoted, this is obtained as the sum in quadrature of this systematic uncertainty and the statistical uncertainty calculated according to Ref. [141].

4.5.5 Pointing resolution

The effective final pointing resolution at the location of the DUTs is affected by possible uncertainties associated with multiple scattering, generated by the material between the first and the last tracking plane of the telescope. While multiple scattering for the telescope planes is precisely taken into account by the broken-line fit, the difficult determination of the additional material introduced between the two telescope arms can have a significant impact on the accuracy of the alignment and thus on the track reconstruction. When passing through matter, a charged particle is subject to a large number of scattering events mostly due to Coulomb interaction with the nuclei. The resulting particle deflection can be described by a Gaussian

<div align="center">(a) Pixel cell   (b) Module   (c) Beam test</div>
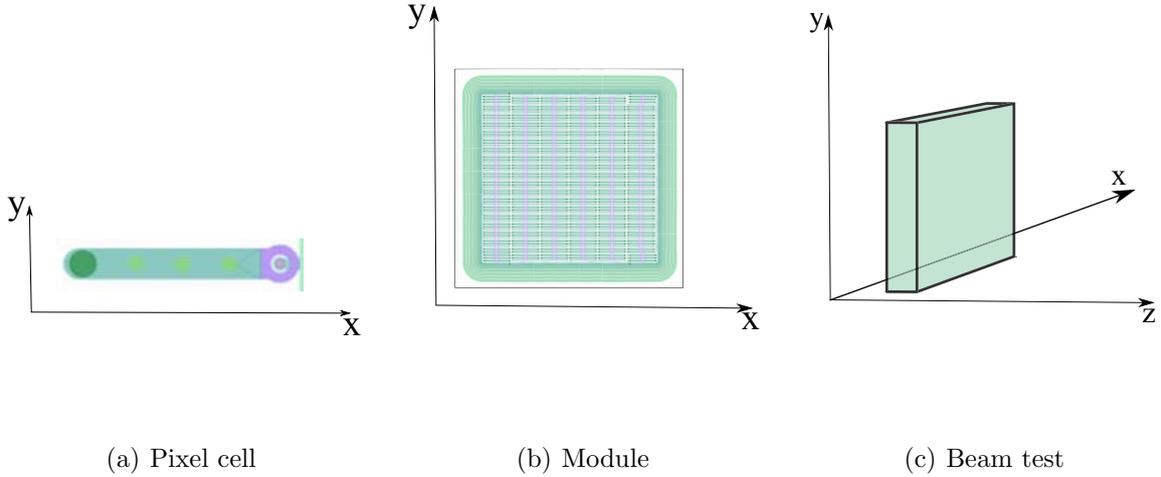
Figure 4.14: Definition of the coordinate systems used in the analysis for the single pixel cell (a), the module (b) and the beam test (c). The long pixel side lies along the x axis and the short pixel side along the y axis. Rotations around the x and y axis are indicated by ϕ and ϑ, respectively.

approximation, for which the Root Mean Square (RMS) of the projected angular distribution $\theta_{\mathrm{MS}}^{\mathrm{rms}}$ is given by [81, 142, 143]:

$$\theta_{\mathrm{MS}}^{\mathrm{rms}} = \frac{13.6\,\mathrm{MeV}}{\beta c p}\, z_{\mathrm{ch}}\, \sqrt{\frac{t}{X_0}}\left[1 + 0.038 \ln\frac{t}{X_0}\right] \qquad (4.7)$$

where βc and p are the particle velocity and momentum, z_{ch} is the charge number of the incident particle and t/X_0 is the material thickness in radiation lengths. As shown in Figure 4.15, this effect is small in the case of high energetic pions, which are used at SpS, but becomes critical at DESY even with the highest electron energy available of $6\,\mathrm{GeV}$. Hence, for the measurements performed at this facility, particular care was taken to optimise the setup as much as possible to reduce the effect of the multiple scattering.

An a posteriori estimation of the final pointing resolution is obtained from the width of the residuals on the reference DUT for perpendicular incident tracks. For this purpose one and two pixel clusters are reconstructed assigning the hit position to the centre of the cell with the maximum charge. Assuming a uniform flux over the pixel cells, the expected residual distributions in x and y are flat distributions over the pixel pitch, convoluted with the telescope pointing resolution, which has a Gaussian shape. The distribution of the residuals R is therefore described by a box distribution convoluted with a Gaussian i.e. by the equation:

$$f(R) = \begin{cases} \frac{N}{2}\mathrm{Erfc}\left(\frac{-R+p/2}{\sqrt{2}\sigma_{\mathrm{tel}}}\right) & \text{if} \quad R > 0 \\ \frac{N}{2}\mathrm{Erfc}\left(\frac{R+p/2}{\sqrt{2}\sigma_{\mathrm{tel}}}\right) & \text{if} \quad R < 0 \end{cases} \qquad (4.8)$$

where Erfc is the complementary error function (Eq. 4.2) and p is the pitch of the pixel cell. The telescope pointing resolution is the σ_{tel} of the Gaussian distribution. Some examples of
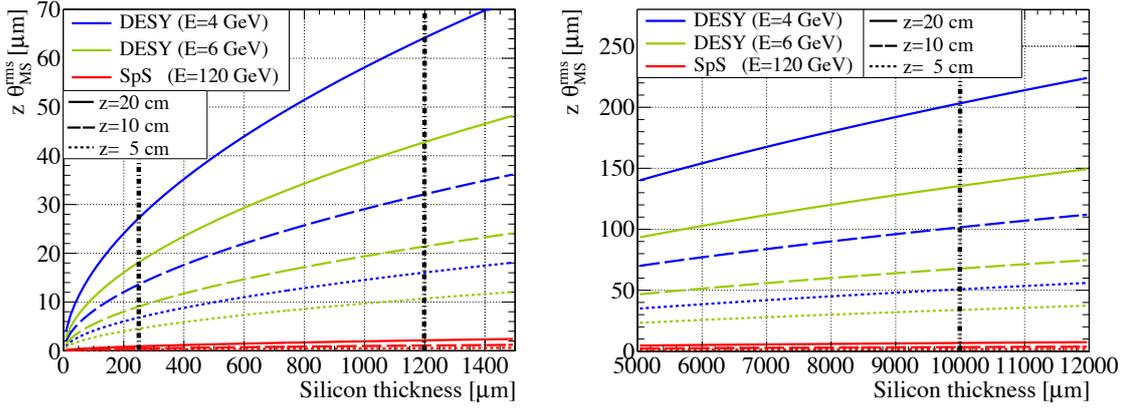
Figure 4.15: Particle scattering in silicon ($X_0 = 9.37$ cm) as a function of the thickness. The rms of the deviation is calculated from Eq. 4.7 and projected to various distances z from the scattering plane and for different particle energies. The vertical black lines indicates the equivalent silicon thickness of (from the thinner to the thicker) the walls of the cardboard box ($X_0 = 27.29$ cm) used at DESY for not irradiated modules, the average module thickness (including aluminium supports ($X_0 = 8.90$ cm)) and the walls of the beam test cooling boxes ($X_0 = 41.31$ cm).

the pointing resolution obtained with the EUDET telescope for different beam energies with different setups are shown in Figures 4.16 and 4.17. For measurements of not irradiated modules at DESY, where no cooling is needed, a small cardboard box is used, which reduces the material and allows to position the two telescope arms at less than 5 cm from the DUTs. This setup minimises the distance between the scattering planes and allows to obtain a pointing resolution similar to the one at SpS. As calculated from the residuals in Figure 4.16, the pointing resolution at SpS is about 4 μm, while at DESY with the small cardboard box and a distance between the telescope planes of about 10 cm, a pointing resolution of less than 6 μm was achieved. Such a compact setup is not possible in case of irradiated modules, due to the space necessary for the cooling system. Therefore, a smaller version of the cooling box was designed for DESY, which allows a distance between the two telescope arms of about 30 cm, instead of the more than 40 cm necessary with the larger version. A general improvement of the pointing resolution with this setup is obtained at DESY measuring only two DUTs at a time and minimising the distance between them inside the box. The residuals in Figure 4.17(b) show the best pointing resolution of 12 μm obtained for a setup with irradiated modules, while in Figure 4.17(a) is shown an example of a not optimised setup, where the larger cooling box was used. In this latter case the pointing resolution measured from the x residual is about 38 μm. Since this value is larger than half of the pixel pitch in y, the method here described fails to calculate the pointing resolution fitting the y residual as can be noticed from the wrong result obtained for the estimation of the pitch itself.

4.6 Simulation

A full simulation of the beam test environment is performed inside the *Allpix* framework [144] which provides a simulation package for pixel detectors based on GEANT4. The software allows

(a) CERN SpS

(b) DESY
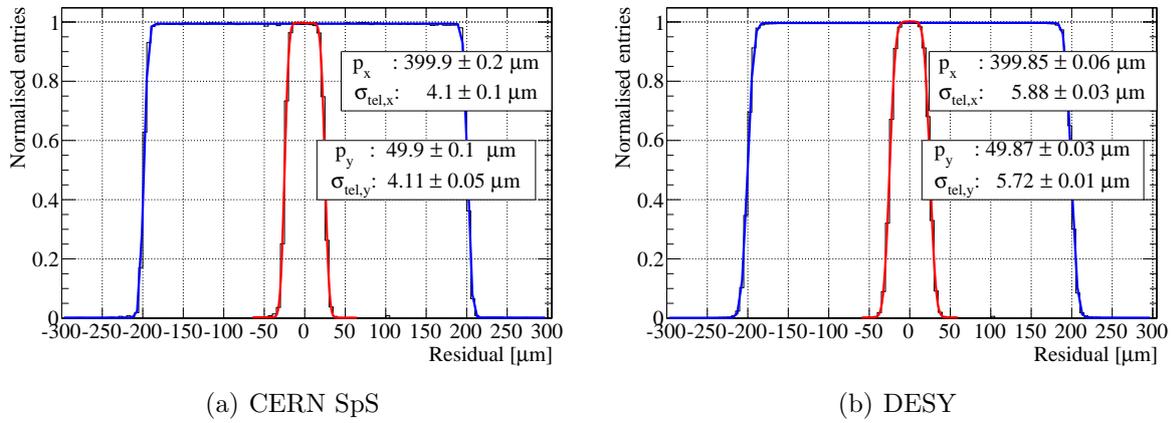
Figure 4.16: Comparison of the residual distributions of an FE-I3 module obtained at CERN SpS with 120 GeV pions, using the large version of the cooling box (a), and at DESY with 4 GeV electrons with the small cardboard box (b). The residuals for the x coordinate (blue) and for the y coordinate (red) are fitted using Eq. 4.8.

(a) Large box

(b) Small box
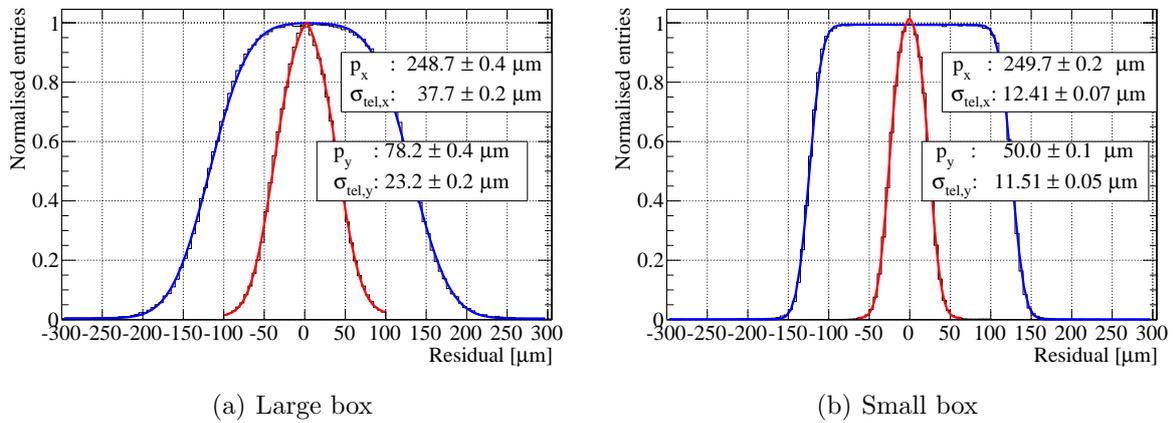
Figure 4.17: Comparison of the residual distributions of an FE-I4 module obtained at DESY with 4 GeV electrons, using the large (a) and the small (b) versions of the cooling box. The residuals for the x coordinate (blue) and for the y coordinate (red) are fitted using Eq. 4.8.

to simulate any module geometry and its environment. It also provides a simulation tool for the EUDET telescope which is used to study the expected behaviour of pixel modules at beam tests. The software simulates a particle beam with a defined energy and dispersion and computes the interactions with materials. The particle trajectory inside the active volume of the detector is divided into small steps and the energy deposition at each step is translated in the creation of electron-hole pairs following a Poissonian statistics. The description of the signal formation in the detector is then delegated to a *digitiser*. This computes the motion of the charge carriers according to the sensor geometry and derives the final ToT output taking into account the chip characteristics such as threshold, noise and energy resolution.

4.6.1 The planar sensor digitiser

For simulations of planar pixel sensors a digitiser developed at LAL[4] [144] and implemented in Allpix is used which employs an inductive model based on the Shockley-Ramo theorem described in Section 2.1.3. The motion of the charge carriers is computed taking into account the saturation of the drift velocity and the lateral charge diffusion according to Eq. 2.12. The drift trajectory integration is obtained with the Runge-Kutta-Fehlberg method [145]. For the simulation of irradiated sensors, the bulk resistivity and the trapping time are considered according to the equations described in Section 2.2. The digitiser has been adapted to the n-in-p sensor technology and the geometry of the modules presented in this thesis. The one-dimensional electric field for irradiated sensors is provided by external TCAD simulations performed at LPNHE[5] and implemented in the digitiser.

4.6.2 The 3D sensor digitiser

The 3D digitiser [146] used in this thesis is also based on the Shockley-Ramo theorem which considers the motion of both holes and electrons in the weighting field. Due to the electrodes geometry, the electric field is considered constant over the bulk thickness and the charge drift is treated in two dimensions. To calculate the induced signal both charge carriers are propagated in discrete time steps inside the electric field according to their drift velocity until they reach the collecting electrodes. At each step the contribution for the two carrier species is obtained from Eq. 2.9 and the total signal is given summing the results over the full drift path. The simulation of the induced charge in one pixel is performed at different points in an extended map of four times one pixel cell with a granularity of 1 µm and the results are stored in a lookup table. The final algorithm implemented in Allpix uses this lookup table to calculate the total signal S by multiplying the charge Q created by the particle to the value in the lookup table χ_{hit} corresponding to the hit position p:

$$S = Q \cdot \chi_{\text{hit}}(p) \tag{4.9}$$

When a hit is registered inside one pixel cell the same lookup table is used to calculate the induced signal for the neighbouring pixels as shown in Figure 4.18.

---

[4]Laboratoire de l'Accélérateur Linéaire http://www.lal.in2p3.fr/
[5]Laboratoire de Physique Nuclèaire et des Hautes Ènergies
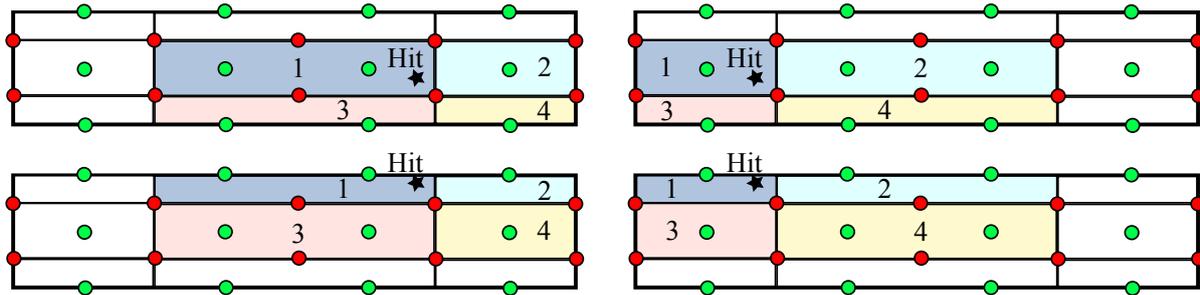
Figure 4.18: Map of the lookup table of the 3D sensor digitiser. The pixel for which the signal is calculated is in the centre of the map. The example of a hit occurring in the low-right quarter of pixel 1 is showed. The signal is calculated for the pixel 1 (top left) and for its neighbouring pixels 2 (top right) 3 (bottom left) and 4 (bottom right) using the same lookup table. Image adapted from [146].

4.7 Irradiation facilities

Irradiations of the pixel modules were performed at different facilities. The characteristics of each irradiation site are briefly described in the following.

4.7.1 TRIGA Mark II reactor (Ljubljana)

The TRIGA Mark II research reactor at the Jožef Stefan Institute (JSI) in Ljubljana is a light water pool type reactor, cooled by natural convection. It is used as a source of neutrons and γ rays for irradiation of silicon modules and related radiation damage studies for the ATLAS detector at CERN [147]. To reach the reactor core, the facility offers four channels (empty fuel roads), with a diameter of 15.5 cm, where, installing a heating/cooling module, silicon detectors can be irradiated at different temperatures. Due to the limited space available and the difficulties of shielding the electronic components to avoid their activation, the modulees are irradiated without PCB. The highest achievable neutron flux is in the central channel, where it can reach almost $2 \times 10^{13} \, \mathrm{cm^{-2} \, s^{-1}}$ at the reactor full power of 250 kW. The most significant radiation damage for silicon detector comes from fast neutrons with energy $\leq 100 \, \mathrm{keV}$ which have a flux of up to $5 \times 10^{12} \, \mathrm{cm^{-2} \, s^{-1}}$ with a hardness factor of 0.9. The contribution of thermal neutron and gamma irradiation is not significant since their damage in silicon is negligible compared to that of fast neutrons [148].

4.7.2 Compact Cyclotron (KIT)

The Zyklotron AG provides a 23 MeV proton beam, available for irradiations, from the cyclotron installed at the Karlsruher Institut für Technologie (KIT) [149, 150]. The protons have an hardness factor of 2.0 with a typical flux of about $9 \times 10^{12} \, \mathrm{cm^{-2} \, s^{-1}}$. The samples are hosted in a cooling box where the temperature is monitored to avoid annealing during the irradiation. A moving table allows to scan the beam across the detector surface to achieve a uniform irradiation of the samples over an area larger than the 7 mm beam spot size. The full modules can be irradiated directly on their PCB which is protected by a 2 cm thick screen made of high purity aluminium. This avoids repeating the wire bonding of the chips to the cards and possible damages during the handling. Because of the low energy of the protons the maximum

(a) Diode array

(b) FE-I4 module
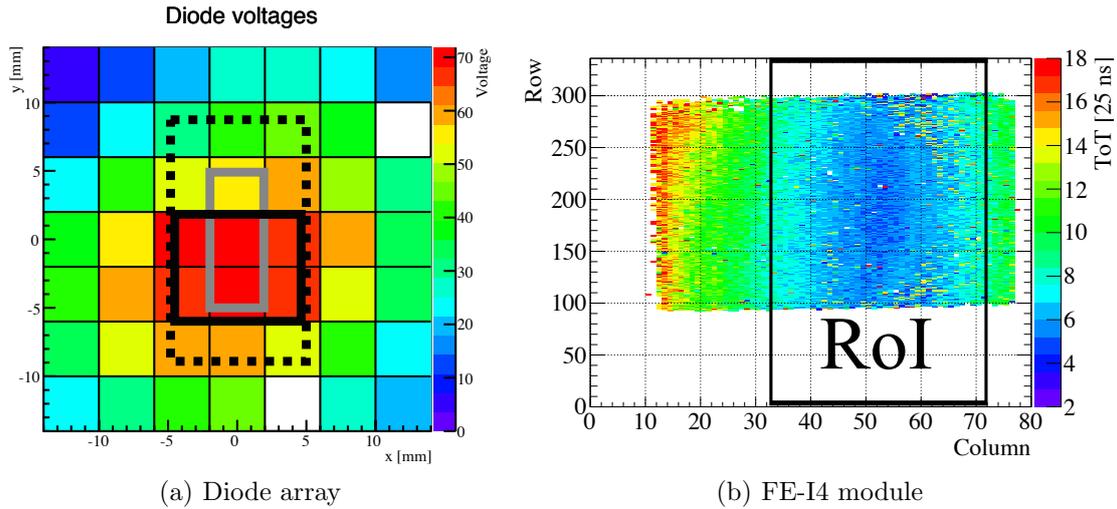
Figure 4.19: Irradiation beam profile at the LANSCE facility. (a) shows the measurement of the beam profile obtained with an array of diodes on which the position of the FE-I4 sensor (dotted black rectangle), the aluminium foil (grey rectangle) and the RoI (solid black rectangle) used for the analysis are sketched. (b) shows the measurement of the ToT over the module surface obtained at the beam test where the RoI used for the analysis is highlighted. Image adapted from Ref. [152].

achievable fluences at the KIT facility are limited by the damage induced in the readout chips by the ionising radiation. The FE-I3 modules were found to withstand a maximum fluence of $2 \times 10^{15} \, \mathrm{n_{eq}/cm^2}$, while FE-I4 chips can be irradiated up to $5 \times 10^{15} \, \mathrm{n_{eq}/cm^2}$, corresponding to about 600–700 Mrad, with a good surviving probability.

4.7.3 LANSCE (Los Alamos)

The Los Alamos Neutron Science CEnter (LANSCE) in New Mexico [151] offers an 800 MeV proton beam for sample irradiation with a flux of almost $1.5 \times 10^{12} \, \mathrm{cm^{-2} \, s^{-1}}$ and a hardness factor of 0.71. Since the facility does not provide any cooling and only bare sensors or modules can be irradiated to avoid activation of the boards, an annealing time of almost 1.5 days is inevitable for the mounting and wire bonding procedures. The beam is approximately circular with an RMS of about 1 cm. Since no scanning of the beam is available, larger samples like FE-I4 modules are tilted by 60° with respect to the beam direction to achieve a more uniform irradiation in one dimension. The beam profile is monitored by a diode array and the average fluence on the samples in a $(1 \times 1) \, \mathrm{cm^2}$ area is measured by an aluminium foil with an uncertainty of 10 %. Figure 4.19 shows an example of a diode array result where the positions of an FE-I4 module and the aluminium foil are highlighted. This information is used to calculate the fluence in the most uniformly irradiated area of the FE-I4 modules as discussed in Ref. [152]. The quoted fluences and the performed analysis for FE-I4 modules irradiated at this facility are reported for this area.

5 The IBL 3D pixel sensors

The new ATLAS IBL employs FE-I4 pixel modules exploiting the 3D silicon sensor technology described in Section 3.2.2, which is used for the first time in a high energy physics experiment. These new pixel modules are located at the edges of the staves covering the high-η region ($|\eta| > 2.4$) of the detector and are tilted by $\varphi = 14°$ to allow for the overlapping of the inactive regions and at the same time compensate for the Lorentz angle. The layout of the new IBL is also implemented in the ATLAS offline software based on the ATHENA framework, for which the digitisation algorithm described in Section 4.6.2 was developed. In this chapter a comparison of simulation and beam test results is presented to validate the 3D module digitiser. Section 5.1 summarises the results obtained for the two 3D sensor technologies at beam tests and in Section 5.2 the cluster distributions of simulated and beam test data are compared for perpendicular incident tracks and in the case of highly tilted particles as expected at high-η in IBL.

5.1 Beam test results

The two types of 3D sensors from the IBL productions at CNM and FBK introduced in Section 3 were investigated at beam tests at CERN before irradiation. The sensors were measured at a temperature of about $-15\,°C$ with perpendicular incident beam and were operated at a threshold of $1.6\,ke$. The hit efficiency over the pixel cell is shown in Figure 5.1. For the FBK design with fully passing columns, an inefficiency is observed for particles crossing n^+ or p^+ electrodes, while for the CNM design the inefficiency is confined to the p^+ columns. Since the columns in this design are penetrating in the bulk for $200\,\mu m$, perpendicular crossing particles can still produce electron-hole pairs in the remaining $30\,\mu m$ of active silicon and generate a hit if the threshold is lower than about 2–$2.5\,ke$. In the case of the p^+ columns instead, the charge collection is hampered by the p-stop implants. In this configuration, a global hit efficiency of $97.4\,\%$[1] and $98.6\,\%$ is measured for the FBK and CNM designs, respectively. Since in the real detector the modules are tilted and the tracks are bended by the magnetic field, the probability of particles solely passing through the column electrons is negligible and the limitations of the two designs are no more significant.

5.2 Comparison of beam test data and simulation

The charge sharing properties measured at test beams for CNM modules are compared with simulation. The full EUDET telescope setup was reproduced with the simulation software including scintillators and reference DUTs. The comparison of the cluster distributions is performed for both perpendicular incident tracks and in the IBL conditions at high-η with a $15°$ inclination in φ.

---

[1]An absolute systematic uncertainty of $0.3\,\%$ is associated to all hit efficiency measurements in this thesis as discussed in Section 4.5.4.

(a) Pixel cells

(b) FBK

(c) CNM
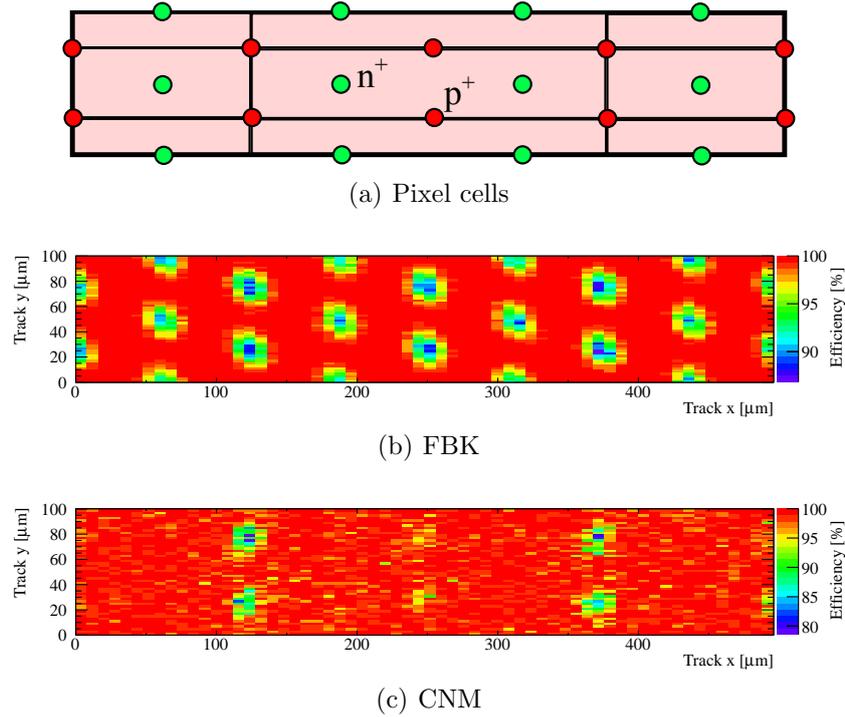
Figure 5.1: Hit efficiency distribution over the pixel cell of 3D sensors for perpendicular incident tracks at CERN SpS. (a) schematises the area onto which the reconstructed track impact points are projected. This is centred on one pixel cell and includes part of its neighbouring pixels. The hit efficiency maps obtained projecting the data for all identical structures onto this image are shown for the FBK design in (b) and for the CNM design in (c).

5.2.1 Perpendicular incidence

The distributions of the cluster size and the cluster width in x and y for perpendicular incident tracks are shown in Figure 5.2. The simulation reproduces with high accuracy the experimental data for the most relevant cluster sizes with one and two pixels, demonstrating a precise reproduction of the charge sharing effects. A worse agreement is instead observed for larger cluster sizes which are mainly generated in the areas between four pixel cells or by γ-rays and δ-electrons.

5.2.2 Highly inclined incidence

One 3D module with the CNM design was measured at test beams with an inclination of $\vartheta = 80°$, corresponding to $|\eta| \sim 2.4$, and of $\phi = 15°$ to reproduce the conditions in IBL. The same setup was simulated with Allpix and the 3D digitiser and results are compared in Figure 5.3. For this track incidence, an average cluster width in x of about 6.2 pixels and in y of about 2.2 pixels are expected from pure geometrical calculations. The position of the peak is well reproduced by the simulation for the distribution of the cluster width in x correspondent to the 80° angle. Significant differences are instead observed in the cluster width in y. The simulated distribution shows mostly a cluster width of two and three pixels. This is compatible with the

(a) Cluster width x

(b) Cluster width y

(c) Cluster size

(d) Ratio of simulation and data
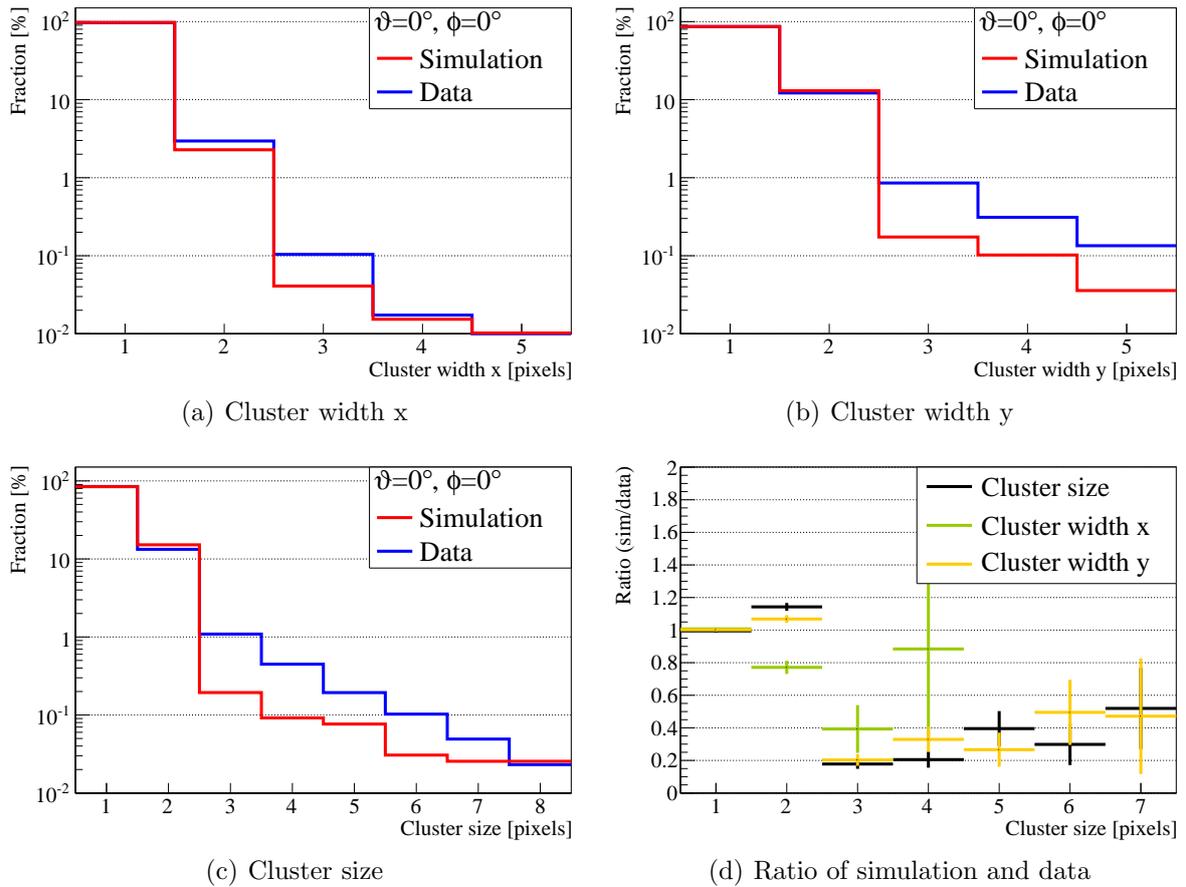
Figure 5.2: Comparison of simulated and beam test data for the cluster distributions of perpendicular incident tracks. The distributions of the cluster width in x and y are shown in (a) and (b), respectively. The distribution of the full cluster size is shown in (c). (d) shows the ratio of simulated and the beam test data.

geometrical expectation since, at this angle, a cluster width of one pixel can only be due to threshold effects which are expected to be small before irradiation. Moreover, the average of the two most populated bins in the simulated distribution is perfectly matching the expectation. This discrepancy with the beam test data could be related to the geometry of the CNM sensors which has partially passing columns leading to a different configuration of the electric field close to the frontside and the backside of the sensor. This aspect was not considered in the design of the digitisation model and could explain the single pixel inefficiencies, resulting in a reduced cluster size, with the lower charge collected for the pixels at the edge of long clusters when crossed close to the column implants. This effect would be enhanced in the cluster width y due to the five times larger cell dimension of the FE-I4 pitch.

5.3 Conclusions

An investigation of the performance of 3D modules presently employed in the ATLAS pixel detector was presented. The results obtained from the analysis of the beam test data of both

(a) Cluster width x

(b) Cluster width y
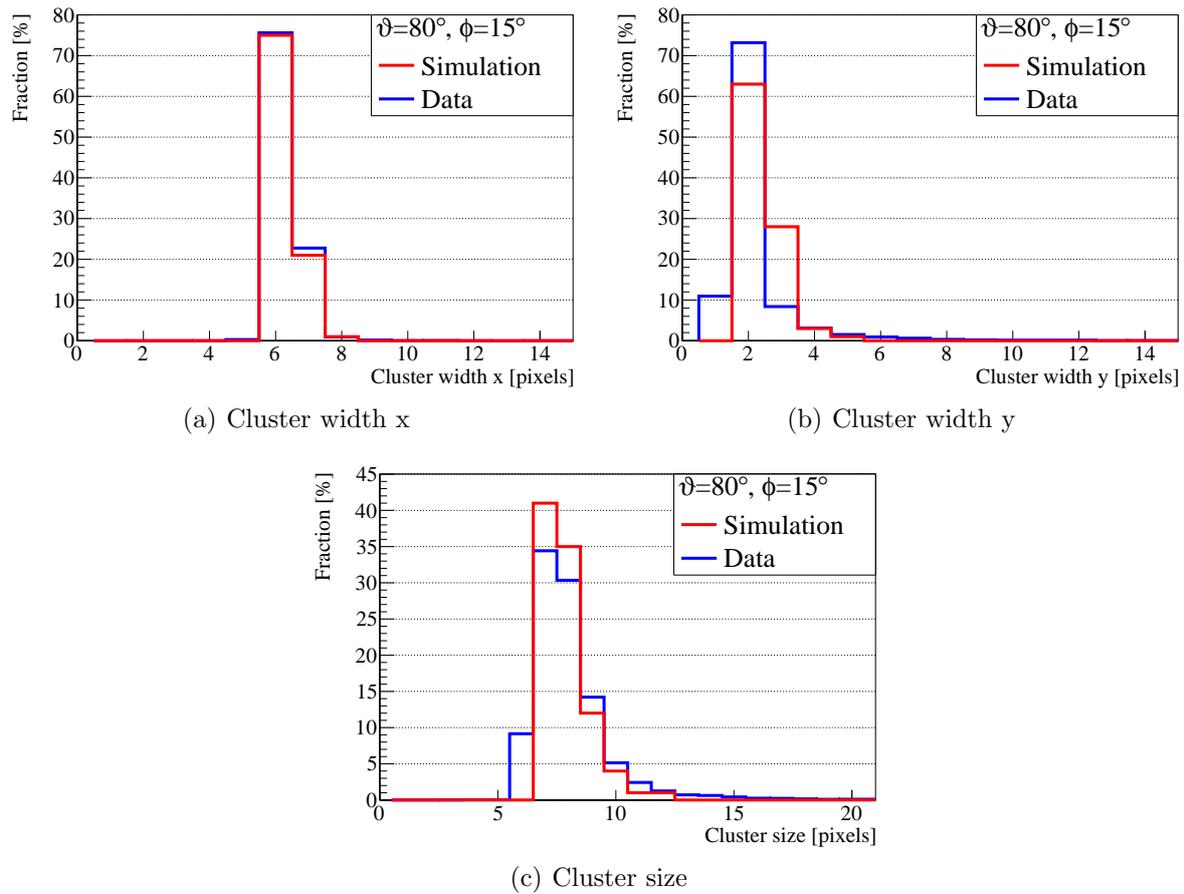
(c) Cluster size

Figure 5.3: Comparison of simulated and beam test data for the cluster distributions at high-η. The distributions of the cluster width in x and y are shown in (a) and (b), respectively. The distribution of the full cluster size is shown in (c).

FBK and CNM designs are in agreement with the analysis already published in Ref. [100]. To validate the digitiser implemented in the ATLAS simulation software, these data were analysed and compared with simulated data in case of perpendicular incident tracks and reproducing the conditions at high-η in IBL. The digitisation model reproduces with good accuracy the cluster distributions for perpendicular incident tracks especially for the most important cluster sizes of one and two pixels. At high-η the difference between beam test and simulated data is instead significant, in particular for the cluster width in y. This effect could be related to the geometry of the partially passing columns in the CNM sensors which compromises the assumption of the electric field uniformity along the depth of the bulk on which the digitisation model is based. Further measurements on 3D sensors from FBK will be necessary to verify this hypothesis.

6 Planar n-in-p pixel sensors

In this chapter the properties of planar n-in-p pixel modules are investigated and compared for different sensor designs. In Section 6.1 the sensor productions are described and in Section 6.2 a summary of the irradiations of the pixel modules and their IV characteristics is presented. The performance of different sensor thicknesses in terms of radiation hardness and tracking capabilities in the high-η regions of the pixel detector are then discussed in Section 6.3. In Section 6.4 sensors with different edge designs for the innermost layers are investigated, while Section 6.5 is dedicated to large sensors, interconnected to four FE-I4 chips, resulting in an assembly designed to cover the extended area in the outer layers of the pixel detector. Finally, investigations for the foreseen new chip geometries are discussed in Section 6.6. The presented measurements have been partially performed within the RD50 collaboration, and the Planar Pixel Sensor (PPS) group of ATLAS, focusing on the requirements for the ATLAS pixel detector upgrade at HL-LHC. Part of the results was already published in Ref. [153–156].

6.1 Production and processing

The design of the pixel sensors here presented has been carried out by the ATLAS SCT group at the MPP incorporating the results previously achieved and discussed in Ref. [79, 97], and following the outcome of the investigations and analysis presented in this thesis. In this section the design and the processing of the different sensor productions are described and the IV characteristics before irradiation are presented. A list of the sensor designs relevant for this thesis is summarised in Table 6.1

6.1.1 MPP/HLL productions

Two pixel productions, SOI1 and SOI2, were carried out at MPG HLL on 6-inch wafers of standard p-type FZ silicon with a resistivity of $2\,\text{k}\Omega\,\text{cm}$, using a thinning procedure developed at this facility. The layout of the wafers and the design of the structures therein included were performed at MPP in collaboration with the MPG HLL.

Thinning process

The thinning process, schematised in Figure 6.1, requires two oxidised silicon wafers: one that will be the active pixel wafer and a handle wafer. After the processing of its backside with an oxidation and boron implantation, the active wafer is directly bonded to the handle wafer which offers mechanical support during the thinning of the active area and keeps the rigidity of the structure for the subsequent processing steps [157]. The thinning to the desired active thickness is then performed from the frontside using the Chemical Mechanical Polishing (CMP) technique [158]. After thinning, the frontside is processed. As passivation layer a coating with a $3\,\mu\text{m}$ thick BCB layer was realised to avoid possible sparks between the readout chip and the sensor surface. This passivation requires an additional photolithographic process to open the

Table 6.1: Overview of the pixel productions. All sensors are made of FZ silicon except for *
which is made of MCz silicon.

Production	Resistivity [kΩ cm]	Thickness [µm]	Read-out chip	Coating	Edge distance [µm]
CiS1	10	285	FE-I3	BCB	1055 625
CiS2	15	300 200	FE-I4	BCB	460
CiS3	16	270	FE-I4	BCB	460
SOI1	2	75 150	FE-I2 FE-I3	BCB -	1055
SOI2	2	150	FE-I4	BCB	1055 465
VTT	10	200	FE-I4	-	460 125
		100	FEI-3	-	125 50 460
			FEI-4	Parylene - -	460 460 125
	2	100	FE-I4	-	125 *

electric contacts in correspondence to the positions of the Under-Bump Metallisation (UBM) pads. For applications requiring low material budget, the handle wafer can then be selectively etched away under the sensitive area with a Tetramethylammonium hydroxid (TMAH) solution up to the SiO$_2$ passivation layer that protects the active wafer. Since the sensors can be biased by applying the voltage through the handle wafer, in both MPP/HLL productions this last step was not performed.

1. Implant backside on sensor
2. Bond sensor wafer to handle wafer
3. Thin sensor side to desired thickness
4. Process on top side
5. Structure resist, etch backside up to oxide/implant
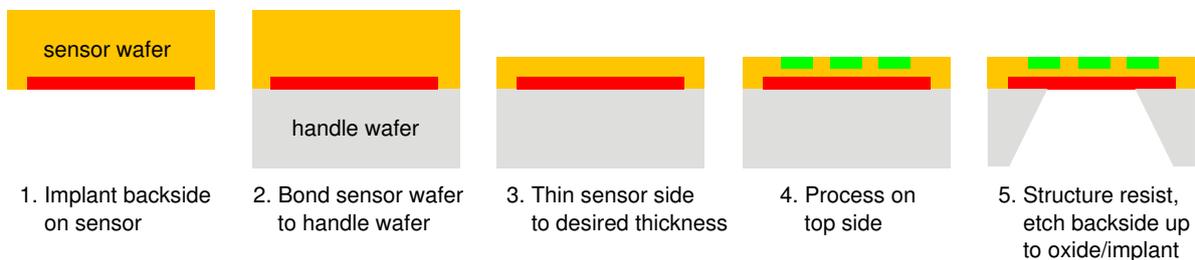
Figure 6.1: Sketch of the MPG HLL thinning process [157].

SOI1 production

The first production consists of eight wafers thinned to 75 µm or 150 µm. Each wafer contains ten ATLAS FE-I3 compatible structures which were interconnected to front-end chips through SLID. Other structures, such as strips, diodes and multi-chip modules, were implemented in this production which are not relevant for this thesis. The characterisation of pixel modules from this production and the performance of the SLID interconnection are extensively discussed and published in Ref. [79, 113]. The results obtained for 75 µm thin sensors are used in this thesis for comparison.

SOI2 production

For the second production a thickness of 150 µm was chosen to process five remaining wafers of the SOI1 production. In each wafer eight FE-I4 compatible single chip sensors and seven double chip sensors were implemented. Except for two single chip sensors which were designed with 19 guard rings, with a resulting distance between the last pixel implant and the sensor edge of d_e=1055 µm, all the other structures are characterised by a reduced edge structure of d_e=465 µm including only 11 guard rings and the bias ring. Homogeneous p-spray was used for inter-pixel isolation. Due to phosphorous contamination in the oxidation process, which compromised the quality of this production, additional implantations were required and only eleven out of thirty single chip sensors with reduced edge structure on three wafers were finally functional. The wafer layout and the IV characteristic of the repaired structures before interconnection are shown in Figure 6.2.

(a)   (b)
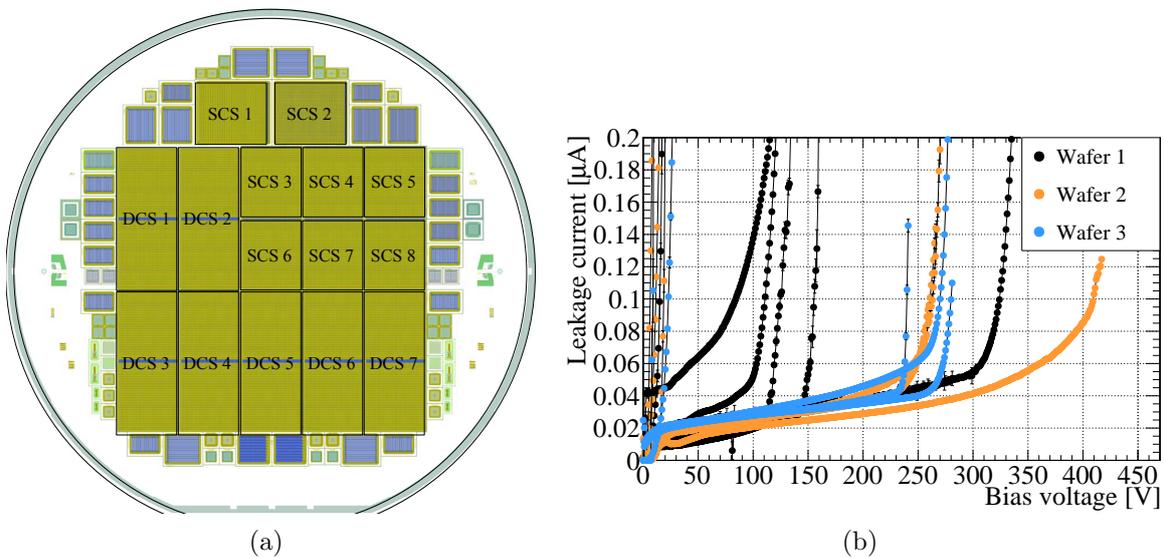
Figure 6.2: Layout of the SOI2 wafer and IV characteristics of the FE-I4 compatible structures. (a) shows the layout of the SOI2 wafer on which the FE-I4 compatible single chip sensors (SCS) and double chip sensor (DCS) structures are indicated. (b) shows the IV characteristics for the single chip sensors after UBM and BCB deposition [79].

The post-processing of the remaining good wafers was performed at the Fraunhofer Institut für Zuverlässigkeit und Mikrointegration (IZM), in Berlin, where the UBM and a 3 µm layer of

BCB were applied. As last step the single chip sensors were interconnected to front-end chips via solder bump-bonding.

6.1.2 VTT productions

A first production of n-in-p pixel sensors with active edges was completed at VTT[1] (Finland), within a multi project wafer production. This consists of 6-inch SOI wafers, with a FZ silicon active bulk, except for one wafer made of MCz silicon. The FZ wafers have an initial resistivity of $10\,\mathrm{k\Omega\,cm}$ and were thinned to $100\,\mathrm{\mu m}$ or $200\,\mathrm{\mu m}$, while the MCz wafer has an initial resistivity of $2\,\mathrm{k\Omega\,cm}$ and is $100\,\mathrm{\mu m}$ thick.

Thinning and active edge processing

The thinning process at VTT [159] is similar to the one used at MPG HLL but for the handle wafer which is completely etched at the end of the processing. After the frontside implantation the support wafer allows for etching trenches at the sensor borders using the Deep Reactive Ion Etching (DRIE) technique [160] illustrated in Figure 6.3. At the beginning of the process a photo resist mask is applied to cover the whole wafer except for the regions where the trenches need to be created. Then the etch with SF_6 is alternated with a passivation of the trench using C_4F_8. After the trenches have reached the SiO_2 layer, the boron implant of the backside of the p-type sensors is extended to the sides with a four-quadrant ion implantation as shown in Figure 6.4. Low dose homogeneous p-spray was used for inter-pixel isolation. At the end of the process, after UBM deposition, the handle wafer was completely removed and the sensors were interconnected with solder bump bonding to either FE-I3 or FE-I4 ATLAS chips.

| Photo resist | First etch (SF_6) | Passivation (C_4F_8) | Start of second etch | Second etch continues |
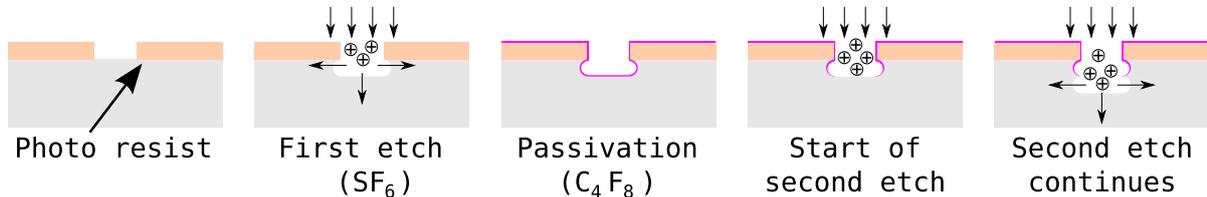
Figure 6.3: Sketch of the DRIE process [97].

Four different edge designs were implemented, which are shown in Figure 6.5: a classic design with an inactive region between the last pixel implant and the sensor edge of d_e=460 µm, which includes ten guard rings and one bias ring; a slim edge design employing only a bias ring and a similar design with an additional guard ring, both resulting in d_e=125 µm; and an active edge design with a distance between the last pixel implant and the activated edge of only d_e=50 µm with just one guard ring at floating potential. Due to the absence of bias structures in the latter design, it is not possible to test the functionality of the pixel cells before interconnection. Moreover, after bump-bonding the pixels are grounded only through the connection with the chip and a disconnected channel will cause a local modification of the electric field which may lead to a lower breakdown voltage. On the positive side, the lower hit efficiency already observed after high irradiation doses in the proximity of the punch through structure is absent in this design. The d_e=125 µm and d_e=460 µm edge designs are implemented both on FE-I4 and FE-I3

---

[1]Valtion Teknillinen Tutkimuskeskus (`http://www.vtt.fi/`)
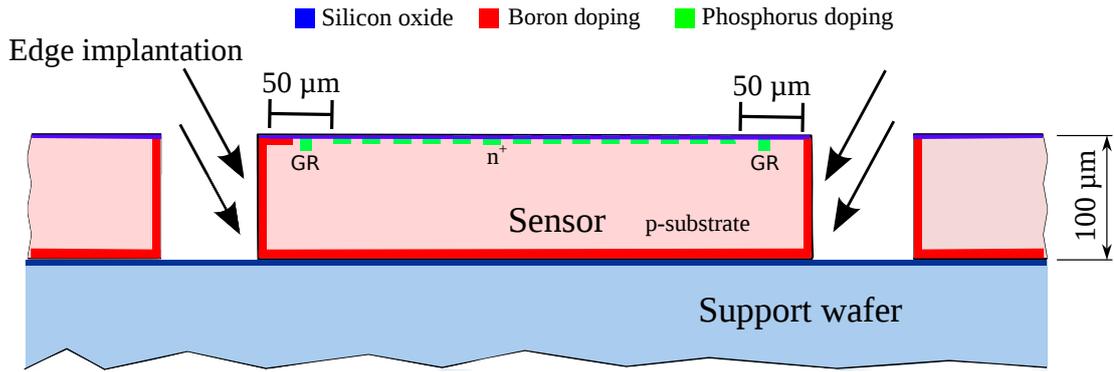
Figure 6.4: Schematic view of the sensor processing at VTT, with the four-quadrant Boron implantation in the trenches.

compatible sensors, while the most aggressive design with d_e=50 μm is only realised as FE-I3 compatible structure.

(a) d_e=460 μm   (b) d_e=125 μm   (c) d_e=125 μm   (d) d_e=50 μm
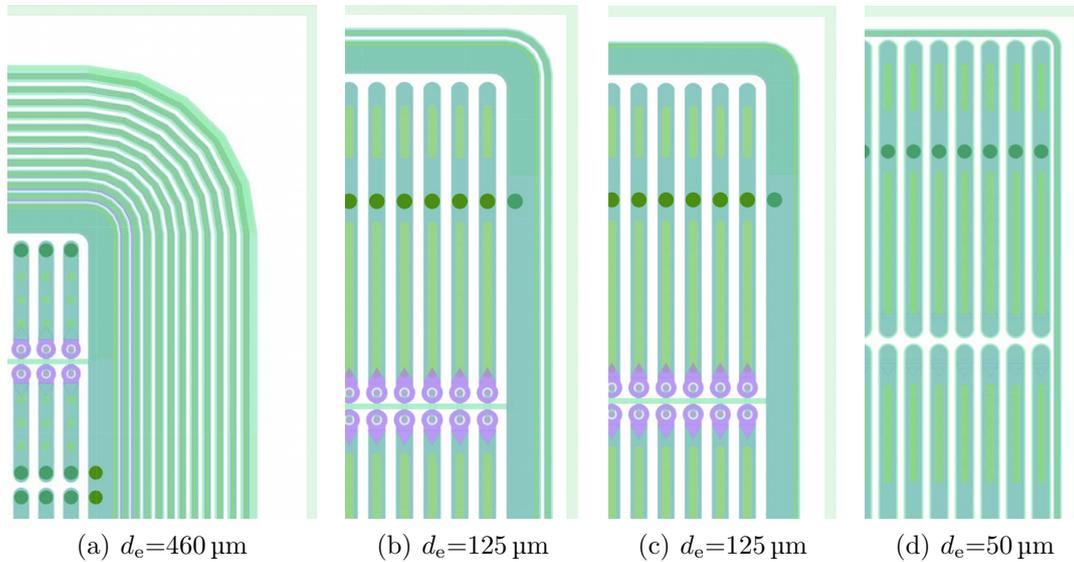
Figure 6.5: Design of the active edge structures of the VTT production. (a) shows the standard design with d_e=460 μm including ten guard rings and one bias ring. The slim edge design with d_e=125 μm which includes one bias ring and one guard ring or only one bias ring is shown in (b) and (c), respectively. (d) shows the active edge design with d_e=50 μm and just one floating guard ring.

6.1.3 CiS productions

Three productions of planar pixel sensors were carried out at CiS[2] on standard p-type FZ silicon.

CiS1 production

The first production includes eighteen 4-inch wafers with a resistivity of $10\,\mathrm{k\Omega\,cm}$ and a thickness of $285\,\mathrm{\mu m}$. Two FE-I4 and ten FE-I3 compatible pixel sensors were implemented on each wafer using a design developed by MPP and MPG HLL. Three types of guard ring schemes were realised for FE-I3 compatible sensors: one conservative design employing 19 guard rings with $d_{\mathrm{e}}{=}1055\,\mathrm{\mu m}$ and two reduced edge structures with 8 and 15 guard rings, resulting both in $d_{\mathrm{e}}{=}625\,\mathrm{\mu m}$. For the FE-I4 modules only the conservative design was adopted. All designs include bias structures and either homogeneous or moderated p-spray was used for inter-pixel isolation. The characterisation of this production was documented in Ref. [79] and these results are used in this thesis for comparison.

CiS2 production

The second CiS production was also performed on 4-inch wafers with a resistivity of $15\,\mathrm{k\Omega\,cm}$ and thicknesses of $200\,\mathrm{\mu m}$ or $300\,\mathrm{\mu m}$. The wafer layout of this production is shown in Figure 6.6. It includes six single chip sensors, FE-I4 compatible, and two double chip sensors, oriented back to back to be diced as a single piece and interconnected to four FE-I4 chips as a pseudo-quad sensor. The latter design follows the one planned for the outer layers of the ATLAS pixel detector at HL-LHC and is discussed in detail in Section 6.5.

(a) Wafer layout   (b) guard ring designs
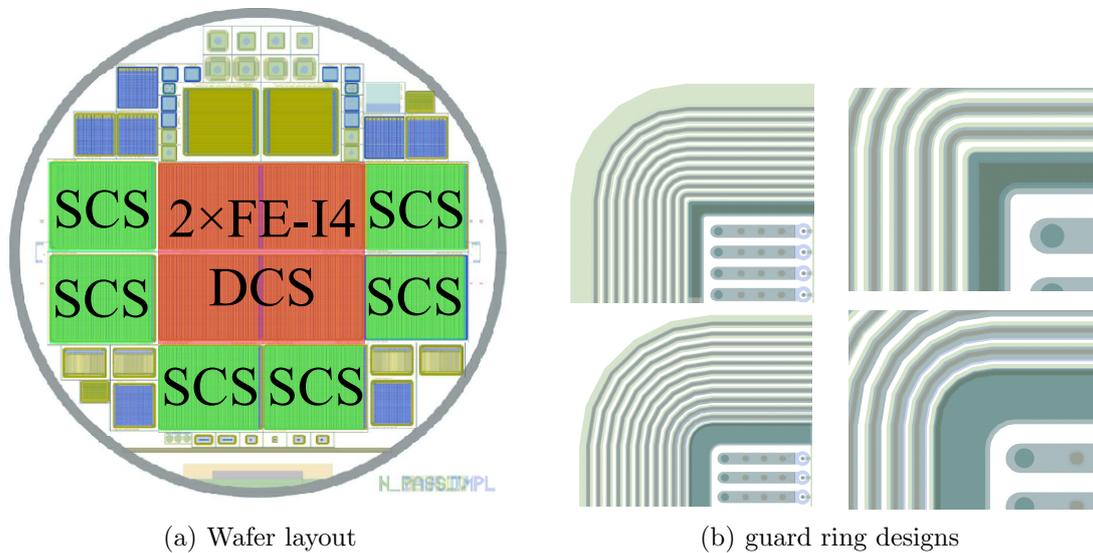
Figure 6.6: Layout of the CiS2 wafer (a): the FE-I4 single chip sensors (SCS) and the two double chip sensors (DCS) arranged as a quad sensor are indicated in green and red, respectively. (b) shows the type I (top) and type II (bottom) guard ring designs implemented for the FE-I4 compatible structures.

---

[2]CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH

Two guard ring designs were implemented for this production, which are shown in Figure 6.6(b): the type I design containing 11 guard rings, with a layout consistent with the one implemented in the SOI2 and VTT productions, together with the new type II design employing ten guard rings, which differs from the type I for the overhang of the metal layer with respect to the n^+ implant underneath, in the three inner rings. Both designs include also one bias ring and exhibit an edge distance of d_e=450 µm. Half of the single chip sensors have the type I design and half the type II, while all the quad modules have the type I design. The IV characteristics presented in Figure 6.7 show different breakdown voltages depending on the guard ring layout. Given the better performance, i.e. higher breakdown voltage, of the type II design, this was selected as standard guard ring structure for the following productions. Homogeneous p-spray with low dose boron ions on the frontside was used for inter-pixel isolation. The post processing with UBM deposition and the sensor coating with a 3 µm thick layer of BCB were performed at IZM.
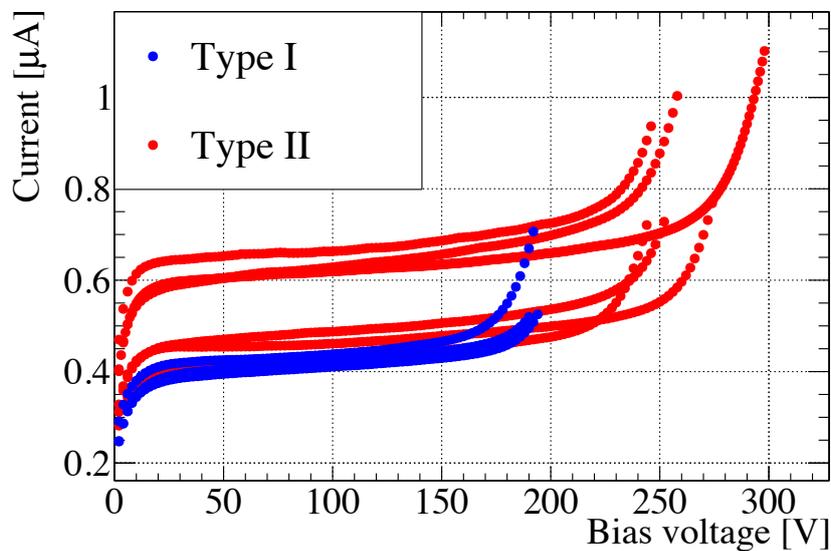
Figure 6.7: IV characteristics of the single chip sensors of the CiS2 production before irradiation.

CiS3 production

The third production was the first CiS production realised on 6-inch wafers. It consists of sixteen wafers with a resistivity of 16 kΩ cm and a thickness of 270 µm. The wafer layout for this production is shown in Figure 6.8. Each wafer contains ten single chip sensors compatible with FE-I4 chips and two quad sensors. The latter are designed to be interconnected with four FE-I4 chips and their layout will be described in detail in Section 6.5. All pixel sensors were designed with the type II guard ring introduced in the CiS2 production and one bias ring, resulting in d_e=450 µm. One single chip sensor has a new layout with (25×500) µm^2 pixel cells, which is still compatible with FE-I4 chips. In this design four pixel cells are biased with a single bias dot structure which is expected to lead to a higher overall efficiency of the sensor. Another single chip sensor layout implements new bias grid designs, reducing the inefficiency after irradiation by superimposing the bias rail on the pixel implants in such a way that the

n^+ layer can act as a screen for the ground potential of the aluminium. The BCB and UBM depositions were performed at IZM, where the modules were also interconnected to FE-I4 chips.

(a) Wafer layout

(b) Bias rail design I

(c) Bias rail design II

(d) $(25 \times 500)\,\mu m^2$ pixel cell arrangement
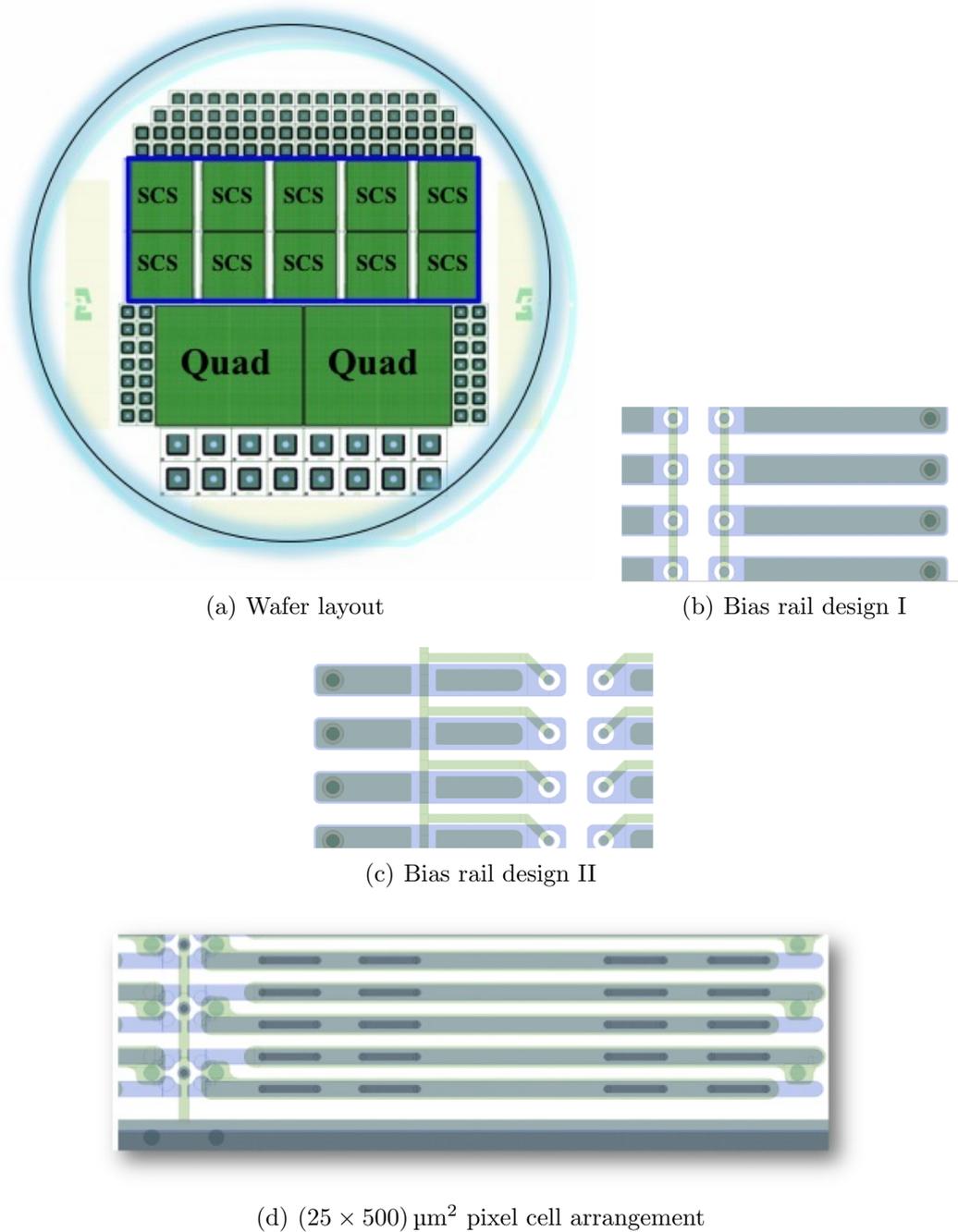
Figure 6.8: Layout of the CiS3 wafer (a), single chip sensor (SCS) and quad structures are indicated. The layout of the two new bias structures implemented in the single chip sensors is shown in (b) and (c). A detail of the FE-I4 compatible single chip sensors with a $(25 \times 500)\,\mu m^2$ pixel cell arrangement is illustrated in (d).

6.2 Irradiations

To study the radiation hardness of the various sensor designs and thicknesses, different facilities, described in Section 4.7, were used to perform the necessary irradiations. For a better comparison of the results obtained from sensors irradiated with different particles, the radiation doses are expressed in 1 MeV equivalent neutron fluences as discussed in Section 2.2.1. To avoid a harsh annealing during the bump-bonding process, which requires high temperatures, most sensors have been irradiated after interconnection to readout chips. Since the readout chip itself is sensitive to high radiation doses, it limits the choice of the irradiation facilities depending on the desired fluence. The radiation damage for chips is higher for ionising particles in particular if their energies are significantly lower than the minimum energy loss. Hence, at KIT, where irradiations are performed with low energy protons, a maximum fluence of 2 and $5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ was used with FE-I3 and FE-I4 chips, respectively. To reach radiation fluences closer to the one expected for the innermost layer of ATLAS at HL-LHC, FE-I3 modules can only be irradiated with reactor neutrons at JSI, while FE-I4 chips have demonstrated a good radiation hardness up to $14 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ also with 800 MeV protons at LANSCE. An overview of the irradiations performed for single chip modules is presented in Table 6.2. The irradiations of the quad modules and the new sensors designed in the CiS3 production are discussed in Section 6.5 and 6.6, respectively.

Table 6.2: Overview of the irradiated single chip modules. All sensors are made of FZ silicon except for * which is made of MCz silicon. Sensors marked with † have been irradiated and measured only before interconnection to readout chips.

Production	Readout chip	Thickness [µm]	Edge distance [µm]	Irradiation site	Fluence [$10^{15}\,\mathrm{n_{eq}/cm^2}$]	
SOI2	FE-I4	150	475	KIT	2	
				LANSCE	4	
				JSI	10	
VTT	FE-I4	200	460	KIT+JSI	2+4	
		100	460	KIT	5	
				JSI	10	†
			125	KIT+KIT	2+3	*
	FE-I3	100	125	KIT+JSI	1+4	
			50	JSI	2	
CIS2	FE-I4	200	450	KIT	2	
					5	
				JSI	10	†
					13	†
				LANSCE	7	
					14	
		300	450	LANSCE	14	

6.2.1 Different silicon materials

The charge collection properties of FZ and MCz silicon sensors from the VTT production are compared in Figure 6.9. Before irradiation, the only difference between the two materials is in the depletion voltage. Due to its higher resistivity, the FZ sensor depletes around 20 V, while the MCz sensor needs 30 V to reach the full depletion. After irradiation to a fluence of $5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$, no particular benefit is observed for the MCz material. Since the two materials show compatible behaviours even after high radiation doses, their results will be used indistinctly in the following.
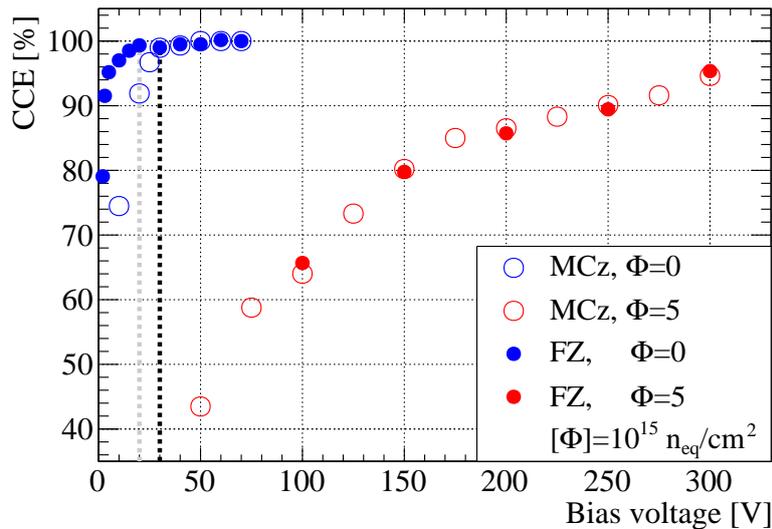
Figure 6.9: Comparison of the CCE for FZ and MCz silicon sensors from the VTT production before and after irradiation to a fluence of $5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$. Both modules are FE-I4 assemblies with 100 μm active thickness. The CCE is calculated with respect to the collected charge measured for each device before irradiation at V_b=70 V. The gray and black lines show the depletion voltage before irradiation of the FZ and MCz sensors, respectively. The uncertainties are statistical and smaller than the marker size.

6.2.2 IV characteristics

The IV characteristics of irradiated modules from different productions are measured in a climate chamber with an environmental temperature of $-50°$C without powering the chip. The results for single chip modules of the SOI2 and the CiS2 productions are shown in Figure 6.10. After irradiation, the leakage current and the breakdown voltage of the sensors increase considerably. As before irradiation, the sensors of the CiS2 production show a higher current than the SOI2 production for similar radiation fluences up to $5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$, given their larger thickness and the linear dependence of the leakage current on the depleted volume. The expected linear increase of the leakage current with the radiation fluence after full depletion (see Section 2.2) is observed up to $5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ for both productions. As discussed in Section 2.2 and also shown in Figure 6.10(b), small deviations from the linearity of this relation can be associated to

different annealing times, which are expected for the various modules, due to different periods spent at room temperature during shipping and wire bonding. The leakage currents for the three CIS2 modules at fluences of 7 and $14 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ are lower than expected, since the nominal fluence was reached only for a fraction of the sensor area, due to the inhomogeneous irradiation, as explained in Section 4.7.3. The sensor irradiated to a fluence of $10^{16}\,\mathrm{n_{eq}/cm^2}$ was measured on the probe station at a temperature of $-40\,^\circ\mathrm{C}$ and its IV curve is rescaled to $-50\,^\circ\mathrm{C}$ for better comparison with the other results. All modules of these two productions were coated with BCB to avoid sparks between the sensor and the readout chip. After irradiation, for sensors out of the SOI2 production, a breakdown exceeding $550\,\mathrm{V}$ is observed, while for the sensors from the CiS2 production no breakdown is observed up to $700\,\mathrm{V}$ and some sensors were operated even up to $900\,\mathrm{V}$.

(a) CiS2   (b) SOI2
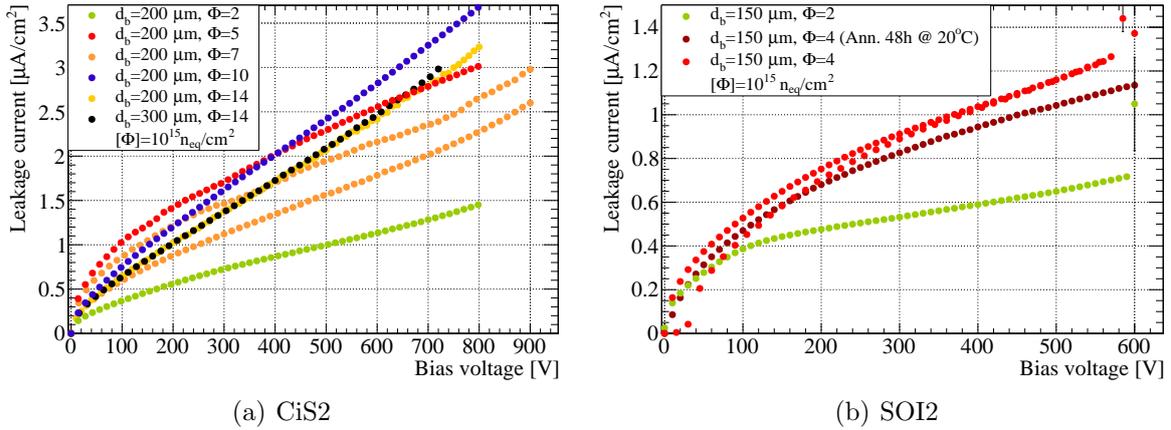
Figure 6.10: Leakage current as a function of the bias voltage of the irradiated FE-I4 sensors from the CiS2 (a) and SOI2 (b) productions. To avoid damage of the modules due to sparks between the sensor and the chip at high voltages, the IV curves for the CiS2 sensors were stopped before the breakdown. For the CiS2 modules irradiated at LANSCE to a fluence of 7 and $14 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$, the quoted fluence correspond to the irradiation of less than half of the module. All uncertainties are statistical and smaller than the marker size. Image (b) is adapted from Ref. [79].

For the active edge sensors of the VTT production the IV curves, before and after different irradiation steps, are shown in Figure 6.11. Before irradiation the sensors with only one bias ring or guard ring have a V_{bd} between 100 and $150\,\mathrm{V}$, which is well above the full depletion voltage of around $15\,\mathrm{V}$ expected from the high bulk resistivity. The sensors with a full guard ring structure have instead a higher V_{bd}, between 150 and $250\,\mathrm{V}$. After irradiation, the difference in terms of breakdown voltage for the different edge structures becomes larger. Sensors with $d_{\mathrm{e}}{=}450\,\mathrm{\mu m}$ and ten guard rings can be operated up to $500\,\mathrm{V}$ while sensors with $d_{\mathrm{e}}{=}125\,\mathrm{\mu m}$ have a V_{bd} between 250 and $350\,\mathrm{V}$, still higher than the voltage at which the charge saturation is expected for these fluences (as observed in the charge collection measurements in Figure 6.13). The sensor with the more aggressive $50\,\mathrm{\mu m}$ active edge design shows instead a lower $V_{\mathrm{bd}}{=}180\,\mathrm{V}$ after irradiation to a fluence of $2 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$, which is just at the beginning of the charge saturation. Since no BCB layer was applied for this production, after irradiation a lower V_{bd}, with respect to the SOI2 and the CiS2 sensors, is observed even for structures which employ the design with ten guard rings.

(a) Before irradiation

(b) After irradiation
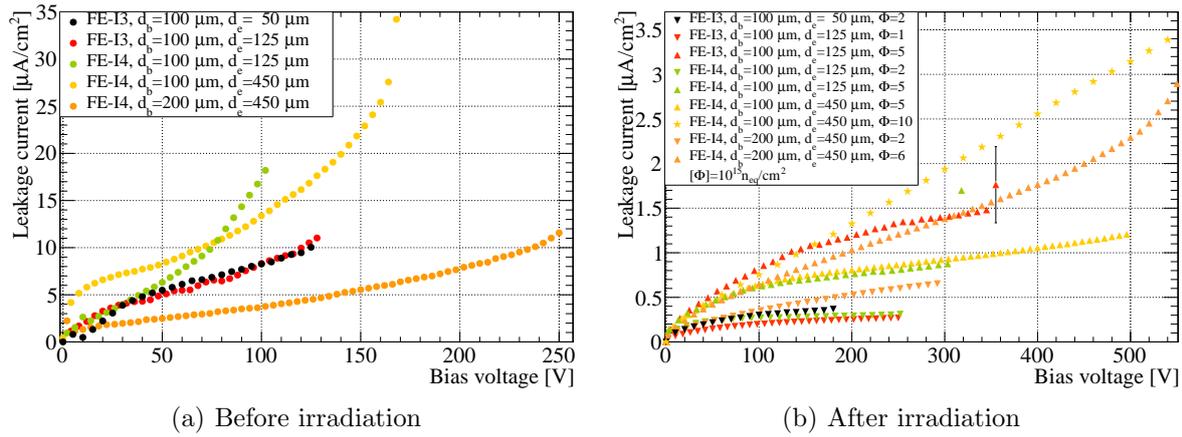
Figure 6.11: Leakage current as a function of the bias voltage for VTT sensors of different designs before (a) and after irradiation (b). With the exception of the sensor with d_e=50 μm, the IV curves after irradiation for $\Phi \leq 2 \times 10^{15}\,n_{eq}/cm^2$ were stopped shortly before their V_{bd} to avoid sparks between the sensor and the chip. The breakdown for the 100 μm thick sensors irradiated to a fluence of $10 \times 10^{15}\,n_{eq}/cm^2$ is not shown in the picture and occurs at $V_b = 800\,V$. Where not visible, the statistical uncertainties are smaller than the marker size.

One FE-I4 module employing a 100 μm thick sensor with standard guard ring design from the VTT production was coated with parylene-C at IZM and then irradiated to a fluence of $5 \times 10^{15}\,n_{eq}/cm^2$ at KIT. Differently than the BCB, parylene-C is applied after the assembly of the module, with a thickness of 5 μm per side, and it penetrates only into the opening between the chip and the sensor for a depth of about 100 μm. The comparison of the IV curves with an uncoated sensor, irradiated at the same fluence, is presented in Figure 6.12. The two sensors have similar values of V_{bd} before irradiation, while after irradiation the coating allows to extend the operating voltage by almost 300 V resulting in $V_{bd} \geq 800\,V$. A similar value to the one observed with BCB for the CiS productions.

6.3 Thin sensors

With the design of readout chips capable of handling small signals, hybrid pixel modules employing thin silicon sensors become of great interest for high energy physics experiments. Thin sensors are radiation hard, because of the small distance between the electrodes which increases the electric field and reduces the mean collection path of the charge carriers leading to a lower trapping. They also require a lower bias voltage both before, and especially after irradiation to achieve the charge saturation. Moreover, the higher electric field close to the collecting electrodes can lead to charge multiplication for heavily irradiated modules [161–163]. Along with the radiation hardness, thin sensors also offer low material budget and, therefore, reduced multiple scattering allowing a more precise track reconstruction. Another advantage is the low occupancy for tilted tracks which is particularly important in the high-η region of the detector, where particles are crossing several pixels along their x dimension. In this section, the different properties of thin sensors are investigated and their performance in terms of charge collection and hit efficiency are compared to thicker sensors.
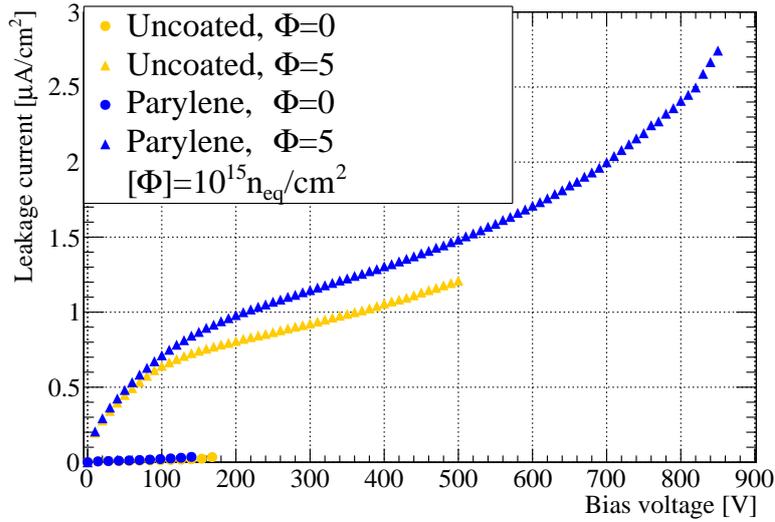
Figure 6.12: Comparison of the IV characteristics before and after irradiation for two FE-I4 modules from the VTT production employing $100\,\mu m$ thick sensors with the standard edge design, one with and one without parylene-C coating. The results before and after irradiation to a fluence of $5 \times 10^{15}\,n_{eq}/cm^2$ at KIT are shown. All uncertainties are statistical and smaller than the marker size.

6.3.1 Charge collection

The absolute collected charge of different sensor thicknesses was measured up to a fluence of $10^{16}\,n_{eq}/cm^2$ and results are compared in Figure 6.13. After irradiation the collected charge of very thin sensors ($\leq 100\,\mu m$) starts to saturate at around $200\,V$ both at a fluence of $2 \times 10^{15}\,n_{eq}/cm^2$ and at $5 \times 10^{15}\,n_{eq}/cm^2$, while thicker sensors are still under depleted. At a fluence of $2 \times 10^{15}\,n_{eq}/cm^2$, sensors with a thickness between 100 and $200\,\mu m$ show the highest collected charge at moderate voltages (between 200 and $300\,V$), while thicker sensors need at least $600\,V$ to reach a sufficient depleted region to reach comparable results. On the other hand, the $75\,\mu m$ thick sensors, even if fully depleted, show a collected charge which saturates between 4 and $5\,ke$, giving the smallest absolute collected charge among the tested thicknesses. At a fluence of 4–$5 \times 10^{15}\,n_{eq}/cm^2$, among the measured thicknesses, the 100 and $150\,\mu m$ thick sensors collect the highest charge of almost $6\,ke$ at $V_b = 300\,V$, nearly $2\,ke$ more than the $200\,\mu m$ thick sensors which require at least $500\,V$ to obtain a similar result. With respect to the other thicknesses, $75\,\mu m$ thick sensors and $285\,\mu m$ thick sensors have always a lower collected charge up to $600\,V$. Increasing the fluence to $10^{16}\,n_{eq}/cm^2$, the collected charge of thin and thick sensors for moderate voltages becomes similar. The signal of $150\,\mu m$ thick sensors does not saturates up to $500\,V$, but this sensor thickness still shows the higher charge up to this bias voltage when compared to 75 and $285\,\mu m$ thick sensors.

Further irradiations of FE-I4 modules from the CiS2 production were performed at LANSCE to fluences of 7 and $14 \times 10^{15}\,n_{eq}/cm^2$. Due to the limitation of this irradiation facility discussed in Section 4.7.3, no uniform irradiation for these modules was achieved. The analysis is therefore restricted to the central area of the irradiation beam spot where a more uniform fluence was estimated as discussed in Section 4.7.3. Figure 6.14 shows the result of the measured collected

(a) $\Phi=2 \times 10^{15} \, \mathrm{n_{eq}/cm^2}$

(b) $\Phi=2 \times 10^{15} \, \mathrm{n_{eq}/cm^2}$

(c) $\Phi=4\text{--}5 \times 10^{15} \, \mathrm{n_{eq}/cm^2}$

(d) $\Phi=4\text{--}5 \times 10^{15} \, \mathrm{n_{eq}/cm^2}$
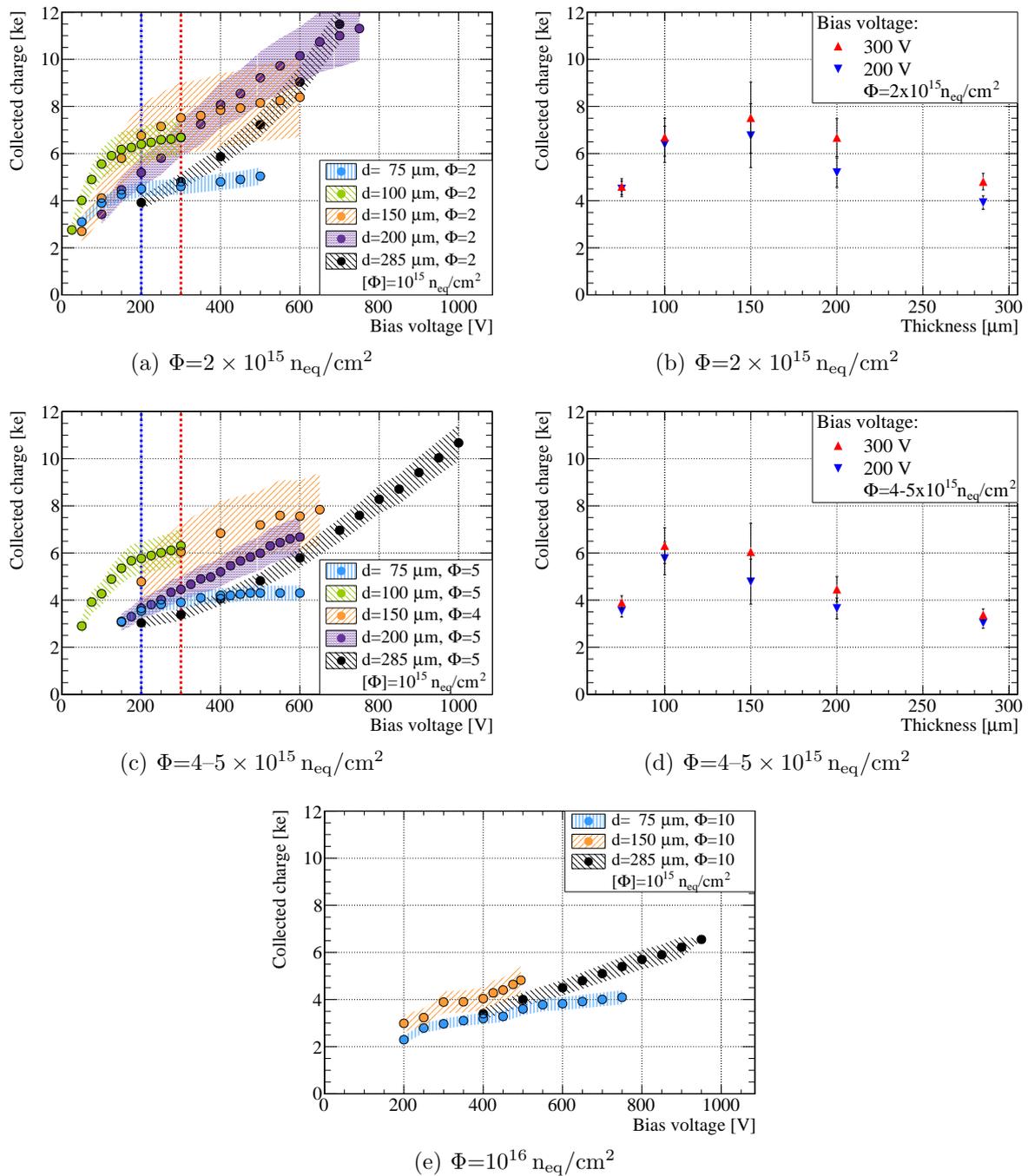
(e) $\Phi=10^{16} \, \mathrm{n_{eq}/cm^2}$

Figure 6.13: Overview of the charge collection for irradiated pixel modules of different thicknesses. The results at a fluence of 2×10^{15} and $2 \times 10^{15} \, \mathrm{n_{eq}/cm^2}$, $4\text{--}5 \times 10^{15} \, \mathrm{n_{eq}/cm^2}$ and $10^{16} \, \mathrm{n_{eq}/cm^2}$ are shown in (a), (c), (e), respectively. The collected charges at $V_\mathrm{b} = 200 \, \mathrm{V}$ and $300 \, \mathrm{V}$ for the different sensor thicknesses of (a) and (c) are highlighted in (b) and (d), respectively. All the results for 75 and 285 μm thick sensors and the results for 150 μm thick sensors in (a, b, c, d) are taken from Ref. [79].

charge for 200 and 300 μm thick sensors. At a fluence of $2 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ the collected charge saturation starts around 700 V, while no charge saturation is observed for these thicknesses after irradiation to higher fluences even at the maximum applied voltages. At fluences higher than $5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$, a bias voltage of more than 500 V is required to obtain a charge above 5 ke. At the highest fluence of $14 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$, the collected charge of the 200 and 300 μm thick sensors becomes very similar and at the highest measured voltage of 1000 V is between 5 ke and 5.5 ke.

(a) Collected charge vs bias voltage   (b) Collected charge vs fluence
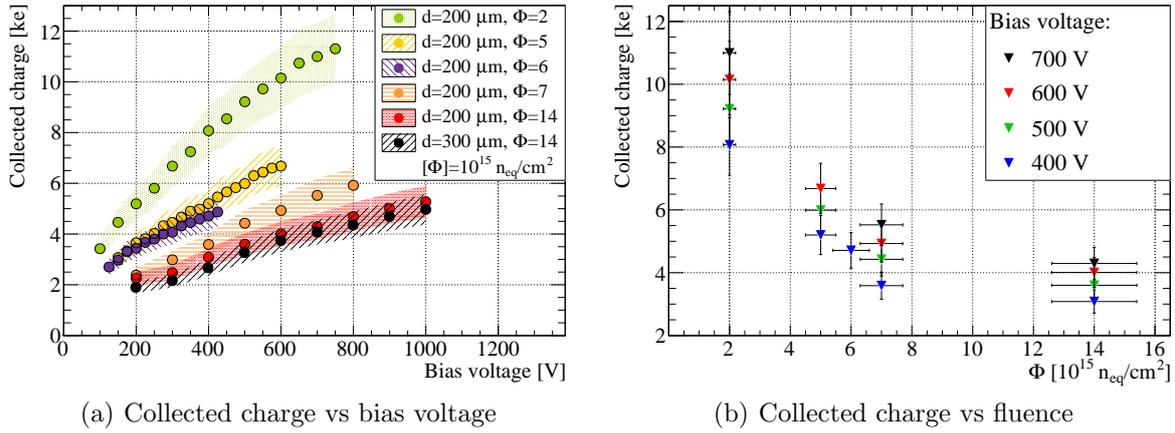
Figure 6.14: Charge collection of 200 and 300 μm thick sensors as a function of the bias voltage for different fluences (a) and as a function of the fluence for different bias voltages (b). All sensors are from the CiS2 production except for the sensor irradiated to $6 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ which is from the VTT production.

Figure 6.15 shows the charge collection for 100 μm thick sensors. At a radiation fluence of $1\text{–}2 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ the collected charge starts its saturation at $V_\mathrm{b} = 150\,\mathrm{V}$, reaching a collected charge of almost 6.5 ke at $V_\mathrm{b} = 300\,\mathrm{V}$. At a fluence of $5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ a moderate voltage between 200 and 300 V is sufficient to obtain a collected charge of about 6 ke. As discussed in Section 6.2, this result is valid both for FZ and MCz sensor materials.

6.3.2 Hit efficiency

A critical aspect for tracking devices after high radiation doses is the hit efficiency. A low hit efficiency of the modules in the ITk would affect the precision of track and vertex reconstruction and the overall particle detection efficiency and fake track rejection. After high radiation fluences, the main cause of inefficiency is the decrease of the collected charge in the sensor due to trapping and partial depletion of the bulk. As the MPV of the collected charge gets closer to the threshold of the chip, the probability of a missing hit increases. This could lead to just a degradation of the tracking resolution of the device, if the particle hit is still detected by at least one pixel, or to a complete inefficiency of the detector in case none of the pixels traversed by the particle gives a hit. The hit efficiency of pixel modules after irradiation was measured in beam test experiments both at DESY and SpS facilities. The high resolution of these measurements allows to study not only the performance of the entire module, but also the properties of different structures inside the sensor with a precision of a few microns. In this

(a) Collected charge vs bias voltage

(b) Collected charge vs fluence
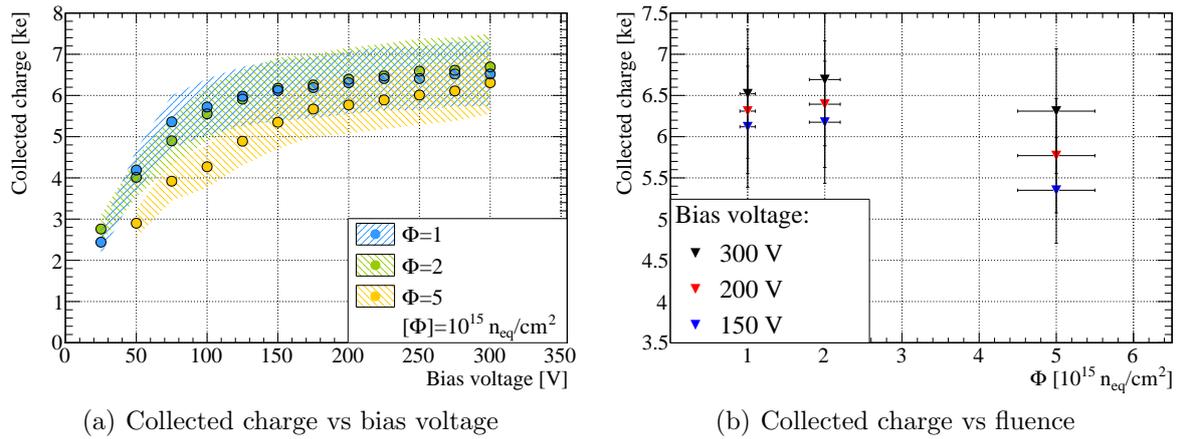
Figure 6.15: Charge collection of $100\,\mu m$ thick sensors as a function of the bias voltage for different fluences (a) and as a function of the fluence for different bias voltages (b). All the sensors are from the VTT production.

section the results obtained for the different sensor productions and thicknesses are presented and compared.

For the $150\,\mu m$ thick sensors of the SOI2 production, the hit efficiency at different bias voltages and radiation fluences was measured at SpS and is shown in Figure 6.16. For tracks perpendicular to the sensor surface, the hit efficiency drops from $99.9\,\%$[3] at a fluence of $2 \times 10^{15}\,n_{eq}/cm^2$. At a fluence of $4 \times 10^{15}\,n_{eq}/cm^2$ an efficiency of $97.7\,\%$ is still obtained when increasing the bias voltage to $V_b = 690\,V$. Figure 6.16(b) shows that the main inefficiency regions inside the single pixel cell at this fluence are located at the bias dot area and near the bias rail. This is due to the fact that a fraction of the charge carriers drifts towards these structures, which are kept at ground potential and not connected to the readout. This effect is much reduced for inclined tracks: tilting the module by $\phi = 15°$, a hit efficiency of $98.3\,\%$ at $V_b = 650\,V$ is measured. Other regions where a lower hit efficiency is observed are the corners of the pixel cell, where the energy released by crossing particles is shared among four pixels. In the central part of the pixel cell highlighted in Figure 6.16(b), which excludes these critical areas, a hit efficiency of more than $99\,\%$ is observed already at $V_b = 400\,V$ and it saturates around $99.7\,\%$ for $V_b > 500\,V$.

Figure 6.17 shows the hit efficiency, measured at DESY, of VTT modules irradiated to a fluence of 5–$6 \times 10^{15}\,n_{eq}/cm^2$. For $200\,\mu m$ thick sensors the hit efficiency at a fluence of $2 \times 10^{15}\,n_{eq}/cm^2$ increases from $98.0\,\%$ at $V_b = 200\,V$ up to $98.9\,\%$ at $V_b = 350\,V$. After irradiation to a fluence of $6 \times 10^{15}\,n_{eq}/cm^2$, a maximum hit efficiency of $96.9\,\%$ is measured at $V_b = 500\,V$. The FE-I4 modules with $100\,\mu m$ thick sensors from the same production show instead a hit efficiency between 97.0 and $97.2\,\%$ at a fluence of $2 \times 10^{15}\,n_{eq}/cm^2$. Similar results are obtained also after irradiation to the higher fluence of $5 \times 10^{15}\,n_{eq}/cm^2$ with $V_b > 200\,V$, where the hit efficiency starts to saturate between 97.0 and $97.4\,\%$. Also in this case, the region with reduced efficiency after irradiation corresponds to the bias dot and bias rail areas. As shown in Figure 6.17(b), because of the smaller fraction of area that this structure occupies for the FE-I3 module, the latter shows a higher hit efficiency with respect to the FE-I4 module irradiated at the same fluence of $5 \times 10^{15}\,n_{eq}/cm^2$. Restricting the analysis to the central area

---

[3]An absolute systematic uncertainty of $0.3\,\%$ before irradiation to $98.8\,\%$ is associated to all hit efficiency measurements in this thesis as discussed in Section 4.5.4.

(a) Hit efficiency   (b) Pixel cell efficiency
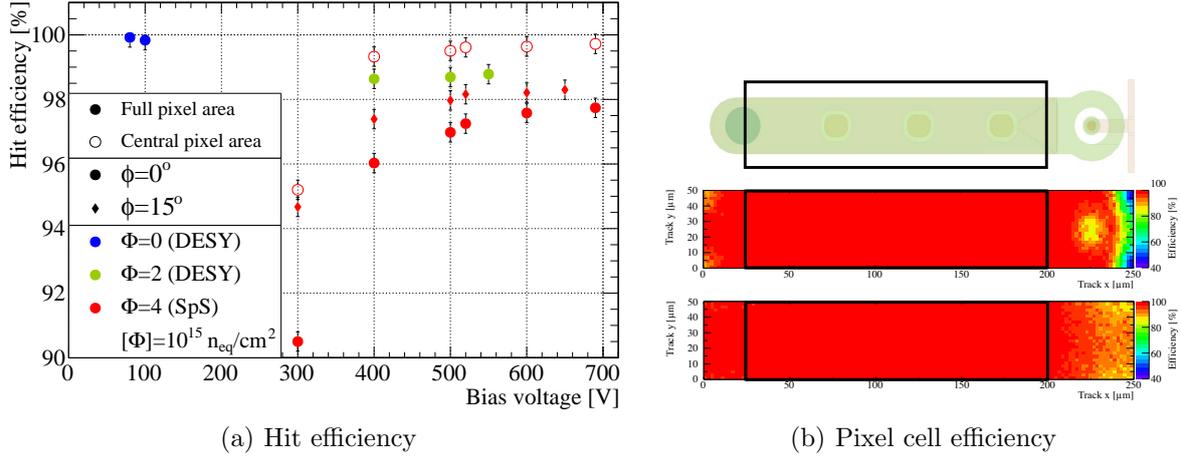
Figure 6.16: Hit efficiency of the FE-I4 modules with 150 μm thick sensors from the SOI2 production. In (a) the hit efficiency as a function of bias voltage is shown for different radiation fluences. The filled symbols denote the hit efficiency of the full pixel cell, while the open symbols denote the hit efficiency in the central region of pixel cell defined by the black rectangles in (b). At the highest radiation fluence of $4 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ the hit efficiency at perpendicular beam incidence is compared to measurements where the module is tilted by an angle $\phi=15°$ around its y axis with respect to the beam incidence. (b) shows the corresponding hit efficiency across the pixel surface at the highest measured voltage, at $V_\mathrm{b} = 690\,\mathrm{V}$ for perpendicular incident tracks (top) and at $V_\mathrm{b} = 650\,\mathrm{V}$ for $\phi=15°$ tilted tracks (bottom). The modules were tuned to a threshold of 1.6 ke for the measurements after irradiation and with a threshold of 2.5 ke before irradiation. The hit efficiency maps of the pixel cells are obtained displaying the reconstructed track impact point expressed in pixel coordinates and projecting the data for all identical structures onto the same image.

of the pixel cell, i.e. excluding the biasing regions and the area of charge sharing between four adjacent pixels, the FE-I3 and FE-I4 sensors irradiated to the same fluence show consistent results with a saturation of the hit efficiency around 99.7 % at $V_\mathrm{b} = 300\,\mathrm{V}$.

The hit efficiency for 200 μm thick modules of the CiS2 production irradiated at LANSCE is shown in Figure 6.18. At a fluence of $7 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ the hit efficiency starts to saturate at around 600 V and reaches a maximum value of 97.2 % at $V_\mathrm{b} = 800\,\mathrm{V}$. For the highest radiation fluence of $14 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ no saturation of the hit efficiency is observed up to this voltage and a hit efficiency of only 89.4 % is measured.

The final comparison of the hit efficiency for different sensor thicknesses is shown in Figures 6.19 and 6.20. At a fluence of $2 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ the modules employing 150 and 200 μm thick sensors still show a better hit efficiency than the 100 μm thck sensors, which are mainly limited by the lower collected charge near the biasing structures. With an radiation fluence between 4 and $6 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ FE-I4 modules with 150 and 200 μm thick sensors show similar performances reaching a hit efficiency of about 97 % at V_b=500 V, while the same module type with 100 μm thick sensor starts to saturate to this value already at $V_\mathrm{b} = 300\,\mathrm{V}$. Figure 6.20(b) compares the hit efficiency measured in the centre of the pixel cell for the different thicknesses and

(a) 200 μm

(b) 100 μm

(c) Pixel cell efficiency: FE-I3 vs FE-I4
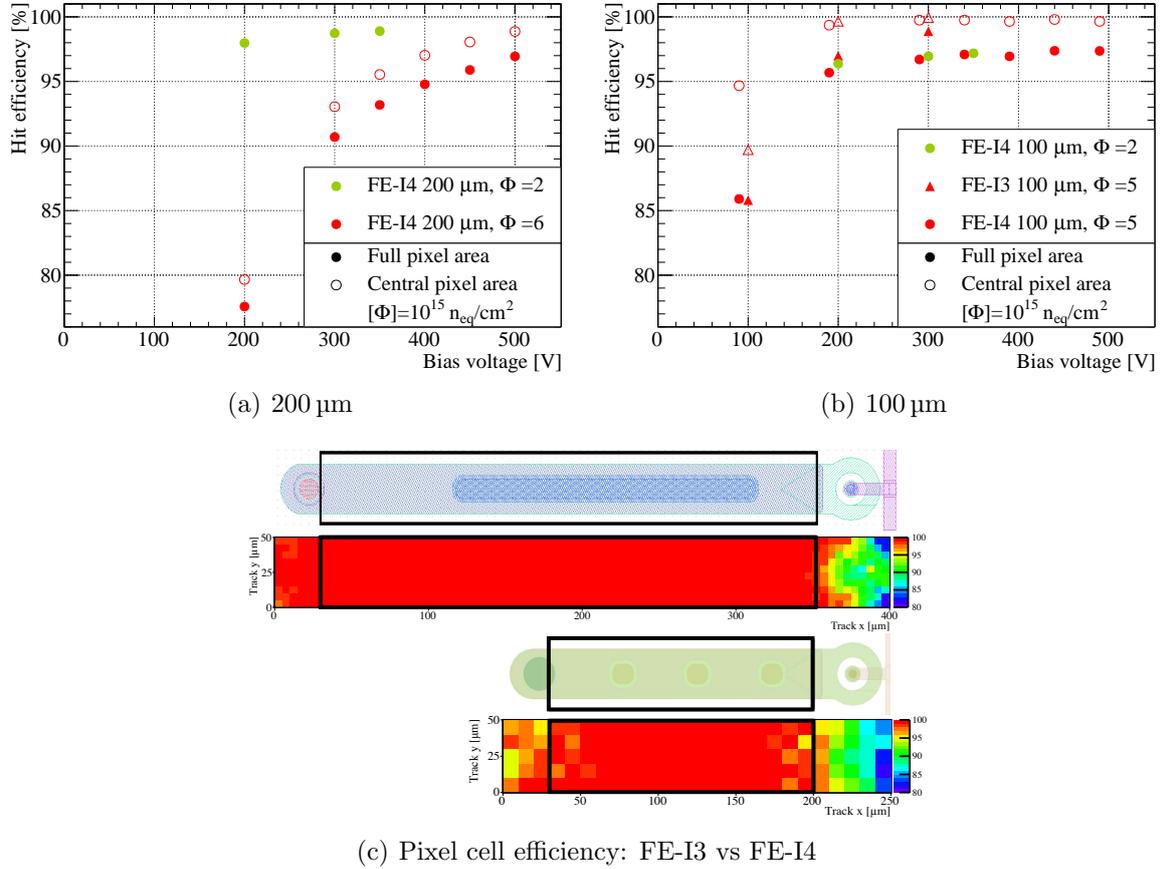
Figure 6.17: Hit efficiency for VTT modules irradiated to different fluences. The hit efficiency as a function of V_b is shown in (a) for 200 μm thick sensors and in (b) for 100 μm thick sensors. The full symbols represent the hit efficiency of the full module. The open symbols are the hit efficiency calculated for the central area of the pixel cell as represented by the black boxes in (c). For better visibility the red circles in (b) are displaced by −10 V. The hit efficiency measured at the highest voltage and fluence is shown in (c) for the pixel cell of the FE-I3 (top) and the FE-I4 (bottom) modules with 100 μm thick sensors. The 100 μm thick FE-I3 and the two 100 and 200 μm thick FE-I4 modules were tuned to a threshold of 1.5, 2.3 and 1.6 ke, respectively. The hit efficiency maps of the pixel cells are obtained displaying the reconstructed track impact point expressed in pixel coordinates and projecting the data for all identical structures onto the same image. A different binning was chosen according to the pointing resolution of the telescope.

(a) $\Phi = 7 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$

(b) $\Phi = 14 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$

(c) Hit efficiency vs bias voltage
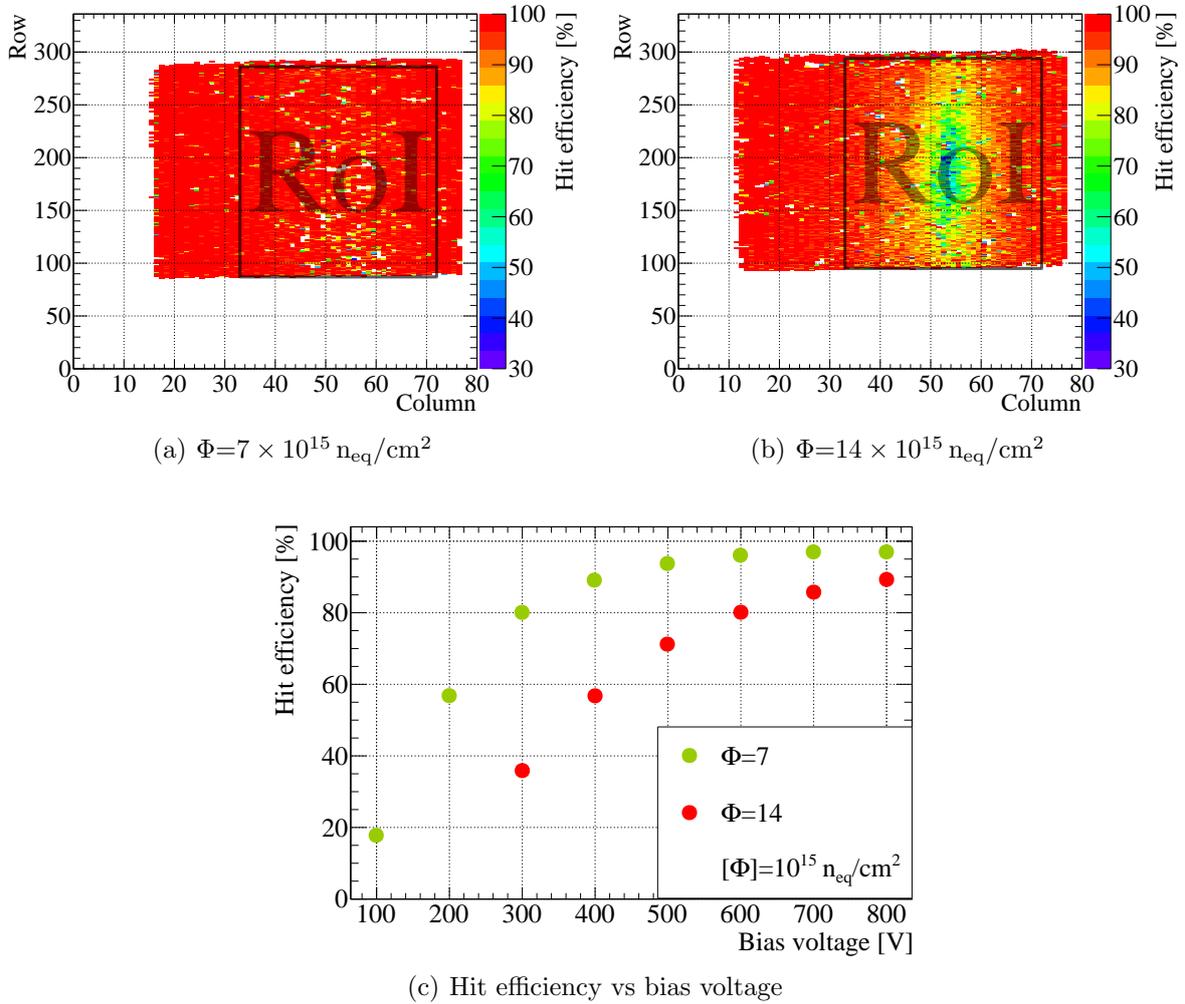
Figure 6.18: Hit efficiency of the $200\,\mu\mathrm{m}$ thick CiS2 modules irradiated at LANSCE. The distribution of the hit efficiency over the sensor surface at a voltage of $800\,\mathrm{V}$ is shown for the modules irradiated to a fluence of $7 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ in (a) and $14 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ in (b). For each module the RoI considered for the analysis is highlighted. The hit efficiency as a function of V_b calculated for the RoI is shown in (c). The modules were operated at a threshold of 1.6 ke. The measurements performed at DESY are taken from Ref. [79].

demonstrates again that bias dot and bias rail are the main limitations for thin sensors after irradiation: in fact the $100\,\mu m$ thick sensors show a hit efficiency of $99.7\,\%$ already at $V_b = 200\,V$ which saturates to $99.9\,\%$ for larger bias voltages, while thicker sensors still require more than $500\,V$ to reach similar efficiencies. A summary of the estimated operational voltages for the different sensor thicknesses according to the measured hit efficiency saturation is given in Table 6.3.
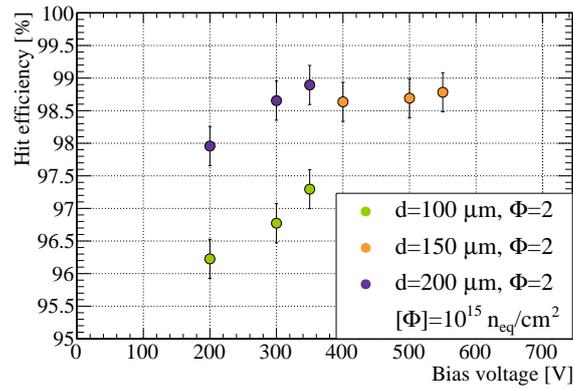
Figure 6.19: Hit efficiency as a function of V_b for FE-I4 pixel modules of different thicknesses irradiated to a fluence of $2 \times 10^{15}\,n_{eq}/cm^2$. Results for $150\,\mu m$ thick sensors are taken from Ref. [79].

(a) Full pixel area

(b) Central pixel area
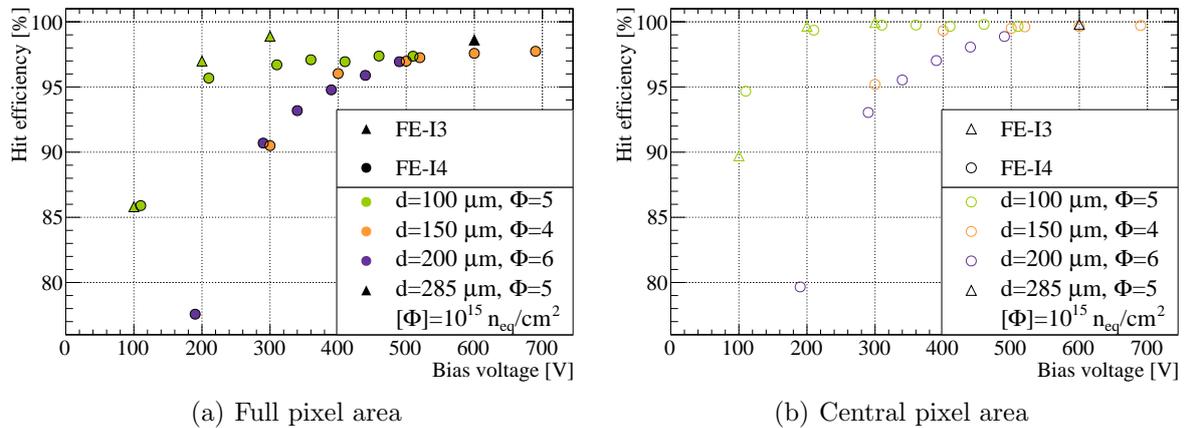
Figure 6.20: Hit efficiency as a function of V_b for pixel modules of different thicknesses irradiated to a fluence of 4–$6 \times 10^{15}\,n_{eq}/cm^2$. The hit efficiency measured over the entire module is shown in (a), while the hit efficiency calculated in the central pixel area is shown in (b). For better visibility the green circles are displaced by $+10\,V$ and the purple circles by $-10\,V$. Results for $285\,\mu m$ are taken from Ref. [79].

Table 6.3: Estimated operational voltages for the different sensor thicknesses according to the measured hit efficiency saturation. The values are estimated for the full (central) pixel area.

Thickness [µm]	Fluence [$10^{15}\,n_{eq}/cm^2$]	Saturation voltage [V]	
100	2	≥ 350	
	5	350	(300)
150	2	400	
	4	520	(520)
200	2	≥ 350	
	6	≥ 500	(≥ 500)
	7	700	
	14	≥ 800	

6.3.3 Power dissipation

To operate in the ATLAS detector, pixel modules have to fulfil the requirements imposed by the cooling system. The power dissipation of the sensors P_S depends on the leakage current I and the bias voltage as:

$$P_S = I \cdot V_b \tag{6.1}$$

As already discussed in Section 2.2, the leakage current rises with the radiation fluence, leading to a consequent increase of the sensor power. If the cooling system is not able to absorb the additional heat, the sensor goes in thermal runaway. Since this effect limits the achievable operational voltage of the modules, it has to be considered together with the hit efficiency results presented in the previous section, to determine the practical performance of the different sensor thicknesses. In this section the constraints set by power dissipation and thermal runaway on highly irradiated sensors are investigated using as reference the CO_2 cooling system of IBL [36].

In addition to the power dissipation of the sensor, the main parameters which affect the sensor temperature are the power dissipation of the chip P_{FE}, the thermal conductivity of the stave, characterised by its thermal figure of merit Γ_s, which describes the temperature increase of the stave per power density of the attached module, and the evaporation temperature of the coolant T_c. For CO_2, the typical T_c ranges from $-30\,°C$ to a minimum of about $-40\,°C$ depending on the achievable pressure in the pipes [164]. The sensor power at different temperatures T is obtained from the IV curves measured at $T_0 = -50\,°C$ and presented in Section 6.2.2 according to:

$$I = I_0 \left(\frac{T}{T_0}\right)^2 \exp\left(\frac{E_g}{2k_B}\left(\frac{1}{T_0} - \frac{1}{T}\right)\right) \tag{6.2}$$

where k_B is the Boltzman constant and E_g is the energy gap of silicon, which is calculated at different temperatures with the equation [165]:

$$E_g(T) = E_g(0\,K) - \frac{\alpha T^2}{T + \beta} \tag{6.3}$$

where $E_{\mathrm{g}}(0\,\mathrm{K}) = 1.66\,\mathrm{eV}$, $\alpha = 4.73 \times 10^{-4}\,\mathrm{eV/K}$ and $\beta = 636\,\mathrm{K}$ are the experimental parameters for silicon [166, 167]. To determine the thermal equilibrium and the runaway point, the sensor temperature T as a function of the sensor power is calculated iteratively according to [36]:

$$T = T_{\mathrm{c}} + \frac{\Gamma}{A_{\mathrm{S}}} \cdot (P_{\mathrm{S}} + P_{\mathrm{FE}}) \tag{6.4}$$

where A_{S} is the sensor area and Γ is the total thermal figure of merit. This is obtained as the sum of two contributions: one related to the stave conductivity Γ_{s} and a convective term Γ_{p}:

$$\Gamma = \Gamma_{\mathrm{p}} + \Gamma_{\mathrm{s}}. \tag{6.5}$$

Variations in the total thermal figure of merit are mostly due to Γ_{s}, while Γ_{p}, which describes the heat transfer of the coolant to the pipes, has a smaller and more predictable contribution. Two possible values of Γ_{s} were used in the calculation: a conservative value of $15\,\mathrm{K\,cm^2/W}$ according to the average IBL performance and a more challenging value of $10\,\mathrm{K\,cm^2/W}$ which relies on possible improvements of the stave characteristics to be achieved in the next few years. In the iterative calculation of the sensor temperature a maximum power dissipation of the chip of $1.5\,\mathrm{W}$ and the dimensions of an FE-I4 compatible sensor are assumed. A complete list of all parameter values used for this calculation is given in Table 6.4.

Table 6.4: Parameters used in the calculation of the sensor temperature according to the IBL design values and present performance [36]. Two possible values of Γ_{s} and T_{c} are considered.

Parameter	Unit	Value
T_{c}	[°C]	-35 (-30)
Γ	[K cm^2/W]	19.42 (14.42)
Γ_{s}	[K cm^2/W]	15 (10)
Γ_{p}	[K cm^2/W]	4.42
P_{FE}	[W]	1.5
A_{S}	[cm^2]	2.01×1.68

The sensor operational temperature as a function of the sensor power per area at $-50\,°\mathrm{C}$ is shown in Figure 6.21. For the most conservative case in which a lower evaporation temperature of $T_{\mathrm{c}} = -30\,°\mathrm{C}$ and $\Gamma_{\mathrm{s}} = 15$ are considered, the resulting sensor temperature is estimated to be above $-21.5\,°\mathrm{C}$ and the runaway is calculated to start for a sensor power dissipation above at $3.9\,\mathrm{mW/cm^2}$. A more comfortable thermal runaway point at about $6.6\,\mathrm{mW/cm^2}$ is instead calculated with $T_{\mathrm{c}} = -35\,°\mathrm{C}$ and $\Gamma_{\mathrm{s}} = 15$ or $T_{\mathrm{c}} = -30\,°\mathrm{C}$ and $\Gamma_{\mathrm{s}} = 10$. The optimal case with $T_{\mathrm{c}} = -35\,°\mathrm{C}$ and $\Gamma_{\mathrm{s}} = 10$ allows for operation at stable temperatures below $-25\,°\mathrm{C}$ up to about $8.0\,\mathrm{mW/cm^2}$ with a runaway at $11.3\,\mathrm{mW/cm^2}$.

The power dissipation curves calculated for 100 to 200 µm thick FE-I4 modules irradiated at fluences from 4 to $10 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ are shown in Figure 6.22. Up to a fluence of $5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ the power per area calculated for the thinner sensors of 100 and 150 µm at the optimal operational voltage of 300 and 500 V estimated from the hit efficiency measurements in Figure 6.20, is about seven times lower than the runaway point of the worst case considered. Also for the 200 µm thick sensors up to a fluence of $10^{16}\,\mathrm{n_{eq}/cm^2}$, operations up to 800 V have

a reasonable safety margin. Nevertheless, for fluences exceeding $7 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ even higher bias voltages could be necessary to reach an optimal hit efficiency as shown in Figure 6.18. The power dissipation as a function of the bias voltage for a $200\,\mathrm{\mu m}$ thick FE-I4 sensor irradiated to a fluence of $1.3 \times 10^{16}\,\mathrm{n_{eq}/cm^2}$ is shown after different annealing times in Figure 6.22(b). At this fluence the thermal runaway starts to be critical for $200\,\mathrm{\mu m}$ thick sensors which demonstrated already poor performance at $V_\mathrm{b} = 800\,\mathrm{V}$. Even after an annealing time of 12 days, the high power dissipation still represents a challenge for the cooling system. In this scenario the possibility of reaching optimal performance with bias voltages below $800\,\mathrm{V}$ which could be obtained with thinner sensors is very appealing and will have to be investigated with further measurements already planned for the present and future thin sensor productions. In addition, the development of novel technologies such as micro-channel cooling [168] could significantly improve the performance of the cooling system significantly reducing Γ_s and thus extending the operational voltage range of planar pixel sensor even after high radiation doses.
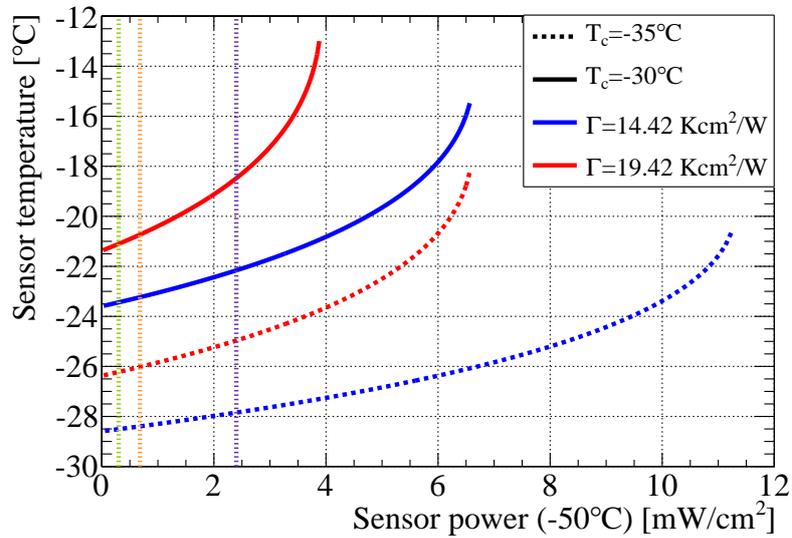
Figure 6.21: Sensor temperature as a function of the sensor power per area at $-50\,^\circ\mathrm{C}$. Two different evaporation temperatures inside the stave pipe and two different thermal figure of merit are used. The iterative calculation of the curves is stopped at the thermal runaway. The vertical lines indicate the power dissipation of 100 (green), 150 (orange) and $200\,\mathrm{\mu m}$ (violet) thick sensors irradiated to a fluence of 4–$6 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ at the operational voltages according to the saturation of the hit efficiency observed in Figure 6.20 and reported in Table 6.3.
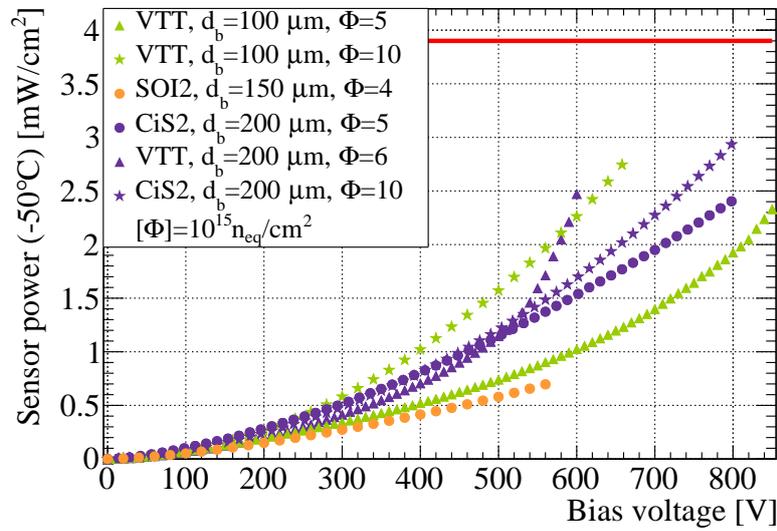
(a) 4–$10 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$
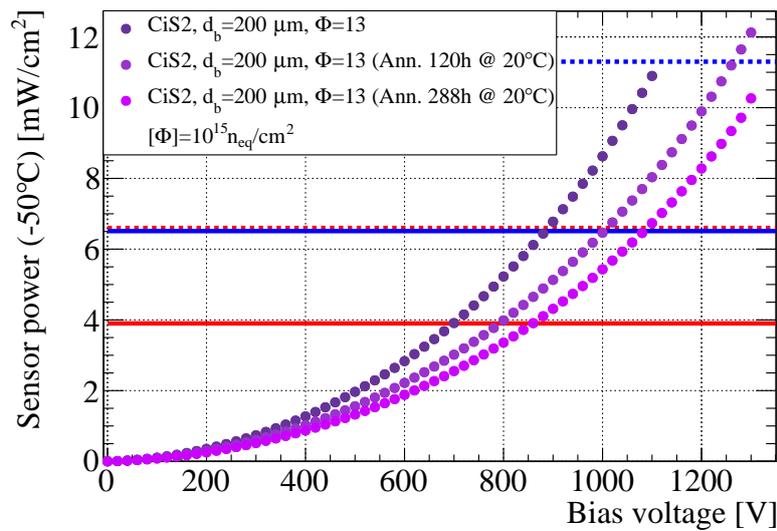
(b) $1.3 \times 10^{16}\,\mathrm{n_{eq}/cm^2}$

Figure 6.22: Power density as a function of the bias voltage for irradiated sensors of various thicknesses and productions. The curves for sensors irradiated from 4 to $10 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ are shown in (a). The curves for $200\,\mu\mathrm{m}$ thick sensors irradiated to a fluence of $1.3 \times 10^{16}\,\mathrm{n_{eq}/cm^2}$ are shown in (b). The horizontal lines indicates the thermal runaway points according to the four cases shown in Figure 6.21. All uncertainties are smaller than the marker size.

6.3.4 Performance at high pseudorapidity

The B-layer of the original ATLAS pixel detector covers a pseudorapidity range of $|\eta| < 2.5$ and with the insertion of the IBL, the coverage of the barrel for Run 2 is extended up to $|\eta| < 3$. Even if the most interesting physics in ATLAS is in the high-p_t range, an innermost pixel layer which covers a large η range provides several advantages (like forward jet vertex tagging, converted photon rejection, seeding track reconstruction) to improve the detector performance with a minimal added cost and material. In the high-η region of the pixel detector the particles are impinging on the module surface with an angle larger than $\vartheta = 80°$ with respect to the direction perpendicular to the pixel surface and cross several pixels along their long dimension. The mean cluster width $\overline{w}$ assuming an uniform particle flux can be calculated as:

$$\overline{w} = \frac{d_a \cdot \tan(\vartheta)}{p} + 1 \qquad (6.6)$$

where p is the pixel pitch crossed by the particles. Thus, as shown in Figure 6.23 in the case of an FE-I4 module, in the high-η region of the detector the cluster width depends strongly on the active thickness d_a. Thin sensors have therefore the advantage of reducing the occupancy at high η.
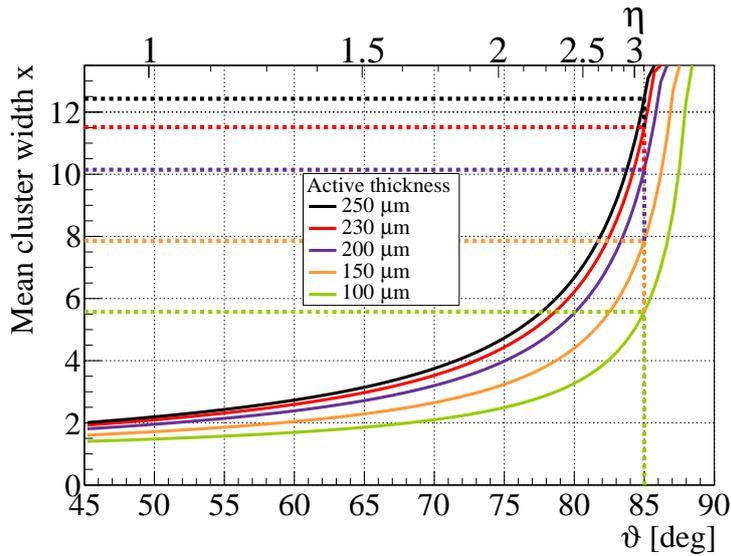
Figure 6.23: Mean cluster width along the x direction for an FE-I4 module as a function of beam incidence angle. The geometrical expectations for different sensor thicknesses are calculated according to Eq. 6.6.

The behaviour at different η was studied at beam tests by tilting an FE-I4 module around its y axis up to $\vartheta = 85°$ ($|\eta| \sim 3.1$). For these studies a module from the SOI2 production irradiated to a fluence of 4×10^{15} n_{eq}/cm^2 was used. This module employs a 150 µm thick sensor and was operated at V_b=500 V with a threshold of 1.6 ke. In Figure 6.24 the hit efficiency over the full pixel cell is compared to the one of the central region. The efficiency increases with the track incident angle up to a homogenous hit efficiency over the full pixel cell of 99.5 % at $\vartheta = 45°$ ($\eta \sim 0.88$).

(a) Hit efficiency

(b) Pixel cell efficiency
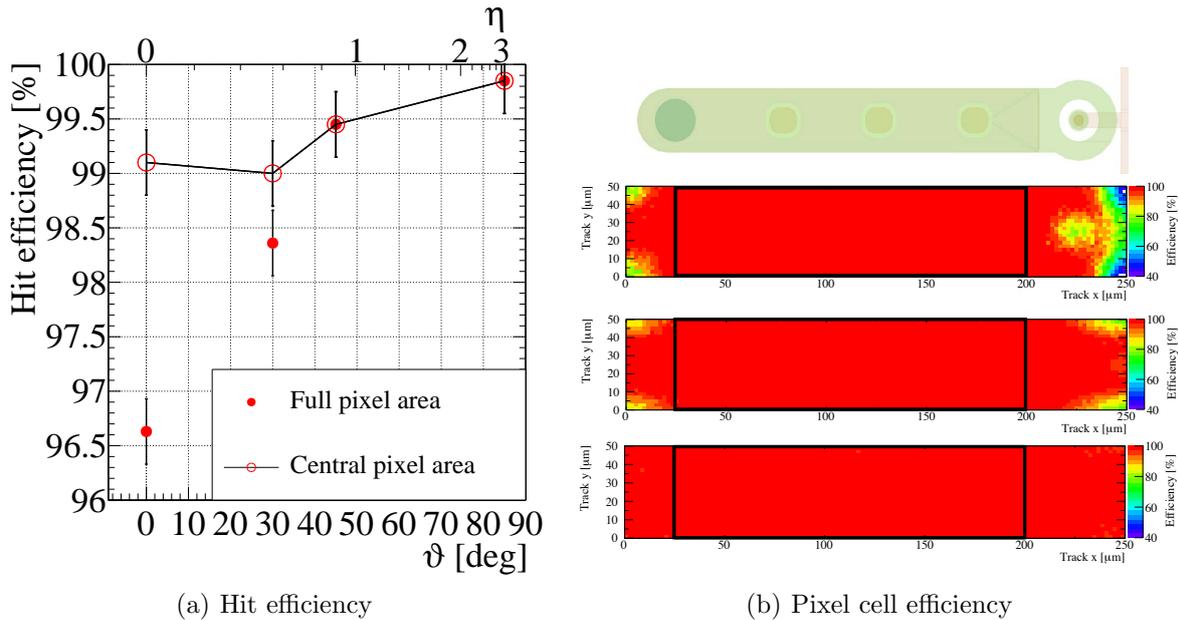
Figure 6.24: Efficiencies of FE-I4 pixel modules with a $150\,\mu$m thick sensor at different η. In (a) the hit efficiency of the full pixel (filled dots) is compared to the one obtained for the central pixel area (open dots) defined by the black rectangles in (b), where the hit efficiency over the single pixel surface is shown (from top to bottom) at $0°$ (η=0), $30°$ ($\eta \sim 0.55$) and $45°$ ($\eta \sim 0.88$) beam incident angle. The module was operated with a threshold of $1.6\,$ke. The hit efficiency maps of the pixel cells are obtained displaying the reconstructed track impact point expressed in pixel coordinates and projecting the data for all identical structures onto the same image.

At $\vartheta = 85°$ the corresponding hit efficiency is compatible with $100\,\%$ as expected, since a particle crosses almost $1.7\,$mm inside a $150\,\mu$m thick sensor. For the FE-I4 pixel shape this leads to a mean cluster width in the tilted direction of 7.9 pixels when the bulk is fully depleted as shown in Figure 6.23. As a comparison for an FE-I4 module with the thickness of the present IBL pixel sensors of $200\,\mu$m, in the same conditions a mean cluster width of 10.1 pixel cells is expected. After irradiation, at a bias voltage of $500\,$V the $150\,\mu$m thick sensor is not completely depleted. The active depth is estimated to be around 130–$140\,\mu$m for which a cluster width in x lower than at full depletion is expected. In Figure 6.25 the simulation, which takes into account also the threshold effects as discussed in Section 4.6, shows a result very close to the geometrical expectations for the not irradiated case. The measured cluster width distribution along the x direction in Figure 6.27 shows instead a lower mean of the cluster width of 6.2 pixels. This difference is mainly due to the lower charge collected after irradiation for the pixels at the edge of a long cluster, which has a higher probability of being below the threshold. This is demonstrated in Figure 6.26, where the ToT distribution is shown for the different pixels of long clusters along the x coordinate. Depending on the particle entrance point on the leftmost pixel, the two pixels at the edge of the cluster are only partially crossed and therefore exhibit a lower average signal with respect to the other pixels. Comparing the signals in the central pixels of the cluster, where particles cross always the same amount of silicon, it is possible to study the effect of the charge collection at different depths inside the active bulk. The quantitative

accuracy of the measurement is limited by the small ToT range of the FE-I4 chip and the chosen charge calibration, which was optimised for perpendicular incident tracks with a charge tuning of 10 ToT for 10 ke. Since, at high η, particles travel along the 250 μm size of the pixel cell, the expected signal is instead around 20 ke, resulting in a saturation towards high ToT values of the collected charge. Nonetheless, the results show a significant decrease of the ToT signal when the particles cross the depleted bulk at larger distances from the electrodes. This effect is mainly due to trapping centres, which prevent charge carriers to reach the high weighting field regions reducing their mean free path as described in Section 2.2.
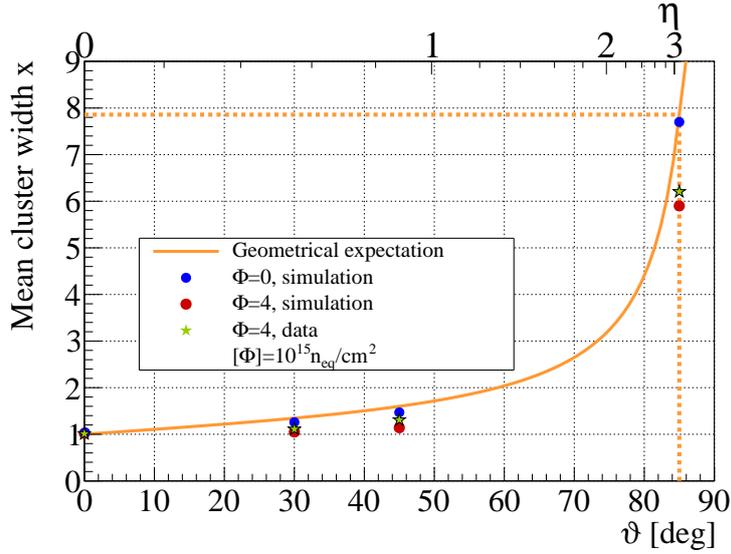
Figure 6.25: Comparison of simulated and beam test data for the cluster width in x at different beam incident angles of an FE-I4 module with a 150 μm thick sensor before irradiation at full depletion, and after irradiation at V_{b}=500 V.

The distribution of the cluster width in x and the correspondent residual distributions are shown in Figure 6.27. The core of the residual distributions is well described by a gaussian for which the resulting σ is a good estimation of the tracking resolution of the detector. When all cluster widths are considered, a resolution of $\sigma=(103 \pm 7)$ μm is measured, while the best resolution of $\sigma=(97 \pm 7)$ μm is obtained for a cluster width of seven in the x direction. The quoted uncertainties take into account the pointing resolution of the telescope and the alignment precision of the detector. The measured resolution is in all cases larger than for the perpendicular case, where, given the uniform pion flux over 250 μm long pixel cells, a resolution in x of 72 μm is expected in the worst case of single hit clusters, while a resolution of $\sigma=(70.4 \pm 2.0)$ μm was measured for these modules in Ref. [79].

One possible option for a readout chip under investigation for Phase II is a reduced pixel pitch of (50×50) μm². To study the performance of such a geometry in the high-η regions of the ATLAS detector, an FE-I4 module with a 100 μm thick sensor was measured at SpS tilted by $\phi = 80°$ ($\eta \sim 2.4$) around their x axis with respect to the perpendicular beam incidence. The geometrical expectation for the cluster width in this configuration as a function of the particle incident angle on the detector surface is shown in Figure 6.28. Given the large cluster width

(a) 6 hit clusters

(b) 7 hit clusters

(c) Sketch of the particle impact
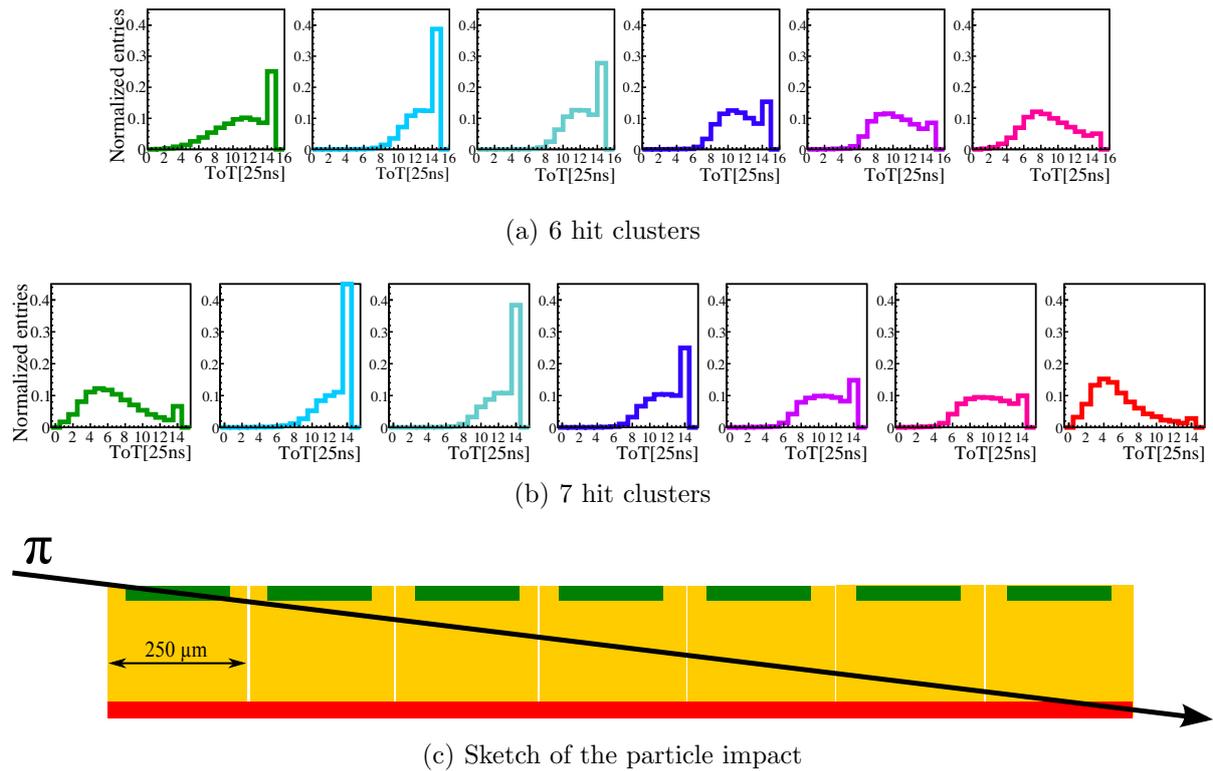
Figure 6.26: Measured ToT for cluster widths six (b) and seven (a) pixel long clusters. From left to right the particle is passing the module with increasing distance to the pixels on the module surface as shown in (c). The 14th bin contains the entries for charges which exceed the ToT range.

(a) Cluster width x distribution

(b) Residual distribution along x
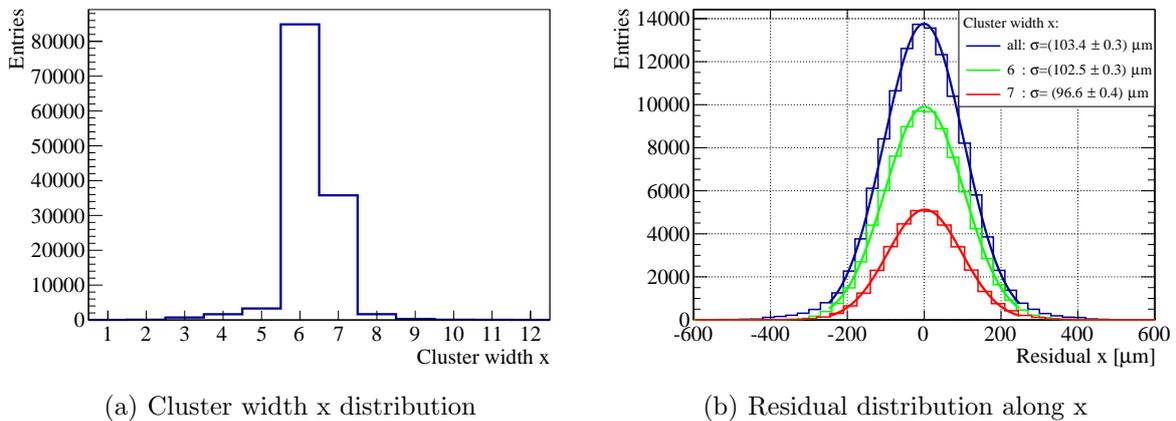
Figure 6.27: Distribution of the cluster width in x (a) and the residual distribution (b) of a SOI2 module irradiated to a fluence of 4×10^{15} n_{eq}/cm^2 and biased at V_b=500 V. The detector is tilted by $\phi = 85°$ around its y axis with respect to the beam incidence. The residual distribution for all cluster sizes (blue), for cluster width in x of 6 (green) and 7 (red) are shown. The core of the residual distribution, corresponding to a fraction of more than 97 % of the events, is fitted to a Gaussian function.

expected already at small angles due to the small pitch along the beam direction, resulting in a reduced path length and released charge of particles in the silicon bulk, the efficiency of single pixel cells is crucial for the tracking performance.
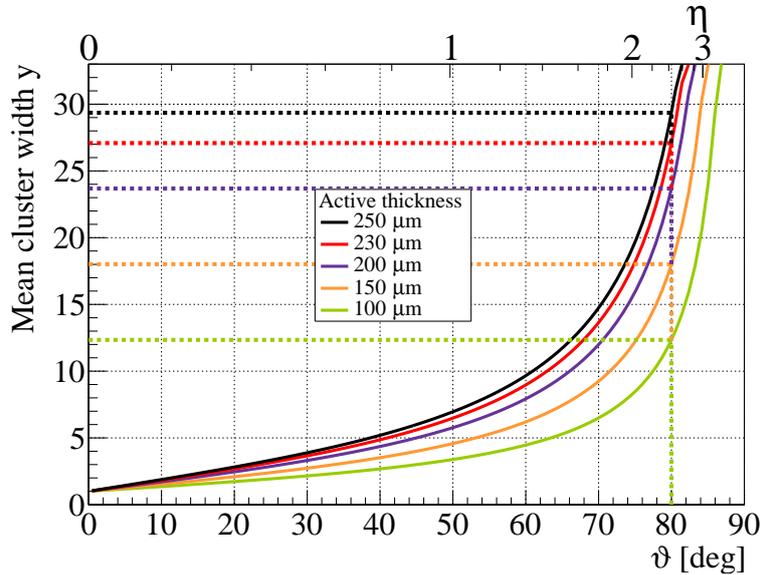
Figure 6.28: Mean cluster width along the y direction for an FE-I4 module as a function of beam incidence angle. The geometrical expectations for different sensor thicknesses are calculated according to Eq. 6.6..

Figure 6.29 shows the distribution of the cluster width in y for a not irradiated FE-I4 module employing an 100 µm thick sensor operated with a threshold of 1 ke. Different cluster separations in y are used in the cluster reconstruction to take into account possible cluster splits due to pixel inefficiencies. The cluster separation is defined as the maximum allowed distance between two hits, in number of pixels, to still be associated to the same cluster. Hence, with a cluster separation of 1, only clusters with adjacent hits are reconstructed, while, with a higher cluster separation, split clusters are also joined together. Only negligible differences in the cluster width distributions are observed for different cluster separations. The peak of the distributions is at 10 pixels, while, given Figure 6.28, an average cluster width in y of 12.3 pixels is expected for this thickness.

The difference with respect to the geometrical expectation can be explained as a combination of two effects: the inefficiency of the pixels at the edge of the clusters, which are mostly only partially traversed by the particles, and small misalignments in the setup, which have a large impact on the cluster width at large angles as shown in Figure 6.28. The former effect can be observed in Figure 6.30 where the MPV of the ToT distribution is shown for the different pixels inside clusters with different width in y. Given the tuning of the module with a target ToT of 6 for a charge of 4 ke, the central pixels of the clusters, which are fully crossed by pions, show a collected charge of almost 4.5 ToT (about 3 ke) compatible with the expectation for a high energetic particle crossing 50 µm of silicon presented in Figure 2.2(b). No dependence on the interaction depth in the active bulk is observed. The pixels at the edge of the clusters have instead a lower average ToT with respect to the central pixels, with the lowest values observed for clusters with a width of 11 pixels. Therefore, this cluster width is assumed to
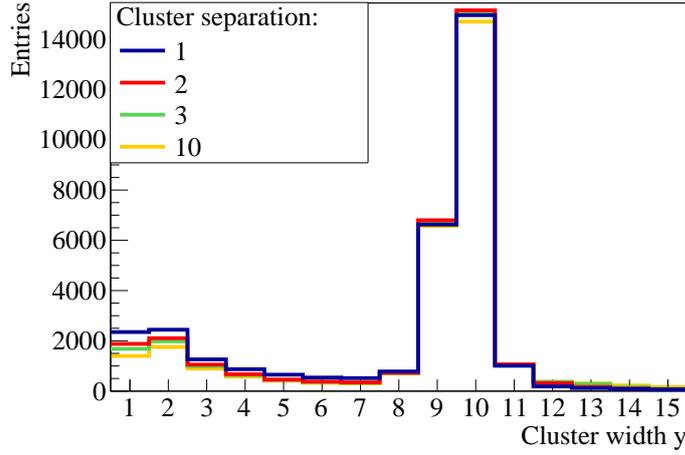
Figure 6.29: Distribution of the cluster width in y for a not irradiated FE-I4 module employing a $100\,\mu$m thick sensor and tilted by $\phi = 80°$ around its x axis with respect to the perpendicular beam incidence. The detector was operated fully depleted with a threshold of 1 ke. The results obtained using different cluster separations for the clustering algorithm are shown in different colours. Due to the cluster splitting, histograms with different cluster separation have different number of entries.

correspond to particles which cross the full active bulk thickness with a signal over threshold for all traversed pixels. The average ToT for the edge pixels increases for clusters with a width of 10 pixels, where the signal of only one of the two edge pixels is below threshold, and an almost flat distribution is observed for clusters with a width of 9 pixels. This means that the particles are crossing the same amount of silicon in each pixel and both cells at the edge of the cluster are lost because of the threshold.

Since for these measurements no tracking information from the telescope was available, a precise determination of the impact angle of the tracks is not possible and the following analysis was performed considering only clusters with a width in y between 9 and 11 pixels and of 1 pixel in x. Due to the low noise occupancy of the detector before irradiation these clusters have a high probability of being produced by beam particles, while noisy pixels are more likely to have a cluster size of 1. Moreover, a cluster width in y less than 9 has a high probability to be associated with particles which cross the detector close to the border of the sensor and is therefore not considered. The efficiency of single pixels (ϵ_{pix}) for different cluster separations is shown in Figure 6.31 as a function of the cluster separation. The single pixel efficiency is defined by:

$$\epsilon_{\mathrm{pix}} = 1 - \sum_{c=1}^{N} \frac{h_{\mathrm{miss}}^c}{w_{\mathrm{x}}^c - 2} \tag{6.7}$$

where the inefficiency is calculated dividing the number of missing hits h_{miss} inside a cluster c by the width w_{x} of the cluster in x subtracting the first and the last pixels, which by definition are always efficient. The efficiency ϵ_{pix} saturates between 99.6 and 99.7 % for a cluster separation of at least 3 pixels. This value defines a lower bound of ϵ_{pix}, since with a larger cluster separation the probability of clustering noisy pixels or hits produced by different particles increases.
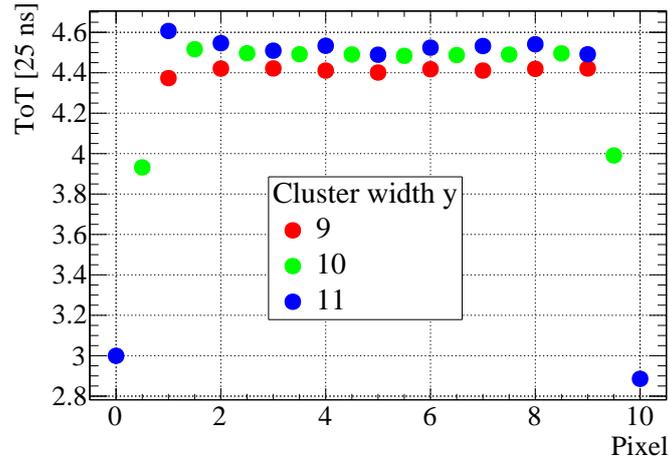
Figure 6.30: MPV of the ToT distribution as a function of the traversed pixel in the cluster for an FE-I4 module employing a 100 μm thick sensor and tilted by 80° around its x axis with respect to the perpendicular beam incidence. The particles cross the sensor from pixel number 0 to pixel number 10 entering from the backside. For better visibility and understanding, the points corresponding to a cluster width in y of 10 (green) are shifted by 0.5 pixels. The uncertainties of the points are smaller than the marker size.
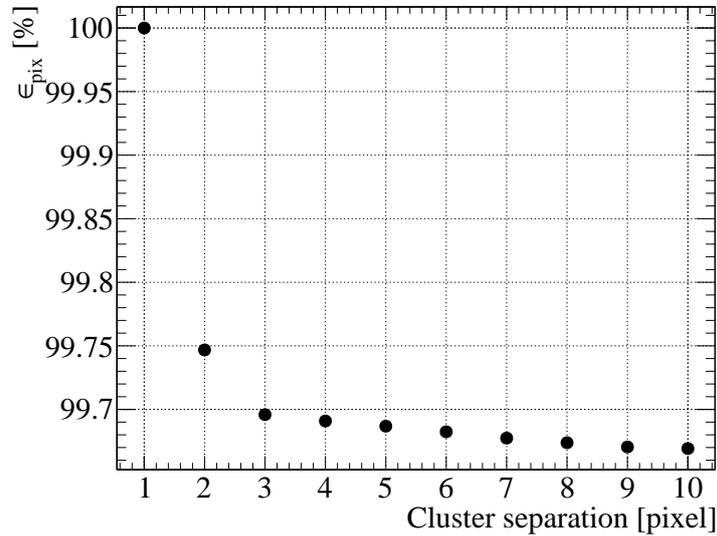
Figure 6.31: Hit efficiency of single pixels as a function of the cluster separation for an FE-I4 module employing a 100 μm thick sensor and tilted by 80° around its x axis with respect to the perpendicular beam incidence. The statistical uncertainties are smaller than the marker size.

6.4 Active and slim edge sensors

For slim and active edge sensors of the VTT production, the characterisation in the proximity of the implanted edges is particularly interesting. Therefore, a dedicated analysis of the performance of the edge pixels in terms of charge collection and hit efficiency was carried out with both radioactive sources and high energetic particles at beam tests. A comparison for sensors with different edge designs before and after irradiation is here presented for $100\,\mu m$ thick sensors. A list of the measured modules and their irradiations is given in Table 6.5.

Table 6.5: Overview of the characterised $100\,\mu m$ thick active and slim edge modules of the VTT production.

Edge distance [µm]	Guard rings	Bias ring	Readout chip	Irradiation site	Fluence $[10^{15}\,\mathrm{n_{eq}/cm^2}]$
125	0	yes	FE-I4	-	0
			FE-I3	KIT+KIT	1+4
50	1	no	FE-I3	JSI	2

6.4.1 Charge collection at the edge

In this section the charge collection properties of central pixels and edge pixels of the VTT modules are compared. The collected charge is shown as a function of the bias voltage for the edge designs with $d_\mathrm{e}{=}50\,\mu m$ in Figure 6.32 and $d_\mathrm{e}{=}125\,\mu m$ in Figure 6.33. Before irradiation, all $100\,\mu m$ thick sensors show the expected collected charge of almost 7 ke with a compatible distribution for the central and the edge pixels, as discussed in Ref. [79]. Also after irradiation the charge collected by the edge pixels is very close to the one measured for the central pixels, with a comparable shape of the charge distribution for both edge designs. In Figure 6.32(b) and 6.33(b) a significant difference in the charge distribution shape can only be noticed at low energies where the edge pixel distribution shows a higher tail. This difference is associated with inclined particles which only cross partially the active area at the border of the sensor and it is therefore not related to a different charge collection capability of the edge pixels.

6.4.2 Edge efficiency

To measure the effective active area for the different designs of active edge sensors, the modules were characterised at beam tests with particles crossing perpendicularly to their pixel implants. Due to the limited beam size and the high statistics required in this analysis, for each measurement the beam was centred on only one of the two edge pixel columns. The hit efficiency for the FE-I3 module with the $50\,\mu m$ active edge design was measured before irradiation both at DESY and at SpS with consistent results, as shown in Figure 6.34. In both cases the module was operated with a threshold of 1.5 ke. Despite the low statistics of events collected at the border of the sensor at SpS, this edge design was demonstrated to be sensitive up to the activated edge showing an average hit efficiency of $(91^{+8}_{-18})\%$ in the last $50\,\mu m$ after the end of the last pixel implant. The measurement was repeated at DESY optimising the experimental setup by reducing the distance of the two telescope arms, thereby minimising the

(a) Charge collection

(b) Charge distribution at 160 V
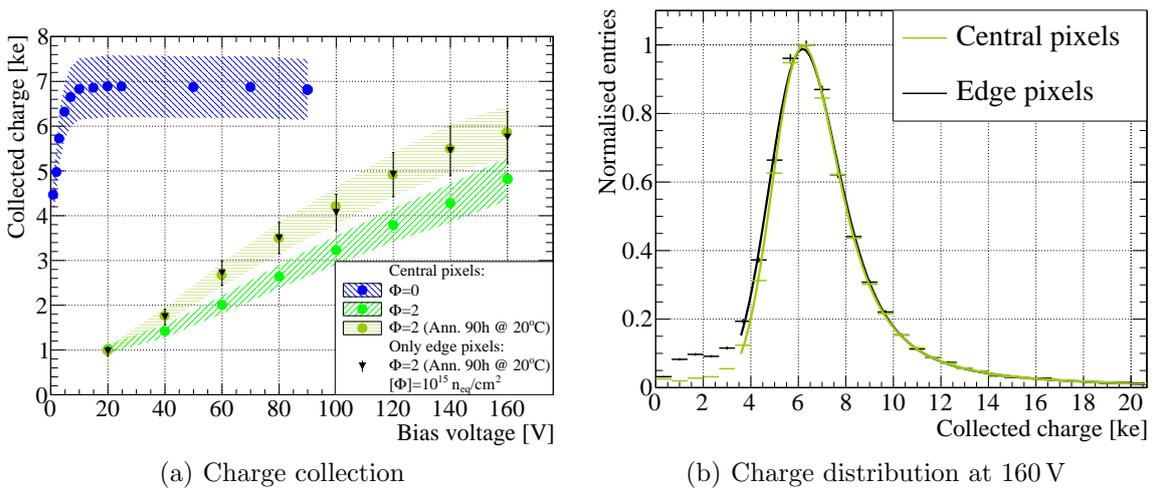
Figure 6.32: Charge collection of the FE-I3 module from the VTT production employing a 100 µm thick sensor with the 50 µm active edge design. In (a) the collected charge as a function of the bias voltage is shown before and after irradiation to a fluence of 2×10^{15} n_{eq}/cm^2. After irradiation, the charge collection is measured before and after an annealing of 90 hours at room temperature, for the central pixels and for the edge pixels of the sensor. In (b) the shape of the charge distribution for central and edge pixels is compared after annealing and for a bias voltage of 160 V. The module was operated with a threshold of 1.8 ke before irradiation and 1.5 ke after irradiation.

impact of multiple scattering on the telescope pointing resolution as discussed in Section 4.5. With the optimised setup a resolution close to the one at SpS was achieved and, thanks to the higher statistics collected, a more precise measurement at the sensor border was achieved, showing an average hit efficiency of $(87.4 \pm 0.7)\%$ in the region from the last pixel implant up to the activated edge. As shown in Figure 6.34(c), the sensor is fully efficient up to 20 µm from its nominal edge.

For comparison Figure 6.35 shows the hit efficiency at the edge of the FE-I3 module with $d_e=125$ µm measured before irradiation at SpS. In this edge design the bias ring is at ground potential but not read out, preventing the signal generated in the edge region to reach the active region. A residual hit efficiency of $(69 \pm 3)\%$ is still observed between the end of the last pixel implant and the bias ring. In this case the inactive area is effectively 110 µm wide. Due to the very thin active bulk, a small hit efficiency drop is also observed near the biasing structures, around -600 µm, in Figure 6.35(a).

A similar behaviour is observed in Figure 6.36 for the FE-I4 module with the same 125 µm edge design. The hit efficiency of this module was measured at DESY with a threshold of 1.6 ke. Since for these measurements the setup of the telescope was not optimised to reduce the multiple scattering, a larger smearing of the hit efficiency drop near the bias ring structure is observed. An average hit efficiency of $(45 \pm 1)\%$ is estimated for the region between the last pixel implant and the bias ring. Also in this case a small hit efficiency drop is observed in Figure 6.36(a) near the biasing structures.

(a) $\Phi=1 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$

(b) $\Phi=1 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$, $V_\mathrm{b}=300\,\mathrm{V}$

(c) $\Phi=5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$

(d) $\Phi=5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$, $V_\mathrm{b}=300\,\mathrm{V}$
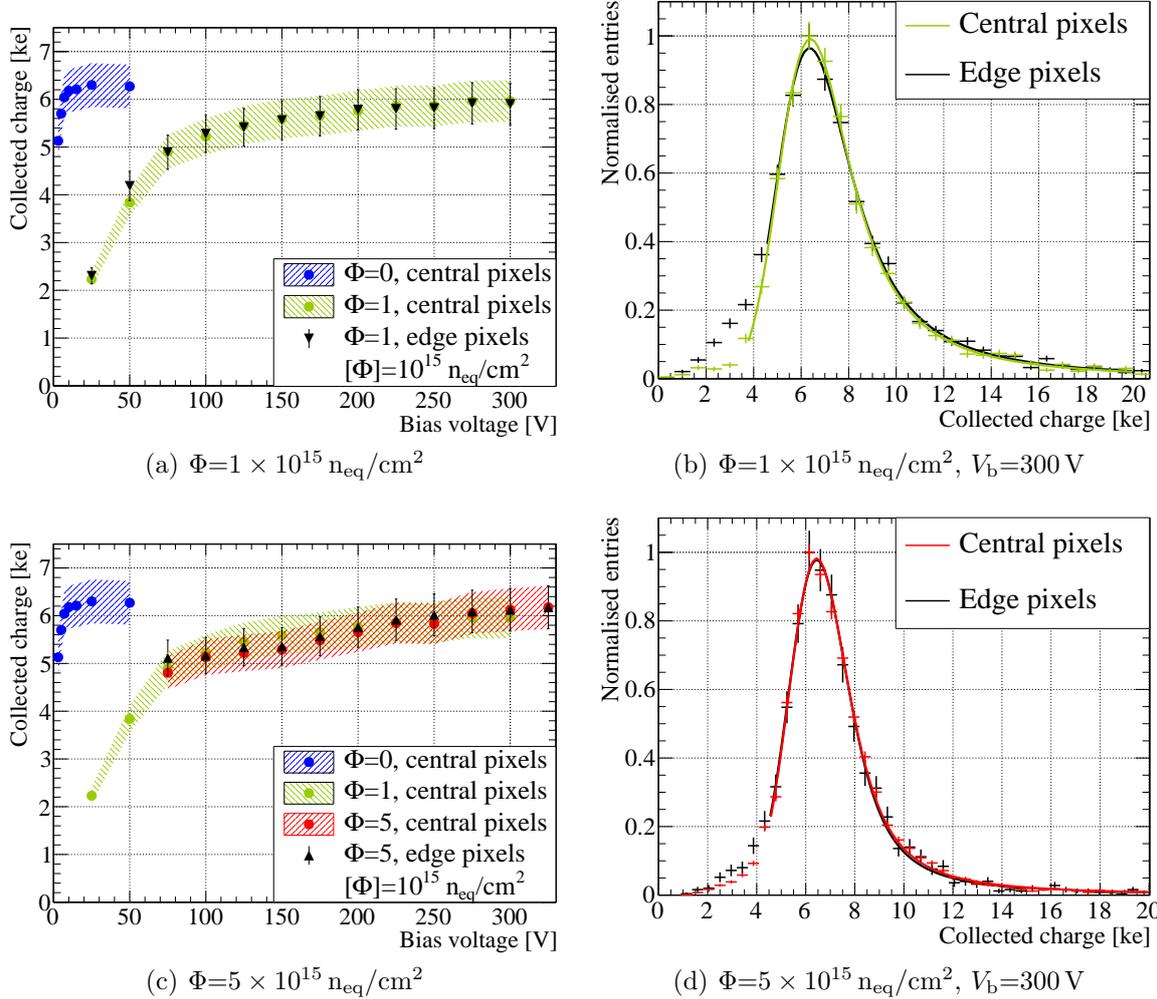
Figure 6.33: Charge collection of the FE-I3 module from the VTT production employing a 100 μm thick sensor with the 125 μm slim edge design. In (a) and (c) the collected charge as a function of the bias voltage is shown before and after irradiation to a fluence of 1 and $5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$, respectively. After irradiation the charge collection of the central pixels is compared to the one of the edge pixels only. The shape of the charge distribution of the central and the edge pixels is compared at a bias voltage of 300 V for an irradiation fluence of 1 (b) and $5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ (d). The module was operated with a threshold of 1.5 ke.

(a) SpS

(b) DESY

(c) DESY, edge detail
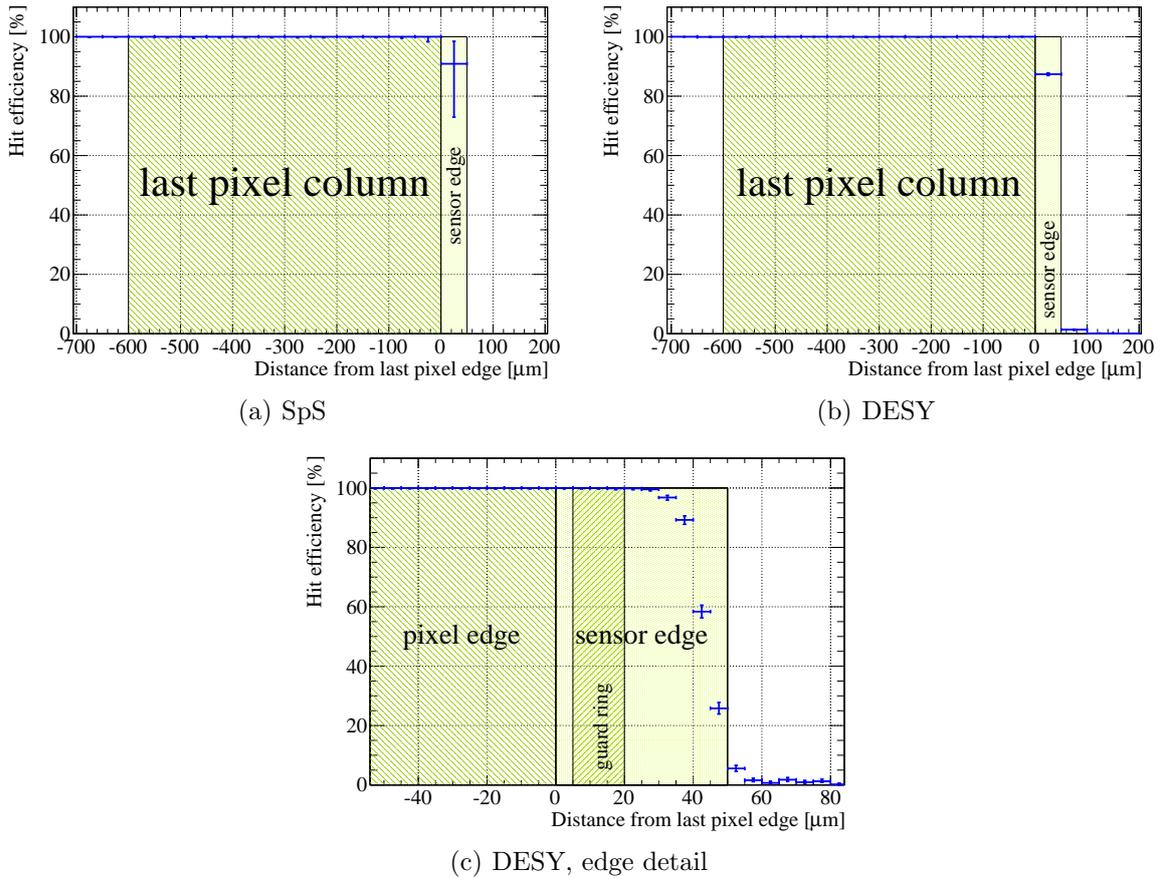
Figure 6.34: Hit efficiency at the edge of the $100\,\mu m$ thick FE-I3 module with the $50\,\mu m$ edge design. The module was measured before irradiation at SpS (a) and at DESY (b, c), in both cases it was operated with a threshold of $1.5\,ke$. Figure (a) and (b) show the hit efficiency in the last pixel column and up to the sensor edge, while (c) is a zoom into the sensor edge of (b) showing the hit efficiency within the different structures.

After irradiation to a fluence of $5 \times 10^{15}\,n_{eq}/cm^2$ the hit efficiency of an FE-I3 module with $d_e{=}125\,\mu m$ was measured at DESY for different bias voltages. The results compared in Figure 6.37 show that the hit efficiency extends up to the bias ring structure even for the lowest $V_b{=}100\,V$. At the highest measured voltage of $V_b{=}300\,V$ the behavior at the edge of the sensor is similar to the one observed before irradiation with an average hit efficiency of $(69 \pm 2)\,\%$ measured in the gap between the last pixel implant and the bias ring. A smearing of the efficiency drop near the bias ring structure with the respect to the measurements before irradiation can still be observed due to a worst pointing resolution at DESY compared to the one obtained at SpS. The effect of the radiation damage is visible close to the bias dot and bias rail regions where the hit efficiency has a significant drop.

(a) Full pixel column

(b) Edge detail
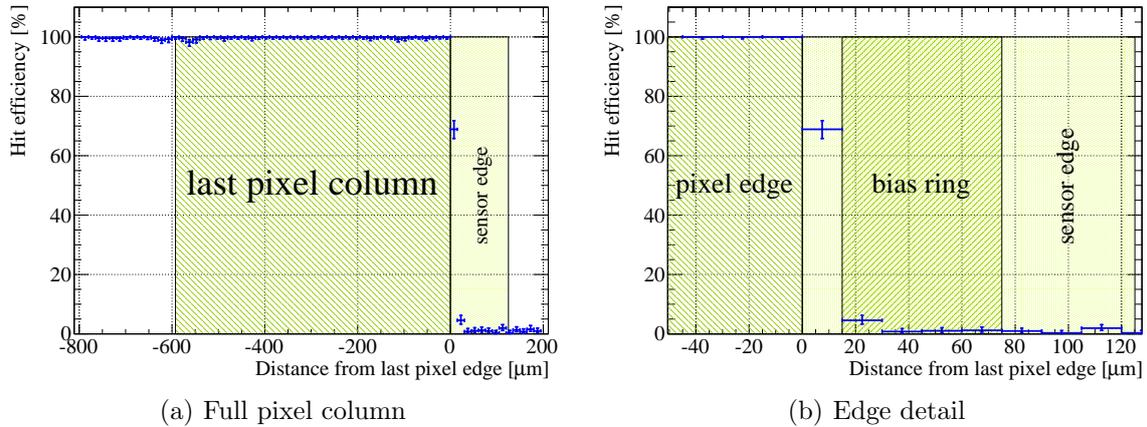
Figure 6.35: Hit efficiency at the edge of the $100\,\mu m$ thick FE-I3 module with the $125\,\mu m$ edge design before irradiation. The module was measured at SpS and operated with a threshold of $1.5\,ke$. Figure (a) shows the hit efficiency in the last pixel column and up to the sensor edge, while (b) is a zoom into the sensor edge showing the hit efficiency within the different structures.

(a) Full pixel column

(b) Edge detail
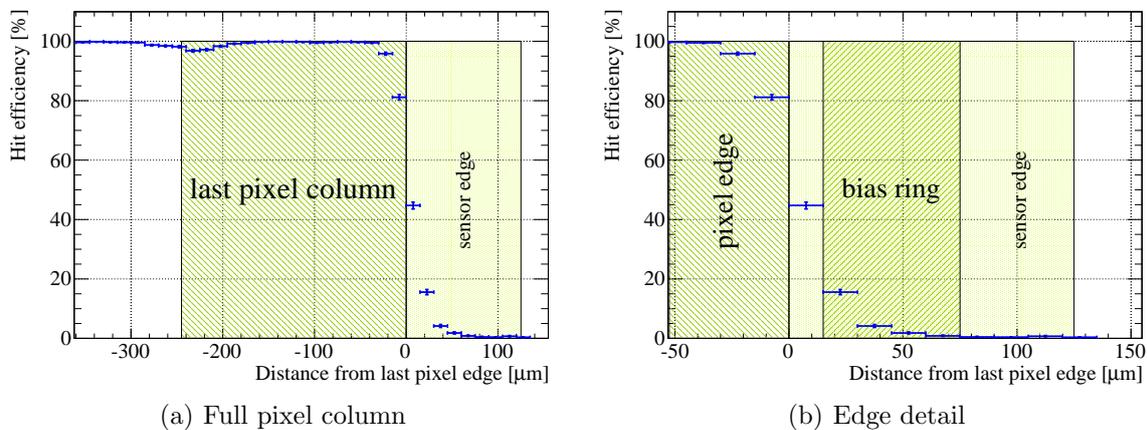
Figure 6.36: Hit efficiency for different bias voltages at the edge of the $100\,\mu m$ thick FE-I4 module with the $125\,\mu m$ edge design before irradiation. The module was measured at DESY and operated with a threshold of $1.6\,ke$. Figure (a) shows the hit efficiency in the first pixel column and up to the sensor edge, while (b) is a zoom into the sensor edge showing the hit efficiency within the different structures.

(a) Full pixel column

(b) Edge detail
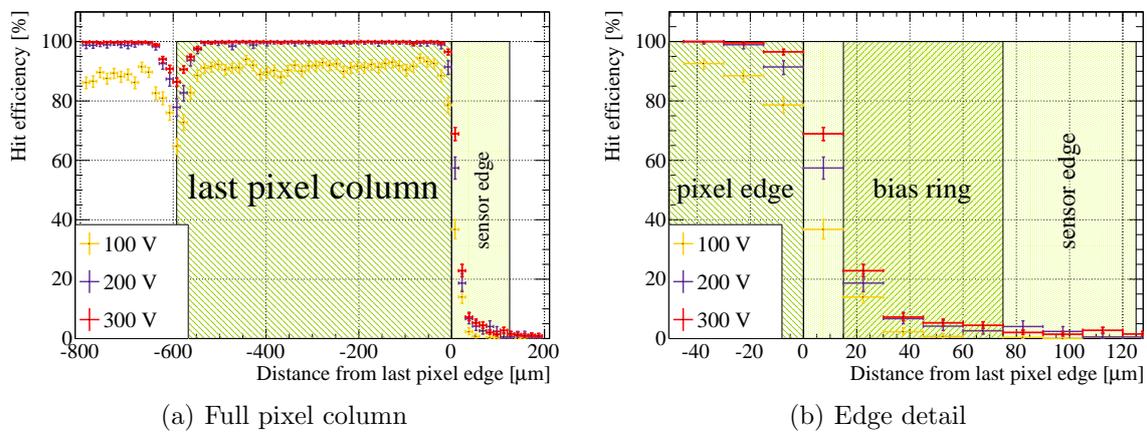
Figure 6.37: Hit efficiency at the edge of the $100\,\mu m$ thick FE-I3 module with the $125\,\mu m$ edge design after irradiation to a fluence of $5 \times 10^{15}\,n_{eq}/cm^2$. The module was measured at DESY at different bias voltages and operated with a threshold of $1.5\,ke$. Figure (a) shows the hit efficiency in the last pixel column and up to the sensor edge, while (b) is a zoom into the sensor edge showing the hit efficiency near the different structures.

6.5 Quad modules

To cover a surface of several square meters in the outer barrel layers of the future pixel detector, larger sensors are necessary to avoid the overlap of many small modules. Due to the fixed chip size such a sensor needs to be read out with more chips at the same time and is required to have a full active surface also in the gaps between the chips. In this section the characteristics of newly designed quad module prototypes are investigated and compared to the ones of single chip modules before and after irradiation.

6.5.1 Prototype designs

The quad modules from the CiS2 production employ $200\,\mu m$ thick sensors interconnected to four FE-I4B chips that were thinned to $150\,\mu m$ at IZM. A glass substrate was attached to the chip backside to avoid the bending of the corners after thinning, which would otherwise likely lead to a decrease of the bump-bonding efficiency. These first prototypes of quad sensors are made of two double chip sensors diced as a single piece of silicon, and therefore they have an inactive gap of $1.6\,mm$ between the rows of the two double sensors, where guard ring and bias ring structures are located. Moreover, the two pixel columns in the middle of each double sensor are $450\,\mu m$ long to allow the necessary space for the placement of the two neighboring chips. The quad modules of this production were interconnected to PCBs designed by the University of Liverpool, and described in Section 4.1. This quad module production is part of a collaboration between the MPP and the Universities of Göttingen and Bonn.

Another prototype of quad modules was assembled with quad sensors from the CiS3 production, which are designed to have a full active area between the four chips. As in the CiS2 design, the two pixel columns in the central region of the quad sensors are $450\,\mu m$ long, instead of the standard FE-I4 pitch of $250\,\mu m$. In addition, eight ganged pixel rows (four for each chip) cover the area between the four chips, allowing to create the clearance needed for the placement of two neighbouring chips, while maintaining a fully active area in the centre of the detector. The $270\,\mu m$ thick sensors were bump bonded to four FE-I4B chips at IZM. For the interconnection of these quad sensors a dedicated chip wafer was used in which the top test pads of the chips were diced away. This is necessary to reduce the huge space between the last rows of two neighbouring chips, which was inactive in the quad module design of the CiS2 production, and allow for a more compact design of the sensor. The chips were thinned to $100\,\mu m$ and the resulting quad modules were wire bonded to flex readouts in Bonn. The results presented in the following are obtained from three quad modules of the CiS2 production. One of these quad modules was irradiated at KIT to a fluence of $3 \times 10^{15}\,n_{eq}/cm^2$, after irradiation only 3 out of 4 chips were still operative. A list of the measured quad modules and single chip modules used for comparison is given in Table 6.6.

6.5.2 IV carachteristics

Figure 6.38 shows the IV characteristic of the quad modules from the CIS2 production, measured before and after irradiation to a fluence of $3 \times 10^{15}\,n_{eq}/cm^2$, compared to the one of a single chip module from the same production and with the same guard ring design. The quad modules show a slightly higher leakage current per area with respect to single chip modules of the same thickness which is compatible with the variation observed in the sensor production before irradiation and with the different fluences after irradiation. The leakage current is instead significantly higher for the quad modules when the chips are all configured, reflecting the

Table 6.6: Overview of the measured quad modules (Quad) and single chip modules (SCM) used for comparison from the CiS2 production.

Production	Module type	Module interface	Irradiation site	Fluence [10^{15} n_{eq}/cm^2]
CiS2	Quad	Quad PCB	-	0
			-	0
			KIT	3
	SCM	FE-I4 single chip card	-	0
			KIT	2

temperature of the sensor due to the heating of the four chips estimated to be about 3 °C higher than for single chip modules. The breakdown voltage is compatible with the one of the single chip modules both before and after irradiation.

(a) Before irradiation

(b) After irradiation
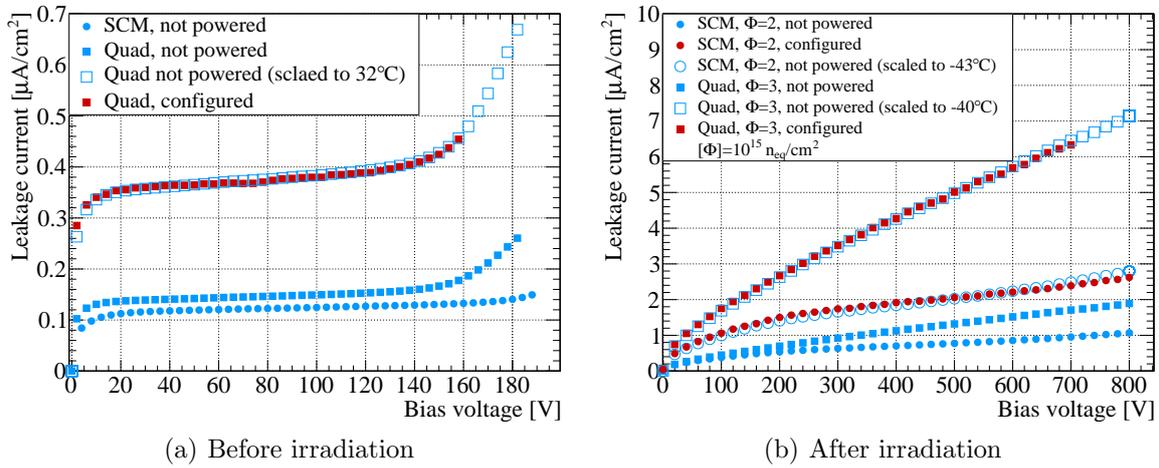
Figure 6.38: IV curves of the quad module from the CiS2 production. The leakage current of the sensor of the quad module is compared to the one of a single chip module from the same production and with the same guard ring design, both in the case of "chip not powered" and "chip configured". The measurements were performed for a not irradiated module (a) and for a quad module irradiated to a fluence of 3×10^{15} n_{eq}/cm^2, and a single chip module irradiated to a fluence of 2×10^{15} n_{eq}/cm^2 (b). Both irradiations were performed at KIT. The temperature of the sensors when the chips are configured is estimated scaling the IV curves when the chips are not powered according to Eq. 6.2. The statistical uncertainties are smaller than the marker size.

6.5.3 Tunability

Typical tuning results of the quad modules obtained with the USBPix system are shown in Figure 6.39. Before irradiation a good uniformity of the ToT and the threshold for all chips

is obtained. After irradiation the average standard deviation of the two distributions is much larger than before irradiation.

(a) Threshold

(b) ToT
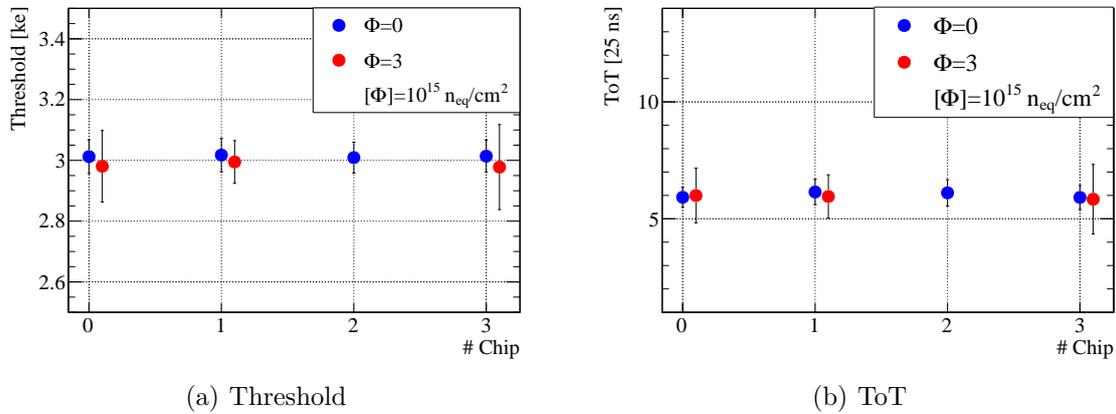
Figure 6.39: Comparison of the threshold (a) and ToT distribution (b) for the different chips of a quad module from the CiS2 production before and after irradiation to $3 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$. The uncertainties are statistical and correspond to the standard deviation of the distributions. After irradiation the chip 2 was not working.

6.5.4 Noise

Figure 6.40 shows the noise as a function of the bias voltage of the four chips for the same tuning. Before irradiation and above the full depletion voltage, the noise is stable with values between 100 and 120 e, and it is comparable to the typical noise level of a single chip module from the same production. After irradiation, the measured noise level ranges from 350 e to 600 e, which is higher than for single chip modules irradiated to similar fluences. The high noise level in the quad modules seems to be connected to the PCB. A systematic relation between the noise and the position of the chip on the card was observed for all three measured quad modules.

6.5.5 Charge collection

The collected charge as a function of the bias voltage was measured using the USBPix system and a burn-in adapter card as described in Section 4.1. The module was tuned to a threshold of 3 ke. Results in Figure 6.41 show a collected charge before irradiation of almost 14–15 ke consistent with the expected value for a 200 μm thick silicon sensor when operated above the full depletion voltage. After full depletion, the maximum spread of the collected charge of the different chips is of the order of 1 ke. After irradiation to a fluence of $3 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ the collected charge is consistent with the measurements of single chip modules with the same sensor thickness presented in Section 6.3. The largest spread between the results of the different chips is of the order of 2 ke. Both before and after irradiation the chip 0 is the one that shows the highest collected charge and the largest difference to the expectations.

(a) Before irradiation

(b) Before irradiation, V_b=100 V

(c) After irradiation

(d) After irradiation, V_b=600 V
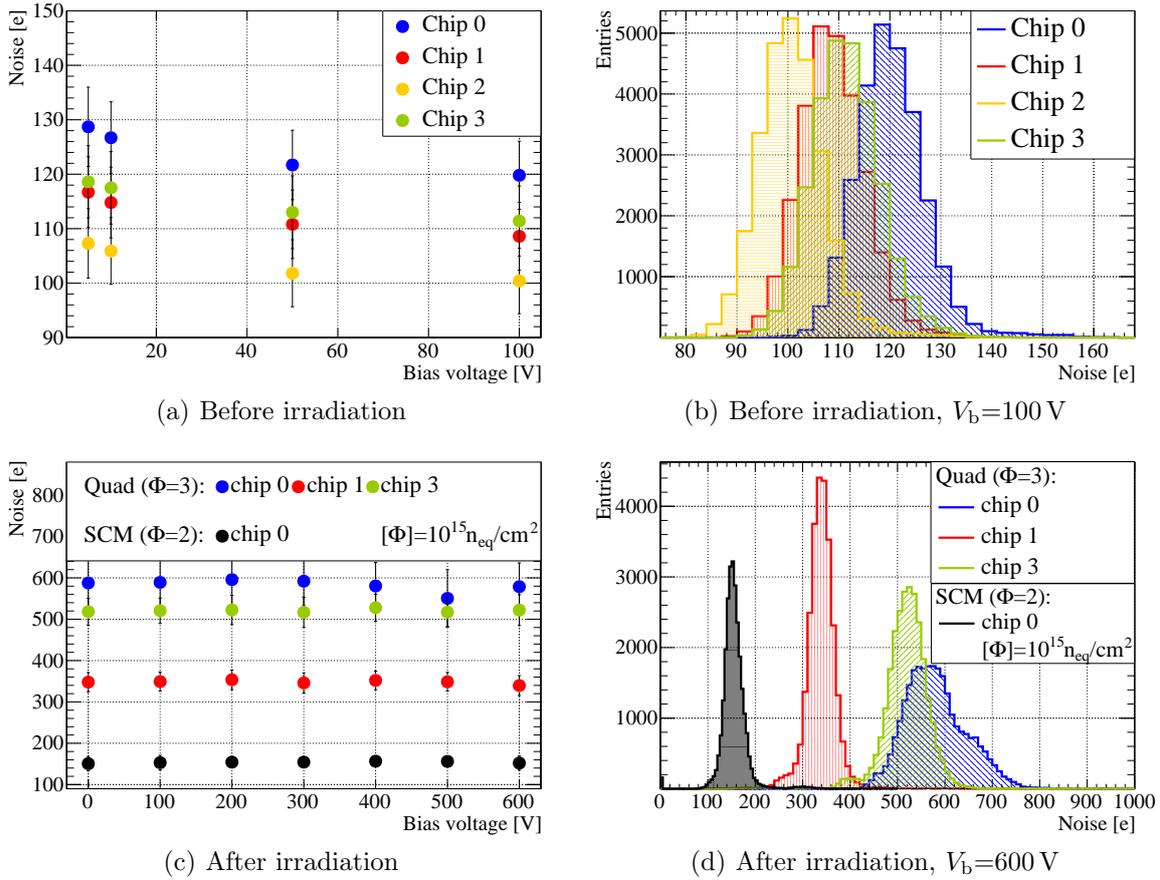
Figure 6.40: Noise of the four chips of a quad module. The noise as a function of the bias voltage is shown before irradiation (a) and after irradiation to a fluence of 3×10^{15} n_{eq}/cm^2 (c). The distributions of the noise before irradiation at V_b=100 V and after irradiation at V_b=600 V are shown in (b) and (d), respectively. The statistical uncertainties associated to the measurements are the standard deviations of the noise distributions.

6.5.6 Hit efficiency

The hit efficiency for perpendicular incident particles obtained at DESY is shown in Figure 6.42. The threshold was tuned to 3 ke and the chips were simultaneously read out with the RCE readout system. The beam spot was centred in the module to study the efficiency in the critical area where all four chips are involved in the data taking. The full module shows an overall efficiency of 99.0 %. A lower hit efficiency of the pixel rows at the edge between the two double chip sensors is observed due to the multiple scattering that degrades the telescope pointing resolution, and thus leads to the inclusion of tracks in the efficiency calculation that are crossing the inactive area between the two double sensors.

(a) Before irradiation
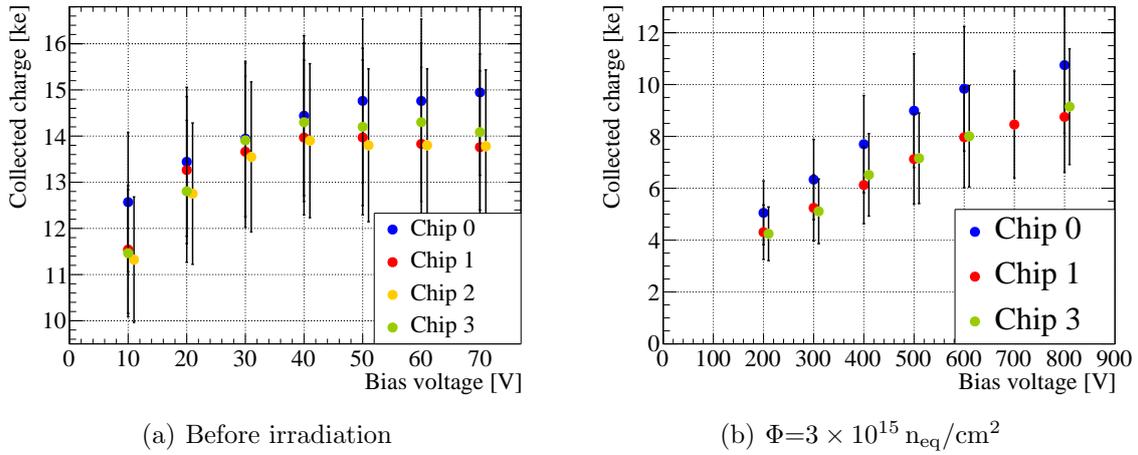
(b) $\Phi = 3 \times 10^{15}\ \mathrm{n_{eq}/cm^2}$

Figure 6.41: Charge collection of the quad modules. The collected charge for each chip of a quad module is measured as a function of the bias voltage in (a) before irradiation and in (b) after irradiation to a fluence of $3 \times 10^{15}\ \mathrm{n_{eq}/cm^2}$. For better visibility the fully correlated uncertainties are drawn as simple bars, the yellow points in (b) are displaced by $+1\,\mathrm{V}$ and the green points in (b) are displaced by $+10\,\mathrm{V}$.

(a)

(b)
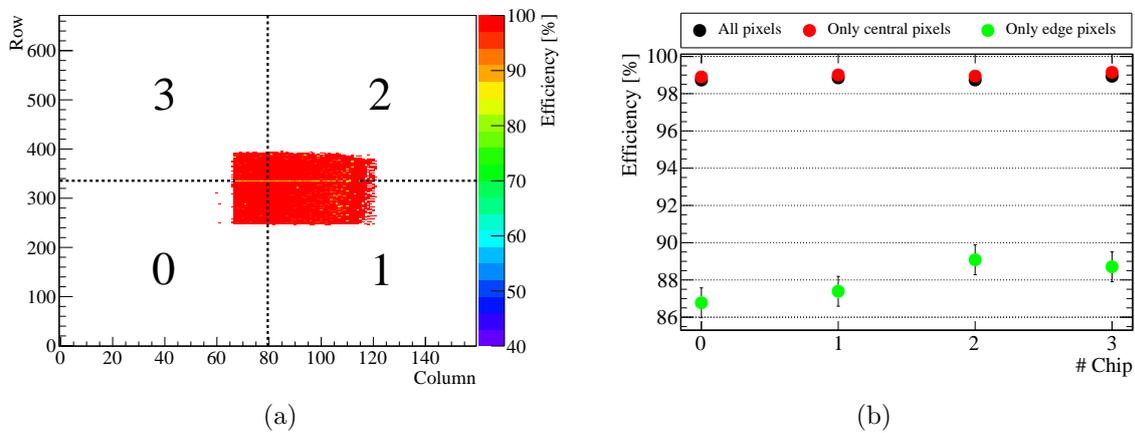
Figure 6.42: Hit efficiency of the quad module before irradiation. (a) shows the distribution over the full module surface. The pairs of chips 0-1 and 2-3 are interconnected to a double sensor each. In (b) the hit efficiency is shown per chip for all pixel cells (black dots), for the pixel cells at the edge between the two double sensors (green dots), and for all pixel cells but the ones at the edge between the two double sensors (red dots). Where not visible, the uncertainties are smaller than the marker size.

6.6 New sensor designs for Phase II

Two new sensor designs were implemented on FE-I4 modules in the CiS3 production, with an active thickness of 270 μm, to investigate the performance of a smaller pixel pitch and study the effect of different bias rail layouts. The characterisation of these new structures was performed with beam test measurements at DESY and is presented in the following. An overview of the measured modules is given in Table 6.7. The results obtained for the FE-I4 sensor design with $(25 \times 500)\,\mu m^2$ pitch are shown in Section 6.6.1. In Section 6.6.2 the performance of the different bias rail structures is compared.

Table 6.7: Overview of the measured modules of the CiS3 production and their irradiations.

One bias dot per four pixels	Different bias rail layouts	Pitch x [μm]	Pitch y [μm]	Irradiation site	Fluence $[10^{15}\,n_{eq}/cm^2]$
yes	no	25	500	-	0
				KIT	3
no	yes	50	250	-	0
				KIT	3

6.6.1 Smaller pitch

For the Phase II upgrade of the ATLAS pixel detector, a new readout chip is under development to be employed in the two innermost barrel layers [68]. In addition to the radiation hardness, this chip will have to fulfil the occupancy requirements for pixel modules at HL-LHC which lead to the implementation of a smaller pitch. The proposed chip design foresees a $(50 \times 50)\,\mu m^2$ grid of pixel cells, compatible both with pixel pitches of $(50 \times 50)\,\mu m^2$ or $(25 \times 100)\,\mu m^2$. To investigate the performance of these different pixel dimensions planned for the φ coordinate of the ATLAS detector, a planar sensor prototype featuring a pixel pitch of $(25 \times 500)\,\mu m^2$ was included in the CiS3 production (see Section 6.1.3). This sensor design, shown in Figure 6.43, is compatible with the presently available FE-I4 chip through a rearrangement of readout channels leading to a module with 40 columns and 672 rows. Moreover, each bias dot is connected to four pixel implants reducing to 1/4 the area occupied by this structure in the pixel cell with respect to standard FE-I4 sensors. In this section the cluster properties of the 25 μm pitch and the effects on the hit efficiency of the new punch through design are investigated and compared with the standard FE-I4 layout before and after irradiation.

Cluster size

An FE-I4 module with the standard $(50 \times 250)\,\mu m^2$ pitch and the new $(25 \times 500)\,\mu m^2$ layout were measured before irradiation in the same beam test at DESY using perpendicular incident tracks. The cluster width distribution measured for the x and y direction are compared in Figure 6.44. For the width in the x direction the difference is less than 1 %, while in the y direction the diffusion effect is dominant for the $(25 \times 500)\,\mu m^2$ design for which the clusters with a width of two pixels are more than 50 %, almost twice as for the standard FE-I4 design. The smaller pitch reduces the overall occupancy, but at the same time increases the charge sharing probability due to diffusion of the charge carriers. The sum of these two effects leads to

Figure 6.43: Layout of the $(25 \times 100)\,\mu m^2$ FE-I4 compatible sensor design with a photograph of the produced device in the insert.

a 42 % lower occupancy per length in the x direction for the 25 µm pitch with respect to the 50 µm pitch. The occupancy is expected to decrease for thinner or irradiated sensors, since the lateral diffusion is proportional to the drift time of the charge carriers (see Section 2.1.3), and thus depends on the depleted thickness.

(a) Cluster width x
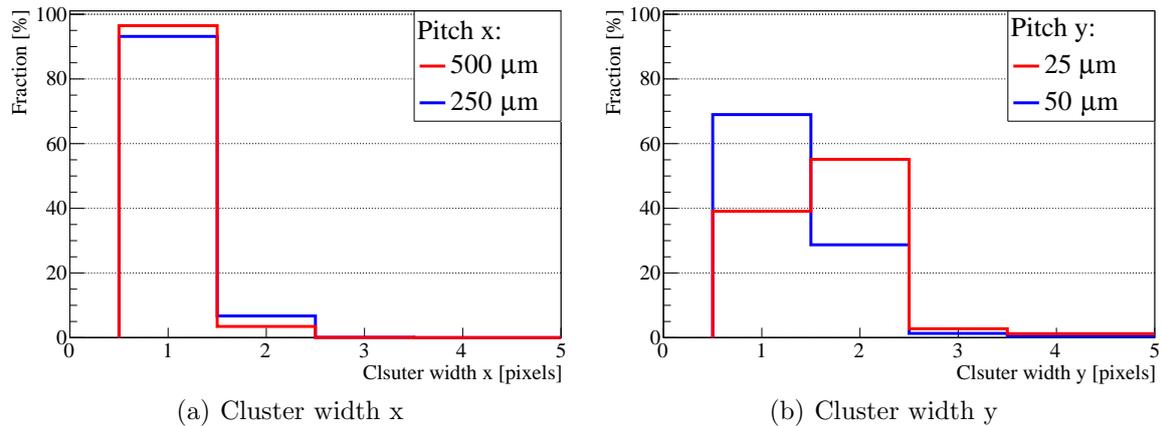
(b) Cluster width y

Figure 6.44: Comparison of the cluster width in x (a) and y (b) of two not irradiated sensors with different pitches of $(25 \times 500)\,\mu m^2$ and $(50 \times 250)\,\mu m^2$. Both sensors are from the CiS3 production and have a thickness of 270 µm.

The same $(25 \times 500)\,\mu m^2$ FE-I4 module design was measured with perpendicular incident tracks at DESY after irradiation to a fluence of $3 \times 10^{15}\,n_{eq}/cm^2$. The results obtained for the cluster width in x and y are shown for different bias voltages in Figure 6.45. With respect to the measurement before irradiation the cluster width 2 is always very low even at the highest measured voltage of 500 V where it represents only 15 % of the clusters. The charge diffusion is in fact strongly limited by the trapping and only a small increase of the charge sharing with the bias voltage is observed which reflects the increase of the depletion depth.
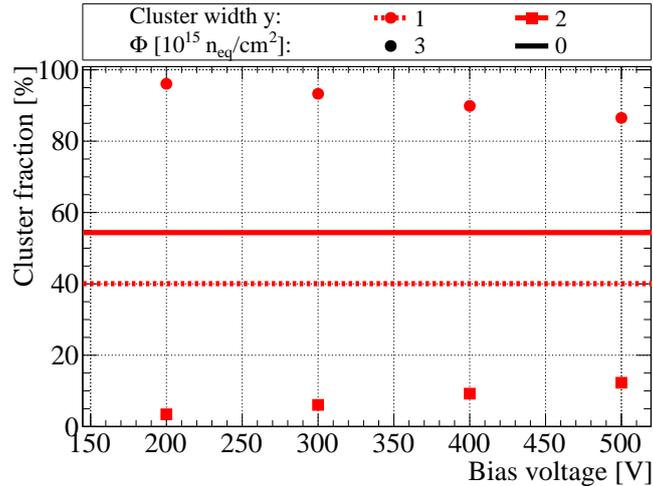
Figure 6.45: Cluster width in y as a function of the bias voltage of the CiS3 module with $(25 \times 500)\,\mu m^2$ pitch after irradiation to a fluence of $3 \times 10^{15}\,n_{eq}/cm^2$. The horizontal lines denote the cluster fractions of cluster width 1 and 2 in y before irradiation.

Hit efficiency

The performance of the bias dot structure of the $(25 \times 500)\,\mu m^2$ FE-I4 module design is investigated through the measurement of the hit efficiency. The distribution of the hit efficiency inside the pixel cell for the $(25 \times 500)\,\mu m^2$ design and for a standard FE-I4 design of the same thickness and production is shown in Figure 6.45. The two modules are both irradiated to a fluence of $3 \times 10^{15}\,n_{eq}/cm^2$ and operated at V_b=500 V. Because of the poor resolution at DESY, due to multiple scattering, the shape of the bias dot cannot be clearly distinguished. The overall area where a lower hit efficiency is observed is anyhow clearly reduced with respect to the standard FE-I4 design. The hit efficiency reaches 99.4 % at the highest measured voltage of 500 V which is around 2 % higher than the 97.7 % measured for the standard FE-I4 design before irradiation.

6.6.2 New bias rail layouts

The biasing structures were found to be the main limitation for the performance of planar pixel modules when dealing with high irradiation doses or even for very thin modules. A reduced collected charge was observed not only in the bias dot region, but also in correspondence of the bias rail. As previously shown in Section 6.3.2, this effect becomes more critical as the area of the pixel cell is reduced, since the fraction of space that these structures occupy on the sensor surface increases. In the CiS3 production, two new bias rail layouts, designed at the Dortmund University for n-in-n sensors [128], are implemented on n-in-p sensors. In these designs, shown in Figure 6.8, the bias rails are partially superimposed to the pixel implants, instead of being located between them, hence they are expected to have a reduced impact on the electric field and on the charge collection in the active bulk. In this section the performance of these designs after irradiation are investigated and compared with the standard one presently used for the FE-I4 ATLAS modules.

(a) $(25 \times 500)\,\mu m^2$ shared bias dot
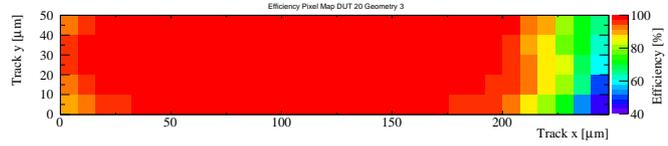
(b) $(50 \times 250)\,\mu m^2$ standard bias dot

Figure 6.46: Comparison of the hit efficiency over the pixel cell for the FE-I4 modules of the CiS3 production irradiated to a fluence of $3 \times 10^{15}\,n_{eq}/cm^2$, with different pixel pitches and when employing a different bias dot layouts. (a) shows the hit efficiency for the module with $(25 \times 500)\,\mu m^2$ pitch and one bias dot shared among four pixels. (b) shows the hit efficiency for the standard FE-I4 design with $(50 \times 250)\,\mu m^2$ pitch and one bias dot per pixel. The hit efficiency maps of the pixel cells are obtained displaying the reconstructed track impact point expressed in pixel coordinates and projecting the data for all identical structures onto the same image. For better visibility the map dimension in y are not to scale.

Hit efficiency

Three different bias rail designs based on the punch through mechanism are implemented on the same FE-I4 module. The module surface is divided in bands of ten columns each which alternate the three layouts. These include the standard FE-I4 bias rail shown in Figure 6.47(a), and two new layouts in which the bias rail is superimposed on the pixel implants shown in Figures 6.47(b) and 6.47(c). The hit efficiencies for the different structures of this module, after irradiation to $3 \times 10^{15}\,n_{eq}/cm^2$ were measured at DESY with perpendicular incident tracks to the pixel surface operating the module at 800 V. The distributions across the pixel cell, shown in Figure 6.47, reveal that the lower hit efficiency is measured in correspondence to the bias rail when this lies outside the pixel implant. The highest hit efficiency of 98.7 % is measured for the layout in Figure 6.47(b), while the standard bias structure, in Figure 6.47(a), shows an hit efficiency of 97.7 %. As expected, the layout in Figure 6.47(c) shows the lowest hit efficiency of 95.8 %, due to the large space occupied by the bias rail outside of the pixel implants. This is anyhow the only design in which the inefficiency caused by the bias dot is completely disentangled from the effect of the bias rail. From Figure 6.47(c) it is indeed evident that the hit efficiency is higher where the bias rail is completely superimposed to the implant than in the bias dot area, even if the low pointing resolution at DESY does not allow for a quantification of the inefficiency given exclusively by this area. Further measurement to be performed at CERN will allow to obtain a quantification of these different effects.

(a) Standard bias rail

(b) Design I

(c) Design II
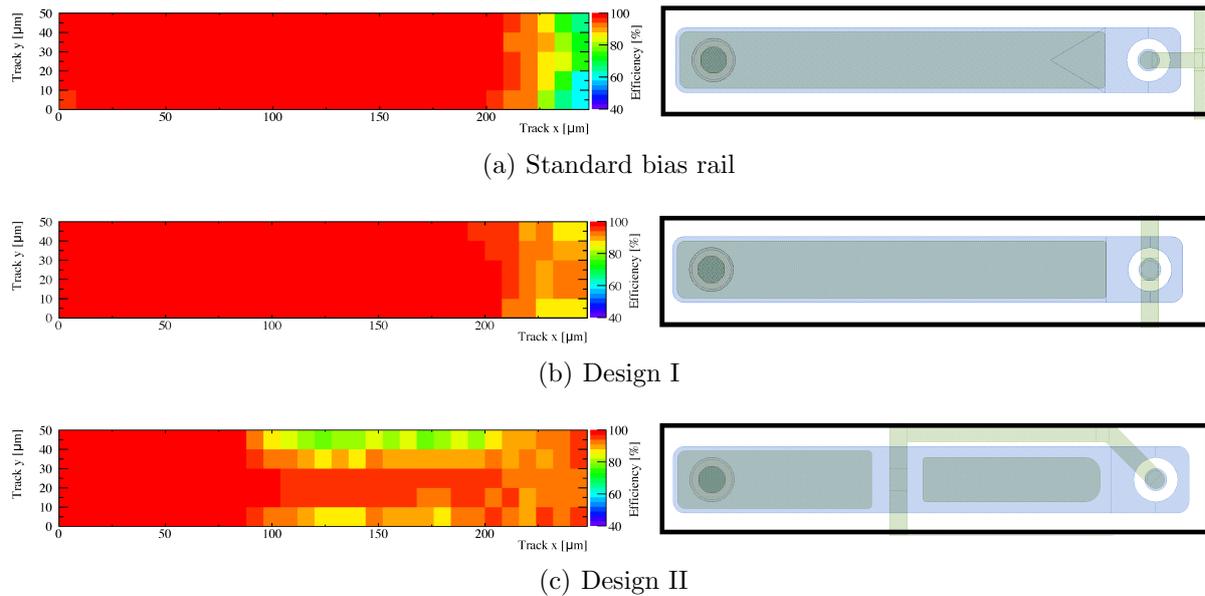
Figure 6.47: Hit efficiency over the pixel cell for the different bias rail designs implemented in the CiS3 production after a fluence of $3 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$. The hit efficiencies over the pixel cell for perpendicular incident tracks are shown on the left and the correspondent pixel cell structures on the right. The standard bias rail structure of the FE-I4 planar pixel sensors is shown in (a) and the two new designs are shown in (b) and (c), respectively. All modules were operated at $800\,\mathrm{V}$ with a threshold of $1.6\,\mathrm{ke}$. The hit efficiency maps of the pixel cells are obtained displaying the reconstructed track impact point expressed in pixel coordinates and projecting the data for all identical structures onto the same image.

6.7 Conclusions and outlook

Different prototypes of planar n-in-p pixel sensors were investigated as possible candidates
for the ATLAS Phase II upgrade. These include thin sensors, thin sensors with active edges
for the innermost layers, large area sensors for the outer layers and new pixel designs. Many
aspects were considered to fulfil the requirements imposed by the HL-LHC scenario, namely
the radiation hardness, the active area and the occupancy in different regions of the detector.

6.7.1 Radiation hardness and hit efficiency

At the high radiation fluences expected at HL-LHC, thick sensors, as the ones presently employed
in the ATLAS pixel detector, will operate inevitably under depleted. Given the new generation
of readout chips capable of handling very small signals, a reduction of the sensor thickness is
thus a natural step for planar pixel sensors to face harsh radiation environments. Pixel modules
with different sensor thicknesses were characterised and $100\,\mu m$ thick sensors showed the best
performance in terms of collected charge and hit efficiency at moderate voltages (200–300 V) at
a fluence of $5 \times 10^{15}\,n_{eq}/cm^2$. The characterised FE-I4 and FE-I3 modules with $100\,\mu m$ thick
sensors produced at VTT showed a hit efficiency of more than 95 % already at $V_b = 200\,V$.
Their performance was observed to be mainly limited by the bias dot and bias rail structures. In
fact, excluding these areas, a hit efficiency for perpendicular incident particles of $(99.7 \pm 0.3)\,\%$
was measured. Even if the inefficiency caused by the biasing structures was shown to be less
critical for particles crossing the sensor not perpendicularly to the pixel surface, an optimisation
of the bias rail and bias dot design is fundamental for the performance of the foreseen pixel
modules of Phase II, where due to the reduced pixel pitch, the fraction of active area occupied
by these biasing structures will become larger. A common bias dot shared by four pixel cells
was implemented on $270\,\mu m$ thick FE-I4 sensors and characterised after irradiation to a fluence
of $3 \times 10^{15}\,n_{eq}/cm^2$. This layout showed a hit efficiency of $(99.4 \pm 0.3)\,\%$ at $V_b = 500\,V$, almost
2 % higher than for the standard bias dot design. Moreover, the investigations performed
for different bias rail designs have shown an improved hit efficiency when these structures
are superimposed to the pixel implants. Based on these investigations, the new thin sensor
prototypes under development will thus maximise the fraction of bias rail area over the implant
employing at the same time the common bias dot layout.

6.7.2 Active area

The active edge process developed at VTT was demonstrated to be an optimal solution to
extend the active area of n-in-p sensors. The edge implantation allows to reduce the number of
guard rings and achieve slim edge designs with only $125\,\mu m$ of inactive edge or also fully active
edge sensors. This last design was demonstrated to be fully active before irradiation, showing a
optimal hit efficiency even in the last $50\,\mu m$ between the last pixel implant and the activated
edge. However, this design still needs to be further investigated after high radiation fluences
with beam test measurements, due to the early breakdown observed, which could compromise
its use for the innermost layers of the future pixel detector. In particular additional studies are
needed to understand if the breakdown behaviour should be attributed entirely to the short
distance between the edge and the active area or if it could be at least partially explained with
the absence of a coating layer such as Parylene or BCB. In the next active edge productions
the slim edge design will be pushed further for modules with only $100\,\mu m$ of inactive area at the

sensor edge and the fully active edge concept will be implemented for FE-I4 chips and further characterised after irradiation.

6.7.3 Large sensors

A prototype activity for large area modules suitable for the outer layers has started by producing quad assemblies with FE-I4 chips. A first design of quad modules composed of two double chip sensors was characterised before and after irradiation to a fluence of $3 \times 10^{15} \, \mathrm{n_{eq}/cm^2}$. The overall performance was measured to be mostly compatible with single chip modules both before and after irradiation, even if, in this second case, a higher noise and difficulties in the tuning procedure were experienced. Further investigations on quad modules are planned both for the CiS2 and the new CiS3 productions using the flex readout described in Section 4.1, which is expected to solve most of the problems encountered with the present readout system.

6.7.4 Small pixel pitch

The new readout chip under development for both ATLAS and CMS will be compatible with two pixel pitches of $(50 \times 50) \, \mathrm{\mu m^2}$ and $(25 \times 100) \, \mathrm{\mu m^2}$. The performance of these two possible layouts was investigated with module prototypes employing the presently available FE-I4 chip. An FE-I4 compatible module prototype employing a $270 \, \mathrm{\mu m}$ thick sensor from the CiS3 production, with $(25 \times 500) \, \mathrm{\mu m^2}$ pixel pitch was characterised before and after irradiation to a fluence of $3 \times 10^{15} \, \mathrm{n_{eq}/cm^2}$. The smaller pitch leads to an increase of the charge sharing of more than $40 \, \%$ with respect to the presently used $50 \, \mathrm{\mu m}$ pitch. Nevertheless, the charge sharing effect is strongly suppressed after irradiation and is expected to be even further reduced for thinner sensors. The pixel efficiency of a $50 \, \mathrm{\mu m}$ pitch was measured for highly tilted incident tracks as expected in the high-η region of the ATLAS detector. A pixel efficiency of more than $99.5 \, \%$ was measured before irradiation. For $150 \, \mathrm{\mu m}$ sensors irradiated to a fluence of $4 \times 10^{15} \, \mathrm{n_{eq}/cm^2}$, the collected charge showed a strong dependence on the distance from the pixel implant at which the particle crosses the sensor and it is therefore sensitive to the detector thickness. To quantify this effect, further investigations are ongoing, combining TCAD simulations and beam test measurement, to better understand the charge collection properties after irradiation at different depths and for different sensor thicknesses.

7 The Through Silicon Via technology

In the ATLAS experiment, the space constraints for the design of an innermost pixel layer placed as close as possible to the IP set severe requirements for the active area of the pixel modules. In the present pixel module design a large inactive area is represented by the chip balcony dedicated to the wire bonding pads as illustrated in Figure 3.7(a). In the MPP module concept for the ATLAS Phase II, described in Section 3.3, a solution to remove this balcony is given by the TSV approach which, combined with the active edge technology on the sensor side, would lead to a fully active four side buttable module. The TSV technology allows to convey the signal to the backside of the readout chip by etching conductive channels (vias) through the chip itself. The connection with the flex readout can then be performed directly on the backside of the chip and the sensor can extend up to the chip edge in all four module sides.

   In the recent years the use of TSVs has been widely investigated in the field of hybrid pixel sensors for high energy physics experiments, especially in the framework of the AIDA project[1]. In particular, successful experiences were reported for TSV with a low aspect ratio, in the range from 1:2 to 1:3 (depth : diameter), applied, as a proof of concept, on the wire bonding pads of the chip. A first prototype of TSVs was processed by IZM on FE-I3 chips [169], while a second one consists of TSVs with a technology developed by CEA-LETI[2] for the MEDIPIX[3] Collaboration [170]. A further challenge is represented by TSVs with a higher aspect ratio, up to 10:1, which could in the future be implemented at the single pixel level allowing a physical separation of the analog and digital parts of the chip. In this chapter the experience of the realisation of high aspect ratio TSVs on prototype chips is reported.

7.1 The TSV process

A TSV process was developed by EMFT [171], with the "via last" approach, which is performed on the already finished chips at wafer level. The process was performed on FE-I2 chips to realise a first prototype. Since this chip is not designed for TSVs, the vias were etched below the wire bonding pads, to avoid the damage of the analog and digital layers. The different processing steps performed at EMFT to achieve the TSVs are described in the following.

7.1.1 Frontside processing

After having removed the aluminium layer present on the wire bonding pads, 50–60 µm deep channels are etched through the chip layers from the frontside using the DRIE technique and insulated with Chemical Vapour Deposition (CVD) of a silicon dioxide layer. A trench is also etched down to the same depth around the via volume to insulate the wire bonding pads from each others. As shown in Figure 7.1 both the trench and the channels have a width of about 2.6 µm. With the same CVD technique a 60 nm thick conductive layer of TiN is deposited to

---

[1]aida.web.cern.ch
[2]http://www-leti.cea.fr/
[3]http://medipix.web.cern.ch/

cover the internal walls of the channels and serving as an adhesion layer. The vias are then filled with tungsten to allow the signal transmission to the backside.

(a) Vias before tungsten filling

(b) Vias after tungsten filling

(c) Insulating trench

(d) Via
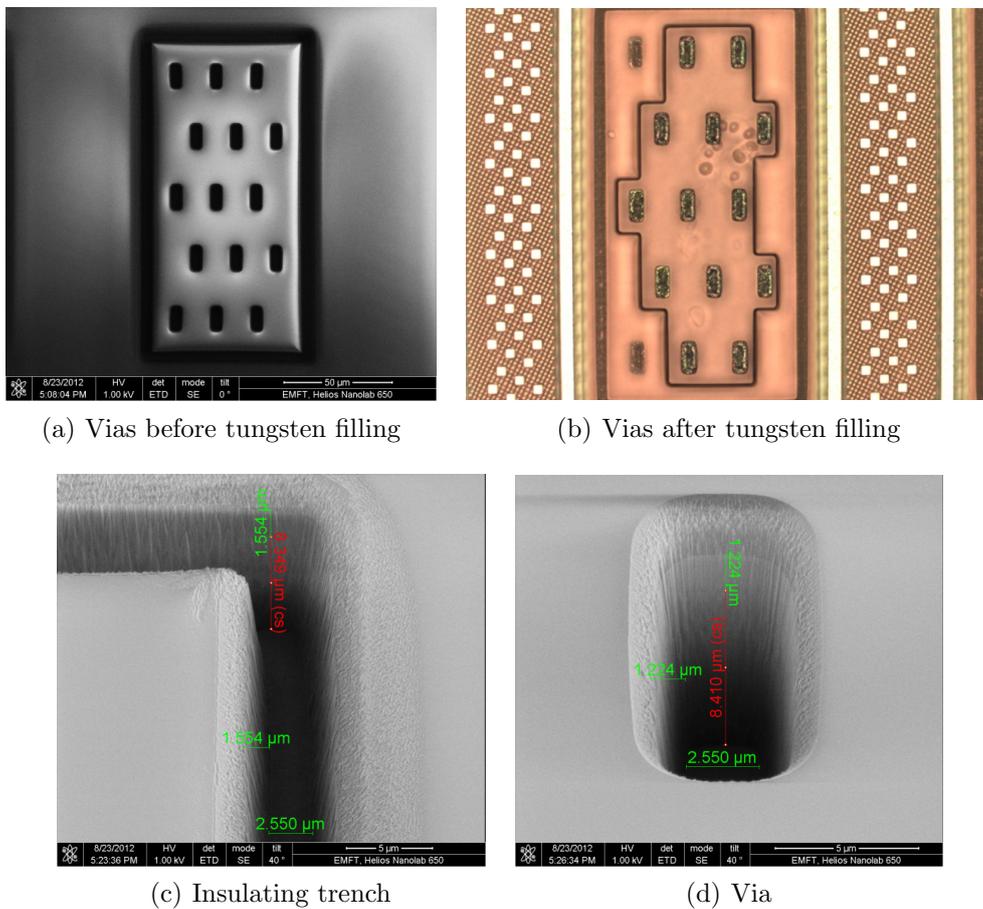
Figure 7.1: The TSV process on the chip frontside. The vias on one wire bonding pad are shown before (a) and after (b) the tungsten filling was performed. A close up of the trench (c) and of one via (d) are shown before the tungsten filling in which the widths and the depth are noted in green and red, respectively. Photographs from [114].

7.1.2 Backside processing

For the next processing steps the frontside of the chip wafer is attached to a handle wafer and is thinned from the backside to around $60\,\mu m$ to expose the vias and the trench. At this stage, an additional CMP process was necessary to cut down the insulation trench, which resulted to be $3\,\mu m$ deeper than the enclosed vias in a such a way that the walls were extruding from the backside surface. After this process a further deposition of insulation oxide was performed in the trench. The access to the metallic core of the TSVs was obtained by dry etching, but after this process the vias were found to be hollow, showing a failure in the tungsten filling. As shown in Figure 7.2, only the CVD TiN coverage is visible, which was done before the tungsten filling, but this is not sufficient for the electrical contact since its resistance is too high, due to its small

thickness. Previous filling trials with tungsten on test wafer with the same TSV geometry were successful. A possible explanation of the failure in this particular run is a deterioration of the tungsten gas used in the CVD process, probably due to its ageing.
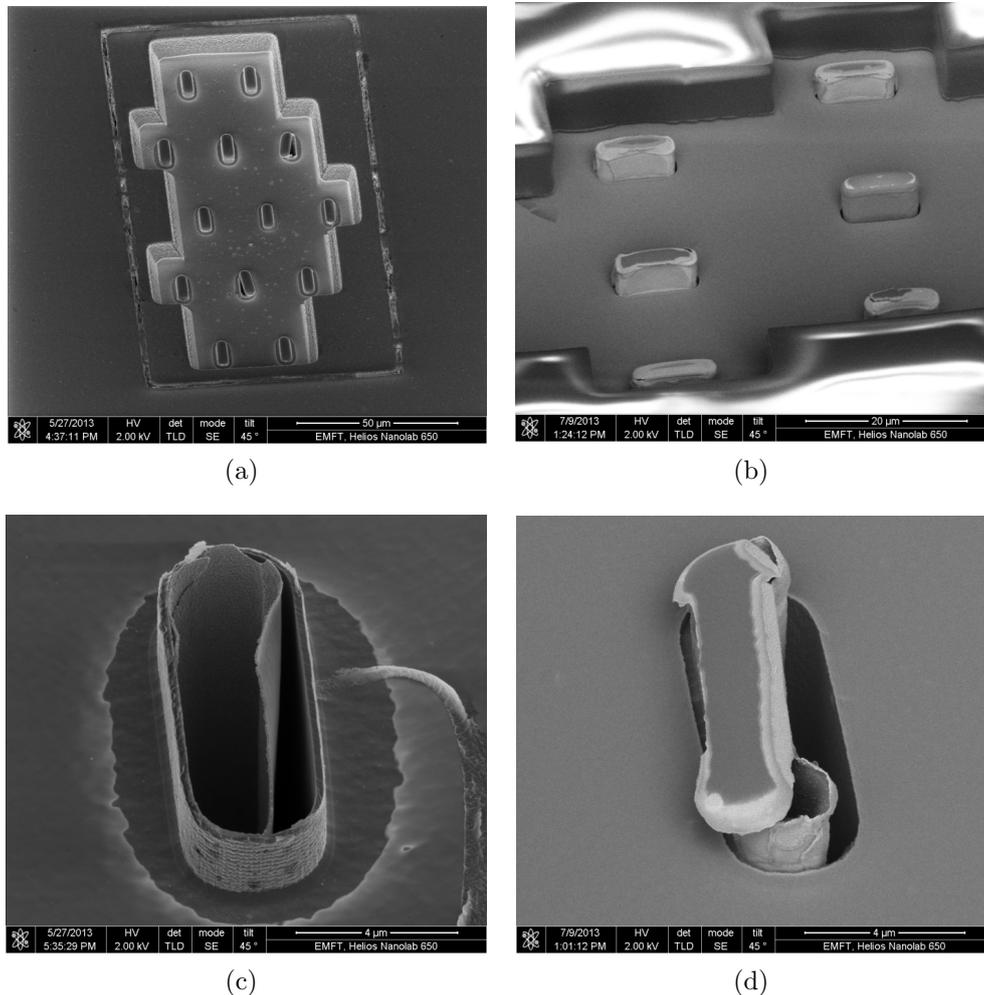
Figure 7.2: The TSV process on the chip backside. (a) shows the vias in the area corresponding to the wire bonding pads. The details of the hollow vias are shown before (b) and after (c, d) the TiN cover removal on the bottom of the channel. Photographs from [114].

7.2 Chip test

The subsequent steps would have implied the processing to create the redistribution layer on the backside, including lithography, aluminium etch and resist strip. Instead, as an alternative solution, the chip wafer was placed on a third handle wafer to electroplate the vias on the frontside and create a test contact for the chip characterisation after the partial TSV process. The aim was the verification of the chip functionality after the TSV formation, even if the vias could not be used to transport the signals to the backside. The functionality of four diced chips

was investigated through a wire-bond connection on the frontside. None of them was found to be working and they were all showing an analog current two times as higher as the operative one for an FE-I2 readout chip.

7.3 Conclusions and outlook

The attempt of implementing TSVs with high aspect ratio on FE-I2 chips by EMFT was presented. After the successful etch of the vias below the wire bonding pads from the frontside, the failure of the tungsten filling resulted in hollow channels and prevented to bring the electrical connection to the backside. The subsequent tests of the chip functionalities performed with usual wire-bond connections on the frontside revealed damages in the processed chips which hinder their operation.

In summary, even if the trials here reported for the implementation of TSVs at EMFT were unsuccessful, the feasibility of the application of this technology at the periphery of the new ATLAS chip, based on the previous fruitful experiences of low aspect ratio TSVs, is still of interest to extend the active area of the future ATLAS pixel modules. The possibility of further projects for the realisation of high ratio TSVs is presently under discussion.

8 Conclusions and Outlook

Two different silicon pixel sensor technologies designed for the upgrades of the pixel detector of the ATLAS experiment at LHC were investigated. The pixel modules presently employed in the high-pseudorapidity region of the new Insertable B-Layer, which adopt the 3D sensor technology, were characterised before irradiation and the results have been compared to simulations performed using the digitalisation algorithm implemented in the ATLAS offline software.

A novel planar module concept was presented to face the challenges imposed by the high luminosity upgrade of the LHC. This is based on n-in-p planar sensors relying on innovative aspects: thin sensors to ensure radiation hardness, active edges to maximise the sensitive area of the sensor and 3D-integration based on the TSV technology to extend the active area on the chip side. An extensive characterisation before and after high irradiation doses of different module prototypes was performed with the aim of identifying the best designs to fulfil the requirements for the different layers and pseudorapidity regions of the ATLAS pixel detector at HL-LHC.

The radiation hardness of different sensor thicknesses ranging from 100 to 300 μm was investigated by measuring the charge collection properties with beta electrons from a ^{90}Sr radioactive source and the hit efficiency with high energetic particles at beam tests. The results have been compared to the ones previously obtained for thinner and thicker sensors in Ref [79]. Planar pixel modules employing 200 μm thick n-in-p silicon sensors irradiated up to a fluence of $2\text{--}3 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$, both single chip modules and quad modules have shown a performance compatible with requirements for the outer layers where large areas need to be covered. For integrated radiation fluences of $4\text{--}6 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ as expected for the second pixel layer at HL-LHC, the best performance was instead observed for 100 μm thick sensors which reach the same hit efficiency as thicker sensors already with a bias voltage of 200–300 V. The highest hit efficiency obtained for perpendicular incident tracks at these fluences is around 97–98 % with the main inefficiency regions corresponding to the bias dot and the bias rail areas of the pixel cell. Considering only the pixel region excluding these structures a hit efficiency of more than 99 % was measured. As the pixel area reduces, the fraction of pixel surface occupied by the biasing structures increases, therefore an optimisation of these structures will be essential to improve the performance of planar pixel sensors in view of the smaller pixel pitch of the future chip design. An investigation of different biasing structures was thus performed which showed a higher hit efficiency when the bias rail is superimposed to the pixel implants, and also for a design with a single bias dot connecting four pixel cells. A design which combines these two features will be thus implemented in the next productions and further investigated. An alternative solution would be to completely remove these structures relying on the high production yield, and on the good efficiency of the bump bonding process to avoid disconnected channels.

The possibility of obtaining an optimal performance with a moderate bias voltage was demonstrated to be the fundamental advantage of thin pixel sensors after irradiation. While at the irradiation fluence of $1.4 \times 10^{16}\,\mathrm{n_{eq}/cm^2}$ expected for the innermost layer, 200 μm thick sensors require at least 800 V to achieve a hit efficiency of $(89.4 \pm 0.3)\,\%$, planar pixel modules

with 100 µm thick sensors are promising candidates especially for the high-pseudorapidity region where 3D sensors lose the conceptual advantage of decoupling charge collection distance and active thickness. Further characterisation of these modules will be therefore necessary to measure their performance at irradiation fluences exceeding 10^{16} n_{eq}/cm^2 and in particular to understand the requirements in terms of cooling to operate them avoiding the risk of thermal runaway.

Another challenge for the two innermost layers is given by the space constrains imposed by the Phase II layout which prevents the overlap of modules along the z direction and therefore demands to reduce as much as possible the dead areas. A solution based on active edge sensors was investigated which allows to obtain slim edge sensors where the active area extends up to a distance of 125 µm from the edge and even fully active sensors. The edge pixels of the 100 µm thick slim edge sensors showed charge collection and hit efficiency properties consistent with the central pixels even at an irradiation fluence of 5×10^{15} n_{eq}/cm^2. The active sensor design was demonstrated to be effectively fully active before irradiation showing an average hit efficiency of $(87.4 \pm 0.7)\,\%$ in the last 50 µm between the last pixel implant and the activated edge. Further investigations of this design are required to understand if the low breakdown voltage observed after irradiation is due to sparks between the sensor edge and the chip surface. In this case the operational bias voltage can be extended by applying an insulating layer of BCB or Parylene. If demonstrated to be radiation hard, active edge sensors eventually completed on the chip side by 3D-integration using the TSV technology would allow the design of a fully active module for the innermost layers of the ITk at HL-LHC.

Additional studies were performed for the pixel modules in the innermost layer at high pseudorapidity where the particles traverse several pixels. In these conditions, thinner sensors have the advantage of a lower cluster size which results in a reduced occupancy and, after irradiation, are expected to perform better since the higher electric field counteracts the trapping effects. For the ATLAS Phase II a smaller pitch in the z direction is foreseen, which together with an optimal single pixel efficiency would allow to increase the precision for measuring both the entrance and the exit point of particles crossing the pixel modules at high pseudorapidity and thus obtaining a track seed with the standalone innermost layer. The performance of a 50 µm pitch along z was therefore investigated with FE-I4 modules showing a single pixel efficiency of more than 99.6 % before irradiation. Further measurements after irradiation will be crucial to determine the real advantages of employing such a small pixel pitch in the high-pseudorapidity region of the detector instead of a $(25 \times 100)\,µm^2$ pitch solution which would guarantee a higher collected charge with a reduced occupancy in φ as demonstrated with the first investigations performed on 270 µm thick sensors with a pitch of $(25 \times 500)\,µm^2$.

Due to the reduced production costs and the radiation hard properties demonstrated, quad modules employing n-in-p planar pixel sensors with an active thickness of 200 µm are the most promising candidates to cover the large areas of the outermost two or eventually three pixel layers. Moreover, 100 µm thick n-in-p planar pixel sensors complemented with the active edge technology were demonstrated to be able to fulfil the requirements in terms of hit efficiency and active area imposed by the high luminosity upgrade of LHC up to the second innermost layer of the foreseen ATLAS pixel detector. Further investigations will be crucial to understand the necessary operational bias voltage and the consequent cooling requirements for which this sensor technology could be employed in the innermost layer.

List of Abbreviations and Acronyms

ADC   Analogue to Digital Converter

ALICE   A Large Ion Collider Experiment

ASIC   Application Specific Integrated Circuit

ATCA   Advanced Telecommunication Computing Architecture

ATLAS   A Toroidal LHC ApparatuS

BCB   BenzoCycloButene

BSM   Beyond the Standard Model

CCE   Charge Collection Efficiency

CERN   Conseil Européen pour la Recherche Nucléaire

CIM   Cluster Interconnect Module

CiS   CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH

CMOS   Complementary Metal Oxide Semiconductor

CMP   Chemical Mechanical Polishing

CMS   Compact Muon Solenoid

CNM   Centre Nacional de Microelectrònica

CSC   Cathode Strip Chamber

CVD   Chemical Vapour Deposition

DAC   Digital to Analogue Converter

DAQ   Data Acquisition

DESY   Deutsches Elektronen-Synchrotron

DRIE   Deep Reactive Ion Etching

DUT   Device Under Test

ECAL   Electromagnetic CALorimeter

EMFT   Fraunhofer-Einrichtung für Modulare Festkörper-Technologien

EOC   End-Of-Column

FBK   Fondazione Bruno Kessler

FPGA   Field-Programmable Gate Array

FWHM   Full Width Half Maximum

FZ   Float Zone

HCAL   Hadronic CALorimeter

HL-LHC   High Luminosity Large Hadron Collider

HSIO   High Speed Input/Output Module

IBL   Insertable B-Layer

TSV   Through Silicon Via

ID   Inner Detector

IP   Interaction Point

ITk   Inner Tracker

IZM   Fraunhofer Institut für Zuverlässigkeit und Mikrointegration

JSI   Jožef Stefan Institute

KIT   Karlsruher Institut für Technologie

LAr   Liquid Argon

LANSCE	Los Alamos Neutron Science CEnter
LAL	Laboratoire de l'Accélérateur Linéaire
LEIR	Low Energy Ion Ring
LEP	Large Electron Positron collider
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LINAC	LINear ACcelerator
LOI	Letter Of Intent
LPNHE	Laboratoire de Physique Nuclèaire et des Hautes Ènergies
LS	Long Shutdown
MAPS	Monolithic Active Pixel Sensors
MCC	Module Controller Chip
MCz	Magnetic Czochralski
MDT	Monitored Drift Tube
MIP	Minimum Ionising Particle
MPG HLL	Halbleiterlabor der Max-Planck-Gesellschaft
MPP	Max-Planck-Institut für Physik (Werner-Heisenberg-Institut)
MPV	Most Probable Value
MWPC	Multi-Wire Proportional Chamber
NIEL	Non-Ionizing Energy Loss
PCB	Printed Circuit Board
PPS	Planar Pixel Sensor
PS	Proton Synchrotron
RCE	Reconfigurable Cluster Element
RMS	Root Mean Square

RoI	Region of Interest
RPC	Resistive Plate Chamber
SCT	SemiConductor Tracker
SLAC	Stanford Linear Accelerator Center
SLID	Solid Liquid Inter-Diffusion
SM	Standard Model
SpS	Super proton Synchrotron
SUSY	Supersymmetry
TGC	Thin Gap Chamber
ToT	Time over Threshold
TMAH	Tetramethylammonium hydroxid
TRT	Transition Radiation Tracker
TTL	Transistor-Transistor-Logic
UBM	Under-Bump Metallisation
USB	Universal Serial Bus
VME	Versa Module Eurocard
VTT	Valtion Teknillinen Tutkimuskeskus

List of Figures

List of Tables

Bibliography

[1] L. Evans and P. Bryant (editors), *LHC Machine*, JINST **3** (2008) S08001.

[2] S. Myers, *The Large Hadron Collider 2008-2013*, Int. J. Mod. Phys. **A28** (2013).

[3] O. S. Brüning et al., *LHC Design Report*, CERN, (2004).

[4] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, JINST **3** (2008) S08003.

[5] ALICE Collaboration, *The ALICE experiment at the CERN LHC*, JINST **3** (2008) S08002.

[6] CMS Collaboration, *The CMS experiment at the CERN LHC*, JINST **3** (2008) S08004.

[7] LHCb Collaboration, *The LHCb Detector at the LHC*, JINST **3** (2008) S08005.

[8] C. Lefèvre, *The CERN accelerator complex*, CERN, (2008), CERN-DI-0812015.

[9] CERN, *LHC Performance and Statistics*, `https://acc-stats.web.cern.ch/acc-stats/`.

[10] HL-LHC Parameter and Lay-out Committee, *HL-LHC Parameters V4.1.1*, (Last updated on 16 December 2014), `https://espace.cern.ch/HiLumi/PLC/default.aspx`.

[11] O. S. Brüning and F. Zimmermann, *Parameter Space for the LHC Luminosity Upgrade*, Proceedings of the 3rd International Conference on Particle accelerator (IPAC 2012) (2012) 127.

[12] A. Piwinski, *Intra-Beam-Scattering*, Proceedings of the IXth International Conference on High Energy Accelerators (1974) 405.

[13] ATLAS Collaboration, *Luminosity Public Results*, `https://twiki.cern.ch/twiki/bin/view/AtlasPublic/LuminosityPublicResults`.

[14] F. Englert et al., *Broken Symmetry and the Mass of Gauge Vector Mesons*, Phys. Rev. Lett. **13** (1964) 321.

[15] P. W. Higgs, *Broken Symmetries, massless particles and gauge fields*, Phys. Lett. **12** (1964) 132.

[16] P. W. Higgs, *Broken Symmetries and the Masses of Gauge Bosons*, Phys. Rev. Lett. **13** (1964) 508.

[17] P. W. Higgs, *Spontaneous Symmetry Breakdown without Massless Bosons*, Phys. Rev. **145** (1966) 1156.

[18] G. Guralnik, C. Hagen, and T. W. B. Kibble, *Global Conservation Laws and Massless Particles*, Phys. Rev. Lett. **13** (1964) 585.

[19] T. W. B. Kibble, *Symmetry Breaking in Non-Abelian Gauge Theories*, Phys. Rev. **155** (1967) 1554.

[20] ATLAS Collaboration, *Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC*, Phys. Lett. **B716** (2012) 1.

[21] CMS Collaboration, *Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC*, Phys. Lett. **B716** (2012) 30.

[22] ATLAS Collaboration, *ATLAS Inner Detector: Technical Design Report 1*, CERN, (1997), CERN-LHCC-97-016.

[23] ATLAS Collaboration, *ATLAS Inner Detector: Technical Design Report 2*, CERN, (1997), CERN-LHCC-97-017.

[24] ATLAS Collaboration, *ATLAS Calorimeter Performance: Technical Design Report*, CERN, (1996), CERN-LHCC-96-040.

[25] ATLAS Collaboration, *ATLAS Liquid-Argon Calorimeter: Technical Design Report*, CERN, (1996), CERN-LHCC-96-041.

[26] ATLAS Collaboration, *ATLAS Tile Calorimeter: Technical Design Report*, CERN, (1996), CERN-LHCC-96-042.

[27] ATLAS Collaboration, *ATLAS Muon Spectrometer: Technical Design Report*, CERN, (1997), CERN-LHCC-97-022.

[28] ATLAS Collaboration, *Review of the ATLAS Muon TDR*, CERN, (1997), CERN-LHCC-97-047.

[29] ATLAS Collaboration, *ATLAS Magnet System: Technical Design Report*, CERN, (1997), CERN-LHCC-97-018.

[30] J. P. Badiou et al., *ATLAS barrel toroid: Technical Design Report*, CERN, (1997), CERN-LHCC-97-019.

[31] ATLAS Collaboration, *ATLAS End-Cap Toroids: Technical Design Report*, CERN, (1997), CERN-LHCC-97-020.

[32] ATLAS Collaboration, *ATLAS Central Solenoid: Technical Design Report*, CERN, (1997), CERN-LHCC-97-021.

[33] J. Pequenao, *Computer generated image of the whole ATLAS detector*, CERN, (2008), CERN-GE-0803012.

[34] ATLAS Collaboration, Pixel Detector Technical Design Report, `http://atlas.web.cern.ch/Atlas/GROUPS/INNER_DETECTOR/PIXELS/tdr.html`.

[35] G. Aad et al., *ATLAS pixel detector electronics and sensors*, JINST **3** (2008) P07007.

[36] M. Capeans et al., *ATLAS Insertable B-Layer Technical Design Report*, CERN, (2010), CERN-LHCC-2010-013.

[37] Y. Unno, *ATLAS silicon microstrip Semiconductor Tracker (SCT)*, Nucl. Instr. Meth. **A453** (2000) 109.

[38] A. Ahmad et al., *The silicon microstrip sensors of the ATLAS semiconductor tracker*, Nucl. Instr. Meth. **A578** (2007) 98.

[39] F. Martin, *The ATLAS transition radiation tracker (TRT) from construction to installation*, Nucl. Instr. Meth. **A581** (2007) 535.

[40] A. Vogel, *ATLAS Transition Radiation Tracker (TRT): Straw tube gaseous detectors at high rates*, Nucl. Instr. Meth. **A732** (2013) 277.

[41] L. Rossi and O. Brüning, *High Luminosity Large Hadron Collider A description for the European Strategy Preparatory Group*, CERN, (2012), CERN-ATS-2012-236.

[42] ATLAS Collaboration, *Physics at a High-Luminosity LHC with ATLAS*, CERN, (2012), ATL-PHYS-PUB-2012-001.

[43] ATLAS Collaboration, *Search for Supersymmetry at the high luminosity LHC with the ATLAS experiment*, CERN, (2014), ATL-PHYS-PUB-2014-010.

[44] ATLAS Collaboration and CMS Collaboration, *Combined Measurement of the Higgs Boson Mass in pp Collisions at $\sqrt{s} = 7$ and 8 TeV with the ATLAS and CMS Experiments*, Phys. Rev. Lett. **114** (2015) 191803.

[45] J. Wess and B. Zumino, *Supergauge Transformations in Four-Dimensions*, Nucl. Phys. **B70** (1974) 39.

[46] H. P. Nilles, *Supersymmetry, Supergravity and Particle Physics*, Phys. Reports **110** (1984) 1.

[47] R. Barbieri, S. Ferrara, and C. A. Savoy, *Gauge Models with Spontaneously Broken Local Supersymmetry*, Phys. Lett. **B119** (1984) 343.

[48] S. Dawson, E. Eichten, and C. Quigg, *Search for Supersymmetric Particles in Hadron - Hadron Collisions*, Phys. Rev. **D31** (1985) 1581.

[49] H. E. Haber and G. L. Kane, *The Search for Supersymmetry: Probing Physics Beyond the Standard Model*, Phys. Reports **117** (1987) 75.

[50] ATLAS Collaboration, *Search for high-mass dilepton resonances in pp collisions at $\sqrt{s} = 8$ TeV with the ATLAS detector*, Phys. Rev. D **90** (2014) 052005.

[51] ATLAS Collaboration, *A search for $t\bar{t}$ resonances with the ATLAS detector in $2.05\,\mathrm{fb}^{-1}$ of proton-proton collisions at $\sqrt{s} = 7\,\mathrm{TeV}$*, The European Physical Journal C **72** (2012).

[52] HL-LHC: High Luminosity Large Hadron Collider, `http://hilumilhc.web.cern.ch/`.

[53] L. Arnaudon et al., *Linac4 Technical Design Report*, CERN, (2006), CERN-AB-2006-084.

[54] O. Brüning, H. Burkhardt, and S. Myers, *The large hadron collider*, Prog. in Part. Nucl. Phys. **67** (2012) 705.

[55] G. Apollinari, O. Brüning, and L. Rossi, *High Luminosity LHC Project Description*, CERN, (2014), CERN-ACC-2014-0321.

[56] L. Bottura et al., *Advanced Accelerator Magnets for Upgrading the LHC*, IEEE Trans. Appl. Supercond. **22** (2012) 4002008.

[57] A. Ballarino, *Development of superconducting links for the Large Hadron Collider machine*, Supercond. Sci. Tech. **27** (2014) 044024.

[58] K. Oide et al., *Beam-beam collision scheme for storage-ring colliders*, Phys. Rev. **A40** (1989) 315.

[59] K. Akai and M. Tigner, *Deflecting and Crab Cavities*, in *Handbook of Accelerator Physics and Engineering*, p. 617, World Scientific, 2006, (3rd printing).

[60] B. Muratori and T. Pieloni, *Luminosity levelling techniques for the LHC*, Proceedings of ICFA Mini-Workshop on Beam-Beam Effects in Hadron Colliders (BB2013) (2014) 177.

[61] M. Garcia-Sciveres et al., *The FE-I4 pixel readout integrated circuit*, Nucl. Instr. Meth. **A636** (2011) S155.

[62] I. Peric et al., *The FEI3 readout chip for the ATLAS pixel detector*, Nucl. Instr. Meth. **A565** (2006) 178.

[63] S. Parker et al., *3D - A proposed new architecture for solid-state radiation detectors*, Nucl. Instr. Meth. **A395** (1997) 328.

[64] ATLAS Collaboration, *Letter of Intent for the Phase-I Upgrade of the ATLAS Experiment*, CERN, (2011), CERN-LHCC-2011-012.

[65] Y. Giomataris et al., *MICROMEGAS: a high-granularity position-sensitive gaseous detector for high particle-flux environments*, Nucl. Instr. Meth. **A376** (1996) 29.

[66] J. Anderson et al., *FTK: A fast track trigger for ATLAS*, JINST **7** (2012) C10002.

[67] T. A. Martin, *Towards a Level-1 tracking trigger for the ATLAS experiment at the High Luminosity LHC*, JINST **9** (2014) C10021.

[68] J. Christainsen and M. Garcia-Sciveres, *RD Collaboration Proposal: Development of pixel readout integrated circuits for extreme rate and radiation*, CERN, (2013), CERN-LHCC-2013-008.

[69] M. Abbrescia et al., *ECFA High Luminosity LHC Experiments Workshop: Physics and Technology Challenges.*, 94th Plenary ECFA meeting, (2013), ECFA-13-284.

[70] D. Abbaneo et al., *ECFA High Luminosity LHC Experiments Workshop: Physics and Technology Developments Summary submitted to ECFA.*, 96th Plenary ECFA meeting, (2015), ECFA-15-289.

[71] ATLAS Collaboration, *ATLAS Phase-II Upgrade Scoping Document*, CERN, (2015), CERN-LHCC-2015-020. LHCC-G-166.

[72] H. Correia et al., *ATLAS Large eta task force report*, CERN, (2015), ATL-UPGRADE-INT-2015-001, (internal note).

[73] A. J. Barr et al., *Higgs Self-Coupling Measurements at a 100 TeV Hadron Collider*, JHEP **02** (2015) 016, 1412.7154.

[74] S. McMahon et al., *High Level Functional Requirements of the ITk: High Level Functional Requirements of the ITk*, CERN, (2015), ATL-COM-UPGRADE-2015-015, (internal draft).

[75] ATLAS Colaboration, *Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment*, CERN, (2013), ATL-COM-UPGRADE-2012-040, (draft version).

[76] S. McMahon et al., *Initial Design Report of the ITk*, CERN, (2014), ATL-COM-UPGRADE-2014-029, (internal draft).

[77] P. S. Miyagawa and I. Dawson, *Radiation background studies for the Phase II inner tracker upgrade*, CERN, (2013), ATL-UPGRADE-PUB-2013-012.

[78] M. A. Green, *Intrinsic concentration, effective densities of states, and effective mass in silicon*, J. Appl. Phys. **67** (1990) 2944.

[79] P. Weigell, Investigation of Properties of Novel Silicon Pixel Assemblies Employing Thin n-in-p Sensors and 3D-Integration, PhD thesis, Technische Universität München, (2013), MPP-2013-5.

[80] H. Bethe and J. Ashkin, *Passage of Radiations through Matter*, in *Experimental Nuclear Physics*, volume 1, p. 253, New York: Wiley, 1953-59.

[81] Particle Data Group, *Review of Particle Physics*, Chin. Phys. **C38** (2014) 090001.

[82] H. Bichsel, *Straggling in thin silicon detectors*, Rev. Mod. Phys. **60** (1988) 663.

[83] R. Sternheimer, M. Berger, and S. Seltzer, *Density effect for the ionization loss of charged particles in various substances*, Atomic Data and Nucl. Data Tab. **30** (1984) 261.

[84] S. Ramo, *Currents Induced by Electron Motion*, Proceedings of the IRE **27** (1939) 584.

[85] W. Shockley, *Currents to Conductors Induced by a Moving Point Charge*, Journal of Applied Physics **9** (1938) 635.

[86] J. Becker, Signal Development in Silicon Sensors Used for Radiation Detection, PhD thesis, University of Hamburg, (2010), DESY-THESIS-2010-033.

[87] C. Leroy and P.-G. Rancoita, *Silicon Solid State Devices and Radiation Detection*, World Scientific Publishing Co. Pte. Ltd., Singapore, (2012), ISBN 978-981-4390-04-0.

[88] J. Wüstenfeld, Characterization of Ionization-Induced Surface Effects for the Optimization of Silicon-Detectors for Particle Physics Applications, PhD thesis, TU Dortmund, (2001).

[89] V. A. J. van Lint et al., *Mechanisms of Radiation Effects in Electronic Materials*, John Wiley & Sons, (1980), ISBN 978-0471041061.

[90] J. R. Srour et al., *Review of Displacement Damage Effects in Silicon Devices*, IEEE Trans. Nucl. Sci. **50** (2003) 653.

[91] A. Vasilescu, *The NIEL scaling hypothesis applied to neutron spectra of irradiation facilities and in the ATLAS and CMS SCT*, CERN, (1999), ROSE RD-48 Technical Note, ROSE/TN/97-2.

[92] A. Vasilescu and G. Lindström, *Notes on the fluence normalisation based on the NIEL scaling hypothesis*, CERN, (2000), ROSE RD-48 Technical Note, ROSE/TN/2000-02.

[93] R. Wunstorf, Systematische Untersuchungen zur Strahlenresistenz von Silizium-Detektoren für die Verwendung in Hochenergiephysik-Experimenten, PhD thesis, Universität Hamburg, (1992).

[94] M. Moll, Radiation Damage in Silicon Particle Detectors, PhD thesis, Universität Hamburg, (1999).

[95] G. Kramberger et al., *Effective trapping time of electrons and holes in different silicon materials irradiated with neutrons, protons and pions*, Nucl. Instr. Meth. **A481** (2002) 297.

[96] R. H. Richter et al., *Strip detector design for ATLAS and HERA-B using two-dimensional device simulation*, Nucl. Instr. Meth. **A377** (1996) 412.

[97] M. Beimforde, Development of thin sensors and a novel interconnection technology for the upgrade of the atlas pixel system, PhD thesis, Technische Universität München, (2010), MPP-2010-115.

[98] R. Nisius et al., *R&D on a novel interconnection technology for 3D integration of sensors and electronics and on thin pixel sensors*, CERN Engeneering & Equipment Data Management Service (2007) 1, ATL-P-MN-0019.

[99] A. Macchiolo et al., *Development of thin pixel sensors and a novel interconnection technology for the SLHC*, Nucl. Instr. Meth. **A591** (2008) 229.

[100] ATLAS IBL Collaboration, *Prototype ATLAS IBL Modules using the FE-I4A Front-End Readout Chip*, JINST **7** (2012) P11010.

[101] G. Aad, Mise en service du détecteur à pixels de l'expérience ATLAS auprès du LHC et étude du canal $t\bar{t}H, H \to b\bar{b}$ pour la recherche du boson de Higgs, PhD thesis, Université de la Méditerranée Aix-Marseille II, (2009), CERN-THESIS-2010-015.

[102] R. Beccherle et al., *MCC: the Module Controller Chip for the ATLAS Pixel Detector*, Nucl. Instr. Meth. **A492** (2002) 117.

[103] I. Perić, Design and realisation of integrated circuits for the readout of pixel sensors in high-energy physics and biomedical imaging, PhD thesis, Universität Bonn, (2004), CERN-THESIS-2004-055.

[104] L. Blanquart et al., *FE-I2: a front-end readout chip designed in a commercial 0.25-μm process for the ATLAS pixel detector at LHC*, IEEE Trans. Nucl. Sci. **51** (2004) 1358.

[105] FE-I4 Collaboration, *The FE-I4A Integrated Circuit Guide*, 2011, Version 11.6 (unpublished).

[106] FE-I4 Collaboration, *The FE-I4B Integrated Circuit Guide*, 2012, Version 2.3 (unpublished).

[107] V. Zivkovic et al., *The FE-I4 pixel readout system-on-chip resubmission for the insertable B-Layer project*, JINST **7** (2011) C02050.

[108] C. Da Via et al., *3D active edge silicon sensors: Device processing, yield and QA for the ATLAS-IBL production*, Nucl. Instr. Meth. **A699** (2011) 18.

[109] G. Darbo, *Experience on 3D Silicon Sensors for ATLAS IBL*, JINST **10** (2015) C05001.

[110] G. Pellegrini et al., *3D double sided detector fabrication at IMB-CNM*, Nucl. Instr. Meth. **A699** (2013) 27.

[111] G. Giacomini et al., *Development of double-sided full-passing-column 3D sensors at FBK*, IEEE Trans. Nucl. Sci. **60-3** (2013) 2357.

[112] A. Klumpp et al., *Vertical System Integration by Using Inter-Chip Vias and Solid-Liquid Interdiffusion Bonding*, Jpn. J. Appl. Phys. **43** (2004) L829.

[113] L. Andricek et al., *Production and characterisation of SLID interconnected n-in-p pixel modules with* 75 μm *thin silicon sensors*, Nucl. Instr. Meth. **A758** (2014) 30.

[114] *Fraunhofer-Einrichtung für Modulare Festkörper-Technologien*, `http://www.emft.fraunhofer.de`.

[115] P. Garrou et al., *Handbook of 3D Integration*, Wiley-VCH, (2008).

[116] J. Große-Knetter et al., *USBpix - USB based readout system for ATLAS FE-I3 and FE-I4*, `http://icwiki.physik.uni-bonn.de/twiki/bin/view/Systems/UsbPix`.

[117] M. Backhaus, Development of an USB-based test system for the FE-I3 readout chips of the ATLAS pixel detector and Noise Occupancy Studies, Diploma thesis, Universität Bonn, (2009), BONN-IB-2009-14.

[118] *The Reconfigurable Cluster Element*, `http://www.slac.stanford.edu/exp/atlas/upgrade/tdaq/RCE-20100712.pdf`.

[119] D. Dobos, Production accompanying testing of the ATLAS Pixel module, Diploma thesis, TU Dortmund, (2004), CERN-THESIS-2007-016.

[120] K. Einsweiler, *ATLAS Pixel FE Chip: Description and Failure Summary*, LBNL, (2003), Draft 3, (unpublished).

[121] J. Große-Knetter, Vertex Measurement at a Hadron Collider – The ATLAS Pixel Detector, Habilitation thesis, Universität Bonn, (2008), BONN-IR-2008-04.

[122] M. Backhaus, *Characterization of new hybrid pixel module concepts for the ATLAS Insertable B-Layer upgrade*, JINST **7** (2012) C01050.

[123] M. Backhaus, *Characterization of the FE-I4B pixel readout chip production run for the ATLAS Insertable B-layer upgrade*, JINST **8** (2013) C03013.

[124] M.-M. Bé et al., *Table of Radionuclides*, volume 3 of *Monographie BIPM-5*, Bureau International des Poids et Mesures, Pavillon de Breteuil, F-92310 Sèvres, France, (2013), ISBN 978-92-822-2248-5.

[125] P. Shulek et al., *Fluctuations of Ionization Losses*, Soviet Journal of Nuclear Physics **4** (1967) 400.

[126] M.-M. Bé et al., *Table of Radionuclides*, volume 7 of *Monographie BIPM-5*, Bureau International des Poids et Mesures, Pavillon de Breteuil, F-92310 Sèvres, France, (2013), ISBN 978-92-822-2248-5.

[127] P. D. Autiero et al., *Characterization of the T24 electron beam line available at DESY*, (2004), OPERA internal note.

[128] G. Troska, Development and operation of a testbeam setup for qualification studies of ATLAS pixel sensors, PhD thesis, TU Dortmund, (2012).

[129] I. Rubinskiy, *An EUDET/AIDA Pixel Beam Telescope for Detector Development*, Phys. Proc. **37** (2012) 923.

[130] J. Behr, Jets at High Q^2 at HERA and Test Beam Measurements with EUDET Pixel Telescope, PhD thesis, Universität Hamburg, (2010), DESY-THESIS-2010-038.

[131] C. Hu-Guo, *A ten thousand frames per second readout MAPS for the EUDET beam telescope*, CERN, (2009), CERN-2009-008.

[132] A. Bulgheroni et al., *EUTelescope, the JRA1 tracking and reconstruction software: a status report*, (2008), EUDET-Memo-2008-48.

[133] *EUTelescope: A Generic Pixel Telescope Data Analysis Framework*, `http://eutelescope.web.cern.ch`.

[134] V. Blobel, *Software alignment for tracking detectors*, Nucl. Instr. Meth. **A566** (2006) 5.

[135] R. E. Kalman, *A New Approach to Linear Filtering and Prediction Problems*, Journal of Basic Engineering **82** (1960) 35.

[136] V. Blobel, *A new fast track-fit algorithm based on broken lines*, Nucl. Instr. Meth. **A566** (2006) 14.

[137] K. N. Sjøbæk, Full simulation of a testbeam experiment including modeling of the Bonn ATLAS Telescope and ATLAS 3D pixel silicon sensors, Master thesis, University of Oslo, Department of Physics, (2010).

[138] R. Turchetta, *Spatial resolution of silicon microstrip detectors*, Nucl. Instr. Meth. **A335** (1993) 44.

[139] E. Belau et al., *Charge collection in silicon strip detectors*, Nucl. Instr. Meth. **214** (1983) 253.

[140] J. Weingarten et al., *Planar Pixel Sensors for the ATLAS Upgrade: Beam Tests results*, JINST **7** (2012) P10028.

[141] M. Paterno, *Calculating Efficiencies and Their Uncertainties*, Fermilab, (2004), FERMILAB-TM-2286-CD.

[142] V. L. Highland, *Some practical remarks on multiple scattering*, Nucl. Instr. Meth. **129** (1975) 497.

[143] G. R. Lynch and O. I. Dahl, *Approximations to multiple Coulomb scattering*, Nucl. Instr. Meth. **B58** (1991) 6.

[144] M. Benoit, Étude des détecteurs planaires pixels durcis aux radiations pour la mise à jour du d'etecteur de vertex d'ATLAS, PhD thesis, Université Paris Sud - Paris XI, (2011), LAL-11-118.

[145] E. Fehlberg, *Low-order classical runge-kutta formulas with stepsize control and their application to some heat transfer problems*, NASA Technical Report (1969) R315.

[146] M. Borri, Characterization of 3D Silicon Assemblies for ATLAS Pixel Upgrade, PhD thesis, University of Manchester, (2013).

[147] L. Snoj, G. Žerovnik, and A. Trkov, *Computational analysis of irradiation facilities at the JSI TRIGA reactor*, Appl. Rad. Iso. **70** (2012) 483.

[148] I. Mandić et al., *Bulk Damage in DMILL npn Bipolar Transistors Caused by Thermal Neutrons Versus Protons and Fast Neutrons*, IEEE Trans. Nucl. Sci. **51** (2004) 1752.

[149] A. Dierlamm, Untersuchungen zur Strahlenhärte von Siliziumsensoren, PhD thesis, Universität Karlsruhe, (2003), IEKP-KA/2003-23.

[150] A. Furgeri, Qualitätskontrolle und Bestrahlungsstudien an CMS Siliziumstreifensensoren, PhD thesis, Universität Karlsruhe, (2006), IEKP-KA/2005-1.

[151] P. Lisowski et al., *Los Alamos National Laboratory spallation neutron sources*, Nucl. Sci. and Eng. **106** (1990) 208.

[152] B. Paschen, Investigation of the Performance of Pixel Modules from thin Silicon Sensors with active Edges, Master thesis, Ludwig-Maximilian-Universität München and Max-Planck-Institut für Physik, (2014), MPP-2014-557.

[153] A. Macchiolo et al., *Thin n-in-p pixel sensors and the SLID-ICV vertical integration technology for the ATLAS upgrade at the HL-LHC*, Nucl. Instr. Meth. **A731** (2013) 210.

[154] A. Macchiolo et al., *Development of active edge pixel sensors and four-side buttable modules using vertical integration technologies*, Nucl. Instr. Meth. **A765** (2014) 53.

[155] S. Terzo et al., *Heavily Irradiated N-in-p Thin Planar Pixel Sensors with and without Active Edges*, JINST **9** (2014) C05023.

[156] S. Terzo et al., *Thin n-in-p planar pixel sensors and active edge sensors for the ATLAS upgrade at HL-LHC*, JINST **9** (2014) C12029.

[157] L. Andricek et al., *Processing of Ultra-Thin Silicon Sensors for Future e^+e^- Linear Collider Experiments*, IEEE Trans. Nucl. Sci. **51** (2004) 1117.

[158] A. Nenadic and R. W. Pasco, *Method of chemical-mechanical polishing an electronic component substrate and polishing slurry therefor*, US Patent 5084071, (1992).

[159] S. Eränen et al., *3D processing on 6 in. high resistive SOI wafers: Fabrication of edgeless strip and pixel detectors*, Nucl. Instr. Meth. **A607** (2009) 85.

[160] F. Lärmer, *Verfahren zum anisotropen Ätzen von Silizium*, DE Patent 4241045 C1, (1994).

[161] G. Kramberger et al., *Investigation of electric field and evidence of charge multiplication by Edge-TCT*, IEEE Nucl. Sci. Symp. Conf. Rec. (2009) 1740.

[162] C. Betancourt et al., *A charge collection study with dedicated RD50 charge multiplication sensors*, Nucl. Instr. Meth. **A730** (2014) 62.

[163] J. Lange, Differential Top-Quark-Pair Cross Sections in pp Collisions at $\sqrt{s} = 7\,\text{TeV}$ with CMS and Charge Multiplication in Highly-Irradiated Silicon Sensors, PhD thesis, University of Hamburg, (2013).

[164] L. Zwalinski et al., *CO_2 cooling system for Insertable B Layer detector into the ATLAS experiment*, PoS **TIPP2014** (2015) 224.

[165] Y. Varshni, *Temperature dependence of the energy gap in semiconductors*, Physica **34** (1967) 149.

[166] J. Singh, *Physics of Semiconductors and Their Heterostructures*, Electrical engineering series, McGraw-Hill, (1993), ISBN 9780071128353.

[167] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*, Wiley-Interscience, 3rd edition, (2007), ISBN 0-47114323-5.

[168] A. Francescon et al., *Application of micro-channel cooling to the local thermal management of detectors electronics for particle physics*, Microelectronics Journal **44** (2013) 612.

[169] L. Gonella, Low mass hybrid pixel detectors for the high luminosity LHC upgrade, PhD thesis, Universität Bonn, (2013).

[170] T. Tick and M. Campbell, *TSV processing of Medipix3 wafers by CEA-LETI: A progress report*, JINST **6** (2011) C11018.

[171] A. Klumpp, P. Ramm, and R. Wieland, *3D-integration of silicon devices: A key technology for sophisticated products*, in *Design, Automation Test in Europe Conference Exhibition*, pp. 1678–1683, 2010.

Acknowledgements