Power Efficiency in Communication Systems from a Circuit Perspective

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***Abstract*— We consider the minimization of the overall power consumption when communicating over a noisy *single-input single-output* channel while satisfying a certain throughput and error rate constraint. The total power dissipation includes the radiated power as well as the circuit power consumption. In the context of battery operated short range communication, where low power, low cost and small size are key requirements (e.g. standard IEEE 802.15.4), this circuit aware system optimization is crucial given the growing importance of "*Green Communication*". In fact, the power dissipation of certain analog and digital components along the signal path reaches values in the order of or is even higher than the transmit power in such applications. Using an appropriate information-theoretic framework we derive the optimal bit-resolution of the analog-to-digital converter (ADC), the optimal choice of the noise figure for the low noise amplifier (LNA), the optimal operating input back-off (IBO) of the power amplifier (PA), as well as the optimum decoding (DEC) strategy as a function of the path-loss (i.e. the communication distance), that guarantee a certain net data rate R under a certain error probability P_e. This work is an extension to the work [1], where only the power of the analog components was considered.**

I. Introduction

In his famous work [2], Shannon showed that the maximal achievable rate of an AWGN channel with given transmit power P_T and bandwidth B is given by

$$R = B\log_2(1+\mathrm{SNR}) = B\log_2\left(1+\frac{G_c\cdot P_T}{N_0\cdot B}\right), \quad (1)$$

where G_c is the radio path-gain (even though $G_c \leq 1$) and N_0 is the one-sided noise spectral level (in Joule). The classical measure for power efficiency in communications takes only the radiated energy per bit $E_b = P_T/R$ into account. Since the rate function is monotonically increasing with the bandwidth B, the minimum transmit signal energy per information bit is obtained by taking the bandwidth to infinity

$$\left[\frac{E_b}{N_0}\right]_{\min} = \lim_{B\to\infty}\frac{P_T}{N_0\cdot R} = \frac{\ln 2}{G_c}. \quad (2)$$

Obviously, since there is no penalty from taking the bandwidth to infinity, the maximum power-efficiency is obtained at infinite bandwidth. Besides, it is assumed that the receiver has access to the channel data with infinite precision. This classical information theoretic approach is motivated by long range communication and thus neglects the conversion and processing power. However, when communicating over smaller distances using energy-constrained devices (e.g. sensor networks or wireless medical implants), the transmit power can be comparable to the analog/digital processing power. Thus, the power consumption of certain analog and digital components can have a strong impact on the total power consumption. In this paper we aim to jointly minimize the power consumption of certain transceiver components, in addition to the radiated power. This is motivated by the fact that the transceiver chip transmits and receives almost at the same data rate. The problem of jointly minimizing the transmission and the electronic processing power has been considered in [3], [4] among others. A common assumption is that the power consumption of the circuit components is a constant quantity. The best strategy in that case is to employ bursty transmission with an optimized duty cycle. Nevertheless, the power consumptions of the circuit components are generally mutually coupled with other system parameters (bandwidth, modulation scheme, input back-off, noise power, bit resolution, decoding strategy...) which in turn directly affect the achievable throughput. Therefore, we carefully model the system components in order to get well founded results. The components involved in our power minimization framework are the power amplifier (PA), the low noise amplifier (LNA), the analog-to-digital converter (ADC) and the decoder (DEC). The channel encoding is usually much less complex than decoding and thus we neglect its power dissipation.

II. Framework description

We first present briefly the results of our literature search on communication circuits and their modeling [5], [6], [7].

A. Power consumption of the Power Amplifier (PA)

The power consumption of the power amplifier is denoted by P_{PA} and already includes the radiated power P_T. They are in fact related by

$$P_T = \bar{\eta}P_{\mathrm{PA}}, \quad (3)$$

where $\bar{\eta} \leq 1$ is the average power efficiency of the amplifier. The instantaneous power efficiency η usually depends on the ratio of the instantaneous amplitude of the RF sinusoid a_x to the maximum output voltage A. Based on a simplified push-pull amplifier model and depending on the operating mode, i.e., the case when the amplifier operates on its linear region or when it is overdriven into saturation, we get [1]

$$\eta = \begin{cases} \frac{\pi}{4}\frac{a_x}{A} & \text{for } a_x < A \\ \frac{\sqrt{1-(\frac{A}{a_x})^2}+\frac{a_x}{A}\arcsin\frac{A}{a_x}}{2} & \text{for } a_x \geq A. \end{cases}$$

For a complex Gaussian input alphabet with variance σ_x^2 the amplitude a_x is Rayleigh distributed, and we obtain the average PA efficiency

$$\begin{aligned}\bar{\eta} &= \int_0^\infty \eta(a_x) f_{a_x}(a_x) da_x \\ &= \frac{1}{8}\pi^{3/2}\frac{1}{z}\mathrm{erf}(z) + \frac{(4-\pi)(\exp(-z^2)+\mathrm{Ei}(-z^2)z^2)}{4},\end{aligned}$$

where $z = \frac{A}{\sigma_x}$ represents the Input back-off (IBO) of the power amplifier and $\mathrm{Ei}(u) = \int_{-\infty}^{u} \mathrm{e}^t/t\cdot \mathrm{d}t$ denotes the exponential integral. Obviously, there is a trade-off between power efficiency and the signal distortion due to clipping. To quantify the distortion effects we decompose the output

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of the amplifier y into a desired signal component and an uncorrelated distortion n_{PA} using the Bussgang theorem

$$y = \alpha \cdot x + n_{\mathrm{PA}}. \quad (4)$$

Assuming a soft-limiter type of nonlinearity and an IBO z, α and the variance of n_{PA} take the values

$$\alpha = 1 - \mathrm{e}^{-z^2} + \frac{\sqrt{\pi} z}{2} \mathrm{erfc}(z), \quad (5)$$

$$\sigma_{n_{\mathrm{PA}}}^2 = (1 - \mathrm{e}^{-z^2} - \alpha^2)\sigma_x^2. \quad (6)$$

B. Power consumption of the low noise amplifier (LNA)

Although, there are many performance factors in LNAs, we concentrate on four important parameters such as power gain, bandwidth, noise figure and power dissipation. These are included in a figure-of-merit expression $\mathrm{FOM}_{\mathrm{LNA}}$ [8]

$$\mathrm{FOM}_{\mathrm{LNA}} = \frac{G_{\mathrm{LNA}} \cdot B \cdot N_0}{(N_F - 1) \cdot P_{\mathrm{LNA}}}, \quad (7)$$

where G_{LNA} is the power gain, N_F is the noise figure, P_{LNA} is the power consumption and B is the operating bandwidth. Note that we multiplied the figure-of-merit definition in [8] by N_0, just to make it dimensionless. A noise figure of value N_F means that the LNA enhances the thermal noise level N_0 by the factor N_F. It turns out that for "good" designed LNAs the $\mathrm{FOM}_{\mathrm{LNA}}$ can be considered as an invariant quantity that only depends on the process technology and certain transistor parameters, and thus can not be influenced by our system optimization. Recent LNA designs found in the literature exhibit an $\mathrm{FOM}_{\mathrm{LNA}}$ in the range of 10^{-7} to 10^{-9}. The gain G_{LNA} is not subject of the optimization and is set to 10, so that the effect of noise from subsequent stages can be neglected.

C. Power consumption of the A/D Converter (ADC)

The ADC complexity grows with the resolution b and the bandwidth B and it heavily affects the complexity of the following digital signal processing, e.g. the required memory size. In fact, it has been observed that new ADC architectures like pipelined ADCs are thermal noise limited and thus their minimum possible power is proportional to $N_0 \cdot 2^{2b} \cdot f_s$, where f_s is the sampling frequency [6]. In other words, under Nyquist rate sampling, the power needed for converting a complex signal with bandwidth B can be modeled as (see [6] for further motivation):

$$P_{\mathrm{ADC}} = 2 \cdot c_{\mathrm{ADC}} \cdot N_0 \cdot 2^{2b} \cdot B, \quad (8)$$

with some proportionality constant c_{ADC} depending on the ADC architecture. Although (8) is still not representative for the broad amount of actual ADC designs (especially at low resolution), it can be seen as the fundamental limit on conversion power due to thermal noise. Eq. (8) results in a trade-off between power consumption and performance loss due to quantization. It is therefore of interest to design the system parameters like bandwidth and ADC resolution in order to minimize the total power consumption including the conversion power.

D. Power consumption of the channel decoder (DEC)

Let us consider for instance low density parity check (LDPC) codes which are emerging in many new applications and standards. A regular binary (N, λ, ρ) LDPC block code [9] is described by an $N \times K$ parity check matrix. N is the number of variable nodes (i.e. the block length), K is the number of check nodes, whereas λ is the number of edges connected to each variable nodes (i.e. the number of ones in each column) and ρ is the number of edges connected to each check nodes (i.e. the number of ones in each row). Hence, the number of useful information bits is $N - K$ and the LDPC code rate is given by

$$r_{\mathrm{COD}} = 1 - \frac{K}{N} = 1 - \frac{\lambda}{\rho}. \quad (9)$$

Each iteration of the decoding algorithm, well-known as belief propagation, consists in, first sending messages from each variable node to each adjacent check node, and then vice versa. The messages contain the extrinsic information of each information bits in form of density functions computed based on the previously received messages. Let us assume the energy consumed by computing and exchanging messages over one edge at each iteration, E_{edge}, to be a constant parameter, then the total energy consumption of decoding one block with ℓ iterations is roughly

$$E_{\mathrm{DEC}} = E_{\mathrm{edge}} \cdot \lambda \cdot N \cdot \ell. \quad (10)$$

Typical values for E_{edge} extracted from the literature are in the range $10^7 \cdot N_0$ to $10^8 \cdot N_0$ (when taking $N_0 = k_B \cdot T$). Please refer to [7] and the references therein for more precise energy modeling of LDPC decoders. Now, under a certain target information rate R (in bits/sec) the power consumption of the decoder can be obtained as

$$P_{\mathrm{DEC}} = \frac{E_{\mathrm{DEC}}}{N-K} R = E_{\mathrm{edge}} \cdot \lambda \cdot \frac{1}{r_{\mathrm{COD}}} \cdot \ell \cdot R. \quad (11)$$

Since the $r_{\mathrm{COD}} < 1$ and the overall code rate (or bandwidth efficiency in bits/channel use) is obtained from the combination of the modulation order $L \geq 2$ (any modulation alphabet includes at least 2 symbols) and the channel code rate as

$$r = \frac{R}{B} = r_{\mathrm{COD}} \log_2 L, \quad (12)$$

we get $r_{\mathrm{COD}} < \min\{1, r\}$, and we can deduce a lower bound on the decoding power consumption as function of the target rate and the bandwidth

$$P_{\mathrm{DEC}} = E_{\mathrm{edge}} \cdot \lambda \cdot \max\{R, B\} \cdot \ell. \quad (13)$$

In many applications, besides of the target rate, a certain maximum error probability P_e is specified. Therefore we need to evaluate the performance of the LDPC code in terms of achievable error rate. In [10], it has been shown that the error probability for regular LDPC codes under iterative decoding can decrease double-exponentially with the iteration index ℓ as long as $\ell < \frac{\log(N)}{\log(\lambda-1)\log(\rho-1)}$, that is

$$P_e \approx 2^{-E_r(\lambda-1)^{\ell}}, \quad (14)$$

for a certain constant error exponent E_r, which is difficult to be determined in general. Motivated by the simple characterization of the error exponent for random codes [11], we approximate E_r by the difference between the theoretic achievable rate r_0 (or channel capacity), which will be discussed next, and the actual overall code rate $r = R/B$ (both in bits/channel use), i.e., $E_r = r_0 - r$. All in all, the decoding power as function of the system specifications is

$$P_{\mathrm{DEC}} = \lambda E_{\mathrm{edge}} \max(R, B) \log_{\lambda-1}\!\left(\frac{-\log_2 P_e}{r_0 - R/B}\right). \quad (15)$$

E. Achievable Rate

Taking into account the distortion noise caused by the power amplifier and the noise figure of the LNA, we obtain the effective SNR as

$$\mathrm{SNR} = \frac{G_c \cdot \alpha^2 \cdot \sigma_x^2}{G_c \cdot \sigma_{n_{\mathrm{PA}}}^2 + N_F \cdot N_0 \cdot B}. \quad (16)$$

In [12], a lower bound on the achievable channel capacity under output quantization by means of an MMSE approach has been derived, as follows

$$r_0 \geq \log_2 \left(\frac{1 + \mathrm{SNR}}{1 + \mathrm{SNR}/\mathrm{SQR}} \right), \quad (17)$$

where SQR is the signal-to-distortion ratio related to the ADC resolution b. This bound is tight at low SNR and its derivation does not assume uncorrelated additive quantization noise. In order to maximize SQR, an AGC-circuit is placed before the ADCs, which scales the noisy inphase and quadrature signals by a factor such that the ADCs are driven with an optimal input power. In this case, $\mathrm{SQR} \propto 2^{2b}$ and we can approximate the channel capacity under finite resolution b as

$$r_0 \approx \log_2 \left(\frac{1 + \mathrm{SNR}}{1 + \mathrm{SNR} \cdot 2^{-2b}} \right), \quad (18)$$

which is consistent with the fact, that the achievable rate per channel use with infinite P_T is $2b$. The ADC resolution is commonly chosen such that the ADC distortion noise is about 10dB below the overall noise level. However, such an approach is inappropriate for designing low power systems.

III. Total Power Minimization

Using the above energy consumption models, we aim to jointly minimize the transmission and the analog processing power consumption with respect to the different system parameters (resolution, bandwidth, noise figure, input back-off). The considered setting is free of a bandwidth constraint, which is quasi-true in UWB, but the optimization can be easily modified to include a bandwidth limitation. We also determine the fractions of power that should be optimally allocated to each of the components (PA, LNA, ADC, DEC). Let us consider the total power spent in the transmission,

$$P_{\mathrm{total}} = P_{\mathrm{PA}} + P_{\mathrm{ADC}} + P_{\mathrm{LNA}} + P_{\mathrm{DEC}}, \quad (19)$$

We aim to minimize the total power consumed for a given target rate R and error probability P_e, with respect to the operating bandwidth B (assumed to be unconstrained), the IBO z of the PA, the noise figure N_F of the LNA, the resolution b of the ADC and the number of decoding iterations ℓ. Evidently, the parameter λ of the LDPC code can be also optimized but it is considered to be fixed here. Using numerical optimization methods, the global optimizer of this function is easily found, since only a relatively small number of parameters are involved.

IV. Numerical Results

As an example, let us take $c_{\mathrm{ADC}} = 10^5$, which is a typical value of recent comparator-based ADCs [6], $\mathrm{FOM}_{\mathrm{LNA}} = 10^{-7}$ [8], while the decoder is specified by $\lambda = 6$, $E_{\mathrm{edge}} = 10^7 \cdot N_0$ and a target error probability $P_e = 10^{-14}$. First of all, the normalized combined energy per bit required to communicate across the noisy channel is depicted in Fig. 1. The term $\frac{P_{\mathrm{total}}}{N_0 R_{\max}}$ corresponds to the minimal energy per bit.

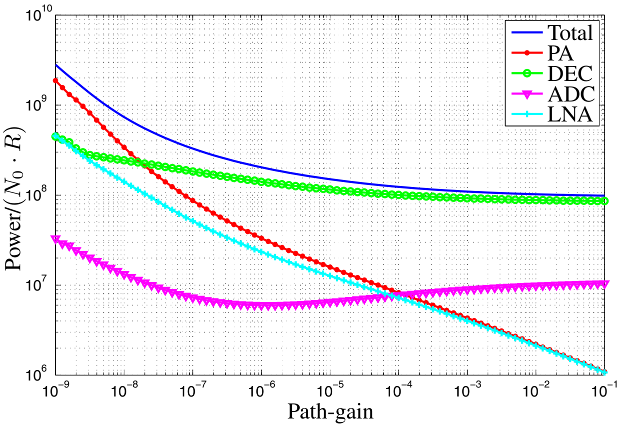

Fig. 1. Normalized energies per bit vs. the path-gain.

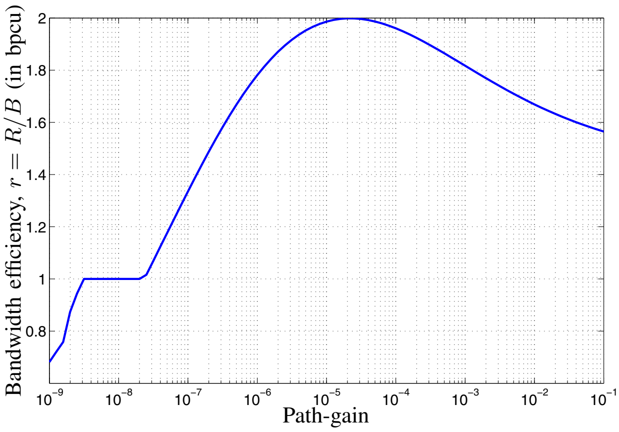

Fig. 2. Optimal bandwidth efficiency vs. the path-gain.

The fractions of energy per bit needed by each component are also illustrated. Remarkably, even at a very small path-loss, the required total energy per bit is quite large due to the decoding power consumption. Observe that, only for very small G_c (long range communication), the transmission power is dominant, in accordance to the classical approach, while for high G_c (short range communication), the decoding power becomes dominant. As already mentioned, for large G_c, the ADC power becomes significant compared to the transmit power but remains smaller than the decoding power. On the other hand, the fraction of power that should be dedicated to the LNA remains insignificant even for high path-gains. All in all, at very short communication distances, the decoding power is dominant.

The behavior of the bandwidth efficiency (net bit rate R divided by the bandwidth B) versus the path-gain is shown in Fig. 2. Obviously, even if the system is free of a bandwidth constraint, there is no advantage from taking the bandwidth to infinity contrary to the result stated by the Shannon theory. Interestingly, the optimal operating bandwidth efficiency in the medium and high path-gain range takes values between 1 and 2 bits per channel use (bpcu), which are quite common in the practice.

Fig. 3 shows the optimal operating IBO of the power amplifier. At short distances, it is advantageous to operate the PA at high IBO values, i.e., at low drain efficiency, in order to reduce the distortion effects, due to the negligible PA power dissipation. On the other hand, Fig. 4 shows, that the optimal

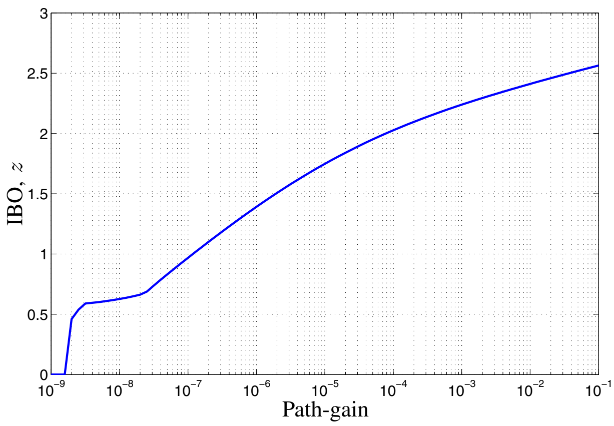

Fig. 3. Optimal operating IBO vs. the path-gain.

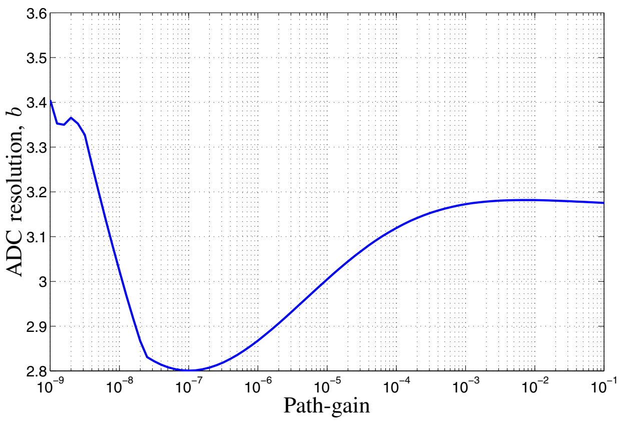

Fig. 4. Optimal ADC resolution vs. the path-gain.

resolution for short range communication is indeed quite low and is about 3 bit. This suggests, that low resolution ADCs may be a good choice for low power short range communication. The optimal choice of the noise figure for the LNA is shown in Fig. 5. Clearly, there is no advantage from putting a lot of effort to reduce the noise figure at a high channel gain, i.e., at short communication distances, since this would require much higher LNA power relatively to the transmission power. Fig. 6 illustrates the optimal number of decoding iterations. As expected, this number should be decreased with increasing path-gain in order to reduce the power dissipation mainly due to the decoder.

V. Conclusion

We have presented a circuit-aware design framework for energy efficient communication systems that takes into account the characteristics and the power consumptions of the PA, LNA, ADC, DEC. In the context of short range communication, we showed that, the channel decoder dominates the total power consumption under the state-of-the-art technology. On the other hand, low-resolution sampling exhibits a good performance, while reducing the total power consumption. It is also beneficial to design LNAs with poor noise figure in terms of overall power consumption. Besides, the well-known trade-off between bandwidth efficiency and power efficiency becomes less effective and maybe inexistent in medium to short communication distances. We believe that these results also hold for more general channel settings, e.g. MIMO channels.

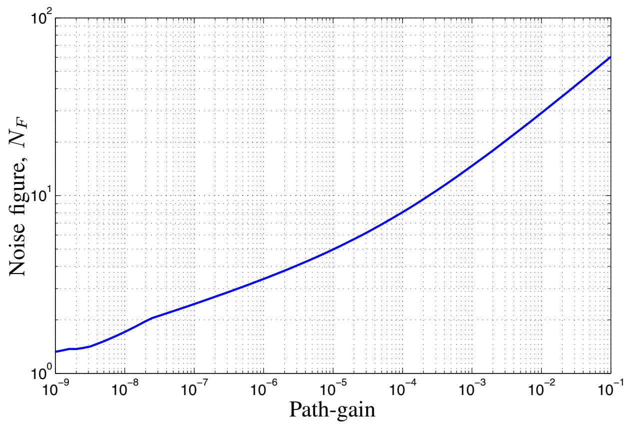

Fig. 5. Optimal noise figure vs. the path-gain.

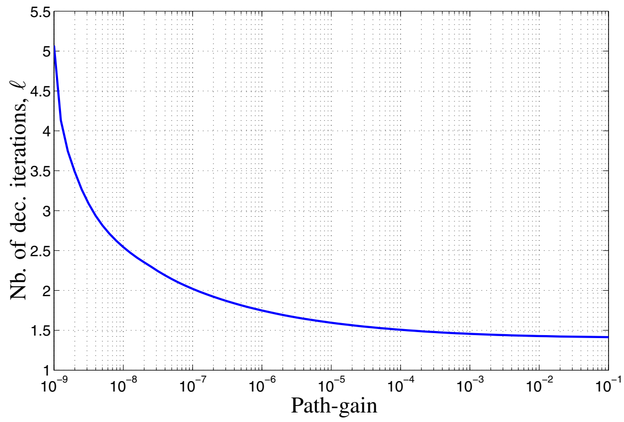

Fig. 6. Optimal number of dec. iterations vs. the path-gain.

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