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SEMICONDUCTOR NANOWIRES AND THEIR FIELD-EFFECT DEVICES

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Thesis summary

Semiconductor nanowires have attracted significant attention in the last decade for their potential in improving existing or enabling novel devices. An important challenge in the field is to reproducibly control the electronic properties and to fabricate high purity nanowires.

The goal of this thesis is to apply nanowires for the realization of field effect transistors and sensors, whose performance proves all the benefits of having high quality nanoscale materials. The nanowires used in this thesis are synthesized in our group and are mainly gallium arsenide (GaAs) nanowires grown by Molecular Beam Epitaxy (MBE) and germanium (Ge) nanowires grown by Chemical Vapor Deposition (CVD). Special in these nanowires is that they are synthesized by avoiding the use of gold in the nucleation and growth process, which should lead into higher purity and improved overall properties. The study is mainly realized by electrical measurements and by electronic microscopy in smaller part. In a first phase the nanowires are contacted in a 2-points configuration by means of optical lithography. In the following part, more complex methods, like Electron Beam Lithography (EBL), are applied in order to place the multiple contacts on the single nanowire. EBL technique enabled 4-point transport measurements which allowed accurate determination of the nanowire resistance and contact resistance. Even more than this, mentioned techniques allowed to understand what the effect of smaller size contact is and to realize devices in the size of few hundred nanometers. Additionally, we were able to realize more complex device geometries, for example by providing different gate configurations.

We investigated different semiconductor materials (GaAs, Ge and Si), designed and realized multiple geometry field-effect transistors and sensors based upon them and characterized their properties, particularly regarding possible applications in future electronic devices architectures. Special attention was paid to ensure reliable and reproducible results.

Zusammenfassung

Halbleiter-Nanodrähten wurde in den vergangenen zehn Jahren aufgrund ihres Potenzials, bestehende Bauelemente zu verbessern oder die Entwicklung neuartiger Bauelemente zu ermöglichen, erhebliche Aufmerksamkeit zuteil. In diesem Bereich stellt die Reproduzierbarkeit der elektronischen Eigenschaften sowie die Herstellung hoch-reiner Nanodrähte eine bedeutende Herausforderung dar.

Das Ziel dieser Arbeit ist, Nanodrähten bei der Realisierung von Feldeffekt-Transistoren und Sensoren einzusetzen, um die Vorzüge der Verwendung von qualitativ hochwertigen Nano-Materialen zu belegen. Die in dieser Arbeit verwendeten Nanodrähte werden in unserer Gruppe hergestellt und sind hauptsächlich GaAs Drähte, die mit Molekularstrahl-Epitaxie (Molecular Beam Epitaxy MBE) gewachsen wurden, und Ge Drähte die mit Gasphasenbeschichtung (Chemical Vapor Deposition CVD) gewachsen wurden. Die Besonderheit dieser Nanodrähte ist, dass während des Nukleations-Prozesses und des Wachstums der Drähte auf den Einsatz von Gold verzichtet wird, was zu einem erhöhten Reinheitsgrad und allgemein verbesserten Eigenschaften führen sollte. Die Studie wurde hauptsächlich anhand von elektronischen Messungen und teilweise mit Elektronenmikroskopie durchgeführt. In einem ersten Schritt wurden die Nanodrähte mithilfe von optischer Lithographie in einer Zwei-Punkt-Konfiguration kontaktiert. Anschließend wurden aufwendigere Methoden wie Elektronenstrahl -Lithographie (Electron Beam Lithography EBL) eingesetzt, um die Anordnung von Mehrfachkontakten auf einem einzelnen Nanodraht zu ermöglichen. Diese Technik ermöglichte 4-Punkt Messungen und somit eine präzise Bestimmung des elektrischen Widerstands eines Nanodrahts und des Kontaktwiderstands. Darüber hinaus konnte durch diese Techniken der Einfluss einer verringerten Größe der elektrischen Kontakte untersucht und Bauelemente in der Größenordnung von einigen hundert Nanometern hergestellt werden. Außerdem wurde die Umsetzung von komplexeren Geometrien, beispielsweise durch unterschiedliche Gate-Anordnungen, erreicht.

Verschiedene Halbleitermaterialeien (GaAs, Ge und Si) wurden untersucht und Feldeffekttransistoren mit unterschiedlichen Geometrien und darauf aufbauende Sensoren wurden entworfen, realisiert und hinsichtlich ihrer Eigenschaft en untersucht, besonders im Hinblick auf Anwendungsmöglichkeiten in zukünftigen Geräte-Architekturen. Besonderes Gewicht wurde auf die Verlässlichkeit und Reproduzierbarkeit der Ergebnisse gelegt.

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1. Basic concepts

1.1. Introduction

From a historical point of view, the semiconductor technology started to develop in the second half of the 19th century. Yet, first important step forward happened later, in 1947 when first transistor was realized. Today's life and modern civilization are virtually impossible to imagine without devices based on transistors or, in general, semiconductor technology. Personal computers, different types of memories and telecommunication hardware are only few of semiconductor technology products that we take for grant, as if they always existed. This fact is already enough to see how significant influence the semiconductors have and to know why do we want to investigate them.

The areas of nanoscience and nanotechnology have been experiencing an exponential growth and have gained an extreme importance with the beginning of the 21st century. In the same frame, semiconductor nanowires have attracted significant attention in the last decade for their potential in the improving existing or enabling novel devices. An important challenge in the field is to reproducibly control the electronic properties and to fabricate high purity nanowires. The goal of this thesis is to apply such nanostructures for the realization of the transistors and sensors, whose performance proves all the benefits of having high quality nanoscale materials.

Nanowires are becoming more and more interesting for future nanoscale devicesbecause of their properties, which can be improved with respect to bulk materials or even completely change[1-10]. This enables development of new devices, or, equally important, realization of existing devices with different concepts.

Nanowires are usually synthesized by the Vapor-Liquid-Solid (VLS) method in which gold nanocrystals are used for the nucleation and growth of the nanowires. An issue of major importance is to find a way to avoid the use of gold as there is a risk that gold will incorporate in material structure. It has been shown that this degrades the properties of semiconductor.[11,12] In this respect, different groups have been looking for alternative metals as catalyst.[13-15] Another solution would be growing nanowires without catalyst. As it was already reported, our group has obtained the growth of catalyst-free GaAs nanowires.[16,17] These nanowires are grown with Molecular Beam Epitaxy (MBE) technique. MBE allows not only extremely high purity, but also incorporation of different materials in the nanowire.

In order to use nanowires as building blocks for electronic and/or optoelectronic devices, controlled doping should be achieved. Silicon is an interesting material for doping GaAs because it has an amphoteric behavior: it can be either a p or n dopant. Whether Si acts as p or n dopant, finally depends on whether it is incorporated in As or Ga sites in the crystal structure. This process may be controlled during the growth by switching growth parameters, like temperature or Ga-As ratio. Different amount of Si results in different degree of doping in nanowires. Therefore, we should be able to produce wires a wide range of doping, from nominally undoped to highly doped.

Another interesting system are Ge nanowires. These nanowires are grown by Chemical Vapor Deposition (CVD). Germanium is important material because of better electronic properties compared to Si which is basic building element of today's semiconductor industry. Basically, germanium has a smaller effective mass - which leads to larger mobility - and the bandgap lies close to optical communication wavelengths. In our case, germanium nanowires are grown by Chemical Vapor Deposition, nominally without dopants. Again, here we avoid the use of gold as a catalyst.[18] We have obtained the synthesis of germanium nanowires by using indium and bismuth as catalysts. In this case, if indium or bismuth were to be incorporated in the nanowire core, the result would be a background doping. We seek for experiments which will prove if there is residual doping from catalyst material and compare the electronic properties of such nanowires with the ones obtained with gold as a catalyst.

In this thesis, I explore possibilities of using different nanowires as building elements for electronic devices. In order to do this, electrical properties of the above mentioned nanowires are investigated. After examining the electronic properties of the different nanowires, various transistor configurations will be examined for optimization of the device functioning.

1.2. Statement of the problem and the previous work

We will start this part by introducing few important definitions and parameters of the operation of a transistor. The transistor itself is an active electronic component having three terminals. In this work we are focused only on the so–called Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). The three terminals of MOSFET are source (S), drain (D) and gate (G), as depicted in Figure 1.6. The fourth electrode on Figure 1.6, body (B), is added to improve operational parameters and it is not necessary for a standard operation, i.e. the school model of transistor always contains only 3 electrodes. The gate electrode makes the transistor an active component, i.e. voltage applied on gate changes conductivity of transistor's channel. In order to make transistor working, we must bring it in so-called active mode. This is done by two power sources. The first power source is connected between the drain and the source electrode and corresponding applied voltage is called drain to source voltage, V_{DS}. The second power source is connected between the gate and

the source electrode, while the corresponding voltage is called gate to source voltage, V_{GS}. V_{DS} determines how the transistor will behave, like a voltage tunable resistor or like a current source. V_{GS} determines resistance in first case, or magnitude of current in second case.

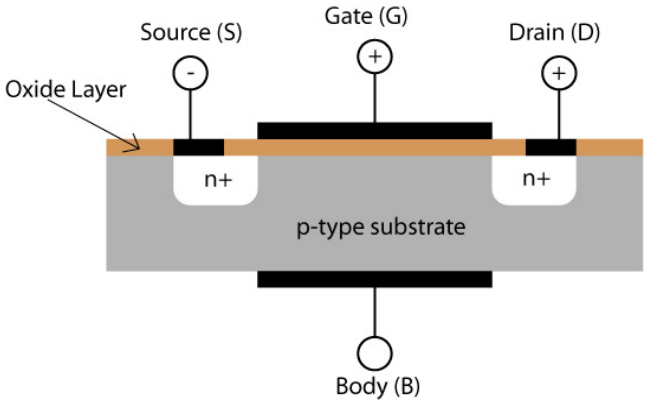


Figure 1.1. Schematic drawing of the MOSFET

The MOSFET modes of operation are depicted in Figure 1.2. As it can be seen, there are three regions of operation. Cutoff mode is characterized by $V_g = 0$ (or smaller than certain threshold, V_{th}). Under these conditions, transistor is in stand-by mode. If used as an electronic switch, described conditions correspond to OFF-state.

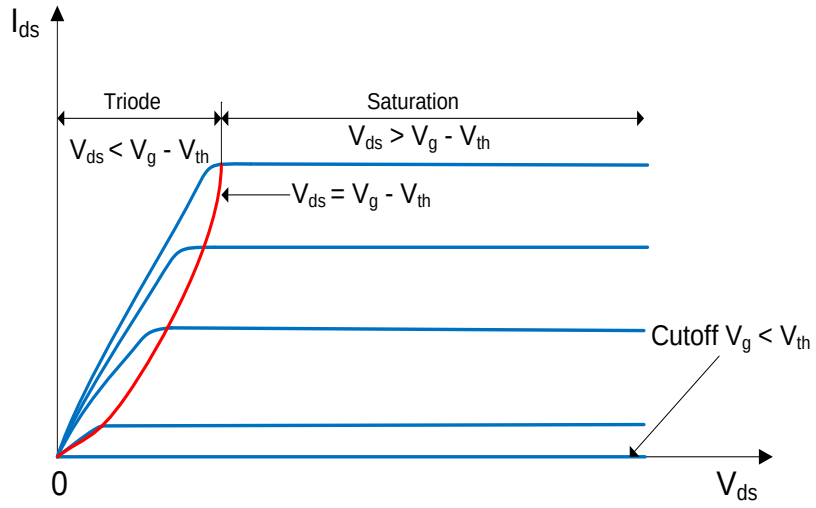


Figure 1.2. MOSFET I_{ds}-V_{ds} characteristics

Triode mode is achieved for $V_{ds} < V_g - V_{th}$. In the ideal transistor approximation, this mode of operation can be compared to voltage controllable resistor. Assuming V_{ds} small enough, drain source current can be given by:[19]

$$I_{ds} = k \frac{W}{L} (V_g - V_{th}) V_{ds} = r_{ds}^{-1} V_{ds} \qquad (1.1)$$

In equation (1.1), W and L stand for channel width and length, respectively, while k stands for process transconductance parameter. It can be defined as $k = \mu \frac{\varepsilon_{ox}}{T_{ox}}$ where μ, ε_{ox} and T_{ox} stand for mobility, oxide dielectric constant and oxide thickness, respectively.[20] r_{ds} is defined as the resistance between the drain and the source terminals. As it has already been pointed out, value of r_{ds} is controlled by gate-source voltage, V_g.

Saturation mode of operation is characterized by $V_{ds} > V_g - V_{th}$. In the ideal transistor approximation, this mode of operation can be compared to perfect current source, meaning, output current should not depend on the load connected to output terminals. Again, if used as an electronic switch, described MOSFET condition corresponds to ON-state. Drain to source current can be given by:[19]

$$I_{ds} = ½ \, k \frac{W}{L} \, (V_g - V_{th})^2 \qquad (1.2)$$

As it can be seen from equation (1.2) and Figure 1.2, I_{ds} in saturation mode does not depend on V_{ds}. In ideal case, saturated MOSFET behaves as perfect current source controlled by V_g only. However, due to finite output resistance (r_o), segment of the Figure 1.2 attributed to saturation mode will have a certain slope given by $1/r_o$ and, in general, will exhibit functional dependence of V_{ds} as well.

The first value to take care about in transistor design is so called off-current, I_{off}. It is a current consumed in stand-by mode of operation, i.e. current which flows when $V_{DS} = V_{DD}$ and $V_{GS} = 0$. Obviously, this current should be as small as possible. Another value of interest is the so called on-current, I_{on}. This one flows when $V_{DS} = V_{DD} = V_{GS}$. Therefore, this current determines the consumption in on-sate operation mode. The third parameter is the sub-threshold swing, S. S is defined as the number of milivolts for which we have to increase gate voltage in order to increase drain current by a factor 10. For the well designed MOSFETs we have $S < 80$ mV/dec. A good transistor should exhibit high on-current, low off-current and small S, meaning, fast transitions between on and off state. However, this kind of devices is challenging to produce, nearly impossible with nowadays standard technology. The required reduction in size of transistor, following Moore's law, implies higher $I_{on.}$ In order to explain this, let us define a new parameter, delay time τ. Delay time is a time required for electron to pass the channel length, meaning, distance between the source and the drain electrode. Modeling channel as a plate capacitor, this time my simply be defined as:

$$\tau = RC = C \frac{V}{I} \qquad (1.3)$$

As it has already been pointed out, Moore's law requires reducing in overall transistor size, leading to shorter channel. On the other hand side, shorter channel means shorter inter-plate distance in the capacitor model, which implies increased capacitance. However, as it can be seen from equation (1.3), increased capacitance will result in increased propagation time. However, many applications require fast transistors (electronic switches, memories). In order to gain from the miniaturization, effect of increased capacitance should be compensated. Possible solution is increasing I_{on}, leading to reduced R and prevailing same or reduced τ. Moreover, low I_{off} is required due to reduction is stand-by mode power consumption. As we have already pointed out, required decrease in delay time implies higher I_{on}. Unfortunately, higher I_{on} implies higher V_{th} which results in higher I_{off}, see Figure 1.3.

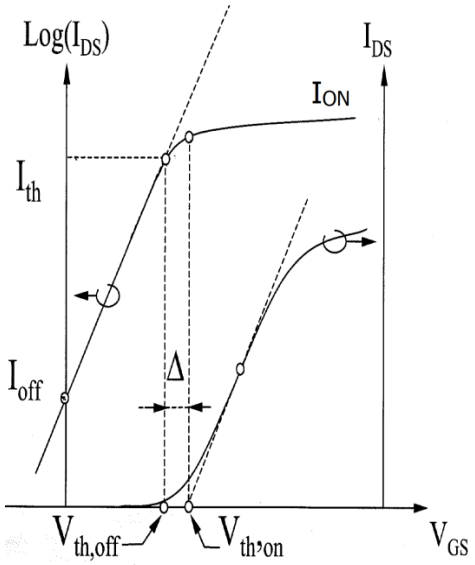


Figure 1.3. Graphical representation of relations between I_{on}, I_{off} and V_{th}. Figure is taken from [21].

Therefore, one can just consider a trade-off between these requirements or look for new mechanisms, like mechanical coupling.[22] Low Stand-by Performance (LSTP) transistors have small I_{off}, but also I_{on}. On the other hand, High Power (HP) transistors have high I_{on}, but also I_{off}. In the middle are Low Operation (LOP) transistors. This is displayed in the Figure 1.4.

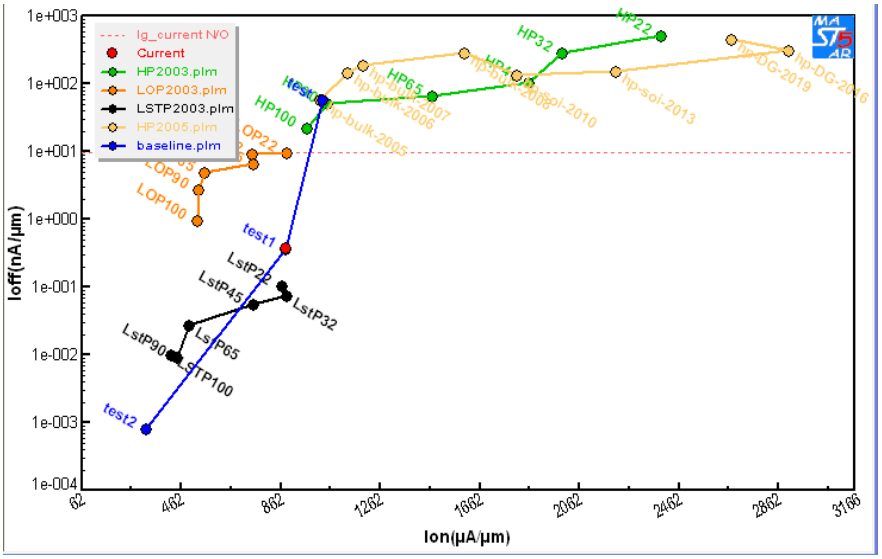


Figure 1.4. ITRS 2003 CMOS I_{on} – I_{off} roadmap. Figure taken from [21]

One way to achieve a small I_{off} is by increasing the oxide thickness T_{ox}.[21] But, this is against the reduction in size of the components in an integrated circuit. Another less conventional solution is to use novel materials like high-k dielectrics and/or semiconductor nanowires. Better electrostatic control and enhanced transport properties make the gate-all-around (GAA) nanowire MOSFET structure a potential candidate for the end-of-the roadmap devices.[23, 24] Simulation results show that the gate lengths in these devices can be scaled down to as small a dimension as the nanowire diameter itself.[25] These devices yield large current per diameter of silicon body. Still, the current through the single nanowire channel is limited to a few microamperes. This limitation can be of importance for industrial applications like analog and radio-frequency.[26] One way of increasing the drive current is assembling more nanowires per device. A typical example is the multi-Fin device. However, since the lateral arraying reduces the density of integration, this solution cannot be completely applied. Vertical stacking of nanowires is expected to improve solution of this problem.[27-29] Using this approach, excellent short channel performance was demonstrated despite the short gate length. The authors also presented evidence of quasi-ballistic room temperature transport.

Threshold voltage control by channel doping is not practical for FinFETs (Figure 1.5) because of the small channel dimensions. Instead, the principal mechanism for threshold voltage control is the gate work function. Metal gates with work functions located in the semiconductor bandgap are required, and the metal must also be compatible with the thermal processing required for device fabrication. [27]

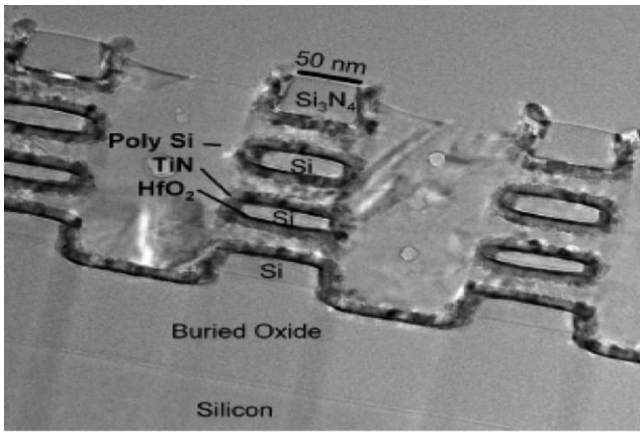


Figure 1.5. Cross-section TEM image of the 3D stacks GAA Si. Figure taken from [27]

In following section of the chapter, we will shortly mention work realized by other research groups in the area of interest of this thesis. Of course, it is not possible to discuss all relevant results, but only some of them, namely ones proving potential of novel materials and structures, and indicating possible research directions.

Silicon nanowires grown by chemical vapor deposition and other methods have been used to fabricate vertical surrounding gate MOSFETs and MESFETs for an area-efficient technology.[25] It was demonstrated that surrounding gate FETs (SGFET) can be used for SRAM, DRAM and high-speed logic circuits.[28] Theoretical studies investigated the electronic, transport and device properties of silicon nano-wires.[29] Nanometer-range device physics, modeling and scaling issues were investigated for the future technological solutions. Simulations on maximum drive current and off - current of metal-gated have already been reported.[25] A process flow simulating the fabrication steps and extracting non-ideal I-V characteristics of the processed transistors is also described. The following equation is presented:

$$\mathrm{I_{DSAT}} = \frac{\mu_{eff}\pi\varepsilon_{ox}}{L\, ln\left(1+\frac{t_{ox}}{R}\right)}\left\{\left[V_{GS} - V_{FB} - \frac{2kT}{q}\, ln\frac{N_A}{n_i^2} - \frac{2}{2\varepsilon_{OX}}\ln(1+\frac{t_{ox}}{R})R^2N_A\right]^2 - \frac{16kT}{\varepsilon_{ox}}n_i^2\, x\, exp\left[\frac{q}{kT}(V_{GS} - V_{DS} - V_{FB})\right]\ln(1+\frac{t_{ox}}{R})\frac{R^2}{N_A}\right\} \qquad (1.4)^{25}$$

which allows us to estimate relation between $\mathrm{I_{DSAT}}$ and nanowire radius R. For low doping concentrations, I_{DSAT} increases quadratically with *R.* This due to the term being negligible compared to value $V_{GS} - V_{FB}$. However, as the radius of the device increases, the effect of term $\frac{2kT}{q} ln\frac{N_A}{n_i}$ becomes significant, and as a consequence of this, the slope of I_{DSAT} starts to decrease. The magnitude of I_{DSAT} deteriorates even

more as both wire radius and doping concentration increase, as shown in Figure 1.6. The importance of this work relies in fact that for the first time it is showed NMOSFET design with high body doping concentrations should be avoided. Figure 1.6 summarizes these conclusions.

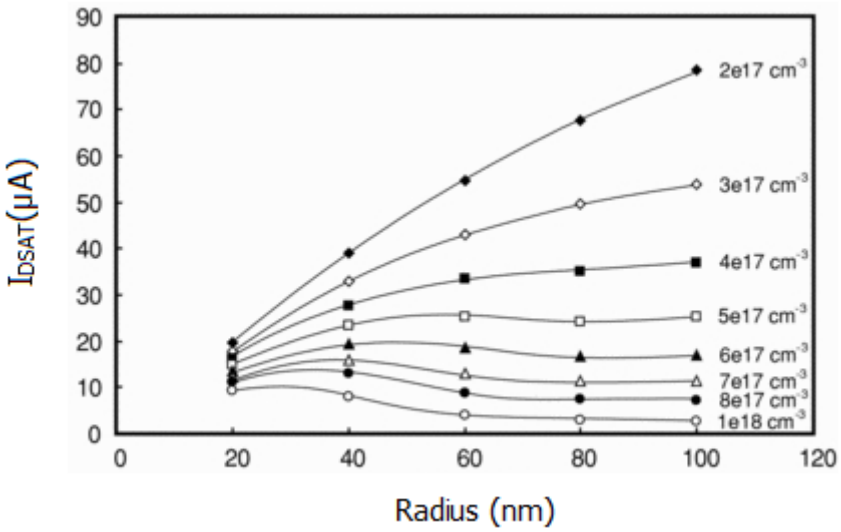


Figure 1.6. Maximum saturation currents (I_{DSAT}) of NMOS transistors used as evaluate elements for different body radius and doping concentrations at L_{EFF} = 250 nm. I_{DSAT} is obtained when V_{GS} = 1 V and V_{DS} = 1 V. Figure is taken from [25]

The same paper reports the output I-V characteristics of the NMOSFET after the processing, as shown in Figure 1.7. This figure also includes the I-V characteristics of the 'ideal' transistors that contain Gaussian source/drain doping profiles and uniform body doping concentration for comparison purposes.

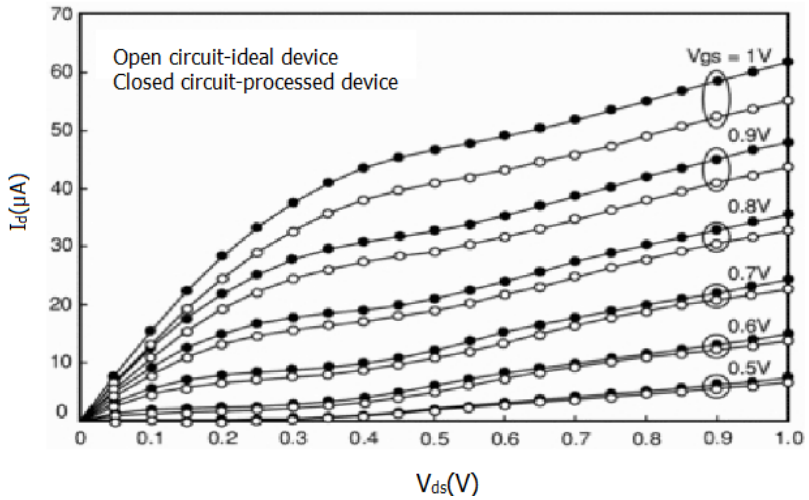


Figure 1.7. Output I-V characteristics of the ideal and processed vertical stacked NMOSFET. Figure is taken from [25]

The next section of the chapter will give short overview of some of the devices realized and their important properties.

The fabrication of the devices based on mentioned concepts has also been reported.[23] $Si_{0.75}Ge_{0.25}$ (50 nm) and Si (30 nm) epitaxial layers were alternately deposited using a cold wall ultrahigh vacuum chemical vapor deposition reactor.

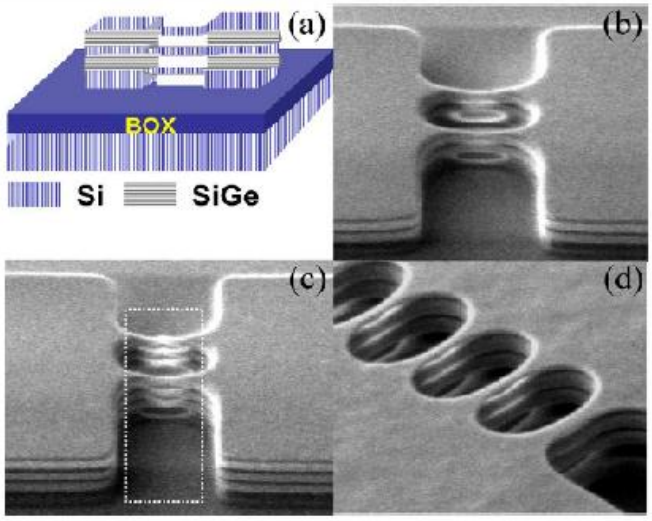


Figure 1.8. Tilted view SEM images after release of stacked NW. (a) Schematic of SiGe NW stacks after oxidation and release. (b) 2X laterally arrayed three stacked NWs. (c) 2X laterally arrayed four-stacked NWs with the dashed line indicating the gate layout. (d) 5X laterally arrayed four-stacked NWs. Figure is taken from [23]

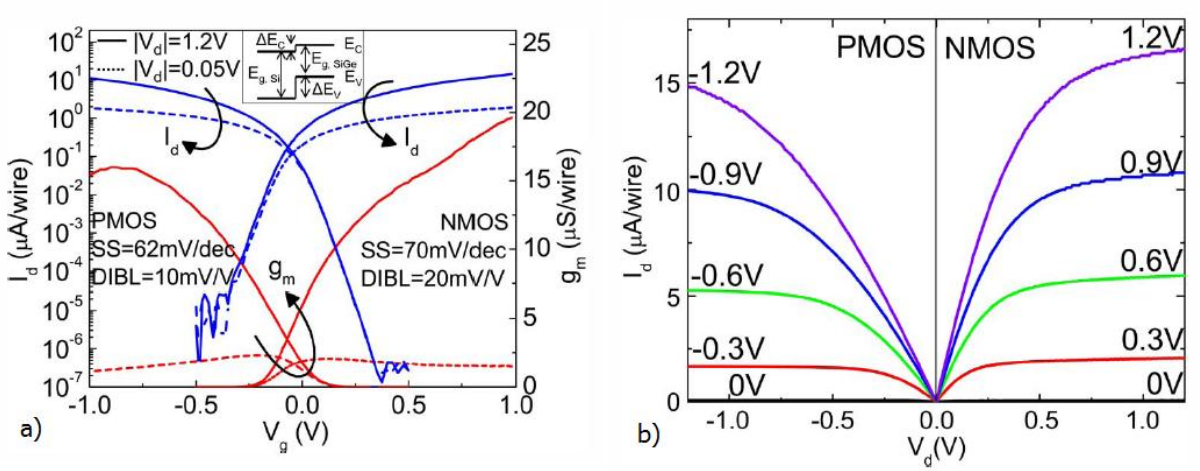


Figure 1.9. a) shows I_d–V_g and gm–Vg plots for stacked NW n-FETs and p-FETs with L_g = 500 nm and NW diameter around 30 nm. b) shows I_d–V_d plot for n-FETs and p-FETs with gate overdrive voltage varying in steps of 300 mV. Figures are taken from [23]

The devices on the figures above have a physical gate length of 0.5 μm and have very interesting properties: near ideal sub-threshold slope S (62–75 mV/dec), low drain induced barrier-lowering (DIBL) (~20 mV/V) and high I_{on}/I_{off} ratios (~10^6). I_{on} and I_{off} currents were measured at $V_{G(ON)} = V_{th} \pm 0.7\ V_{dd}$ and $V_{G(OFF)} = V_{th} \mp 0.3\ V_{dd}$, respectively. V_{dd} is |1.2| V in all measurements. Fig. 1.9 also includes the $g_m(dI_d/dVg)$ behaviors for both devices. For n-FET, the g_m continues to increase with the gate voltage for V_{DS} = 1.2 V while the p-FET shows the peaking in g_m value due to mobility dependence on gate-field which is well known for the bulk FET devices. Authors believe the reason for this is confinement in Ge rich zone capping of the nanowire with a SiGe layer, which avoids the existence of surface states and provides a barrier for holes in germanium. The $I_D - V_D$ characteristics for n- and p-FET in Fig. 1.8 show similar on-currents. Also, it is expected that the optimization of S/D contacts fabrication will lead to further improvements in n-FET characteristics.

Memories based on vertically stacked nanowires have also been reported and explained.[28] Conventional NAND-type nonvolatile flash memory reaches its critical scaling limitations . However, the emerging FinFET and Gate-All-Around (GAA) structures promise improvements for the scalability of future devices.[28] The optimism of researchers is based on better electrostatic control of the short-channel body obtained in these structures. FinFET and GAA silicon nanowire combined with SONOS flash memory have demonstrated improved performance over planar structure device.

Figure 1.10 shows the I_D-V_G characteristics for two kinds of SONOS devices (with and without trap layer engineering - TLE), with L_G ~ 850 nm and diameter ~ 5 nm.

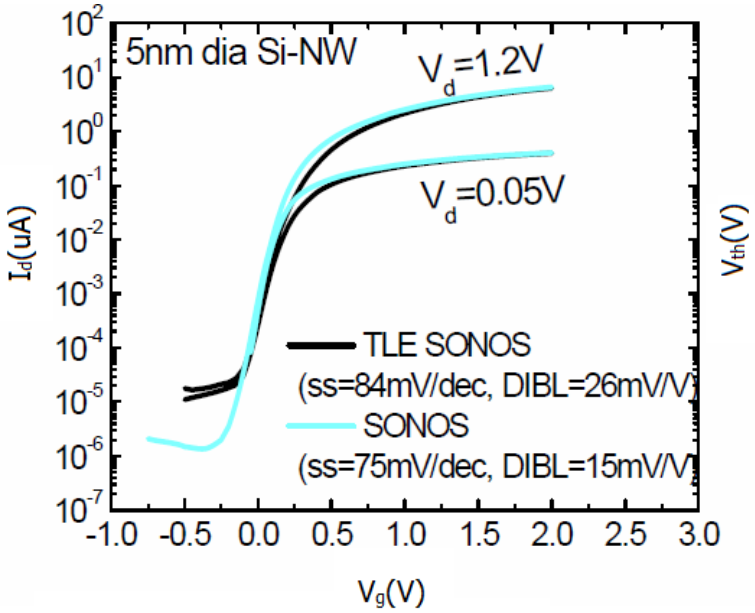


Figure 1.10. I_d-V_g characteristics for diameter 5 nm and gate length 850 nm nanowire devices, with and without TLE. Figure is taken from [28]

Differences in the sub-threshold slope could be due to a better interface quality between gate stack layers. Low DIBL (≤ 30 mV/V) with EOT = 15 nm represents good short channel effect control for the nanowire structure channel. The program/erase (P/E) characteristic on TLE SONOS memory is shown in Fig. 1.11, for two different wire diameters (5 and 8 nm).

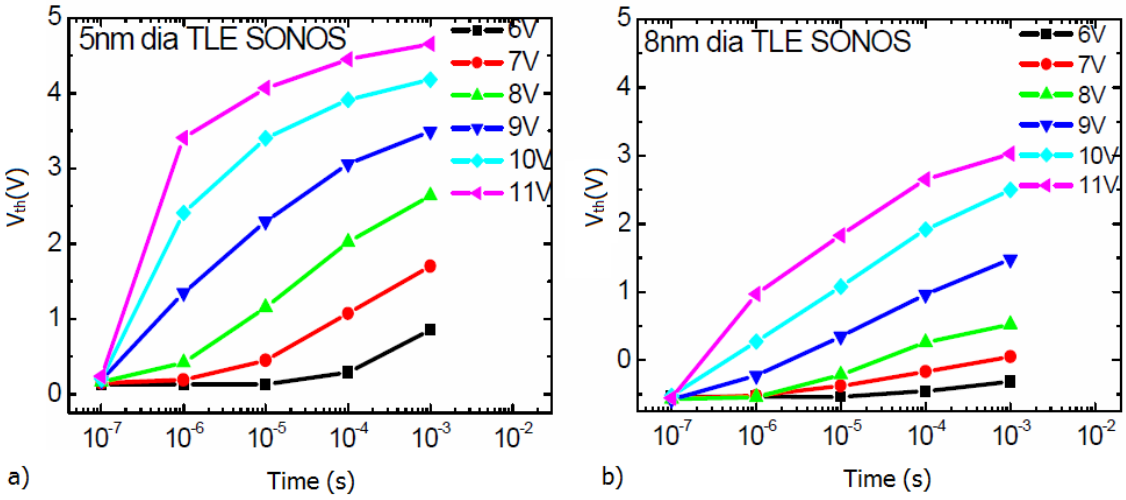


Figure 1.11. Programming characteristics using FN tunneling mechanism of TLE SONOS memory device with diameter 5 nm a) and 8 nm b). The wire with smaller diameter shows much faster program speed. Figure is taken from [28]

Finally, we would like to refer on work on Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors.[30] Temperature dependent measurements are applied in order to demonstrate that the tunneling process is indeed responsible for the electrical characteristics obtained. Even more, for the BTB tunneling, sub-threshold slope of only 40 mV/dec is reported (Figure 1.12). This is an extremely encouraging result.

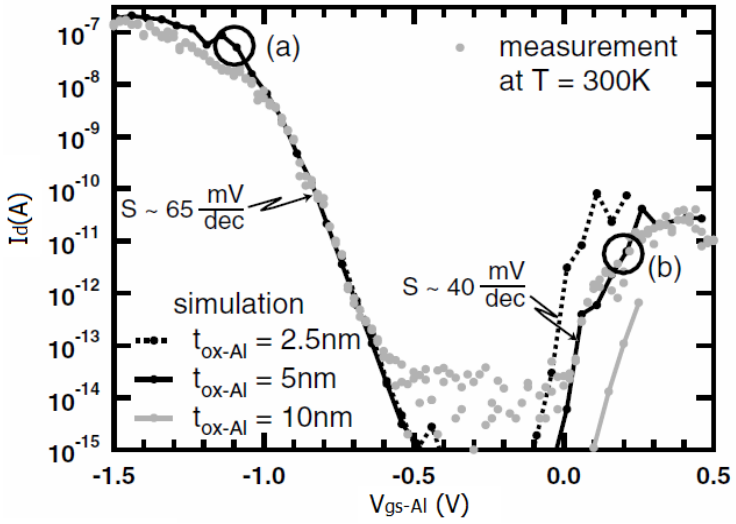


Figure 1.12. I_D-$V_{GS\text{-}Al}$ characteristics for V_{DS} = -0,5 V and $V_{GS\text{-}Si}$ = -3V Figure is taken from [30]

According to authors, the reason why S can become smaller than 60 mV/dec at room temperature is the band-pass-filter-like operation of the BTB tunneling device. A tunneling current can flow only once the conduction band in the aluminum gated region bends below the valence band in the source area that is controlled by the silicon back gate.[30]

Before ending this part of the chapter, we would also like to shortly mention simulations reported on this topic.[31] The authors present simulation results suggesting that S is not governed by thermal limit of 60mV/dec. Due to these sub-threshold swings bellow 60mV/dec, low supply voltage (V_{DD}< 0.3V) and rail-to-rail logic are possible.[31] Important conclusion of this simulation is that unlike UTB MOSFET where S becomes smaller with decrease of Si thickness, double gate tunneling FET exhibits reduction in S with reduction of SOI thickness. This is depicted in Figure 1.13.

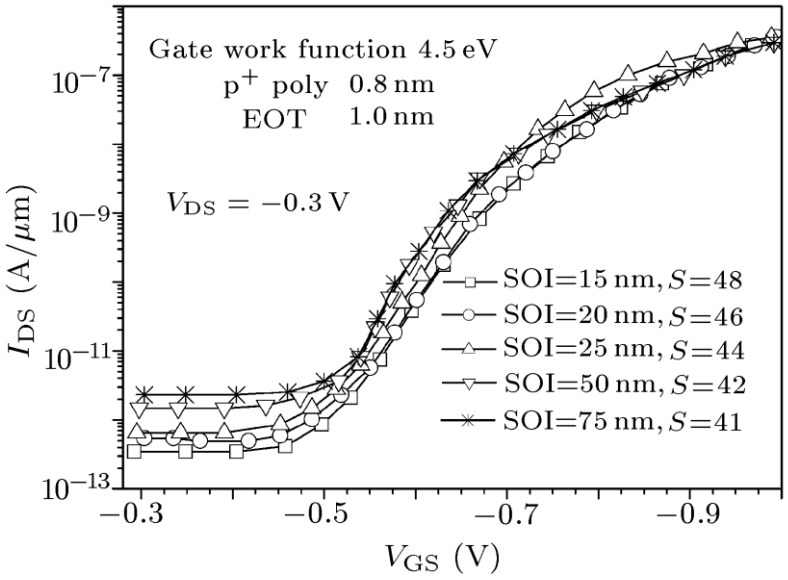


Figure 1.13 Sensitivity of lateral tunneling transistor performance to the Si layer thickness and extracted sub-threshold swing from corresponding I-V characteristics. Figure is taken from.[31]

The presented results are very important since they prove there is enough space for research in area of nanotechnology. Scaling device's dimensions to nano-range enables properties which could not be observed in bulk devices. We would like to point out again, role of this section of the Chapter 1 was not to mention all interesting results but to point out only few of them which clearly demonstrate possibilities hidden in nanometer scale and allow researchers to look for possible improvements in that direction.

Before using nanowires to build MOSFET devices, we should be aware of certain limitations. We must have methodology and technology to analyze electrical properties of nanowires. To do this, we are to know how to contact them, and keep

in mind that contact surface will be from order of few hundred nanometers up to 1 μm. Finally, we should be aware of the best configuration for fabricating transistor out of the nanowire.

In the following chapters, we will present experimental efforts and try to provide theoretical explanations for the results obtained on design and fabrication of the GaAs and Ge nanowire based MOSFETs.

1.3. **Conclusion**

In this Chapter we motivated the research done on the nanowires as the promising candidates in an ongoing miniaturization of the technology. We briefly explained two types of nanowires used in thesis, GaAs and Ge, and motivated avoiding of gold as the growth catalyst. Furthermore, we defined current problems regarding the integrated circuit components scaling, namely I_{on}/I_{off} ratio and delay time. At the end of Chapter we showed representative results done by other research groups (both experimental and simulations) and motivated research described in following chapters.

2. Experimental

2.1. Introduction

In this chapter we present experimental techniques and methods which were used in the frame of this thesis. We explain how the nanowires were obtained, both by Molecular Beam Epitaxy (MBE) and Chemical Vapor Deposition (CVD) technique and give an overview of all experimental steps we performed for the fabrication of functional nanowire devices.

2.2. Nanowires and their growth process

2.2.a. Nanowires

A nanowire is a longitudinal crystal with a diameter of the order of nanometers (10^{-9} meters). It can be made of different materials, including metals (e.g. Au, Ag, Pt,…)[32], semiconducting (e.g. Si, InAs, GaN, GaAs,…)[33], and insulating (SiO_2, TiO_2,…).[34] Nanowires can also contain heterostructures, by presenting a variation in composition along its length (GaAs-InGaAs-GaAs) or with a core/shell geometry, when the composition is varied along the radius .[35,36] Typical nanowires have a length-to-width ratio of 1000 or more, so that they are often referred to as one dimensional materials. Due to this particular dimensions, nanowires are expected to present different optical, electrical, and magnetic properties from their bulk counterparts.

Typically, nanowires are obtained by the Vapor-Liquid-Solid method, in which gold nanoparticles are used to gather the growth precursors and induce the nucleation and growth of nanowires. A very important challenge in this area is to avoid the use of gold in the growth process, as gold is known to be a fast-diffusing metal that significantly influences the properties of semiconductors.[11,12] Different research groups have worked in this area, and have found methods of using alternative metals such as aluminum and titanium or simply avoiding the use of a catalyst. [13-17]

The GaAs nanowires investigated in this thesis are synthesized without the use of an external catalyst. They exhibit diameter of about 100 nm (from 40 nm to 200 nm depending on growth conditions) and length from few µm to more than 20 µm. A clear prismatic geometry with a hexagonal section is observed. The crystal structure is zinc-blende. Under certain growth conditions a mixture of wurtzite and zinc-blende is observed.[37]

The Ge nanowires investigated in this thesis were grown via Chemical Vapor Deposition (CVD) technique using gold, bismuth and indium as catalyst.

2.2.a.1 GaAs nanowires growth process

The GaAs nanowires were grown by molecular beam epitaxy. Figure 2.1 depicts the schematics of the MBE system used. Two-inch GaAs wafers were coated with a 30–40 nm thick silicon dioxide film by means of sputtering and used as substrates. In order to avoid possible contaminations, the sputtered substrates were treated with buffered 10% hydrofluoric acid (aqueous solution, $HF:H_2O$ = 1:2), stored in isopropanol, dried with nitrogen and finally, immediately loaded in MBE.

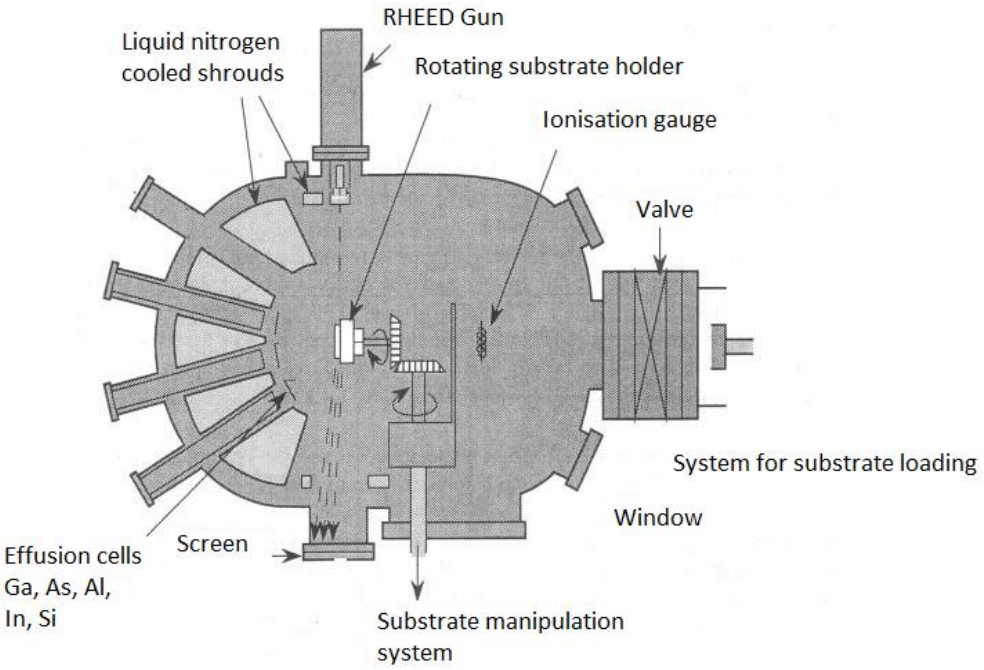


Figure 2.1. Schematics of III-V Gen-II MBE system

After the HF dip, the thickness of the remaining oxide was between 6 and 20 nm. Prior to the growth itself, the wafers were heated at 650 °C for 30 min. The purpose of this step is to desorbe any remnant adsorbed molecules of the surface. The synthesis was performed at a temperature of 630 °C, arsenic pressure was kept between $3.5x10^{-7}$ and $2.3x10^{-6}$ mbar, the Ga rate varied from 0.12 to 0.82 Å/ s, and under rotation of 4 rpm. A typical example of a nanowire formed under such conditions is shown in figure 2.2 a). Wires from this micrograph were grown on (111)B GaAs wafer. The nanowires grow in direction perpendicular to the surface, following the (111)B orientation of the GaAs substrate.

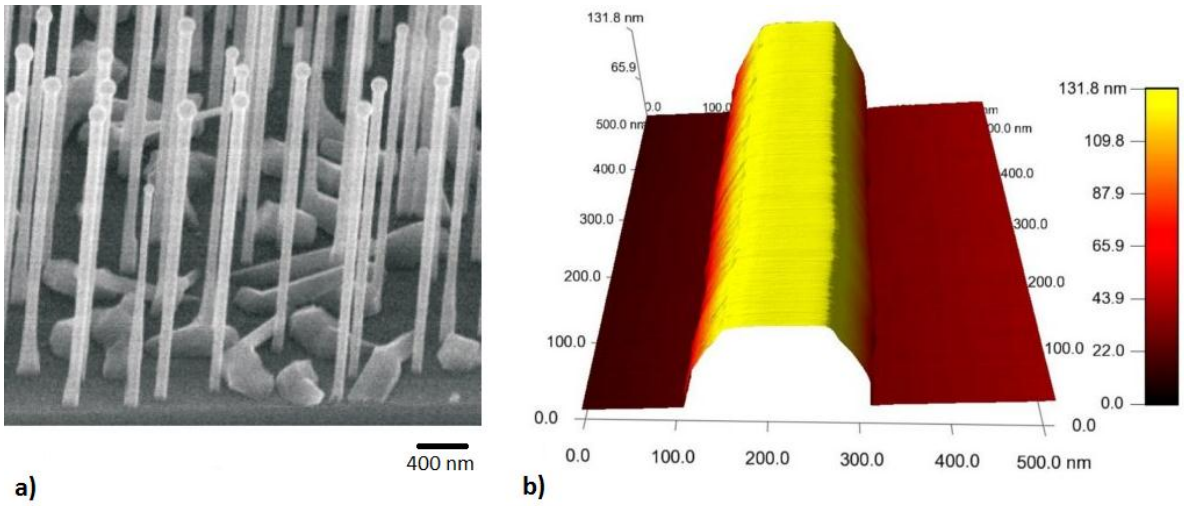


Figure 2.2. a) SEM micrograph of MBE grown GaAs nanowires on (111)B GaAs substrate sputtered with 10 nm of SiO_2. b) A single GaAs nanowire lying on a substrate imaged with atomic force microsocpy. Figures are taken from. [38]

In order to improve understanding of the growth mechanisms of the GaAs nanowires, the growth of the nanowires was studied as a function of different conditions for which nanowire growth occurred. [38,39]

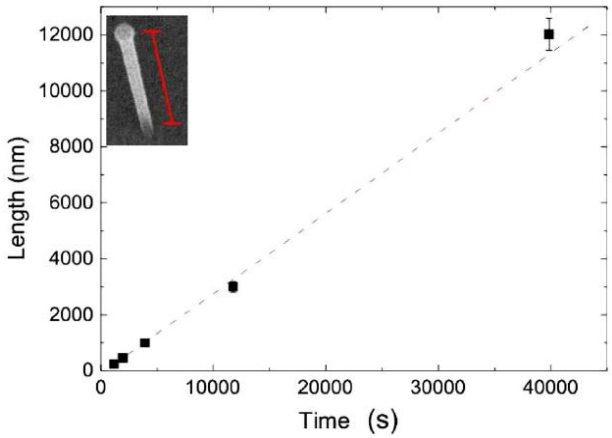


Figure 2.3. Time dependence of the length of the nanowires grown with a 0.25 Å/ s Ga rate, $7x10^{-7}$ mbar of As pressure and temperature of 630 °C. The figure is taken from [38]

Figure 2.3 reports the length as a function of growth time. The different points in the graph correspond to different growth runs performed with same growing conditions. In case showed on Fig. 2.3., the As_4 partial pressure was $7x10^{-7}$ mbar while Ga rate was kept on 0.25 Å/s. The length linearly increases with time, no saturation in the growth rate is observed for growth runs shorter than 11 h. The calculation of growth rate is based on determining the slope of the linear fit. The value obtained is 2.8 Å/s, which is more than a factor 11 of the nominal Ga rate. As already reported [38], the existence of an offset in the beginning of the growth is related to the nucleation time. Moreover, the analyses of the growth rate of the

nanowires for other growth conditions was performed as well. We discuss first the influence of Ga rate.

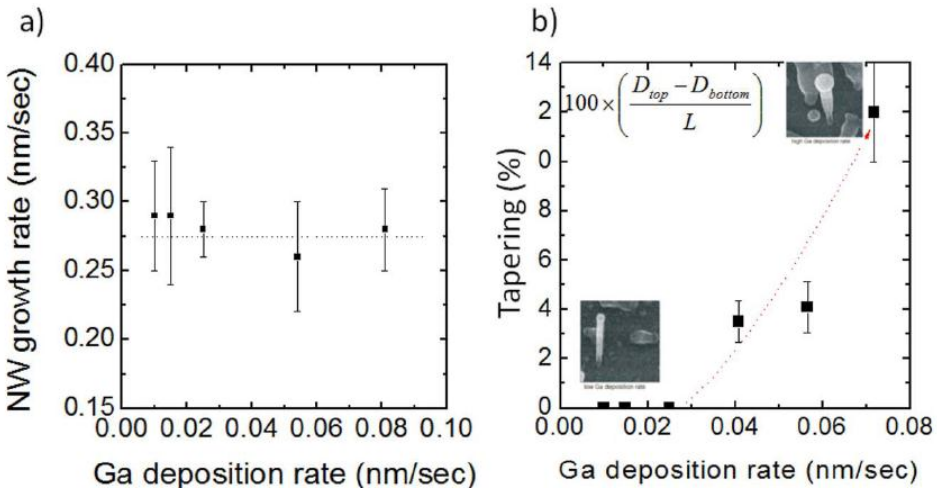


Figure 2.4. Effect of the Ga deposition rate: a) growth rate of the nanowires as a function of the Ga deposition rate and b) tapering of the GaAs nanowires as a function of the Ga rate, defined as the percentage increase of the diameter between the top and the bottom of the nanowire. Figures are taken from [38]

As shown in figure 2.4. a) the growth rate of the nanowires does not significantly change when the Ga rates are varied from 0.12 to 0.82 Å/s. This observation leads to conclusion that, under these conditions, the growth of the nanowires is not limited by the number of Ga atoms arriving at the surface, unlike the case of GaAs thin films. We should also stress that nanowires grown under high Ga rate conditions exhibit an inverse tapered geometry, meaning, the diameter of the nanowire increases from the base towards the tip where it exhibits the maximum value. The effect of the As_4 partial pressure was also measured and analyzed. Relation between the growth rate and As_4 pressure is plotted in figure 2.6. For As_4 pressures in range between $3.5x10^{-7}$ and $8.0x10^{-7}$ mbar, the growth rate of the nanowires is directly proportional to the pressure. Moreover, we were able to calculate As_4 threshold pressure of $1.4x10^{-7}$ mbar, meaning, growth cannot occur for pressures bellow this value.

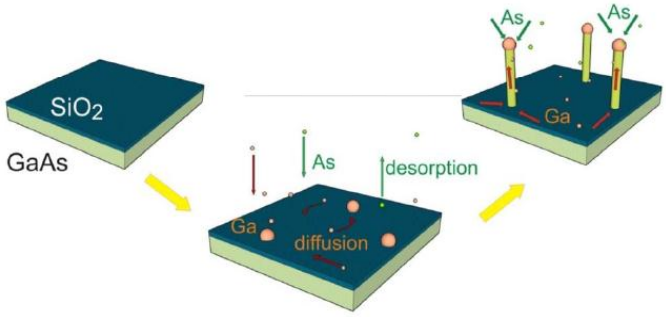


Figure 2.5. Schematics representation of the nanowire growth. Figure is taken from [38]

Figure 2.6. represents the nanowire growth rate as a function of As_4 pressure. The As_4 molecules reach the Ga droplet where they decompose into single As atoms. After that, As atoms diffuse through the droplet until they reach the interface with the nanowire. There, they create covalent bonds with the Ga atoms and form GaAs. When the pressure of the As_4 molecules arriving at the surface equals the vapor pressure, the Ga droplet is in equilibrium and the growth of nanowires cannot occur. A schematics of the growth model is shown in Fig. 2.5.

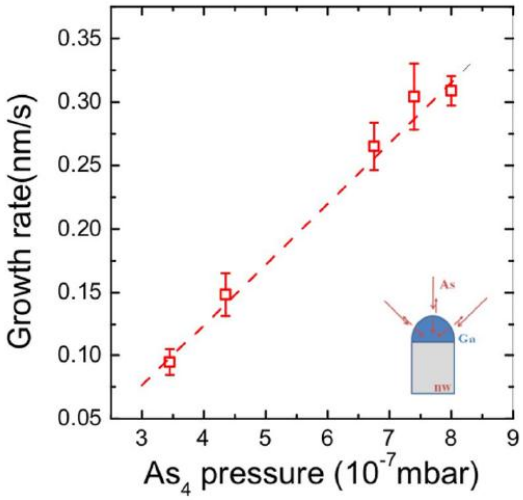


Figure 2.6. Growth rate of GaAs nanowires as a function of the As4 pressure. The inset schematically shows the As4 arrival, diffusion, as well as desorption from the Ga droplet. Figure is taken from [38]

Nanowires continue to grow with further increase of the As_4 partial pressure up to $4x10^{-6}$ mbar. However, it should be noted that for pressures between $1x10^{-6}$ and $4x10^{-6}$ mbar, a large distribution of lengths is observed. Due to this, statistical analysis and growth trend determination is not possible. If the As_4 partial pressure is increased even more, the growth process stops and no nanowires are observed. The behavior of the diameter during growth was also analyzed as a function of time and As_4 pressure, the results shown in figure 2.7. The diameter of the nanowires is homogeneous through the length of the nanowire. Moreover, diameter tends to increase with time for Ga rates equal to or lower than 0.25 Å/s. Figure 2.7 reports and example were nanowires are grown with an As_4 partial pressure of $2.3x10^{-6}$

mbar and a Ga rate of 0.25 Å/s with the resulting radial growth rate of 0.07 Å/s. In case of shorter nanowires and shorter corresponding growth times, effect of radial growth can be neglected. However, for long growth times, neglecting contribution of the radial growth would introduce errors. Radial growth rate increases proportionally with the As_4 pressure up to $7x10^{-7}$ mbar while for higher As_4 pressures it saturates.

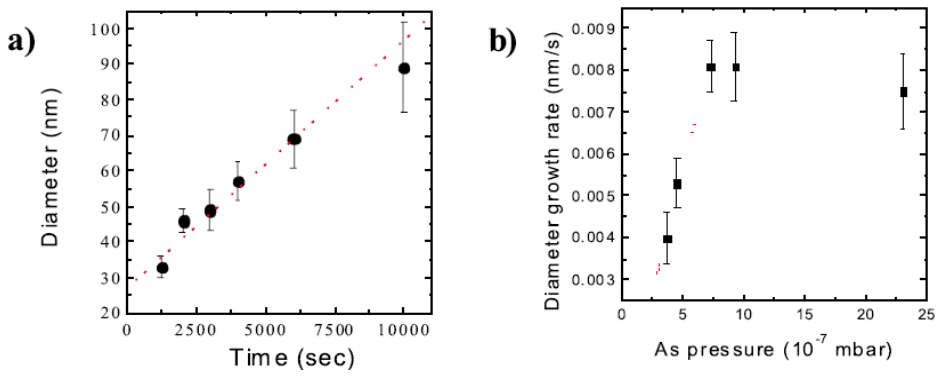


Figure 2.7. a) Behaviour of the diameter of the nanowires with respect to the deposition time, As_4 pressure is $2x10^{-6}$ mbar. b) Radial growth rate of the nanowires plotted with respect to the As_4 pressure. Saturation appers for pressures above $7x10^{-7}$ mbar. Figure is taken from [38]

2.3. Ge nanowires growth process

Chemical Vapour Deposition (CVD) growth process based on Vapor-Liquid-Solid (VLS) mechanism presented here was realized by Dr. Ying Xiang during her stay at the group of Prof. M. Brongersma in Stanford University. Dr. Xiang's contribution in growing Ge nanowires used in this thesis is kindly acknowledged.

2.3.a.1. Ge nanowires grown using Au as catalyst

The concept of VLS growth is based on the fact that the melting temperature of the catalyst can be lowered by alloying it with another element.[40] The lowest temperature at which the alloy of two or more elements liquefies is known as the eutectic temperature. For the purpose of Ge nanowires the growth alloy is a binary system, consisting of Au and Ge. The eutectic composition is at 28% of Ge in Au. This results in drop of melting temperature decreases from 1064 °C to 361 °C. A schematic of the VLS growth mechanism is shown in Figure 2.8. A catalyst particle, in this case Au, is heated to a temperature above the eutectic temperature. Exposing the heated catalyst particle to vapor phase semiconductor reactants, in this case

germane (GeH_4), results in the creation of a liquid alloy with the precursor (see Figure 2.8 a)). Germane decomposes at the catalyst surface to germanium and hydrogen. Germanium diffuses into the catalyst causing the increased Ge concentration inside the liquid alloy. Concentration gradient inside the droplet is formed leading to germanium diffusion through the gold droplet, see Figure 2.8 b). The process flows until Ge concentration inside the catalyst is saturated. After that, the semiconductor underneath the droplet starts to precipitate resulting in Ge nanowire growth. This process can also be described by so called binary phase diagram of Au-Ge system, Figure 2.9.

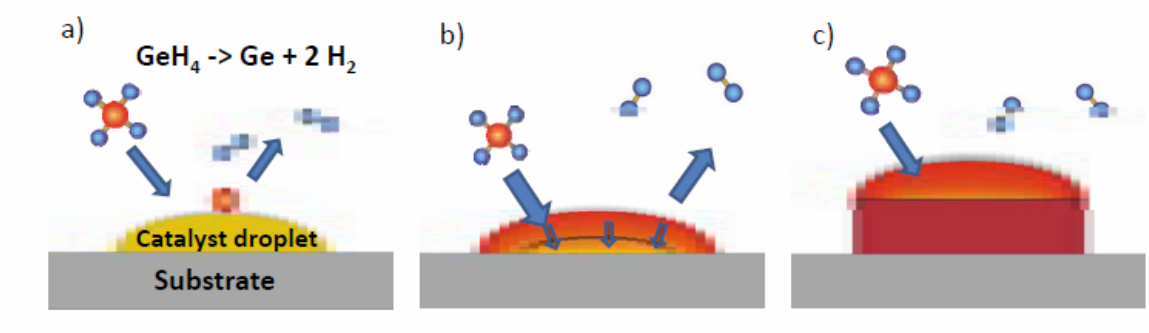


Figure 2.8. Schematic showing the VLS growth mechanism. a) The precursor decomposes and forms a liquid alloy with the catalyst for temperatures higher than eutectic temperature. b) Germane decomposes to germanium and hydrogen, Ge diffuses into the catalyst (eg. Au) increasing Ge concentration in the droplet. C) Once saturation conditions are achieved, Ge percipitates under the droplet leading to nanowire growth. Figure is taken from [40]

The depicted phase diagram denotes the alloy melting temperature with respect to the content of the gold. The process is initiated when the temperature is higher than the eutectic temperature of a pure solid gold. The precursor (germane) is decomposed to hydrogen and germanium when its molecules impinge on the gold surface. Hydrogen molecules leave away from catalyst droplet while germanium diffuses into it. Since decomposition and diffusion at this point are continuous processes, concentration of Ge in the droplet increases, while the Au concentration decreases.

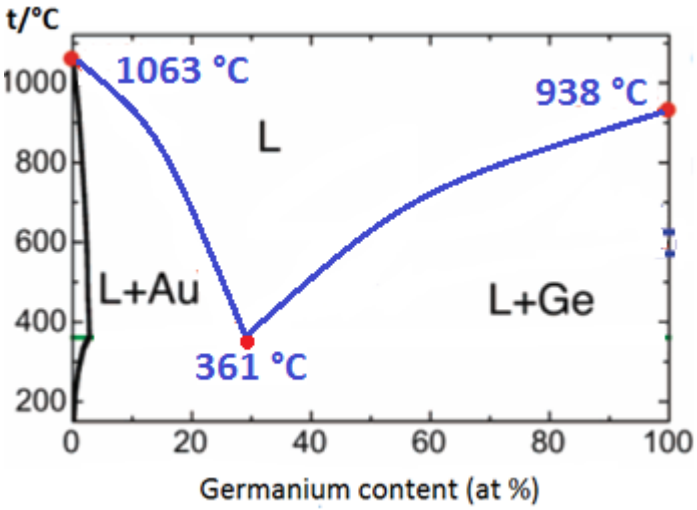


Figure 2.9. Au-Ge binary alloy phase diagram.

Analyzing the diagram 2.9 one can distinguish few specific areas. Between the starting point (100% Au, 0% Ge) and position corresponding to 25% of Ge, solid phase Au and liquid phase alloy do coexist. However, between position corresponding to 25% of Ge and 33% of Ge the concentration of both Au and alloy allows only a liquid phase to exist. The saturation is reached for concentration of Ge equal to 33%. For concentrations equal to or higher than 33%, germanium nanowire starts to grow. The time necessary for Ge to enter the catalyst, form an alloy, saturate and start the nucleation process is known as the nucleation time. More information on the nucleation time can be found in [40].

As it has been mentioned above, although known as a very good catalyst enabling successful growth of Ge nanowires, use of gold should be avoided. It is because of this why alternative materials for catalyst are explored. Potentially promising metals are indium and bismuth. Due to the electronic configuration of their outermost shells, indium and bismuth are acceptor and donor impurities in germanium, respectively. Moreover, from application point of view it is worth of mentioning that both Bi and In are compatible with current Si based CMOS technology.[40] In next subchapter we will present growth of Bi and In catalyzed Ge nanowires, while analyses of their electrical properties and comparison to Au catalyzed Ge nanowires will be given in Chapter 5.

The germanium nanowires were synthesized in a thermal chemical vapor deposition (CVD) furnace. A mixture of germane (GeH_4) in argon was used precursor gases. in the following, we present a short description of CVD set-up. Figure 2.10 a) displays a picture of the used CVD setup. The main parts of the set-up are the quartz tube, the heater, the gas flow controller, and the pressure controller. Figure 2.10 b) shows a zoomed image of the quartz tube and the heater. A schematic representation of sample holder is given in figure 2.10 c). The samples are placed on a quartz plate. Both sample and flowing gases in the tube are heated homogenously due to the uniform radiation of heating elements. A precise control of the growth temperature is achieved, resulting in well controllable growth rate. The operation temperature in the furnace is measured by means of thermocouple and can be precisely adjusted, starting from the room temperature up to 1200 °C. The CVD furnace is equipped

with the silane and germane lines. Source of pure hydrogen (H_2) is connected to furnace, which provides operator with possibility to clean and anneal sample inside hydrogen environment. Noble gas argon (Ar) is used for flushing the chamber before and after the growth. Finally, the flow and the pressure of the gases are controlled by precise flow meter controlling the pump speed via the feedback.

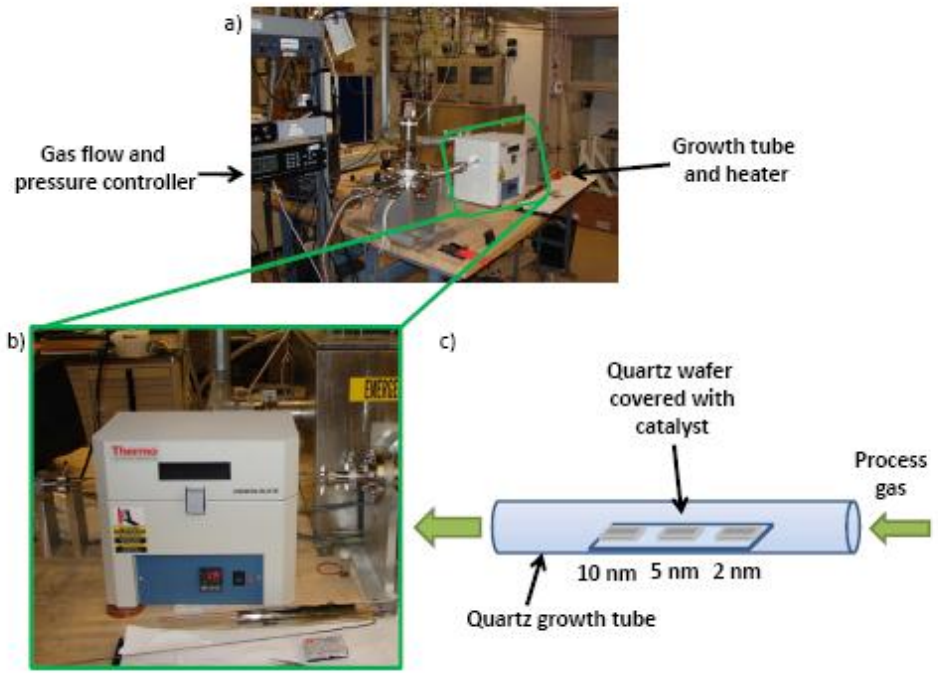


Figure 2.10. Pictures of the CVD setup used to synthesize germanium nanowires. a) setup overview, b) zoom of the growth chamber and heating element and c)sketch of the growth chamber and the position of the samples during growth. The figure is taken from [40]

2.3.a.2. Ge nanowires using Bi as catalyst

Now we turn to the description of the Ge nanowires growth using bismuth as catalyst. Bi acts as a low solubility n-type dopant in germanium. Moreover, the Bi-Ge system has a relatively low temperature eutectic point of 271 °C.[40]

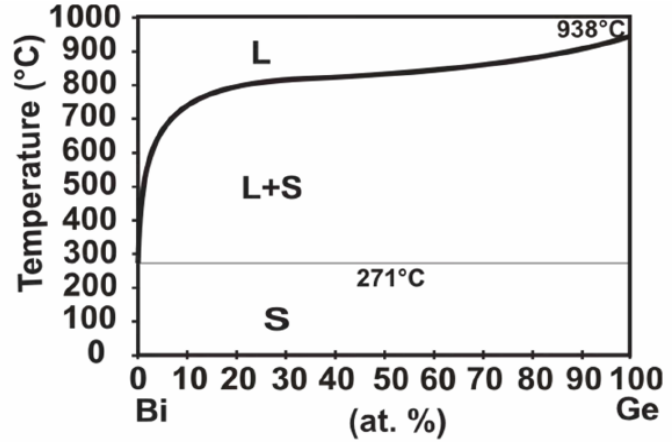


Figure 2.11. The bi-Ge binary phase diagram. Figure is taken from [40]

The phase diagram of the binary Bi-Ge system is showed in Figure 2.11. The eutectic alloy is composed of nearly pure Bi. The liquidus line in the diagram shows the composition of a Bi-Ge alloy in the liquid state as a function of temperature. For a temperature range between 270 and 500 °C, the composition stays quite close to 100% Bi. This indicates an extremely low solubility of Ge in Bi. In the process of growth, the precursor diffuses through the droplet resulting in deposition at the interface between solid and liquid phase. Necessary pre-condition for the diffusion is possibility of certain amounts of Ge to dissolve in Bi. However, due to the low solubility of Ge, nucleation at temperatures close to the eutectic is a challenging task. Analyzing the phase diagram leads to conclusion that the nanowire growth will be easier to achieve at higher temperatures, due to higher solubility of germanium in bismuth.

The growing substrates were 1 cm x 1 cm squares cut out of 5 inch fused quartz wafers. Cleaning the sample includes first step consisted of boiling in acetone for 10 min, followed by 10 min of cooling in room temperature acetone. Second step includes washing inside isopropanol and final one is nitrogen drying. After that, a bismuth layer with different thicknesses (1.5, 5 and 10nm) was evaporated by a electron beam evaporation from a high purity Bi source. In order to obtain Bi droplets prior to the growth, a high temperature anneal in H_2 atmosphere was performed inside the CVD furnace at 825 °C for a 5 min period and under the 30 Torr pressure. After that, the native Bi oxide was reduced and temperature was very slowly decreased to the actual growth temperature. It is very important to change the chamber temperature slowly, otherwise bismuth will form powder on the surface. For the Ge nanowire synthesis, GeH_4 (10 %) in Ar was introduced into the growth chamber. Bismuth oxide reduces the decomposition of GeH_4 and therefore the nanowire growth as well, so the role of the oxide reduction is crucial.

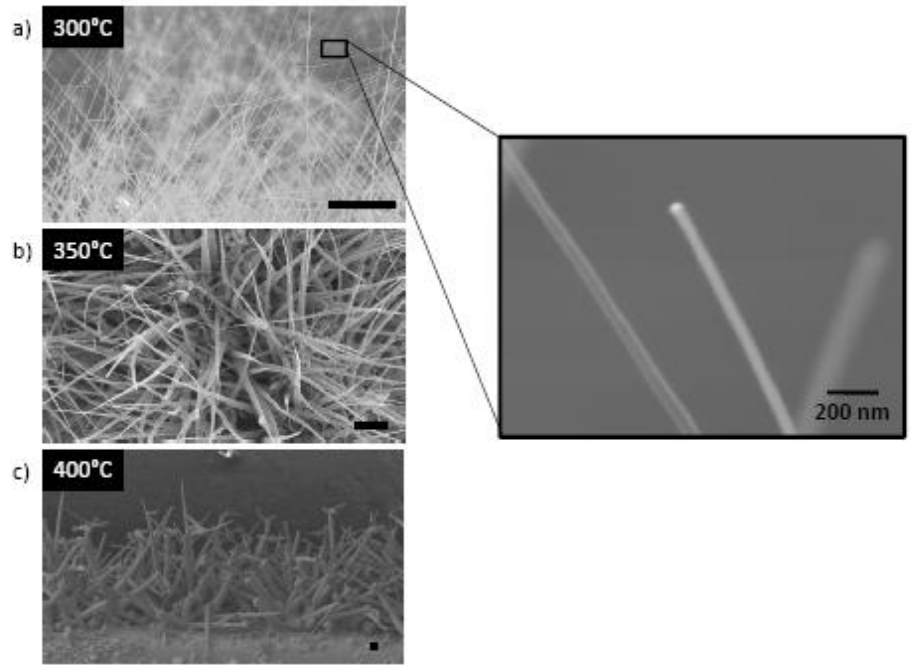


Figure 2.12. Scanning electron micrographs of Bi catalyzed Ge nanowires grown at a) 300 °C, b) 350 °C, and c) 400 °C. Figure is taken from [40]

It can be found in the literature that the decomposition of molecular hydrogen is enhanced at high temperatures and gas pressures.[40] We observed that catalyst annealing in H_2 atmosphere, high temperatures and a pressure of 30 Torr are the necessary conditions. We have seen that the annealing step should be short in order to prevent the evaporation of the liquid Bi droplets formed by the annealing. The temperature of 825 °C is found to be optimal for this purpose. Without this annealing step, a thin native oxide layer would form around the catalyst, causing only small amount of nanowires to grow. For all growth sessions, a hydrogen flow of 1 sccm and a flow of 50 sccm of 10 % germane in argon were used. The overall pressure ratio was altered between 30 and 300 Torr. Four temperature values were applied (280, 300, 350 and 400 °C) for each value of pressure. On figure 2.12 we report SEM micrographs of nanowires obtained at a temperature of 300, 350 and 400 °C. The lowest temperature of 280 °C was proved to be insufficient for nanowires to grow, due to the very low solubility of Ge in Bi. From 300 to 400 °C, the nanowire density tends to increase with the gas pressure. Not only the nanowire diameter but also the tapering effect increase with temperature. More details on the growth mechanism can be found in [40].

2.3.a.3. Ge nanowires using In as catalyst

Here we describe the growth of the germanium nanowires with indium as catalyst alternative to gold.

The In-Ge phase diagram is plotted in Figure 2.13. The eutectic temperature of the binary In-Ge system is 157 °C and it is achieved for alloy consisted of the almost pure In. This is significantly different situation compared to Au-Ge binary system, in which the eutectic point solubility of Ge in Au is 72 at%. For temperatures above 157 °C, the liquidus line defines the composition of the In-Ge alloy in the liquid state as a function of temperature. However, for temperature range between 157 °C and 250 °C, the liquidus line is very close to pure In composition. Simillar to situation described in 2.2 c-2), this indicates a very low solubility of Ge in In. As described in literature[40], the growth precursor diffuses through the droplet to deposit at the interface between solid and liquid phase. Necessary condition for the diffusion to occur is presence of certain amount Ge in In. As a consequence, one can conclude that temperatures above 250 °C are the most favorable for the growth of Ge nanowires [40].

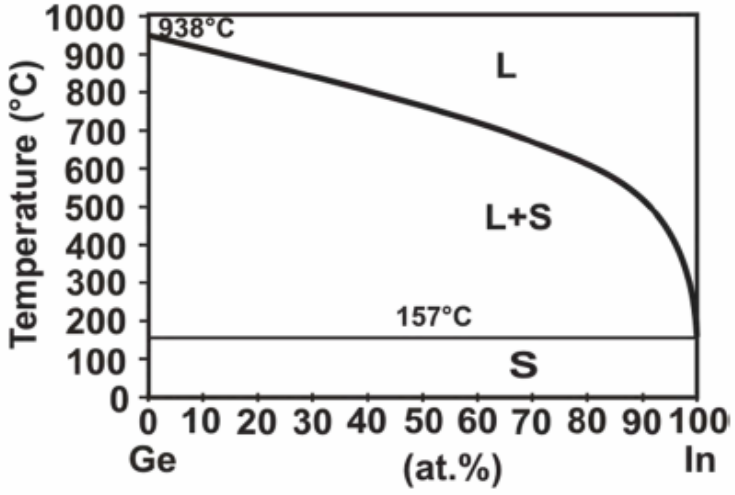


Figure 2.13. Phase diagram of the In-Ge system. Figure is taken from [40]

Unfortunately, in the presence oxygen indium oxidizes.[40] Indium oxide interferes with the catalytic decomposition of GeH_4 resulting in reduced nanowire growth. Oxidation rate may be decreased by exposing it to a reducing gas such as atomic hydrogen [40]. We found that annealing of the indium catalyst in H_2 atmosphere at high temperatures and a pressure of 30 Torr is a necessary condition to obtain a high yield of nanowires on the substrate. Omitting this step results in the complete oxidation of the catalyst. As a consequence, number of nanowires grown per sample is significantly reduced [40]. Due to technical characteristics of the used CVD machine (figure 2.10), synthesis is not realized under ultra high vacuum conditions. It is because of this why a small percentage of oxygen is always present in the gas

phase. In general, growth conditions including a certain concentration of atomic hydrogen will prevent re-oxidation of indium.

Furthermore, we studied influence of the temperature and gas pressure to the nanowire growth. The growth temperature was altered within a range from 250 to 400 °C, while the GeH_4 partial pressure was changed in steps between 3 and 30 Torr. Since we did not observe nanowire growth on the substrates containing no catalyst, we can exclude the possibility of catalyst independent nanowire growth. Figure 2.14 displays representative SEM images of the nanowires obtained after 30 minute growth.

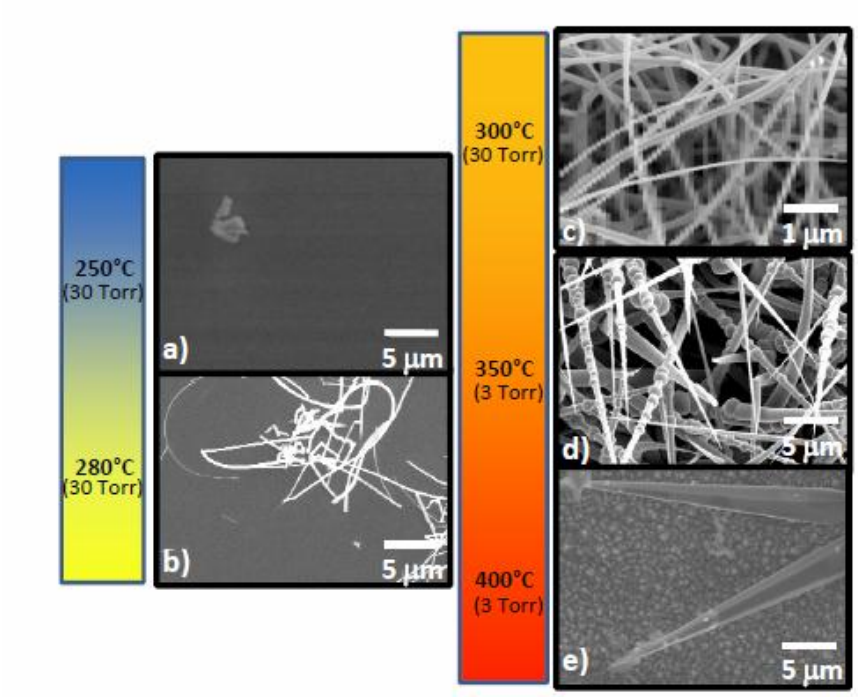


Figure 2.14. SEM images of In catalyzed Ge nanowires grown at a)250 °C and 30 Torr, b) 280 °C and 30 Torr, c) 300 °C and 30 Torr, d) 350 °C and 3 Torr, and e) 400°C and 3 Torr. Higher number of nanowires was observed for germane partial pressure of 30 Torr and temperature of around 300 °C. Figure is taken from [40].

The growth sessions realized for temperatures between the eutectic point and 250 °C did not yield nanowires, Fig. 2.14 a). This result could be consistent with the very low solubility of germanium in indium in that range of temperatures. More details can be found in [40].

Successful nanowire growth is obtained at a temperature of 280 °C and a partial pressure of 30 Torr, as shown in Fig. 2.14 b). The micrograph shows an existence of numerous indium catalyzed germanium nanowires. However, the nanowire density is very low. Moreover, nanowires are randomly distributed over the sample surface. Further improvement was obtained by increasing the growth temperature to 300 °C. As shown in Fig. 2.14 c), density of the nanowires on the sample surface is much higher. Tapering effect is observed (diameters range between 10nm and 160nm). When the growth temperature is 350 °C, the tapering increases, resulting in conical nanowire geometry, as illustrated in Fig. 2.14 d). The growth performed at 400 °C resulted in highly tapered wires, with lengths in micrometer range, as presented in Fig. 2.14 e).

The growth temperature of approximately 300 °C was found to be optimal for growing indium catalyzed germanium nanowires. SEM micrographs clearly demonstrate that both higher and lower temperatures result in reduced density of nanowires on the sample and increased nanowire diameter. The tapering of the nanowires is found to decrease with temperature [40].

2.4. Sample fabrication. From nanowire to device

In this subchapter we will describe experimental procedures and techniques necessary to fabricate samples. The description is presented step by step:

2.4.a. Substrate preparation and cleaning

This is the first step and it is same for all kind samples. 3 inch wafers made of highly n-doped silicon coated with thermally grown silicon-dioxide layer are cleaved on smaller pieces with diamond scriver and cleaned. The use of a highly doped substrate is necessary so that it can be used as back gate electrode. The presence of a thermal oxide serves to prevent any leakage. The substrates are cleaned by sonicating them at room temperature in acetone, flushed with isopropanol and blow-dried with nitrogen.

2.4.b. Nanowire transfer

In case of four or more contact devices, additional steps are required prior to this one. For two point devices based on optical lithography (to be explained later) we go directly to this step. Reasons why nanowire transfer is necessary are two. First, original substrate on which nanowires are grown normally contains huge number of nanowires. Due to this, fabrication of single nanowire device would be extremely difficult. A second reason is the orientation of nanowire with respect to growing substrate. The nanowires are normally perpendicular to substrate or form 35° angle with it. In order to make contacting procedure simpler, all devices we produced are planar and nanowires are lying on the substrate. To achieve this we investigated few transferring techniques. The first one was based on friction between original substrate with grown nanowires and new one on which we want to transfer the nanowires. The new substrate is fixed via a vacuum pump while the sample with nanowires is rubbed against it. As a result, certain number of nanowires are transferred from the substrate on which they are grown to the new one. Although

fast and simple, this technique showed some drawbacks. The density of transferred nanowires was regularly too high and rubbing was damaging the oxide layer. To be able to focus on single nanowire, an alternative technique needed to be found. The solution was sonication. Samples with nanowires were placed in glass vessels contaning proper amount of isoproanol and exposed to ultra-sound waves. As a consequence of ultra-sound, nanowires are removed from substrate and form a solution in isopropanol. A few drops of the solution containing the mixture of the isopropanol and the nanowires are transferred to the new substrate by a pipette. After 5 min of drying at room temperature under laboratory flow box, isopropanol evaporates while nanowires, due to Van Der Waals forces, remain attached to the substrate. Using this method, we obtained both lower density of nanowires as well as managed to avoid damaging the silicon-dioxide. This technique proved to be very useful for GaAs nanowires. However, in case of the Ge nanowires the ultra-sound waves resulted in the breaking of the nanowires. It is because of this why we tried an alternative method, consisting of direct mechanical transfer. Sharp tip was made of laboratory paper and samples with nanowires carefully rubbed with it. After this, new substrate was rubbed with same tip leading to transferring of nanowires to new surface. This technique was found to be optimal for Ge nanowires, while, as we have already said before, optimal technique for GaAs nanowires was sonication.

2.4.c. Lithography

Once nanowires are transferred, additional acetone-isopropanol cleaning step is performed to remove residuals of transferring method, for example particles of dust or remains of isopropanol. After this, pre-defining of contacts can be initiated. Contacts are predefined by means of lithography. It is a process in which local properties of certain materials can be altered by exposing it to light of certain wavelength. Lithography is a standard procedure in modern integrated circuit fabrication and can be divided into different categories depending on the wavelength of the light we use for the exposure. In this thesis we will describe two techniques we used, optical lithography and electron-beam lithography.

2.4.c.1. Optical lithography

Optical lithography (photolithography) is the process of transferring geometric shapes, in our case contacts, from the mask to the surface of a substrate. The steps involved in the photolithographic process are differing depending on final goal. In our case, these are wafer cleaning, photoresist spin-coating, soft baking, mask

alignment, exposure and development. We will first describe each step and then present actual protocols we used.

The cleaning step is similar to the cleaning procedures described in 2.3. a). Cleaning is followed by spin-coating of photoresist. The rotation time and velocity used during the spin-coating process depend on the resist used and the desired thickness of photoresist. There are two types of photoresist: positive and negative. For positive resists, the resist is exposed with UV light wherever the underlying material is to be removed. In these types of resists, exposure to the UV light changes the chemical structure of the resist so that it becomes more soluble in the developer. Exposure is followed by developing in proper solution, leading to areas of the bare underlying material. Because of this, the mask contains an exact copy of the contacts which we want to produce to remain on the wafer. We used positive lithography for Ge nanowires, photoresist type S1818, spinning time 40 s at 4000 rounds per minute, resulting in total thickness of more than 600 nm.

Negative resists show the opposite behavior. Exposure to the UV light results in polymerization making exposed zones of photoresist more difficult to dissolve. Therefore, the negative resist remains on the sample surface wherever it is exposed, developing solution removes photoresist only from non-exposed segments of the surface. Consequence of this is that masks used for negative photoresists contain the inverse of the contacts we want to transfer. The figure 2.15 shows basic differences between positive and negative resist.

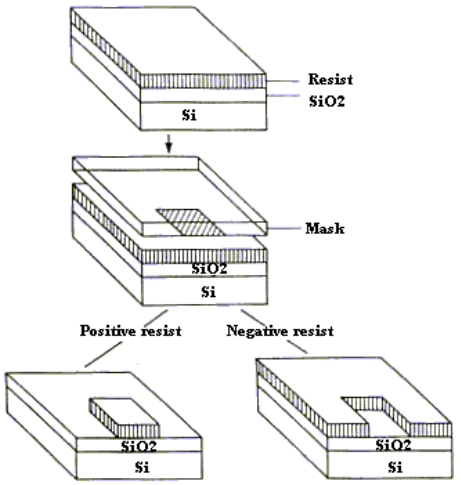


Figure 2.15. Differences between positive and negative photoresist

We should mention a third type of photoresist. This last type is called universal resist, since depending on the exposure and developing conditions it can exhibit properties of both positive and negative photoresist. For contacting GaAs nanowires

we used universal photoresist AZ 5214 in negative mode, spun with 3 steps, 10 s at 1000 round per minute, 20 s at 4000 rounds per minute and finally 8s at 7000 rounds per minute leading to final thickness of more than 400 nm.

The purpose of soft-baking step which follows the spinning is to ensure that most of the solvent evaporates from the coating photoresist. The coated photoresist layer becomes sensitive to UV light only after soft-baking. This step is critical also because too long or too short soft-baking will degrade the photosensitivity of resists, for example by reducing the developer solubility.

One of the most important steps in the photolithography process is the mask alignment. An optical mask itself is a square glass plate with a patterned chromium film on one side. Chromium is used to create alternative transparent and non-transparent zones on the mask. Only certain parts of samples placed under transparent zones of the mask will be exposed. The mask is aligned with the sample, so that the pattern can be transferred to sample surface, in our case so that contacts can be placed on the single nanowire. Once the mask is accurately aligned so that contacts are placed on desired nanowire, the photoresist is exposed through the pattern on the mask with a high intensity ultraviolet light. Out of many different exposure methods, we used so called contact exposure, see figure 2.16.

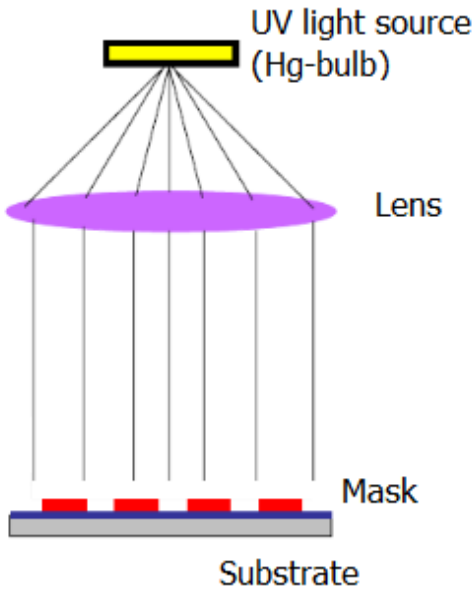


Figure 2.16. Schematics of contact exposure method. Red structures represent non-transparent segments of the optical mask while vacancies between them represent transparent zones.

During procedure of contact exposure, the sample coated with photoresist is brought into the close contact with the mask. The sample is placed on a vacuum chuck, and the system is elevated until the sample and the mask contact each other. The

photoresist is exposed with UV light (mercury lamp) while the wafer is in contact position with the mask. This exposure method enables highest resolution, around 1 μm. However, drawback is possible damage on mask or substrate due to friction.

The last step is the development, where the exposed segments of photoresist for positive and non-exposed segments of photoresists for negative lithography are removed, enabling formation of metallic contacts for future nanowire based devices.

As it has already been pointed out, for Ge nanowires we used positive lithography. We spun S1818 photoresist 40 s at 4000 rounds per minute, obtaining thickness of not less than 600 nm. Samples were soft-baked in oven for 15 min at 90 °C. Exposure is done for 8 s under 18 mW/cm^2 of UV light while development consisted in 40 s long treatment with E-351 developer followed by 5s long flushing with DI-water and nitrogen blow-drying. Figure 2.17 displays the design of masks we used.

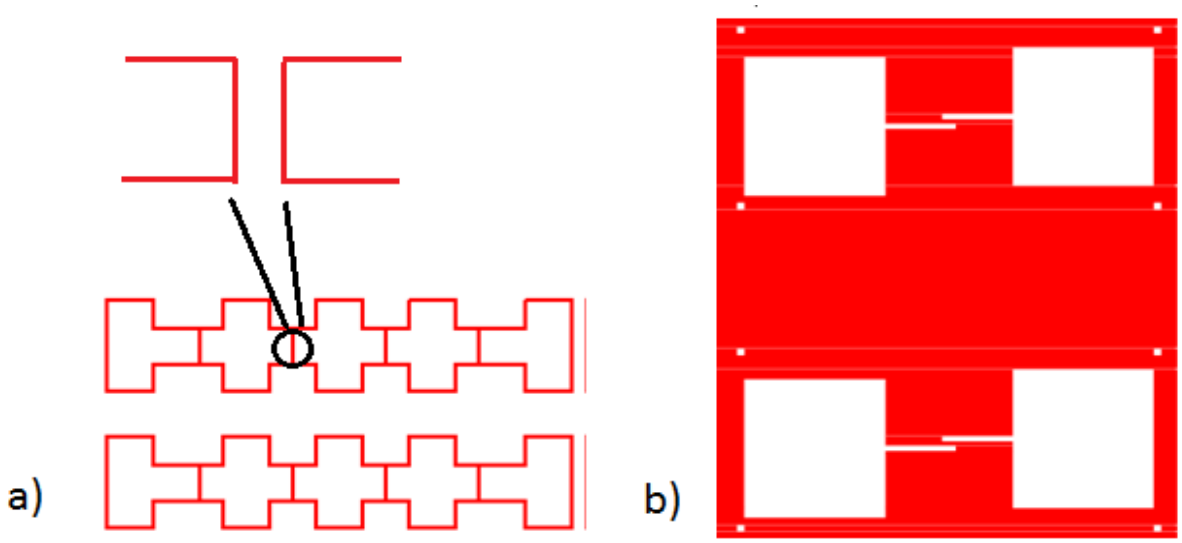


Figure 2.17. Schematics of a) positive nad b) negative mask segments used in optical lithography. Positive mask, used for Ge nanowires, has separations of 1.5 and 5 μm while negative mask, used for GaAs nanowires, has four zones with inter-contact distances of 1.5, 3, 5 and 7 μm respectively. Postive mask is mostly covered by cromium, only seperations between structures are transparent. This is exactly opposite in case of negative mask were everything excpt the structure is positive, resulting in easier and more precise contacting.

The procedure for negative photolithography was slightly different. We used universal photoresist AZ 5214 with protocol resulting in negative process. Spinning was done in 3 steps, 10 s at 1000 rounds per minute, 20 s at 4000 rounds per minute and finally 8s at 7000 rounds per minute leading to final thickness of more than 400 nm. Samples were soft-baked first time on hot-plate for 90 s at 90 °C followed by first exposure for 2s at 18 mW/cm^2 of UV light. After this, we performed additional soft-bake step for 30 s at 130 °C and an additional exposure step, so

called flood exposure, without lithography mask, i.e. the entire sample was exposed for 20 s. Finally, the samples were developed for 45 s in solution prepared of AZ 400K developer diluted with DI-water in ratio 1:5, flushed with DI-water and nitrogen blow-dried.

After lithography and prior to evaporation of metallic contacts, detailed cleaning steps needed to be performed. These are consisted of oxygen plasma etching and hydrofluoric acid (HF) etching. Role of oxygen plasma etching is to remove residuals of photoresist and for optical lithography it is performed for 300 s at 200W. HF etching solution is prepared with HF and water mixed in ratio 1:2. It is used to remove native oxide layer which is forming on nanowire surface. Samples are dipped in etching solution for 4s, flushed with DI-water and loaded into evaporation chamber. Avoiding any of these steps would harm properties of future contact, resulting in increased global resistance and non-reliable data.

2.4.c.2. Electron beam lithography

Many light-based nanotechnology measuring and fabricating tools are limited by the wavelength of light. In general, shorter wavelength of the light used for exposure will lead to higher resolution. One way to obtain shorter wavelengths is to use electrons instead of light. Lithography techniques based on this is called electron beam lithography, usually known as E-beam lithography. Due to the shorter wavelength of electrons under an acceleration voltage of few kV, it is possible to write smaller structures and structure resolution is limited by resolution of the electro-resist and proximity effect. Compared to optical lithography, E-beam allows to place higher number of contacts per nanowire, while contacts itself can be reduced in size and separated for shorter inter-pad distances. Moreover, E-beam enables contacting more than one nanowire per sample.

E-beam lithography requires additional steps, differing from ones used in optical lithography process. Details on E-beam are given in Appendix A, here we are presenting only the key points. Prior to the nanowire transfer, each sample has to be treated with optical pre-step, see Appendix A. Compared to optical lithography, E-beam lithography is a time consuming process. If entire contact from micrometer to nanometer size would be done exclusively by E-beam, the exposure would last hours or days, depending on number of contacted nanowires. Moreover, high precision of E-beam is not required once when contact size is of order of microns. It is because of this why most of the macro-contacts are still done optically, while short and precise final step is performed by means of E-beam lithography. Except reducing the exposure time, another use of optical step is defining markers which will be used for aligning during the process of E-beam lithography. Once when optical pre-step is done, nanowire transfer is performed, followed by spin-coating of electroresist.

Electroresist is a material analogous to photoresist, meaning, it changes its properties when exposed to beam of electrons. We used positive double layer electroresist, PMMA (Polymethyl methacrylate)) 220 k and 950 k, spun at 2000 rounds per minute for 40 s resulting in total thickness of 630 nm (for details, see Appendix A). Spin-coating is followed by soft baking on hot plate for 6 min at 180 °C. After this, samples is imaged by optical microscope, pictures were stored in digital format and mapped with AutoCAD 2006 in order to determine relative position of nanowire with respect to the optical step. The obtained values are scaled to actual sizes and future contacts designed. A more detailed explanation on this can be found in Appendix.

E-beam lithography consists of shooting a narrow, concentrated beam of electrons onto a resist coated substrate. E-beam lithography enables the operator to design and place elements at the scale of up to 5-10 nm. The mask fabrication process is simpler than for photolithography since e-beam masks are so called software masks. Computer-stored pattern, mask, is directly converted to position of the writing electron beam. This enables sequential pattern exposure, meaning, whole wafer can be exposed point by point. Since mask is software-based, it can be easily altered to fit the exact position of specific nanowire, while for optical lithography it is necessary to tilt the sample to fit it under fixed physical mask. E-beam lithography is based on high current density of narrow electron beam. Reducing the size of beam, leads to the better resolution, but also to more time necessary to complete the writing. This type of exposure results in exposing one pattern element at the time, Figure 2.18. Electron beam current has its maximum within area exposed. Basic advantages of E-beam with respect to optical lithography are: higher precision of beam deflection (EM fields instead of classical lenses), no need for physical mask, ability to precisely move across the substrate and write a pattern adopted for specific position of the contact. However, E-beam exhibits certain disadvantages, exposure speed is lower and alignment longer (due to fact that same electron beam is used for exposure and visualization, operator is not allowed to see nanowire meant to be contacted).

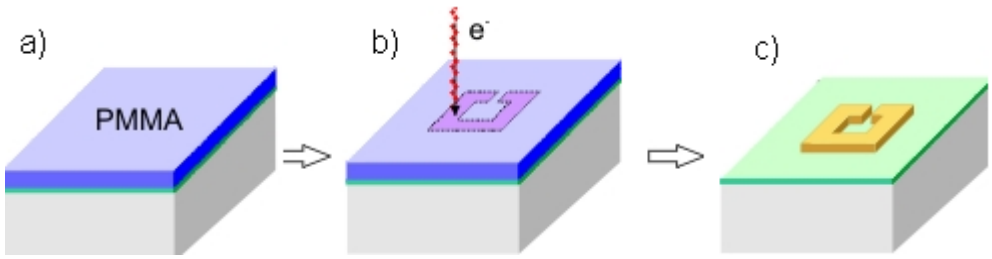


Figure 2.18. Schematics of electron beam lithography: a) electroresist spin-coating, b) exposure and c) development

Once the sample is exposed, it has to be developed. For development we use homemade solution of MBIK (Methyl Isobutyl Ketone) and isopropanol in ratio 1:3. Developing time is 75 s followed by 30 s of flushing with isopropanol and short nitrogen blow-drying. Post-development cleaning steps are similar to the steps for

optical lithography with one exception, shorter O_2 – etching, which, due to higher sensitivity of PMMA to O_2 plasma, is done for 55 s only.

2.4.d. Evaporation

Evaporation is a technique applied to deposit metallic layers after the contacts have been predefined by means of lithography (optical or E-beam). It is done under vacuum conditions (10^{-6} to 10^{-8} mbar) by two basic approaches, electron-beam evaporation and thermal evaporation. In first case, electron beam accelerated by high voltage (order of magnitude 10 kV) is focused on piece of metal to be evaporated. Intensity of beam is gradually increased until metal is heated enough to obtain stable evaporation rate. In case of thermal evaporation, metal is mounted on resistive holder (W, for example) across which current is applied. Joule's dissipation heats the holder and metal peace on it. Again, heating current is gradually increased until stable evaporation rate is achieved. In both cases, sample is covered by shutter until evaporation rate reaches optimal value. During evaporation, thickness of metal layer is measured indirectly on so called x-tal crystal. Once actual thickness is equal to desired, shutter is to be closed and evaporation rate gradually reduced to zero.

Ohmic contacts for GaAs nanowires have been obtained by evaporating Pd/Ti/Pd/Au heterolayers (typical thickness 10nm/40nm/40nm/100nm, respectively). Contrary, for Ge nanowires we realized Ohmic contacts with 3 different heterolayers: Ti/Pd/Au (15 nm/100nm/10nm, respectively) Ti/Bi/Au (15 nm/100 nm/10 nm, respectively) and Ti/Cu (15 nm/155 nm, respectively). Contact nature and related issues will be discussed later in this chapter.

2.4.e. Lift-off

Through evaporation, metal layers are deposited over entire sample surface. The purpose of lift-off is to remove the metal that does not pertain to the contact areas. There are different approaches, mainly depending on size of desired structures. The procedure which we found to be optimal is based on 5 to 10 min long acetone treatment at room temperature, followed by a short isopropanol dip and finally, nitrogen blow-drying. Once when metal layers are peeled away, the sample is rinsed in isopropanol for 10 s and dried. In the case of E-beam lithography, the best results are achieved after treatment in ~60 °C acetone for 5-10 min. Isopropanol and drying step are the same as for optical lithography. However, in cases where the metal layers are hard to remove, the samples are placed in acetone shortly in an

ultrasonic bath. This step is very delicate since too short ultrasonic treatment will not remove metals while too long step in general leads to breaking of the nanowires. Once lift-off is realized, the samples are inspected with the optical microscope and placed in the measurement set up.

Due to sake of clarity, all basic steps in lithography process are schematically displayed in figure 2. 19.

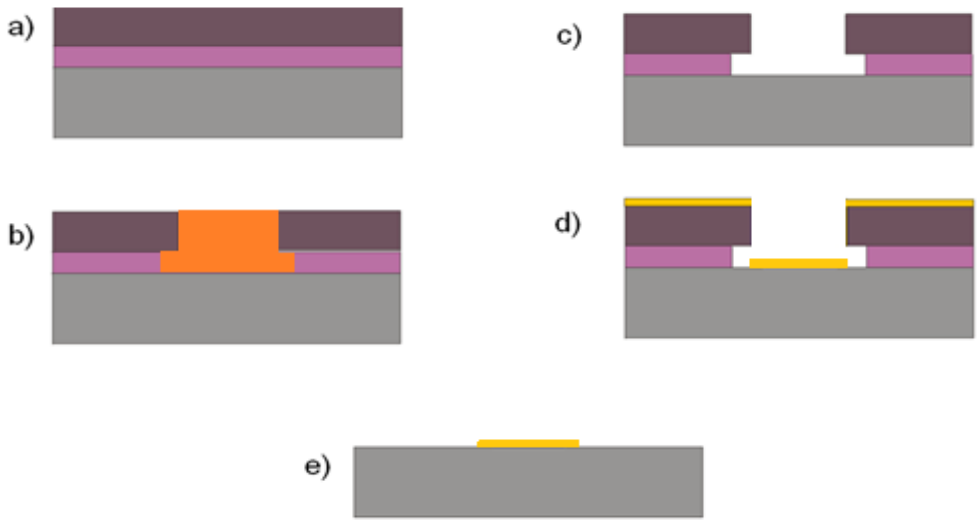
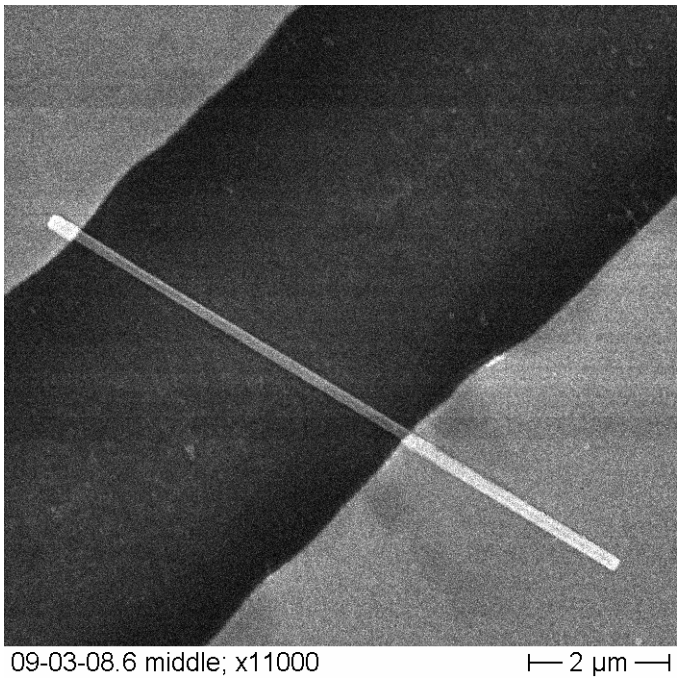


Figure 2.19. Schematics representation of lithography process: a) spin-coating of photoresist for optical or electroresist for E-beam lithography, b) mask exposure, c) development, d) deposition of metal layers (evaporation) and e) lift-off.

Typical example of nanowires contacted with optical and E-beam lithography is given in figure 2.20.

a)



b)

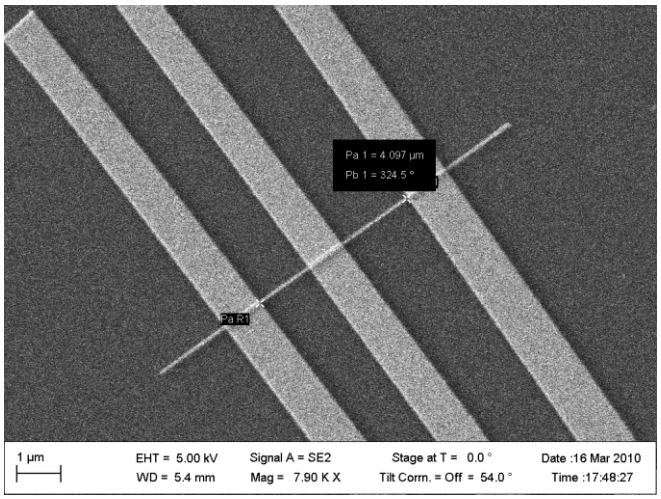


Figure 2.20. SEM micrograph of a) optically and b) E-beam contacted nanowire

2.5. Metal-semiconductor contacts

Metal semiconductor contacts are an issue of major importance in the area of semiconductor device physics. Thanks to the contacts, the electrical properties of the semiconductors can be obtained and/or a device operated. The behavior of the contact is determined by the characteristics of the interface and can be mainly divided in two types, Schottky contact and Ohmic contact. An ideal Ohmic contact would supply the required current with a negligible voltage drop at the interface. In this subchapter we will present the basics of the energy band profiles in the immediate vicinity of the metal-semiconductor junction and present expressions for the current in case of the thermionic emission and quantum mechanical tunneling for given drain to source voltage. Moreover, we will present an equivalent circuit for the junction. More details on this topic can be found in.[41,42] Finally, we will describe actual experimental challenges related to obtaining Ohmic contacts with p-doped GaAs nanowires as a necessary pre-condition for studying the electrical properties.

2.5.a. Theoretical background

We will start this section by discussing metal and semiconductor separated by a distance large enough to prevent the influence of one material to another. A metal is material whose conduction and valence bands are overlapping. As a consequence of this, the Fermi level ends up within an allowed band (Figure 2.21a.) This leads to high electron density at the Fermi level and high concentration of free electrons for the current to flow. Number of these electrons depends on type of metal and temperature. An electron not being bound to an element is said to be at the vacuum level and corresponding electron energy is zero. On the other side, bound electrons have negative energies. In order to release electrons from a metal one must add energy equal to $e\Phi_m$, where Φ_m stands for metal work function (specific for each metal), see Figure 2.21.

Electrons in semiconductors require additional energy in order to be emitted. However, except for heavily doped semiconductors, its Fermi level is normally placed within the forbidden energy zone (commonly known as band gap). It is because of this that the required energy to release electron $e\chi_s$ is measured from the top of the conduction band (Figure 2.21). The value χ_s is called electron affinity and, like Fermi level, it is also specific for each material. Analogous to the metals, a certain amount of free carriers will also exist in the semiconductor. Assuming p-type semiconductor, there will be certain number of majority carriers (holes) within the valence band, depending on temperature and doping concentration. Table 2.1. gives an overview of work functions for some metals and electron affinities of some semiconductors.[43]

Element	Work function, Φ_m(V)
Ag	4.26
Al	4.28
Au	5.1
Cr	4.5
Mo	4.6
Ni	5.15
Pd	5.12
Pt	5.65
Ti	4.33

Element	Electron affinity, χ_s(V)
Ge	4.13
Si	4.01
GaAs	4.07

Table 2.1. overview of work functions for some metals and electron affinities of some semiconductors. Data is taken from [43].

Since semiconductor can be both p or n doped, and it can have higher or lower work function with respect to metal, there are totally 4 cases to discuss. However, we will limit ourselves to p-doped semiconductor since our nanowires are found to exhibit p-type behavior.

Let us assume a semiconductor with work function higher than work function of the metal (Figure 2.21 a). If we put the metal and the semiconductor into the close contact, the holes from the semiconductor will diffuse into the metal. Since holes are depleted from the semiconductor, a negative charge zone is created in the semiconductor at the junction. This negative charge will lead to formation of an electric field opposing the diffusion current. Equilibrium conditions are achieved when these two phenomena cancel. As a consequence, the semiconductor energy bands are bending.

The negative charge region in the semiconductor is called depletion region. The amount of band bending is described via so-called built-in potential, V_{bi}.

The holes crossing from the semiconductor to the metal must overcome V_{bi}. However, a carrier crossing from metal to semiconductor must overcome barrier of $e\Phi_b$. Described processes and concepts are depicted in Figure 2.21 b.

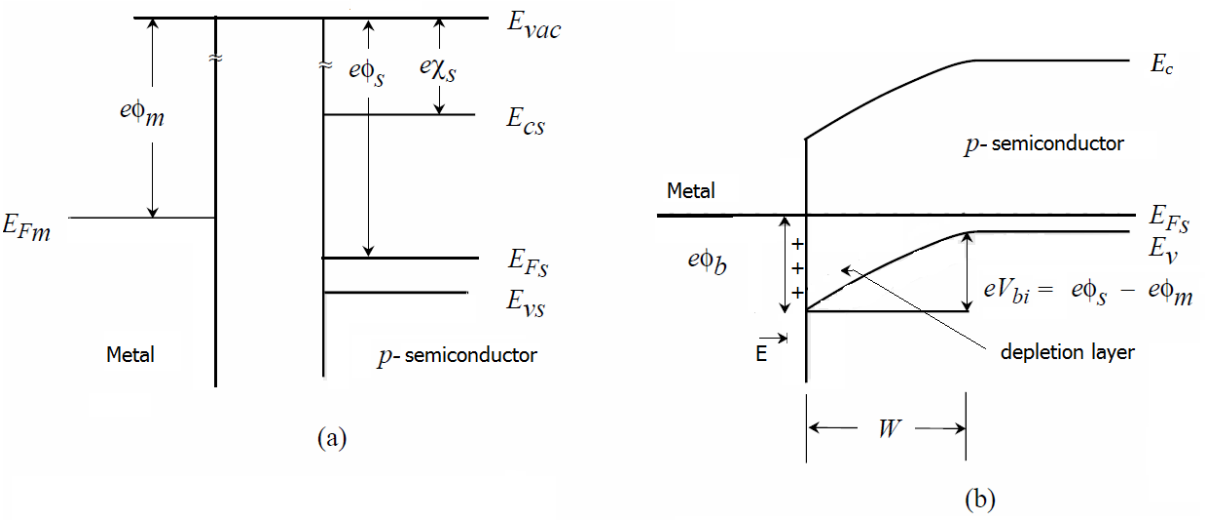


Figure 2.21. Successive stages in the establishment of equilibrium between metal having smaller work function and p-type semiconductor. a) shows band diagrams prior and b) after bringing metal and semiconductor into immediate vicinity. Vector quantity $\vec{E}$ stands for electric field, while scalar quantity E stands for corresponding energies. Figure is addopted from [43].

For a p-type semiconductor with a work function higher than work function of metal (depicted in Figure 2.21), barrier height is given by $e(\Phi_s - \Phi_m)$. In case of semiconductor work function being equal metal work function, $e(\Phi_s - \Phi_m) = 0$, barrier will not exist.

As we have already pointed out, for the thermal equilibrium conditions, Figures 2.21 b) and 2.22 a), bands are bent in depletion layer of semiconductor by an amount equal to the difference of semiconductor and metal Fermi levels. This bending represents the built-in voltage in semiconductor, $eV_{bi} = e(\Phi_s - \Phi_m)$.

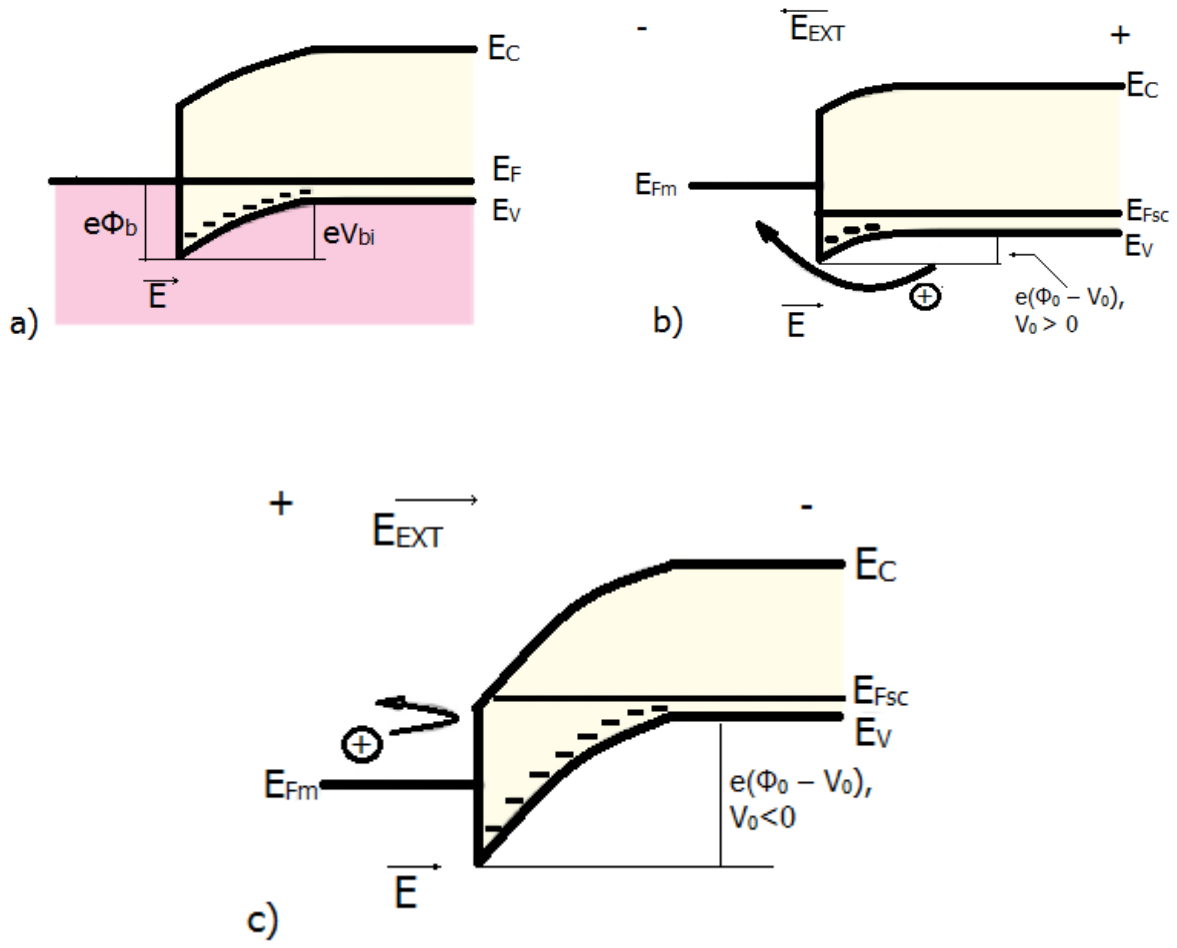


Figure 2.22. a) Zero external bias conditions, b) forward and c) reverse external bias applied over metal-semiconductor (p-type) junction.

However, inside the metal there is no important change in band diagram, since electric filed penetration depth is limited to few atomic distances [42]. Hence, the energy barrier on metal side is given by $e\Phi_b = e(\Phi_m - \chi_s)$ and it does not depend on doping in the semiconductor or applied voltage [42].

Figure 2.22 gives an overview of the possible situations when an external bias is applied to a metal-semiconductor junction. The equilibrium barrier height in depletion layer of semiconductor is given by $e(\Phi_s - \Phi_m) = e\Phi_0$. If an external potential is applied across the junction, the added electric field will disturb the thermal equilibrium conditions, Figure 2.22. Barrier height on the semiconductor side will be altered to a new value given by $e(\Phi_0 - V_0)$, where V_0 stands for applied bias.

We will first take into the consideration a positive external potential ($V_0>0$), meaning a positive bias is applied on p-type semiconductor and a negative on the metal (Figure 2.22 b)). This external bias will result in the electric field across the junction with the orientation opposite to the electric field caused by the depleted semiconductor layer, see Figure 2.21 b). At $V_0>0$ the barrier height on the semiconductor side, $e(\Phi_0 - V_0)$, will be lower than equilibrium barrier height $e\Phi_0$. As

a consequence of this reduction in the barrier, assuming the barrier is smaller than kT, a larger quantity of holes will overcome the barrier and flow from the semiconductor to the metal. However, the barrier on the metal side, $e\Phi_b$, is not influenced by applied bias. The number of carriers which can overcome the barrier and flow from metal to semiconductor is exactly same as in equilibrium conditions. Still, this number is negligible compared to number of holes overcoming the barrier on semiconductor side, resulting in dominant current being based on stream of holes from the semiconductor to the metal.

However, if a negative voltage is applied to the p-type semiconductor and positive to metal, the external field is added to the electric field caused by the depleted charge zone. As a consequence, the band bending at the junction increases, see Figure 2.22 c). The barrier height on the semiconductor size, $e(\Phi_0 - V_0)$, will be higher than equilibrium barrier height $e\Phi_0$ (V_0=0), preventing flow of holes from semiconductor.

On the other hand, the barrier in the metal ($e\Phi_b$) does not change with external bias. This means that a small amount of holes can tunnel through the barrier and appear in the p-type semiconductor creating a reverse-bias current of metal-semiconductor junction. If reverse bias is further increased, the barrier on the semiconductor side will become even higher, but at the same time the barrier width reduces, enabling increased tunneling of holes to semiconductor. This will result in an increase in reverse bias current.

Under abrupt barrier approximations [42], which are valid for junctions between metals and semiconductors [44], the barrier width W (see Figure 2.21 b)) is given by:

$$W = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{eN_d}\left(V_{bi} - V_0 - \frac{kT}{e}\right)} \qquad (2.1)$$

where N_d is the doping concentration, k is Boltzmann's constant, and e is the elementary charge (1.6 x 10^{-19}C) [42]. The term kT/e, called thermal voltage V_T, is approximately 26 mV at 300 K (room temperature) and can often be neglected due to fact that V_{bi} and V are a few volts. From equation (2.1), one can conclude that the depletion width becomes smaller for the highly doped semiconductors. It is clear that a positive bias increases current flow and decreases the depletion width while the opposite occurs for a negative bias. For small enough bias (and high enough doping)small, tunneling can occur and results in an increase of current due to reduced depletion width.

In next paragraph we are shortly discussing influence of doping. We will consider two typical values of doping concentrations, N_d = 10^{17} cm^{-3} (observed in nominally undoped GaAs nanowires) and 10^{19} cm^{-3} (observed in GaAs nanowires doped with 13 A current heating Si source). The depletion widths for these two doping concentrations when no external bias is applied would be around 48 nm and 8 nm, respectively.

An additional relevant parameter regarding the metal-semiconductor contact is the electric field across the depletion region. One should pay special attention to keep the maximum electric field smaller than the breakdown field, 4 x 10^5 V/cm for GaAs . If the applied field reaches a value higher than the breakdown field, charge carriers will have enough kinetic energy to create electron/hole pairs during electron/atom collisions at a faster rate than the free charges can recombine [42]. New carriers are accelerated by the electric field and create more electron/hole pairs. This process is known as avalanche breakdown and it is used in various devices, like particle detectors and avalanche photodiodes. Avalanche breakdown is obviously a non-desirable side effect in our proposed device and should be avoided to ensure normal device operation.

In the following lines we will derive an expression for the electric field for a metal-semiconductor junction. The details of this calculus in case of a general pn junction can be found in [45], here we present the solution adopted for metal-semiconductor junction.

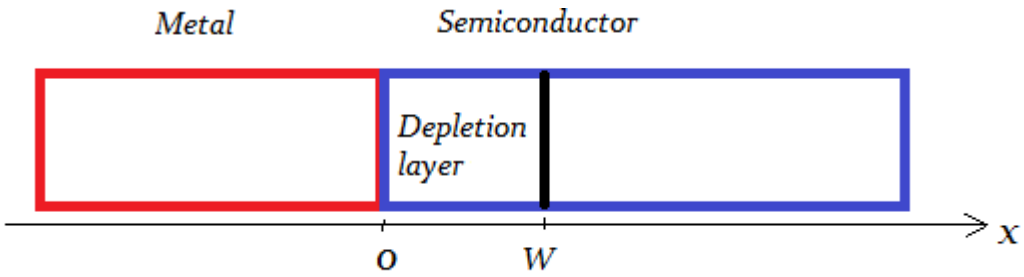


Figure 2.23 Simplified model of metal semiconductor junction (for derivation of the maximal electric field across the junction)

An expression for field is derived from Poisson equation

$$\Delta\varphi = -\rho/\varepsilon \qquad (2.2)$$

were φ, ρ *and* ε stand for electric potential, volume charge density and dielectric constant, respectively. Assuming infinitely long y and z dimensions (Figure 2.23), the geometry becomes one dimensional and the Poisson equation can be expressed in a simpler way where Laplace operator becomes second order differential:

$$\frac{d^2\varphi}{dx^2} = -\rho/\varepsilon \qquad (2.3)$$

We can consider 3 different regions in terms of charge:

1. For x < 0, we are in metal region, away from the metal-semiconductor junction. Volume charge density in this region is 0.
2. For $0 \leq x < W$, we are in depletion region. In this region, negative ions are only charge centers. To obtain volume charge density, we have to multiply elementary charge with number of ions. There are N ions per cubic centimeter, each one carrying charge of –e. Therefore, volume charge density is given by ρ = -eN.
3. For $x \geq W$, we are in electroneutral p-region in which acceptor ions are compensated by the holes. Total volume charge density is again 0.

These conclusions are summarized in equation (2.4).

$$\frac{d^2\varphi}{dx^2} = \begin{cases} 0, & \text{for } x < 0 \\ \frac{eN}{\varepsilon}, & \text{for } 0 \leq x < W \\ 0, & \text{for } x \geq W \end{cases} \qquad (2.4)$$

Since the value of the electric filed E is given by $-d\varphi$/dx, the electrical field is obtained integrating equation (2.4). When the field is differing from zero, the existing charge carriers would be moved by the field producing an electric current. As we already pointed out, there should be no current in equilibrium state. Therefore, total field should be zero.

Strictly speaking, if the second derivative is equal to zero, first derivative should be constant, but not necessarily zero. Due to this, for x < 0 and for $x \geq W$ electrical field should be equal to C_1 and C_3, where C_1 and C_3 are the integration constants. For $0 \leq x < W$ integral (electric field) is equal to $\frac{eNx}{\varepsilon}$+C_2. However, as we have already stated, for x < 0 and for $x \geq W$ total volume charge density is zero, which means electric field should also be zero ($C_1 = C_3 = 0$). In order to fulfill equilibrium condition for total filed being zero, for $0 \leq x < W$ we must have $C_2 = -\frac{eNx}{\varepsilon}$. These conclusions are summarized in equation (2.5).

$$E(x) = \begin{cases} 0, & for\ x < 0 \\ \frac{-eN(x-W)}{\varepsilon}, & \text{for } 0 \leq x < W \\ 0, & for\ x \geq W \end{cases} \qquad (2.5)$$

Deriving this expression and making first derivative equal to zero, we obtain maximal electric field for depletion region:

$$E_m = \frac{eN}{\varepsilon_0 \varepsilon_r} W \qquad (2.6)$$

Combining equations (2.1) and (2.6) we conclude that E_m is higher for more doped semiconductors and for high reverse bias (see eq. (2.1)).

Finally, we will consider the junction capacitance which is a consequence of charge storage inside of the depletion region. Capacitance scaled per surface is given by [42]:

$$C_J = \frac{\varepsilon_0 \varepsilon_r}{W}. \qquad (2.7)$$

From (2.7) it is clear that capacitance per surface depends on applied voltage and doping concentration, since W depends on both of these values. This makes the metal-semiconductor junction a very good candidate for numerous devices where voltage-controlled capacitance is used, such as varactor diodes, phase shifters and oscillators [42]. In general, current flow through the junction is due to two mechanisms, namely the thermionic emission and the quantum mechanical tunneling [41]. Thermionic emission is transport of the charge carriers over the potential barrier. It is assumed that only carriers with energies greater than the energy of the potential barrier add to the current flow. This process is dominant for moderate doping levels and/or moderately high temperatures [42]. Current density can be determined by [41]:

$$J = J_0 \, e^{-q\Phi_b/kT} \left(e^{qV/nkT} - 1\right) \qquad (2.8)$$

J_0 increases with the doping concentration N_d and temperature, while dimensionless factor n depends on quality of diode. An ideal diode would have n equal to unity but for actual diodes it is higher. Specific contact resistance for thermionic emission can be derived from (2.8) and the obtained relation for $V_{ds} = 0$ is [41]:

$$R_C = \frac{k}{qAT} \, e^{q\Phi_b/kT}, \qquad (2.9)$$

where A denotes Richardson constant, 120 $\frac{m^*}{m_0}$ A/cm^{2}K^2. Here, m_0 represents electron rest mass (9.1 x 10^{-31} kg) while m^* stands for effective mass.

The second mechanism, quantum-mechanical tunneling, is dominant in case of highly doped semiconductors or in case of extremely high reverse bias. If the potential barrier is thin enough (see Figure 2.24), there is a non-zero probability that some carriers will travel through the barrier [42]. This current component is called tunneling current and it is proportional to exponential factor, as given by (2.10) [41]:

$$J \propto e^{\left(\frac{4k}{h}\sqrt{\varepsilon_0 \varepsilon_r m^*}\frac{\Phi_b}{\sqrt{N_d}}\right)} \tag{2.10}$$

Tunneling current can be dominant in the transport for concentrations above 10^{17} cm^{-3} and for low temperatures. The corresponding specific contact resistance for V_{ds} = 0 can be described as [41]:

$$R_C \propto e^{\frac{2}{\hbar}\sqrt{\varepsilon_0 \varepsilon_r m^*}\frac{\Phi_b}{\sqrt{N_d}}} \tag{2.11}$$

Equation (2.11) shows that increased doping in immediate vicinity of contact would lead to reduced specific contact resistance.

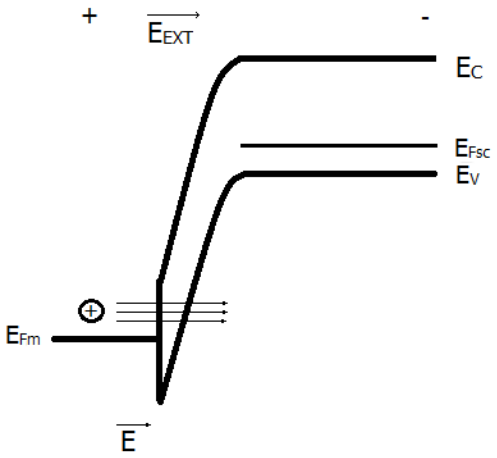


Figure 2.24. Junction between metal and p-type semiconductor in case of high reverse bias

2.5.b. Experimental challenges

We will start this section by presenting an electrical equivalent circuit of metal-semiconductor junction.

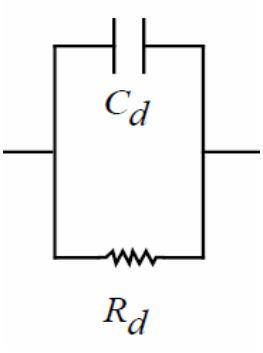


Figure 2.25. Equivalent circuit of metal-semiconductor junction

The meaning of concentrated elements in Figure 2.25 is following: C_d stands for capacitance of metal-semiconductor junction, while R_d stands for metal-semiconductor junction resistance.

In order to decrease the contact resistance one has to increase the doping concentration and/or lower the barrier height. In practical terms, since a well fabricated contact should exhibit much lower voltage drop than device body (semiconductor nanowire), influence of the resistor R_d should be reduced.

Devices described in this thesis were based on GaAs and Ge nanowires. These nanowires were grown under different doping conditions, from nominally undoped to highly doped nanowires. However, once a nanowire is grown and contacted, the only possible method to increase the concentration of the dopants in immediate vicinity of contact and by that extent the contact resistance is annealing. But, as it can be derived from equation (2.7), increasing the doping will increase C_d. Still, due to fact that capacitor represents high pass filter, DC current induced by applied DC bias will "see" the capacitor as a resistor with huge resistance R_{cap}. In the first approximation, R_c can be treated as open circuit. As a consequence of $R_d \ll R_{cap}$, the current is flowing through R_d and we can neglect the capacitor.

In the case of Pd-based GaAs nanowire contacts and Au, In, Bi and Al-based contacts for Ge nanowires, this method showed no improvements, see Chapters 3 and 5. The next available method is to reduce the barrier by choosing the contacting metal with the most suitable work function. In following text we will provide an experimental solution for achieving the Ohmic contacts in case of GaAs nanowires. A similar reasoning can be applied to Ge nanowires.

The initial point in contacting GaAs nanowires was standard Ti/Au heterolayer with thicknesses of 10 nm and 150 nm, respectively. Since we did not know if GaAs nanowires would exhibit p or n behavior, we chose this material system due to its favorable properties in terms of a contacting process. Titanium is well known as material with good adhesion properties, making a lift-off process much easier. Gold is a noble metal, it does not oxidize and it is resistive to all acids, except mixture of HCl and HNO_3 in ratio 3:1. 14 carat gold is stable in dry air only, while 18 carat one is stable even in humid atmosphere. Moreover, if thick enough, gold is easy to solder.[46] As it will be discussed in Chapters 3 and 4, our GaAs nanowires proved to be p-type. This is why the Ti/Au heterolayer did not result in Ohmic contact, as it is reported by the blue curve in Figure 2.26. We can observe a clear non-linearity originating from offset in work function of gold (at 5.1 V) and electron affinity of GaAs (4.07 V). Clearly, an alternative contacting film needed to be found in order to reduce contact influence. Furthermore, contacts needed to be resistive to oxidation and adhesive enough to enable successful lift-off procedures. After studying possible solutions in literature [47], we tried with a novel material system: Pd/Ti/Pd/Au (10 nm/40 nm/40 nm/100 nm, respectively) heterolayer. Obtained results are reported by the red curve in Figure 2.26.

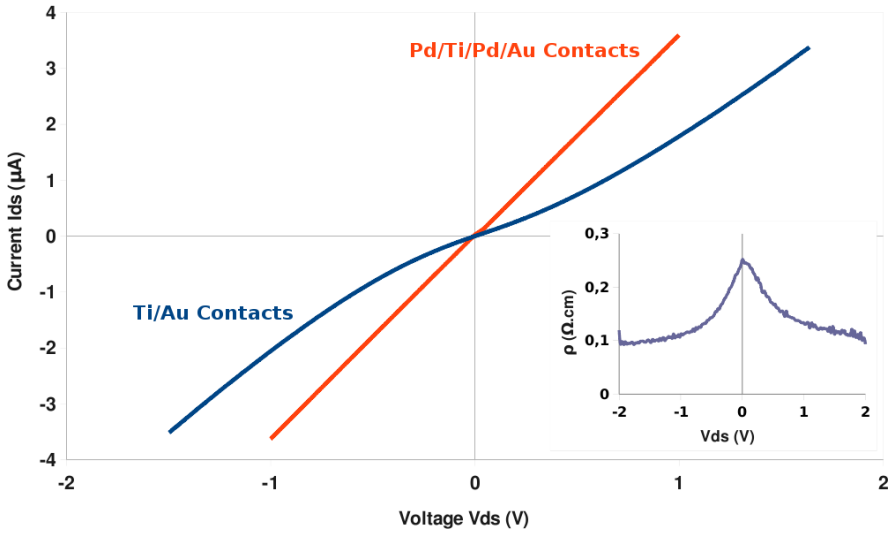


Figure 2.26. Comparison between Schottky (blue line) and Ohmic contact (red line). Inset shows nanowire resistivity vs V_{ds} with Ti/Au contacting heterolayer.

Comparing Ti/Au-based contacts (blue curve) to Pd/Ti/Pd/Au-based(red curve)contacts, one can see clear improvement in terms of not only linearity but also overall resistance. Reported results mean we successfully reduced the barrier width. Moreover, reduced overall resistance implies reduction in R_d.

The actual physics of this particular contact is not well understood. However, it is believed that some Pd diffusion through native GaAs oxide layer occurs and reacts with the GaAs. This leads to the creation of As and Ga-rich compounds and, as a consequence of that, reduction in barrier width. [47] The Ti layer serves as a shield preventing the diffusion of As out of the nanowire.[47] Since we did not apply an annealing technique, future investigations should reveal more details regarding the possible role of the Pd diffusion.

2.6. Transport setup. Electrical measurements

The electrical measurements performed during this work are based on testing device with a probe station, see Figure 2.28. Two or more needles are connected on each pad of the device while the sample is lying on an electrical floating copper plate connected to an additional needle. This plate is providing the backgate contact. We did standard transport characterization, where bias was sourced and current measured (Figure 2.27), both in 2-point and 4-point measurements.

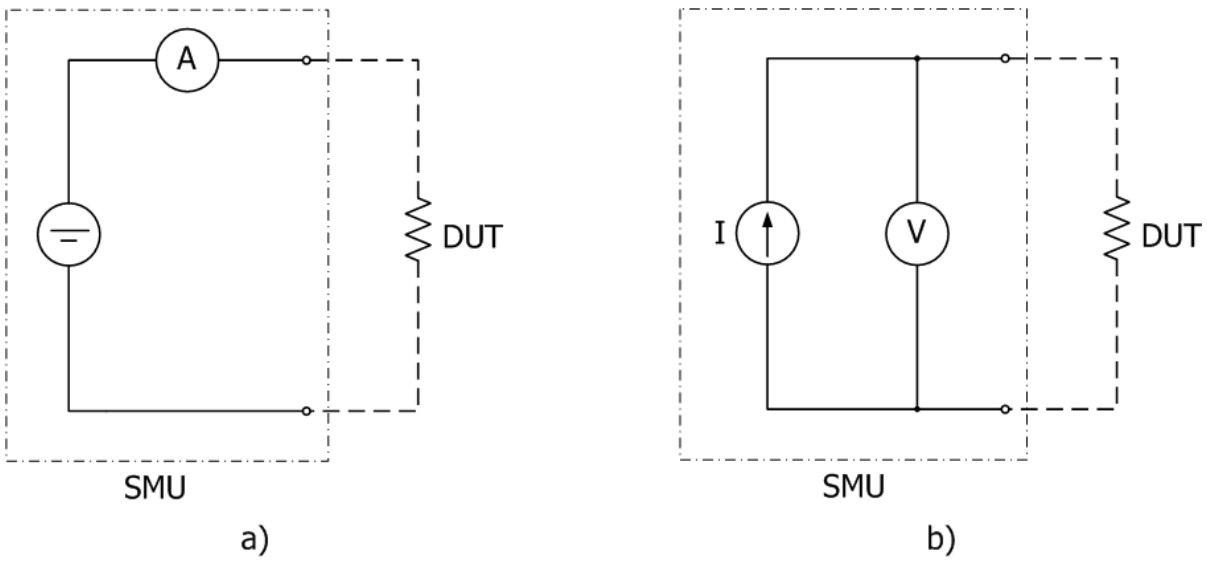
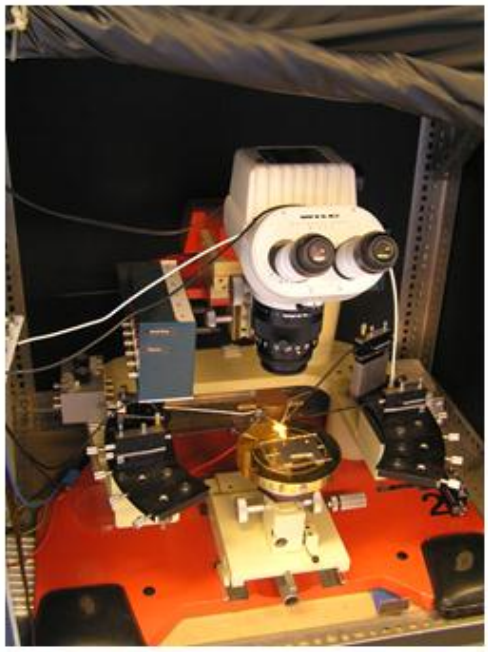


Figure 2.27. Simplified schematics of a source-measure unit (SMU) configured to: a) source voltage and measure current and b) source current and measure voltage. Transport measurements described in this thesis are performed in a) configuration. DUT stands for device under test.

No matter which measurements configuration was used, attention was paid to reduce the noise. Cabling was mostly done by standard 50 Ω BNC coaxial lines short enough to avoid formation of the loops. Chassis of all measuring devices was connected to power grid ground while additional flat copper line was placed in immediate vicinity of setup providing low resistance ground point for metal parts of probe station. For more delicate measurements, additional arm bracelets connected to power outlet ground via high resistive cables were used to discharge the body of setup operator.

In the case of 2-point configuration, voltage bias and current measurements on these connections are performed with two Keithley measuring devices (Source Meter model 2611 for drain- source voltage application and current measurements and Voltage Source model 6487 for gate voltage). Both instruments are linked together and communication with computer is established via LabVIEW programs realized by Dr. Joseph Dufouleur. Two kinds of measurements were performed: drain-source current (I_{ds}) versus drain-source voltage (V_{ds}) with different gate-source voltage (V_g) and drain-source current (I_{ds}) versus gate-source voltage (V_g) with different drain-source voltage (V_{ds}). V_{ds} typically sweeps from -0.1V to 0.1V or -0.5 to 0.5V while V_g is typically changed from -10V to 10V (for a 50 nm thick SiO_2 layer). These measurements provided raw data regarding the linearity of the contact and resistance of the nanowire. Moreover, we extracted approximated values of resistivity and gained an idea on the type of doping. Usually, V_g sweeps from the same ranges as before, when V_{ds} is kept constant typically to 0.1V or 0.3V. Mentioned values for applied bias are obtained after initial measurements and are found to be suitable for most of measured nanowires.

In the case of linear I-V characteristics, the bias interval was increased or decreased depending on the typical value of the nanowire resistance. For nanowires with the lower resistance (eg. 13 A doped GaAs nanowires), we used shorter V_{ds} intervals (eg. -0.1V to 0.1V) in order to avoid too large current densities and heating (Chapter 3). However, in the case of more resistive nanowires (eg. Ge nanowires), we applied higher bias to obtain optimal current readings without damaging samples.



a)

b)

Figure 2.28. Photo of the a) 4-point probe station and b) measuring instruments used for electrical transport measurements.

For samples exhibiting non-linear 2-point I-V curves, we applied higher V_{ds} to extract nanowire resistance while lower V_{ds} was used to obtain total resistance, including contact resistance (see Chapters 3 and 4).

This experimental procedure enables the calculation of the transconductance, from which we evaluate the mobility and then carrier concentration. Special attention was paid to ensure no leakage through backgate occurred. All mentioned measurements are performed at room temperature, if necessary also in dark to avoid the influence of carriers induced by photon excitations.

All parameters used for 2-point measurements were applied in case of 4-point measurements. We should point out that bias was applied between outer contacts while additional high input impedance multimeter was used to measure voltage drop between inner contacts, see Chapter 3. Basic advantage of this measuring configuration is possibility to quantify the contact resistance and separate it from nanowire resistance, see Figure 2.29.

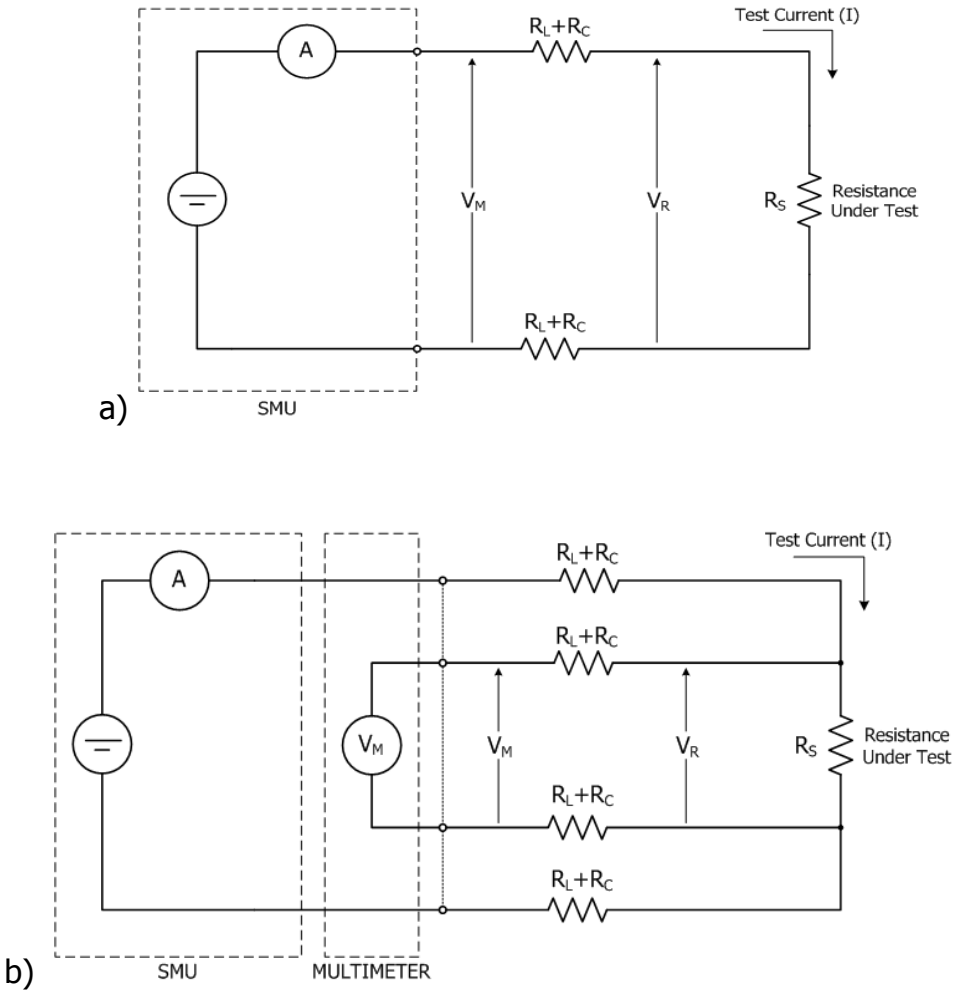


Figure 2.29. Difference between a) 2-point and b) 4-point transport measurements in case of SMU configured for applying voltage and measuring current

As it can be seen on Figure 2.29 a), in case of 2-point measurements test current goes through the resistance under test (nanowire) but also through resistor representing the test leads and the contact, in our case metal-semiconductor junction. This is why voltage drop V_M consists of voltage drop across the nanowire, V_R, increased by voltage drop across the contact and across the test lead. The resistance of the test lead can be neglected with respect to nanowire resistance. However, influence of contact resistance in general case cannot be neglected. Analyzing schematics for 4-point measurements and assuming non-diffusive metal-nanowire contacts, one sees clear improvement. The test current still flows through the test leads, contacts (metal-semiconductor junction) and nanowire itself, but voltage drop is measured only across the nanowire. Since input impedance of voltmeter (multimeter in voltmeter mode) V_M has value of TΩs, only negligible part of the test current flows through inner leads. Assuming this current is zero, there is no voltage drop across the contact or inner test leads, and measured voltage drop V_M is equal to voltage drop on "pure" nanowire, V_R.

However, we were faced with additional challenges. When measuring in 4-point mode, GaAs nanowires were sometimes destroyed due to charging effects. In order

to prevent this, further setup modifications were performed. Prior to placing measuring needles to contact pads, the core and shield of each coaxial line were shortcut and connected to low resistance ground point. Once the needles were placed to the measuring pads, the core and shield were disconnected. This approach proved to be optimal in terms of protecting nanowires from charging effects, while at the same time this method showed no side effects harming the nanowire properties.

2.7. Conclusion

We have defined concept of nanowire and described growth techniques we applied in obtaining different types of nanowires. We presented Molecular Beam Epitaxy (MBE) technique, used for growth of catalyst free GaAs nanowires. Moreover, a description of Chemical Vapor Deposition (CVD) technique, used for Ge nanowires is presented as well. Since we grew Ge nanowires with different catalyst materials, we provided comparison regarding the growth theory. Furthermore, we described experimental procedures used to produce nanowire based devices. Special attention was paid to stress experimental challenges we have been faced as well solutions we derived. Finally, we presented characterization techniques, namely electrical transport measurements.

3. Electrical properties of GaAs nanowires

3.1. Introduction

The goal of this chapter is to provide and understanding of the electrical properties of GaAs nanowires as well as the complete picture of the doping mechanisms. To do that, we will answer the following questions, related to the issues we were dealing with:

- How can we ensure reproducibility and reliability of electrical measurements performed on nanowires?
- Is it possible to dope semiconductor the nanowire?
- How is that influencing its transport properties?
- Can doping be controlled in a reproducible way?

Sample fabrication, experimental set up design and analyses (measurements and calculations) have been performed enabling gathering of sufficient data to derive sustainable conclusions and answer these questions. Although some of the doping related questions have already been mentioned (Chapter 2), doping mechanism issues remained unclear. Challenges we have been faced with regarding the measurements reproducibility will be explained. Moreover, electrical properties analyses performed on nanowires with different nominal doping will be presented and obtained values of resistivity, mobility and carrier concentration compared. This will provide basis for conclusions regarding doping effectiveness and influence on transport properties. Finally, we will show that, when investigated with proper techniques, nanowires show high reproducibility of electrical properties, indicating possibility to effectively control the doping process.

3.2. Experimental results

3.2.a. Methodology

The electrical properties of GaAs nanowires were investigated. We were using wide range of different nanowires, from nominally undoped nanowires exhibiting almost ideal insulating properties to highly doped nanowires, exhibiting quasi-metallic nature. Details on growth conditions as well as doping characteristics are discussed

in the previous chapter and will be shortly repeated later. Prior to characterization, samples were fabricated, as described in Chapter 2. We had to transfer nanowires from the original growing substrate to a new one. For this purpose, we used highly n-doped silicon coated with 50nm - 1µm silicon dioxide. As we will explain later, this will play role in effectiveness of backgate in terms of both response and leakage. After transfering nanowires, contacts were pre-defined by means of lithography (both optical and electron-beam), samples were developed and necessary cleaning steps performed. As pointed out in Chapter 2, cleaning consists of O_2- plasma etching and hydrofluoric acid etching. Role of the cleaning is vital for the quality of the contact. Once cleaning is done, contacts were deposited by standard evaporation, metals were lifted-off and samples were ready for electrical characterization. In order to characterize these nanowires and understand their electrical properties, we performed both two- and four-point transport measurements, combining advantages of each method. Basic advantage of two-point measurements is simplicity of sample fabrication. The major problem is that this did not enable us to obtain the contact resistance. Four-point measurements are more challenging. However, in 4 points configuration it is possible to deduce the intrinsic resistance of the nanowire. Additionally, as we will point out later, the measurements tend to be more reproducible. To have better understanding of doping nature, we combined transport measurements with Raman spectroscopy on same nanowires. Raman spectroscopy provided information regarding the type of doping and also about the existence and relative concentration of impurities, allowing us to understand better the doping mechanism itself, and solve the issue of rather puzzling results obtained with two-point transport measurements.

3.2.b. Sample overview

Four different types of GaAs nanowires were analyzed. The growth model is explained in Chapter 2, here we just stress key elements, namely ones which are crucial for complete understanding the rest of this Chapter. GaAs nanowires characterized in this thesis are grown via Molecular Beam Epitaxy (MBE) technique, avoiding the use of gold as a catalyst. A Ga droplet behaves as a catalyst. [17] The key parameters for this Ga-assisted growth of GaAs nanowires are arsenic pressure, gallium rate and temperature. Additional information can be found in [17]. We made difference between two growth modes, High Beam Flux (HBF) corresponding to As pressure of $2x10^{-6}$ mbar and Low Beam Flux (LBF) and corresponding to As pressure of $7x10^{-7}$ mbar. Nanowires with higher arsenic beam flux grow faster, around 0.25 Å/s, while typical rate for low As beam flux can be as low as 0.1 Å/s.

Growth name	Average nanowire length (μm)	Description	Type of transfer substrate
02-08-08.1	≥ 10	Doped, 13 A, HBF	Doped Si, 50 nm of SiO_2
03-13-08.2	3.8	Undoped, HBF	Doped Si, 1 μm of SiO_2
04-11-08.1	4.2	Doped, 10 A, HBF	Doped Si, 50 nm of SiO_2
04-20-08.1	7.4	Doped, 11.5 A, HBF	Doped Si, 50 nm of SiO_2
02-15-08.1	5.5	Doped, 13 A, LBF	Doped Si, 50 nm of SiO_2
02-05-08.1	5.1	Doped, 11.5 A, LBF	Doped Si, 50 nm of SiO_2
02-03-08.2	4.7	Doped, 10 A, LBF	Doped Si, 50 nm of SiO_2

Table 3.1. Overview of different types of contacted nanowires

We found that the radial growth rate of the nanowires is more than 2 orders of magnitude lower than the axial growth rate. We observed tapering effect, a phenomenon whose characteristic is different diameter on the base and on the tip of the nanowire. It is defined as ratio of difference between diameter on the base and on the tip of the nanowire and length of nanowire. It ranges from 0 to 14% depending on Ga deposition rate.[17] During the process of growth, it is also possible to use silicon for purpose of doping. This is done by applying a current, which via Joule's effect heats a Si piece and enables incorporation of Si into structure of nanowire. Since silicon behaves as amphoteric dopant in GaAs, it can exhibit both donor and acceptor type properties. In case of our nanowires, it seems like general behavior is p-type. This, as well as different possible doping mechanisms, will be discussed with more details later.

By using four different heating currents (13 A, 11.5 A, 10 A and 0 A) it was possible to grow nanowires with four levels of doping, from highly doped ones (13 A of heating current) to nominally undoped ones (0 A of heating current). Keeping in mind that any type of doping can be done under high or low As pressure growing conditions, we analyzed 8 types of nanowires. Table 1 gives an overview of contacted nanowires, including sample name, arsenic beam flux and heating current.

3.2.c. Initial results

As already mentioned, the first challenge we have been faced with was the design and production of electrical contacts for GaAs nanowires. We started working with relatively long (10 μm) nanowires. Prior to the contacting, we had to develop methods to transfer nanowires. This is necessary since contacting cannot be done on the original substrate.

The device fabrication starts with transfering nanowires on Si wafer covered by 50 nm of SiO_2. The role of SiO_2 is to prevent leakage currents through substrate and ensure signal is coming from nanowire only. Then, two contacts were formed by optical lithography followed by development, evaporation and lift-off. Although fast and relatively non-complicated, this method showed one basic disadvantage, reproducibility of contact location. It is not possible to guarantee two different nanowires will be contacted in same way. This is due to limitations in the alignment done with optical microscope, at the edge of resolution. This makes a reproducibility between devices produced in different sessions an issue, as we will show and discuss later. Another point of major importance is contact resistance, which cannot be excluded from measured values. A typical SEM image of contacted nanowire is reported in Fig. 3.1.

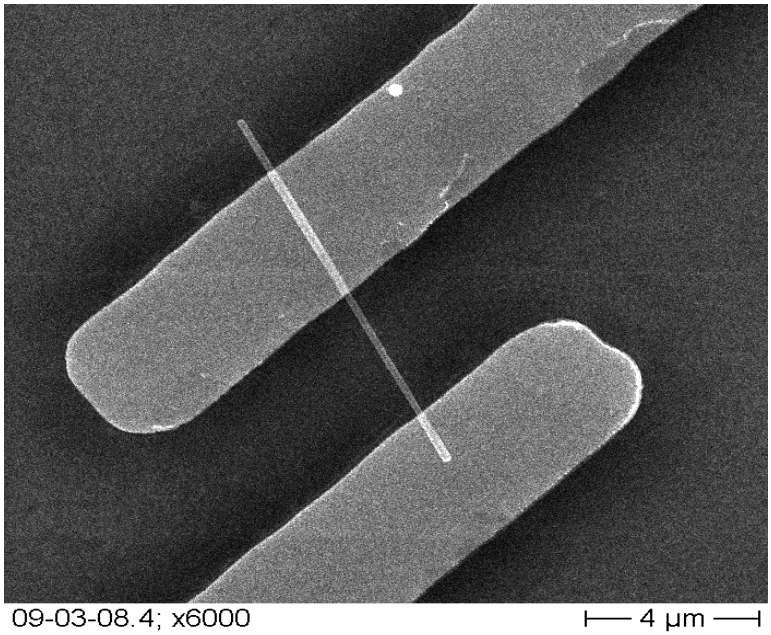


Figure 3.1. SEM image of contacted GaAs nanowire

The number of working devices was strongly dependent on the type of nanowire used. Highly doped nanowires are the most simple to contact because of their length (typically more than 10 μm), but even more important, their low resistivity and lower Schottky barrier, see Chapter 2. Undoped wires have very low conductance. It is because of this why thicker oxide layer is necessary (1μm instead of 50 nm) to be

sure that gate resistance, R_G, is much higher than nanowire resistance, R_{NW}. Furthermore, presence of very low currents (in the range of pA) required measuring under reduced signal to noise ratio. Moreover, RC constant in coaxial lines becomes relevant (see figure 3.2.b). Unfortunately, due to presence of capacitor between core and shall of coaxial cable, DC bias reaches its value gradually. When performing measurements on highly doped nanowires, this effect can be neglected. However, as we will later, same is not possible for undoped and 10 A doped nanowires.

Contrary to nanowires grown under high As beam flux conditions, nanowires grown in a low pressure environment are harder to contact since they present a smaller length (less than 4 μm) due to their lower growth rate. At the end of this initial study, we had characterized several nanowires of each sample.

As it will be shown in the following, two-point measurements based on optical lithography gave us a first idea of effects of doping parameters on nanowire transport properties. We were able to estimate resistivity, mobility and carrier concentration but a complete study still needed to be done to present more reliable conclusions. A schematic drawing of two point measurements is depicted in figure 3.2. We will shortly comment on figure 3.2 b) and c). Details of the setup are given in Chapter 2, here we mention only key points, namely ones related to origin of cable RC constant which will be important for explaining results on less conductive nanowires. The equivalent electrical circuit corresponding to the contacted nanowire is represented by a resistor R_{NW} and two diodes in opposite direction, S and D, presenting contacts between semiconductor nanowire and metal. Gate is modeled with gate capacitance C_G, while gate leakage, modeled with R_G, can normally be neglected. Samples for which R_G was not high enough (10^{12} Ω) were excluded from analyses. R_{BNC} and C_{BNC} present resistance and capacitance between core and shield of coaxial line. Data sheets provide values scaled per length, typically 10^{10} Ω/m and 100 pF/m, respectively. Using these values, and knowing length of cables (1.5 m), we can estimate RC time constant of coaxial line to value of 2.3 s. C_{DG} and R_{DG} present the capacitance and leakage resistance between fabricated drain contact pad and back gate. Equivalent values exist for source pad and back gate as well. Both C_{DG} and C_{SG} are calculated and obtained value is around 5 pF. Because of their high values (10^{12} Ω), leakage resistances R_{DG} and R_{SG} can normally be neglected. Due to fact one contact is always grounded impedance of corresponding cable can be neglected (see figure 3.2.b). C_{DG} and C_{SG} are for factor 30 lower than C_{BNC} and can be excluded from analyses as well. On the other hand, influence of gate cable is minor, since current should not flow through gate.

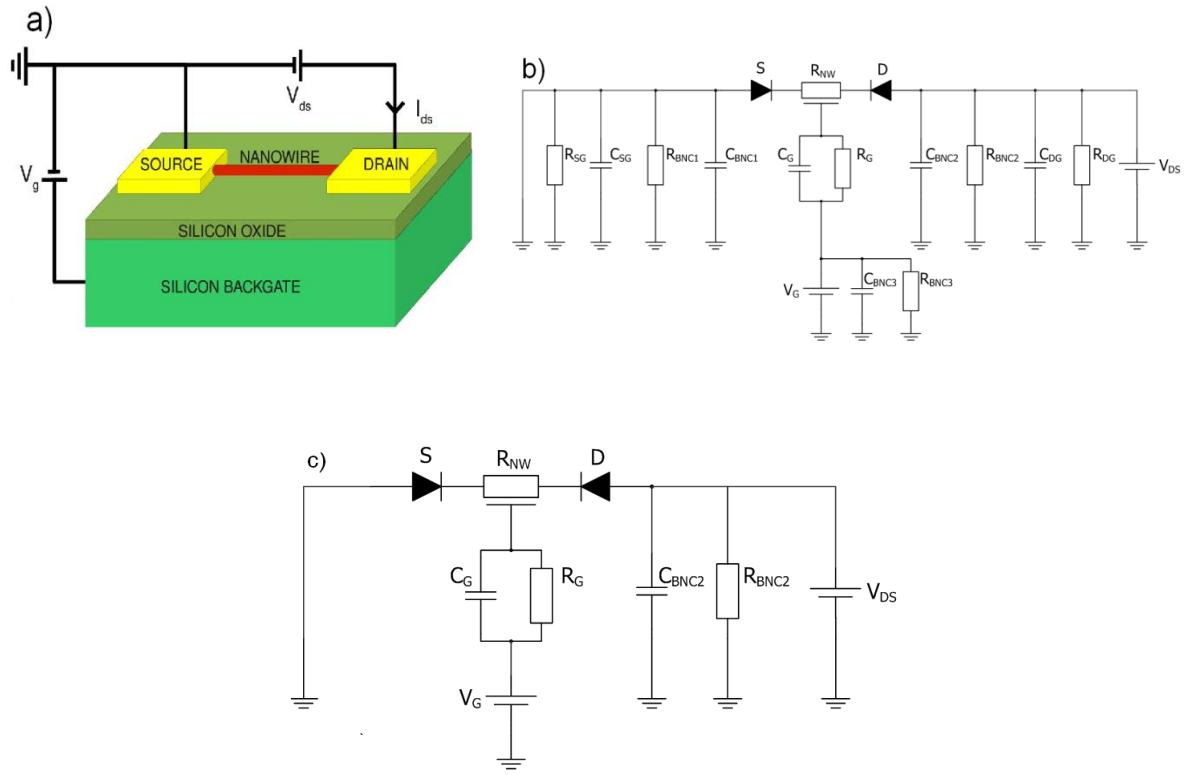


Figure 3.2. a) schematic drawing, b) complete equivalent circuit and c) simplified equivalent circuit of two point measurements

Finally, after neglecting all elements with minor influence, we obtained the equivalent simplified circuit schematically displayed in figure 3.2. c).

Prior to discussing actual two-point measurements, we would like to remind problem of Ohmic contact, more details can be found in Chapter 2. As discussed before, contact properties between metal and semiconductor layers strongly depend on both the semiconductor and the metal used. For the first trial, we used Ti/Au layers (10 and 150 nm respectively) for deposition and contacting the GaAs nanowire. This type of contact is easy to evaporate and lift-off. However, Ti/Au layers do not result in Ohmic contact with p-type GaAs nanowires.

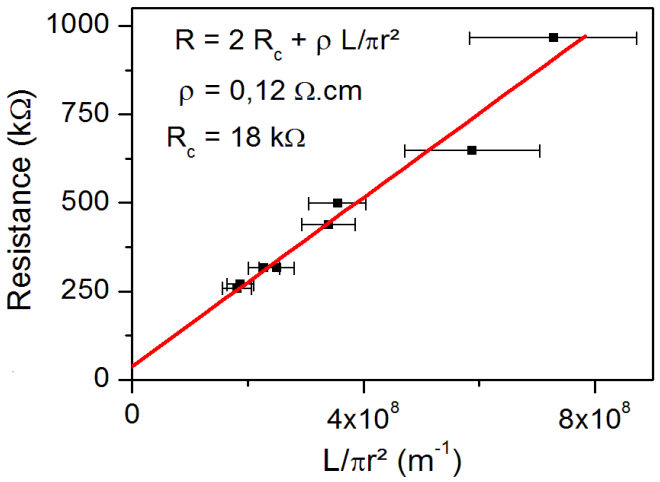


Figure 3.3: Resistance vs geometrical factor $L/\pi r^2$ for doped nanowire, linear fitting enables estimation of nanowire resistivity and contact resistance R_C.

A detailed research on existing bibliography resulted with new contacting scheme containing palladium as crucial metal layer.[47] Pd/Ti/Pd/Au layer (typical thickness 10/40/40/100nm) resulted in good Ohmic contact, see figure 3.4. Contact mechanisms for this particular case are not precisely understood but it is believed that Pd diffuses through the native oxide layer and reacts with GaAs, creating As and Ga-rich compounds, reducing barrier width while Ti is believed to block As from diffusion out of nanowire.[47] Experimentally, Schottky barrier seems to be strongly reduced and nearly inexistent at room temperature and I_{ds}-V_{ds} curves show clear linear behavior for all kinds of nanowire. If we assume there is no contact resistance, the resistivity of the highly doped nanowires (13A of current heating Si chamber and low pressure), is around 0.1 Ωcm. We should stress here that the resistivity of the nanowire is actually indirectly measured and that contact resistance, due to linearity of the I-V curve can be to have value of zero. However, if we want to know order of magnitude for contact resistance, we can apply transmission line method[48,49] as showed in Figure 3.3. A value for contact resistance R_c can be approximated using the formula of the total resistance measured:

$$R_{tot} = 2R_c + \rho\frac{L}{\pi r^2}, \qquad (3.1)$$

assuming that R_c and nanowire resistivity are constant for all devices. As we will show later, this is not always the case. A more detailed study done on 13A doped samples, with different diameters and length between contacts, yields a plot presenting R versus $L/\pi r^2$. On this plot, resistivity ρ is given by slope of the curve, while its intersection with y-axis give value $2R_c$. As it can be seen on Fig. 3.3., the values which we calculated are not very accurate as they depend a lot on linear fit.

Still, it is clear that R_c has value bellow 30 kΩ when global resistance, measured between 2 points separated for 3 μm, is more than hundreds of kΩ, meaning when resistance per length is higher than 10^5 Ω/μm. Specific contact resistivity can be estimated using same method and obtained value is about $2x10^{-5}$ Ωcm^2. This is comparable with values for thin films contacts found in literature (10^{-5} -10^{-6} Ωcm^2).[47,50]

According to literature[47], a rapid thermal annealing should decrease this resistivity for more than one order of magnitude. Several tries were made but every time properties were harmed. In some cases, nanowires were broken or contacts peeled away. Because of this, we did not proceed with the annealing process. Still, this could be done as part of some future work. To have a precise evaluation of contact resistance for all doping levels, 4-points contact devices should have been implemented. These results will be discussed later. However, for 2-point measurements, contact resistance is supposed to be small enough compared to nanowire resistance and will always be neglected in the resistivity calculation. The MOSFET clearly shows a linear regime, indicating good contact, and doping of the channel is p-type since I_{ds} is higher for negative gate bias. Using geometrical characteristics obtained by analyses of SEM micrographs (nanowire diameter and contact distance), and applying certain approximations, we were able to calculate values for resistivity.

Prior to discussing resistivity, mobility and carrier concentration, we will present typical transport curves for representative nanowires from each doping level category. As we will show later, nanowires grown under high As beam flux conditions (HBF) displayed strong dispersion.

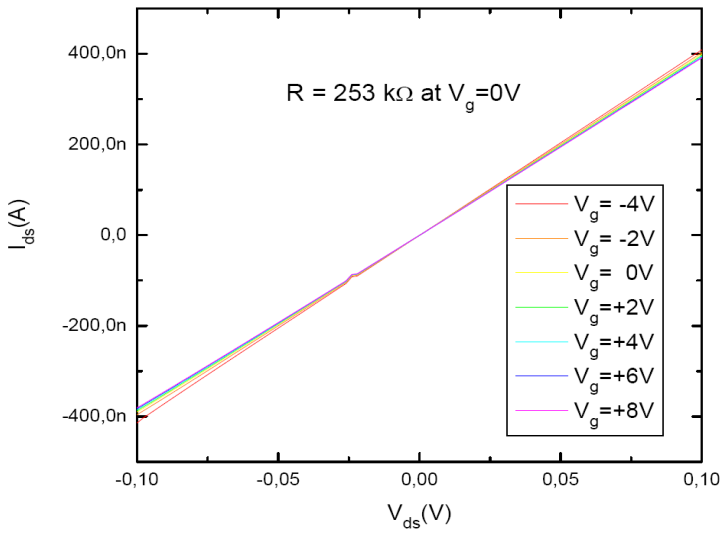


Figure 3.4. I-V characteristics of GaAs nanowire grown under low beam flux conditions, doped with 13 A of current heating Si cell. Small peak at 0.02 V comes from systematic error of measurement method and can be neglected since it does not exhibit important influence on measurements. Peak is induced by automatic adjustments in the measurement range of the KEITHLEY SMU 2611 at 100 nA.

It is because of this why we chose to present I-V curves measured only on nanowires grown under low As beam flux (LBF) conditions. This is done due to sake of clarity, since I-V curves for HBF nanowires display lower reproducibility. Figure 3.4 displays I-V characteristics of representative highly doped GaAs nanowire grown under LBF conditions. A clear Ohmic behavior and linear response to voltage feed can be observed. At zero gate voltage, for V_{ds} sweep from -0.1 to 0.1 V, nanowire resistance of 253 kΩ is measured. Contact distance was 3 μm leading to resistance per length of 84.3 kΩ/μm. Assuming average diameter of 100 nm, current flow over entire cross-section of nanowire and same bias conditions, current density slightly above 5 kA/cm^2 is obtained.

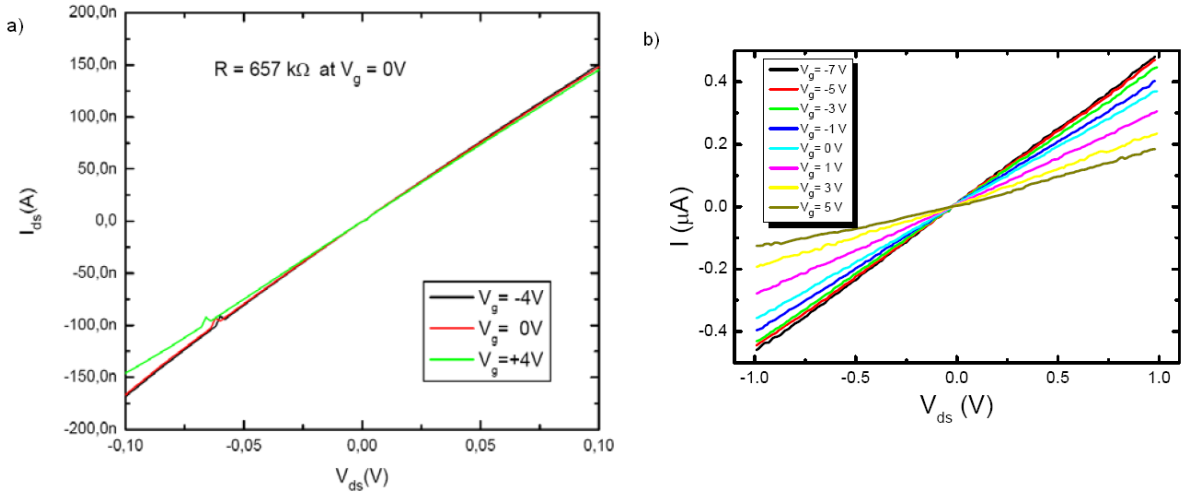


Figure 3.5. I-V characteristics of GaAs nanowire grown under low beam flux conditions a) and high beam flux b), doped with 11.5 A of current heating Si cell

Electrical behavior of 13 A LBF GaAs nanowires can be described as quasi-metallic since response to gate is very low due to small nanowire resistance per length. To make this issue more clear, temperature dependent transport measurements were required. In case of low temperature measurements, reduction of resistance while decreasing temperature would indicate metallic behavior, while strong enhancing of resistance while reducing temperature would indicate semiconductor behavior. Measurements performed by other group members, Dr. Joseph Dufouleur and Dančе Spirkosa[51], exhibited only slightly higher resistance for cryo temperatures, indicating quite metallic behavior of highly doped GaAs nanowires.

Figure 3.5a) represents I-V characteristics of typical 11.5A doped GaAs nanowire grown under LBF conditions. Electrical measurements still show quite linear current response to applied bias. Resistance measured without gate voltage being applied, for V_{ds} sweep between -0.1 and 0.1 V, is slightly above 650 kΩ. With inter-contact distance of 3 μm, we obtain resistance per length of 217 kΩ/μm, which is roughly 2.5 times more than for highly doped nanowires. Assuming same cross-section approximation, and with same applied biases, one obtains current density of around 1.9 kA/cm^2. As expected, gate effect is more pronounced. Just for sake of comparison, I-V curve for nanowire doped with same heating current but in HBF

conditions (figure 3.5. b)), shows both lower resistance and better gate response. Still, as we will show later, HBF nanowires display strong dispersion of measured electrical properties.

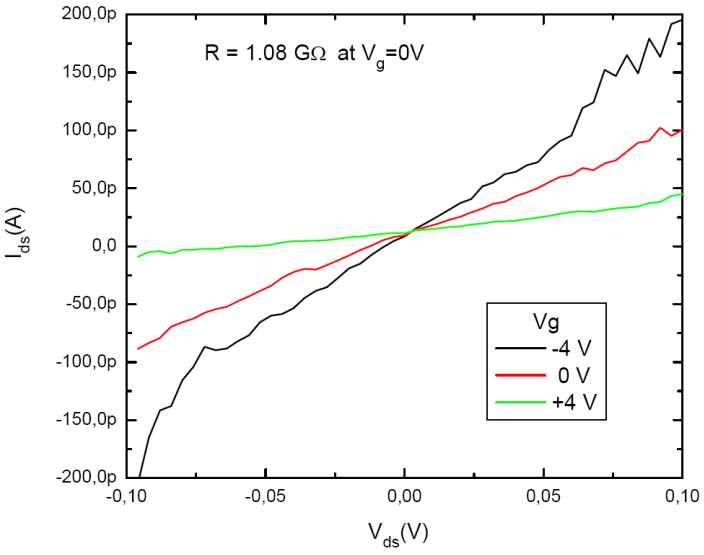


Figure 3.6. I-V characteristics of GaAs nanowire grown under low beam flux conditions, doped with 10 A of current heating Si cell

Typical I-V curve of representative 10 A doped LBF GaAs nanowire is reported on figure 3.6. Contacting surface for optical lithography between various samples differs only slightly (because of UV light scattering and mask-sample distance). It is because of this why lower conductivity of nanowire could be explained by lower concentration of free carriers, not by the contact surface. Global resistance is more than 1 GΩ for zero gate voltage and V_{ds} sweep between -0.1 and 0.1 V. Corresponding resistance per length is 360 kΩ/μm. Due to high resistance per length of the nanowire, time constant of coaxial cable (see figure 3.2.b) becomes important and superposes to actual signal, as we can see on black curve for higher negative voltages. In general, influence of cable RC constant cannot be neglected when non-instantaneous change of DC bias sweep becomes relevant. For nanowires with lower global resistance this effect has negligible influence.

There is a clear gate response. Moreover, unlike for the higher doping levels, on-off transition is observed. However, certain part of global resistance originates from cable (RC constant of real capacitor) and more detailed analyses are necessary. Possible solution is increasing integration time to periods longer than currently used 100 ms. We roughly estimated RC constant to 2.3 s which suggests longer delay periods between 2 measured points would be required to eliminate time constant.

A statistical analysis of the nanowires with different nominal doping levels enables an estimation of the doping effects regarding the transport properties. The calculated values are ranging from not less than 1000 Ωcm for nominally undoped wires to 0.1 Ωcm for the nanowires with the highest level of doping. This is depicted in figure 3.7.

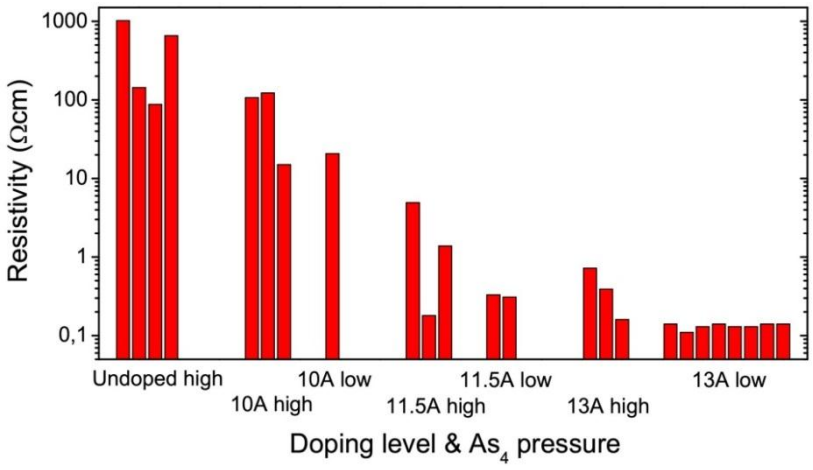


Figure 3.7: Resistivity measured on several single nanowires with different growth conditions (level of doping and As4 pressure).

This obvious change in resistivity (roughly about 4 orders of magnitude) is a strong evidence of controlling the doping concentration (Fig.3.7). Moreover, the use of different Si flux really has an influence in the dopant incorporation. The average resistivity for each growth condition drops from high values for nominally undoped to lower values for the most highly doped samples. This is very important conclusion since it implies it is possible to control the doping level by adjusting the Si flux.

It is also crucial to notice dispersion in values for resistivity even within nanowires grown under same growth conditions. This could be attributed to the influence of contact resistance, but also to non-homogeneity of doping. If non-homogeneity of doping along the single nanowire should be the actual reason for dispersion, results are not surprising. We already pointed out how challenging would be to experimentally realize 2 contacts in approximately same location for different contacting sessions. The measurements are realized on two different segments of nanowires, which, if nanowire is not homogeneous, could exhibit different mentioned properties.

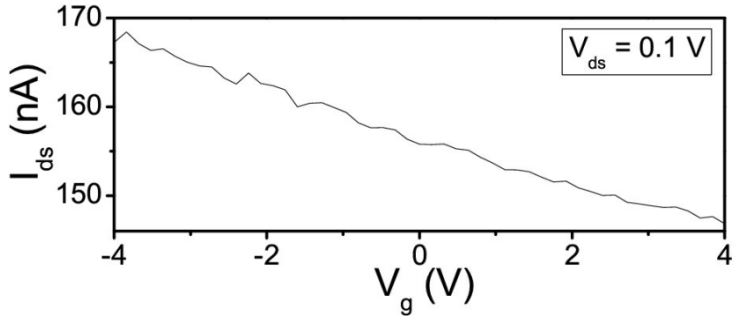


Figure 3.8: I_{ds}-V_g plot for a single 13A doped, high As_4 pressure nanowire.

In order to obtain a better picture about the dopant incorporation mechanisms, values of carrier concentration and mobility needed to be investigated. Prior to discussing results, we will shortly explain the theoretical background. With geometries such as nanowires, it is not possible to perform Hall bar measurements and directly obtain carrier concentration and mobility. Due to this, we have to introduce assumption regarding nanowire geometry and corresponding gate capacitance, as we will show later. Moreover, every nanowire for which we want to calculate mobility and carrier concentration must present transconductance differing from zero. In case of 4-point measurements on 13 A doped HBF nanowires, we observed lower nanowire resistance due to shorter inter-pad distance. Due to this, no transconductance was detected and carrier concentration needed to be extracted from concentration of doping Si atoms. However, in case of optical lithography, due to higher inter-pad distance, non –zero transconductance is observed for all doping levels.

I_{ds}-V_{ds} dependence is related to channel resistivity. If we approximate nanowire geometry with cylinder, the following equation will be obtained:

$$\frac{dI_{ds}}{dV_{ds}} = \frac{\pi r^2}{\rho L}, \tag{3.2}$$

where r, ρ and L stand for radius, resistivity and inter-pad distance, respectively (figure 3.9). In case of all measurements discussed so far, gate is implemented as a global back contact, with a thin layer of thermally grown oxide on which the quasi-cylindrical channel is lying.

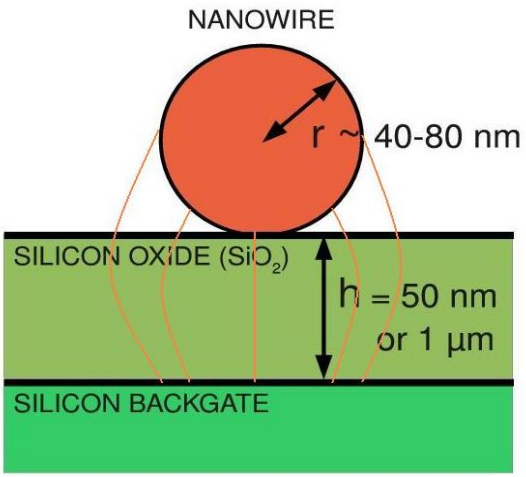


Figure 3.9. Schematics of the GaAs nanowire cross section. Orange lines represent electrical field in back-gate capacitor. Geometrical relations are exaggerated due to sake of clarity.

This geometry leads to an expression for capacitance between conductive back gate electrode and conductive channel, separated by insulating silicon dioxide. Back gate capacitance is given by[52]:

$$C_g = \frac{2\pi\varepsilon_o\varepsilon_r L}{ar\,ch\left(1+\frac{h}{r}\right)}, \tag{3.3}$$

where C_g stands for back gate capacitance, h is oxide thickness and ε_r stands for dielectric constant of gate oxide, in this case 3.9. One should keep in mind that exact treatment of this problem would require introduction of air as dielectric too, since air surrounds segment of nanowire as well. However, we will assume that lines of electrical filed (figure 3.9) pass through SiO_2 only. Also, although electric filed between two plates of capacitor in figure 3.9 is not homogeneous, we will assume it is. Once back gate capacitance is obtained, we can derive equation for mobility. We will start from Ohm's law:

$$I_{ds} = G\, V_{ds}, \tag{3.4}$$

Substituting conductance with conductivity, we obtain:

$$I_{ds} = \frac{S}{L}\sigma\, V_{ds}. \tag{3.5}$$

If we use relation between conductivity and mobility ($\sigma = ep\mu$), we will get equation (3.6).

$$I_{ds} = \frac{S}{L} ep\mu\, V_{ds}, \tag{3.6}$$

Substituting product *ep* with gate capacitance, gate voltage and volume leads to

$$I_{ds} = \frac{S}{L}\frac{C_g(-V_g + V_{th})}{V}\mu V_{ds} == \frac{C_g(-V_g + V_{th})}{L^2}\ \mu\, V_{ds} \quad (3.7)$$

Finally, when calculating total differential of both sides with respect to gate voltage ($\frac{d}{dV_g}$), one obtains following equation

$$\frac{dI_{ds}}{dV_g} = -\mu\frac{C_g}{L^2}V_{ds}. \quad (3.8)$$

In equations (3.6) to (3.8) meaning of symbols is following: e, p and μ stand for elementary charge (1.6 x 10^{-19} C), hole concentration and mobility. S and L are cross section and inter-contact length of nanowire, respectively. G stands for conductance while $\frac{dI_{ds}}{dV_g}$ stands for transconductance.

Knowing the mobility and resistivity, we can calculate hole concentration from equation (3.6). Mobility and carrier concentration are plotted together in the same graph, Fig. 3.10.

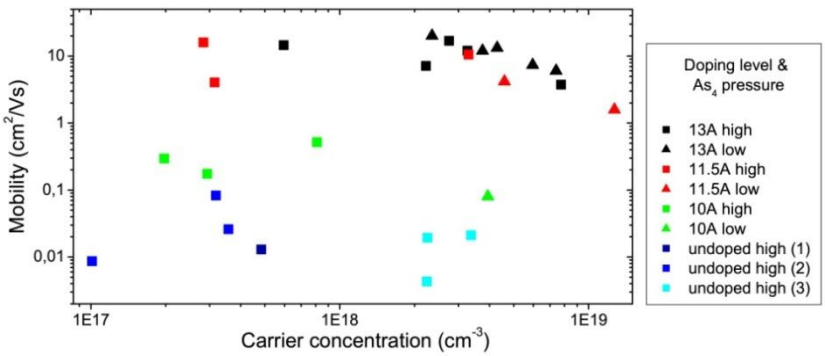


Figure 3.10.: Mobility vs carrier concentration. Level of doping is marked with different colors, while different growing pressure is pronounced with shape. Mark (1) corresponds to a couple of nominally undoped nanowires contacted in parallel to increase conductance. Mark (2) corresponds to single nanowires with 50 nm oxide layer. Leakage current is here same order of magnitude as I_{ds} and results are not completely reliable. Finally, mark (3) is presenting single nanowires with 1 μm thick oxide layer. These last ones show a higher carrier concentration which does not agree with global description presented

Values for mobility are increasing from less than 0.01 cm^2/Vs for nominally undoped nanowires and reaching final 20 cm^2/Vs for highly doped nanowires for which only

slight gate effect can be observed. Again, mobility dispersion for nanowires grown under same growth conditions is around one order of magnitude. Carrier concentration has values within range from 10^{17} cm^{-3} for nominally undoped nanowires up to 10^{19} cm^{-3} for higher doping levels. With high As_4 pressure conditions, mobility and carrier concentration seems to be increased for each higher doping level but still both values for a same growth condition can be dispersed in one order of magnitude. One additional comment should be pointed out here. Values for resistivity are calculated from measured resistance and geometrical parameters. Mobility is calculated from transconductance and geometrical properties which were measured, but also from gate capacitance which was calculated. Comparison of both mobility and carrier concentration for nanowires grown under same conditions is depending on assumption that nanowires resistivity is same in every segment of nanowire. Moreover, assumption seems to be reasonable considering structural homogeneities confirmed by Transmission Electron Microscope (TEM) analyzes. However, dissipation on nanowires grown under same conditions puts question mark on mentioned assumption, as it will be discussed in 3.3.d). We will show that resistivity depends on location of measured nanowire segment.

Coming back to the results obtained, it has to be noticed that undoped nanowires do not show clear properties. Except for these values on undoped nanowires, the overall results are a clear evidence a global and coherent behavior for dopant incorporation in nanowires. It is worth of mentioning that dopant incorporation here is different from bulk material. As we know, hole mobility is lowered from 400 to 50 cm^2/Vs when carrier concentration is increased in bulk GaAs.[53] The very low mobility which we calculated for nominally undoped GaAs nanowires can be a consequence of non-perfect crystal structure, with many possible defects along the nanowire. Those defects can lead to numerous scattering processes during the transport, making a mean free path shorter and finally leading to reduced mobility.

As our measurements and calculations suggest, it appears that introducing even a small doping (10 A of current heating Si chamber) of Si atoms in the lattice quickly improves the global structure, increasing the mobility significantly. The highest mobility that can be obtained is still lower than the one for bulk material. This could be due to surface scattering in the nanowire. After the mentioned mobility improvement, it seems that doping causes only gain in numbers of extrinsic carriers with a slight decrease regarding mobility.

At the end of this section, we will shortly comment on the influence of As_4 pressure as, together with temperature, one of the key growing parameters. Nanowires grown with a lower pressure present slightly different properties. The overall increase of conductivity and mobility with nominal doping level is clear. Still, as already briefly mentioned while commenting figure 3.7., nanowires grown under low beam flux conditions display a more homogeneous behavior. Moreover, a higher carrier concentration seems to be obtained for all doping levels in LBF nanowires, Fig. 3.10. These conclusions are reasonable keeping in mind that a lower As_4 pressure during the growth results in a lower growth rate. Lower growth rate with same Si flux means higher Si atoms concentration and, therefore, more carriers. Above mentioned characteristics, especially the reproducibility of the resistivity, are very important. In order to make a functional and useful device, it is crucial to show

certain effects, for example transistors effect, but, it is equally important show that reported properties are reproducible, i.e. when repeating well defined experimental procedure, one should be able to obtain same results.

Further investigations will be performed in order to understand dispersion observed in GaAs nanowires grown under high As beam flux conditions. We will study properties of different segments within same HBF GaAs nanowire, analyze their homogeneity and reproducibility. Discussion of doping model will be provided as well. In order to perform necessary analysis, we will combine transport and Raman spectroscopy measurements.

3.2.d. Spatially resolved measurements

As we have already mentioned, optical lithography in principle enables production of 2 contacts only. Moreover, since alignment is done with optical microscope, and therefore on the very edge of resolution, it is virtually impossible to fabricate two comparable devices. This means that contacts will hardly ever be done at approximately same position on the nanowire with respect to the tip. This is one of reasons why we obtained significant dispersion of electronic properties, particularly pronounced in case of nanowires grown under high As beam flux conditions. But, due to promising results that we already discussed, we were seeking for experiments which could provide us with deeper understanding and suggest possible improvements towards better and more reliable devices.

One of the solutions for achieving a better reproducibility was electron-beam lithography. Details on this technique can be found in previous chapter were we discuss device fabrication as well as in Appendix. We shortly mention basic advantages and disadvantages. E-beam lithography enables fabrication of devices with higher number of contacts. Number of contacts can be higher due to

significantly increased resolution, which enables contacts with adjustable width and inter-contact distance. Another important property is fact that more than one nanowire can be contacted per session. Basic disadvantages are coming from nature of e-beam lithography. Unlike optical lithography were operator can see exact nanowire of interest, in e-beam lithography same electron beam is used for visualization and for exposure, resulting in longer alignment. This, as a consequence, leads to much longer time for pre-exposure settings. Still, being able to produce four or more contacts on same nanowire is a powerful tool.

Basic reasons why we want four or more contacts are two. First, it enables four-point measurements. These measurements are better than two-point measurements simply because they separate contact resistance from nanowire resistance. Another point is, placing more contacts along the nanowire length, one can study electrical properties of different segments within the same nanowire and derive important conclusions, for instance ones regarding homogeneity.

We pointed out already in optical lithography section that observed doping in GaAs wires is type p. This means that Si atoms dominantly take As places in GaAs crystal

during the process of growth. In fact, type of doping strongly depends on the geometry of surface. [35] This is due to free chemical bonds available to dissociate As_4 molecules. Furthermore, the Si incorporation behavior depends on the ratio of As and Ga.[35,38] Reducing As_4 pressure should increase incorporation of Si leading to higher doping. However, it is not clear how the dopants are incorporated into GaAs nanowire structure, meaning, is the dominant path one through the side of the nanowire or one from the nanowire tip. By placing more contact on same nanowire and combining transport with Raman spectroscopy measurements, we were able to give answer on this. We have already reported a work whose purpose is to understand the doping mechanisms in catalyst-free gallium assisted grown GaAs nanowires using above mentioned approach.[38] The two techniques mentioned gave us important information regarding the doping mechanism. Transport experiments enabled determination of properties such as resistance per length or carrier concentration for entire volume of nanowire segment between two contacts. On the other hand-side, Raman spectroscopy provided us with better understanding of the incorporation sites and space distribution of Si atoms concentration in the layers of nanowire closer to surface. Crucial difference is in volume of nanowire segment encompassed in measurements.

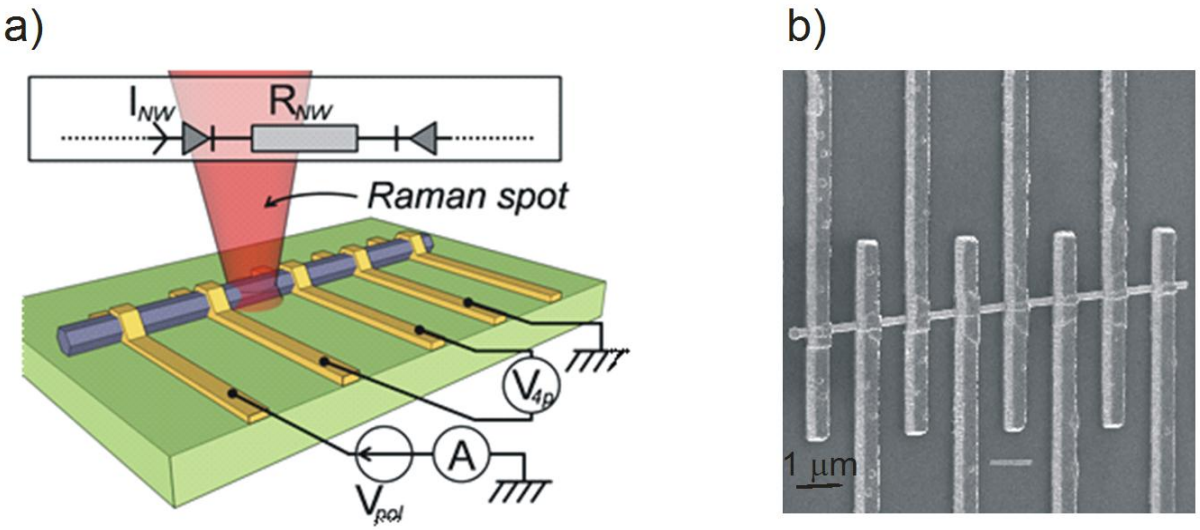


Figure 3.11.: a) Schematic drawing of sample characterized by both 4 point transport measurements as well as Raman spectroscopy measurements. b) SEM image of GaAs nanowires with multiple contacts

Let us now shortly describe obtained results. Multiple electric contacts were made with regular spacing between each of them, in a way that entire length of nanowire can be characterized. Details of experimental procedure are already described in previous chapter as well as in Appendix. The contacts themselves were predefined with process of positive electron beam lithography. Prior to evaporation of metals for contacting material, standard cleaning steps were made. We evaporated same combination of metal layers as for optically predefined contacts, Pd/Ti/Pd/Au

(10/40/10/100nm, respectively). Crucial difference with respect to optically made contacts is adjustable width of contacts as well as number and location of contact. For different samples we were changing contact thickness for several discrete values in range between 1000 and 250 nm. Of course, for specific sample were we wanted to perform both transport and Raman measurements, we needed to keep contact separation larger or at least equal to the size of the illumination spot (800nm). Although systematic study of contact size was not performed, it is important to stress that significant contact resistance increase by reducing the contact size was not observed, also including very thin contacts of 150 nm in width.

The nanowire resistance was measured both in two point and four point configurations, R_{2p} and R_{4p}, respectively. It is worth of repeating that the R_{4p} configuration has the advantage of separating contact resistance from 'pure' nanowire resistance. All the transport measurements were performed at room temperature. Detailed description of measuring set up as well as special efforts taken to reduce noise can be found in previous chapter. The schematic representation of electrical contacts in R_{4p} configuration is shown in the Fig. 3.11 a): The probing voltage was applied between the outer contacts, while the voltage drop was measured with the high impedance multimeter between the two inner contacts. Measurements in R_{4p} configuration are necessary to avoid superposition of parasitic contact resistance to actual nanowire resistance. In a two-point configuration the equivalent electrical circuit is constituted by two Schottky diodes in opposite direction with the resistance of the nanowire (R_{NW}) in series. When applying finite bias, the potential drop occurs more importantly across the diode polarized in reversed mode and the nanowire. However, under presence of bias high enough, minority carriers can be injected through the Schottky barrier and the global resistance is then dominated by R_{NW}.[35] More detailed explanation on Schottky barrier and related issues is discussed in Chapter 2. Our goal during 2-point measurements was to measure in regime when total resistance is dominated by nanowire resistance and parasitic effects of contact can be neglected. Initial results and high linearity of I-V curves suggested this was reasonable approximation. However, as we noticed later in 4-point configuration, even in described higher bias regime, a residual contact resistance is still measured by comparing R_{4p} and R_{2p}, even for a linear I-V characteristic $(\partial^2 V/\partial I^2 = 0)$, see figure 3.12. Influence of contact seems to be less pronounced in the middle segments of nanowire, while segment closer to nanowire base exhibits stronger influence of contact. As a direct result of this fact, the values of the nanowire resistance obtained by measuring in R_{2p} configuration are generally bigger since they include certain part coming from contact, not from nanowire itself. R_{4p} was measured along the wire, with the exception of the first and last point. At this two points, namely at very begin and end of nanowire, the resistivity is extracted from the measurement of R_{2p} at high bias voltage.

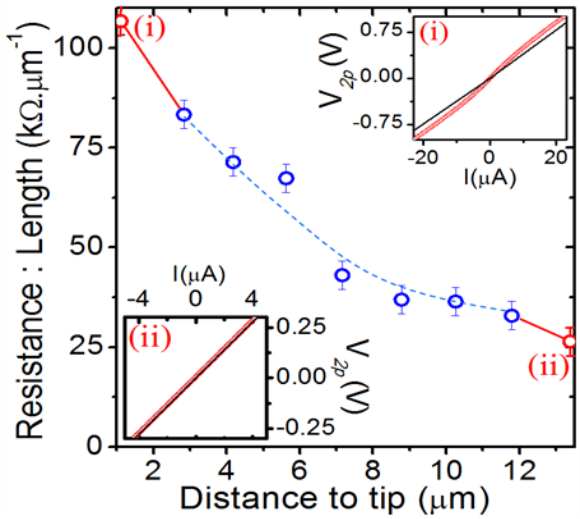


Figure 3.12.: Resistance per length, calculated using four points measurements (blue curve) and two points measurements at high bias (red). The distance between two contacts is constant along the nanowire and equal to one micron. In the insets, we show two typical I-V curves in a 2-points configuration.

We have measured the behavior of resistance with respect to position of the measured segment in 15 samples. The results of a representative nanowire are shown in. 3.12. The resistance per length decreases along the nanowire, it has the highest value at the tip and the lowest in the segment closest to the bottom. These changes in value of the resistance per length can differ even for one order of magnitude, if we compare one side to the other for a 20 micron long nanowire. The resistance per length can go down to values of $2\,x10^{10}\,\Omega\mathrm{m}^{-1}$. In order to understand how small this number is, we will do a short comparison. Literature value for resistivity of undoped bulk GaAs is $3.3\text{x}10^{8}$ Ωcm.[53] If we assume 1 μm long cylinder made of bulk GaAs with average diameter of 200 nm and entire cross section as path for current, we will get value for resistance equal to $1.05\text{x}10^{14}$ Ω. Considering length of 1 μm, we obtain resistance per length of $1.05\text{x}10^{20}$ Ω/m. Value we measured, $2\text{x}10^{10}$ Ω/m, is significantly lower giving a clear evidence of doping process effectiveness that we are able to perform during the growth of GaAs nanowires.

As it is already mentioned in the previous text, we performed comparative analyses of the resistance per length between nanowires obtained on the same run and with parallel identical runs. What we observed is a constant decrease in the resistance per length, from about 110 kΩ/μm from one side to about 20 kΩ/μm to the other one. They are all consistent, indicating a real reproducibility of the nanowire properties.

Dispersions we obtained from 2-point transport results (figure 3.7) were caused by measurements insufficient for definite conclusions. There are 2 reasons for this. Minor one is contact resistance which we could not exclude from nanowire resistance in 2-point measurement. However, dominant reason is non-homogeneity of resistance per length which is changing, as we said, from about 110 kΩ/μm from one side to about 20 kΩ/μm to the other one. Since we were not aware of this, we tried to compare segments of nanowires with different positions with respect to tip, meaning, with properties which can significantly differ. Still, 2-point measurements

gave us good initial idea for order of magnitude for expected values and provided us with better understanding of contact resistance and its influence on measured and calculated values.

The variation in resistance per length observed in 4-point measurements cannot be explained simply by geometrical differences, namely diameter values dispersion, along the nanowire(s). Obvious differences in resistance per length of our semiconductor nanowires can be due to a variation in doping and/or due to a change in the carrier mobility. Since detailed (HR)TEM analyses do not give reason to believe in existence of structural non-homogeneities, we assumed variation in carrier mobility could be excluded from further considerations and alternative explanation was sought. We concluded the most reasonable cause for the spatial dependence of the resistance per length could be lying in homogeneity of doping, which does not seem to be same along the length of nanowire. Electrical transport measurements are not enough to resolve issue of doping (non-)homogeneity. Just from electrical measurements, one cannot derive precise conclusion towards the location of the dopants within the nanowire because transport measurements give response from entire volume of contacted nanowire segment. If there are sections within contacted segment with properties different from rest of the segment, we could not resolve this with electrical measurements. Since we wanted to understand this issue better, we needed to look for alternative measurements techniques to prove whether doping homogeneity is the dominant reason for differences in resistance per length.

Since Raman spectroscopy provides information regarding the material structure and also about the existence and relative concentration of impurities, it was a reasonable method to continue with. We combined transport measurements and Raman spectroscopy on same nanowire. Raman measurements were performed to understand better the average concentration of Si dopants. Again, details on Raman spectroscopy operation and physics behind this measurement technique are given in previous chapter.

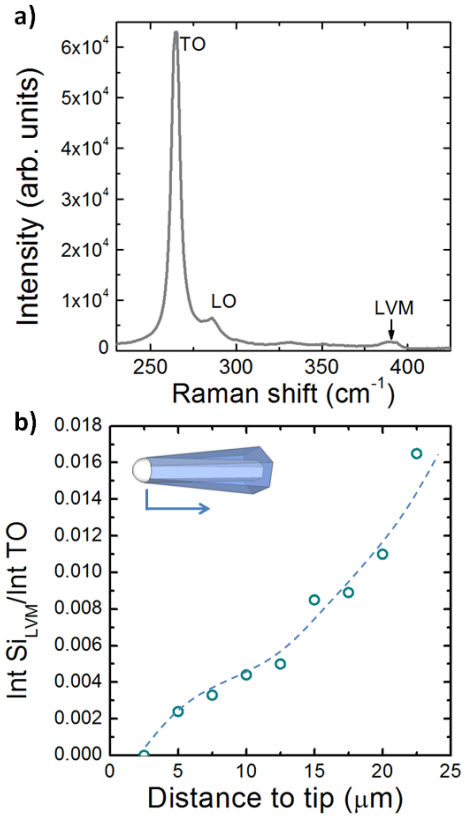


Figure 3.13.: a) Raman spectrum of a single GaAs nanowire doped with silicon. The local vibrational mode (LVM) around 390 cm^{-1} corresponds to the incorporation of silicon in arsenic sites. b) Spatial dependence of the intensity ratio between the LVM and TO modes along the nanowire.

It should be noted that Raman measurements results discussed in this thesis are not author's personal work. Measurements and analyses described in this chapter are done by another doctoral candidate from the group, Bernt Ketterer, whose help is kindly acknowledged. A typical Raman spectrum of a doped GaAs nanowire is shown in Figure 3.13 a). The big peak at wave number of 267 and less pronounced one at wave number of 290 cm^{-1} correspond to the transversal optical (TO) and longitudinal optical (LO) phonon modes of GaAs, respectively. These two peaks are the result we would have to get with or without silicon as doping material. However, a peak corresponding to lower relative intensity which we can notice around 390 cm^{-1} indicates the local vibrational mode (LVM) of silicon in GaAs. To be more exact, this mode corresponds to the presence of silicon dopants in arsenic sites.[35] This is consistent with already reported I_{ds}-V_{gs} curve (figure 3.8.) which also suggested that Si behaves as p-type dopant. If Si would be n-type dopant, and, therefore, take the place of Ga atoms in lattice, we would observe peak at wave number of 384 cm^{-1}.[35] One should keep in mind that under this measurement conditions, the intensity of the TO mode is proportional to the volume of the tested nanowire segment. On the other hand-side, the intensity ratio between the LVM and the TO mode (I_{LVM}/I_{TO}) should be proportional to the average concentration of silicon incorporated in the part of nanowire's volume exposed to the laser beam. Since penetration depth of the laser's light is around 40 nm, Raman spectroscopy gives information only from the outer part of the nanowire.[35] We have plotted the behavior of the I_{LVM}/I_{TO} fraction

along the same nanowire of figure 3.13. b). From the shape of this curve, it is clear that the average concentration of Si dopants increases along the nanowire from top to bottom. Let us recall this is consistent to already discussed decrease in resistance per length. What this result means is that average concentration of silicon in the outer part of nanowire changes from the tip to the bottom, changing in the same time concentration of free carriers, and by this, resistance per length in a way that it has minimum at the nanowire base and maximum at the nanowire tip. However, regarding the penetration depth of the laser beam in Raman setup, question of Si concentration in inner part of nanowire remains unclear. Each measured nanowire exhibited same behavior, maximum of resistance per length is measured on segment closest to tip, while minimum on segment closest to base of nanowire. More detailed analyses on doping model could provide additional information. In order to clarify this, we will first assume two extreme cases, as it is depicted in figure 3.14.

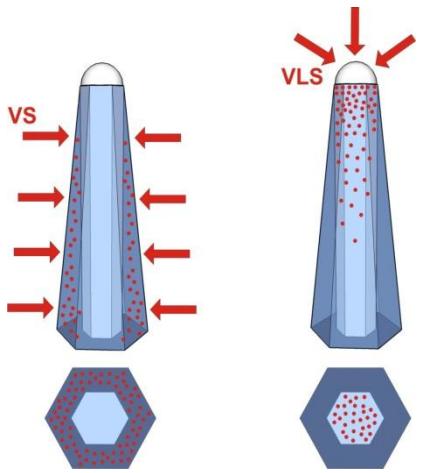


Figure 3.14. Drawing of two extreme doping mechanisms in nanowires: through side facets and b) through the droplet

The first mode for dopants to be incorporated is through the nanowire facets. This mode becomes more pronounced when the dopants are not soluble in the droplet and/or when radial growth cannot be neglected. Taking into account last condition, even for a minor growth in radial direction, the Si dopants can be gradually incorporated during the nanowire growth. If doping happens as a side effect of radial growth, consequence would be higher number of dopants at the nanowire bottom. Moreover, this number should continually decrease as we move closer to the nanowire tip. The second incorporation mode is the Ga droplet at the nanowire tip. In this case, the amount of Si atoms incorporated in the nanowire structure should be proportional to the concentration of Si atoms in the droplet.[35] If this would be actual state of doping mechanism, the doping concentration in the nanowire should be very small, virtually negligible, at the nanowire bottom, increase continuously as we approach the nanowire tip where it should reach maximal concentration. This will be explained in more details later. Since we observe higher concentration of dopants near the base of nanowire, the first dopant incorporation mechanism, namely one through side facets, is clearly dominant. Mentioned incorporation of silicon could be just the consequence of the radial growth of the

nanowires. For the previously described MBE growth of nanowires, the radial growth is about a 2-3 orders of magnitude smaller than the axial growth.[38] We tried to verify this statement by analyzing diameter at nanowire bottom and tip. We assumed that no radial growth occurs on nanowire tip, meaning, radial shell should have zero thickness at this point. Due to this, nanowire diameter close to the tip should correspond to core diameter. On the nanowire base, thickness of the radial shell should have maximal value, given by difference between diameter at base and diameter at tip. Estimated maximal shell thickness in that case would be around 50 nm. If we correlate radial shell thickness (0-50 nm) with typical nanowire length (20 μm) we obtain radial growth lower than axial growth for 2-3 order of magnitude, as stated before. If we take into account geometrical factors of the flux toward the nanowire facets[35], the concentration in the shell should be 6 x 10^{19} cm^{-3}. If we consider middle segment of nanowire with resistance per length of 50 kΩ/μm and shell diameter of 25 nm, we can determine resistivity of 0.0275 Ωcm. Assuming mobility equal to one obtained in 3.3.c) for 13 A doped HBF nanowires (20 cm^2/Vs), we can calculate carrier concentration of 1.13x10^{19} cm^{-3}. Such doping concentration is in same order of magnitude as previously mentioned concentration of Si atoms in shell.

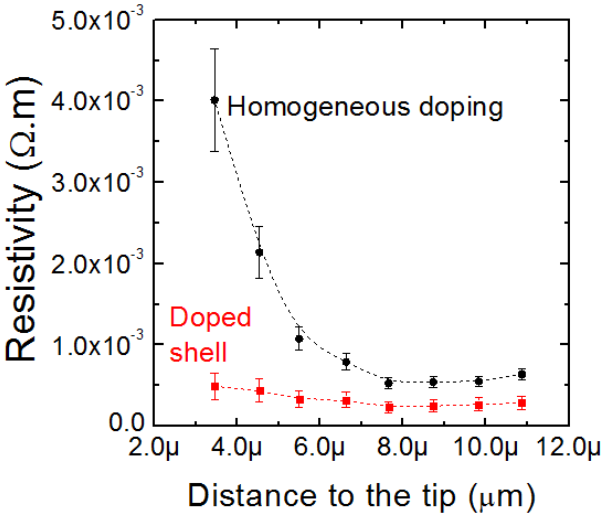


Figure 3.15. Dependence of the resistivities in different zones of same nanowire based on homogenous doping and shell doping

However, value for mobility obtained in 3.3. c) is based on homogeneous doping assumption which is not the actual case. Therefore, additional calculations needed to be done to confirm first doping model as actual one.

We have calculated the resistivity assuming two geometrical cases. First, we assumed that current flows through the total nanowire cross-section. As a second case, we assumed current to be flowing only through doped shell. As stated before, the thickness of the doped shell can be approximately calculated from the changes in diameter along the nanowire axis. In figure 3.15, we plotted the resistivity obtained with these two different assumptions. Two resistivity plots are different, simply because of different cross-section through which current is assumed to flow. If we assume that silicon is incorporated in the shell, one obtains a relatively

constant resistivity in all sections of nanowire. The same kind of behavior was observed for all the tested nanowires proving that shall dominantly participates in transport and that mobility and carrier concentration seem to be quite constant. This conclusion is not in contradiction to figure 3.13 b). Quite constant resistance of the shell suggests constant carrier concentration in the shell. Laser beam in figure 3.13 b) is limited by the penetration depth (40 nm), which, depending on laser beam location can reach not only shell but also undoped core as well.

However, doping through the droplet should not be neglected. As we already pointed out, we are assuming that the diameter of nanowire core corresponds to nanowire diameter measured close to tip, while thickness of the shell can be obtained deducing this diameter value from values measured in sections between the tip and the base. This would imply that zones of nanowire close to the tip have core only, without presence of shell. If the resistivity is approximately constant along the nanowire, dopants are incorporated in the core in segments close to the tip, which directly confirms existence of doping path through the droplet. Still, we will provide another comparison showing that this doping mode is not dominant.

When assuming doping through the droplet as dominant, one should pay attention to both steady state concentration of Si atoms in droplet and incubation time.[35] The incubation time is the period necessary for the droplet to achieve steady state concentration of silicon. The steady state concentration of the Si can be analyzed assuming that difference between Si flux from gas phase to liquid droplet and flux from liquid droplet to and solid nanowire must be zero. The silicon concentration in the liquid gallium and in the GaAs nanowire are related via the factor called the distribution coefficient, k, where k can be given as ratio $c_{Si(s)}/c_{Si(l)}$. In this case, $c_{Si(s)}$ and $c_{Si(l)}$ denote concentrations of Si in nanowire and droplet, respectively. The value of the distribution coefficient of silicon in the GaAs solid/liquid system at 630 °C are 0.1 for silicon incorporated in As sites and 0.06 for incorporation in Ga sites.[35] Due to simultaneous incorporation of silicon in both As nad Gas sites, compensation will exist. At 630 °C, the incorporation of Si occurs preferentially in As sites (p-type doping) in a ratio 5:3, given by the different values of k for acceptors and donors.[35] Keeping in mind nanowire growth rate (5.5 μm/h) and the silicon flow (1.62×10^{12} Si at/cm^{2}s) used in this study, $c_{Si(s)}$ is equal to 1.06×10^{18} Si at. cm^{-3}, while $c_{Si(l)}$ in the droplet is 0.015 %. The incubation time necessary for droplet to reach concentration of Si equal to 0.015% is about 3 min. This means that already after 3 min of growth the silicon concentration in the droplet would be high enough to start precipitation of Si atoms into the nanowire. Nucleation time of 3 min is much shorter than growth time (4 h) and due to this can be neglected. Important thing to point out is that high compensation leads to the effective doping of 2.6×10^{17} cm^{-3} which is too low to obtain values for resistance per length we measured (figure 3.12). Moreover, doping through the droplet is not in agreement with Raman spectroscopy results.

Finally, we would like to discuss mentioned concentration value of 6×10^{19} cm^{-3}. As we pointed out before, assuming mobility from 3.3. c), this value is comparable to what we obtain from resistance per length measurements. However, mobility obtained in 3.3 c) is based on homogeneous doping and it can be inaccurate. It would be reasonable to assume reduced carrier concentration due to compensation effect which, in minor percentage, happens in side wall doping mode as well. Since

we did not observe transconductance with e-beam fabricated 13 A samples, we cannot resolve this issue accurately. However, as we will show in chapter 4, mobility of e-beam processed 11.5 A doped nanowires is around 50 cm^2/Vs. General trend we have already showed is that higher doping in general results in higher mobility. It is because of this why we can assume mobility for 13 A doped HBF nanowires is at least 50 cm^2/Vs while corresponding carrier concentration should not be more than $5.0x10^{18}$ cm^{-3}.

3.3. Conclusion

Electrical characterization of GaAs nanowires initiated with around 10 μm long nanowires which we contacted optically, providing only two contacts for measurements plus back gate. After improvements on fabrication process, we were able to experimentally observe Ohmic contacts (linear I-V characteristics) which made us conclude that contact resistance could be neglected. Assuming this, we calculated resistivity, mobility and carrier concentration for wide range of nanowires, from nominally undoped to the highest levels of doping. We showed that silicon, as amphoteric dopant in GaAs structures, dominantly becomes acceptor resulting in p-doping. Unfortunately, we were faced with the significant dispersions in calculated values for nanowires grown under same growth conditions. Results were better for nanowires grown under low beam flux conditions, but still, with 2-point measurements we could not understand what was the origin of this dispersion. We assumed it was due to non-homogeneities within same wire and (in smaller percentage) due to contact resistance.

When applying e-beam lithography, we were able to produce four contacts and realized contact resistance is present, making the actual nanowire resistance bigger. Even more, when placing more contacts on same nanowire, from the tip to the bottom, we realized there is clear difference in resistance per length depending on position of measured nanowire segment. From transport measurements only, we could not deduce origin of changes in resistance per length. We supposed it could be due to mobility variations or due to doping non-homogeneity. Since TEM analyses did not show presence of structural non-homogeneities we assumed mobility variation could be neglected and considered doping as more probable reason. Raman spectroscopy measurements were performed on same nanowires on which we performed transport measurements in order to understand better relative concentration and location of dopants. These measurements showed that average concentration of Si atoms encompassed by laser beam continuously changed from one side of nanowire to another and suggested that doping in nanowire is non-homogeneous. Since Raman spectroscopy provides information from outer segments of nanowires, it was not sufficient to derive the doping model. Analyzing both possible models (path through nanowire side walls and through the droplet), discussing Si atoms concentrations and comparing resistivities obtained, we showed

that doping mechanism was mostly consisted of doping through side facets of nanowire although doping through the catalyst droplet existed as well.

4. GaAs nanowire-based metal-oxide-semiconducotor field-effect transistors

4.1. Introduction

In this chapter, we will present a work dealing with metal-oxide-semiconductor field-effect transistors (MOSFETs) fabricated out of a single nanowire. We will start with the comparison between (MOS)FETs and bipolar transistors, explaining the motivation of described research. The comparison will be followed by a description of nano-MOSFETS design and fabrication. Finally, we will present the gate dependent measurements, proving the occurrence of field effect and, therefore, a transistor. Figure 4.1 reports a top-view of two typical nano-MOSFETs fabricated out of single GaAs nanowires. More details will be given in the rest of the chapter.

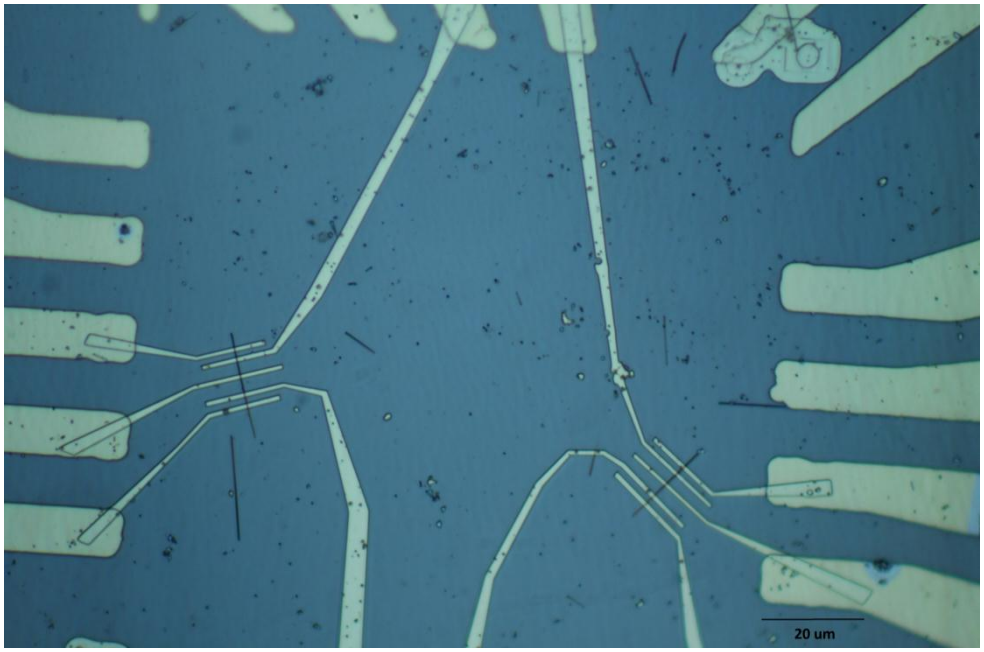


Figure 4.1. Top view optical micrograph of nano-MOSFETs. Figure is showing 2 typical nanowire-based MOSFETs. Nanowire material is GaAs. Each transistor has a source (lowermost electrode), two drains (middle electrode an uppermost electrode) and two top gate electrodes (second electrode both from upper and lower side). Substrate serves as global back gate electrode.

4.2. Comparison of bipolar and field effect transistors

Here we compare the properties of bipolar and field effect transistors (FETs), contrasting them with our goal of constructing nanowire-based field-effect transistors. Details on bipolar transistor operation can be found in [45, 54]. Figure 4.2 displays a schematic representation of these two types of transistors. As we can see on 4.2 a), a bipolar transistor consists of two p-n junctions. Depending on the application, one uses p-n-p or n-p-n bipolar transistor. Similar to the already discussed MOSFET model of Chapter 1, a bipolar transistor also contains 3 electrodes, called emitter, base and collector. The role of these can be compared to the role of source, gate and drain in an FET or MOSFET, respectively. A bipolar transistor is typically considered as being connected in way that emitter electrode is grounded*, while base and collector are biased with respect to emitter. The exact configuration differs for each specific application.

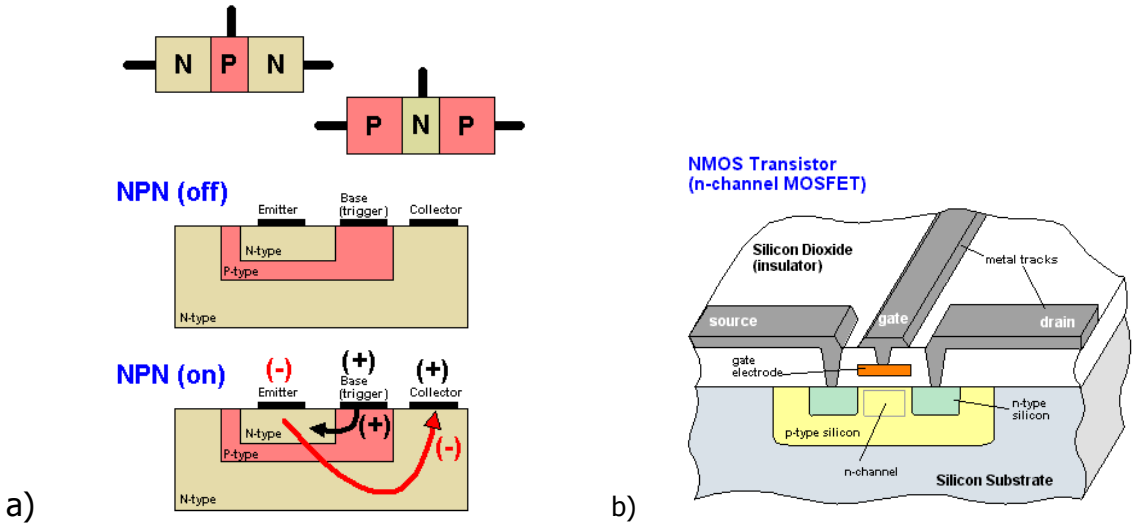


Figure 4.2. Schematic representation of bipolar transistor a) and MOSFET b).

This scheme corresponds to the source mode of a MOSFET, when the source electrode is grounded while the drain and the gate are biased with respect to it. The crucial difference between these two transistors is the mode of control. In the case of the bipolar transistor, control is achieved via base electrode current.

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* For consistency, we should note that, like any other electrode, emitter can not be connected to ground in a strict meaning of the word. Because of finite doping, emitter contains internal resistance, r_E, and can be modeled as serial junction of ideal electrode and resistor. However, in this simple model r_E can be omited without harming the accuracy.

In the first approximation, the collector electrode current is proportional to the base current, meaning, increase in lower base current (μA or less) results in gain of higher collector current (mA or more) for same collector-emitter voltage. Unlike current controllable bipolar transistor, a MOSFET (Figure 4.2. b)) is a voltage driven element. As explained in Chapter 1, applying voltage on gate electrode changes the conductive channel width (concentration of free carriers), leading to altered source-drain current for same source-drain voltage.

We will now compare some of the basic properties of both mentioned types of transistor. The first device characteristic considered is on-state resistance for a given breakdown voltage. The current flow must be evenly distributed across the chip area.[55] Bipolar transistors benefit from conductivity modulation of the resistive collector region when operated as a saturated switch. Applying this mode of operation reduces the effective on-resistance, R_{CEsat}. This effect shows increases as the collector-emitter breakdown voltage increases.[55] To make this issue clearer, Figure 4.3 shows the reduction in specific resistance for both bipolar devices and MOSFETs as a function of generation.

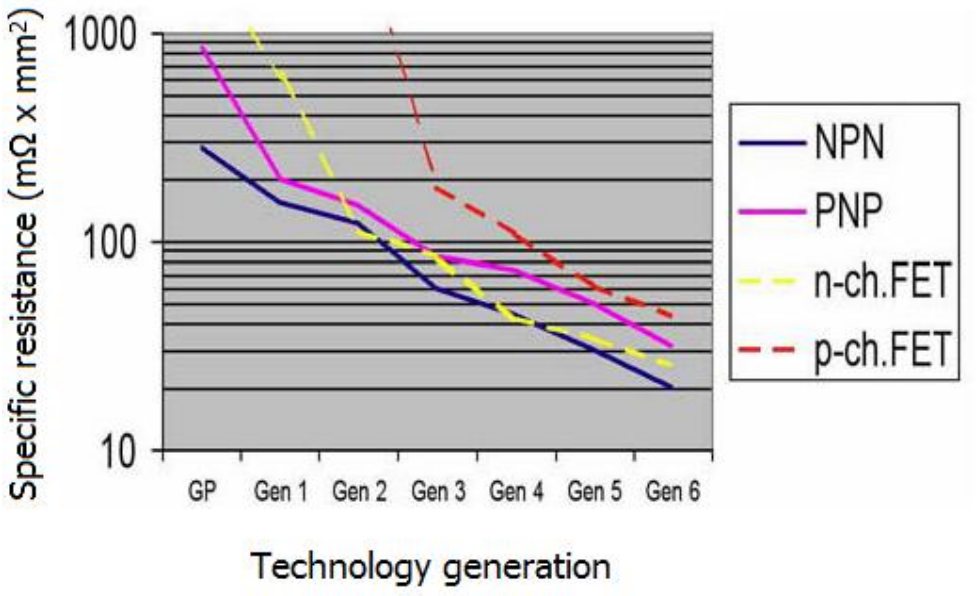


Figure 4.3. Specific resistance for bipolar (p-n-p and n-p-n) transistors and FETs (n-channel and p-channel). Figure is adopted from [55].

We should point out here that bipolar transistors block voltage in two directions, as specified by their characteristics (base-emitter-reverse voltage, BV_{EBO}, and collector-emitter-reverse voltage, BV_{ECO}).[55] Depending on specific application, this can eliminate the need for a series diode. Moreover, bipolar transistors also exhibit a temperature coefficient of resistance approximately a half of same value for

MOSFETs. This leads to higher efficiency at given temperature and colder running at higher currents.

Bipolar transistors require sufficient base current to achieve the lowest saturation output resistance, R_{CEsat}. The base current loss must be taken into account. While MOSFETs allow saturated switching at higher gains to minimize these losses, bipolar transistors become less useful at currents greater than a few amperes due to the high base currents required. However, bipolar transistors require less than 1 volt in order to turn on and exhibit high transconductance at low drive voltages. In conjunction with the better temperature stability of bipolar transistor, this can be of use in low voltage applications.[55]

MOSFETs require sufficient gate over-drive voltage (V_{GS}-V_T) to reach the lowestON output resistance, R_{DSon}. Moreover, this resistance increases fast as drive voltage approaches the gate threshold voltage.[54,55] When connected to a sufficiently high current circuit, MOSFETs can be used as fast electronic switch at MHz frequencies. On the other hand, a bipolar transistor in saturation mode requires the removal of stored charge during each cycle. This leads to longer off times, limiting the practical switching speed to a few hundred kHz. Finally, unlike bipolar transistors which are very resistant to electrostatic discharge (ESD), MOSFETs are more sensitive. Increased sensitivity to ESD results in operation errors in conditions when the gate rupture voltage is exceeded.[55] Table 4.1 contains a summary of the crucial differences of both transistor technologies.

Characteristic	MOSFET	Bipolar transistor
ON resistance	Good, depends on drive voltage	Equal to the best MOSFET
Blocking voltage	One direction, diodes in series may be required	Bi directional blocking capability
Pulse current	Moderate, limited by channel saturation	High
Current sharing	Good at higher voltage drive, may be poor at low voltage drive	Poor
Drive voltage	R_{DSon} can be adjusted with range of 1.8 to 10 V, full optimization at not less than 2.5 V	Less than 1V for full enhancement
Temperature stability	Moderate, V_T 4-6 mV/°C, R_{DSon} 0.6%/°C	Excellent, V_{BE} 2 mV/°C, R_{CEsat} 0.4%/°C
Drive power	DC: excellent, AC: HF may need buffer stage	Moderate
Speed	Fast	Linear switch fast, saturated switch moderate
ESD sensitivity	Very sensitive	Very low

Price per area of Si	Comparable	Comparable

Table 4.1. Parametric differences between MOSFET and bipolar transistor. Data is based on [55].

Analyzing the data from table 4.1 one can clearly see that both technologies have advantages and disadvantages. The choice should be made depending on the final application. For example, for the purpose of amplifying audio signals, more reasonable choice is a bipolar transistor based circuit. However, if the application is a fast electronic switch (memories, for example), the favorable choice is MOSFET.

Nanowires used in this thesis do not exhibit a double p-n unction. As shown in Chapter 3, our wires exhibit p type of doping. In the rest of the Chapter, we will explain procedures applied to fabricate GaAs nanowire-based MOSFET.

4.3. Design and fabrication

Due to the structure and type of doping nature of the GaAs nanowires, we decided to use MOSFET configuration in order to explore the possible electronic applications of these nanowires. The source and drain contacts were produced in the same way as described in Chapter 3. The gate electrodes were fabricated in two configurations, back and top gate. When possible, both approaches were applied on same nanowire and the gate effects compared. In the case of long enough nanowires (>5 μm), multiple top gate configurations were produced as well.

We used two basic approaches in fabrication of GaAs nanowire-based MOSFETs, photolithography and electron beam lithography. Basic lithography and evaporation steps were discussed in Chapters 2 and 3. In the case of photolithography, only back gate configuration can be obtained due to limitations in optical microscope alignment. Highly doped Si substrate is used as global gate electrode, while thermally grown silicon-dioxide played the role of gate dielectric.

The high precision of e-beam lithography enables production of top gate MOSFET configuration. Top gate electrode is a more challenging experimental realization. It requires two (e-beam) lithography steps. In first step, we define source and drain contacts (contacts 1, 3 and 5 in Figure 4.4) as described in Chapter 3. Prior to metalization (10 nm Pd/ 40 nm Ti/ 40 nm Pd/ 100 nm Au), samples were developed and cleaned. –The purpose of a second lithography step is to define a top gate electrode (contacts 2 and 4 in Figure 4.4). Since we need a dielectric layer (eg. oxide) between nanowire and metal contact to achieve gate operation, we do not perform O_2-etching nor HF etching. Omitting these steps, as explained in Chapter 2, results in residuals of electro-resist and native oxide being located between the

nanowire and contact. However, this is desirable in case of top gate electrode. Furthermore, a 1-2 nm thick Al layer is evaporated to additionally improve gate dielectric properties. Since Al oxides very fast, this results in formation of Al_2O_3. Here is important to obtain a Schotkky contact and not ohmic, since it should act as a gate electrode and no current should flow through it, simple Ti/Au (10 nm and 150 nm, respectively) bilayer can be evaporated for defining the contacts.

It should be pointed out that the second lithography step requires an extremely precise alignment (error below 100 nm). Due to the last requirement, definition of the top gate electrode by means of optical lithography is bordering on the impossible (unless the wires are longer than 20 μm).

4.4. Field-effect measurements

Here we present gate dependent electrical measurements. All measurements are performed at room temperature with the same setup configuration as described in the Chapters 2 and 3. Schematics of the used instrumentation can be seen on Figure 3.2. Again, due to issues discussed in Chapter 3, we will report results only for nanowires grown under low beam flux (LBF) conditions.

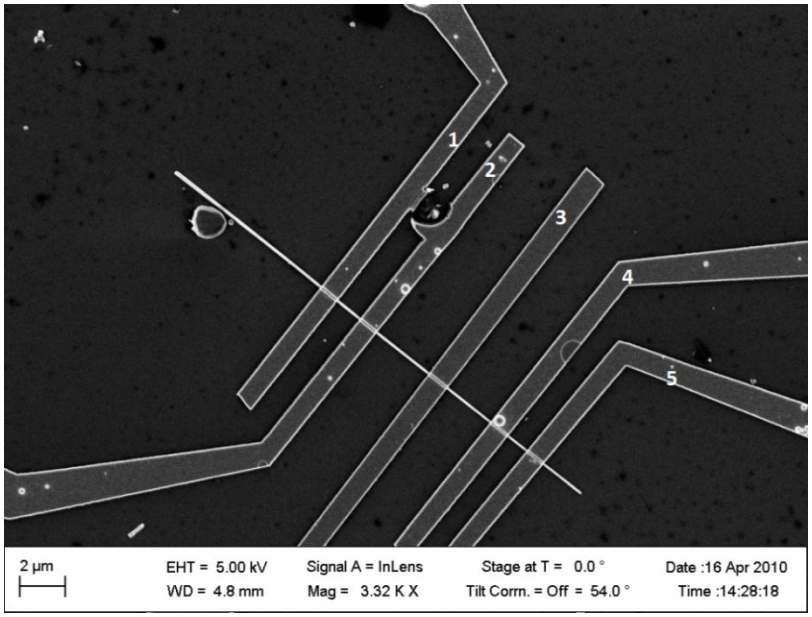
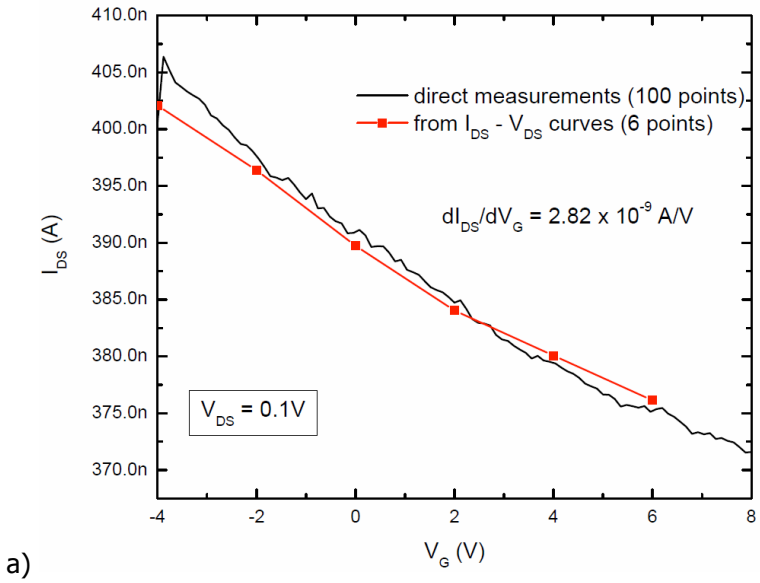


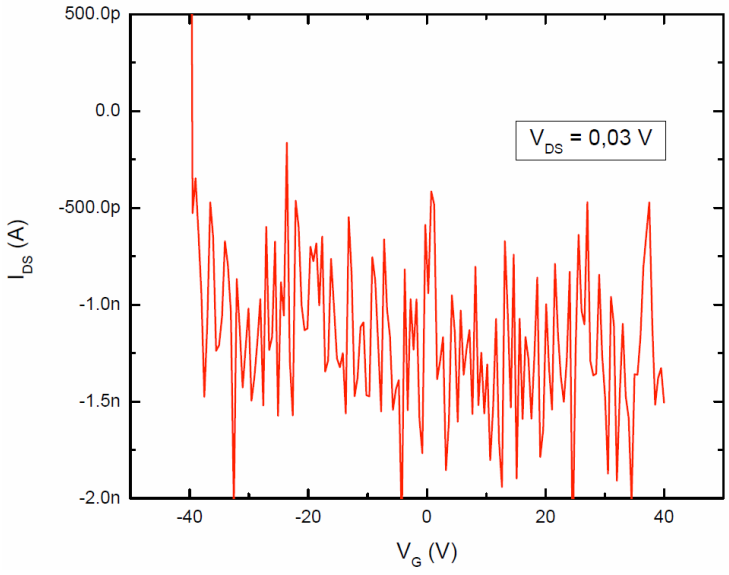
Figure 4.4. . SEM micrograph of 13A doped LBF GaAs nanowire in e-beam lithography-defined MOSFET configuration. Contact 1 is source electrode, contacts 3 and 5 are drain electrodes while contacts 2 and 4 work as gate electrode. Back gate is applied via conductive substrate

We started the work with 13A doped LBF GaAs nanowires. Figure 4.4 shows example of typical nanowire-based MOSFET in dual back gate and top gate configuration.

The source electrode (contact 1 in Figure 4.4) was grounded while the electrodes 3 and 5 were alternatively used as drain and biased with respect to source. Electrodes 2 and 4, as well as the substrate were alternatively used to apply gate voltage and to estimate field effect. Figure 4.5 shows the results.



a)



b)

Figure 4.5. Transconductance back gate measurements for 13A doped LBF GaAs nanowires in case of a) optical lithography and b) e-beam lithography.

Resistivity, mobility and carrier concentration for these nanowires are already calculated in Chapter 3, in case of both optical and e-beam lithography fabricated devices. Here, we will comment on significant difference in shape of

transconductance curve, depending on the fabrication method. In the case of optical lithography-based device, a change of the conductance as a function of the applied gate voltage can be observed. We plot results directly obtained by changing the gate voltage and (black line on 4.5 a)) and the values obtained from the I_{DS}-V_{DS} curve under different gate voltages (red line on 4.5 a)) on the same graph. Both measurements are in good agreement, and they prove that the wires are p-type. However, due to doping inhomogeneity issues dealt within Chapter 3, the exact shape of the curve was irreproducible. Most of the samples showed lower or even negligible gate response. In e-beam fabricated samples, the gate response is always negligible, as showed in Figure 4.5 b). The nanowires used in the optical lithography samples exhibited lengths of 10-12 μm. Consequently, those nanowires exhibit a shorter average diameter compared to the 20 μm or even longer nanowires used for e-beam lithography-based study. For equal inter-contact distance, a smaller diameter will result in higher resistance. This results in stronger back gate bias induced changes in current for optically-fabricated samples. In the case of e-beam fabricated samples, resistance per length was up to an order of magnitude lower (see Chapter 3) resulting in practically negligible transconductance, not only in the case of back gate but also for top gate. This result is in agreement with the quasi metallic behavior of highly doped GaAs nanowires as described in Chapter 3.

Figure 4.6 and 4.7 display I_{DS}-V_G curves measured on 11.5 A doped LBF GaAs nanowires.

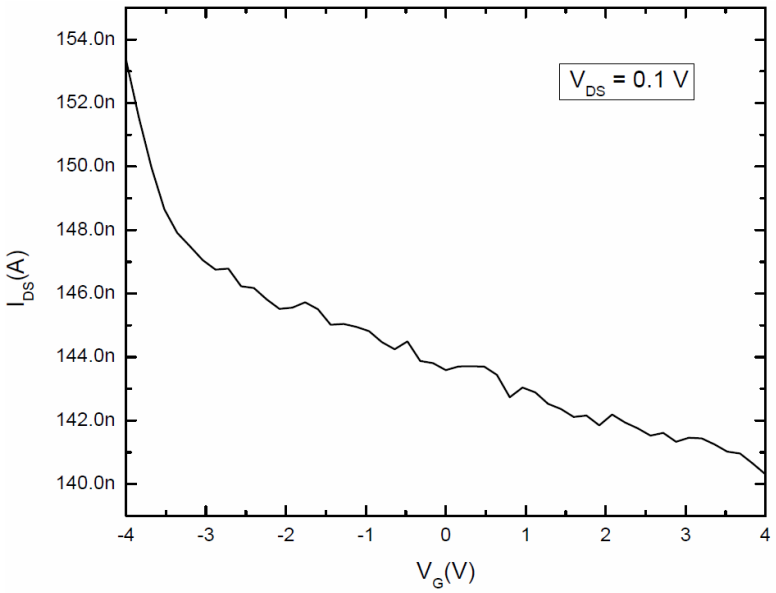
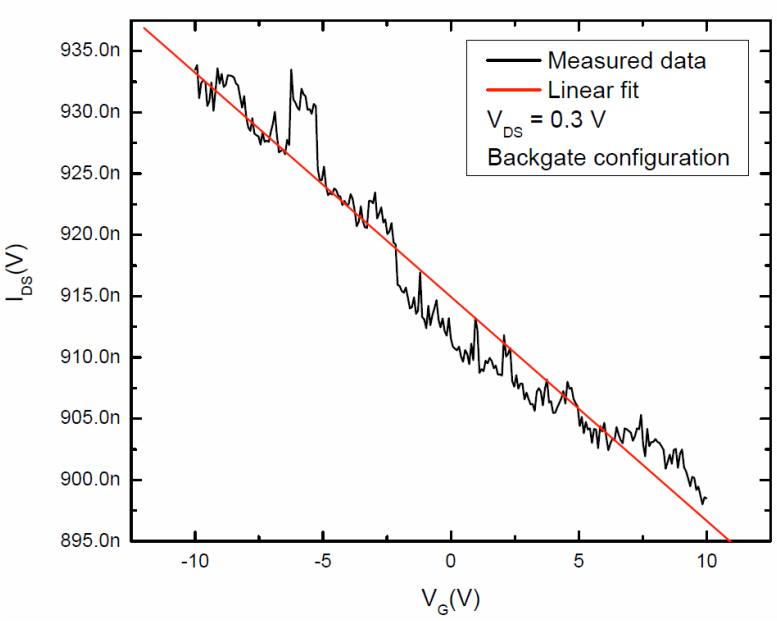
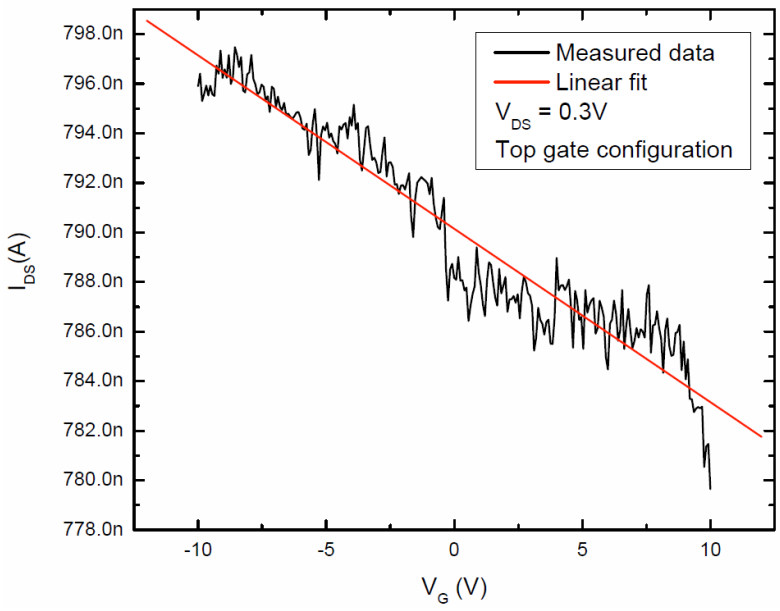


Figure 4.6. I_{DS}-V_G graphs for 11.5 A doped GaAs nanowires in case of optically contacted samples.



a)



b)

Figure 4.7. I_{DS}-V_G graphs for 11.5 A doped GaAs nanowires in case of e-beam contacted samples. a) and b) show samples for back gate and top gate configuration, respectively. Results are measured on same nanowire.

As we have already shown with I_{DS}-V_{DS} curves measured on 11.5 A doped LBF GaAs nanowires (Chapter 3), the gate response is improved compared to highly doped (13A) nanowires. Both optically and e-beam processed samples show clear gate effect. We attribute this to lower (p-type) doping and, consequently, lower concentration of free carriers (holes). The reaction to back gate is more pronounced in case of optically-fabricated samples, even though V_{SD} is 3 times lower (0.3 V for e-beam-fabricated samples and 0.1 for photolithography-fabricated samples). This is most likely due to longer channel in case of optical mask, resulting in stronger influence of back gate bias. Furthermore, the back and top gate response measured

on same nanowire (Figure 4.7 a) and b)) are also different. Surprisingly, the field effect for the back gate configuration is stronger although back gate architecture includes thicker gate oxide (50 nm). This is most likely due to influence of contact resistance. As we will show later, global back gate bias is influencing contact resistance stronger than the top gate bias (Figure 4.8). We have already reported a value for resistivity, mobility and carrier concentration for 11.5 A doped samples fabricated using optical lithography in Chapter 3 and the following paragraphs discuss them for e-beam-fabricated samples.

We have demonstrated earlier the existence of non-negligible contact resistance in case of 13 A doped nanowires. Here, in case of 11.5 A LBF GaAs nanowires, due to shorter length with respect to highly doped nanowires, we were not able to fabricate 4 contacts and the top gate on same nanowire. Consequently, we were not able to strictly exclude contact resistance from measurements. We applied the assumption that under high drain to source bias Schottky barrier becomes negligible (see Chapter 2). We assume that the resistance measured in these conditions is equal to the nanowire resistance. Contact resistance is derived by measuring corresponding total lower bias resistance and deducing nanowire resistance from it. Figure 4.8 shows an evolution of contact the resistance with respect to drain to source voltage.

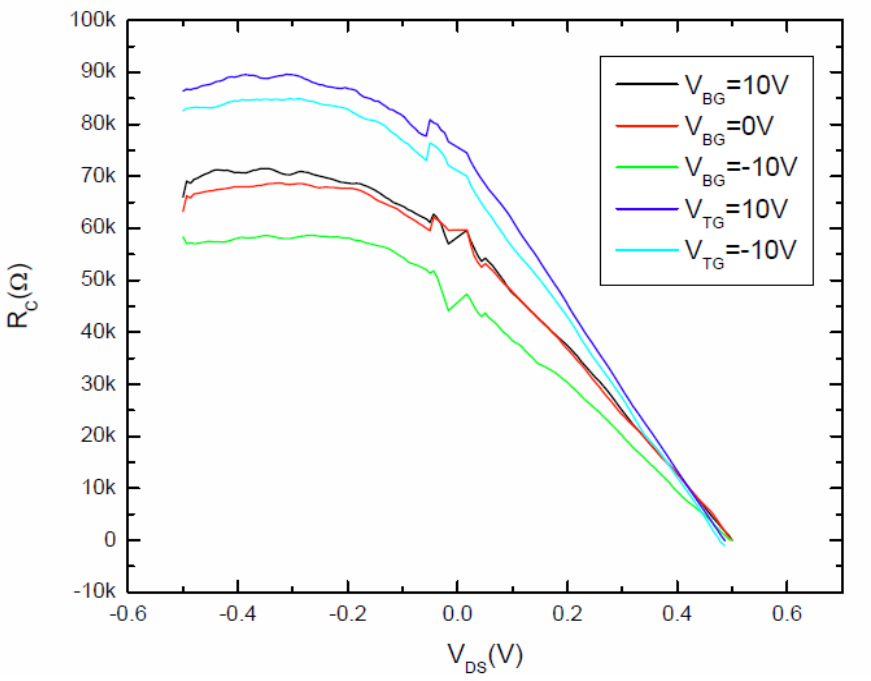


Figure 4.8. Evolution of contact resistance with respect to drain-source voltage. Influence of back gate is stronger than influence of top gate, especially for V_{DS} lower than 0.2 V

The global back gate is influencing contact resistance as well. The top gate configuration will be discussed later.

As a crucial difference with respect to analysis reported in Chapter 3, additionally to calculations reported in Figure 4.8, here we will apply the more precise model to

estimate the resistivity. In a first approximation, we assumed homogenous doping and a cylindrical nanowire. Furthermore, we included tapering effect only by calculating an average diameter and assuming constant diameter being equal to this value. Under these approximations, resistivity was calculated using the simple ratio for resistance of cylinder, equation (3.2). However, as described in section (3.3.d), we have been faced with non- homogeneous doping and dominant side facets doping of the nanowire. To account for this geometrical doping a more precise calculation is applied, taking into account the fact that current dominantly flows through the doped shell. Here, we will increase precision by assuming nanowire is not a cylinder but a cone, the geometry closer to the actual form of the nanowire.[35]

Figure 4.9 shows proposed cone geometry and cross sections.

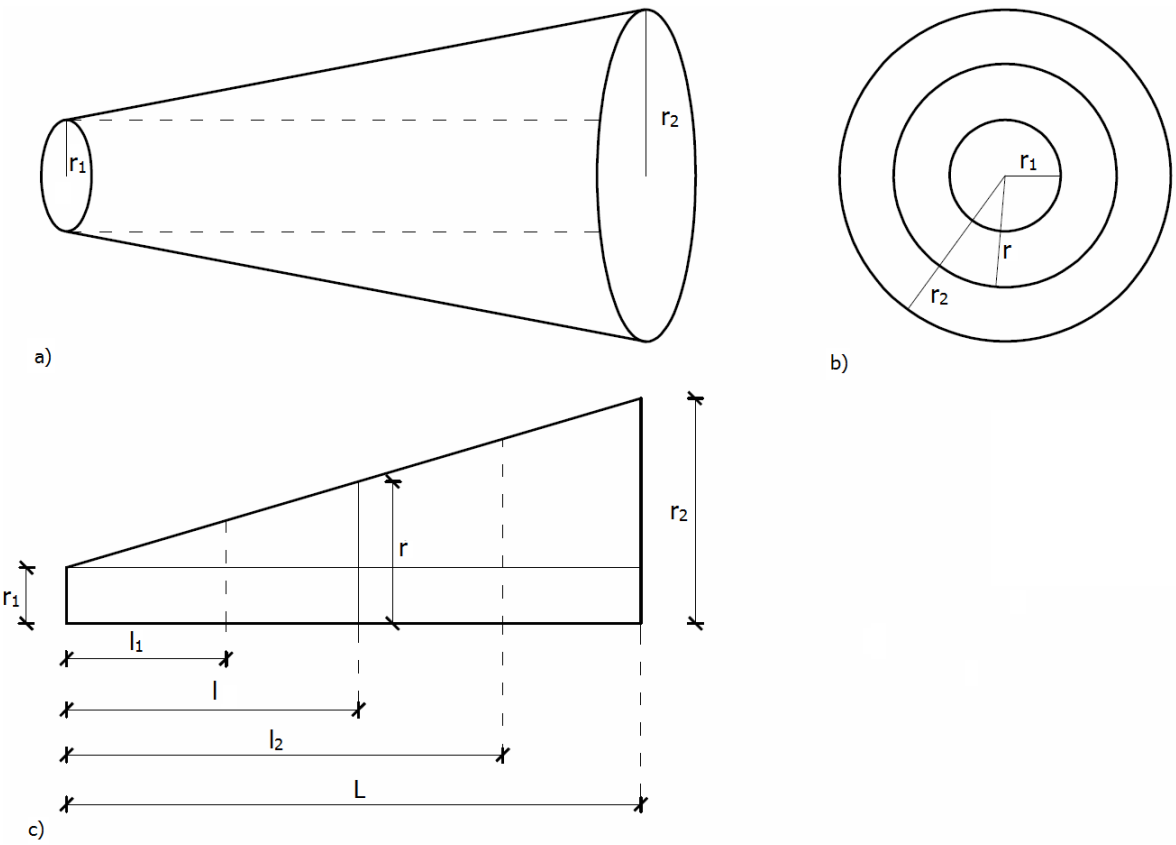


Figure 4.9. a) Proposed conical nanowire geometry, b) top view and c) side cross section

E-beam lithography-fabricated contacts are placed on locations l_1 and l_2, see Figure 4.9 c). For V_{DS} = 0.3 V (at V_{GS} = 0) resistance of 310.9 kΩ is measured (Figure 4.10), resulting in resistance per length of 66.57 kΩ/μm.

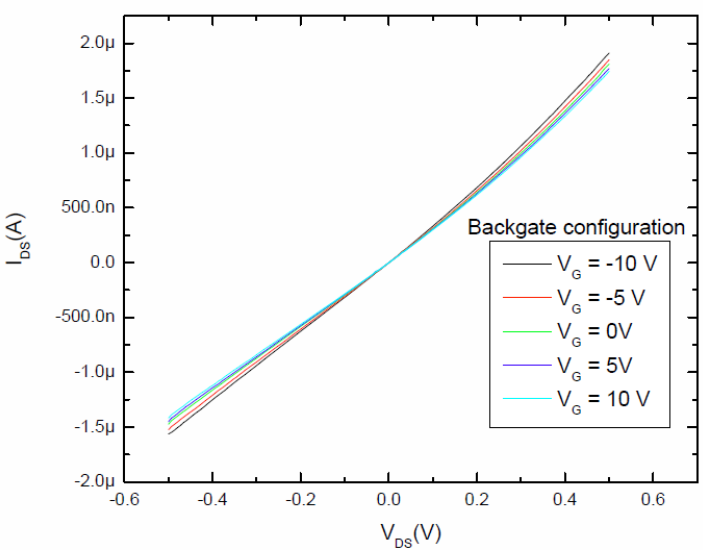


Figure 4.10. I_{DS}-V_{DS} characteristics of 11.5 A doped LBF GaAs nanowire.

Deducing the corresponding contact resistance of 23.5 kΩ from the measurements of Figure 4.8 we obtain a nanowire resistance (R_{NW}) of 287.4 kΩ. We can start the analysis using the nanowire resistance for geometry proposed in Figure 4.9 and extract the material resistivity. The nanowire resistance can be analytically obtained from the following expression:

$$R_{NW} = \int_{l_1}^{l_2} \frac{\rho}{S(l)}\, dl, \tag{4.1}$$

where ρ, l and S stand for resistivity, length and cross section surface, respectively. Resistivity is assumed to be constant, and, therefore, not being dependent of integration path. If we assume current location l so that $l_1 \leq l \leq l_2$ as defined in Figure 4.9 the corresponding radius r is well defined. The effective cross section surface for a radii r will be given by:

$$S = r^2\pi - r_1{}^2\,\pi \tag{4.2}$$

Where r_1 is a nanowire diameter on the tip side and therefore a constant, and r is a variable. Considering that r_2 is the radius of the nanowire on base side and L is total nanowire length and analyzing Figure 4.9. c), we see that the triangle with catheti L and r_2-r_1 is similar to the triangle with catheti l and r-r_1. Due to similar triangles theorem, we can write:

$$\frac{r_2 - r_1}{L} = \frac{r - r_1}{l} \quad \rightarrow \; r = \frac{l}{L}(r_2 - r_1) + r_1, \tag{4.3}$$

Combining (4.2) and (4.3) we obtain this expression for cross section surface:

$$S = \frac{l^2}{L^2}(r_2 - r_1)^2\pi \; + 2\,\frac{l}{L}(r_2 - r_1)\, r_1 \tag{4.4}$$

As we can see from (4.4), all parameters, except l, are constants, making this suitable for integral in (4.1). Introducing (4.4) to (4.1) and using full square method we obtain integral of the form $\int \frac{dx}{x^2 - a^2}$ whose solution is:

$$R_{NW} = \frac{-\rho L}{2r_1\pi(r_2 - r_1)} \ln\left|1 + \frac{2r_1 L}{(r_2 - r_1)l}\right|_{l=l_1}^{l=l_2} \tag{4.5}$$

Introducing integration borders, we obtain following:

$$R_{NW} = \frac{-\rho L}{2r_1\pi(r_2 - r_1)} \ln \frac{l_1 l_2(r_2 - r_1) + 2r_1 L l_1}{l_1 l_2(r_2 - r_1) + 2r_1 L l_2} \tag{4.6}$$

Finally, knowing the nanowire resistance (R_{NW} = 287.4 kΩ for inter-contact distance of l_2-l_1 = 4.67 μm) and measuring radii and length with SEM, we can obtain a resistivity of 3.75 x 10^{-4} Ωm. Applying the calculation explained in Chapter 3, equations (3.3) – (3.8), we can obtain following parameters: the back gate capacitance is 4.15 x 10^{-16} F, the hole mobility 50 cm^2/Vs while carrier concentration has value of 3.33 x 10^{18} cm^{-3}. We would like to remind the reader that all values of the hole mobility calculated for optically fabricated 11.5 A doped LBF GaAs nanowires (3.3. c)) lie within range of 5-9 cm^2/Vs. Values for samples obtained by means of e-beam lithography, combined with more exact calculus, show a clear

improvement compared to samples containing nanowires grown within the same growth session but processed by means of the optical lithography.

The analysis discussed so far is dealing with GaAs-nanowire-based MOSFETs in back gate configuration. Strictly speaking, the same approach cannot be applied for top gate configurations. Using previous approach, we are able to calculate resistivity and top gate capacitance. The mobility must be estimated in a different way, as we will show in following calculation*.

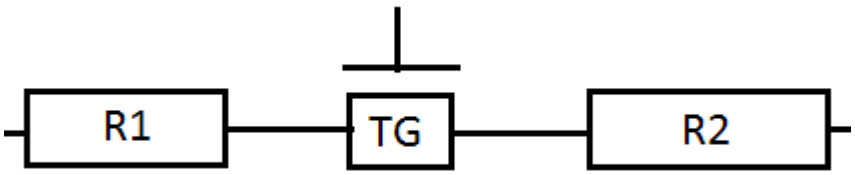


Figure 4.11. Schematics representation of nanowire based MOSFET in top gate configuration. Assuming contact resistance is eliminated, resistors R_1 and R_2 represent segment of channel not covered by top gate. Variable resistor TG represents part of channel under the top gate. Non symmetries in schematics are done on purpose, to stress non-ideal device fabrication

Prior to presenting the calculations, we will shortly comment on Figure 4.11. The key difference between this model and one discussed in Chapter 3 is the existence of resistors R_1 and R_2. These elements represent segments of nano-MOSFET channel which is not covered by top gate and, due to this, is not influenced by bias applied across it. In case of previously discussed back gate configuration, the entire channel is influenced by the gate. Calculus, where R_{NW}^{TG} is the top gate induced resistance, is derived as follows:

$$V_{DS} = R_{TOT} I_{DS} \tag{4.7}$$

$$= R_{NW}^{TG}\, I_{DS} + (R_1 + R_2)\, I_{DS} \tag{4.8}$$

$$= \frac{L_G^2}{\mu C_G (V_{th} - V_G)}\, I_{DS} + R_{12}\, I_{DS} \tag{4.9}$$

$$= \left[\frac{L_G^2}{\mu C_G (V_{th} - V_G)} + R_{12}\right] I_{DS}. \tag{4.10}$$

We should note that L_G in these equations stands for gate length, not the nanowire length (L), as in equations (4.3) – (4.5). Finally, we obtain a drain to source current expression:

$$I_{DS} = \frac{1}{\frac{L_G^2}{\mu C_G (V_{th} - V_G)} + R_{12}} V_{DS}. \quad (4.11)$$

The variable in this equation is V_G, L_G is measured from SEM images, while C_G can be calculated from equation (3.3). However, μ, V_{th} and R_{12} are obtained from data fit done on 4.6 c) using equation (4.11). Note that in case of negligible R_{12} we have same equation as in case of back gate.

As already pointed out, resistivity and top gate capacitance can be calculated from (4.6) and (3.3), respectively. Values obtained are 3.75 x 10^{-4} Ωm and 4.15 x 10^{-16} F. However, the equation (4.11) is a non-linear function of V_G. We were not able to fit the data reported on Figure 4.7 b) with this function by the time of thesis submit. Further numerical analyses should be performed as a part of future work in order to calculate μ, V_{th} and R_{12} and quantitatively estimate performance of top gate MOSFETs based on 11.5 A LBF GaAs nanowires.

At the end of this subchapter, we will comment on results obtained on GaAs nanowires grown with lowest doping level, meaning, current used for heating Si source during the growth was 10 A. Nanowires were grown under low beam flux conditions (LBF). As in case of 11.5 A doped nanowires, both back gate and top gate configurations have been achieved. Figures 4.12 and 4.13 show transfer characteristics of 10 A doped LBF GaAs nanowires.

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*Help of Dr. Joseph Dufouleur is kindly acknowledged

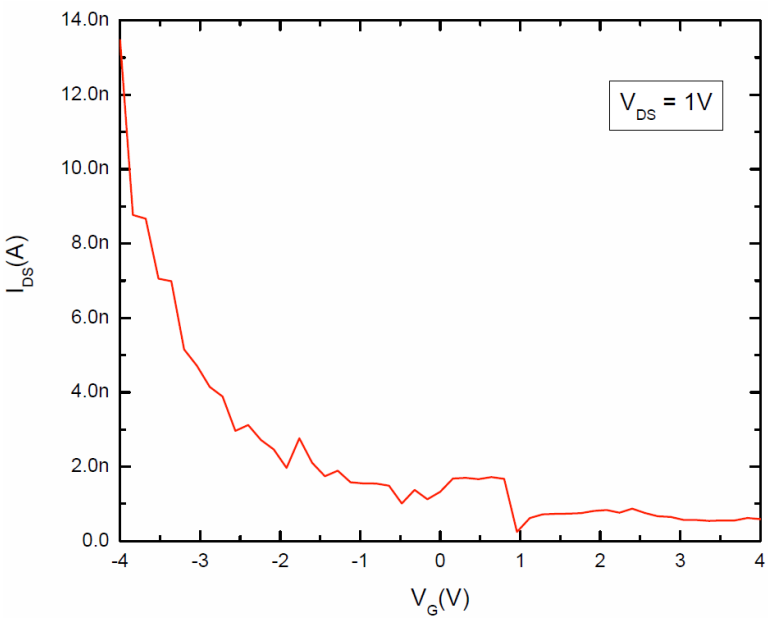
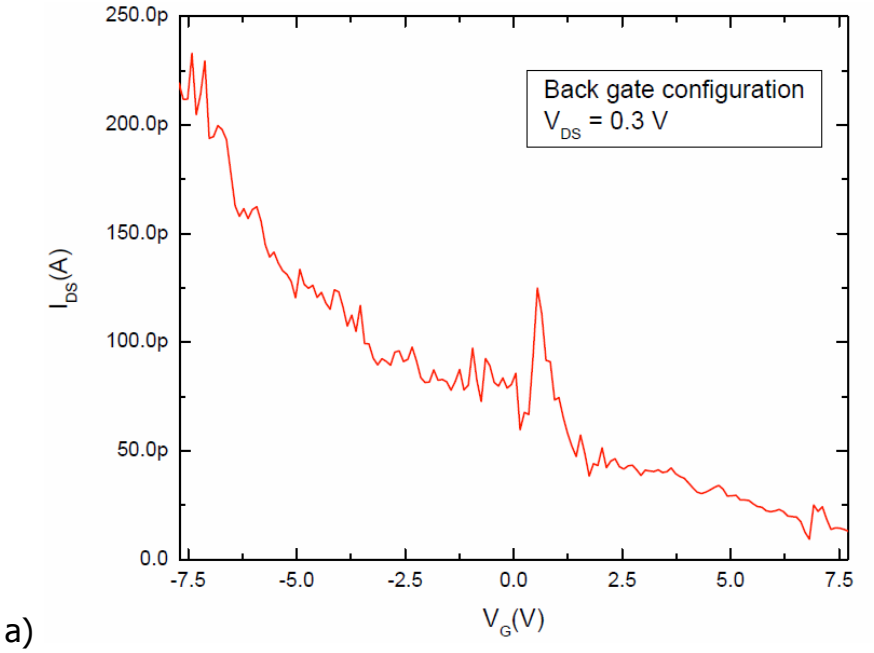
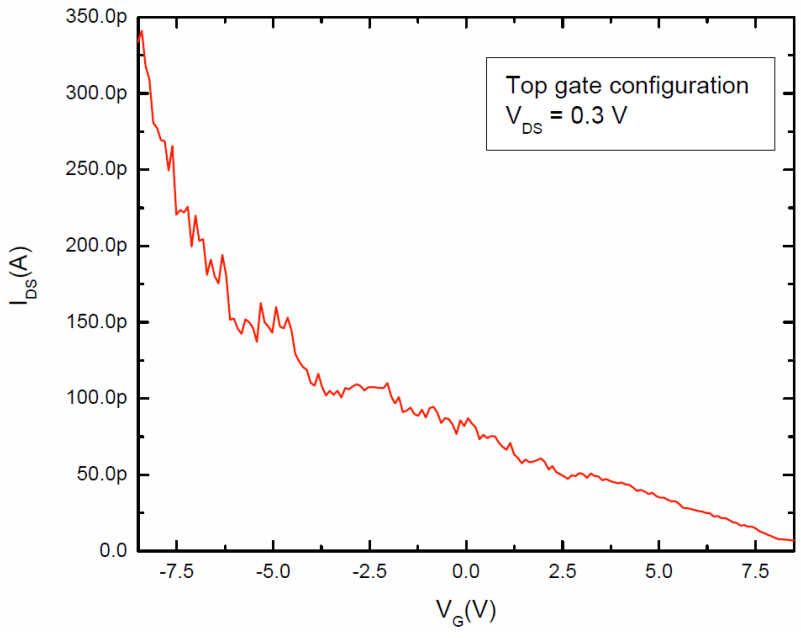


Figure 4.12. I_{DS}-V_G graph for 10 A doped GaAs nanowires in case of optically contacted samples.

Analyzing the measurements of the Figures 4.12 and 4.13 we clearly see already reported p-type behavior of GaAs nanowires. However, in case of 13 A doped nanowires, gate response was low and overall behavior quasi metallic, see chapter 3. As we showed previously in this Chapter, 11.5 A doped nanowires exhibited improved field effect, but a clear transition from ON to OFF transistor state (Chapter 1) could not be detected. From Figure 4.12 and 4.13 we can conclude that no matter which fabrication method or gate configuration was used, 10 A LBF GaAs nanowire based MOSFET reaches an OFF state. We should point out that we define an OFF state as current of magnitude close to or under the set up resolution. Furthermore, comparing currents measured on optically and e-beam fabricated devices for same gate configuration (back gate), one observes non-negligible differences. We attribute this to different channel geometries and V_{SD} bias. In case of MOSFETS fabricated with optical lithography, the channel is longer, resulting in stronger influence of bias applied between back gate and source. Moreover, we used V_{SD} = 1 V while measuring I_{DS}-V_G curves, while for MOSFETS fabricated via e-beam lithography the value used was 0.3V.



a)



b)

Figure 4.13. I_{DS}-V_G graphs for 10 A doped GaAs nanowires in case of e-beam contacted samples. a) and b) show samples for back gate and top gate configuration, respectively. Results are measured on same nanowire.

However, the differences are also measured on same nanowire in case of back gate and top gate configuration. Comparing Figure 4.13 a) and b), we conclude that top gate configuration results in stronger field effect for same bias applied. For instance, a back gate source voltage equal to -5V results in a drain-source current of 150 pA.

In theh same conditions, but in back gate geometry, the measured drain-source current is 125 pA. Differences in transconductance are probably due to thinner gate dielectric of top gate geometry (< 10 nm with respect to 50 nm for the back gate) as well as due to differences in dielectric constant (9.1-9.8 for Al_20_3, depending on purity, compared to 3.9 for SiO_2).[53,56] Both a thinner oxide and higher dielectric constant result in a higher gate capacitance, leading to ahigher gate response, see equation (3.8).

Resistivity, mobility and carrier concentration for 10A doped GaAs devices fabricated optically were reported earlier in Chapter 3. Here we continue with same type of calculation for devices produced via e-beam lithography. The calculation of the resistivity is based on the measurements reported in Figure 4.14. We will start the analysis with MOSFETs in back gate configuration.

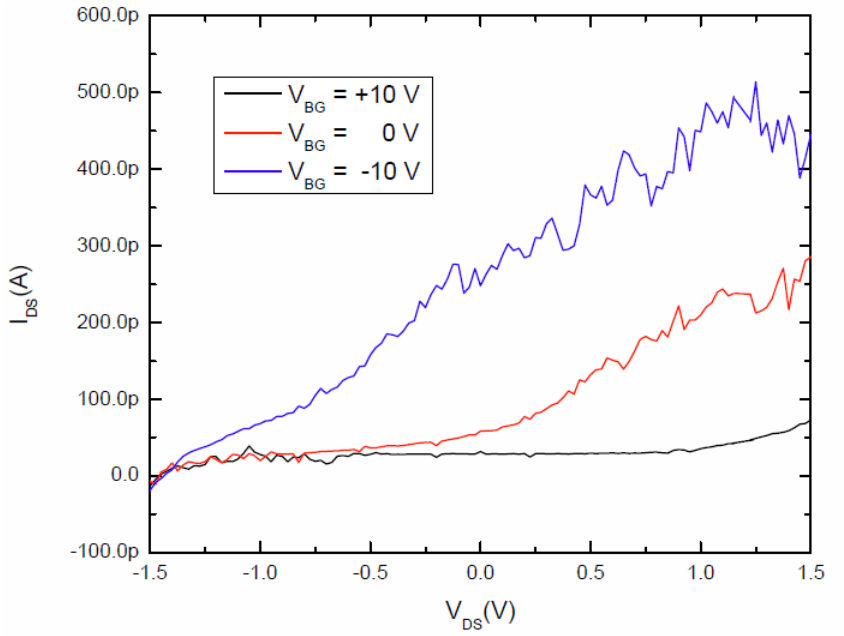


Figure 4.14. Transport properties of 10 A doped LBF GaAs nanowires. gate bias is applied in back gate configuration.

Unlike 13 and 11.5 A doped GaAs nanowires, 10 A doped nanowires exhibit very low conductance. Obviously, reducing the heating current from 11.5 A to 10 A significantly reduces the incorporation of Si atoms during the nanowire growth (Chapter 2). As a consequence of this, we expect a lower carrier concentration resulting in higher global resistance. The previously presented model of the dominantly doped shell and dominantly intrinsic core will not be used because of the lower doping level. Instead of that, we will assume carriers are homogeneously distributed, as if nanowires are undoped. Moreover, since 10 A doped nanowires exhibit the shortest length ($\leq$ 5 μm), the cone geometry introduced for longer 11.5 A doped nanowires is less pronounced and can be neglected. In conclusion, the

effect of tapering will be taken into account by introducing the average diameter, while simple cylindrical geometry and homogeneous doping will be considered for the resistivity calculation.

A detailed analysis of contact resistance performed on 11.5 A doped nanowires, Figure 4.8, indicates values bellow 75 kΩ in lowest V_{DS} bias conditions. In an extremely conservative approximation, contact resistance for 10 A doped nanowires can be considered to be an order of magnitude higher, which is still well below 1 MΩ. We chose treshold of 1 MΩ as a value 3 order of magnitude lower than total resistance. We assume every contribution being lower than that value is too low and therefore negligible. Two-point resistance measured on 10 A doped nanowires is around 5.4 GΩ leading to resistance per length of 1.3 GΩ/μm. Taking into account value of resistance, we conclude with high level of certainty that any additional resistance with contribution bellow 1 MΩ can be neglected. We can than omit the influence of contact resistance in the further analysis. Considering an average diameter of 95 nm and inter-contact distance of 4.097 μm, the obtained value of resistivity is 933.2 Ωcm. This value is quite high, confirming strongly reduced doping. From equation (3.3) we calculated back gate capacitance of 8.03×10^{-16} F. Knowing this value, and applying it to equation (3.8), hole mobility is calculated, obtaining a very low value (0.014 cm^2/Vs). Finally, using equation (3.5), we calculated carrier concentration equal to 4.78×10^{17} cm^{-3}. As assumed previously, carrier concentration is significantly reduced compared to 13 A and 11.5 A doped nanowires (5×10^{18} cm^{-3} and 3.33×10^{18} cm^{-3}, respectively). Although exhibiting clear field effect and OFF state, possible application in more complex device architectures is challenging due to very low mobility and high resistance per length.

As a simple illustration of this statement, let us assume the following circuit configuration. Standard ON current in conventional CMOS technology is of order of μA.[54] For resistance per length equal to 1.39 GΩ/μm and standard CMOS channel length of 45 nm, we would obtain channel resistance of 63 MΩ under zero gate bias conditions. ON current in range of μA would result in estimated Joule's heating equal to 63 μW. Considering only 10^6 transistors per integrated circuit will lead to matrix of so called hot-spots with total emitted heat of 63 W. Obviously, normal operation of such a circuit would require additional passive cooling system increasing total dimension, or an active cooling system increasing total consumption. Both solutions are not favorable in terms of the possible applications. A reasonable step forward in the research towards possible applications of these nanowires would be analyzing nanowires with a novel doping current level, combining low resistance of 11.5 A and high gate response of 10 A doped LBF GaAs nanowires.

The analysis of MOSFETs in top gate configuration is omitted, due to reasons explained for 11.5 A doped nanowires. As it has already been pointed out, top gate I_{DS}-V_G curve (Figure 4.13 b) is a non-linear function of V_{DS}, and should be fitted using equation (4.11). By the time of thesis submit, this could have not been

achieved. A possible solution could be using software tools specifically designed for non-linear data fitting, instead of general purpose software.

4.5. Conclusion

Metal-oxide field-effect transistors (MOSFETs) fabricated from single GaAs nanowires grown under low beam flux conditions (LBF) were reported. We analyzed gate response on three types of GaAs nanowires, in highly doped (13 A of heating current), moderately doped (11.5 A), and in low doped (10 A) samples. For all levels of doping both back gate and top gate architectures are achieved and compared. The 13 A doped nanowires exhibited negligible field effect in both configurations. Resistance of 11.5 A doped nanowires is higher compared to 13 A doped nanowires, but field effect is more pronounced, not only for back gate, but also for top gate geometry. The best results in terms of gate bias response have been achieved for 10 A doped nanowires. Both back and top gate configurations exhibited OFF state. Field effect is better for top gate due to thinner gate oxide. However, it also results in very high resistance per length and low mobility. A reasonable step forward in future work would be fabricating a MOSFET out of 11 A doped GaAs nanowires. These wires should have higher conductance than 10 A doped nanowires as well as better response to gate bias with respect to 11.5 A doped nanowires.

5. Electrical properties of germanium nanowires

5.1. Introduction

Although from historical point of view first widely used semiconductor material, Ge was suppressed by silicon which is basic building element of today's semiconductor industry. However, interest in germanium is being reactivated again because of high carrier mobility.[57-60] Moreover, recently a very interesting type of heterostructures consisting of a germanium nanowire with a silicon shell has been demonstrated.[61] Due to the band alignment between silicon and germanium, this kind of heterostructure leads to the accumulation of holes in the core of the nanowire. Such a structure is ideal for the study of one-dimensional related phenomena, as well as for high mobility applications.

In this chapter, we will focus on the electrical characterization of germanium nanowires. The nanowires have been synthesized with three different catalysts: gold, bismuth and indium. We will compare the electrical properties of the nanowires obtained with the different catalyst materials. We will measure I-V characteristics, determine nature of gate dependence in FET configurations, calculate resistivity, mobility and carrier concentration.

5.2. Device fabrication

Here we briefly present two fabrication methods we have used to create electrical contacts on the germanium nanowires: optical and electron beam lithography. The advantages and disadvantages of each technique will be discussed and compared. A criterion of major importance will be influence of fabrication process on the properties of the nanowires. For instance, by exposing the nanowire to high-voltage-accelerated electron beam, one can create surface or impurity states significantly altering the electrical performance of the future device. The second issue that will be presented are the metal layers used for the contacts.

5.2.a. Optical lithography. Initial results.

Our initial germanium nanowires were contacted using positive optical lithography. Figure 5.1 illustrates the process of fabrication. First, the nanowires were removed from the growth substrate and transferred onto a highly n-doped Si substrate coated by SiO_2. Transfer itself is done either by mechanical methods (sharp tips) or by combination of mechanical and liquid transfer (sonication). An optical mask with sets of two contacts separated by 1.5, 3, 5 and 7 μm was used. After the transfer, the sample was cleaned with acetone and isopropanol in order to remove particles of

dust remaining after transfer. Then, it was sputtered with 36 nm of SiO_2, in order to improve the adhesion between the nanowires and the substrate. After that, the optical lithography process was realized. After developing the exposed pattern, the sample was cleaned with O_2 plasma to remove residual photo-resist layer.

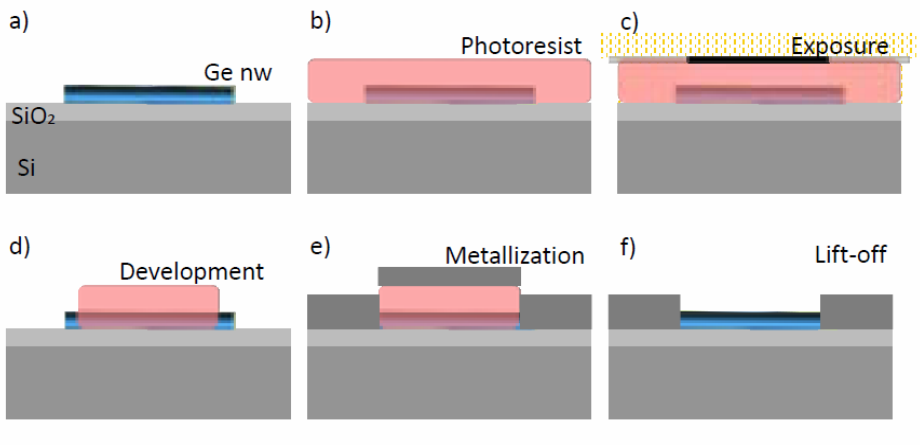


Figure 5.1. Process flow for optical lithography. a) Wire transfer. b) Surface cleaning, spin coating, and softbake. c) Exposure, d) Resist development and etching e) Metallization, and f) Lift-off. Figure is taken from [40].

Prior to the evaporation of metals for contacting (Fig. 5.1 e)), samples were treated with wet-etching to remove native oxide layers from Ge nanowires. This step plays a vital role in terms of future contact quality. As we found out after detailed studying of literature[62], Ge nanowires show two types of oxide, GeO and GeO_2 which both needed to be removed. Unlike nanowires with Au as catalyst, Bi catalyzed nanowires exhibit amorphous shell which also required special etching steps. After 300 s long oxygen plasma etching at 200 W (removal of photo-resist residuals), the samples were dipped in diluted hydrofluoric acid ($HF:H_20=1:2$) for 20 s to remove the sputtered SiO_2. An additional 60s etching step in DI water removed GeO_2. The amorphous Ge shell was etched for 10 s in 30% hydrogen-peroxide (H_2O_2). Since GeO is created by the contact of germanium with DI water, we needed to apply final 30 s diluted hydrofluoric acid etching step. After that, the contacting metals were evaporated (15 nm Ti + 100 nm Pd + 10 nm Au) and lift-off performed.

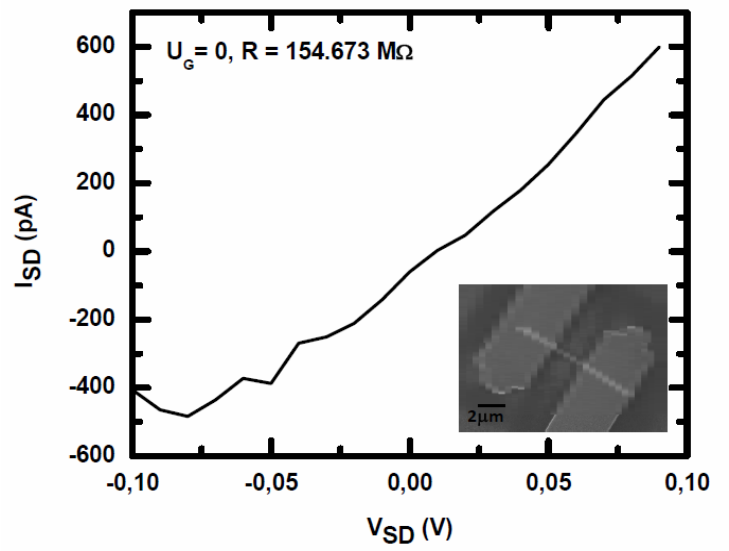


Figure 5.2. I-V curve at zero gate voltage of a Au catalysed germanium nanowire contacted via optical lithography. The inset illustrates a SEM micrograph of a contacted nanowire.

In Figure 5.2, the output transport characteristics of a gold catalyzed germanium nanowire contacted via standard optical lithography is reported. Quasi-Ohmic contacts have been fabricated using titanium, palladium and gold for both source and drain. The gate contact was applied via the substrate (back gate). For V_{SD} sweep from -0.1 to 0.1 V, in presence of zero gate voltage, we observed resistance of more than 150 MΩ. Knowing that inter-contact length used was 1.5 μm, we obtain resistance per length of around 100 MΩ/μm. Unfortunately, the characteristic is not ideal linear curve, especially in the range between -0.1 and -0.05 V. These nonlinearities are most likely coming from nature of contact which could not be further improved by optical lithography based process. As we pointed out in Chapter 3, use of optical lithography is restricted to the fabrication of micron-sized structures. It is because of this why nanowires must have length of at least several microns. Moreover, only 2 contacts per nanowire can be fabricated. For high resistive samples like our Ge nanowires, this is a further disadvantage. Electron beam lithography technique allows the fabrication of contacts in much closer distances, resulting in easier measurements for high resistance samples. This technique allows also the contacting of smaller nanowires and fabricating more than two contacts on the same nanowire.

5.2.b. Electron beam lithography

Details of electron beam lithography (EBL), including exact protocols can be founded in the Chapter 2 and in the Appendix. Here, we point out only most important aspects, necessary for following rest of the text.

Highly n-doped silicon substrates covered with 200nm of SiO_2 have been used. Prior to EBL, Ti/Au (20/200 nm, respectively) macroscopic contacts have been defined on

the sample surface via optical lithography, metallization, and lift-off process. The defined e-beam writing field consists of 20 contacts that border a square of 130 µm x 130 µm. Nanowires were mechanically transferred onto the mentioned squares using a sharp tip. After the transfer, the samples were cleaned with acetone/isopropanol dipping and sputtered with 36 nm of silicon dioxide. After that, the samples were spin-coated with double layer PMMA electro-resist. Prior to the e-beam lithography process, the nanowire positions were determined by means of optical axioscopy, geometry measurement, followed by coordinate transformation. Finally, a proper development technique was applied followed by cleaning steps exactly same as described in 5.2.a) with only one exception, shorter O_2-etching step (55 s). This is

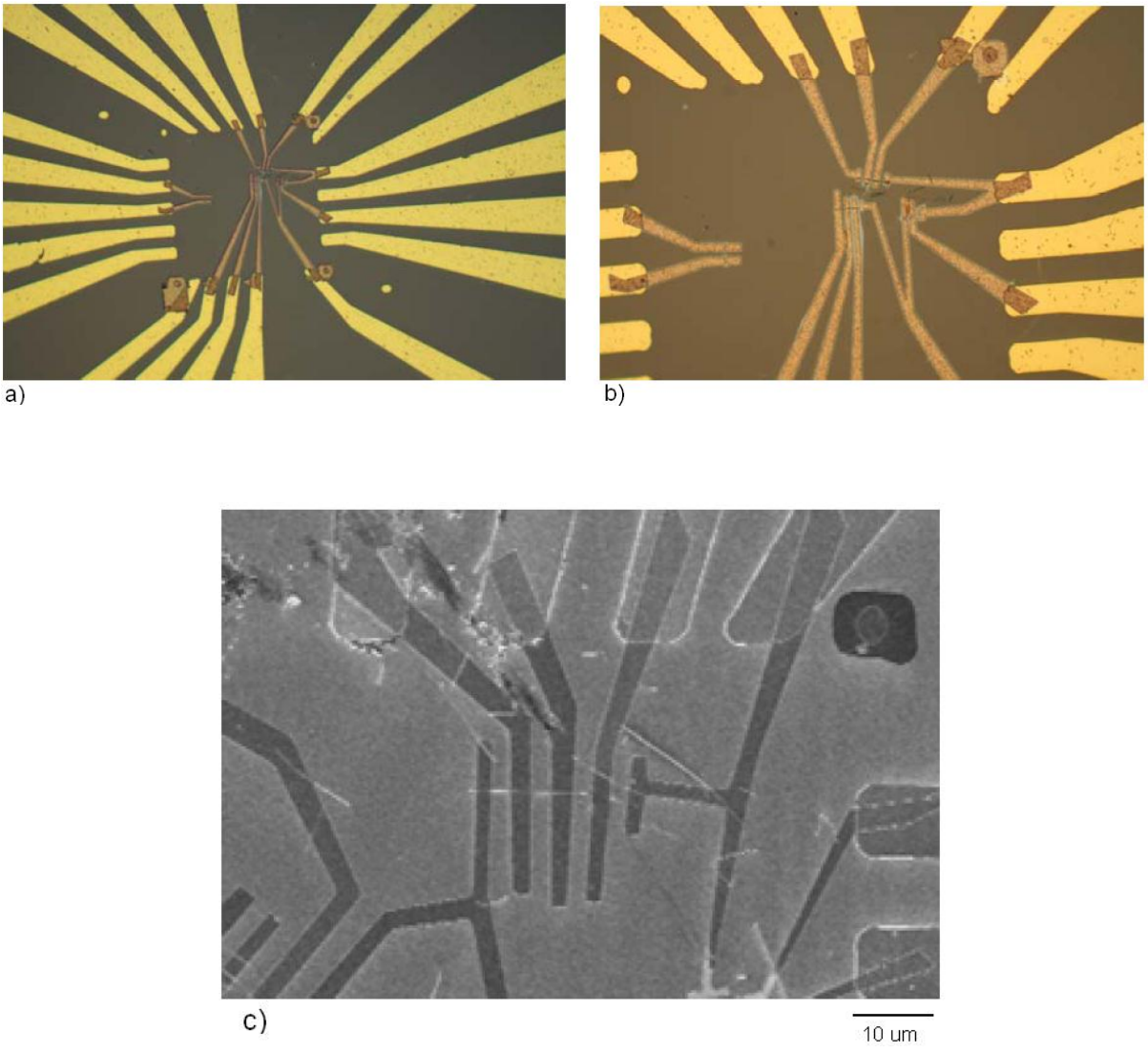


Figure 5.3. Germanium nanowires contacted via E-Beam lithography: a) Writing field including optical pre-step and final e-beam step, magnification 20X. b) Zoomed optical image showing 2 contacted Ge nanowires, magnification 50X. c) SEM micrograph showing single Ge nanowire contacted with e-beam lithography, magnification 330X.

done since electro-resist (PMMA) exhibits higher sensitivity to O_2-etching compared to photo-resist. Since we evaporated different combination of metal layers, that segment will be discussed separately. Figure 5.3 reports typical example of Ge nanowires contacted by e-beam technique.

5.3. Contacting materials and annealing study

5.3.a. Au catalyzed Ge nanowires

For the germanium nanowires obtained with gold as a catalyst, the contact material systems explored contacts were:

- 100 nm Pd + 10 nm Au
- 15 nm Ti + 100 nm Al + 10 nm Ti
- 15 nm Ti + 100 nm In + 10 nm Au
- 15 nm Ti + 100 nm Bi + 10 nm Au

Source and drain contacts created using palladium and gold were reported in literature to create Ohmic contacts in gold catalyzed germanium nanowires.[58] We have chosen total metal thickness of 110 nm to ensure a complete coverage of the nanowire ends. Moreover, aluminum, indium, and bismuth have been investigated as contact materials. A thin titanium layer of 15nm underneath the contact material is serving as adhesion layer, and importance of this step for successful lift-off was already discussed in previous chapters. The thin Au layer on top of the contact material serves as oxidation protection. Our transport experiments clearly verify that Pd and Au serve the best as ohmic contact materials for this type of Ge nanowires. On the other hand, nanowires contacted with In and Bi based metal contacts how clear Schottky behavior. Surprisingly, Al was not working at all. All transport experiments performed using nanowires contacted with Ti/Al/Ti show properties of an ideal insulator. I-V curves showing transport behavior of Au catalyzed Ge nanowires are reported in 5.4.

5.3.b. Bi catalyzed Ge nanowires

An Ohmic I-V characteristic can be observed for germanium nanowires obtained with bismuth as a catalyst when the sequence 15nm of Ti, 100nm of Bi, and 10nm of Au is used as source and drain contacts. Considering that Bi acts as n-dopant in the Ge nanowire, Bi should form highly n-doped regions to create ohmic contacts to the nanowire. Further investigation in existing literature resulted Ti/Cu metal combination which was also proven to result in Ohmic contacts.[63] Analogous to Au catalyzed Ge nanowires, first Ti layer improves adhesion, while final Au layer protect

contact from oxidation. The intermediate metal diffuses in the nanowire, enabling the Ohmic characteristic. For Ti/Cu combination, we observed similar behavior with and without Au. The transport results will be discussed later in this chapter.

5.3.c. In catalyzed Ge nanowires

Ge nanowires synthesized with indium as catalyst exhibit thick amorphous shell. Only about 20 nm thin core of the nanowire is crystalline. In order to electrically characterize these nanowires, amorphous shell needed to be etched prior to contact metalisation. Doing this would enable direct contact between conductive core and metal. Unfortunately, thickness of the shell as well as etching rate of hydrogen-peroxide was not well investigated. Due to this, intermediate amorphous layer was always located between metal contact and crystalline core, creating an insulating shield. It is because of this why we could not observe any transport behavior on these nanowires. Future investigations should lead towards better understanding of etching rate and enable actual contact between metal and crystalline core, without intermediate insulating layer. Once that is made possible, reasonable combination for contacting layers would be 15 nm Ti, 100 nm In and finally 10 nm Au.

5.3.d. Annealing study

Annealing is a technique often used on contacted structures in order to obtain Ohmic characteristics. Annealing should lead to the diffusion of metal into the semiconductor, which should result in the high doping of the interface with the metal. This makes the tunneling of carriers from the contact to the semiconductor easier and often leads to Ohmic characteristics. Our contacts have been annealed in a home-made rapid thermal annealer under N_2 forming gas atmosphere. The annealing temperature has been chosen slightly above the eutectic temperature between the semiconductor and the contacting metal. A systematic annealing time study has been performed for each material with the annealing time varying between 5 s and 5 min. In general, only Ti/Cu metal layers show improvement. For all other combinations of metals different sample morphology has been observed after annealing, independent of the materials used. In Figure 5.4, a SEM image in a) and an optical image in b) of a typical outcome of annealing steps are shown. In most of the cases, the contacts were peeled off the surface, as shown in a).

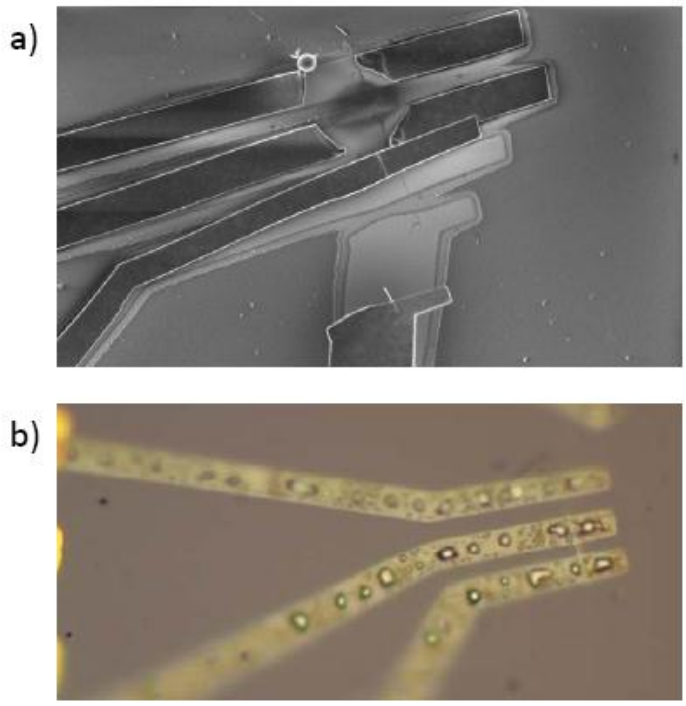


Figure 5.4. a) SEM and b) optical image showing the sample surface after annealing. a) displays example of sample for which metal heterolayer (15 nm Ti/ 100 nm Bi/ 10 nm Au) separated while b) presents example of situation where metal heterolayer (100 nm Pd/ 10 an Au) form droplets. Figure is taken from [40].

Different metal layers used for the contacts seem to separate one from another and the contacts seem to break. In most cases, this happens at the nanowire-contact interface.

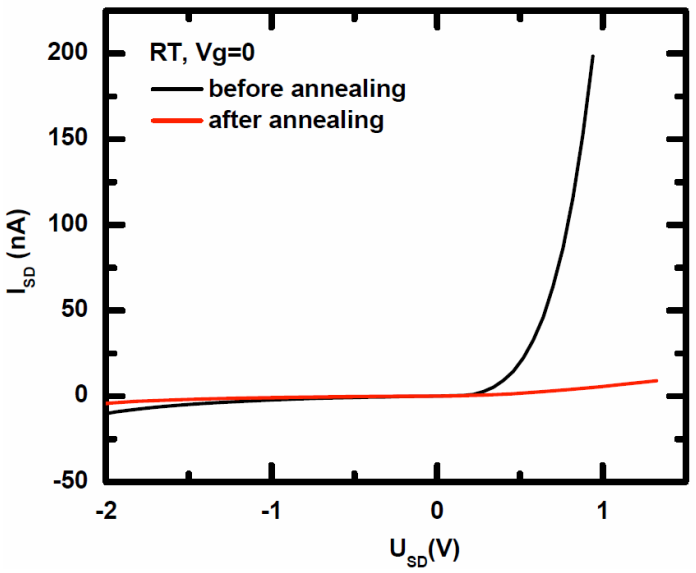


Figure 5.5. I-V characteristics of Au catalyzed Ge nanowire before and after annealing. Contacting metals are 100 nm Pd + 10 nm Au

A possible explanation for this could be the different coefficients of thermal expansion of different materials. Moreover, even the transport properties of nanowires whose contacts did not separate (Figure 5.4. b)) do not exhibit relevant improvements. In figure 5.5 we report the transport characteristic of an Au catalyzed Ge nanowire annealed for 30 s at 370 °C. Here, the room temperature two-terminal source-drain characteristic is shown at zero gate voltage. Figure clearly shows Schottky behavior prior to annealing (black curve). After the annealing procedure was completed, same nanowire was re-measured. Obtained results (red curve on Figure 5.5.) show improved linearity, but strongly reduced conductance. Current response to same bias feed becomes 2-3 order of magnitude lower, suggesting partially pealed contacts and/or thermally destroyed nanowire (figure 5.4). Obviously, contact properties were not improved.

However, as we pointed out on previous page, annealing results are significantly better for Bi catalyzed nanowires when contacting metal combination is consisted of Ti/Cu (15 nm/155 nm, respectively) layers. As it can be seen on Figure 5.6, for specified material combination metal-nanowire bond does not break.

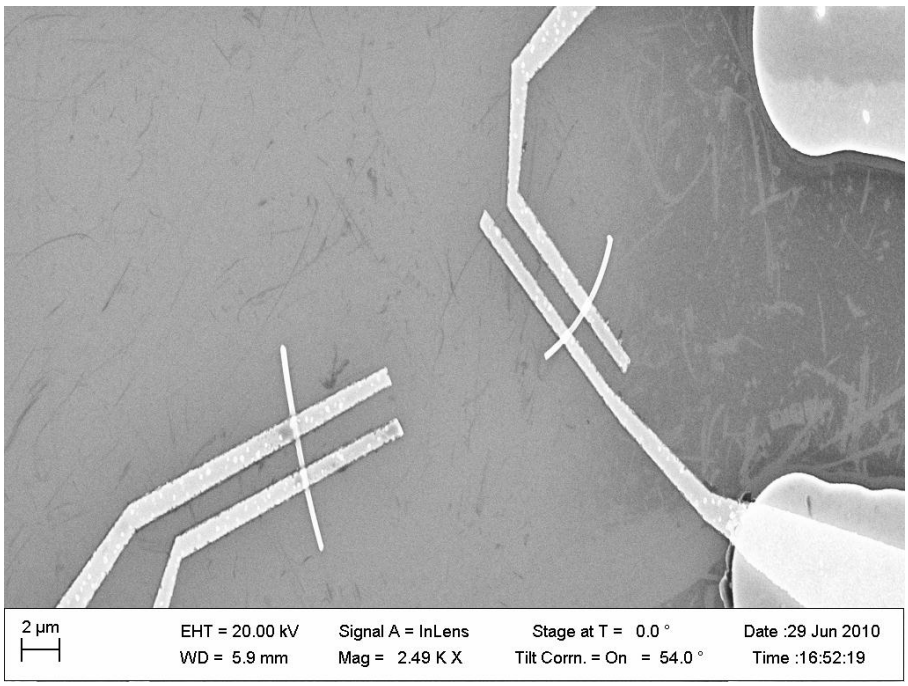


Figure 5.6. SEM image of Bi catalyzed Ge nanowires contacted with 15 nm of Ti and 155 nm of Cu, after successful annealing

Samples were annealed for 1 minute at 310 °C. In order to verify effect of annealing step, we did initial transport measurements. Figure 5.7 reports those measurements, showing clear improvement.

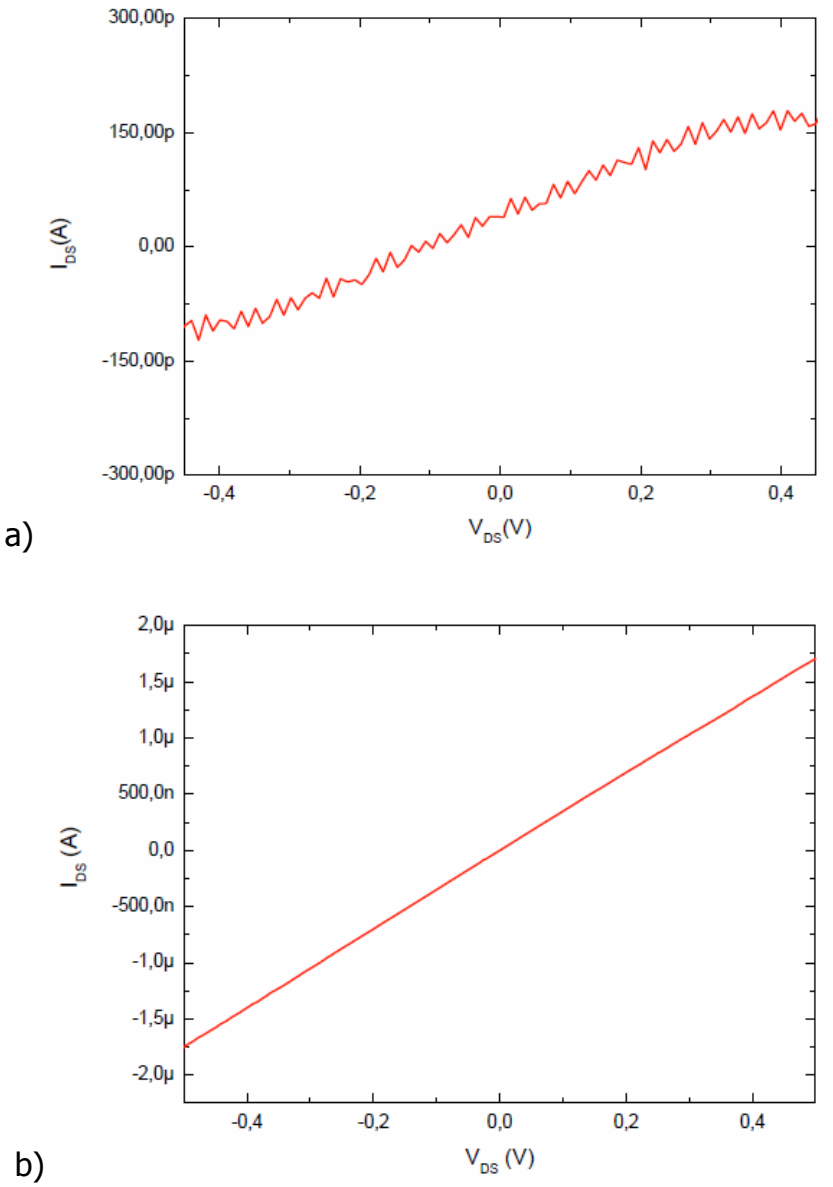


Figure 5.7. I-V characteristics of Bi catalyzed Ge nanowires a) before and b) after annealing for 60 s at 310 °C. Contacting metal layer is 15 nm Ti and 155 nm Cu

Already before annealing, this contacting recipe shows better response in terms of both conductance and linearity. Furthermore, after the annealing under the above described conditions, both of the parameters improved. We achieved very high linearity of current response to same bias, obtained characteristics is regular and symmetric, indicating a good Ohmic contact. Moreover, conductance seems to be drastically improved from range of 100 pA to range of 1 µA. Annealing procedure is obviously improving overall transport properties for Bi catalyzed Ge nanowires in

case of Ti/Cu based contacts. According to literature[63], this is due to formation of quasi-metallic copper-germanide (Cu_3Ge) leading to atomically sharp interfaces.

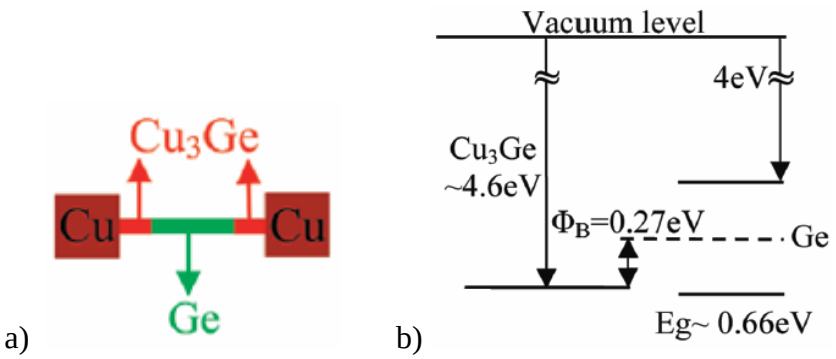


Figure 5.8. a) The schematics of the contacted NW. Brown fields denote the Ti/Cu contact pads, red is the Cu_3Ge segment, while green shows the residual intrinsic Ge nanowire. b) Band relation between the Cu_3Ge contacts and the intrinsic Ge. Figure is taken from [63].

Formation of Cu_3Ge is induced by axial diffusion of copper. Expected barrier height of ~0.06 eV (Figure 5.8) with respect to the valence band of germanium enables Ohmic contacts to p-type Ge nanowires.[63]

5.4. Measurements, device performance and analyses

After finishing the fabrication, the sample was mounted on a the 3 –point needle probe station setup. Source-drain voltage (V_{SD}) vas applied and the source-drain current (I_{SD}) measured by a Keithley 6487 voltage source – picoammeter characterization unit. The gate-source voltage (V_{GS}) was controlled by a Keithley 2611 single channel sourcemeter.* Schematic drawing of measuring set-up is same as for the GaAs nanowires, figure 3.2.

The source-drain current through the nanowire was measured as a function of the bias voltage (V_{SD}) and the gate voltage. Based on the output and transfer characteristics of the devices, we evaluated their properties. We will separately discuss the germanium nanowires obtained with gold as a catalyst from the ones obtained with bismuth. All measurements were done at room temperature.

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*Note that we did exactly opposite for GaAs nanowires. Due to higher resistivity, Ge nanowires are easier to characterize with higher internal impedance device, which, out of two mentioned, is Keithley 6487.

5.4.a. Germanium nanowires obtained with gold as a catalyst

In order to enable electrical measurements, 100nm of Pd and 10nm of Au were evaporated on both ends of the nanowire. As we have already mentioned, the heavily n-doped silicon substrate was used as backgate electrode, while 200nm of thermally grown SiO_2 served as gate dielectric. The output characteristic (I_{SD}-V_{SD}) of an elementary device based on gold catalyzed germanium nanowire is given in Figure 5.9. The output characteristic was measured for different gate voltages varying in range between -10 V and 20 V. The I_{SD}-V_{SD} curve shows linear behavior and calculated resistance per length for V_{SD} sweep between -80 and 80 mV with gate voltage switched off has value slightly bellow 2 MΩ/μm. The I-V curve remains linear for negative gate voltages. Contrary, for positive voltage applied between gate and source electrode, the transport characteristic becomes non-linear. For V_G = 10 V, MOSFET reaches off-state and current reaches set-up resolution limit. The transfer characteristic (I_{SD}-V_G) is shown in Figure 5.10.

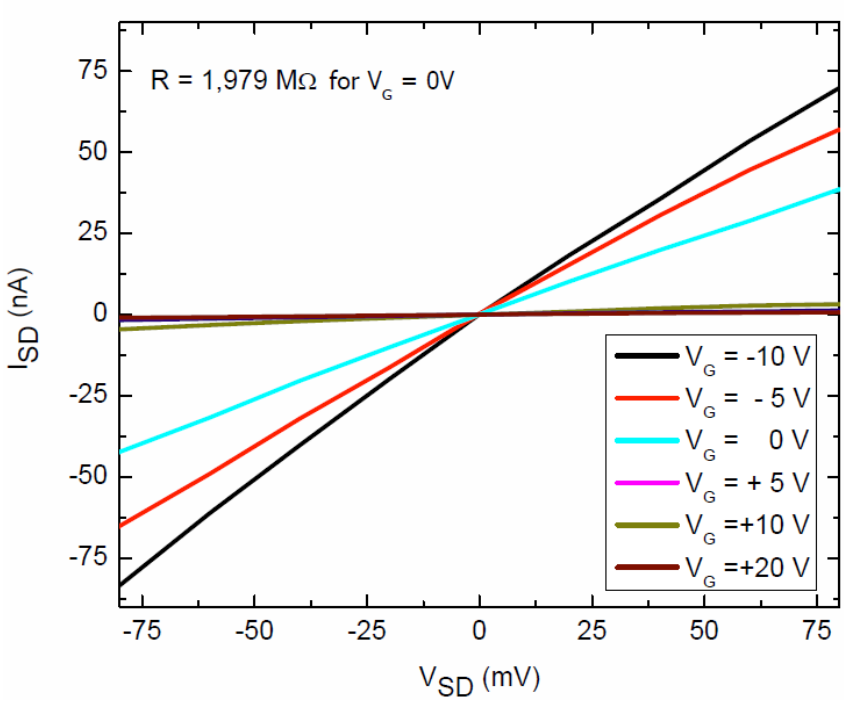


Figure 5.9. I_{SD}-V_{SD} room temperature characteristics of Au catalyzed Ge nanowire

The behavior depicted in graph is comparable to a p-channel MOSFET. As shown in the graph, by increasing the gate voltage from -10V to 20V, the source-drain current strongly decreases, showing clear transistor effect. From the output characteristic and the transfer characteristic we can calculated several parameters for operation for

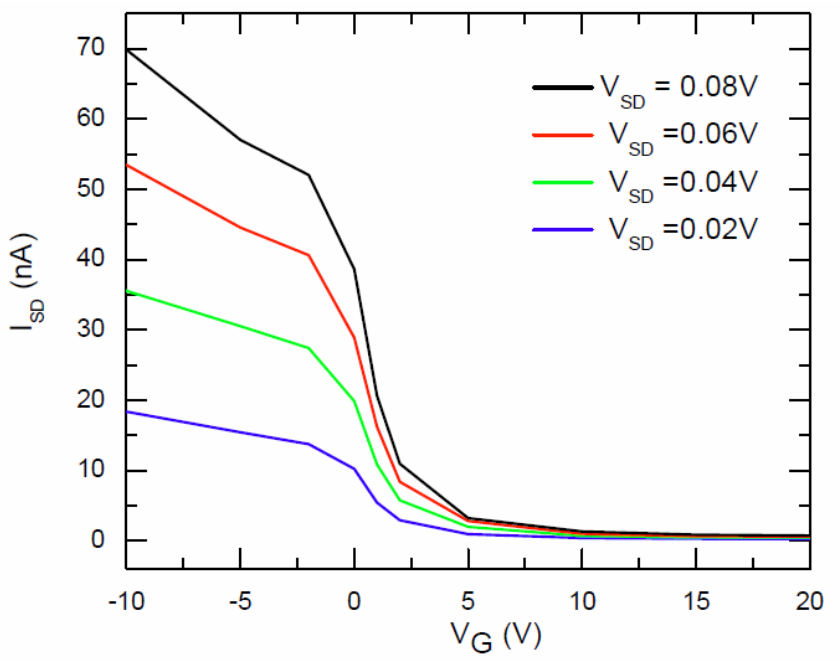


Figure 5.10. I_{SD}-V_G room characteristics of Au catalyzed Ge nanowire

this type of transistor. To begin with, both characteristics demonstrate a field effect behavior. Moreover, the electrical transport through the nanowire is dominated by positive holes. It is because of this why channel seems to be p-type, operating in depletion mode, normally on. The linear behavior in the output characteristic suggests that we have fabricated good contacts to the device. However, we could not produce four contacts and more reliably confirm that the resistivity of the contacts was much smaller than the one of the nanowire.

To estimate the hole density, the capacitance consisted of the conducting channel, the back gate and the SiO_2 gate dielectric was considered. If we assume that the entire nanowire consists of crystalline germanium contributing to conduction, and that the nanowire is cylindrical, we can apply calculus discussed in Chapter 3, equations 3.2. – 3.8. Using that, the gate capacitance can be estimated and obtained value is $C_g = 3.3x10^{-16}$ F. The carrier mobility μ can be estimated from eq. 3.8. In the case of gold catalyzed germanium nanowires, for V_{SD} =0.02 V, the calculated hole mobility is μ = 40.5 cm^2/Vs. This value is significantly below the equivalent mobility of bulk Ge (1900 cm^2/Vs) and it suggests that the nanowire contains a large number of scatterers, such as defects. Another source of reduced mobility could lie in the roughness at the nanowire-gate oxide interface, and the existence of surface trap levels.[64] Additionally, from I-V characteristics for zero gate voltage (figure 5.9) we calculated resistivity and obtained value of 1.13 Ωcm. Finally, using eq. 3.5, we can extract carrier concentration to value of $1.37x10^{17}$ cm^{-3}.

5.4.b. Germanium nanowires obtained with bismuth as a catalyst

The second type of field effect devices based on germanium nanowires were fabricated Ge nanowires obtained with bismuth as a catalyst. As so far, the back gate configuration was used, with 200nm of SiO_2 as the gate dielectric. We evaporated 2 different metal heterolayers, Ti/Bi/Au (15 nm/100 nm/10 nm, respectively) and Ti/Cu (15 nm/155 nm, respectively) to obtain source and drain contact pads. Both cases will be presented separately. Prior to metallization, both source and drain contacts were carefully treated with different solutions, as it is described in optical lithography section (5.2.1). The obtained output characteristic is shown in Figure 5.11 and 5.13.

Figure 5.11 shows I_{SD} versus V_{SD} ,for gate voltages between 20 V and -20 V. For all gate voltages, the source-drain current increases with an increased source-drain voltage, at first linearly, but then starts to saturate, reaching so called on-state. At V_G = 0, for V_{SD} sweep from 0 to 2 V, we calculated resistance of 7.6 MΩ.

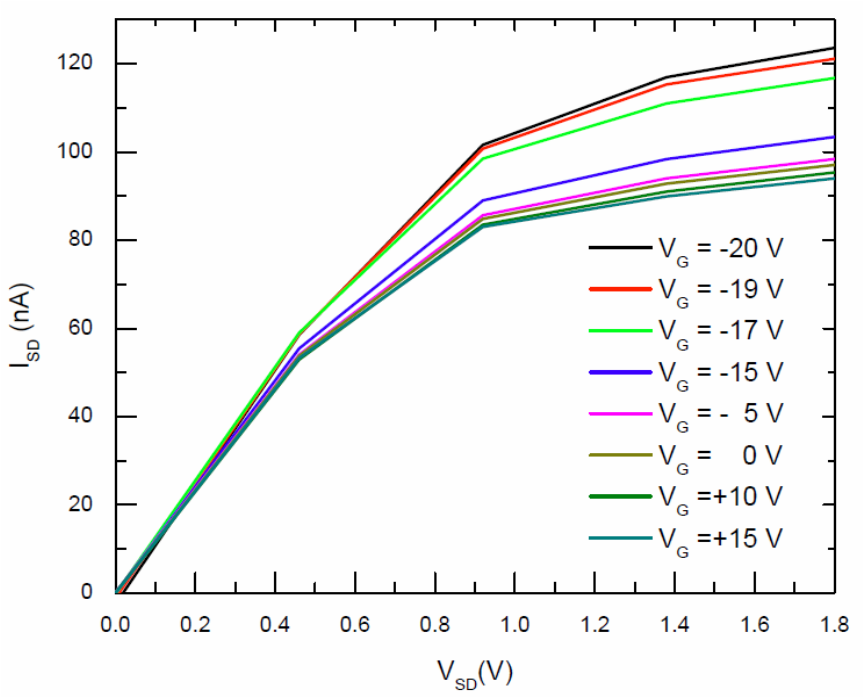


Figure 5.11. Two-terminal source-drain currents versus source-drain voltages of a bismuth catalyzed germanium nanowire.

For separation distance between 2 contacts of 1.5 μm, this gives resistance per length equal to 5.1 MΩ/μm. The value of the on-current and the linear behavior indicates that good contacts were formed to the conducting channel. Still, analogous to the case of Ge nanowires obtained with Au as catalyst, we could not produce 4 working contacts to verify this assumption. When the gate voltage is decreased from

0 V to -20 V, the conductance increases. The output characteristic shows the operation of the device comparable to operation of a field effect transistor. The carriers dominating in the transport are found to be holes. The Ge nanowire based MOSFET operates in p-channel depletion mode, normally on. A gate capacitance of C_g = 3.17x10^{-16} F was obtained from equation 3.3. The transfer characteristic of the Bi catalyzed Ge nanowire at V_{SD} = 1.84 V is shown in Figure 5.12. From this plot, the threshold voltage was estimated to have an approximate value of -14V. Assuming cylindrical geometry of the nanowire, the resistivity ρ is 12 Ωcm. Again, using equation 3.8, a hole mobility of μ= 1.2 cm^2/Vs was obtained. Moreover, a hole density of p = 4.4x10^{17} cm^{-3} could have been determined from eq. 3.5. The carrier density is about four times larger than equivalent for gold catalyzed germanium nanowires. This conclusion becomes reasonable if one compares the I_{SD}-V_{SD} characteristic of both nanowires. In the case of gold catalyzed nanowires, at a very low source-drain voltages (between -80 mV and +80 mV), the conductance depends on the gate voltage significantly, indicating a lower carrier concentration. In the case of Ge nanowires obtained with Bi as a catalyst, the influence of the gate voltage on the conductance is much weaker, which indicates a higher carrier concentration inside the channel. However, measurements show that the positive carriers dominate the

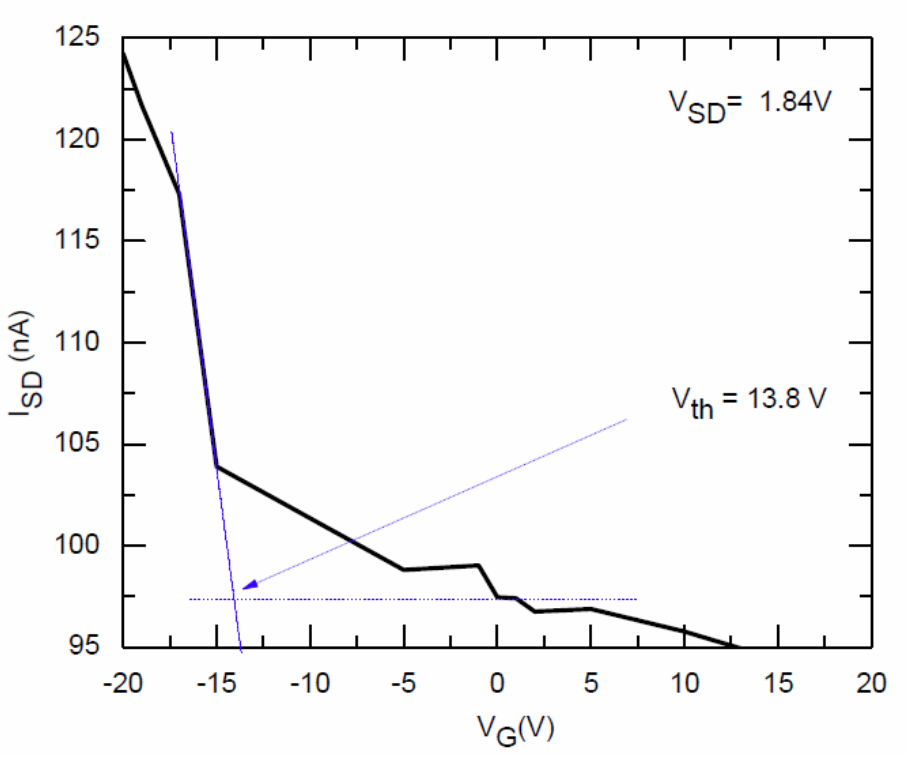


Figure 5.12. Transfer characteristic of Bi catalyzed Ge nanowire. A linear fit was used to estimate the threshold voltage.

conduction while n-doping by the bismuth catalyst during the nanowire synthesis was expected. The absence of electrons as majority carriers can be explained by the low solubility of bismuth in germanium. Since only few Bi atoms are incorporated inside the nanowire, the germanium nanowire shows an almost intrinsic behavior, which usually exhibits residual p-doping. However, measurements show that the positive carriers dominate the conduction while n-doping by the bismuth catalyst during the nanowire synthesis was expected. The absence of electrons as majority carriers can be explained by the low solubility of bismuth in germanium. Since only few Bi atoms are incorporated inside the nanowire, the germanium nanowire shows an almost intrinsic behavior, which usually exhibits residual p-doping.

Due to the linear relation of the carrier mobility to the mean free path, the carrier mean free path is smaller (around 56 nm for Au catalyzed and around 2 nm for Bi catalyzed Ge nanowires) and scattering events inside bismuth catalyzed germanium nanowires occur more often than in gold catalyzed ones. Possible explanation for this could be presence of more defects in those nanowires. It is because of this why further studies have to be done to improve the structural quality of Ge nanowires synthesized with Bi as catalyst. In the high source-drain voltage regime, a field effect has been observed on the nanowire. We could not observe complete channel depletion even at a source-drain voltage of 20 V.

Finally, we would like to present results measured on the Ge nanowires synthesized with Bi as catalyst contacted with Ti/Cu (15 nm/ 155 nm, respectively).

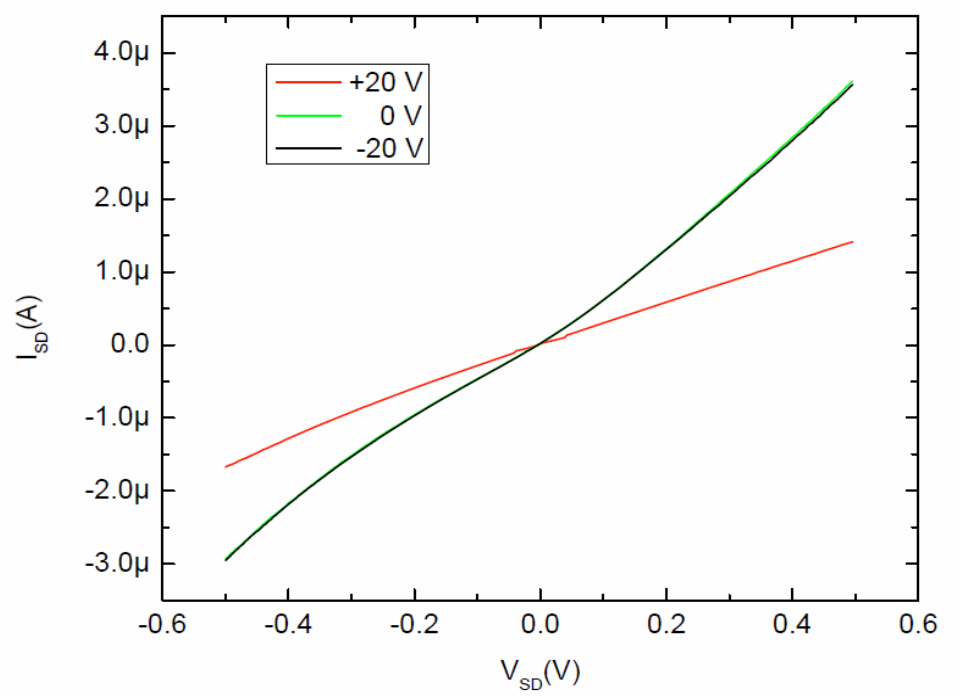


Figure 5.13. I_{SD}-V_{SD} characteristic of Bi catalyzed Ge nanowire contacted with Ti/Cu heterolayer

We are reminding reader we have already reported annealing results for this combination of contacting metals (section 5.4.d) and figure 5.6 and 5.7). However, overall transport behavior is different compared to previously described sample when Ti/Bi/Au contacting heterolayer was used. Differences can be observed in terms of resistance per length, which is 5.1 MΩ/μm for nanowires contacted with Ti/Bi/Au. In case of Ti/Cu based contacts, for zero gate voltage and V_{SD} sweep from -0.5 to 0.5 V (Figure 5.13), we measured values below 200 kΩ, leading to resistance per length of 250 MΩ/μm. The drop in resistance per length for factor of 20 with respect to previously discussed nanowires is most likely due to axial diffusion of Cu atoms into the body of Ge nanowire, leading to creation of quasi metallic Cu_3Ge, see [63]. As described in [63], when applying SEM imaging during the process of annealing, one can observe Cu atoms diffusion, leading to spreading of Cu_3Ge and shrinking of Ge segments on nanowire. An example of the SEM image we took after the annealing procedure is reported in figure 5.14. One can observe darker nanowire zones on the segments in the immediate vicinity of the contact, indicating a different material with respect to rest of the nanowire. This could be evidence of same process as described in [63]. However, further chemical content oriented analyses would be required to confirm this hypothesis.

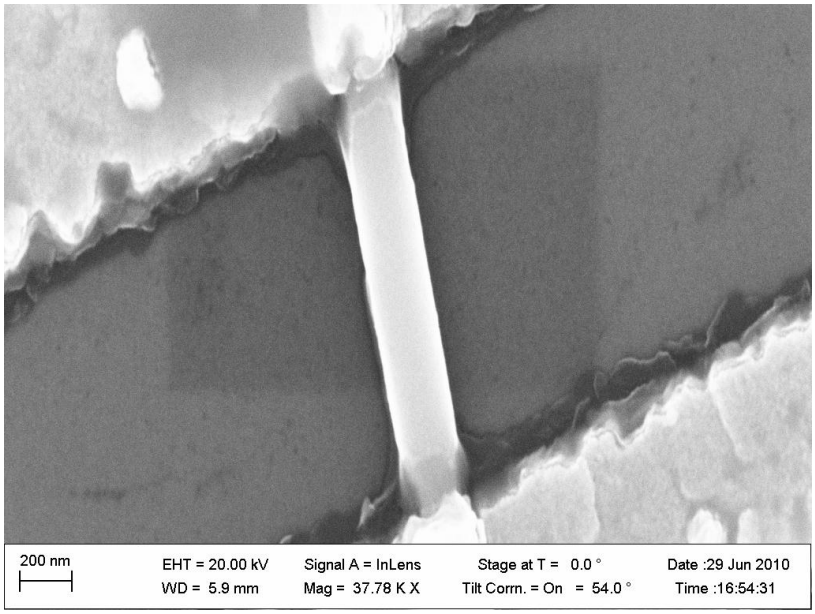


Figure 5.14. SEM micrograph of BI catalyzed Ge nanowire, contacted with Ti/Cu bilayer. Darker segments of nanowire show possible Cu diffusion and formation of quasi metallic Cu_3Ge.

With same geometrical assumption, resistivity can be estimated and obtained value is 0.32 Ωcm. Electrical response is quite linear, but reaction to gate voltage is altered with respect to Bi based contacting heterolayer. For Bi based contacts, negative gate voltage increases conductance significantly, while only small difference between zero and positive voltages is observed. For Cu based contacting layers, measured values are found to suggest exactly opposite. Overall behavior is still p-type, but positive gate voltages significantly reduce conductance while in the same

time no difference between negative and zero gate voltages are detected. Gate capacitance for these nanowires can be calculated in same way as described so far. Obtained value is comparable to previously reported values, 2.16×10^{-16} F. Minor difference is due to slight deviation is intra-contact distance (0.8 μm) and lower oxide thickness (50 nm). From figure 5.15 reporting transfer characteristics, we calculated hole mobility of 25.26 cm^2/Vs. This value is much lower than literature value for bulk Ge (1900 cm^2/Vs), but could be explained by higher concentration of Cu impurities and therefore, shorter mean free path (35 nm) and more scattering events. Finally, the calculated value for the hole concentration is $p = 7.73 \times 10^{17}$ cm^{-3}. This order of magnitude is expected due to already mentioned equation relating conductivity, mobility and carrier concentration (3.5). Unfortunately, further device investigation on this promising material system could not been completed by the time of thesis submitting. Full potential of Bi catalyzed Ge nanowires with Ti/Cu based contacts should be investigated as a part of future work.

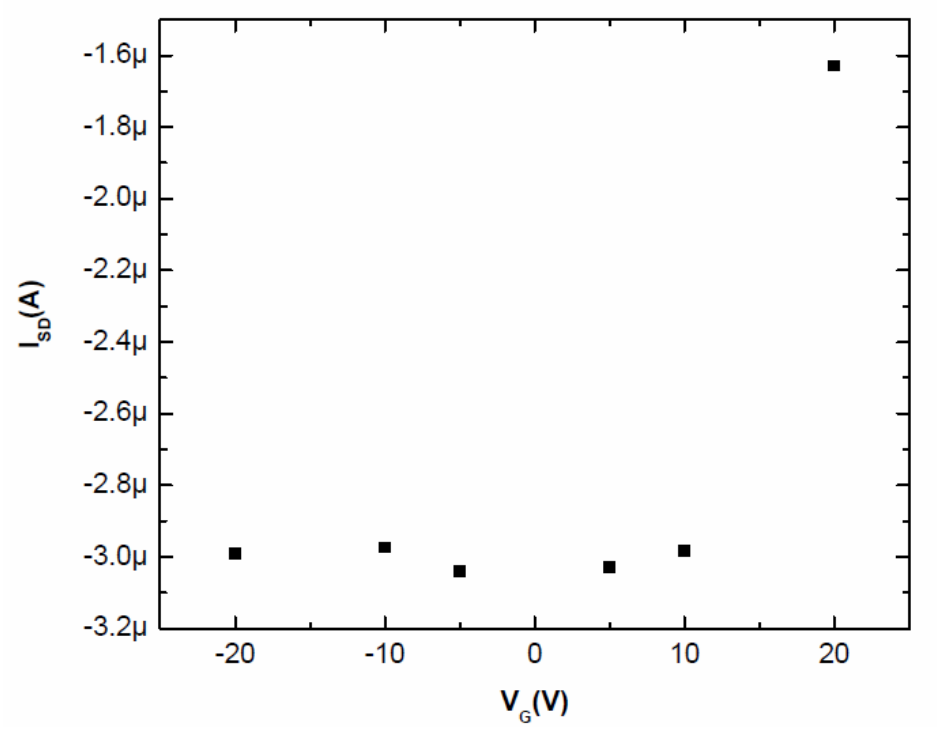


Figure 5.15. Calculated values for transfer characteristics of Bi catalyzed Ge nanowires. Contacting material is Ti/Cu heterolayer, VSD is -0.3V

5.5. Conclusion

In this chapter we have discussed the electrical properties of germanium nanowires and electronic elements based on them. Field effect transistors have been fabricated using two different approaches. While standard optical lithography showed certain limitations in performance, electron beam lithography was found to be the most reliable approach for a nanowire contacting. Different contact materials were examined for gold and bismuth catalyzed germanium nanowires to obtain Ohmic contacts. For gold catalyzed wires, Pd/Au was proved to exhibit the best properties, while for bismuth catalyzed wires, a trilayer consisting of Ti/Bi/Au as well as a bilayer consisted of Ti/Cu showed linear contact characteristics. Initial room-temperature transport results proved that both Au and Bi catalyzed nanowire devices show field effects. Further transport investigations are needed for better understanding of the transport and scattering mechanisms in those different nanowire structures, especially for Ti/Cu contacts.

6. Summaries and outlook

In this Chapter we summarize the main results obtained on both GaAs and Ge nanowires. Moreover, we introduce suggestions for a future work regarding the optimization of already achieved results as well as continuation towards experiments which could not be completed in this thesis.

6.1. Summary of the main results

6.1.a. GaAs nanowires

- The optimization of Ohmic contacts to doped GaAs nanowires was presented. After initial tests, we achieved an Ohmic contacts using Pd/Ti/Pd/Au (10nm/40nm/40nm/100nm, respectively). The first measurements were based on the optical lithography and 2-point measuring configuration. Using highly conductive substrate as the global backgate, we determined that the doping was p-type. Moreover, we calculated values of the resistivity, mobility and carrier concentration for a wide range of GaAs nanowires, starting from highly doped to nominally undoped nanowires. Unfortunately, a strong dispersion of the values obtained on the nanowires grown under the same conditions was observed. After this, we performed systematic study of the electrical properties, based on e-beam lithography and 4-point measurement configuration. Analyzing the evolution of the resistivity with respect to the position along the nanowire and introducing 2 possible dopant incorporation paths, we concluded that the dominant doping path depends on the growth rate of the nanowire. As a result of this, nanowires can be doped in a non-homogeneous fashion, which explains the dispersion of the results obtained in 2-point configuration measurements.

- GaAs nanowires were used to fabricate the MOSFETs as well. These devices were realized using single nanowire body as a channel, while a source, drain and gate electrodes were fabricated by means of the lithography. The initial devices were fabricated applying the optical lithography and the global backgate. Next step was the production of the more sophisticated devices containing both backgate and topgate electrode, based on the e-beam lithography. Performance of all devices was analyzed and compared. Highly doped (13 A) nanowires showed low resistance per length but negligible field effect.

In case of 11.5 A doped nanowires, resistance was slightly higher and field effect improved. Reaction to back gate seems to be more pronounced in case of optically fabricated samples, most likely due to longer channel in case of optical mask. The comparison between the backgate and the topgate - response measured on same nanowire showed was in favor of the backgate, most likely due to influence of the back gate to the contact resistance.

10 A doped GaAs nanowires showed a clear field-effect and the OFF state. However, resistance per length in this case was very high, making a possible application quite challenging. Similar to 11.5 A doped nanowires, backgate response is stronger in case of optically fabricated channel. However, comparing backgate and topgate response on same (e-beam fabricated) nanowire, we observe opposite situation. It seems like the effect of the thinner topgate oxide overcame the influence of the backgate to the contact resistance, resulting in a higher field effect in case of the topgate configuration.

6.1.b. Ge nanowires

- Using the same transport setup as in case of the GaAs nanowires, we performed room temperature electrical characterization of the Ge nanowires, comparing the properties of the nanowires using different catalyst materials. Contacting metals evaporated in order to achieve Ohmic contacts were differing depending on the growth catalyst. In case of Au catalyzed Ge nanowires, an optimal solution was a layer consisted of 100 nm of Pd and 10 nm of Au. For the Bi catalyzed Ge nanowires we used two metal combinations, 15nm of Ti, 100nm of Bi, and 10nm of Au as well as 15 nm of Ti and 155 nm of Cu. In order to improve the properties of the contacts, an annealing study has been performed. Both types of Ge nanowires were investigated in MOSFET configuration using a substrate as a global back gate. We calculated the resistivity, carrier concentration and mobility and compared it to the bulk material values. Both Au nad Bi catalyzed Ge nanowires exhibited a clear p-type behavior. In catalyzed Ge nanowires, due to their thick amorphous shell, showed the insulating behavior.

6.2. Outlook

- As we pointed out in Chapter 3, literature suggests that annealing step would improve properties of the Pd/Ti/Pd/Au contacts on the GaAs nanowires. We did not observe any improvements after annealing, moreover, annealing seems to harm overall electrical properties. A more detailed analysis should be performed in order to investigate this. Tests should be performed varying both the annealing temperature and time.

- Analyzing the GaAs nanowire based MOSFETs, we obtained a wide range of electrical behavior, from a low resistance and a low gate response (13 A doped) to the high gate response, but the high resistance as well (10 A doped). A further investigation should include the nanowires with a novel level of doping, 11 A for example, which could combine the moderate resistivity of the 11.5 A doped nanowires and a high field effect of the 10 A doped nanowires.

- The transport properties of the Ge nanowires grown with a Bi as the catalyst and contacted with the Ti/Cu heterolayer should be studied in more details. The annealing significantly improved an overall transport behavior, but the further investigations should be directed towards studying of the transconductance for a wider range of the gate voltages, trying to reach an OFF state. A possible step towards this goal could be shortening the annealing time. This should lead to reducing the size of Cu_3Ge region (see Chapter 5) and the higher field-effect due to the lower Cu doping. Considering the increased resistivity as a side effect, an optimal protocol resulting in both lower resistance and higher gate response is to be found.

- Ge nanowires grown with indium as catalyst showed an insulating behavior. As we pointed out in Chapter 5, this is due to the thick amorphous shell surrounding a thin crystalline core. In order to reach the conductive core, a systematic etching study should be performed, combining the different etching solutions and the etching times. Moreover, instead using a data obtained on thin films, an etching rate should be calibrated directly on the nanowires, for example by using AFM technique to determine the thickness of the etched zone.

In conclusion, even though the numerous questions and issues are to be overcome, we believe work described in this thesis gives a modest contribution towards a better understanding of the semiconductor nanowires growth, electrical properties and the possible applications.

Appendix A

Protocol for E-beam lithography based device fabrication

A.1 Introduction

In the Appendix A we are giving an overview of recipe developed for e-beam based contacting technique. Due to fact that nanowire contacting requires writing the structures on the strictly determined position, described procedures are differing from the recipes used in case of periodically writing the same structure, for example for producing photonic crystals or cantilevers.[65] We will describe sample preparation techniques (cleaving, optical mask patterning), mapping (optical axioscope imaging, distance calculation, coordinate transformation) and finally, e-beam lithography itself including the development.

A.2 Sample preparation

Sample preparation starts with cleaving. It is a procedure in which highly doped 3 inch silicon wafer is cut in smaller pieces. This is done manually, using diamond tips. However, size of the cleaved sample cannot be arbitrary selected. Upper limit is determined by sample holder of measuring setup. For example, in case of cryo-measurements, limiting factor is size of sample holder (4x4 mm or less). For room temperature measurements, this is more flexible and typical sample size used for e-beam fabricated samples in this thesis was 5.5x5.5 mm. Lower limit for sample size is determined by properties of electroresist. In case of very small samples (3x3 mm or less), due to edge effects, thickness of the resist after spinning will not be homogeneous which, in general case, may result in wrong current dose (to be explained later).

Once samples are cleaved, standard acetone-isopropanol cleaning step is performed in order to remove remains of cleaving (Si dust). This step is followed by optical lithography. We used standard positive photoresist (S 1818), spun at 3000 rounds per minute for 40 s and soft-baked in oven at 90 °C for 15 min. An image of positive optical mask used in this step is depicted in Figure A.1.

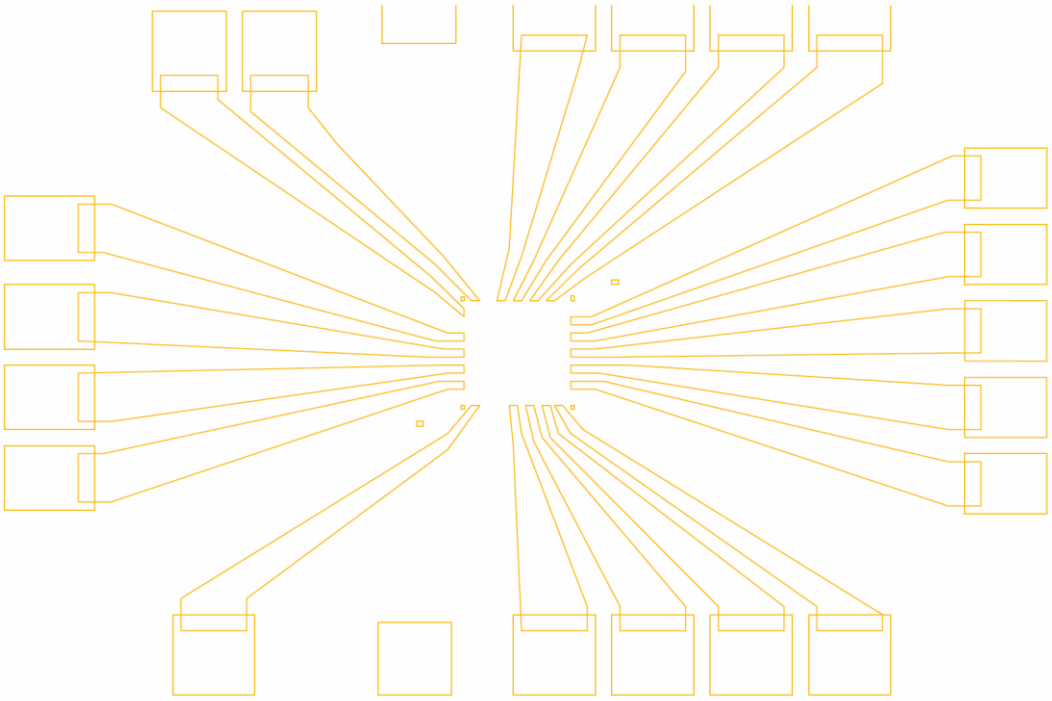


Figure A.1. Schematics of the one field in the optical mask used for e-beam mapping. Mask contains 8 fields, divided in 2 columns, each containing 4 fields.

After exposure, sample is developed and standard Ti/Au (20 nm/ 200 nm, respectively) layer evaporated, followed by lift-of. At this point we do not aim towards Ohmic contact since these structures will not directly meet nanowires. It is because of this why we chose material heterolayer providing fine adsorption to surface and facilitating the lift-off.

Optical lithography step has 3 basic reasons. First, it enables better focusing and facilitates aperture adjustments during the e-beam alignment (to be explained later). Second, in order to be able to write contacts for exact nanowire of interest, position of that nanowire is to be determined with respect to designated origin. Depending on nanowire location, different parts of optical step are used as origin. Finally, as we already explained in Chapter 2, it would be time consuming to write entire contact with e-beam. Using optical step, macroscopic contacts ($\geq 10\ \mu m$) can be written very fast while final and precise contacts from nanowire to optical step are written with e-beam lithography.

A.3 Mapping

After completing sample preparation, nanowires are transferred. As we pointed out in Chapter 2, transfer method is chosen depending on type of nanowires and desired

density of nanowires. Unfortunately, final position of the transferred nanowire is rather random. Moreover, only certain number of transferred nanowires, namely ones being located in the inner square of the field (see Figure A.1), can be contacted. Once density of the nanowires transferred in the inner square is acceptable, samples are cleaned again (acetone-isopropanol dip) and spin-coated with the electroresist. We used two layers of electroresist (Polymethyl methacrylate - PMMA, 220k and 950k), both spun at 2000 rounds per minute for 40 s. This combination of angular velocity and spinning time results in 520 nm of thickness in case of 220k PMMA and 130 nm in case of 950k PMMA, providing total thickness of 650 nm. Total resist thickness is critical for the lift-off since it may be slow and difficult for resist thickness thinner than value of 3 times evaporated metal layer thickness. However, reason for using two PMMA layers is not only to increase the total thickness. More important than this is to obtain inversion layer so that path of electron beam is conical, see Figure A.2. Omitting 220k layer and putting double/multiple 950 k layers would result in the strait electron path and reduce the adhesion of the metal to the surface, making the lift-off more challenging.

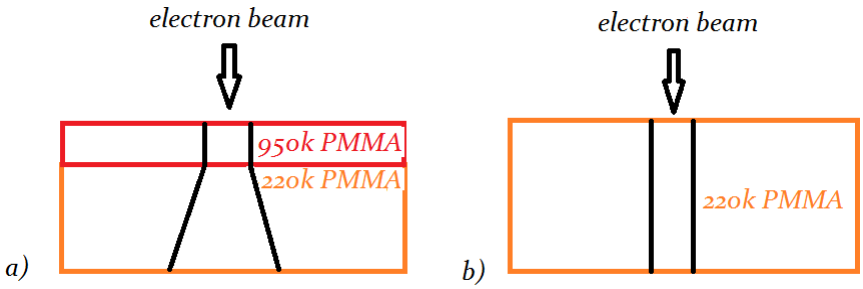


Figure A.2. Comparison of exposure in case of two a) and one b) PMMA layer

Spin-coating is followed by soft-baking (hot plate, 180 °C for 6 min) and axioscope imaging. Pictures taken with Zeiss axioscope are stored .JPEG format and processed with AutoCAD. Goal of this step is to determine relative position of the nanowire with respect to the chosen reference. Figure A.3 is showing a procedure of the nanowire mapping done in AutoCAD.

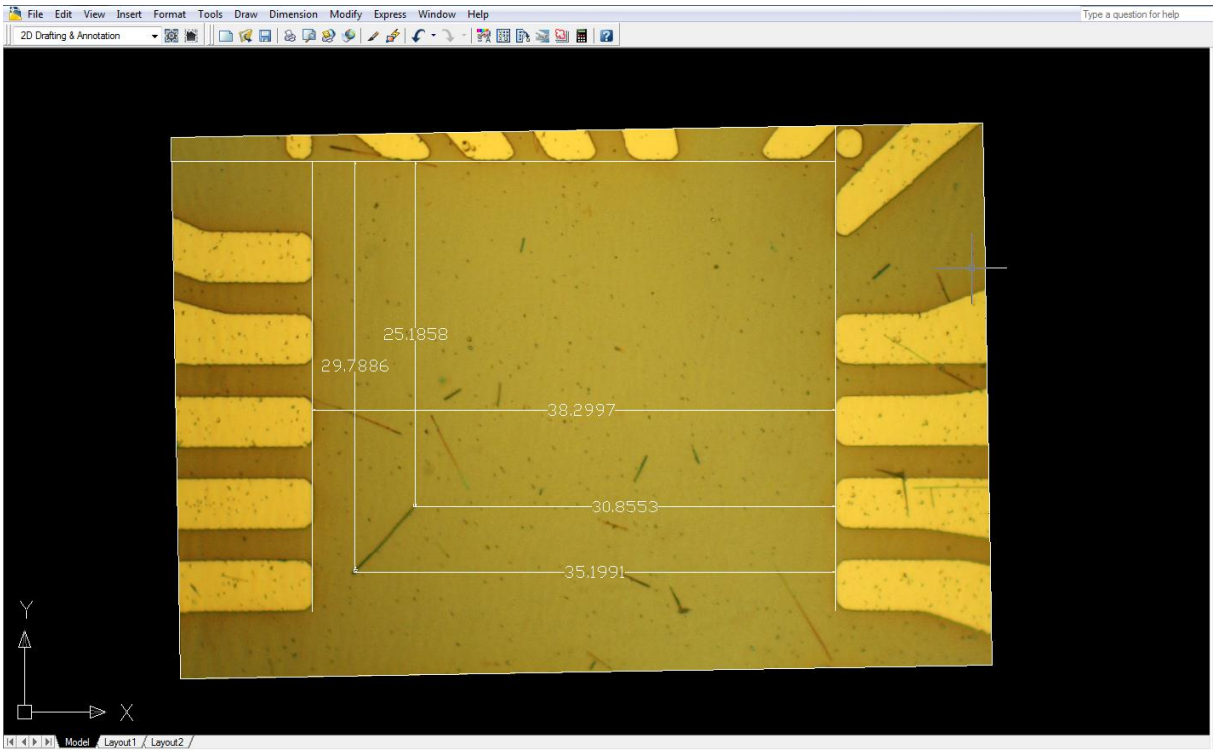
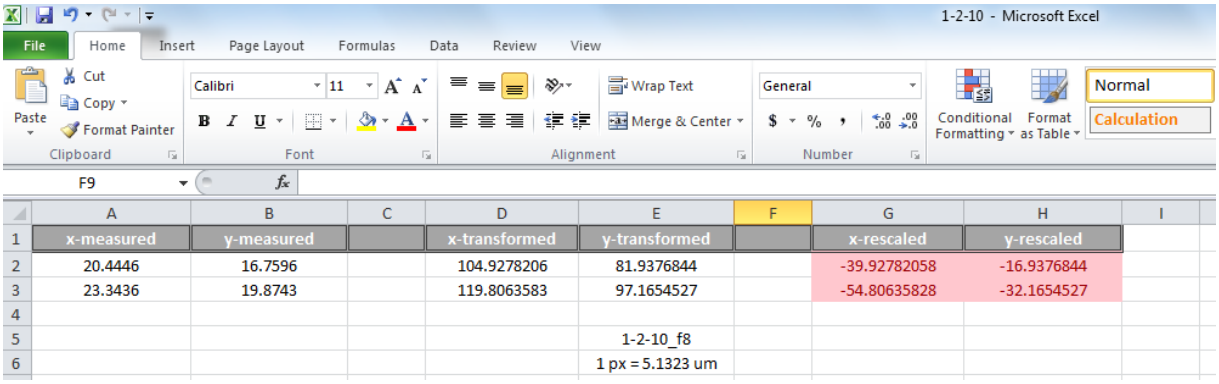


Figure A.3. AutoCAD screen shoot of the mapped GaAs nanowire. Relative position is determined with respect to upper and left border of the inner square formed by optical lithography.

As it can be seen in Figures A.2 and partially on A.3, each inner square is formed by 20 fingers (5 on each side) and it contains circle in each of 4 corners. These corner circles (two of them can be seen in Fig. A.3) are used as reference markers. Distance between the circle centers is exactly 134 μm. Consequently, if we imagine a Cartesian coordinate system with origin placed in the middle of the square, centers of four circles would have coordinates (67, 67), (67,-67), (-67,-67) and (-67,67) starting from upper right circle and moving clockwise. Unit for all coordinates is μm. Example from Figure A.3 shows that position of nanowire is measured with respect to left and upper wall of the square. However, AutoCAD is giving a position of the nanowire in arbitrary units. It is because of this why each measured distance must be scaled according to ratio between AutoCAD "units" and micrometers. This is done by measuring one known distance. For example, we know that the distance between 2 opposite sides of the square should be 130 μm. In example shown in Figure A.3, this distance corresponds to 38.2997 AutoCAD "units". Since ratio between AutoCAD "units" and actual dimensions (in μm) is constant for same .JPEG image, we can use this to convert all other values. However, even value converted with this approach does not correspond to actual nanowire coordinate. This is due nanowire position being determined with respect to left and upper side of the square, not the square center. We are doing this since we do not know exact location of this center. Still, since we know exact dimensions of the square, center position can be calculated and coordinates rescaled with respect to it. This is done by Microsoft Excell. Example of coordinates transformation and rescaling is shown in Figure A.4.



	A	B	C	D	E	F	G	H	I
1	x-measured	y-measured		x-transformed	y-transformed		x-rescaled	y-rescaled	
2	20.4446	16.7596		104.9278206	81.9376844		-39.92782058	-16.9376844	
3	23.3436	19.8743		119.8063583	97.1654527		-54.80635828	-32.1654527	
4									
5					1-2-10_f8				
6					1 px = 5.1323 um				

Figure A.4. Microsoft Excell screen shoot showing an evolution of the calculus starting from measured values (columns A and B) to rescaled values (columns G and H) corresponding to actual nanowire position with respect to center of square in which nanowire is located.

Prior to turning to the description of the lithography itself, we would like to mention a possible alternative solution for the mapping. Method we proposed (including nanowire transfer followed by spin-coating, axioscopy and AutoCAD mapping) can be simplified. In principle, it would be less time consuming to do the SEM mapping prior to spin-coating. Like this, obtained values would not require any conversion or scaling. However, as already shown in literature[66], in case of our nanowires (GaAs and Ge), highly energized electron beam used for SEM imaging damages the nanowire structure, which harming the electronic properties. It is because of this why we used longer, but in terms of nanowire electronic properties safer, optical microscope and AutoCAD based mapping.

A.4 E-beam lithography and development

Once sample is mapped, lithography procedure can be initiated. Exposure is performed in vacuum conditions (pressure bellow 10^{-6} mbar). Prior to exposure, we have to design the mask and perform alignment procedure. As we have already pointed out in Chapter 2, unlike optical lithography, e-beam does not require a physical mask. Structures meant to be written are simply drawn in proper software (eLINE), using multiple layer option. With this approach, we can overlap the image of already written optical step with the image of the final e-beam step. Moreover, by selecting certain exposure layer, it is possible to avoid rewriting of already existing structures. Example of (software) mask design is shown in Figure A.5.

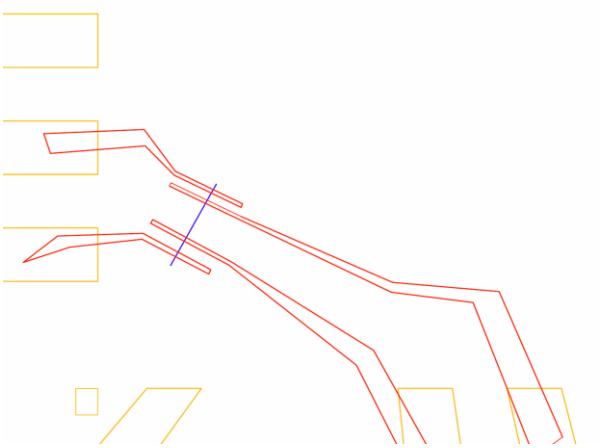


Figure A.5. The example of the e-beam mask. Orange structures are made optically, blue line is representing nanowire, while red structures are four contacts meant to be written with e-beam.

Once mask is designed, stage is moved enabling positioning of the beam on the so called Faraday cup. Faraday cup is connected to picoampere-meter enabling current measurements. Current has to be determined to calculate exposure parameters (to be explained later).

In order to make sure contacts will be written on the nanowire and e-beam and optical step will overlap, a precise alignment procedure is to be performed. This is crucial difference with respect to optical lithography where sample is moved under the physical mask until nanowire is positioned in a desired way. Since in the e-beam lithography we use same electron beam for the visualization and exposure, analogous procedure cannot be done. It is because of this why nanowire position is determined with respect to certain origin. If this origin is far enough from the nanowire, electron beam can be brought on it manually without overexposing future contact and then directed to nanowire using its coordinates measured with respect to origin. Alignment procedure starts with defining a straight line and correcting corresponding angle. At this point we also perform focusing and aperture and stigma corrections, normally on structures at least 10 times smaller than shortest dimension of the structures meant to be written.

After this, ratio between absolute coordinates ((x,y,z) - defining the position of the stage with respect to the chamber) and relative coordinates ((u,v,w) - defining the position of the origin with respect to the stage) is to be determined. This is done in one of the 8 optically produced fields (Figure A.1), normally in one containing no nanowires so overexposing it will not result in destroying the sample. Since we know distances between the fields, we can easily move from "safe" location in the aligning field to corresponding origin in field containing nanowires. As we have already pointed out, we can contact only nanowires placed in the inner square of the field, formed by 20 macroscopic contacts. In each corner of the field there is a circle, 3 of this 4 circles are used as markers. We know coordinates of these markers with

respect to imaginary zero position in the middle of the square (see section A.3). Moving beam from one marker to another and saving these positions, both in (x,y) and (u,v) coordinate systems, enables machine to calculate the origin (0,0) position. Due to this, we can move the beam to (0,0) position without looking where it is. Since nanowire coordinates with respect to origin have been determined by mapping, machine can extract the precise location of the future contacts.

In order to increase the precision of the contact position and ensure overlapping of the optical and the e-beam fabricated step, write-field alignment is performed. During this procedure, the beam is positioned on the unique object, piece of dust for example, and sequence of 9 scans is initiated. Scans are divided in 3 groups, according to corresponding scan field. In the final scan, the filed is only 1 μm. The goal of the scans is to reduce the distance between actual (physical) and calculated position of the beam with respect to unique object. If properly completed, this procedure will reduce the error to less than 100 nm. Prior to initiating exposure, additional focusing and aperture correction step is performed to ensure optimal exposure conditions. This is particularly important in case of structures smaller than 1 μm.

Now we shortly describe exposure parameters. The acceleration voltage is kept constant (20 kV). Current amplitude is constant during one exposure session, but depending on cathode conditions, it can vary from 18 pA to more than 40 pA. Charge dose is an exposure parameter determining the amount of charge to be radiated per cm^2 of the sample surface. It should be selected depending on the PMMA thickness and the structure size. After detailed dose tests, we obtain optimal value of 350 $\mu C/cm^2$. The area step size determines the distance between 2 beam positions. It should be selected with respect to size of the smallest written structure. In our case, the smallest structure was 200 nm so we selected area step size of 10 nm. Area dwell time determines how long (in ms) beams stays on certain location, while beam speed limits the speed of the beam (in mm/s) between 2 points. However, if we select the dose and the area step size, software will calculate the area dwell time and beam speed automatically. Once alignment and parameter settings are completed, exposure can be initiated.

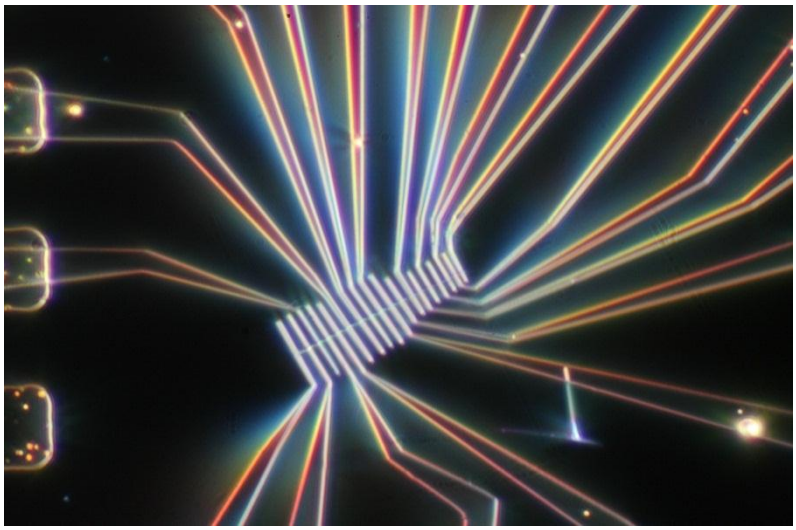


Figure A.6. Photograph of multiple contacts fabricated on single nanowire by means of electron beam lithography

The development is performed at the room temperature with a homemade solution, consisted of isopropanol and Methyl-Isobutyl-Ketone (MBIK), mixed in ratio 3:1. Recipes for etching and evaporation are already described in Chapter 2. Figure A.6 reports representative image of a single nanowire contacted with e-beam lithography.

A.5 Conclusion

In Appendix A, we described protocol for device fabrication based on e-beam lithography. We presented sample fabrication, from cleaving to nanowire transfer and spin-coating. Moreover, we explained technique of mapping and provided alternative (faster) solutions in case of nanowires being non-sensitive to highly energized electron beam. Finally, a description of the e-beam lithography itself and the challenges faced is provided.

Appendix B

A micron-sized nanoporous multifunction sensing device

B.1. Introduction

In the Appendix B, we would like to shortly mention work on side project which is not strictly related to the thesis title. The work on sensing devices is done as internal group collaboration with Dr. Lia Moreno i Codinachs. Work was focused on a micron-sized nanoporous multifunction sensing devices. The basic idea was to build a sensor which could detect changes in temperature and pH as function of capacitance. Results obtained so far are encouraging, this project is still in progress and significant part of work is yet to be done. Here we present only basic concepts, more details can be found in [67].

The current tendency in the research of sensors is the development of nano-sized devices enabling parallel sensing of several parameters. Moreover, further goal is continuous reduction in circuit size following ongoing miniaturization of the electronic appliances. Our work is a step towards this goal.

B.2. Sample fabrication

A capacitive sensor capable of detecting temperature and pH, based on Anodic Aluminium Oxide (AAO) porous structures, has been developed. Medium for temperature dependent measurements was de-ionized (DI) water. In case of the pH measurements used solution was KNO_3, 0.05 M. pH variations have been performed by adding either KOH 0.1 M or H_3PO_4 0.1 M.

The pores have been obtained by anodization in the home made teflon electrolytic cell. The cell cathode was designed in form of mash and placed at the bottom of the cell. In order to ensure a constant anodization temperature of 6–8 °C, the cell is cooled with a low temperature fluid circuit. After the pores fabrication process has been completed, a thin Ti/Au layer has been evaporated over the pores using e-beam evaporation. This layer is to be thick enough to result in stable electrical contact, but, in the same time, thin enough not close the pores, allowing the contact between the alumina and the solution. Figure B.1 shows schematic representation of the sample.

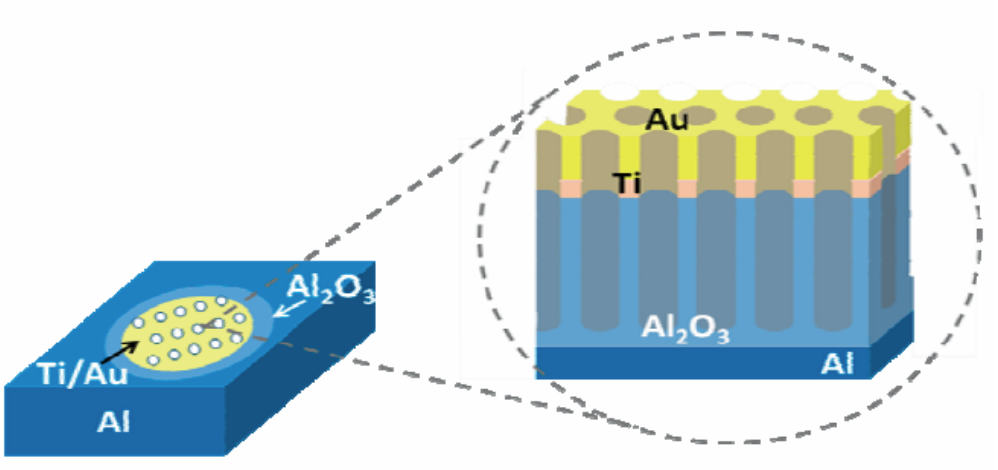


Figure B.1. Schematics of the fabricated samples, left drawing is showing top view while right drawing shows side cross section. Figure is taken from 67.

Once the sample fabrication is completed, measurement pre-steps have to be performed. Samples have been fixed in a glass support and the Au layer on one side and the Al foil on the other have been contacted using the Au wire and silver paste to fix the electrical contact to two Cu lines. Using this approach, connection of sensing unit to the readout electronics was facilitated, contributing to more reproducible measurements.

B.3. Measurements and analysis

Capacitance measurements as a function of pH and temperature have been performed using a RCL bridge (Philips PM 6303). Instrument has embedded electrolyte function mode, in which an AC voltage (2 V effective, 1 kHz) is applied and the capacity is measured. Other pH measurements have been performed using a Potentiostat (PerkinElmerTM instruments, PARSTAT 2263) fixing a frequency of 1 kHz (and the AC amplitude at 10 mV). In this setup, capacity is measured from the voltage sweeps, similar to current measurements in SMUs. We used sweep interval between –0.1 V and 0.1 V, measuring the capacity at any applied potential within the range. A basic advantage of potentiostat based measurements is that the potential can be set to a desired value in order to study and minimize the possible charging effects of the oxides and therefore to compare hysteresis and stability effects. Temperature analysis has been performed in a home-made thermostatic bath, measuring the capacitance as a function of temperature. Medium for temperature modifications (from 20 °C to 90 °C) was DI water. The capacity values have been taken every 1 °C.

On the other hand side, pH measurements have been performed doing pH cycles between pH 3 and pH 9 adding base (KOH, 0.1 M) or acid H_3PO_4 (0.1 M) to background solution. Using this approach, studies about the C–pH characteristic

have been done. Moreover, we analyzed the hysteresis of the device. The capacity values have been taken every 1 pH unit.

Figure B.2 shows a SEM image of the pores after the Ti/Au bilayer is has been evaporated. We can see that thickness of layer is carefully chosen, in order to keep the pores open and allow contact between pores and solution.

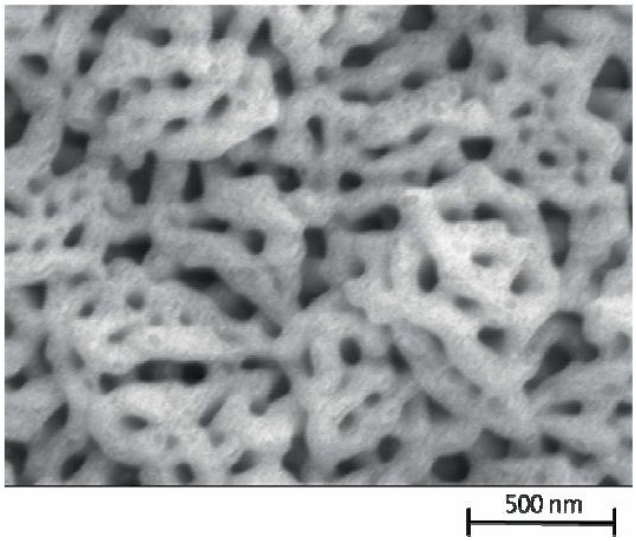


Figure B.2. SEM micrograph of the sample for measuring the temperature. Alumina pores are partially filled with Ti/Au. Figure is taken from [67].

Analyzing the influence of temperature, one should think about the temperature dependence of the parameters defining the capacitor, such as the geometry – volume expansion – and the dielectric constant. An increase in the temperature T causes an expansion in the crystal lattice of the solid. As it can been seen in [67], analysis we performed showed that volume thermal expansion should lead to a slight increase of the sensor capacitance. However, the dielectric constant of many material systems increases also with temperature. This is effect is stronger and, hence, its influence dominant with respect to the volume expansion. If we take the example of alumina, the expansion coefficient has a value of 7.2×10^{-6} °C^{-1}. This results in a 0.072% volume expansion in case of temperature range between 1 °C and 100 °C. For the same temperature interval and for frequency fixed to 10 GHz, capacitance will increase for factor of 2%.[68]

On the other hand, changes in the pH of the solution are resulting in changes on the charge stored. As described in the bibliography[67,69], the solution side of the double layer (Figure B.3.) is considered to contain several layers. There is an inner layer (also called compact, Helmholtz or Stern layer, IHP) that mostly contains solvent molecules. These molecules are believed to be specifically adsorbed. Solvated ions can reach immediate vicinity of the electrode only keeping a certain distance and forming the so called Outer Helmholtz Plane (OHP). These ions are said to be nonspecifically adsorbed. Because of thermal agitation in the solution, the nonspecifically adsorbed ions are distributed in a three dimensional region called diffuse layer, which extends from the OHP into the bulk of the solution.[70]

This model describes that the double layer capacitance C_d is made up of two components, similar to geometry of the two capacitors in series. Thus, two terms can be identified C_H (capacitance of the charges held at the OHP) and C_D (capacitance of the truly diffuse charge). At larger electrolyte concentrations, C_D becomes very large As we know from basic electrostatics, serial combination of huge and small capacitor is effectively equal to capacity of small capacitor itself. It is because of this why at a larger electrolyte concentrations C_D no longer contributes to C_d and one measures only the constant capacitance of C_H.[69]

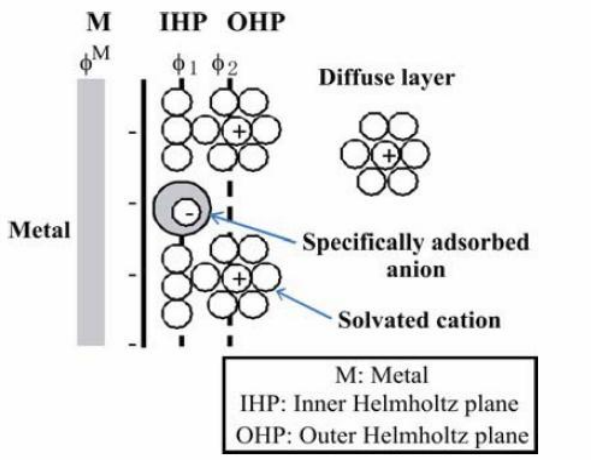


Figure B.3. Scheme of the different layers at the solution side of the double layer model. Anions are assumed to be specifically adsorbed. Figure is taken from [67].

B.3.1. Temperature measurements

Temperature measurements have been performed with $Si/SiO_2/Al/Al_2O_3/Au$ structures. The results of three different measurements are reported in Figure B.4. As shown on figure, the capacitance increases linearly with the temperature. Moreover, there is a matching of the three curves, indicating the high reproducibility of the tested sensor. However, we should point out that the capacity in the first 10 °C for the first measurement (green curve) presents a deviation with respect to the other two curves. The origin of this phenomenon is probably reduced accuracy due to the acquisition data time. Overall results show an increase in capacitance corresponding to the increase of the dielectric function predicted by the theory.[67] However, the increase we observed is about 35%, while the theory predicted value of 2%. This high difference of the theoretical prediction with respect to experimentally obtained capacitance can be attributed to the fact that the dielectric constant of alumina depends on several parameters sometimes not obvious to predict. For example, stress induced by the increase of the temperature could result in higher capacitance variations.

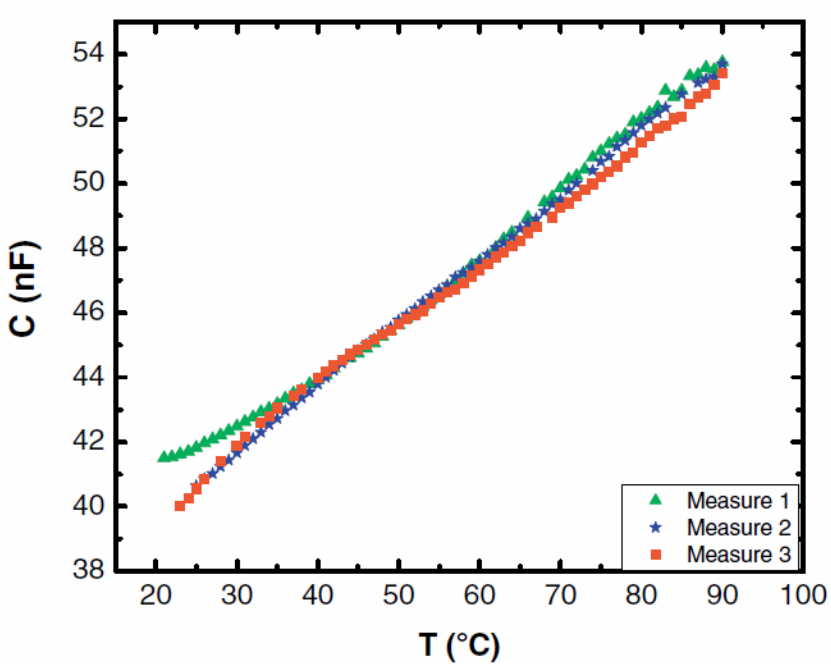


Figure B.4. C-T measurements performed on Si/SiO2/ Al/Al_2O_3/Au structures. Medium for measurements was DI-H_2O environment. Figure is taken from [67].

B.3.2. pH measurements

pH measurements have been performed on two types of samples. In first case, we used samples with Al_2O_3 pores while in second case Al_2O_3 pores have been coated with 20 nm SiO_2. This is done to investigate the stability in different pH environments of both materials as well as the C-pH response. Analogous to C-T measurements, experiments we carried out with two different devices in order to investigate the response of the sensor for different applied potentials.

B.3.2.a) pH measurements with Al_2O_3 pore samples

The C–pH curves obtained using the RCL bridge and the potentiostat are reported in Figure B.5. Measured value of the capacitance increases with the pH value in both cases. Increase in pH value (increase in the concentration of OH^- ions in solution) leads to increasing of the charge density on the double layer. Consequently, increase in the capacitance value also occurs. Contrary, for pH values below 7 the decrease of pH leads to a lower surface charge due to the recombination with protons in the solution that increase in concentration as the pH decreases.

Moreover, a hysteresis in the behavior of the sensor is detected as well. This effect is not significant (less than 2 nF). In the measurements performed with the potentiostat this hysteresis is also observable. We attribute this to the porosity of the alumina, which may be more prone to store charges.

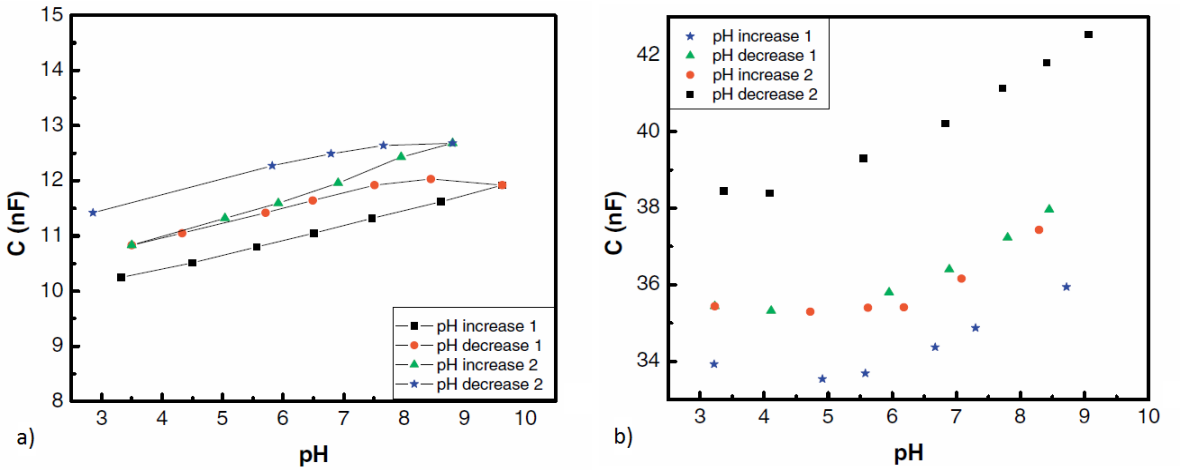


Figure B.5. C-pH curves measured on sample with Al_2O_3 pores. a) shows response detected with RLC bridge while b) shows response of potentiostat at 0V. Reproducibility of device in both cases is high. Figure is taken from [67].

Comparing measurements obtained with different devices (RCL bridge and potentiostat) one can observe a difference in the slope values. This difference seems to be due to technical characteristics of devices as well as to the hysteresis effect. Also, the detection limit of the sensor slightly varies. In case of the measurements done with the potentiostat (voltage: 0 V), the limit of detection is around pH 4–5. However, for the RLC bridge based measurements, the sensor is able to respond at pH of around 3. As a final value of overall sensor performance, we calculated the relative error of the measurements (calculus is done using two replicates performed for each measurement). Obtained values are 0.13% and 0.19% for the RCL bridge and the potentiostat respectively, indicating quite high precision.

B.3.2.b) pH measurements with Al_2O_3 pore samples coated with 20 nm of SiO_2

In order to reduce the hysteresis effect, we coated the alumina pores with a high quality SiO_2. The results of the pH measurements preformed on samples in which the alumina pores have been coated with 20 nm of SiO_2 are shown in Figure B.6.

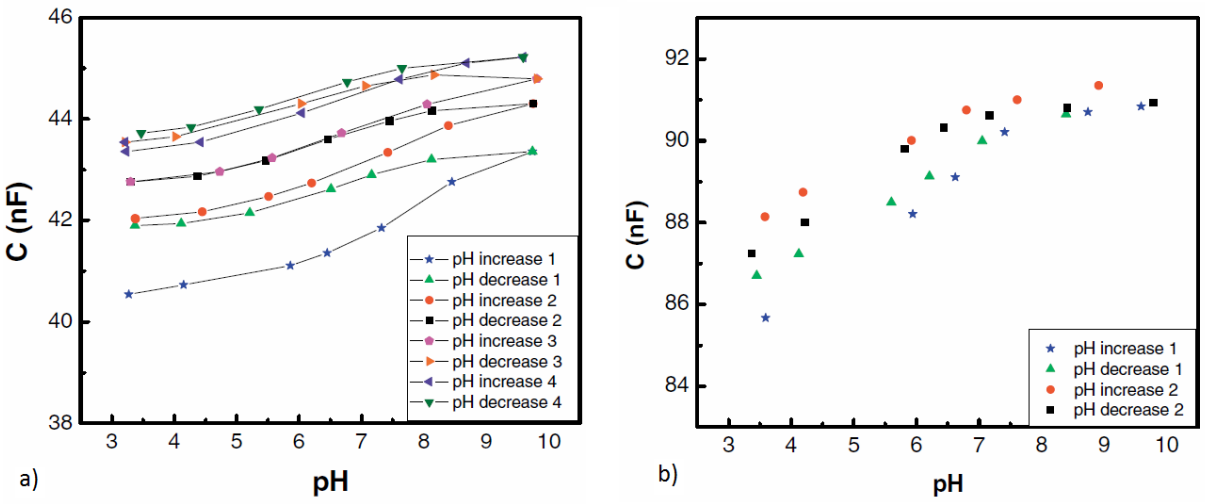


Figure B.6. C-pH measurements performed on samples with Al_2O_3 pores coated with 20 nm of SiO_2. a) shows data measured with RLC bridge while b) shows data obtained with potentiostat at 0V. Figure is taken from [67].

As it has been explained in case of Al_2O_3 pores samples without SiO_2, the capacitance increases with the pH. In the case of the measurements based on RLC bridge setup, the hysteresis decreases with time, probably due to the storage of the charges on the oxide after the application of the voltage (2 V), see Figure B.6.a). However, we should point out that after three cycles the hysteresis disappears. This phenomenon could be expl ained by lower porosity of the SiO_2 and the high chemical purity of this material. Same effect can be observed in case of potentiostat based experimental setup, see Figure B.6.b). In this case, the hysteresis has been drastically reduced, probably due to the measurement conditions of the potentiostat (in this case the potential applied is 0 V). Moreover, additional contribution to this significantly reduced hysteresis could be coming from fact that these measurements were done after the ones performed with the RCL bridge. It is because of this why the oxide was already polarized and stabilized, potentially resulting in lower hysteresis.

B.4. Conclusion

In Appendix B we showed a work towards a new device based on Anodic Aluminum Oxide (AAO) pores structures ($Al/Al_2O_3/Au$ and $Si/SiO_2/Al/Al_2O_3/Au$). Measurements of the temperature in DI water have been performed with the device and a linear and reproducible response has been obtained. Measurements with the device in solutions of different pH have been done using two different measuring devices and in both cases, a linear response of the capacity as a function of the pH can be observed as well as a high reproducibility of the sensor. A future work should be orientated towards development of equivalent circuit and optimization in device geometry.

List of Figures

List of Tables

List of publications

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*Equal contribution

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Ivani Trogrlić, jer di ćeš naći boljeg Bosanca za tako male pare?

Sunny Lane, jer amicus certus in re incerta cernitur

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Mojoj obitelji (mami, tati i seki) zbog svega što ne mogu opisati nikakvim riječima.

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