DEVICE LEVEL BASED CELL MODELING FOR FAST POWER ESTIMATION

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ABSTRACT

In this work, a method for fast power estimation in complex digital circuits is presented. Properties like delay and power consumption of a circuits basic cells are extracted precisely by circuit level simulations. The cell model then includes delay and power consumption values for all possible transitions at the cell inputs. The total power consumption is finally determined by logic simulation at higher architectural levels. The cell model also includes the glitching behavior at the outputs resulting from different path delays inside a cell. It is shown experimentally that this delay model, including glitches generated by the basic cells, leads to good power estimation results of complex circuits within an accuracy of 8% in the worst case and needs 4 and 2 orders of magnitude less simulation time than SPICE and PowerMill respectively.

1. INTRODUCTION

Low power digital design is still one of the most important challenges for VLSI engeneers as mobility and complexity of digital systems is rapidly increasing. Besides design methods, the accurate estimation of the power consumption of a system at all levels of the design process is necessary. Probabilistic approaches for estimating the switching activity are considered in [2] and [4], where the accuracy could be improved by considering temporal and spatial correlations of the signals. Also fast simulation based methods have been developed [7].

However, the accurate estimation of the switching activities inside a circuit is only one part of a quantitative power estimation method. Also the power consumption per switch at the corresponding nodes has to be determined properly. In [6] partitions of the circuit are simulated at circuit level, then the total power is determined by summation of the switching activities weighted with the predetermined power consumption of the partitions. Pseudo random stimulus vectors are used for the circuit level simulations which allows only to predict an average power consumption per switch. Another simulation based approach is presented in [3] where the power consumption of each cell is determined by circuit simulation for each input/output transition. The total power is then estimated by summation of the power consumptions of the corresponding input/output transitions after logic simulation with a simple unit delay model.

In this paper a method is presented that is based on accurate *d*evice level based *c*ell *m*odeling (*DCM*). All parameters for this model are extracted from circuit simulations. Also glitches that occur at a cell output due to different signal delays inside the cell are considered in the cell model. These glitches can have significant influence on the power consumption of the whole circuit and are neglected in previous approaches. All basic cell models are formulated in VHDL-descriptions. A special cell library is built up were every cell description includes the specific timing and power parameters.

The paper is structured as follows: In Section 2 the delay model and the extraction of the delay values of basic cells by circuit simulation are described. The glitching behavior and its consideration in the model is discussed in Section 3. Section 4 describes the extraction and modeling of the power consumption of the basic cells. In Section 5 the power estimation method at higher architectural levels by logic simulation based on the new cell model is presented. Section 6 shows experimental results for a variety of test circuits. Some concluding remarks are made in Section 7.

2. BASIC CELL DELAY MODELING

An important criterion for the accuracy of the simulation based switching activity determination at logic level is the delay model applied to describe the timing behavior of the gates. With a zero delay model, different signal delays and resulting glitches are not considered. Thus, the switching activity is underestimated. In certain circuits like combinatorial array multipliers, where a large part of the total switching activity is due to glitches, this will lead to completely erroneous results. On the other hand in a transport delay model every glitch is considered as a full transition

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that propagates through the gates, no matter how short the glitch is. A simple inertial delay model considers only those glitches, that are longer than the inertial delay of a gate and cancels every impulse that is shorter, which leads in fact also to an underestimation of the switching activity.

For the purpose of a more accurate switching activity estimation, a special delay model is developed. This model reflects the real timing behavior of each cell and takes into account glitches at a length where they really lead to considerable power consumption when occurring at the gates inputs. All the necessary parameters for this delay model are extracted by circuit simulations with SPICE. A cell library is built up that includes all basic cells with their specific parameters. The cells considered here are 2- and 3-input NAND-, NOR-, XOR-, AND- and OR-gates, multiplexors and 1 bit fulladders, realized in different logic. Before simulation, all cells are implemented as full custom mask layouts. The layouts are then extracted with all parasitics. The load that a cell has to drive when it is included in a circuit has strong influence on the delay and the power consumption of the cell. Therefore, every cell is simulated with a load that is similar to the load that the cell output has to drive inside the circuit. In general, a load parameter l_d can be extracted that is multiplied to the intrinsic cell delays and takes into account different load cases for different circuits.

As the delay in general depends on the input data, the cell is simulated for every possible input transition. The specific delays of the cell for each of these input transitions are stored in the model description. For the example of a symmetric CMOS 1-bit fulladder in $0.7\mu m$ technology loaded with another fulladder of the same type, these delays are between $1.2ns$ and $2.4ns$ at the sum output. For other logic types, e.g. transmission-gate- or pass-transistor-logic, the times differ even more. Let n be the number of inputs, then each cell has

$$x = 2^{2n} - 2^n \qquad (1)$$

possible input transitions, e.g. for a 1-bit fulladder with its 3 inputs the number of possible input transitions is 56. This shows, that this model becomes very complex for cells with a large number of inputs. However, in this case it is always possible to reduce the complexity drastically, as many of the delays are quite similar. All transitions with similar delay times can than be collected together in a group of transitions with one representative delay time. This is still a reasonable heuristic. This heuristic is not applied throughout this paper, all cells are modeled considering every possible input transition separately. If multiple load cases shall be taken into account, the delay time value for transition i is considered as the intrinsic delay $t_{d_{int},i}$ that has to be multiplied with the load parameter l_d which depends on the load situation of the cell inside the circuit under test. The corresponding delay for a transition i is then given by

$$t_{d,i} = l_d \cdot t_{d_{int},i} \quad . \qquad (2)$$

Input transitions that are shorter than a certain threshold time, which is also determined by a SPICE simulation, are canceled, as they cannot propagate through the cell.

3. MODELING THE GLITCHING BEHAVIOR

Besides the specific delays of all input transitions, the glitching behavior of the cell is also included in the model. Due to the fact, that not all transistors on a signal path switch at the same time for certain input transitions, spurious transitions can occur at the outputs of a cell. These glitches can be assumed to be "generated" by the cell itself, even when all input signals occur at the same time. The length of these glitches depends on the output load. Therefore they are included in the model with an intrinsic length, multiplied again with a load parameter. Glitches with lower voltage swing than the threshold voltage of the process are not included, as they do not cause power dissipation. Figure 1 shows the equivalence of the modeled behavior of a 1-bit fulladder sum output (S_{model}) and the SPICE-simulation (S_{SPICE}). Note the modeling of the glitches.

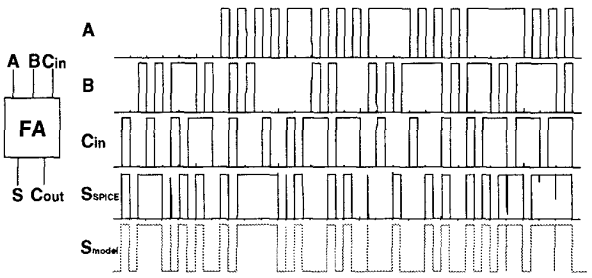

Figure 1: Comparison of a SPICE-simulation of a 1-bit fulladder with a logic simulation based on the new delay model.

To show the good quality of the delay model described in Section 2 combined with the glitch model, a 5x5-bit array multiplier consisting of 20 1-bit fulladders (including the final carry-ripple adder) is simulated with SPICE and the switching power of each fulladder is plotted versus the number of toggles at the corresponding fulladder determined by logic simulation based on the proposed new model. The same is done for a classical inertial- and a transport-delay model. Figure 2 shows the desirable linear dependence between the simulated switching power and the number of toggles for the proposed model, the underestimation of the toggle number caused by the inertial delay model and the overestimation caused by the transport delay model.

4. BASIC CELL POWER MODELING

For a quantitative power estimation based on the logic simulation of a circuit, the necessity of an accurate power model

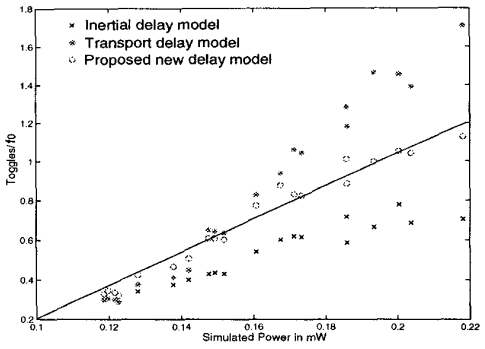

Figure 2: Simulated switching power vs. number of toggles for each fulladder in a 5x5-bit array multiplier with three different delay models.

for each basic cell is evident. The power consumption as well as the delay depends highly on the input data. A model that assumes the same power consumption of a cell for every output transition independent of the causing input transition as in [6] in general will not lead to an accurate estimation of the total power consumption of a circuit. The switching activity is, as well as for the method presented in this paper, determined by logic simulation. For each transition at the output of a cell, an average value for the energy consumption of the cell is added to the total energy consumption. This average value is commonly determined by circuit simulation with random input patterns. The total power consumption is then calculated as the sum of all transitions weighted with the specific energy value, divided by the total number of periods. This model is applicable only in the very special case when all the signals in the circuit have the same distribution as the random patterns used for the circuit simulation. Even in this case a large number of test patterns is necessary for the final logic simulation to achieve really randomly distributed signals inside the circuit.

The parameters of the power model presented here are also extracted from circuit simulations of the basic cells. Once the parameters are determined, they are included in the model descriptions of the cells besides the parameters of the delay and glitch model. Again, like for the delay model, all possible transitions at the cell inputs are considered separately in the circuit simulation. Thus, for every transition a specific power consumption value can be determined. For the example of a symmetric standard CMOS 1-bit fulladder in $0.7\mu m$ technology, loaded with another fulladder cell at both outputs, these power consumption values differ between $1.32 \cdot 10^{-6} W$ and $3.91 \cdot 10^{-5} W$. For taking into account various loads, all power values are considered as intrinsic values that have to be multiplied with a load parameter l_P. The power consumption P_i of a cell for transition i is calculated as follows:

$$P_i = l_P \cdot P_{int,i} \quad , \tag{3}$$

where $P_{int,i}$ is the intrinsic power consumption value for transition i. Obviously the load parameter in (2) can be set equal to that in (3), $l_d = l_P$.

5. POWER ESTIMATION AT HIGHER ARCHITECTURAL LEVELS

Once the cell model library is constructed with the delay, glitch and power model included in every cell description, the power consumption of complex circuits can be estimated in a logic simulation. The block diagram in Figure 3 shows the two phases of the simulation. In *Phase* 1 the cell

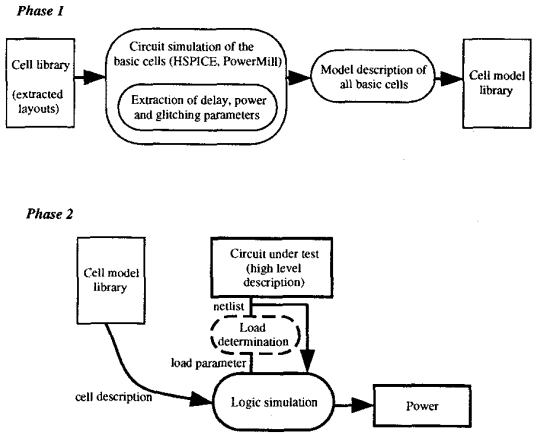

Figure 3: Scheme of the proposed power estimation method. *Phase* 1: Construction of the cell model library, *Phase* 2: Power estimation at higher architectural level.

model library is constructed with the methods described in Sections 2, 3 and 4. *Phase* 1 is executed only one time. The power estimation for all circuits under test is carried out in *Phase* 2. The circuits under test are described at a higher architectural level, e.g. at logic- or register-transfer-level. A netlist description at the specific level combined with the cell descriptions from the cell model library is then used by the logic simulator. The determination of the load parameters is implicitly included and needs no further processing step. However, for comprehensibility it is included in the diagram. Finally, the total power consumption of the circuit, P_{DCM}, using the presented device level based cell modeling method (DCM) is calculated by:

$$P_{DCM} = \frac{1}{N} \sum_{j=1}^{M} \sum_{k=1}^{S_j} P_{j,k} \quad . \tag{4}$$

N is the number of periods, M the number of cells in the circuit under test, S_j the number of transitions at the input of cell j during logic simulation, and $P_{j,k}$ is the power consumption of cell j for transition k.

6. EXAMPLES AND EXPERIMENTAL RESULTS

For testing the new power estimation method in terms of accuracy and CPU-time, the following circuit examples are considered: 5x5-, 8x8- and 16x16-bit array multipliers, 8x8-bit Wallace tree multipliers (Wal) and 16- and 32-bit carry lookahead adders (CLA). The multipliers are implemented with different fulladder types: a symmetric CMOS adder (CMOS), shown in [5], a transmission-gate-logic adder (TG), shown in [1], and a 16 transistor adder cell (T16) presented in [8] (there denoted as "NEW"). After extraction of the parameters by SPICE simulations, the basic cell models are described in VHDL ($Phase1$). Also all the circuit examples are described in VHDL. For the comparison with SPICE, only the 5x5-bit array multiplier is considered due to the very long simulation times for larger circuits. For this purpose the 5x5-bit array is implemented as a mask layout, one for each of the three adder types CMOS, TG and T16. The extracted layouts are then simulated with SPICE. All other circuits are simulated with PowerMill. In these cases, the power parameters of the basic cells are also determined with PowerMill. For logic simulation in $Phase2$ a conventional VHDL-simulator is used. Every simulation is executed using 1000 random test vectors. The results are shown in Table 1 and Table 2. In Table 1 P_{SP} denotes the

Circuit	P_{SP} (mW)	P_{DCM}^{SP} (mW)	Δ (%)	t_{SP} (sec)	t_{DCM} (sec)
5x5 (CMOS)	0.492	0.496	0.8	38398	8
5x5 (TG)	0.764	0.772	1.0	25354	8
5x5 (T16)	0.717	0.714	0.4	22290	7

Table 1: Power consumption of a 5x5-bit multiplier with different adder types. The new DCM method compared with SPICE.

power simulated with SPICE, P_{DCM}^{SP} the power estimated with the new DCM method where SPICE is also used for the determination of the power parameters of the basic cell models. In Table 2 P_{PM} denotes the power simulated with PowerMill, P_{DCM}^{PM} the power estimated with the DCM method where the power parameters of the basic cell models are also determined with PowerMill. The difference between the power estimation with SPICE or PowerMill and the DCM method in % is shown in the Δ-column. The results show the good accuracy of the proposed method compared to the basic circuit simulator at less simulation time.

7. CONCLUSION

In this paper a device level based cell modeling method (DCM) for fast power estimation is presented. The key to this method is the accurate determination of delay and power parameters and also the glitching behavior of the basic cells. These parameters are then included in the cell model. The power consumption of complex circuits consisting of these

Circuit	P_{PM} (mW)	P_{DCM}^{PM} (mW)	Δ (%)	t_{PM} (sec)	t_{DCM} (sec)
8x8(CMOS)	1.13	1.16	2.1	424	30
8x8(TG)	1.80	1.85	2.9	640	31
8x8(T16)	1.55	1.64	5.7	3252	28
16x16(CMOS)	7.56	7.76	2.6	3043	186
16x16(TG)	12.01	12.66	5.4	5941	215
16x16(T16)	8.28	8.94	7.9	84326	209
Wal(CMOS)	0.91	0.92	1.5	330	21
Wal(TG)	1.43	1.49	4.8	431	22
Wal(T16)	1.65	1.73	4.8	3150	23
CLA_16	1.25	1.29	3.2	311	35
CLA_32	4.95	5.18	4.6	551	126

Table 2: Power consumption of some circuit examples determined with the new DCM method and PowerMill (PM).

basic cells can then be determined by simple logic simulation. The results show, that this method has an accuracy within 8% of the basic circuit simulator for the considered circuits and is up to 2 orders of magnitude faster than PowerMill and even 4 orders of magnitude faster than SPICE. The new method can be used in future research for comparing the power consumption of large circuits.

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