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Silicon to Nickel Silicide Longitudinal Nanowire Heterostructures: Synthesis, Electrical Characterization and Novel Devices

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Abstract

The scope of this thesis is the synthesis and electrical characterization of Si to Ni silicide nanowire heterostructures with the focus on investigating their electronic transport properties and conceiving a novel type of transistor with added functionality. Nominally intrinsic Si nanowires (SiNW) were grown by chemical vapor deposition employing the vapor-liquid-solid mechanism. Growth was optimized to provide a controllable and uniform SiNW diameter distribution with mean values down to 7 nm. As a first step towards vertical monolithic integration, SiNWs were grown on amorphous metallic layers and guided vertically through high aspect ratio trenches. An innovative approach to transform SiNW segments into metallic Ni silicide nanowires was developped. Accordingly, Ni silicide intrudes longitudinally into the SiNWs, resulting in interfaces with a sharpness of at most a couple of nanometers. By synthesizing Ni silicide/ Si / Ni silicide longitudinal nanowire heterostructures on top of back gate stacks, Schottky barrier field effect transistors (SBFET) were formed. As the silicide formation advances from both SiNW ends, the metallurgic gate length (L_g) was reduced, e.g. from 1 µm down to 7 nm. Hundreds of SBFETs based on single nanowire heterostructures with different active region geometries were fabricated and extensively electrically characterized. Devices built from thin SiNWs (diameters ~20 nm) exhibited unipolar p-conductance with remarkable electrical performance: record on-conductances, on/off current ratios and on-current densities for intrinsic SiNW SBFETs. The efficient gate control is attributed to the electric field enhancement at the needle-shaped silicide electrode tips where the Schottky contacts are located. Measurements indicate that the gate potential can effectively tune the Schottky barrier width to control carrier injection. The effect of scaling the active region size in SiNW based devices was systematically studied for the first time. A gate length dependent study showed current limitation by the Schottky contacts for devices with $L_g < 1$ µm and exponentially decreasing currents for $L_g > 1$ µm. The scaling behavior of the SiNW diameter revealed the impact of the Schottky contacts on the electronic transport. As the diameter increases a gradual transition

from unipolar p-type to ambipolar conduction was observed, approaching the expected operation of bulk devices. It was proven that the device polarity is exclusively controlled by the Schottky junctions. This property was used to develop a novel device concept, where each Schottky contact is independently gated. Carrier injection of one type of carrier was stimulated while the other carrier type was blocked at the other Schottky junction. Consequently, the same SiNW SBFETs were tuned to enable n-type and p-type operation, completely avoiding doping. The sharp metallurgical interfaces, thin Si body, and dopant-free control of polarity are promising attributes which may principally enable complementary logic at nanoscale gate lengths.

Kurzfassung

Im Kern befasst sich diese Dissertation mit der Synthese und der elektrischen Charakterisierung von longitudinalen Silizium zu Nickel-Silizid Heterostrukturen in Nanodrähten mit dem primären Ziel, die elektronischen Transportmechanismen darin zu untersuchen und neuartige Bauelemente daraus zu entwickeln. Nominell intrinsische Si-Nanodrähte wurden durch chemische Gasphasenabscheidung mittels einer Gas-Flüssigkeit-Festkörper-Reaktion gewachsen. Die Wachstumsparameter wurden so optimiert, dass kontrollierbare und gleichmäßige Durchmesserverteilungen der Nanodrähte erzielt wurden. Des weiteren wurde zum ersten Mal das senkrechte Nanodraht-Wachstum auf amorphen metallischen Schichten demonstriert, indem die Si-Nanodrähte aus vorprozessierten Gräben herausgeführt wurden. Einen Hauptteil dieser Arbeit stellt die Entwicklung eines neuartigen Prozesses dar, der die Umwandlung von longitudinalen halbleitenden Si-Nanodrahtsegmenten in metallisches einkristallines Ni-Silizid ermöglicht. Die dabei entstehenden Grenzflächen wiesen eine Schärfe im Nanometerbereich auf. Somit konnten Ni-Silizid / Si / Ni-Silizid Nanodraht-Heterostrukturen erzeugt werden, die zusammen mit einer darunter liegenden Gatter-Anordnung einen Schottky-Barrieren Feld Effekt Transistor (SBFET) bildeten. Durch das beidseitige Voranschreiten der Silizid-Bildung im Nanodraht konnte die metallurgische Gatter-Länge (L_g) verkürzt werden, beispielsweise von 1 µm auf 7 nm. Hunderte SBFETs mit unterschiedlichen Abmessungen des aktiven Gebietes wurden hergestellt und elektrisch charakterisiert. Transistoren aus dünnen Nanodrähten zeigten unipolares p-leitendes Verhalten und Rekordwerte für Ströme und Leitfähigkeiten im eingeschalteten Zustand sowie für die Stromverhältnisse zwischen ein- und ausgeschaltetem Zustand für SBFETs basierend auf intrinsischen Si Nanodrähten. Die effiziente Gatter-Kopplung wird der elektrischen Feldüberhöhung an den Schottky-Kontakten durch die nadelartige Form der Silizid-Segmente zugeschrieben. Messungen deuteten auf die Kontrolle der Schottky-Barrierenbreiten durch das Gatter-Potential und auf die daraus resultierende Kontrolle der Ladungsträger-Injektion durch die Kontakte hin. Zum ersten Mal wurde eine systematische Untersuchung

des Skalierungsverhaltens von Si-Nanodraht SBFETs durchgeführt. Die L_g-Abhängigkeit zeigte für $L_g < 1\,\mu m$ eine Strombegrenzung durch die Schottky-Kontakte sowie für $L_g > 1\,\mu m$ ein exponentielles Abklingen mit steigendem L_g. Die Untersuchung der Abhängigkeit vom Nanodraht-Durchmesser ergab einen stetigen Übergang von unipolarer p- zu ambipolarer Leitung mit steigendem Durchmesser, wobei die erwartete Ambipolarität eines klassischen Volumen-SBFETs angenähert wurde. Daraus lässt sich vermuten, dass die Polarität der SBFETs allein durch die Schottky-Barrieren bestimmt wird. Um diese Annahme zu beweisen, wurden neuartige SBFETs mit voneinander unabhängigen Gatter-Kopplungen der einzelnen Schottky-Barrieren entwickelt. In diesem Konzept werden die Ladungsträger einer Art durch die eine Schottky-Barriere injiziert, während die andere Ladungsträgerart durch die andere Barriere blockiert wird. Demgemäß konnte ein und derselbe intrinsische Si-Nanodraht-SBFETs sowohl n- als auch p-leitend betrieben werden, ohne von Dotierung Gebrauch zu machen. Die scharfen metallurgischen Grenzflächen, die dünnen aktiven Si-Gebiete und die dotierungsunabhängige Kontrolle der Polarität könnten prinzipiell zukünftige komplementäre Logik auch bei nanoskaligen Gatter-Längen ermöglichen.

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Introduction

Motivation

Most of today's semiconductor industries rely on inexpensively doubling the number of components per chip approximately every second year. This trend, which is known as Moore's law [Moo65] has been successfully applied since the mid 1960's. To partially fulfill this goal, the electrical devices integrated within these chips are miniaturized every technology generation, i.e. the device density is increased. Simultaneously, Moore's law enables to boost the device's performance, since its power consumption is lowered and the speed per function is increased. As the 45 nm technology node has recently been introduced for mass production [Int], transistors with ∼160 nm gate pitch are readily fabricated. For future device generations, technological and physical apparent roadblocks are approached at a fast pace.

Independently from the challenging fabrication of nanoscale transistors, their miniaturization following the classical scaling rules leads to a performance degradation. For instance gate leakage currents increase due to quantum mechanical tunneling through the thin gate oxides, short-channel-effects degrade the off-currents and shift the threshold voltages, and the resistivity of small diameter interconnects rises exponentially as size-effects rise up. A common approach to compensate short-channel-effects is to introduce doping pockets near the source and drain regions. This in turn is difficult to control accurately as sharper doping profiles are required. Due to these technological and device-performance related limitations, there is an increasing effort in finding alternative fabrication approaches as well as device concepts to guarantee the continuation of Moore's law.

In this context, bottom-up fabrication approaches are attractive candidates which could provide possible add-on or replacement components to and of the established top-down processed complementary metal oxide semiconductor (CMOS) technology. One promising bottom-up fabrication approach extensively investigated today is the *particle mediated growth of nanowires*. A nanowire (NW) can be defined as a rod-like structure with a thickness

or diameter in the nanometer scale and a significantly larger length. In a very simplified phenomenological manner the particle mediated NW growth can be described as follows. A material is supplied in the gas phase and is finally preferentially deposited in the solid phase between the particle and the underlying substrate. The deposition takes place layer by layer, where the size of the deposited layer is in most cases similar to that of the particle. As the layers are stacked over, the particle is being displaced upwards and a monolithic extension, i.e. the NW, is formed between the particle and the substrate. A large variety of materials have been grown as NWs, most of them are single-crystalline semiconductors or metals.

Distinctly from today's semiconductor top-down manufacturing approach, the inherent bottom-up nature of the NW particle assisted growth gives simple access to the fabrication of sub-lithographic structures. Once the particle´s diameter is defined, the NW´s diameter will consequently be adjusted by the latter one as well. Another advantage is that remarkably smooth NW surfaces can be synthesized in contrast to lithographically patterned structures. In addition, given the fact that the NW's lattice is able to relax more efficiently than a layer, heterogeneous integration of a large variety of materials is possible.

Numerous studies currently concentrate on NWs made of silicon (Si), the mostly used semiconductor in today's electronics. Silicon nanowires (SiNW) are interesting to electronic applications, because principally they enable the potential to combine the well established Si CMOS technology developed and studied for the last 50 years with the advantages of one dimensional electronics.

Aims and Approaches

The objective of this thesis, is to study the synthesis and electrical transport properties of metallic and SiNWs. In particular, the fabrication and characterization of high performance devices is expected. These are then to be assessed and benchmarked with state-of-the-art electronics. In the coarse of this work, a special arrangement of these materials was chosen as a promising material combination to be studied and implemented to enable high performance electronics. This is the case of longitudinal nickel (Ni) silicide to intrinsic SiNW heterostructures, i.e. the sequential arrangement of these materials along the length axis of the NW. The studies are of special interest, because metal to semiconductor contacts with nanoscale contact areas have not been yet studied extensively enough.

To fulfill the main objective of this work, the following approach was fol-

lowed. First, the chemical vapor deposition chamber had to be adapted to be capable of growing SiNWs with the particle mediated growth. Following this, the growth of SiNWs had to be established and optimized to give single-crystalline SiNWs with controllable diameters. Consequently a processes had to to engineered to transform the grown SiNWs into Ni silicide NWs by a solid state reaction between the SiNWs and Ni. With the help of test structures, the fabrication of SiNW field effect transistor demonstrators should be performed. Consequently the SiNW devices should be characterized electrically and the transport mechanisms had to be studied in detail. From the characterization data and transport studies information needed to be extracted to optimize the transistor fabrication or even the NW growth.

Structure of This Thesis

Chapter 1 will describe the state-of-the-art of current CMOS technology and recent advances in order to motivate these studies. Basic issues of the growth and electrical characteristics of NWs will be sketched as well. In the same chapter a brief overview is then given on the current status of research in NWs. Chapter 2 will then present the growth experiments performed in this work and will give a structural analysis of the NWs grown under the most convenient conditions for post-processing. The transfer of SiNWs from the growth substrates onto test chips for post-processing and contacting with Ni reservoirs is described in Chapter 3. Consequently, the solid state reactions giving the Ni silicide formation along the SiNW and enabling Ni silicide to Si NW heterostructures are studied in Chapter 4. Chapter 5 deals with the fabrication and electrical characterization of Schottky barrier FETs. The transport properties and scaling properties of these devices are studied in Chapter 6. The conclusions from Chapter 6 are used to design novel transistors with added functionality as shown in Chapter 7. Given the fact that the present work encompasses different topics, most chapters contain a brief theory section. As a consequence Chapter 1 only contains a short theory section.

This work was performed in both a universitary and industrial research environment. This was given through the cooperation between the Institute of Nanoelectronics at the Technische Universität München and the company Infineon Technologies AG, since Mai 1st. 2006 Qimonda AG. Most of the experimental work was carried out in Infineon's Corporate Research labs an was continued in Qimonda's Materials Research group. Measurements and simulations both took place at the Institute for Nanoelectronics and the industrial labs cited above.

Chapter 1

From CMOS Scaling to Nanowire Electronics

This chapter has the purpose of motivating the interest in NWs as elementary units for future electronic applications as well as describing the basic issues of NW fabrication. Accordingly, the first part describes the ongoing classical CMOS scaling development and its possible future roadblocks. The currently proposed possible solutions to these limitations are discussed. It is shown why amongst various alternatives, NW electronics are promising candidates for post-CMOS applications. In addition, this chapter shows different concepts for fabricating NWs, including both top-down and bottom-up approaches. Finally, a brief historical overview on the synthesis of NWs is given.

1.1 CMOS and Moore's Law

The vast majority of semiconductor devices implemented in today's microelectronic applications are *Metal Oxide Semiconductor Field-Effect Transistors* (MOSFETs) [Han02b]. The success of the planar MOSFET in comparison to the bipolar transistor is mainly due to its cheaper fabrication costs and to its design and development simplicity while scaling down the dimensions.

As predicted by Gordon Moore in 1965 [Moo65], the integration density per chip has quadrupled every technology generation, corresponding to approximately three years. As a contribution to this integration increase, the transistor area has shrunk by a factor of two every generation yielding a length scaling factor of $1/\sqrt{2}$. The remaining factor of two has been achieved by employing a larger chip area and an optimized layout design [Han02a]. Down-scaling of the devices increases the transistor speed, since the electrons have a shorter channel path, or gate length L_g, to overcome between source

and drain. In addition, following this classical classical scaling reduces the power consumption per function.

MOSFET down scaling without major transistor design modifications has been possible possible down to 1 µm gate lengths [TN98], where the depletion layer between the source and drain regions and the bulk silicon have a considerably short characteristic length in comparison to L_g. The effects below $L_g = 1\,\mu m$ known as *Short Channel Effects* are circumvented by doping profiles in the channel which, in turn, reduce the carrier mobilities [Sze81]. Sub 100 nm gatelength MOSFETs furthermore require am enhanced electrostatic channel coupling to the gate in order to reduce parasitic effects [TN98]. As a consequence, new device geometries and concepts are needed to be able to continue with the ongoing increase of the chip density.

1.1.1 Bulk MOSFET Scaling

From a functional point of view a MOSFET is a three terminal device, where the potential applied at one electrode, named *gate*, steers the conductance between two other electrodes, *source* and *drain*. The conductance control is provided by electrostatically adjusting the carrier concentration of a semiconductor layer which extends between source and drain. Specifically, a metal / dielectric / semiconductor capacitor stack is used to provide this layer and its required electrostatic coupling from the gate. The cross-section of a classical n-type MOSFET is sketched in Fig. 1.1. Here, the capacitor is formed by the surface of the p-silicon and the gate metal separated by Si dioxide as the dielectric material. Source and drain electrodes are the degenerately doped n^+ contact regions.

By applying a positive gate bias V_g the p-Si surface next to the gate oxide is depleted of its majority carriers, in this case holes. Simultaneously, the minority carriers(electrons) are attracted to the oxide/Si interface. For sufficiently high V_g values the band bending at the interface is so strong, that the intrinsic Fermi Level $E_F i$ aligns with the actual Fermi level E_F of the semiconductor. The region where this is given, is named *inversion layer*. In this case the inversion layer is a n-channel bridging from source to drain. Accordingly, the transistor type is denoted as n-type. The minimal V_g required to form the inversion layer is called the threshold voltage V_{th}. The resistance between source and drain is reduced as the inversion is reached and as the inversion increases. The abrupt channel resistance difference at V_{th} makes the MOSFET a gate controlled switching device. By applying, a positive voltage between drain and source V_{ds} the electrons are drifted through the channel and a significant drain current I_d flows.

A p-type MOSFET works under the same principle, only that the formed

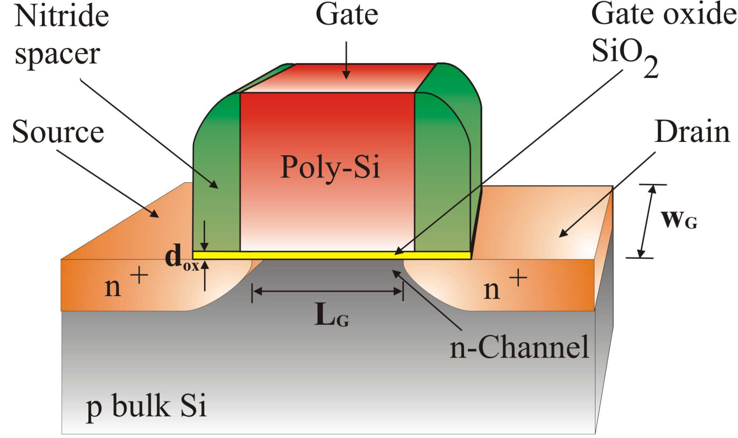


Figure 1.1: Schematic view of a bulk MOSFET, n-type.

inversion layer is a hole channel. To enable its operation it is therefore required to invert the doping polarities in comparison to the n-type MOSFET as well as to invert the sign of the operating voltages.

Constant field scaling The most adequate and simplest method to scale down the MOSFET's dimensions is the constant field scaling. Here, the the device performance is ideally maintained, by keeping the internal electric field constant. The dimensions, as noted in Fig. 1.1, the operating voltages and the doping concentrations of the acceptors N_a and donors N_d are scaled by a factor $\alpha > 1$ as described in equations 1.1 and 1.2, where the apostrophe denotes the quantities after scaling:

$$L_g{}' = \frac{L_g}{\alpha}, \quad d'_{ox} = \frac{d_{ox}}{\alpha}, \quad W_g{}' = \frac{W_g}{\alpha} \tag{1.1}$$

$$V' = \frac{V}{\alpha}, \quad N'_{a,d} = \alpha N_{a,d} \quad . \tag{1.2}$$

The resulting physical quantities after scaling are [Sze85]:

$$I'_{d\,\mathrm{sat}} = \frac{I_{d\,\mathrm{sat}}}{\alpha}, \quad J'_{d\,\mathrm{sat}} = \alpha J_{d\,\mathrm{sat}} \tag{1.3}$$

$$f'_{\max} = \alpha f', \quad P' = I_d V_{ds} = \frac{I_d}{\alpha} \cdot \frac{V_{ds}}{\alpha} = \frac{P}{\alpha^2} \tag{1.4}$$

$$\xi' = \frac{V_g{}'}{h} d'_{ox} = \frac{V_g}{\alpha} \cdot \frac{\alpha}{d_{ox}} = \xi, \quad V'_{th} = \frac{V_{th}}{\alpha} \quad . \tag{1.5}$$

Equation 1.3 shows that the drain saturation current $I_{d\,\mathrm{sat}}$ is reduced and its density $J_{d\,\mathrm{sat}}$ is increased, because the cross-sectional area decreases. The maximum operation frequency f_{max} rises as the carriers have to travel a shorter path between source and drain (Equation 1.4). The power consumption P for direct and alternate current is strongly reduced by α^2. As described by Equation 1.5 the electric field ξ remains constant and the threshold voltage V_{th} is lowered, since the volume to invert is reduced [Sze85, TN98].

1.1.2 Short Channel Effects

The MOSFET miniaturization under these conditions was possible down to gatelengths L_g of approximately 1 µm [Pau94, TN98]. For the *long channel* MOSFET ($L_g >$ µm) the depletion region width (L_{dr}) between the source/drain implants and the channel lie far away from each other: ($L_g \gg L_{dr}$). As the depletion regions of source and drain approach each other, so that L_{dr} is comparable to $L_g/2$, the gate control over the channel is affected and the device performance is degraded. The observed deviations from the behavior of the long-channel MOSFET are described by the *short channel effects*. Two of them are described below in more detail.

SCE A further threshold voltage V_{th} reduction takes place because L_{dr} reduces the volume for inversion below the gate. According to the charge sharing model the inversion volume V_{inv} is given by

$$V_{inv} = (L_g - \frac{L_{drS}}{2} - \frac{L_{drD}}{2}) \ d_{ch} \cdot W_g \ , \tag{1.6}$$

where L_{drS} and L_{drD} are the depletion layer widths of source and drain respectively and d_{ch} is the thickness of the inversion layer. For short gate lengths, the depletion regions are in the order of L_g and reduce the inversion volume significantly, i.e. the depletion charge is reduced and a lower threshold voltage V_{th} is needed to displace the charge [TN98, Pau94]. This effect by its own is known in the literature as the Short Channel Effect (SCE).

DIBL For a long channel MOSFET the potential at the interface between the Si channel and the oxide, known as the surface potential φ_S is almost constant at the entire channel length. This means that the electric field at the channel primarily has a vertical component. For the short channel MOSFET the lateral electric fields between source and drain are comparatively high

and influence a great part of the channel. As a consequence φ_S is lowered. A high drain potential V_{ds} increases this effect and shifts the maximum of φ_S towards the source. This effect is named *Drain Induced Barrier Lowering* (DIBL). The lower φ_S barrier increases the subthreshold current $I_{\mathrm{sub\,th}}$ (I_d at $V_g < V_{th}$ for the n-MOSFET) reducing V_{th} to a further extent. Other effects related to the lateral source/drain fields are the *Punch-Through* and the *Channel Length Modulation*.

1.1.3 Novel Device Concepts

To countervail the drop of V_{th} caused by the DIBL and the the SCE effects extra doping regions within the active region and adjacent to S/D have been introduced. To generate these doping pockets, sharp doping profiles are necessary. As the MOSFET's down-scaling advances, it is increasingly difficult to accurately control this process. Also, high channel doping has the disadvantage of decreasing the carrier mobilities [SL00, Sze85]. For very short channels ($L_g < 50\,\mathrm{nm}$) alternative device concepts are in discussion as described below.

SOI MOSFET An interesting approach to improve electrostatics is the narrowing of the Si region below the gate. This is achieved for example with MOSFETs fabricated on *Silicon on Insulator* (SOI) wafers, which have a thin (e.g. 5 nm to 50 nm) crystalline silicon (c-Si) layer on top of a thick (e.g. 100 nm) Si oxide layer. The lateral source/drain field penetration into the bulk Si is thereby hindered. If the top Si layer below the gate is thin enough so that it can be depleted to its totality, the transistor is named *fully depleted*, otherwise *partially depleted*. The great advantage of fully depleted transistors is that they do not require a channel doping, if the gate work-function can be adjusted. Undoped channels have a higher carrier mobility, as a consequence the transistors drain current at the on-state I_{on} is larger [Sch01].

Double gate One of the most promising devices which effectively reduces short channel effects is the double gate field effect transistor (DGFET). In contrast to the SOI MOSFET, the Si channel of a DGFET is controlled by two opposing gates. Therefore the source/drain (S/D) lateral fields are shielded from the channel with more efficiency. A large fraction of the lateral field lines consequently end at the gates corners without entering the channel region [Sch01]. In the first instance, the DGFET works as two MOSFETs connected in parallel doubling I_d. For the case of a *volume inversion*, where

the entire Si layer is under strong inversion, I_{on} is expected to rise to a further extent [Sch01]. All in all the I_{on}/I_{off} ratio of a DGFET is high even at short channel lengths [SGZe03, Won02].

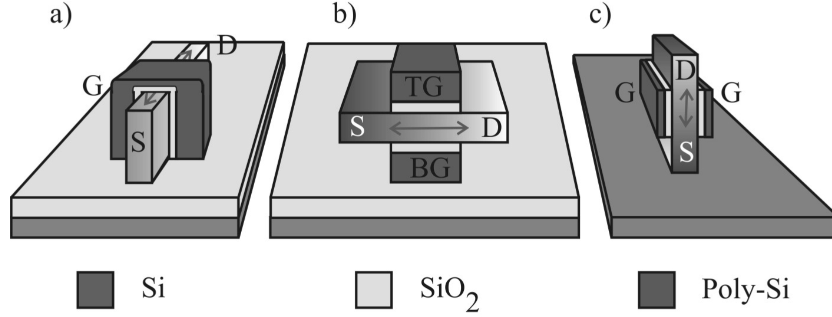


Figure 1.2: Double gate realization concepts, the red arrows show the current direction. a) FinFET, b) planar and c) vertical.

Double gate concepts Basically three different DGFET realizations can be distinguished, their designations depend on the direction of the electric current in respect to the wafer surface, they are depicted in Fig. 1.2. In the FinFET concept the current flow is parallel to the wafer surface, yet the channel and the gates are perpendicular to the surface. In the planar version, the stack layers of both gates as well as the channel are parallel to the wafer surface, causing the current flow to be parallel to the surface. In contrast, in the vertical DGFET the channel as well as the gates are perpendicular to the wafer surface, i.e. the current flow is also vertical to the surface. The DGFETs that are easier to fabricate are FinFETs. However, the Si surface facing the gate stack experiences a roughness caused by lithography and etching. This can lead to a mobility degradation due to increased surface scattering. Accordingly, the thickness of the active region can strongly fluctuate within the same device and from device to device, which could lead to a strong variability. These last two mentioned problems are also valid for the vertical DGFET. However, the advantages of this last implementation, is that it allows a lithography independent definition of L_g as well as a smaller device foot print. A double gate concept able to deliver flat Si surfaces facing the gate stack as well as a reproducible thickness of the active region is the planar one. Its fabrication is complex, since the gate structures have to be formed below and above the crystalline Si layer [IRWe04]. Moreover an

alignment between both gates is critical and self-aligned methods are difficult to be implemented [WIK+05].

Surround-gate nanowire FET The ultimate FET geometry should provide the highest possible gated surface per unit volume of the active region. The logical extension of this trend, which started with SOI FETs and continued with DGFETs is to completely surround the active region with a gate stack and to thin down the active region.This is the case of the wrap-gated nanowire (NW) geometry, as schematically seen in Fig. 1.2 d). In this concept the gate field can penetrate perpendicularly into the active region from all of the NWs' circumference. Consequently, it is easier to achieve a fully depleted active region even by applying lower electric fields. This fact relaxes to some extent the need of ultra-thin and high-κ dielectrics. As the area of the inversion layer is maximized with respect to the active regions volume, as compared to the DGFET concepts, high current densities are expected to flow in the on-state. Even with a single-sided gate the NW geometry shows beneficial electrostatics which could easily lead to a full depletion of the entire NWs volume.

1.2 Nanowires as Attractive Device Components

The interest in integrating nanowires is not only linked to the fabrication of ultimate FET concepts. Group III-V nanowires are used for other applications such as active regions for light emitting diodes, LASER diodes and wave guides. Also metallic NWs can be used as interconnects and field emitters. Recently, even phase change materials have been synthesized in the form of NWs. The following section compares the main methods used to pattern or synthesize NWs. The historical development of the vapor liquid solid growth mechanism is then summarized in Sect. 1.2.2.

1.2.1 Nanowire Fabrication Methods

Nanowires which can be used as the active region of FETs can be produced by two kind of methodologies: the top-down and bottom-up approach. In the top-down technique, the objects are formed by a layer deposition, local masking and consequent removal of the unmasked regions. This commonly encompasses the lithographical definition of the geometry followed by its etching. Both, horizontal and vertical NWs have been fabricated by the top-down

method as reported in literature. The great advantage of top-down fabricated NWs is its full compatibility with the state-of-the-art semiconductor manufacturing technology. However, the realization of NWs with thin diameters is limited by the available lithographic resolution. This poses great challenges for feature sizes below 65 nm. Other concerns of using the top-down technique for NWs are the large variability of the device dimensions within one wafer, as well as large surface roughness obtained for the NWs. For thin NWs the latter even translates into large diameter fluctuations affecting the reproducibility of the devices.

Distinctly from top-down fabricated NWs, the bottom -up approaches do not rely on masking and local etching. The NW-structures are rather 'built up' or grown at a defined position. Basically, two types of bottom-up techniques are popular, the growth in holey or porous templates and the particle assisted NW growth. The former method creates the negative structure of the template. Thus, the surface quality of the NWs depends on the wall-roughness of the template holes. In contrast, in the latter method, the NWs are grown as an extension to the particles. Once the diameter of the particle has been defined, the NW diameter is set as well. This also holds for small feature sizes making the growth of NWs with sub-lithographic diameters possible. Other dimensional parameters, as the length and the surface roughness are given by the growth conditions. Another benefit of the bottom-up approach is the principal ability to synthesize heterostructures with materials that could not be created as planar layers due to lattice miss-match.

1.2.2 Historical development of the nanowire growth

The ongoing research on nanowires has a rather long history. 1964, R. S. Wagner and W. C. Ellis from the *Bell Telephone Laboratories* reported for the first time the growth of semiconducting wires mediated by a metal particle [WE64]. In particular, they observed that under certain conditions using a Si-precursor, crystalline-silicon monoliths were formed in the presence of Au and more precisely extending between Au particles and the substrate. They named these Si-structures, Si-whiskers and proposed the first growth theory called vapor-liquid-solid (VLS) growth. Numerous studies followed to describe the VLS mechanism. Probably the most thorough models were given by the studies of E. Givargizov [Giv75] based on thermodynamic considerations. The calculations predicted that the VLS growth mechanism had a critical NW diameter ($\sim$100 nm) below which no NWs could be grown. This was in accordance with the results obtained up to then. Regardless of the large efforts in whisker research between the 1960's and 1970's the focus

in this field faded away.

It was not until the early 1990's when bottom-up and self-assembled approaches regained a strong attention. This was and still is mainly driven by the technological difficulties in fabricating structures with small feature sizes on a large scale wafer at a reasonable amount of time. The investigations were restarted by the group of Kenji Hiruma [HKO+91], [YKH91] from *Hitachi Central Research*, which explored the growth and electrical properties of group III-V whiskers with significantly smaller diameters (below 20 nm) than the ones synthesized previously. The discovery of the carbon nanotube (CNT) by Sumio Ijima [Iji91] in the year 1991, also brought the VLS model again into consideration as a possible mechanism of the CNT synthesis. But also the fact, that the electrical transport investigations in low-dimensional structures became increasingly important gave a large impulse in the need to synthesize NW structures. Alfredo Morales and Charles Lieber were the first to show the synthesis of Si-Nanowires with nanometer-scale diameters in 1998 [ML98]. From then on the efforts spent in NW research have been strongly increasing. The materials presently grown as NWs are numerous and mainly include group IV, III-V, II-VI semiconductor NWs, but also extend to metal silicides, transition metals and even chalcogenide materials. The NW synthesis is an increasingly active topic in the solid state matter research today as measured by the number of published articles per year [LL07].

Chapter 2

Growth of Silicon Nanowires

This chapter presents the main results of the SiNW growth experiments performed in this work. The main aim of these experiments was to establish a controllable and reproducible scheme for the synthesis of SiNWs with high structural quality. This is an important requirement for their posterior electrical characterization and implementation in electrical devices. The methods presented and dependencies studied here systematically lead to the established growth procedures applied for the posterior integration and characterization of the NWs. The first part of this chapter (Sect. 2.1) briefly describes the basic theory of the particle assisted growth of nanowires. From there on, Sect. 2.2 will present the setup used for the growth experiments. This will be followed by the description and results of the NW-growth experiments in Sects. 2.4 and 2.5. The last part of this chapter (Sect. 2.7) focuses on the structural characterization of the SiNWs by transmission electron microscopy. No vertical device integration was envisioned in this work. Nevertheless, the vertical growth of SiNWs on amorphous metallic layers is studied in Sect. 2.6 as a perspective for the fabrication of vertical SiNW based devices decoupled electrically from neighbor devices.

2.1 Basics of Nanowire Growth

In this section the fundamentals of the growth mechanism of nanowires are summarized. First, the Vapor-Liquid-Solid growth mechanism is described in Sec. 2.1.1. Note that in this work the following terms are reserved for the clarity of the descriptions. The term *growth-mechanism* denotes the physical and chemical reactions describing the NW-growth. Whereas, *growth-technique* refers to the setup-dependent implementation of the mechanism.

2.1.1 Nanowire Growth Mechanism

The VLS model This model will be explained in a simplified manner, according to the original model proposed by the pioneers Wagner and Ellis [WE64]. It should be mentioned, that depending on the growth conditions, techniques and starting materials used, the growth mechanism may differ from the VLS model. It is also noteworthy to mention that the VLS model is not able to account for numerous observations and thus still is under continuous development. The central idea of the VLS model states that the material to be grown as a NW has to undergo different phase transitions and that a mediator particle or impurity is required to enable these. The sequence is as follows: the material starts in its gaseous phase, passes through the liquid phase forming an alloy with a mediator particle and finally condenses as a crystal out of the alloy. Basically, the starting material in the gas phase can be a pure element or can build a compound with other elements. The following description considers the latter case. The process can be divided into the following crucial steps, also depicted schematically in Fig. 2.1:

1. Adsorption of the precursor molecules at the surface of the mediator particle

2. Catalytic decomposition of the precursor at the mediators' surface

3. Diffusion of the species into the mediator particle

4. Liquid alloy formation between the species and mediator

5. Supersaturation of the species in the alloy

6. Condensation of the excess material at the interface between the particle and the substrate as a crystalline monolayer

7. Monolithic extension of the deposited material

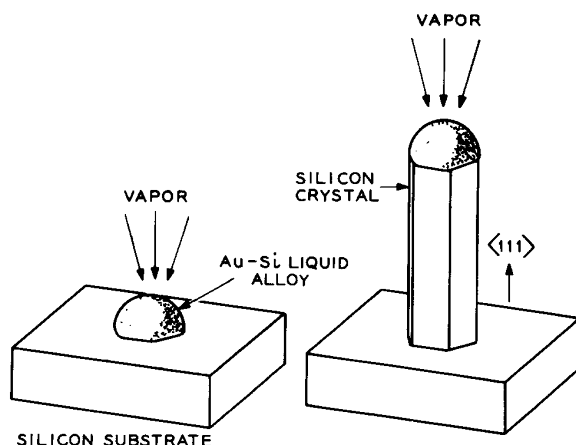


Figure 2.1: Sketch of the main steps for VLS growth. From [WE64]

Au-Si phase diagram The VLS process will be explained in more detail in the example of the Si nanowires synthesized with Au particles, as these are the materials of choice in this work. In order to better understand the phase transitions involved it is convenient to to analyze the Au-Si phase diagram reproduced in Fig. 2.2. Au and Si are miscible at all concentrations in the liquid phase if the temperature is sufficiently high. In contrast to that in the solid phase both elements practically do not create an alloy. A solid mixture can only be found when one of the elements minimally contains the other element, i.e. in a concentration below 2 atomic %. This is represented by the *solubility-gap* in Fig. 2.2 for temperatures below 363°C at practically all concentrations. However, transition regions exist where liquid Au can coexist with solid Si and liquid Si can be observed with solid Au. These regions are separated from the Au-Si melt by the so called *liquidus lines*. Following both liquidus lines to lower temperatures a crossover can be observed at the minimal Au-Si melt temperature of 363°C. This state, the *eutectic point*, is given at an atomic Au concentration of 18.6%. The uniqueness of this point is that a Au-Si melt can be precipitated into solid Au *and* solid Si if slowly cooled down. However, as noted above both solids are separated and do not create a homogenous solid alloy.

VLS step by step Throughout the following paragraphs the individual VLS steps will be elaborated on. The growth experiments are usually carried

out in a vacuum furnace. The substrate can be an amorphous material such as SiO_2 or Si_3N_4 or crystalline surfaces, such as (111) or (100) oriented-Si. Gold particles decorate the substrate surface to act as the mediator or catalyst. The compound silane, SiH_4, is used as the Si precursor. In the first step the Au-decorated substrate is heated in the vacuum chamber where the Si precursor is introduced in the gas phase. A certain amount of precursor molecules are adsorbed on the Au-surface, either through direct impingement or by impinging on the substrate and diffusing on the substrate surface until they reach the Au particles. Dissociation of the precursor preferentially takes place at the Au surface in the second step, due to the catalytic activity of Au.

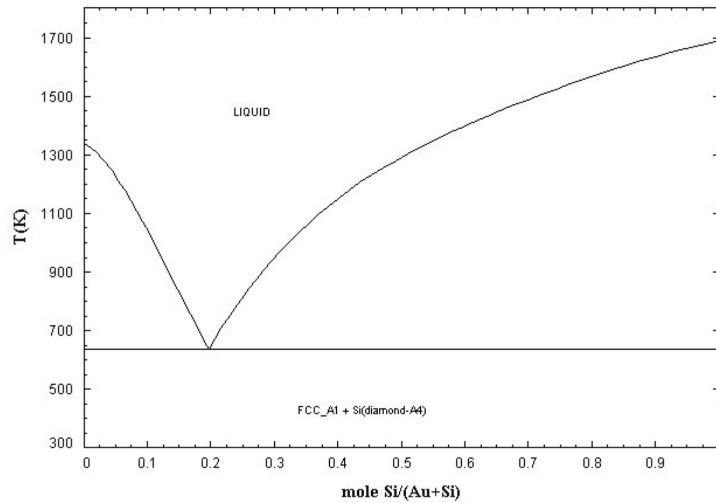


Figure 2.2: Phase diagram of Au-Si. From [SGT]

In the third step, free Si atoms are incorporated into the Au particle by diffusion. Commonly, the Au-particle is in its solid state at the beginning of the process. If the temperature is sufficiently high the incorporation of Si into the Au particle will eventually form a liquid alloy according to Fig. 2.2 and corresponding to step 4. Additional Si atoms can be introduced into the Au-Si melt until the *liquidus* line in the phase diagram is reached. If the pressure of the incoming Si atoms in the Au-Si melt is sufficiently high even more Si atoms will be introduced kinetically into the melt *supersaturating* it, this is denoted by the fifth step. Nevertheless, supersaturation is thermodynamically unfavorable so that the excess-Si condensates to lower the

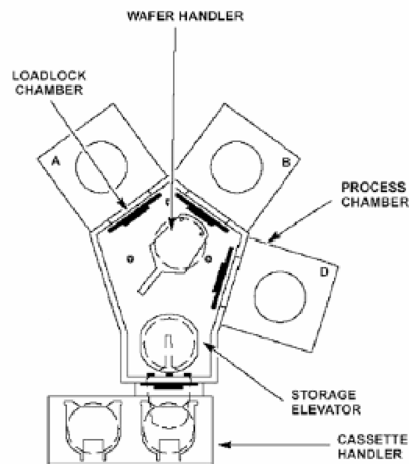
Au-Si systems energy, i.e. by returning to the Au-Si composition dictated by the liquidus line. The Si precipitation, which is the sixth step in the VLS process, preferentially occurs at the interface to the existing solid state, i.e. on the substrate. At the beginning a crystalline Si mono-layer is completed just below the Au-Si droplet. This Si layer roughly has the size or foot-print of the Au-Si droplet. After the completion of the first monolayer the next monolayer is formed on top. The Au-Si droplet is correspondingly elevated by each deposited monolayer. This process continues as long as more excess-Si atoms are incorporated into the Au-Si system, and the temperature of the Au-Si particle is above the eutectic temperature. The stacked Si-layers create a crystalline monolith as an extension to the Au-Si droplet, which is the seventh and last step in the VLS model.

Deposition selectivity Ideally, the substrate temperature is below the pyrolytic decomposition temperature of the Si precursor molecule, i.e. the temperature required to crack the molecule by the thermal energy provided, and above the temperature of catalytic dissociation at the gold surface. Given this scenario, no Si will be deposited on the substrate as a layer and radial growth of the Si-monolith will be suppressed. The particular characteristic of this growth mechanism is that the wire diameter is given by the foot-print size of the Au-Si droplet on the substrate in a self-adjusted manner. When the length of the monolithic Si-extension is substantially larger than its diameter it can be geometrically regarded as a wire and shows that the deposition mechanism is selective.

Limits of the VLS model The VLS model described above is limited to the observations gained in common chemical vapor deposition furnaces. However, the growth mechanisms seem to strongly depend on the techniques and materials used. For techniques like molecular beam epitaxy and metal organic chemical vapor deposition the surface diffusion of species to be deposited play an important role and limit the incorporation rate at the catalyst particle. Although enormous advances have been reported on the VLS study, this model has not been able to completely describe all phenomena observed in experiments. Alternative and complementary growth models to the VLS have been introduced. To explain for instance the growth at lower temperatures than the eutectic temperature of the mediator-particle and the species to be deposited, the vapor-solid-solid (VSS) synthesis [DKM+05] has been proposed. To avoid confusion, the term *particle-mediated* growth will be used here to name the nanowire synthesis, unless there are clear signs of a VLS growth.

2.2 Setup for Nanowire Growth

A low pressure chemical vapor deposition (LPCVD) cluster tool: *Precision 5000* fabricated by *Applied Materials* was used to perform the growth experiments. The cluster was equipped to process 6" diameter wafers. It comprised three independently controlled CVD chambers hooked onto a mainframe, as seen in Fig. 2.3. The mainframe chamber included a transfer robot as well as a storage unit with a capacity of up to 25 wafers. It was capable of being evacuated down to a base pressure of 100 mTorr and thus, served as a load-lock for the sample loading/unloading. Therefore, all CVD chambers remained in vacuum during the loading/unloading procedures and a sample transfer between chambers could be performed under vacuum. Two chambers (B + C) were used correspondingly for the deposition of Tetra ethyl ortho-silicate (TEOS) based silicon oxide and SiH_4-based Si_3N_4 and SiO_2. A third chamber (D) was chosen for the SiNW growth. This chamber was conceived as a single-wafer, cold-wall reactor. In its original conception, the gas flow was conducted vertically onto the substrate from a shower head and was exhausted from the bottom. The susceptor together with the residing process gases in the chamber were heated by lamps. These were located outside, at the bottom of the chamber. A quartz window allowed the heat coupling.



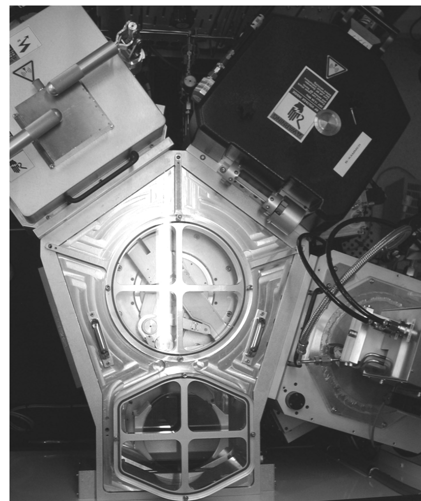


Figure 2.3: P5000 LPCVD-Cluster Tool. With three independent process chambers. a) Schematic top view, b) corresponding picture

In principle the D-chamber was viable for the NW growth experiments. However, some major modifications and additions were made to enable and improve the growth and pre-processing conditions:

- Exchange of the heater system to a direct resistive susceptor heater.
- Installation of a RF-plasma generator.
- Installation of a quadrupole mass spectrometer.
- Installation of the process-gas lines.

Heater system The original lamp heater had two major disadvantages. The first was the upper temperature limitation to 500°C and the second one the fact, that the process gases were also heated before the surface reactions took place, depending on the pressure applied. For these reasons a direct resistive heater located in the inner part of the susceptor was designed. A 500 cm long resistive coil with a resistance of 15.5 Ω/m was wrapped in the form of a spiral inside the susceptor made of *Inconel-600*. *Inconel* is a proprietary Fe-Ni alloy with high corrosion and oxidation resistance. It is stable up to 800°C and does not react with SiH_4. Two different thermo-couples were located inside the susceptor, one near the substrate surface and an other one near the heating coil. This susceptor was fabricated according to the costumers specifications by the company *Thermochuck*.

The susceptor was mounted on a ceramic arm to isolate it electrically and thermally from the chamber body. The four cables (two thermocouples and two ends of the heater coil) had to be brought out of the chamber for contacting. They were fed through an electrically isolated aluminum plate at the bottom of the chamber. An isolating-transformer *Statron, model: 5315.72* with variable power output (maximal value of 4.6 kW) serves as the current source for the heating coil. By this method, the growth substrate is mainly heated by conduction from the susceptor. Since the incoming gas into the chamber is at room temperature and has a high temperature gradient towards the heated substrate, heat transfer trough convection can play an important role depending on the gas flow and total pressure.

Plasma generator As pre-processing of substrates such as substrate cleaning from organic residuals is important prior to growth, a plasma generator was installed on top of the substrate. This radio-frequency generator (*R^3T Rapid Reactive Radicals Technology, TWR-2000T*) works in a downstream fashion, i.e. all gas lines are routed through the core of the generator, where a 2 kW magnetron is able to ignite a plasma inside three concentric discharge

regions. As a consequence of the gas stream, the remote plasma "flows" evenly on top of the substrate. The construction does not hinder the gas flow when no plasma is ignited. In this case the gas flow is also evenly distributed across the complete 6" substrate.

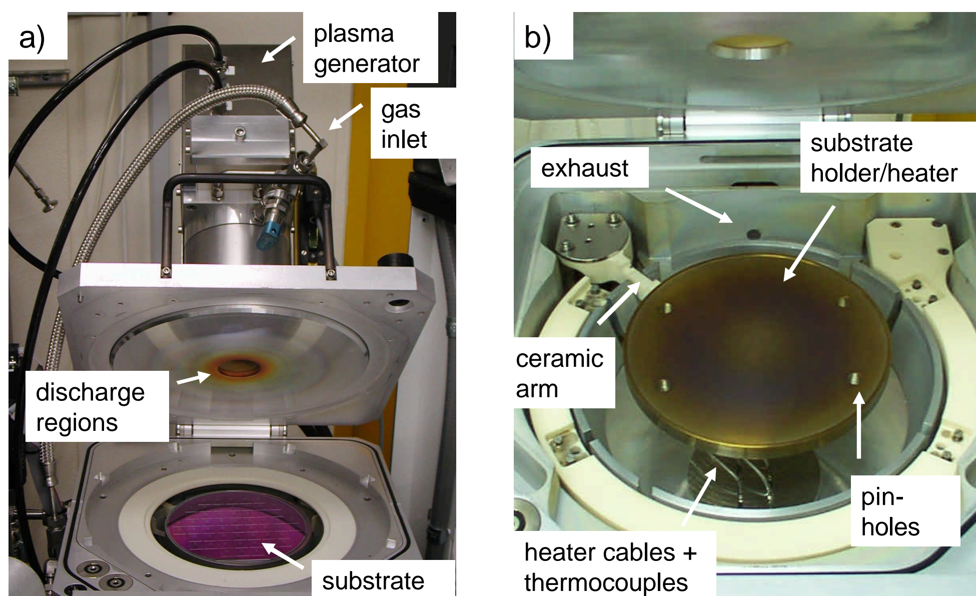


Figure 2.4: Modified CVD chamber for the growth of NWs. a) Microwave plasma generator mounted on top of the chamber. b) Direct resistive heater, electrically and thermally isolated from the chamber body.

Mass spectrometer To monitor the presence and composition of volatile species such as gaseous compounds and elements inside the chamber, a quadrupole mass spectrometer (QMS) was connected at the exhaust-side of the chamber. The QMS, *Hiden Analytics*, works at high vacuum, differing from the typical working pressures between 1 mTorr and 50 Torr in the chamber. Thus a capillary gas line connects the chamber to the QMS to accordingly reduce the pressure. This has the limitation of being slow and not being able to determine the exact composition ratios, since smaller species such as H_2 diffuse faster than larger molecules.

Gas lines and choice of gases Process lines and gases were installed for undiluted mono-silane (SiH_4) as the Si precursor, Ar, H_2, N_2 as process gases

and nitrous oxide (N_2O) as an oxygen source for oxidation. Silane has various advantages over the also commonly used Si precursors $SiCl_4$ and SiI_2. Silane has a lower pyrolytic decomposition temperature of about 630°C at 60 Pa [WMF96], [RM84] instead of 1150°C for $SiCl_4$ [RM84] and no etching reactants are created during the reaction as HCl in the case of $SiCl_4$ and I_2 in the case of SiI_2, preventing etch-back effects. Undiluted SiH_4 was preferred over a dilution with Ar or H_2 to offer a higher dilution flexibility. n-silane molecules of higher order n (Si_nH_{2n+2}), such as di-silane $n = 2$ (Si_2H_6) are thermally more stable than mono-silane and require substantially higher temperatures to be cracked.

2.3 Aims of the Growth Experiments

The aim of the growth experiments was to establish a reproducible bottom-up process process giving SiNWs which fulfill the following criteria, to make them suited for their integration as nano-scale components of electronic devices, particularly as the active region of field effect transistors:

- Single crystalline.
- Control of the crystalline growth direction.
- High structural quality, i.e. constant diameter along the NW length and low surface roughness.
- Tailored processes that enable different NW diameters with an homogeneous distribution.
- Access to sub-lithographic NW-diameters.

In particular, the single-crystalline quality is essential to guarantee good transport properties. Dislocations and grain boundaries are not desired, since they may degrade mobility or could induce undesired charge traps. The control of the diameters and crystal orientation as well as their homogeneity throughout the NW length are important parameters to guarantee the reproducibility of the electrical experiments. The reason for this is that the effective mass of the carriers and thus their mobility is strongly dependent on the direction in which they move along the crystal lattice, according to the dispersion relations [Kit66]. In order to explore the transport properties of NWs with diameters in the nanometer scale, it is extremely important that their surface roughness is low. These sub-lithographic structures are not easily accessible by industrial state-of-the-art top-down processing and

are in principle possible by the bottom-up approaches as the NW particle assisted growth. The process should be able to be tuned to give different NW-diameter distributions to enable size dependent transport studies. Finally, the compatibility with common *CMOS* manufacturing needs to be addressed, in particular the temperature budget and the introduction of metals at the *front end* of line.

In this work it was envisioned to process and characterize the electronic SiNW-devices planarly, by transferring individual NWs from the growth substrate to device processing substrates. However, a first approach in the vertical integration of SiNWs was also to be explored.

2.3.1 Catalyst Selection and Deposition

The selection of the catalyst plays a fundamental role in the temperature range required for the NW growth, the quality of the synthesized SiNWs and may influence their electrical characteristics. An important concern is the control of the size of the catalyst particles. As discussed in Sect. 2.1.1, the size of the catalyst particle determines the NW diameter. The shape of this catalyst particle is very likely to change during the catalyst pre-treatment, so that the actual NW diameter will be defined by the particle's shape at the moment of the nucleation. The suitability of a catalyst treatment is ultimately judged by the results of the grown NWs. Therefore, the effect of the catalyst treatment will be discussed in the respective growth Sections 2.4.1 and 2.5.

Selection of the catalyst material According to the VLS growth mechanism described in Sect. 2.1.1 a transition into the liquid phase between the catalyst and the material to be grown (Si) is a perquisite. In the best case this is given by the eutectic point in the phase diagram of the materials involved. In this experimental setup the pyrolytic decomposition temperature of SiH_4 (~600°C) restricts the choice of possible catalyst materials. This is due to the fact that the eutectic temperature between Si and the choice of catalyst must be well below this pyrolytic limit to suppress the planar deposition of Si. Some binary material combinations that have a low eutectic point are: Au-Si, Al-Si and In-Si. Their respective eutectic temperatures are: 366°C, 576°C and 646°C. This clearly shows that only Au matches the temperature criteria. However, the major concern about Au is its fast diffusion into Si and that it is able to create deep trap levels in Si [Sze81]. Also, its difficulty to be etched selectively poses major problems for its compatibility with CMOS integration. Nevertheless, the best results concerning the crystalline and structural quality of SiNWs have been obtained with the use of

Au. Also good electrical results have been previously presented for SiNWs grown with Au particles [CDHL00]. This makes Au the best candidate as a catalyst particle for the SiNW growth in this work.

Au deposition Two different methods were used to decorate the substrate surface with Au particles. One is the deposition of readily synthesized Au-particles or colloids suspended in solution. The other one is the deposition of a Au layer on the substrate with a following annealing step. The latter leads to coalescence and thus to the formation of Au clusters.

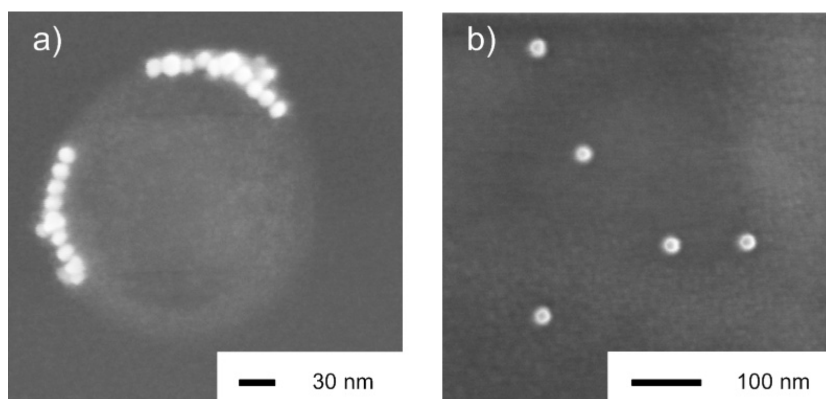


Figure 2.5: a) SEM image of as deposited colloidal solution. A large dried stabilizer particle with numerous Au particles adhered to its side. b) Au colloids on SiO_2 after a H_2O treatment.

Colloidal Au solution The deposition of the colloidal solution is a simple method, since these solutions contain already formed Au particles with a well defined diameter. Water based colloidal suspensions having different colloid diameter distributions are available with mean values down to 5 nm. However, *Van-der-Waals* forces lead to the aggregation of the particles in the suspension. To prevent this, the Au colloids are usually electro-stabilized with molecules promoting their electrostatic repulsion. This means that the colloid surface is negatively charged with a polar citrate molecule. The used colloidal solution, *Fluka 50755*, contains tri-sodium citrate hydrate as a polar stabilizer amongst other diluted salts. Figure 2.5 a) shows a SEM-micrograph for the deposition of 1 ml of this suspension on a SiO_2 substrate with an area of approx. 2.25 cm^2 inspected after drying on a hot plate. The crystallized salts can be seen as large spheres containing the small Au colloids (bright

particles) at its edges. These contaminate the substrate and must be removed entirely prior to growth.

Several processes were tested for the contaminant removal. These included H_2 and N_2O plasma treatments. Nevertheless, some contamination still remained. Alternatively, H_2O was used to dissolve the salts, as these are polar. This proved to be successful as seen in Fig. 2.5 b). The disadvantage of this process was, that most of the Au clusters were also washed away from the surface and only a few remained on the substrate. Using this process, a mean Au particle density of 5.5 particles per μm^2 was obtained on SiO_2 substrates. The diameter distribution of the Au colloids was measured by SEM. A mean value 17.5 nm with a standard deviation of only 2.1 nm was determined. Note that the resolution of the SEM is approximately 1 nm.

PVD deposited Au The second method for depositing the Au particles is physical vapor deposition (PVD) and subsequent annealing for coalescence. Among the various PVD-techniques *sputtering* was available. Here an Ar^+ ion beam is accelerated towards the Au-target with adjustable kinetic energies between 2 keV and 10 keV. The highly energetic Ar^+ ions kick-out Au atoms from the target by means of their kinetic energy. This results in a material beam directed towards the substrate. It is noteworthy to consider the remaining kinetic energy of the Au when impinging on the substrate. Through an applied substrate rotation a homogeneous coating over a range of up to 4 cm in diameter is obtained. The deposition rate is monitored with a quartz micro-balance. The nominal thickness of the Au layer, d_{Au}, is thus controlled by the duration of sputtering at a constant deposition rate. In order to obtain the particles, surface diffusion and coalescence of Au is required. Coalescence depends on various parameters such as the anneal temperature, pressure and duration as well as the substrate used.

Evaluating the success of coalescence The coalescence process is closely linked to the growth step, since it can be altered up to the point where NW-nucleation takes place. Probably the best possible method available to judge the success of coalescence is to directly analyze the SiNW growth results. Therefore, it makes sense to study the catalyst pre-treatment within the growth sections 2.4 and 2.5. An exception is given for Au particles deposited from a colloidal suspension because no significant changes such as fragmentation or clustering could be observed after annealing at 450°C on SiO_2 substrates. Therefore, no extra details on the behavior of Au colloids on SiO_2 need to be given in the next sections.

2.4 Growth on Amorphous Substrates

The main results of the experiments of growing SiNWs on amorphous substrates are shown in the present section. The experiments are carried out on 130 nm thick SiO_2 grown thermally on Si. Alternatively Si_3N_4 of the same thickness is used for comparison. These layers have a smoothness in the nanometer scale or better as confirmed by Atomic Force Microscopy (AFM) measurements. First the catalyst coalescence are optimized. Posteriorly, the dependance on basic process parameters as the total and partial pressure the ideal process parameters are determined.

2.4.1 Catalyst Treatment for Enhanced Coalescence

First a process had to be engineered to obtain a reproducible Au cluster formation with uniform diameters and density. As mentioned above, the most important criterion to judge the suitability of the coalescence processes was the quality of the SiNWs obtained.

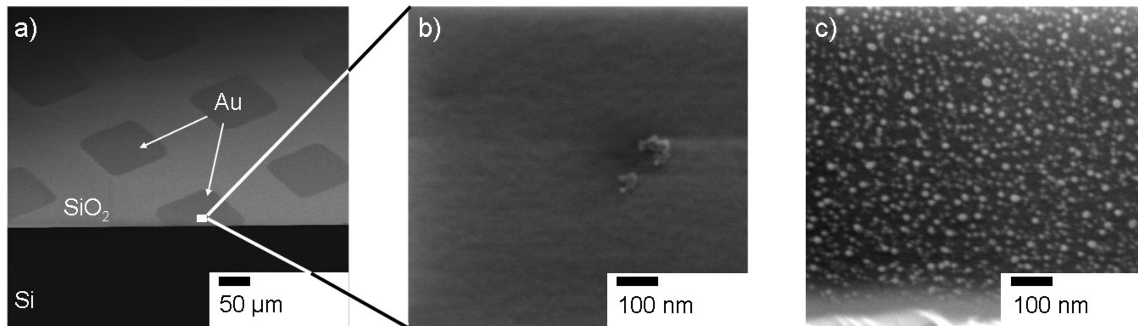


Figure 2.6: Tilted SEM images of sputtered Au with $d_{Au} = 1\,\text{nm}$. a) and b) directly after sputtering. b) shows a magnified view of a) inside the Au sputtered region. c) equivalent view of b) after approximately one year of shelf time.

As deposited Au layers Directly after sputtering Au on SiO_2 substrates, the Au has the form of a closed layer or an open layer depending on the deposited amount. Figure 2.6 a), b) shows a tilted SEM-view of a Au coated SiO_2 substrate with $d_{Au} = 1\,\text{nm}$. A shadow mask with a half-pitch of 100 µm was used to compare deposited with un-deposited areas on the same substrate. The SEM images were taken approximately one hour after the

Au sputtering, an important information as discussed below. As seen in Fig. 2.6 a) the surface has bright and dark regions resembling the shadow mask, where the dark squares correspond to the areas containing Au. However, as observed in the magnified image (Fig. 2.6 b)) within the region with deposited Au, the SEM is not able to resolve the structure or topology of this layer. It seems to be evident that at this initial stage no Au clusters are formed. Figure 2.6 c) shows an SEM micrograph taken from the same sample approximately one year after the Au deposition. Although the same parameters as in the sample depicted in Fig.2.6 b) were used a coalescence of the Au layer resulting in islands or clusters can be clearly observed. Since small Au-particles are not found in the surroundings of the largest ones, the coalescence is most probably governed by *Ostwald-Ripening* [Ost96]. This thermodynamic model describes the preferential coalescence of large islands at the cost of small ones. It should thus be noted that the "shelf-life" of the samples is an important parameter to consider before initiating the NW growth.

Coalescence enhancement of Au through annealing To speed up the coalescence, thermal activation was used. All anneal processes were carried out in the CVD chamber. This enabled a direct continuation with the growth process immediately after the catalyst treatments. Substrates having a nominal Au layer thickness d_{Au} of 0.2 nm, 0.5 nm and 1 nm were used for the experiments. The optimized coalescence process consisted initially of a single anneal step at 450°C, a pressure $p = 254$ mTorr for 300 s in H_2 atmosphere at a flow of 500 sccm. This indeed lead to the coalescence of Au into small islands as proven by Figs. 2.7 a) and b) in the example of a sample with d_{Au}= 0.5 nm. Nevertheless, the catalyst size varies strongly from 150 nm in diameter down to 5 nm. Also, the shape of the clusters is uneven and many of the particles are in contact with other ones. The size and shape inhomogeneity thus pose problems for a uniform and reproducible NW growth. Similar or greater diameter variances as the ones depicted in Figs.2.7 a), b) were the result of different anneal durations (30 s up to 1800 s) and temperatures (up to 550°C). The use of an alternative process gas, Ar, did not make a markable difference, either. Alternative catalyst treatments needed to be explored.

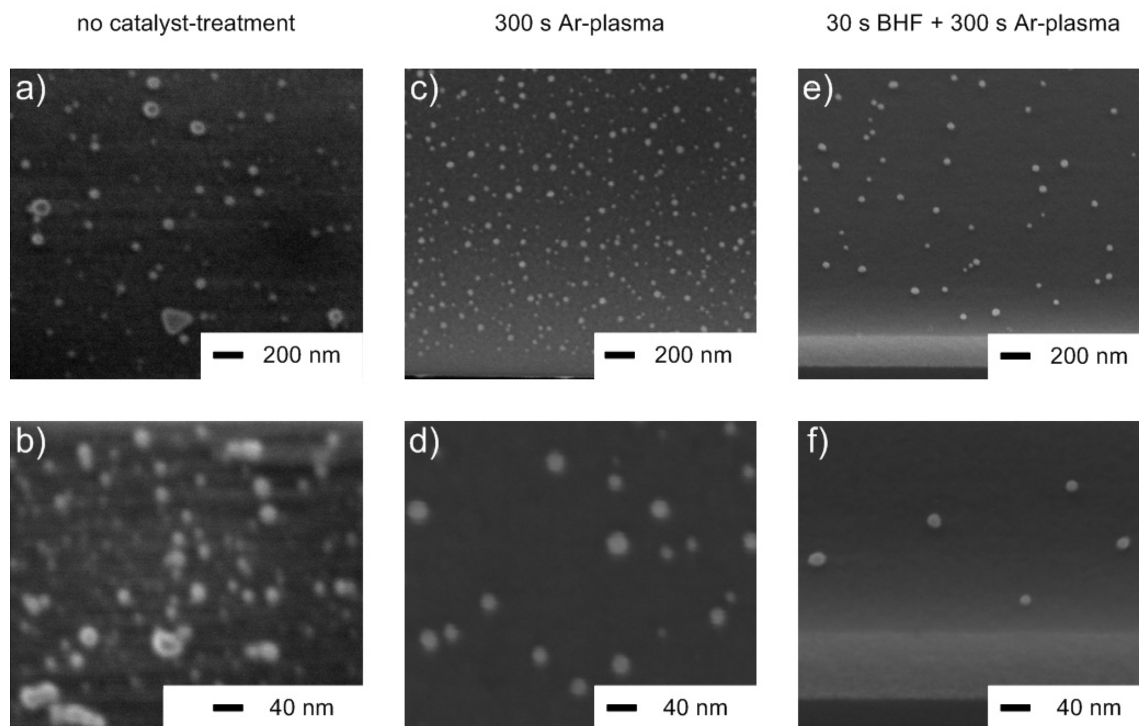


Figure 2.7: SEM images show the effect of Ar-plasma and BHF treatments on the coalescence of sputtered Au. All samples are SiO_2 substrates with d_{Au}= 0.5 nm, annealed at 450°C in H_2 at p= 500 mTorr. a), b) without pre-treatments, anneal for 600 s in H_2. c), d) anneal for 300 s in H_2 and posterior Ar plasma for 300 s at 450°C. e), f) As the previous sample but additionally 30 s in BHF 100:1 after sputtering.

Coalescence enhancement of Au through Ar plasma Further experiments showed that by applying a plasma process uniform coalescence strongly improved. Both, H_2 and Ar plasma processes were effective. However, the Ar plasma treatment was preferred, because the hydrogen radicals etched Si for example from the substrates side-walls and posteriorly deposited it in the surroundings. The best result was given as a combination of an anneal in H_2 at 450°C for 300 s directly followed by an Ar-plasma process. The anneal in H_2 had the same process parameters as the one reported above for the sample in Figs. 2.7 a), b). The Ar-plasma was employed at a substrate holder temperature of 450°C for a duration of 300 s with an Ar flow of 500 sccm at p= 416 mTorr. The power of the plasma generator was kept at 750 W.

Figures 2.7 c), d) depict the results of applying this recipe to a substrate with d_{Au}= 0.5 nm. The improvement in uniformity by using the Ar-plasma is evident when comparing this sample with the one on Figs. 2.7 a), b). The Au clusters have a rounder shape and are well separated from each other. Most importantly, the size variance between clusters is smaller. However, the diameters still typically range between 7 and 30 nm. One probable impediment for a homogeneous island formation is that a certain amount of the deposited Au is partially buried in the SiO_2. This is due to the considerable kinetic energy of the sputtered Au when impinging on the substrate surface. This assumption is based on the fact that thermally evaporated Au with the same d_{Au} and anneal conditions as the sputtered one showed different coalescence behavior as confirmed by later experiments not shown here. Sputtering was more accessible during this work than evaporation and was preferentially used.

Oxide etching for improved Au coalescence In order to improve the surface diffusion of the sputtered Au, a process was required to *free* or undig the Au particles. The solution was to slightly etch the SiO_2 surface. Starting from the newly sputtered Au layer, the substrates were dipped in NH_4F-buffered hydrofluoric acid (BHF) with a concentration of 100:1 for 30 s. This minimally etched the underlying SiO_2 nominally by 2.4 nm freeing the Au particles and breaking down the Au layer into pieces which can coalesce easily, as proven by SEM images not shown here. No significant change in the surface roughness of the substrate is expected by the SiO_2 etching step. The sample was then subjected to the H_2 anneal and Ar-plasma treatment explained above for Figs. 2.7 c), d). The result for d_{Au}= 0.5 nm is shown in Figs. 2.7 e), and f). Although the total quantity of Au seems to be reduced, uniform coalescence is greatly improved. The Au particle diameter ranges typically from 15 to 23 nm. AFM measurements in tapping mode corroborated the SEM results. Using this technique substrates with varying Au thickness d_{Au}= 0.2, 0.5 and 1.0 nm being subjected to the complete catalyst treatment process with the parameters given above for Figs.2.7 e), f) are compared in Fig. 2.8. The thicker d_{Au} is, the larger and denser the Au particles are formed. The complete process, encompassing BHF etch, anneal in H_2 and Ar-plasma treatment was reproducible and showed large advantages over the other processes when performing the NW growth. Note that the particle height in the AFM data is more representative than their width. Note that the width is a result of the convolution between the tip and the particle. A tip with a 18 nm radius was used for these measurements.

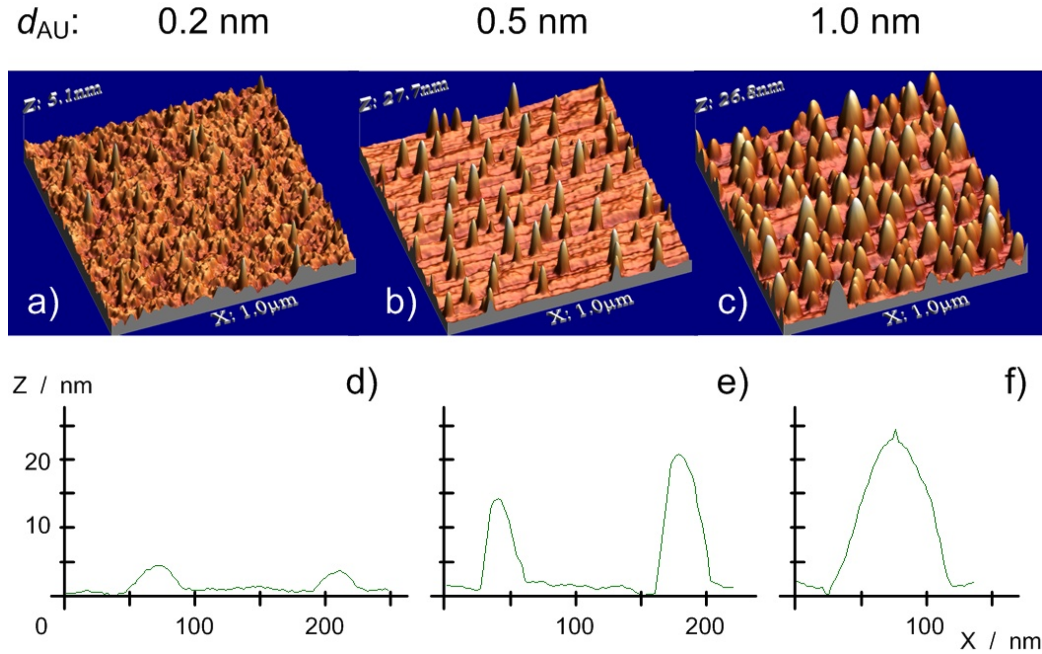


Figure 2.8: AFM measurements of Au sputtered SiO_2 substrates using tapping mode. Substrates with different d_{Au} are compared after BHF and Ar plasma treatments: 0.2 nm, 0.5 nm and 1.0 nm. a)- c) depict the topography of 1 µm × 1 µm areas. d)- f) show the cross-sectional sampling of individual clusters.

Impact of catalyst treatment on the NW growth Having optimized the catalyst treatment towards uniformity, the actual SiNW growth can be performed. In order to conclude with the evaluation of the coalescence the results on the grown SiNWs are presented here. For this, the optimized growth conditions to be shown in Sect. 2.4.2 were applied here. Here, the results of a series of growth experiments with and without the application of the different catalyst pre-treatments described above are compared. In the example of a SiO_2 substrate with d_{Au}= 0.5 nm growth was performed for 300 s at the following conditions: substrate growth temperature T_{grw} = 450°C, SiH_4 diluted in H_2 at a SiH_4 partial pressure p_{SiH_4} = 1.22 Torr, and a total pressure of p_{tot} = 50 Torr. Figure 2.9 a), b) show the SiNW growth results for substrates only having a heat treatment of the catalyst at 450°C for 300 s in H_2. The effect of the latter anneal and subsequent 300 s of Ar plasma, both at 450°C on the NW growth is seen Fig. 2.9 c), d). Finally,

Fig. 2.9 e), f) depict the impact of a 30 s BHF dip combined with the latter anneal in H_2 and Ar plasma treatment.

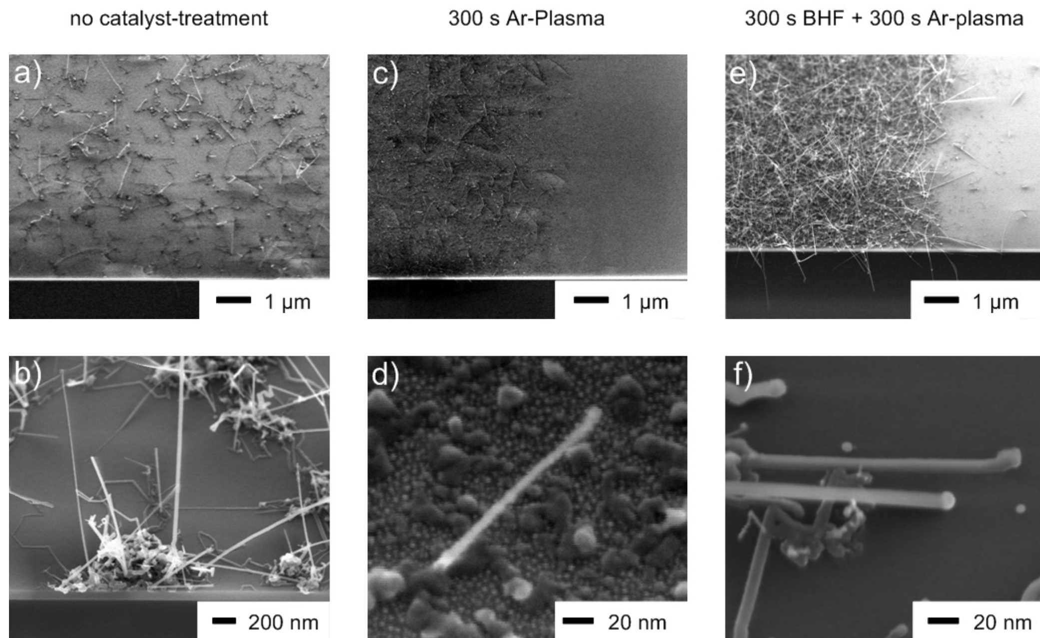


Figure 2.9: SEM images showing the dependence of the NW growth on the conditions of the pre-treatment of PVD deposited Au on SiO_2. All grown at 450°C for 300 s with $p_{SiH_4} = 1.22$ Torr. a), b) Without pre-treatments. c), d) With Ar-plasma for 300 s. e), f) With the same Ar-plasma treatment and a previous 30 s BHF etch.

For the case of no catalyst treatment the NWs exhibit a wide range of diameters and low density. Moreover, they principally grow in bundles out of large debris-like clusters composed of Si most probably in its amorphous or poly-crystalline form as seen in Fig. 2.9 b). The composition of the clusters was confirmed to be Si and Au by energy dispersive X-ray (EDX) spectroscopy. In the case that anneal in H_2 and Ar plasma is applied, a higher number of NWs per unit area seem to nucleate as seen in Fig. 2.9 c). However, small Au particles seem not to nucleate NWs and lead to the deposition of small Si clusters as seen in Fig. 2.9 d). In contrast to the debris-like deposition in Fig. 2.9 b), the Si clusters in Fig. 2.9 d) are deposited "planar" on the substrate and seem to be the result of single Au particles. Whereas in Fig. 2.9 b) the large over-stacked depositions are probably the

result of a large number of particles which appear to cluster together. This is in good agreement with the SEM image of the cluster in Fig. 2.7 b). The density of NWs grown is highly increased when the Au sputtered substrates are dipped into BHF as shown in Fig. 2.9 e). Although less particles are available per unit area due to the BHF etch, more particles nucleate NWs. One reason, why NW-nucleation is significantly enhanced when applying BHF could be that the Au catalyst is not partially embedded in the SiO_2 in contrast to the samples without BHF treatment. These results clearly show the importance of the catalyst treatments with the aim of enhancing the NW yield and quality.

2.4.2 Growth Conditions

In the following experiments, the growth conditions are optimized with an emphasis in obtaining a high yield of NWs grown with high morphological quality (no tapering, no kinks), and engineered towards suppressing the deposition of amorphous or poly-crystalline Si between the NWs. First, the dependance on p_{SiH_4} on the NW growth is investigated. Following this, the effect of p_{tot} and the carrier gas on the SiNW growth is analyzed. Finally the dependence on temperature is explored.

Dependence on Partial SiH_4 Pressure

Evaluation method The search for the appropriate growth pressure was carried out by employing undiluted SiH_4. The remaining growth parameters were maintained constant in all experiments: $T_{grw} = 450°C$, growth duration $t_{grw} = 300\,s$. In each case the substrates with $d_{Au} = 0.5\,nm$ were used and were subject to the previously described catalyst treatment: BHF dip for 30 s, a 300 s anneal in H_2 at 450°C as well as an Ar plasma treatment at 450°C for 30 s. Figure 2.10 summarizes the results using representative SEM images at various magnifications for different growth pressures ranging from 87 mTorr up to 50 Torr. The top row mainly shows the typical NW growth yield, density and length. The regions displayed here encompass the transition between a region containing Au located at the left and a Au-free region at the right. The second row depicts the Au deposited region at a higher magnification where the NW morphology can be seen with more detail at the substrate surface. The last row of SEM images is taken at an even higher magnification and shows the surface quality of the NWs and the substrate surface. These images allow an assessment of the deposition of planar Si between and on the SiNWs.

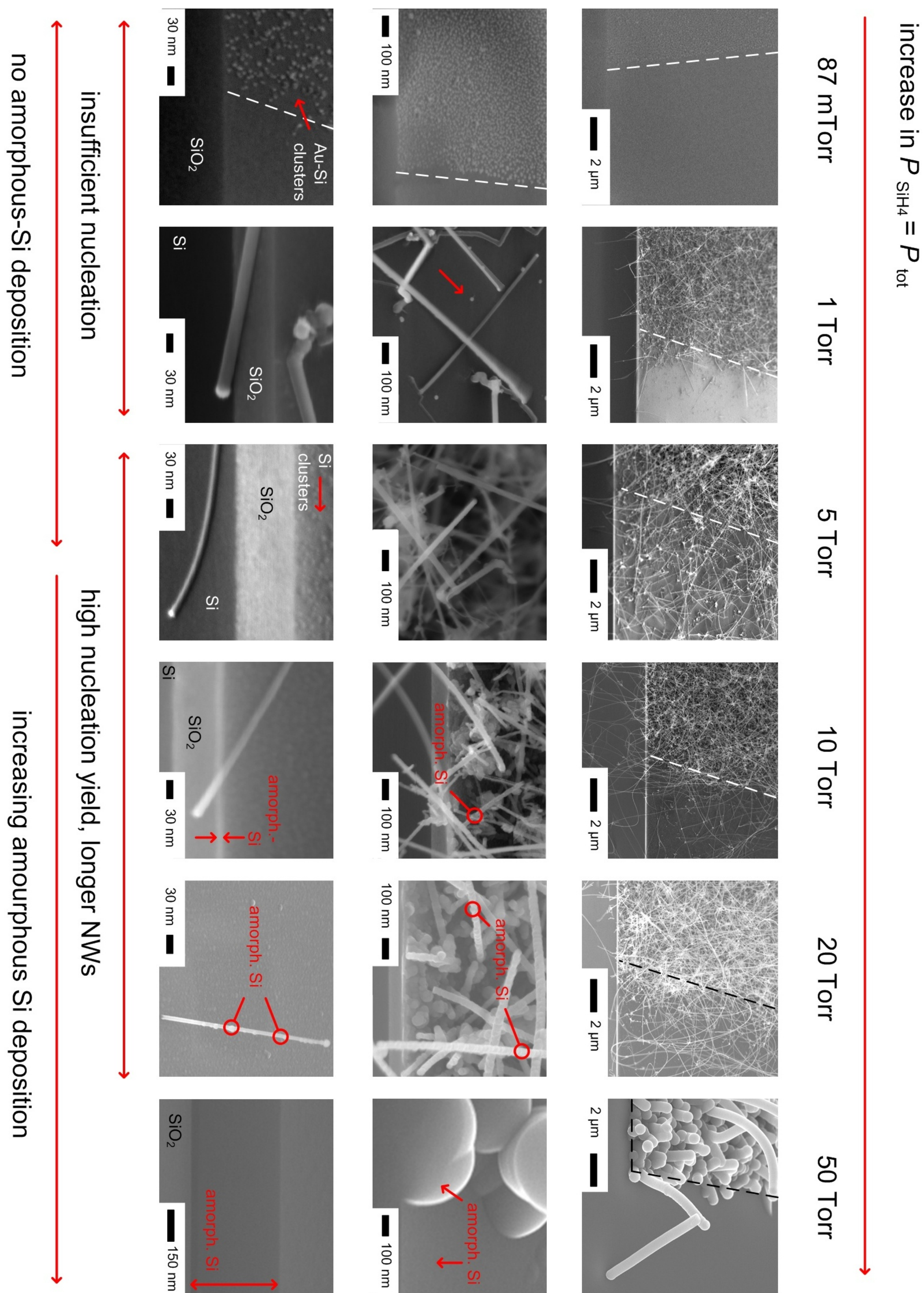


Figure 2.10: Dependance of NW growth on SiH_4 partial pressure.

Insufficient p_{SiH_4} Principally it can be observed that a minimal pressure is needed to nucleate NWs at all. At 87 mTorr, only the Au clusters can be observed, without any sign of forming a monolithic Si extension or NW. The minimal p_{SiH_4} for NW growth under the described conditions is between 87 mTorr and 1 Torr. At 1 Torr NWs clearly form, although not all Au clusters are effective in nucleating NWs, as seen in the second row of images. Also, a close look at the base of the NWs reveals that before the formation of a free standing NW there is some Si deposition resembling a "creeping" NW on the substrate. This confirms that the deposition took place from the Au particle. However, the effective NW nucleation was initially not successful. Only, after a first stage of growth resulting in Si without a well-defined shape, a free-standing NW forms.

Optimal p_{SiH_4} A further increase in pressure leads to a higher yield in the NW nucleation. At p_{SiH_4}= 5 Torr, effectively all Au clusters form NWs. The typical length of NWs increases from 2 µm at 1 Torr to 5 µm at 5 Torr. In the image in the lowest row it can be noticed that the SiO_2 surface is decorated with small Si clusters, although no Au catalyst particles are left on the substrate according to EDX measurements. These small Si clusters are the beginning of the formation of an amorphous or poly-crystalline planar deposition of Si. Also, note that at this pressure no Si clusters are formed on the NW surface, probably because the latter experiences a lower temperature due to the reduced heat conduction of a 1-D structure (NW) in contrast to the one in the bulk substrate.

Excessive p_{SiH_4} If the pressure is doubled to 10 Torr the NW length increases even further to typically 20 µm in length. As seen in the SEM image of the third row, a closed Si layer is formed on the SiO_2 substrate. Its thickness amounts to approximately 10 nm. It can be further observed that the tip of the NW does not have such a coating, because the NW diameter is comparable to the layer thickness. However, the second row SEM image shows that the NW surface near the substrate is rough suggesting the planar deposition of Si between the NWs. The Si layer can be either be amorphous or poly-crystalline. In the following text this deposition will be named amorphous mainly because no grain boundaries as typically observed in poly-Si are not found and because, the conditions applied here do not correspond to the ones for optimal poly-Si formation [WMF96]. When the pressure is increased to 20 Torr, larger NsWs are grown resembling long fibers. The typical NW lengths amount to 30 µm. The planar Si deposition on the substrate increases as well, amounting to 20 nm. The deposition of Si is now

also found on the NW sidewalls. In contrast to growth at p_{SiH_4}= 10 Torr, at 20 Torr the Si coating is formed along the entire NW's length. In the case that p_{SiH_4} is increased to 50 Torr, the planar Si deposition is so strong that it strongly suppresses NW growth. Only NWs with a maximal length of 4 µm are formed. A conformal Si coating covers the NWs. This implies that the NWs were initially formed in the time when the pressure was risen to 50 Torr. At a certain pressure above 20 Torr the planar deposition was so strong, that it eventually covered the catalyst Au particle quenching the SiH_4 supply and consequently stopping the NW growth. The higher magnification SEM images show that the deposited Si layer has a thickness of 300 nm.

Analysis Summarizing the results of the p_{SiH_4} series at 450°C using undiluted SiH_4, SiNW growth is only possible above a threshold pressure which lies between 87 mTorr and 1 Torr. However, p_{SiH_4} has to be increased up to 5 Torr so that every Au cluster is able to form a NW, indicating an efficient NW nucleation. But also, starting from this pressure a competing planar Si deposition begins. Initially, at 5 Torr the deposition of Si starts in the form of small Si clusters only on the substrate which at higher pressures first covers the substrate and eventually the NWs. An overshoot in pressure finally quenches off the NW growth. In order to interpret these results it is important to mention that during the experiments the gas flow towards the exhaust was set to its minimal value with a controllable throttle valve until the desired "accumulated" pressure was reached. Due to the fact that the gas supply is at room temperature a strong thermal conduction from the substrate upwards takes place by convection. Thus, at higher pressures a faster NW heating is expected, which would explain why the deposition on the NW is delayed in reference to the deposition on the substrate. Simultaneously, the number of available SiH_4 molecules at higher p_{SiH_4} increases linearly, principally leading to increased molecular collisions and pyrolytic decomposition. The bottom of the line is that the most convenient p_{SiH_4} to grow NWs is around 5 Torr. This is the only region in pressure combining a high NW nucleation yield with the suppression of a radial growth.

Dependence on Total Pressure and Effect of Carrier Gases

Next, the effect of a carrier gas is investigated. Hydrogen is used as the dilution gas, because SiH_4 is more stable in it compared to Ar or N_2. In addition, hydrogen is able to passivate open Si bonds principally hindering the NW's oxidation, given the background O_2 pressure. By keeping p_{SiH_4} constant at 5 Torr, which turned out to be the optimal value according to the experiments above, the total pressure is set by adding H_2 with a par-

tial pressure p_{H_2}. Thus the effect of p_{tot} on the NW-growth is able to be analyzed. Correspondingly, the total gas flow is increased. As in the previous experiments, other growth parameters are maintained constant: d_{Au}= 0.5 nm, T_{grw}= 450°C, and t_{grw}= 300 s. In all cases the standard catalyst treatment described above is performed directly before growth. Figure 2.11 visualizes the dependence on p_{H_2}.

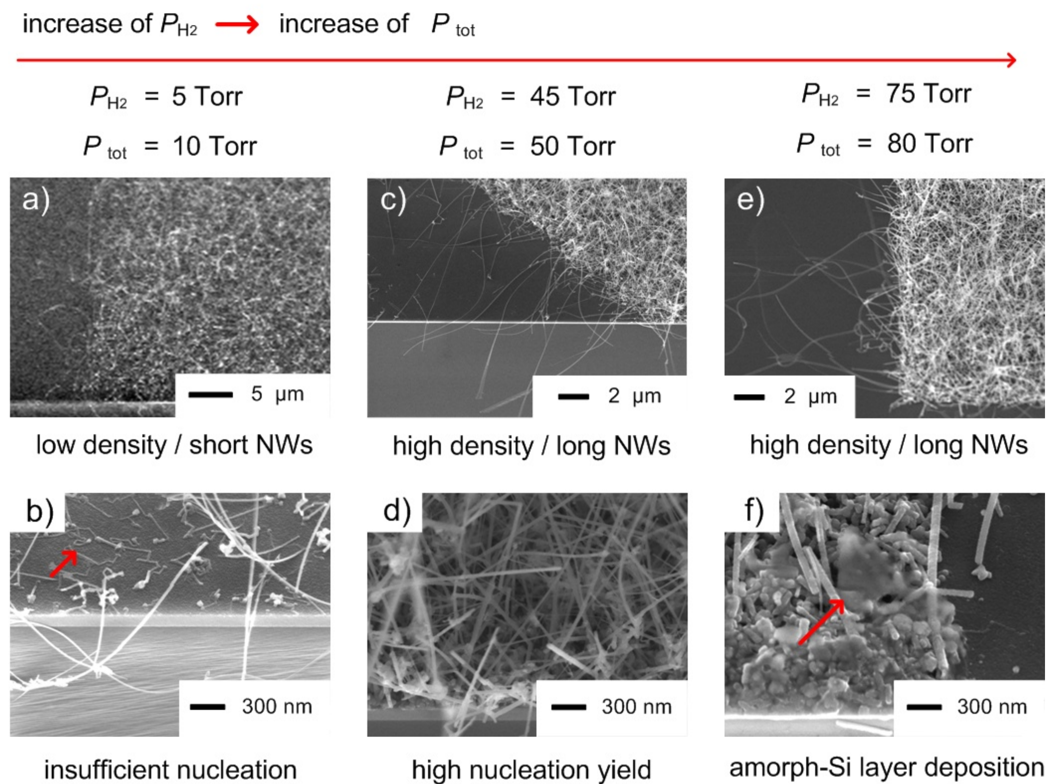


Figure 2.11: Dependance of NW growth on total pressure p_{tot} through increasing H_2 partial pressure p_{H_2}. "amorph." stands for amorphous.

In Fig. 2.11 a), b) 5 Torr of H_2 are given to the SiH_4 increasing the p_{tot} to 10 Torr. A large amount of the catalyst particles exhibit no NW nucleation but only induce a creeping-like deposition behavior, as already described above. This translates into a lower NW yield. The typical NW length amounts to 5 µm. When 45 Torr of p_{H_2} are added to the 5 Torr of SiH_4, the NW nucleation is strongly enhanced as seen in Fig. 2.11 d). The NW

length also increases to typically 10 µm. A last experiment was carried out with p_{H_2}= 75 Torr and p_{tot}= 80 Torr. Under these conditions the deposition of planar Si clearly limits NW growth, as seen in Fig. 2.11 f). Here some NWs can have lengths of up to 10 µm. Nevertheless some of them are covered by a planar Si deposition and can not continue to grow. This deposition takes place only at the NW's bottom, near the substrate surface. In contrast to Fig. 2.10 for p_{SiH_4}= 80Torr, the deposition starts before many of the NWs can form and it is not conformal. Although the layer morphology is different, this shows that both the amount of available SiH_4 and an increased gas temperature by convection are both critical parameters to be controlled in order to suppress a Si layer growth.

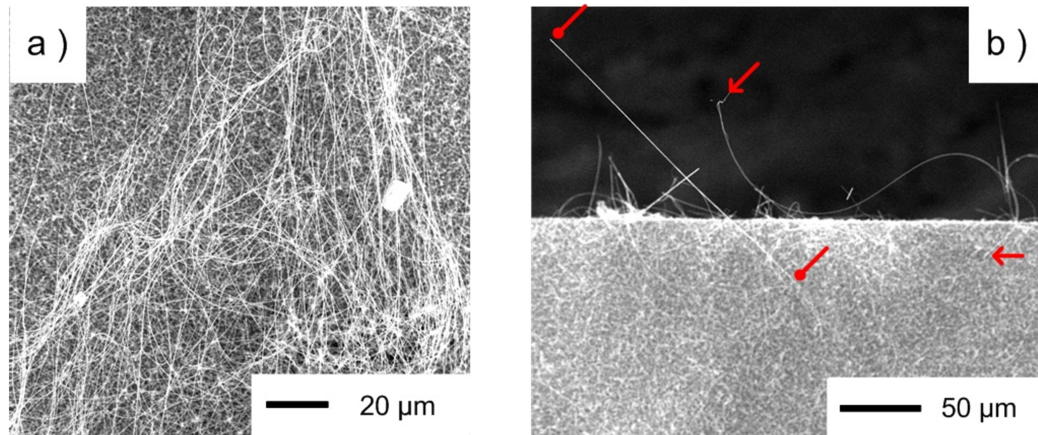


Figure 2.12: Growth of 0.25 mm long NWs.

Effect of Convection

Examining these data it can be concluded that at a constant SiH_4 pressure by adding H_2 into the system and thus increasing p_{tot}, heat transfer through convection is increased. This principally does not affect the number of SiH_4 molecules available at the surface of the catalyst. Under these assumptions, an hypothesis is formulated, stating that convection transferred heat to the Au-Si droplet maintains the NW growth. In this case growth will continue even if the NWs are so long, that heat transfer through the NWs length is negligible. By increasing p_{H_2}, over a limit, i.e. 75 Torr in this case, pyrolytic cracking of the molecule will take place near the substrate giving the observed deposition of a Si layer. Thus, in order to test the above stated hypothesis

the growth duration was increased to 1800 s by applying the same parameters used in the experiment of Fig. 2.11 c), d). Nanowires as long as 0.25 mm could be grown, supporting this hypothesis as observed in Fig. 2.12. If most heat transfer would occur alon the NW's length, at a certain length the heat would not be sufficient to keep the Au-Si cluster in the liquid phase. The NW length would therefore saturate in dependence of t_{grw}.

Effect of Temperature

The effect of temperature is not presented here in detail in order to not exceed the scope of this thesis. However, it should be said that the optimal temperature ranges between 400°C and 450°C. At $T_{grw} > 500$°C increasing planar Si deposition takes place even when p_{tot} is as low as 10 Torr. At $T_{grw} < 400$°C the nucleation efficiency is low. Individual NW nucleation can be observed at temperatures as low as 350°C. A more comprehensive temperature dependence will be shown for the growth on Si substrates in Sect. 2.5, because growth can be observed at temperatures substantially lower than the Au-Si eutectic temperature.

2.4.3 Concluding Remarks: Optimal Parameters

The performed series of experiments lead to the finding of optimal growth conditions on SiO_2 substrates. First, the uniform coalescence of Au layers was enhanced by a three-step pre-growth treatment. After the Au deposition by sputtering the SiO_2 substrate is slightly etched in BHF. This partially uncovers the buried Au atoms in the oxide and additionally tears up the deposited Au film. Annealing follows in H_2 at 450°C for 300 s. Subsequently an Ar plasma is ignited on the substrate, which significantly enhances homogeneous coalescence. Growth experiments were used to confirm the optimized effects of the pre-treatment. The optimal conditions for the SiNW growth on SiO_2 are: SiH_4 with $p_{SiH_4}= 5$ Torr diluted in H_2 with $p_{H_2}= 45$ Torr at a temperature of 450°C. At these conditions the NW morphology exhibits the best results. A growth duration of 180 s gives SiNWs with a typical length of 20 µm.

2.5 Growth on Crystalline Substrates

The growth on crystalline silicon (c-Si) substrates was carried out on (001) oriented surfaces. The task was to obtain a uniform diameter distribution of the NWs with mean diameters below 20 nm. Moreover, a unique crystalline

orientation of the NWs was aimed at. The idea was to grow the NWs epitaxially, so that the substrate surface orientation could be transferred onto the NWs. In this section the effect of the catalyst pre-treatment is shortly discussed. From there on, the established NW growth process on SiO_2 was transferred for the growth on Si. In this case a temperature dependent study on the NW growth is presented here, because NW nucleation was observed already at much lower temperatures.

Substrate preparation For epitaxial growth to take place, the substrates surface is required to be oxide free prior to the Au deposition. The difficulty is to maintain this surface un-oxidized till the NW-nucleation is successful. For the experiments 6" diameter (001) oriented Si wafers with production quality were used. The substrates were cleaned in the *Infineon, Perlach* fabrication line, thus no extra organic or inorganic residual clean had to be carried out, like an *RCA* clean. Only the native oxide was removed by a dip in 5% hydrofluoric acid (HF). Although the native oxide was etched away almost immediately, the substrate was kept in HF for 60 s to ensure that the free hydrogen atoms could bind to practically all Si dangling bonds. This hydrogen passivation gave an effective protection from oxidation for up to 600 s, as measured by the change from an hydrophobic to a hydrophillic surface. Immediately after the HF-etch, the samples were brought into vacuum ($p = 10^{-6}$ Torr), and sputtered with Au of different d_{Au}. Due to the relatively good vacuum, the duration of the latter step was not crucial to prevent the oxide formation. However, after the Au deposition oxidation is enhanced, because Au acts as a catalyst for an enhanced Si oxidation [KTRR06]. Thus, the samples had to be immediately transferred to the load lock of the CVD tool, and quickly brought into the NW-growth chamber. If this was faster than 7 minutes in total from the oxide dip to the loading in the CVD chamber no oxide formation was observed, as proven by the hydrophobicity of the surface.

Effect of Ar-plasma The first experiment consisted in growing NWs with the standard growth conditions determined for the successful growth of NWs on SiO_2. The catalyst pre-treatment had to be changed significantly to adapt to the different substrate. The BHF etch after Au sputtering was omitted, because it practically does not etch Si and cannot uncover buried Au or tear up a Au film. Alternatively no Si etching agents as KOH or TMAH were used, because of the anisotropy of the etching rate in Si. Au behaves very differently on SiO_2 than on Si, not only the wetting properties are different, but Au diffuses much easier on the surface of Si than SiO_2. Due to the

enhanced diffusivity coalescence should be easier (provided that the surface energies are comparable). In the case of Si substrates an analysis of the Au coalescence as the one performed in Sect. 2.4.1 is not very meaningful for the posterior experiments. Au induced oxidation could alter the morphology significantly. The results of the growth experiments will be the best criterion to evaluate the effect of coalescence. Nevertheless, for the established process explained below a retrieved sample prior to the NW growth will be shown to show that coalescence indeed takes place.

After the Au deposition the samples were annealed for 300 s in H_2 at 450°C followed by the Ar-plasma at a holder temperature of 450°C for 300 s. This was immediately followed by growth with $p_{SiH_4} = 5$ Torr and $p_{H_2} =$ 45 Torr for 300 s at 450°C. As analyzed with SEM images, the results were practically identical to the ones performed on SiO_2 substrates, without the application of the post-PVD applied BHF etch. No preferential NW orientation was observed, showing that epitaxial NW growth was not successful. This suggests that the Si substrate is re-oxidized before nucleation occurs hindering an epitaxial growth. Most probably, the residual O_2 contained in the chamber, as confirmed by QMS measurements, is also ionized in the plasma enhancing Si oxidation. An H_2 plasma was ignited with the aim of maintaining the substrate passivation. However, the hydrogen ions heavily etched the Si surface, depositing the etched material on the Au particles and completely suppressing NW growth.

2.5.1 Immediate Growth

A new coalesce procedure was developed to achieve epitaxial growth. First, the plasma catalyst pre-treatment was avoided. Second, remaining O_2 from the load process could also be problematic when heating the substrate. The standard sample loading process imposed a problem, because the substrate was put in contact with the hot susceptor directly after introducing the wafer from the load chamber, when the O_2 content is high. Loading the substrate on a cold chuck would have the inconvenience of a long temperature ramping time due to the large thermal mass of the holder. Therefore, the substrate loading routine was altered to initially leaving the wafer suspended on the ceramic lifting-pins (see Fig. 2.4), without lowering it onto the hot chuck. After closing the load lock, the remaining gas in the chamber was purged with 1000 sccm of H_2 for 300 s. The substrate was then only heated by convection and radiation from the substrate but not through conduction. Subsequently, the silane was adjusted to $p_{SiH_4} = 5$ Torr and H_2 to $p_{H_2} = 45$ Torr. Only then, the substrate was then lowered onto the 450°C hot substrate to initiate the NW growth. This growth period lasted for 300 s. It was ended by lifting

the wafer holder with the ceramic pins and purging the chamber with H_2.

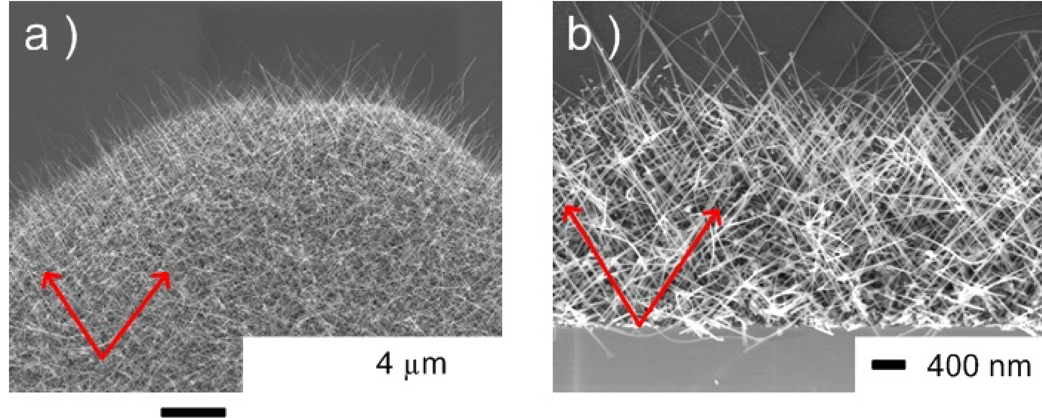


Figure 2.13: SEM tilted view of epitaxially grown SiNWs on Si substrates. Red arrows are a guide to the eye. To better distinguish the NWs orientation the boundary marked by the shadow mask is shown, i.e. between a region with Au catalyst and a catalyst free region (top).

The results of this experiment for $d_{Au} = 0.5\,\text{nm}$ are seen in Fig. 2.13. The NWs now have a clear orientation with respect to the substrate. However, due to the elasticity of the SiNWs and their high density, this orientation is difficult to observe at first sight, the preferential orientation for epitaxial nucleation of the NWs. It is important to note that the NWs seem to have a uniform diameter distribution and rather small mean diameters.

From the angles of the NWs´ longitudinal axis towards the substrates surface the crystalline growth direction of the NWs can be easily determined. This analysis is carried out with the SEM images of Fig. 2.14 a)-c). Figure 2.14 c) shows the plane-view in the $[00\bar{1}]$ direction to the substrate, where the NW projections on the (001) surface are oriented at an angle of 90°, 180° and 270° to each other. An SEM cross-sectional view in the substrate's $[\bar{1}\bar{1}0]$ direction is depicted in Fig. 2.14 a), where the NW projections exhibit an angle of 63° to the substrate surface. Finally, a view in the $[\bar{1}00]$ direction shows that some of the the NWs have an angle of 45° towards the substrate, Fig. 2.14 b). The rest of the projected NWs are normal to the surface. This geometrical information is gathered in Fig. 2.14 d). There, a schematic of the [001] substrate with the corresponding viewing angles as well as the reconstructed NW orientations is shown. The NW growth direction is easily and unequivocally determined to be the <011> and equivalent crystal

directions: $<\bar{1}01>$, $<0\bar{1}1>$ and $<101>$. This fact will be confirmed with HR-TEM images in Sect. 2.7.

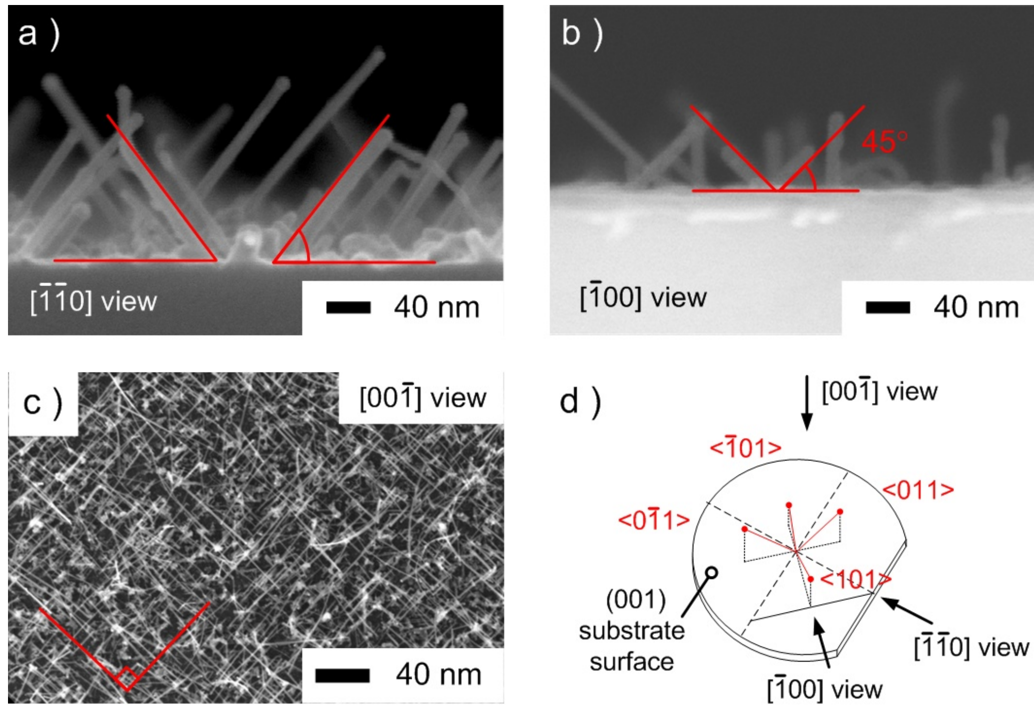


Figure 2.14: Crystalline growth orientation of epitaxial SiNWs. Crystalline direction is $<011>$ and equivalent directions.

For the procedure resulting in epitaxial growth, the Au coalescence occurs in SiH_4 flow at the instant when the wafer is lowered onto the hot holder and is heated abruptly. It is therefore difficult to determine how long the actual coalescence step takes, and when NW nucleation starts. To study how this first step affects the substrate surface, a Si substrate with $d_{Au} = 0.5\,\mathrm{nm}$ is processed with the same parameters as for the last experiment, but with only a short duration on the chuck of 3 s. Figure 2.15 shows an SEM image of the coalesced layer. Although the coalescence is not as uniform as the coalescence on SiO_2 with the developed processes in Sect. 2.4.1, all Au clusters are smaller than 10 nm in diameter. As noted previously, the actual morphology of the substrate at the moment of nucleation does not necessarily need to resemble this image. Coalescence can be altered by cooling the substrate when retrieving the sample and by the Au enhanced Si oxidation.

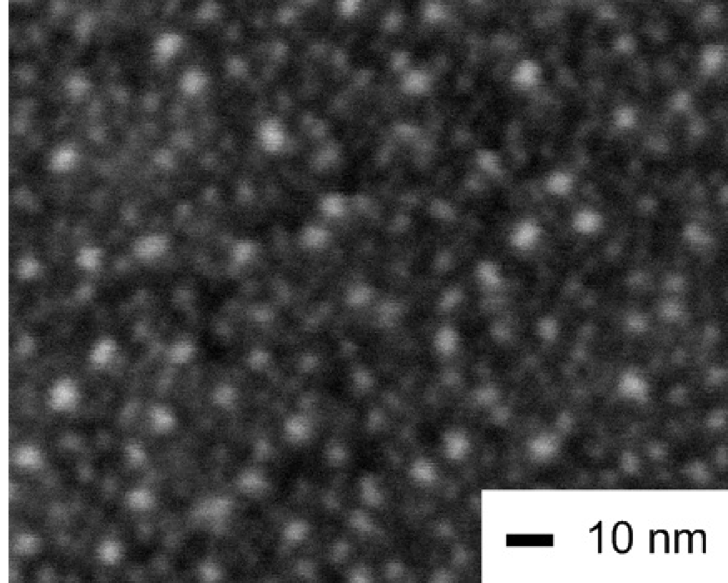


Figure 2.15: SEM plane view of coalesced Au after heating for 3at 450°C. All Au clusters are smaller than 10 nm.

2.5.2 Minimal growth temperature

Next, the minimal temperature required to grow NWs on Si is determined. This can be regarded as a temperature dependent growth study. This study is limited to the temperatures around the Au-Si eutectic temperature of 363°C and below. For temperatures higher than 400°C no unexpected results are observed, i.e. planar Si deposition above 500°C. In contrast to the growth on SiO_2, the NW growth on Si was observed at much lower temperatures than the Au-Si eutectic temperature making this study more interesting.

For the T_{grw} dependent experiments, the standard growth conditions were used ($d_{Au} = 0.5$nm, $p_{SiH_4} = 5$ Torr, $p_{H_2} = 45$ Torr, and $t_{grw} = 300$ s), while T_{grw} was varied step-wise from experiment to experiment. Figure 2.16 summarizes the results by depicting representative SEM images for each T_{grw}. In this case T_{grw} is taken as the highest registered growth temperature during growth. Figures 2.16 a) -e) show plane-view images of the substrates giving a large area overview and an impression of the NW density. Whereas Figs. 2.16 f) -i) depict SEM tilted-views at a higher magnification, giving a detailed view of the nucleated NWs. Starting the temperature series at $T_{grw} = 293$°C, no NWs are formed as seen in Fig. 2.16 a). A close look in

Fig. 2.16 f) denoted by the red arrow reveals that Si is being deposited as an extension of the brighter Au particle. Nevertheless, it is not possible to determine if this structure is a free standing Si monolith (i.e. successfully nucleated NW) or a creeping-like surface deposition of Si, such as amorphous ar poly-crystalline Si. The information of having deposited Si extending from a Au particle, regardless of its crystallinity, reveals that at 293°C SiH_4 can be cracked catalytically on a Au surface. Even more importantly, it shows that Si can diffuse through the Au particle or alternatively along its surface to be finally deposited on the substrate.

Figure 2.16: Temperature dependent growth of SiNWs on (001)Si. The highest T_{grw} recorded during growth is listed.

Minimally rising T_{grw} to 299°C results in a few single free-standing SiNWs, see Figs. 2.16 b), g). However, the large majority of deposited Si has the form of a creeping deposited Si. A further rise in T_{grw} to 319°C, as seen in Figs. 2.16 c), h) increases the NW density. Moreover Au particles without

nucleation can not be observed any more. The NW density and length are enhanced for higher temperatures. In particular, surpassing the Au-Si eutectic temperature (353°C) makes a large difference in NW-growth: no creeping Si deposition is found meaning that practically all Au particles nucleate crystalline SiNWs, see Fig. 2.16 i).

These results imply, that the minimal temperature required to nucleate SiNWs amounts to $T_{grw} = 299°C$. According to the Au-Si phase diagram (Fig. 2.2), the Au-Si system cannot be liquid below 353°C. The substantially lower growth temperature can be attributed to two different scenarios. First, the Au-Si phase diagram could be different for the nano-scale than for the bulk, because surface forces are larger and fewer atoms are involved. In this case, VLS growth could still be valid. The alternative scenario is that a different NW-growth mechanism takes place at these temperatures. This could be explained by a VSS growth mechanism as previously explained in Sect. 2.1.1. Nevertheless it must be noted, that the Au-Si eutectic temperature does play an important role in the SiNW growth, because only above it *all* Au particles seem to nucleate free standing NWs. From a practical point of view, the temperature most suited for growing SiNWs to bring them into a high yield suspension is 390°C- 400°C.

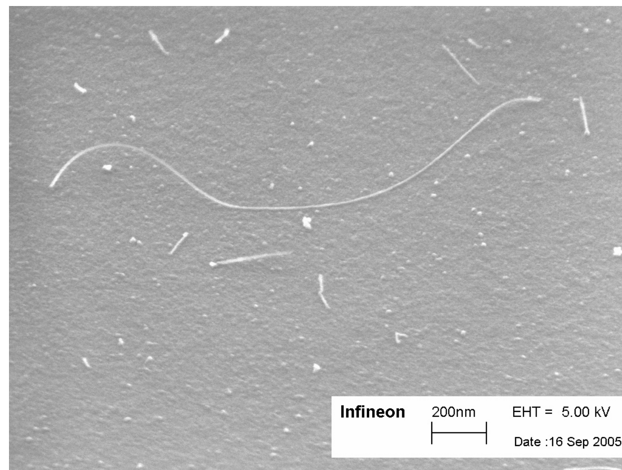


Figure 2.17: SEM plane view of direct growth on SiO_2, as performed for the standard growth on Si, i.e. without catalyst pre-treatment

As a final remark, this growth process was only successful for NWs grown on Si. A SiO_2 substrate with $d_{Au} = 0.5$ nm with the BHF dip applied after the

Au sputtering for 30 s was processed under the same conditions and is shown in Fig. 2.17. Almost no NWs are formed, and no clear Au cluster formation can be observed. The comparison between Figs. 2.13b) and Fig. 2.17 shows the different Au coalescence dynamics, depending on the substrate used.

2.6 Position Controlled Vertical Growth of SiNWs

The previous experiments were constricted to the investigation of the process parameters with the aim to obtain NWs with high structural quality and homogeneity. These NWs were exclusively grown for fabricating NW suspensions for their subsequent implementation as building blocks for horizontal devices. However, one of the main expectations of implementing NWs in electronics is the ability to enable monolithic vertical integration.

State-of-the-art Large efforts have been made by several research groups on vertical NW growth. The most impressive developments have been achieved in the position controlled vertical growth of group III-V NWs on (111) oriented group IV substrates [BvDDF+04]. In the case of SiNWs vertical growth has been reported already since the 1960's [WE64, SSG05, HFHP05]. Group III-V NW based devices such as diodes, light emitting diodes and FETs have been implemented vertically [BWFS06, SMT+08]. In the case of SiNWs, FETs[GHFY06] and impact-ionization transistors [BHS+07] have been shown. Nevertheless, all these SiNWs were grown on Si-(111) surfaces, giving <111> oriented SiNWs. However, as noted in [WCL+04] and [SSG05] the <111> oriented SiNWs can only grow with diameters greater than 40 nm, limiting the minimal pitch for integration to 80 nm. Another disadvantage of integrating these devices on a Si substrate, is that the bottom contact to the NWs is common on the entire substrate. A way out would be structuring the top Si layer of (111) oriented SOI wafers. Unfortunately, there are no Si(111) oriented SOI wafers suitable for production processing up to date.

Vertical concept used here The aim of the following work was twofold. First, the NWs should grow vertically aligned out of pre-patterned holes. Second, the NWs should nucleate on amorphous metallic materials commonly used in the semiconductor industry. The first aim provides position control of the NW as well as the vertical alignment. The second aim is necessary to give an individual bottom electrical contact to the NW, because the amorphous metal can be deposited and patterned easily. The proposed growth out of

holes is a template like growth. In contrast to the growth in porous alumina templates, as described in Sect. 1.2.1, d_{NW} should be smaller than the holes diameter. This way, the NW can be guided during growth without acquiring the negative imprint of the template and therefore its surface roughness.

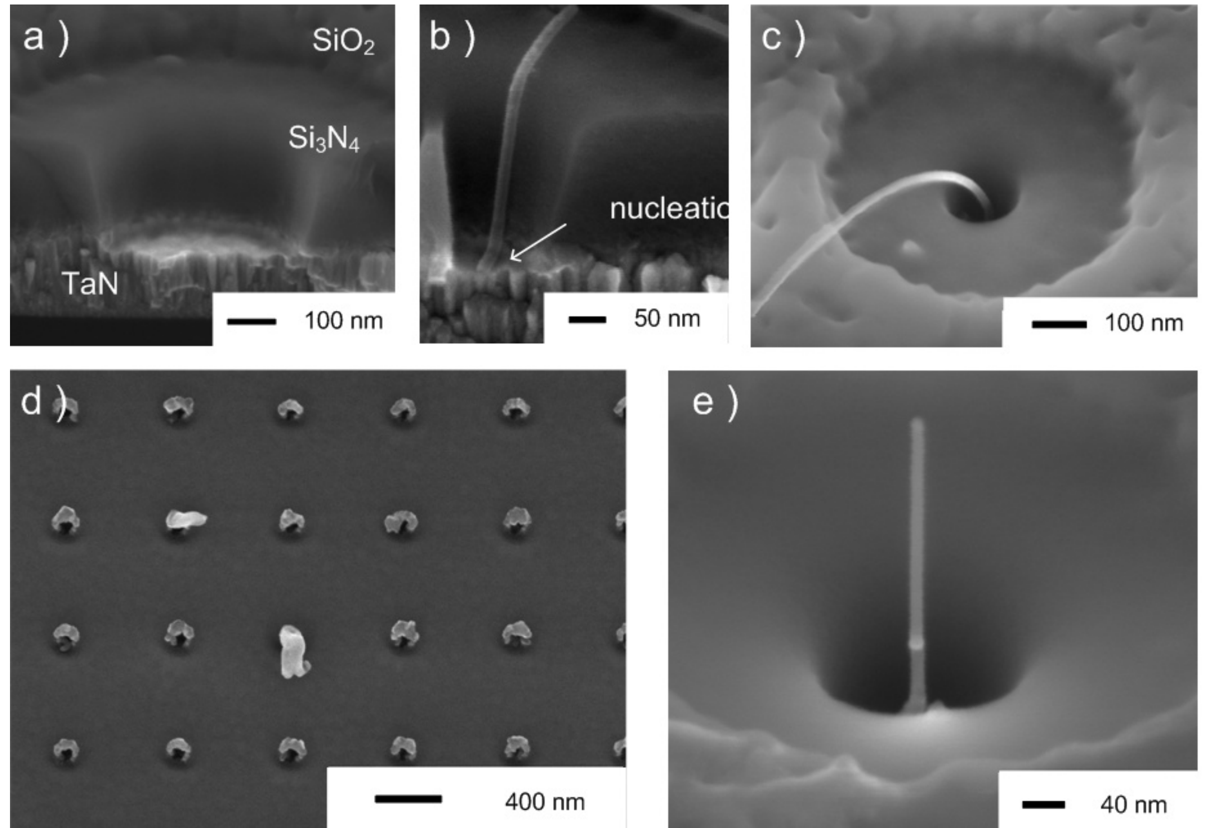


Figure 2.18: SEM images of single, position controlled and vertically aligned SiNWs. a) Cross section SEM view of an etched hole in SiO_2 with Si_3N_4 spacers and a buried TaN layer as a contact. SiNWs are grown inside these holes b) where the NW actually nucleates on the amorphous-TaN layer and the NW is forced to grow out of the hole. c), e) Single 10 nm thick NWs are grown out of 100 nm-diameter holes. d) Array of vertically aligned amorphous Si-tubes growing out of the template.

Substrate Processing and Growth The metal of choice was TaN, because it offers various processing advantages: it is highly conductive, can be

deposited easily and at low temperatures by atomic-layer deposition (ALD) and can be etched selectively to Si and SiO_2. Very importantly, it is stable and does not react or create alloys with Au or Si at the NW growth temperatures used. Also relevant for possible interconnect applications is that it acts as a diffusion barrier for many metals such as Cu and Ni. The holes were structured by optical lithography and Si_3N_4 spacer etching on a 350 nm thick SiO_2 layer. This way holes of various diameters and as small as 40 nm were obtained. A cross section of one of this holes can be seen in Fig. 2.18 a). Au is deposited with PVD with different d_{Au} normally to the substrates surface. Subsequently, the Au deposited on the surface is removed by kinetic ion- etching (sputtering) so that only NWs grow inside the hole and not at the surface. Finally, the standard catalyst pre-treatment for amorphous substrates was applied, followed by a growth at $T_{grw} = 450°C$ for $t_{grw} = 150\,s$ with $p_{SiH_4} = 5\,Torr$ and $p_{H_2} = 45\,Torr$.

The main results can be seen in Figs. 2.18 b)-e). The amount of deposited Au has important consequences for the vertical growth of SiNWs. The exact amount needed depends on the diameter of the hole. Sufficient Au is needed to coalesce into a single Au particle during annealing. In the case that this Au particle is smaller than the diameter of the hole, the NW can nucleate on the TaN layer and be guided to the outside of the hole as seen in Fig. 2.18 b). The nucleation on TaN appears to be very clean and direct and should render a good electric contact. The SiNWs in Figs. 2.18 b), c) and e) have diameters between 10-15 nm as well as a smooth surface. This smoothness is qualitatively much better than the one observed for template grown SiNWs or top-down vertically aligned SiNWs. When an excess of Au is deposited inside the holes, so that the coalesced Au particle occupies the complete bottom of the hole, no free standing NWs with smooth surfaces are grown out of the holes. Instead, cylindrical or tube-like Si structures are grown as seen in Fig. 2.18 d). Their crystallinity has not been studied yet, but they seem to be amorphous or poly-crystalline, as judged by the surface inhomogeneity. Another interesting aspect is, that the catalyst particle is not found at the tip of the Si-tubes. The probable reason, why these structures are irregular and cylindrical is that the Au-Si droplet cannot move as freely as when its size is smaller than the hole diameter. In the case of excess Au, Si-nucleation seems to be more favorable at the SiO_2 hole walls than on the TaN. The deposited Si is then pushed-up, forming the Si-tubes.

Small Au particles would practically only have contact to the TaN when nucleating, because the TaN is recessed at the hole's site, see Fig. 2.18 a) and b). Once the NW is successfully nucleated, it will grow in a random direction and very probably will get in contact with the SiO_2 wall. Since no sharp NW kinks are observed, it appears that the tip of the NW smoothly

slides out of the hole as it is continued to be pushed by the NW growth. This hypothesis can be questioned, since clear kinks have been reported when growing horizontal SiNWs across trenches [ISKW04]. When these NWs reach the opposite Si wall, the catalyst also nucleates there creating a kink in the NW. In contrast to those experiments the hole wall used here is Si_3N_4. It is assumed that it is energetically more favorable for the Au-Si melt to precipitate the Si on the Si than on Si_3N_4.

To provide further evidence of this SiNW behavior of growth inside holes, Si NWs were grown out of 10 µm deep and 120 nm wide dynamic random access memory (DRAM)-trenches. At these high aspect ratios it is practically impossible to deposit Au at the bottom of the trenches by PVD. Instead, the Au colloids described in Sect. 2.3.1 were dispersed on the substrate. The Au colloids statistically fell in the trenches. As seen in an SEM image of a cleaved trench in Fig. 2.19 b), a SiNW can be guided to grow vertically over a distance of 6.5 µm without kinks.

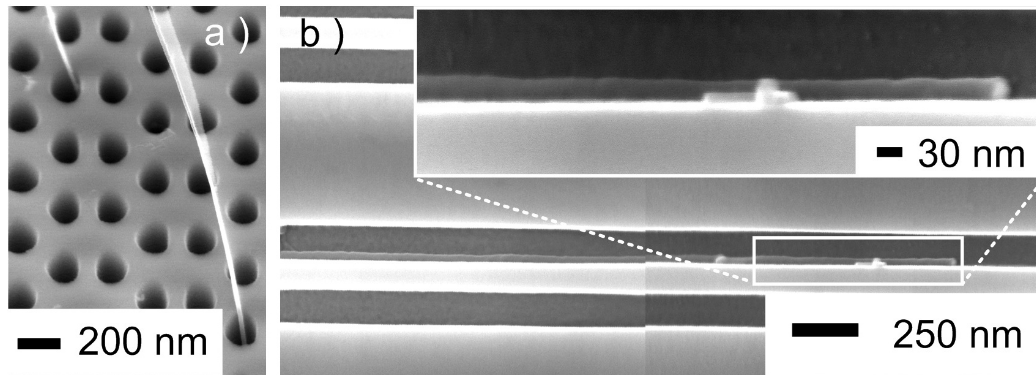


Figure 2.19: SEM images of SiNWs grown inside of DRAM trenches. a) Tilted SEM view showing SiNWs growing out of DRAM trenches. b) Cross section of a DRAM trench rotated for convenience, the NW is growing toward the outside of the trench. SiNWs are able to be guided vertically inside high aspect-ratio trenches for up to 6.5 µm in length, without kinking.

In this section, the growth of vertically aligned SiNWs nucleated on amorphous metals is shown for the first time. This method could in principle enable the implementation of VLS SiNWs in the . The ability to nucleate SiNWs on TaN could in principle simplify the use of Au in the back-end of CMOS processing lines, because TaN acts as a diffusion barrier for Au. This

process also enables complex circuitry with overstacking device layers. Unfortunately, further growth experiments were not possible during this work due to the sudden closure of the central research division of Infineon Technologies AG on November 2005. The P5000 CVD-equipment was dismantled to provide spare parts useful for the production lines.

2.7 TEM Characterization of Si-Nanowires

An important analysis performed on the SiNWs was transmission electron microscopy (TEM). With help of the high resolution (HR) TEM images, information could be obtained about the crystalline quality of the NW surface roughness, thickness of the amorphous native Si-oxide shell as well as the interface between the catalyst particle and the SiNW. To get an atomic resolution the NWs had to be oriented along their length axis so that the crystal-planes ware parallel to the incident electron beam. Both NWs grown on SiO_2 and Si were investigated.

2.7.1 SiNWs Grown on SiO_2 Substrates

Figure 2.20 shows a TEM micrograph taken at 200 kV of a SiNW nucleated on SiO_2. The nominal Au layer thickness used was 1 nm, and the following growth parameters were used: $p_{SiH_4} = 5\,\text{Torr}$, $p_{H_2} = 45\,\text{Torr}$, $t_{grw} = 300\,\text{s}$ and $T_{grw} = 450°\text{C}$. The micrograph depicts the tip of the NW showing the interface between the Au-Si particle and the SiNW. The NW has a diameter of 36 nm, the amorphous shell has a thickness of approximately 1.5 nm and is most likely composed of native silicon oxide. The inset of Fig. 2.20 shows a magnified view of the crystal lattice the NW's lower side. The crystal orientation of the NW axis is the $<11\bar{2}>$ or an equivalent orientation: $\{112\}$. Moreover, the atomic resolution of the micrograph shows, that the SiNW exhibits crystal twining. This means that the crystal lattice is mirrored along one line, called the twin boundary. In this case, the twin boundaries are parallel to the growth direction and are repeated every few atomic layers. This effect is known as *micro-twining.* One interesting aspect to consider is the Si to catalyst particle interface.

The amorphous mushroom shaped particle is indeed composed of Au and Si as confirmed by EDX-measurements. The particles interfaces to the SiNW at least at the outer NW radius are group $\{111\}$ oriented surfaces, which meet in the middle of the NW. This suggests, that $\{111\}$ mono-layers are grown preferentially, instead of closed $\{112\}$ layers. This probably leads to the observed twining. Indeed, the $\{111\}$ surfaces exhibit the lowest sur-

face energies of all Si planes [Smi95], because the Si atoms within the {111} plane have the lowest number of dangling bonds. Therefore, the energy required to construct the surface would be minimized. Interestingly, in recent publications Au has been found at the twin boundaries of <112> oriented NWs [HAP+08, AHP+08]. The bright and amorphus insertions surrounding the outer part of the NW at the catalyst to NW intersection are most probably composed of silicon oxide. Their formation can be attributed to the Au-catalyzed oxidation of Si, because it is only formed at the interface between Si and Au, where O_2 is present when the samples are retrieved form the furnace. Atomic resolution was only obtained for this NW grown on SiO_2. However, the TEM images of the other NWs confirm that the <111> planes are oriented parallel to the axis of growth, which is in accordance with the <$11\overline{2}$> axis direction but leaves other possible NW-orientations open.

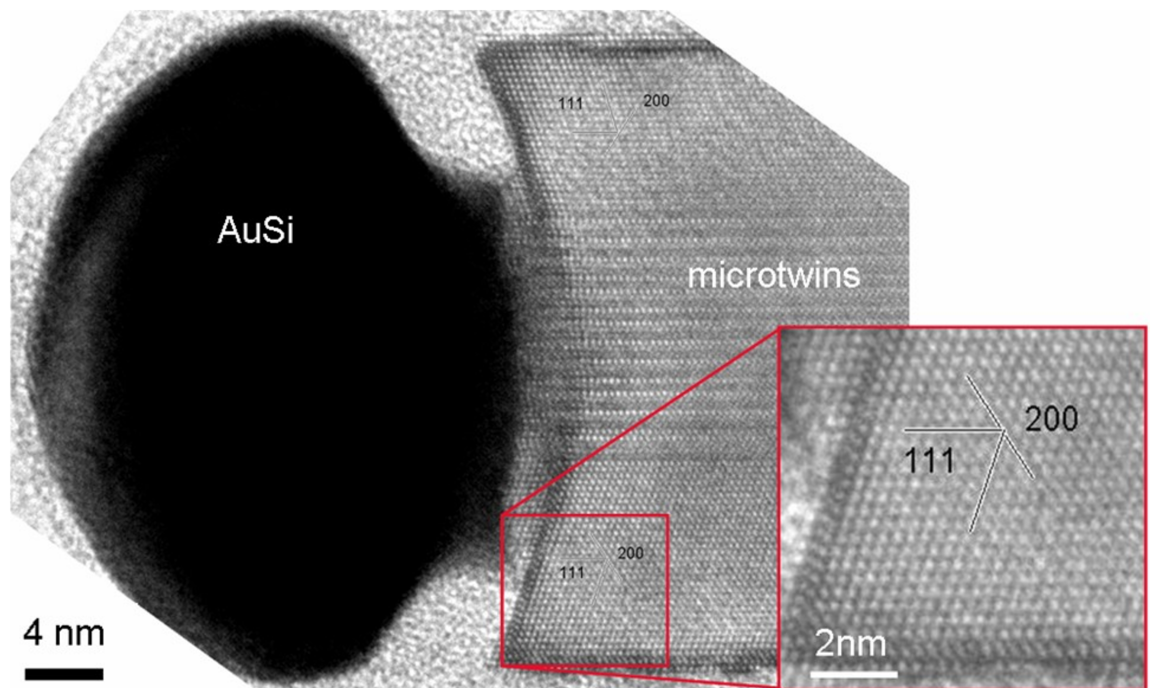


Figure 2.20: High resolution TEM micrograph of a SiNW nucleated on SiO_2. The growth orientation is the <$11\overline{2}$> as noted by the magnification in the inset. Along the growth axis, micro-twins are observed. The amorphous mushroom-like structure composes the Au-Si catalyst particle.

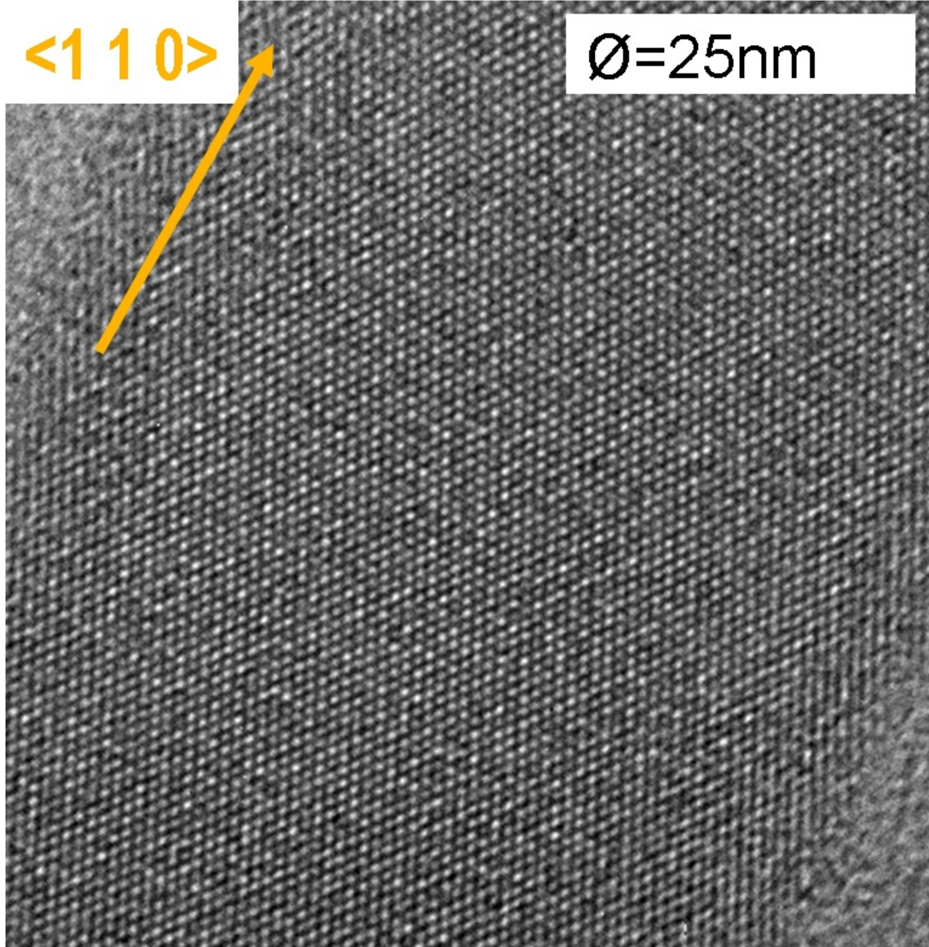


Figure 2.21: High resolution TEM micrograph of a SiNW nucleated on (001)-Si. The NW is single crystalline and the growth orientation is <110>.

2.7.2 SiNWs grown on (001) Si

The NWs grown on Si were analyzed as well, Fig. 2.21 shows the HR-TEM micrograph of a NW nucleated on Si under the following conditions: $p_{SiH_4} = 5\,\text{Torr}$, $p_{H_2} = 45\,\text{Torr}$, $t_{grw} = 300\,\text{s}$ and $T_{grw} = 400$°C. Differently from Fig. 2.20, the 25 nm thick NW is single crystalline along over its entire thickness. The amorphus coating is 1.5 nm thick. The NWs growth orientation is the <110> or equivalent. This confirms the results determined from SEM images presented in Fig. 2.14. Previous studies by Y. Wu, C. M. Lieber et

al. [WCL+04] showed that <110> oriented NWs have and hexagonal cross section where four of its facets are {111} and two {001} oriented. For thin NWs <110> is the most favorable NW orientation because the total energy seems to be minimized by the large area contribution of the {111} facets [LLM+03].

Both TEM images also show, that the surface roughness is on the order of single Si layers. Most of the surface roughness is given by the amorphous coating which is easily etched away selectively to the Si with HF.

2.7.3 Conclusions on the SiNW Growth

Throughout this chapter the results concerning the SiNW growth have been summarized. First the basic theory of the VLS growth mechanisms has been discussed. A CVD chamber was modified to enable the growth of SiNWs with undiluted SiH_4 as the Si precursor. SiNWs were successfully grown on amorphous SiO_2 substrates and on (001) Si with the aim of posteriorly harvesting them for their implementation in electrical devices. For each processes an optimal Au coalescence procedure was established rendering a uniform distribution of the size of Au particles. Important dependencies on key growth parameters such as p_{SiH_4}, p_{tot} and T_{grw} were analyzed. The studies lead to optimized growth recipes for each substrate used exhibiting the same growth directions and controllable diameters. These were used as the standard growth procedures for the posterior physical and electrical experiments. The vertical growth of SiNWs vertically on amorphous metals was shown for the first time. This process could enable multilevel vertical NW integration as well as the electrical isolation between NW devices.

Chapter 3

Silicon Nanowire Integration and Device Fabrication

For the pursued investigations of solid-state reactions as well as for the formation of electrical devices built from SiNWs several fabrication schemes are required. These basically encompass three different processes: the fabrication of a test platform or template to host the NWs, the transfer of SiNWs to these templates and the contact formation. Throughout this chapter these procedures and methods will be presented. The simplest and very often the most effective geometry to integrate and test NWs is to implement them horizontally and in a random orientation. First, Sect. 3.1 will explain the methods used to transfer the as-grown SiNWs onto other substrates via the formation of SiNW suspensions. Thereafter, Sect. 3.2 will describe the fabrication of the test-substrates. Finally the contacting method with electroless Ni which provides an improved electrical contact and the necessary reservoir for the posterior Ni diffusion will be presented in Sect. 3.3.

3.1 Nanowire Suspension and Dispersion Methods

The as grown NWs need to be released from the substrate where growth took place and transferred onto another substrate for further processing. The NW transfer is enabled by the creation of a NW suspension in a liquid and posterior dispersion of this solution on the template substrates.

3.1.1 Nanowire Suspensions

The NWs are difficult to detach from the growth substrates. Mechanical agitation is used in the form of an ultrasonic bath to deliberately break and thus to detach the SiNWs. The substrates with as-grown NWs are submerged into the liquid used to suspend or host the released NWs. This liquid has to provide certain properties which will become important when dispersing the NWs. On the one hand Nanowire clustering and sedimentation in the solution should be minimal. On the other hand the solution should be able to be completely removed when depositing the NWs on a substrate without leaving other traces than the NWs themselves. This includes the minimization of condensed water on the substrate coming from from the ambient.

Choice of host solutions The first criteria implies the use of a solution which is strongly polar, because the SiNWs surface is oxidized and therefore is polar [WMF96]. This avoids NW clustering and therefore sedimentation. The next important requirement for the solution is to have a low vapor pressure, this reduces the substrate cooling while depositing the solution minimizing the condensation of moisture from the ambient. The best trade-off found was iso-propyl-alcohol (IPA) as well as ethanol. For yet an unknown reason n-methyl-pyrrolidone (NMP) was not successful, although it has a significantly lower vapor pressure and is more polar according to the eluotropic-series than IPA or ethanol. To suppress contamination, surfactants such as tensides were avoided.

Sonication When performing the ultrasonic agitation care was taken to do this smoothly. High agitation power or duration lead to the crumbling of the SiNWs into small pieces of useless length. Typically two substrates of as grown SiNWs with an area of approximately $4\,\mathrm{cm}^2$ where submerged into 5 mL of IPA or ethanol. Ultra-sonication only lasted 15 s. Immediately after starting sonication the suspension got a distinctive color. In the case of SiNWs grown on SiO_2 it became yellowish and for SiNWs grown on Si the color was grayish. Inspecting the growth substrates after sonication reveals that a large amount of NWs are still on the substrate without exhibiting obvious damage. In fact qualitatively they hardly differentiate themselves from the untreated samples. However, re-sonicating the samples only breaks a small amount of extra NWs. As proven by SEM images of deposited NWs, the suspended NWs are broken at different lengths and seldom at its bottom or nucleation site. Typically their lengths amount from several micrometers up to 10 µm.

3.1.2 Nanowire Dispersion

Common dispersion methods Two main requirements are given for the successful dispersion of the NW suspension. First, the method has to provide a homogeneous distribution of deposited NWs. Second, a fast liquid evaporation is needed to reduce the amount of particles from the ambient that easily adhere on liquids. Tests were performed on SiO_2 substrates since this is the targeted surface of the templates. The most usual method to deposit NW or nanotube suspensions is to deposit a droplet of the suspension on the substrate and to let it dry in air or to heat up the substrate to reduce the condensation of moisture. The application of the droplet method resulted in a strong inhomogeneity of the NW density on the substrate. In the area where the droplets edges were located, large amounts of bundled NWs were found resembling a SiNW film. In contrast, within the area of the droplets footprint a very small amount of NWs were found.

Spraying To circumvent these problem an alternative method was used here. Small droplets are sprayed on the substrate with the use of N_2 as a carrier gas by using a spray pistol. A significant amount of IPA or ethanol is evaporated while the droplets are suspended in the air. The small deposited droplets evaporate relatively fast due to their high surface to volume ratio. This method strongly reduces the bundling of the NWs and gives a homogeneous distribution of randomly oriented NWs on the substrate, as proven by SEM images. The already deposited SiNWs proved to have a good adherence to the SiO_2 substrate even after rinsing the substrates with polar solutions as H_2O, HF or IPA. Most probably, not only because of electrostatic forces between both polar surfaces but also because of van-der-Waals forces.

3.2 Fabrication of Test Structures

Requirements Having described the method to transfer the NWs onto a remote substrate, the fabrication of the template where the NWs are deposited is explained here. The aim was to provide a template useful for the silicidation experiments of NWs as well as to deliver the necessary components for fabricating planar SiNW FETs. This encompasses the definition of electrode regions which have two main functions. They provide the location for the posterior placement of the source and drain leads of the transistors and the contact pads for the placement of the probes. Simultaneously, they define the placement of the material reservoirs for required for silicidation. The template also needs to provide a common bottom gate stack to steer the

planar devices.

Back gate stack fabrication First the back gate stack was fabricated. Six inch diameter n-doped (001)-Si wafers with production quality were used. The surface was implanted with Phosphorous to render a degenerately n-doped Si surface working as the gate metal. Posteriorly, SiO_2 was deposited as the gate dielectric with various thicknesses d_{ox} and by different methods. For d_{ox}= 10, 20, 100 and 200 nm, SiO_2 was grow by wet thermal oxidation. Thicker oxides, i.e. 300 nm, were deposited by a SiH_4 plasma CVD deposition.

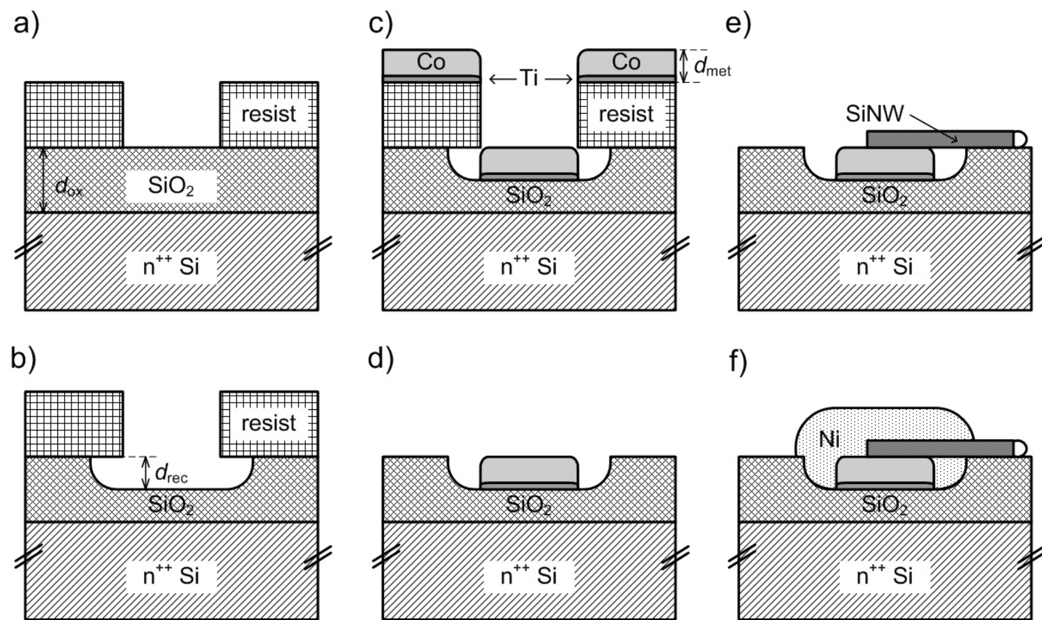


Figure 3.1: Schematic cross-sectional views of the test chip through different fabrication steps. Dimensions are not in relation. a) n-Si substrate after phosphorous implantation, SiO_2 growth with thickness d_{ox}, optical lithography and resist development. b) Recess of unmasked SiO_2 by a depth d_{rec}. c) Evaporation of metal stack: Ti and Co with a total thickness d_{met}. d) Lift-off process finishes the pre-patterning of the test-chips. e) Dispersion of SiNWs on test-chip and f) selective electroless Ni deposition on Co. Note that the dimensions and relations do not correspond to the actual values.

3.2.1 Patterning of Electrodes

The next step consisted in lithographically defining an array of electrodes which should statistically make contact to the subsequently randomly dispersed NWs. The metal electrodes were structured with the *lift-off* technique due to its technological simplicity by avoiding at least one anisotropic etch step of the metal stack.

Optical Lithography The only available optical lithography was inside the *Infineon-Perlach* production line, where substrates containing NWs were obviously not allowed due to contamination hazards. Therefore, the lithographical step and metal electrode formation was performed prior to the NW deposition. More specifically, a 0.8 µm thick positive photo-resist was exposed and developed. As a consequence, unmasked regions remained at the exposed areas as depicted schematically in the cross-section schematic of the substrate in Fig. 3.1 a).

Recess etching The unmasked regions were first used to recess the SiO_2 layer locally prior to the metal deposition. BHF with a concentration of 100:1 was used for the isotropic SiO_2 etch as seen in Fig. 3.1 b). Differently form HF, BHF does not damage the resist even after long etching durations. Depending on the SiO_2 layer thickness different recess-depths (d_{rec}) were performed. In the case of d_{ox}=300 nm, d_{rec}=70 nm, for d_{ox}=20 nm only d_{rec} =4 nm were removed to avoid oxide breakdown at high electric fields when testing the NW devices. There are three main reasons for the recess. First, the under-etch below the resist enables a more effective lift-off, because the resist-solvent is able to penetrate easier at the lower part of the resist. Second, in the case of evaporating a metal stack with a thickness equal to the recess depth the top of the metal will align to the substrates level. For thicker metal stacks than the recess depth, the surface topography is reduced accordingly. The NWs to be deposited will then lie flatter on the substrate, which is relevant for the device performance as will be seen in Sect. 5.3. Third, the undesired fence formation at the structures edges can be significantly reduced or even suppressed.[1]

Metal evaporation The metal stack of choice was then deposited by a standing electron beam evaporation, see Fig. 3.1 c). In the case of metals that do not oxidize immediately, like Ni or Co, [Wea69] an intermediate layer

[1]Fence formation occurs when the angle of the material beam towards the substrates surface deviates from 90°.

of a metal which easily oxidizes, like Ti, Al or Ta, is indispensable to provide adhesion to the SiO_2. For a substrate with d_{ox}=300 nm with a SiO_2 recess of d_{rec} =70 nm, 15 nm of Ti are deposited as the adhesion layer and subsequently 55 nm of the contact metal, mostly Co, are deposited on top. After the metal deposition, lift-off is carried out by dipping the substrate in acetone with a short (30 s) ultra-sonic agitation. The total metal stack height (d_{met}) adds up to 70 nm, aligning its top to the un-etched SiO_2 surface, as seen in Fig. 3.1 d).

3.3 Contact Improvement by Electroless Plating

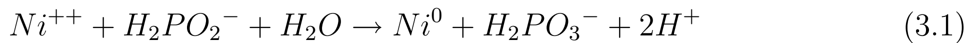
Contact before plating At this stage the test template is ready for the NW-deposition as explained previously in Sect. 3.1. As noted above, the deposited NWs show a random distribution and orientation. Statistically, some NWs make contact to a single or two adjacent metal pads as shown schematically in Fig. 3.2 e). Principally, a metallurgic junction between this metal pad and the SiNW can be made if the native oxide of the SiNW is removed and annealing follows. Nevertheless, the contact area between the roughly cylindric NW and the flat metal pad is very small and limits the metal diffusion into the NW as well as the contact conductance when forming a device. To overcome this problem a novel contact improvement scheme is used without the need of an extra lithographical step. An extra metal layer is deposited by plating, exclusively on the pre-patterned metal pads. The used electroless deposition method has several advantages over alternative bottom-up approaches commonly used to contact NWs.

Electroless plating Electroless plating is a wet-chemical method which describes the selective deposition of a metal on catalytically active surfaces. The process is driven by the thermal energy of the system. Historically it is called an electroless plating, because in contrast to the previously developed electroplating no external electrical potential is required. Different metals such as Au, Co, Pd, Ag, and Ni were deposited in this work by electroless plating to provide contacts to the NWs. The focus of this thesis is on the deposition of Ni, since the most important results of this thesis were achieved by using this contact material.

Catalytic activation To deposit Ni selectively on the contacts formed previously by Lift-Off the contacts surface must be catalytically active. Ap-

propriate metals with strong catalytic properties are usually Au, Pd and Co. Nickel also has some catalytic properties itself, but turned out to be not as catalytically efficient as the previously mentioned metals. Cobalt was the catalyst material of choice, because it does not diffuse as fast in Si as Au and Pd.

Reaction mechanisms for electroless Ni The solution used for the Ni deposition is H_2O based and uses nickel-chloride ($NiCl_2$) as the Ni source. In order to break up this salt a reduction reaction is used. A reducing-agent: sodium-hypoposphite (NaH_2PO_2) provides the additional electrons needed for reduction. According to [Rie91, LUD$^+$03] the reaction can be written as:



$$Ni^{++} + H_2PO_2{}^- + H_2O \rightarrow Ni^0 + H_2PO_3{}^- + 2H^+ \tag{3.1}$$

The reduction is initiated on the catalytically active surface with the help of external heat. It is then maintained by the catalytic action of the newly deposited Ni. Ammonium Chloride (NH_4Cl) is added for subsequent pH adjustment, giving the ammoni-alkaline nature of the deposition solution. Sodium tricitrate hydrate is further used as a buffer solution for long term pH control.

3.3.1 Practical Implementation

Next, the embodiment of this electroless-bath is briefly explained. Prior to the Ni deposition it is necessary to remove the native silicon oxide surrounding the SiNWs. Silicon oxide isolates the NW electrically and acts as a diffusion barrier for Ni. The SiO_x is etched with BHF (100:1) for 30 s and rinsed with de-ionized (DI)-water. HF can not be used, because it rapidly etches the Ti adhesion layer destroying the pre-formed contacts. The proton concentration of the BHF solution is sufficient to terminate the dangling Si bonds with hydrogen atoms. Accordingly, oxidation of the Si is suppressed for a short period (approximately 7 minutes at room temperature for bulk Si). Immediately thereafter and prior to the re-oxidation of Si, the substrate is submerged into the electroless bath at a temperature of 80°C. After only 20 s, of deposition time a Ni layer of approximately 150 nm thickness is deposited.

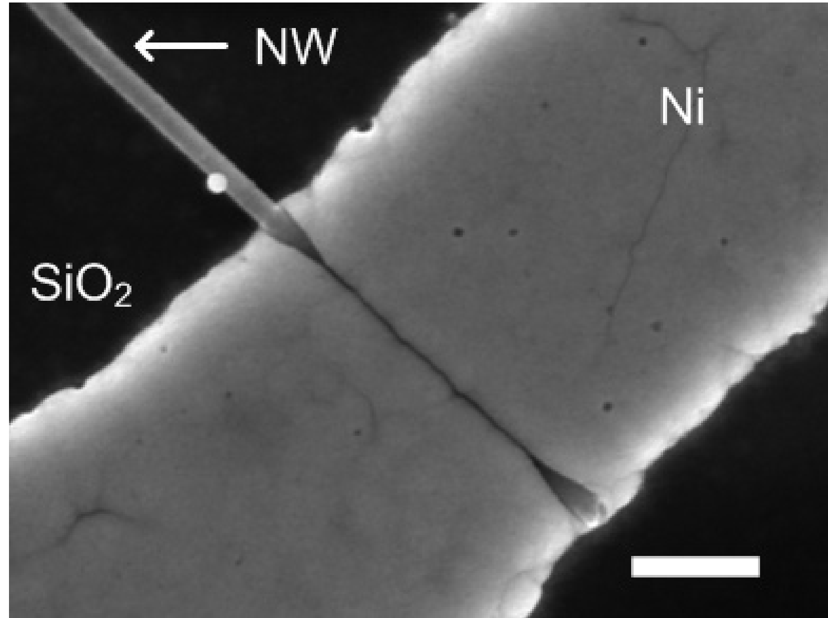


Figure 3.2: SEM plan-view of an embedded SiNW in electroless deposited Ni. Selective Ni deposition on Co with no precipitation on SiO_2 or Si. Scale bar is 200 nm.

Results Figure 3.2 depicts an SEM image of a SiNW contacted at one end with electroless deposited Ni, a corresponding schematic cross section can be seen in Fig. 3.1 f). The SEM image confirms the good process selectivity since the Co is completely covered with Ni and practically no Ni precipitation takes place on the SiO_2 or Si. It can further be observed that the SiNW is completely embedded within the deposited Ni. Thus the contact area between the metal electrode and the SiNW increases significantly in comparison to the NW which simply lies on a metallic contact (Fig. 3.1 e)), i.e. before Ni plating. Moreover, it can also be observed that the grooves created by the under-etch with BHF (see Fig. 3.1 b)) are completely filled with Ni due to the iso-tropic nature of the deposition. This implies that the NWs will be in contact with the substrates surface throughout their complete length, which is of paramount importance for the device performance, as will be seen in Sect. 5.3.

3.3.2 Evaluation of Electroless Plating Contacting NWs

This work shows the first application of electroless plating time on any kind of NWs. Due to the novelty of this technique the main advantages of applying the electroless Ni deposition in contrast to common top-down structuring should be underlined. These are summarized in the following points.

- Bottom-up approach.
- Selectivity and self-alignment.
- Low temperature process.
- Excellent step coverage.
- Large contact area.
- (High mechanical stability of the NWs.)

Approach type The process is of bottom-up nature enabling possible fabrication schemes previously not possible. In the the classical top-down approach the NWs contact is patterned after the NW deposition. In the case of Ni this is problematic due to the poor adhesion between Ni and SiO_2. The Ni contacts can even detach when applying mechanical forces for instance with measurement probes. Commonly, an adhesion layer is used but in contrast to the method used here the adhesion layer will be the actual material at the Si interface. This has two important consequences: the intended diffusion of Ni into the SiNW is hindered or influenced by the interface material and the actual material making electrical contact to the NW is unknown.

Selectivity and Temperature The second point reflects the simplicity of the process. The selectivity towards Si and SiO_2 implies that the process is self-aligned, therefore no extra lithography is required. The third listed point of benefits is the low temperature required, 80°C, this only consumes a minimal of the available thermal budget for the complete process.

Step coverage The fourth point refers to the isotropic growth which enables a deposition following the substrates and NWs topography. For a top-down patterned contact the step coverage is poor when using standard deposition tools would be poor, specially at the bottom part of the NW. These problems are circumvented with the electroless deposited Ni, since it grows around the NW. As proven by further SEM images, the Ni layer even grows below the NW, lifting it slightly. This fact is indeed relevant to the device

performance. However in Sect. 5 it will be shown, that the actual active region will be entirely gated after the intrusion of nickel silicides.

Contact area and NW-fixation A Ni contact surrounding the complete cross-sectional perimeter of the NW is formed as summarized in the fifth point. The large contact area is important for various reasons. First, a large area for the Ni diffusion into the NW is given. Second, the electric contact from the pad to the NW is enhanced by the reduction of serial resistances. Third, a good thermal contact is achieved which is important to enhance the thermal conductivity between the SiNW and the Ni contact. This is important for the pursued diffusion experiments as well as for the heat dissipation from the devices under operation. (The embedding of the NWs in Ni further gives a high mechanical stability of the NW-Ni junction. This Nw fixation method will be important when performing TEM analysis avoiding NW vibrations. Also, for additional processing steps involving wet-chemistry, mechanical stability proved to be important to fix the NW at its place.)

Possible disadvantages In this context, the possible related disadvantages should also be mentioned. One major issue is the potential contamination of the Si with the remaining elements contained in the solution for deposition, such as phosphorous and carbon. For instance EDX measurements of the electroless Ni showed traces of phosphorus. Also the reproducibility of exact amount of deposited Ni is an issue to consider. Variations in the pH and temperature change the deposition rate. The numerous advantages however show the high potential of this method for rendering contacts to one-dimensional structures.

3.4 Concluding Remarks

This chapter showed the main processing steps used to integrate SiNWs on test-chip templates for their posterior use in silicidation and transistor fabrication experiments. Of special interest are the novel electroless-plating contact techniques which were applied to contact NWs for the first time. The method is simple contacting procedure which yields maximal contact area to a NW with only one lithographical step. A later published work by S. Ingole et al. from *Los Alamos Natl. Lab* has shown the electroplating of Ni-pads to contact NWs [IAHP07] with similar results. The method shown here has the advantage of not needing to contact every electrode to be plated electrically, therefore allowing fast parallel processing practically applicable up to a wafer level. The next fabrication step is the annealing of the test chip which will

lead to the pursued diffusion of Ni into the NW. This will be dealt separately in the next chapter due to its special importance for this work.

Chapter 4

Longitudinal Nanowire Silicidation

Metal silicides are solid state compounds of metals with Si. Its vast majority exhibits metallic behavior whereas only a few of them show a semiconducting one. A large number of metallic silicides have important applications in modern integrated circuitry. They are mostly utilized as contacts between the degenerately doped Si source and drain regions and the first metallization layer, usually tungsten, to reduce serial resistances. Currently, they are used as gate electrodes to prevent depletion effects common in poly-Si gates. Recently, they have been implemented to induce local strain in Si or SiGe channels to enhance carrier mobility. The present chapter presents an innovative bottom-up approach able to transform segments of SiNWs into metallic ones. This is enabled by the longitudinal diffusion of Ni inside the SiNWs and a subsequent solid-state reaction resulting in a nickel silicide with metallic properties. The most remarkable characteristic of this reaction is that an abrupt metal to semiconductor interface is formed, which is useful for numerous electronic applications. Due to the novelty of the results and its central importance on this work an exclusive chapter was dedicated for this finding.

Outlook First, a brief theoretical description of the theory of atomic diffusion in a crystal and solid state reactions is given with an emphasis on the silicon system. Following this introduction, the state-of-the-art on silicide NW formation at the beginning of the experiments performed here is summarized. The silicidation experiments are then described and the results analyzed. At the end of this chapter an overview will be given on the current status of the longitudinal NW silicidation which has been adopted by other research groups.

4.1 Basic Theory of Impurity Diffusion in Solids

In this section the basic physical mechanisms responsible diffusion of atoms in solids are summarized. Diffusion is a phenomenon which very commonly takes place in all aggregate states. The first studies date as early as the 1820's, when Thomas Graham made the first numerical descriptions. From an atomistic point of view, the brownian motion of each atom in a medium can lead to its displacement as described by a probability function. Phenomenologically, it was found that concentration variations leads to the atomic movement. The main thermodynamical and microscopic descriptions of diffusion are briefly explained below.

4.1.1 Thermodynamical Description of Diffusion

In general thermodynamical terms, the driving force of all diffusion mechanisms is the presence of a gradient in the electrochemical potential. In most cases this can be simplified by a gradient in the concentration (N) of the species involved. In the case of a crystal, both impurity atoms and vacancies are subject to flow until a uniform distribution is established. The net atomic Flux (J_N) is described by *Fick's law* [Kit66, RM84]:

$$J_N = -D\nabla N. \tag{4.1}$$

Where, J_N is the number of atoms crossing a control area in a unit time; and D is the diffusion constant. The direction of flow takes place from high concentrations to lower ones, which is implied by the negative sign. Typically, J_N has an exponential thermal activation, which is reflected in D as:

$$D = D_0 e^{-E/k_B T}. \tag{4.2}$$

Here, E is the energy barrier named the activation energy required to be surpassed by each atom for diffusion to take place. Due to the validity of the *continuity equation* in diffusion phenomena, the time (t) and spacial relationship of the diffusing atoms can be written as [RM84, KK89]:

$$\frac{\partial N}{\partial t} = -\nabla \cdot J_N = D\nabla^2 N. \tag{4.3}$$

Equation 4.3 is known as the *diffusion equation.* Simplifying Equation 4.1 and Equation 4.1 to one-spacial dimension (x) gives, for Ficks law,

$$J_N = -D\frac{\partial N}{\partial x}, \tag{4.4}$$

and for the diffusion equation,

$$\frac{\partial N}{\partial t} = -\frac{\partial J_N}{\partial x} = D\frac{\partial^2 N}{\partial x^2}. \quad (4.5)$$

Boundary Conditions

When solving the equations above boundary- and initial-state conditions are required. There are two specific scenarios which describe the most relevant diffusion experiments: the presence of an unexhaustible and an exhaustible reservoir. With these conditions the Equations 4.4 and 4.5 are solved.

Unexhaustible reservoir The first case implies having a constant concentration N_0 at the interface $x = 0$ for all times and no diffused species in the crystal at $t = 0$, i.e. $N(x = 0; t > 0) = N_0$ and $N(x > 0; t = 0)$. Equation 4.5 has the solution [RM84]:

$$N(x,t) = N_0 \cdot erfc(\frac{x}{2\sqrt{Dt}}) \quad (4.6)$$

where $erfc(y)$ is the complementary error function $erf(y)$, see for example: [BAMM99] p.455 for a definition of this function. Figure 4.1 a) plots $N(x)$ for different diffusion parameters $\sqrt{Dt}$ (from [RM84]).

Exhaustible reservoir The other common case featuring an exhaustible reservoir is based on the assumption that the reservoir has N_0 atoms and a thickness h and that for $t > 0$ there is no flux, i.e.

$$N(x = 0) = \{ \begin{matrix} N_0, 0 < x < h \\ 0, x > h \end{matrix} \}; \qquad \frac{\partial N}{\partial x}|_{x=0;t>0} = 0 \quad (4.7)$$

The solution of Equation 4.5 is:

$$N(x,t) = \frac{N_0}{2}(erfc\frac{x-h}{2\sqrt{Dt}} - erfc\frac{x+h}{2\sqrt{Dt}}) \quad (4.8)$$

which according to [RM84, WMF96] can be approximated by a Gaussian profile:

$$N(x,t) = \frac{N_0 h}{\sqrt{\pi Dt}} e^{-(x/2\sqrt{Dt})^2}. \quad (4.9)$$

For this approximation, the result is plotted in Fig. 4.1 b) from [RM84] for different diffusion parameters $\sqrt{Dt}$. Analyzing Figs. 4.1a), b) the following

trivial observation is done: for both cases the impurity concentration drops as the distance x from the reaction interface increases. It can also be seen that for higher diffusion times, i.e. higher $\sqrt{Dt}$, the gradient of the impurity concentration decreases in both examples. For the unexhaustible reservoir this means that towards the reaction interface, N readily increased with t, consequently giving a smaller gradient in N between the reservoir and the crystal surface. As ∇N is the driving *force* for diffusion, J_N is lowered. A similar argumentation can be given for the $\sqrt{Dt}$ behavior of the slope of $N(x)$ for exhaustible reservoirs in Fig. 4.1 b), however for higher t inside the crystal the gradient will be lower because there is no more supply of diffusing species at the reaction interface. The decreasing $N(x = 0)$ for longer t or larger D is a consequence of the vanished source of diffusion species at the interface. Note that in order to create steep impurity profiles, short diffusion times and/or diffusion constants are required for both cases.

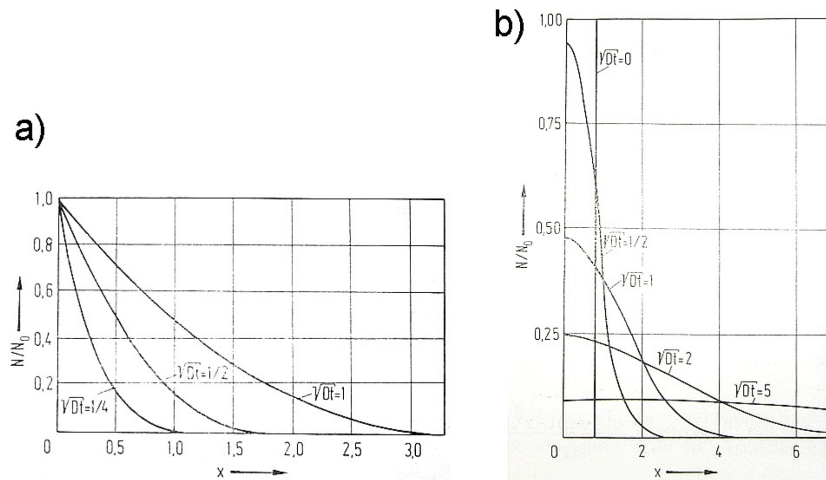


Figure 4.1: Typical impurity concentration profiles after diffusion with boundary conditions. a) Unexhaustible impurity reservoir at $x = 0$ for different parameters $\sqrt{Dt}$. b) Exhaustible reservoir at $x = 0$ also for different $\sqrt{Dt}$. From [RM84].

4.1.2 Microscopic Diffusion Mechanisms

In crystals basically three different diffusion mechanisms have been proposed [WB07]: diffusion through vacancies, interstitial diffusion and by place exchange. In the first case atoms "hop in" to occupy vacancies. As the vacancy

is displaced other atoms take its site. Therefore, the movement of vacancies implies a movement of atoms. This diffusion mechanism typically implies a comparably small D in its thermodynamical description, because large activation energies are required to break the covalent bonds. In the interstitial diffusion the diffusing atoms do not occupy regular lattice sites, they are bound in between these. Therefore, their interaction with the neighboring atoms is lower than in the previous case, which is expressed phenomenologically by a higher D. In this type of diffusion mechanism the lattice cell type is an important parameter to consider, because compact cells can difficultly accommodate interstitial atoms.

4.2 Basic Theory of Silicidation: Metal Silicon Solid State Reaction

Now that the basic diffusion mechanisms of impurities have been presented, the reaction between the diffused impurities with the host crystal is described. This is constricted to the solid state formation of silicides. Silicides are compounds formed of Si together with elements of higher electropositivity. That means the reaction with impurities that have a higher tendency to donate electrons, which include all transition-metals. Since low temperature processes are desired in the Back-End CMOS manufacturing most silicidation experiments are carried out as reactions in the solid-state. Most of the silicide reactions are possible at the solid-state and interestingly, as a rule of thumb silicide formation readily takes place at temperatures between one third and one half of the corresponding melting temperature in the Kelvin scale [Ohr02].

4.2.1 Kinetics of Silicidation

Bulk metal-silicides are usually created by depositing a thin layer of a metal on top of an oxide-free Si surface followed by annealing. Two main types of solid-state silicide reactions can be differentiated: diffusion limited and interface-reaction limited. Typically, the thickness of the formed silicide is proportional to $\sqrt{t}$ for the diffusion-limited reaction and directly proportional to t for interface-reaction limited reactions, where t is the reaction time [Böe90, Che05]. In both reactions metal atoms diffuse across the metal/silicide interface and/or Si atoms diffuse across the Si/silicide interface. Generally, in metal-rich silicides the dominant diffusing species are metal atoms, whereas in monosilicides and disilicides Si atoms are the dominant diffusing species. Nickel monosilicide (NiSi) is an exception, here Ni is

the dominant diffusing species [Che05].

4.2.2 Interface Reactions

When a silicide is formed the lattice is reordered, which requires the breaking of the bonds of both the impurity and Si atoms. Usually the energies required for breaking Si bonds are substantially higher than for most metal impurities. At high temperatures, Si atoms become free and react with the metal atoms. However, at lower temperatures the thermal energy is insufficient to break the Si bonds. Thus, for metal rich silicides alternative Si bond-breaking mechanisms have been proposed, e.g. by rapid interstitial migration of the metal atoms within the Si lattice [Ohr02]. This explains why metal-rich silicides are usually formed at lower temperatures than for Si rich ones. Typical activation energies for disilicide formation are 1.5 eV, for monosilicides 1.6-2.5 eV and for disilicides 1.7-3.2 eV [Ohr02].

Crystal orientation and epitaxial nucleation The crystalline orientation of the surface which reacts with the metal also plays a fundamental role. Planes with lower surface energyare more prone to react. In cubic lattices e.g. in Si the plane with the highest density of available bonds and thus with the lowest surface energy is (111)-oriented. Silicides can either have a poly-crystalline or single-crystalline structure, which usually depends on the lattice mismatch at the reaction interface. When the lattice mismatch is small enough, epitaxial and single crystalline silicide layers can principally be formed. In the contrary case of a large lattice mismatch, polycrystalline films are usually formed.

4.3 Nickel Silicides

One of the most commonly applied silicides in microelectronics is nickel silicide (Ni_xSi_y). Its bulk as well as thin film reactions have been studied extensively over the past decades. Figure 4.2 a) shows the eutectic- phase-diagram of the Ni/Si system. A first glance the diagram revels the complexity of the system: numerous stoichiometries in the solid-state can be formed. However, it is well known that the desired Ni-silicide phase can be formed by an accurate control of the anneal parameters and initial conditions [Mur83]. Due to the fact that most Ni silicides are readily formed in the solid state, the forming temperatures are significantly lower than the eutectic temperature. Table 4.1 lists selected parameters related to various commonly used Ni silicide phases according to different sources. The parameters are: the forming

temperature T_{form}, structure, melting temperature T_{melt}, resistivity ρ and Schottky barrier height to n-type Si ϕ_{Bn}.

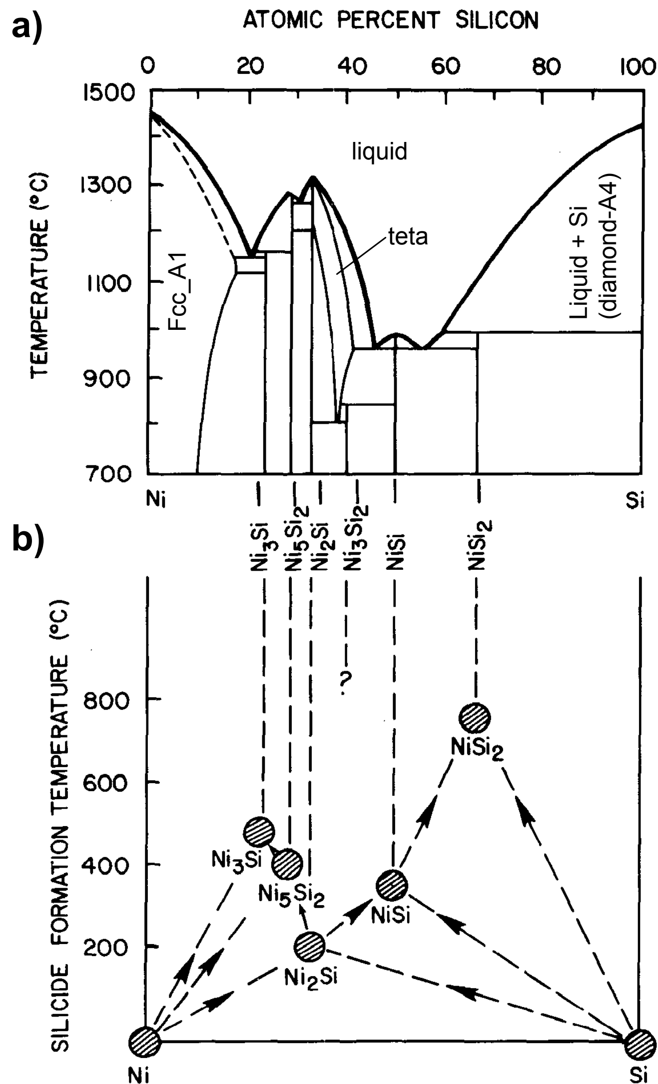


Figure 4.2: a) Eutectic diagram of the Ni-Si bulk system in Kelvin. b) Sequence for the formation of a specific silicide phase, reproduced from [Tu85].

The Ni rich phases can be readily formed at temperatures as low as 200°C. At a temperature of 400°C NiSi is formed, which exhibits the lowest resistivity of all Ni silicide phases. At much higher temperatures, 800°C, the silicon

Table 4.1: Physical properties of various nickel silicide phases. References (Ref.), (1): S. M. Sze [Sze81], (2): G. Ottaviani et al. [OTM81], (3): Rhoderick, E. H. [Rho78], (4): Tan T. Y. et al. [SHY82] and (5): Erskine J. L. et al. [CE83].

Phase	Structure	T_{form} [°C]	T_{melt} [°C]	ρ [µΩcm]		Φ_{Bn} [eV]		
Ref.	(1)	(1,5)	(1)	(2)	(1)	(3)	(4)	(2)
Ni_2Si	Orthohomb.	200	1318	25	0.70-0.75	0.71	0.63	0.66
NiSi	Orthohomb.	400-430	992	14	0.66-0.75	0.79	0.65	0.66
$NiSi_2$	Cubic, CaF_2	800	993	40	0.7	0.70	0.63	-

rich $NiSi_2$ phase is formed. Table 4.1 shows that from these three main stoichiometries only $NiSi_2$ has a cubic lattice structure and lattice constant which are compatible with the diamond-structure of Si. Therefore, $NiSi_2$ can be principally grown epitaxially on bulk Si. However, an epitaxial single crystalline formation is difficult to achieve because prior to the $NiSi_2$ formation, Ni_2Si and NiSi with orthorhombic lattices are sequentially formed as the temperature rises [DM00, WB76]. The sequence of silicide phases formed is given by kinetics, Fig. 4.2 b) shows the usual paths dependent in temperature and composition which are usually followed to obtain the desired Ni_xSi_y stoichiometry [Ohr02, Tu85]. The first silicide formed at low temperatures is Ni_2Si, depending on the amount of available species different paths are followed. In the case of a thin Ni layer on a Si substrate NiSi and then $NiSi_2$ is formed. For a thin Si layer on bulk Ni, Ni_5Si_2 and then Ni_3Si is formed.

4.3.1 Nickel Silicide NWs

Prior and parallel to this work, nickel silicide NWs can be formed either by direct synthesis or by the reaction of Ni with SiNWs. Directly synthesized NWs have been produced by the decomposition of SiH_4 on Ni films in a VLS-type of growth process [DSF+04]. NiSi NWs have also been grown by the metal induced growth, where a Si film is deposited on top of a Ni film followed by annealing [KA05].

Radial silicidation of SiNWs Alternatively SiNWs have been transformed into NiSi NWs by radial silicidation. The group of Charles M. Lieber [WXY+04] has shown this, by depositing a thin layer of Ni on a SiO_2 sub-

strate with dispersed SiNWs, and subsequent annealing. The Ni layer has a thickness comparable to the NWs diameter d_{NW}. Upon annealing The Ni layer surrounding the NW diffuses radially forming a single-crystalline Ni-monosilicide NW. The diffusion conditions clearly correspond to a limited reservoir, described previously in Sect. 4.1.1. In the same paper the authors showed that by locally masking the SiNWs with a photoresist, and then depositing Ni they were able to form longitudinal NiSi/SiNW heterostructures. HRTEM analysis revealed atomically sharp NiSi/Si interfaces.

Radial silicidation of Poly-Si NWs In another work [ZHs+06] top-down processed horizontal poly-Si NWs of various µm in length, 20-32 nm height and 30 nm width structured on SiO_2 layers were radially silicided. Evaporated Ni films of different thicknesses d_{Ni} covering the poly-Si NWs were used as the metal reservoir. Radial diffusion and subsequent annealing at 500°C transformed the poly-Si NWs into poly-crystalline Ni_xSi_y NWs of different composition depending on the Ni film thickness and NW height. For 32 nm high NWs $NiSi_2$ was formed for d_{Ni}=20 nm and NiSi for d_{Ni}=10 nm. Reducing the NW height to 20 nm and using d_{NM}=20 nm, $Ni_{31}Si_{12}$ was formed. A post-anneal of the Ni_2Si NWs at 800°C lead to larger crystal grains along the NWs length and to a reduction in resistivity from 25 µΩ cm to 10 µΩ cm while the stoichiometry was left intact [ZLH+06].

4.4 Longitudinal Nickel Silicidation of SiNWs

The previously explained experiments where SiNWs were transformed into NiSi NWs are limited to small Ni reservoirs, i.e. layer thicknesses comparable to the NW thickness. In contrast, the work performed here makes use of significantly larger Ni reservoirs, i.e. the Ni volume at the contacts is much larger than the NWs volume and can practically regarded as infinite reservoirs. The effect of SiNW silicidation with surplus Ni leading to a longitudinal silicidation of the nanowire is studied here.

4.4.1 Furnaces for Annealing

Several furnaces were used to carry on the diffusion experiments. These were the *P-5000* CVD chamber used for the NW growth, a lamp heated rapid thermal anneal (RTA) furnace as well as a resistive heater. The last two furnaces work at ambient pressure under a gas flow, whereas the CVD chamber can work under vacuum. The samples containing SiNWs contacted with Ni reservoirs as described in Sect. 3.3 and depicted schematically in

Fig. 3.1 f) are used for the diffusion experiments. Note that the actual temperature at the reaction interface was not measurable, the furnaces heated by a resistive holder are equipped with thermocouples locates at the holders surface. For both resistively heated furnaces, the heat is mainly transferred by conduction from the holder to the substrate and further onto the NW, and is limited by the contact roughness between the substrate and holders surfaces. For the resistive heaters the temperature at the NW is probably lower than at the heater, because the strong gas injected at room temperature into the chamber directly blows on the NWs.In the case of the RTA oven, the test-chips were placed on top of a Si carrier wafer which was heated both on its top and bottom sides. In addition to the heat transfer through the substrate the NW was also heated directly by the top lamps. The temperature was measured by pyrometry at the bottom side of the carrier wafer. In this case the NWs could have a higher temperature than the one measured.

4.4.2 Sample Preparation

First, the native Si-oxide surrounding the SiNW is removed entirely with a dip in BHF 100:1 for 30 s. Although a BHF dip was already performed prior to the Ni deposition, the Si/Ni interface is subject to oxidation. It was experimentally confirmed that an exclusion of the BHF step hindered the Ni diffusion into the SiNW. SiO_2 is known to be an effective diffusion barrier for Ni even with a thickness of a few nanometers. This suggests that O_2 was able to diffuse and oxidize the SiNW's surface. Possible diffusion paths are along the Ni grain boundaries or at the Ni/SiNW interface. The BHF dip ensures a clean interface at least at the outermost portion of the embedded NW, where BHF is able to penetrate the small cavities, (e.g. by capillarity forces). This region at the contacts edge is the most relevant for these silicidation experiments, because it is the only one which can be used as a reference (or marker) to determine the Ni diffusion length. Immediately after the oxide removal the substrates were transferred into the furnace where an inert atmosphere, i.e. Ar or N_2, delayed the re-oxidation of Si.

4.4.3 Annealing

As previously discussed in Sect. 4.3 there is a large variety of different Ni/Si compositions in the solid state, which makes the targeting of a specific phase difficult. The aim was to obtain silicides with low-resistivity, thus the formation of NiSi was envisioned at most, followed by Ni_2Si and $NiSi_2$. See Table 4.1 for the resistivity (ρ) values of different Ni-silicide phases for the thin film system according to several literature sources. As recommended in [Fog05]

a gentle temperature ramp was applied to avoid Ni void formation.Initial experiments were carried out in the CVD chamber used for the NW growth. First the chamber was purged with Ar for 60 s. The target temperature was 470°C, i.e. above the 400°C required for the NiSi formation. A heating ramp of 44.5°C/minute from 25°C to 480°C was used, then the temperature remained constant for 300 s, posteriorly the sample was cooled down to 25°C at a ramp of 40°C/minute.

4.4.4 SEM and EDX Analysis of Results

Figure 4.3a) shows the plane-SEM view of a typical NW embedded in Ni at its left side after the described oxide etching and the above mentioned annealing.The used SiNWs for this experiments were grown under the standard growth condition on SiO_2 substrates and most probably grow in the <112> direction. The NW exhibits two clearly distinguishable brightness regions along its length, where the segment adjacent to the Ni reservoir is significantly brighter than the NW-segment lying on the opposite side. The brightness enhancement is attributed to the presence of Ni in the NW. There are two reasons for the stronger intensity or brightness. One is the stronger backscattering of electrons due to the presence of atoms with higher atomic radii or numbers Z, Ni has Z=14, Si has Z=14 and O has Z=8. The other is attributed to the higher electrical conductivity of the material [LB81, Sch94].

EDX analysis To further study the composition of both regions as well as its interface, EDX measurements were carried out. First, a measurement with a primary electron energy of 20 keV was performed on the bright NW segment to identify the present elements. These only included Si, Ni and O, whereas the other contact metals Co, Ti and P were not found. Further, the electron beam of 5 keV energy was sampled at different spots along the NWs length. The lower acceleration energy is a trade-off between a sufficiently high energy to excite the Ni X-ray signal and the lowest possible energy in order to minimize the scattering length and therefore the acquisition volume [LB81, Sch94]. Throughout the entire bright segment a strong EDX signal corresponding to Ni signal was registered.

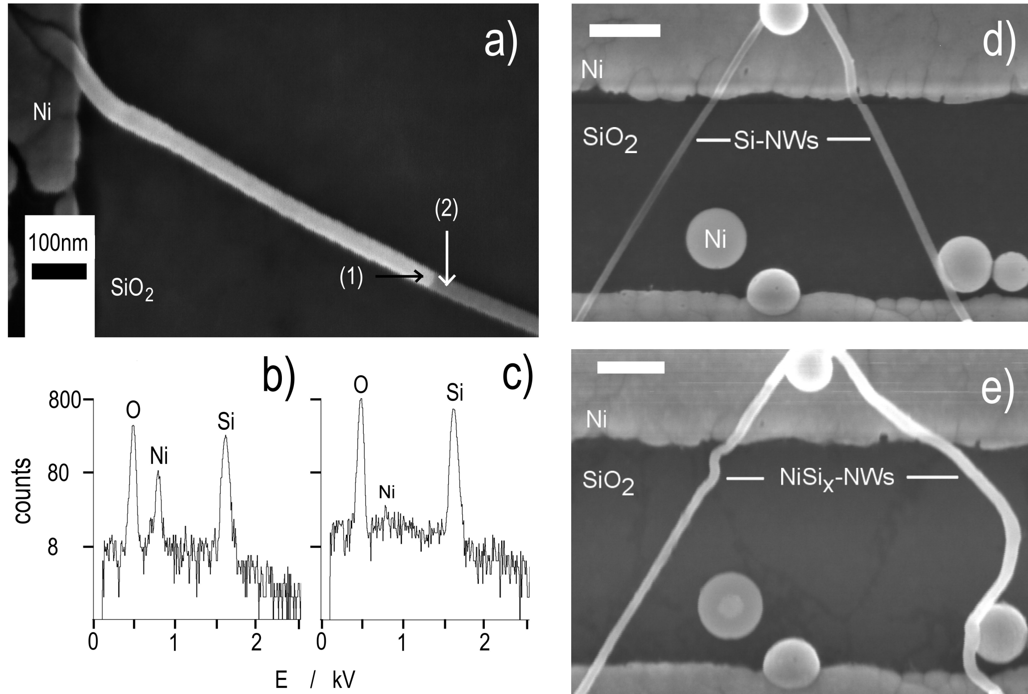


Figure 4.3: Ni-diffusion inside < 112 > SiNWs. a) SEM image of contacted SiNW with Ni at its left side after annealing. The bright segment contains Ni as confirmed by EDX sampling. b), c) EDX spectra at the interface for points (1) and (2) in a) respectively. The Ni signal drops down to the noise level at a distance of 20 nm from the brightness interface, showing the sharpness of the interface. SEM images of two SiNWs contacted at both sides with Ni before d) and after c) annealing. Ni diffuses throughout the entire NWs length expanding the NWs volume indicating its incorporation into the NWs volume.

Of special interest is the sharp brightness interface along the NWs length. EDX spectra were taken at two points located 20 nm away from the brightness interface and within the respective NW segments, see points (1) and (2) in Fig. 4.3 a). The EDX spectrum in point (1) showed that the bright NW segment adjacent to the contact pad clearly contained Ni, as seen in Fig. 4.3 b). In contrast the Ni peak of the spectrum corresponding to point (2), see Fig. 4.3 c), inside the darker NW section is barely higher than the noise level. The small Ni signal in Fig. 4.3c) is attributed to the still relatively large electron scattering range inside the sample. These observations show

that Ni has diffused into the SiNW and along its longitudinal axis from the metal pads up to the abrupt NW interface. The sharpness of the interface should be well below the distance between the brightness interface and point (2), i.e. 20 nm.

Volume enlargement for <112> oriented NWs Some aspects of the experiment still need further explanation. First, the question on whether the observed Ni diffusion took place inside the volume of the SiNW or over the NWs surface. Second, it should be determined whether the bright segments consisted of Ni-silicides or just contained Ni atoms which did not react with the SiNW, i.e. located interstitially inside the NW or on its surface. Some insight to these questions is given in Fig. 4.3 d), e). Here, SEM images of the same SiNWs contacted at both ends with Ni acquired before and after annealing are compared. The same anneal conditions were used as in the previous experiment. In this example Ni has diffused along the entire length of the NWs starting from both Ni pads, meaning that no brightness interface between the Ni rich NW segment and the pristine segment remains. It can be observed that the NW-length and width increased by up to 30%. The NWs elongation clearly shows, that Ni was incorporated in its volume. It further suggests, that the Ni diffused through the SiNWs volume, which would be expected to lead to the formation of solid Ni-silicides. Depending on the phase formed, different lattice constants are expected. The volume expansion by approximately 30% suggests the formation $NiSi_2$ NWs.

4.4.5 TEM Analysis

To further investigate the longitudinal Ni diffusion in SiNWs TEM-analysis in combination with electron energy loss spectroscopy (EELS) was performed on the SiNWs after Ni diffusion.

TEM sample preparation To enable this study special samples were fabricated on Cu TEM grids coated with a holey carbon layer. In this case a suspension of SiNWs grown on Si and exhibiting the <110> direction was deposited on the TEM grid. The same process steps and conditions previously applied to the test-chips were reproduced here. This includes both BHF dips, prior to metallization and to annealing. The electroless Ni plating was carried out for 60 s at 80°C and is selectively deposited on the Cu grid. Here the un-oxidized Cu works as a catalyst surface for the Ni deposition. The deposited Ni has the additional feature of providing mechanical stability to the embedded NWs, reducing unwanted vibrations in order to improve

high resolution TEM imaging. The anneal in Ar atmosphere encompassed a two-step heating with a linear rate of 4°C/s from 22°C to 200°C followed by a step at 2°C/s to 480°C, T then remained constant for 120 s and subsequent cooling down to 22°C took place at a ramp of 1.5°C/s. After SEM inspection a small amount of SiNWs were found, sticking out of the Ni-plated Cu grid. These were analyzed with TEM.

TEM imaging The results of one <110> oriented SiNW are summarized in Fig. 4.4. The SiNW is embedded in Ni at its bottom side sand stands out freely over a TEM-grid hole. Figure 4.4 a) shows a low resolution transmission image of the embedded NW. In contrast to the SEM back-scattered image (not shown here), the brightness is reversed, i.e. the darker NW segment is now adjacent to the Ni reservoir. In fact this proofs that back scattering is strongly enhanced by the larger Ni nucleus so that fewer electrons are transmitted through the sample, resulting in a lower signal. Far more importantly, this image shows that the sharp interface is indeed perpendicular to the NWs length axis and that it has a sharpness of at most a few nanometers.

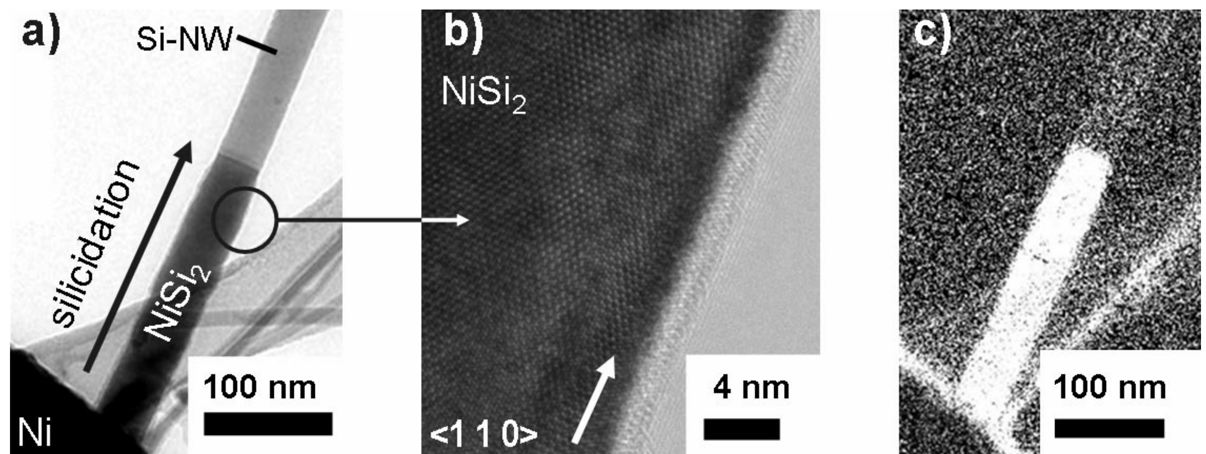


Figure 4.4: TEM images showing Ni-silicidation of longitudinal NW segments.

A comparison with the EELS mapping for Ni seen in Fig. 4.4 c) shows that the longitudinal NW segment adjacent to the Ni reservoir exactly corresponds to the EELS Ni signal. This is another proof that the brightness contrast in the SEM images can be attributed to the Ni content in the NW. One practical consequence of this is that SEM imaging can be used to ac-

curately locate the interface between the Ni-rich NW and the pristine SiNW thanks to the thin NW thickness. Moreover, the EELS Ni-map shows a uniform intensity within the Ni-rich segment. This implies that no gradual drop in the Ni concentration along the NWs length axis is observed, in contrast to what would be expected as a consequence of the diffusion equation 4.5.

Crystal structure The composition of the Ni-rich NW segment still needs to be determined. Therefore, HR-TEM imaging was performed on the area circled in Fig. 4.4 b) within the Ni-Rich NW-segment. The image with atomic resolution, shown in Fig. 4.4 b), proofs that Ni indeed reacted with the SiNW transforming it into a single crystal Ni silicide NW segment throughout the entire NWs thickness. The crystal lattice is identified as the fluorite or calcium-difluorite (CaF_2) cell. This cubic lattice configuration is well known for bulk $NiSi_2$ as previously shown in Table 4.1. The atomic arrangement inside the $NiSi_2$ fluorite lattice can be described as a face-centered cubic cell made from Ni, with the center of the cell inhabited by a cubic arrangement of Si [Mar02]. The crystalline orientation of the $NiSi_2$ NW segment corresponds to the <110> direction. Interestingly, this is the same orientation than the one exhibited by the SiNW. This and the fact that the $NiSi_2$ segment is single crystalline suggests that an epitaxial relation is given to the SiNW.

Amorphous coating An amorphous coating of around 1.5 nm thickness wraps up the Ni-silicide NW most probably is a Si-oxide. Silicon oxide formation on the surface of Ni-disilicides has been reported in [BN82] which basically is given by the higher tendency of Si to oxidize in comparison to Ni. The surface coating does not seem to consist of elemental Ni since this one would give a darker transmission signal and would tend to build clusters rather than a homogeneous layer.

Discussion

The fact that the coating does not contain Ni and the flat $NiSi_2$ to Si interface strongly suggest that the Ni diffuses inside the NWs volume and not on its surface. If the Ni would have diffused on the SiNW's surface, un-reacted Ni would still be present. Also the silicides NW segment would not be expected to be a single-crystal because the $NiSi_2$ crystal would grow form the shell to the core. Lastly, it would be unlikely that the interphase to the pristine SiNW segment resembles a straight line perpendicular to the NWs length axis. Ni surface diffusion could advance further at one side of the NW so that radial diffusion would not be evenly distributed in most of the cases.

The identified $NiSi_2$ phase is expected to form at around 800°C as seen in Table 4.1, but not at 480°C. Rather, the NiSi and Ni_2Si phases would be expected in a thin film reaction. $NiSi_2$ has only been reported at comparable temperatures as a thin interphase sheet with a couple of mono-layers of thickness between Ni-rich silicide phases and the un-reacted Si [CE83]. The reason is that this phase is more compatible to Si than the other phases due to its cubic lattice. Nevertheless, in this experiment the entire silicided NW segment showed this phase and single crystallinity. It must be noted that silicidation experiments with the same SiNW orientation, <110>, at temperatures as high as 350°C, no longitudinal silicidation was observed and that at temperatures between 350°C and 480°C the silicided NWs did not seem to exhibit a different phase. This is judged by the fact that the NWs are not elongated after silicidation, what would be expected for the NiSi and Ni_2Si stoichiometries. This fact and the flat reaction interface suggests that the $NiSi_2$ phase is formed directly without passing through other phases, which clearly is in contrast to the reaction between bulk-Si and a film Ni film. [DM00].

The longitudinal Ni diffusion process described here differs from those found in literature to create Ni-silicide NWs, since they utilize the radial diffusion of Ni deposited directly onto the surface of either synthesized SiNWs [WXY+04] or lithographically defined polycrystalline SiNWs [ZLH+06]. Lateral diffusion of Ni into thin silicon on insulator layers has been previously reported, [SHL+05, KZZ+05] where two-dimensional Ni-silicide regions were formed. The method shown here introduces the one-dimensional case.

In general terms the Ni reservoir is exhaustable, however the amount of atoms available at the Ni/NW interface is practically constant with time. The reason is that the small NW volume or rather the number of Si atoms will not be able to accommodate a the total amount of Ni atoms available at the large reservoirs.

Gradient in Ni diffusion An EELS scan for Ni was carried out along the NWs length and across the metallurgic interface. Throughout the silicide NW segment the Ni concentration is constant, i.e. no gradient is observed as a consequence of Ni diffusion. Crossing the metallurgic interface from the silicide to the Si segment, the Ni signal drops abruptly. Within the Si segment no Ni gradient is observed. This implies that the diffused Ni atoms easily react with the silicon at the interface, without diffusing over large distances into the the Si region.

4.4.6 Reaction Kinetics, In-Situ TEM Silicidation

It is difficult to analyze the silicidation rate at a constant temperature because of the relatively slow heating and cooling ramps, where Ni diffusion and silicidation is also expected to take place. To address this issue in-situ TEM analysis of the silicidation was carried out in collaboration with the Max Planck Institute for Microstructure Physics in Halle, Germany.

Sample preparation In order to boost the yield of NWs contacted to Ni reservoirs and bridging over the TEM holes, the holy carbon layer of the TEM grid was electroless Ni-plated as well. Since the carbon layer does not act catalytically, the TEM grid was submerged in a solution containing H_2PdCl_4 and HCl at 75°C. Palladium clusters of a few nanometers in size are formed and randomly adhere onto the TEM grid to act as catalyst particles and seeds for the posterior electroless plating [Rie91]. Subsequently <111> oriented SiNWs were deposited from a suspension. After a dip in 100:1 BHF for 25 s Ni was electroless plated for 30 s at 82°C, the NWs bridging over the holes were contacted with the Ni reservoir on both ends. A pre-heating step at 400°C for 60 s was performed to initially silicidize a portion of the SiNWs in order to locate the metallurgic interfaces with an SEM prior to the TEM analysis.

Pre-annealing After a BHF dip for 30 s the TEM grid was annealed first from 22°C to 280°C with a ramp of 4°C/s, then to 400°C at 2°C/s followed by a dwell time of 150 s at 400°C. Cooling down to 22°C took place with a rate of 3.5°C/s. An example of one NW is shown in Fig. 4.5 a) and at a higher magnification in c). The process of Ni-plating and pre-annealing the TEM grid has several advantages. Both metallurgic interfaces are well located over a hole to allow analysis with TEM. The NW is fixed at both ends with the Ni reservoirs, reducing unwanted NW vibrations during imaging due to electrostatic forces. Heat conduction is considered to be sufficiently high through the Ni layer for NW silicidation to occur.

In-situ TEM annealing Annealing was then performed in the TEM by heating the holder at a ramp of 20°C/minute. At 400°C, longitudinal Ni diffusion started to be observed. The temperature was then kept constant at 400°C. It was observed that both metallurgic Ni-silicide to Si NW-interfaces advanced towards each other at a constant rate. After only 240 s the NW was silicided completely. During this experiment other important observations were made: interference fringes could be observed at the silicide NW-segment; the metallurgic interfaces remained sharp and perpendicularly oriented to

the NWs direction <110>; no significant NW elongation was observed. The appearance of interference fringes reinforces the fact that this is a solid state reaction as expected at these temperatures and elementary composition. The fast diffusion rate suggests that the diffusion mechanism of Ni atoms is indeed through interstitial locations not only inside the SiNW but also within the already formed $NiSi_2$ NW segments. This is consistent with the results in thin film experiments [Tu75]. The steady longitudinal silicide formation rate implies that the silicidation is limited by the interface-reaction as discussed in Sect. 4.2.1. Moreover, the reaction directly forms the $NiSi_2$ phase without passing through the usual sequence of stoichiometries listed in Fig. 4.2 b).

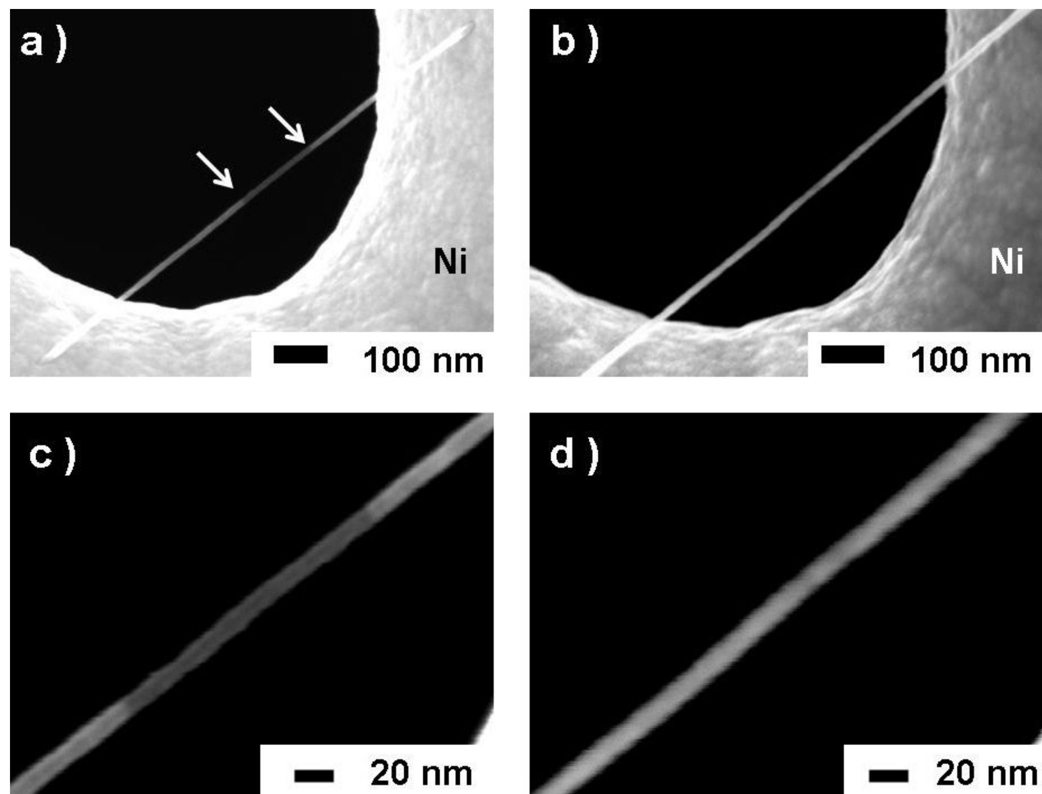


Figure 4.5: In-situ TEM imaging of SiNW silicidation. a) SEM image of SiNW embedded in Ni at both ends after pre-annealing at 450°C. Both metallurgic interfaces are located over a layer hole to enable transmission imaging. b) SEM image of silicidation after in-situ anneal in a TEM at 400°C, the complete NW was converted into $NiSi_2$. c), d) magnified views of a) and b) correspondingly.

4.4.7 State-of-the-Art: Silicide NWs

Longitudinal Ni-silicidation Following the publication of the main results presented here on the longitudinal silicidation of SiNWs [WGG+06] in November 2006, various related interesting studies have been published since then. Joerg Appenzeller et al. from IBM-Research simultaneously worked on the longitudinal silicidation of SiNWs at temperatures as low as 280°C. In [AKT+06] the effect of the SiNW diameter in the longitudinal silicidation length l_{NiSi} was studied. It was found that the silicidation length increases proportional to $1/d_{NW}^2$. This confirms that the NW silicidation/diffusion is a volume effect, which is in accordance with this work. Another work [LWW+07] by Kuo-Chang Lu and K. N. Tu was dedicated to the in-situ TEM analysis of NW Ni-silicidation. In those experiments, the authors analyzed the reaction between superimposed <111> oriented SiNWs and Ni-NWs. In contrast to the work presented here, the Ni/Si contact area is reduced to a point contact. Further the silicon oxide shell surrounding the SiNW was not removed. After heating the sample at temperatures between 500°C and 700°C inside the TEM, single crystalline <111> oriented orthorhombic NiSi segments were formed. Their interface to the SiNW segments was epitaxially and atomically sharp and parallel to the <111> plane of the Si-segment as shown by HRTEM. Nevertheless, the authors claim that the silicide grows from the free standing end of the silicide instead of from the contact with the Ni reservoir. In the present work, this effect was never observed as seen for instance in Fig. 4.3.

Other materials Recently the concept of longitudinal silicidation has been extended to alternative material systems. The group of Charles Lieber employed the longitudinal formation of Ni-germanides and Ni-silicides in Ge/Si core/shell NW heterostructures for the fabrication of contacts to NW transistors [HXL+08]. Also recently longitudinal platinum silicidation of SiNWs has been shown in [LLW+08]. These publications show that the longitudinal NW silicidation opened a small niche in nanowire research with interesting potential for applications.

4.5 Electrical Characteristics of Ni-Silicide Nanowires

Next, the electrical characteristics of $NiSi_2$ NW segments were determined. For this purpose, single SiNWs bridging two adjacent Ni pads were silicided with Ni throughout their entire length as shown in Fig. 4.6 a). The NWs

transformed into $NiSi_2$ were subject to two point $I-V$ measurements. Figure 4.6 b) shows the recorded $I-V$ curve for the structure shown in Fig. 4.6 a). The curve has two parts, one a linear one for low voltages and a breakdown part at higher values. In the left part of the curve, the current response indeed behaves linear to the voltage applied, as expected for an Ohmic conductor. This is yet another proof, that the SiNW is completely transformed into a silicide. The inverse slope of this linear segment gives the resistance R of the complete measurement setup, i.e. the $NiSi_2$ NW connected in series to the two Ni leads and measurement needles, amounting to R=160 Ω. (Since a simple (sheet) resistance measurement of the Ni leads, typically gives a resistance of 10 Ω, the largest series resistor is considered to be the NW itself.) Further, the total resistance together with the geometric dimensions of the NWs give an upper estimate of the resistivity ρ_{NW} by the simple relation:

$$\rho_{max} = R\frac{A_{NW}}{l_{NW}} = R\frac{\pi d_{NW}^2/4}{l_{NW}} \tag{4.10}$$

where A_{NW} denotes the cross sectional area of the NW given by the NWs diameter d_{NW}, and l_{NW} the length of the NW between two adjacent Ni contacts. Thus, ρ_{NW} = 96 µΩ-cm. As a comparison, the resistivity, ρ, of bulk $NiSi_2$ is approximately ρ = 40 µΩ-cm [OTM81].

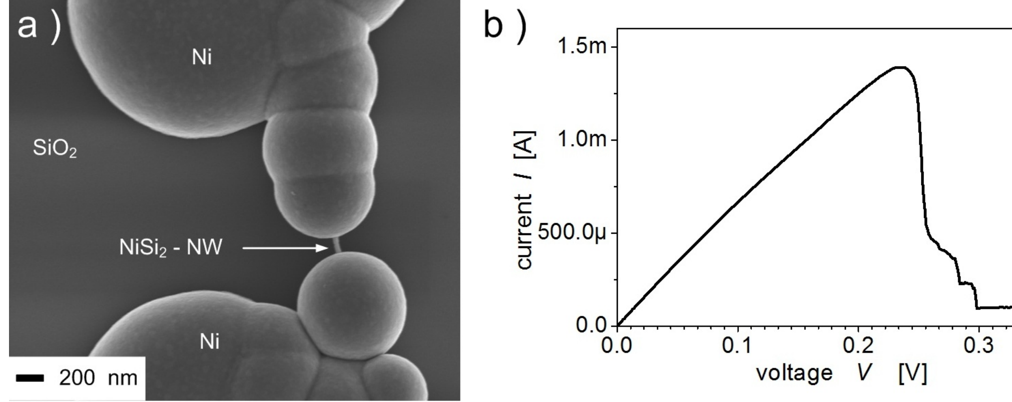


Figure 4.6: Ohmic behavior of $NiSi_2$ NWs. a) SEM plane-view of measured 2-point structure with a 112 nm long and 30 nm thick $NiSi_2$ NW. b) Recorded I-V curve showing ohmic behavior till breakdown of the NW due to Joule heating. From the linear part the total resistance is determined: 160 Ω and the maximal resistivity ρ = 96 µΩ-cm. The breakdown current density J_{max} = 205 MA/cm^2.

The significantly higher value obtained here can be explained by the contribution of the serial resistance of the Ni leads. On the other hand it should also be considered, that small metallic conductors behave differently than their implementation in bulk. When the thickness of the conductor is reduced down to the mean-free-path of the electrons or below, scattering at the conductors side-walls becomes dominant. Consequently, ρ increases with thinner conductor diameters, this phenomena is known as the *size-effect*. In the case of small poly-crystalline metallic conductors the grain size can be limited by the width of the conductor. The size effect then has a higher impact when the grain size is comparable or smaller to the mean free path. According to [SSSE02], scattering at the grain boundaries is stronger than at the side-walls (because the grain is always confined and must be smaller than the conductor).

Due to the fact, that the $NiSi_2$ NWs have single-crystalline lattice, as described previously in Sect. 4.4, grain boundary scattering is suppressed. Thus, a ρ near to the bulk value is expected. In order to extract the exact $NiSi_2$-NW resistivity alternative methods are required, where the serial contact resistance is subtracted for example a four point measurement or a transmission line method. Indeed, the group of Charles Lieber has performed four point measurement of radially Ni-silicided NWs, obtaining the same ρ as in thin films 10 µΩ-cm [WXY+04].

As the voltage is further increased above 0.21 V, the resistance increases until breakdown occurs at 0.24 V. The resistance un-linearity observed before breakdown is caused probably due to Joule-heating, where stronger scattering translates into higher resistance. Next, the breakdown current-density J_{max} is calculated from the maximal current I_{max} and A_{NW} after: $J_{max} = I_{max}/A_{NW}$. Accordingly, J_{max}=205 MA/cm^2. This value is higher than the one commonly achieved with state of the art of nano-interconnects made out of Cu [SCKYTV03, Sti07] and is approximately one order of magnitude smaller, than what single-walled CNTs can achieve [KGD+02, KGL+04]. In electrical conductors, breakdown mainly occurs at the grain boundaries. The high breakdown-current is another favorable feature of the single-crystalline structure of $NiSi_2$ NWs.

4.6 Conclusions

The first studies to report longitudinal NW-silicidation were presented in this chapter. Segments of SiNWs can be transformed into metallic ones by the longitudinal formation of a silicide within the NW upon annealing at temperature between 400-480°C. Nickel silicide segments of various micrometers

of length can be obtained. The most interesting aspect is the flat interface formed between the nickel-silicide and the pristine SiNW segments, which exhibits a sharpness in the nanometer scale or better. In fact, atomically flat interfaces have been shown recently by other groups. SiNWs oriented in the <110> direction seem to directly form <110> oriented $NiSi_2$ with a cubic fluorite lattice without passing through the usual stoichiometries so far reported in thin film silicide reactions. Further, the $NiSi_2$ lattice exhibits single crystallinity, an interesting attribute for electrical applications. The longitudinal NW silicidation is limited by the reaction kinetics at the interface and not by the diffusion length, at least at a length of hundreds of nanometers. In contrast <112> oriented SiNWs seem to form the metal-rich Ni_2Si phase, exhibiting a larger volume expansion of 30%. The electrical properties of fully Ni silicided NWs were determined. $NiSi_2$ NWs exhibited linear $I-V$ behavior with maximal resistivities of 96 $\mu\Omega$-cm. The NWs resisted high breakdown current densities of up to 205 MA/cm^2, higher than state-of-the-art Cu nano-interconnects. In the next chapter these NW heterostructures will be implemented to enable high performance electronics.

Chapter 5

Silicon Nanowire Schottky Barrier Field Effect Transistors

This chapter will present the implementation of Ni_xSi_y/Si/Ni_xSi_y NW heterostructures for the realization of high performance field effect transistors. In this context the technological and device related advantages gained by the use of these heterostructures will be emphasized. The electrical characteristics of these devices will be presented and compared with state of the art FETs.

An important attribute of these transistors is the presence of Schottky barriers at the source and drain contacts. Therefore, the basic theory of the Schottky contact formation and transport through it will be summarized briefly at the beginning of this chapter in Sect. 5.1. The actual experimental description will then follow. The combined approach to fabricate SiNW SBFETs will be described in Sect. 5.2. Further, the electrical characterization of the devices will be presented and discussed in Sect. 5.3. The impact of the gate oxide thickness scaling on the SBFETs will be studied in Sect. 5.3.3. Finally, the devices will be benchmarked with state-of-the-art nanowire-, nanotube-FETs and other novel transistors in Sect. 5.3.4 Note that a deeper analysis on the electronic transport in SiNW Schottky-barrier FETs will be dealt separately in chapter 6.

5.1 Schottky Barrier Field Effect Transistors

An interesting alternative to the classical MOSFET is the Schottky-barrier FET (SBFET). Structurally the only difference is that the degenerately doped source and drain (S/D) regions are replaced by a metal. This however, has a strong implication on the electronic transport through the device.

The implementation of a metal contact to a moderately or undoped semiconductor usually introduces a potential barrier at the semiconductor/metal interface ideally only dependent of the work function and electron affinity of the metal and semiconductor respectively used.

The use of metal source and drain contacts leads to the following direct effects. On the one hand the serial resistance is decreased by replacing the degenerately doped S/D semiconductor contacts with low conductance by highly conductive metal electrodes. On the other hand the potential barrier limits the current flow. Thus, the performance gain seems to be ambiguous at a first glance. Nevertheless, low RC-delays have been demonstrated in SBFETs making them promissing candidates for high speed Si circuits [FCS+04] with cut-off frequencies of up to 280 GHz. Other significant advantages are expected in the technological implementation and performance of SBFETs. The realization of sharper interfaces and thus the implicit omission of sharp doping profiles is one clear technological benefit, which alleviates the problems related to the fluctuation of the dopant concentration in nanoscale devices. Furthermore, no $p-n$ junctions and related depletion regions are formed, so that the classical short channel effects can be circumvented. Further on parasitic bipolar operation and latch-up effects are also hindered.

5.1.1 Schottky Barrier Formation

For a thorough analysis of the SBFET it is helpful to previously describe the Schottky contact formation and carrier transport over the barrier. The metal and semiconductor of band gap E_g sketched in the energy-band diagram of Fig. 5.1 will be considered. Figure 5.1 a) shows the case of separated metal and semiconductor under the premise that no surface states are present. The metal is said to have a work function ϕ_m in Volts. Therefore, with q being the magnitude of the electronic charge $q\phi_m$ is defined as the mean energy that an electron is required to surpass in order to be emitted to the vacuum. Accordingly,

$$q\phi_m = (E_{vac} - E_F) \tag{5.1}$$

where E_{vac} is the vacuum level and E_F is the Fermi level both last ones, in eV. Analogous, for the Si the energy required for emission from the conduction band E_c is

$$q\chi = (E_{vac} - E_c) \tag{5.2}$$

where χ is called the electron affinity.

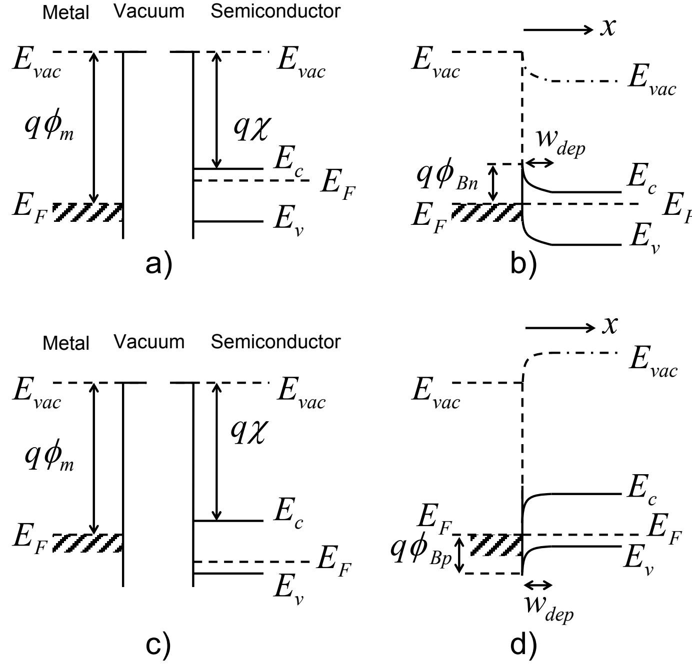


Figure 5.1: Schematic band diagrams of the Schottky barrier formation. a) , b) for a n-type and c), d) for a p-type semiconductor. In a) and c) the metal and semiconductor are separated by vacuum, whereas in b) and d) they are contacted and in thermal equilibrium.

The schematic energy-band diagram resulting from bringing the Si in contact with the metal and establishing thermal equilibrium, i.e. by a carrier flow between both regions, is depicted in Fig. 5.1 b). Due to thermal equilibrium the fermi levels of the metal and Si are aligned. Simultaneously, as a boundary condition the vacuum levels are required to align at the metallurgic interface. Consequently, the semiconductors energy-bands will be forced to bend towards the metallurgic junction. Between E_F of the metal and E_c an energy barrier of height $q\phi_{Bn}$ arises. The potential barrier ϕ_{Bn} is called the Schottky barrier for electrons and is ideally simply given by:

$$\phi_{Bn} = \phi_m - \chi. \tag{5.3}$$

Analogous, a potential barrier for holes ϕ_{Bp} arises between the E_F of the metal and the valence band E_v, see Fig. 5.1. ϕ_{Bp} is given by:

$$\phi_{Bp} = E_g/q - (\phi_m - \chi). \tag{5.4}$$

It can be easily confirmed that the sum of both barrier heights is equivalent to E_g:

$$\phi_{Bn} + \phi_{Bp} = E_g. \tag{5.5}$$

Equations 5.3 and 5.4 are based on ideal considerations. In real implementations ϕ_B can be affected by interface layers and states as the sensitivity of ϕ_m towards surface contamination [Sze81].

Schottky Effect

The Schottky effect describes the lowering of the SB height due to the image force induced by electric charges in the semiconductor, especially by the ones located near the metallurgic interface. According to electrostatics an electron with charge $-q$ located at a distance x from the metal induces a positive image charge with charge $+q$ located inside the metal at the location $-x$. The attractive image force F induced is given by

$$F = \frac{-q^2}{4\pi(2x)^2\epsilon_s} \tag{5.6}$$

where ϵ_s is the permeativity of the semiconductor. As a consequence of the image force and the presence of an external field ξ acting on the interface, the potential barrier for charge carrier emission is lowered. The potential energy experienced by the electron at the location x is the addition of the work required to bring the electron from infinity to x as a consequence of F and the energy delivered by ξ:

$$E_{pot} = \int_{\infty}^{x} F dx + q\xi_x = \frac{q^2}{16\pi\epsilon_s x} + q\xi_x \tag{5.7}$$

As a consequence E_{pot} exhibits a lower and shifted maximum in contrast to the ideal Schottky barrier. The Schottky barrier lowering is given by

$$\Delta\phi = \sqrt{\frac{q\psi}{4\pi\epsilon_s}}. \tag{5.8}$$

This implies that for stronger ψ acting on the interface, the Schottky effect will be stronger, e.g. for a larger reverse bias.

5.1.2 Electronic Transport Mechanisms Through the Schottky Contact

There are various charge transport mechanisms through a Schottky contact. Figure 5.2 schematically shows the basic transport paths in the energy band diagram of a metal contact with a n-doped semiconductor in forward bias. The dominating mechanism at room temperature where the bands are not strongly bent at the contact is thermionic emission, i.e. carrier injection over the barrier enabled by the thermal energy distribution. Whenever a barrier is thin enough quantum mechanical tunneling of electrons becomes possible. Other basic mechanisms include electron-hole recombination inside the space-charge region.

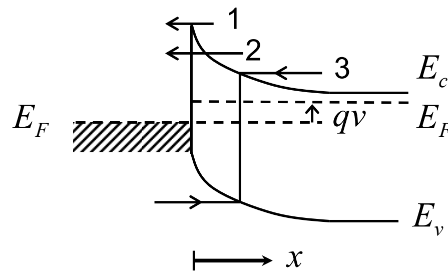


Figure 5.2: Basic transport mechanisms through a Schottky contact, 1.- thermionic emission, 2.- quantum mechanical tunneling and 3.- electron-hole recombination. After [Sze81].

Thermionic Emission

Thermionic Emission describes the current transport over the Schottky barrier, for instance with a height $\phi_B = \phi_{Bn} - \Delta\phi$, readily reduced by the Schottky effect as described by Equation 5.8. This transport mechanism was proposed by Hans Bethe under the assumption that $\phi_B >> kT$ and that a net current flow does not affect thermal equilibrium. The total current density J_{TE} is the addition of the contributions from the semiconductor to the metal, $J_{s\mapsto m}$, and from metal to the semiconductor $J_{m\mapsto s}$,

$$J_{TE} = J_{s\mapsto m} + J_{m\mapsto s} \tag{5.9}$$

For $J_{s\mapsto m}$, only the electrons with sufficiently high energies to overcome the barrier, i.e. with $E \geq E_F + q\phi_B$, define the current density $J_{s\mapsto m}$:

$$J_{s\mapsto m} = \int_{E_F+q\phi_B}^{\infty} qv_x dn \tag{5.10}$$

where n is the electron concentration and v_x is the carrier velocity in the direction of transport x. Taking into account that the electron energy density in an incremental energy range is given by: $dn = N(E)F(E)dE$, Equation 5.10 can be integrated in terms of dE. Here, $N(E)$ and $F(E)$ are the density of states and the Fermi-Dirac distribution function respectively. Assuming that the electron energy in the conduction band is kinetic, i.e. $E - E_c = 1/2m^*v^2$, the differential of the electron concentration can be written as:

$$dn = 2(\frac{m^*}{h})^3 e^{-\frac{E_c-E_F}{kT}} e^{-\frac{m^*v^2}{2kT}} 4\pi v^2 dv \tag{5.11}$$

where m^* is the effective mass of the semiconductor. Equation 5.11 gives the number of electrons per unit volume that have speeds between v and $v + dv$ in all directions. Resolving v and dv into its components, substituting Equation 5.11 into 5.10 and solving the integrals gives

$$J_{s\mapsto m} = A^*T^2 e^{-\frac{q\phi_B}{kT}} e^{\frac{qV}{kT}}. \tag{5.12}$$

Here, the current density from the semiconductor into the metal is given in terms of the Schottky barrier height ϕ_B, applied forward bias V and temperature T. The material related parameters are summarized in the effective Richardson constant A^*.

$$A^* = \frac{4\pi q m^* k^2}{h^3} \tag{5.13}$$

where optical phonon scattering and quantum mechanical reflection at the Schottky contact are neglected [Sze81]. In the case of semiconductors with isotropic effective mass in the lowest minimum of E_c, A^* can be written in terms of the Richardson constant for free electrons A=120 A/cm^2/K^2 and the free electron mass m_0, as: $A^*/A = m * /m_0$. In the case of n-Si different E_c minima with distinct m^* are given for different crystallographic orientations. For p-Si the two energy maxima at the wave vector $\mathbf{k} = 0$ are approximately isotropic [Sze81]. Some A^*/A values are summarized in Table 5.1. Next, the current density flowing from the metal to the semiconductor $J_{m\mapsto s}$ is

Table 5.1: Selected values of A^*/A. From [Sze81]

p-Si	n-Si$_{<111>}$	n-Si$_{<100>}$
0.66	2.2	2.1

determined. At thermal equilibrium, i.e. V=0, a perquisite is that $J_{m\mapsto s} = -J_{s\mapsto m}$, therefore from Equation 5.12

$$J_{m\mapsto s} = -A^*T^2e^{-\frac{q\phi_B}{kT}}. \tag{5.14}$$

Inserting this term in Equation 5.9 leads to

$$J_{TE} = A^*T^2e^{-\frac{q\phi_B}{kT}}[e^{\frac{qV}{kT}} - 1]. \tag{5.15}$$

Current injection in thermionic emission over a potential barrier is thus exponentially activated by the forward bias applied and drops exponentially as the barrier height increases. The temperature dependence is given by the Fermi-Dirac distribution. Since the SiNWs used in this work are nominally undoped, the collisions within the depletion region are excluded, i.e. the diffusion theory derived by Walter Schottky is not considered here. However, note that if this effects would be included the basic dependencies would still be equivalent to Bethe's description in Equation 5.15, only that the saturation current density would show a stronger dependence on the applied bias.

Tunneling through the SB

The other important transport mechanism to be discussed here is quantum mechanical tunneling. C. Y. Chang and S. M. Sze derived a description combining the contributions of tunneling and thermionic emission as well as including the Schottky effect [Sze81]. Equation 5.10 for thermionic emission is extended to include the tunneling component, and also incorporates the Schottky effect. $J_{s\mapsto m}$ is proportional to the quantum transmission coefficient Γ, the Fermi-Dirac occupation probability in the semiconductor F_s and the unoccupied probability in the metal $(1 - F_m)$. Therefore,

$$\begin{aligned} {}_{s\mapsto m} &= \tfrac{A^*T}{k}\int_0^\infty \Gamma(\zeta)e^{\frac{-q(V_b+\zeta-\Delta\phi)+E_F-E_C}{kT}}d\zeta \\ &+\tfrac{A^*T}{k}\int_0^{q(V_b-\Delta\phi)} F_s(V)\Gamma(\eta)(1-F_m)d\eta \end{aligned} \tag{5.16}$$

where ζ and η are potential differences measured upward and downward from the potential maximum. The first term is the contribution from thermionic emission, for $\Gamma(\zeta)$ =1 it takes the expression in Equation 5.12. The second term corresponds to the tunneling component, where $\Gamma(\zeta)$ and $\Gamma(\eta)$ are the transmission coefficient above and below the potential maximum, respectively. A similar expression can be derived for the current density flowing from the metal to the semiconductor

$$
\begin{aligned}
{}_{m\mapsto s} = -\tfrac{A^*T}{k} e^{-\frac{-q\phi_B}{kT}} \textstyle\int_0^\infty \Gamma(\zeta) e^{-\frac{\zeta}{kT}} d\zeta \\
-\tfrac{A^*T}{k} \textstyle\int_0^{q(V_b-\Delta\phi)} F_m \Gamma(\eta)(1-F_s) d\eta.
\end{aligned}
\tag{5.17}
$$

The total current density through the Schottky contact J_{SB} is the sum of Equations 5.16 and 5.17 and can be expressed as

$$
J_{SB} = J_{m\mapsto s} + J_{s\mapsto m} = J_S[e^{qV/nkT} - 1] \tag{5.18}
$$

or approximated as

$$
J_{SB} \simeq J_S e^{\frac{qV}{n_{id}kT}} \text{for } V \gg kT/q. \tag{5.19}
$$

Here, J_S is the saturation value for the current density and n is the ideality factor defined as

$$
n \equiv \frac{q}{kT} \frac{\partial V}{\partial(lnJ)}. \tag{5.20}
$$

Both J_n and n_{id} can be determined experimentally from the $I - V$ characteristics of Schottky diodes. Typically, the ideality factor is close to unity for low doping concentrations and high temperatures, i.e. where thermionic emission dominates. As the current contribution deriving from tunneling is higher, the ideality factor increases substantially. This is the case at high doping concentrations (where the potential barrier is thin enough for tunneling) and low temperatures (where thermionic emission is reduced). In the case of dominating tunneling current, the transmission coefficient decays exponentially as the barrier height increases:

$$
\Gamma(\eta) \sim e^{-\dfrac{q\phi_B}{E_{00}}} \text{with} E_{00} \equiv q\tfrac{\hbar}{2}\sqrt{\tfrac{N_D}{\epsilon_s m^*}}. \tag{5.21}
$$

The last equation implies that the tunneling current increases exponentially with $\sqrt{N_D}$. Therefore in conventional CMOS devices highly doped regions are used to contact the semiconducting source and drain contacts with metal interconnects. In these contacts the SB is so thin that practically all carriers tunnel through it so that the $I - V$ characteristic of the constant is linear for a certain voltage range.

5.1.3 Electrical behavior of Schottky Barrier FETs

Substituting the source and drain regions of FETs with metal electrodes introduces Schottky barriers at the metallurgic junctions as described above in Sect. 5.1.1. Depending on the material combination of choice different ϕ_B and related contact resistances will be given. The Schottky barriers will therefore strongly influence the electrical behavior of the device. In the case of Si-FETs mostly silicides are used as metal contacts, as these are known to build a clean and stable interface to Si. Interestingly, most silicide to Si Schottky contacts are known to have a lower ϕ_{Bp} than ϕ_{Bn}. A few exceptions have been reported showing $\phi_{Bp} < \phi_{Bn}$ by implementing rather exotic metals: yttrium-disilicide and various rare-earth metal silicides like erbium-, dysprosium-, holmium-, gadolinium-disilicides [TTT81].

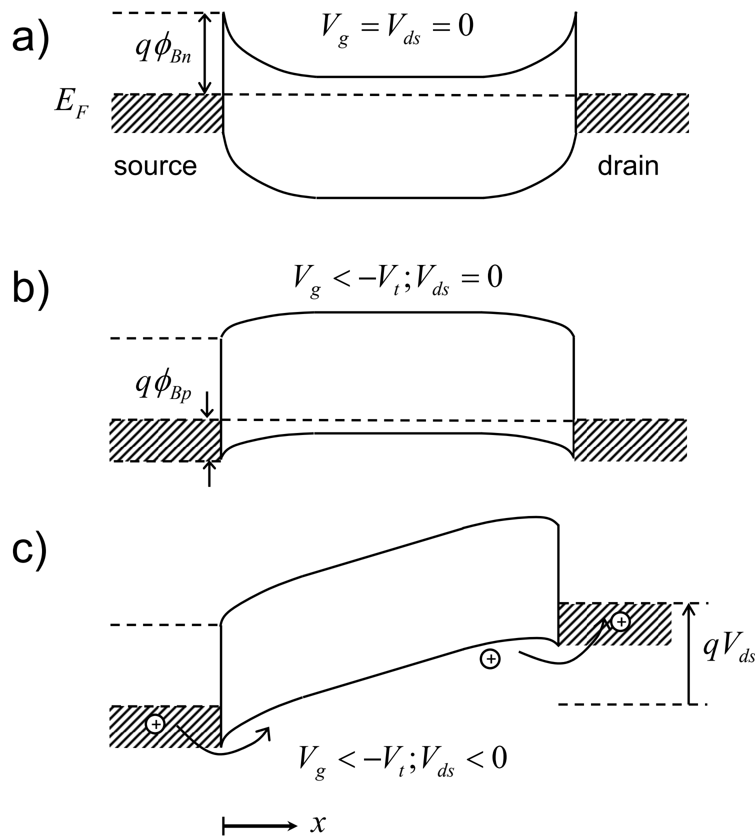


Figure 5.3: Energy band diagrams of an n-doped SBFET at different gate potentials.

The control over the active region of SBFETs is subject to the same field-effect mechanisms occurring in classical FETs, only that the carrier transport is limited by the respective potential barriers for electrons and/or holes. This translates into an extra series resistance acting on the respective carrier type. The dominant transport mechanism through the Schottky contacts in SBFETs has been reported to be thermionic emission [Sze81]. Since the current injection is exponentially dependent on ϕ_B as seen in Equation 5.15 the ratio between ϕ_{Bn} and ϕ_{Bp} will determine the dominant type of charge carriers that can be injected through the Schottky contacts. To further explain this the schematic energy band diagrams of an n-doped SBFET with $\phi_{Bn} > \phi_{Bp}$ depicted in Figure 5.3 will be used.

The source contact is contacted to the common mass and external electric fields are applied by the gate voltage V_g and the V_{ds} drain to source voltage as in a conventional MOSFET. At thermal equilibrium, V_g =0 and V_{ds}=0 the barrier $q\phi_{Bn}$ for electrons is formed at the S/D electrodes as seen in Fig. 5.3 a). For holes, the barrier is higher than ϕ_{Bp} and specifically amounts to $E_g - (E_C - E_F)$ measured outside the depletion width of the SBs.

Applying a negative V_g beyond the threshold voltage ($|V_g| > V_t$) and keeping $V_{ds} = 0$ inversion would take place within the active region and outside of the depletion width of the Schottky S/D contacts as seen in Fig. 5.3 b). In contrast to the conventional MOSFET, the p-channel or inversion layer would be separated from the S/D contacts by the SBs for holes, ϕ_{Bp}. An application of $V_{ds} < 0$ would allow a net hole current flow towards the drain electrode by thermionic emission over the source potential barrier as seen in Fig. 5.3 c). In contrast, the electron current from drain to source can be neglected due to the significantly higher barrier at the conduction band, which is ϕ_{Bn} plus the band bending according to the surface potential at inversion.

Adjusting V_g >0 under the same source-drain bias would bend the band bands downwards giving n accumulation as shown in Fig. 5.3 d). Now hole injection is inhibited by the large barrier at the valence band. A smaller barrier is given for electrons in contrast to the case with V_g <0, enabling a certain degree of electron injection. The electron current flow in the latter case is smaller than for the hole current in the case of inversion (Fig. 5.3 c). Nevertheless, the current flow which corresponds to the off-state of the device can be substantial if ϕ_{Bn} is not high enough. The corresponding subthreshold characteristic of this device is depicted schematically in Fig. 5.3 e) The phenomenon of turning-on of a transistor for both V_g >0 and V_g <0 is known as *ambipolarity*. A transistor which only turns on at one polarity of V_g is called *unipolar*, respectively p- or n-type. The latter case is known from the conventional $p-$ and $n-$ MOSFET.

Thus, the ratio between the SB height for electrons ϕ_{Bn} and that for holes ϕ_{Bp} indirectly determines the uni- ar ambi-polarity of a SB-transistor. For instance PtSi contacts to n-type Si have ϕ_{Bn} =0.85 eV and only ϕ_{Bp} =0.25 eV for p-type Si [Sze81] and consequently give unipolar p-type behavior FETs as reported experimentally in [WST99]. For $NiSi_2$ contacts to Si, the values ϕ_{Bn}=0.66-0.75 eV and ϕ_{Bp}= 0.39-0.48 eV [OTM81] have been measured and strong ambipolar behavior has been observed in [KZZ+05] when dopant segregation is not applied. In synthesis, ambipolar behavior takes place when both the electron and hole transmission through the SBs are considerable. Whenever the transmission is substantially higher for one carrier in comparison to the other, unipolar behavior is said to take place.

Complementary devices in SOI structures have been shown down to the 20 nm gate length regime with the use of PtSi contacts for the p-type and ErSi for the n-type device [KXA+00]. An alternative method to enable n-type performance was shown by J. Knoch et. al [KZZ+05] in SOI SBFETs with NiSi S/D-contacts. Control devices exhibited the expected ambipolar behavior due to the comparable SB heights. After implantation of arsenic atoms and segregation by the lateral encroachment of the silicide, the transistors exhibited n-type behavior. This without explicit dopant activation.

5.2 The SiNW SBFET with Intruded Ni-Silicide Segments: Fabrication

The overall aim of this work is to fabricate and analyze SBFETs made of one dimensional metal/Si/metal heterostructures. The specific advantages concerning its technological implementation and the device performance are emphasized in this section.

5.2.1 Horizontal Back-Gated Geometry

Most FETs formed of one-dimensional semiconductors which have been characterized electrically up to date have been contacted with large and blunt metal source- and drain-electrodes. The simplest integration scheme consists of a horizontal geometry with a common back-gate architecture. This simple geometry was developed for the first CNT transistors [TVD98] and was successfully applied for the first NW-FETs [CDHL00], it has also shown to be very successful for the extraction of basic transport mechanisms of 1-D semiconductors. In more detail, the structures consist of 1-D semiconductors which are horizontally arranged over a common back-gate stack consisting of a conductive substrate covered with an electrically insulating layer. The

S/D contacts can either be patterned prior or posterior to the deposition of the 1-D structures.

Since the electrodes are usually blunt and substantially larger than the structure to be measured, the analysis with these scheme is constricted to the special case of a 1-D semiconductor contacted to 3-D electrodes. From the point of VLSI integration, large area contacts are unpractical. Alternatively, a nanoscale contact makes more sense to be implemented to a 1-D test-object. In contrast to the previous example, the present work focuses on the implementation of longitudinal metal/semiconductor/metal heterostructures by applying the longitudinal silicidation method presented in Sect. 4.4. Their specific contact geometry is a realistic interface between the "outer world" and the nanoscale conductor. Although these type of contacts are attractive, they have not been studied thoroughly enough up-to-date. Another disadvantage of the horizontal patterning method commonly applied, is that the metal/semiconductor interface is subject to large fluctuations between different devices. For instance the contact area and the actual contact shape after annealing is difficult to evaluate without the use of tedious characterization like TEM analysis of each sample.

5.2.2 Initial Fabrication Steps

The test-chip described in section 3.2 was designed to facilitate the fabrication of planar NWFETs with a back-gated architecture. The starting structures consist of single SiNWs bridging between two adjacent metal contacts as depicted schematically in Fig. 5.4 a). This specific NW placement is given statistically by the random NW-dispersion on the substrates. Subsequently, the NWs are then contacted with electro-less Ni as previously described in Sect. 3.3 and shown schematically in Fig. 5.4 b). Notice, that these structures exhibit an FET architecture with large blunt S/D electrodes described above in Sect. 5.2.1, whenever an oxide free SiNW/metal interface is provided. The metallurgical gate length of these FETs amounts to the distance along the NW's length (because the NW can bend) confined between two adjacent metallic electrodes, here denoted as the *initial metallurgical gate length*, L_{g0}.

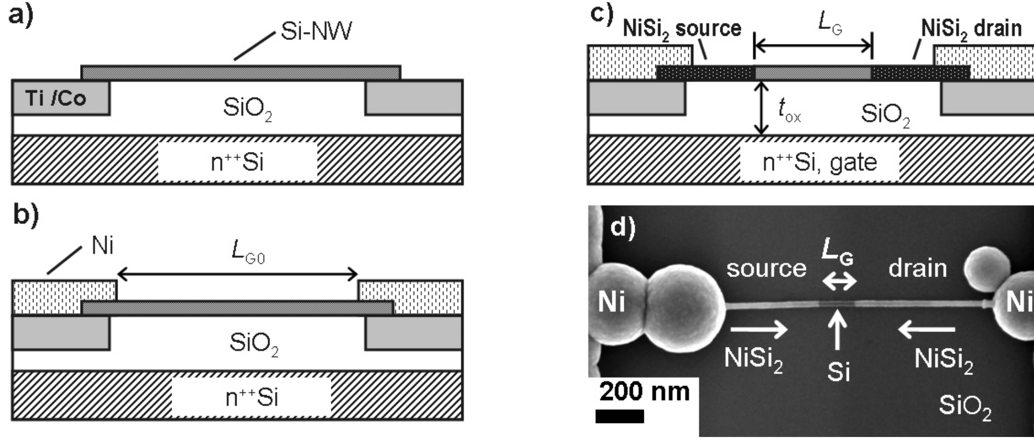


Figure 5.4: Processing steps for the fabrication of SiNW SBFETs with intruded Ni silicide contacts. a) Random dispersion of Si-NWs on pre-patterned substrates. b) Selective and self-aligned electro-less Ni deposition on Co. c) Longitudinal Ni-silicidation of the NW, leaving a pristine Si segment in between, thus creating a SBFET with reduced L_g. d) An exemplary top SEM-image of such a device with reduced metallurgical gatelength from $L_{g0} = 1.2$ µm to $L_g = 180\,\text{nm}$.

5.2.3 Self-Aligned Down-scaling of the Active Region's Length

Following the NW dispersion, the Ni-silicidation of the NW is carried out by annealing as described in Sect. 4.4.3 forcing the two silicidation fronts advance towards each other from both NW ends. When the annealing is abruptly stopped before the two silicidation fronts meet each-other, longitudinal Ni-silicide/Si/Ni-silicide NW heterostructures are formed. Figure 5.4 c) and d) shows this schematically and in a SEM micrograph respectively. This last step has important consequences on the device fabrication schemes, architecture and performance, as will be elucidated throughout the next paragraphs.

Reduction of Metallurgical Gate Length

Figure 5.5 gives a spacial impression of the device created. Practically speaking, the source and drain regions of the transistor are introduced into the NW. The direct consequence of this Ni silicide encroachment into the NW is the

reduction of the metallurgical gate-length, from initially L_{g0} to L_g. Figure 5.6 shows that the sharp silicide to Si interfaces enable the drastic reduction of the gatelength to values far below the feature size limits achievable with state-of-the-art optical lithography methods. For instance, in Fig. 5.6 a), b) the length of the Si region of a $d_{NW} = 30\,\mathrm{nm}$ and <112> oriented NW was reduced from $L_{g0} = 900\,\mathrm{nm}$ down to $L_g \sim 20\,\mathrm{nm}$. Moreover Fig. 5.6 c) shows the results for a $d_{NW} = 15\,\mathrm{nm}$ and <110> oriented NW, where the Si active region confined between the two longitudinal $NiSi_2$ segments is as short as $L_g \sim 7\,\mathrm{nm}$. The formation of such ultrashort active region lengths is extremely difficult to be achieved by common patterning methods, even with advanced electron beam lithography [Web04].

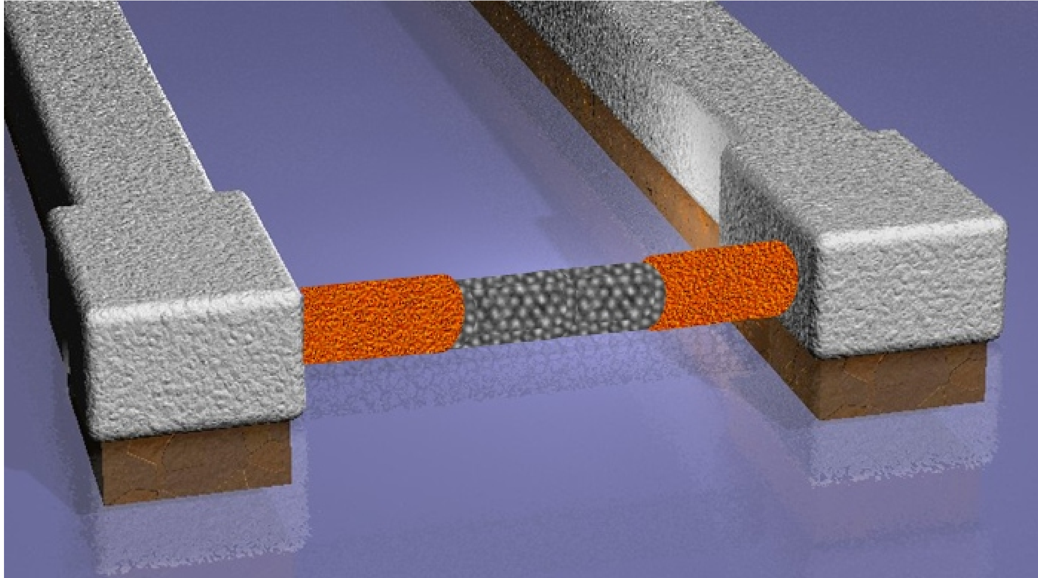


Figure 5.5: Birds-eye schematic perspective of a Si-NW FET with intruded $NiSi_2$ contacts. The S/D regions are extended into the NW shortening the metallurgical gate length. Gate control is provided by the common substrate with the stack: n^{++}-Si/SiO_2.

The main advantage of this method is its simplicity, since complex structuring steps like electron-beam lithography and anisotropic etching of a hard mask are circumvented. Access to sub-lithographic active regions can be achieved with a coarse lithography and two self-aligned and bottom-up fabrication steps: the electroless Ni deposition and and the lateral silicidation

of the NW segments. Nevertheless, it must be noted that this method is not self-limited and relies on the accurate temperature and duration control of the annealing step. This poses challenges concerning its reproducibility in a large-scale integration due to the high diffusion constant of Ni in Si and its strong dependance on d_{Si}, see Sect. 4.4.4. In the case of a horizontal implementation as in an SOI-SBFET architecture the size of the device cell will not change and substantial lithographic efforts would still be required to structure the actual gate length. However, in a vertical FET architecture this scheme is very promising.

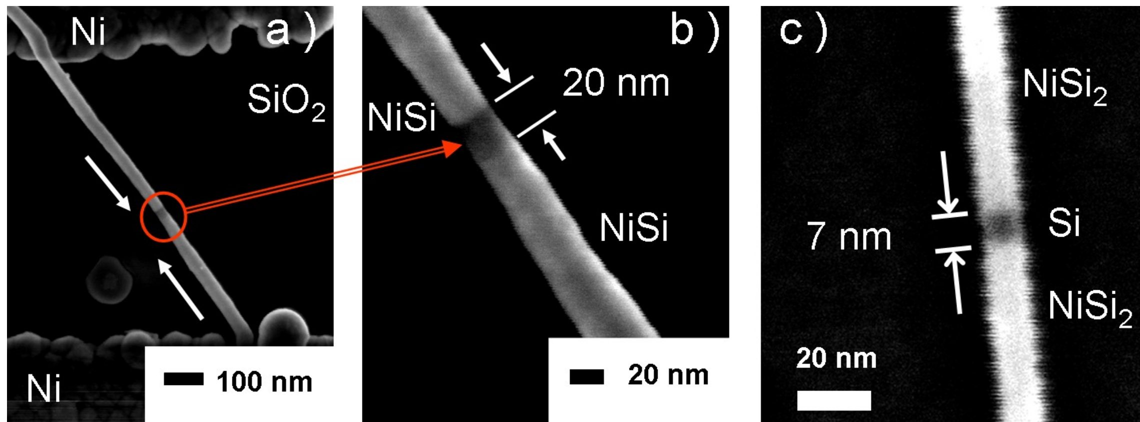


Figure 5.6: a) , b) NiSi/Si/NiSi lateral NW heterostructure with sub-lithographic active region length. The metallurgic gate length is aggressively reduced from $L_{g0} = 1\,\mu m$ to $L_g = 20\,nm$. c) $NiSi_2$/Si/$NiSi_2$ heterostructure with $L_g \sim 7\,nm$ and $d_{NW} \sim 8\,nm$.

The advantages are not restricted to the fabrication procedures but extend to device geometry related aspects. Figures 5.4 c), d) clearly show that as a consequence of the partial silicidation of the NW the Schottky junctions are now located within the NW. The SB contact changes from a large contact area between the Ni and the SiNW as seen in Fig. 5.4 a) to a nano-scale contact, Fig. 5.4 c). Moreover, the area of the Schottky contact previous to the Ni silicide encroachment is difficult to define, whereas the area posterior to the encroachment is easily defined by the NWs diameter. The reproducibility of Schottky contact areas has been reported to be one of the most critical factors in producing bulk Schottky diodes. The method developed here, facilitates the study of devices with a well known contact geometry. Furthermore,

it enables the study of quasi zero-dimensional Schottky contacts. The electrical effect of employing such nanoscale contacts will be studied in detail in Sect. 6.3.

5.3 Electrical Characteristics of SiNW SBFETs

For the electrical characterization, the following device geometric parameters are important: the final metallurgical gate length L_g; the active regions d_{Si} body thickness, i.e. d_{NW} after extracting twice the silicon oxide shell thickness; the SiO_2 gate dielectric thickness d_{ox}; the total length of the Ni silicide segments l_{NiSi} and their thickness d_{NiSi}. Most of these parameters are shown in Fig. 5.4 c) and d). Analysis with SEM was used to locate the contact pairs containing single transistor structures: single $Ni_xSi_y/Si/Ni_xSi_y$ NWs in between them. This analysis delivers L_g, d_{NW}, l_{NiSi} and d_{NiSi}.

Measurement equipment The test structures were measured in an electrostatically shielded probe station: *Suess PA 200*. Tungsten probes were used to make contact to the specified source and drain pads, whereas the common gate contact was made by placing the doped Si substrate on the metallic sample holder. The measurements were performed in a semiconductor characterization system *Keithley 4200* with the use of low-noise tri-axial cables. For all measurements, unless explicitly stated differently, the drain contact was connected to a source measurement unit (SMU) equipped with a pre-amplifier *Keithley 4200 PA* capable of measuring currents down to 1 fA in a noise range of 10 fA. The source contact was forced to the common potential and the gate contact was connected to an extra SMU with a measuring accuracy of 1 pA at a noise level of 1 pA.

Measurement schemes For measuring the *transfer characteristic* of the devices, a source to drain bias V_{ds}=V_d was forced at the drain electrode. At the same time the gate potential V_g, also in reference to source, was swept between equidistant positive and negative values. V_g was swept in two directions at a particular sweep rate in mV/s to detect hysteresis effects. The maximal absolute values of V_g were limited depending on d_{ox} to prevent oxide-breakdown. Simultaneously the drain current I_d as well as the gate leakage current I_g were measured. The semi-logarithmic representation of the transfer characteristic is commonly named *subthreshold characteristic* because it allows to observe the off-current behavior bellow the threshold

voltage. For the *output characteristics*, I_d was measured while sweeping V_{ds} for constant V_g values as a parameter.

Typical electrical results for SiNW SBFETs with thick d_{ox} will be shown first. The transistor depicted in Fig. 5.7 a) is analyzed, its electrical characteristics are representative for all SiNW SBFETs with a comparable geometry. The effects of the geometric scaling are complex and will be dealt in separate chapters. The SiNW SBFET device under test (DUT) shown in Fig. 5.7 a) has $d_{ox} = 300\,\text{nm}$ of SiH_4 plasma deposited SiO_2, a gate length reduced to $L_g = 1.3$ µm and $d_{NW} = 25$ nm. The corresponding SiNW was grown on SiO_2 substrates and is consequently most probably oriented in the $< 112 >$ direction. Accordingly, the silicide NW segments most probably have the NiSi stoichiometry. Next, its subthreshold and output characteristics will be analyzed and several properties will be listed below.

5.3.1 Subthreshold Characteristics

Polarity The subthreshold characteristic is shown in Fig. 5.7 b). The arrows show the direction of the V_g sweep. Since $I_d < 0$, $|I_d|$ is plotted in a half logarithmic scale. The transistor exhibits the highest $|I_d|$ towards more negative V_g and shows the lowest values for positive V_g values. Interestingly, $|I_d|$ does not increase substantially towards more positive V_g indicating a strong *unipolar p-type* behavior of the FET. This is unexpected, because the SiNW is nominally undoped and because the SB heights for both electrons and holes at the NiSi/Si junctions are comparable as seen in Table 4.1. A detailed investigation of the polarity behavior is given in Sections 6.3 and 7.2.

On- and Off-states Next it can be observed, that I_d saturates fairly well at 1.2 µA for $V_g < 0$. The I_d saturation is a clear sign of a sufficient electric gate-field ξ_{gate} penetration into the active region, giving a *full-depletion* throughout the entire NW thickness [TN98]. This saturation region corresponds to the on-state of the transistor, thus the *on-current* of the device is I_{on}= 1.2 µA and consequently the on-conductance G_{on}=1.2 µS. This translates into a high on-state current density, J_{on}=$I_{on}/(\pi d_{NW}^2/4)$ =0.25 MA/cm^2. In contrast the minimal I_{sd} values range from 80 fA to 300 fA for V_g >0. This range is denoted as the off-state with the *off-current* I_{off}. Accordingly, on/off ratio I_{on}/I_{off} reaches the high value of up to 10^7.

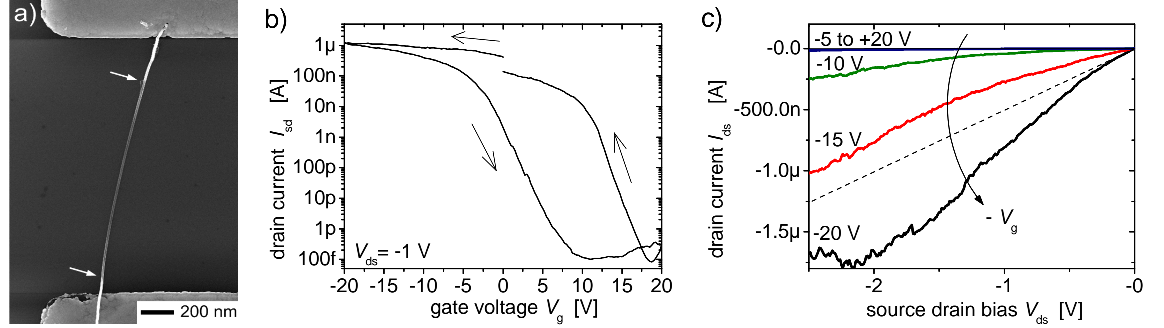


Figure 5.7: Electric characteristics of a Si-NW SBFET with L_g= 1.3 µm, d_{NW} = 25 nm and d_{ox} = 300 nm. a, SEM image of the device, the arrows point at the $NiSi_2$/Si metallurgic interfaces. b, Subthreshold $|I_d|(V_g)$ characteristic at V_{ds}=-1 V. Arrows indicate the V_g sweep direction starting from 0 V. c, Output characteristic $I_d(V_{ds}, V_g)$, V_g varies from -20 V to 20 V in 5 V steps

Hysteresis The next clear attribute is the shift of the entire characteristic in the V_g scale, when sweeping back V_g. Hysteresis shifts the threshold voltage V_t of the device so that an explicit assignment of the voltage range of the on- and off- states is not given. In fact this effect is expected, because the NWs were not passivated and charge traps can charge and shift the effective ξ_{gate}. A detailed study on hysteresis is presented in Sect. 6.1.

Subthreshold slope An important figure of merit is the *inverse subthreshold slope* S, which is defined as the inverse of the mean-slope at the region where the transition between the on- and off- states take place in the half-logarithmic $|I_d|(V_g)$ plot. Its unit is mV/dec with "dec" meaning the decade of current. The lowest S is limited thermodynamically to $S \sim \frac{kT}{e} ln(10)$ which amounts approximately to 60 mV/dec at room temperature [Sze81]. This parameter gives a value for the effectiveness of the gate control over the active region and is an indicator of the power consumption of the device while switching. Due to the very thick d_{ox}, S has a high value: 1.44 V/dec. Nevertheless, the high I_{on}/I_{off} and the almost perfect I_d saturation for $V_g < 0$ show a very effective electrostatic control of the gate over I_d. This effect is particularly intriguing considering the simple back gate architecture of the device with a low contact area between the gate stack and the active region, resembling a cylinder on a plate.

5.3.2 Output Characteristics

The corresponding output characteristics $I_d(V_{ds})$ of the transistor depicted in Fig. 5.7 a) is plotted in Fig. 5.7 c) for $V_{ds} < 0$, as a parameter V_g is varied from +20 V to -20 V in 5 V steps.

Enhancement mode The output characteristics corroborate, that the transistor has a *p*-type behavior, i.e. it turns on for V_g <0 and exhibits negligible currents for V_g >0. Moreover, it can be observed that the device works as a normally-off or *enhancement-mode* FET, since its practically off at V_g =0. This information could not be obtained from the $I_d(V_g)$ curve because of hysteresis. Note, that sweeping back V_{ds} only causes a negligible hysteresis in the output characteristics. Most charge traps are expected to be located in the amorphous Si-oxide shell, where ξ is substantially stronger for typically applied V_g values than for the V_{ds} ones due to geometrical reasons.

Signature of Schottky contacts At low negative V_{ds} values (within the triode region) $|I_d|$ increases exponentially, the dashed line in Fig. 5.7 c) serves as a guide to the eye. This would be an atypical feature FETs with ohmic contacts, where the behavior is linear. The parabolic-like $I_d(V_{ds})$ dependence is a clear sign of the presence of a potential barrier across the band structure of the device and is evidence of the Schottky S/D contacts. Note the exponential dependence of the thermionic emission current from V in Equation 5.15. Also note, that the exponential regime in Fig. 5.7 c) is dependent on V_g which wouldn't either be the case for a classical MOSFET with ohmic contacts. This will be analyzed further in Sec. 6.4.

Saturation region Independently, the output characteristics start to saturate at high $-V_{ds}$, especially for high $-V_g$. The noise level at saturation is very high, which is also a representative characteristic of most measured SiNW devices. The strong ambient sensitivity, related to the high surface to volume ration of quasi one-dimensional structures can be accounted for $1/f$-noise [RBSI+06, Jon06].

General SiNW SBFET characteristics

Summarizing the main observations of both the subthreshold and output characteristics of SiNW SBFETs measured in ambient conditions it can be said that for comparable device geometries the devices show:

- Unipolar p-type FET in enhancement-mode.

- Hysteresis.
- High on-current densities J_{on} for a SBFET.
- High and I_{on}/I_{off}.
- Efficient gate control through back gate structure.

It should be emphasized that these conclusions are based on the result of numerous devices meausured and by no means only represent a single SBFET. Also, no difference was observed between <112> and <110> oriented SiNWs even when having a comparable diameter. The good device performance and characteristic properties are somewhat unexpected, because previously published SBFETs made of intrinsic NWs only showed a poor performance [BTF05]. The effect of important device variables will be studied carefully and in detail in Sect. 5.3.3 and in chapter 6 to understand the working principle of the SiNW SBFET. With the help of the geometrical scaling behavior of the devices as well as simple electrostatic calculations and temperature dependent measurements the transport properties will be analyzed.

5.3.3 High Performance SiNW-SBFETs

The effect of the scaling of the gate dielectric thickness d_{ox} will be briefly investigated. The enhancement of the electric gate-field ξ_{gate} applied at the FETs active region is the first step in analyzing and improving the NWFETs. Thus, the implementation of a higher quality of SiO_2 as well as a thinner d_{ox} is studied. The SiH_4-plasma SiO_2 with d_{ox} =300 nm implemented in the previous examples is substituted by a high quality SiO_2 of different thicknesses, grown by wet thermal-oxidation. Thinner d_{ox} effectively reduces the magnitude of V_g required for operation and accordingly decreases the inverse subthreshold slope S. Figure 5.8 a) depicts a SiNW SBFET with d_{ox} = 20 nm of thermally grown SiO_2, a gate length reduced to L_g = 595 nm and a <110> oriented SiNW as the channel with a diameter of d_{NW} = 23 nm. In this case the S/D regions are made form $NiSi_2$ NW segments.

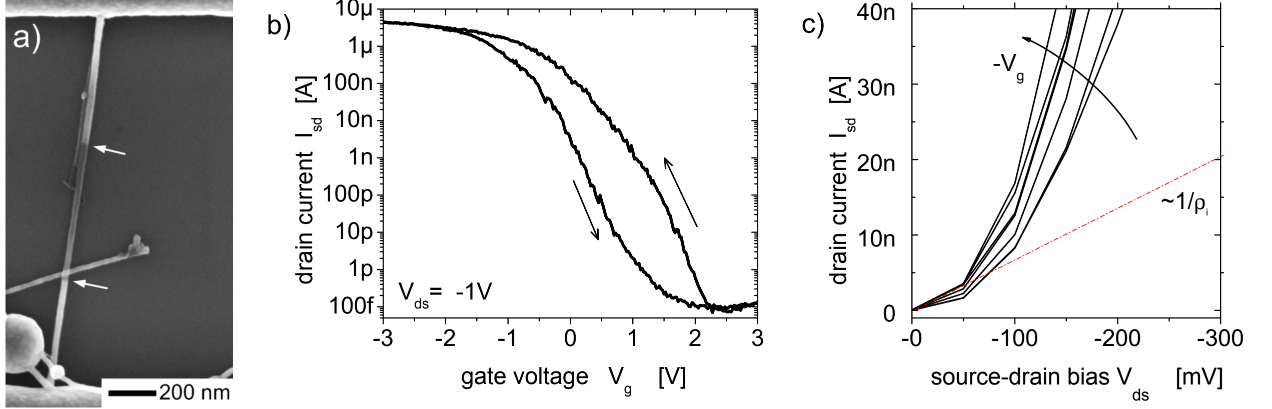


Figure 5.8: Electric characteristics of a SiNW SBFET with L_g= 595 nm, d_{NW} = 23 nm and d_{ox} = 20 nm as seen in a). The arrows point at the $NiSi_2$/Si metallurgic interfaces. Note that the NW crossing on top of the FETs active region has no electrical effect, since it is not connected to any electrode. Also there is no current flow between the NWs, because they are electrically isolated by their native oxide. b) Subthreshold $|I_d|(V_g)$ characteristic at V_{ds}=-1 V. Arrows indicate the V_g sweep direction starting from +3 V. c) Output characteristic $|I_d|(V_{ds}, V_g)$ for low V_{ds}, V_g varies from 0 V to -3 V in 0.5 V steps. The slope of the dashed line is inversely proportional to the specific contact resistivity for V_g =-3 V.

Subthreshold and output characteristics The subthreshold characteristic is seen in Fig. 5.8 b) and the output curves are shown in Fig. 5.8 c) for low $-V_{ds}$ values. Basically the main attribute reported previously for the SiNW SBFET with d_{ox}=300 nm in Fig. 5.3 b) and c) are maintained. The higher quality and thinner thermal gate Si-oxide in fact reduces the required V_g for the device operation. Consequently, as seen in the subthreshold characteristic S is improved to 249 mv/dec. The major improvement is the enhanced on-current as seen in Fig. 5.8 b). For V_{ds} =-1 V, and -2.7 V> V_g >-3 V, I_{on} exhibits a mean value 4.5 µA and a peak value of 4.7 µA, consequently the mean on-conductance is G_{on} =4.5 µS. Concurrently, I_{off} is kept as low as 81 fA, with a mean value of 106 fA for 2.7 V< V_g <3 V. I_{off} therefore seems to be limited by the resolution of the measurement equipment. Accordingly, the mean J_{on}=1.1 MA/cm^2. Assuming a Si native oxide thickness of 1.5 nm surrounding the SiNW, as observed in the TEM images (see Fig. 2.21), the actual J_{on} would amount up to the outstanding value of

1.4 MA/cm^2.

Despite the simple device back gated geometry, the device depicted in Fig. 5.8 a) exhibits a high device performance comparable to state-of-the-art FETs and multi-gate FETs. A comprehensive comparison is therefore given in section 5.3.4 to benchmark the SiNW SBFETs fabricated and characterized here.

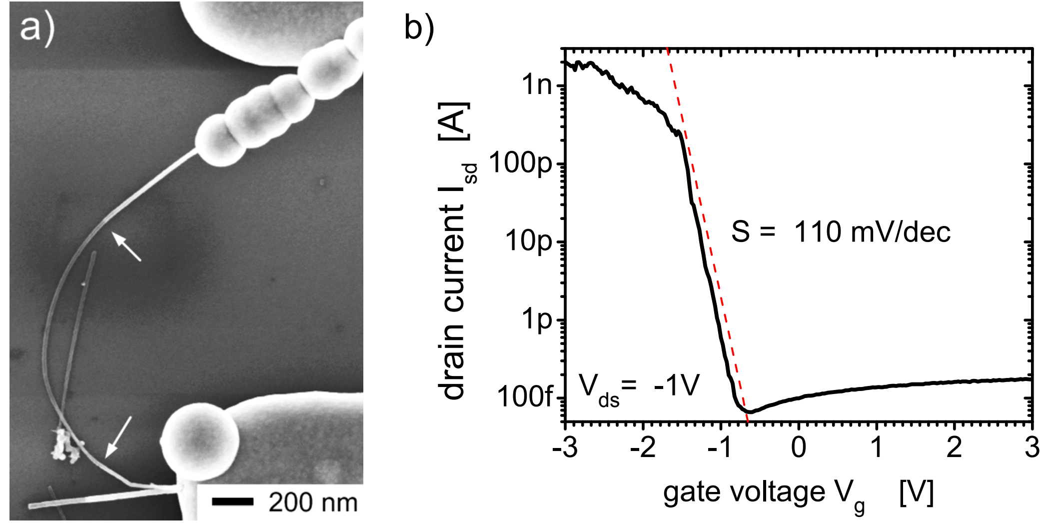


Figure 5.9: Electric characteristics of a SiNW SBFET with L_g= 1.4 µm, d_{NW} = 16 nm and d_{ox} = 18 nm as seen in a). The arrows point at the $NiSi_2$/Si metallurgic interfaces. The NW crossing the device NW is not expected to influence the behavior of this device. b) Subthreshold $|I_d|(V_g)$ characteristic at V_{ds}=-1 V. Arrows indicate the V_g sweep direction starting from +3 V.

Back gate devices with S= 110 mV/dec A further reduction of d_{ox} down to 18 nm by etching down the gate oxide with BHF prior to the SiNW deposition leads to an S as low as 110 mV/dec as seen in the subthreshold characteristic, Fig. 5.9 b). This device, depicted in Fig. 5.9 a) has L_g= 1.4 µm built from a <110> oriented SiNW d_{NW} = 16 nm. The saturation current I_{on} =2 nA for V_{ds} =-1 V is relatively low in comparison to the previous SiNW FETs, because L_g is substantially longer and unconventional L_g scaling effects take place in these devices that will discussed later in Sect. 6.2.2. Another possible reason is the large curvature of the NW, stress or piezo electrical effects could impact the saturation current.

Ultimately S can be improved by using thinner d_{ox} and/or introducing high-κ gate dielectrics. Applying a multi-gated architecture and even better wrap-around or surround-gate device geometry is expected to decrease S down to the limit of 60 mV/dec at T=300 K. The improved electrostatics would also increase the total current flow in the on-state.

5.3.4 Benchmark

Table 5.1 compares numerous electrical parameters of various state-of-the-art FETs and SBFETs extracted from $I - V$ characteristics reported in literature. The devices selected are state-of-the-art FETs built from doped and undoped SiNWs, III-V and Ge/Si core/shell-NW, as well as novel FETs, e.g. as strained SOI devices and FinFETs. This work demonstrates the highest J_{on} and G_{on} for catalytically grown and intrinsic SiNWs. In the work of Lu, Lieber et al. [LXT+05] where Ni-silicide contacts are also used the current density of such SiNWs does not saturate and could even reach higher values. The best doped SiNW devices have higher J_{on} values [CZW+03, WXY+04] however, these are within the same order of magnitude as the ones presented here. FinFETs exhibit comparable J_{on} values for a similar cross-section [RLK+04b] and L_g but larger J_{on} values for shorter devices [RLK+04a]. Their inherent advantages are their ohmic contacts and the increased channel coupling given by their double gate architecture.

Higher current-densities can be achieved with materials of higher mobility, and when no potential barrier is formed. For instance in Ge/Si core/shell NWs the Ge-core's E_v is significantly higher than the one from the Si shell, so that the holes are confined inside the Ge-core [XLH+06]. In the case of CNTs [SGU+05] E_F of the contact can be aligned to E_v for instance by using a particular CNT diameter and Pd as contacts. Accordingly $\phi_{Bn} \sim 0$. CNT-FETs with Schottky contacts typically have a comparable G_{on} with our SiNW SBFETs [SLD+03]. Nearly ideal S-values can be achieved with advanced geometries as FinFETs [RLK+04a] and strained SOI devices with high-κ dielectrics [BPA+07]. However, significantly steeper subthreshold slopes have been shown in [BHS+07] by impact-ionization, in *p-i-n* NWs at reverse bias.

Numerous strategies are applied in literature to evaluate nanoscale transistors. These are often trimmed to show particular advantages of the devices. In order to compare the device performance for low power and high performance applications, Robert Chau from *Intel Corp.* proposed a benchmark method in [CCD+05].

Table 5.1 Comparison of SiNW SBFETs with state-of-the-art FETs

work	this work	Byon	Cui 2000	Lu	Apenzeller iedm06	Wu	Cui 2003
reference	-	[BTF05]	[CDHL00]	[LXT+05]	[AAK+06]	[WXY+04]	[CZW+03]
active region	*i*-Si NW	*i*-Si NW	*i*-Si NW	*i*-Si NW	*i*-Si NW	*p*-Si NW	*p*-Si NW
geometry	BG --	BG --	BG --	BG --	DG --	BG --	BG --
dielectric/ d_{ox}/ EOT	SiO_2/ 20nm	Si_3N_4/ 100 nm	SiO_2/600 nm	SiO_2/50 nm	SiO_2/5 nmTG, 100nmBG	SiO_2/600 nm	SiO_2/600 nm
L_g [µm]	0.60	-	-	1	0.5	3	0.8-2
d_{NW}[nm] cross-section	23	10 *	70	20	30-90	30	10-20
I_d sat	yes	no	no	no	yes	yes	yes
I_{on} [µA/µm]	**196**	6.5	0.013	18.5	4.4-13.4	190	**200-400**
J_{on} [A/cm²]	**1.08M**	41k	23	0.1M	0.1M-12.6k	0.81 M	1-5M
G_{on} [S]	**4.5µ**	22n	0.9n	0.4µ	0.9µ	1.9µ	4.0µ
V_{ds} [V]	-1	-1	-1	-1	0.9	-3	-1
I_{on}/I_{off}	10^7	-	-	-	10^7	-	-
S [mV/dec]	249				140		
contact: material	$NiSi_2$	Ti/Au	Al/ Au	NiSi	Ni_2Si	NiSi	Ti/Au
behavior	SB	SB	SB	SB	SB	SB	SB

work	Gold-berger	Björk		Koo	Rös-ner	Rösner	Barral IEDM07	Xiang	Seidel
reference	[GHF+06]	[BHS+07]		[KEL+05]	[PLK+04b]	[PLK+04a]	[BPA+07]	[XLH+06]	[SGU+05]
active region	*i*-Si NW	*pin*-SiNW		*p*-Si SOI-NW	*i*-Si Fin-FET	*p*-Si Fin-FET	Si Strain SOI	Ge/Sicore/ shell	SW-CNT
		FET	I-MOS						
geometry	**SG |**	**SG |**		BG --	Fin--	Fin --	SOI--	TG --	BG --
dielectric/ d_{ox}/ EOT	SiO_2/ ~30-40 nm	SiO_2/ PECVD 25nm		SiO_2/100 nm	SiO_2/ 3nm	SiO_2/3 nm	**HfO_2/1.7nm eot**	HfO_2/4 nm	SiO_2/12 nm
L_g [µm]	1.0-1.5	1.0		28	1	0.080	**0.030**	0.190	**0.018**
d_{NW}[nm] cross-section	20-30	60		(50× 60) nm^2	(20× 50) nm^2	(20× 45) nm^2	10µm × 9.1nm	14.6/ 1.7	1.5 *
I_d sat	yes	yes	yes	yes	yes	yes	yes	yes	yes
I_{on} [µA/µm]	1.3-0.5	10.6	5.3	5.8	40	284	350	**5055**	**10330**
J_{on} [A/cm²]	7-16k	71k	35.1k	12 k	0.4 M	3.2 M		**40 M**	**877 M**
G_{on} [S]	0.8µ	2.0µ	0.2µ	0.4µ	3.3µ	23.7µ		**9.1µ**	**38.8µ**
V_{ds} [V]	-1.25	+1	-4.5	-1	-1.2	-1.2	-1.2	-1	-0.4
I_{on}/I_{off}	10^6	10^4	10^4	10^7	10^6	**10^8**	10^7	10^4	10^7
S [mV/dec]	120		**5**				75	100	
contact: material	Si/metal	n-Si/ Ni		Ti/Au	p^{++} Si	p^{++} Si	p^{++} GeSi	Si/ NiSi/GeSi	Pd
behavior	O /SB	SB		SB	O	O	O	O	O

Basically, the operation voltages are defined in function of the operating voltage V_{dd}. In this case V_{dd} is chosen to be -1 V, since V_{ds} =-1 V. The operating interval for V_g is here proposed to be V_{dd} =1 V. The threshold voltage is defined at the V_g where the peak transconductance occurs then, i.e. V_t =0.3V. I_{on} is then defined to be located at $V_g = V_t - 2/3V_{dd} \sim$ -0.36 V. Analogous, I_{off} is defined at $V_g = V_t + 1/3V_{dd} \sim 0.64$ V. Correspondingly, I_{on} =0.21 µA and I_{off} = 0.18 nA, which reduces I_{on}/I_{off} to three orders of magnitude. The use of thinner gate oxides or dielectrics with higher κ-values and somewhat higher V_{dd} should enable characteristics optimized to the operation voltages.

5.4 Conclusions

Throughout this chapter the fabrication and electrical characteristics of SBFETs built from Ni_xSi_y/Si/Ni_xSi_y NW heterostructures were demonstrated. In particular, this work was the first to show the formation of nanoscale active region lengths in NWs starting from coarsely patterned structures. L_gs as small as 7 nm starting form structures with a typical size of 1 µm could be fabricated by only employing two self-aligned steps. The SBFETs fabricated, show high performance: unipolar p-type characteristics, total $I_{on}/I_{off} > 10^7$ and record $J_{on} > 1\,MA^2$ and $G_{on} > 4.5$ S for undoped SiNWs. The characteristics show good electrostatic control as shown by the good saturation and low S down to 110 mV/dec. This, despite a relatively thick d_{ox} of 18 nm and simple back gated architecture only yielding a small contact area between the active region and the gate stack. A comprehensive transport study follows in chapter 6.

Chapter 6

Scaling and Transport of SiNW SBFETs

The previous chapter showed that the subthreshold and output characteristics of typical SiNW transistors are indeed promising for electrical applications. Some attributes of their electrical behavior are surprising and demand a deeper understanding of the underlying transport mechanisms. The present chapter focuses on the systematic study of the transport properties of SiNW SBFETs. Geometric scaling and simple calculations are used to study the observed transport phenomena. The first effect to be explained is the hysteresis observed in the I_d-V_g curves. The following analysis will deal with the charge carrier transport mechanism in SiNW SBFETs. The scaling behavior in dependence of the gate length and nanowire diameter is investigated to reveal information on the transport properties of these NW devices. They will underline the transition from *bulky* 3-D to quasi 1-D nanoscale devices. The scaling investigation should not be confused with a study of the scaling *rules* for the ultimate performance of SiNW SBFETs.

6.1 Combined Study on Hysteresis

Hysteresis in the subthreshold characteristics is an expected phenomena which is principally a well known behavior in FETs lacking of passivation of trap states in the oxide. Recent studies on nanotubes and nanowires have studied the effect of Hysteresis [SRR06, RPR05]. The Si active region of the FETs studied here is covered with a thin natural or native Si-oxide coating, as it was detailed in Sect.2.7. Within this amorphous layer and at its interface to the Si charge traps are expected to be located. Moreover, in the SiNW FETs studied here, Ni and Au are present during front-end processing

and could introduce ionic fixed charges. By applying an electrical gate potential the traps can be charged and remain charged after returning to V_g =0 for a specific amount of time called the retention time t_r. In case that V_g is reapplied within t_r, the actually applied electric gate field ξ_{gate} at the active region and contacts will be changed by the trapped charges.

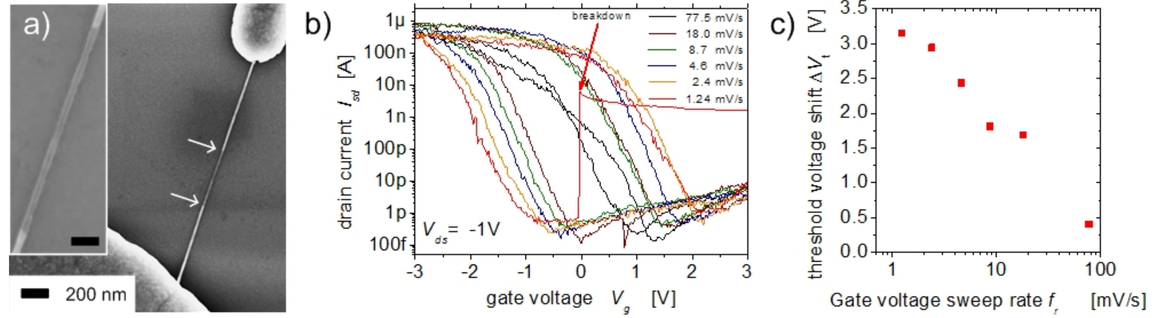


Figure 6.1: Sweep rate dependent hysteresis of SiNW-SBFETs. The device with L_g= 430 nm, d_{NW} = 11 nm and d_{ox} = 18 nm is seen in a). The arrows point at the $NiSi_2$/Si metallurgic interfaces. The inset shows a magnified view of the active region, scale bar is 50 nm. b) Subthreshold characteristic at V_{ds}=-1 V for different f_s ranging between 1.24 to 77.5 mV/s. The arrows indicate the V_g sweep direction starting from +3 V. c) Extracted ΔV_t for different f_s showing an exponential behavior. The hysteresis approaches zero for f_s >100/s.

Measurements To study the hysteresis mechanisms a combined study encompassing electrical measurements and finite element simulations was performed. $I_d - V_g$ measurements were performed at different different V_g sweep rates (f_s). Figure 6.1 a) shows the studied device with the following dimensions: L_g = 430 nm, d_{NW} = 11 nm and d_{ox} = 18 nm. The hysteresis increase for lower f_s, i.e. slower sweeping rates, can be clearly observed in Fig. 6.1 b). If the threshold voltage V_t is defined at the peak transconductance, the V_t shift between the forward and backward sweep is ΔV_t. The extracted ΔV_t values are plotted in dependance f_s in Fig. 6.1 c). The dependance is exponential with a characteristic decay length of 17 mV/s. For f_s > 77.5 mV/s the hysteresis is minimal, as seen in Fig. 6.1 b). According to the trend in Fig. 6.1 c) hysteresis should disappear for f_s >100 mV/s. The charge-traps can therefore be categorized as *slow* ones. Note, that for f_s <<1 mV/s ΔV_t needs to saturate, because of the fixed V_g span applied.

Drift-diffusion simulation The simulations were performed in the framework of a diploma-thesis by Zied Fahem [Fah06]. These considered a 2-D geometry to simplify the calculations. The transistor of Fig. 6.1 was modeled. First, charge traps at the Si/SiO_2 interface were considered. In particular, the type of traps, their energy distance to E_c or E_v and their density can be used to describe hysteresis. To explain the V_t shift towards more positive V_g >0 acceptor-like interface traps, i.e. which trap electrons, located near E_c are required. Analogous, the V_t shift towards more negative values for V_g <0 can be described by donor-like traps, i.e. trapped holes located near E_c. The trap density gives the total charge and therefore the maximal V_t shift. Specifically, the characteristic of Fig. 6.1 taken at f_s=2.4 mV/s was fitted.

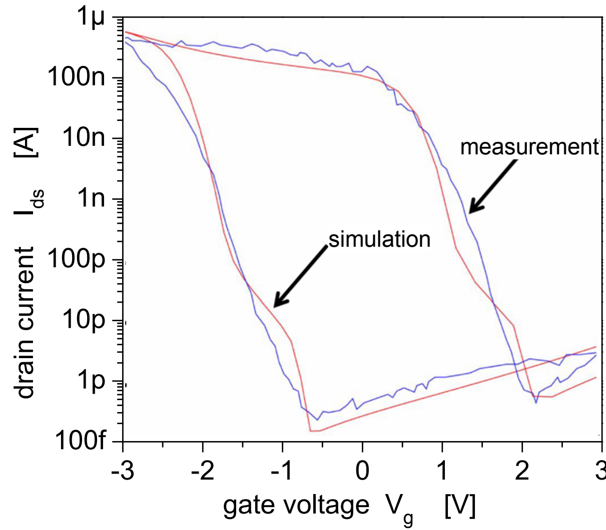


Figure 6.2: Subthreshold characteristic as measured and calculated by drift-diffusion simulation. The device from Fig. 6.1 is considered for V_{ds} =-1 V and f_s=2.4 mV/s. Charge trapping parameters were tuned to fit the curves. Simulation from [Fah06].

The result with the best agreement between the calculated and measured curves was obtained by assuming diffused Au atoms on the NWs surface. It is well known that Au creates deep trap states in Si: donor like at 0.54 eV and acceptor like at 0.35 eV away from E_c and E_v respectively [Sze85]. Assuming an equal trap area- density for both states of: 1.7×10^{12} cm^{-2} as well as for a small capture cross-section of 10^{-27} cm^2, the fit seen in Fig. see Fig. 6.2 was

obtained. Additional fitting parameters as the Schottky barrier heights were employed to describe the current levels and the ascribed unipolar behavior. As they do not affect hysteresis, these will be discussed in Sect. 6.4. In fact numerous studies have proven that Au can diffuse during NW growth on the NWs surface. This preferentially occurs on UHV-CVD growth of SiNWs. In contrast, in LPCVD growth like the one performed here the Si-oxide shell formed readily during growth effectively hinders Au diffusion [KTRR06].

6.1.1 Hysteresis Prevention

Provided that the charge traps are given by dangling bonds at the Si/SiO_2 interface and defects inside the oxide layer, hysteresis can be prevented by appropriate passivation. One kind of passivation could be the growth of a high quality thermal SiO_2 covering the Si active region as applied in today's CMOS manufacturing [WMF96], [Pau94] [Sze81]. A subsequent annealing treatment in forming gas is required to saturate the dangling bonds with hydrogen atoms. Since both, the thermal oxidation and the annealing are high temperature processes, some process modifications should be made to implement this in the NWs used here. Unreacted Ni at the contacts needs to be removed prior to annealing to prevent further NW silicidation.

6.2 Effect of Length Scaling

In this section the transport behavior in SiNW SBFETs is studied by comparing various transistors with different L_g. This is of paramount importance, since the scaling behavior of transistors gives important information on the transport properties and is a key issue in device integration.

Common resistivity measurement setups The most common method used to determine the intrinsic resistance of materials is a four-point measurement [Sch98]. However, in this case the intrinsic conductance of undoped SiNWs is at the limit or even below the measurement resolution available here, as can be seen in Figs. 5.7 b) and 5.9 b) in the off-state. Note that the shift from V_t shift caused by hysteresis as discussed in Sect. 6.1. The resistivity can only be extracted when the transistor is in the on-state, i.e. at $V_g < V_t < 0$ Gated four-point measurements have been often used to characterize semiconductors. Nevertheless, in this case such a measurement scheme would not give the intrinsic SiNW resistivity, since additional band bending would be introduced at the inner contacts and thus the measurement would be corrupted. Moreover, the Ni silicide contacts are highly intrusive

and would distort transport. The best setup to measure the intrinsic resistivity of the SiNW FETs would be a to apply a transmission-line-method (TLM) [Sch98], ensuring that no intruded contacts are present in between the measuring leads.

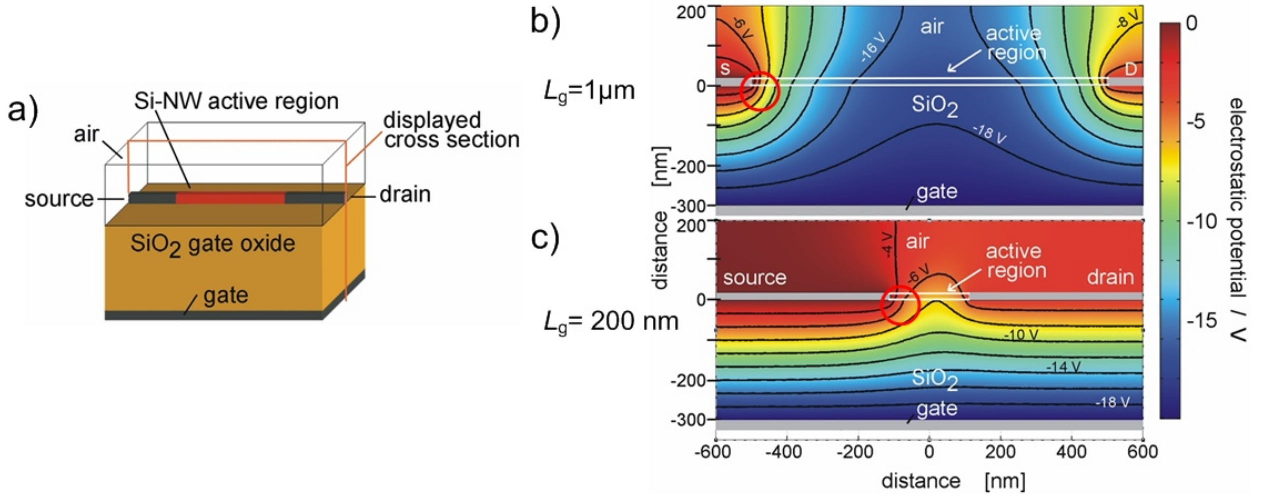


Figure 6.3: Electric field distribution in SiNW-SBFETs of different L_g. a) Geometry considered for the 3-D Poisson calculation. b), c) Cross-section through device showing the electric potential contours. In the transistor with L_g =1 µm b) ξ_{gate} penetrates into the active region more effectively than for the L_g =200 nm device b). The coupling from V_g to the S/D contacts is also higher, see red circles.

Comparison method One possible implementation of the TLM method would be to measure a SiNW-SBFET with short Ni silicide intrusions as S/D-contacts. After this, the sample would be re-annealed to continue the silicide intrusion, reducing L_g and the device would be measured again. Repeating this sequence numerous times the data for varying L_g can be compared until the source- and drain-electrodes reach each other. This experiment could not be performed successfully because of the fast diffusion rate of Ni into the SiNWs and flat heating ramps available, see Sect. 4.4.4. Also, it cannot be discarded that an accumulative annealing of a SiNW can change its electrical characteristics, regarding its surface trap density and possible distribution of interstitially located atoms. An alternative method similar to the TLM is proposed and applied here. It encompasses the comparison of different

SiNW-FETs with different L_g under the following premises. First, the SiNW synthesis and device fabrication are performed under the same conditions for all devices to be compared. Second, the NW diameter d_{NW} should be constant. The later premise ensures the decoupling between the Schottky contacts and their size, which are strongly dependent as will be shown below in Sect. 6.3. The SBFETs compared below are formed by <112> oriented SiNWs, i.e. they have Ni_2Si contacts. A relatively thick SiH_4 plasma oxide of d_{ox} = 300 nm was used, because it was the only one available when the experiment was performed.

6.2.1 Selection of Comparable Device Geometries

The next important constrain for the L_g dependent comparison is to guarantee sufficient ξ_{gate} penetration into the channel region and contacts. Ultimately, this will depend on the *competition* between the electric field between the S/D-contacts ξ_{sd} and ξ_{gate}. The selection of the appropriate device geometries suitable to be compared was performed by calculating the ξ distribution of devices with varying L_g. Specifically, the question to solve is how near to each other the S/D-electrodes can be located, or in other words how short can L_g be, so that ξ_{sd} does not *shield* ξ_{gate}, ensuring the gate control over the device. The finite element calculations were performed by solving Poisson's equation in three dimensions. More details on these type of simulations and the importance of considering the 3-D geometry will be given in Sect. 6.4.2. Transistors with varying L_g and a constant NW-diameter d_{NW} of 20 nm were calculated for the on-state, i.e. with V_g = -20 V and V_{ds} = -3 V to ensure I_d saturation. The considered device geometry is depicted in Fig. 6.3 a).

Electric gate field coupling Figures 6.3 b), c) visualize the resulting potential landscape through the cross-section of the devices with L_g=1 µm and 210 nm respectively. For the L_g =1 µm long device (Fig. 6.3 b), there is a good coupling of ξ_{gate} to the channel and contact regions. In contrast the relatively strong ξ_{sd} in the L_g = 210 nm SBFET (Fig. 6.3 c) reduces the penetration of ξ_{gate} into the active region, thus the gate control over the channel is diminished. In addition, the equipotential lines near the Schottky contacts are denser for the long device than for the short one, as highlighted inside the circled region. Thus, the ξ_{gate} acting on the SBs is lower for short devices. The transmission through these SBs is expected to be lower, since the lower gate field gives a lower band bending at the contacts and a broader SB-width, an important effect discussed in Sect. 5.1.2. Further simulations show that the gate coupling to the contacts and active region is practically lost for devices with L_g <200 nm. This is a direct result of the very thick

d_{ox} used. The bottom of the line is, that a length dependent study can be compared fairly for devices with d_{ox} = 300 nm whenever L_g >200 nm.

6.2.2 L_g Dependent Comparison of SiNW SBFETs

Given this electrostatic constriction, SiNW SBFETs with a constant diameter d_{NW} =21 nm +/- 1 nm are compared for varying gate length L_g ranging between 210 nm and 8.5 µm. Figure 6.4 a) shows the subthreshold characteristics of four different SiNW SBFETs with this geometry. The SBFETs compared were processed under the same conditions as discussed previously and measured in the same way: biased at V_{ds}=-1 V and V_g varied from -20 V to 20 V. The V_g interval where the I_d saturation takes place is reproduced in Fig. 6.4 b) for the backward V_g sweep. All curves show a perfect saturation behavior, even for the *short* device with L_g =210 nm. This fact experimentally confirms that for devices as short as L_g =200 nm ξ_{gate} still penetrates into the active region, as calculated in Sect. 6.2.1.

A very remarkable characteristic is that the I_d saturation values for the 210 nm and 1 µm long devices are practically identical, i.e. constant at I_{on} = 1 µA even if L_g differs by almost a factor of five. Interestingly, the 2.5 µm long SiNW SBFET does show saturation at a lower I_{on} of approximately 100 nA, i.e. one order of magnitude below the two previous devices. Surprisingly, doubling L_g to a value of 5 µm leads to a drop in I_{on} by more than four orders of magnitude. Evidently the behavior of I_{on} vs. L_g is non-linear. To deepen the study of this unexpected behavior even more SiNW SBFETs with a comparable diameter of d_{NW}=21 nm +/-2 nm were analyzed as well. The results of their I_d saturation values are summarized in dependence of L_g in Figs. 6.4 c), d). Figure 6.4 c) (black squares) shows the representation in a full-logarithmic plot and Fig. 6.4 d) in a semi-logarithmic one. It can be observed clearly in Fig. 6.4 c) that within the regime of L_g <1 µm, the saturation current is independent of L_g for constant d_{NW}. However, for SBFETs with L_g >1 µm, I_{on} is supra-linearly reduced over several orders of magnitude.

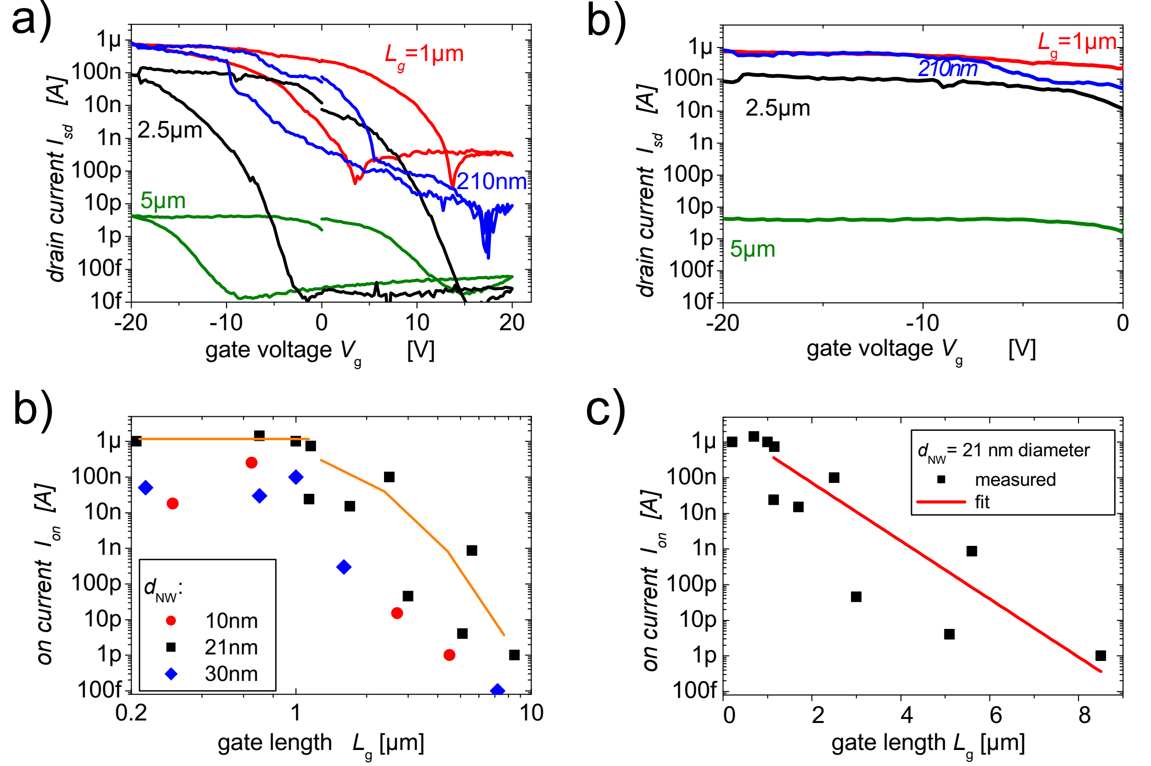


Figure 6.4: L_g dependent comparison of SiNW SBFETs for constant d_{NW}. a) Subthreshold characteristics of transistors with different L_g but same d_{NW} =21 nm and d_{ox} =300 nm for V_{ds}=-1 V. b) Close look to the saturation region of curves in a). The perfect saturation for all devices shows, that ξ_{gate} steers the devices effectively as predicted in Fig. 6.3. c) Extracted I_{on} in dependence of L_g for constat d_{NW}, logarithmic plot. For L_g <1 µm, I_{on} is constant. d) Half-logarithmic representation showing exponential decay of I_{on} for L_g >1 µm.

Additional data was gathered for SiNW SBFETs with other mean NW thickness: d_{NW} =10 nm and 30 nm, both within a total d_{NW} tolerance of +/- 2 nm. The results are included in Fig. 6.4 c) as red dots and blue rhomboids. Evidently, these transistors follow the same behavior sub-divided in two L_g regimes. Two main aspects of the gate-length dependence of the on-current need to be discussed, namely its invariance for short gate lengths and the rapid decrease for long ones.

6.2.3 Limited I_{on} for $L_g <$ 1 µm

The fact that the conductance is essentially constant for $L_g < 1$ µm can be explained by the presence of Schottky contacts. The hypothesis is that the Schottky contacts dominate the resistance and that the current modulation in these short SBFETs is simply given by the carrier injection through the SBs. This implies that the channel conductance $G_{channel}$ is substantially higher than the conductance through both Schottky contacts G_{SB} and consequently the total conductance of the device in the on-state G_{on} practically is given by the conductance through the Schottky contacts:

$$\mathrm{G}_{channel} \gg G_{SB} \quad (6.1)$$

$$\mathrm{G}_{SB} \approx G_{on} = I_{on}/U_{ds} = 1\,\mu\mathrm{S}. \quad (6.2)$$

Current limiting by Schottky Contacts To support this idea, the corresponding output characteristics of the SiNW-SBFETs are also analyzed. Figure 6.5 compares the characteristics of two devices with constant d_{NW} =21 nm and different L_g: below and above 1 µm. For the output characteristics of devices shorter than L_g =1 µm, e.g. L_g=210 nm in Fig. 6.5 a) the operating point (V_{ds} =-1 V and V_g =-20 V) is located within the exponential region, confirming that the transport is dominated by the Schottky contacts. Rising V_{ds} to higher negative values in fact leads to the saturation of the curve without actually entering a *linear triode region*. This means, that the actual channel resistance is not measured, because it is simply overshadowed by the resistance of the Schottky contacts. Note, that the series resistances from each of the Ni-silicide segments plus the Ni connectors is typically around 160 Ω(6.25 mS) and can therefore be neglected as the limiting factor of I_d. Alternative explanations of the constant I_{on} currents, such as an insufficient gate coupling to the channel due to the screening by ξ_{ds} as mentioned above for shorter transistors than L_g 200 nm can be ruled out, because there is a clear current saturation in the $|I_d| - V_g$ characteristics as seen in Fig. 6.4 b).

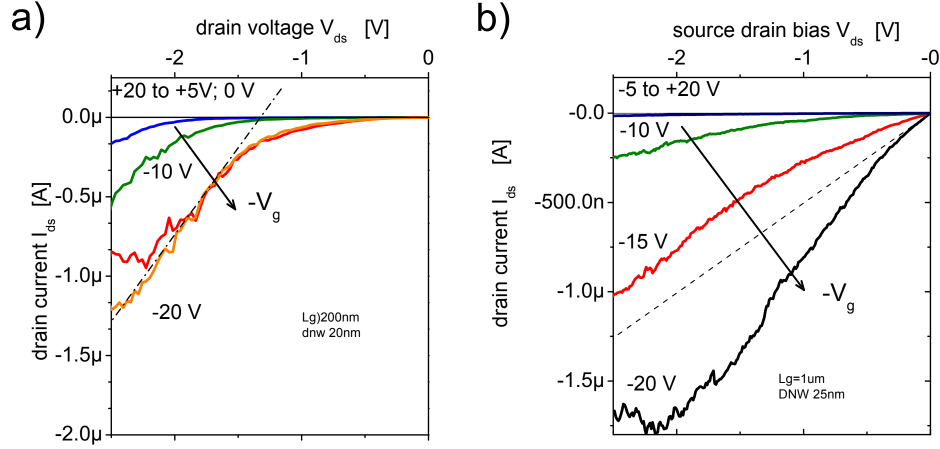


Figure 6.5: Comparison of output characteristics of SiNW SBFETs with different L_g and same d_{NW} =21 nm. a) Transistor with L_g =210 nm. For V_g=-20 V, the characteristic changes from the exponential behavior for low negative V_{ds} onto the saturation region, for higher negative V_{ds}. b) Device with L_g =1 µm

6.2.4 Exponential Decay of I_{on} for $L_g > 1$ µm

The other important feature in the I_{on} vs. L_g dependence is the supra-linear decrease of I_{on} for L_g >1 µm. This occurs despite the fact that the longer L_g is, the better the coupling between ξ_{gate} and the contacts regions is, see Sect. 6.2.1. Therefore, the total resistance increase can be attributed to an increase in the channel resistance. As the resistance of the NW channel increases with increasing length, e.g. due to hole scattering, it will eventually dominate the total transistors conductance. This state appears to be reached for L_g =1 µm. The output characteristics of devices with L_g >1 µm taken at $V_{ds=}$-1 V and V_g =-20 V (e.g. the SBFET in Fig. 6.5 b) with L_g =1.3 µm) are located inside the linear region. This fact shows that transport is now primarily controlled by the channel and not by the Schottky contacts.

In contrast to the linear decrease that is expected for ohmic behavior, I_{on} drops roughly exponentially with increasing V_g. In the case of the SiNW SBFETs with d_{NW} =21 nm, I_{on} is fitted for L_g >1 µm by a first-order exponential decay with a characteristic decay length L_c of around 530 nm. This

behavior is visualized by the red line in the semi-logarithmic plot seen in Fig. 6.4 d).

Anderson Localization

Similar exponential resistance increase dependent on the length have been observed earlier in metallic and semiconducting CNTs as well as in amorphous semiconductors. In these cases, it has been attributed to *Anderson localization* effects [And58]. Localization describes the state where the amplitude of the wave function ψ is *localized* at a certain position. This is in contrast to a perfectly ordered and periodic system, where the wave function is evenly spread along the entire lattice, and can be described by Bloch-functions [Kit66]. In systems, which do not exhibit periodically placed scattering centers, i.e. disordered systems, ψ can be scattered at various defects so that a closed loop can be formed. Within the closed loop, ψ propagates in both directions with the same change in phase. Wherever this loop gives constructive interference, ψ is said to be localized [Dat97]. As a consequence, the amplitude of ψ, $|\psi|^2$, exhibits a local maximum and decays to its surroundings. A perquisite for localization is that ψ with a wavelength λ scatters within the coherence length l_c, i.e. $2\pi \cdot l_c < \lambda$ [IR60], known as the Ioffe criterium.

Strong- vs. weak-localization Basically two different types of localization regimes can be categorized depending on the systems length L in reference to the localization length L_c. When L of a phase-coherent system is comparable to L_c, the system is described as *strongly localized*. The basic characteristic of strongly localized systems is its limited conductance G to $2e^2/h \approx 80$ µS, where h is Planck's constant. Further, the conductors G does not scale linearly with L but rather decays exponentially [Dat97]. Also, large G fluctuations are observed, when λ varies or if different scattering configurations take place. For the regime, where $L >> L_c$, the conductor is said to exhibit *weak localization*. In contrast to the strong localization, G can be higher than $2e^2/h$, but can still exhibit strong G fluctuations $\sim 2e^2/h$ when quantum interference takes place especially in low-dimensional systems like NWs. A special feature of weak localization is that a magnetic field is able to *destroy* the phase coherent interference and accordingly the loss in G. It is important to mention, that most localization effects are observed at low temperatures and under low bias conditions where electron-phonon scattering does not break phase coherence [cRS].

Discussion Returning to the observations in this work the question arises, whether the observed exponential decay trend between I_{on} and L_g can be attributed to localization effects. To answer this question with more certainty further measurements would be required, for instance at low temperatures and/or under the presence of a strong magnetic field. Nevertheless, due to technological limitations these measurements could not be performed here. Assuming localization effects, a classification in weak or strong localization would be necessary. The G limitation criteria cannot be applied here, because the Schottky contacts limit the total G to 1 µS, far below the strong localization limit of 80 µS. Assuming localization, the characteristic exponential decay length of 530 nm would be approximately equal to L_c. In this case the system would be strongly localized, since L_g >1 µm. Strong localization would also explain the large data scattering specially, because each SiNW exhibits a different disorder distribution. This assumption is to be considered carefully, because of the large bias and V_{ds}=-1 V and the measurements at T =300 K. However, localization effects have been recently reported in metallic multi-walled CNTs, where the disorder has been induced by ion irradiation [GNdPGH+05]. The localization length observed there amounts to approximately 600 nm.

Localization in SiNWs *Disorder* mechanisms are usually responsible for localization effects. Principally, defects, diameter or strain variations along the SiNWs length can introduce the required disorder for localization to take place. Also trapped charges at the NWs surface or SiNW / oxide interface could enhance elastic scattering, leading to such transport behavior. Recently, several groups have performed theoretical studies on the impact of disorder mechanisms in SiNWs. A. Lherbier, S. Roche at al. [LPN+08] have studied the effects of surface roughness in [100] oriented SiNW with d_{NW}= 3 nm. They employ an atomistic approach by combining the the Kubo-Greenwood approach with the Landauer-Büttiker formalism, enabling the calculation of structures with a large amount of atoms (10^5) and giving a direct access on the mobility. In this case electron-phonon scattering was suppressed, i.e. T =0 K. The results show, that a small roughness can lead to localization in SiNWs. Another study using the Kubo-Greenwood formalism was published by Troels Markussen, Antti-Pekka Jauho et al. [MRBJ06]. They analyze two different disorder scenarios: Hydrogen-passivated SiNWs with randomly placed H-vacancies and unpassivated surface reconstructed SiNWs with bulk disorder. For the last ones they report, that transport switches from ohmic onto localization behavior, when their length surpasses 200 nm. Yet another group from Stanford University, studied localization

in SiNWs, see Alexei Svizhenko and Kyeongjae Cho [SLC07]. They made use of the non-equilibrium Green's function formalism, studying [110], [111] and [100] oriented SiNWs integrated as transistors. As in [LPN+08] they study the effect of surface roughness. Their results lead to localization and to the exponential decay of the saturation currents of the SiNW FETs for $L_g > 200$ nm. Due to the large similarity of their results with the experimental results shown here, their I_{on} vs. L_g behavior for [110] oriented SiNWs is reprinted from [SLC07] in Fig. 6.6. Interestingly, an I_{on} saturation at 1 µA is also observed for devices with L_g <200 nm. However, in contrast to our work no Schottky contacts were applied here. When introducing electron-phonon coupling the curve starts rising until linear scaling behavior is reached as expected for Ohmic behavior [Cho07]. This group is currently working on the effects of strain variation as a source of disorder in SiNWs [Cho07], where they also observe localization effects.

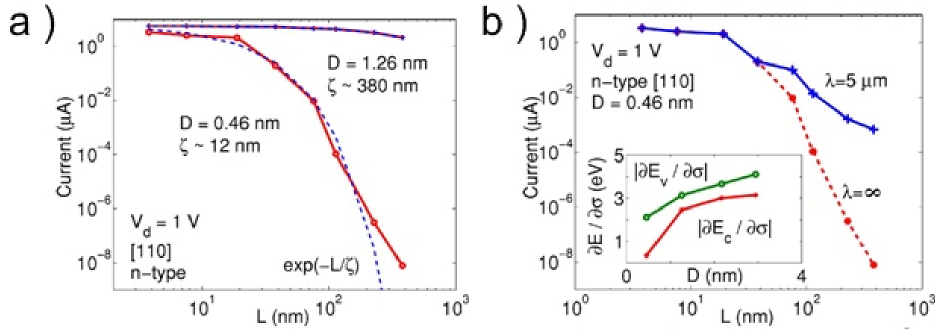


Figure 6.6: Calculated localization in SiNW FETs with different L_g. The drain saturation currents (I_{on}) are plotted vs. L_g. Note the high similarity with the experimental results in Fig. 6.2 c). The curve is constant for short L_g and drops exponentially for L_g >200 nm. From [SLC07].

These calculations show, that SiNWs can exhibit localization effects under the premise, that electron-phonon scattering is low or even suppressed. However, at a temperature of T=300 K, i.e. the one used for the experiments, the strong electron-phonon interaction is expected to break the phase coherence. Consequently, no localization effects should be observed. Nevertheless, in small scale structures as in CNTs it has been proven, that electron-phonon scattering can be suppressed due to confinement effects as proposed by Hiroyuki Sakaki. The NWs measured here range between d_{NW} =10-30 nm, where such a radial confinement would not be expected. However, the SiNWs

used grown on SiO_2 can exhibit micro-twining every couple of monolayers as observed in the TEM image in Fig.2.20. Under the careful assumption that electronic transport would be confined within this thin region, that is if quantum-interference takes place inside these micro-twins, electron-phonon scattering could principally be suppressed, and localization effects would be measurable even at room temperature. This is difficult to proof, because there is not yet much information available on the actual atomic order within this region. For instance, recently it has been observed that Au atoms are located within the twining planes inside SiNWs [HAP+08, AHP+08]. This intriguing abnormal behavior still requires future studies and preferentially a transport study decoupled from the Schottky contacts.

6.3 Effect of Diameter Scaling.

The next geometric device-parameter to be studied in terms of its scaling impact on transport is the SiNWs diameter d_{NW}. Very often the advantages of the electronic transport in NWs are emphasized, but a systematic study showing the transition between the "bulk limit" and the low-dimensional one has been missing so far. The present study, is the first to show this transition in the specific example of SBFETs. This study is also interesting from the point of view of the classical enhancement of nano-FET performance. Analogous to the down-scaling of the top-Si thickness d_{Si} of SOI FETs, a smaller d_{NW} is expected to provide a stronger electric field coupling between the gate and the channel, enhancing the device performance [TN98]. Besides from this device related issue, these experiments enable the investigation of the scaling behavior of the Schottky contact area, an experimental study which has been missing so far at least in the nano-scale regime. The procedure is simple, because d_{NW} straightly yields the area of the Schottky contacts.

6.3.1 Characteristics of SiNW SBFETs with thick NW diameters

Figure 6.7 shows the subthreshold characteristic of a SiNW-SBFET device made of a thick SiNW: d_{NW}=60 nm, i.e. a substantially thicker NW than the devices analyzed previously in Fig. 5.3 b) and 5.8 b). Analyzing this curve for negative V_g reveals that much higher absolute values are needed to saturate I_d in comparison to the device in Fig. 5.3 b), even though they have an equivalent d_{ox}. Evidently thicker NWs require a higher V_g than thinner ones for a more effective electric gate field penetration. This is analogous to a full depletion of the Si-body of SOI-FETs [TN98].

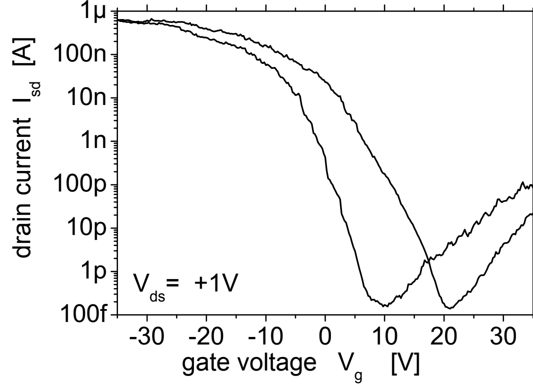


Figure 6.7: Subthreshold characteristic $|I_d| - V_g$ of d_{NW}=60 nm SiNW SBFET(at $V_{ds} = +1\,V$). L_g=900 nm and d_{ox}=300 nm. The device is ambipolar and requires high V_g values to saturate the current.

Ambipolar behavior One peculiar dissimilarity between this characteristic and the curves of thinner NWs studied previously is noteworthy. For positive V_g, I_d rises up to three orders of magnitude above its minima. However, note that the I_d levels for $V_g > 0$ are lower than for $V_g > 0$. The substantial drain current increase or "turning-on" for both $V_g \gg 0$ and $V_g \ll 0$ clearly corresponds to the ambipolar FET behavior described previously in Sect. 5.1. Given the fact that the SB heights for electrons and holes in bulk Si/Ni-silicide contacts are both rather located near the mid-gap of Si (see Table 4.1) ambipolarity is expected, independently of the contact size. From the point of view of the device functionality I_{off} is strongly degraded, which makes SiNW SBFETs with thick SiNWs unpractical for realistic electronic applications. It must be emphasized that both, the unipolarity for thin d_{NW} and ambipolarity for thick d_{NW} is representative and reproducible for devices with similar geometries.

6.3.2 Diamater-dependent Ambipolarity

I_d saturation vs. d_{NW} To elucidate the transition between the transport properties of thick NWs and thinner ones, the diameter scaling behavior is studied systematically for NWs with d_{NW} between 10 nm and 70 nm. The SiNWs analyzed up to $d_{NW} \sim 50$ nm are all <110> oriented, i.e. nucleated

on (001)-Si substrates as shown in Sect. 2.5. NWs thicker than 50 nm could not be grown on Si. For this diameter range NWs nucleated on SiO_2 were used typically growing in <112> direction, as presented in Sect. 2.7. The analysis compares the subthreshold characteristics of SiNW SBFETs with varying d_{NW} and thus varying Schottky contact area A_{NW}. Due to the high sensibility of SiNW FETs on L_g, discussed previously in Sect. 6.2.4, only SiNW SBFETs with comparable L_gs were considered. In particular, the L_g range between 1.0 and 1.3 µm was chosen because the Schottky contacts exhibit a large contribution to the resistance of the carrier transport, as discussed previously in Sect. 6.2.3. Direct information of the impact of the SBs on the electronic transport in SiNW SBFETs is thus delivered by this comparison.

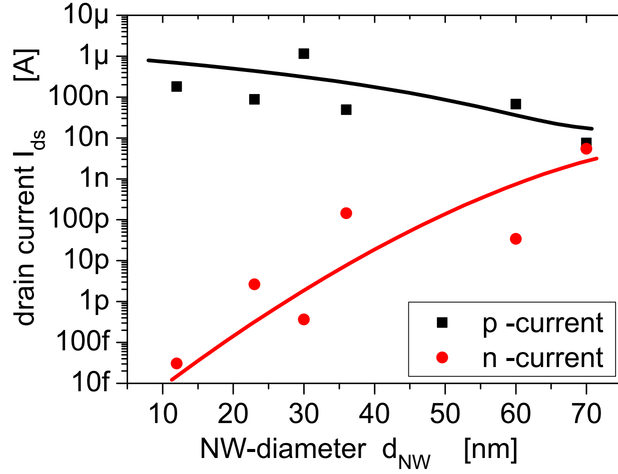


Figure 6.8: NW-diameter dependent polarity of SiNW SBFETs. The I_{ds}-saturation values of both p- and n- branches extracted from $I_{ds} - V_g$ (at $V_{ds} = -1\,V$) plots for different NW diameters d_{NW} are plotted. Only devices with comparable L_g are considered: 1.0-1.3 µm. Thin NW-SBFETs show unipolar p-type behavior, the thicker d_{NW} gets, the more the n-type current increases. A 70 nm thick device has an ambipolar behavior approximating to the bulk limit. Lines are a guide to the eye.

Steady transition between uni- and ambipolarity Figure 6.8 summarizes the results for transistors with 12 nm $< d_{NW} <$ 70 nm. Both $|I_d|$ saturation values are compared for $V_g < 0$ (black squares) and $V_g > 0$ (red dots) i.e. for the p-type and n-type branches. Starting from thin d_{NW}, unipolar p-type behavior is clearly observed. As d_{NW} increases the p-type current decreases gradually even if the cross section of the active region is larger. However, in the case of the n-type current, the $|I_d|$ saturation strongly increases with higher d_{NW} until it reaches the same order of magnitude than its corresponding p-type current. Note that the p-type current is always higher than the n-type one. The behavior for increasing d_{NW} approaches the "bulk limit" observed for Si/NiSi SBFETs.

Independence of lattice orientation For both p- and n- type currents in Fig. 6.8 the transistion is gradual, i.e. no abrupt changes are observed when the NW crystal orientation switches between <110> and <112>. The same continuous tendency is observed clearly within the d_{NW} region for each NW orientation. It should also be mentioned that NWs grown on SiO_2 as thin as 20 nm are unipolar. Therefore, the crystal orientation does not influence the behavior of Fig. 6.8. This study gives further important information. Since the NWs are grown under the same conditions and the SBFETs are processed similarly, a systematic background doping of the SBFET's active region cannot account for this effect.

Possible Explanation on Polarity Control

Possible mechanisms enabling the transition between unipolar and ambipolar behavior are discussed here.

Surface effects One important aspect to be considered when scaling down d_{NW} is the increasing surface to volume ratio. It can be easily calculated that the surface $A_{NW-surf}$ to volume V_{NW} ratio of a NW scales inversely proportional to d_{NW}. Assuming a perfectly cylindrical SiNW:

$$\frac{A_{NW-surf}}{V_{NW}} = \frac{\pi d_{NW} L_g}{\pi d_{NW}^2 L_g} = \frac{1}{d_{NW}}. \tag{6.3}$$

Thus, NWs can be increasingly sensitive to the surrounding environment for thinner NW diameters. For instance the effect of charge transfer from molecules docking at the NWs surface would be preferentially registered in thin NWs. Simultaneously, the effect of charge traps in the native oxide shell and at its interface to the Si is stronger for thinner NWs. Numerous $I-V$ measurements in N_2 and Ar showed no difference in the FETs characteristics

compared to measurements in air. Under vacuum and after desorbing H_2O molecules from the NWs surface by heating and UV irradiation, electrical measurements of thin d_{NW} SBFETs still showed unipolar p-type behavior. Thus, at the first glance the external environment does not seem to be responsible for the NWs polarity. The effect of the native oxide shell on the device polarity could not be studied due to the technological limitation of etching SiO_x selectively to $NiSi_2$, i.e. 0.5% HF as well as 100:1 BHF immediately etched the $NiSi_2$ NW-segments. In the next section it is proposed that the altered SBs determine the polarity of the devices.

Impact of Schottky Contacts on Polarity As mentioned above, an unintentional doping of the active regions can be ruled out almost completely and a trivial coupling between the environment and the transport measurements could not be found. A possible model to explain this effect would be given by the introduction of an internal energy barrier which would be tunable indirectly by d_{NW}. At a certain d_{NW} the barrier could hinder the carrier transport of one kind, while allowing the other carrier to be transmitted more effectively. This would be the case of a SBFET with asymmetric Schottky barrier heights previously discussed in Sect. 5.1.1. Principally, if the effective Schottky barrier heights are displaced when d_{NW} is scaled, for whatever mechanism to be defined below, a change in polarity would be possible. This model could also explain, why the p-type current even drops for thicker d_{NW}.

First, it is possible that due to the small number of atoms at the contact quantum mechanics can behave differently than in bulk or large area contacts, e.g. the Bloch functions. Second, the circumference to area ratio of the Schottky contact is approximately inversely proportional to d_{NW}. Consequently, from the total amount of atoms forming the Schottky contact the fraction that is in contact to the native oxide is significant in thin NWs. The Schottky contacts of thin NWs are more sensitive to the outer Si bonds as well to its surroundings. The third mechanism is of pure electrostatic nature, the Schottky contacts of thinner NWs experience stronger electric fields than that of thicker NWs. This is specially enhanced by the special geometry of the SiNW-SBFETs made of metalsemiconductormetal heterostructures. Under the premise that the SBs are the limiting factor in these devices, which is expected for this L_g-range, the impact of the SBs on the charge carrier transport can be assessed. This analysis and the search for the possible reasons accounting for this behavior will be carried out in the following section.

6.4 Nanoscale Schottky Contacts

Most of the remarkable electrical characteristics of the SBFETs still require to be explained. Specifically, an answer has to be given to the following phenomena observed in devices with thin d_{NW}: high current densities in the on-state, unipolar p-type behavior and fairly steep subthreshold slopes by only using a gate with a minimal contact area to the active region. In this section it is proposed that the used device geometry facilitates an effective coupling of the gate electrode to the Schottky contacts, thus giving a possible answer to the questions stated above. The argumentations will be based on the previous geometry dependent studies.

6.4.1 Specific Contact Resistivity

The electrical characteristics studied in Sect. 5.3 give important insight on the electronic transport through the Schottky contacts. A close look at the output characteristic in Fig. 5.8 c), shows an exponential behavior of I_d near $V_{ds} = 0$ as V_{ds} decreases. This behavior is a clear signature of the Schottky barriers located at the S/D contacts as discussed in Sect. 5.1.2 and described by Equation 5.15. Given the fact that this SBFET has $L_g < 1\,\mu\text{m}$, transport is assumed to be limited by the Schottky contacts and not by the active region, as proposed in Sect. 6.2.3. Therefore, it is straightforward to calculate the specific contact resistance (often also called specific contact resistivity) ρ_i of its Schottky junctions, as is commonly done in Schottky diodes. This device variable is defined as the slope of the output characteristic at $V_{ds} = 0$ according to:

$$\rho_i = \frac{\delta V}{\delta J}|_{V_{ds}=0}. \tag{6.4}$$

ρ_i can be calculated for different gate potentials, in this example it is specially interesting to analyze it in the SBFETs on-state: V_g=-3 V. By taking the NWs cross-sectional area A_{NW} as the SB contact area, ρ_i=33.2 µΩ-cm^2. The line drawn in Fig. 5.8 c) has a slope inversely proportional to ρ_i. This value can be compared with usual contact resistances. Indeed it is significantly smaller than the usual Schottky contact resistances [Sze81]. This explains the high J_{on} surpassing 1 MA/cm^2. Equivalent values of ρ_i are commonly achieved, when the semiconductor at the Schottky contact is heavily or even degenerately doped. For instance a Si/NiSi$_2$ bulk contact having a ϕ_{Bp} of 0.4 eV should have a doping concentration at the contacts of $1 \times 10^{19} cm^{-3}$ to equal the ρ_i reported here [Sze81]. Such a high unintentional doping concentration in these SiNWs can be ruled out, on the one hand by the

observations of the diameter dependent polarity as explained in Sect. 6.3 and on the other hand because the doping concentration level would be too high to explain such small I_{off}.

Principally, ρ_i can be reduced strongly by thinning down the SB width in respect to its width in an intrinsic Si/$NiSi_2$ bulk contact. A local electric field is able to bend the bands of the SiNWs at the interface with the $NiSi_2$ practically thinning the SB width. By doing this, the top part of the triangularly shaped SB can be so thin that charge carriers can tunnel through it, see Sect. 5.1.2. The effective SB height ϕ_{B-eff} required for thermal emission is thus diminished. The output characteristic in Fig. 5.8 c) gives another important hint, ρ_i increases as V_g is increased towards 0 V, implying that ϕ_{B-eff} is tuned by V_g. Consequently, the carrier injection through the Schottky contact is controlled by V_g. This clearly corresponds to a widening of the SB. The effect can be regarded as a gate-field *doping* of the SBs. This is different than in conventional bulk SBFETs where the SB is not strongly affected by ξ_{gate}. In order to support the hypothesis that transport in these SiNW SBFETs is controlled by ξ_{gate}-tunable Schottky barriers and to emphasize why the applied device geometry promotes this control, the electric field distribution for different devices is analyzed below.

6.4.2 Field Enhancement at the S/D Contacts

Already in Sect. 6.2 the electric field distribution within the transistor was analyzed. Figure 6.9 compares the electric field distribution and potential of two SiNW SBFETs with equal L_g =800 nm, d_{ox} =300 nm and d_{NW} =20 nm but with different contact geometry. The device shown on the left row has the conventional NW-SBFET geometry, i.e. with large and blunt S/D electrodes, whereas the one on the right row exhibits the longitudinal heterostructure geometry applied in this work. The electric potential ($\varphi(\mathbf{x})$) was calculated in the on state: V_g =-20 V, V_d =-1 V and V_s =0 considering a three dimensional geometry and solving Poisson's equation.Figures 6.9 a) , b) show the considered geometry as well as $\varphi(\mathbf{x})$ within two cross-sections. Both planes are oriented along the NWs length, one has the vertical direction ($x - y$ plane) and the other one the horizontal one ($x - z$ plane). The color scale for φ shown on the right side ranges between -20 V and 0 V and is the same for all graphs within this Figure. The remaining graphs show planes depicting $\varphi(\mathbf{x})$ in the color scale as well as the normal projection of exemplary electric field lines onto this plane. Figures 6.9 c) and d) show a magnified region in the $x - y$ plane through the source electrode, whereas Figs. e), f) depict a magnified view of the ($y - z$) plane, i.e. perpendicular the NW, located exactly at the metallurgic metal/Si junction of the source contact.

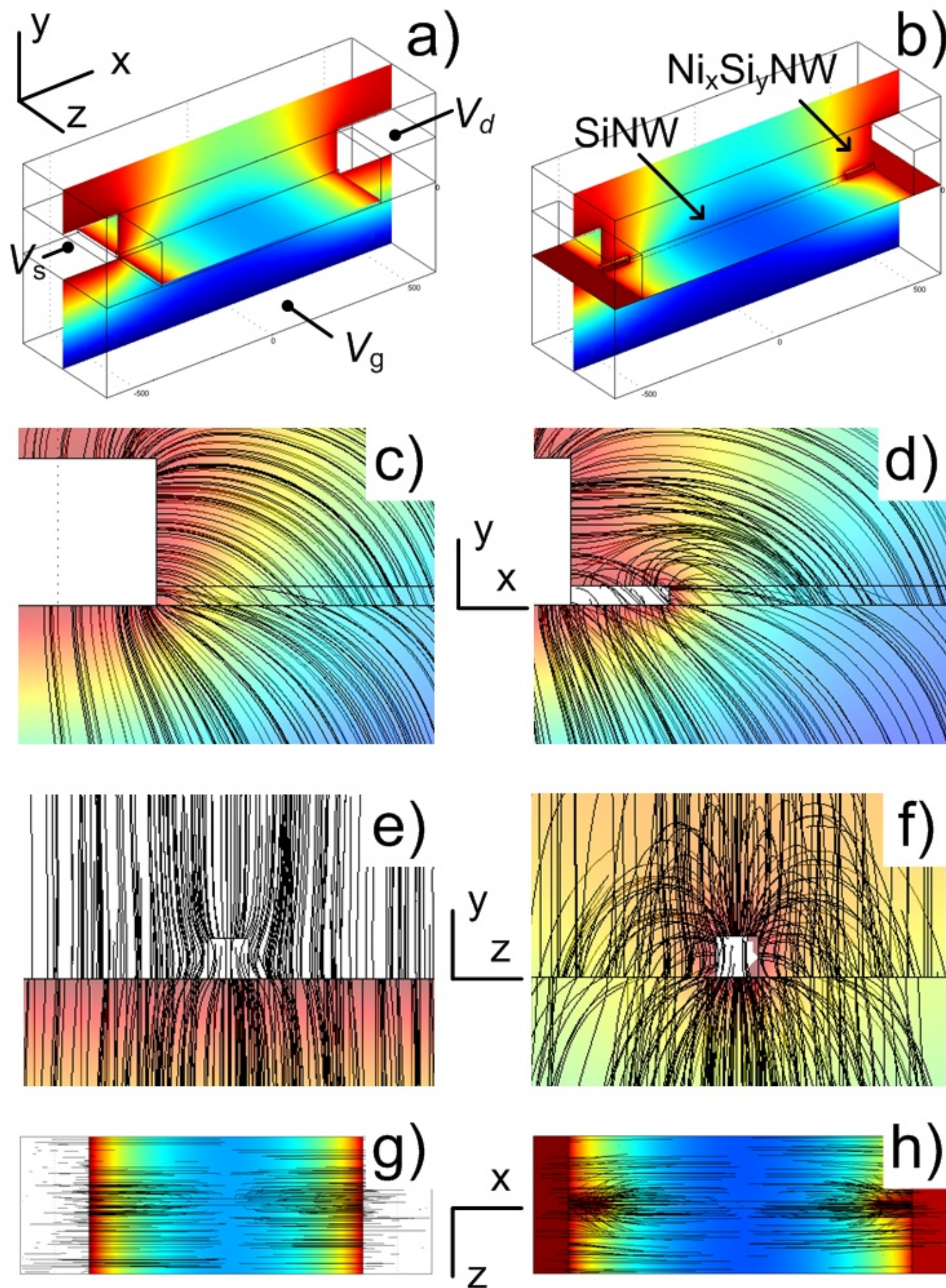


Figure 6.9: Comparison of electric potential distribution of SiNW SBFETs with different S/D electrode geometry. Both with L_g = 800 nm, d_{ox} = 300 nm and d_{NW} =20 nm. The left row has conventional S/D electrodes: blunt and large, whereas the right one exhibits the metal/Si NW heterostructure used in this work. Different planes are shown where the colors corresponds to a certain φ. For images c) to h), the black lines are the projection of the ξ lines an the displayed planes.

Figures 6.9 g) and f) show the complete $(x - z)$ plane along the NWs length at the interface between the air and SiO_2 dielectric, with both S/D electrodes. The density of field lines entering the source contact region to the NW is significantly higher for the device with intruded Ni silicide S/D electrodes. Accordingly, the gradient of φ within the SiNW, and adjacent to the source electrode is stronger for the heterostructure geometry in Fig. 6.9 d) in comparison to the one with the blunt contact in c). The images of Fig. 6.9 clearly proof that there is a significant ξ enhancement at the Schottky junctions for the metal/semiconductor longitudinal heterostructure geometry applied here. Evidently, the electric field lines bundle at the ends of the one- dimensionally shaped metallic Ni silicide electrodes due to their tip-like shape.

6.4.3 Effective Barrier Height

The electric field enhancement at the Schottky contacts by the tip-like shape of the electrodes has important consequences on the charge carrier transport through the Schottky junction. As discussed in Sect.5.1.1 charge injection through a Schottky contact consists of mainly two components, thermionic emission and thermal assisted tunneling. The dominant mechanism in bulk SBFETs typically is thermionic emission over ϕ_B. [Sze81]. In Sect. 6.4.1 the concept of the effective Schottky barrier height ϕ_{B-eff} was introduced. Alternative to the usual methods used to lower ϕ_{B-eff} like a strong doping of the contact region, sufficient band bending induced by an applied ξ can lead to a similar effect. It is therefore plausible to consider that the enhanced ξ_{gate} enabled by the S/D electrode geometry can effectively tune ϕ_{B-eff} and therefore control the current injection.

By assuming, that the limiting carrier injection mechanism is thermionic emission It must be mentioned that

Assessment of the Effective Schottky Barrier

Measurement method In order to confirm the V_g control of the carrier injection through the Schottky contacts it is helpful to quantify ϕ_{B-eff}. Amongst numerous methods, like the $C - V$, and the photoelectric measurements, ϕ_{B-eff} can be determined by an activation energy measurement which in turn is one of the most reliable methods to accomplish this.

From equation 5.15, ϕ_{Beff} can be determined easily by assuming $J_{TE} = I_d/A_{NW}$,

$$ln\frac{I_d}{T^2} = ln(A_{NW}A*) - \frac{q(\phi_{B-eff}) - V_d}{kT} \tag{6.5}$$

where $q(\phi_{B-eff}) - V_d$ is the activation energy. A great advantage of applying this method with these NWs is that the contact area is simply given by the known parameter A_{NW}. According to Equation 6.5, ϕ_{B-eff} can be extracted from the slope of the plot of $ln\frac{I_d}{T^2}$ vs. $1/T$. From the extrapolated value at $1/T = 0$, A^* can be calculated. Note that the parameter extraction must be limited to a certain T-range, usually 150 K, for A^* to be temperature independent [Sch98].

Measurement setup To extract the effective Schottky barrier height for holes (ϕ_{Bp-eff}) electrical measurements were performed for different temperatures for the device shown and characterized in Fig. 5.8. This is an ideal candidate, since L_g <1 µm, i.e. the SBs are the limiting transport factor at room temperature. To avoid possible Ni diffusion, high temperatures were avoided. The measurements were performed in a liquid N_2 cooled cryostat from *Oxford Instruments*, which was modified to measure these SiNW SBFETs. The setup, built by Florian Ponath as a master thesis, replaces the need for bonding wires to the S/D connectors, since ultrasonic boding created leakage paths through the gate oxide. The setup encompasses four high precision positioning probes steered by piezo-electromechanical manipulators from *Attocube* each with three degrees of freedom. The probe needles were fabricated from a laser-cut copper-beryllium sheet, combining low resistivity and mechanical bendability.

Measurements Prior to evacuation, reference measurements were made. The cryostat was then evacuated and H_2O molecules were desorbed from the substrate surface by heating at 150°C and illuminating with an ultraviolet-light. Subthreshold characteristics taken before and after evacuation as well as after desorption showed no difference in its current levels, unipolar p-type shape and hysteresis. As the heating of the sample was substantially slower than the cooling, the measurements were done while heating to guarantee a constant temperature for each set of measurements. Some control measurements were carried out during cooling for later comparison with the data taken while heating at the same readout T. After reaching 117 K, The measurement set applied every 5 K consisted of $I_d - V_g$ characteristics for ten established V_d values ranging between 10 mV to 2 V.

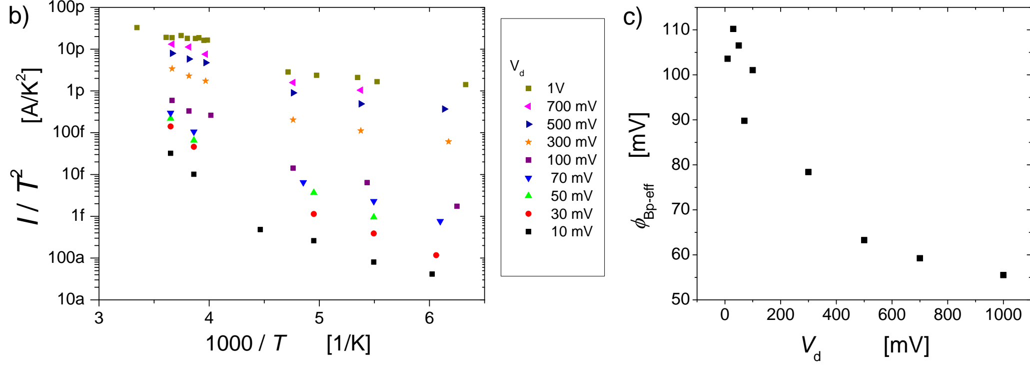


Figure 6.10: Schottky barrier height measurement by energy activation. Device measured is the one from Fig. 5.8. a) $|I_d| - V_g$ measurements at different T for $V_d = -1\,V$. b) Arrhenius plots of I_d at V_g =-3 V in dependence of $1000/T$ for different V_d. c) Extracted ϕ_{Bp-eff} for different V_d.

Parameter extraction Throughout the complete temperature range, unipolar behavior remained. As expected I_d was reduced with decreasing T as seen in the set of subthreshold curves depicted in Fig. 6.10 a). To asses the effect of V_g on I_d, Arrhenius plots were extracted from the characteristics at on-state, i.e. at V_g =-3 V, as seen in Fig. 6.10 b). Since I_d is expected to be mainly limited by thermionic emission, $I_d/T^2 \sim 1/T$ according to Equation 6.5 for a 3-D space of the carrier velocity. According to Equation 6.5 ϕ_{B-eff} for holes can be determined from the slope of the graph in Fig. 6.10 b) [Sch98]. Depending on V_d, $\phi_{Bp_{eff}}$ will range between 56 meV (V_d =-0.01 V) and 100 meV (V_d =-1 V) following the curve in Fig. 6.10 c). The exponential decrease of ϕ_{Bp-eff} with increasing V_d shows that the drain bias has a strong effect of the band bending at the Schottky junction. The Richardson constant A^* has a mean value of $7.14 \cdot 10^{-10}$.

6.4.4 The Role of Nanoscale Schottky Contacts

Tunable ϕ_{Bp-eff} with V_g At the on-state for V_g =-3 V and V_d =-1 V ϕ_{Bp-eff} = 56 meV, which is significantly lower than the values reported for junctions between thin $NiSi_2$ films and Si: 420-490 meV, see Table 4.1. The strong reduction almost by one order of magnitude can be attributed to the band bending at the Schottky junction, induced by ξ and mostly by ξ_{gate}.

Herein lies the evident advantage of the metal/semiconductor longitudinal heterostructure geometry developed here. The ξ_{gate} control over the SBs has been proposed as the dominant charge carrier transport mechanism in CNT SBFETs by S. Heinze, J. Appenzeller et al. [HTM$^+$02]. There it was already proposed to use of sharp needle-like S/D electrodes to enhance the coupling between the gate and the Schottky contact. The work done here is the first one to apply this, in the example of SiNWs. The field enhancement at the Schottky junctions, calculated in Sect. 6.4.2 is able to explain the high J_{on} and low ρ_i.

Polarity control It was proposed in Sect. 6.3 that the polarity of the SiNW-SBFETs analyzed here is simply determined by the respective ϕ_{B-eff} for electrons and holes and not by unintentional doping of the active region. Lastly, it is proposed that the local ξ at the Schottky contacts could be responsible for giving the polarity of these SiNW SBFETs. In an ideal system it would be expected that both, ϕ_{Bn} and ϕ_{Bp} are tuned by V_g in a comparable manner. Subsequently, ambipolar behavior would be expected, as in the bulk system. However in system which is not ideal, charge traps can be responsible for pinning ϕ_B at a certain level or alternatively electrostatically shift ξ at the contacts, which could lead to a unipolar behavior. The NW-diameter dependent study of $I_d - V_g$ provides meaningful evidence, to believe that pinning of the energy bands at the Schottky junction should not be actual mechanism for unipolarity, because this would be valid for thick NWs as well. In order to prove this, a strong local ξ will be applied at each Schottky contact independently to control polarity. This study will be shown next in Chapter 7.

6.5 Conclusions

Important transport properties of SiNW SBFETs were discussed throughout this chapter. With the help of geometric scaling, electrostatic and drift diffusion calculations, more insight into the charge carrier transport in these devices could be given. The effect of hysteresis in the $I_d - V_g$ characteristics was first analyzed by a combined experimental and drift diffusion study. Hysteresis takes place for V_g sweep rates slower than 77.5 mV/s, in principle the measured hysteresis can be reproduced by considering charge traps located at the Si/Si oxide interface with the energy levels of Au impurities.

The first geometry dependent study on SiNW SBFETs to be reported was performed here. First an L_g dependent study of the $I_d - V_g$ saturation currents of <112> SiNWs with constant d_{NW} shows an I_d limitation by the

Schottky contacts for $L_g < 1\,\mu m$. For longer L_g, I_d drops exponentially, an intriguing behavior which might be explained by Anderson localization effects. A diameter dependent study of SiNW SBFETs was also performed, where a steady transition from unipolar p-type conduction to ambipolar behavior is observed as d_{NW} increases. The experiments imply that the SiNWs are not systematically doped during growth or processing. Alternatively it was proposed that the ratio between ϕ_{Bn} and ϕ_{Bp} determines the device polarity.

Further, the role of the Schottky contact on the carrier transport was assessed. Electrostatic calculations confirmed that the developed SBFET geometry with intruded metallic NW electrodes enhances ξ at the Schottky contacts. It was proven by energy activation measurements that external electric potentials can switch the carrier injection between thermionic emission and tunneling consequently explaining the high I_{on}/I_{off} ratio and low ρ_i observed. An effective barrier height ϕ_{Bp-eff} was introduced to asses the transition between thermionic emission and tunneling.

Chapter 7

Polarity Control in Multi Gated SiNW SBFETs

All SiNW SBFETs studied in the previous chapters were steered by a single, common gate coupled to both, the Schottky contacts and the active region. In this chapter the design, fabrication and characterization of multi-gated devices is studied. The aim of this transistor architecture is to ensure independent coupling to each SB junction, providing additional control over the carrier injection and therefore enabling the manipulation of the device polarity.

7.1 Fabrication

The ideal geometry of a local gate on a NW, is the one which surrounds the NW over its total outer perimeter. Nevertheless, this *surround gate* architecture is difficult to realize in a horizontal NW arrangement. It is considerably simpler to place a gate stack on top of the NW. For insulators with thicknesses comparable to the NW´s diameter the top-gate electrode embraces the NW, coupling not only to its top but also to its sides. This arrangement, which is referred to as *omega gate* renders the next best effective gate coupling succeeding the surround gate. In this work, multiple omega gates are placed along the NW´s length for coupling onto different SiNW segments. Two main requirements need to be fulfilled for the top gate fabrication. The first one concerns the deposition of a thin high-κ dielectric on top of existing SBFET structures. The second deals with the fabrication and accurate placement of top gate electrodes on top of the SBs. The latter implies the use of electron beam lithography and lift-off.

7.1.1 Top Gate Dielectric

Different stringent requirements are set to the top dielectric insulator. The primary aim of the top gate stack is to provide a strong local electric field. For the top gate dielectric, this means that the thinnest possible layer thickness with the highest possible relative dielectric constant κ is needed. Simultaneously, low leakage currents through the dielectric are indispensable. The combination of these aspects readily discard SiO_2 as the choice of top dielectric. Finally, fabrication related requirements must be considered. The deposition has to be conformal to render a good step-coverage over the NW. For simplicity, the S/D Ni electrodes were retained for a later reuse in measurements. To prevent further silicide encroachment into the SiNW, the deposition and treatment temperatures have to be limited to well below 400°C according to the results in Sect. 4.4.3. Considering all these aspects, two types of dielectrics were chosen: Ta_xO_y deposited by a sol-gel method and Al_2O_3 deposited by atomic layer deposition (ALD). The deposition of both dielectrics is shortly described next.

Tantalum Oxide Sol-Gel Deposition

The sol-gel method describes the chemical transition from a liquid into a gel and finally into a solid. One great advantage of this method is its technological simplicity, since it can be deposited at low cost. Another convenience is that it can be deposited at room temperature. In the case of Ta_xO_y, the precursor solution is tantalum ethoxide $Ta(OCH_2CH_3)_5$, which at normal conditions has a liquid phase. At contact with moisture the following hydrolysis reaction takes place:

$$2Ta(OCH_2CH_3)_5 + 5H_2O \longrightarrow Ta_2O_5 + 10HOCH_2CH_3. \qquad (7.1)$$

In practical terms, the samples to be coated are dipped into the Ta ethoxide solution in an inert and H_2O-free atmosphere, then they are retrieved to react with the air moisture. First, a gel and subsequently a solid Ta_xO_y layer is formed. The deposited layer thickness per dip is mainly adjusted by the solutions viscosity. Different solvents, as dry-ethanol and toluol are used for this. The solvent´s vapor pressure determines the speed of the solution´s evaporation and indirectly the time required for hydrolysis. For large thicknesses accumulative dips were applied. The thickness was measured by ellipsometry.

Experiments of single deposition dips on hydrophillic SiO_2 surfaces only showed open layers in contrast to the deposition on unoxidized hydrophobic Si. Only after numerous dips the Ta_xO_y layer had a close form with a rather

rough topography. By pre-treating the substrate with the adhesion promoter hexamethyldisiloxane (HMDS) at 100°C under vacuum, methyl groups were attached on the SiO_2 making the surface hydrophobic. A following dip in the deposition solution showed the formation of closed Ta_xO_y layers of approximately 4 nm thickness. Following each dip annealing at 150°C was performed to evaporate remaining solvents and methyl-group molecules.

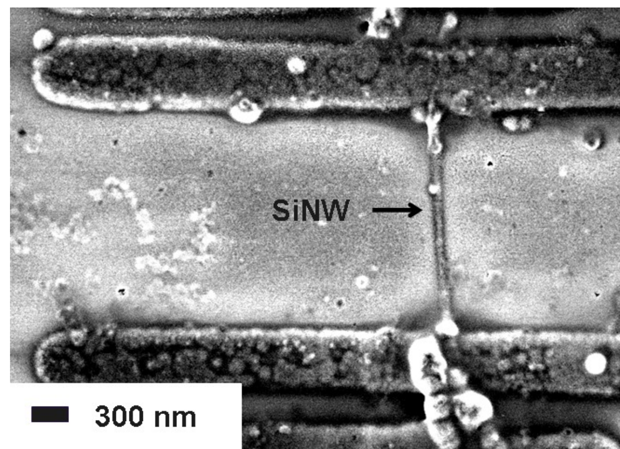


Figure 7.1: SEM image of a test structure with sol-gel deposited Ta_xO_y as a top dielectric. A good step coverage over the SiNW and silicide segments can be observed.

Figure 7.1 shows a SEM top view of a SiNW SBFET structure after the deposition of Ta_xO_y. Following the HMDS treatment the test chip was dipped ten times in a 4 mMol/l tantalum ethoxide solution diluted in ethanol, isopropanol and toluol. The image shows a good step coverage over the Si-/$NiSi_2$-NW as well as over the Ni pads.

Al_2O_3 Atomic Layer Deposition

Aluminum oxide was deposited on the structures with trimethylaluminium, $(CH_3)_3Al$, as the Al precursor by ALD. The deposition was carried out at *Instituto MDM* in Agrate, Italy. A low temperature process at 210°C was chosen to inhibit further silicidation. A total of 13 cycles were required to deposit a 20 nm thick Al_2O_3 film.

7.1.2 Top Gate Patterning

The exact FET geometry and location of the Schottky contacts was determined by electron microscopy prior to the top dielectric deposition. Electron beam lithography was used to structure the top gates as it provides flexible patterning at a high resolution. Accordingly, the top-gate electrode placement was individually fitted for each transistor structure in order to render the best electrostatic coupling possible. A *Raith 200* electron beam lithography tool was used by applying an alignment method previously described in [KDR03, Web04, WIK^{+}05] yielding an overlay accuracy of 20 nm. A double layer PMMA/MA positive electron sensitive resist was used to facilitate lift-off. The top-metal stack was deposited by standing evaporation and consisted of 15 nm Al as the adhesion layer and 35 nm of Au. Lift-off was carried out in NMP at 100°C.

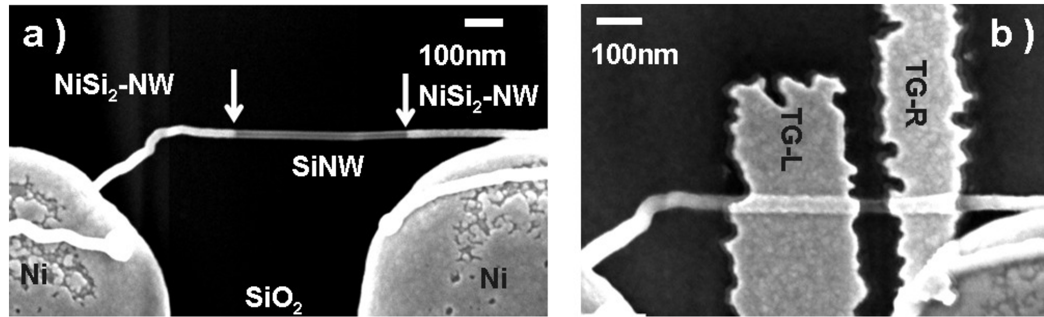


Figure 7.2: SEM images of SiNW SBFET with individually tunable SBs. a) Back gated device with $L_g = 500$ nm, $d_{ox} = 300$ nm and $d_{NW} = 20$ nm.

7.2 Local Control of Carrier Injection by Multiple Top-Gate Structures

A total number of 17 SBFETs were processed as described above to provide them with multiple top gate (TG) structures. In all cases the electrical characteristics were taken prior and posterior to the TG processing. One example is shown in Fig. 7.2. There, a) shows a micrograph of the SBFET device ($L_g = 500$ nm; $d_{NW} = 26$ nm; $d_{ox} = 300$ nm SiO_2) prior to the dielectric deposition, where the location of the Schottky junctions is clearly visible.

Posteriorly, Ta_xO_y was deposited with a thickness of 25 nm and two independent TG electrodes were patterned directly overlapping with the Schottky junctions. The result is seen in Fig. 7.2 b).

7.2.1 Back Gated Measurements

Back gated $I-V$ measurements of the device as seen in Fig. 7.2 were carried out to asses the effect of the TG dielectric lacking of passivation. The subthreshold characteristics prior to and posterior to the TG stack formation are respectively observed in Figs. 7.3 a) and b) for V_d =-1 V . The device in Fig. 7.3 a) exhibits the unipolar p-type behavior, previously described in Sects. 5.3 and 6.3. For the case in Fig. 7.3 b) both TG electrodes were grounded. Although S and I_{on} are strongly degraded the device polarity is unaltered. A possible reason for the performance degradation could be the lifting of the SiNW by the deposited tantalum oxide or the lack of passivation. Also, the electrostatics obviously change by the implementation of the TG electrodes.

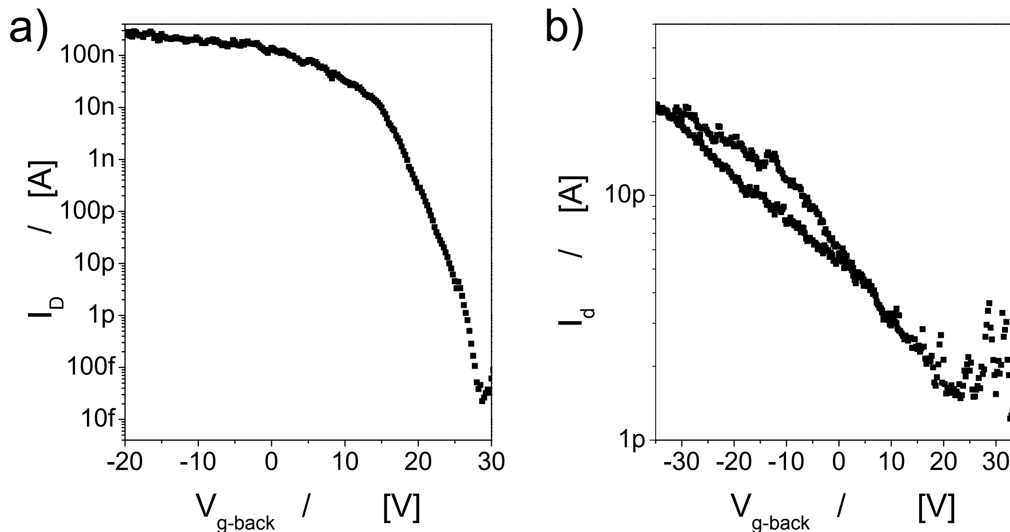


Figure 7.3: Subthreshold characteristics of back-gated SiNW SBFET before a) and after b) Ta_xO_y deposition. Unipolar p-type behavior is retained after the deposition.

7.2.2 Polarity Control by TGs

TG arrangement Next, the top gate electrodes are used to bend the energy bands at the Schottky contacts in such a way that electron and hole transport is stimulated respectively. The TGs are refereed to as TG-L for the left electrode and TG-R for the right one, in accordance to Fig. 7.2 b). Further, the left $NiSi_2$ NW-electrode is grounded and thus defined as source. Concurrently, the right $NiSi_2$ NW-electrode is biased at V_{ds}=-1 V. In the following experiments, TG-R is biased in such away that either a hole- or electron-*transparent* Schottky barrier is promoted. TG-L is used for a potential sweep. Initially, the back gate (BG) is grounded (V_{bg}=0) in order to asses the direct effect of the the top gates, then the measurements are repeated for different V_{bg} ranging between -30 V to +30 V.

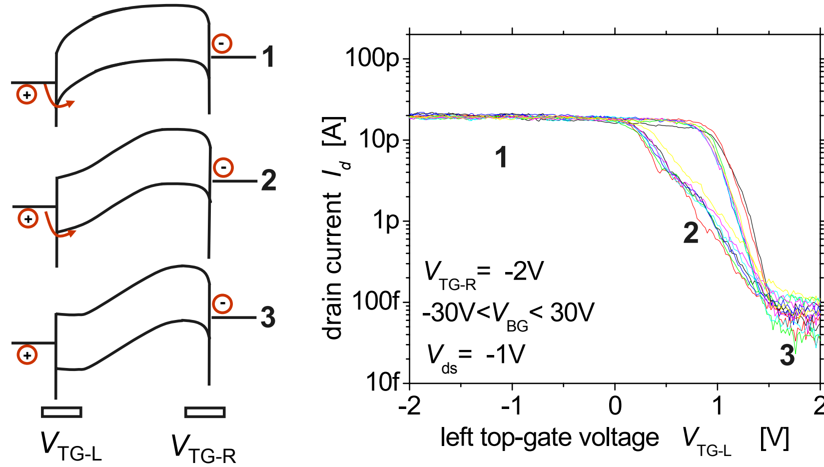


Figure 7.4: Multi-top-gated SiNW SBFET in p-type operation. $|I_d| - V_g$ of the SiNW-SBFET of seen in Fig. 7.2 accompanied by schematic band diagrams at different operation points labeled 1-3.

p-type conduction In this experiment TG-R is biased at V_{TG-R} =-2 V, and TG-L is sweept between V_{TG-L} =-2 V and +2 V. Figure 7.4 depicts the schematic band diagrams at different operation points together with the measured subthreshold characteristics. For V_{TG-L} =-2 V the left Schottky contact is as transparent as the right one for holes. The holes are injected through both Schottky junctions towards the drain electrode, the device is at the on-state. Here, the bands practically resemble the case of the back

gated device for $V_{bg} \ll 0\,\mathrm{V}$. As V_{TG-L} gradually increases, the bands at the left Schottky junction are shifted down, diminishing hole injection through this contact and finally quenching it off for V_{TG-L} =+2 V. Throughout the complete experiment, electron injection from the drain electrode is effectively blocked by the large barrier: ϕ_{Bn} plus the upwards bent conduction band.

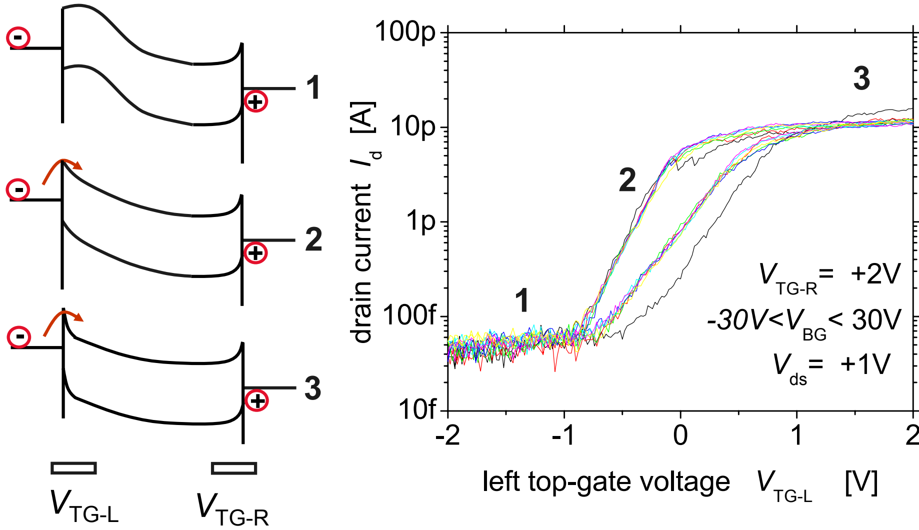


Figure 7.5: Multi-top-gated SiNW SBFET in n-type operation. $|I_d| - V_g$ of the SiNW-SBFET of seen in Fig. 7.2 accompanied by schematic band diagrams at different operation points labeled 1-3.

n-type conduction Analogous to the previous experiment, forcing electron injection is now tested. Under ideal conditions the setup is symmetric in an initial approximation, because both potential barriers ϕ_{Bp} and ϕ_{Bn}, are close to $E_g/2$ according to Table 4.1. In this case TG-R is constantly biased at V_{TG-R} =+2 V, and TG-L is varied between V_{TG-L} =-2 V and +2 V as in the previous experiment. Figure 7.5 shows the schematic band diagrams and measured subthreshold characteristics analogous to the previous example. In all cases, the application of V_{TG-R} =+2 V effectively blocks hole injection by ϕ_{Bp} plus the additional downward band bending at the drain Schottky junction. Applying V_{TG-L} =-2 V leads to the upward bending of the bands at the source junction, so that electron injection is suppressed as well. However, increasing V_{TG-L}, lowers the bands at this junction making the SB for electrons thinner and thus allowing electron injection. This is proven by the

I_d increase in the measured characteristics.

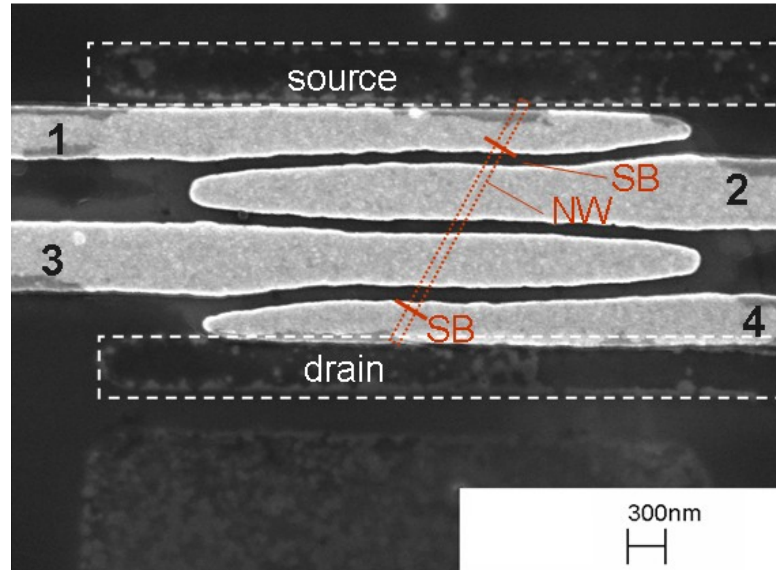


Figure 7.6: SiNW SBFET with four top gates. TGs 1 and 4 are located above the Schottky junctions, whereas TGs 2 and 3 only above the SiNW active region

Four TG Setup In order to confirm the actual band bending model directly at the Schottky junctions, measurements of structures with up to four TGs distributed along the NW´s length were performed. One device is seen in Fig. 7.6, with Al_2O_3 as the top dielectric, where the outer TGs labeled as 1 and 4 are directly located above the SBs. Performing the previous experiments with the outer TG electrodes leads to the same results, however if the inner electrodes are used and the outer ones are grounded, polarity control could not be achieved. These results corroborate that polarity control is achieved by electrostatically tuning the SBs and not another segment within the Si region.

7.2.3 Interpretation

The previously shown experiments give important information on the transport properties of SiNW SBFETs and simultaneously give rise to a novel type of logic device. First it must be noted, that the results are all repro-

ducible and that they also take place in the other multi- top-gated devices built. The experiments can be reproduced symmetrically, that is the same results are obtained when source and drain contacts are exchanged with each other. Each characteristic works for the forward and for the backward TG voltage sweep as well as for different sweep rates, which shows that this is not an effect of charged traps. It should be noted again that theoretically either mobile or fixed charges are required to bend the energy bands since the Si is undoped. In the actual measured devices, these charges could be readily injected charge carriers located near the Schottky junction or fixed charges located at the interface or surface.

Polarity Control

Back gate vs. top gates In contrast to the back gated experiments in Sects. 5.3 and 6.3, the thin and high-κ dielectric is able to provide strong electric field coupling to the Schottky contacts. Note that the BG has almost no electrostatic control over the Schottky junctions in comparison to the biased TGs, as confirmed by the invariance of the characteristics of Figs. 7.4 and 7.5 from V_{bg}. For obvious reasons the field coupled by the TGs locally through the thin high-κ dielectric is significantly stronger than the one available through the extremely thick SiO_2 bottom dielectric.

Mechanisms of polarity control The experiments strongly suggest that the unipolarity observed in back gated SiNW SBFETs with thin NW diameters, is given by local charges that shift the applied electric potential at the Schottky junctions, favoring an upward bend of the bands so that hole injection at the Schottky contacts is enhanced. Since polarity is not V_g sweep rate dependent, the charges shifting the electric field could be fixed charges such as metal ions or dipoles like H_2O molecules attached at the NW surface. Sufficiently high positive V_g in back gated devices would probably lead to an n-type behavior as well. Only, that these voltages are above the operation range of the device and lead to dielectric breakdown. In contrast, a band pinning at the Schottky junction enhancing hole transport would not allow n-type operation of the device. The actual nature of location of the assumed charges is still unknown, but this does not affect the main conclusion of the experiment. The bottom line is the fact that the SiNWs themselves are not doped and that the polarity is tunable by a direct electrostatic coupling to the Schottky junctions. Note that the lack of passivation should not affect the main conclusion from these experiments. Despite the fact that the SBFET tries to behave as a p-type device as confirmed in Fig. 7.3 it can be *forced* to act as an n-type device.

7.2.4 Dopant-Free Logic Device

Novel device The experiments shown in Sect. 7.2.2 show the conception of a novel transistor type, the *SBFET with controllable polarity by tunable Schottky contacts*. The major implication of this concept is the deliberate circumvention of doping. The real beauty of this device is its simplicity and double functionality, as the same device can be tuned as a p- and n-type conductor. This means that no different technological treatment is required to differentiate between n- and p-devices during fabrication, reducing fabrication complexity. Simultaneously, novel logic schemes that profit from the higher device functionality, such as the increased number of logic states, can be applied.

Device performance The I_{off} amounts to approximately 50 fA and are low enough for most electronic applications. However, they are slightly higher than the measurement resolution of the characterization system. This is probably given by gate leakage currents. Appropriate annealing might reduce the leakage paths even further. Principally this device should exhibit lower I_{off} than the back gated devices, because the barrier heights in the off state are significantly higher. Concurrently I_{on} is rather low for usual applications. The current levels are possibly also affected by the unpassivated dielectric. Here passivation, a better dielectric and a surround gate architecture should also yield higher I_{on} higher than the ones reported here for the back gated devices in Sect. 5.3.3.

7.2.5 Doping in Nanowires

Accurate doping of nanoscale semiconductors is a difficult task. Not only its practical implementation but also its reproducibility are critical issues, the actual effect of doping effect needs to be revised. As calculated by Y.-M. Niquet et al. [DNDA07] depending on the dielectric media surrounding the NWs, the active region may require a higher doping concentration than in bulk devices to provide the same doping efficiency. In this context, it is plausible to develop dopant-free device concepts.

Alternative control of doping in NWs

Dopant free polarity control in SBFETs has been demonstrated for devices with asymmetric SB heights. That is, n-type devices are formed with contacts with low ϕ_{Bn} (yttrium silicide/Si or erbium silicide/Si) and p-type devices are built from Schottky contacts with low ϕ_{Bp} (PtSi/Si or PdSi/Si).

Nevertheless, a small ambipolarity is still observed in these devices, since the respective ϕ_B are never null or negative for the Si system.

Previous experiments by other groups have shown the ability to transform ambipolar devices into unipolar ones. This has been first shown in top-down patterned SiNWs [KLE+05] and posteriorly in CVD synthesized ones [AKT+06]. In both cases a common back gate gives ambipolar operation. The device works by adjusting V_{bg} for the device to operate either at the n- or p- branch of the subthreshold characteristic and then using a top gate placed in the middle of the active region, i.e. as far away possible from the Schottky junctions. In the off-state, the top gate bends the energy bands in order to block the carriers in the middle of the active region which were already injected through one of the barriers. In contrast, the distinctive feature of the transistor concept developed in this work is the fact that the off-state is settled by the direct control of the effective Schottky barrier height itself. Accordingly, in the off-state most charge carriers are blocked from entering the active region.

Another innovative concept has been developed by H.-Y. Li, E.P.A.M. Bakkers et al. at Philips Research [LWB+07] where a p-InP shell is able to remotely p dope an i-InAs NW core.

7.2.6 Further Implementation Issues

The concept of polarity-tuning with TGs works best by using SiNWs with longitudinally intruded S/D segments. The enhanced electrostatic coupling at the Schottky junctions enables the efficient carrier injection control by local TG structures as proven in Sect. 6.4.2. This is probably the reason why this concept has not been developed previously for instance in thin- film- or SOI-SBFETs. Although this concept is facilitated by the heterostructure NW architecture it is not limited to this one and could be extended to SOI-SBFETs or even SB-FinFETs as long as an efficient gate coupling to the SBs is guaranteed.

The price for circumventing doping is the need for two independent gates. For a possible future implementation, the tunable SB concept fabrication techniques need to be developed in detail to align the TGs to the Schottky junctions, for instance in a self aligned process. In order to reduce the minimal device size MESA spacers could be used to act as the two metallic TGs so that only one lithographic structure is needed to process both TGs.

7.3 Conclusions

The experiments performed in this section have a twofold meaning for this work. On the one hand they are a proof, that transport in *i*-SiNW SBFETs is controlled mainly by the Schottky S/D contacts as proposed in Sect. 6.4. On the other hand, they provide the basics of a novel device concept which could enable complementary logic without the use of doping.

Conclusions

This thesis focuses on a novel bottom-up fabrication approach and the electrical characterization of quasi one-dimensional metal to semiconductor heterostructures with the primary aims of investigating their transport properties, enabling high performance electronics and developing innovative device concepts. The studies were carried out in the example of the intrinsic-silicon to nickel silicide material system. The work encompasses the overall process flow starting from the material synthesis, comprising the device fabrication and characterization and culminating in the invention of a novel field effect device.

Nominally intrinsic and single-crystalline silicon nanowires were grown by catalytic chemical vapor deposition employing the vapor liquid solid mechanism. Longitudinal silicon nanowire segments were transformed into metallic ones by an innovative longitudinal silicidation, where the interface between the silicided nanowire segment and the un-reacted silicon segment exhibited a sharpness in the nanometer range or better. With this technology longitudinal nickel silicide to silicon to nickel silicide nanowire heterostructures were synthesized to act as the central components of Schottky source and drain contact field effect devices. In a planar back gated geometry these heterostructures yielded promising transistor characteristics for possible future electronic applications. The inherent nanowire geometry and bottom up processing techniques enabled a systematic study on the scaling properties of the length of the active region and of the nanowire diameter. The scaling studies were complemented by simulations and special measurements to provide important information on the electronic transport mechanisms in these devices. These transport mechanisms were used to conceive innovative field effect devices which address end of ITRS roadmap problems.

Silicon Nanowire Growth

To implement the vapor liquid solid growth of nominally intrinsic Si nanowires catalytic chemical vapor deposition was used. The required catalyst parti-

cles were provided by the coalescence of sputtered Au layers whereas the Si source was undiluted SiH_4. As the initial step, a low pressure chemical vapor deposition cluster tool was rebuilt and adapted to become capable for the Si nanowire synthesis.

The growth experiments were performed on amorphous SiO_2 and on oxide free (001)-oriented Si substrates. In both cases the processes were optimized to yield single-crystalline Si nanowires with a controllable and uniform diameter, high structural quality and high nucleation yield. This was closely linked to the uniform coalescence of Au layers, developed separately for both substrate types. Also the growth parameters were varied to suppress planar Si deposition. Silicon nanowires grew on SiO_2 commonly in a random direction but predominantly in the crystallographic direction <112>. In contrast, the Si nanowires grown on Si showed a specific orientation towards the substrate suggesting epitaxial growth in the direction <110>.

Position control and vertical growth of nanowires on metallic layers
An important accomplishment was the first vertical Si nanowire growth to be reported on amorphous metallic layers. Through a novel procedure, the nanowires nucleated on TaN layers were guided vertically out of high aspect ratio holes without kinking and without adapting their surface morphology This scheme enables position controlled vertical integration of nanowires. The characteristic advantages are the possibility of decoupling the nanowires from neighboring ones as well as enabling a stacking of various layers containing devices based on vertically aligned nanowires.

Longitudinal Si Nanowire Nickel Silicidation

A fundamental aspect of this work is the synthesis of nickel silicide to silicon longitudinal nanowire heterostructures by implementing innovative bottom-up approaches. This work was the first to show longitudinal nickel silicidation of Si nanowires. In a combined top-down and bottom-up approach, Si nanowires were contacted with Ni reservoirs by electroless Ni plating at one of their ends, completely embedding the nanowire end . The process has the distinctive advantage of being self aligned and selective to SiO_2 and Si. Upon controlled annealing at 400°C - 480°C Ni diffused into the Si nanowire up to various micrometers in length. Along the diffusion path Ni and Si reacted to create a nickel silicide nanowire segment. Depending on the initial nanowire orientation used, different silicide stoichiometries were observed even at the same reaction temperatures. In <112> oriented Si nanowires, very likely the nickel-rich phase Ni_2Si seems to have been formed. For <110> silicon nanowires the $NiSi_2$ phase was directly formed without passing through

other stoichiometries in contrast to thin film and bulk experiments, where the Ni_2Si and NiSi phases have to be sequentially formed prior to the $NiSi_2$ formation. In-situ TEM silicidation experiments showed a linear reaction rate, confirming that the the longitudinal nanowire silicidation was interface reaction limited instead of diffusion limited for diffusion lengths of up to at least a couple of hundreds of nanometers. The formed $NiSi_2$ showed single crystalline nature, suggesting an epitaxial relation to the silicon nanowire segment.

Completely silicided $NiSi_2$ nanowires showed linear ohmic behavior with maximal resistivities of 98 µΩ-cm. The single crystalline structure enables high breakdown current densities surpassing 205 MA/cm^2, higher than state-of-the-art Cu nano-interconnects. The most remarkable characteristic of the longitudinal nanowire silicidation is the abrupt interface between the nickel silicide and Si segments, which is sharper than a couple of nanometers as measured for both $NiSi_2$ and Ni_2Si stoichiometries. In fact, the interface reaction limitation of the silicidation suggests atomically flat interfaces, which in turn has been demonstrated by other research groups.

Silicon Nanowire Schottky Contact FETs

Transistor fabrication and reduction of metallurgical gate length The remarkably sharp metal to semiconductor nanowire interfaces achieved here, were employed for interesting electronic applications. In single Si nanowires contacted with Ni reservoirs from both ends, longitudinal Ni-silicide to Si to Ni-silicide nanowire heterostructures were formed. By providing the nanowires with a common back gate stack silicon nanowire Schottky contact field effect transistors (SBFET) were fabricated. The main advantage of the transistor fabrication concept developed here is the ability of reducing the metallurgic gate length from initially 1 µm down to sub-lithographic domains by only applying an initial coarse lithographic patterning and two self-aligned steps , avoiding the need of nanoscale patterning tools. Consequently, the feasibility of forming ultra-small Si active region lengths down to 7 nm was shown. For high density integration the concept only is advantageous in a vertical geometry, because the lithographic pitch and therefore the device density is not reduced.

Electrical characteristics of Si nanowire transistors Electrical characteristics of Si nanowire transistors The SBFETs were electrically characterized in detail Regardless of the simple back gated architecture, the transistors exhibited a high electrical performance with promising properties. Devices with a nanowire diameter of 23 nm and a gate length of 500 nm

featured on/off-current ratios of over 10^7, on current densities surpassing 1 MA/cm^2 at -1V source to drain bias and inverse subthreshold slopes as low a 180 mV/dec. Peculiarly, the nominally intrinsic devices with nanowire diameters of 30 nm or thinner exhibited a unipolar p-type conduction despite the fact that ambipolar operation was expected, since the Schottky barrier heights are close to $E_g/2$. Hysteresis in the subthreshold characteristics was observed for gate potential sweep rates below 77.5 mV/s and was most likely caused by charge trapping in the unpassivated native Si oxide surrounding the nanowires. Benchmarked to other state-of-the-art transistors, these devices have on-current densities comparable to FinFETs of equal length and to doped Si nanowire FETs. The devices presented here exhibit the lowest conductances and largest current densities in the on state for nominally intrinsic Si nanowire transistors published up to date.

Electronic Transport in Si Nanowire SBFETs

A thorough and systematic study of the transport properties of Si nanowire SBFETs was carried out. Device geometry scaling, electrical measurements as well as simulations were performed to address various transport related aspects. Hysteresis in the transfer characteristics was studied by a combined electrical measurement and finite element simulation study.

Nanowire length scaling As one fundamental part of this thesis, a detailed study on the geometric scaling properties of the Si nanowire SBFETs was presented for the first time. Devices based on <112> oriented Si nanowires with a constant diameter were investigated in dependence of their metallurgical gate length. The saturation currents of the subthreshold characteristics exhibited two distinct regimes. For gate lengths between 210 nm and 1 µm the conductance was constant at 1 µS, whereas for increasing gate lengths up to 8.5 µm an exponential decay was registered. The constant conductance for short gate lengths is attributed to the limiting Schottky junctions. In contrast, it was shown that the Schottky contacts could not account for the exponential decay in conductance. Thus, only the channel conductance should been the limiting mechanism. The supra-linear relation is an intriguing, unexpected phenomenon. Such a behavior could be explained by localization of the electron wave function as indicated by atomistic simulations of Si nanowires performed by various groups under the premise that electron-phonon coupling does not break phase coherence. In carbon nanotubes electron-phonon coupling appeares to be suppressed by quantum confinement even at room temperature. However, this is questionable for the

relatively thick Si nanowires used for the experiment, 10-30 nm in diameter. The study made clear that scaling rules of these SBFETs are not trivial and that further special transport investigations are required to elucidate the complex dependencies.

Nanowire diameter scaling Another important scaling study, which was performed here for the first time was a diameter dependent investigation of the electrical behavior of SBFETs. Devices with constant gate length 1 µm and varying nanowire diameter between 7 nm and 70 nm were studied. The thinnest devices exhibited unipolar *p*-type behavior. As the diameter increased a gradual transition to higher ambipolarity approaching the expected bulk behavior was clearly observed. The experiment showed that systematic unintentional doping of the devices can almost be ruled out completely and suggested that the device polarity is controlled by the Schottky barrier contacts as its area directly scales with the nanowire diameter.

Field control over Schottky contacts The silicide source and drain contacts of the SBFETs resemble needles that highly enhance the electric field at the Schottky junctions. As a consequence the applied gate field is able to bend the energy bands adjacent to the Schottky junctions more effectively than in the case of transistors with blunt electrodes, as proven by electrostatic calculations. To quantify this effect the effective Schottky barrier height for the thermionic emission of holes was determined by energy activation measurements giving 56 meV in the transistor on-state. These results show that the barrier height is in fact reduced by almost a factor of ten. Herein, lies the great advantage of the metal/semiconductor/metal heterostructure architecture applied here. Even a simple back gate stack having a minimal contact to the approximately cylindrical nanowire is able to effectively steer the transistors drain current. The gate control over the carrier injection across the Schottky contacts is the key ingredient for the high on-currents, low off-currents, low specific contact resistivities and steep subthreshold slopes observed in these devices.

Polarity Control of Nanowire SBFETs

As a final step an electrostatic control over the individual Schottky barriers was achieved by a multi-top gate geometry. This concept, which was first developed during this work, fulfilled a double function. On the one hand, it gave evidence that the devices were not unintentionally doped and demonstrated that the device polarity was solely controlled by the ratio between

the effective barrier heights for electrons and holes. On the other hand, the effective gate control over the Schottky contact transmissibility was used to enable novel SBFETs. In the transistor concept proposed, fabricated and proven here, one Schottky contact is tuned to transmit a certain kind of carrier, while the other Schottky contact is used to block the other type of carrier. Via this method it was possible to show that the same transistors can be tuned to work as p- and as n- type devices. These FETs with individually tunable Schottky contacts made possible complete omission of doping and enable a complementary technology. Thus, this concept solved two important challenges related to device doping, the mobility degradation through doping and the increasingly difficult accurate control of doping in nanoscale structures. Moreover, classical short channel effects should effectively be suppressed by the Schottky barrier architecture and thin Si body thickness. The device concept was facilitated by the nanowire heterostructure geometry but can be extended to other nanoscale SBFETs built with conventional top down technology.

Variables and Constants

A	Richardson Constant
A^*	Effective Richardson Constant
A_{NW}	Cross-Sectional Area of a Nanowire
BG	Back Gate
D	Diffusion Constant
d_{Au}	Nominal Gold Layer Thickness
d_{ch}	Thickness of the Inversion Layer or Channel Thickness
d_{met}	Total Height of Metal Stack
d_{Ni}	Thickness of the Ni Layer
d_{NiSi}	Thickness of a $NiSi_2$ NW
d_{NW}	Nanowire Diameter (As Measured by SEM)
d_{ox}	Gate SiO_2 Thickness
d_{rec}	Recess Depth
d_{Si}	Si-NWs Thickness Excluding the Native Oxide Thickness
E	Energy
E_c	Conduction Band (Energy)
E_F	Fermi Level
E_g	Band Gap
E_{vac}	Vacuum Level
$F(x)$	Force
$F(E)$	Fermi-Dirac Function
$F_s(E)$	Fermi-Dirac Function for the Semiconductor
$F_m(E)$	Fermi-Dirac Function for the Metal
f_s	Sweep Rate
I	Electric Current
I_{off}	Off-Current
I_{on}	On-Current
I_{ds}	Drain Current
I_g	Gate Leakage Current
J_{on}	Current Density in the On-State
J_{TE}	Current Density due to Thermionic Emission
$J_{s\mapsto m}$	Current Density from Semiconductor to Metal
$J_{m\mapsto s}$	Current Density from Metal to Semiconductor

J_N	Net Atomic Flux
J_S	Saturation value of Current Density
J_{SB}	Current Density through Schottky Contact
k	Boltzmann's Constant
l_c	Coherence Length
L_c	Localization length
L	Length
L_g	Metallurgical Gate Length
L_{g0}	L_{g0} Prior to Silicidation
L'_g	L_{g0} After Silicidation
l_{NiSi}	Total Length of the Silicided NW Segments
l_{NW}	Length of the Nanowire
$m*$	Effective Mass of the Electrons/Holes
m_0	Free Electron Mass
n	Electron concentration
n_{id}	Ideality Factor
N	Atomic Concentration
$N(E)$	Density of States Function
N_D	Dopant Concentration
$PMMA$	Poly-Methyl-Methacrylate
R	Electrical Resistance
R_C	Contact Resistance
R_{SB}	Serial Resistance of a Schottky Contact
S	Inverse Subthreshold Slope
t_r	Retention Time
p	Hole Concentration
p	Pressure
p_{Ar}	Argon Partial Presure
p_{H_2}	Hydrogen Partial Pressure
p_{N_2}	Nitrogen Partial Presure
p_{SiH_4}	Silane Partial Pressure
p_{tot}	Total Pressure
q	Magnitude of Elementary Charge
T	Temperature
T_{grw}	Substrate Growth Temperature
$\mathbf{v}$	Carrier Velocity
v_x	Carrier Velocity Parallel to the Transport Direction
V	Voltage
V_{dd}	Operating Voltage

V_{ds}	Source - Drain Voltage
V_g	Gate Voltage
V_t	Threshold Voltage
w_{dep}	Depletion Width
Z	Atomic Number
∇	Nabla Operator
$\triangle$	Laplace Operator
ΔV_t	Shift in Threshold Voltage
Γ	Transmission Probability
ζ	Potential Difference Above the Barrier Height
η	Potential Difference Below the Barrier Height
ϵ_0	Permeativity of Free Space
ϵ_s	Permeativity of Semiconductor
$\epsilon_o x$	Permeativity of Oxide
λ	Wave Length
ξ	Electric Field
ξ_{gate}	Electric Gate Field
ξ_{sd}	Electric Source to Drain Field
ρ	Resistivity
ρ_{max}	Maximal NW resistivity
κ	Relative Dielectric Constant
ϕ_m	Work Function
ϕ_{Bn}	Schottky Barrier for Electrons
ϕ_{Bp}	Schottky Barrier for Holes
ϕ_{B-eff}	Effective Schottky Barrier Height
$\varphi(\mathbf{x})$	Electric Potential
ψ	Wave Function
χ	Electron Affinity

Abbreviations

AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
BHF	Ammonium fluoride buffered hydrofluoric acid
BG	Back Gate
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
CNT	Carbon Nanotube
c-Si	Crystalline Silicon
CVD	Chemical Vapor Deposition
DI	De-Ionized
DUT	Device Under Test
EELS	Electron Energy Loss Spectroscopy
EDX	Electron Dispersive X-Ray Spectroscopy
HR	High-Resolution
IPA	Iso-Propyl-Alcohol
LPCVD	Low Pressure Chemical Vapor Deposition
MBE	Molecular Beam Epitaxy
MOCVD	Metal Organic Chemical Vapor Deposition
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NW	Nanowire
NMP	N-Methyl-Pyrrolidone
PVD	Physical Vapor Deposition
pH	Pondus Hydrogenii (potential of hydrogen)
QMS	Quadrupole Mass Spectrometer
RF	Radio Frequency
RTA	Rapid Thermal Anneal

SB	Schottky Barrier
SBFET	Schottky Barrier Field Effect Transistor
SCE	Short Channel Effects
STM	Scanning Tunneling Microscope
SE	Secondary Electron
SEM	Scanning Electron Microscope
SiNW	Silicon Nanowire
SOI	Silicon on Insulator
SMU	Source Measurement Unit
Solgel	Soluble-Gel
TEM	Transmission Electron Microscope
TG	Top Gate
TG-L	Left-Top Gate
TG-R	Right-Top Gate
TLM	Transmission Line Method
TEOS	Tetra Ethyl Orto Silicate
UHV	Ultra High Vacuum
VLS	Vapor Liquid Solid
VSS	Vapor Solid Solid

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Publications and Peer-Review Proceedings as a Direct Result of this Thesis

Tuning the Polarity of Si-Nanowire Transistors Without the Use of Doping W. M. Weber, L. Geelhaar, F. Kreupl H. Riechert, L. Lamagna, M. Fanciulli, G. Scarpa and P. Lugli. Presenter: P. Lugli.
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