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Topologically Defined Neuronal Networks Controlled by Silicon Chips

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Summary

Small neuronal networks with defined synaptic connection patterns could provide a unique tool for studying fundamental concepts in neuroscience, because they are much simpler than *in vivo* systems and give easy access to individual neurons. Field-effect transistors and capacitive stimulators implemented on a semiconductor chip establish a non-invasive neuron-silicon interface, that enables the long term supervision even of large neuronal assemblies.

The present thesis addresses the experimental and technological aspects of network design. Based on existing transistor chips a new device was processed for the specific requirements here. Small chip-controlled networks were grown from neurons of the snail *Lymnaea stagnalis* and characterized.

First, a new method for directing neurite outgrowth was developed. It is based on topographic guidance cues consisting of pits and narrow connecting grooves, which were processed from SU-8 polyester photoresist. Neurons placed into the pits grew neurites that followed the grooves and established electrical synapses upon contact with other neurites or somata. These networks were studied with standard electrophysiology and the conductance of the synapses was determined. On average, it was larger than the conductance of synapses between cell pairs grown on protein tracks.
Besides guiding their outgrowth, the topographic structures also keep neurites in the final geometry and confine cell bodies to the pits. This is a major advantage compared to techniques using chemical patterns; there, neurites and somata are frequently pulled away by forces exerted by the growth-cones. Moreover, the structures are reusable many times, which makes them very efficient.

Building on established technologies for extracellular recording and stimulation of neural activity, a transistor chip was processed next. Its layout, 16 bidirectional contacts arranged in a 4x4 array, was especially designed for monitoring small, defined networks of snail neurons. Each contact comprised a buried channel field-effect transistor for recording action potentials, surrounded by capacitive stimulation spots. Chips were characterized electronically and tested with single neurons. The transistors recorded a variety of signal types, similar to the results of previous works. Most of the extracellular signals could be qualitatively explained with the point-contact model for the neuron-silicon interface and the Hodgkin-Huxley model describing the voltage dynamics of the neuron. Extracellular stimulation was very reliable, 5-10 square wave pulses with 1V-5V amplitude applied to the capacitive spots evoked action potentials in the cell above.

The third step combined both technologies, SU-8 topographic structures and silicon chips. For the first time, hybrid networks with defined geometry were realized. The most fundamental system, the silicon-neuron-neuron-silicon loop, was studied in detail. Upon extracellular stimulation the respective presynaptic neuron fired an action potential, which was detected by the transistor. The signal propagated along the neurites, passed the synapse and depolarized the postsynaptic cell where it triggered an action potential, if the input was strong enough. Again, neuronal activity was recorded from the transistor underneath. Larger networks with three and four neurons were also grown and characterized.

The examples presented here constitute proof-of-principle experiments. They demonstrate that topologically defined hybrid networks, combining biology and semiconductor technology, can be implemented in functional systems, and pave the way for future applications such as a ‘living’ neurocomputer.

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Chapter 1

Introduction

This first chapter outlines the ideas and questions that led to the present thesis and briefly reviews relevant technologies. An overview of the contents of the other chapters concludes the introduction.

1.1 Why build topologically defined hybrid networks?

In vivo neural networks are highly complicated systems comprising up to 10^{11} neurons with a complex pattern of synaptic connections. While recent advances in functional magnetic resonance imaging and positron emission tomography provide tools for monitoring the activity of whole brains, their temporal and spatial resolution is still far too low for studies at the single cell level.
Despite these technological deficits, results from rather simple experiments, with impaled microelectrodes, inspired fundamental theoretical concepts like Hebbian learning or associative memory. Artificial systems have been developed, e.g. Hopfield networks, that resemble the natural ones to a smaller or larger extent. Such artificial systems can perform difficult tasks of information processing and are even used for commercial applications. However, most of them are implemented in special software running on ordinary computers and can therefore not profit from the massive parallel computing capabilities of the living neural networks they were adapted from. There are only a few examples where these ideas have been realized in hardware, namely custom made silicon chips. The high number of synaptic connections restricts network size on these chips to about 1000 neurons or less, even in the VLSI (very large scale integration; silicon processing technology) era [96].

In consequence there is a large technological gap between theory on the one hand and the real world on the other. Eventually this gap could be bridged with a **bottom up approach, the controlled assembly of well organized networks** from living neurons *in vitro*. These networks would provide a unique tool for studying signal processing in biological nervous systems and their parallel computing capabilities could lay the foundations for novel computer systems.

Nerve cell cultures are a common technique in neuroscience. They considerably reduce the number of neurons, compared to living brains and restrict the network to the 2D surface of the culture dish, thereby giving easy access to all neurons. Yet, synapses are still numerous and their connections remain unknown, obstructing any attempt to establish a theoretical model of the system.
The problem could be overcome if it were possible to grow networks with defined synaptic connection pattern, e.g. the two layer perceptron in fig. 1.1.

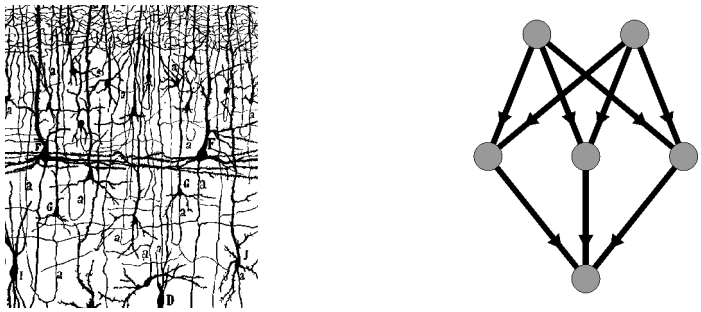


Figure 1.1: *Left: Piece of the human visual cortex with highly branched neurites and complex synaptic connection pattern, from [20]. Right: Schematic drawing of a simple, designed feed-forward network.*

Studying these systems, once they are established, requires **long term control of network activity at the single cell level**; action potentials must be evoked in and recorded from individual neurons. Standard electrophysiology, using impaled microelectrodes or patch clamp, is inappropriate because it harms the nerve cells, thereby limiting the recording time to a few hours before cells die. Furthermore, spatial constraints with micromanipulators used for positioning the pipettes considerably restrict the number of cells that can be monitored. **Alternative techniques are needed that are non-invasive**, as sketched in fig. 1.2, and also can be scaled up to large neuronal assemblies .

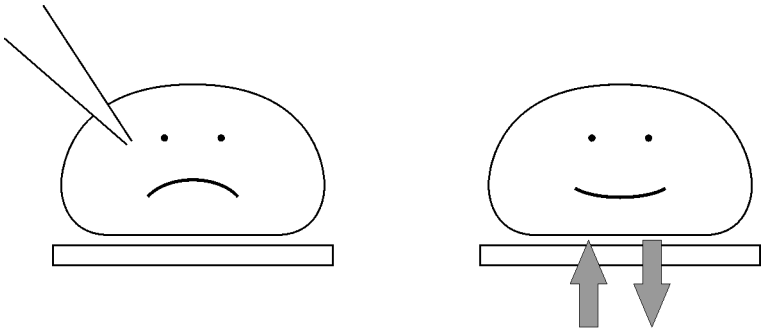


Figure 1.2: *Invasive (left) and non-invasive (right) recording and stimulation of individual neurons.*

The aim of this thesis is to implement and study small networks of living neurons with a defined synaptic connection pattern. This requires advances in network design and extracellular recording, and lays the foundations for systematic tests of fundamental concepts in neuroscience.

1.2 Defined networks and extracellular recording, state-of-the-art

Since the ideas outlined above are not new, much work has already been done on network design and non-invasive recording. This paragraph gives a short overview of relevant technologies reported in the literature.

A variety of methods exists for **building topologically defined networks**. Most of them use patterns of substrate-bound molecules that either promote or inhibit neurite outgrowth, e.g. silanes [56], poly-L-lysine [8] or proteins [81]. Neurons cultured on these substrates grow neurites that follow the permissive tracks while avoiding inhibitory areas. The patterns are made with techniques adapted from semiconductor processing, like photolithography [56], laser ablation [15] or microcontact printing [97]. Although they guide advancing neurites rather well, somata and already grown neurites are frequently

displaced by pulling forces exerted by the growth-cones.
In a preceding study [129], pillars processed from photoresist were used to mechanically immobilize the cell bodies on predefined sites.
Much smaller topographic structures consisting of grooves or edges in the micrometer and nanometer range have been shown to affect neurite outgrowth, too [84]. Even though they have been proposed as a tool for designing networks, there are no reports about successful applications so far.

Long term control of neuronal activity is only possible with techniques that contact neurons extracellularly. The simplest systems consist of metal spots processed onto planar substrates and connected to external amplifiers via insulated leads. Arrays of these electrodes, so-called MEAs (multi electrode arrays) are a common tool for monitoring network activity, for example in studies about the effects of chemicals on neuronal viability [76].
In 1972, Bergveld [2] used field-effect transistors with non-metal gates to make recordings from muscle fibers of guinea pigs and in 1990 Fromherz et al. were able to detect action potentials from neurons of the leech *Hirudo medicinalis* with similar devices [33]. Since then, the neuron-silicon interface has been studied in detail and recordings were made from rat hippocampal neurons (only with signal averaging to reduce noise) and nerve cells from the snail *Lymnaea stagnalis* [50, 114, 129].

1.3 Outline of this thesis

Building chip-controlled networks raises several questions and problems that can be divided into three parts: choosing the appropriate neuronal cell culture, growing topologically defined networks of synaptically connected neurons, and bidirectional interfacing of neurons to silicon chips. In the course of the experimental work, these parts were first addressed separately, though sometimes in parallel, and then joined at the end. The thesis roughly follows this order.

The next chapter covers all aspects of network design, from cell culture to theoretical concepts of signal propagation in neurites. After introducing the mechanisms governing axon guidance *in vivo*, methods for controlling neurite outgrowth *in vitro* are reviewed. The cell culture is then described, and the technological details of protein patterns and topographic structures are given, followed by a theoretical section on neurons and synapses. Finally, examples of defined neural networks are shown, characterized and discussed.

Once these networks can be reliably grown, their activity should be controlled non-invasively, and this is the subject of chapter 3. It illustrates the theoretical and technological aspects of buried channel field-effect transistors and describes relevant processing steps. Fundamental principles of the neuron-silicon interface are given in a further theoretical section. At the end, experimental results on stimulation and recording via the chip are presented and discussed.

Chapter 4 combines these techniques to establish chip-controlled, defined neural networks. After a brief recapitulation of theoretical concepts, three examples of increasing complexity are shown. The final discussion focuses on the efficiency of the single steps involved in growing the networks and the overall yield, and on how it may be increased.

The final chapter 5 summarizes the results and provides an outlook towards future experiments and applications.

Technological details of the cell culture and semiconductor processing, as well as parameters for simulations are outsourced to appendices.

Chapter 2

Networks of defined topography

The first section of this chapter summarizes the techniques for growth-cone guidance reported in the literature and discusses which best meet our experimental needs. Then the cell culture is introduced, followed by a detailed description of the methods used for guiding neurite outgrowth here, including relevant technological aspects. Basic theoretical concepts of neural networks like cable theory, synapses and the Hodgkin-Huxley model are introduced next. The chapter ends with a presentation of the results and their discussion.

2.1 How to control neuronal outgrowth - an overview

In the developing nervous system, axons must find the way to their target tissue over long distances. Many cues are involved in the process of pathfinding, which often act synergistically, thus increasing overall directional information. To elucidate the influence of individual cues on growing neuronal processes, many *in vitro* studies have been done. Their results are the basis for the engineering approach of growing defined neural networks.
The cellular mechanisms, signaling pathways and molecules governing pathfinding are briefly introduced in the next subsection. Various techniques used for controlling neuronal outgrowth *in vitro* are presented thereafter, followed by a discussion of which are most appropriate for the applications here.

2.1.1 Axon guidance *in vivo*

The mature human nervous system consists of about 10^{11} neurons with highly specific synaptic connections [53]. For example, axons emerging from the retina form an exact topographic representation of their origin at their target in the optic tectum.
Guiding axonal outgrowth is the most important process in establishing these precise connection schemes. Axons grow and respond to environmental cues with specialized terminal protuberances called growth-cones. These are both sensory and motor structures that bear numerous receptors for directional cues as well as cytoskeletal proteins and actin based motors that propel them froward. Growth-cones have three main domains: a central core which is rich in microtubules, mitochondria and many other organelles; the filopodia, thin extensions that project from the body; and lamellipodia, flat structures in between. Filopodia are highly mobile, rod-like actin-rich structures that scan their environment for directional cues. They are the major element of growth-cone sensory capability. Ligands binding to receptors in the filopodia membrane, e.g. extra cellular matrix protein (ECM) binding to integrin, stimulate the advance, retreat, or turn of growth-cones. The exact signaling pathways from ligand binding to directional movement are not yet fully understood [37], however, Ca^{2+} plays an important role as a second messenger [39, 46].

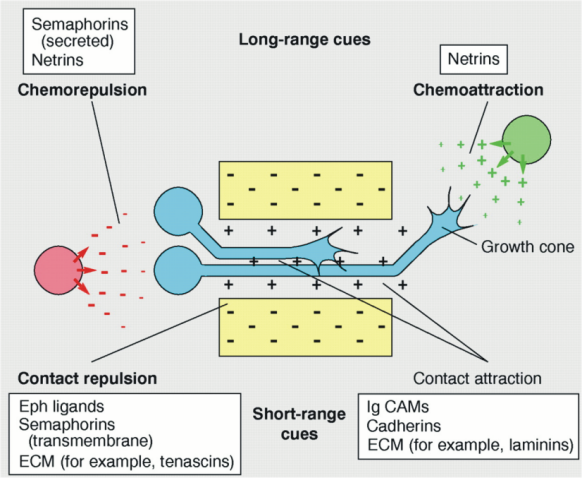


Figure 2.1: *Four types of mechanisms contribute to guiding growth-cones: contact attraction, chemoattraction, contact repulsion and chemorepulsion. Individual growth-cones might be 'pushed' from behind by a chemorepellant (red), 'pulled' from afar by a chemoattractant (green), and 'hemmed' in by attractive (grey) and repulsive (yellow) local cues; from [110].*

Directional cues are either attractive or repulsive, long-range or short-range. The long-range guidance mechanism, called chemotaxis, is based on gradients of diffusible, soluble molecules, whereas the short-range contact-mediated mechanism is mediated by tissue-bound, non-diffusible molecules. Fig. 2.1 depicts the four forces guiding growth-cones: contact attraction, chemoattraction, contact repulsion and chemorepulsion, and lists examples of ligands governing these mechanisms. Some guidance molecules are not exclusively attractive or repulsive but rather bifunctional, depending on their concentration, type of receptor and presence of other molecules. *In vivo*, neuronal outgrowth is generally controlled by several cues acting simultaneously and synergistically, e.g. the growth-cone is repelled from its origin by one ligand and attracted to the target tissue by another.
Besides these ligand-mediated cues, axonal outgrowth is further influenced by trophic factors that are needed for survival and growth as well as by adhesion molecules providing adhesive surfaces for the growth-cone.
Although many directional signals are present *in vivo*, *in vitro* studies revealed that a single ligand is often sufficient for controlling neuronal outgrowth. These studies set the stage for the design of defined neuronal nets.

2.1.2 Chemical patterns

Tracks of substrate bound molecules that are either attractive or repulsive to growth-cones (haptotaxis) are the most widely used technique for growth-cone guidance *in vitro*. In contrast to gradients of soluble molecules, they are easy to produce and can be kept in culture medium for a week or more without loosing their potency.
Two major issues are raised with chemical patterns: what molecules are best and how to deposit them on the substrate? The vast body of literature on this subject is summarized by several comprehensive reviews [5, 22, 30, 52, 54].

In an early experiment, P.C. Letourneau deposited areas of palladium onto different substrates by evaporation through EM-grids as masks [61]. Growth-cones from chick sensory ganglia neurons preferentially elongated on the more adhesive areas; for Pd on glass petri dishes they stayed on the Pd, while if polyornithine-coated dishes were used they preferred the Pd-free areas.
Since then, many chemicals have been tested for patterns controlling cell adhesion and neuronal outgrowth. Among them are adhesive proteins like extracellular matrix protein (ECM) [35], laminin [42], growth factors [81] and nonadhesive proteins like albumin [21]. Artificial growth-promoting molecules such as poly-L-lysine and poly-D-lysine [8], and inhibitors such as poly ethylene glycol (PEG) are also common [121]. All these substances are only physisorbed to the substrate. Due to the weak binding

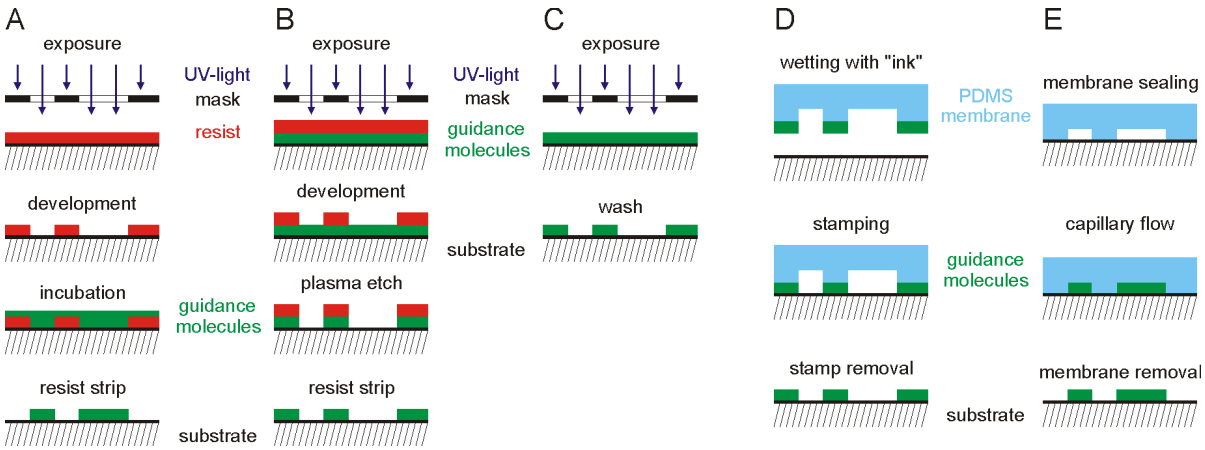


Figure 2.2: *Techniques for patterning chemicals onto surfaces. A, B: Photolithography with selective deposition (A) or removal (B) of molecules. C: Resist free lithography. D: Microcontact printing. E: Microfluidic networks.*

forces involved, this may result in gradual desorption and release to the cell culture medium with a subsequent loss of directional information. Conversely, self-assembled monolayers of silanes and thiols are tightly bound to silicon or gold surfaces by covalent bonds, making them very resistant to desorption. Silane patterns on Si-wafers have been cleaned and reused in hippocampal cell culture several times without loosing their directional information [23]. Above all, their adhesive properties can be tailored by appropriate terminal groups. Fluorinated, chlorinated and alkyl chains [56, 87, 100] inhibit protein binding and neuronal outgrowth, while amino groups promote it [87]. Complex molecules that are not compatible with silane or thiol chemistry, like proteins and peptides, can be covalently bound to substrates by heterobifunctional crosslinkers [8, 95, 121].

Molecules are patterned onto the substrate with techniques adapted from microelectronic device fabrication. These are summarized in fig. 2.2.

D. Kleinfeld et al. were the first to use photolithography for producing pathways of adhesive and non-adhesive silanes [56]. Their technique has been adapted by many researchers since then [16, 126]. Photoresist is spin-coated on a substrate, usually a silicon wafer, silica or glass, exposed through a lithographic mask, and developed. The substrate is then incubated with a solution containing growth mediating molecules; the molecules bind to the resist as well as to uncovered areas. Stripping the resist leaves patterns of guidance molecules surrounded by areas of blank substrate, see fig. 2.2A.
In fig. 2.2B, a similar technique is illustrated, with the main difference being that surface-bound molecules are selectively removed rather than deposited [16]. Before spinning photoresist, the substrate is uniformly coated with the desired molecules. Again, substrates are exposed and the resist is developed. A plasma etch removes guidance molecules in regions not protected by the resist, leaving a pattern complementary to the one in fig.2.2A after resist stripping.

Photolithography is an excellent tool for functionalizing surfaces with down to sub-micrometer resolution in any desired geometry. However, the harsh solvents (e.g. acetone) involved in the lithographic process are not compatible with many guidance molecules such as proteins. This problem is overcome by recently developed techniques illustrated in fig.2.2C-E.
Photoresist and solvents are completely omitted if UV light is used directly to selectively destroy, ablate or photocleave a homogeneous layer of growth mediating molecules. Washing away the residues in the exposed areas leaves intact chemicals in the areas shielded from the UV light by the mask. The only requirement here is UV light with a wavelength short enough to destroy or photocleave molecules, or with sufficient power for ablation (e.g. ArF laser λ=193nm). Several chemicals have been patterned

with this technique, ranging from the denaturation of laminin [42], growth factors [81], ECM [35] and ablation of poly-L-lysine [15, 87] to the photocleavage of covalently bound organosilane monolayers [24].

Conversely, UV light can also be used to selectively bind molecules in exposed areas to the substrate by special photoreactive cross-linkers [5].

Softlithography is the general term for a number of methods that use soft devices (usually consisting of PDMS, polydimethylsiloxane, Sylgard 184, Dow-Corning) to stamp or generate chemical tracks by capillary flow. They are made by curing a prepolymer on a photoresist master or structures etched into a Si-wafer.
Stamps wetted with 'ink' (guidance molecules) are gently pressed onto the substrate. Molecules attach to the surface and reproduce the raised areas of the stamp. G.M. Whitesides was the first to use microcontact printing for covalently linking thiol patterns to gold surfaces [97].
Microfluidic networks consist of PDMS membranes with relief structures that seal tightly against planar surfaces, forming micro-conduits [21]. Solutions are driven into the network of channels by capillary forces or application of pressure. Molecules adhere to the channel walls, one of which being the substrate. Removing the PDMS device leaves a pattern identical to the conduits on the surface, see Fig.2.2E. Complex structures with lanes of different molecules can be produced in a single step by multiple laminar fluid flow in capillary networks [11, 109].
Softlithography is an easy to use, inexpensive technique for producing complex patterns of surface-bound molecules. Except for master fabrication, no cleanroom equipment is required. Resolution is slightly reduced as compared to photolithography, but feature sizes down to 2μm are more than sufficient for most biological applications. For more information refer to the comprehensive reviews by G.M. Whitesides et al. [54, 127]

So far, all protocols resulted in chemical patterns surrounded by blank substrate. To increase directional information these areas are often coated with molecules bearing the complementary signal [56], e.g growth-promoting tracks surrounded by inhibitory regions. This is simply done by incubating the respective molecules on the prepatterned substrates as they only bind to the blank but not to the functionalized areas. The synergistic action of both cues increases directional information on growth-cones. This is especially important to prevent non-specific binding of serum (sometimes used with the culture medium) or proteins released by cells to the surface, which otherwise reduce the potency of the initial cues.

2.1.3 Substrate topography

In vivo, topographic features of the surrounding tissue provide morphogenetic guidance cues to growth-cones. For example, growing axons fasciculate with pioneer axons, follow them for a certain distance, and defasciculate again. During fasciculated outgrowth, the growth-cone of the elongating axon is in physical contact with the pioneer axon and follows its topographic information.

In vitro experiments are an elegant way to study the so far poorly understood signal transduction pathways involved in contact-mediated guidance and the role of the cytoskeleton [84]. Chemical cues abundant in *in vivo* systems can be completely excluded, leaving topographic structures as the only environmental information. A multitude of cells such as neurons, astroglial cells, MDCK, epithelial cells and many more were explanted onto glass, polymer and silicon substrates with rough surfaces or regular structures such as steps and grooves, with feature sizes ranging from nanometers to micrometers; see reviews by [4, 18, 19, 22, 29, 52].

For example, astroglial cells preferentially grow on top of a regular array of columns with 0.5μm diameter etched into silicon, while avoiding irregular nanometer-sized surface roughness [17]. BHK cells and

chicken neurons align and extend processes along simple step cues of sufficient height (1μm-10μm) processed into perspex [12] and orient in parallel to multiple grooved substrates [13]. Hippocampal neurons grow in parallel to deep, wide grooves but perpendicular to shallow narrow grooves [73, 83]. Some studies examined the synergistic and hierarchic effects of chemical and topographic cues simultaneously presented to BHK cells [9], while others tested the behavior of cells embedded into an artificial three-dimensional structure [63].

Most experiments done in this area of research so far were focused on studying the general features of cell-substrate interaction and how they relate to *in vivo* systems. Up to now, there were only few attempts to use topographic information for growing defined neural networks [22, 51].

2.1.4 Alternative techniques

Growth-cones of vertebrate and invertebrate neurons turn towards the cathode of a weak **DC electric field** applied to the culture medium [23, 69].
This electric field guided neuronal outgrowth is called galvanotropism. It is based on the rearrangement of charged membrane proteins and receptors that are subject to an electrophoretic force. However, as most of these molecules bear negative excess charges outside the cell membrane, they should accumulate in the direction of the anode and promote growth towards it, away from the cathode. Electroosmotic effects might account for this contradictory behavior. Positively charged molecules surrounding the membrane (diffuse double layer) are driven towards the cathode, generating a flux of medium in this direction. The net force on the membrane proteins results from the superposition of the shear force created by the electroosmotic flux, and the electrophoretic force on the charged proteins themselves. Theoretical considerations and experiments have shown that, depending on membrane and protein parameters, this may result in proteins being pulled towards the anode or the cathode [70].
Furthermore, the electric field depolarizes the membrane facing the cathode opening voltage-dependent Na^+ and Ca^{2+} channels. Although the signalling cascades are not completely understood, Ca^{2+} seems to play an important role in controlling neuronal outgrowth, with the growth-cone moving towards higher internal Ca^{2+} concentrations [69]. Thus, the influx of Ca^{2+} makes the neurite grow towards the cathode.

Only recently, **light** was successfully used to guide growing neurites [27]. Unlike the established technique of optical tweezers, the laser power was too low to hold or move growth-cones. Instead, the light may influence biological processes by mediating the actin polymerization-driven extension of lamellipodia through weak gradient forces generated by the laser beam.

Pulsed magnetic fields have been shown to influence neuronal outgrowth [64], too. Dorsal root ganglia exposed to these fields exhibit asymmetric growth and an enhancement of neurite length. Unfortunately, the effect is not very controllable so far.

2.1.5 Which technique is best?

Out of the various techniques presented above, only a few are optimized sufficiently to reliably guide growing neurites. Even fewer fulfill the requirements arising from the combination with transistor chips for extracellular recording, listed in subsection 2.5.5.

In their present developmental stage, DC electric fields, light and pulsed magnetic fields are not suitable. Either guidance is too weak, as with light and magnetic fields, or it is very difficult, if not impossible, to control the growth of several neurites simultaneously, as in the case of constant electric fields applied with pipettes. However, light, electric and magnetic fields can be turned on and off whenever needed. This inherent flexibility makes them first choice for directing growth-cones to the left or to the right on

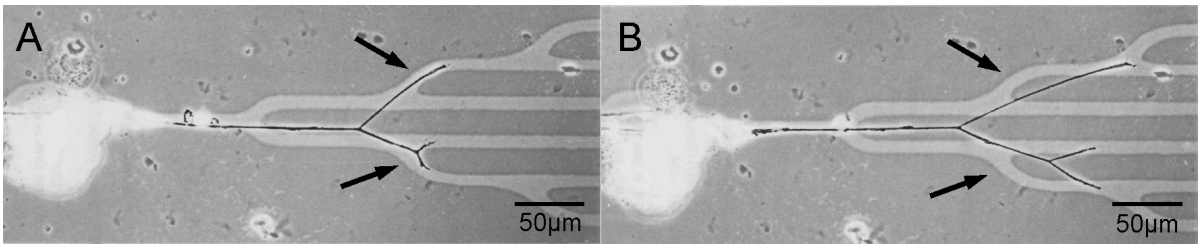


Figure 2.3: *Leech neuron growing on tracks of intact ECM proteins (bright grey) surrounded by regions of inactivated ECM. A: After 44h. B: After 68h. Pictures from [35].*

an intersection of chemical tracks [23].

Patterns of substrate bound molecules represent the most developed technique for controlling neuronal outgrowth *in vitro*. They reliably guide growing neurites and can be aligned to any flat structures, e.g. micro-electrode arrays. Most molecules conveying directional information are compatible with extracellular recording. Moreover, pathways made from silane have been reused several times in culture before losing their directive properties, which makes them very efficient with respect to labor and cost [23]. The major drawback with this technique is that the molecules frequently do not provide enough force to keep the network in the grown geometry. Fig. 2.3 shows how neurites initially grown on tracks of extracellular matrix proteins (ECM) get pulled off by forces generated by the advancing growth-cones. This problem is even more severe when somata are pulled away from electrodes or transistors as this makes extracellular recording impossible [50].

Topographic structures are promising since they confine cells and neurites to the desired areas on the substrate by mechanical forces strong enough to prevent any dislocation. For example, pillars arranged in a circle around FETs reliably retained somata on the gates [130]. Moreover, substratum topography can also control neurite outgrowth, as shown by many studies culturing neurons on groove ridge structures, see 2.1.3. Although not confirmed experimentally, there is no obvious reason why this technique might interfere with extracellular recording.

With the two latter approaches having their pros and cons, we decided to follow them both in the initial phase of the thesis: chemical patterns made from adsorbed growth-promoting factors and substrates with topographic structures.

2.2 Cell Culture

Choosing the right type of neurons and appropriate cell culture conditions is crucial for establishing chip-controlled neural networks. After a discussion of these issues, the isolation procedure for neurons and various cell culture methods are described. The section ends with an overview of the cleaning procedures applied to different types of substrates.

2.2.1 What neurons should be used?

As shown in section 2.1, many different types of neurons can be used for growing topologically defined networks. However, the combination with extracellular recording by FETs reduces the options considerably. Furthermore, not every neuron couples to the chip underneath (see 3.6.5 for details), making additional measurements with conventional microelectrodes necessary. This limits the number of cells that can be monitored at the same time to just a few. From these considerations the following criteria are deduced:

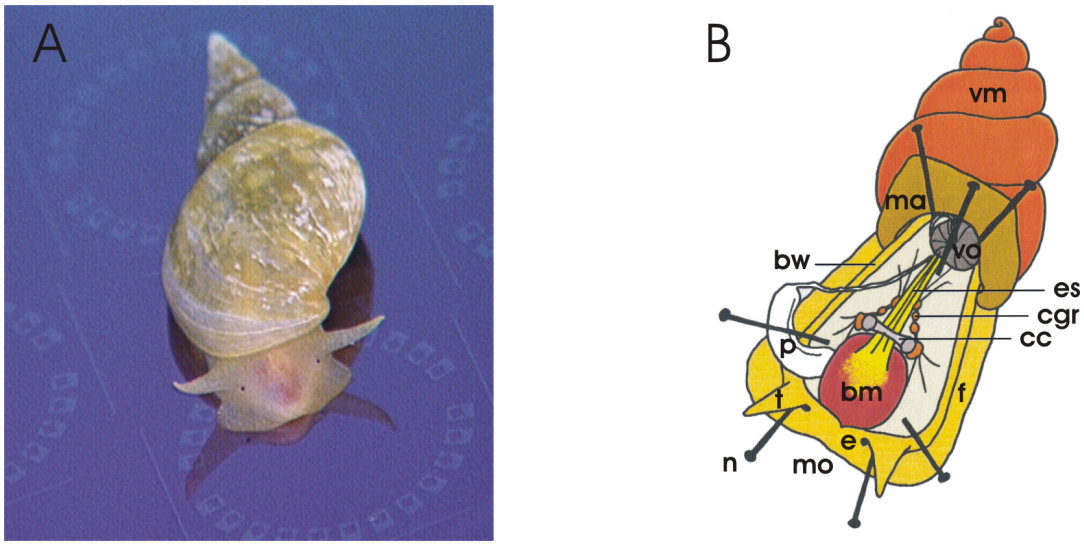


Figure 2.4: *A: Pond snail Lymnaea stagnalis on a Si-wafer. B: Schematic drawing of the dorsal view of the snail during preparation. n = needle, t = tentacle, p = penis, bw = body wall, ma = mantle, vm = visceral mass (deshelled), vo = visceral organs (pinned aside), es = esophagus, cgr = central ganglionic ring, cc = cerebral commissure, f = foot, bm = buccal mass, e = eye, mo = mouth; from [79].*

- large soma diameter to enable identification, isolation and positioning of individual cells
- reliable stimulation and recording of single action potentials with silicon chips
- formation of peripheral synapses
- strong synaptic connections with inputs from some or even just one neuron triggering post-synaptic action potentials
- small networks of only a few neurons should perform simple tasks of information processing

Although vertebrate neurons, e.g. rat hippocampal neurons, are frequently cultured on multielectrode arrays [40] and are used to build networks of defined geometry *in vitro* [95], they are not ideal for our experiments. Soma diameters in the range of just 10μm make the isolation and positioning of individual cells very difficult. Also, small neurons give rise to only small electrical signals, resulting in bad signal-to-noise ratios. So far, recording action potentials from individual rat hippocampal neurons with field-effect transistors was only possible when signals were averaged to reduce noise [114, 115]. In addition, functional neuronal units in vertebrates are generally rather complex, with single neurons receiving about 10^3 synaptic inputs. This makes the *in vitro* reconstruction of the functional units impossible.

These problems put the focus on invertebrates, particularly molluscs. Their large (sometimes more than 100μm in diameter) and robust cell bodies facilitate the isolation and positioning of neurons and give rise to acceptable signal-to-noise ratios. The first neuron-silicon coupling has been achieved with neurons from the leech *Hirudo medicinalis* [33] and many experiments have been done since [112]. Leech neurons also grow processes along predefined pathways of ECM proteins and seem to form neural networks. Despite these promising features, leech neurons are not used here because only very weak peripheral synapses are established *in vitro*, and at an extremely low yield [38, 93].

Lymnaea stagnalis is a freshwater snail that can be found in ponds all across Europe; fig. 2.4A shows a picture of the species. Its neurons have soma diameters up to 100μm and are known to form synaptic

connections *in vitro* [65, 66, 106]. Small networks of only a few neurons perform tasks such as generating the rhythm for feeding and breathing. Due to their simplicity, these networks are ideal for studying principles of information processing at a single cell level. N.I. Syed et al. were able to reconstruct the central pattern generator that controls the animal's breathing rhythm, from dissociated neurons *in vitro* [105]. However, these identified neurons, R.Pe.D1, V.D4 and Ip.3.1, are difficult to isolate. Generally, the number of cells forming chemical synapses in culture is very small.
The A-clusters of the two paired pedal ganglia comprise about 60 cells with similar electrophysiological properties [98] and electrical synapses between them [58]. Due to the large number and diameters ranging from 40μm-70μm, A-cluster neurons are ideal for designing artificial neural networks *in vitro*.
A more pragmatic reason for choosing *Lymnaea stagnalis* and not *Aplysia californica*, an even better analyzed mollusk with equally promising neural properties, as a neuron donor is *Lymnaea's* simple and robust nature and its availability. The snails are kept in four 200L basins that are cleaned twice a week. They are fed on lettuce and fish food pellets. To prevent inbreeding or population decreases due to reproduction rates not matching the number of animals needed, new snails are added at irregular intervals. A quarantine basin prevents the contamination of the laboratory stock with parasites.

2.2.2 Culturing neurons from *Lymnaea stagnalis*

The isolation and culture of *Lymnaea* neurons follows protocols from the literature [90, 107], with minor modifications. For a detailed, well illustrated description see [49].
All steps, except the removal of the shell, are executed under sterile conditions in a flowhood. Dissection instruments are either autoclaved or soaked in a solution of 70% ethanol and 30% water prior to the preparation. The entire procedure is divided into two parts, the isolation of individual neurons including their positioning on the chip, and the subsequent cell culture to enable neuronal outgrowth and synapse formation. While the general aspects are outlined below, details of single steps and recipes for solutions and culture media are described in appendix A.

Isolation of individual cells

Animals with a shell length of 1.5cm-2cm are selected from the laboratory stock and deshelled. They are soaked in antibacterial solution for 5min to remove dirt and bacteria and to anaesthetize them. They are then pinned to a culture dish with a rubber coating at its bottom which is filled with antibiotic normal saline (ABS). An incision is made on the dorsal surface from the mouth to the visceral mass. The body wall and internal organs are pinned aside to expose the brain, consisting of a loop of ganglions located at the end of the buccal mass, see fig. 2.4B for a sketch of the snail at this stage of the preparation. Next, the cerebral commissure and the esophagus are cut with fine scissors and the buccal mass is removed. After cutting the remaining nerves connecting the ganglia to the body, the central ganglionic ring is transferred to a small dissection dish also filled with saline.

To extract individual neurons, the brains are pinned to the rubber coated dish and the outer sheath, the connective tissue surrounding the ganglia, is carefully removed with fine tweezers. The saline is exchanged to remove debris and tissue parts. Central ganglionic rings now look like the one shown in fig. 2.5A. After 15min, during which the brains recover from the previous step, they are treated with an enzyme solution for 27min-33min. The enzymes partly digest the extracellular matrix, thus facilitating the isolation of individual neurons from the ganglia. The brains are then washed three times with defined medium to remove the enzymes and are incubated in trypsin inhibitor for 15min, which inactivates any trypsin remaining in spite of the previous washes. Following three more washes, the medium is replaced with high osmolarity defined medium. The increased osmolarity causes a slight shrinkage of the neurons that makes the somata less susceptible to mechanical damage and facilitates their isolation. The inner connective tissue sheath surrounding each ganglion is opened with a microneedle, and indi-

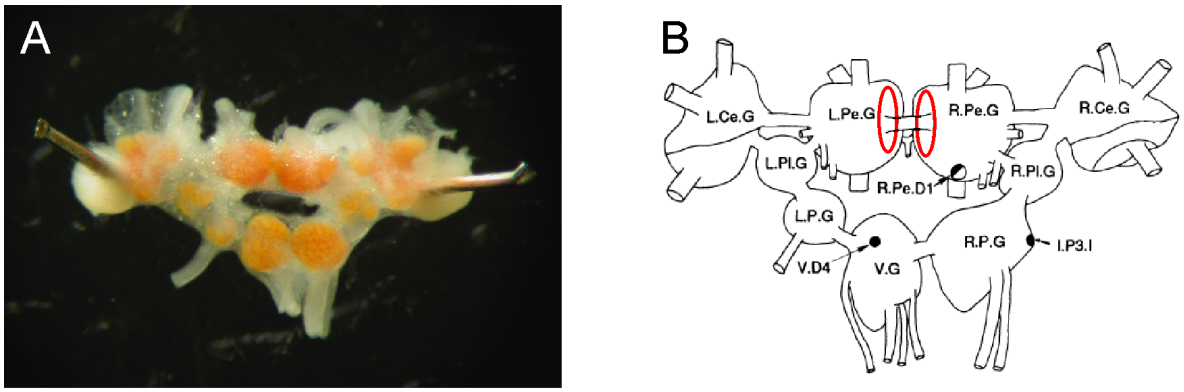


Figure 2.5: *A: Dorsal view of a central ganglionic ring pinned to a dissection dish after removal of the outer sheath. B: Schematic drawing with the A-clusters of the left and right pedal ganglion marked in red. The neurons forming the central pattern generator for respiration are also highlighted.*

vidual neurons are removed with a glass micropipette by aspiration. To check the vitality, neurons are gently flushed out of the pipette and optically inspected after settling to the bottom of the dish. Healthy cells have a pearly shine and an intact cell membrane. Only these are transferred to the prepared culture chamber and placed in the pits on the substrate. Culture chambers are incubated at 20°C in a humid environment to prevent evaporative loss of medium. Neuronal outgrowth begins a few hours after plating the cells and lasts for several days.

About 10-15 vital neurons can be extracted from the A-cluster regions of the paired pedal ganglia. Therefore, 6 to 8 brains are usually processed in parallel to provide enough cells for up to six transistor chips to be prepared at the same time.

Cell culture methods

While *Lymnaea* neurons can survive for several days in plain defined medium, neurotrophic factors are needed to promote the outgrowth of neurites [125]. These presumably proteinaceous substances are released from snail brains directly into the defined medium in which they are incubated. Although nerve growth factor has a similar effect on some types of brain cells, the composition of the secreted substances is more complex and not yet known [90].
There are several ways to deliver these factors, which are essential for the growth of neural networks *in vitro*, to the neurons in the culture dish. They all depend on brains for growth factor production. Central ganglionic rings are isolated from animals with a shell length of about 3cm, following the first part of the procedure outlined above. They are transferred to Falcon 3001 culture dishes and incubated for roughly two hours in antibiotic saline that is exchanged five times during this period. After this treatment the tissue is sterile and ready to be used in one of the methods described below:

Conditioned medium (CM): A convenient and common way to deliver growth factors to neurons is the use of brain conditioned medium [66, 107]. Central ganglionic rings are incubated in defined medium at a concentration of 2brains/ml in a humid environment. A glass culture dish coated with Sigmacote SL2 (Sigma) is used to reduce loss of proteins. After 72h the supernatant is filtered through a low protein binding syringe filter, shock frozen in cryovials and stored at -20°C in the freezer. The CM is thawed prior to use and filled into the culture chambers.
However, this elegant method did not produce satisfactory results, neuronal outgrowth was poor. Possible reasons might be excessive protein loss during numerous media transfers due to proteins adhering to the surfaces of the syringe, vials etc., or unknown contamination of the CM.

Substrate adsorbed material (SAM): This method is based on the adhesive properties of the trophic factors that adhere very well to poly-L-lysine coated substrates, forming a robust layer of growth-promoting proteins [79, 124]. *Lymnaea* brains are incubated directly in the culture chamber at 2brains/ml medium for 72h. Before plating the neurons, the brains are removed and the supernatant is either diluted 1:1 or completely replaced by defined medium. The growth factors attached to the bottom of the chamber are sufficient to promote vigorous neurite outgrowth.
Layers of SAM are also used to grow topologically defined networks with a technique described in 2.3.1. However, SAM is incompatible with extracellular recording by transistors. The adsorbed proteins form a cushion on the chip surface, thereby increasing the distance between transistor and neuron, obstructing a successful neuron-silicon coupling.

Co-culture: The drawbacks of the aforementioned methods can be avoided if neurons and brains are cultured together, with the ganglionic rings added after the neurons are plated. This allows the neurons to adhere tightly to the uncovered sticky poly-L-lysine coated surface of the substrate, while the growth factors are delivered directly to the medium without any loss. As no proteins are present at the time neurons are placed and secretion starts only after brains are added to the medium, neuronal outgrowth is delayed for about one day compared to the other methods. The overall success of the co-culture is not affected by this.

2.2.3 Cleaning of substrates

Before neurons were plated, the substrates had to be cleaned, sterilized and coated with poly-L-lysine. The two latter steps, being rather simple, are described in appendix A, whereas cleaning is discussed here since it turned out to be problematic. It must be aggressive enough to reliably remove tissue and debris from previous cell cultures, yet mild enough so as not to affect the substrates. As substrates became more sophisticated, the demands on the cleaning procedure increased as revealed by the following list:

Glass coverslips: Round cover glasses (diameter 30mm, thickness 1, Assistent) were treated with acidic and alkaline detergent in an ultrasonic cleaner at 80°C according to a procedure adapted from [34] (for details see appendix A). The coverslips were only used once.

Substrates with topographic structures: Topographic structures consist of polyimide or SU-8 polyester photoresist processed onto glass coverslips and oxidized silicon wafers, see subsection 2.3.2. Due to internal stress and a different thermal expansion coefficient than the underlying substrate, the resist layers peel off upon prolonged sonication and temperature shocks. To meet these new requirements, the previously described procedure was modified. While the time the substrates were immersed in the detergents was not altered, the temperature was reduced to 50°C and the overall sonication time was limited to 5min. Preheated water was used for rinsing to avoid thermal shock. The method allowed substrates to be recycled five times before the resist began to peel off, but was efficient enough to reliably remove tissue and dirt in the pits and grooves of the topographic structures.

Transistor chips: Transistor chips are rather complex devices with many different materials (SiO_2, polyester resist, silicone adhesive and PMMA) exposed to the cell culture and thus to subsequent cleaning. For a detailed description of the chips refer to subsection 3.3.2 and fig. 3.6.
Without the topographic structures, removal of tissue and debris would be easy; mild detergent and Q-tips for a slight scrubbing are sufficient for conventional chips [49]. However, feature sizes down to 14μm render the mechanical cleaning of the chips here difficult. There are no brushes with bristles that fit in the narrow grooves. Methods solely based on chemical treatment are problematic though, because they either are too aggressive to the device or the results are not satisfactory, with impurities

remaining in the structures. The following list shows various procedures tested throughout this study. All chips were precleaned with Q-tips and a pressurized water jet to mechanically remove as much tissue as possible.

- The alkaline detergent of the process described above has pH14. It etches the gate oxide at a considerable rate (0,5Å/min at 80°C [59]), leading to a quick failure of the transistors if devices are exposed to the solution for extended times. To minimize negative effects on the gate oxides, the liquid was applied for only 2 minutes and sonication was omitted completely to prevent damaging the structures. The cost of these modifications were modest results with tenacious dirt remaining in the grooves.
- A lukewarm solution of dishwasher detergent proved very efficient. Organic material was dissolved within minutes, leaving a clean surface even within the structures. The gate oxide does not deteriorate because the solution has a rather mild pH11. Moreover the detergent was applied for only 5min. Despite these promising features, neuronal outgrowth was poor on chips subjected to this procedure and many neurons died.
- Treatment with the enzymes collagenase dispase and trypsin or with contact lens cleaner was not satisfactory; not all cell rests were removed.
- In [129] a hot, very reactive mixture of 2:1v/v H_2SO_4 and H_2O_2, called piranha solution was used on chips with polyimide columns. Due to their larger surface and different material properties, the topographic structures here are much more susceptible to thermal shock than the columns. To prevent SU-8 resist from peeling off, only cold solution could be used. The decreased activity was compensated by increasing the residence time to 90s. Unlike the procedure described in [129], only small drops of piranha solution were applied to the center of the chip with conventional plastic pipettes. Any contact between drops and culture chamber had to be avoided, since the acid dissolved the silicone adhesive, leaving a whitish scum on the chip. If executed correctly the chips were clean after the procedure and could be reused many times.
- Instead of piranha solution, chromosulfuric acid was applied for 3 x 15s following the same protocol. Results were very good, as no tissue remained on the chip. Except for minor damage to the PMMA chamber if it came in contact with the liquid, the device was not affected at all. However, the analysis of I-V curves revealed a strong effect of the Cr ions on the transistor characteristics, see 3.3.3. Since chromosulfuric acid is very toxic, a thorough rinsing was mandatory afterwards.
- Ordinary dishwashing liquid assisted by mechanical scrubbing with a brush is a mild way for removing dirt. While the chamber walls and even the pits of the topographic structures got perfectly clean, some tissue remained in the grooves because they were not accessible to the brush.

After cleaning, no matter which protocol was used, the chips were washed several times with the pressurized water jet to remove detergent and rinsed frequently during at least 3h. Milli-Q water (Millipore) was used throughout all steps.
Except for the dishwasher detergent, all protocols provided chips that did not harm cells and enabled neuronal outgrowth. Due to the varying success of cell culture, many different procedures were tested. At the moment, none of them allows reliable results. Sometimes many neurons were vital and grew processes that followed the grooves, sometimes survival and growth was poor. Whether this can be solely ascribed to the cleaning protocol, or if other factors are involved remains unclear; see the discussion in 2.5.5.

2.3 Building defined networks - technological aspects

Initially, two techniques were tested for growing defined networks with snail neurons, one based on chemical patterns, the other on surface topography. Their technological aspects are presented in the following paragraphs, detailed parameters for SU-8 processing are listed in appendix B.

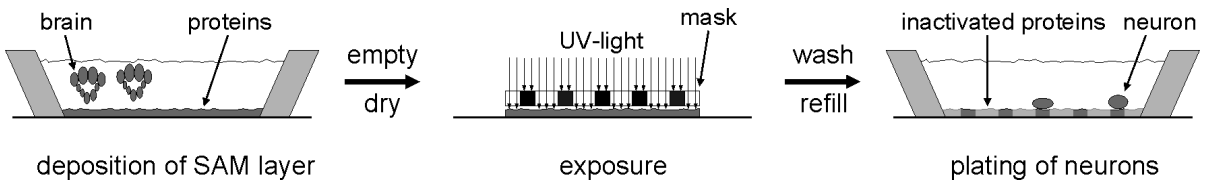


Figure 2.6: *Schematic illustration of the patterning procedure.*

2.3.1 Patterns of growth-promoting proteins

Tracks of intact extracellular matrix proteins (ECM) surrounded by UV-inactivated areas have shown to reliably guide growing leech neurites [35]. This technique has been adapted to the requirements of *Lymnaea* neuronal cell culture by A. Prinz [79]. Instead of ECM, substrate-adsorbed material (SAM) is patterned with UV light. The procedure involves the following steps, which are also illustrated in fig. 2.6:

- deposit a layer of SAM on glass coverslips as described in section 2.2.2
- remove conditioning brains, supernatant and flexiPERM adhesive culture chambers (*in vitro* Systems & Services, Osterode, Germany) and dry the coated coverslips in a sterile flow hood
- 20min exposure to the full spectrum of a 200W mercury lamp (Osram HBO 200, intensity of the 366nm-line approximately 170mW/cm^2) through a lithographic mask in direct contact with the proteinacious layer
- remove the mask and rinse with defined medium to wash away denatured protein from exposed areas
- attach flexiPERM chamber and refill with DM or a 1:1 mixture of DM and supernatant
- place neurons on the patterned substrate and cultivate for two to three days

Masks consist of 1mm-2mm thick silica plates transparent to UV light. They are coated with a thin but nontransparent layer of aluminum into which the desired patterns are etched [35].

To avoid any contamination, the entire procedure, including UV exposure, is carried out under a sterile flowhood and the masks are immersed in a solution of 70% ethanol and 30% water for 30min prior to use.

2.3.2 Topographic structures

The first topographic structures were made from the n-type **polyimide photoresist HTR3-200** (Olin GmbH, Munich, Germany) processed onto glass coverslips and pieces of Si-wafers. Process parameters and steps are similar to those described in [129]. Although compatible with cell culture and resistant to all cleaning procedures, including the short application of piranha solution (see 2.2.3), structures made from polyimide are not satisfactory. Resolution and feature accuracy is poor, especially for deep, narrow grooves with aspect ratios of 2 or higher (ratio of structure height to width). Also polyimide layers of 10μm thickness or more detach frequently at the sides of the grooves, leaving a gap between substrate and resist into which neurites can grow; as shown in fig. 2.7. Due to these limitations, HTR3-200 is not used any more for making topographic structures directly in contact with cell culture.

Nevertheless, thin polyimide layers with well resolved features are ideally suited as sacrificial masks for etching the structure directly into the substrate underneath. However, the RIE80 Plasmalab etcher (Oxford Instruments) available in the departmental cleanroom facility cannot etch silicon anisotropically. Walls of grooves are not vertical but inclined, reducing the directional information drastically, with many neurites leaving the guidance structure. Etching topographic structures directly into the substrate was not followed any further, even though there are ways to process vertical walls into silicon,

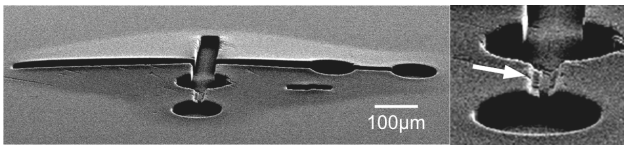
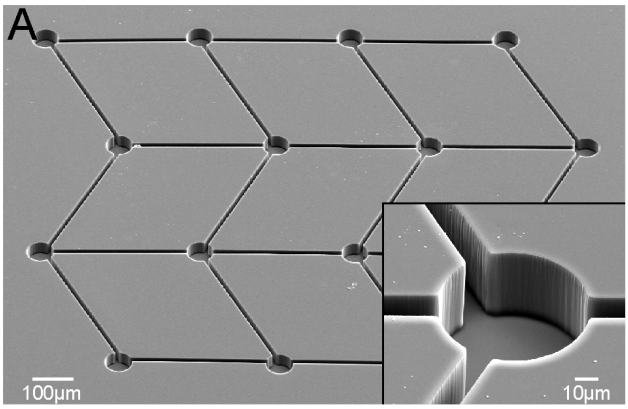


Figure 2.7: *Electron micrograph of a partly detached layer of polyimide after several days in cell culture. The white arrow points to a poorly developed narrow groove connecting two pits.*



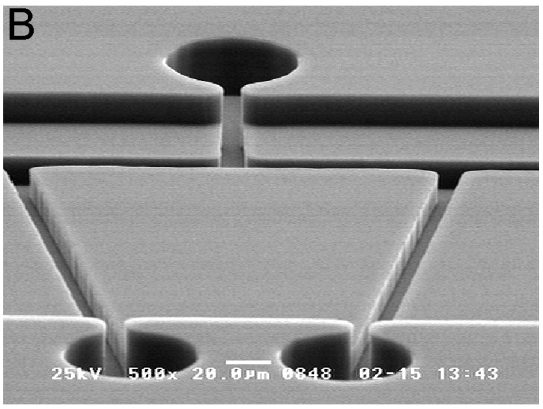


Figure 2.8: *A: Electron micrograph of a one-layer SU-8 structure consisting of an array of 16 pits with 70μm diameter and 14μm wide connecting grooves. The overall height is about 25μm. B: Two layer structure. Both layers are approximately 15μm thick.*

e.g. with cryo etching or plasma chopping [86]. The approach is not compatible with the processing of transistors on the same substrate, since the deep pits and grooves are not accessible with established semiconductor technologies such as photolithography. The only feasible way is to deposit topographic structures on top of an already existing transistor chip.

SU-8 is a rather new polyester photoresist with excellent lithographic qualities. Aspect ratios of 10 and more can be attained with it. Like HTR3-200, it is a n-type photoresist, which means that material in exposed areas is crosslinked and resist in unexposed areas is dissolved during development. In general, this photoresist type is compatible with cell culture, as is SU-8, in marked contrast to most p-type resists, which are toxic.

Processing SU-8 comprises the following steps: cleaning the substrate, dehydration bake, spin-on of resist, softbake, bead removal, exposure in a mask-aligner, post exposure bake, development and an optional hardbake; process parameters are listed in appendix B.

The first two steps are detrimental for a good resist-to-substrate adhesion. During softbake, solvent evaporates from the liquid SU-8 so that it solidifies. To avoid any deterioration of structural resolution due to proximity effects, the beads forming at the wafer's rim in previous steps are removed with acetone. This allows the mask to be in direct contact with the resist. After exposure the SU-8 layer is heated again; the so-called post exposure bake makes the illuminated areas more resistant to the solvent applied in the subsequent development. An optional hardbake at the end crosslinks the polyester resist even further, resulting in an extreme resistance to harsh chemicals; it even withstands concentrated sulfuric acid for some time and presumably is chemically more inert, which is important for the biocompatibility required in cell culture. However, this final step drastically increases mechanical stress within the resist layer, promoting peel-off at the edges. A strong mismatch in thermal expansion coefficients between SU-8 and silicon substrate accounts for this adverse property. Its negative effects can be minimized by avoiding temperature shocks applied to the finished device and using shallow temperature ramps throughout all thermal processing steps.

The topographic structures in this study consisted of pits with 70μm and 80μm diameter for taking up the cells and $14\mu m$ wide connecting grooves, see fig. 2.8A. Their overall height ranged from 10μm to 40μm. Note the perfectly vertical walls shown in the inset, they are essential for controlling neuronal outgrowth and confining cells to the pits.

Although a structure height of 10μm is sufficient to reliably guide growing neurites and retain them in the grown geometry, somata are sometimes pulled out of the pits, as they are too shallow, especially to confine large cell bodies. By increasing the resist thickness to 30μm-40μm even large somata are kept in place, but at the cost of a poor visibility of neurites at the bottom of the grooves. Diffraction at the edges of the groove walls diminishes optical resolution with increasing structure depth.
This dilemma is elegantly solved by processing two resist layers on top of each other. A single thin layer for guiding neurites while not impairing visibility and two layers in areas surrounding the somata to provide enough force to keep them in place. The process is adapted from the single layer process, but slightly more complex. Its first steps, including the post exposure bake, are identical to those described above, but are then followed by: spin-on of second resist layer, softbake, bead removal, second exposure, post exposure bake, development and hardbake. As the first resist layer remains photosensitive in areas not illuminated in the first exposure, care must be taken that the second mask also protects them during the second exposure, otherwise the first pattern is overwritten by the second. This constraint limits the three-dimensional features that are accessible with the procedure, e.g. bridges and covered conduits cannot be made, as they require an exposed layer on top of unexposed areas, see [44] for a technique to build these structures. Fig. 2.8B depicts such a two layer device, again note the vertical walls and the perfectly aligned second layer.

2.4 Theory part I: Neurons, synapses and cables

Understanding the behavior of an entire neuronal network at the basic level requires profound knowledge about its building blocks, namely neuronal somata, neurites and synapses; a theory describing these building blocks is presented in this section.
All neurons used throughout the study only form electrical synapses, which also transmit negative, hyperpolarizing signals; in contrast to chemical synapses. Because of this behavior the voltage-independent synaptic conductances can be determined with a passive model. The model implies that all parameters, such as synapse and membrane conductance, do not depend on the transmembrane voltage. These conditions can be experimentally realized best, when neurons are hyperpolarized. Based on these assumptions, subsection 2.4.1 and 2.4.2 present equivalent circuits and related equations for a single soma, a soma with neurites and small networks.
More complex neuronal behavior, such as the generation of action potentials, can only be described with an active model including voltage-dependent conductances, as outlined in 2.4.3.

2.4.1 Passive model and cable theory

The isolated soma is the elementary unit of all neural networks. In a passive model its equivalent circuit is represented by a single, isopotential compartment with a capacitance C_s in parallel to an ohmic conductance G_s and a battery V_0, see fig.2.9A. C_s and G_s are properties of the soma membrane (index s), the resting potential V_0 is generated by different ionic concentrations between intra and extracellular space; for more details refer to subsection 2.4.3. A current I_{inj} injected into the cell via an electrode charges its capacitance and leaves through the membrane conductance. The dynamics of the somatic membrane voltage, V_s, of this circuit is described by the following differential equation:

$$I_{inj} = C_s \frac{dV_s}{dt} + G_s(V_s - V_0) \tag{2.1}$$

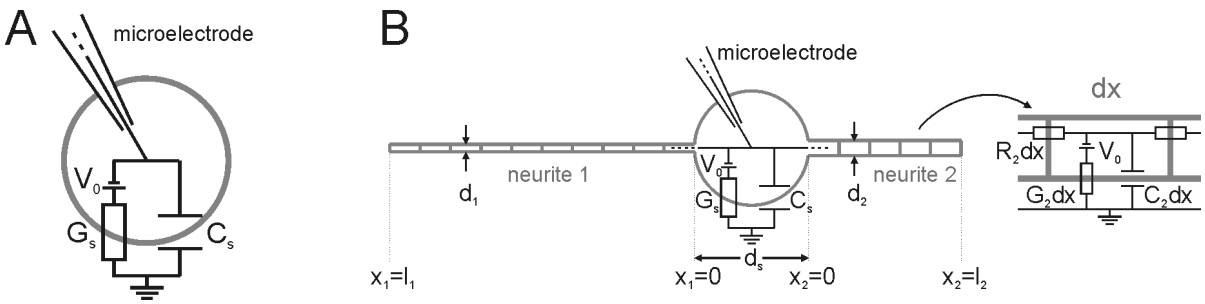


Figure 2.9: *A: Equivalent circuit of a neuronal soma with passive membrane. B: Passive model of a neuron with neurites. Soma and neurites can have different membrane conductance and capacitance, but the same cytoplasmic resistance r.*

Its solution for a current step from $I_{inj,0}$ to $I_{inj,\infty}$ applied at time zero is given by:

$$V_s(t) = V_\infty + \frac{I_{inj,0} - I_{inj,\infty}}{G_s} e^{-\frac{t}{\tau_s}} \tag{2.2}$$

This monoexponential voltage transient decays with the time constant $\tau_s = C_s/G_s$ governed by the cell membrane. $V_\infty = V_0 + I_{inj,\infty}/G_s$ is the steady state voltage after the current step.

The realistic description of an individual neuron as part of a network must include neurites, along which electrical signals are exchanged. In contrast to somata, long, thin neurites can usually not be considered isopotential because changes of the somatic membrane potential decrease as they propagate from the cell body to the tip of the neurite. This is due to electrical currents leaving via the neuritic membrane and charging the membrane capacitance, as well as to the voltage drop caused by the finite conductance of the cytoplasmic solution inside the neurite.

W. Rall [85] derived a differential equation for the potential distribution in a passive neuron with neurites under the following set of assumptions: neurites are cylindrical, uniform electrical properties over the entire surface of the neuron, constant extracellular potential, isopotential soma, intracellular potential and currents are continuous throughout the entire neuron, axial ohmic resistance inside the neurite is proportional to its cross-sectional area; the equivalent circuit for a patch of membrane consists of an ohmic resistance in parallel to a capacitance with a constant electromotive force in series to the resistance.
Problems with fitting voltage and current transients calculated from the Rall model to experimental data led to a more general version, the 'somatic shunt cable model' [25]. The postulate of uniform electrical properties is abandoned, the soma can have different membrane capacitance and conductance than the neurites. These generalizations are the basis for the equivalent circuit depicted in fig. 2.9B. The somatic conductance G_s and capacitance C_s are the product of the soma-specific quantities and the somatic membrane area, with d_s denoting the diameter of the cell body.

$$G_s = g_s \pi d_s^2 \qquad \text{and} \qquad C_s = c_s \pi d_s^2 \tag{2.3}$$

For practical reasons the respective neurite parameters are defined as quantities per unit length and are calculated from the specific values c and g according to:

$$G_j = g\pi d_j \qquad \text{and} \qquad C_j = c\pi d_j \qquad \text{and} \qquad R_j = \frac{4r}{\pi d_j^2} \tag{2.4}$$

R_j is the axial ohmic resistance of neurite j and r is the specific resistance of the cytoplasm inside. Note that while different neurites can have diverse diameters d_j, resulting in different values of R_j, their specific electrical properties g, c and r are identical for all.

From fig. 2.9 a differential equation is derived that describes the voltage dynamics in neurites [57], the 'cable equation'

$$\lambda_j^2 \frac{\partial^2 V_j^e}{\partial x_j^2} = V_j^e + \tau \frac{\partial V_j^e}{\partial t} \tag{2.5}$$

with the deviation of the membrane potential from the resting potential in neurite j, the electrotonic potential

$$V_j^e = V_j - V_0 \tag{2.6}$$

and the neuritic space and time constants λ_j and τ

$$\lambda_j = \sqrt{\frac{d_j}{4gr}} \qquad \text{and} \qquad \tau = \frac{c}{g} \qquad . \tag{2.7}$$

Throughout the literature equation 2.5 is frequently used in its normalized version:

$$\frac{\partial^2 V_j^e}{\partial X_j^2} = V_j^e + \frac{\partial V_j^e}{\partial T} \tag{2.8}$$

where $X_j = x_j/\lambda_j$ is the normalized distance from the soma, the so-called electrotonic distance, which depends on d_j and $T = t/\tau$ the normalized time.

The linear cable equation given above is a partial differential equation which is quite similar to the heat and diffusion equation. Its behavior is characterized by dissipation without any wavelike solution. To solve it, appropriate initial and boundary conditions must be specified. For the axial resistance at the neurites' distal end any value from zero to infinity is theoretically possible. The killed end boundary condition assumes zero resistance, i.e. a short circuit between the intra and extracellular potential. It is of little biological relevance, as the neurite must be physically cut open to meet it. More realistic is the case of infinite resistance, the sealed end boundary condition, if the actual value is not known.
Setting $\partial V_j^e/\partial T = 0$ in equation 2.8 yields the time-independent distribution of the electrotonic potential, e.g. resulting from a current step applied to the soma after initial transients have decayed.

$$\frac{\partial^2 V_j^e}{\partial X_j^2} = V_j^e \tag{2.9}$$

Its general steady state solution for the electrotonic potential in neurite j, $V_j^e(X_j)$, governed by the electrotonic potential at the soma, V_s^e, is:

$$V_j^e(X_j) = \left[\frac{V_s^e}{\cosh L_j} - \lambda_j R_j I_j(L_j) \tanh L_j\right] \cosh(L_j - X_j) + \lambda_j R_j I_j(L_j) \sinh(L_j - X_j) \tag{2.10}$$

where $L_j = l_j/\lambda_j$ is the electrotonic length, with l_j denoting the physical length of the neurite j. $I_j(X_j)$ is the axial current along neurite j at the distance X_j from the soma given by [85]:

$$I_j(X_j) = -\frac{1}{\lambda_j R_j} \frac{\partial V_j^e}{\partial X_j} \tag{2.11}$$

Inserting 2.10 into 2.11 yields:

$$I_j(X_j) = \left[\frac{V_s^e}{\lambda_j R_j \cosh L_j} - I_j(L_j) \tanh L_j\right] \sinh(L_j - X_j) + I_j(L_j) \cosh(L_j - X_j) \tag{2.12}$$

Using the sealed end boundary condition, implying $I_j(L_j) = 0$, simplifies the equations above to:

$$V_j^e(X_j) = \frac{V_s^e}{\cosh L_j} \cosh(L_j - X_j) \tag{2.13}$$

$$I_j(X_j) = \frac{V_s^e}{\lambda_j R_j \cosh L_j} \sinh(L_j - X_j) \tag{2.14}$$

Thus, the overall current leaving the soma through the sealed end neurite j is:

$$I_j(X_j = 0) = \frac{\tanh L_j}{\lambda_j R_j} V_s^e \tag{2.15}$$

The time dependent solution of the cable equation is substantially more complex than the steady state case above [111]. It was solved for voltage and current steps as well as short current pulses applied to a cell body with arbitrarily many neurites [79]. An analytical solution could be derived only for the voltage step, the two latter cases lead to equations that could not be solved completely. Fitting the theoretical model to experimental data of signal propagation in neurites determined from optical recordings with voltage sensitive dyes, A. Prinz obtained the following values for the specific conductivity g of the neurite membrane and the specific resistance of the cytoplasm r inside the neurites of *Lymnaea stagnalis* [79]:

$$g = (0.035 \pm 0.007)\text{mS/cm}^2 \quad \text{and} \quad c = 1.0\mu\text{F/cm}^2 \quad \text{and} \quad r = (394 \pm 137)\Omega\text{cm}$$

c is taken from the literature and kept constant in the fit. The respective values for the soma membrane are:

$$g_s = (0.020 \pm 0.017)\text{mS/cm}^2 \quad \text{and} \quad c_s = (1.1 \pm 0.4)\mu\text{F/cm}^2$$

Because of their rather large diameter in cell culture, which is about 5μm, and the electrical membrane parameters above, the space constant for snail neurites is $\lambda \approx 950\mu$m. Neurites considerably shorter than λ, i.e. with an electrotonic length $L < 1$, are called electrotonically compact. They are quasi isopotential to the soma and signal propagation is very fast. For snail neurites this can be clearly seen in the spatio-temporal maps of signal propagation shown in [79]. There is almost no delay between the signal in the soma and in the distal parts of the neurites. Additionally, these experiments support the sealed end boundary condition implied to solve the cable equation.

2.4.2 Neural networks

So far only individual neurons with their neurites have been considered. In networks, these building blocks are connected by synapses, which are purely electrical for A-cluster neurons from *Lymnaea stagnalis*.
Electrical synapses are part of a class of cell-cell contacts called gap junctions. They are established from two hemichannels, one from each neuron. Each hemichannel consists of six monomeric subunits with four transmembrane helices. Compared to other ion channels the pore size of gap junctions is relatively large, with 1nm-3nm diameter, allowing the nonspecific passage of ions and molecules with molecular weights up to 1,000Da. Because of these features, the electrical behavior of such a synapse is well described by an ohmic conductance and a passive model can be used to determine the actual value of the conductance.

Isopotential model

The equivalent circuit depicted in fig. 2.10 is the simplest model for a synaptically connected neuron pair. Neglecting the cable properties of the connecting neurites introduces only minor errors if their

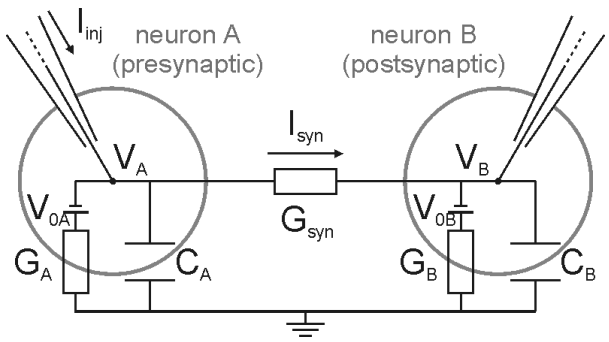


Figure 2.10: *Simple model of two electrically coupled neurons. In this equivalent circuit each cell is represented by a single isopotential compartment. Neuron A is presynaptic, B postsynaptic.*

overall length is much smaller than λ, that means if they are electrotonically compact; for details refer to the previous subsection.
Note that throughout this subsection voltage, capacitance and conductance are somatic quantities; the index 's' used in the previous subsection to distinguish between somatic and neuritic quantities is omitted here. Capital letters denote the respective neuron the variable refers to.
Injecting a constant current I_{inj} into neuron A causes a voltage response $V_A(t)$ in the presynaptic cell that is governed by the following differential equation, with G_{syn} denoting the conductance of the synapse and V_{0A} the resting potential of neuron A:

$$I_{inj} = C_A \frac{dV_A}{dt} + G_A(V_A - V_{0A}) + G_{syn}(V_A - V_B) \tag{2.16}$$

The current flowing across the synapse changes the voltage in the presynaptic neuron B, $V_B(t)$, according to the current balance:

$$G_{syn}(V_A - V_B) = C_B \frac{dV_B}{dt} + G_B(V_B - V_{0B}) \tag{2.17}$$

After transients have decayed, i.e. in the steady state where $dV_A/dt = dV_B/dt = 0$, the somatic voltages of A and B are:

$$V_A = V_{0A} - \frac{G_B G_{syn}(V_{0A} - V_{0B})}{G_A G_B + G_{syn}(G_A + G_B)} + \frac{G_B + G_{syn}}{G_A G_B + G_{syn}(G_A + G_B)} I_{inj} \tag{2.18}$$

$$V_B = V_{0B} + \frac{G_A G_{syn}(V_{0A} - V_{0B})}{G_A G_B + G_{syn}(G_A + G_B)} + \frac{G_{syn}}{G_A G_B + G_{syn}(G_A + G_B)} I_{inj} \tag{2.19}$$

Even if $I_{inj} = 0$, V_A and V_B are not equal to the resting potentials if $V_{0A} \neq V_{0B}$. This deviation is caused by a small permanent current which flows across the synapse, pulling the membrane voltages towards each other and away from the resting values.

All unknown electrical parameters of the simple network in fig. 2.10, except for the membrane capacitances, can be obtained from steady state current measurements. In that case, current balances for each neuron before (index: 0) and after (index: ∞) a current step from $I_{inj,0} = 0$ to $I_{inj,\infty}$ are given by:

$$0 = G_A(V_{A,0} - V_{0A}) + G_{syn}(V_{A,0} - V_{B,0}) \tag{2.20}$$

$$I_{inj,\infty} = G_A(V_{A,\infty} - V_{0A}) + G_{syn}(V_{A,\infty} - V_{B,\infty}) \tag{2.21}$$

$$G_{syn}(V_{A,0} - V_{B,0}) = G_B(V_{B,0} - V_{0B}) \tag{2.22}$$

$$G_{syn}(V_{A,\infty} - V_{B,\infty}) = G_B(V_{B,\infty} - V_{0B}) \tag{2.23}$$

A is presynaptic and B postsynaptic.
Eliminating V_{0B} by subtraction of 2.22 and 2.23 yields an expression which is frequently used in the literature to characterize electrical synapses. The coupling coefficient $k_{A,B}$ is defined as the ratio of the stationary postsynaptic and presynaptic response of the membrane voltage to a hyperpolarizing current step

$$k_{A,B} = \frac{\triangle V_B}{\triangle V_A} = \frac{V_{B,\infty} - V_{B,0}}{V_{A,\infty} - V_{A,0}} = \frac{G_{syn}}{G_B + G_{syn}} \tag{2.24}$$

Although this parameter describes the synapse in its function by quantifying the impact of a presynaptic voltage change on the postsynaptic neuron, it conveys little information about the synapse itself. For a given pair of neurons, $k_{A,B}$ can attain two values, depending on which neuron is postsynaptic with the respective membrane conductance G_B. The real parameter characterizing the behavior of an electrical synapse, namely its conductivity G_{syn}, is obtained from 2.20 and 2.21 by solving for G_A and equating the two terms.

$$G_{syn} = \frac{V_{A,0} - V_{0A}}{V_{A,\infty}V_{B,0} - V_{A,0}V_{B,\infty} - V_{0A}(\triangle V_A - \triangle V_B)} I_{inj,\infty} \tag{2.25}$$

Dividing 2.22 by 2.23 gives the resting potential of neuron B in terms of the membrane voltages before and after the current step.

$$V_{0B} = \frac{V_{A,\infty}V_{B,0} - V_{A,0}V_{B,\infty}}{\triangle V_A - \triangle V_B} \tag{2.26}$$

Furthermore, from equations 2.20 to 2.23 the following expressions for the membrane conductivities of cell A and B are derived:

$$G_A = \frac{V_{B,0} - V_{A,0}}{V_{A,\infty}V_{B,0} - V_{A,0}V_{B,\infty} - V_{0A}(\triangle V_A - \triangle V_B)} I_{inj,\infty} \tag{2.27}$$

$$G_B = \frac{V_{A,0} - V_{0A}}{V_{B,0} - V_{0B}} \cdot \frac{V_{A,0} - V_{B,0}}{V_{A,\infty}V_{B,0} - V_{A,0}V_{B,\infty} - V_{0A}(\triangle V_A - \triangle V_B)} I_{inj,\infty} \tag{2.28}$$

To calculate G_{syn} and the soma conductance, the resting potential of neuron A must be known, too. Obviously, it cannot be obtained from the equation system 2.20 - 2.23 as there are only 4 equations but 5 unknown variables. A second set of current step measurements is necessary to determine V_{0A}, this time with B as the presynaptic and A as the postsynaptic neuron. Exchanging indices A and B in equation 2.26 and inserting the respective voltages yields the desired quantity.

Until now, only the steady state case has been considered. The two coupled differential equations 2.16 and 2.17 characterize the dynamic behavior of a synaptically connected cell pair. From the system's characteristic polynomial two expressions can be deduced, describing the time course of the membrane voltage in both neurons, each being the sum of two mono-exponential transients and a constant; for the solutions refer to [79].

Detailed model

The isopotential model above neglects voltage drops in the neurites and therefore gives only approximate values of G_{syn}. To obtain the exact synaptic conductivity, the cable properties of the neurites have to be taken into account, resulting in the equivalent circuit shown in fig. 2.11. As before, the synapse is represented by a conductance, but this time it is located at the end of neurites, whose electrical behavior is described with the somatic shunt cable model, discussed in subsection 2.4.1. In analogy to the isopotential model G_{syn} is defined by the current flowing across the synapse I_{syn} and the membrane

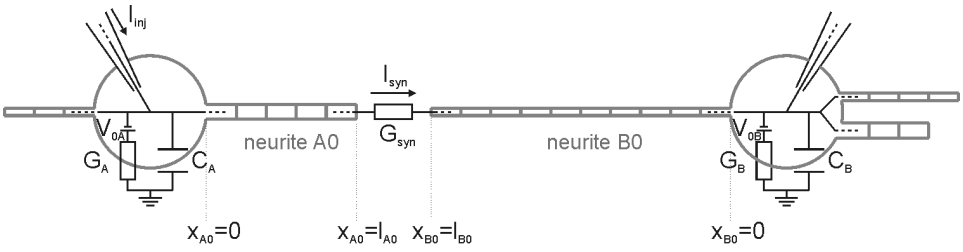


Figure 2.11: *Detailed model of two electrically coupled neurons. In the equivalent circuit the connecting neurites are described by the cable equation. Neuron A is always presynaptic.*

voltages at the tips of the pre and postsynaptic neurite, $V(L_{A0})$ and $V(L_{B0})$, according to (the index A0 denotes the 0th neurite of neuron A):

$$G_{syn} = \frac{I_{syn}}{V(L_{A0}) - V(L_{B0})} \tag{2.29}$$

These quantities are not directly accessible experimentally, but they can be calculated from the somatic voltages and the injected current with the cable equation, if the electrical parameters of the neurites are known. From a current balance similar to equations 2.20 - 2.23, but with the neurite properties included, an expression for the exact synaptic conductivity G_{syn}^{cable} was derived, based on the value obtained with the simplified model G_{syn} (remember $L_j = l_j/\lambda_j$) [82].

$$\frac{1}{G_{syn}^{cable}} = \frac{1}{G_{syn}} \frac{1}{\cosh L_{A0} \cosh L_{B0}} - \lambda_{A0} R_{A0} \tanh L_{A0} - \lambda_{B0} R_{B0} \tanh L_{B0} \tag{2.30}$$

Neglecting the neurites completely by setting $L_j = 0$ leads to $G_{syn}^{cable} = G_{syn}$ as expected. For electrotonically short neurites with $L_{A0} \ll 1$ and $L_{B0} \ll 1$ equation 2.30 is reduced to:

$$\frac{1}{G_{syn}^{cable}} = \frac{1}{G_{syn}} - R_{A0} l_{A0} - R_{B0} l_{B0} \tag{2.31}$$

Only the series resistance of the synapse and the neurites matter in this approximation.

As mentioned in subsection 2.4.1, neurites from *Lymnaea stagnalis* growing on patterned substrates are electrotonically compact, i.e. their influence on propagating signals is small. Therefore, the error from calculating G_{syn} instead of G_{syn}^{cable} is moderate if the coupled neurons are close to each other, with short connecting neurites, and if G_{syn} is small. With increasing synaptic conductivity, the synaptic current rises, causing a bigger voltage drop in the neuritic cables that must be taken into account. The last requirement is also obvious from eq. 2.31. The smaller G_{syn}, the smaller the impact of the terms $R_j l_j$ on the fraction. Experimental data show that these conditions are met for networks of *Lymnaea* neurons. The average deviation between G_{syn}^{cable} and G_{syn} was just 13% for 11 pairs in [82] and 20% for the experiments here, see subsection 2.5.4. This is also confirmed by model calculations, showing that cable effects can be omitted if the overall neuritic length doesn't exceed approximately 500μm and if G_{syn} <1nS.
However, this only holds true for the thick neurites of snail neurons with 5μm diameter or more. In networks of vertebrate neurons the cable properties are much more pronounced. Because neurite diameters are in the range of only 1μm in vertebrate networks, their influence cannot be neglected.

Networks with multiple synaptic contacts

Determining the conductance of a synapse connecting two neurons is complicated if these are part of a larger network. Current injected into one cell flows along many paths that must be taken into account

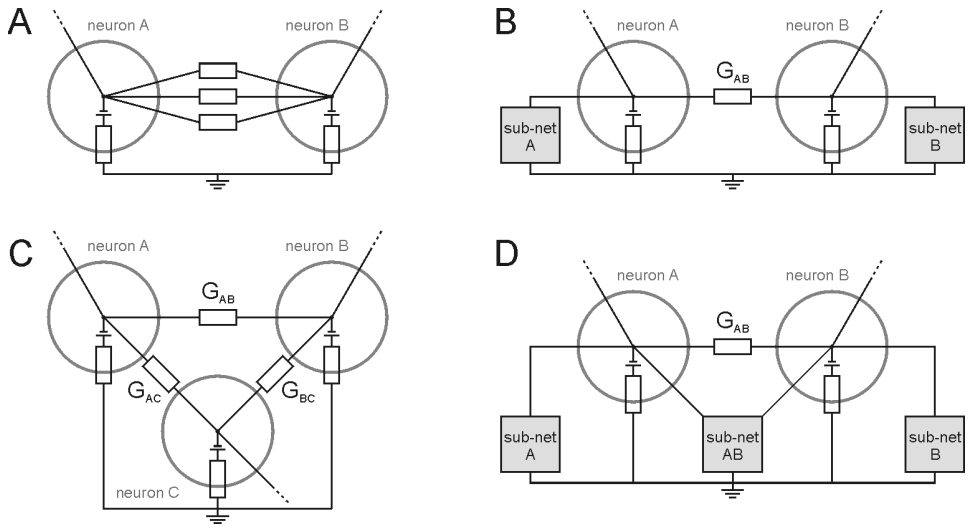


Figure 2.12: *Pairs of neurons arranged in different network configurations. D is the most general case where sub-networks are attached to each cell and additional indirect connections via sub-network AB in parallel to the direct synapse between A and B exist.*

when designing an appropriate equivalent circuit.
The following discussion is focused on networks of snail neurons. For the reasons outlined above, the cable properties of the connecting neurites can be safely omitted. Furthermore, the cell capacitances are neglected because they are irrelevant in the steady state considered here. Each neuron is represented as an isopotential compartment with a battery in series to a conductance.

Starting from the model introduced previously, the next, more complex system is an isolated cell pair coupled with arbitrarily many neurites, as depicted in fig. 2.12A. This is the situation of two randomly growing neurons that make physical contact at several locations. Obviously, all synapses are in parallel and the system can be reduced to a cell pair coupled with a single 'equivalent' synapse whose conductance is the sum of the conductances of the individual synapses. All other parameters, such as resting potentials and cell conductances, remain unaffected.

In conclusion, measuring conductivity between two neurons only yields a yes/no answer on whether an electrical coupling exists or not, and the conductance of the equivalent synapse. It does not reveal how many synapses are involved, a single strong or several weak, and what their respective conductances are.

Fig. 2.12B illustrates a cell pair embedded in a larger structure. In this special case two networks, consisting of neuron A coupled to sub-net A and neuron B coupled to sub-net B, are connected only by a single synapse between A and B that is to be characterized. Each neuron forms a two-terminal network with its attached sub-net, the soma being one terminal and ground the other. According to Thévien's theorem [47] they can be described by a single voltage source in series to a conductance. After the transformation, the equivalent circuit of the entire network is reduced to an isolated cell pair coupled by the synapse of interest. Note that while G_{syn} can be determined from eq. 2.25, the other equations give only the conductance and resting potentials of the 'equivalent' cells, but not of neurons A and B.

The system in fig. 2.12C represents the simplest network with an indirect signal pathway between A and B in addition to the direct snapse. As all three neurons are connected to each other, the voltage change in neuron B is not only governed by the current via the synapse between A and B, but also by the current via synapses A, C and C, B. In analogy to equations 2.20 - 2.23 an equation system can be formulated, describing the steady state membrane voltages of cells A, B and C upon a current injected

into A.

$$I_{inj,A} = G_A(V_{A,\infty} - V_{0A}) + G_{AB}(V_{A,\infty} - V_{B,\infty}) + G_{AC}(V_{A,\infty} - V_{C,\infty}) \tag{2.32}$$

$$G_B(V_{B,\infty} - V_{0B}) = G_{AB}(V_{A,\infty} - V_{B,\infty}) + G_{BC}(V_{C,\infty} - V_{B,\infty}) \tag{2.33}$$

$$G_C(V_{C,\infty} - V_{0C}) = G_{AC}(V_{A,\infty} - V_{C,\infty}) + G_{BC}(V_{B,\infty} - V_{C,\infty}) \tag{2.34}$$

G_{AB} is the conductivity of the synapse between A and B. Index i denotes which neuron the current $I_{inj,i}$ is injected into. The equations characterizing the situation before the current step are almost identical, but this time $I_{inj,i} = 0$ and index k in $V_{j,k}$ is set to 0 instead of ∞.
To determine the synaptic conductivities G_{AB}, G_{AC} and G_{BC}, additional data are necessary from current step measurements with B and C being presynaptic. Providing another 12 equations, the resulting equation system yields rather lengthy solutions.
Equations 2.32 - 2.34 can be brought into the same form as 2.21 and 2.23 by eliminating V_C from 2.32 and 2.33 with 2.34 and some rearrangements. This means that the three-neuron network again behaves like an isolated cell pair if probed with just two electrodes, one in A the other in B. Of course, the values for the somatic conductance and resting potentials differ from G_A, V_{0A} etc. as these 'equivalent' quantities are governed by the network properties rather than the individual cells. Calculating the conductance between neuron A and B in analogy to an isolated pair results in a quantity G_{AB}^{approx} that is related to G_{AB} by:

$$G_{AB}^{approx} = G_{AB} + \frac{G_{AC}G_{BC}}{G_{AC} + G_{BC} + G_C} \tag{2.35}$$

For typical values of the somatic and synaptic conductance of snail neurons (G_{syn}=0.5nS and G_{soma}=2.0nS), the relative deviation between G_{AB}^{approx} and G_{AB} can be approximated by G_{syn}/G_{soma}. It is on the order of some ten percent, similar to the error introduced by using the isopotential model instead of the detailed model, which accounts for the neurites' cable properties.

In principle, all unknown parameters of an n neuron network with an arbitrary connection pattern can be determined from current step measurements. Based on the $n^2 + n$ equations describing the system, the $2n$ soma parameters and the at most $(n-1)n/2$ synapses (the ones in parallel are regarded as a single synapse) can be calculated. Experimental constraints, e.g. the limited number of neurons that can be probed simultaneously, impede this approach rapidly, however.
Alternatively, the 'equivalent' synaptic conductance between the embedded pair A and B in fig. 2.12D can be calculated from eq. 2.25 for the same reasons as discussed above. The deviation from the real value of G_{AB} decreases with increasing length of the path parallel to the synapse directly coupling A with B. It is about $(G_{syn}/G_{soma})^m$ where m denotes the number of neurons connected in series between A and B. For every additional path in parallel, the error increases because their conductances add up in analogy to the situation depicted in fig. 2.12A. In any case, the value obtained from eq. 2.25 is larger than G_{AB}.

2.4.3 Active model: Hodgkin-Huxley dynamics

Most interesting electrical properties of neurons, including their ability to fire action potentials and propagate them actively, arise from the nonlinear behavior of their membrane conductances. These unique features have been omitted so far to simplify the mathematical description, ohmic resistors being used instead. In reality, membrane current is mediated by transmembrane channels that are often highly selective to one sort of ion and whose conductivity is controlled by the membrane potential or ligands bound to specific receptors. Ligand gated channels are essential in signal transmission via chemical synapses, but they are hardly involved in action potential generation. This process is governed

by voltage-gated channels, as outlined below.

A single ion channel can either be open or closed. The transition between the two states is a stochastic event which is influenced by the membrane voltage for voltage-gated channels. Depending on the conductance type they are called persistent or transient. For a persistent or noninactivating conductance, the probability P that the gate is open increases if the neuron is depolarized and decreases if it is hyperpolarized. In general, several independent gating processes are required for a channel to open. In the case of the potassium channel, the open probability is:

$$P_K = n^4 \tag{2.36}$$

where the activation variable n denotes the probability that any of the 4 independent events has occurred. Usually the integer exponent is fit to the experimental data, but for the K channel the value is identical to the number of structural channel subunits.
The behavior of transient conductances is governed by two processes with opposite voltage dependence. Depolarizing the neuron first increases its conductivity, followed by a decrease, resulting in a transient opening of the channel. Thus, two independent variables, one for activation, the other for inactivation, are needed to characterize the open probability; for the sodium channel it is:

$$P_{Na} = m^3 h \tag{2.37}$$

The temporal dynamics of each gating variable $j \in \{m, n, h\}$ is described by a simple rate equation according to

$$\frac{dj}{dt} = \alpha_j(1 - j) - \beta_j j \tag{2.38}$$

where α_j is the rate for the transition *closed* $\rightarrow$ *open* and β_j for the reverse direction. α_j and β_j both depend on the transmembrane voltage; the respective mathematical expressions are listed in appendix C. Equation 2.38 can be transformed into:

$$\frac{dj}{dt} = \frac{1}{\tau_j}(j_\infty - j) \tag{2.39}$$

$$\tau_j = \frac{1}{\alpha_j + \beta_j} \qquad \text{and} \qquad j_\infty = \frac{\alpha_j}{\alpha_j + \beta_j} \tag{2.40}$$

illustrating that if the voltage V is changed suddenly, j approaches its new equilibrium value j_∞ exponentially with the time constant τ_j.

Moving from single channels to entire neurons with many channels allows an approximation of the number of channels in the open state by the probability that a single one is open, multiplied by the overall channel number. The sodium and potassium conductances in the whole neuron are:

$$g_{Na} = \overline{g}_{Na} m^3 h \qquad \text{and} \qquad g_K = \overline{g}_K n^4 \tag{2.41}$$

$\overline{g}_{Na}$ denotes the sodium conductance when all channels are open and $\overline{g}_K$ the respective value for the potassium conductance.

In 1952 Hodgkin and Huxley first described the generation of action potentials in the squid giant axon mathematically with a set of differential equations [45]. The current density flowing across the cell membrane is:

$$i_m = c\frac{dV}{dt} + g_{Na}(V - V_0^{Na}) + g_K(V - V_0^K) + g_L(V - V_0^L) \tag{2.42}$$

in accordance to the equivalent circuit shown in fig. 2.13. For this system $\overline{g}_{Na}$ =120mS/cm^2 and $\overline{g}_K$ =36mS/cm^2. In fact, the voltage-dependent gating of the Na and K channel was deduced by

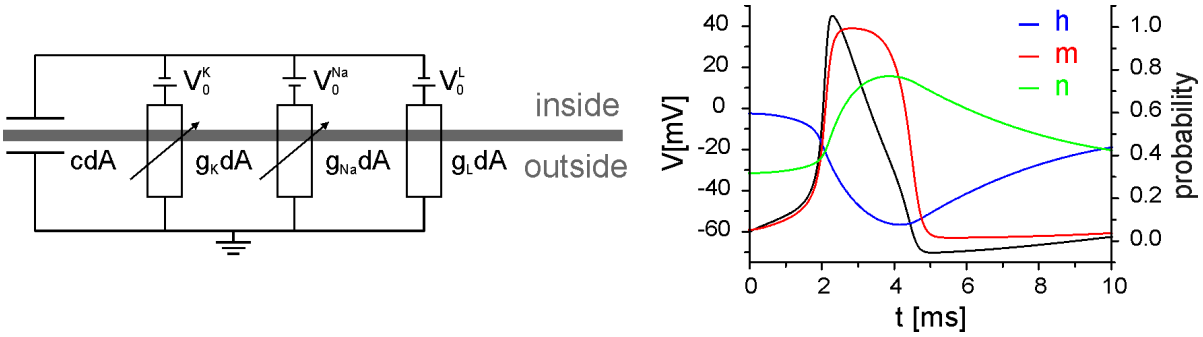


Figure 2.13: *Left: Equivalent circuit of a membrane patch of area dA according to the Hodgkin-Huxley model. The thick grey line represents the cell membrane. Right: Temporal evolution of the intracellular potential and the dynamic variables h (blue), m (red) and n (green) during an action potential.*

Hodgkin and Huxley from their experimental observations. The voltage independent leak conductance g_L =0.3mS/cm^2 subsumes all other ionic conductances, that are assumed to be passiv, e.g. Cl^- and Ca^{2+}, and c=1μF/cm^2 is the specific membrane capacitance.
Instead of the single battery representing the resting potential in the simplified models discussed before, separate voltage sources are introduced for each ion type i because of their different concentrations inside, c_i^{in}, and outside, c_i^{out}, the cell. The corresponding reversal potential is given by the Nernst equation

$$V_0^i = \frac{k_B T}{z_i q} \ln \frac{c_i^{out}}{c_i^{in}} \tag{2.43}$$

k_B is the Boltzmann constant, T the temperature, q the elementary electrical charge and z_i the valence of ion type i. For the squid giant axon $V_0^{Na} = V_0$+115mV, $V_0^K = V_0$−12mV and $V_0^L = V_0$+10.6mV. The resting potential of the cell is calculated from the steady state form of eq. 2.42 where dV/dt and i_m are set to zero, it is about -60mV for *Lymnaea* neurons.

If an artificial neuron modelled with the Hodgkin-Huxley dynamics is depolarized by a brief current injection, it fires an action potential which is similar to those observed in living neurons, see fig. 2.13. Upon a hyperpolarizing stimulus the temporal behavior of the membrane voltage is almost identical to the simplified models in subsections 2.4.1 and 2.4.2. This justifies the assumptions of voltage independent conductances in the range below the resting potential and validates the expressions obtained for the synaptic conductivity.

Modelling the signal propagation in neurites with active conductances is frequently done with numerical simulation programs like NEURON (it can be downloaded from: http://neuron.duke.edu).

Since the rate equations in the Hodgkin-Huxley model have been derived from the squid giant axon, they describe the behavior of *Lymnaea* neurons only qualitatively. The action potentials especially are considerably longer in snail neurons than in the model.

2.5 Results

This section summarizes the experimental data obtained from the two methods tested for growing defined neural networks, namely chemical patterns of substrate adsorbed conditioning factors made by UV-lithography (hereafter referred to as UV-patterning) and topographical structures processed from SU-8. After a brief presentation of randomly growing neurites on plain SiO_2 and SU-8 substrates, several examples of controlled outgrowth are shown, followed by electrophysiological recordings from

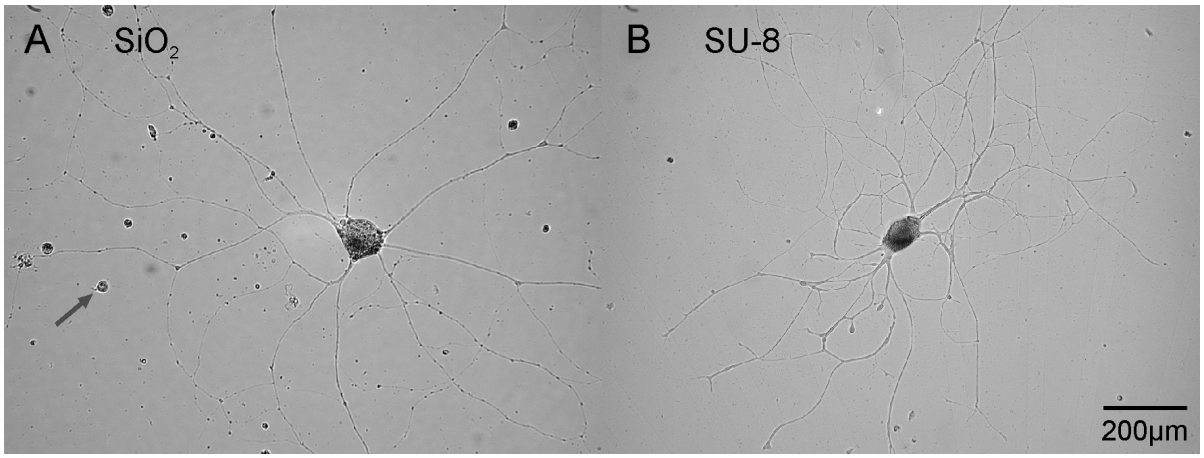


Figure 2.14: *A: Neuron on SiO_2 substrate with adsorbed conditioning factors after 3div (dimensions are similar to B). The arrow points to a non-neuronal cell. Such cells are abundant in the vicinity of conditioning brains (not shown) and appear in smaller quantities throughout the culture chamber. B: Random outgrowth on SU-8 in co-culture after 2div.*

simple defined networks. A discussion of the advantages and disadvantages of each technique concludes the section.

2.5.1 Standard cell culture

Before introducing new materials into a cell culture system, they have to be tested for biocompatibility. For SU-8 photoresist this was done by culturing neurons on SiO_2 surfaces with SU-8 stripes processed on top.

In the first test, the whole substrates were coated with poly-L-lysine and preconditioned for 3 days, before cells were placed, to form a layer of substrate adsorbed material (SAM, refer to 2.2.2). Normally, neurites started sprouting a few hours after plating and continued growing for a maximum period of 3-4 days, during which they extended up to 1mm.
On the test substrates outgrowth was very robust, with neurons having almost identical morphology and neurite length on both surfaces. 96% of plated cells adhered to the SiO_2 and also to the SU-8 ($n = 48$) surface. Of these, 65% on SiO_2 and 70% on SU-8 grew at least one neurite with a minimum length of one soma diameter (definition of growth according to [90]), indicating that the physiological conditions on the two materials are very much alike.

Similar results were obtained, if instead of SAM, conditioning factors were delivered by co-culturing *Lymnaea* brains. Under these conditions 95% and 86% of plated cells adhered to SiO_2 and SU-8, with a growth rate of 80% and 79% respectively (n=120). As shown in fig. 2.14B, the neuron on SU-8 in co-cultured medium looks very similar to the one in fig. 2.14A on SiO_2 coated with SAM.

The major difference between the two cell culture protocols is that in co-culture the growth is delayed for about one day because the conditioning factors must be released from the brains first, whereas on SAM they are present immediately when cells are plated. However, this time lag has already vanished after 2div (days *in vitro*), see fig. 2.14A and B, where the neuron in A is shown after 3div on SAM and in B after 2div in co-culture. Also, neurons adhere much better to surfaces of fresh poly-L-lysine present in co-culture than to the protein layer formed by the SAM. This has a marked effect on the neuron-silicon contact, which is discussed in section 3.5.

From the culturing assays presented here, the following conclusions are drawn:

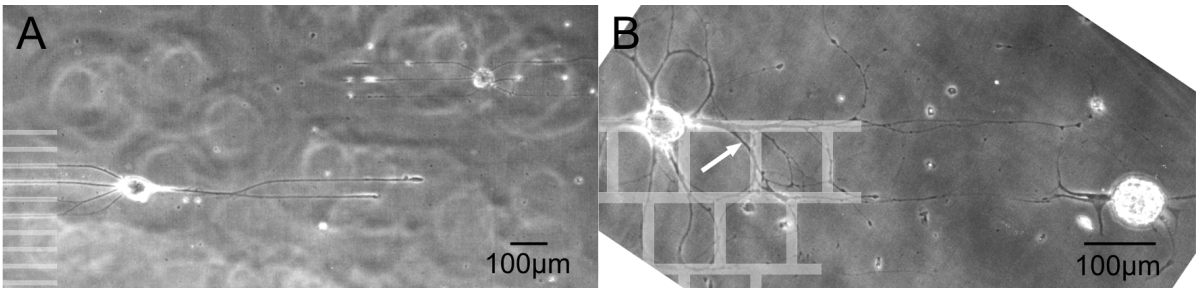


Figure 2.15: *Neurite outgrowth controlled by UV-patterning of SAM. A: Parallel lanes 12μm wide and 45μm apart, after 1div. B: Brick wall pattern with a feature size of 100μm and a line width of 15μm after 2div. Invisible patterns are sketched at the bottom left corner.*

- SU-8 is fully compatible with the culture of *Lymnaea* neurons. It neither releases any toxic substances to the medium, otherwise cells would be unhealthy or even dead including those on the SiO_2, nor does it impair the metabolism of the adhering cells.
- As neurite growth and morphology is almost identical on both substrates SiO_2 and SU-8, indicating that neurons show no preference, guidance mechanisms governed by chemical cues can be largely ruled out when neuronal outgrowth is controlled with SU-8 topographic structures.

Even though the last point seems to be obvious from these results, effects of the different surfaces can not be excluded totally. Doing so would require further, more detailed experiments that are beyond the focus of this thesis.

2.5.2 Controlling neurite outgrowth

UV-patterned substrates

Neurons cultured on UV-patterned substrates, see subsection 2.3.1 for the technical details, grew neurites that followed the lanes of intact protein. The percentage of neurons adhering to the substrate and sprouting neurites, as well as their length and morphology, was similar to plain pre-conditioned substrates. Guidance was very good on the line pattern, where only a few processes cross the areas of inactivated protein after 1div, as illustrated in fig. 2.15A. In contrast, compliance to the brick wall pattern depicted in fig. 2.15B was clearly reduced, although the protein lanes still provide some directional information.

Three reasons may account for this poor control of neuronal outgrowth.

Firstly, the proteins in the irradiated areas may not have been fully inactivated. This problem can be solved easily by longer UV exposure.

Secondly, although the growth-cones follow the lanes of intact protein, the neurites span across inactivated regions, especially where the guidance tracks make sharp turns. The white arrow in fig. 2.15B marks such a situation. During outgrowth, the growth-cone exerts a pulling force on the trailing neurite which, if bigger than the adhesive forces of the substrate, rips the neurite from the lanes, minimizing its overall length. Such effects are inherent to this technique, they have already been reported before [35, 79] and are also described in 2.1.5.

Thirdly, compliance to protein patterns decreases with increasing culture time. The micrograph shown in fig. 2.15B was taken after 2div, whereas the one in fig. 2.15A was taken after 1div. This effect is presumably caused by trophic factors present in the supernatant or released by the plated neurons themselves. They adhere to the entire substrate, rendering the formerly irradiated areas equally permissive to neuronal outgrowth. Excluding the presence of trophic factors in the culture medium by using plain

DM (without diluting it with supernatant from the conditioning procedure) and changing it regularly could improve the fidelity to the patterns even after prolonged culture periods.

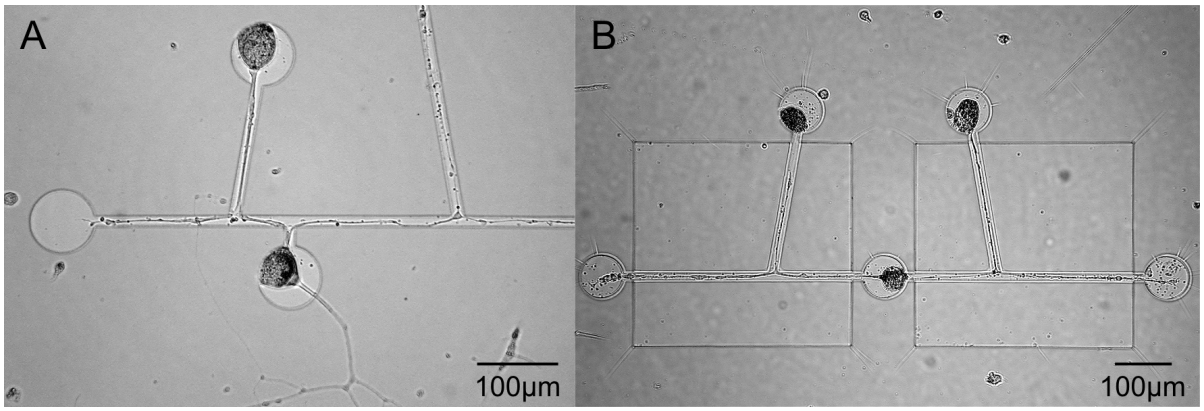


Figure 2.16: *Topographical guidance of snail neurons on SAM after 3div. A: One layer structure, 17μm thick. Growth was so strong that one neurite left the structure directly at a pit. B: Two layers of SU-8, each about 18μm thick. Two out of three neurons sprouted neurites that followed the grooves.*

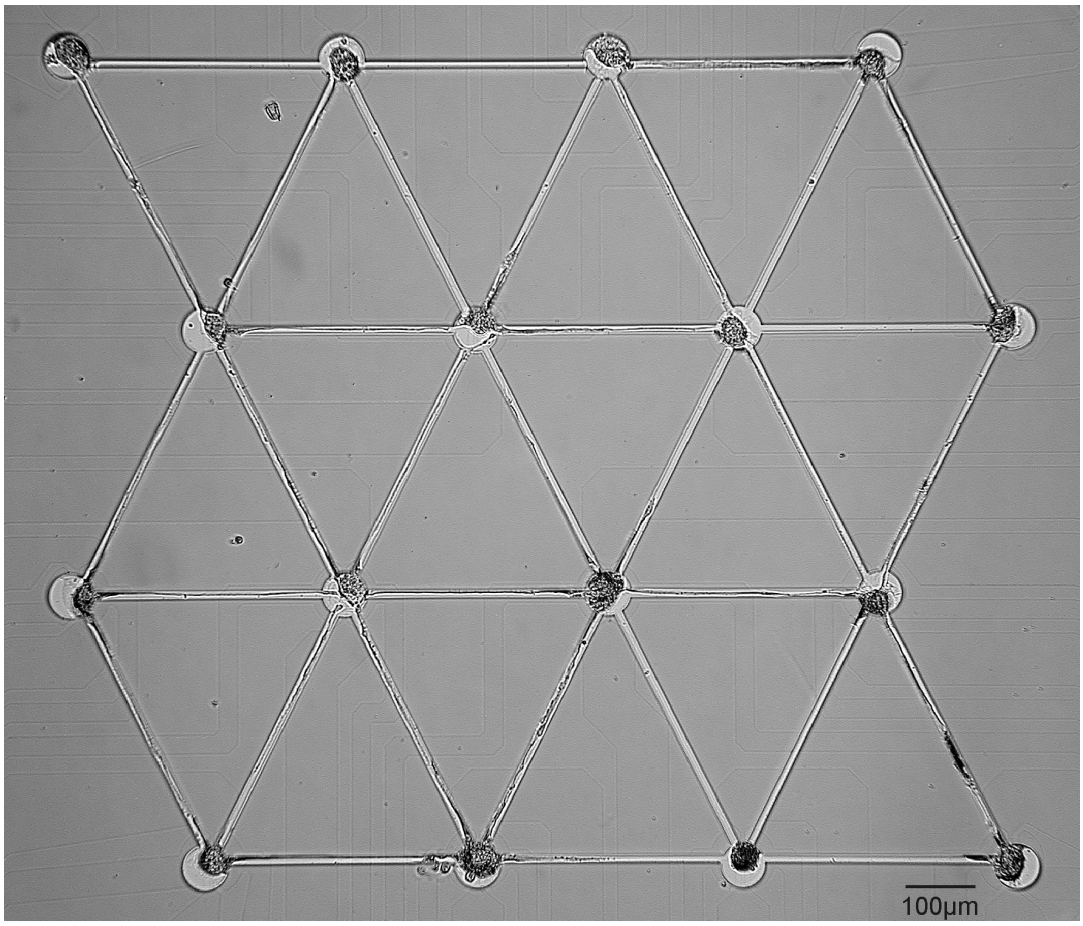


Figure 2.17: *Large network of 15 vital neurons grown on a chip, after 2 days in co-culture. The height of the walls was about 33μm.*

SU-8 topographic structures

About 60% of the vital neurons placed in the pits of SU-8 topographic structures grew at least one neurite that followed the grooves. Again, neurite length and morphology was similar to plain or UV-patterned substrates. There was also no difference between SAM or co-culture, except for the delayed sprouting of processes in co-culture as reported in the previous subsection. Fig. 2.16 shows neurites that were nicely guided by the grooves. The structure depicted in A consisted of a single 17μm thick resist layer, the one in B of two layers each about 18μm thick.

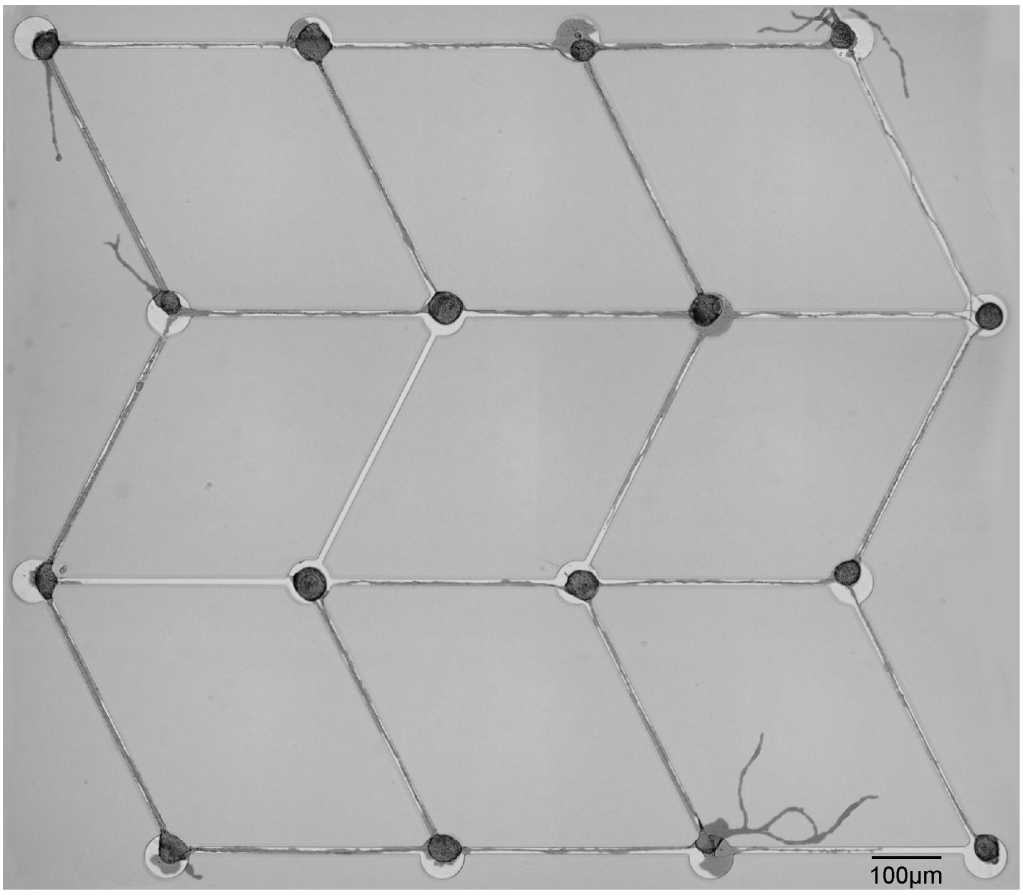


Figure 2.18: *Network of 16 neurons in a one layer test structure (without transistors) of about 20μm height, after 2 days in co-culture. Somata and neurites were selectively colorized with an image editor to increase their visibility in the pits and narrow grooves.*

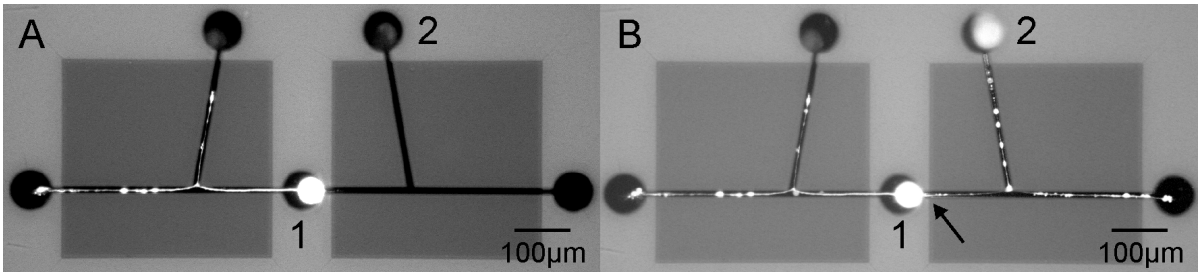


Figure 2.19: *A: Fluorescence micrograph of the central neuron stained with Lucifer Yellow. B: Additional staining of the right neuron. The location of the synapse connecting both neurons is marked.*

Based on the assumption that neurites do not branch or turn at intersections when they can advance straight on, the substrates were designed for localizing synapse formation at the intersection of the grooves. To further reduce the probability of a neurite growing in the wrong direction, the nearly vertical grooves cross the horizontal ones at an angle of 100°. Processes sprouting from the pit in the middle, e.g. from neuron 1 in fig. 2.19A, were supposed to grow straightly to the left and right. The distance from neuron 1 to the intersection is shorter than from neuron 2, so that the growth-cone from the latter should encounter the already present neurite from neuron 1 at this location and form a synapse there.

Unfortunately, mother nature did not follow these ideas, at least not always. When a neurite grew onto a T-shaped intersection vertically, the growth-cone usually bifurcated as expected. However, the situation was less defined when it tangentially met such a crossing. In only two thirds of the cases it passed on unperturbed, but sometimes it turned into the branching groove or bifurcated, see fig. 2.19A. These uncertainties, in combination with the large variability in growth rate and timing when neurites start sprouting, render the prediction or even the control of the exact location of synapses virtually impossible.
Neurites advancing towards an obstacle, such as the wall of the topographic structures or debris in the grooves, stopped growing or left the structure if growth was very strong; see the example in 2.16A.

Fig. 2.17 and 2.18 depict two beautiful networks with a well defined connection pattern among individual neurons. All cell bodies were confined to the predefined location. Guidance by the topographic structures was almost perfect, only a few processes left the pits directly at the somata.

As conventional micrographs neither allow the assignment of neurites to the neuron they originated from, nor to localize synapses, some networks were sequentially stained with Lucifer Yellow [102]; refer to appendix A for the staining protocol. The dye quickly spreads throughout the cytoplasm including the neurites, but does not pass synapses [79]. In fig. 2.19A the central neuron was stained, showing that it had only one neurite grown to the left with an unexpected bifurcation at the intersection, whereas the neurite on the right side originated from neuron 2 as shown in 2.19B. The synapse connecting neuron 1 and 2 was therefore located directly at the soma of 1.

2.5.3 Simple, defined networks

The techniques for neurite guidance presented above are a decisive pre-requisite for building defined neuronal nets *in vitro*. Equally important, though, is the establishment of functional connections among the neurons.
Synapses between cell pairs are formed in three different configurations, namely two growth-cones collide frontally, a growth-cone encounters the existing neurite of another cell, e.g. as with the intersecting grooves discussed above, or it meets the other neuron directly at its cell body. Electrophysiological measurements are needed to check whether neurons are vital and if they are really coupled synaptically. To do so, each neuron was impaled with a sharp glass microelectrode, hyperpolarizing and depolarizing currents were injected in one cell and the resulting voltage transients were recorded in both cells.

Pairs without synapses

Only 60% (n=84) of the electrophysiologically tested cell pairs grown in SU-8 patterns were synaptically coupled, although all were in physical contact with each other by their neurites, as revealed by optical inspection. Several reasons might account for the failure to reestablish a functional synaptic connection during guided outgrowth *in vitro*.

It can not be excluded that, apart from the desired A-cluster neurons, cells from the neighboring clusters were isolated and cultured. However, pairs of mixed composition consisting of A-cluster and non-A-

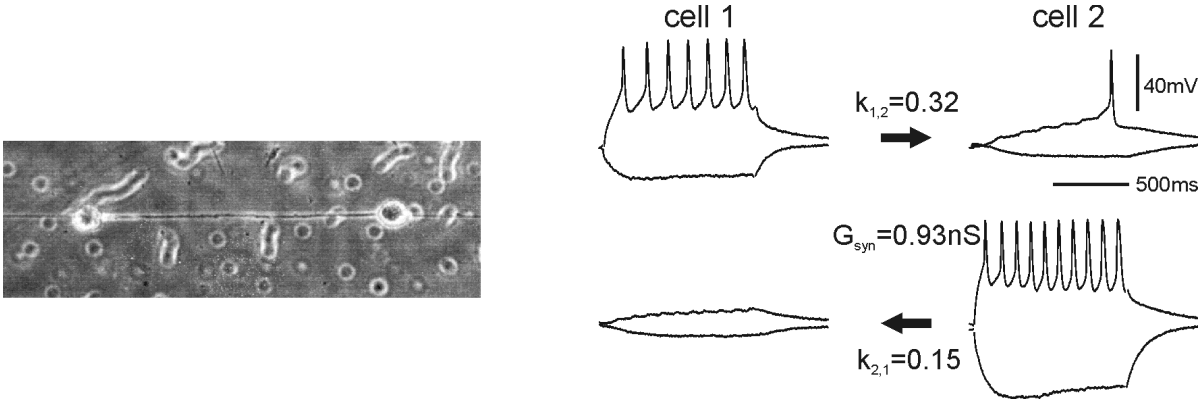


Figure 2.20: *Left: Synaptically coupled cell pair on a UV-patterned glass substrate. No scale bar is available, somata have an estimated diameter of about 30μm. Right: Electrophysiological recordings with impaled microelectrodes. Top row, cell 1 is presynaptic, bottom row, cell 2 is presynaptic. Top traces, injection of a depolarizing current of 0,15nA; bottom traces, hyperpolarizing current injection with -0.15nA. Coupling coefficients are displayed for each direction of signal transfer and the synapse conductance is shown. The transients were corrected for electrode artifacts.*

cluster neurons need not necessarily establish synaptic connections *in vitro*, especially if they have not been connected *in vivo*.

Studies with *Helisoma* neurons indicate the importance of both neurons being in a state of active growth to form a synapse [41]. Time lapse photographs of developing networks suggest a similar situation in the case of *Lymnaea stagnalis* [79].

A third, yet very speculative reason might be a negative influence of the SU-8 topographic structures on synapse formation. It is supported by studies with UV-patterned substrates, where 73% (n=15) of the pairs were coupled, as compared to just 60% here. However, due to the small number of networks tested, the statistical relevance is low. The difference could also arise from a more careful selection of neurons, for example.

Electrophysiological recordings of coupled cell pairs

The following paragraph discusses signal transfer between coupled neuron pairs on the basis of three example networks.

Fig. 2.20 shows two nerve cells growing neurites collinearly on a track of intact conditioning factors on a **UV-patterned substrate**. As illustrated by the electrophysiological recordings on the right, a functional synaptic connection has been formed. Transients can not be assigned to a specific cell in the micrograph, because they were not labelled during the experiment. This is of little relevance to the following discussion, however.
Injecting a hyperpolarizing current of -0.15nA into cell 1 hyperpolarized its membrane potential by about 25mV. The signal passed via the synapse and also hyperpolarized the postsynaptic cell 2 by 10mV. Determination of the coupling coefficient according to eq. 2.24 yields $k_{1,2} = 0.4$ (the actual value given in the diagram is averaged over several measurements with currents of different amplitude injected). Switching the roles of the two neurons, such that cell 2 was now presynaptic and cell 1 postsynaptic, resulted in similar recordings, but with a somewhat smaller coupling coefficient. The difference in values $k_{1,2}$ and $k_{2,1}$ is attributed to the varying soma conductance of the respective postsynaptic neuron as described by eq. 2.24.
The behavior found with this cell pair, i.e. signal transfer in both directions across the synaptic connection and transmission of hyperpolarizing currents, is characteristic for electrical synapses. They were

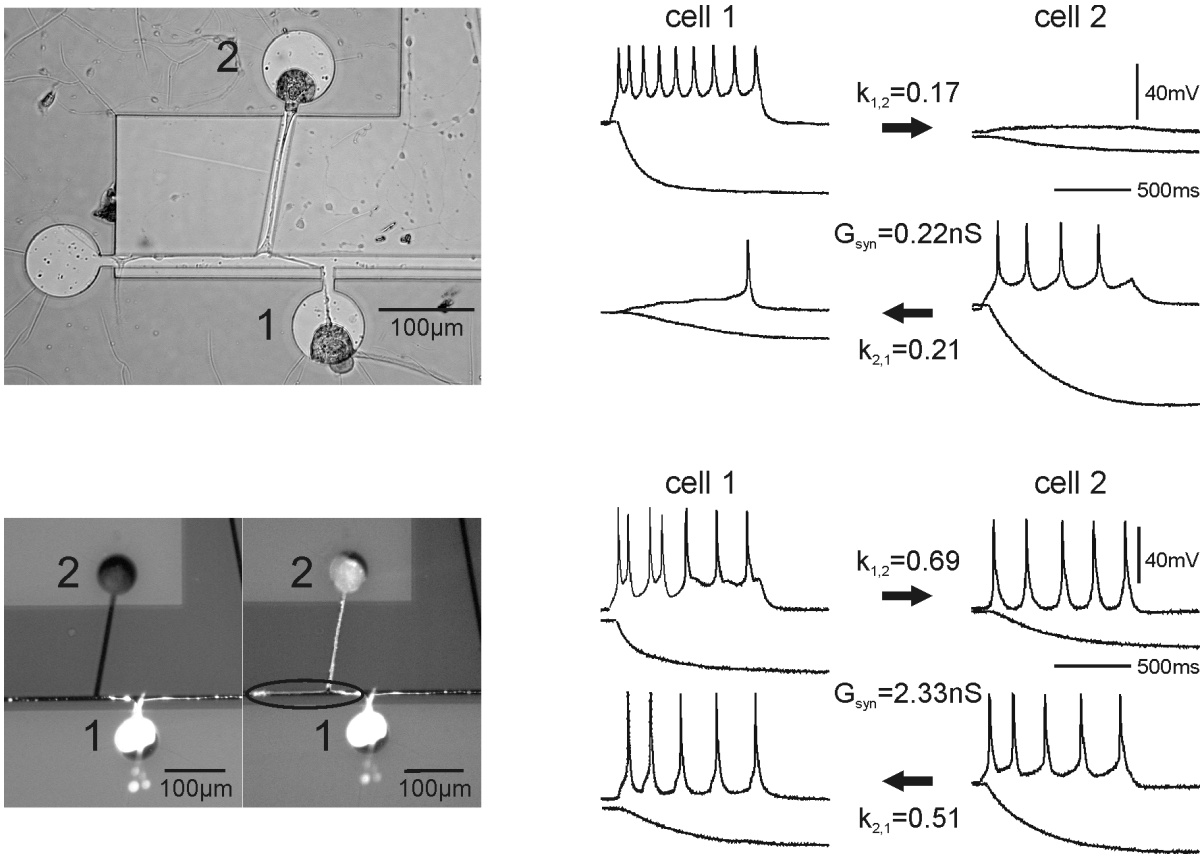


Figure 2.21: *Electrical coupling in two example networks. Top row: Pair with weak synapse. On the right hand side intracellular recordings are shown in the following order: top row, cell 1 is presynaptic, bottom row, cell 2 is presynaptic; top traces, injection of a depolarizing current of 0,05nA; bottom traces, hyperpolarizing current injection of -0.05nA. Coupling coefficients are displayed for each direction, and so is the synapse conductance. Bottom row: Pair with strong coupling. The order is identical to the example above, injected current was ±0.10nA. Signals were corrected for electrode artifacts.*

expected to be established between the A-cluster neurons cultured in this study.
Action potentials are triggered by injecting depolarizing, positive currents that raise the membrane potential above a certain threshold, approximately -40mV. Once this value is exceeded the AP is fired automatically and the neuron repolarizes thereafter.
In this example, a current of 0.15nA and 1000ms duration elicited a train of 7 spikes in cell 1 with the postsynaptic neuron firing only one AP after temporal integration of the synaptic input. Steps in its membrane potential are clearly visible after each presynaptic voltage peak. The situation was somewhat different when a positive current was injected into cell 2. Although each of the 11 presynaptic spikes caused a depolarization of neuron 1 which was summed up, its membrane potential failed to reach the firing threshold. Increasing stimulus length and amplitude might have evoked a postsynaptic AP, if enough presynaptic peaks were integrated.

The top row in fig. 2.21 shows a two-neuron network in a **double layer SU-8 structure**. Growth is almost perfect and the neurites are easily visible at the bottom of the grooves. Only one neurite left the structure directly at the soma of neuron 1, growing towards the bottom right corner of the micrograph.
Again, both cells were impaled and depolarizing or hyperpolarizing currents with ±0.05nA amplitude were injected. The electrophysiological behavior was very similar to that of the network on the UV-patterned substrate in fig. 2.20, with weak coupling coefficients of similar magnitude. Also, postsy-

naptic spikes were only fired in neuron 1 upon presynaptic stimulation of 2. Neuron 2 was depolarized only a little when it was postsynaptic and remained quiescent.

To localize the synapse in the network depicted in the bottom row of fig. 2.21, it was stained with Lucifer Yellow, first cell 1, see left micrograph, then cell 2, as shown in the right micrograph. Most neurites nicely followed the grooves, only a small one left the structure at the pit of neuron 1. Compared to example 2.19, the position of the synapse was much less defined here. The neurite from cell 2 grew in parallel to that of neuron 1. Note the white 'dots' in the left side groove in the left micrograph indicating the presence of a rather thin neurite originating from 1. The synapse must be somewhere along the line of fasciculated growth of both neurites marked in the right micrograph, but its exact location is unknown.
Electrophysiological recordings revealed a very strong connection, the averaged coupling coefficients were $k_{1,2}$=0.69 and $k_{2,1}$=0.51. Most presynaptic APs in neuron 1 also triggered spikes in cell 2. Changing the direction of signal transfer resulted in even stronger postsynaptic activity, with every spike in 2 triggering a spike in cell 1.

Given the examples above, one might conclude that the strength of synaptic coupling is the only parameter governing the generation of postsynaptic action potentials, with a larger coupling coefficient increasing the probability for a spike being triggered. However, the resting membrane potential of the postsynaptic neuron plays an important role, as well. If it is very high, near the firing threshold, just a small increase of the membrane potential is sufficient to trigger an AP. In this case, even a weak synaptic coupling is sufficient. But if the resting potential is rather low, a large postsynaptic depolarization resulting from a strong synapse may still not be sufficient to raise the cell above its firing threshold. Therefore, two parameters have to be taken into account when discussing the triggering of postsynaptic action potentials, the coupling coefficient and the respective resting potential.

2.5.4 Characterization of synapses

Of 84 networks grown on SU-8 structures in this assay, 51 were synaptically connected, but only 26 were evaluated in detail. The others had ambiguous connection patterns that made the assignment of coupling to an identified synapse impossible, e.g. three neurons with unknown signaling path. Fig. 2.22A shows a histogram of coupling coefficients for the 26 pairs. Two values are included per pair, one for each direction of signal transfer $k_{1,2}$ and $k_{2,1}$. The numbers are averaged from several recordings with currents of different amplitude injected in the cell pair. Most values range between 0.1 and 0.6, with extrema of 0.01 and 0.78. In general, they are higher than the coupling coefficients in networks on UV-patterned substrates [79] and the example net depicted in fig. 2.20. Still, they are well within the range found with the mollusks *Helisoma* and *Aplysia* on plain, unpatterned substrates [7, 41].

Although the coupling coefficient is an ideal quantity for describing the effects of the presynaptic input on a postsynaptic neuron, it conveys only limited information about the synapse itself. As shown by eq. 2.24, $k_{pre,post}$ is not only determined by synaptic properties but also by the soma conductance of the postsynaptic neuron. The synaptic conductance G_{syn} is the quantity that entirely characterizes electrical synapses. It is determined from electrophysiological recordings by the following procedure:

- First, $V_{A,0}$ and $V_{B,0}$ are obtained from recording the membrane potentials of both neurons, A and B, before current injection.
- Then, a constant hyperpolarizing current $I_{inj,\infty}$ is injected in neuron A and the stationary presynaptic and postsynaptic response is measured after initial transients have decayed, $V_{A,\infty}$ and $V_{B,\infty}$. G_A, G_B and V_{0B} are calculated from 2.26, 2.27 and 2.28.
- The steps above are repeated to determine V_{0A}, but this time with B as the presynaptic neuron where

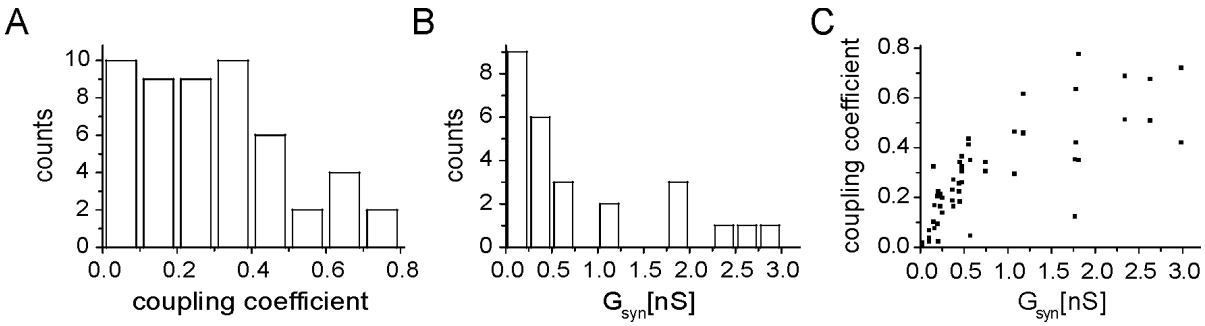


Figure 2.22: *A: Histogram of the coupling coefficients determined from 26 neuron pairs. Owing to the asymmetry of $k_{pre,post}$, two values are included for each pair. B: Histogram of the synaptic conductance from the same pairs. C: Coupling coefficient plotted versus synaptic conductance, two coefficients per G_{syn}.*

the current is injected. Exchanging index A versus B and vice versa in eq. 2.26 and inserting the respective values yields the resting potential of neuron A.

– G_{syn} is calculated from eq. 2.25.

The membrane potential was often not constant during the measurements but varied by up to 15mV, without the application of any current. Leaky cell membranes or ions diffusing from the impaled pipettes into the neuron, thereby changing V_{0A} and V_{0B}, might account for this effect. Because determination of G_{syn} crucially depends on the resting potential being constant, these variations cause errors that sometimes even lead to negative conductance values. To avoid such erroneous results, corrected values are inserted into eq. 2.25. $V_{A,0}$ and $V_{B,0}$ taken from the first step are set as reference. $V_{A,\infty}$ and $V_{B,\infty}$ in step 3 are calculated by adding $\triangle V_A$ and $\triangle V_B$ from the respective measurements.

The synaptic conductance was independent of the direction of signal transfer, as expected. However, some temporal variations were observed, possibly due to changes in the resting potential that could not be corrected entirely. These variations were eliminated by averaging several values obtained from different injection currents and from reversing the order between pre and postsynaptic neurons.

Fig. 2.22B shows a histogram with mean values of the synaptic conductance determined from the 26 pairs. Like the coupling coefficients they are larger than the numbers found in [79] for networks on UV-patterned substrates, but are still within a reasonable range. Plotting the coupling coefficients against the respective synaptic conductance reveals a minor correlation between both quantities; illustrated in fig. 2.22C. This is not surprising since $k_{pre,post}$ not only depends on G_{syn}, but also on the soma conductance of the postsynaptic neuron (see eq. 2.24), which varies considerably with the size of the cell body.

Determination of G_{syn} here is based on the isopotential model, which neglects voltage drops in the connecting neurites, see subsection 2.4.2. In [79, 82] the impact of cable properties on signal propagation between coupled nerve cell pairs was studied in detail. For the thick neurites connecting *Lymnaea* neurons only minor differences in G_{syn}, calculated from a detailed model and from the isopotential model, were found. The values obtained from the latter were just 13% smaller than the real conductances, demonstrating that the isopotential model is a good approximation for such networks.

Similar results were obtained for the 26 cell pairs in this study. Synaptic conductances as given by the detailed model were calculated with eq. 2.30 using the following parameters: g=0.035mS/cm^2, r=394Ωcm and d=5μm, which were supposed to be identical for all neurites. If the position of the synapse was unknown, the prevalent case here, it was assumed to be located at the intersection of

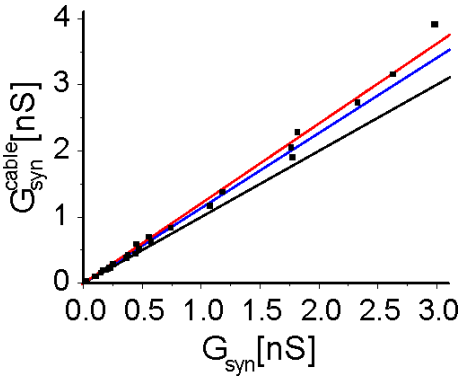


Figure 2.23: *Synaptic conductances obtained from the detailed model G_{syn}^{cable}, plotted against the values from the isopotential model G_{syn}. The black line is a guide to the eye with a slope of 1, the blue line is a linear fit to the values up to G_{syn} =1.3 and the red line results from fitting all values. Intercept with the y-axis is 0 for all.*

grooves or right in the middle between both cells.
In fig. 2.23 the exact conductance G_{syn}^{cable} is plotted versus the values obtained from the isopotential model. The latter are slightly too small, since all data points lie above the black line with slope 1. Fitting only values below G_{syn}=1.3 yields the blue line of slope 1.13, denoting an average deviation of 13%, which is identical to the results in [79]. If the entire data set is fitted a slope of 1.20 is obtained, shown by the red line. The error of the simplified model increases as G_{syn} increases, as illustrated by almost all data points with G_{syn} >1.3 located above the blue line.
This behavior is obvious from eq. 2.30. The bigger G_{syn} in the denominator, the larger the influence of the correcting terms $\lambda r \tanh L$. With increasing synaptic conductivity, the voltage drop in the neuritic cables rises with respect to the voltage drop across the synapse. Neglecting it, as in the isopotential model, results in a larger deviation. The other source of error is governed by the current leaving through the neurite membrane, which depends on the membrane conductance g.
In conclusion, the results obtained from the isopotential model are acceptable with most of the networks studied here. Only in strongly coupled pairs with conductances G_{syn}=3nS do errors rise to 32%.

Comparing the synaptic conductance of defined networks grown in SU-8 structures with those on UV-patterned substrates raises an important question. Why is the coupling generally stronger in the topographic structures? Except for the irradiated regions on the UV-patterned surfaces, cell culture conditions are quite similar. Both substrates are homogeneously coated with poly-L-lysine and covered by a layer of conditioning factors. Effects of different chemical environments on synapse formation can therefore be largely ruled out.
To assess the influence of the patterns themselves, a control network was grown on a plain, unirradiated substrate. Fig. 2.24 shows this 3 neuron network, yielding a synaptic conductance between neurons 1 and 2 G_{syn}=0.39 and between neurons 2 and 3 G_{syn}=1.67. The respective values clearly correlate with the maximum number of possible signaling paths connecting both cells. 2 synapses for the cell pair 1 and 2 and 6 synapses for pair 2 and 3 as revealed by the number of neurites intersecting the dashed lines in fig. 2.24. Even though the relation between overall conductance and number of connections is not linear, due to variations among individual synapses, it can be concluded that a large G_{syn} usually implies several synapses connected in parallel. In that case, the resulting conductance is given by the sum of the single ones; for a discussion refer to subsection 2.4.2.

This finding is further supported by attempts to localize synapses by sequential staining with Lucifer Yellow. The weakly coupled cell pair depicted in fig. 2.19 with G_{syn}=0.25 is only in physical contact at a single spot where the neurite of cell 2 touches the soma of cell 1. In contrast, the exact position of the synaptic connection is not known in the network shown in the bottom row of fig. 2.21, which has a very large conductance of G_{syn}=2.33. The neurites from both cells do not just meet at one point but grow along side each other in the horizontal groove. Due to the large contact area it is very likely that not only one but several synapses exist, explaining the strong coupling.

Fasciculated outgrowth has not been observed on UV-patterned substrates [79]. (This might also result from the special culture protocol, where pairs were measured immediately after they had formed a vis-

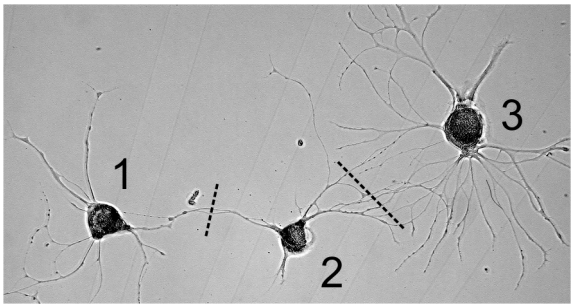


Figure 2.24: *Three neurons randomly grown on a plain substrate coated with conditioning factors. The number of neurites intersecting the dashed lines are an indication for the maximum number of synapses between the respective neurons. Cell 3 is approximately 70μm in diameter.*

ible contact. There was no time for any further, probably fasciculated, growth. [80]) Therefore only single point synapses were established resulting in comparably small conductance values.

In conclusion, differences in neuronal outgrowth on both substrates with fasciculation occurring in the SU-8 grooves but not on the UV-patterns, very likely account for the differences in overall synaptic conductance.

2.5.5 Discussion

The aim of the first part of this thesis was to find a technique for controlling neurite outgrowth that is compatible with extracellular recording. Two methods were assessed in detail; tracks of growth-promoting proteins processed by UV-patterning and topographic structures from the photoresist SU-8. Before discussing their pros and cons the requirements for combining them with transistor chips are listed:

- reliable guidance of neurites along predefined pathways
- establishment of functional synaptic connections
- retention of somata on recording sites and neurites in the grown geometry
- compatibility with extracellular recording
- high efficiency, easy use and quick preparation
- defined, reproducible substrates

UV-patterning, processing tracks of growth-promoting proteins by UV-irradiation of a homogeneous protein layer through a lithographic mask, is a well established technique. It has been successfully used with different systems such as the leech, *Hirudo medicinalis* [35] and the snail *Lymnaea stagnalis* [79] in our department. Due to the vast body of experience, its potential for building chip-controlled neural networks has been tested here, as well. As expected, growth-cone guidance and synapse formation was reliable and small functional networks of *Lymnaea* neurons were obtained.
However, somata were often dislocated from their initial positions and neurites were frequently pulled from the guidance tracks. The displacement of the cell bodies is particularly unacceptable with extracellular recording, as cells get pulled away from the recording site.
Immobilizing the somata by fences made from small polyimide pillars proved very efficient [129], but due to their three-dimensional nature they can hardly be combined with lithography needed for UV-patterning. The distance between mask and substrate imposed by the pillars causes proximity effects which deteriorate the pattern resolution drastically or even make lithography impossible. Special masks correcting these effects or a projection apparatus could be used instead, but the technological challenges and the overall effort are very high. Because these restrictions were already obvious at the beginning we did not invest too much time and effort into improving the technique and adapting it to the transistors, but rather started to look for alternatives. Much later it became clear that the decision was absolutely

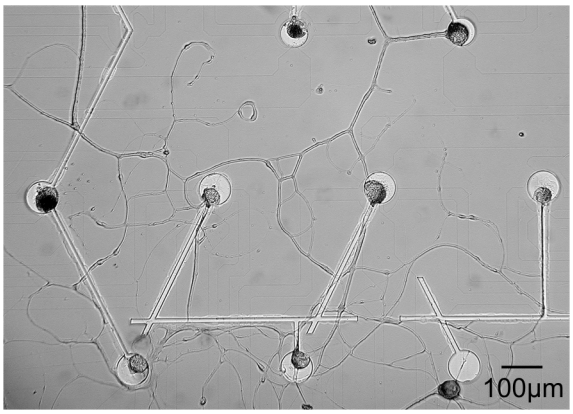


Figure 2.25: *Uncontrolled growth on topographic structures after 4 div (co-culture). Neurites left the pits directly at the soma or grew out of the grooves.*

right. The layer of growth-promoting proteins forming the basis of the UV-patterns increases the distance between chip surface and cell membrane considerably. This obstructs transistor recordings on SAM coated substrates.

Topographic structures consisting of pits for taking up the cell bodies and connecting grooves that guide the growing neurites provide an alternative tool for building small, defined networks *in vitro*. They are made from the n-type photoresist SU-8, which is very well compatible with cell culture as revealed by growth assays on various substrates. Neurite length and morphology is very similar on both SU-8 and SiO_2 surfaces, see 2.5.1, indicating that outgrowth on the SU-8 structures is solely controlled by directional cues conveyed by the topographic features. Chemical guidance effects caused by variations in the surface chemistry in different areas, like SiO_2 at the bottom of the grooves and polyester resist on top of the SU-8 structures, can be largely ruled out. This is also due to the culture protocol, which provides almost identical conditions across the whole surface. The substrate is entirely coated with poly-L-lysine, followed by a homogeneous deposition of conditioning factors as described in 2.2.2.
The restrictions imposed by topographical guidance have no significant effect on neurite diameter and length, which is similar to those on unpatterned, plain glass substrates. Therefore, their physiological behavior should not be considerably altered either.
Apart from controlling outgrowth, the SU-8 structures exert enough mechanical force to confine the grown neurites in the desired geometry provided by the grooves and to keep the cell bodies in the pits. The latter is an essential requirement for extracellular recording, as somata must sit directly on top of the recording sites to obtain acceptable signals. Alignment of the structures to the transistors and stimulators is done during chip processing and thus is not an issue in cell culture. Moreover, the technique works also with co-culture instead of SAM layers for promoting neurite outgrowth. This is important for the combination with extracellular recording.
Unlike most chemical patterns that are removed by cleaning the substrate after cell culture, polyester pits and grooves are permanent and can be reused several times, which makes them very efficient and convenient.

Despite all these qualities, topographic control of neuronal outgrowth suffers from a major drawback; **reproducibility and reliability** is not satisfactory. Fig. 2.25 shows an example where all neurites left the structure directly at the somata or grew out of the grooves after a short distance. The reason is unknown so far, as the culture protocol and conditions were, theoretically, identical to those of the perfect networks depicted in fig. 2.17 and fig. 2.18.

Statistical analysis of the results further revealed an extremely low yield of neurites in the grooves. Of 5240 neurons (more than 95% on pre-conditioned SAM substrates, the others in co-culture) adhering to the substrate 83% were located in the pits. The rest was either displaced by vibrations from moving the culture chamber directly after placing neurons in the pits, or they were pulled out by the growing neurites during the subsequent culture period. (Initially, about 10% to 15% more neurons were plated

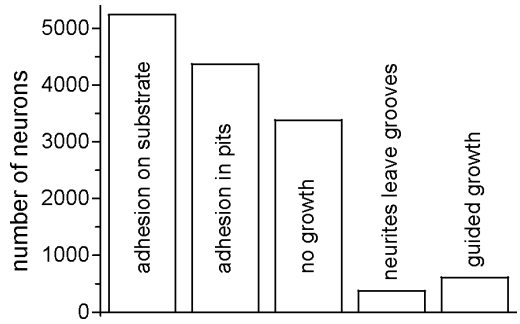


Figure 2.26: *Statistics of neurite growth on substrates with SU-8 topographic structures.*

into the pits one by one, but they failed to adhere to the substrate, presumably because they were not vital, e.g. their membrane was ruptured during the isolation procedure.)
Only 23% of the 4368 neurons in the pits grew neurites, of which 62% were nicely guided by topographic cues as expected, but 38% left the structures directly at the pits or during growth along the grooves, see diagram 2.26. Comparing the last two values shows that guidance itself is not so bad, the main issue being the large number of neurons that did not sprout any neurites at all. In contrast, 64% (n=872) of the nerve cells outside the pits had at least one neurite, almost three times more than inside.

Assuming neurons had initially the same vitality no matter where they adhered and further assuming that the number of cells pulled out of the pits was negligible, the large percentage of cells inside the pits without processes must be attributed to detrimental influences of the topographic structures themselves. Perhaps heavy metabolic ‘waste’ products and remainders of dead cells such as enzymes and organelles accumulate inside pits and grooves, creating a harmful environment which prevents other neurons from sprouting neurites. Imperfect cleaning with tissue from previous cell cultures or toxic chemicals from semiconductor processing (especially with new chips) inside the structures may account for the problems, as well. Various cleaning protocols have been tested, see subsection subsection 2.2.3, but with only modest result. The adverse environmental conditions within pits and grooves might also be responsible for neurites leaving them, thereby reducing the efficiency of growth-cone guidance.
Frankly speaking, chip surface chemistry and cell culture ranging from isolation of neurons to release of growth factors by conditioning brains are not as reliable as needed for an efficient and reproducible growth of defined neural networks.

On the other hand, the nice examples presented above demonstrate that there are no fundamental deficits implicit to topographic guidance. Increasing yield seemed merely a question of improving the cleaning procedure and better cell culture. Therefore, we decided to combine SU-8 topographic structures with transistors and stimulators.

Chapter 3

Single neurons on chips

As outlined in the introduction, long-term supervision of living neural networks requires a non-invasive method for recording from and stimulation of individual neurons.
This chapter briefly discusses various techniques of extracellular recording and introduces the fundamentals of field-effect transistors, inversion channel type as well as buried channel type. Relevant technological aspects of their manufacturing, from design and mask layout to processing in the cleanroom and test measurements, are outlined. The infrastructure needed for operating the devices, such as the custom built amplifier, software and the mechanical setup with the microscope, are presented and a typical experimental situation is described. Section 3.5 introduces the theory of the neuron-silicon interface with capacitive stimulation and extracellular recording, followed by a summary of the results, which demonstrate that individual neurons are fully controllable from the chip.

3.1 Why extracellular recording with silicon chips?

Conventional electrophysiological measurement techniques, like patch clamp or impaled microelectrodes, harm nerve cells, thereby limiting the recording time to a few hours before the cells die. Even though there are methods to control neuronal activity non-invasively with microelectrodes, like the 'whole cell lose patch' configuration [91] where the electrode only touches the neuron but does not rupture its membrane, these are only applicable to small networks. Every electrode needs a micromanipulator for its positioning, which is quite large and limits the number of cells that can be simultaneously controlled to just a few.

An elegant way to monitor neuronal activity are voltage sensitive dyes [14]. Amphiphilic dye molecules incorporate into the cell membrane with their lipophilic part and change their fluorescence depending on the electric field across the lipid bilayer. They do not puncture the neuron, as conventional electrophysiology does, but they are even more harmful, since the dyes become toxic under UV exposure, killing the cells within a few seconds. Except for some special applications where signal propagation along neurites is observed with high spatial resolution, they are hardly suited for monitoring network activity. Calcium sensitive dyes are far less toxic, they alter their fluorescence intensity according to the Ca^{2+} concentration in the surrounding medium. Action potentials are nicely recorded, but they cannot be elicited. This lack of control, common to all dyes, requires additional means to stimulate neuronal activity, like impaled electrodes, making them less favorable for our application.

Metal electrodes are the most well established technique for non-invasive extracellular measurement and stimulation. Although there are several reports about rather fancy configurations in the literature, e.g. electrodes contacting neurons being 'pressed' onto them from above [89, 92] or trapping them in deep vertical cave-like structures with recording sites located at the bottom [67], most electrodes are processed onto planar substrates and nerve cells are cultured on top [40]. They can be used for stimu-

lation and recording simply by connecting them either to a current source or an amplifier circuit. Noise is very small, on the order of a few microvolt, allowing the measurement of individual action potentials even from small vertebrate nerve cells such as rat hippocampal neurons.
Despite these virtues, their metallic nature raises several problems. Currents entering from different locations beneath the cell are integrated by the metal layer, resulting in the signal being averaged over the entire junctional area. This is rather severe if the electrode is only partly covered by the neuron, as signals are short-circuited to the bath, reducing their amplitude considerably. Another issue is that the measurement process itself can influence the recorded transient. Depending on whether the electrode is connected to a high impedance operational amplifier or to a low impedance circuit, allowing currents to flow to ground, the signal is either the voltage or its first temporal derivative (if the capacitance dominates). While both configurations are used [71, 72, 76], their specific features are not considered even in detailed theoretical models of the neuron-electrode junction [10, 88]. In consequence, the physics behind the recorded signal is hardly understood.
Most electrodes are very large, with diameters between 10μm and 50μm, and are usually platinized or coated otherwise, presumably to improve the signal-to-noise ratio. Surfaces treated in such a way are mechanically unstable, due to the fine fragile structures that build up.
Complex electrochemical reactions at the metal-electrolyte (cell culture medium) interface, such as local miniature battery currents and release of metal ions into the electrolyte, may also affect extracellular recording. Yet they are of much greater concern for stimulation, where voltage or current pulses are applied to the metal layer [26]. If the voltage between metal and bath exceeds a threshold of about 1.2V, irreversible electrochemical reactions occur, e.g. electrolysis of water, that are toxic to the tissue and corrode the electrodes. To minimize such adverse effects, biphasic stimulation pulses with a zero total charge flow are generally used.
Furthermore, stimulation artifacts often saturate the amplifiers, preventing the recording of neuronal activity for up to a few tens of milliseconds immediately afterwards.
Most issues discussed above are considerably improved by a careful choice of pulse protocol, amplifier circuit and electrode impedance, enabling reliable stimulation of and recording from cultures of dissociated neurons and slices with multielectrode arrays. However, a major drawback remains, the ill defined metal-electrolyte interface.

Field-effect transistors surrounded by capacitive stimulators are an interesting alternative for the non-invasive control of neuronal activity. Due to a thin insulating layer, usually SiO_2, electrochemical reactions are excluded, providing a well defined electrolyte-silicon interface. This allows an accurate modelling of the signal transfer across the neuron-silicon junction, with the transistor represented by a simple capacitance. Also, the measurement itself is of no concern, since the gate voltage directly modulates the source-drain current without any current flowing across the oxide.
At the present developmental stage one important tradeoff exists; the noise generated by field-effect transistors is substantially higher than in metal electrodes, by about a factor of 5 to 10. Action potentials from small neurons are only detectable when several transients are averaged [113]. Because of these restrictions, most studies are done with large cells that tightly seal with the chip and generate strong currents, providing an acceptable signal-to-noise ratio.
Unlike metal electrodes, FETs are still a new extracellular recording technique that offers further room for improvement. The chances are high that the noise level can be reduced to values comparable to established techniques by employing better semiconductor processes and a different transistor technology. Moreover, CMOS technology allows easy scale-up, such that devices with several thousand transistors can be made. Because of these advantages, field-effect transistors are used in the present thesis.

3.2 Theory part II: Field-effect transistors

The devices for extracellular recording discussed in this section are adapted from conventional metal oxide field-effect transistors (MOSFET). Instead of a thin metal layer, the gate is contacted here by an electrolyte; the device is therefore called electrolyte oxide field-effect transistor (EOSFET). In the past, a transistor type based on an inversion channel beneath the gate oxide has been used in our department. This device, also a standard in semiconductor industry, is briefly introduced together with fundamental concepts of semiconductor physics, followed by a more comprehensive discussion of the buried channel transistor. The latter has been used here for its supposedly better noise performance. Various noise mechanisms are described at the end of this section.
All equations and aspects outlined below are taken from the standard semiconductor literature [78, 108, 128] and textbooks about field-effect transistors [77, 119].

3.2.1 The pn junction

Doping a pure silicon crystal either with elements of the fifth main group like phosphorous (donor) or the third main group like boron (acceptor) shifts the fermi level with respect to the intrinsic value up or down by

$$\phi_F = \frac{kT}{q} \ln \frac{N_D}{n_i} \qquad or \qquad \phi_F = \frac{kT}{q} \ln \frac{N_A}{n_i} \tag{3.1}$$

and it becomes n or p conducting. k is the Boltzmann constant, T the temperature in K, q the elementary charge, n_i the intrinsic carrier concentration and N_D and N_A the respective donor and acceptor concentration.

If the doping profile changes abruptly, e.g. by implanting boron into an n-type substrate, a pn junction is formed, associated with a redistribution of mobile charges at the interface. Holes from the p-region diffuse into the n-region, where they recombine with electrons and vice versa, leading to a depletion of mobile charges. Due to the fixed charges that are still present on each side of the interface a voltage builds up, the 'built-in' voltage

$$V_{bi} = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} \tag{3.2}$$

which causes a drift current of equal magnitude but opposite direction to the diffusion current, resulting in zero net current under static conditions. On both sides of the metallurgic pn junction, defined as the plane where N_D=N_A, remain areas depleted of mobile charges. Their width depends on substrate parameters and the external voltage across the pn junction, V_{pn}, according to:

$$x_n = \sqrt{\frac{2\varepsilon_0 \varepsilon_{Si}}{q} \frac{N_A}{N_D(N_D + N_A)} (V_{bi} - V_{pn})} \tag{3.3}$$

$$x_p = \sqrt{\frac{2\varepsilon_0 \varepsilon_{Si}}{q} \frac{N_D}{N_A(N_D + N_A)} (V_{bi} - V_{pn})} \tag{3.4}$$

and the overall width of the depletion layer is:

$$x_{dep} = x_n + x_p = \sqrt{\frac{2\varepsilon_0 \varepsilon_{Si}}{q} \frac{N_A + N_D}{N_A N_D} (V_{bi} - V_{pn})} \tag{3.5}$$

ε_0 is the vacuum permittivity and ε_{Si} the dielectric constant of silicon. Note that these equations are only valid for a reverse bias that increases x_{dep}. Forward bias conditions are not static and a current flows across the junction.

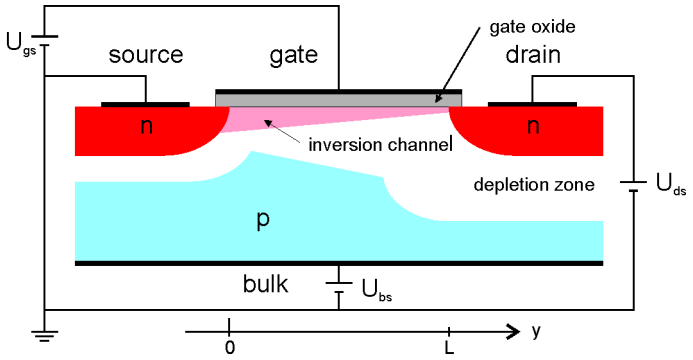


Figure 3.1: *Inversion channel transistor. The width of the gate is W. All connections and the respective voltages are indicated, source is connected to ground.*

3.2.2 The inversion channel FET

Fig. 3.1 shows the schematic drawing of an inversion channel field-effect transistor; two n doped regions, source and drain, are separated by a channel of length L consisting a of p-type semiconductor. The channel is covered by a thin SiO_2 layer insulating it from the metal gate electrode on top. Source is usually the reference connected to ground. No current flows between source and drain terminal as one pn junction, either between source and bulk or drain and bulk, is always reverse biased. This is why the transistor is called a 'normally off' device. When a positive voltage is applied to the gate terminal the holes in the p substrate underneath are repelled, forming a region depleted of mobile charge carriers. The width of the depletion layer, $x_{dep}^{mos}(\phi_S)$, depends on the surface potential ϕ_S of the semiconductor according to:

$$x_{dep}^{mos}(\phi_S) = \sqrt{\frac{2\varepsilon_0\varepsilon_{Si}}{qN_A}\phi_S} \tag{3.6}$$

Raising the voltage between gate and source, V_{gs}, increases ϕ_S and thereby x_{dep}^{mos}. If ϕ_S exceeds $2\phi_F$, the width of the depletion layer does not increase any further, but remains constant at its maximum value of $x_{dep,max}^{mos}(2\phi_F)$. For even higher voltages, electrons accumulate at the silicon oxide interface, forming an n-conducting inversion layer directly connecting the n type regions of source and drain. The area specific charge q_n in this layer is given by:

$$q_n = -c_{ox}(V_{gs} - V_T) \tag{3.7}$$

$$V_T = 2\phi_F + \frac{\sqrt{4\varepsilon_0\varepsilon_{Si}qN_A\phi_F}}{c_{ox}} \tag{3.8}$$

where V_T is the threshold voltage above which inversion sets in, and $c_{ox} = \varepsilon_0\varepsilon_{ox}/d_{ox}$ is the area specific capacitance of the gate oxide, with thickness d_{ox} and dielectric constant ε_{ox}.

The channel allows a current to flow from source to drain as both terminals are now connected by a continuous n conducting path. For the determination of q_n, the voltage drop in the channel $V(y)$, caused by its finite conductivity, has to be taken into account. Therefore, $(V_{gs} - V_T)$ is replaced by $(V_{gs} - V_T - V(y))$ in eq. 3.7, yielding a position dependent specific charge $q_n(y)$. With the electron drift velocity given by $\mu_n dV(y)/dy$, where μ_n is the electron mobility, the drain current is:

$$I_{ds} = -W\mu_n q_n(y)\frac{dV(y)}{dy} \tag{3.9}$$

and after substitution of $q_n(y)$ and integration over the channel length, L, and width, W:

$$I_{ds} = \begin{cases} 0 & V_{gs} - V_T \leq 0 \\ K(2(V_{gs} - V_T)V_{ds} - V_{ds}^2) & V_{gs} - V_T > 0,\ V_{ds} < V_{gs} - V_T \\ K(V_{gs} - V_T)^2 & V_{gs} - V_T > 0,\ V_{ds} \geq V_{gs} - V_T \end{cases} \tag{3.10}$$

$$K = \frac{\mu_n c_{ox}}{2} \frac{W}{L} \tag{3.11}$$

Obviously, I_{ds} is split into three regions, the first where zero current flows since no channel exists, the second, called the linear region, where I_{ds} depends on V_{ds} and the third, saturation region with I_{ds} being independent of V_{ds}. The latter is governed by a partly vanishing inversion due to $V(y)$ exceeding $V_{gs} - V_T$. Increasing V_{ds} has no effect on the current but merely shifts the position where the inversion vanishes towards the source. The model presented above is not valid in this regime, since I_{ds} should be zero without a conducting channel along the full length of the gate.

The threshold voltage of a real device is only poorly approximated by eq. 3.8. Charges within the gate oxide layer and at the semiconductor oxide interface amounting to a total value of q_{ox} as well as the difference in the work functions between metal and semiconductor denoted by ϕ_{MS} strongly affect V_T. This can be accounted for by adding the flatband voltage

$$V_{FB} = \phi_{MS} - \frac{q_{ox}}{c_{ox}} \tag{3.12}$$

to eq. 3.8. It is the voltage that must be applied to the metal-oxide-semiconductor stack in order to achieve flat, unbent energy bands at the junction oxide-semiconductor in the semiconductor.
However, the introduction of V_{FB} shifts the problem to determining this quantity instead of V_T. Usually both values are obtained empirically from measurements at existing transistors, as q_{ox} highly depends on process parameters and conditions during device fabrication.

3.2.3 The buried channel FET

In contrast to inversion channel FETs, the source and drain terminals of buried channel transistors are connected by a permanent channel of the same conduction type; the following discussion always relates to n terminals and n channel in a p substrate, as illustrated in fig. 3.2. Since a conducting layer already exists without any gate voltage applied, the transistor is called a 'normally on' device. The source-drain current is controlled by applying a negative voltage to the gate, constricting the width of the channel. This occurs from two sides: electrons are repelled from the the oxide-semiconductor interface at the chip surface, and the depletion region of the pn junction in the bulk silicon becomes wider. The narrower the channel, the higher is its resistance and the smaller is I_{ds}. Decreasing V_{gs} even further finally causes the conduction path to pinch off and the current ceases.

Approximating the actual gaussian shape doping profile of the implanted channel by a step-profile where the depth of the metallurgic pn junction is denoted by x_j, yields the following expression for the total effective implanted charge per unit area:

$$q_i = q(N_D - N_A)x_j \tag{3.13}$$

N_D is the concentration of implanted donors, N_A the acceptor concentration in the p substrate and q the elementary charge.
$q_s(y)$ is the charge repelled by depletion at the silicon oxide interface when V_g is negative. It depends on the position y due to the voltage drop $V(y)$ along the current path.

$$q_s(y) = -c_{ox}(V_{gs} - V_{FB} - V(y)) \tag{3.14}$$

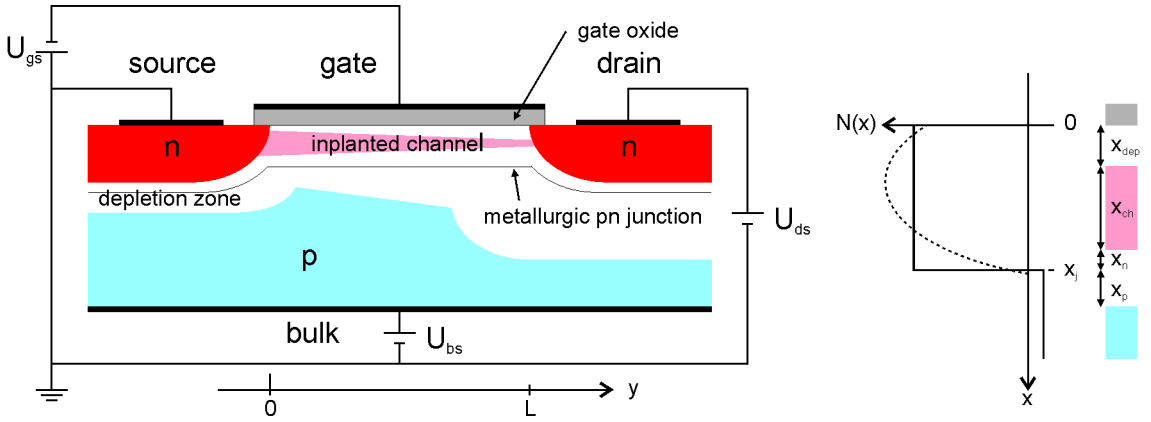


Figure 3.2: *Left: Buried channel transistor. The zone above the line denoted 'metallurgic pn junction' is n conducting. The donor concentration in the channel is much smaller than in the source and gate. Right: Vertical cut through the channel region (magnified). The actual gaussian shape doping profile (dashed line) and the approximated step profile are displayed.* x_j *is the depth of the metallurgic pn junction,* x_{ch} *the width of the channel at the actual position* y*;* x_n*,* x_p *and* x_{dep} *are the widths of the respective depletion layers of the pn junction and at the surface. The colored boxes indicate the electronic conditions; grey: oxide, white: depleted zone, red: n channel and blue: p substrate.*

The charge depleted at the pn junction, $q_b(y)$, can be derived from eq. 3.3 with $-V_{pn}$ substituted by $V_{bs} + V(y)$ according to:

$$q_b(y) = qN_D x_n(y) = \sqrt{2\varepsilon_0 \varepsilon_{Si} q \frac{N_D N_A}{N_D + N_A}(V_{bi} + V_{bs} + V(y))} \tag{3.15}$$

With the relations above, the net mobile charge contributing to the transistor current is:

$$q_n(y) = q_i - q_s(y) - q_b(y) \tag{3.16}$$

In analogy to the inversion channel FET, I_{ds} is obtained from integrating eq. 3.9 with $q_n(y)$ given by eq. 3.16.

$$\begin{aligned} I_{ds} \quad = \quad & \frac{\mu_n W}{L}(q_i V_{ds} + c_{ox}[(V_{gs} - V_{FB})V_{ds} - \frac{1}{2}V_{ds}^2] - \frac{2}{3}\sqrt{2\varepsilon_0 \varepsilon_{Si} q \frac{N_D N_A}{N_D + N_A}} \\ & \cdot[(V_{bi} + V_{bs} + V_{ds})^{\frac{3}{2}} - (V_{bi} + V_{bs})^{\frac{3}{2}}]) \end{aligned} \tag{3.17}$$

Again the current can be assigned to three regions, see fig. 3.3 for a simulation of I_{ds} with parameters typical for the transistors used in this thesis. If V_{gs} is below pinch-off I_{ds} is zero. In the linear region the current is described by eq. 3.17 and in the saturation region, for $V_{ds} \geq V_{ds,sat}$, I_{ds} is independent of V_{ds} and assumes a constant value identical to the maximum current for a given V_{gs}.

As the transistor is controlled by the depletion of mobile charges in the channel it is operated in depletion mode. The device can also be driven with a positive gate voltage, thereby accumulating electrons from the p-bulk into the conduction channel and increasing it conductivity. However, this mode is merely of theoretical interest.

Besides the source-drain current itself, its modulation by changes in the gate or drain voltage is of great concern for the application of transistors in electronic circuits. Two parameters are defined to characterize the respective behavior, the transconductance g_m and the channel conductance g_d

$$g_m := \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}=const} \qquad and \qquad g_d := \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs}=const} \tag{3.18}$$

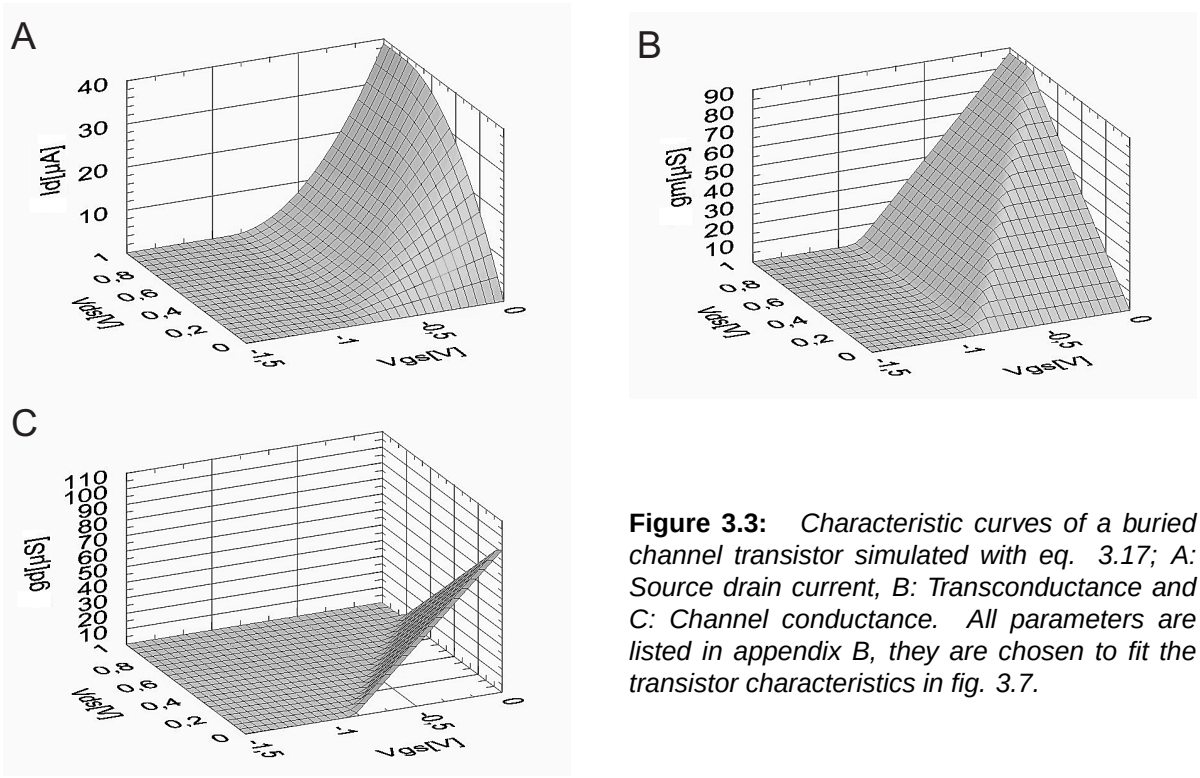


Figure 3.3: *Characteristic curves of a buried channel transistor simulated with eq. 3.17; A: Source drain current, B: Transconductance and C: Channel conductance. All parameters are listed in appendix B, they are chosen to fit the transistor characteristics in fig. 3.7.*

Both parameters are calculated for the simulated device and displayed in fig. 3.3.

The rather simple model of a buried channel FET outlined above describes the electrical behavior of our devices very well. Special cases like short channel effects or saturation of drift velocity are not important here.

3.2.4 Noise mechanisms

Electronic noise generally originates from three sources with a different amplitude and frequency characteristic.

Scattering processes among the charge carriers and scattering centers in the conduction path cause white or thermal noise [6]. The voltage-related power spectral density $S_{V_R}(f)$ of a resistor is proportional to the temperature T and the resistance R, but independent of the frequency f according to:

$$S_{V_R}(f) = 4kTR \tag{3.19}$$

For the definition of $S_V(f)$ see appendix B. All dissipative components with non-zero ohmic resistance are subject to this noise mechanism.

Shot noise results from random passage of individual charge carriers across a potential barrier, e.g. electrons tunnelling through a reverse biased pn junction. The spectral noise density is constant, it neither depends on frequency nor on temperature.

The major source of noise in the low frequency regime of FETs exhibits a striking $1/f$ dependence, and is therefore termed $1/f$ noise. Its physical origin are traps in the gate oxide that emit charges into the conducting channel or capture them from it, thereby modulating its conductance. Every electron removed from an n-conducting channel decreases the density of mobile charge carriers and reduces

the source-drain current, whereas adding electrons has the opposite effect. As thermally grown oxide incorporates traps at various distances from the silicon oxide interface and at different energetic levels, the probability of charges tunnelling from the conducting layer to the traps or being released back shows a abroad distribution. The wide range in time constants of the capture and emission processes associated with the tunnelling probability is the reason for the $1/f$ dependence. A detailed analysis, first done by Mc Worther [68], reveals the following relation for the gate related power spectral density of $1/f$ noise in field-effect transistors:

$$S_{Vgs}(f) \sim \frac{kT}{c_{ox}^2} \frac{n_{ot}}{WL} \frac{1}{f} \tag{3.20}$$

where n_{ot} is the density in oxide traps per unit area [48].

Improving the noise performance of inversion channel FETs is mainly a question of reducing $1/f$ noise, as this is the main source (thermal and shot noise are usually negligible in these devices). According to eq. 3.20 a larger gate area $W \cdot L$ and a smaller oxide capacitance substantially decrease $S_{Vgs}(f)$. However, modifying the geometrical transistor parameters is limited by several constraints. In industrial production, gate width and length are restricted by cost and performance requirements such as cutoff frequency, whereas for our applications the size of the neurons is the limiting factor. The minimal thickness of the gate oxide and its maximum capacitance is governed by the onset of electronic breakthrough, which depends on the maximum voltage across the oxide. For EOSFETs it is usually thicker than for standard MOSFETs, about 10nm, as the layer also protects the bulk semiconductor from ions diffusing into it from the electrolyte.

An important way to improve device performance is reducing the trap density n_{ot}. It can be achieved by a low temperature (450°C) hydrogen anneal which efficiently removes interface trap charges. Yet, the remaining traps still cause considerable noise, not acceptable for many applications.

Because of its different mode of operation, the adverse effects of these traps are considerably lower in buried channel FETs. When operated in depletion mode, the constricted implanted channel is inside the bulk substrate. This reduces the probability of tunnelling and generation-recombination processes with the oxide traps considerably, unlike the inversion layer in inversion channel FETs, which is in direct contact with the gate oxide. Furthermore, the charge carrier mobility inside the bulk is higher than at its surface, allowing larger currents and transconductances.

Alternatively, there are devices such as the junction field-effect transistor (JFET) that completely omit the gate oxide. The source-drain current flows deep in the bulk of the semiconductor, excluding detrimental effects caused by the surface. Due to the lack of traps associated with an oxide layer, these devices have a very low noise, which is dominated by shot noise. Despite these properties, several aspects of JFET fabrication and operation seem incompatible with our application. For example, the oxide-free gate is not stable in the electrolyte and electrochemical reactions might occur, if the voltage applied between transistor and bath is too high.

3.3 The transistor-stimulator chip

Noise is a major issue when neuronal activity is extracellularly recorded with field-effect transistors. Since the dominant source is the FET itself, a reduction can only be achieved with a better device.
Inversion channel transistors, which have been used in our department for many years, are very noisy; see the discussion in the previous section. Better and cleaner processing provides only very limited

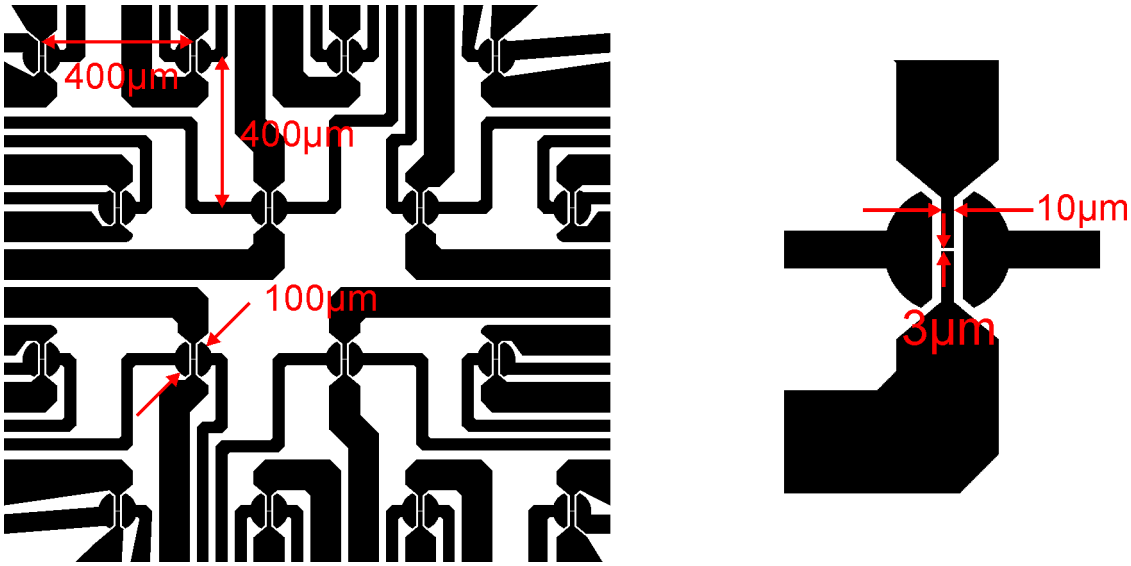


Figure 3.4: *Left: Arrangement of bidirectional units (transistor and stimulator) and leads on the chip. Right: Single unit consisting of a transistor surrounded by two semicircular stimulators.*

room for improvement. A major step forward is therefore only possible with a completely new device. M. Völker was the first in the department who designed and processed buried channel transistors because of their lower noise level compared to the inversion channel devices [116].
Many design features and process recipes given below were adapted from his work.

3.3.1 Design considerations and layout

The following paragraph discusses the design principles of the chip. Neuronal network dimensions as well as the size of individual nerve cells determine the arrangement and geometric features of the transistors.
Unlike the device described in [116], action potentials should not only be recorded, but also triggered extracellularly; this requires a bidirectional interface. In principle, the transistor could be employed for stimulation, too, simply by disconnecting it from the amplifier and applying a stimulation pulse to source and drain. However, this approach results in long settling times after the amplifier is reconnected, during which recording is impossible. The problem is overcome by using two separate sites, one for recording, the other for stimulation [49, 101, 129]. In the actual design here, the transistor is surrounded by two stimulation pads, as shown on the right part of fig. 3.4.

The size of the gate area is governed by two opposing requirements. To minimize transistor noise, the gate should be as large as possible, according to eq. 3.20. Yet, it is limited by the size of the neuron, which has to cover both the transistor and the stimulator. A gate width of 8μm - 10μm is a good compromise. It allows even small cells of 30μm - 40μm diameter to cover at least parts of the stimulators, when placed directly on the gate. The gate length L is either 3μm or 4μm, similar to the chips made in the department so far [49, 129]. This value is the nominal length as defined by the mask. It is reduced by about 0.5μm due to lateral straggling of implanted ions and diffusion during subsequent high temperature processes.

Capacitive stimulation is done via semicircular stimulation pads on each side of the FET. The overall diameter is 100μm, enough to safely evoke action potentials. In contrast to recording, there is no decrease in efficiency if the stimulator is larger than the neuron. Oversized stimulators result in a stronger coupling to the bath and a higher load for the driving electronics, but are of no concern otherwise.

Stimulators and transistors are separated by a 7μm wide insulating zone of bulk silicon with opposite conduction type.

Each chip consists of 16 stimulation and recording sites arranged in a two-dimensional array, where every other horizontal line is shifted by half the internode distance to the right. This configuration enables a multitude of synaptic connection patterns. Promising results from the growth assays described in subsection 2.5.2 suggested that an internode distance of either 400μm or 600μm is easily bridged by growing neurites. These distances provide enough space to route the leads to the transistors and stimulators.
The number of bidirectional units on the chip is sufficient for the studies here. A larger array, e.g. 8x8, which is common for most multielectrode arrays, requires a lot of additional electronics that is too elaborate at this stage.

All masks were drawn with AutoCAD and produced by an external service provider (ML&C GmbH, Jena, Germany). They consist of 5" quartz substrates with a thin nontransparent chromium layer on those areas that shall not be exposed.

Since buried channel transistors are operated in depletion mode with the gate defined by a separate doping step, no local insulation oxides and field oxides are necessary. This is in marked contrast to inversion channel FETs, where both oxides are mandatory. Without, the entire device would be short-circuited by the inversion layer, which would also build up between the leads in enhancement mode. Omitting the insulation oxides on buried channel FETs offers the interesting possibility of producing a completely flat device with potentially better neuron-silicon coupling. Cell adhesion is not disturbed by surface heterogeneities resulting from local oxides protruding up to several tens of nanometers. For these reasons the first chips were processed without local and field oxides, only the gate oxide was present, which covered the entire device.

The conduction type of the channel is defined by the direct contact of the gate with the culture medium (electrolyte). To prevent highly mobile ions like Na^+ from entering the gate oxide, creating traps and shifting the flatband potential, the semiconductor must always be positively biased with respect to the bath. In depletion mode this is only possible with an n channel doped into a p substrate. A positive side effect of this configuration is the higher mobility of electrons compared to holes, leading to an increased transconductance of the n channel devices.
The optimum doping profile with donor concentration N_D and depth of the metallurgic pn junction x_j is determined from the condition that the channel must pinch off before inversion sets in. If the donor concentration is too small, transistor current and sensitivity are below maximum, whereas the channel cannot be pinched-off if it is too high. At $V_{ds} = 0$, implying $V(y)$=0, the channel width is:

$$x_{ch} = x_j - x_{dep}^{mos}(\phi_S) - x_n \tag{3.21}$$

For $V_{bs} = 0$, as the transistor is generally operated, the condition that the channel vanishes immediately before the onset of inversion, yields:

$$x_{j,opt} = x_{dep}^{mos}(2\phi_F) + x_n(V_{bs} = 0) \tag{3.22}$$

and with eq. 3.1, 3.2, 3.3 and 3.6

$$x_{j,opt} = \sqrt{\frac{4\varepsilon_0\varepsilon_{Si}kT}{q^2N_D}\ln\frac{N_D}{n_i}} + \sqrt{\frac{2\varepsilon_0\varepsilon_{Si}kT}{q^2}\frac{N_A}{N_D(N_D+N_A)}\ln\frac{N_AN_D}{n_i^2}} \tag{3.23}$$

Note that N_A in eq. 3.6 is replaced by N_D because of the n doping here. Assuming a step-like doping profile, the dose required for the implantation of a channel with the effective donor concentration N_D is:

$$D = x_j(N_D + N_A) \tag{3.24}$$

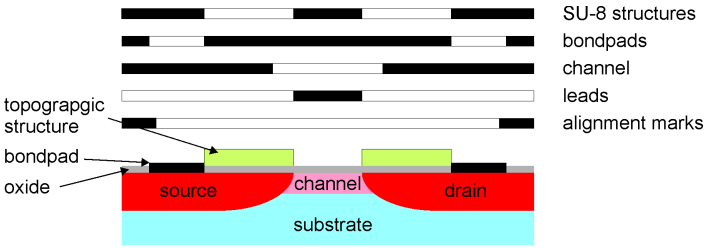


Figure 3.5: *Schematic drawing of the masks needed for chip manufacturing. They are aligned to the respective structures on the chip. Note that the topographic structures are made with a n type resist where the unexposed areas are removed by the development.*

Eliminating N_D in eq. 3.23 by eq. 3.24 gives an implicit relation for the optimum implantation dose for a channel with a predefined depth of the metallurgic pn junction, x_j.
The deeper the junction, the smaller the dose and therefore the donor concentration. A nominal depth of about 100nm seems reasonable. It provides a sufficient distance between the partly constricted channel and the oxide during operation, while allowing a high channel conductance. If it were too deep, the implantation dose would have to be very small, according to eq. 3.23, implying a low donor concentration in the channel, which results in a small transistor current and a poor transconductance and sensitivity.
When determining the implantation energy, several effects must be taken into account. The thin oxide layer protecting the wafer from contamination is removed after this step and a new oxide is grown; both lead to a decrease of x_j. In addition, the profile is broadened by diffusion during subsequent high temperature processes.
Various parameter sets for the channel implantation were selected. The energy was either 60keV, 70keV or 80keV and the dose ranged between $6 \cdot 10^{11}\text{cm}^{-2}$ and $1.3 \cdot 10^{12}\text{cm}^{-2}$. The dopant was phosphorous.

3.3.2 Processing

This subsection outlines fundamental aspects of chip and cleanroom technology; a comprehensive description can be found in the literature [75, 123]. After briefly summarizing relevant steps, important processes are discussed in more detail.

Manufacturing the transistor chip described above comprised six major process steps. Five of them required a separate mask; all masks are drafted in fig. 3.5. First, alignment marks were etched into the wafer. They are important for the accurate alignment of masks to existing structures in subsequent steps. Next, source and drain as well as the stimulation spots and their leads were implanted. A rather thick photoresist layer (1.5μm) protected all other regions. Ions became trapped in it and were removed together with the resist afterwards. To provide low-resistance feed lines the dose was very high, close to the maximum solubility of the implanted element in the substrate. The channel was implanted separately because the dopant dose was approximately a factor of 10^3 smaller and the profile was much shallower than that of the leads. Its mask slightly overlapped the source and drain terminals, rendering the alignment less sensitive to errors in that direction. The entire wafer was covered by a 10nm thin thermally grown oxide that is essential for transistor operation and also protects the whole device from the electrolyte. Thin layers of aluminum on top of the leads, the bondpads, served as electrical contacts. Finally, topographic guidance structures were processed onto the chips with SU-8 resist. After cutting the wafer in single dice, they were glued to ceramic packages and electrically contacted with wire bonds. A cell culture chamber attached to die and package takes up the medium and protects the bond wires. The device was now ready for use, see fig. 3.6.

All steps above are listed in table B.2 in appendix B under process line A. Unfortunately, these chips did not function because leads were short-circuited by the SU-8. Additional measures were necessary to prevent this. They comprised either an insulation implant as in process line B, or the deposition of

a thick field oxide between semiconductor and SU-8 as realized in C. Both procedures were combined in line D, yielding the best results in terms of electrical insulation between adjacent lines. The adverse influence of SU-8 on device properties and appropriate ways of improvement are discussed in 3.3.4.

In the following paragraphs several technological details of chip processing are presented.

The substrate

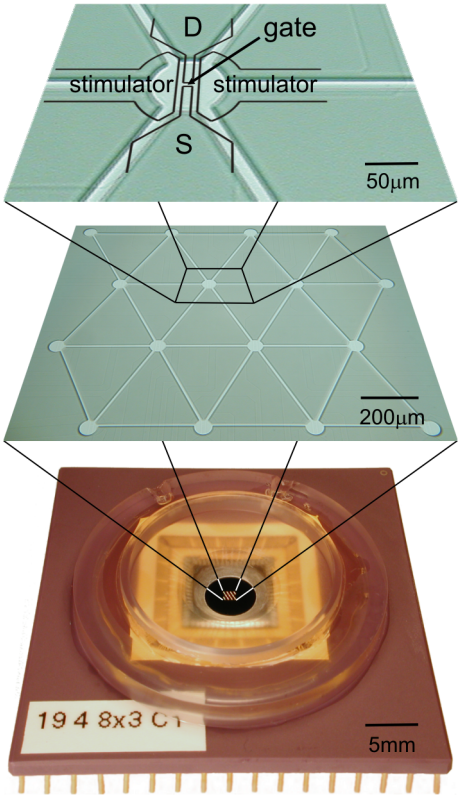
Boron doped 100mm CZ-wafers with [100] crystal orientation and a bulk resistance of 2Ωcm - 4Ωcm were used as substrate. The [100] orientation was preferred over the [111] orientation, which is also readily available commercially, because the density of interfacial traps is much smaller. Also, the number of fixed oxide charges influencing the flatband voltage is reduced by a factor of 3 [78]. Czochralski crystals (CZ) are mechanically more stable and less sensitive to thermal stress and the generation of slips than float zone (FZ) wafers. The higher purity and resistance of the FZ wafers do not outweigh the increased difficulties associated with their processing.
Exact dopant concentration and substrate resistance were of little concern here, which is why wafers with standard parameters were used.

Cleaning

Device characteristics and performance significantly depend upon the purity of the wafers during all steps of processing. Contaminations with metals like sodium and gold especially, can increase noise considerably and even lead to a complete failure.
To ensure that wafers were clean, a three step procedure was applied before every high temperature process and after those processes which might cause contamination, such as ion implantation. First, organic impurities were dissolved in a hot solution of concentrated sulfuric acid and hydrogen peroxide (31%) in a ratio of 3:1, called CARO. Organic residues and metals were removed by SC-1, a mixture of ammonia (25%), hydrogen peroxide and water at 1:1:5, heated to 80°C. The thin oxide layer that grew during the SC-1 process was etched by a short dip in HF (2%), before wafers were immersed into SC-2 at 80°C. It contained hydrochloric acid (37%), hydrogen peroxide and water at 1:1:6. Except for the HF dip, which only took about 10s, all other steps lasted 10min. In between, the wafers were thoroughly rinsed in a quick dump rinser.

Photolithography

Processing a resist mask onto a wafer comprises three steps; deposition of the photoresist, UV-exposure in a mask-aligner and development.
2.5ml resist was spun on the wafer at 4000rpm for 30s, yielding a final thickness of 1.3μm. After a bake at 100°C for 30min, which evaporated excessive solvent, the wafer was irradiated with UV light in a mask-aligner (24mW/cm^2 at 405nm). Best structure resolution, about 1μm, was achieved in vacuum contact mode where the space between wafer and mask was evacuated. However, this mode sometimes resulted in wafers sticking to the mask. In that case the resist had to be removed and the whole procedure repeated. This problem did not occur in hard contact mode, but at the cost of a slightly lower resolution. All mask steps with large structures were done in hard contact mode. Exposed wafers were submersed into MF-84 MX developer (Shipley, Coventry, UK) to dissolve irradiated areas, and thoroughly rinsed afterwards.
The photoresist (ma-P1250, micro resist technology GmbH, Berlin) was p-type; exposed areas were removed by development, leaving a positive image of the mask on the wafer. This type of resist offers the best resolution but is incompatible with cell culture due to its toxicity. Hence, topographic guidance structures were made from the n-type resist SU-8. Its processing was basically the same but more steps were involved, the exact procedure is listed in table B.1.



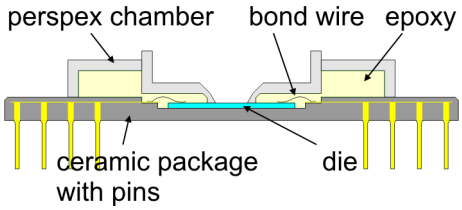


Figure 3.6: *Left: Chip with ceramic package and cell culture chamber, ready to use. Gate, source S, drain D and stimulators are labeled in the magnification of a single bidirectional unit. Parts of the stimulators are covered by the SU-8 guidance structures. Right: Cross-section of a chip, adapted from [49].*

Silicon dioxide

Throughout chip manufacturing many oxide layers were needed, as protective layer, gate oxide and field oxide. They were made by two processes, thermal growth and deposition from the gas phase assisted by a plasma (PECVD, plasma enhanced chemical vapor deposition).
In the first process a 1000°C-1100°C hot wafer is exposed to an oxygen atmosphere. Thin oxide layers up to 30nm can be grown in a RTP (rapid thermal processing) system, where single wafers are heated by light for 30s-60s. Layers of several hundred nanometer thickness are grown in a conventional furnace in a humid atmosphere over several hours.
Long exposure to high temperatures considerably broadens doping profiles due to diffusion. This effect has to be kept in mind when the layout was made. Otherwise short circuits are caused by neighboring leads diffusing into one another.
Alternatively, thick oxide layers can be deposited from silanes and NO_2 in an argon plasma. PECVD is a low temperature process running at 300°C, where diffusion is negligible. Very thick layers, up to several micrometer, can be deposited, which cannot be obtained by thermal growth. The oxide is not very dense and its quality is poor, with many traps incorporated. The quality can be somewhat improved by a subsequent anneal in the RTP at 1100°C for 30s but is still much worse than of thermally grown oxide.

Implantation

Selective doping of wafers can be done either by thermal diffusion or by ion implantation. The latter offers better control over the actual concentration and profile and requires only simple resist masks. For these reasons leads, channels and insulation were doped by ion implantation. They were the only steps that could not be performed in the departmental cleanroom but were carried out by an external service company (IBS, Peynier, France).
Masked wafers were uniformly implanted with the desired ion dose. Ions were absorbed by the photoresist in the masked areas and were incorporated into the wafer in uncovered regions. During the

implantation process the wafer surface was tilted several degrees with respect to the incident beam to prevent high energy ions from travelling along the axis of the crystal too deep into the semiconductor, an effect known as channelling. Channelling was further reduced by a thin scatter oxide. The oxide also protected the wafer from contamination during shipment and handling. After implantation, the ions have to be activated, i.e. they are incorporated into the crystal lattice of the semiconductor by a high temperature anneal which also heales irradiation-induced damage. Annealing was automatically done by thermal growth of oxides in the RTP during consecutive steps.
Mask removal after the lead implantation proved to be difficult. The high-dose, high-energy irradiation crosslinked the photoresist to such an extent that it could not be completely removed even by applying CARO cleaning three times. An additional resist strip in oxygen plasma was necessary.

Bondpads

The metal spots contacting the chip were made by a lift-off process, comprising the following steps. A mask was processed onto the wafer that covered everything, except for the designated areas of the bondpads. After etching the gate oxide in HF, the wafer was sputter coated with a 200nm-300nm thick layer of AlSi and then removed by sonication in acetone. Metal on the resist was lifted off, such that only the layer adhering to the wafer surface remained. The subsequent H_2 anneal alloyed the AlSi with the silicon to reduce the contact resistance. It also decreased the number of traps in the gate oxide, improving the noise performance of the transistor.

Infrastructure

Wafers were cut into dice which were attached to ceramic packages (Spectrum CPGA 208L, San Jose, CA) and electrically contacted with wire bonds as depicted in the right side of fig. 3.6. Custom-made perspex cell culture chambers (6mm in diameter at the bottom) were glued to die and package using a medical silicone adhesive (MK3, Sulzer Osypka, Grenzach Whylen, Germany). The chambers hold the culture medium and protect the fragile bond wires. Epon, a polyester epoxy, was filled in the space between chamber and package. It provides additional mechanical support and prevents medium from coming into contact with the bond wires, if the silicone becomes leaky.

3.3.3 Performance

Process lines B, C and D produced functional chips, with the chips from line D performing best. The insulation between leads proved to be a major problem, especially with the chips of line A. It was tested by applying a voltage between adjacent leads and measuring the resulting current.
As shown in table 3.1, the current between the leads of chips from line A was much larger than the source-drain current of a single transistor, which was in the 5μA-100μA range. The device is completely short-circuited. Only the chips from B and D provided enough insulation for reliable operation. The issue of short circuiting and related aspects are discussed in the next subsection.

process line	:	A	B	C	D
current	:	20μA-3mA	50pA-1nA	200nA-10μA	10pA-20pA

Table 3.1: *Absolute current between two neighboring leads at $\pm$1V for different process lines.*

All functional chips exhibited an I-V characteristic similar to that in fig. 3.7A. It shows the measured source-drain current versus the gate-source and drain-source voltage of a buried channel transistor from process line D with a nominal gate width W=10μm and length L=3μm. Its maximum value is about I_{ds}=40μA for V_{gs}=0V, and V_{ds}=1.0V. The almost horizontal course of the I_{ds} versus V_{ds} curves for

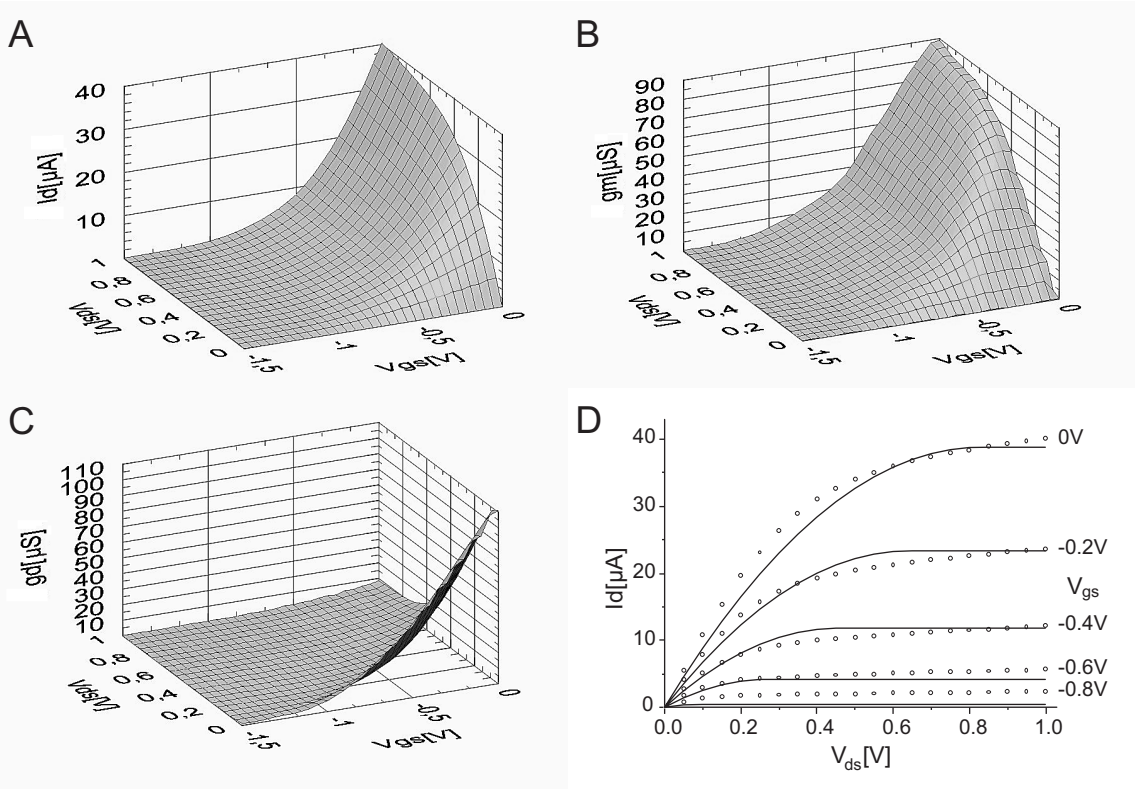


Figure 3.7: *Measured characteristic curves of a buried channel transistor; A: Source-drain current, B: Transconductance and C: Channel conductance. D: Comparison of measured (circles) and simulated (lines) source-drain currents.*

V_{ds} >0.6V indicates that the transistor is in the saturation region for such high source-drain voltages.

Fig. 3.7D displays measured and simulated currents; for easier comparison the diagram is two dimensional. The curves agree rather well, despite the simplifying assumptions in the model, such as the step-shape doping profile. They only deviate for low source gate voltages near channel pinch-off. The theoretical values, which are identical to those in fig. 3.3A, were obtained from fitting eq. 3.17 to the measurement with the flatband voltage V_{FB} and the charge carrier mobility μ_n as free variables. Both quantities are highly affected by the processing and are hard to control. Furthermore, their determination from other tests is elaborate and difficult. All other parameters were fixed, they are well defined by the chip layout and process conditions and are listed in appendix B.

For the measurements in fig. 3.7D, the fit yields V_{FB}=-0.73V and μ_n=112cm^2/Vs. The value of the flatband voltage is quite reasonable. According to eq. 3.12, it is governed by the difference in the work functions of metal and semiconductor, ϕ_{MS}, and the density of the oxide charges, q_{ox}. ϕ_{MS} varies between $\pm$1V, depending on the metal, the dopant type and its concentration [108]. Conditions are different in the system here, because the metal gate is substituted by an electrolyte. Nevertheless, the result indicates that ϕ_{MS} should be in the same range as for the metal gate. Its exact value cannot be calculated from V_{FB} because the number of oxide charges is also unknown.
The fitted electron mobility is considerably smaller than the literature value of μ_n=1500cm^2/Vs [108]. However, when both are compared, one must take into account that the latter refers to the mobility in the bulk, whereas the transistor current flows in a channel near the silicon oxide interface. In this case, electrons are scattered by surface heterogeneities, reducing their mobility.

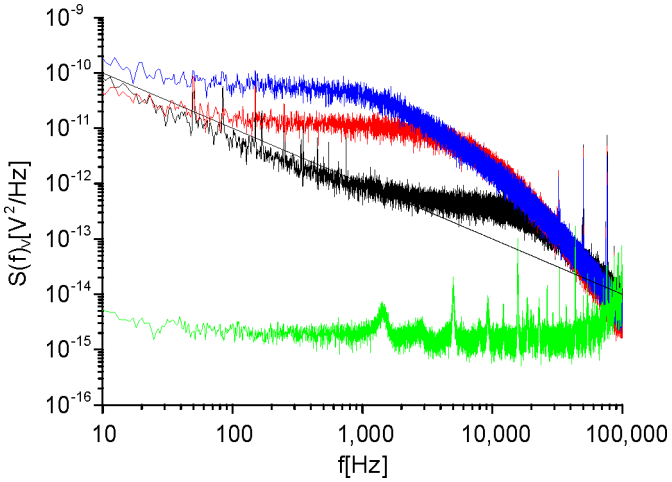


Figure 3.8: *Gate related spectral noise density, $S_{V_{gs}}$ of two transistors on the same chip for different operating conditions. Black: FET 6 with V_{gs}=-1.0V and V_{ds}=0.5V, red: Same transistor operated at V_{gs}=-0.7V and V_{ds}=0.5V, blue: FET1 with V_{gs}=-1.0V and V_{ds}=0.5V. The green curve shows the voltage related spectral noise density, S_{V_R} of an ohmic resistor with 34kΩ. The black line represents the $1/f$ characteristics.*

Noise

As mentioned before, transistor noise is of great concern for successful extracellular recording. It is characterized by the gate-related noise power spectrum $S(f)$, which is the squared absolute Fourier transform of the measured gate voltage; see appendix B. For low frequencies some transistors show the $1/f$ noise behavior discussed in 3.2.4. The black trace in fig. 3.8 nicely coincides with the straight line indicating the $1/f$ law for f <1000Hz. In the two other examples (blue and red curve), the $1/f$ law is only observed for f <100Hz.
The almost horizontal progression followed by a very steep linear drop of the black, blue and red curves in fig. 3.8 corresponds to a Lorenz curve, which is characteristic for the random telegraph signal of a trap with defined transition probability. Thus, the high noise level is presumably due to a single contamination type, in accordance with results from the TXRF analysis in 3.3.4. This conclusion is further supported by the strong dependence of $S(f)$ on the operating point. For example, the black and red trace are from the same device with different gate source voltages applied, -1.0V and -0.7V, respectively. Changing V_{gs} shifts the Fermi level with respect to the trap, resulting in new transition probabilities and consequently in different noise spectra.

Noise also varies greatly among transistors on the same die. This is evident from the blue (FET1) and black (FET6) trace in fig. 3.8, which differ by up to two orders of magnitude; note the logarithmic scale. Both devices were operated under identical conditions.

For comparison, a transistor was replaced by an ohmic 100kΩ resistor. The resistance value is similar to the channel conductance of the transistors. Due to the amplifier circuit with the additional resistor R_S=51kΩ, refer to subsection 3.4.1 for details, the equivalent resistance is 34kΩ. The voltage noise power spectrum of this equivalent resistance is given by the green trace. As expected, the purely thermal noise does not depend on the frequency, but is constant. The broad peaks in the spectrum presumably originate from resonances in the amplifier, whereas the sharp peaks are caused by pick-up from external sources, due to improper shielding. Measured resistor noise is about $2.0 \cdot 10^{-15}$V^2/Hz, not too far away from the theoretical value of $5.6 \cdot 10^{-16}$V^2/Hz given by eq. 3.19. This demonstrates that the amplifier works fairly well and adds little noise by itself.

Classification of device performance is simplified by introducing a new characteristic figure; V_{LFN}. It describes the noise in the low frequency region up to 2kHz, which is relevant for the extracellular recording of action potentials; the definition is given in appendix B. FET1 has V_{LFN}=277μV and FET6 has V_{LFN}=51μV for V_{gs}=-1.0V and V_{ds}=0.5V. The inversion channel transistors of the Adhesios series, that have been a standard device in our department for many years, have a noise between V_{LFN}=90μV

and V_{LFN}=190μV, similar to the transistors above [116]. However, if the gate size is taken into account the Adhesios perform better, with an area of only 3.6μm^2 compared to the 40μm^2 of the transistors in this study. According to eq. 3.20 noise inversely depends on the gate length and width, so that the transistors with the larger gate should have a $\sqrt{11}$-fold lower V_{LFN} value under otherwise identical conditions.

In conclusion, the new chips are worse than the standard devices, despite their theoretically superior technology. The buried channel design cannot be held responsible for this, as the first transistors in [116] have a noise of only V_{LFN}=40μV at a gate size of 5μm x 2μm. Reasons for the poor performance here, such as contaminations and adverse effects of the SU-8, are discussed in subsection 3.3.4.

Stimulators

The capacitive stimulators surrounding the FETs are passive elements that are not critical in processing and operation. To evoke action potentials in the neuron above, voltage steps or pulses are applied, charging the spots. The maximum amplitude is determined by the break-down voltage of the oxide on the stimulator, which is about 10V. It is of no concern here since the amplifier only supplies 5V.
The calculated oxide capacitance of each semicircular spot is approximately 7pF (oxide thickness 10nm, spot size approximately 2000μm^2). This capacitance is connected in series to the capacitance of the Helmholtz layer at the oxide-electrolyte interface and the capacitance of the space charge region in the semiconductor at the semiconductor-oxide interface. The latter strongly depends on the voltage applied between spot and bath; refer to [108] for the capacitance of a metal-insulator-semiconductor system. Recent studies revealed that the oxide capacitance might be further affected by ions diffusing from the electrolyte into the oxide [118]. For the doping concentrations of the stimulator spots and the electrolyte used here, the oxide capacitance has the smallest value and therefore dominates the series connection of all three capacitances; the two others can be neglected.

Repeated use and corrosion

The I-V characteristic of the transistors changes considerably during their lifetime. Unlike commercial devices, which are completely sealed and protected from environmental influences, their gate oxide is in direct contact with biological tissue, culture medium and detergent. Ions diffuse into the gate oxide and affect the device characteristics. Furthermore, the oxide is corroded by alkaline cleaning solutions and the cell culture itself. For example, the culture of hippocampal slices is so aggressive that the oxide is completely dissolved after a few weeks and holes of several micrometer depth appear in the bulk silicon [3]. Culturing snail neurons is far less harsh, but still affects the devices.

New chips, no matter from which process line, behaved more like an ohmic resistor than a field-effect transistor. The expected current characteristic is only observed after an ‘activation’ clean in 50°C Tickopur solution (1% in water, see appendix A, glass coverslip cleaning) for 5min. This very unusual behavior is probably due to charged residues from previous process steps, that bend the energy bands in the silicon and render the device inoperative. Alternatively, the chip surface must be made hydrophilic first in order to enable direct contact between the electrolyte and the gate. The special design with deep topographic structures might increase the need for hydrophilicity. In some cases, little air bubbles were seen in the pits after filling medium into the culture chamber. These bubbles insulate the gate from the reference electrode. Once the chip is activated, it is ready for use.

Before cells are plated, the I-V characteristic of each transistor is measured for the calculation of the

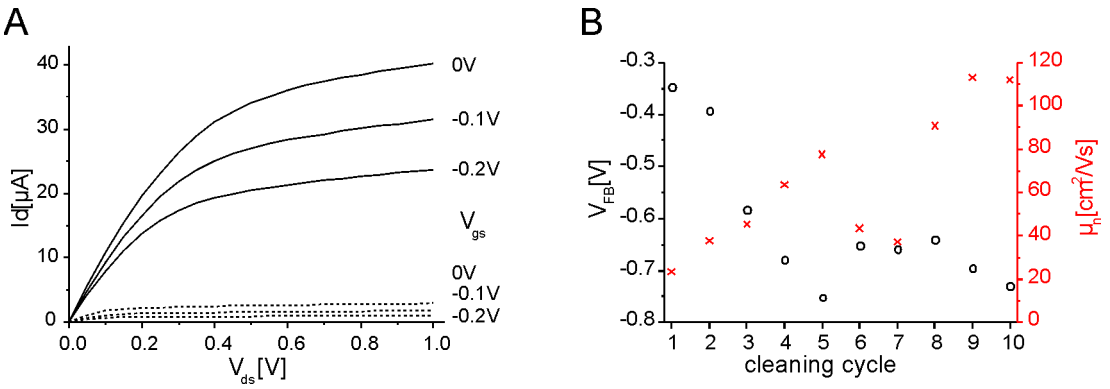


Figure 3.9: *Aging of a transistor. A: Drain current after the first (dotted lines) and tenth (solid lines) cleaning cycle. B: Flatband voltage (black circles) and charge carrier mobility (red crosses) fitted to the source-drain current measured after every cleaning cycle.*

gate voltage from the drain current, refer to section 3.4.1 for details. The procedure is carried out after every cell culture with subsequent cleaning cycle, to minimize errors in the calculated extracellular potential caused by a change in device characteristics. Fig. 3.9A shows the source-drain current curves of a transistor for different gate-source voltages, measured after the first (dashed) and tenth (straight) cleaning cycle. The increase in transistor current is by more than a factor of 10. A similar behavior is observed with most chips used in cell culture. In the 3D diagrams, the I-V curves are shifted towards the left side (lower gate-source voltages), with increasing age. This strongly points to a change in the pinch-off voltage, which is governed by the flatband voltage. Indeed, fitting the theoretical model described in 3.2.3 to the I-V curves measured at different times reveals a drastic decrease in V_{FB}, as shown in fig. 3.9B (black circles). The diagram plots the flatband voltage versus the number of cleaning steps. The parameter 'cleaning cycle' on the horizontal axis denotes the cleaning cycle after which the respective I-V curve was acquired. Assuming a constant ϕ_{MS}, equation 3.12 states that a change in V_{FB} is solely due to the incorporation of ions into the gate oxide, a very realistic phenomenon.
Interestingly, the flatband voltage increases for cycles 6 to 8. This coincides with tests of a new cleaning protocol. Only for cycles 6 and 7 has the chip been treated with chromosulfuric acid. As sulfuric acid has been used before in the form of piranha solution, the change is ascribed to the chromium ions. Theoretically, the flatband voltage should decrease even further because of the positively charged chromium ions, in complete contradiction to the observed effect.

The other free variable in the fit, the electron mobility at the surface, is extremely low, only 23cm^2/Vs. Typical values reported in the literature range from 100cm^2/Vs to 500cm^2/Vs, depending on the electric field transverse to the channel [43]. During chip use μ_n increased by more than a factor of 5, which is somewhat surprising. Since oxide and interface charges influence current transport by coulomb potential scattering and fluctuations of the surface potential [99], one might expect the mobility to decrease with an increasing number of oxide charges. However, the case is far more complicated, as the charges themselves affect the electric field in the gate and screening must be taken into account. A detailed investigation of the observations here is beyond the scope of this thesis.
As for the flatband voltage, the chromosulfuric acid clean has a strong impact on electron mobility, see the drastic decrease of μ_n for cleaning cycle 6 and 7 in fig. 3.9B.

The oxide thickness changes only little. Before the first use it was 10nm, and after the tenth cleaning procedure 8nm were measured. Because its actual value has not been determined every time, all fits were done with d_{ox}=10nm. Resulting errors are not so big and do not alter the effects of aging. For example, fitting the current curves measured after cycle 10 with d_{ox}=8nm instead of 10nm, yields V_{FB}=-0.76V and μ_n=89cm^2/Vs, the overall rise of the mobility becoming slightly smaller.

Clearly, alterations in oxide thickness do not account for the observed aging of the chip. Rather, it is caused by changes in its composition, namely the incorporation or removal of ions.

3.3.4 Discussion

Unfortunately, the manufacturing of the new buried channel transistors with SU-8 guidance structures on top turned out far more difficult than expected. Also, device performance is rather disappointing, especially in terms of noise. The following paragraph discusses possible reasons. Some are of a speculative nature due to the lack of clear information about contaminations and the influence of the SU-8 resist.

The first chips fabricated according to process line A (see appendix B) turned out to be inoperative because of a **short-circuit** between the leads. To determine its origin, a second wafer was processed under identical conditions and with the same parameters. This time, the lead insulation was tested after every step, the results are listed in the table below.

step No.	:	28	29	30
description	:	lift-off	H_2-anneal	SU-8 structuring
current	:	2nA-60nA	0.1nA-2nA	46μA-3mA

Table 3.2: *Absolute current between two neighboring leads at $\pm$1V after different process steps. The step number refers to table B.2 in appendix B.*

Since testing device properties requires electrical contacts for the probe tips, such tests can be carried out the first time after the bondpads are processed. At this point, the insulation is acceptable, with leak currents of 2nA-60nA. The H_2-anneal substantially improves the situation as it reduces the currents by more than a factor of 10. Processing of the topographic structures on top of the chips destroys them completely. The leak currents increase by six orders of magnitude and the device is short-circuited.

Obviously, the SU-8 photoresist is the cause of the failure. Positively charged residues in the resin might account for this. They attract electrons to the surface of the p bulk areas, creating an inversion layer between the leads which short-circuits them. This would also explain why functional chips from later process lines must be activated first before they exhibit the typical I-V characteristic. If only a thin layer of resist, or even a few molecules, remain on the gate, additional electrons are attracted from the bulk to the n-channel and the device runs in enhancement mode. Large gate-source voltages are needed to compensate for this and pinch-off the channel.
A proof of the hypothesis above would require a detailed analysis of the composition of SU-8 to find out whether it contains a heavily charged component or not.

The problem would never have occurred with the conventional inversion channel FETs used thus far, because of their local insulation oxide (LOCOS). It prevents an inversion layer from building up between the leads in this operation mode and therefore also prevents the adverse influence of SU-8.
LOCOS is definitely the best protection against device short-circuiting. However, its deposition is elaborate, requiring an additional mask, and the entire processing would have to be repeated with new wafers. As more than 10 wafers already had the leads implanted at the time the problem was discovered, two alternative solutions were tested.
A higher acceptor concentration in the bulk raises the threshold voltage according to eq. 3.8. The idea is to increase N_A to such an extent that the onset of inversion is shifted beyond the field induced by the charges in the SU-8. This is realized in process line B by the additional steps 14-16 in table B.2. The whole wafer, only the gates are protected by resist, is additionally implanted with boron at a dose of $9{\cdot}10^{12}\text{cm}^{-2}$, yielding a concentration of $2{\cdot}10^{18}\text{cm}^{-3}$. Leads are not affected by the implant as their

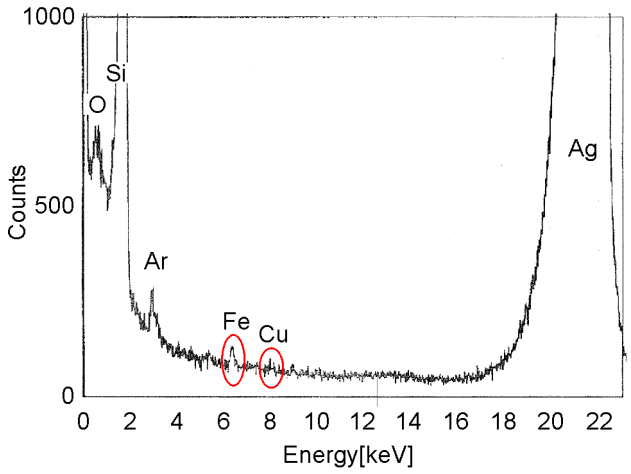


Figure 3.10: *TXRF spectrum of a wafer. Red marks indicate small peaks of iron (6.4keV) and copper (8.1keV). The large Ag-peak originates from the silver X-ray tube.*

charge carrier concentration is $2{\cdot}10^{20}\text{cm}^{-3}$, two orders of magnitude larger. This solution proves to be very efficient, the insulation is improved considerably see table 3.1, and the chips work well.
Alternatively, the short circuit can be prevented by a thick oxide layer between chip and SU-8, shielding the semiconductor from the resist's influence. Before the topographic structures are processed, a 700nm thick PECVD field oxide is deposited onto the wafers in process line C, steps 17-23 in table B.2. It is etched away at the pits and grooves to enable direct contact between neuron and transistor. Although the devices are functional, the insulation is much worse than that of the chips from process line B. In fact, it is very close to a short circuit, as the drain current of about 30μA is only slightly above the leak current between 200nA-10μA.
Best results are obtained by combining the insulation implant and the field oxide in process line D. These transistors have an excellent insulation and perform fairly well, as demonstrated by the example in the previous section.

The second major issue associated with the new buried channel transistors here is the **unsatisfactory noise level**. It is so high that only signals from neurons with a strong coupling to the chip can be recorded. To obtain a high yield of electrically controlled cells, low noise transistors are required.
The chips in [116] demonstrate that a low noise level is achievable with buried channel transistors manufactured in our cleanroom. They have V_{LFN}=40μV at a gate size of 5μm x 2μm. The question is, why are the transistors here so much worse? Since most process steps and parameters are identical or very similar, only two reasons may account for the poor performance: contaminations or an adverse influence of SU-8. The latter is not used in [116].
Wafer contamination was tested with total-reflection X-ray fluorescence spectroscopy (TXRF) by an external service provider (GeMeTec, Munich, Germany). Fig. 3.10 shows the TXRF spectrum of a wafer after the lead implant, the protective oxide still on top. The two marked peaks indicate contaminations with iron and copper at concentrations of $9.2{\cdot}10^{12}\text{cm}^{-2}$ and $3.3{\cdot}10^{12}\text{cm}^{-2}$ respectively (these are close to the detection limits of the technique). Due to the extremely high diffusion coefficients, especially that of Cu, both elements are spread all over the wafer, including the very sensitive gate areas. There they can form traps causing the $1/f$ noise described in 3.2.4. The source of the contamination is unknown. Probably one of the basins used for wet-etching was contaminated, or it originated from abrasion of the metal tweezers used for wafer handling. As there are no copper instruments in the entire cleanroom, the element might have been introduced during ion implantation.

A closer analysis of individual chips points toward other, additional causes. Transistors at the corners of the 4x4 array perform generally much worse than the four transistors in the center. This geometric distribution is in marked contrast to the rather statistical contamination. However, the chip layout gives no

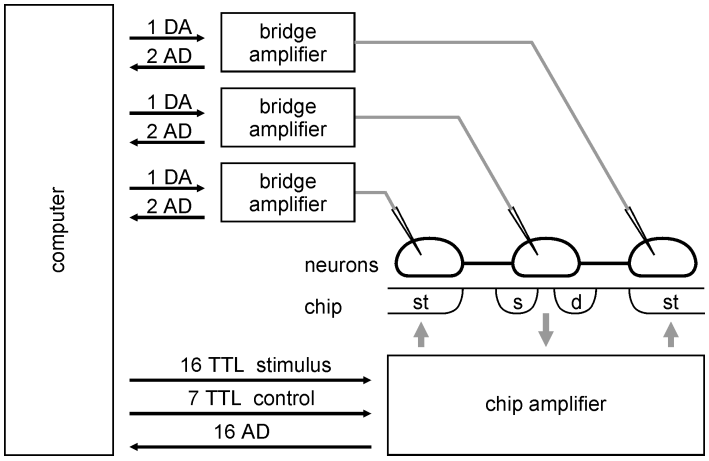


Figure 3.11: *Sketch of the measurement setup. The computer controls the bridge amplifiers via voltages obtained from digital-analog conversion, DA. Measured analog signals from the bridge and chip amplifiers are digitized and stored, AD. 16 TTL (transistor-transistor-logic) lines control the extracellular stimuli and 7 TTL lines set the on-board DACs of the chip amplifier. The chip is represented by the stimulators, st, and the transistor terminals source, s, and drain, d.*

hints for an explanation. Gate dimensions and arrangement are identical for all transistors and only the 'wiring' varies somewhat. Running diagonally across the die, the leads of the FETs in the corners are a little bit longer than those of the transistors in the center. The increase in resistance, at maximum 25% for a total value of about 500Ω, cannot account for the effect, since thermal noise in ohmic resistors is irrelevant. This fact is nicely demonstrated by the green curve in fig. 3.8. Interestingly, the geometric distribution is hardly observed on a special die where the SU-8 resist was not exposed and therefore was dissolved during development; there are no SU-8 topographic structures on this chip. Also, its overall noise level is much smaller.
In conclusion, SU-8 might also be responsible for the high level of noise, in addition to short-circuiting the leads.
Presently, these arguments are mere speculation. A fundamental analysis is needed, with transistors that never got in touch with SU-8 serving as reference.

3.4 Measurement setup

An entirely new setup was designed, built and programmed for this thesis because none of those existing in the department matched the requirements. It is capable of controlling network activity of up to 16 neurons via the chip, while recording the membrane potential of three nerve cells with conventional impaled microelectrodes at the same time. Fig. 3.11 depicts a sketch of the setup with the connections between the individual components. The microelectrodes serve as a reference for checking whether cells are dead or the neuron-silicon junction is bad, in cases where no signal is detected by the transistors. Furthermore, standard electrophysiology is required to characterize synapses. The following paragraphs describe some aspects of setup construction and operation in more detail, and all steps of a typical experiment are shown.

3.4.1 Chip amplifier

The custom-built amplifier comprises two separate units, the actual amplifier and a circuit for generating the voltage pulses applied to the stimulators. Both are implemented on the same PC-board. Chips are connected by a ZIF (zero insertion force) socket that minimizes mechanical stress on the neural networks during insertion and removal, see fig. 3.14. To prevent noise pick-up from the power supply and avoid ground loops, the whole system runs on batteries.

Fig. 3.12 depicts the layout of a single amplifier unit; altogether 16 are implemented on the PC-board.

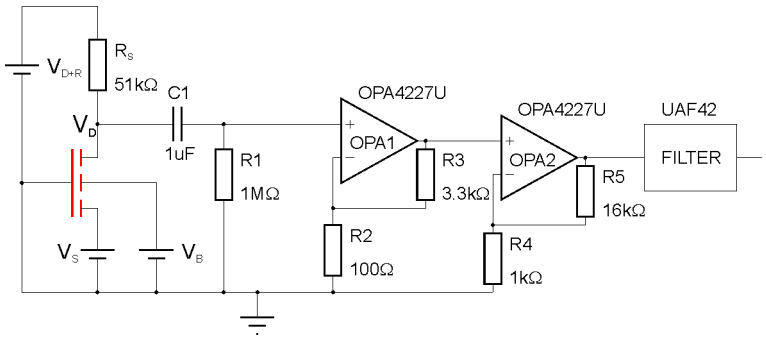


Figure 3.12: *Circuit diagram of the amplifier. The FET is marked in red with its four terminals gate, source, bulk and drain. OPAs and filter are from Burr Brown (now Texas Instruments).*

All transistor voltages are supplied from DACs with driver units and filters, they are symbolized by simple voltage sources in fig. 3.12. In contrast to the theory section 3.2 gate and not source is set to ground potential. This is more convenient and reduces noise pick-up, since the bath electrode also serves as a reference for the electrophysiology amplifiers.
Conversion of the source-drain current into a voltage is done by the serial connection of the FET and the ohmic resistor R_S. For small signals this circuit has a gain of [116]:

$$A = \frac{dV_{ds}}{dV_{gs}} = -\frac{g_m}{g_S + g_d} \qquad \text{with} \qquad g_S := \frac{1}{R_S} \tag{3.25}$$

The major contribution to V_D originates from the constant source-drain current at a defined working point and bears no information on network activity. It is removed by a high pass RC-filter with 1000ms time constant. Filtered signals are amplified by two stages, OPA1 and OPA2, with an overall gain of 578.
Aliasing is suppressed by a 4kHz lowpass Bessel filter after OPA2. Signals are digitized with a data acquisition card at 10kHz/channel in the computer and saved to disk.

The other on-board circuit provides voltage pulses for extracellular stimulation. It comprises two DACs with driver units and 16 switches. TTL pulses from a DIO-card in the computer open and close the switches, toggling the stimulators between the two voltages supplied from the DACs. Both voltages are freely selectable between 0V and +5V, but care must be taken that the pn junctions on the chip are always reverse biased. Due to the simple design, only square wave pulses with identical amplitude for all stimulators can be generated. This constraint is somewhat alleviated by the large flexibility in the pulse protocols; arbitrary patterns are programmable for every single stimulator.

Signals at the transistor gate are not directly accessible, but are calculated from the drain voltage. According to eq. 3.25 the values for g_S, g_m and g_d must be known for this. Whereas g_S is given by the amplifier circuit and fixed, the transconductance and channel conductance must be determined from the transistor's I-V characteristic and are highly dependent on the working point. Because of the capacitive coupling between FET and OPAs, the amplifier cannot detect constant currents associated with constant gate voltages. I-V curves are therefore measured with a separate device, the I-V box. It consists of a current-to-voltage converting amplifier directly connected to the drain of the transistors via a 16-channel multiplexer. V_{gs} and V_{ds} are supplied externally from the data acquisition card.

3.4.2 Hard and software

All electronic components of the setup are operated by a Pentium-II computer equipped with two cards from National Instruments. A NI6071E multifunction DAQ-card supplies the analog signals for the I-V box and the electrophysiology amplifiers and acquires all data. DACs on the chip amplifier are programmed and stimulators are controlled by a NI6534 digital pattern I/O-card. It has a very large

onboard memory to which the whole pulse protocol is saved. During a measurement the stimulus pattern is generated from this memory without the need for computer resources; they are fully available for data acquisition. Both cards are synchronized and exchange trigger signals via a special bus system (RTSI).

The software comprises three autonomous programs: one for the I-V box, the genuine measurement program and a viewer for processing the saved data. All were written in LabView 5.1 (National Instruments).
The measurement program is a multichannel transient recorder, similar to a storage oscilloscope, with some additional features. After setting the working points for the transistors, pulses can be applied to the stimulators on the chip as well as to the microelectrodes, and data from the chip and electrophysiology amplifiers are acquired and displayed. To speed up processing and save disk space, data is stored in a binary file format. A special viewer reads and displays the contents of the files and provides several functions, such as export options into other formats, fit routines and filters.

3.4.3 Microscope and electrophysiology

Unlike the electronics, which have been designed to meet the specifications of the transistor chip, the mechanical aspects of the setup are governed by the requirements of intracellular recording. In order to minimize harm to the cells and maximize their lifetime after impalement, any vibration of microelectrodes and chip must be prevented. Amplifier and micromanipulators are therefore mounted on the same table, forming an extremely stable entity. The reflected-light microscope (Olympus, BX50WI) sits on three precision XY stages, which allows scanning of the chip surface without affecting the chips position relative to the microelectrodes. One stage can be seen at the bottom center in fig. 3.13. All components are mounted on a large aluminum plate on top of a vibration damping table. A metal cage enclosing the assembly (not visible in the picture) shields it from noise pick-up.

Electrophysiological measurements are made using sharp glass microelectrodes impaled into the neurons. Electrodes of 30MΩ-60MΩ resistance are pulled from glass capillaries (Hilgenberg, Malsfeld, Germany), filled with saturated K_2SO_4 solution and contacted with a chlorinated silver wire. They are mounted to the XYZ unit of hydraulic micromanipulators (Narishige, Japan) and connected to the input stage of conventional current clamp amplifiers (npi BA-1S, Tamm, Germany). The system is properly shielded, there are no ground loops, and electrode noise is below 500μV peak-peak, unfiltered.

3.4.4 A typical experiment

Many preparatory steps are necessary before neural networks can be studied with the transistor chip. They comprise cleaning the chips, measuring I-V curves, disinfection, coating with poly-l-lysine and placement and culture of the cells. Most of the steps are outlined in great detail in section 2.2.2. Experiments are usually done after 1-3 days *in vitro*, when functional networks have formed.

Ideally, I-V curves of the transistors should be measured immediately before the experiment, to achieve maximum accuracy when calculating the gate voltage with eq. 3.25. This is never done though, since the risk of destroying the precious network is too high. Instead, g_m and g_d are determined from the I-V curves recorded following the cleaning procedure. Since the device characteristics can change during coating and cell culture, affecting g_m and g_d, errors might be introduced by this approach. In cases where the gate voltage must be exact, transistor records are checked by modulating the bath with a reference voltage after the experiment and corrected where necessary.

Compared to the preparations, measurements themselves are relatively easy. The chip amplifier is connected to the batteries and the program is started, initializing the DACs and setting their output to 0V. It is very important that these steps are executed before the chip is connected to the amplifier,

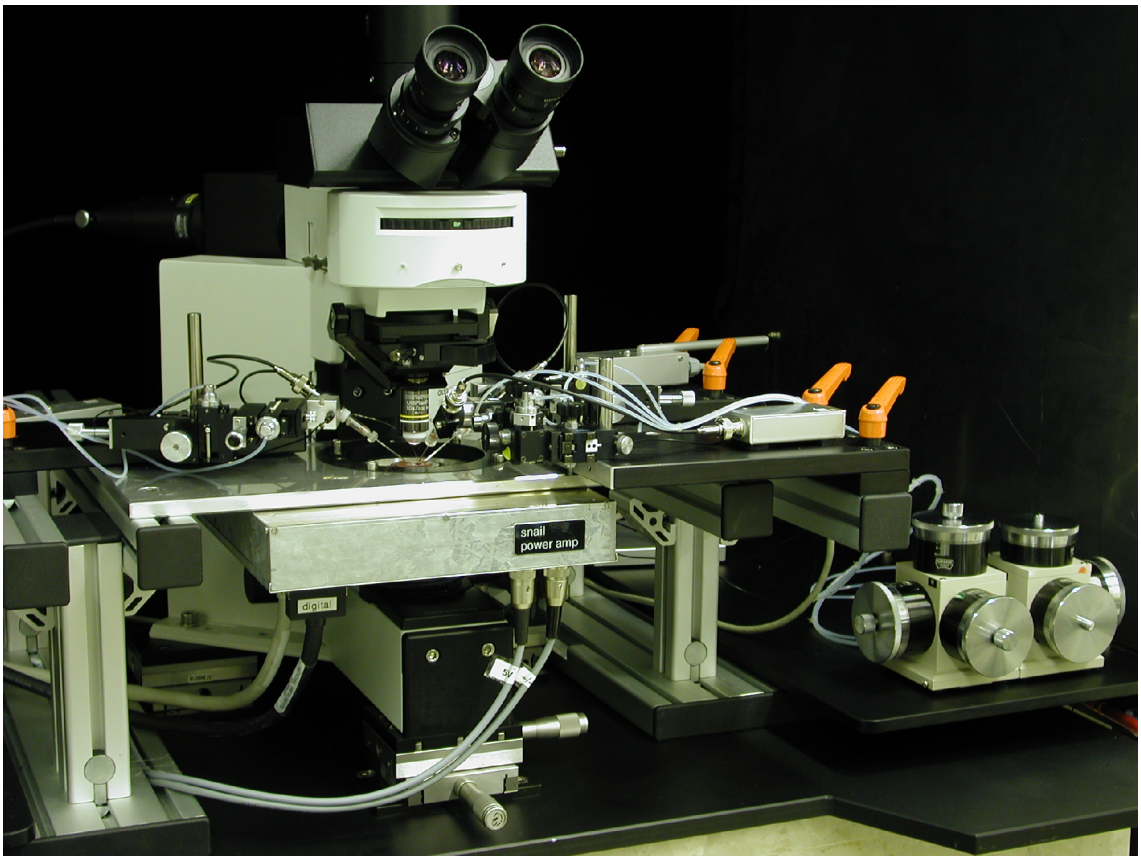


Figure 3.13: *Microscope with manipulators and chip amplifier. Two control units for the hydraulic micromanipulators can be seen on the right hand side.*

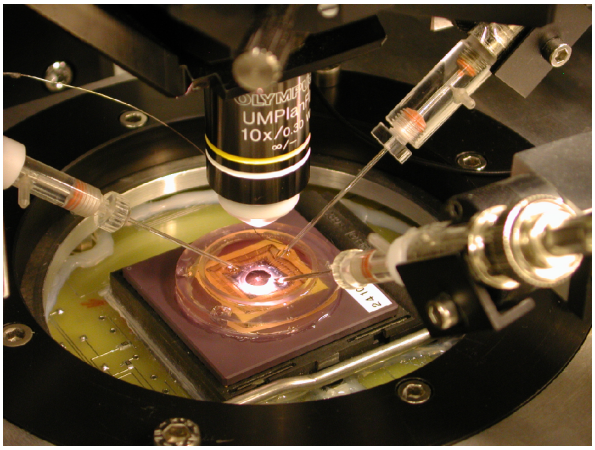


Figure 3.14: *Close-up of a chip connected to the amplifier. Up to three microelectrodes can be used simultaneously. The thin silver wire is the reference electrode grounding the bath.*

otherwise uncontrolled voltages up to ± 15V may destroy the device. The chip is then inserted into the ZIF-socket and grounded by the bath electrode. Some cells are impaled with glass microelectrodes to record their intracellular potential.
Usually, experiments start with checking cell vitality and the neuron-silicon junction. Is it possible to trigger action potentials via the stimulators and are the spikes detectable with the transistors? Next,

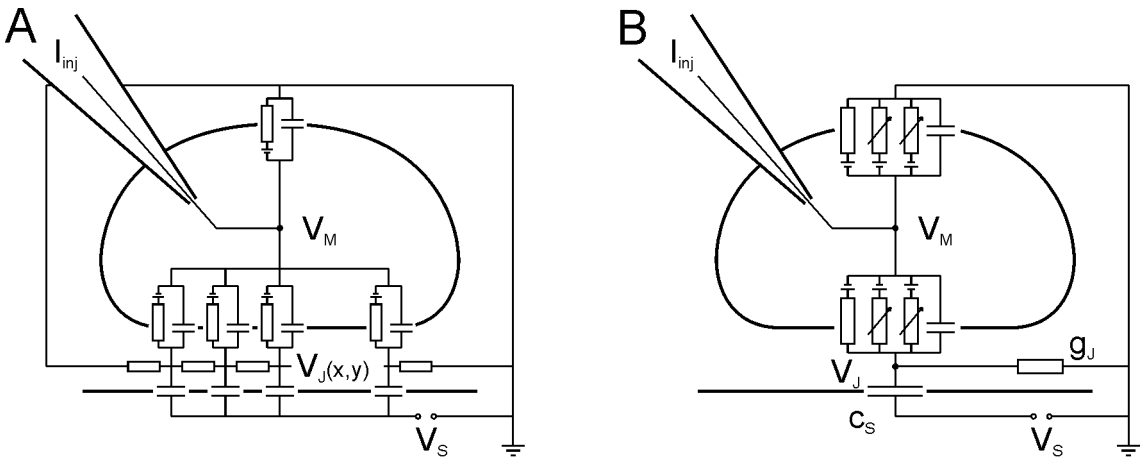


Figure 3.15: *A: Equivalent circuit of the neuron-silicon junction described by the area contact model. For clarity, the cell membrane has only passive components. B: Point-contact model. The behavior of the neuron is described using Hodgkin-Huxley dynamics.*

synapses are characterized electrophysiologically and network activity is studied with the chip. At the end, individual neurons are sometimes stained with Lucifer Yellow to increase the visibility of their neurites and investigate the network's connection pattern.

3.5 Theory part III: Neuron-silicon interface

This section outlines the theoretical relationship between intra and extracellular potential during capacitive stimulation and transistor measurements. Fundamental concepts of the neuron-silicon junction are introduced and applied to the signal transmission from chip to neuron and vice versa. Based on these models, various types of transistor records are characterized and simulated.

3.5.1 Models

When a neuron is attached to a planar substrate, cell adhesion molecules such as integrins and the glycocalix keep the cell membrane at a certain distance from the surface. Depending on cell type and coating of the substrate, the thickness of the cleft ranges between 10nm-100nm as determined from fluorescence interference contrast (FLIC) microscopy [60, 131]. Even this small junction prevents a direct neuron-transistor coupling via electrical polarization.
The extracellular signal detected by the transistor originates from the voltage drop of the current flowing along the cleft. Its basic features can be described by dividing the nerve cell into two compartments, the free membrane and the membrane adhering to the chip, see the drawings in fig. 3.15.

The neuron-silicon junction is a stack of layers with different electrical conductivities. Starting from the chip, there is a thin layer of insulating oxide on top of the bulk silicon, followed by the cleft filled with electrolyte, the cell membrane and the cytoplasm. SiO_2, conducting cleft and cell membrane form a core-coat conductor. Unlike a 'normal' cable, it is stimulated through the coats and its ends are kept at a constant potential defined by the reference electrode in the bath. The voltage profile in the junction $V_J(x, y, t)$ can be calculated from an equivalent circuit consisting of infinitesimal elements of passive membrane, oxide and electrolyte shown in fig. 3.15A. In this picture, the cell membrane in the junction is represented by a battery in series to an ohmic conductance g_{JM} connected in parallel to a capacitance c_M. The resistance of the cleft is governed by the conductivity of the medium and its thickness d according to $r_J = \rho_J/d$ and the oxide layer is described by its capacitance c_S. All parameters are area

specific. Applying Kirchhoff's law yields a modified two-dimensional cable equation [32, 120]

$$-\nabla\left(\frac{1}{r_J}\nabla V_J\right) = c_S\left(\frac{\partial V_S}{\partial t} - \frac{\partial V_J}{\partial t}\right) + c_M\left(\frac{\partial V_M}{\partial t} - \frac{\partial V_J}{\partial t}\right) + g_{JM}(V_M - V_J - V_0) \quad (3.26)$$

V_S is the voltage applied to the chip and V_0 the resting membrane voltage of the neuron. The equation describes the balance of all currents in the junction, where the left side describes the ohmic current along the cleft and the right side the capacitive currents of membrane and chip as well as the ohmic current of the membrane. Taking spatial variations of cell and device properties into account to determine the local potential profile, the **area-contact model** is well suited for studying the properties of the neuron-silicon junction [31].

However, the model is too complicated when transistors are used as ordinary detectors of neuronal activity and the detailed characteristics of the cleft are of minor interest. For such applications, FETs with large gates are generally used to obtain a better signal-to-noise ratio. The extracellular voltage is integrated over the whole gate area, resulting in a spatially averaged transistor signal.
In this case, the electrical properties are more easily described by a simplified system with average parameters, the **point-contact model**. Fig. 3.15B depicts the respective equivalent circuit. The sheet resistance of the cleft is substituted by a global conductance G_J and V_J does not depend on the position, but is constant. The cell membrane is represented by the potassium, sodium and leak conductances of the Hodgkin-Huxley model with their reversal potentials and the capacitance, as described in section 2.4.3. All components are discrete and describe the entire junction. For convenience, specific parameters are defined with respect to the area of the attached membrane, A_{JM}. They are denoted by lower case letters; $c_S = C_S/A_{JM}$, $c_M = C_M/A_{JM}$, $g_{JM} = G_{JM}/A_{JM}$ and $g_J = G_J/A_{JM}$. The potential in the junction, $V_J(t)$, is obtained from Kirchhoff's law

$$g_J V_J = c_S\left(\frac{dV_S}{dt} - \frac{dV_J}{dt}\right) + c_M\left(\frac{dV_M}{dt} - \frac{dV_J}{dt}\right) + \sum_i g^i_{JM}(V_M - V_J - V^i_0) \quad (3.27)$$

where g^i_{JM} is the conductance of the ion channels ($i \in Na, K, leak$) in the junction membrane and V^i_0 the respective reversal potential.

To avoid confusion due to an overcomplicated diagram, a purely passive membrane has been assumed in fig. 3.15A. Of course, the area contact model also works with a membrane described by the Hodgkin-Huxley dynamics. In fact, integrating the voltage profile $V_J(x, y, t)$ across the whole junction area yields the same temporal behavior as with the point-contact model; only the amplitude differs by a scaling factor which is governed by the seal resistance of the cleft and depends on the integration [32, 120].

So far, the neuron-silicon junction was discussed in general, without respect to the direction of signal transfer. This is different in the following subsections, where capacitive stimulation and extracellular recording are outlined.

3.5.2 Capacitive stimulation

Action potentials can be triggered from the chip by applying voltage pulses $V_S(t)$ to the stimulators. The capacitive current through the oxide causes a current in the cleft, associated with a change in V_J. This opens voltage-gated channels or induces reversible electroporation. Both increase the intracellular potential V_M and evoke action potentials if the depolarization is strong enough.
The equivalent circuit in fig. 3.15B applies to a neuron on top of a stimulator which entirely covers the contact area. For a complete description, a second equation in addition to eq. 3.27 is required,

characterizing the dynamics of the entire cell

$$c_M \frac{dV_M}{dt} + \sum_i g^i_{FM}(V_M - V^i_0) = -\beta_M \left[c_M \left(\frac{dV_M}{dt} - \frac{dV_J}{dt} \right) + \sum_i g^i_{JM}(V_M - V_J - V^i_0) \right] \quad (3.28)$$

The left side denotes the current through the free membrane with the ionic conductance g^i_{FM}, the right side the current through the junction membrane. $\beta_M = A_{JM}/A_{FM}$ is the ratio of the areas of the junction membrane A_{JM} to the free membrane A_{FM} and g_{FM} is the channel conductance in the free membrane.
Below, several types of extracellular stimulation are discussed, each defined by a different set of cell and junction parameters.

Neglecting the ion channels in the whole cell, the following equations are derived from eq. 3.27 and eq. 3.28

$$(c_S + \widetilde{c}_M)\frac{dV_J}{dt} + g_J V_J = c_S \frac{dV_S}{dt} \quad (3.29)$$

$$\frac{dV_M}{dt} = \frac{\beta_M}{1+\beta_M}\frac{dV_J}{dt} \quad (3.30)$$

with $\widetilde{c}_M = c_M/(1+\beta_M)$. These conditions are identical to the A-type coupling outlined in the following subsection, but with signal transfer from chip to neuron and not vice versa. If a voltage step $V_S(t) = V^0_S\Theta(t)$ is applied to the stimulator it causes capacitive voltages across the adherent membrane, $V_M - V_J$, and free membrane, V_M. These voltages decay mono-exponentially with a time constant $\widetilde{\tau}_J = (c_S + \widetilde{c}_M)/g_J$ according to:

$$V_M - V_J = -\frac{1}{1+\beta_M}\frac{c_S}{\widetilde{c}_M + c_S} V^0_S e^{-\frac{t}{\widetilde{\tau}_J}} \quad (3.31)$$

$$V_M = \frac{\beta_M}{1+\beta_M}\frac{c_S}{\widetilde{c}_M + c_S} V^0_S e^{-\frac{t}{\widetilde{\tau}_J}} \quad (3.32)$$

The two voltages have opposite sign. With the neuron parameters listed in appendix C and a voltage step of $V_S(t)$=5V$\Theta(t)$, the junction membrane is hyperpolarized by $V_M - V_J$=-1,3V and the free membrane is depolarized by V_M=85mV, decaying with $\widetilde{\tau}_J$=17μs.

In analogy to B-type coupling discussed in subsection 3.5.3, stimulation can be dominated by a leaky membrane in the junction with a conductance g^{leak}_{JM}. Assuming that the intracellular voltage is small compared to the extracellular voltage (since V_J is modulated by the chip), $V_M - V^{leak}_0 \ll V_J$ and $dV_M \ll dV_J$, and omitting all other ion conductances, eq. 3.27 results in:

$$(c_S + c_M)\frac{dV_J}{dt} + (g^{leak}_{JM} + g_J)V_J = c_S \frac{dV_S}{dt} \quad (3.33)$$

Application of a voltage step $V_S(t) = V^0_S\Theta(t)$ causes a transient in the junction

$$V_J = \frac{c_S}{c_S + c_M} V^0_S e^{-\frac{t}{\tau_J}} \quad (3.34)$$

which charges the cell. This capacitive charging decays with the same time constant $\tau_J = (c_M + c_S)/(g_{JM} + g_J)$ as $V_J(t)$; but meanwhile the ohmic current through the leak conductance changes the intracellular voltage by [32]

$$\triangle V_M = V^0_S \beta_M \frac{c_S}{c_M}\frac{g^{leak}_{JM}}{g^{leak}_{JM} + g_J} \quad (3.35)$$

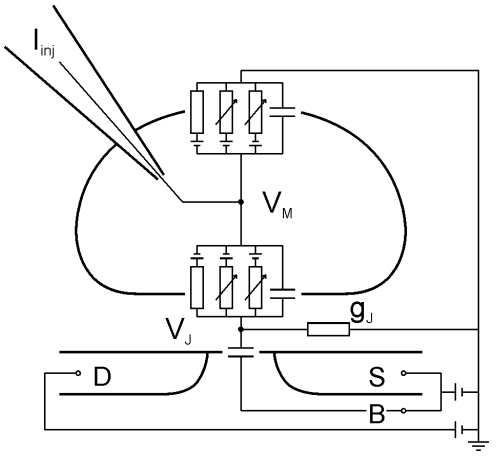


Figure 3.16: *Equivalent circuit of a neuron on a field-effect transistor. The neuron-silicon junction is described by the point-contact model and the behavior of the nerve cell by the Hodgkin-Huxley model. The whole transistor, leads and gate, acts like an ordinary capacitor with capacitance c_s. Here, it is represented by its source S, bulk B and drain D terminals.*

Because ion channels are present in a real neuron, $\triangle V_M$ decays, too, but on a much slower rate. With a leak conductance g_{JM}^{leak}=15mS/cm^2 and all other parameters from appendix C, the membrane voltage increases by about 20mV for V_S^0=5V. Depending on the resting potential, this can be sufficient to trigger an action potential.

So far, only configurations with special cell and junction characteristics were considered. Generally, the adherent and free membrane possess active properties governed by their voltage-gated ion channels. The system is again described by equation 3.27 and 3.28, but since no simplifying assumptions can be made, the membrane potential is determined from simulations with a predefined channel distribution.

The transients induced by capacitive extracellular stimulation are far too short for opening ion channels. They decay with time constants in the ten microsecond region more than two orders of magnitude faster than the channels' switching characteristics. The question is, by which mechanisms are the neurons then stimulated? It is discussed in subsection 3.6.1 where the results are presented.

3.5.3 Extracellular recording

During an action potential, voltage-gated ion channels open and ionic currents flow from cytoplasm to extracellular space and vice versa, changing the intracellular potential $V_M(t)$. Depending on the channel distribution between adherent and free membrane, ionic and capacitive currents are driven through the neuron-silicon junction and modulate its voltage $V_J(t)$, which is detected by the transistor, see fig. 3.16. The system is described by the same equivalent circuit and equations as for stimulation, only that this time signals are transferred from neuron to the chip. Furthermore, the stimulator is replaced by a field-effect transistor, but with identical effects on the electrical properties of the junction. The transistor behaves like a common capacitor. Since its capacitance is smaller than that of the cell membrane and the signal is generated by the neuron, capacitive currents in the chip can be neglected in equations 3.27 and 3.28. With the additional assumption that the extracellular voltage is much smaller then the intracellular (the signal is generated by the neuron and transmitted to the cleft), $V_J \ll V_M$ and $dV_J \ll dV_M$, these are simplified to:

$$g_J V_J = c_M \frac{dV_M}{dt} + \sum_i g_{JM}^i (V_M - V_0^i) \tag{3.36}$$

$$(1+\beta_M) c_M \frac{dV_M}{dt} = -\sum_i (g_{FM}^i + \beta_M g_{JM}^i)(V_M - V_0^i) + (1+\beta_M) i_{INJ} \tag{3.37}$$

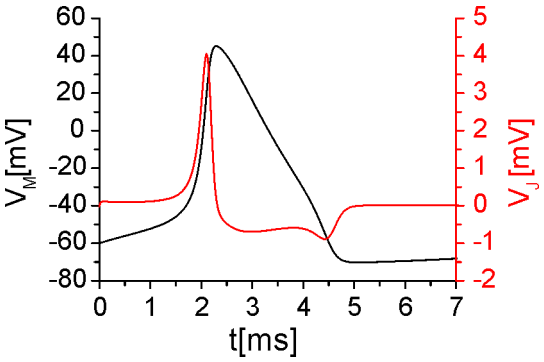


Figure 3.17: *Simulated intracellular voltage V_M (black curve) and junction voltage V_J (red curve) for a completely passive adherent membrane, μ^i_{JM}=0.*

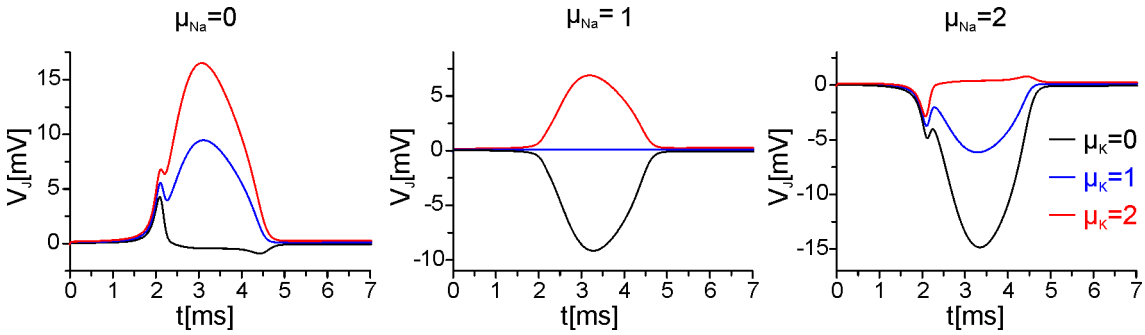


Figure 3.18: *Simulated junction voltages V_J resulting from an action potential. Black curves: μ_K=0, blue curves: μ_K=1, red curves: μ_K=2. The diagram on the left shows transients for μ_{Na}=0, the one in the middle for μ_{Na}=1 and that on the right for μ_{Na}=2. Membrane potentials are identical to those in fig. 3.17 (not shown).*

where i_{INJ} was added to represent the current density injected during stimulation. For a junction membrane depleted of any ion channels, eq. 3.36 is further reduced to:

$$g_J V_J = c_M \frac{dV_M}{dt} \tag{3.38}$$

In this case, which has been termed A-type coupling for historical reasons, the current is completely capacitive and $V_J(t)$ is proportional to the first derivative of the intracellular voltage. Simulating the dynamics of the free membrane with the Hodgkin-Huxley model described in subsection 2.4.3 and the neuron-silicon junction with the equation above yields the junction voltage depicted in fig. 3.17; parameters are listed in appendix C.

If the attached membrane is leaky, with the conductance g^{leak}_{JM} dominating all other ion conductances as well as the capacitive current, $V_J(t)$ is solely governed by the ionic current through the leak.

$$g_J V_J = g^{leak}_{JM}(V_M - V^{leak}_0) \tag{3.39}$$

The shape of the extracellular signal for the B-type coupling here is identical to the intracellular voltage. Its amplitude scales with the factor g^{leak}_{JM}/g_J.

Generally, the adherent membrane is not entirely passive as implied in the cases above, but incorporates voltage-gated ion channels. The junction voltage of this C-type coupling is described by:

$$g_J V_J = \frac{1}{1+\beta_M} \sum_i (g^i_{JM} - g^i_{FM})(V_M - V^i_0) + i_{INJ} \tag{3.40}$$

obtained from inserting eq. 3.37 into eq. 3.36. Interestingly, $V_J(t)$ is zero if the ion channels are distributed homogeneously between free and adherent membrane; no signal is then recorded in the

transistor.
Fig. 3.18 depicts various extracellular signals simulated for different channel distributions using equations 3.28 and 3.27. All conductances of the free membrane and g_{JM}^{leak} are constant, the standard parameters listed in appendix C are used. Only g_{JM}^{Na} and g_{JM}^{K} are varied by multiplication with μ^{Na} and μ^{K}. $\mu^{i} < 1$ indicates a depletion, $\mu^{i} > 1$ an accumulation of the respective channel type in the junction. For a depletion of sodium channels the signals are positive, see the left graph in fig. 3.18, while they are negative for an accumulation, as shown by the right graph. If the capacitance and size of the adhesion region are exactly known, the channel distribution can be determined quantitatively by fitting the simulations to experimental curves [103]; under the assumption that the model describes the actual channel dynamics sufficiently well.

The amplitude of the extracellular signal scales linearly with the conductance in the cleft, with the left side of equations 3.38, 3.39 and 3.40 being $g_J V_J$. Typical values are about g_J =75mS/cm^2 for a distance between adherent membrane and chip of 50nm. The closer the contact between neuron and chip, the higher the signal.

3.5.4 What do transistors measure?

In the theory section about field-effect transistors, 3.2, the gate is always contacted with a metal layer defining the gate-source voltage, V_{gs}. Under the operating conditions here, there is no metal on the gate oxide but electrolyte and the cell membrane. This affects the threshold voltage V_T in eq. 3.10 or the flatband voltage, V_{FB}, in eq. 3.17, because the work function of silicon is different in electrolyte than with the metal contact. Moreover, the contact potential at the Ag/AgCl-electrode and its redox potential of Ag/AgCl must be taken into account, as well as the electrical double layer at the electrolyte-oxide interface.

In the measurements of neuronal activity the gate voltage is not directly accessible but has to be calculated from the source-drain current. For this calculation, the transistor's transconductance and channel conductance must be known at the respective working point; see eq. 3.25. These quantities are determined in separate calibration measurements, where defined voltages, V_{es}, are applied to the bath by the Ag/AgCl electrode, and the resulting source-drain current is measured. V_{es} is used here, instead of V_{gs}, to emphasize that the gate is modulated from the electrolyte and the bath electrode. The conditions are different when neural activity is recorded. There, the bath electrode is set to ground and the voltage in the junction between neuron and transistor, V_J, which is generated by the neuron, modulates the source-drain current.
However, since the transconductance and channel conductance are obtained from the calibration measurements where $g_m = \partial I_{ds}/\partial V_{es}$ instead of $\partial I_{ds}/\partial V_J$ the calculated V_J is merely an 'equivalent' junction voltage. The situation is illustrated by the following equation:

$$dI_{ds} = \left(\frac{\partial I_{ds}}{\partial V_{es}}\right)_{V_{ds}} dV_J \tag{3.41}$$

Depending on the bath electrode's contact voltage and the influence of the neuron on the transistor, this calculated V_J more or less represents the 'real' junction voltage from the neuron. All V_J values of the measurements presented in the following sections are calculated values.

Most of the transistor recordings have a voltage offset, originating form the chip amplifier. These offsets have been corrected by shifting the baseline to 0V. In some graphs with more than one transient recorded from the same neuron the baseline may vary somewhat. This is caused by drifts in the electronics, the effect is of no concern.

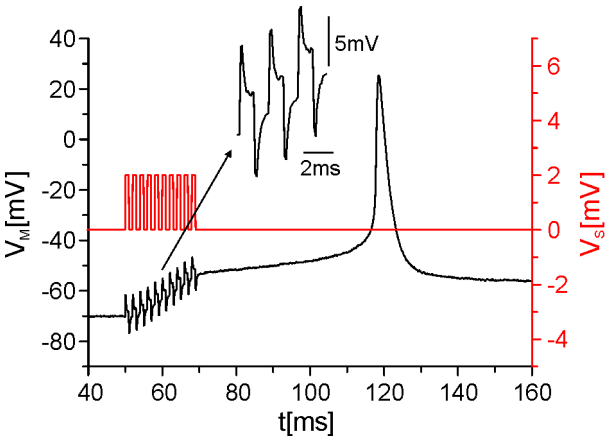


Figure 3.19: *Intracellular potential of a neuron during capacitive stimulation from the chip (black transient). 10 pulses of 2V amplitude, 1ms length and 2ms interval were applied to the stimulator, illustrated by the red curve.*

3.6 Neuron-silicon interface: Experimental results

Before studying network dynamics, the functionality of the setup and various aspects of the neuron-silicon junction are demonstrated with measurements from individual neurons cultured on the new chips for two days. The following paragraphs present data on extracellular stimulation and recording and on the long-term behavior of the cell-transistor coupling. They are followed by a discussion that compares the results obtained here with results from previous experiments.

3.6.1 Capacitive Stimulation

Voltage steps, single square wave pulses and pulse trains applied to the capacitive stimulators on a chip have shown to reliably evoke action potentials without harming nerve cells [36]. Here trains of 10 pulses, each pulse 1ms long with 2ms period, were generally used for extracellular stimulation. In the experiment the pulse height was gradually increased until neuronal activity was triggered. This approach minimized stress on the cells and prevented damage caused by excessive electroporation when the neuron-silicon coupling was strong. The maximum amplitude was limited to $\pm$5V by the amplifier electronics. It was sufficient to evoke action potentials in most cells, including those which were weakly coupled. Although some neurons can be stimulated by a single voltage step [36, 49, 129], the protocol here was preferred since it gave the same result with smaller amplitudes.

Fig. 3.19 shows a typical example for capacitive stimulation. The intracellular potential was recorded with an impaled microelectrode (black trace, the stimulus is red). During the pulse train with 2V amplitude V_M rose almost linearly. The overall increase was about 17mV, sufficient to open enough channels for a continued, yet shallower depolarization, until an action potential was fired after roughly 50ms. This delay could be reduced by more pulses or a higher amplitude. The opposite effect was observed for fewer pulses or a lower amplitude.
The inset in fig. 3.19 magnifies the intracellular voltage while the cell was stimulated. After each capacitive peak had decayed, a net change in V_M remained. Due to the low sampling frequency of only 10kHz and the filter characteristics of the glass electrode, capacitive peaks were not fully resolved, they should have been about 35mV according to subsection 3.5.2 (note that V_S^0=2V here, instead of 5V in 3.5.2). The time constant in the range of 100μs was too long compared to the estimated value $\widetilde{\tau}_J$=17μs. This can be attributed to the electrode or a poorly compensated electrophysiology amplifier.

To better understand the mechanism underlying extracellular stimulation with trains, the effect of a single pulse is analyzed in more detail. In principle, a pulse consists of two steps with equal amplitude but opposite sign; their effect on the membrane potential is described by eq. 3.31 and eq. 3.32, for A-

type coupling. If the coupling were completely capacitive, the intracellular potential would not change, because the positive and negative peaks cancel out. Two effects might account for the increase of V_M; the opening of voltage-gated ion channels or a transient electroporation of the cell membrane. The first is rather improbable, since the depolarization time is too short for opening channels with time constants in the millisecond region. Very likely, the high transmembrane voltage of up to 1.3V causes a temporal and reversible electroporation of the junction membrane where the induced voltage is highest. Charges flow through the temporary pores, similar to the situation in a leaky membrane, and depolarize the cell. A minimum voltage is required for electroporation to occur. This is confirmed experimentally, where an increase in V_M was only observed above a certain threshold in the stimulus amplitude, depending on the strength of the neuron-silicon coupling, namely g_J. Once the threshold is exceeded, the intracellular voltage can be raised either by adding more pulses or by further increasing the stimulus amplitude. The latter is not very practical because electroporation can become irreversible, destroying the neuron if the voltage is too high. No neurons have been harmed by many pulses with a low amplitude, however.

Explaining capacitive stimulation by transient electroporation in this manner is merely hypothetical. Attempts to verify the presence of induced pores by dye molecules passing through them and being detected in the cytoplasm failed [129]. It is conceivable that the molecules were too big for the pores or did not diffuse into the cleft.

3.6.2 Extracellular recording: A gallery of signals

As outlined in the theory section, various extracellular signal types arise from differences in the ion channel distribution between adherent and free membrane. Many of the signal types have been observed experimentally in previous works [49, 94, 129]. A representative selection of the extracellular signals recorded here is displayed in fig. 3.20 together with the respective intracellular voltage.

Fig. 3.20A shows the most abundant signal type, observed in more than three-quarters of all measurements. All other recordings presented here were very rare, occurring in just a few percent of cases. The most abundant signal type consists of a sharp positive peak coincident with the rising edge of the action potential, followed by a slightly broader negative peak. This biphasic behavior is typical for the purely capacitive A-type coupling, where all channels are depleted in the junction membrane, such that $\mu^i = 0$. There is a qualitative agreement with the theoretical curve in 3.17.

For a leaky membrane the transistor record is identical to the intracellular voltage, nicely demonstrated in fig. 3.20B. The amplitude is almost as large as V_M, indicating a very strong neuron-silicon coupling with a very high seal resistance. In an earlier work [49], this signal type was observed only immediately after plating neurons onto the chip, but here the measurements were done after two days *in vitro*. Furthermore, in some cases recordings were made for as long as seven hours without a notable change in transient shape, strong evidence that these neurons were healthy. In conclusion, a leaky membrane does not necessarily imply a bad or dying nerve cell.

Most of the following signals are governed by the presence of at least one active ion channel in the junction membrane. They are characterized qualitatively by comparison with the simulations in fig. 3.18.

The sharp positive peak in fig. 3.20C is caused by a full Na channel depletion and the successive, broad peak by a partial depletion of K channels or a homogeneous K channel distribution. Due to the influence of channel activity on the intracellular and junction voltage, small changes in channel distribution can have marked effect on signal shape.

For example, the transient in fig. 3.20D may be explained by a partial rather than full depletion of Na and K channels. In this special case, the small increase in Na conductivity compared to 3.20C considerably affects the second peak which is governed by K.

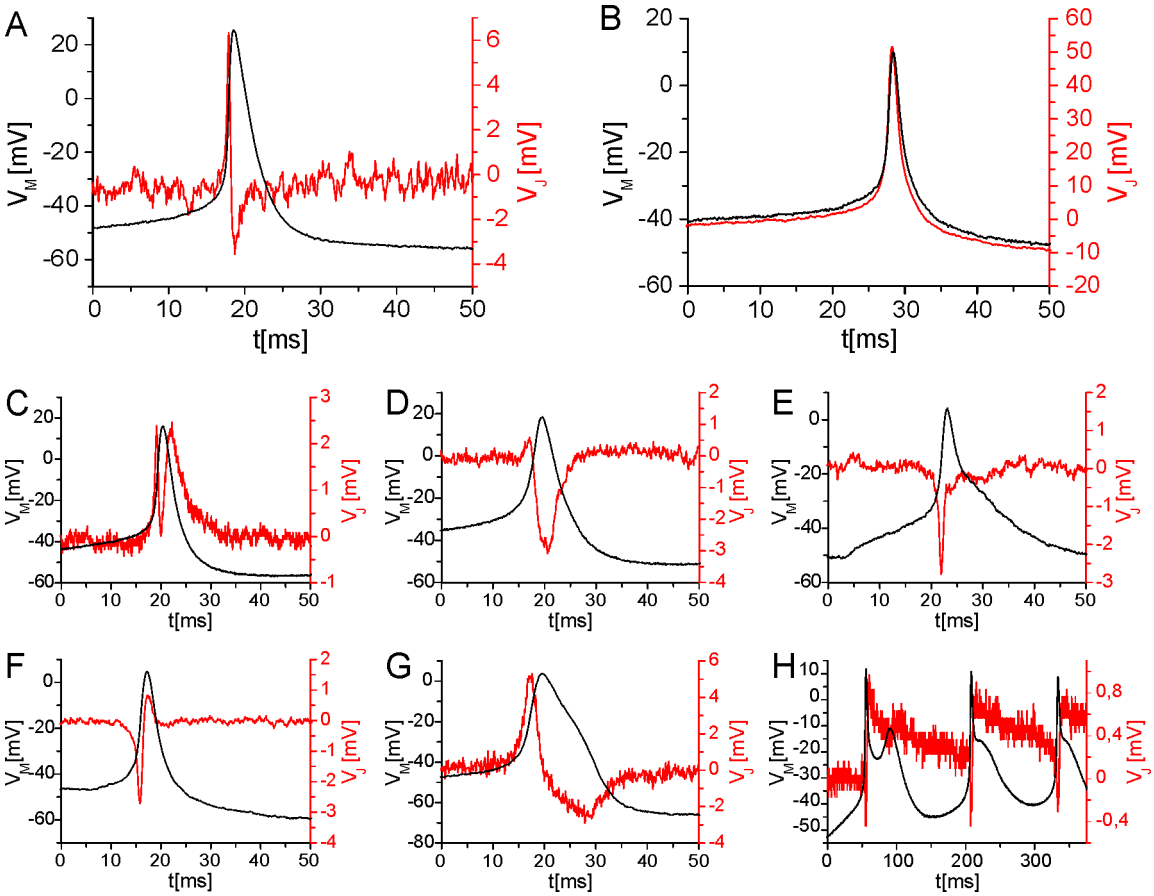


Figure 3.20: *Different extracellular signals V_J recorded with transistors (red curve). For comparison, the intracellular voltage V_M is also shown (black curve).*

If both channels are accumulated to the same extent, that is $\mu_K = \mu_{Na} \approx 2$, the monophasic curve in fig. 3.20E is observed.

With an even further increase of the potassium conductance, such that $\mu_K > \mu_{Na} \approx 2$, the second peak in 3.20F arises.

Unlike the examples above, the signal type depicted in fig. 3.20G cannot be fully explained with existing models. The first peak was certainly caused by a Na channel depletion, but the source of the second peak remains obscure. Presumably, the cell membrane contained additional ion channels, e.g. for Ca, that are not accounted for by the Hodgkin-Huxley model. This hypothesis is supported by the unusually broad action potential with a shoulder at its trailing edge.

The last transient shown in 3.20H is the most unusual one, a sharp negative peak followed by a steep increase with a slow, gradual decay thereafter. While the negative peak may arose from accumulated Na channels in the junction membrane, the slow decay at the end did not originate from the extracellular signal, since it lasted much longer than the action potential itself. The ion sensitivity, a feature of the transistor that has not been considered so far, may be responsible for this effect, refer to [2, 74, 103]. Changes in the ion concentration at the electrolyte-dielectric interface affect the surface potential of the SiO_2 and thereby the flatband voltage of the device. According to eq. 3.17, the flatband voltage has a direct influence on the source-drain current, from which the junction voltage is calculated. In the example here, ions adsorbed to the chip during the action potential and changed its surface potential. Their desorption then governed the slowly decreasing transient. For an exact theoretical description the

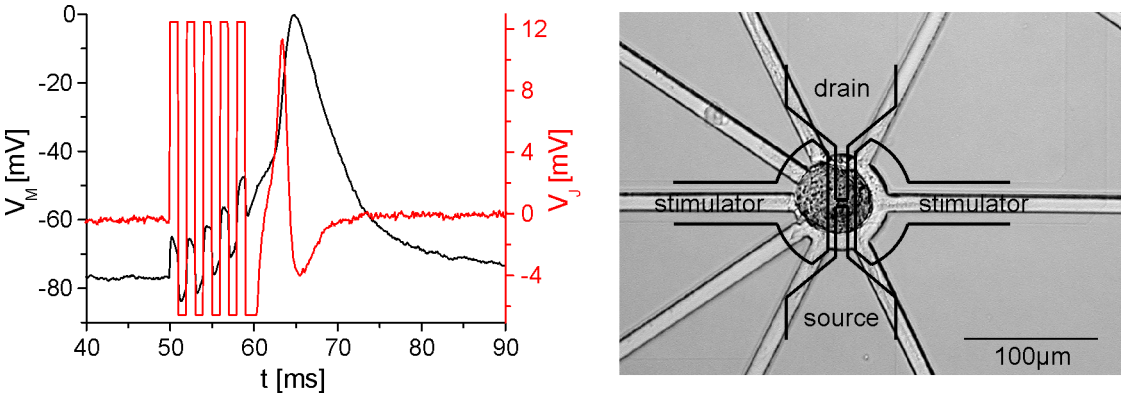


Figure 3.21: *Intracellular (black) and extracellular voltage (red) recorded from a neuron stimulated with a train of 5 pulses and 2V amplitude (not shown). The same neuron on its chip; stimulators, source and drain leads are marked.*

adsorption and desorption kinetics and the ion concentrations in the cleft must be known; this is beyond the focus of this thesis.

The list of signal types presented here is rather comprehensive for neurons from *Lymnaea stagnalis*. Most of the simulated transients in fig. 3.18 were also observed experimentally, confirming the point-contact model for the neuron-silicon interface.
Nevertheless, recordings and theory only agree qualitatively due to limitations in the Hodgkin-Huxley model, which is not adapted to snail neurons. For example, see the different timescales of measured and simulated action potentials. The mismatch between model and experiment relativizes the conclusions on channel distribution drawn for the examples above. It is possible that some of the extracellular signals result from a different channel distribution than predicted, caused by channels with a dynamics that is not accounted for by the model.

3.6.3 Bidirectional junction

So far, extracellular stimulation and recording have been addressed separately. However, studying neuronal network behavior requires full control of the activity of the network components, i.e. it must be possible to stimulate as well as record from individual nerve cells via the chip. This was achieved by combining transistor and stimulator in a bidirectional unit [101]. The right hand side of fig. 3.21 displays such a unit used here, with a neuron grown on top.
Application of a train of 5 square wave pulses, each 1ms long with 2V amplitude, to the stimulators triggered an action potential in the neuron on top, which was recorded by the FET. Both intracellular and extracellular signal are shown on the left hand diagram in fig. 3.21. This so-called 'autoloop' is the basic building block of all chip-controlled networks.

The neuron was almost centered on the gate (area between source and drain) and coverd parts of the two surrounding stimulators. In contrast to the diagrams 3.15B and 3.16, neither FET nor stimulators fill the whole area of the neuron-silicon junction, but rather share it. Since the oxide is the same everywhere on the chip, this configuration has no influence on the recorded signal, the equivalent circuit is not altered. For extracellular stimulation, the reduced stimulator area in contact with the neuron results in a smaller capacitive voltage. The effective capacitance is decreased according to $\widetilde{c}_S = c_S A_{St}/A_{JM}$, where A_{St} is the junction area taken up by the stimulators. Replacing c_S by $\widetilde{c}_S$ in eq. 3.29-3.35 yields a good approximation for the induced voltage under these conditions. Its smaller amplitude is easily compensated by a larger stimulus, but the decrease of the time constant cannot be adjusted in this way. The reduced stimulator area is still sufficient to reliably trigger action potentials from the chip, as

demonstrated by the examples in fig. 3.19 and fig. 3.21.

One side-effect of extracellular stimulation are the strong artifacts in the red curve of fig. 3.21 between 50ms and 60ms. They arise from the coupling of the stimulus to the transistor via two complementary paths. First, the stimulus charges the pn junction capacitances in the bulk semiconductor, causing a direct modulation of the source-drain current in the respective FET and also, somewhat weaker, in the adjacent transistors. Second, the stimulus couples to the electrolyte and from there back to the transistor. Artifacts are also observed in glass electrodes impaled into other neurons on the chip, due to the finite conductivity of the electrolyte and the bath electrode. In the experiment, it must be excluded that these artifacts trigger action potentials, which might mistakenly be interpreted to be of postsynaptic origin. Except for rare cases where neurons are very close to their firing threshold, neuronal activity is not affected, as revealed by many tests. In these tests, voltage pulses were applied to several stimulators in the vicinity but not to the one underneath a specific neuron, and the response of the neuron was recorded. Most cells remained quiescent during this procedure, implying that stimulus artifacts had no marked effect on them.
Overloading the amplifier during stimulation was a big issue in the early phases of its design. The problem is solved with the present version, allowing detection of action potentials fired less than 5ms after the end of the stimulus, see fig. 3.21.

3.6.4 Dynamics of action potentials and transistor signals

Nerve cells, as well as their coupling to the chip, are subject to changes over time. Some of these changes, such as the growth of neurites, are visible. But most are invisible, especially alterations in the activity and distribution of ion channels. Transistors are a sensitive tool for studying these variations without affecting the cell, as microelectrodes do. This subsection presents some observations on the dynamics of the neuron-silicon system and tries to explain them.

Neurons from *Lymnaea stagnalis* are classified electrophysiologically according to the shape of their action potentials. Two major types differ by the presence of a 'plateau' in the repolarization phase that broadens the action potentials of type II neurons, but which does not occur in type I. The plateau width is subject to an activity-dependent change, i.e. it is increased by prolonged injection of a depolarizing current into the cell that evokes a series of action potentials [122]. Ca channels account for this behavior, if they are blocked by cadmium, the plateau disappears [129]. Detailed studies with other molluscs [1] revealed a second effect which acts synergistically to the Ca influx. The delayed potassium outward current is inactivated during repetitive AP firing. This slows down repolarization, thereby broadening the action potential.

A similar effect is seen for extracellular stimulation via the chip. The three transients in the left hand diagram of fig. 3.22 were recorded at different times in an experiment during which the neuron was repeatedly stimulated with a train of 5 pulses and 2.5V (stimulus not shown). The black trace was measured shortly after the beginning, the red trace 4s later and the blue trace after 19s. Clearly, plateau width and overall length of the action potential increased considerably. As shown in the right hand diagram of fig. 3.22, this change was also detected by the transistor. The first sodium-governed peak was not altered, except for the decrease of its height, but the second peak became much broader, in accordance with the intracellular signal.

Unlike in the case above, where the shape of V_J clearly correlated with changes in V_M, the transistor signal can also vary while the action potential features remain constant, as demonstrated in fig. 3.23. This pathological, yet interesting spike train was evoked by a post-inhibitory rebound after a strong and prolonged hyperpolarization with a microelectrode. Eventually, the cell membrane was electroporated by the stimulus. This was indicated by a sudden rise in the intracellular voltage during the hyperpolar-

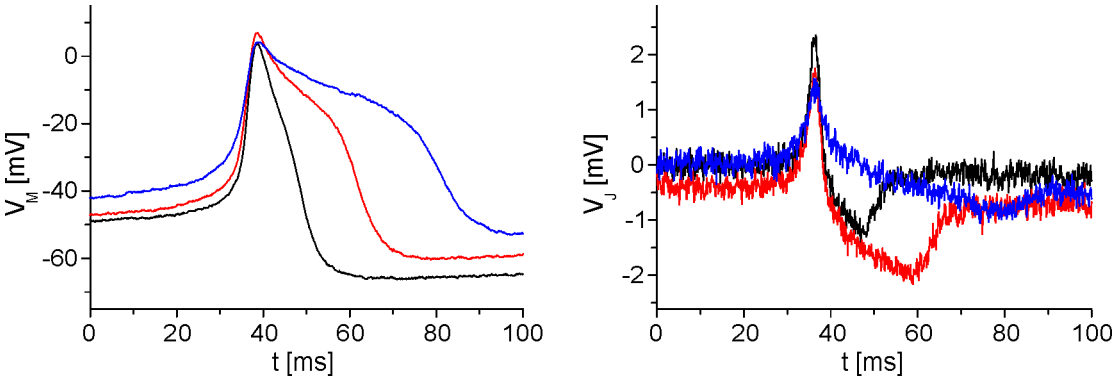


Figure 3.22: *Intracellular voltages (left) and transistor signals (right) recorded from the same neuron during repeated stimulation by the chip. The colors of the transients denote the different times; black: beginning, red: 4s later, blue: 19s after the first.*

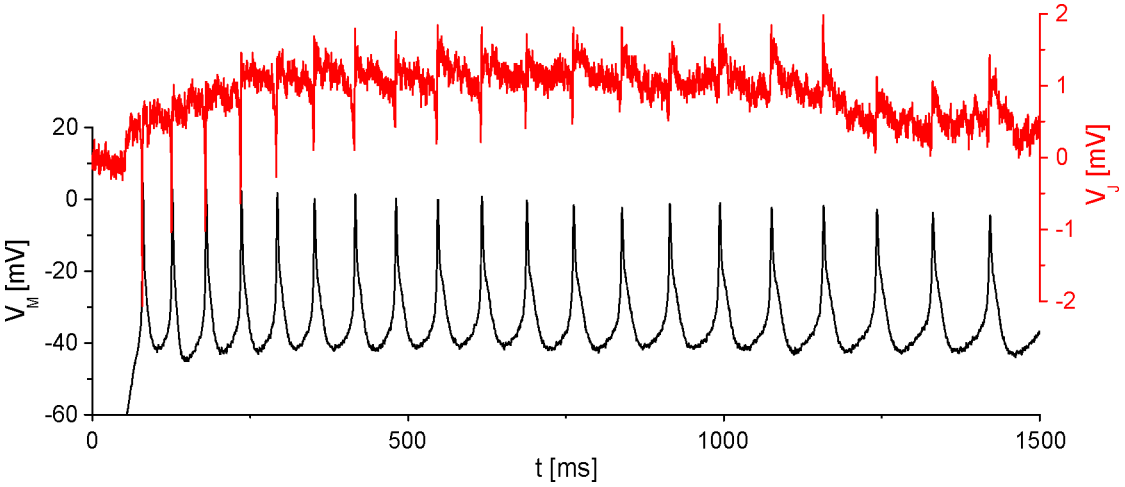


Figure 3.23: *Train of action potentials recorded with an impaled electrode (black trace) and from the chip (red trace).*

izing current application (not shown).
While the 20 action potentials were fired, the transistor signal changed from a single, sharp, negative peak, identical to that in fig. 3.20E, to a transient similar to the one in fig. 3.20C, consisting of a sharp negative and a broad positive peak. Presumably, the inactivation of ion channels during repetitive firing accounts for this effect. Whereas the signal in the early phase of the train was governed by the accumulation of Na and K channels in the junction membrane, the shape of the last action potential indicates a full depletion or inactivation of Na channels and a partial depletion or inactivation of K channels. Whether these changes in channel activity or any other cause, e.g. harm to the cell during the previous hyperpolarization, affected the cell vitality, remains unknown. In any case, no action potentials could be triggered any more after the train had ceased.

The two previous examples are very instructive, but represent rare exceptions. Generally, the signal remained stable over long periods, as shown in fig. 3.24. The black transient was recorded from a spontaneously firing neuron that was part of a large network, after a two day culture period; the red and blue traces were recorded about 7h and 11h later. Apart from the small decrease in amplitude, the curves do not change. Neuronal activity was tested once again after 21h, but at that time nothing was

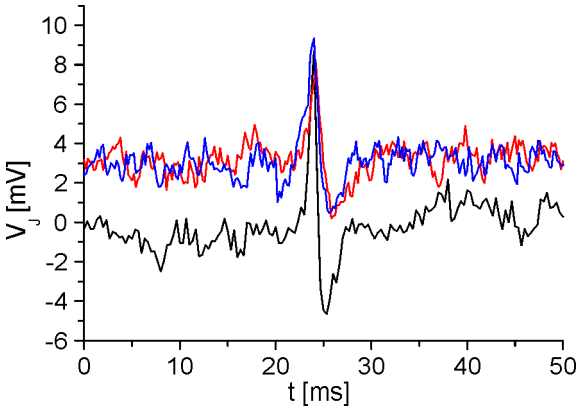


Figure 3.24: *Transistor recordings of spontaneous activity from the same neuron over an extended period. The colors of the transients denote different times; black: beginning, red: 7h later, blue: 11h after the first.*

detected, even when the cell was stimulated from the chip. Since no electrophysiological measurements with impaled electrodes were made, it remains unclear whether the neuron was dead by this point or whether the coupling to the chip was too weak.

The ion concentration in the junction changes during an action potential. Sodium flows from the electrolyte in the cleft to the cytoplasm of the neuron and potassium is released from the neuron. In principle, these temporal variations might affect the neuron-silicon coupling by increasing or decreasing the conductivity of the cleft, and therefore g_J, with its direct impact on the amplitude of V_J. Furthermore, the local reversal potential described by the Nernst equation, 2.43, is altered, influencing the respective ionic currents and thus the shape of the extracellular signal. However, these effects are negligible for most of the systems here with *Lymnaea* neurons on Si-chips. Because of the high diffusion constants of Na and K (D_{Na}=1.33·10^{-5}cm^2/s and D_K=1.96·10^{-5}cm^2/s [62]) and the small junction dimension with a diameter in the range of 30μm, the ion concentration in the cleft is balanced with that of the medium in the culture chamber within approximately 100ms; this is usually before the next action potential is fired.
Only when action potentials are fired with a high frequency, e.g. as in the example in fig. 3.23, ions may deplete or accumulate in the cleft affecting the transistor recordings.

3.6.5 Discussion

In the second part of this thesis, a new transistor chip was designed and processed and the infrastructure, such as the setup, amplifier and software, was built and programmed. Compared to the standard devices in the department, this chip possessed two novel features. The buried channel design allowed transistors without local insulation oxide, resulting in a totally flat surface. Also, the topographic structures with pits for immobilizing neurons have never been used before.
As demonstrated by the examples above, extracellular stimulation and recording behaved as expected and were well explained by existing theories. However, there were small, yet noticeable differences with respect to the measurements obtained from the standard devices like *Lymnos* [49] or the chips in [129].

In many cases a relatively low amplitude of about 2V was sufficient for the **extracellular stimulation** of neurons. This is in contrast to the reports in [49, 129], where much stronger stimuli were needed, usually pulse trains with 5V amplitude.
The pits do not account for this effect, because they only add a series resistance to the bath, which is negligible compared to the junction resistance.
Very likely the new amplifier is responsible for the effect. The theoretical considerations on V_J for the extracellular stimulation all assume a voltage step with infinite edge steepness. In reality, the voltage

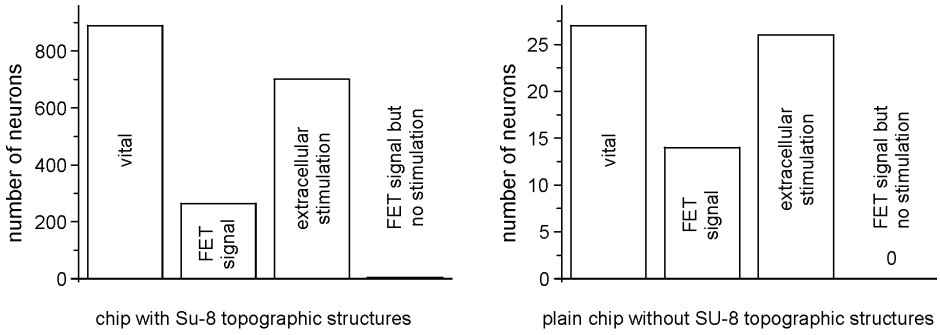


Figure 3.25: *Statistics of the neuron-silicon coupling for devices with and without topographic structures.*

increases with a finite velocity, the slew rate, governed by the electronics and the load. Since V_J decays exponentially according to eq. 3.31 or eq. 3.34, the maximum voltage in the cleft not only depends on the stimulus amplitude, but to a much greater extent on the speed with which the stimulation spots are charged. Tests revealed over a ten-fold increase in slew rate and a ten times larger voltage in the bath with the new amplifier compared to the setup in [129], clearly indicating that the electronics and not the chip is the cause for the smaller amplitude required to trigger action potentials extracellularly.

Comparing the transistor measurements in [129] and those presented here shows some interesting discrepancies. Although many similar signals were detected by both systems, A-type coupling prevailed with the chips here. This type of coupling was observed in approximately 50%-75% of all neuron-silicon couplings, whereas 75% of the recordings in [129] were governed by K channel accumulation in the adherent membrane. This difference in the channel distribution on both devices may either arise from the lack of the local oxide (LOCOS) or the SU-8 topographic structures.
Effects of the topographic structures were studied with a plain buried channel chip that had no SU-8 on top. Indeed, the probability for a given signal type to occur was different with this device. A-type coupling was observed in only 4 out of 14 functional neuron-silicon interfaces, approximately 30%. Other signals such as those shown in diagrams C, E and F of fig. 3.20 were more common than with the SU-8 chips. The mechanism behind this behavior remains unknown. It is possible that waste products accumulate in the pits, affecting cell metabolism and ion channel distribution.
The effect of surface heterogeneities on the signal characteristics could not be tested due to a lack of buried channel chips with local oxide.

One of the major issues when designing chip-controlled neural networks is the percentage of cells establishing a functional, bidirectional neuron-silicon interface. The actual shape of the transistor signal is of minor interest in that respect, what matters is that something is detected at all.
The left hand diagram in fig. 3.25 shows the statistics for extracellular stimulation and recording on chips with SU-8 topographic structures. To check whether neurons that show no activity in the transistor beneath were alive or not, additional electrophysiological measurements were made with microelectrodes. Of 1053 impaled neurons, 889 were vital, i.e. they fired action potentials. In 79% of these (701), action potentials could be evoked from the chip, whereas only 30% (264) showed signals in the transistors. A successful extracellular recording nearly always correlated with a successful stimulation, too. Only 1% (5) of the successfully contacted neurons could be recorded, but not stimulated by the chip. This is in contrast to observations in [49], reporting success rates of 87% for extracellular measurements and 52% for stimulation, with 39% of the neurons coupling bidirectionally (n=67). The relatively low stimulation yield in that study is certainly due to the low slew rate of the electronics, as discussed above (the setup used in [49] and [129] was the same). More striking, though, is the high

percentage of transistor recordings in those studies. This cannot be ascribed to the electronics. Since the noise level in both chips is in a similar range, only differences in their design can account for the difference in successful transistor recordings. The impact of the pits was tested on chips without SU-8. Of 27 vital nerve cells cultured on these devices, 52% could be monitored by the transistors and action potentials were triggered extracellularly in 96%, see the right hand diagram in fig. 3.25. The drastic increase in coupling efficiency unequivocally indicates that topographic structures have a negative influence on the neuron-silicon interface.
According to the theory section 3.5, two requirements are essential for a successful transistor recording; the junction resistance between neuron and chip must be high and the ion channels must be distributed heterogeneously between adherent and free membrane. Both aspects might be affected by the pits.
Neurons can grow up the walls, causing a large gap to the surface with a high conductivity, that results in a junction voltage V_J too low for detection. The high yield of extracellular stimulation, even with the SU-8 structures, contradicts this scenario; if the gap was too large, no action potentials could be triggered from the chip, either. Given our current knowledge, the low percentage of successful transistor recordings from cells in pits would seem to arise from an increased probability of a homogeneous channel distribution.

Despite the improved coupling when the SU-8 is omitted, the overall yield here was still considerably lower than the yield reported in [49]. Theoretically, surface heterogeneities like LOCOS might account for that. A more realistic explanation, however, are differences in the culture period. The longer snail neurons are on the chip, the smaller the chance of a successful transistor recording. All cells in this study were measured after 2div to 3div. Presumably experiments were performed sooner in [49] (no time is given there).
The relation between culture time and coupling efficiency of *Lymnaea* neurons is another poorly understood aspect of the neuron-silicon interface. Either the distance between cell and surface increases, or ion channels rearrange in the membrane. In this context it must be noted that the cell culture protocol is not optimized for long culture periods. Regular medium changes would be required, which might also positively affect neuron-silicon coupling.

In conclusion, the new buried channel transistors with SU-8 topographic structures provide non-invasive control of the activity of individual neurons. Compared to plain chips, the pits affect the channel distribution in the cells, altering the characteristics of the measured signals and reducing the overall number of functional neuron-silicon interfaces. The latter issue is of great concern for designing chip-controlled networks, because the more neurons couple successfully, the higher the yield for nets.

Chapter 4

Defined networks on chips

The two previous chapters extensively described the techniques for controlling neurite outgrowth and extracellular recording and stimulation. Here, both SU-8 topographic structures and field-effect transistors were combined to realize chip-controlled neural networks with defined synaptic connection patterns.
After briefly summarizing the theory of the neuron-silicon interface and signal transfer along neurites and across synapses, three examples of increasing complexity are presented. A detailed discussion, with focus on the yield of the individual steps involved, concludes the chapter.

4.1 Theory part IV: Chip-controlled networks

Neurons that are bidirectionally interfaced to transistors and stimulators represent the fundamental unit of chip-controlled neural networks. On the biological side they are connected by synapses, which have purely electric characteristics in the case of A-cluster neurons from *Lymnaea stagnalis*. Fig. 4.1 depicts the equivalent circuit of the simplest system, the silicon-neuron-neuron-silicon loop. It is a combination of the circuits in fig. 3.15B and fig. 3.16 for stimulation and recording and fig. 2.10 for the synaptic connection.

Here, the fundamental theoretical aspects are reviewed, following the signal path from the stimulation of the left neuron, via the synapse, to its recording by the transistor underneath the right neuron. The various aspects of the neuron-silicon interface, signal transfer in networks and the Hodgkin-Huxley model for action potential generation are outlined in detail in 2.4.2, 2.4.3 and 3.5.

A train of pulses with amplitude $V_{S,A}$ applied to the stimulator beneath the left neuron, A, couples capacitively to the junction between cell and chip and modulates $V_{J,A}$. Due to the low oxide capacitance, the time constants of the induced transients are too small to open voltage-gated ion channels; yet their amplitude is high enough for a transient electroporation of the cell membrane in the junction. Inward sodium currents depolarize the neuron and trigger an action potential, which modulates $V_{J,A}$ in return and is detected by the transistor.
The field-effect transistors are represented by their terminals source S, drain D and bulk B, to which the operating voltages are applied. The gate voltage at the FET is identical to the junction voltage in this configuration; any change in V_J therefore affects the source-drain current in the transistor. Amplitude and shape of the extracellular transient are governed by the conductance in the cleft and the ion channel distribution between the free cell membrane and the membrane in the junction. To check cell vitality in cases where no extracellular signal is detected, microelectrodes are additionally impaled, they record the intracellular voltage V_M.
In the neuronal network the action potential travels along the neurites, passes the synapse and depolarizes the right neuron, B. If the synapse is strong enough, a postsynaptic action potential is fired and

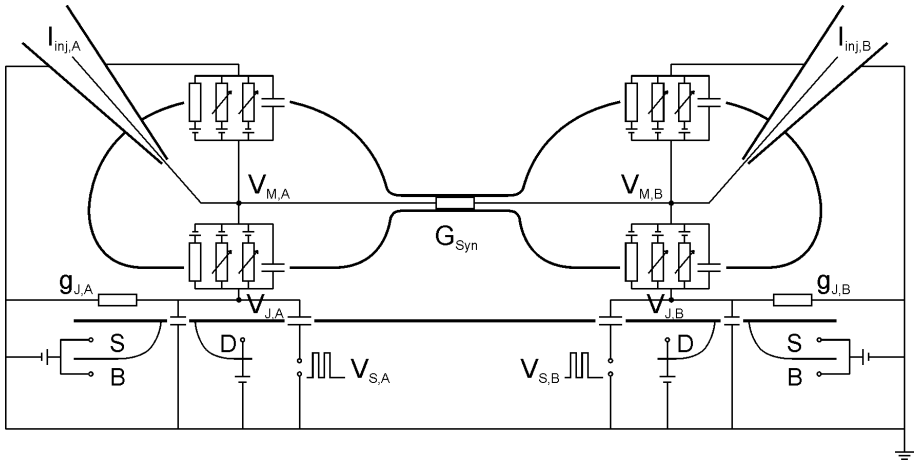


Figure 4.1: *Equivalent circuit of the simplest chip-controlled network, two neurons, A and B, connected by a single synapse. Each neuron couples to a transistor and a stimulator, which are represented by a capacitor.*

recorded by the respective transistor.
Because neurites from *Lymnaea* neurons are electrotonically very compact, they hardly affect the propagating signal and are therefore neglected in the theoretical description of network dynamics. The isopotential model relies on this approximation; only the synapse is taken into account by a conductivity G_{syn}. Unlike chemical synapses, the electrical synapses between A-cluster neurons from *Lymnaea stagnalis* do not have any rectifying characteristics and AP's can pass in both directions. Thus, the direction of signal transfer is reversible in the example above, with the right neuron being presynaptic and the left postsynaptic. There are no restrictions from the chip, since both cells couple bidirectionally to stimulator and transistor.

More complex systems are easily obtained by adding further neurons. The specific design with defined synaptic connections may in the future allow the control of the network dynamics and eventually to realize Hopfield and other networks of fundamental theoretical interest.

4.2 Results

Building on the initial work by M. Jenkner [49], G. Zeck grew several two-neuron networks that could be completely controlled from silicon chips [129]. The examples below extend this approach towards networks with defined geometry and with more than just two nerve cells.

4.2.1 Basic silicon-neuron-neuron-silicon loop

The micrograph in fig. 4.2A, taken after 2 days *in vitro*, depicts an example of the simplest chip-controlled network with defined connection pattern, two neurons coupled by a single neurite. It is the biological implementation of the theoretical model described above. To increase the visibility, the contrast of somata and processes was selectively enhanced with an image processor.

The groove nicely guided the growth of the connecting neurite, but several other neurites left the topographic structures right at the cell bodies. Neuron 1 was displaced from the center of the pit, where the transistor is located. Still, its activity could be controlled extracellularly because the broad, flat neurite at the bottom covered FET and stimulators quite well.

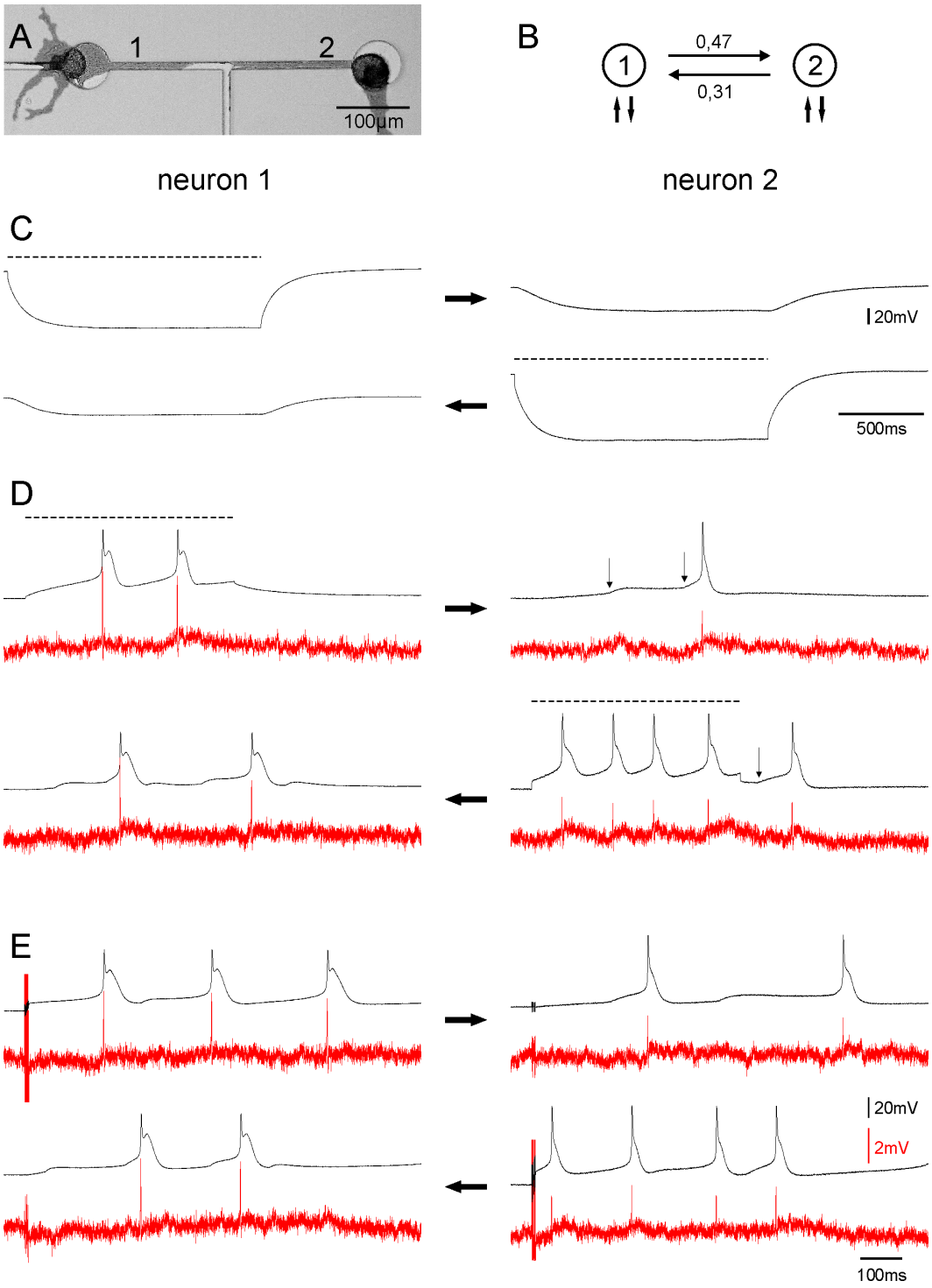


Figure 4.2: *A: Micrograph of a simple two-neuron network with neurites grown in the connecting groove. In the middle of the groove, the left neurite grew very slim and along the upper sidewall. B: Synaptic connection pattern, the numbers denote the coupling coefficient for each direction of signal transfer. Arrows pointing up and down beneath the cells symbolize bidirectional coupling. C to E: Electrophysiological (black curves) and transistor (red curves) recordings of network activity, the horizontal arrows indicate the direction of signal transfer from neuron 1 to neuron 2 and vice versa. Traces in the*

left column belong to neuron 1 and in the right column to neuron 2. C: Injection of a hyperpolarizing current with -0.4nA into neuron 1 (top row) and 2 (bottom row). The injection duration is given by the dashed line. D: Injection of a depolarizing current with 0.1nA into 1 (top row) and 2 (bottom row). Intracellular and transistor measurements are shown. The small vertical arrows indicate when peaks occur in the diagrams on the left hand side. E: Intracellular and transistor recordings after stimulating neuron 1 (top row) and 2 (bottom row) from the chip. Scale bars in E also apply to D.

The arrows underneath the circles in the schematic drawing 4.2B symbolize the bidirectional interface between both cells and the chip, the upward arrow representing stimulation the downward recording. The numbers denote the synaptic coupling coefficients, the horizontal arrows indicate the direction of signal transfer. Furthermore, the synaptic conductivity was calculated, G_{syn}=2.6nS. This very high near the upper limit of the distribution shown in fig. 2.22.

Since the neuron-silicon coupling is not always as reliable as in this example, neurons were additionally impaled with microelectrodes. Fig. 4.2C displays measurements in the voltage range where the cell membrane is passive, i.e. neurons were hyperpolarized. The coupling coefficients and the synaptic conductivity above were determined from these data. Injecting -0.4nA into neuron 1 hyperpolarized its membrane potential by -66mV and the membrane potential of neuron 2 by -30mV; see the top row in fig. 4.2C. The dashed line in the diagram indicates the time during which current was injected. Reversing the direction of signal transfer with the same current applied to neuron 2 yielded a similar result, displayed in the bottom row in 4.2C.
The observed behavior is unequivocal proof that an electrical synapse was established. Its formation was expected with A-cluster neurons.

If a depolarizing current with 0.1nA amplitude was injected into neuron 1 via the microelectrode, it fired two action potentials. They passed along the neurite and across the synapse and depolarized neuron 2, which fired a postsynaptic action potential after integrating the incoming signal. The small arrows in the top right diagram 4.2D mark the timing of the presynaptic peaks, which nicely coincided with onset of the postsynaptic depolarization. This demonstrates that the electrotonically compact neurites of *Lymnaea stagnalis* hardly delay signal propagation. Subsection 2.4.2 discusses this issue in detail.
The red curves are the extracellular recordings from the transistors. Action potentials were nicely detected with a signal-to-noise ratio of about 5:1 for neuron 1 and 3:1 for neuron 2. In both cases the signal shape was governed by the depletion of Na and K channels in the junction membrane of the cells, the so-called A-type coupling described in 3.5.3.
Stimulating neuron 2 in the same way yielded a similar result, as shown in the bottom row. During current injection neuron 2 fired 4 action potentials that depolarized cell 1, triggering 2 postsynaptic APs. The 5th peak in neuron 2 was evoked by the second peak in neuron 1, the arrow marks the timing between presynaptic AP and the beginning of postsynaptic depolarization. In this rather unique example, both cells were pre- and postsynaptic at the same time, with the signal travelling back and forth between them. Again, neuronal activity was also recorded by the transistors. Signal shape and amplitude did not change compared to the top row.

Controlling network activity entirely from the chip requires not only transistor recording but also the excitation of neuronal activity. Fig. 4.2E demonstrates the successful implementation of both requirements in a functional hybrid system. A series of voltage pulses applied to the stimulators in pit 1 evoked a train of action potentials in the neuron above that also triggered postsynaptic activity in neuron 2, see the top row. All peaks were reliably detected by the respective transistors. Since the first action potential was fired with more than 100ms delay, the stimulation artifacts did not interfere with its recording. This issue is addressed in 3.6.3.
Neuron 2 could also be stimulated from the chip as illustrated in the bottom row. Four presynaptic and

2 postsynaptic action potentials were fired and detected by the FETs.
Extracellular stimuli consisted of 5 square wave pulses, each 1ms long, with 1ms interpulse interval. The amplitude applied to neuron 1 was 2V and to neuron 2 2.5V.

Theoretically, extracellular stimulation could also directly affect postsynaptic neurons by coupling to the bath and causing artifacts in the chip and microelectrodes. To assess their effects on the network here, 10 pulses with 4V amplitude were applied to 4 stimulators in its vicinity. Except for the artifacts, the membrane potential did not change in either cell, and, more importantly, no action potentials were fired (data not shown). In consequence, the observed postsynaptic activity was solely due to the input from the presynaptic neuron.

The example above demonstrates the successful implementation of a silicon-neuron-neuron-silicon loop with a defined synaptic connection between the nerve cells. This was achieved by combining the technologies presented in the previous chapters, transistor chips and SU-8 topographic structures.
All requirements were fully met; both neurons were bidirectionally interfaced to the chip with stimulation and recording, the connecting neurite was nicely guided by the groove and the synapse was strong enough to evoke postsynaptic activity.

4.2.2 Partially controlled three-neuron network

Compared to the previous example, the linear arrangement of 3 neurons shown in fig. 4.3A is the next, more complex system. Although barely visible, many neurites grew into the grooves emerging from the pits. Despite their large number, a thorough inspection of the entire micrograph (only a cutout is depicted here) revealed that the neurons were solely connected by the neurites in the horizontal grooves between pits 1, 2 and 3.

Fig. 4.3B illustrates the synaptic connection pattern of the network. Again, only electrical synapses have been established. Unfortunately, the control from the chip was rather unsatisfactory. While neuron 1 could only be stimulated extracellularly, as indicated by the arrow pointing upward, neuron 2 could only be recorded with the transistor; see the arrow pointing down. Neuron 3 did not couple to the chip at all. Network activity was therefore controlled with impaled microelectrodes.

Injecting a hyperpolarizing current with -0.2nA amplitude into neuron 2 also decreased the membrane potential in neurons 1 and 3, demonstrating that electrical synapses existed between both subsystems 1 and 2, and 2 and 3, fig. 4.3C.

Notwithstanding the deficits in the neuron-silicon interface, the network possessed a very interesting feature, illustrated by the graphs in fig. 4.3D. Neuron 1 fired 3 APs upon depolarization with 0.15nA, see the left diagram in the top row. The dashed line marks the timing of current injection. Signals propagated to neuron 2 and from there to neuron 3, depolarizing both, yet they remained quiescent.
Stimulating neuron 3 with 0.1nA yielded a similar situation as shown in the bottom row. As before, the two postsynaptic cells were depolarized, but did not fire action potentials. However, if the same currents were applied to 1 and 3 simultaneously, neuron 2 also fired an AP which was recorded by the transistor; middle row.
The extracellular signal resembles the one in diagram 3.20C, which is governed by a full depletion of Na channels and a partial depletion of K channels in the junction membrane. But there is one big difference: the transistor recording here is much broader than the intracellular peak. This is probably due to the ion sensitivity of the transistors discussed in subsection 3.6.2. The shape of the action potential itself is rather unusual, with the two peaks being so close to each other. However, the neuron was vital during the entire experiment, which took approximately 30min, and its coupling to the chip was very reliable.

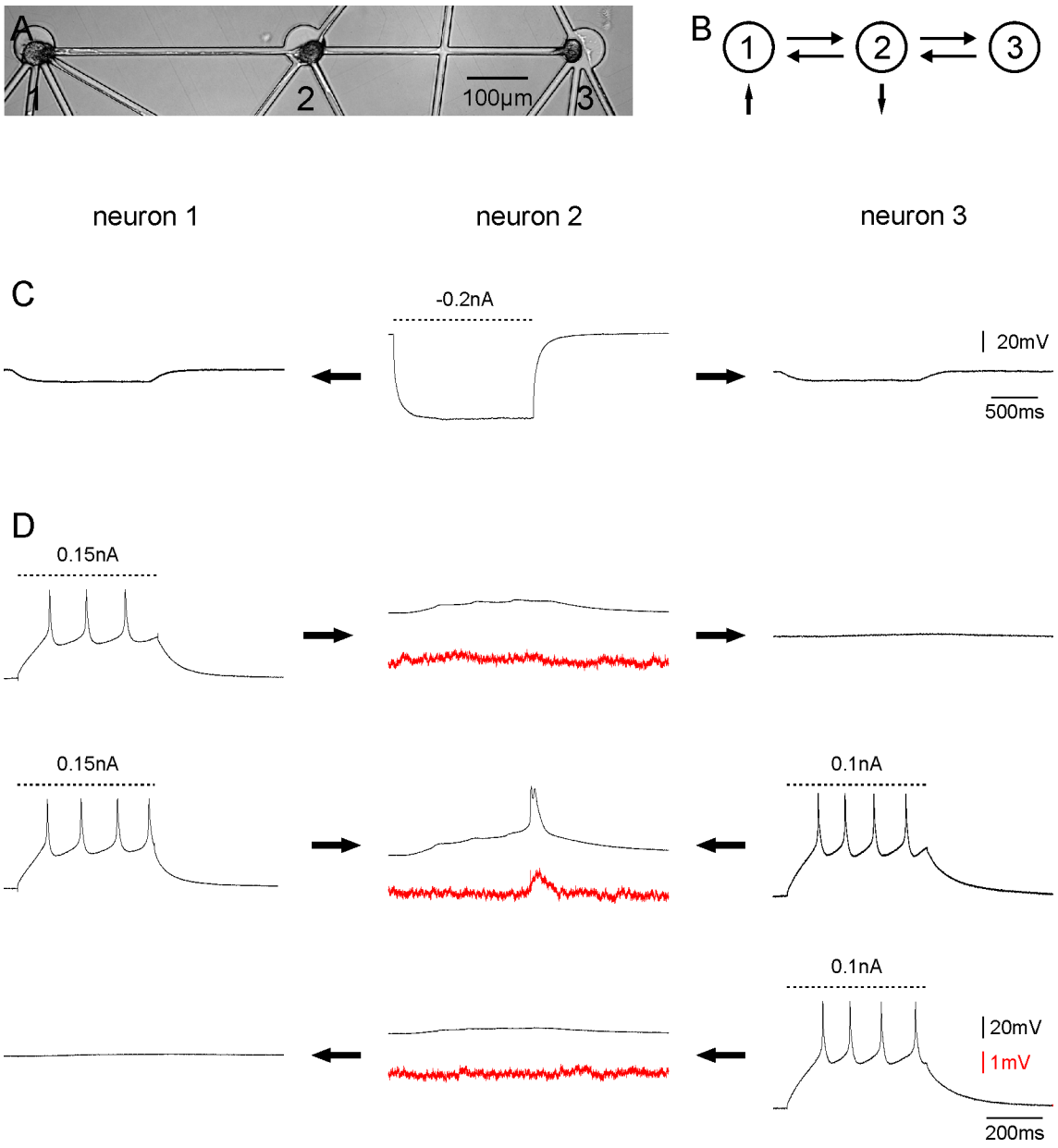


Figure 4.3: *A: 3 neurons arranged in a line after 2 div. B: Synaptic connection pattern and neuron-silicon interfacing. 1 could be stimulated from the chip (arrow pointing up), 2 could be recorded (arrow pointing down) and 3 did not couple at all. C and D: Measurements of network activity; black traces denote intracellular signals, red traces are the transistor recordings. The left column depicts the transients from neuron 1, the middle column from neuron 2 and the right column from neuron 3. Dotted lines indicate when current was injected into the respective cell and the numbers above denote its amplitude. The black horizontal arrows show the direction of signal transfer.*

The experiment above was successfully repeated several times. In its function, the network is the biological equivalent to an electronic 'and' circuit, where the output, in this case neuron 2, is only 'true' if both inputs, neuron 1 and 3, are simultaneously 'true', i.e. firing action potentials at the same time. It is a beautiful example of the *in vitro* implementation of the integrate-and-fire model, one of the fundamental concepts of neuroscience.

Since neuron 1 could also be triggered from the chip, current injection was replaced by an extracellular stimulus and the previous experiment was repeated. All attempts failed to reproduce the ‘and’ with one input (neuron 1) controlled from the chip and the other (neuron 3) from the microelectrode.

The successful implementation of such a system, among many other factors, depends on the precise control of the stimuli applied to the input neurons. If they are too weak the inputs are not sufficient for evoking activity in the output neuron, if they are too strong, stimulating a single input neuron might already trigger action potentials at the output.

In consequence, the extracellular stimulation from the chip is not as defined as current injection with impaled microelectrodes. This conclusion is confirmed by an almost identical experiment with another three-neuron network, where an ‘and’ was realized with the microelectrodes but not with the chip (data not shown). The reason for this reduced precision lies in the mechanism behind extracellular stimulation. Length and extent of the transient electroporation of the cell membrane induced by the extracellular stimulus are far less controllable than current injection with microelectrodes.

4.2.3 Defined network of four neurons

Complex systems such as perceptrons and feed-forward networks are considerably larger than the examples presented so far. Comprising at least 7 vital neurons, the network in fig. 4.4 may be a prototype of such systems. Nearly all nerve cells were connected by neurites in the grooves. Topographic guidance was almost perfect, only two short processes left the structure directly at the somata of neurons 2 and 3. After the experiments, several cells were stained with Lucifer Yellow (the staining protocol is outlined in appendix A), making them more visible in the pits and grooves. The bottom picture displays the fluorescence micrograph.

At the time the network was grown, which was at an early stage of the experiments with chips, only a preliminary version of the amplifier existed. Instead of the 16 channels of the final version, it provided just 4 channels for transistor recording. For this reason, not the entire network, but only subsystems could be controlled from the chip.
Fig. 4.5A depicts the extracellular transients in neurons 1-4 recorded after connecting the chip to the amplifier. Cells were not impaled with microelectrodes at this point. Individual action potentials were nicely detected in all respective transistors, with a signal-to-noise ratio up to 8:1.

Unlike the previous examples, chip calibration was not checked by modulating the bath voltage after the experiments. In consequence, the signal amplitude might be incorrect, reasons for this are discussed in 3.4.4. The strong variations in the noise of the different transistors might arise from this. However, for the experiments here, the actual signal amplitude is of minor concern, what matters is that the signals can be clearly discriminated from transistor noise. This requirement is reliably fulfilled.

Spontaneous network activity was highly correlated, with neuron 4 playing the role of a pacemaker. It triggered the action potentials in the other neurons, which fired in the following order; 3, 1, and 2. The activity pattern shown in fig. 4.5A is maintained over an extended period, as illustrated by the interspike interval plot in diagram C. Each bar represents a single action potential. The grey box highlights the pattern obtained from the transients in diagram A. Due to limitations in the software, activity was not recorded continuously, but only for predefined intervals. Horizontal lines at the bottom mark periods where no measurements were made because the computer was busy saving the acquired data.
The high temporal correlation between neuronal spikes is a strong indicator for the existence of synaptic connections. To study them in more detail, neurons 1, 2 and 3 were impaled with microelectrodes; spontaneous activity considerably changed thereafter. A hyperpolarizing current applied to one neuron also decreased the membrane potential of the others, revealing that electrical synapses had formed (data not shown). These experiments, together with the micrographs in 4.4, enabled the reconstruction of the

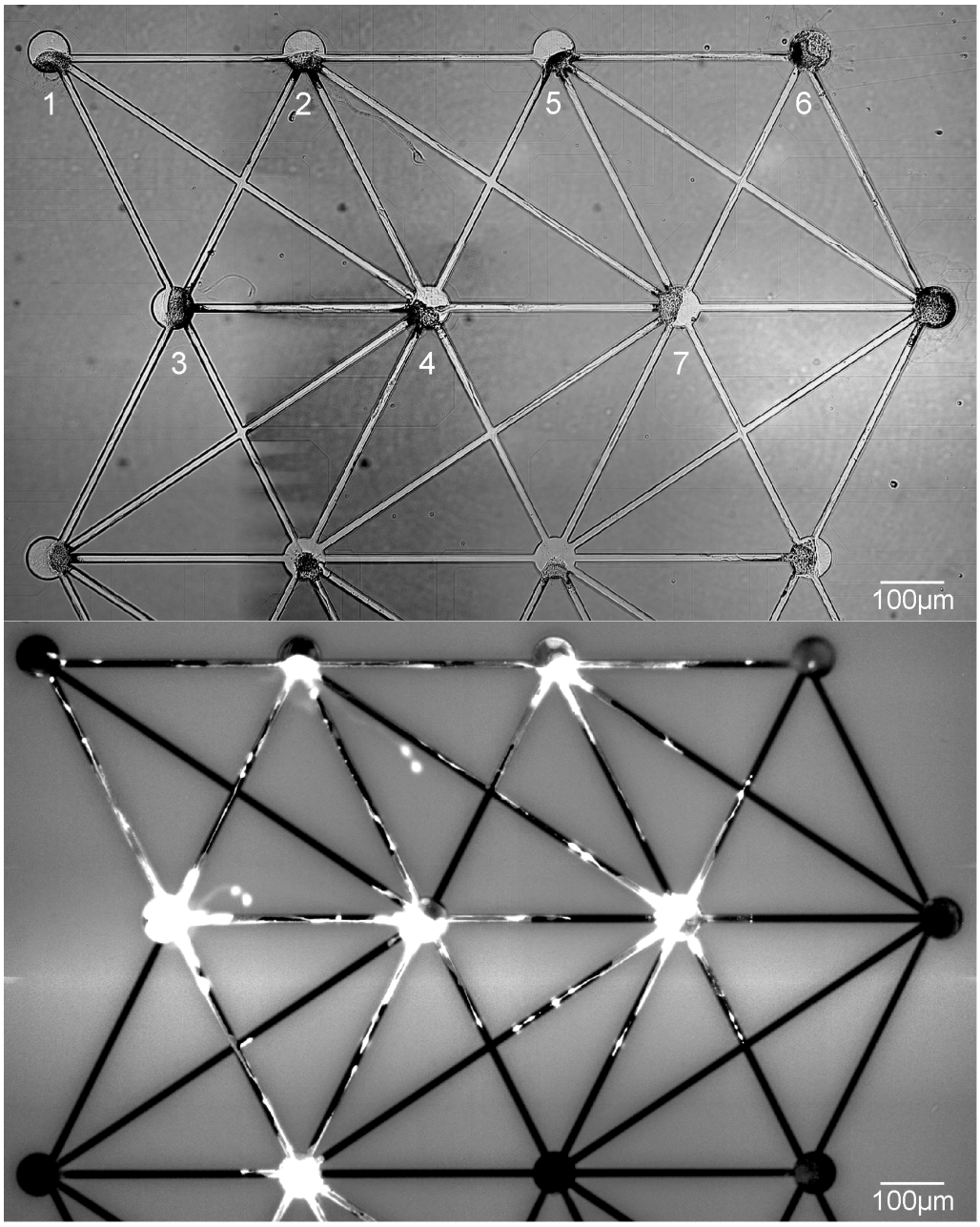


Figure 4.4: *Top: Brightfield micrograph of a large defined neuronal network. Bottom: Fluorescence micrograph of the same net, several neurons were stained with Lucifer Yellow.*

synaptic connection pattern in diagram 4.5B.
Because of its complexity, with several signaling paths between one cell and another, the numbers denote only the upper limit of the synaptic coupling coefficients for the direction of signal transfer indicated by the arrows. Subsection 2.4.2 outlines the theoretical aspects of the issue. Without any intracellular recordings available from neuron 4, its synaptic connection to 2 and 3 is deduced from their correlated firing. The dashed arrows symbolize this lack of precise information.
Every neuron coupled bidirectionally to the chip, as indicated by the arrows pointing up and down beneath the cells.

Diagrams A-D in fig. 4.6 give examples of the network response to the capacitive stimulation of indi-

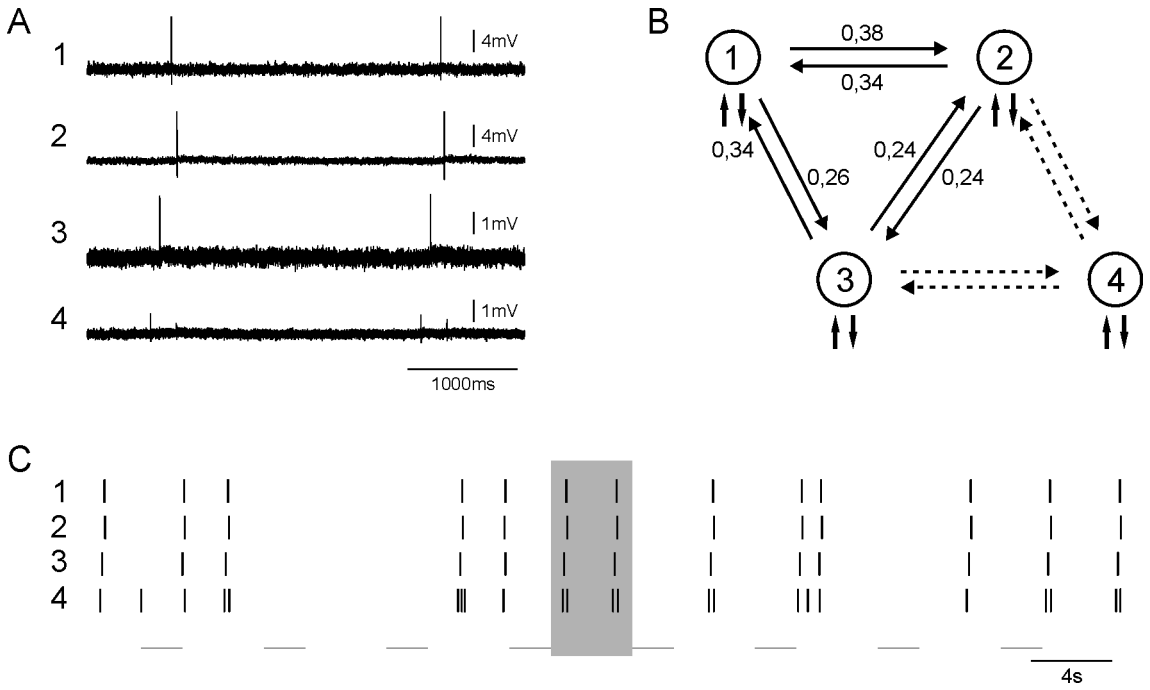


Figure 4.5: *A: Transistor recordings of spontaneous network activity in neurons 1-4. B: Schematic diagram illustrating the synaptic connection pattern between individual neurons. The numbers denote the coupling coefficients for the direction of signal transfer indicated by the arrows. Dashed lines mark synapses that were not tested by measurements with impaled microelectrodes. Arrows pointing up and down beneath the cells symbolize that all neurons coupled bidirectionally to the chip. C: Interspike interval plot; each bar represents a single action potential. The horizontal lines at the bottom indicate periods where no signals could be recorded due to restrictions with the setup. The firing pattern in the grey box was obtained by digitizing the recordings in A.*

vidual neurons. Black curves are the intracellular voltages, red ones are the transistor signals. Number and amplitude of the square wave pulses applied as stimuli are given at the respective transients. Each pulse is 1ms long, with 1ms intervals in between. The scale bars in diagram D are the same for all traces, exceptions are marked.

Immediately after its extracellular stimulation, neuron 1 fired a single action potential. The time scale of the inset at the top of diagram A is expanded by a factor of 5. It shows that the action potential can be discriminated from stimulus artifacts very well, in both the microelectrode and the transistor recording. Neuron 2 was hardly affected by the activity in the other neurons and remained quiescent. Expanding the intracellular transient of neuron 3 by a factor of 5 in amplitude (see the inset) depicts a small depolarization resulting from the presynaptic input of 1. The subsequent increase of the membrane voltage was very slow, so that the action potential was presumably triggered by the peak in transistor 4.

Diagram B displays the transients evoked by stimulating cell 2. The neuron fired an action potential with approximately 180ms delay. More than 50ms before the AP in neuron 2, a spike was recorded by transistor 4. Very likely, neuron 4 was spontaneously active or received additional input from other cells that were not monitored. The intracellular transients reveal a clear correlation between a rising membrane potential in 1 and the action potential fired by 2 as well as the depolarization of 3 by the spike in 4.

Five square wave pulses applied to the stimulator beneath neuron 3 evoked an AP, which triggered postsynaptic activity in 4. 1 and 2 were only weakly depolarized and remained quiescent; see diagram C.

A similar situation was observed when neuron 4 was stimulated from the chip; depicted in diagram 4.6D. Again, 4 and 3 were active and 1 and 2 were not. Whether the second AP in 4 was retriggered

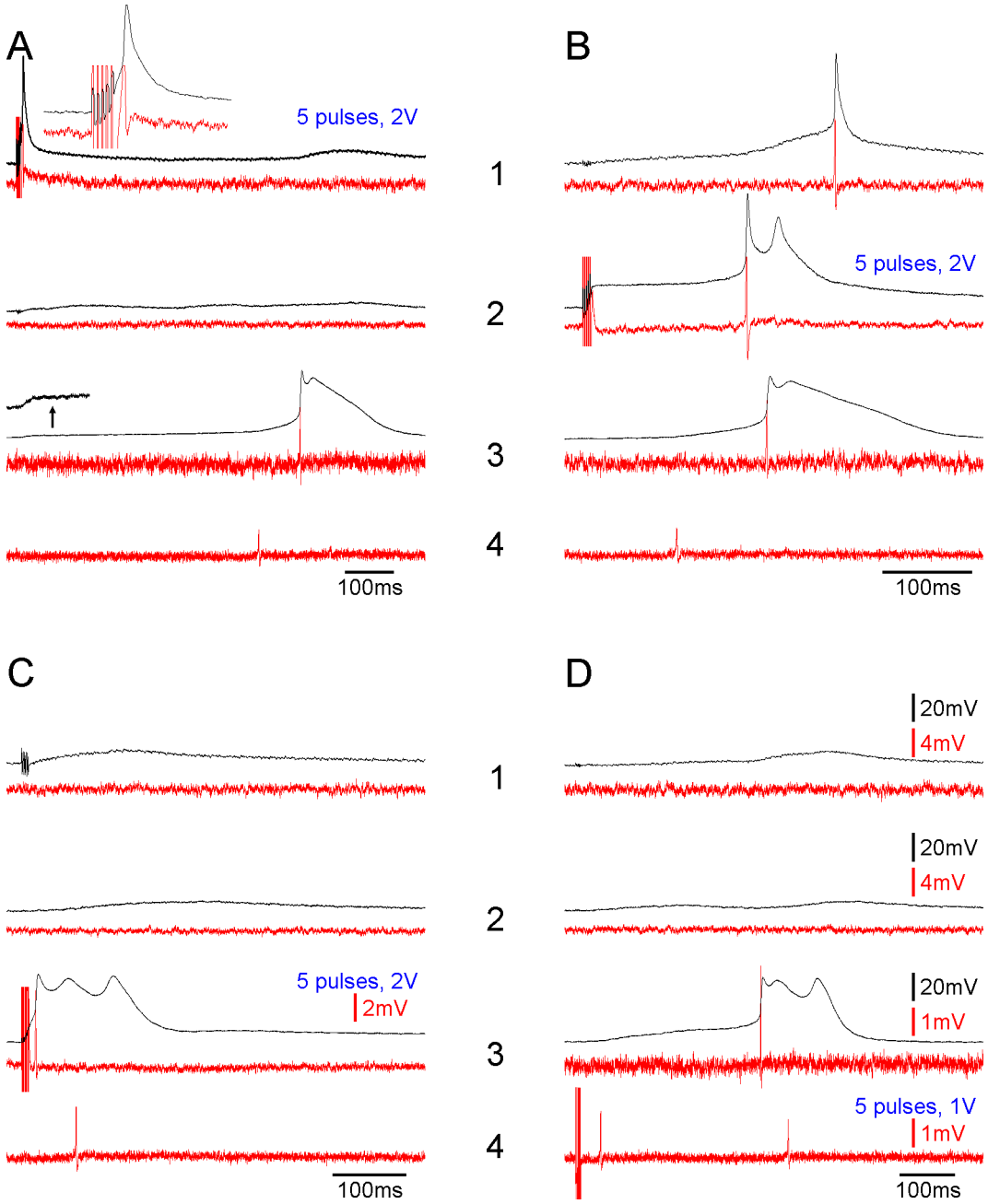


Figure 4.6: *Intracellular (black curves) and transistor (red curves) measurements of extracellularly evoked network activity. The numbers in the middle denote the respective neuron. In every diagram a different neuron is stimulated from the chip. Number and amplitude of the extracellular pulses are written at the respective transient. The scale bars in D also apply to all other diagrams, exceptions are marked separately. The time scale of the inset at the top of diagram A is expanded by a factor of 5, the inset in the middle shows the intracellular signal of 3 with the amplitude expanded by a factor of 5.*

by 3 or if it can be ascribed to spontaneous activity remains unclear. The weak depolarizations in 1 and 2 are correlated with the firing patterns of 3 and 4. While the membrane potential of neuron 1 exhibits a single broad increase in synchrony with the AP in 3, the two depolarizations in neuron 2 result from the peaks fired by 4. The postsynaptic responses were delayed for about 100ms with respect to the presynaptic input.

Data in diagrams A-D agree very well with the synaptic connection pattern shown in fig. 4.5B. They even reveal that synapses exist between neurons 4 and 2, and 4 and 3, which could not be deduced from the electrophysiological recordings due to the lack of sufficient microelectrode channels.
All transistor signals have identical shape, they are biphasic and coincident with the rising edge of the action potentials (at least for neurons 1-3). A full depletion of Na and K channels in the adherent membrane accounts for this behavior, termed A-type coupling.
Intracellularly recorded action potentials of neuron 3 were untypically long, with a second or even third rather broad peak. Ca channels in type II neurons might be the cause for this, as outlined in subsection 3.6.4. Alternatively, the cell was no longer vital. On the other hand, the transistor signal was very strong and reliable.

After these experiments, transistors 5-8 were connected to the amplifier and neurons 5-7 were additionally impaled with microelectrodes; see the micrographs in fig. 4.4 for their arrangement. Except for neuron 8, all coupled bidirectionally to the chip enabling extracellular recording and stimulation (data not shown). Furthermore, hyperpolarizing current injections revealed the existence of electrical synapses at least between the impaled cells. Neuron 7 had a high level of activity, it frequently fired action potentials without stimuli from the chip or microelectrode.

In conclusion, at least two fully functional networks grew on this chip. Their synaptic connection pattern was defined by topographic SU-8 structures. The neuron-silicon interface was very reliable for 7 out of 8 cells. Chances are quite high that both subsystems were synaptically connected, forming a single large network comprising at least 7 vital neurons. The thick neurite between 2 and 5, which is well visible in the fluorescence micrograph 4.4, strongly supports this hypothesis.

4.3 Final discussion

The examples above constitute proof-of-principle experiments for the implementation of chip-controlled neural networks with a defined synaptic connection pattern. This was achieved by combining field-effect transistors and capacitive stimulation spots with SU-8 topographic structures. Despite the success, several issues remain. They are discussed in the following paragraphs.

4.3.1 Controlling neuronal activity from the chip

When assessing the ability of transistor chips to control the activity of individual nerve cells, standard techniques such as patch clamp or impaled microelectrodes are the reference. The comparison must comprise the areas of stimulation, recording and effects on the neuron, as well as the capability of scaling up to large neural networks.

Extracellular stimulation is considerably less precise than current injection with an impaled microelectrode. The three-neuron network presented in subsection 4.2.2 clearly shows this deficit. Even though action potentials are triggered from the chip, the ‘and’ circuit could only be realized if the input neurons were stimulated with the microelectrodes.
To increase precision, the mechanism underlying extracellular stimulation must be changed. Instead of the hard-to-control transient electroporation of the adherent membrane, ion channels must be opened and closed via the chip. This is only possible if the time constants of the capacitive transients in the cleft are longer than those of the ion channels to be opened. However, stimulators covered with SiO_2, the standard dielectric in silicon processing, have a capacitance too small for this. Perhaps new materials with a higher dielectric constant such as TiO_2 will solve the problem in the future. There are already projects working on this subject [118].

Comparing transients from impaled electrodes with transistor recordings clearly demonstrates that the latter convey much less information. Action potentials are detected in a yes/no manner, but usually no subthreshold events, such as weak membrane depolarizations or even hyperpolarizations, are seen. There are examples where the extracellular signal is completely identical to the intracellular signal, even for hyperpolarization; see fig. 3.20. Since this B-type coupling is very rare, and because there are no ways to induce it, alternative approaches are needed to gain more information. For example, the cross-correlation between the activity of two neurons yields a measure for the strength of the synapse between them and can be used instead of the coupling coefficient.
Above all, most theoretical models about information processing in living neural networks, e.g. rate coding, are based on action potentials; subthreshold events are not considered. Transistor recordings are therefore detailed enough for studying networks at the system level.

Whereas the issues discussed above speak against the chip technology, the following aspects emphasize its advantages.
Conventional electrophysiological techniques are highly invasive because they puncture the cell membrane, affecting the entire system under observation. The four-neuron network shown in 4.2.3 is an instructive example. Neuronal activity was substantially altered when neurons 1-3 were impaled. While neurons 1 and 2 regularly fired action potentials in synchrony with 3 and 4 before, their activity ceased thereafter. In contrast, the transistor recordings had no adverse effect.

Another important point is the number of neurons that are monitored. Due to the size of the manipulators needed for positioning the microelectrodes, only a few cells can be impaled at the same time. In contrast, the number of transistors on a chip can be scaled up by several orders of magnitude. Only recently, a 1mm x 1mm array with 16384 recording sites was developed and used for extracellular recording from *Lymnaea* neurons [28].

In conclusion, the application determines which method is appropriate for controlling neuronal activity. If the focus is on studying single neurons with maximum information about the membrane voltage microelectrodes are preferred, whereas for applications such as the one here, transistor chips are the method of choice.

4.3.2 Defined networks in topographic structures

SU-8 topographic structures proved very effective for growing defined neural networks. While the grooves control neurite outgrowth, pits keep the somata at predefined locations, e.g. on the recording sites. This is a major advantage with respect to most other techniques, which are based on chemical patterns.
After initial difficulties with short circuiting had been solved, the combination of topographic structures and transistor chips turned out to be unproblematic. It is possible that the resist causes an increase in transistor noise, but this is not clear, yet.
Currently, pits and grooves have a detrimental effect on cell vitality. 23% of the neurons placed into the pits grew at least one single neurite, compared to 64% for neurons on plain substrates. The reason for this is not clear, possibly metabolic waste accumulates in the grooves, for details see subsection 2.5.5.

4.3.3 Stability of the chips

Manufacturing transistor chips is laborious and expensive, therefore they should ideally last for some time.
The semiconductor part of the devices is very resistant to cell culture and subsequent cleaning. During 10 culture and cleaning cycles, the thickness of the gate dielectric only decreased from 10nm to 8nm. The remaining SiO_2 is good enough for at least another 10 experiments.

Some very harsh detergents, like chromium sulfuric acid, can change the I-V characteristics of the transistors by influencing the charge carrier mobility and the flatband voltage, as outlined in 3.3.3. This is interesting from a semiconductor engineer's point of view, but is not relevant for extracellular recording.

The topographic structures processed from SU-8 polyester photoresist are much more delicate. Due to the mismatch in the thermal expansion coefficients between resist and silicon substrate, the SU-8 layer is under high internal stress. It tends to detach at the edges and peel off if subjected to thermal shock or ultrasonic cleaning. Once the topographic structures come into contact with water for several hours, they should always be kept wet and never dry out, since this may also cause detachment.
If these precautions are followed, the resist layer lasts as long as the semiconductor and chips can be used approximately 20 times.

4.3.4 Yield, the decisive factor

In the experimental part of this thesis, far too much effort went into the preparation and culture of neural networks, rather than studying them.
From 4224 neurons placed onto 264 chips (16 per chip), only three fully functional two-neuron networks, such as the one in 4.2.1, and one large network presented in 4.2.3, were obtained. Furthermore, there were 47 networks of two or three neurons with imperfections, such as synapses not being strong enough for triggering postsynaptic action potentials, neurons that coupled to the chip in only one direction or not at all, damaged cells with strange APs, etc.; see the example 4.2.2. This success rate is much too low.
The reason is quite obvious, all steps must produce perfect results in order to achieve a functional system. These include:

- isolated cells must be healthy
- they have to grow neurites which stay in the grooves
- functional synapses must be established
- the neuron-silicon interface must enable extracellular stimulation and recording

Since so many steps are involved and each one works with a probability $p_i < 1$, the overall success rate is very low

$$\prod_{i=1}^{n} p_i \ll 1 \tag{4.1}$$

The situation is similar to the early days of semiconductor electronics, when the low reliability of individual components impeded the construction of large circuits. At that time, the problem was termed, the tyranny of large numbers. The only difference here is that part of the components are biological.

For example, the beautiful network depicted in 2.17 did not even produce a single chip-controlled cell pair. Either neurons were not vital, no synapse had been established or transistor recording failed.
The last point is currently one of the major limiting factors. Only 30% of the vital neurons (n=889) were fully controllable from the chip, for details refer to 3.6.5.
The other fundamental restriction is the small percentage of neurons that are vital and grow neurites in the grooves. In the pilot study on growth-cone guidance by topographic structures, only 23% of the neurons grew processes at all, of which 62% stayed in the grooves; see subsection 2.5.5.

Interestingly, there were a few cases where growth and network formation was almost perfect, e.g. fig. 2.18 and fig. 4.4. These cases put the focus on the culture conditions and the chips themselves. As outlined in subsection 2.2.3, the cleaning procedures are rather imperfect. Either they are too strong, deteriorating subsequent cell culture, or dirt remains in the structures. Either way, the surface is in an

undefined state after cleaning, which sometimes promotes neuronal outgrowth, but often does not.

Another critical point are neurons dying soon after being placed into the pits because of injuries inflicted during their isolation. If there are too many such cells, their residues accumulate in the grooves and impede the growth of the other cells or even kill them.

The aspects discussed here are the basis for future improvements in cell culture and chip design, which are outlined below.

4.3.5 Next steps

Before transistor chips with SU-8 topographic structures can become a widespread tool in neuroscience, the yield of network growth must be increased considerably. The following paragraphs give suggestions as to how this may be achieved.

Firstly, a more efficient and reliable cleaning procedure must be found. This requires systematic studies where neurons are cultivated on chips subjected to different detergents and protocols. Disinfection with ethanol or UV light and coating with poly-L-lysine should also be considered.

Secondly, the isolation of neurons from the ganglia and their placement into the pits needs improvement. Using a special cell extraction apparatus, the number of vital cells placed onto the chip can be 90% and more [104, 107].

Thirdly, the distance between the recording sites on the chips should be reduced. This would allow even short neurites to contact neighboring cells, increasing the yield of synapse formation. Besides the devices where transistors are 400μm apart, there also exist some with 600μm internode distance. The number of synaptic connections was much lower on these chips. For a new transistor chip, distances between neighboring transistors in the range of 200μm are advisable.

Fourthly, wider grooves could enhance the growth of neurites in the structures, since growth-cones would have more space for filopodia movement. In any case, optical diffraction would be reduced and the neurites would be more visible.

Fifthly, the percentage of neurons coupling to transistors and stimulators must be increased, but this is a very difficult issue. Although the neuron-silicon interface is well understood, its formation is barely controllable, especially the distribution of the ion channels between adherent and free membrane. Genetic modification by transfection of additional channels seems promising. Maybe a much simpler approach with new substrate coatings can also give good results. Still this issue requires quite some additional work.

Chapter 5

Conclusion and outlook

The results presented here demonstrate that small networks of living neurons can be designed *in vitro* and monitored non-invasively by a semiconductor chip. Novel topographic structures processed from SU-8 photoresist guide growing neurites and keep somata in place, while capacitive stimulators evoke action potentials in individual neurons and transistors record their activity. Networks of two to four neurons were obtained and characterized, using the chip as well as with standard electrophysiology.
At their current stage, these examples are mere proof-of-principle experiments, demonstrating the feasibility of the approach and that no fundamental problems are associated with the techniques involved. For defined, chip-controlled networks to become a reliable tool in neuroscience, the rate of their successful growth must be increased. This requires changes in the chip layout and a better cell culture and cleaning protocol.
Once the yield is high enough, perceptrons, Hopfield networks and other systems of fundamental interest will be within reach. Their implementation relies on further advances in cell culture and chip technology as outlined below.

Memory and adaptation processes are generally based on chemical synapses and their ability to modify the efficiency of signal transmission. All experiments in this thesis were done with A-cluster neurons from the snail *Lymnaea stagnalis*, because they are easy to isolate from the ganglia and are present in large numbers. However, they only establish electrical synapses.
There are a few neurons in the snail brain connected by chemical synapses that also reestablish *in vitro*, e.g. those forming the respiratory central pattern generator [105]. In first experiments, such a cell pair could be reconstructed *in vitro*, with its electrical activity partly controlled from the chip [55]. Interesting effects were observed, such as post tetanic potentiation; the increase of synaptic coupling efficiency after a special presynaptic stimulus.

Despite the promising results with snail neurons, vertebrate cell donors are preferred in the long run. They give access to a much broader field of research, because more complex systems can be realized, performing higher tasks of information processing. Furthermore, chemical synapses prevail in vertebrate nervous systems, so there is no need for the time-consuming selection of special cells as with *Lymnaea stagnalis*.
The main challenge with vertebrate neurons is their size between 10μm and 15μm, about 5 times smaller than in the snail. Due to the reduced junction area and lower ionic currents released during an action potential, the extracellular signal is extremely weak. Very low noise transistors are needed to discriminate it from the background.
Only recently, action potentials from rat hippocampal neurons were successfully recorded with an optimized buried channel transistor [117]. Unlike in previous experiments [113], no signal averaging was necessary.

To gain maximum control over neuronal activity in both directions, extracellular stimulation should also be improved. Currently, neurons are stimulated by transient electroporation of the cell membrane in the cleft, a rather undefined method. Opening ion channels via the chip is preferable for its higher precision and reduced stress on the cells. However, this requires the time constants of the extracellular transient from the capacitive stimulator to be longer than those of the ion channels, a precondition that is not met with SiO_2. New dielectrics with higher dielectric constants, such as TiO_2 and HfO_2, could be used alternatively. Preliminary experiments on this subject are encouraging [118].

A rather futuristic aim is the implementation of a large chip-controlled network with complex information processing capabilities, i.e. some sort of hybrid biocomputer. While the number of neurons can be increased almost infinitely simply by adding nerve cells, scaling up the transistor chips is limited by the technology here; because every single transistor has its own source and drain line, problems with routing and connection to the amplifier soon become overwhelming.
A new device circumvents these issues by sequentially reading transistors in single rows rather than all of them simultaneously. Such chips are very complicated, requiring on-chip multiplexer and amplifier units. They are realized in CMOS technology. Infineon Technologies has developed a 128x128 transistor array that allows the sampling of every recording site at 2kHz. First tests with *Lymnaea* neurons have demonstrated that the transistors are operative [28]. Because transistors are densely packed, with just 7.8μm internode distance, we could even record the voltage profile in the cleft under a large cell.

With the advancements in network design presented in this thesis and the novel technologies introduced above, the first steps towards new tools in neuroscience and perhaps a ‘living’ neurocomputer have been made.

Appendix A

Cell culture protocols and recipes

Antibacterial solution

To remove bacterial contamination and dirt and to anesthetize deshelled snails, they were soaked in a solution of 75% autoclaved water and 25% Listerene for 5min [66]. Listerine is a mouthwash commercially available in drugstores.

Antibiotic saline ABS

Antibiotic saline was used for snail dissection, rinsing of brains and chip incubation after poly-L-lysine removal. It contains

NaCl	51.3mM
KCl	1.7mM
$CaCl_2$	4.1mM
$MgCl_2$	1.5mM
HEPES buffer	5.0mM
gentamicin	150μg/ml

in Milli-Q water (Millipore) at pH7.9, sterilized by filtration [90]. All chemicals from Sigma.

Defined medium DM

Lymnaea neurons were cultured in defined medium containing

NaCl	40.0mM
KCl	1.7mM
$CaCl_2$	4.1mM
$MgCl_2$	1.5mM
gentamicin	20μg/ml
glutamine	150μg/ml

and all other ingredients of serum-free Leibovitz L-15 medium at half the standard concentration [90, 107]. The medium was purchased from PAN Systems, Aidenbach with all ingredients included, except for gentamicin (G-3632, Sigma) and glutamine (N-Acetyl-L-Alanyl-L-Glutamin, K0202, Biochrom, Berlin), which were added before use.

High osmolarity defined medium HODM

Cell extraction was facilitated by high osmolarity medium which causes a slight shrinkage of the neurons, making them less vulnerable. The osmolarity of plain defined medium was increased from about 135mOsm/kg to about 165mOsm/kg by adding 30mM D-(+)-Glucose.

Enzymes

Prior to isolating cells, brains were treated with a solution of collagenase/dispase (269638, Boehringer Mannheim) 1.33mg/ml and trypsin (T-4665, Sigma) 0.67mg/ml in defined medium to digest tissue between the neurons in the ganglia, easing neuron removal. To minimize damage to the membranes caused by prolonged exposure to the enzymes, brains were washed 3 times after the enzyme treatment and incubated in trypsin inhibitor.

Trypsin inhibitor

Enzymatic activity of trypsin remaining after the washes was inhibited by treatment with soybean trypsin inhibitor (T-9003, Sigma) at a concentration of 0.67mg/ml in defined medium.

Cell extraction pipettes

Neurons were isolated, transferred and positioned with pipettes attached to a flexible silicone tube. Pressure was applied with a mouth-piece connected to the other end of the tube, allowing liquid to be drawn in or flushed out. The pipettes were made from glass capillaries (No. 564, Assistent) that were pulled to an inner tip diameter of approximately $100\mu m$ and fire polished (both done with a DMZ Universal Puller, Zeitz, Augsburg). They were autoclaved and coated with a siloxane solution (Sigmacote SL-2, Sigma) to prevent cells from sticking to the glass pipette.

Glass coverslip cleaning

In early experiments, glass coverslips were used as substrate. They were cleaned according to a protocol adapted from [34]:

- sonication at 80°C for 60min in 5% Ultrax 102 S (KLN, Heppenheim)
- 5-6 rinses with water
- sonication at 80°C for 60min in 5% Tickopur RP 100 (Bandelin, Berlin)
- 5-6 rinses with water
- sonication at 80°C for 60min in water, changing the water every 15min

Ultra-pure water from a Milli-Q water system (Millipore) was used throughout all steps.
Note: Powdered Tickopur RP100 is not produced any more, alternatively the liquid detergent Tickopur R 60 (Dr.H.Stamm, Berlin) is offered.

Substrate sterilization

Coverslips and substrates with topographic structures were dried in an aseptic flow box and sterilized by UV-exposure for 45min. Aseptic adhesive chambers (flexiPERM, Sartorius AG, Göttingen) were attached to the substrates, to hold the cell culture medium.
The PMMA culture chambers of transistor chips were filled with an antibacterial solution of 70%

ethanol and 30% water during UV-sterilization. This prevented the SU-8 resist from drying out, which can cause topographic structures to blister off.

Poly-L-lysine coating

The success of neuronal outgrowth and neurite morphology highly depends on the substrate properties. Poly-L-lysine is a common coating for culturing *Lymnaea* neurons. It provides an adhesive surface presumably due to the high charge density of the polyanionic molecule [56].
Sterilie substrates were incubated in a solution of 1mg/ml poly-L-Lysine P-6516 (Sigma) in 150mM Tris buffer (Sigma) at pH8.4. After 2h-10h the liquid was removed, the substrates were rinsed 3 times with aqua ad (water for medical use, Braun, Melsungen) and incubated in antibiotic saline for 15min. After 3 more washes, the culture chambers were filled with defined medium and neurons were plated.

Electrophysiology

Neurons were impaled with sharp microelectrodes (glass capillaries from Hilgenberg, Malsfeld) filled with a saturated K_2SO_4 solution. The electrode resistance was 30MΩ-60MΩ. They were connected to current clamp bridge amplifiers (BA-1s, npi Advanced Electronic Systems, Tamm, Germany). Hyperpolarizing and depolarizing currents were injected in one cell and the resulting voltage transients of the pre and postsynaptic neuron were recorded. Artifacts due to unbalanced electrodes were subtracted.

Staining with Lucifer Yellow

Neurons were impaled with sharp microelectrodes (the same as used for electrophysiology) filled with a solution of 100mg/ml Lucifer Yellow (Sigma, L-0259) in milli-Q water. Hyperpolarizing square wave pulses with 1Hz frequency and 1nA amplitude were applied to drive the solution into the cell. After 15min-30min staining was complete. Micrographs were taken with the fluorescence microscope in fig. 3.13 equipped with appropriate filters.

Appendix B

Chip processing and characterization

SU-8 process parameters

Topographic structures were made from the n-type polyester photoresist SU-8 (Micro Chem Corp., MA), for development XP SU-8 developer (micro resist technology, Berlin) was used. The process comprised the following steps:

Nr.	process step	description
1	cleaning	oxidized wafers: hot CARO for 10min; metalized wafers: sonication in acetone for 5min and ethanol for 5min, rinse in QDR and spin dry
2	drying	RTP 400°C 30s, alternatively normal oven 200°C 30min
3	spin resist	dispense with syringe about 3ml/wafer (ø 100mm), spread: 500rpm for 35s, accelerate, spin 20s at final speed, see fig. B.1 for spin speed-thickness curve
4	softbake	bake wafer on hotplate preheated to 50°C for 120s, ramp temperature to 75°C (10°C/min), bake at 75°C for 90s, ramp up to 90°C (10°C/min), bake for 60s, remove wafer from hotplate and put on cleanroom towel for slow cool down and to prevent thermal shock
5	bead removal	spin wafer at 2000rpm and carefully apply acetone at the rim with a syringe with a fine cannula, dry wafer for 2h at 40°C in oven to evaporate residual acetone
6	exposure	mask-aligner, hard contact mode, power: 12mW/cm^2 (at 365nm), exposure time: 100s (for a resist thickness of 30μm, thicker layers require longer exposure times)
7	post exposure bake	identical to softbake, see step 4
8	development	immersion in first bath for 120s, in second bath for 30s (for a 30μm thick resist layer), both baths are filled with SU-8 developer, spin wafer dry
9	hardbake	with hotplate, slowly ramp temperature from 20°C to 200°C (5°C/min), bake at 200°C for 60min, ramp down to room temperature (2°C/min)

Table B.1: *Processing of SU-8 topographic structures.*

For two-layer structures, steps 3 to 7 are repeated after processing step 7 of the first layer.

Spin speed-thickness curve

Fig. B.1 depicts the spin speed-thickness curve of SU8-10. Thicker layers can be made by reducing the revolution, e.g. 500rpm give a final thickness of 120μm-130μm, or using resist with higher viscosity, e.g. SU-8 50.

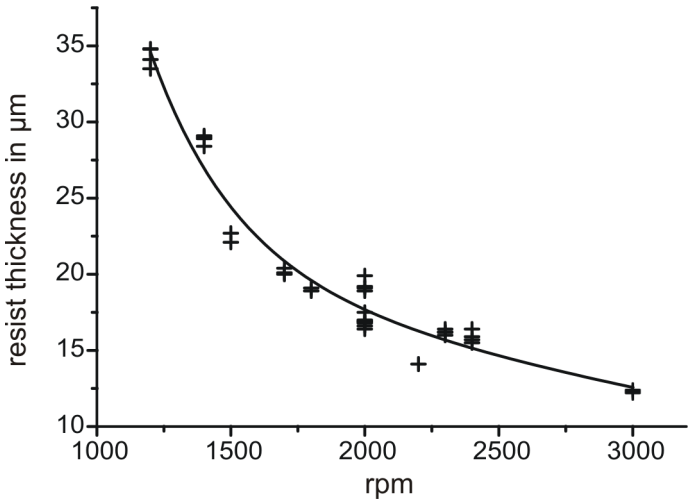


Figure B.1: *Measured spin speed-thickness curve of SU-8 10. The resist is designed to yield a final thickness of 10μm if deposited with 2500rpm. The measured values indicate slightly thicker resist layers.*

Transistor chip process description

Nr.	process step	parameters	A	B	C	D
0	substrate	p doped (boron), 100mm, CZ wafer, [100] , 2-4Ωcm	•	•	•	•
1	cleaning	CARO, SC-1, HF-dip, SC-2	•	•	•	•
2	mask, alignment marks	vacuum contact, 6.0s, MX-84 developer 20s-25s	•	•	•	•
3	plasma etch	post development, O_2-plasma: P=70W, p=0.6Torr, t=120s, O_2=30ccm, Si-etch: P=100W, p=0.1Torr, t=50s, Ar=4.0sccm, O_2=4.0sccm, CHF_3=2.0sccm, SF_6=13sccm	•	•	•	•
4	cleaning	CARO, SC-1, HF-dip, SC-2	•	•	•	•
5	oxide layer	12nm, RTP	•	•	•	•
6	mask, implantation lines	thicker resist 1.5μm, spin speed 3000rpm, vacuum contact, 4.8s, MX-84 developer 20s-25s	•	•	•	•
7	implantantion, lines	phosphorous, 150keV, $5{\cdot}10^{15}cm^{-2}$	•	•	•	•
8	mask removal	5 x CARO, O_2-plasma: P=100W, p=0.6Torr, t=15min, O_2=30sccm, Ar=5.0sccm	•	•	•	•
9	cleaning	CARO, SC-1, HF-dip, SC-2	•	•	•	•
10	oxide layer	12nm, RTP, 1100°C, 29s	•	•	•	•
11	mask, implantation channel	vacuum contact, 4.8s, MX-84 developer 20s-25s	•	•	•	•
12	implantantion, channel	phosphorous, 80keV: $6{\cdot}10^{11}cm^{-2}$, $9{\cdot}10^{11}cm^{-2}$, $1.2{\cdot}10^{12}cm^{-2}$; 70keV: $9{\cdot}10^{11}cm^{-2}$; 60keV: $9{\cdot}10^{11}cm^{-2}$, $1.3{\cdot}10^{12}cm^{-2}$	•	•	•	•

Nr.	process step	parameters	A	B	C	D
13	cleaning	CARO, SC-1, HF-dip, SC-2	•	•	•	•
14	mask, implantation channel	resist SU-8 2 n-type about 2μm thick, hard contact, 50s, SU-8 developer, 40s		•		•
15	implantation, insulation	BF_2, 40keV, $9{\cdot}10^{12}cm^{-2}$		•		•
16	cleaning	CARO, SC-1, HF-dip, SC-2		•		•
17	oxide layer	8nm, RTP, 1100°C, 15s			•	•
18	field oxide deposition	PECVD: 720nm, P=40W, T=300°C, t=10min, 5% silane in He=100sccm, NO_2=500sccm			•	•
19	compaction	RTP, 1100°C, t=15s, oxide thickness afterwards 710nm			•	•
20	mask, guidance cues	resist SU-8 2 n-type, hard contact, 50s, SU-8 developer, 40s			•	•
21	field oxide etch	AHF 12.5%, t=7min			•	•
22	mask removal	CARO in a separate container			•	•
23	cleaning	CARO, SC-1, HF-dip, SC-2			•	•
24	gate oxide	10nm, RTP, 1100°C, 29s	•	•	•	•
25	mask, bondpads	hard contact, 5.5s, MX-84 developer 20s-25s	•	•	•	•
26	etch, bondpads	HF, 1%, 3min	•	•	•	•
27	aluminum deposition	200nm-300nm, sputter, AlSi target, P=150W, p_{Ar}=$6{\cdot}10^{-3}$mbar, t=4min	•	•	•	•
28	lift-off	bake, 120°C, 20min, sonication in acetone, 10min-30min	•	•	•	•
29	H_2-anneal	RTP, 460°C, t=120s, H_2=3sLm	•	•	•	•
30	SU-8 structures	see table B.1	•	•	•	•
31	infrastructure	cutting, gluing dice into ceramic packages, bonding and attachment of culture chambers	•	•	•	•

Table B.2: *Overview of all processing steps with relevant parameters. The last four columns indicate whether a step was part of a specific process line A-D or not.*

I-V curve fit

Theoretical curves obtained from the model in subsection 3.2.3, eq. 3.17, are fit to measured data with a Levenberg-Marquardt algorithm adapted to two-dimensional inputs. The fixed parameters are:

donor concentration	:	N_D =$7.5{\cdot}10^{16}cm^{-3}$
acceptor concentration	:	N_A =$1.0{\cdot}10^{16}cm^{-3}$
depth of pn junction	:	x_j =100nm
thickness of gate oxide	:	d_{ox} =10nm
dielectric constant Si	:	ϵ_{Si}=11.9
dielectric constant SiO_2	:	ϵ_{SiO_2} =3.9
gate length	:	L =3.5μm
gate width	:	W =9.5μm

Table B.3: *Fixed parameters in the I-V fit.*

Actual gate width and length are slightly smaller then the nominal dimensions 10μm x 4μm due to lateral straggling and diffusion of the lead and insulation implants.

The flatband voltage V_{FB} and electron mobility μ_n are free fit parameters. They are ill-defined by the process steps and have not been determined otherwise.

Characterization of noise

The power spectrum of a temporally fluctuating quantity $a(t)$ is defined as:

$$S(f) := \lim_{T\to\infty} \frac{1}{2T} \left| \int_{-T}^{T} a(t) e^{2\pi i f t} dt \right|^2 \tag{B.1}$$

When describing noise, $a(t)$ is either the device current or the voltage; this should always be indicated to avoid confusion. For the extracellular recording of neuronal activity, noise related to the gate voltage is relevant. It determines whether a small voltage change in the cleft between cell and chip can be detected or not.

Comparing transistor performance is facilitated with the characteristic figure

$$V_{LFN} := \sqrt{\int_{100Hz}^{2000Hz} S_{V_{gs}}(f) df} \tag{B.2}$$

which integrates the gate voltage related noise power spectrum over the low frequency range (index LFN, low frequency noise) relevant for this application. The lower integration limit in the definition, 100Hz, is too high for the slow and broad action potentials of snail neurons, 10Hz would be more appropriate. Nevertheless, the definition is retained to allow the direct comparison with the numbers from [116]. Also, the difference in V_{LFN} is almost negligible when integrating from 100Hz instead of 10Hz. For example, it decreases from 67μV at 10 Hz to 51μV at 100Hz.

Appendix C

Simulation of extracellular signals

Cell and junction parameters

specific membrane capacitance	:	c_M=1μF/cm^2
specific chip capacitance	:	$c_S = \varepsilon_{SiO_2}\varepsilon_0/d$=0.35$\mu$F/cm^2
diameter of the contact area	:	d_J=30μm
neuron diameter	:	60μm
ratio of junction to free membrane	:	$\beta_M = A_{JM}/A_{FM}$=1/15
thickness of the cleft	:	d=50nm
specific conductance of the medium	:	ρ=6.7mS/cm
junction conductance	:	g_J=$5d/(\rho(d_J/2)^2)$=75mS/cm^2
injected current	:	I_{INJ}=1nA
channel conductances	:	$\overline{g}_{Na}$ =120mS/cm^2, $\overline{g}_K$ =36mS/cm^2, g_L =0.3mS/cm^2
reversal potentials	:	$V_0^{Na} = V_0$+115mV, $V_0^K = V_0$-12mV, $V_0^L = V_0$+10.6mV

Hodgkin-Huxley rate equations

In their original work [45] Hodgkin and Huxley used the voltage variable V_{HH} which denotes the displacement of the membrane potential V from the resting value V_0, with negative values for depolarization. With the relation $V_{HH} = V_0 - V$ the original expressions were translated into the variables used here. The rate constants in the table below are in units of 1/ms and all voltages are in mV.

particle i	activation α_i	deactivation β_i
n	$0.01\frac{V_0 - V + 10}{e^{\frac{V_0 - V + 10}{10}} - 1}$	$0.125e^{\frac{V_0 - V}{80}}$
m	$0.1\frac{V_0 - V + 25}{e^{\frac{V_0 - V + 25}{10}} - 1}$	$4e^{\frac{V_0 - V}{18}}$
h	$0.07e^{\frac{V_0 - V}{20}}$	$\frac{1}{e^{\frac{V_0 - V + 30}{10}} + 1}$

Appendix D

Abbreviations

ABS	:	antibiotic saline
AP	:	action potential
CARO	:	hot, reactive mixture of H_2SO_4 and H_2O_2 at a ratio of 3:1
CM	:	conditioned medium
DAC	:	digital analog converter
div	:	days in vitro
DM	:	defined medium
ECM	:	extracellular matrix
FET	:	field-effect transistor
NS	:	normal saline
OPA	:	operational amplifier
RTP	:	rapid thermal processing
SAM	:	substrate adsorbed material

Bibliography

[1] R. W. Aldrich, P. A. Getting, and S. H. Thompson. Mechanism of frequency-dependent broadening of molluscan neurone soma spikes. *J. Physiol.* 291 (1979), 531–544.

[2] P. Bergveld. Development, operation and application of the ion-sensitive filed-effect transistor as a tool for electrophysiology. *IEEE Trans. Biomed. Eng.* 19 (1972), 342–351.

[3] B. Besl. Elektrische Kopplung von Hirnschnitten mit Feldeffekttransistoren. Ph.D. thesis, Technische Universität München (2001).

[4] S. N. Bhatia and C. S. Chen. Tissue engineering at the micro-scale. *Biomed. Microdev.* 2 (1999), 131–144.

[5] A. S. Blawas and W. M. Reichert. Protein patterning. *Biomat.* 19 (1998), 595–609.

[6] A. Blum. *Elektronisches Rauschen*. Teubner, Stuttgart (1996).

[7] R. Bodmer, D. Dagan, and I. B. Levitan. Chemical and electronic connections between Aplysia neurons in primary culture. *J. Neurosci.* 4 (1984), 228–233.

[8] D. W. Branch, J. M. Corey, J. A. Weyhenmeyer, G. J. Brewer, and B. C. Wheeler. Microstamp patterns of biomolecules for high-resolution neuronal networks. *Med. Biomed. Eng. Comp.* 36 (1998), 135–141.

[9] S. Britland, H. Morgan, B. Wojiak-Stodart, M. Riehle, A. Curtis, and C. Wilkinson. Synergistic and hierarchical adhesive and topographic guidance of BHK cells. *Exp. Cell Res.* 228 (1996), 313–325.

[10] J. R. Buitenweg, W. L. R. Rutten, and E. Marani. Geometry-based finite-element modeling of the electrical contact between a cultured neuron and a microelectrode. *IEEE Trans. Biomed. Eng.* 50 (2003), 501–509.

[11] D. T. Chiu, N. L. Jeon, S. Huang, R. S. Kane, C. J. Wargo, I. S. Choi, D. E. Ingber, and G. M. Whitesides. Patterned deposition of cells and proteins onto surfaces by using three-dimensional microfluidic systems. *PNAS* 97 (2000), 2408–2413.

[12] P. Clark, P. Connolly, A. S. G. Curtis, J. A. T. Dow, and C. D. W. Wilkinson. Topographical control of cell behaviour: I. Simple step cues. *Development* 99 (1987), 439–448.

[13] P. Clark, P. Connolly, A. S. G. Curtis, J. A. T. Dow, and C. D. W. Wilkinson. Topographical control of cell behaviour: II. Multiple grooved substrata. *Development* 108 (1990), 635–644.

[14] L. B. Cohen, B. M. Salzberg, H. V. Davila, W. N. Ross, D. Landowne, A. S. Waggoner, and C. H. Wang. Changes in axon fluorescence during activity - molecular probes of membrane-potential. *J. Membr. Biol.* 19 (1974), 1–36.

[15] J. M. Corey, B. C. Wheeler, and G. J. Brewer. Compliance of hippocampal neurons to patterned substrate networks. *J. Neurosci. Res.* 30 (1991), 300–307.

[16] J. M. Corey, B. C. Wheeler, and G. J. Brewer. Micrometer resolution silane-based patterning of hippocampal neurons: critical variables in photoresist and laser ablation processes for substrate fabrication. *IEEE Trans. Biomed. Eng.* 43 (1996), 944–955.

[17] H. G. Craighead, S. W. Turner, R. C. Davis, C. James, A. M. Perez, P. M. St John, M. S. Isaacson, L. Kam, W. Shain, J. N. Turner, and G. Banker. Chemical and topographical surface modification for control of central nervous system cell adhesion. *Biomed. Microdev.* 1 (1998), 49–64.

[18] A. Curtis and M. Rhiele. Tissue engineering: the biophysical backgroound. *Phys. Med. Biol.* 46 (2001), R47–R65.

[19] A. S. G. Curtis and C. D. W. Wilkinson. Topographical control of cells. *Biomat.* 18 (1997), 1573–1583.

[20] J. DeFelipe and E. G. Jones. *Cajal on the cerebral cortex - An annotated translation of the complete writings*. Oxford University Press (1988).

[21] E. Delamarche, A. Bernard, H. Schmid, B. Michel, and H. Biebuyck. Patterned delivery of immunoglobulins to surfaces using microfluidic networks. *Science* 276 (1997), 779–781.

[22] M. C. Denyer, S. T. Britland, A. S. G. Curtis, and C. D. W. Wilkinson. Patterning living neural networks on microfabricated microelectronic electrophysiological recording devices. *Cellular Eng.* 2 (1997), 122–131.

[23] S. Dertinger. Kontrolle des neuronalen Wachstums durch elektrische Felder auf chemisch mikrostrukturiertem Silizium. Ph.D. thesis, Technische Universität München (1998).

[24] C. S. Dulcey, J. H. Georger, V. Krauthamer, D. A. Stenger, T. L. Fare, and J. M. Calvert. Deep UV photochemistry of chemisorbed monolayers: Patterned coplanar molecular assemblies. *Science* 252 (1991), 551–554.

[25] D. Durand. The somatic shunt cable model for neurons. *Biophys. J.* 46 (1984), 645–653.

[26] A. M. Dymond. Characteristics of the metal-tissue interface of stimulation electrodes. *IEEE Trans. Biomed. Eng.* BME-23 (1976), 274–280.

[27] A. Ehrlicher, T. Betz, B. Stuhrmann, D. Koch, V. Milner, M. G. Raizen, and J. Käs. Guiding neuronal outgrowth with light. *PNAS* 99 (2002), 16024–16028.

[28] B. Eversmann, M. Jenkner, F. Hofmann, C. Paulus, R. Brederlow, B. Holzapfl, P. Fromherz, M. Merz, M. Brenner, M. Schreiter, R. Gabl, K. Plehnert, M. Steinhauser, G. Eckstein, D. Schmitt-Landsiedel, and R. Thewes. A 128 x 128 CMOS bio-sensor array for extracellular recording of neural activity. *IEEE J. Solid State Circ.* .

[29] R. G. Flemming, C. J. Murphy, G. A. Abrams, S. L. Goodman, and P. F. Nealy. Effects of synthetic micro- and nano-structured surfaces on cell behavior. *Biomat.* 20 (1999), 573–588.

[30] A. Folch and M. Toner. Microengineering of cellular interactions. *Annu. Rev. Biomed. Eng.* 2.

[31] P. Fromherz. Extracellular recording with transistors and the distribution of ionic conductances in a cell membrane. *Eur. Biophys. J. Biophys. Lett.* 28 (1999), 254–258.

[32] P. Fromherz. Neuroelectronic Interfacing. In R. Waser, ed., *Nanoelectronics and Information Technology*. Wiley-VCH, Berlin (2003), 783–810.

[33] P. Fromherz, A. Offenhäuser, T. Vetter, and J. Weis. A neuron-silicon junction: A retzius cell of the leech on an insulated-gate field-effect transistor. *Science* 252 (1991), 1290–1293.

[34] P. Fromherz and G. Reinbold. Energy transfer between fluorescent dyes spaced by multilayers of cadmium salts of fatty acids. *Thin Solid Films* 160 (1988), 347–353.

[35] P. Fromherz and H. Schaden. Defined neuronal arborizations by guided outgrowth of leech neurons in culture. *Eur. J. Neurosci.* 6 (1994), 1500–1504.

[36] P. Fromherz and A. Stett. Silicon-neuron junction - capacitive stimulation of an individual neuron on a silicon chip. *Phys. Rev. Lett.* 75 (1995), 1670–1673.

[37] P. A. Garrity. Signal transduction in axon guidance. *CMLS* 55 (1999), 1407–1415.

[38] J. Geiger. Zur spontanen Synaptogenese in regenerierten Neuriten identifizierter Neurone von hirudo medicinalis in primärer Zellkultur. Diplomarbeit, Freie Universität Berlin (1992).

[39] C. S. Goodman. Mechanisms and molecules that control growth cone guidance. *Annu. Rev. Neurosci.* 19 (1996), 341–377.

[40] G. W. Gross, W. Y. Wen, and J. W. Lin. Transparent indium-tin oxide electrode patterns for extra-cellular, multisite recording in neuronal cultures. *J. Neurosci. Meth.* 15 (1985), 243–252.

[41] R. D. Hadley, S. B. Kater, and C. S. Cohan. Electrical synapse formation depends on interaction of mutually growing neurites. *Science* 221 (1983), 466–468.

[42] J. A. Hammarback, S. L. Palm, L. T. Furcht, and P. C. Letourneau. Guidance of neurite outgrowth by pathways of substratum-adsorbed laminin. *J. Neurosci. Res.* 13 (1985), 213–220.

[43] J. R. Hauser. Extraction of experimental mobility data for MOS devices. *IEEE Trans. Electron Devices* 43 (1996), 1981–1988.

[44] M. O. Heuschkel, L. Guerin, B. Buisson, D. Bertrand, and P. Renaud. Buried microchannels in polymer for delivering of solutions to neurons in a network. *Sens. Act. B* 48 (1998), 356–361.

[45] A. L. Hodgkin and A. F. Huxley. A quantitative description of membrane current and its application to conduction and excitation in nerve. *J. Physiol.* 117 (1952), 500–544.

[46] K. Hong, M. Nishiyama, J. Henley, M. Tessier-Lavigne, and M.-m. Poo. Calcium signalling in the guidance of nerve growth by netrin-1. *Nature* 403 (2000), 93–98.

[47] P. Horrowitz and W. Hill. *The art of electronics*. Cambridge University Press, 2nd edn. (1989).

[48] C. Jakobson, I. Bloom, and Y. Nemirovsky. 1/f noise in CMOS transistors for analog applications from subthreshold to saturation. *Solid-State Electronics* 42 (1998), 1807–1817.

[49] M. Jenkner. Hybride Netzwerke aus Neuronen von Lymnaea stagnalis und Silizium-Chips. Ph.D. thesis, Technische Universität München (1999).

[50] M. Jenkner, B. Muller, and P. Fromherz. Interfacing a silicon chip to pairs of snail neurons connected by electrical synapses. *Biol. Cybern.* 84 (2001), 239–249.

[51] Y. Jimbo, H. P. C. Roninson, and A. Kawana. Simultaneous measurement of intracellular calcium and electrical activity from patterned neural networks in culture. *IEEE Trans. Biomed. Eng.* 40 (1993), 804–810.

[52] D. R. Jung, R. Kapur, T. Adams, K. A. Giuliano, M. Mrksich, H. G. Craighead, and D. L. Taylor. Topographical and physicochemical modification of material surface to enable patterning of living cells. *Crit. Rev. Biotech.* 21 (2001), 111–154.

[53] E. R. Kandel, J. H. Schwartz, and T. M. Jessel. *Principles of neural science*. McGraw-Hill (2000).

[54] R. S. Kane, S. Takayama, E. Ostuni, D. E. Ingber, and G. M. Whitesides. Patterning proteins and cells using soft lithography. *Biomat.* 20 (1999), 2363–2376.

[55] R. A. Kaul, N. I. Syed, and P. Fromherz. Neuron-semiconductor chip with chemical synapse between identified neurons. *Phys. Rev. Lett.* , in press.

[56] D. Kleinfeld, K. H. Kahler, and P. E. Hockberger. Controlled outgrowth of dissociated neurons on patterned substrates. *J. Neurosci.* 8 (1988), 4098–4120.

[57] C. Koch. *Biophysics of computation*. Oxford University Press (1999).

[58] M. Kyriakides, C. R. McCrohan, C. T. Slade, N. I. Syed, and W. Winlow. The morphology and electrophysiology of the neurones of the paired pedal ganglia of Lymnaea stagnalis. *Comp. Biochem. Physiol.* 93A (1989), 861–876.

[59] A. Lambacher. Fluoreszenz-Interferenzkontrast-Mikroskopie von Membranen auf Silizium. Ph.D. thesis, Universität Ulm (1994).

[60] A. Lambacher and P. Fromherz. Luminiscence of dye molecules on oxidized silicon and fluorescence interference contrast microscopy of biomembranes. *J. Opt. Soc. Am. B* 19 (2002), 1435–1453.

[61] P. C. Letourneau. Cell-to-substratum adhesion and guidance of axonal elongation. *Dev. Biol.* 44 (1975), 92–101.

[62] D. R. Lide, ed. *Handbook of chemistry and physics*. CRC Press, 82 edn. (2001).

[63] V. A. Liu and S. N. Bhatia. Three-dimensional photopatterning of hydrogels containing living cells. *Biomed. Microdev.* 4 (2002), 257–266.

[64] M. Y. Macias, J. H. Battocletti, C. H. Sutton, F. A. Pintar, and D. J. Maiman. Directed and enhanced neurite growth with pulsed magnetic field stimulation. *Bioelectromag.* 21 (2000), 272–286.

[65] N. S. Magoski and A. G. M. Bulloch. Trophic and contact conditions modulate synapse formation between identified neurons. *J. Neurophysiol.* 79 (1998), 3279–3283.

[66] N. S. Magoski, N. I. Syed, and A. G. M. Bulloch. A neuronal network from the mollusc Lymnaea stagnalis. *Brain Res.* 645 (1994), 201–214.

[67] M. P. Maher, J. Pine, J. Wright, and Y. C. Tai. The neurochip: a new multielectrode device for stimulating and recording from cultured neurons. *J. Neurosci. Meth.* 87 (1999), 45–56.

[68] A. L. MC Worther. 1/f noise and germanium surface properties. In K. R.H., ed., *Semiconductor surface physics*. University Pennsylvania Press, Philadelphia (1957).

[69] C. D. McCaig, A. M. Rajnicek, B. Song, and M. Zhao. Has electrical growth cone guidance found its potential. *Trends Neurosci.* 25 (2002), 354–359.

[70] S. McLaughlin and M.-m. Poo. The role of electro-osmosis in the electric-field-induced movement of charged macromolecules on the surface of cells. *Biophys. J.* 34 (1981), 85–93.

[71] MED systems (www.med64.com). Tech. rep. (2003).

[72] Multichannel systems, sales representative. (www.multichannelsystems.com) (2003).

[73] I. Nagata, A. Kawana, and N. Nakatsuji. Perpendicular contact guidance of CNS neuroblasts on artificial microstructures. *Development* 117 (1993), 401–408.

[74] K. K. Ng. *Complete guide to semiconductor devices*. John Wiley & Sons (2002).

[75] Y. Nishi and R. Doering, eds. *Handbook of semiconductor manufacturing technology*. Marcel Dekker, Inc. (2000).

[76] J. J. Pancrazio, P. P. Bey Jr, D. S. Cuttino, J. K. Kusel, D. A. Borkholder, K. M. Shaffer, G. T. A. Kovacs, and D. A. Stenger. Portable cell-based biosensor system for toxin detection. *Sens. Act. B* (1998), 179–185.

[77] R. F. Pierret. *Field effect devices*. Addison-Wesley (1990).

[78] R. F. Pierret. *Semiconductor device fundamentals*. Addison-Wesley (1996).

[79] A. A. Prinz. Towards defined networks: Guided growth, cable transmission and electrical synapses of cultured snail neurons. Ph.D. thesis, Technische Universität München (2000).

[80] A. A. Prinz. personal communication (2003).

[81] A. A. Prinz and P. Fromherz. Electrical synapses by guided growth of cultured neurons from the snail Lymnaea stagnalis. *Biol. Cybern.* 82 (2000), L1–L5.

[82] A. A. Prinz and P. Fromherz. Effect of neuritic cables on conductance estimates for remote electrical synapses. *J. Neurophysiol.* 89 (2003), 2215–2224.

[83] A. M. Rajnicek, S. Britland, and C. D. McCaig. Contact guidance of CNS neurites on grooved quartz: influence of groove dimensions, neuronal age and cell type. *J. Cell. Sci.* 110 (1997), 2905–2913.

[84] A. M. Rajnicek and C. D. McCaig. Guidance of CNS growth cones by substratum grooves and ridges: effects of inhibitors of the cytoskeleton, calcium channels and signal transduction pathways. *J. Cell. Sci.* 110 (1997), 2915–2924.

[85] W. Rall. Branching dendritic trees and motoneuron membrane resistivity. *Exp. Neurol.* 1 (1959), 491–527.

[86] I. W. Rangelow and H. Löschner. Reactive ion etching for microelectrical mechanical system fabrication. *J. Vac. Sci. Technol. B* 13 (1995), 2394–2399.

[87] M. S. Ravenscroft, K. E. Bateman, K. M. Shaffer, H. M. Schessler, D. R. Jung, T. W. Schneider, C. B. Montgomery, T. L. Custer, A. E. Schaffner, Q. Y. Liu, Y. X. Li, J. L. Barker, and J. J. Hickman. Developmental neurobiology implications from fabrication and analysis of hippocampal neuronal networks on patterned silane-modified surfaces. *J. Am. Chem. Soc.* 120 (1998), 12169–12177.

[88] W. G. Regehr, J. Pine, C. S. Cohan, M. D. Mischke, and D. W. Tank. Sealing cultured invertebrate neurons to embedded dish electrodes facilitates long-term stimulation and recording. *J. Neurosci. Meth.* 30 (1989), 91–106.

[89] W. G. Regehr, J. Pine, and D. B. Rutledge. A long-term in vitro silicon-based microelectrode-neuron connection. *IEEE Trans. Biomed. Eng.* 35 (1988), 1023–1032.

[90] R. L. Ridgway, N. I. Syed, K. Lukowiak, and A. G. M. Bulloch. Nerve growth factor (NGF) induces sprouting of specific neurons of the snail, Lymnaea stagnalis. *J. Neurobiol.* 22 (1991), 377–390.

[91] B. Sakmann and E. Neher, eds. *Single-channel recording.* Plenum Press (1995).

[92] M. Sandison, A. S. G. Curtis, and C. D. W. Wilkinson. Effective extra-cellular recording from vertebrate neurons in culture using a new type of micro-electrode array. *J. Neurosci. Meth.* 114 (2002), 63–71.

[93] H. Schaden. Experimente zum Aufbau definierter Netzwerke aus identifizierten Neuronen von Hirudo medicinalis in Zellkultur. Ph.D. thesis, Universität Ulm (1992).

[94] R. Schaetzthauer and P. Fromherz. Neuron-silicon junction with voltage-gated ionic currents. *Eur. J. Neurosci.* 10 (1998), 1956–1962.

[95] M. Scholl, C. Sproessler, M. Denyer, M. Krause, K. Nakajima, A. Maelicke, W. Knoll, and A. Offenhaeusser. Ordered networks of rat hippocampal neurons attached to silicon oxide surfaces. *J. Neurosci. Meth.* 104 (2000), 65–75.

[96] D. B. Schwartz, R. E. Howard, J. S. Denker, R. W. Epworth, H. P. Graf, W. Hubbard, L. D. Jackel, B. Straughn, and D. M. Tennant. Dynamics of microfabricated electronic neural networks. *Appl. Phys. Lett.* 50 (1987), 1110–12.

[97] R. Singhvi, A. Kumar, G. P. Lopez, G. N. Stephanopoulos, D. I. C. Wang, G. M. Whitesides, and D. E. Ingber. Engineering cell shape and function. *Science* 264 (1994), 696–698.

[98] C. T. Slade, J. Mills, and W. Winlow. The neuronal organisation of the paired pedal ganglia of Lymnaea stagnalis (L.). *Comp. Biochem. Physiol.* 69A (1981), 789–803.

[99] W. M. Soppa and H. G. Wagemann. Investigation and modeling of the surface mobility of MOSFETs from -25 to 150°C. *IEEE Trans. Electron Devices* 35 (1988), 970–977.

[100] D. A. Stenger, J. J. Hickman, K. E. Bateman, M. S. Ravenscroft, W. Ma, J. J. Pancrazio, K. Shaffer, A. E. Schaffner, D. H. Cribbs, and C. W. Cotman. Microlithographic determination of axonal/dendritc polarity in cultured hippocampal neurons. *J. Neurosci. Meth.* 82 (1998), 167–173.

[101] A. Stett, B. Muller, and P. Fromherz. Two-way silicon-neuron interface by electrical induction. *Phys. Rev. A* 55 (1997), 1779–1782.

[102] W. W. Stewart. Functional connections between cells as revealed by dye-coupling with a highly fluorescent naphtalimide tracer. *Cell* 14 (1978), 741–759.

[103] B. Straub, E. Meyer, and P. Fromherz. Recombinant maxi-K channels on transistor, a prototype of iono-electronic interfacing. *Nat. Biotechnol.* 19 (2001), 121–124.

[104] N. I. Syed. personal communication (2003).

[105] N. I. Syed, A. G. M. Bulloch, and K. Lukowiak. In vitro reconstruction of the central pattern generator of the mollusc Lymnaea. *Science* 250 (1990), 282–285.

[106] N. I. Syed, K. Lukowiak, and A. G. M. Bulloch. Specific in vitro synaptogenesis between identified Lymnaea and Helisoma neurons. *NeuroReport* 3 (1992), 793–796.

[107] N. I. Syed, H. Zaidi, and P. Lovell. In vitro reconstruction of neuronal circuits: A simple model system approach. In U. Windhorst and H. Johansson, eds., *Modern Techniques in Neuroscience Research*. Springer (1999), 361–377.

[108] S. M. Sze. *Physics of semiconductor devices*. John Wiley & Sons (1981).

[109] S. Takayama, J. C. McDonald, E. Ostuni, M. N. Liang, P. J. A. Kenis, R. F. Ismagilov, and G. M. Whitesides. Patterning cells and their environments using multiple laminar fluid flows in capillary networks. *PNAS* 96 (1999), 5545–5548.

[110] M. Tessier-Lavigne and C. S. Goodman. The molecular biology of axon guidance. *Science* 274 (1996), 1123–1133.

[111] H. C. Tuckwell. *Introduction to theoretical neurobiology. Vol.1: Linear cable theory and dendritic structure*. Cambridge University Press, Cambridge, UK (1988).

[112] M. Ulbrich and P. Fromherz. Neuron-silicon self-excitation: A prototype of iono-electronics. *Adv. Mater.* 13 (2001), 344–347.

[113] S. Vassanelli and P. Fromherz. Neurons from rat brain coupled to transistors. *Appl. Phys. A* 65 (1997), 85–88.

[114] S. Vassanelli and P. Fromherz. Transistor records of excitable neurons from rat brain. *Appl. Phys. A* 66 (1998), 459–463.

[115] S. Vassanelli and P. Fromherz. Transistor probes local potassium conductances in the adhesion region of cultured rat hippocampal neurons. *J. Neurosci.* 19 (1999), 6767–6773.

[116] M. Voelker. Optimierung des Signal-Rausch-Verhältnisses bei Neurotransistoren. Diplomarbeit, Technische Universität München (2000).

[117] M. Voelker. personal communication (2003).

[118] F. Wallrapp. Halbleiter mit Hoch-DK-Beschichtung zur Stimulation von Nervenzellen. Diplomarbeit, Technische Universität München (2003).

[119] R. M. Warner and B. L. Grung. *MOSFET theory and design*. Oxford University Press (1999).

[120] R. Weis and P. Fromherz. Frequency dependent signal transfer in neuron transistors. *Phys. Rev. E* 55 (1997), 877–889.

[121] B. C. Wheeler, J. M. Corey, G. J. Brewer, and D. W. Branch. Microcontact printing for precise control of nerve cell growth in culture. *J. Biomech. Eng.* 121 (1999), 73–78.

[122] W. Winlow, A. V. Holden, and P. G. Haydon. Characterization of Lymnaea neurons by determination of action potential trajectories. *J. exp. Biol.* 99 (1982), 207–221.

[123] S. Wolf and R. N. Tauber. *Silicon processing for the VLSI era*. Lattice Press (1986).

[124] R. G. Wong, R. D. Hadley, S. B. Kater, and G. C. Hauser. Neurite outgrowth in molluscan organ and cell cultures: The role of conditioning factor(s). *J. Neurosci.* 1 (1981), 1008–1021.

[125] R. G. Wong, E. C. Martel, and S. B. Kater. Conditioning factor(s) produced by several molluscan species promote neurite outgrowth in cell culture. *J. exp. Biol.* 105 (1983), 389–393.

[126] C. Wyart, C. Ybert, L. Bourdieu, C. Herr, C. Prinz, and D. Chatenay. Constrained synaptic connectivity in functional mammalian neuronal networks grown on patterned surfaces. *J. Neurosci. Meth.* 117 (2002), 123–131.

[127] Y. N. Xia and G. M. Whitesides. Soft lithography. *Angew. Chem. Int. Edit.* 37 (1998), 551–575.

[128] J. S. Yuan and J. J. Liou. *Semiconductor device physics and simulation*. Plenum Press (1998).

[129] G. Zeck. Halbleiterchip mit einfachem biologischen neuronalen Netz. Ph.D. thesis, Technische Universität München (2001).

[130] G. Zeck and P. Fromherz. Noninvasive neuroelectronic interfacing with synaptically connected snail neurons immobilized on a semiconductor chip. *PNAS* 98 (2001), 10457–10462.

[131] G. Zeck and P. Fromherz. Repulsion and attraction by extracellular matrix protein in cell adhesion studied with nerve cells and lipid vesicles on silicon chips. *Langmuir* 19 (2003), 1580–1585.

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