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A 1 Gbit/s FIBRE OPTIC COMMUNICATIONS LINK

J. Gruber, M. Holz, P. Marten, R. Petschacher, P. Russer, E. Weidel

AEG-TELEFUNKEN, Forschungsinstitut Ulm

D-7900 Ulm, Fed. Rep. Germany

Abstract

An experimental 1 Gbit/s fibre optic communications link operating over a distance of 1.6 km is described. A silica based single-mode fibre is used as the transmission line, a directly modulated $Ga_xAl_{1-x}As$ DHS injection laser as the optical source and a silicon avalanche photodiode as the optical receiver. The transmitter contains a step recovery diode multiplexer which interleaves four parallel bit streams of 250 Mbit/s into a single 1 Gbit/s signal. The receiver contains circuits for signal waveform regeneration, for clock extraction and for demultiplexing the 1 Gbit/s signal into four parallel 250 Mbit/s channels. The electronic circuits were mainly realized using hybrid integrated thin film technology.

1. Introduction

Fibre optic communications systems based on single-mode waveguides allow the transmission of Gbit/s signals over a distance of several kilometres without repeaters [1, 2]. The best measured values of fibre attenuation are under 2 dB/km at 0.85 µm wavelength and under 0.5 dB/km at 1.3 µm wavelength [3]. At the wavelength of $Ga_xAl_{1-x}As$ lasers, the dispersion of single mode fibres equals 80 ps $nm^{-1}km^{-1}$, whereas for the dispersion minimum around 1.27 µm, a pulse broadening of approximately 4 ps $nm^{-1}km^{-1}$ has already been measured [3].

$Ga_xAl_{1-x}As$ injection lasers now exhibit lifetimes of several 10000 hours and can be modulated in some cases with up to 2 Gbits/s [4-8]. If injection lasers are biased slightly above threshold and then modulated, they oscillate in several longitudinal modes and have a spectral halfwidth of approximately 1.5 nm which causes a pulse broadening of under 0.5 ns over 4 km fibre length. Biasing the laser above threshold may yield a lower spectral width or even single mode emission [9], but it also enhances the photon noise due to the dc light pedestal [10, 11]. With a $Ga_xAl_{1-x}As$ laser as the optical transmitter and a monomode fibre as the transmission line experiments at 400 and 800 Mbit/s and at fibre lengths up to 7.3 km have been reported [12, 13]. The development of $In_{1-x}Ga_xAs_yP_{1-y}$ lasers in the 1.3 µm wavelength region is proceeding rapidly [14 - 16]. First experiments show the same modulation behaviour for $In_{1-x}Ga_xAs_yP_{1-x}$ injection lasers as for $Ga_xAl_{1-x}As$ injection lasers. Transmission experiments over a distance of 11 km at 400 and 800 Mbit/s have so far been reported [17]. Although a laser with a 1.8 nm spectral width has been used in these experiments, the pulse broadening over the whole fibre length was small enough to yield only a 0.5 dB power penalty.

For lower distance high bit rate transmission links graded index fibres are also of interest [18]. So far the transmission of a 1.12 Gbit/s signal over a 3 km fibre length has been reported

[19]. Since the coupling tolerances needed for monomode fibres are only about three to four times smaller than those for graded index fibres [20], there are no severe difficulties in the application of monomode fibres if a higher distance has to be bridged.

2. The experimental communications link setup

We have realized an experimental fibre optic communications link with a directly modulated $Ga_xAl_{1-x}As$ DHS injection laser as the optical source and a silicon avalanche photodiode as the optical receiver. The transmission line consists of 3 silica based single-mode fibres coupled by double excenter fibre connectors [21] and has a total length of 1.6 km and an attenuation of 6 dB/km. The direct binary code and return-to-zero (RZ) format are used for signal transmission. The direct binary code yields low bandwith and transmitter power requirements [22]. The digital circuits operate with negative logic signals.

Fig. 1 shows the basic circuit diagram of the transmission link. The transmitter contains a multiplexer which interleaves four parallel bit streams of 250 Mbit/s into a single 1 Gbit/s signal.

The signal is amplified in a driver stage to directly modulate the injection laser. In the receiver the electrical output signal of the avalanche photodiode is fed into a linear amplifier with an adjustable low-pass filter. The low-pass filter permits signal equalization dependent on the received signal waveform. At the filter output the PCM signal has non return-to-zero (NRZ) format. The baseline regenerator restores the PCM signal dc component that is lost in the ac coupled front end amplifier. Thereafter the PCM signal is regenerated in the clocked decision detector and divided into four parallel 250 Mbit/s channels by the demultiplexer. The nonlinear signal processing circuit differentiates and squares the PCM signal and by this way provides an output signal with a strong 1 GHz spectral line. The clock signals needed in the decision detector and in the demultiplexer are extracted from this signal in the phase locked loop (PLL).

3. The electronic circuits

The electronic circuits for the transmitter and receiver were mainly realized on alumina substrate in hybrid integrated thin film technology and have been partly described in earlier papers [23-25]. Hybrid integration allows small circuit dimensions and therefore minimization of parasitic inductors and capacitors. In some cases the resistors were realized in TaN or NiCr thin film technology. The other electronic components were used in chip form. The bottom surfaces of the thin film circuits are completely gold plated and used as ground plane. Signal carrying lines were realized as microstrip lines and terminated with their line impedance. Figs. 9 and 10 show photographs of two examples of the thin film circuits which will be discussed now.

Fig. 2 shows the circuit diagram of the step recovery diode multiplexer, consisting of four step recovery diode amplifiers paralleled at the output [25-27]. IN_i (i = 1...4) are the 250 Mbit/s signal inputs and are followed by transistor stages for input impedance matching and amplitude control[25]. The step recovery diode amplifiers consist of the Schottky diodes SD_{1i}, SD_{2i} and the step recovery diodes SRD_{1i}, SRD_{2i}. The application of two step recovery diodes instead of one allows sinusoidal pump signals in-

stead of narrow pulse shaped pump signals [27]. The step recovery diode amplifier acts as follows: The diode SRD_{2i} is charged by the positive half wave of a sine wave pump signal applied to P_i. The diode remains conducting in the reverse direction until the charge is removed, when it then switches off. A signal current across SD_{1i} increases the charge of SRD_{1i} and decreases the charge of SRD_{2i}, so that SRD_{2i} switches off earlier than SRD_{1i} and in the meantime an output current flows across SD_{2i}. The four sequentially clocked step recovery diode amplifiers act as a multiplexer. Fig. 9 shows the hybrid integrated multiplexer, containing the whole circuit of Fig. 2 on a single 1"x2" substrate.

Although a direct modulation of the injection laser with a step recovery diode multiplexer is possible, at 1 Gbit/s the inclusion of a laser driver with bipolar transistors is advantageous since it provides easy control of the modulation current amplitude [23, 25].

The receiver front end consists of several commercially available broad band amplifiers, a monolithic integrated 1 GHz bandwidth amplifier [28], and a simple LC low-pass T-filter. The front end noise bandwidth is reduced by the low-pass filter.

The maximum and minimum values s_{max} and s_{min} of the floating baseline front end output signal are detected in the baseline regenerator (Fig. 3) by the peak detectors consisting of D_1, C_1, R_1, and D_2, C_2, R_2. The operational amplifier V yields the average value $(s_{max} + s_{min})/2$ which serves as threshold for the differential amplifier T_2, T_3.

Fig. 4 shows the circuit diagram of the decision detector. The PCM signal applied to IN_1 is gated by the 1 GHz clock signal applied to IN_2. Since the clock pulses are positioned in the center of the input signal pulses, the output signal timing solely depends on the clock signal.

Fig. 5 shows the circuit diagram of the nonlinear signal processing circuit. The PCM signal is differentiated by the quarter wavelength line connected to the collector of T_1 and then squared in the full wave rectifier SD_1, SD_2. The circuit (Fig.10) was integrated on a 1"x1" alumine substrate using NiCr resistive layers. Fig. 11 shows the input and output signals of the nonlinear signal processing circuit. The output signal exhibits a strong 1 GHz spectral line which is needed to synchronize the phase locked loop.

In the clock regenerator circuit, a second order phase locked loop with a crystal oscillator is used. The PLL provides the 1 GHz clock signal for the decision circuit as well as the 500 and 250 MHz clock signals for the demultiplexer and for subsequent external signal processing. Demultiplexing is performed in two stages; first into two 500 Mbit/s signals and then into four 250 Mbit/s channels [24].

4. Operation of the transmission link

Any 250 Mbit/s source which provides an output signal with a standard ECL logic level can serve as the drive for one of the multiplexer input channels. Fig. 6a-d shows an example of four input signals delivered by pattern generators via F100K logic gates ($CH_1 \ldots CH_4$). In order to ensure correct operation of the

multiplexer, the input signals are shifted by 1 ns so that the pump pulses can discharge the step recovery diodes immediately after an input pulse occurs and thus generate the 1 Gbit/s output pulse stream (Fig. 6e).

The laser driver stage forms the modulation current waveform from the multiplexer output signal. Fig. 7b shows this modulation signal which consists of current pulses with a 400 ps halfwidth. The response of the laser diode (Fig. 7a) as directly detected by a photodiode does not show any significant pattern effect. A new type of stripe geometry laser [29] with a 205 mA threshold current and a spectral bandwidth of 1.5 nm was biased with I_B = 215 mA and modulated with a pulse amplitude of I_M = 20 mA. The laser output was directly coupled into the fibre through the fibre end surface. The same coupling arrangement was used between the fibre end and the avalanche photodiode.
The light output of the transmission line detected by the APD (BPW28, AEG-TELEFUNKEN) is shown in Fig. 12. Due to the low dispersion of the single-mode fibre, pulse broadening can hardly be observed. After passing the front end amplifier, the low-pass filter and the baseline regenerator, the signal, now in NRZ format, is fed to the decision detector which restores timing and pulse shape. This is demonstrated by the eye patterns at the input and the output of the decision circuit (Fig. 13). Finally, the regenerated 1 Gbit/s RZ signal (Fig. 8a) is divided into four 250 Mbit/s signals (Fig. 8b-e) by the demultiplexer. Like the corresponding input signals of the multiplexer (Fig. 6), the output channels (CH_1...CH_4) are also compatible with standard monolithic integrated ECL logic circuits.

5. Summary

While fibre optic transmission links with semiconductor lasers, single-mode fibres and avalanche photodiodes are capable of data transmission in the Gbit/s range over several kilometres, state of the art monolithic integrated logic circuits feature data sources which only reach up to the 300 Mbit/s range. The proposed communications link combines an optical transmission line working at a bit rate as high as 1 Gbit/s with multiplexer and demultiplexer circuits for four parallel 250 Mbit/s signals and thus provides easy interfacing to lower bit rate data channels. This also opens the opportunity to use lower bit rate measurement equipment for the investigation of a 1 Gbit/s transmission link.

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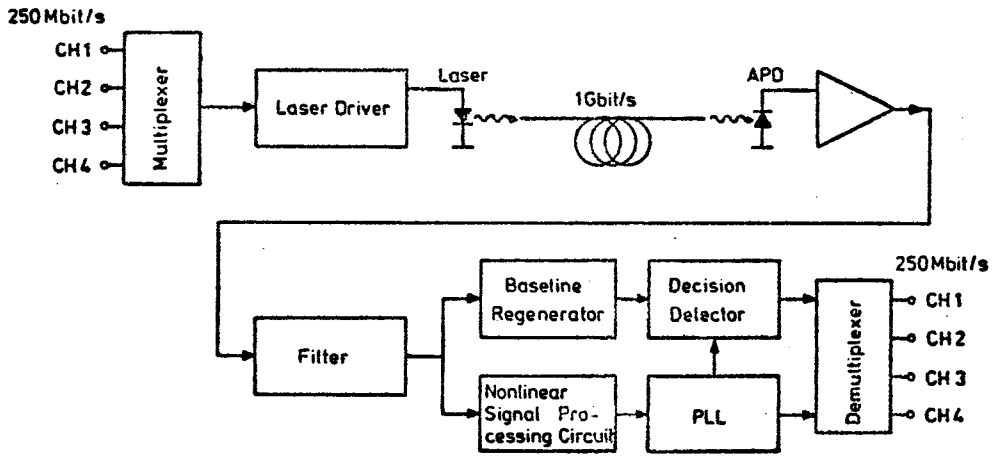


Fig. 1
Basic circuit diagram of the experimental transmission link

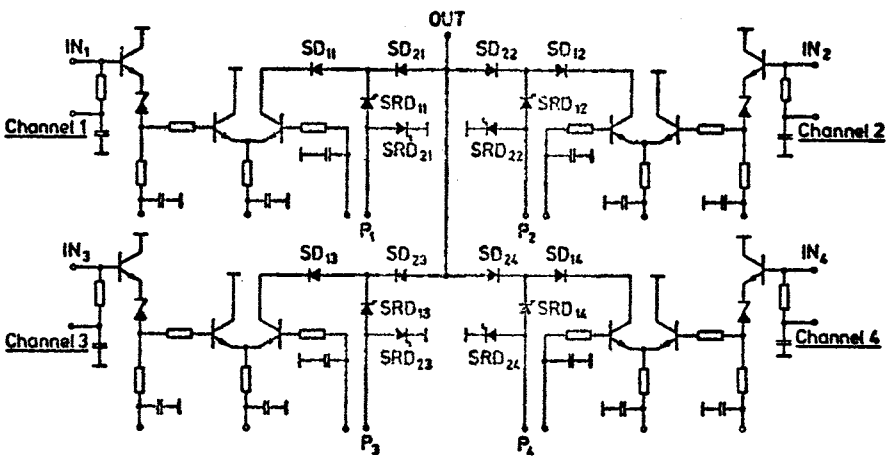


Fig. 2
Step recovery diode multiplexer

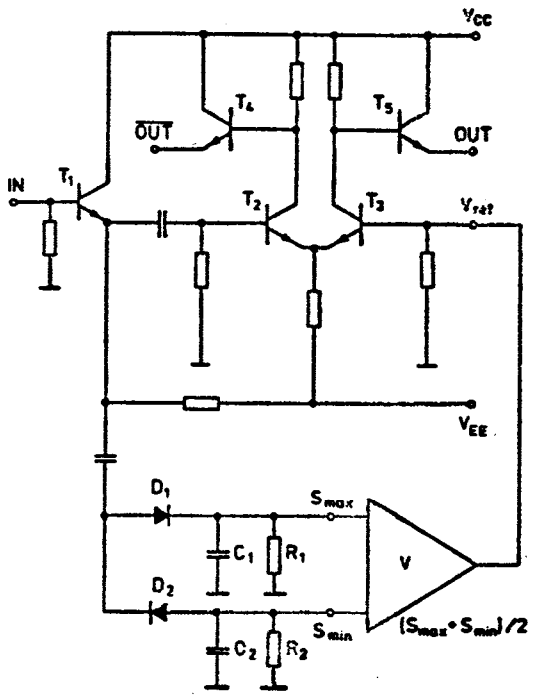


Fig. 3 Baseline regenerator

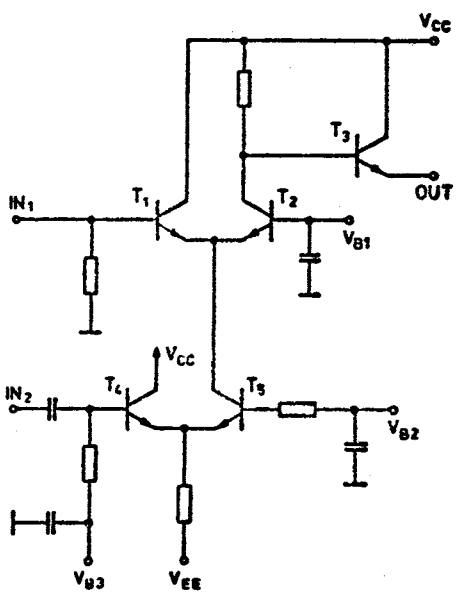


Fig. 4 Decision detector

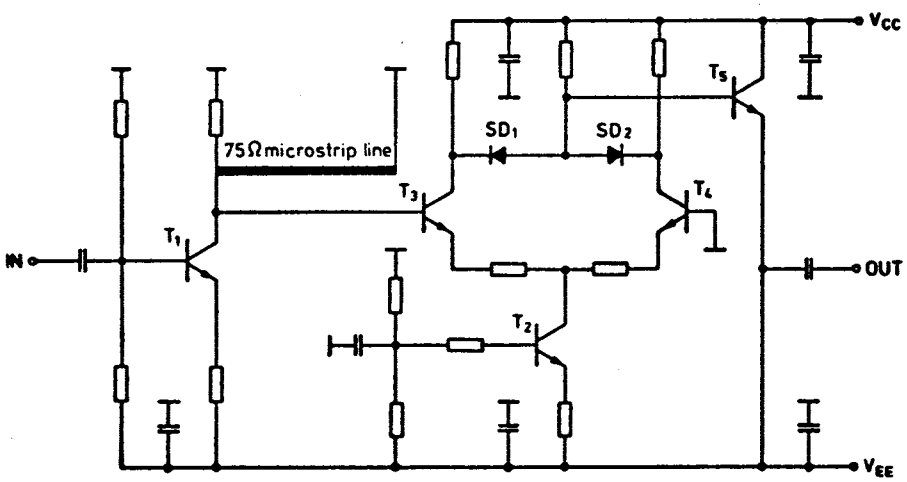


Fig. 5
Nonlinear signal processing circuit

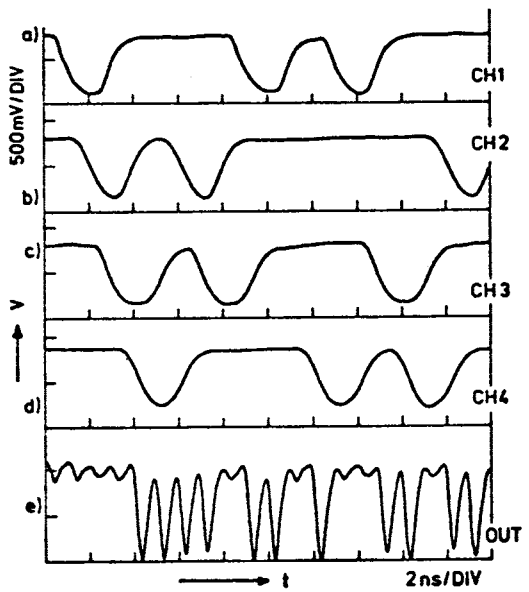


Fig. 6
Input (a-d) and output (e) signals of the multiplexer

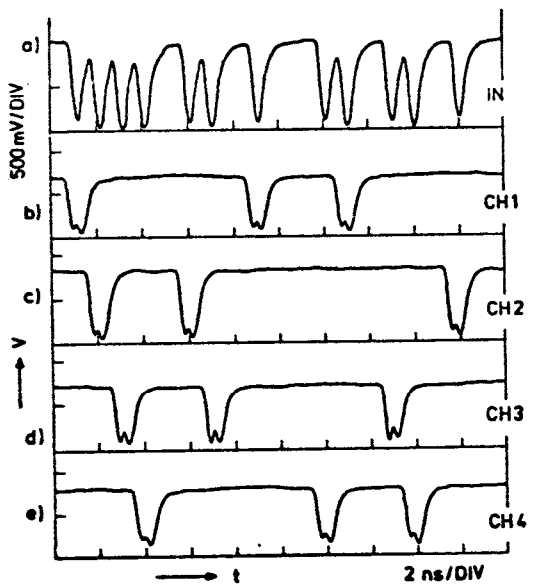


Fig. 8 Input (a) and output (b-e) signals of the demultiplexer

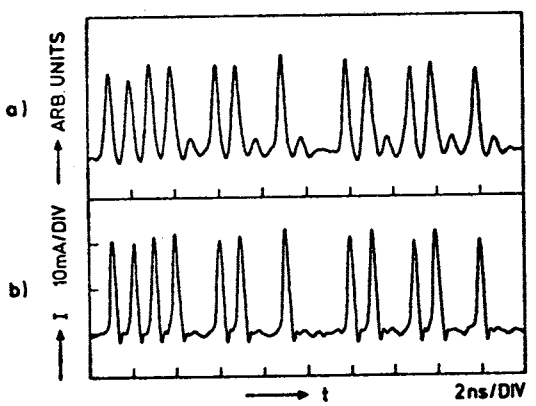


Fig. 7 Light output signal of the injection laser (a) 1 Gbit/s RZ signal output current waveform of the laser driver (b)

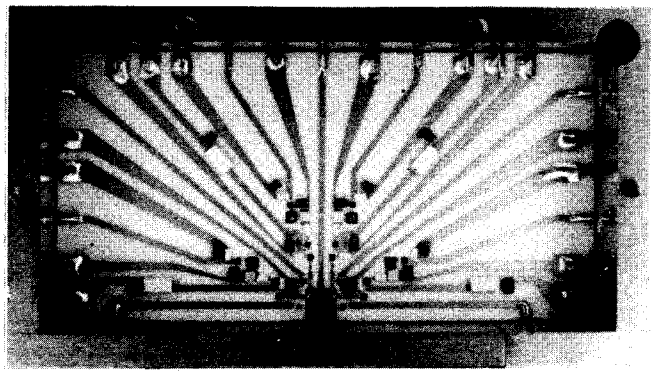


Fig. 9 Photograph of the multiplexer

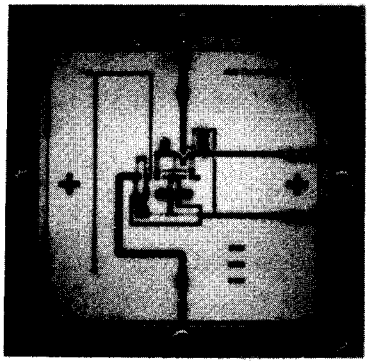


Fig. 10 Photograph of the nonlinear signal processing circuit

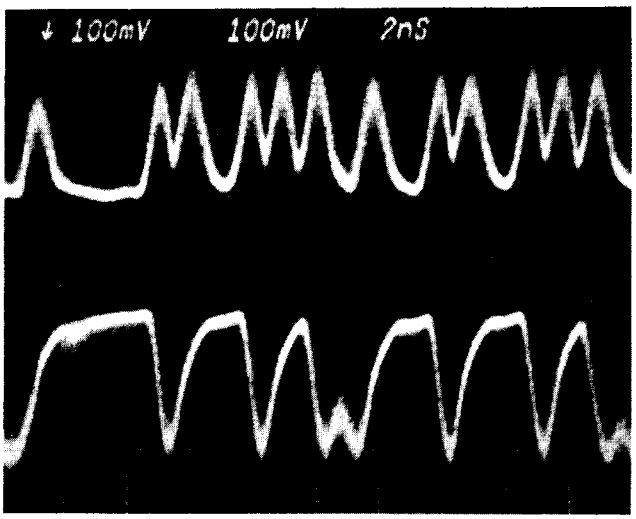


Fig. 11 Input (lower trace) and output (upper trace) signals of the nonlinear signal processing circuit

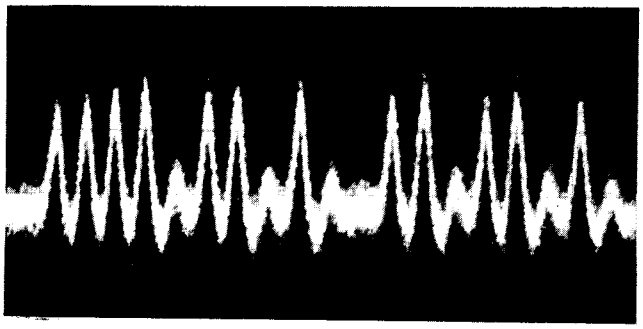
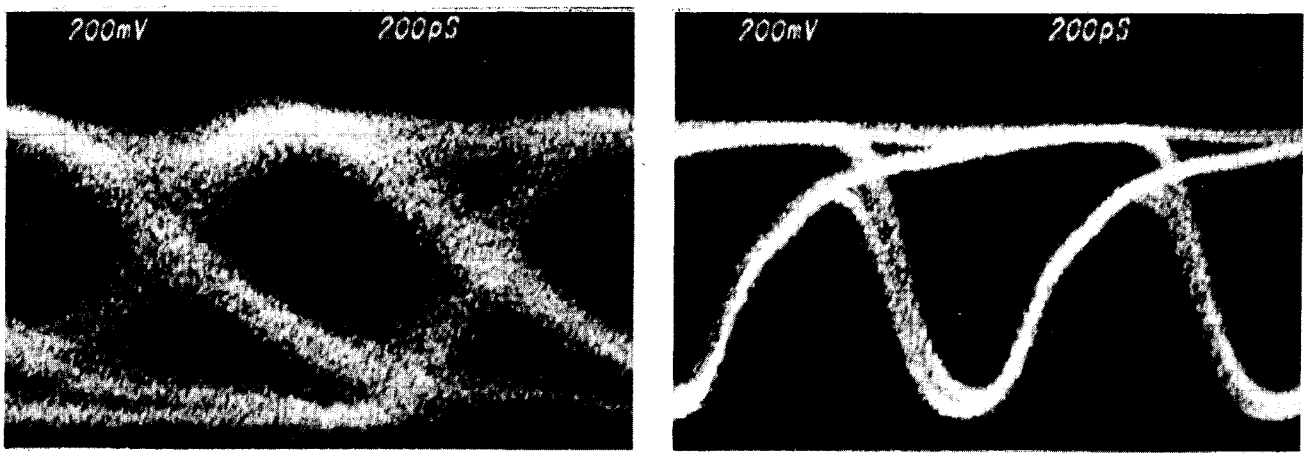


Fig. 12 Light signal detected by the APD at the end of the transmission line (2 ns/DIV)



a) b)

Fig. 13 Eye pattern at the input (a) and output (b) of the decision circuit