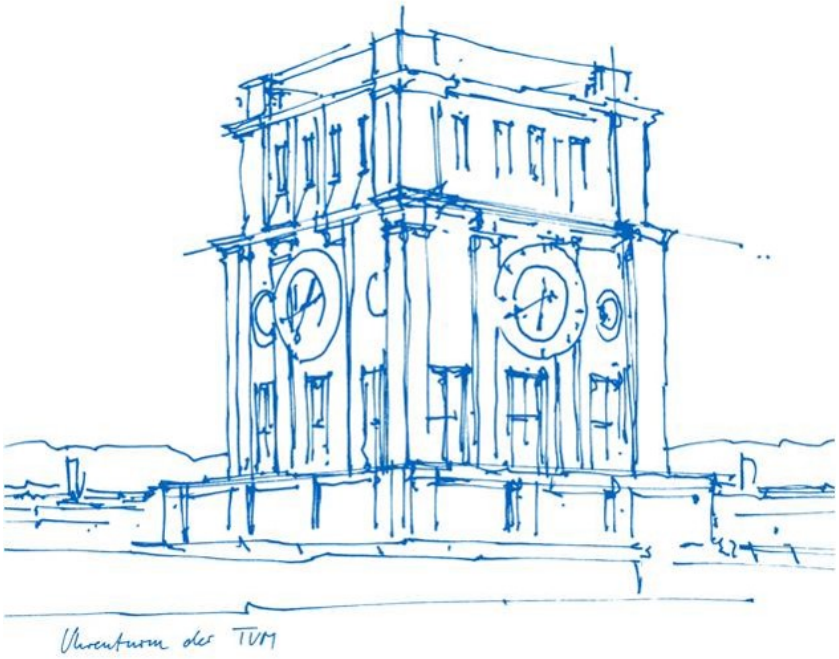
Highly Reliable Graphenic Carbon-Silicon Contacts

Max Stelzer



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"Things have to be faster and lower power, so it's ever-yet more challenging, but we have come up with some new innovations to scale things and keep things on track."

Mark Bohr, Intel

Abstract

To ensure the continued scaling of silicon-based complementary metal-oxide-semiconductor (CMOS) devices, a wide range of challenges had to be mastered throughout its history. Today, the dimensions in modern nanoscaled devices are so small that the contact resistance of the metal-semiconductor contacts significantly limits the performance for individual applications. The additional power dissipation can even lead to thermal degradation of the contact. This is not only relevant for CMOS but also for power devices, since very high temperatures during operation are common there. Many chip manufacturers are therefore returning to titanium silicide (TiSi) in state-of-the-art FinFETs and other devices, as TiSi establishes a very low Schottky barrier height and a low contact resistance to silicon (Si). However, despite its good thermal stability, it can diffuse into the active region of the device under a high current density stress pulse, such as an electrostatic discharge event.

In this work, a novel high performance metal-silicon contact established by synthetic graphenic carbon (GC) was demonstrated. A comparison was made to a TiSi-Si contact with a test vehicle based on the BAT15 Schottky diode from Infineon. The GC to silicon contact has the same low Schottky barrier height of 0.45 eV but could be lowered to 0.36 eV by the process conditions or after a pulse/bias stress. But GC-Si shows independent of the deposition method a much improved reliability against high current pulses. It was more than one billion times more stable against such an overstress than the conventionally used TiSi-Si junction.

The deposition of GC was demonstrated by two different methods directly on the substrate. The chemical vapor deposition (CVD) process used temperatures between 850 °C and 1000 °C and provided a conformal step coverage on all surfaces. A low electrical resistivity down to 1 mΩ cm parallel and 50 mΩ cm perpendicular to the surface was achieved. Furthermore, it was identified that the deposition of GC is possible in a sputter process at temperatures between 100 °C and 400 °C, which render it very attractive for contacts to silicon in modern CMOS devices with temperature restrictions. These films were also doped with nitrogen and this resulted in an improved stability and even lower resistivity of 8.4 mΩ cm compared to 16.9 mΩ cm for undoped sputtered carbon. The thickness of nitrogen-doped sputtered carbon could even be scaled down to 0.7 nm, while the reliability against high current pulses still exceeded that of TiSi-Si by at least a factor of ten million.

The properties render GC a promising alternative for conventional metal silicides and as a candidate for future highly reliable and temperature stable contacts with low contact resistance. But the use in many other applications is possible like as barrier/liner material, gate electrode or just as sacrificial layer.

Contents

Acronyms v

List of Symbols ix

List of Figures xvi

List of Tables xvii

1 Introduction 1
- 1.1 The History of the Transistor and the Integrated Circuit . . . 1
- 1.2 Silicided Junctions are State-of-the-Art . . . 4
- 1.3 Parasitic Resistance: A Limiter for Scaling . . . 9
- 1.4 The Search for a Ultra-Low Contact Resistance . . . 11
  - 1.4.1 Approaches to Realize a Low Contact Resistance . . . 12
  - 1.4.2 The Revival of Titanium Silicide . . . 12
- 1.5 Reliability of Metal-Semiconductor Contacts . . . 14
  - 1.5.1 The Electrostatic Discharge Event . . . 14
  - 1.5.2 Reliability Issues of Metal-Semiconductor Contacts . . . 15
- 1.6 Carbon as a New Contact Material to Silicon . . . 18
  - 1.6.1 The First Attempts with Amorphous and Diamond(-Like) Carbon . . . 20
  - 1.6.2 Graphene as Contact Material to Silicon . . . 21
  - 1.6.3 Graphenic Carbon: The Ideal Contact Material to Silicon? . . . 23
- 1.7 Objective of the Thesis . . . 24

2 Characterization Methods and Theoretical Background 25
- 2.1 Electrical Properties of Graphenic Carbon . . . 25
  - 2.1.1 Electrical Classification of Solids . . . 25
  - 2.1.2 sp^2 Hybridization of Carbon . . . 26
- 2.2 The Metal-Semiconductor Contact . . . 28
  - 2.2.1 Formation of the Ideal Schottky Barrier . . . 29
  - 2.2.2 Current Transport Mechanisms . . . 32
  - 2.2.3 Non-Ideal Schottky Barrier . . . 36
  - 2.2.4 Schottky Diode Test Vehicle . . . 37
- 2.3 Electrical Characterization Methods . . . 38
  - 2.3.1 DC Measurement Setup . . . 38
  - 2.3.2 Schottky Diode Parameter Extraction . . . 39
  - 2.3.3 High Current Pulse Setups . . . 41

2.3.4 Film Resistivity Measurements . . . 46
2.4 Non-Electrical Material Metrology of Graphenic Carbon . . . 47
2.4.1 Surface Analysis . . . 48
2.4.2 Raman Spectroscopy . . . 50
2.5 Finite Element Simulations . . . 51

3 Graphenic Carbon Deposition and Diode Fabrication 57
3.1 Substrate Preparation and Cleaning . . . 57
3.2 Chemical Vapor Deposition of Carbon . . . 59
3.2.1 Theoretical Considerations . . . 59
3.2.2 Process Description . . . 64
3.3 Physical Vapor Deposition of Carbon . . . 73
3.3.1 Theoretical Considerations . . . 73
3.3.2 Process Description . . . 76
3.4 Diode Fabrication Process . . . 84

4 Electrical Evaluation of Graphenic Carbon as Contact 89
4.1 DC Characteristics of TiSi-Si Diodes as a Reference . . . 89
4.2 DC Characteristics of CVD-C-Si Diodes . . . 90
4.3 DC Characteristics of SC-Si and CN-Si Diodes . . . 94
4.4 Additional Properties of GC Films . . . 98

5 Reliability Investigations of C-Si in Comparison to TiSi-Si 101
5.1 Electro-Thermal FEM Simulations . . . 102
5.2 Reliability of TiSi-Si BAT15 Diodes . . . 106
5.3 Reliability of CVD-C-Si Diodes . . . 107
5.3.1 Evaluation of Diodes with Carbon Deposited from C_2H_2 . . . 107
5.3.2 Evaluation of Diodes with Carbon Deposited from C_2H_4 . . . 108
5.3.3 Overview of the Pulse Endurance of CVD-C-Si Diodes . . . 113
5.4 Reliability of Sputtered Carbon-Silicon Diodes . . . 114
5.4.1 Preparation of the Setup . . . 114
5.4.2 Reliability Boost of Sputtered Carbon by Nitrogen-Doping . . . 115
5.4.3 Scalability of Nitrogen-Doped Carbon down to 0.7 nm . . . 119
5.4.4 Overview of the Pulse Endurance of SC-Si and CN-Si Diodes . . . 121

6 Summary and Outlook 123

Bibliography 125
Publications of the Author . . . 125
References . . . 125

Danksagung 155

Acronyms

a	Amorphous (crystal structure)
ac	Alternating Current
AFM	Atomic Force Microscope/Microscopy
Al	Aluminum
Ar	Argon
Au	Gold
BEOL	Back-End-Of-Line processing steps
C	Carbon
CCD	Charge-Coupled Device
CCP	Capacitively Coupled Plasma
CD	Critical Dimension
CGP	Contacted Gate Pitch
CMOS	Complementary Metal-Oxide-Semiconductor
CN	Nitrogen-doped sputtered Carbon
CNT	Carbon NanoTube
Co	Cobalt
CoSi	Cobalt Silicide
Cu	Copper
CVD	Chemical Vapor Deposition
D	Drain terminal of a FET
dc	Direct Current
DI	De-Ionized
DOS	Density Of States
DRAM	Dynamic Random Access Memory
DUT	Device Under Test
EOS	Electrical OverStress
epi	Epitaxial; refers to a epitaxially grown crystalline overlayer on a crystalline substrate.
ESD	ElectroStatic Discharge
EUV	Extreme UltraViolet
Fe	Iron

FEM	Finite Element Method
FEOL	Front-End-Of-Line processing steps
FET	Field-Effect Transistor
FinFET	Fin Field-Effect Transistor
GC	Graphenic Carbon
Ge	Germanium
H	Hydrogen (atomic)
H_2	Hydrogen (molecular)
HF	HydroFluoric acid
HOPG	Highly Oriented Pyrolytic Graphite
IC	Integrated Circuit
IPA	IsoPropyl Alcohol
IRDS	International Roadmap for Devices and Systems
ITRS	International Technology Roadmap for Semiconductors
MFC	Mass Flow Controller
MIGS	Metal-Induced Gap States
MIS	Metal-Insulator-Semiconductor or Metal-Insulator-Silicon
MOL	Middle-Of-Line processing steps
MOS	Metal-Oxid-Semiconductor
MOSFET	Metal-Oxid-Semiconductor Field-Effect Transistor
MS	Metal-Semiconductor or Metal-Silicon
N	Nitrogen (atomic)
N_2	Nitrogen (molecular)
Ni	Nickel
NiSi	Nickel Silicide
NMOS	A MOSFET where the current transfer between source and drain is by electron conduction (n-channel)
NTC	Negative Temperature Coefficient
O_2	Oxygen (molecular)
OTS	Ovonic Threshold Switching
PAH	Polycyclic Aromatic Hydrocarbon
PCB	Printed Circuit Board
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PFA	PerFluoroAlkoxy alkanes
PMOS	A MOSFET where the current transfer between source and drain is by hole conduction (p-channel)
poly	Polycrystalline

PTFE	PolyTetraFluoroEthylene
PtSi	Platinum Silicide
PVD	Physical Vapor Deposition
rf	Radio Frequency
S	Source terminal of a FET
SBH	Schottky Barrier Height
SC	Sputtered Carbon
SEM	Scanning Electron Microscope/Microscopy
Si	Silicon; unless otherwise specified, it is referred to monocrystalline silicon
SiGe	Silicon-Germanium
SMU	Source Measurment Unit
TEM	Transmission Electron Microscope or Microscopy
Ti	Titanium
TiC	Titanium Carbide
TiSi	Titanium Silicide
TLP	Tranmission Line Pulsing/Pulser
TSMC	Taiwan Semiconductor Manufacturing Company
W	Tungsten

List of Symbols

Symbol	Description	Unit
ε_0	Vacuum permittivity ($8.854\,187\,812\,8 \times 10^{-12}\,\mathrm{F/m}$)	F/m
ε_s	Semiconductor permittivity	
Γ	Reflection coefficient	
ϕ_B	Schottky barrier height	V, eV
ϕ_B0	Schottky barrier height without image-force lowering	V, eV
ϕ_m	Metal work function	V, eV
ϕ_s	Semiconductor work function	V, eV
ρ	Electrical resistivity	Ω·cm
ρ	Material density	$\mathrm{g/cm^3}$
ρ_c	Contact resistivity	$\Omega\cdot\mathrm{cm^2}$
σ	Electrical conductivity	S/m
τ	Residence time	s
μ	Drift mobility	$\mathrm{cm^2/Vs}$
μ_e	Electron mobility	$\mathrm{cm^2/Vs}$
χ_s	Electron affinity	V, eV
ΔG^0_f	Gibbs free energy of formation	s
A^{**}	Effective Richardson constant	$\mathrm{A/cm^2\cdot K^2}$
C	Capacitance	F, $\mathrm{F/cm^2}$
C_J	Junction or depletion-layer capacitance per area	$\mathrm{F/cm^2}$
C_P	Heat capacity	J/kg·K
e	Elementary electric charge ($1.602\,176\,634 \times 10^{-19}\,\mathrm{C}$)	C
E	Electric field	V/cm
E_C	Bottom edge of the conduction band	eV
E_F	Fermi level	eV
$E_\mathrm{F,m}$	Metal Fermi level	eV
$E_\mathrm{F,s}$	Semiconductor Fermi level	eV
E_g	Band gap energy	eV
E_V	Top edge of the valence band	eV
h	Planck constant	eVs, Js
$\hbar$	Reduced Planck constant ($\hbar = \frac{h}{2\pi}$)	eVs, Js

Symbol	Description	Unit
H	Heat generation per volume	$\mathrm{W/cm^3}$
I	Electric current	A
I_{DUT}	Current through the device under test or load	Ω
J	Electric current density	$\mathrm{A/cm^2}$
J_0	Saturation current density	$\mathrm{A/cm^2}$
k	Relative dielectric constant	
k	Thermal conductivity	W/m·K
k_{B}	Boltzmann constant ($1.380\,649 \times 10^{-23}\,\mathrm{J/K}$)	J/K
L	Inductance	H, $\mathrm{H/cm^2}$
L_{c}	Contact length	nm
L_{g}	Physical gate length	nm
m_0	Electron rest mass	kg
m^*	Effective mass	kg
m_{e}^*	Electron effective mass	kg
m_{h}^*	Hole effective mass	kg
n	Ideality factor	
n	Free electron concentration	$\mathrm{cm^{-3}}$
n_{ext}	Extrinsic charge carrier concentration	$\mathrm{cm^{-3}}$
n_{i}	Intrinsic charge carrier concentration	$\mathrm{cm^{-3}}$
N_{A}	Acceptor impurity concentration	$\mathrm{cm^{-3}}$
N_{C}	Effective density of states in the conduction band	$\mathrm{cm^{-3}}$
N_{D}	Donor impurity concentration	$\mathrm{cm^{-3}}$
p	Pressure	mbar
p	Free hole concentration	$\mathrm{cm^{-3}}$
P	Electrical power	W
q	Elementary electric charge ($q = e$) or absolute charge value	C
Q	Volumetric flow rate	sccm
R_{c}	Contact resistance	Ω, $\Omega\cdot\mathrm{cm^2}$
R_{ch}	Channel on-resistance of an field-effect transistor	Ω
R_{dev}	Total device on-resistance	Ω
R_{par}	Parasitic resistance of a field-effect transistor	Ω
$R_{\mathrm{s/d}}$	Source/drain resistance of a field-effect transistor	Ω

Symbol	Description	Unit
R_s	Series resistance (area normalized)	Ω, $\Omega \cdot cm^2$
R_s	Sheet resistance	$\Omega/\square$
S_q	Areal root-mean-square surface roughness	nm
t	Film thickness	nm
t	Time	s
T	Temperature	°C, K
V	Volume	cm^3
V_{DUT}	Voltage applied to the device under test or load	Ω
V	Applied voltage	V
V_{bi}	Built-in potential at equilibrium	V
V_f	Forward bias	V
V_n	Fermi potential from the conduction-band edge in n-type semiconductor	V
V_p	Fermi potential from the valence-band edge in p-type semiconductor	V
V_r	Reverse bias	V
W	Depletion width	cm
Z_0	Impedance of the transmission line	Ω
Z_{DUT}	Impedance of the device under test or the load	Ω

List of Figures

1.1 Evolution of the transistor technology node and transistor density per chip . . . 3
1.2 Schematic salicide process sequence and current path in the transistor 7
1.3 Comparison of the volumetric changes during the silicide formation . 8
1.4 Evolution of different transistor dimensions and of the parasitic S/D resistance . . . 10
1.5 Comparison of the contributors to the total resistance of the transistor for different technology nodes and schematic representation of a FinFET. . . . 11
1.6 Schematic current path in a FinFET . . . 11
1.7 Barrier height and contact resistivity at different annealing temperatures of TiSi on n-type Si . . . 13
1.8 Degradation of a TiSi-Si contact under current-induced stress . . . 16
1.9 A schematic cross-section of a TiSi-Si contact with localized grooving 17
1.10 Lattice structure of different carbon allotropes . . . 18
1.11 Ternary phase diagram of carbon allotropes . . . 19
1.12 Schematic representation of a graphenic carbon-silicon contact . . . 23

2.1 Typical density of states and band diagram of solids . . . 26
2.2 Schematic illustrations of hybridized orbitals of carbon and band diagram of different carbon allotropes . . . 27
2.3 Energy-band diagrams of a metal-semiconductor systems . . . 29
2.4 Energy-band diagrams of a metal-semiconductor contact under different biasing conditions . . . 31
2.5 Energy-band diagrams of a metal-semiconductor contact with barrier lowering at different biasing conditions . . . 32
2.6 Transport processes in a forward biased Schottky diode . . . 33
2.7 Schematic J-V curves according to the thermionic emission theory . . 34
2.8 Energy-band diagram of a metal to highly doped n-type semiconductor contact . . . 35
2.9 Energy-band diagram with interface region . . . 36
2.10 Schematic cross-section of a BAT15 diode and top view of the diode without metallization . . . 38
2.11 Measurement setup to characterize the Schottky diodes . . . 39
2.12 Diagrams for the extraction of diode parameters according to Cheung's method and using Lambert W function . . . 40
2.13 Schematic overview of the used dc and pulsed mode measurement setup 42

2.14 Measured pulse waveforms . . . 44
2.15 LTspice schematic of the pulse measurement setup and simulated current and voltage waveforms . . . 45
2.16 Four-point probe resistivity measurement setup . . . 47
2.17 Schematic illustration of the working principle of an AFM . . . 49
2.18 Thickness of a GC film measured with an AFM . . . 49
2.19 Schematic illustration of the Raman setup and typical spectra of carbon materials . . . 50
2.20 Geometric model of the BAT15 diode used in FEM simulations . . . 52
2.21 Measured vs. modeled current waveform . . . 53
2.22 Temperature-dependent characteristics for the thermal conductivity and heat capacity . . . 54
2.23 Carrier concentration, electron mobility and conductivity versus temperature . . . 55

3.1 Carbon-hydrogen ternary phase diagram . . . 60
3.2 Gibbs free energy of formation for some hydrocarbons and the gas phase evolution during the decomposition . . . 61
3.3 Schematic representation of the preferred orientation of GC deposited at different temperatures . . . 62
3.4 Simplified reaction scheme for the pyrolysis from ethylene . . . 63
3.5 Schematic overview of the used CVD equipments . . . 65
3.6 Photograph of the quartz tube with condensed PAHs . . . 66
3.7 Photograph of a GC-coated quartz shovel . . . 66
3.8 Deposition rates at different process parameters for C_2H_2 . . . 68
3.9 Surface roughness of a deposited GC film from C_2H_2 measured with an AFM . . . 69
3.10 AFM measurements of the surface roughness and height profile of GC films deposited from ethylene . . . 71
3.11 SEM images of formed soot particle . . . 71
3.12 Comparison of normalized Raman spectra of GC films deposited at different process conditions . . . 72
3.13 Carbon-nitrogen ternary phase diagram . . . 74
3.14 The structure zone model proposed by Thornton for thin films . . . 75
3.15 A schematic illustration of the used rf magnetron sputtering system . 77
3.16 Photographs of coated shutters . . . 78
3.17 Raman spectra of SC and CN films . . . 79
3.18 Comparison of surface profiles of sputtered carbon films measured with an AFM . . . 80
3.19 Electrical resistivity and sputter rate for different sputter process conditions . . . 82
3.20 Micrographs of patterns etched with KOH using CN as etching mask 83
3.21 Diode fabrication steps after the GC deposition . . . 85
3.22 Shadow mask positioning principles . . . 86

3.23 Capacitively coupled plasma etching setup 87
3.24 Micrographs of metallized BAT15 substrates before and after GC etching 88

4.1 *J-V* characteristics of a TiSi-Si and Ti-Si diode 90
4.2 Comparison of the dc characteristics of a CVD-C-Si diode (deposited from C_2H_2) with a TiSi-Si diode 91
4.3 The area-normalized series resistance of a CVD-C-Si diode as a function of the GC thickness 92
4.4 Comparison of the dc characteristics of CVD-C-Si diodes (deposited from C_2H_4) with a TiSi-Si diode 92
4.5 *J-V* curves of SC-Si diodes sputtered at different temperatures 94
4.6 *J-V* curves of CN-Si diodes sputtered at different Ar/N_2 ratios 95
4.7 Comparison of the dc characteristics of CN-Si diodes with different CN thicknesses 95
4.8 Comparison of the dc characteristics of a TiSi-Si and different types of carbon-silicon diodes 96
4.9 *J-V* curves that show the change of the barrier heights of a SC and a CN diode after an applied bias 97
4.10 Temperature-dependent relative electrical resistivity of different GC films 99
4.11 Change of the relative electric resistivity of SC and CN when exposed to atmosphere or water 100

5.1 Micrographs of failed C-Si diodes after being stressed with a single reverse current pulse 101
5.2 Temperature distribution in coupled transient electro-thermal simulations of the used Schottky contacts 102
5.3 SEM analysis of thinner or etched top metallization after being stress 104
5.4 FEM results of the temperatures in the diode as function of time for different C thicknesses 105
5.5 A schematic cross-section of a TiSi-Si Schottky diode where a high current pulse caused a diffusion of Ti or TiSi 106
5.6 Failure probability of BAT15 for different current densities and degradation of the *J-V* characteristics 107
5.7 Change in diode characteristics of a 58 nm CVD-C-Si diode deposited from C_2H_2 108
5.8 Comparison of the stress pulse endurance of TiSi-Si (BAT15) and CVD-C-Si diodes 110
5.9 SEM images of the top metallization of failed CVD-C-Si diodes . . . 111
5.10 Change in diode characteristics of a 37 nm CVD-C-Si diode deposited from C_2H_4 112
5.11 TLP current pulse, *J-V* curves of a stressed diode and threshold current density for CVD-C-Si diodes with different carbon thickness . 113

5.12 J-V curves of a stressed SC-Si and failure probability of diodes fabricated in a badly C-coated equipment 115
5.13 J-V curves of a pulse stressed CN-Si diode 116
5.14 Pulse endurance comparison of CN-Si with TiSi-Si and CVD-C-Si . . 117
5.15 Failure probability of CN-Si and CVD-C-Si diodes for a higher pulse width and J-V curves a pulse-stressed CN-Si diode 118
5.16 SEM and microscope images of the top metallization of failed CN-Si diodes 119
5.17 Pulse endurance comparison of TiSi-Si with CN-Si diodes of different CN thicknesses 120

List of Tables

1.1 Comparison of basic silicide properties 6

3.1 Evaluated CVD parameters for reliability tests of MS contacts 73
3.2 Evaluated sputter parameters for reliability tests of MS contacts . . . 84

4.1 Extracted TiSi-Si (BAT15) Schottky diode parameters 90
4.2 Extracted CVD-C-Si Schottky diode parameters 93
4.3 Extracted SC-Si and CN-Si Schottky diode parameters 98

5.1 Summary of the pulse endurance of CVD-C-Si diodes 114
5.2 Summary of the pulse endurance of SC-Si and CN-Si diodes 121

1 Introduction

Our way of life and even our culture is today dominated by information, which is why the 21st century is often referred to as the *information age*. But how can that term be understood? It can be used as a post-industrial label for a society that increasingly benefits from — and also becomes dependent on — new computer and communication technologies. In 2018, for example, more than half of the world's population already used the Internet [1]. This fact goes hand in hand with the availability of more high-performance and less expensive mobile devices such as smartphones.

This technological progress was largely made possible by one electronic component: the *transistor*. William Shockley already predicted it in wise foresight as a 'nerve cell' of the information age [2].

1.1 The History of the Transistor and the Integrated Circuit

A change in the electronics industry was initiated more than 70 years ago when the first transistor, a point-contact transistor with gold (Au) contacts on a germanium (Ge) substrate, was experimentally demonstrated in December 1947 by John Bardeen and Walter Brattain at the Bell Laboratories [2, 3]. Until these days, the switching or amplification of electric signals was realized by electron vacuum tubes, which are very power hungry, hardly scalable, packed in a fragile glass housing, and they need to heat up before use. The newly invented transistor was also hardly scalable and not suitable for a mass production. William Shockley recognized the drawbacks of the point-contact transistor, as he was also involved in its fabrication, and invented just one month later the p-n junction and the junction transistor. It is also known as bipolar transistor and was demonstrated experimentally at the Bell Labs in 1950 [2].

But, before a real change could take place, the individual components of an electrical circuit need to be manufactured on a single substrate and not just placed as discrete elements on a board next to each other. In 1958, Jack Kilby from Texas Instruments solved this problem by building an oscillator on a single germanium substrate made of a transistor, a capacitor and resistors, which are connected manually by gold wires [4]. The first integrated circuit (IC) was born, but still not suitable for a mass-production because of non-planar components and wiring. Only one year later Robert Noyce solved several problems of Kilby's concept and manufactured a real IC at Fairchild Semiconductors, which uses planar devices on a silicon (Si)

substrate. The aluminum interconnects were defined by a photolithography process, which made it possible to connect more components and build more complex integrated electronics with higher processing speed [2]. Even if the circuit was quite simple, it opened the path for a large-scale production at lower costs.

Until Noyce's demonstration, most of the inventions used Ge as semiconductor, but Si became the dominant material from that on, not only due to its electrical, but also due to its mechanical and thermal properties. And bear in mind that silicon can be obtained in large quantities at low costs, simply from sand. However, one of the biggest advantages is that Si forms a natural oxide, namely the silicon dioxide (SiO_2). The benefit of SiO_2 for the manufacturing of Si-based devices was on the one hand, that it acts as chemical diffusion barrier and on the other hand, that it electronically passivates the surface [5,6]. In 1960, the new Si/SiO_2 interface gave rise to a new transistor design — the metal-oxide-semiconductor field-effect transistor (MOSFET) [7].

The Beginning of Moore's Law

However, many more inventions were needed before we reached the information age as we know it today. Especially the microelectronic units with their complexity and cleverness enabled internet-of-things applications, self-driving/connected cars, cloud computing, artificial intelligence and, of course, the everywhere visible smartphones. This list can be extended very far, but Gordon Moore, a co-founder of Intel Corporation, laid the foundation for this rapid development back in 1965, when he made his famous prediction, that the number of components in a chip will roughly double every year with cost-efficiency [8]. His observation was previously based on a very limited amount of data, why he updated ten years later the doubling of components per chip to two years [9]. At that time, this statement was no longer just a prediction, but was already accepted by the semiconductor industry as *Moore's law*, as it was the guide and driver for new innovations. Today we know according to B. Krzanich, former CEO of Intel, "Moore's Law is fundamentally a law of economics" to sustain business [10].

The 'real' computer age has begun in fact when the manufacturer recognized that the metal-oxide-semiconductor (MOS) structures are smaller, simpler and easier to fabricate, despite their lower performance compared to bipolar devices. However, performance is a vague term — depending on the application — and can refer among others to the maximum switching speed, linearity and power efficiency. Intel manufactured the first commercially available microprocessor, the Intel 4004, based on PMOS transistors (a MOSFET with hole conduction) at a feature size of 10 µm. It was the beginning of an increasing demand for faster processing systems, higher efficiency and storage capacity and of course lower costs.

To meet these future performance goals, the industry continued to scale down all MOSFET dimensions according to the scaling methodology described by

R. Dennard *et al.* [11]. Fig. 1.1 clearly illustrates that manufacturers — to be precise Intel, since the data is based on their microprocessor units — have progressively reduced their structure sizes by 30 % every three years. A change is visible in the early 1990s as technology node cycles have shifted to a period of two years.

Conversely, the number of transistors per chip also increased considerably, for example the first microprocessor had only about 200 transistors per mm^2, whereas an Intel Core i7 processor in 2016 already had more than ten million transistors per mm^2 (see Fig. 1.1) [14]. So, Moore's law still works and will hopefully be valid for the next decades.

In order to achieve this progress, however, many technological challenges had to be mastered. A major game changer in the IC market was the industrial introduction of NMOS transistors (a MOSFET with electron conduction) with higher performance in the early 1980s, which were manufactured together with the p-channel transistors on the same wafer. As a result, active pull-up and pull-down were available on the same device. That is why memory and logic ICs were from then on almost exclusively

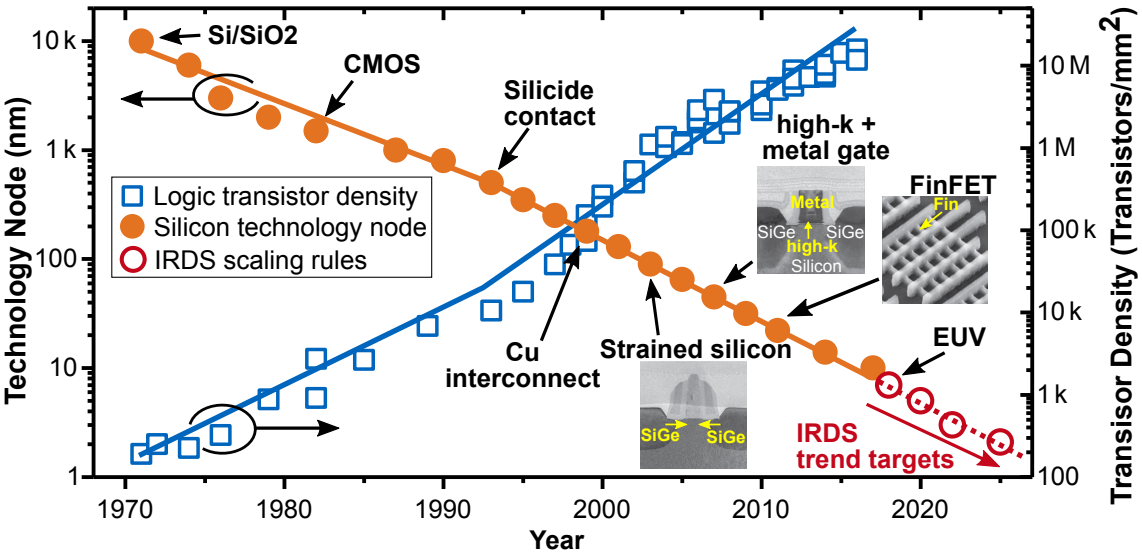

Figure 1.1: Evolution of the technology node of logic transistors (data taken from Ref. [12]), which is not necessarily equal to their physical minimum feature size. Some major milestones in the development in the MOSFETs technology are indicated [12, 13], which lead together with many other optimizations in the manufacturing process to a reduction of the node size by a factor of 0.7 every two years. Back in 1971, the feature size was 10 µm while in 2017 a node size of 10 nm was reached. Consequently, and according to Moore's law, an exponential increase in transistor density per chip of Intel's microprocessors in mass production can be observed (data taken from Ref. [14]). The International Roadmap for Devices and Systems (IRDS) pretends some ground rules for scaling of next transistor generations [15], which is visualized as a forecast. The shown lines are simply to guide the eyes. The inserted images are reprinted with permission from Ref. [12] © 2017 IEEE.

manufactured in the so-called complementary metal-oxide-semiconductor (CMOS) technology and bipolar devices became increasingly insignificant [6].

In the following years, the shrinking of feature sizes brought a new problem to the manufacturers' screens. This is the metal-semiconductor (MS) contact, since the reliability and performance of the previously used aluminum (Al) to silicon contact was no longer sufficient. As a result, the silicide source/drain (S/D) contact was introduced into mass production. Copper (Cu) interconnects and low-k dielectrics (k is the relative dielectric constant) were just the next big innovations in the next years to meet the performance requirements of smaller transistors [12, 13].

Moore's Law is Still Not Dead

The 90 nm node was the beginning of significant innovations in the manufacturing of CMOS devices. Through the newly introduced strain engineering, compression strain for NMOS and tensile strain for PMOS transistors, the charge carrier mobility in the channel was increased, thus enabling higher drive currents. At the 45 nm technology, however, there was a huge milestone in the development of CMOS devices because the reduction of the gate oxide thickness at the 90 nm and 65 nm node has stopped at a thickness of 1.2 nm [16]. This means that the insulator is only a few atomic layers thick and any further reduction would lead to even higher leakage currents. Therefore, SiO_2, used for more than 30 years, was replaced with a hafnium-based high-k gate dielectric with metal gate. The development time was quite huge and took approximately ten years until the first microprocessor was in production [12].

As planer bulk Si-MOSFET scaling was becoming increasingly challenging, the next major innovation — possibly the most revolutionary — was introduced with the 22 nm node: the non-planar FinFET [17]. It is a multi-gate (tri-gate) field-effect transistor (FET) with 3D geometries for a better electrostatic control of the channel. It became the standard for the following generations and today TSMC already manufactures at a 7 nm node in high-volume and ramps-up the usage of extreme ultraviolet (EUV) lithography in a 5 nm node [18]. However, the financial investments for equipment and development at this process node are very substantial, which is why GlobalFoundries has suspended any further work at this node [19].

1.2 Silicided Junctions are State-of-the-Art

In the early days of IC fabrication, as in Noyce's proposal, aluminum (Al) was the preferred interconnect and the contact material to silicon. It has a low electrical resistivity ($\sim 2.8\,\mu\Omega\,\mathrm{cm}$), a good processing capability and forms a low-resistance contact to n- and p-type silicon but less ideal for n-type Si [20, 21]. As the dimensions of the devices shrank progressively over the years, the S/D junctions became shallower, resulting in some difficulties. Post-metallization heat treatments at about

450 °C can lead to the so-called 'spiking' by a thermomigration of Si through Al, which finally leads to Al-filled pits capable to short-circuit the junction of the S/D diffusion region below the contact. This will render the device inoperable. In addition, misaligned metallization caused an undesired increase in the contact resistance [20,21] and Al can act as a p-type dopant in Si and creates an unwanted diode to an n-type contact.

The solution to these problems was the usage of a contact metal that reacts with Si to form a metallic compound called *silicide*. The main reason to use silcides was their low metal-like resistivity, enhanced thermal stability and diffusion barrier properties. Only transition and rare-earth metals are suitable for the formation of a 'metallic' silicide [22]. According to Refs. [21, 23–25], a silicide should fulfill some desired properties to be suitable for a usage in ICs. Of course, most of these attributes are also valid for all kind of metal-semiconductor contacts:

- Forms easily and uniformly;
- low resistivity;
- low contact resistivity to Si, which is correlated to a low Schottky barrier height;
- thermal, mechanical and electrical stable;
- producibility at low temperatures;
- low Si consumption;
- high corrosion and oxidation resistance;
- good adhesion to Si and dielectrics;
- high electromigration resistance;
- does not inject impurities or other point defects into the silicon and does not contaminate working apparatus;
- good lifetime;
- favorable dopant interaction;
- compatibility with other processing steps (lithography, passivation, dry/wet etching);
- controlled interface stress;
- easy to pattern;
- low surface roughness; and
- no reaction with top metallization or liner/diffusion barrier.

In 1965, a silicide, namely platinum silicide (PtSi), was used in Schottky diodes for the first time [26]. It made self-aligned contacts possible [20], but their application was very limited due to the high Schottky barrier to n-type Si, nevertheless, it was used in bipolar transistors [27].

Molybdenum and tungsten disilicide ($MoSi_2$ and WSi_2) were the first silicides used at poly-crystalline silicon (poly-Si) electrodes of a MOSFET transistor gate [28]. In

order to enable a further reduction of the transistor feature sizes at increased performance, the S/D series resistance had to be reduced. The search for a suitable silicide was mainly driven by a low film resistance. Titanium (Ti), cobalt (Co) and nickel (Ni) were the major candidates for this formation, which can also be used at the gate electrode. Tab. 1.1 shows some essential properties of the corresponding silicides — titanium disilicide ($TiSi_2$), cobalt disilicide ($CoSi_2$) and nickel monosilicide (NiSi). They are in the respective crystal phase with the lowest film resistivity (ρ). They can be integrated in a self-aligned process, a so-called 'salicide' process, without extra lithography, in which unreacted metal is subsequently etched away (see Fig. 1.2(a),(b)).

Table 1.1: Comparison of some basic properties or characteristics of the three most used silicides: Titanium disilicide ($TiSi_2$), cobalt disilicide ($CoSi_2$) and nickel monosilicide (NiSi). The C54 crystal phase is considered here for $TiSi_2$. The barrier height to p-Si can be estimated by subtracting the value to n-Si from the band gap of Si (1.12 eV). The data are taken from Ref. [25].

	Silicide		
Properties/characteristics	**C54-$TiSi_2$**	**$CoSi_2$**	**NiSi**
Thin film resistivity (µΩ cm)	15 – 25	15 – 20	10 – 20
Formation temperature (°C)	750 – 850	600 – 750	300 – 500
Melting temperature (°C)	1500	1326	992
Barrier height on n-Si (eV)	∼0.60	∼0.64	∼0.67

Titanium Silicide

However, after demonstrating the suitability of $TiSi_2$ for the use in MOSFETs [31], roughly further ten years of research were required before it was finally used in the early '90s in a mass production in Intel's 0.5 µm node at all transistor terminals. One of the main considerations in the selection of the silicide was clearly a low resistivity. The S/D areas were still very large at that time, which is why they have a large portion in the total resistance of the transistor. As shown schematically in Fig. 1.2(c), a significant part of the current flows laterally in the self-aligned silicide. As a consequence, it is necessary to reduce the sheet resistance here as much as possible.

The formation of $TiSi_2$ is not so simple because it involves several steps and has two crystal phases: C49 and C54, with the latter phase being the more desirable due to the lower resistivity. When Ti and Si are brought initially into contact, an approximately 2 nm thick amorphous (a) Ti/Si intermediate layer is formed at room temperature [32, 33]. This can even be called an amorphous titanium silicide (a-TiSi).

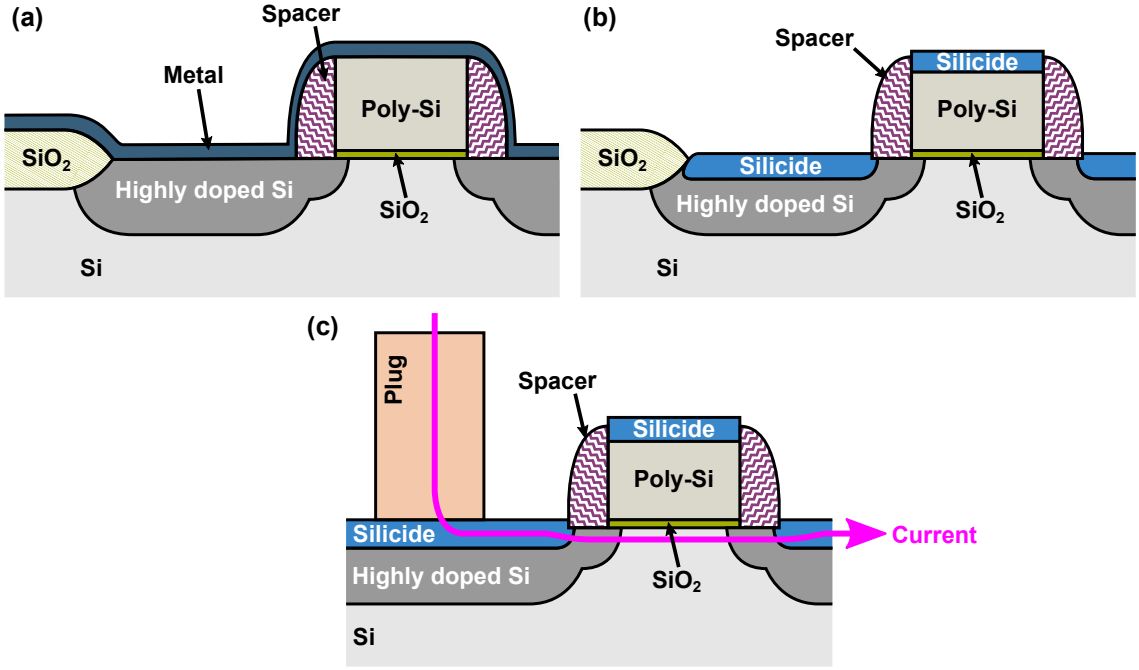

Figure 1.2: Schematic drawings of a MOSFET cross-section, which represent a simplified sequence of the salicide process in (a) and (b) and the current path in the final transistor in (c). (a) The salicide process starts with the deposition of a thin metal film over the entire wafer. The metal reacts with silicon to form the silicide at the whole S/D and gate area in a subsequent heat treatment. (b) The unreacted metal can be selectively etched away and the silicide is left in place. The silicide plays an important role in the lateral current distribution of the finished transistor with contact plug (c). (a) and (b) are adapted from Ref. [29] and (c) is adapted from Ref. [30].

Annealing at lower temperatures up to approximately 400 °C leads to increased material diffusion in which Ti and Si continuously intermix [33]. No crystalline structure is formed yet, but the area of the a-TiSi alloy is enlarged as silicon is consumed. The ratio Ti:Si is roughly 1:1 [32,34]. Nucleation only begins at temperatures above $\sim$ 450 °C and polycrystalline silicide islands are formed. The simultaneous presence of crystalline Ti_5Si_3, Ti_5Si_4, TiSi and C49-$TiSi_2$ beside the a-TiSi can be identified [33]. For simplicity's sake, the group of silicides formed can be abbreviated as $TiSi_x$. As a result of this nucleation, the film resistivity decreases [29, 35]. All the $TiSi_x$ phases are transformed into the metastable C49-$TiSi_2$ at a temperature of at least 600 °C. Still, the film resistivity of this silicide is much too high (70 µΩ cm - 100 µΩ cm [25]) to be used in transistors.

In order to significantly improve ρ, the C49 phase is completely converted into the desired low-ohmic C54 phase in the temperature range of typically 750 °C to 850 °C, resulting in an about four times lower value (see Tab. 1.1). The formation temperature is very restricted, since thermal agglomeration occurs at about 900 °C, resulting in a sharp increase in film resistance [29, 35]. Dopants and impurities can in addition affect the formation of $TiSi_2$ [36].

With the continuous scaling of the structure sizes of the CMOS transistors towards (deep-) submicron, the contact area became ever narrower. Nucleation into the C54 phase was not easy before, but as the line width approaches 0.25 µm, the conversion was not fully possible anymore [28, 37]. This made the fabrication increasingly uncontrollable and the higher resistance of the non-transformed C49 silicide had a negative influence on the speed of the IC.

Cobalt Silicide

Through process optimizations, C54-$TiSi_2$ could still be applied in the 0.18 µm node, but to eliminate the nucleation issue, industry already used a replacement at this node, which was cobalt disilicide ($CoSi_2$) [28,38]. This one was easier to fabricate as it had only one nucleation phase, could be formed at lower temperatures with good thermal stability and has a comparable thin film resistivity to $TiSi_2$. A drawback of the $CoSi_2$ is associated with the Si consumption. Of course, at the beginning the primary focus was on a low resistance, but the silicide depth became an important quantity for sub-100 nm structure sizes and the related shallow S/D junctions. As can be seen in Fig. 1.3, $CoSi_2$ consumes considerably more Si than $TiSi_2$ during its formation. The consumed Si thickness is 3.61 times as high as the original Co thickness, whereas $TiSi_2$ consumes only 2.22 times as much [39]. This in turn increases the risk of a higher leakage current through the reverse biased diode [40]. But also the formation of voids, a higher interface roughness and silicide spiking may limit its applications [24, 28].

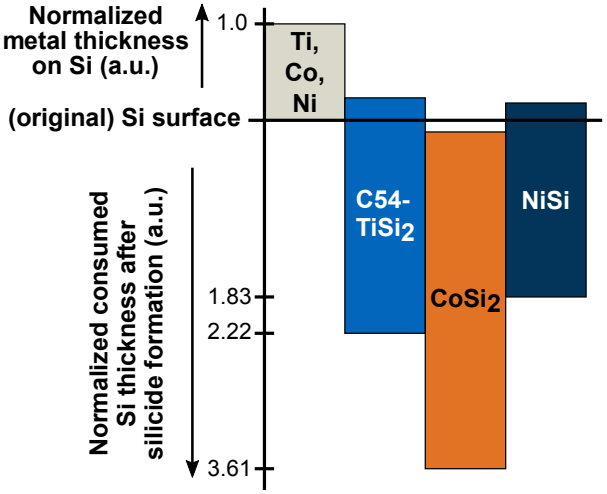

Figure 1.3: Comparison of the volumetric changes as seen from the original Si surface for the formation of C54-$TiSi_2$, $CoSi_2$, and NiSi. The initial metal thickness of Ti, Co and Ni is equal and normalized to unity. $CoSi_2$ is recessed below the original Si surface and consumes almost twice as much Si as NiSi. NiSi is slightly superior to $TiSi_2$ and both have a higher final silicide thickness than silicon was consumed. Adapted from Ref. [41] with data based on Ref. [39].

Nickel Silicide

In sub-100 nm CMOS devices, nickel monosilicide (NiSi), which is the crystal phase with the lowest film resistivity, gradually became the contact material of choice [42]. It has a low ρ, even at a low line width, requires a lower thermal budget for its formation (see Tab. 1.1) and consumes even less Si than the two other candidates (see Fig. 1.3). The lower formation temperature allowed to drop the back-end-of-line (BEOL) processing below 500 °C and even close to 400 °C, which changes the doping profile of the devices less [37]. So it's the perfect contact material?

The barrier height to n-Si is still acceptable low, but unfortunately the thermal stability associated with the low melting temperature is poor. Already an annealing at 700 °C can convert NiSi into the high-ohmic $NiSi_2$ or it agglomerates with negative effect on the resistance [28]. It was also reported, that NiSi heavily suffers from lateral Ni encroachment towards the channel region, as Ni has a very high diffusivity in Si, causing intolerable yield [37]. The solution was to add a small amount of platinum. The resulting NiPtSi has improved thermal stability and reduces the previously mentioned issues, but it leads to higher resistivity [37, 43].

1.3 Parasitic Resistance: A Limiter for Scaling

By 2019, global semiconductor revenues were nearly $ 420 billion [44] and a continuous scaling in these technologies in order to increase performance at higher transistor density and to reduce costs and power to enable 'green' devices is further needed. To ensure this, the International Roadmap for Devices and Systems (IRDS) — it is the successor of the International Technology Roadmap for Semiconductors (ITRS) [45] — writes or recommends time and process rules for prospective developments [15]. It should be mentioned that these data are not necessarily equal to the dimensions of the manufacturers but are nevertheless close to them and reflect the general trend.

Taking a closer look at these data, it becomes apparent that the transistor dimensions such as gate length (L_g), contact length (L_c) and contacted gate pitch (CGP), as shown in Fig. 1.4, have become continuously smaller and need to be further reduced in advanced technologies. The reduction of the gate length had almost saturated in planar MOSFETs and only the introduction of the FinFET led to new progress. Since the FinFET consists of a completely new design, there was not only a positive development with its introduction, e.g. the parasitic transistor resistance (R_{par}) almost doubled with the first FinFET generations. R_{par} is the extrinsic resistance part of the transistor and is related to the S/D areas. It must be minimized for high performance and in the ideal case only the intrinsic channel resistance (R_{ch}) remains. The influence of R_{par} on the performance of scaled MOSFETs is not new and was already addressed more than 30 years ago [47, 48].

Nevertheless, the CMOS devices must be further scaled to meet the requirements for future innovations. In order to achieve these goals, some near-time (until 2025) challenges are identified [15]. One of these challenges addresses the metal-

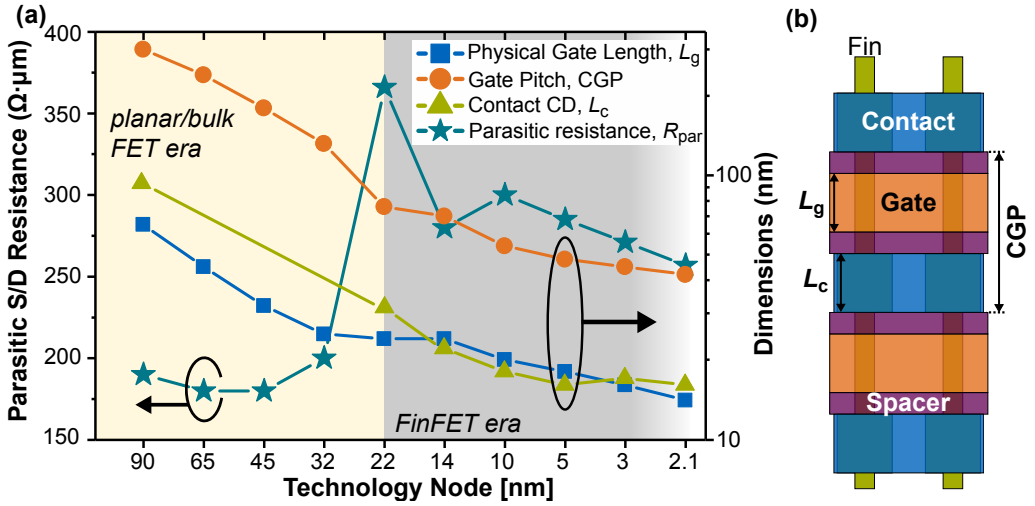

Figure 1.4: (a) The continuous downscaling of MOSFETs led to smaller and smaller dimensions, which can be seen especially in the physical gate length (L_g) and the contacted gate pitch (CGP). However, the parasitic resistance has not changed so much in the past and only a disadvantageous change occurred with the introduction of the FinFET in the 22 nm node. The new device structure resulted in almost two times higher values, since the contact critical dimension (CD) or contact length (L_c) became even smaller than L_g. The data is based on published values at IRDS 2018 [15], ITRS 2001 – 2015 [45] and Ref. [46]. (b) A schematic top view of a FinFET architecture, which shows some crucial dimensions. The fins in this illustration are enlarged at the S/D contact areas.

semiconductor (MS) contact at the source/drain (S/D) regions. Fig. 1.5(a) shows that the contact resistance (R_c) and the S/D resistance ($R_{s/d}$), which includes the accumulations layer, spreading and sheet resistance, become an increasing part of the device resistance (R_{dev}) when scaled from 14 nm to 5 nm. Together they give the parasitic component R_{par} and even get the dominating part. R_{dev} is simply expressed as a series of the channel resistance (R_{ch}) and R_{par}:

$$R_{dev} = R_{ch} + R_{par} = R_{ch} + R_c + R_{s/d} \tag{1.1}$$

A simplified visual representation is shown in Fig. 1.5(b). The reduction of the device sizes leads to a much greater influence on R_c and soon eclipses R_{ch}, which will heavily degrade the on-current.

The reason why the contact resistance becomes a bottleneck is the aggressive scaling itself. The silicide — getting thinner and thinner — is now fully covered with metal, as shown in Fig. 1.6 [30, 37]. So there is almost no lateral current component anymore, which is in contrast to the early days of silicided CMOS transistors (as previously shown in Fig. 1.2(c)). When selecting the silicide, the focus was previously on a low sheet resistivity, which helped to reduce the parasitic resistance. In contrast, today the emphasis is almost entirely on the reduction of contact resistance.

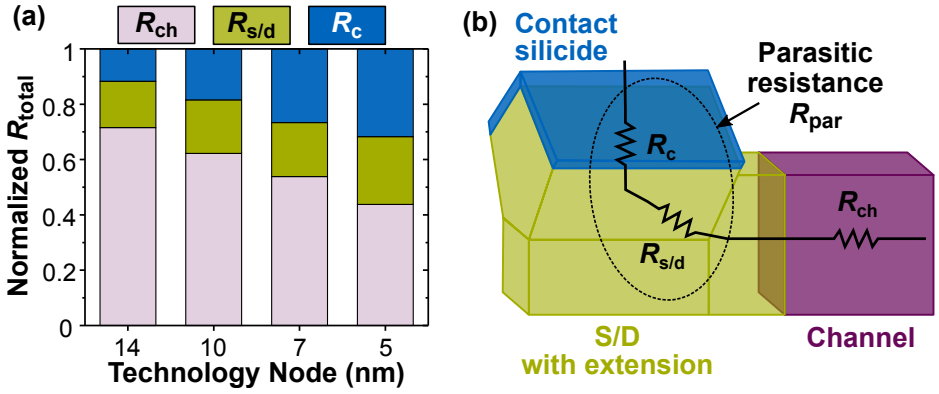

Figure 1.5: (a) Relative contribution of the contact resistance (R_c), S/D resistance ($R_{s/d}$), and channel resistance (R_{ch}) to the total device on-resistance (R_{dev}) of a transistor for different technology nodes, according to data from Ref. [49]. R_c and $R_{s/d}$ can be expressed together as parasitic resistance R_{par}. By the further downscaling, R_{par} gets a greater influence and will already be the dominating part in the 5 nm node. Especially the contact resistance will take up a fraction of more than 30 % of R_{dev}. (b) Schematic illustration of one side of a FinFET showing a simplified view on its resistance components. The contact geometry is enlarged by a diamond-shaped epi region [50].

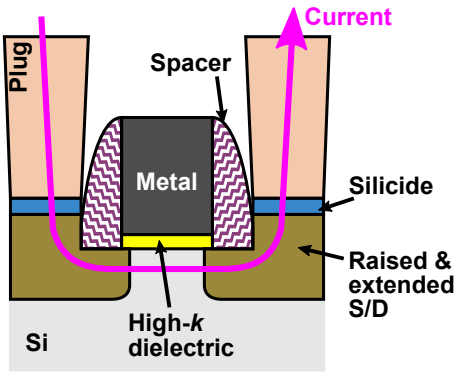

Figure 1.6: Schematic current path in a modern FinFET with a raised and extended S/D region. The dimensions, in particular the contact length, are already compressed to such an extent that the current in the silicide essentially has a negligible horizontal component compared to a traditional planar transistor. Therefore, the contact resistance of the silicide to silicon becomes the most important decision criterion. Adapted from Ref. [30].

1.4 The Search for a Ultra-Low Contact Resistance

The high impact of the contact resistance of the silicide at the S/D region might become a serious problem for future CMOS devices. It is in clear conflict with the goal of a high drive current and a low switching time at a low supply voltage to minimize the power dissipation at the highest possible packing density. The IRDS 2018 report [15] outlines that the conventionally used silicides are getting off-stream in maintaining the required performance goals. The main factors influencing contact

resistance, described in more detail in section 2.2, are the size of the contact area, the Schottky barrier height (SBH) and the silicon doping concentration. New interface materials with low SBH to Si or novel contact geometries are seen as the solution to this dilemma. The focus here is more on the interface material, but a general overview — also on geometry — is given in Ref. [50].

1.4.1 Approaches to Realize a Low Contact Resistance

The IRDS report highlights the metal-insulator-semiconductor (MIS) contact as a promising candidate for the reduction of ρ_c [15]. Addressed already 15 years ago [51], a very thin oxide layer ($\sim 1\,\text{nm}$) is inserted between the metal and silicon interface. In most MS contacts, the Fermi level tends to be pinned to the mid-band gap of silicon. The insulator prevents the so-called Fermi level pinning and, possibly, reduces the barrier height and the contact resistivity [52–54]. However, the use of a MIS contact has some significant weaknesses that discourage its use. The thin oxide represents a tunnel barrier and especially in the case of very high-doped silicon, such as in the source/drain area, it creates a greater resistance than the barrier in the case of pure MS contact [55]. In addition, the thermal stability of the MIS contact is very poor even at very mild annealing temperatures ($< 500\,°\text{C}$) [56, 57], which can lead to a degradation of the electrical properties.

In the past, just a single silicide was used for n- and p-type transistors. The use of two different silicides in the CMOS process — one having a low barrier for electrons and the other for holes — would be very advantageous to reduce the contact resistance. For this dual silicide option also rare earth metals are considered for the NMOS transistor. Unfortunately, as the name suggests, they are very rare and difficult to handle in the manufacturing process [50, 58].

1.4.2 The Revival of Titanium Silicide

It seems that TiSi plays an important role in solving the contact resistance challenge. In the following, TiSi is simply used as the generic term for all possible titanium silicides, unless the exact name is mentioned explicitly. TiSi provides a very low Schottky barrier height to Si, why it can be used in discrete zero-bias Schottky diode detectors and mixers [59], which for example are usable in Lidar and Radar applications. It was reported that TiSi-Si is even suitable for THz detection in integrated CMOS technology [60] and also the application in CMOS image sensors is conceived [61].

Ti-based contacts are intensively investigated for their potential usage in advanced CMOS nodes [30, 62–64]. Since the criteria for selecting the silicide have changed to a low ρ_c and the film resistivity is getting more negligible, it is no longer necessary to form the low-resistance C54-$TiSi_2$ phase. In a current investigation [30], as shown in Fig. 1.7, it was demonstrated that TiSi on n-type Si shows the lowest SBH at

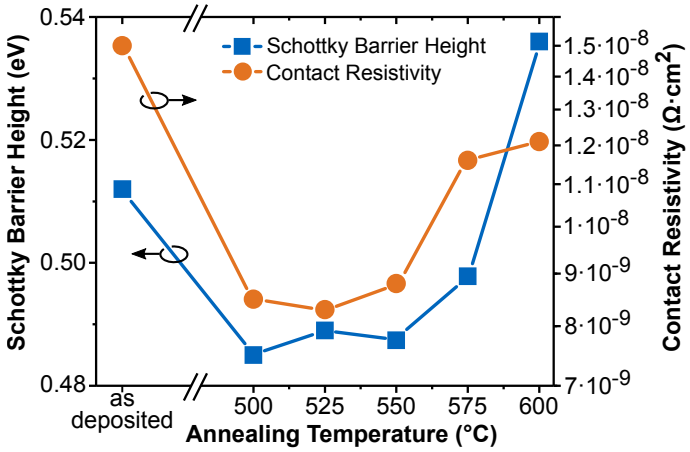

Figure 1.7: Schottky barrier height of TiSi on n-Si and contact resistivity of TiSi on n^+-Si at different annealing temperatures. The doping concentration at the highly doped silicon is $3 \times 10^{20}\,\mathrm{cm}^{-3}$. The contact resistivity is directly related to the barrier height. An annealing is necessary and the temperature should be $\leq 550\,°\mathrm{C}$ to achieve a low ϕ_B and consequently a low ρ_c. The data are taken from Ref. [30].

a post-metal annealing temperatures in the range of 500 °C to 550 °C and thus also the smallest ρ_c, as it nicely follows the trend of the barrier height. In this range TiSi is not yet completely crystallized and is still rather amorphous or first crystalline domains are already forming at the interface. Higher temperatures and the associated crystallization are counterproductive in achieving low ρ_c. The contact properties at annealing temperatures below $< 500\,°\mathrm{C}$ are not clearly identifiable from Fig. 1.7, but the behavior of the deposited contact seems less favorable.

Previous work in the early 1990s [35] showed that no annealing or such at lower temperatures resulted in a lower SBH, but this might be related to a different deposition method of Ti or TiSi. Interestingly, the studies show that the contact resistivity to p-Si is also favorable at annealing temperatures below 600 °C, despite the fact that the SBH is actually higher here.

Nevertheless, many companies — like IBM, GlobalFoundries, Applied Materials, UMC, and STMicroelectronics — participate in the investigation of Ti-based contacts for ultra-low contact resistivity for NMOS and PMOS [65–69]. Thanks to Chipworks it is also known that Intel uses TiSi in its 22 nm and 14 nm, Samsung in its 14 nm and TSMC in its 16 nm process [70]. Intel has even published that they use TiSi in the 10 nm node [71]. The chip reverse engineering of an Apple A12 processor revealed that TSMC also uses TiSi in their 7 nm process [72]. This obviously makes it a state-of-the-art contact material and it's assumed that the other manufacturers also use TiSi in their most advanced technology nodes.

1.5 Reliability of Metal-Semiconductor Contacts

According to M. Ohring and L. Kasprzak [73], *reliability* refers to the ability or probability to operate a product without failure for a certain time period under stated conditions. It reflects the physical performance of products during their length of life and serves as a benchmark of their future trustworthiness. Temperature, voltage and current stress during use accelerate the transition from reliable to failed states.

The metal-semiconductor contact, as an important component, poses a great challenge even during its processing in order to obtain the desired electrical properties. For example, the density of interface states at the silicide-silicon junction can lead to an enhanced noise level [74]. Production problems are followed by reliability issues during device operation. This is mainly due to interdiffusion processes between the metal and the semiconductor and in the worst case it can lead to a catastrophic short circuit at the junctions or merely to a variation in the barrier height or the contact resistance. As a consequence, a degradation of the contact may lead to a complete failure or alter the accuracy of the intended signal by changing its amplitude, time constant and shape [73].

1.5.1 The Electrostatic Discharge Event

This work puts special emphasis on the reliability of the metal-silicon contact when subjected to electrical stress. One form of it is the *electrostatic discharge* (ESD), which is the sudden process of charge balancing when two objects with different potential are brought into contact. The event is characterized as a fast rising pulse with short duration ($< 200\,\mathrm{ns}$) and a high voltage (up to several kilovolt) that creates a large current (up to several ampere) [73, 75]. This type of stress is a subclass of 'electrical overstress' (EOS), whereas latter has a longer duration. ESD is probably known to all people, although not as ESD, but rather as electric shock or a tiny lightning bolt caused by triboelectric charging when you wear the 'wrong' clothes and touch or approach something metallic.

If the electrical power of such an ESD event is injected to an IC, irreparable damage is possible mainly at the gate oxide, interconnects and junctions/contacts [76, 77]. An ESD discharge can occur already during fabrication, testing or just during the operation service by the user. Damage to a single component can lead to the malfunction of an entire system and ultimately to a customer return, which must be avoided. Such an event essentially leads to *Joule heating* — or simply called resistive heating. Under the assumption that the dissipated electrical power P per volume V (power density) in the semiconductor or conductor, neglecting other sources [78, 79], is fully transferred into heat. The heat generation per volume (H) for Joule heating is

$$H = \frac{P}{V} = J \cdot E. \tag{1.2}$$

Here, J is the electrical current density and E is the electrical field. Substituting *Ohm's law*

$$J = \sigma \cdot E = \frac{1}{\rho} \cdot E \tag{1.3}$$

to Eq. (1.2), it follows:

$$H = J^2 \cdot \frac{1}{\sigma} = J^2 \cdot \rho. \tag{1.4}$$

From here it is obvious that J is the main heat source, since it has a squared influence. The rise in temperature can be so enormous that copper (Cu) interconnects break down despite their good thermal conductivity [80]. It has been shown, when interconnects are stressed with a short high current density pulse, possible damage from Joule heating is more likely than by electromigration [81], which decomposes the metal by an 'electron wind'.

As a consequence, protection devices/circuits, on-chip and off-chip, are essential to be inserted to the design to protect an IC [76].

1.5.2 Reliability Issues of Metal-Semiconductor Contacts

Electro-thermal simulations of bulk MOSFETs [82, 83] and FinFETs [84] suggest that at a high J-pulse, approximately 10 to 15 times higher than the normal drive current density, temperatures of 1000 °C can be reached at the drain contact region. Gossner *et al.* [84] verified that the silicide, here NiSi, shows a strong degradation after the short ESD pulse.

The continued downsizing of the physical structure size and the increase in device complexity favors potential damage from high current pulse stress conditions with a short duration (also for protection devices [85]). Simulations suggest, according to data from the IRDS 2018 report [15], that the current density at the contact in a 7 nm FinFET can already reach 15 MA/cm^2 under normal operation conditions with the simplified assumption of a contact area of 18 nm × 32 nm and a current of 90 µA per fin. J can easily exceed this value by a magnitude during an ESD event. In addition, the contact resistance has a significant influence on the heat generation as it becomes the dominant parasitic resistance, like shown previously in Fig. 1.5.

Titanium silicide is known for the good thermal stability [86] and conductivity [87] and does have a higher melting temperature than $CoSi_2$ or Ni(Pt)Si, which also suggests better thermal stability than the two others. Furthermore, the diffusivity of the diffusion species (can be metal or silicon) at 500 °C is in the case of TiSi about two or four magnitudes lower compared to $CoSi_2$ and Ni(Pt)Si, respectively [37]. This fact and the small SBH and contact resistance to silicon renders TiSi a very attractive contact material.

TiSi-Si at Electrical Stress Conditions

Nevertheless, Banerjee *et al.* [88] have shown that a short (100 ns to 500 ns) high current pulse (likely to an ESD event) can indeed degrade a TiSi contact as a result of Joule heating. They analyzed tungsten (W) and aluminum (Al) vias, both with $TiSi_2$ as contact material to the underlying n^+-Si, like depicted in the transmission electron (TEM) cross-section in Fig. 1.8(a). A longer pulse duration and a higher J leads to a more severe degradation of the contact properties. Especially if the current density reaches a critical point, a single pulse can cause a failure. They calculated that the temperature might rise past 800 °C during such a pulse, whereas the impact on the via material was negligible.

More interesting is, however, a look at a cross-section of a failed contact structure. Fig. 1.8(b) indicates that the used $TiSi_2$-Si contact is seriously thermally degraded and Ti or TiSi diffused much further into the Si substrate. The 'damage' is roughly 100 nm deep, sufficient to short-circuit the shallow junctions of modern devices.

They also verified that the polarity of the ESD-like pulse has no influence on the degradation, which points out that the failure mechanism is thermally driven and not caused by the electrical field. Also, the use of a Si substrate with p-type shows the same reliability behavior.

Weisenberger *et al.* [89] already had similar findings in 1975. Short pulses (3 ns) or rf pulse trains (1 µs) can degrade a TiSi-Si contact of a Schottky diode. They clearly showed with an Auger sputter profile of a failed diode that Ti diffused further into

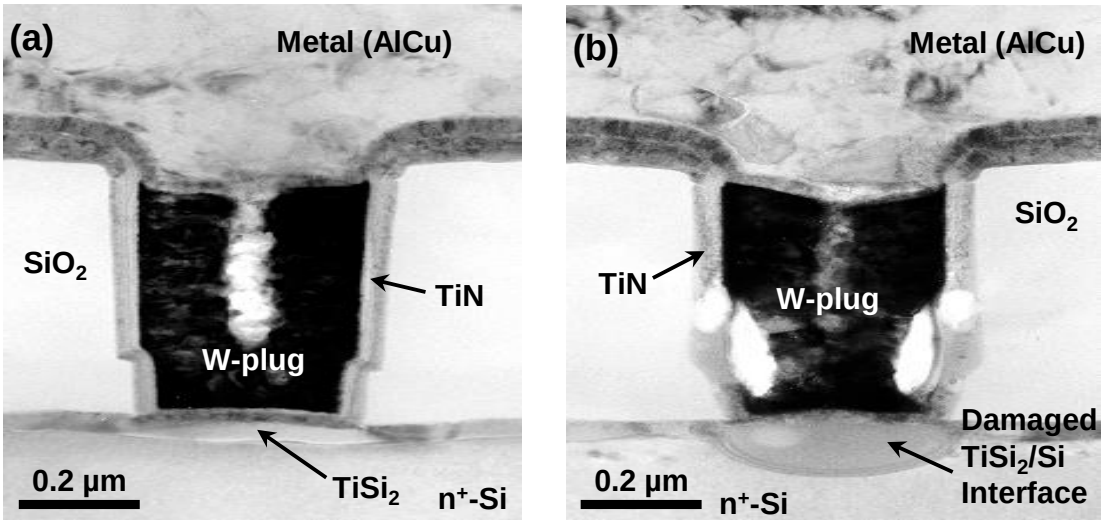

Figure 1.8: TEM images to analyze the contact degradation at the $TiSi_2$ to n^+-Si interface under short-pulse stresses in a tungsten (W) plug. (a) shows the cross-section of the unstressed via. (b) A short pulse with high current density (length and amplitude are not known) was applied to the via and led to Joule heating. The consequence was that interface reactions took place and Ti or TiSi diffused further into the silicon substrate. Reprinted with permission from Ref. [88] © 1997 IEEE.

the substrate as a result of resistive heating. This effect was originally associated with Al, where junction spiking was a major cause for malfunction [90].

In case of a dc stress, it was found that a current induced temperature rise to 465 °C was sufficient to degrade the TiSi-Si contact [91]. Higher current densities can fully destroy the contact by interdiffusion of Ti and Si. It was assumed that the high electric fields promote a degradation by electro-thermomigration.

Process-Related Reliability Concerns of TiSi-Si

Recent studies have revealed that TiSi is highly susceptible to a so-called grooving even at processing temperatures $\leq 600\,°C$. This phenomenon, as illustrated in Fig. 1.9, can occur on Si and especially on silicon-germanium (SiGe) [30, 92]. The latter is used in PMOS transistors. These results extend earlier investigations [93,94] where the appearance of encroachment was studied at higher temperatures. Once the TiSi starts to recrystallize into the C49-$TiSi_2$ phase, diffusion paths at the grain boundaries can promote rapid diffusion of Si at these locations, causing this agglomeration [30,94]. This can lead to a change in the electrical properties, but especially in 3D CMOS devices with heavily scaled dimensions even a slight grooving can lead to a total failure. It is very likely that also a local fluctuation of the SBH is caused [95], which in turn affects the electrical properties.

It cannot be excluded that this grooving also occurs under ESD conditions, since such temperatures in the drain area are easily reached at a high J, as simulations suggest [83]. In addition, it was shown that amorphous TiSi degrades more easily than crystalline TiSi under constant voltage stress. Unbonded Ti diffuses better, especially if it is in ionic form and in the influence of an electric field [96].

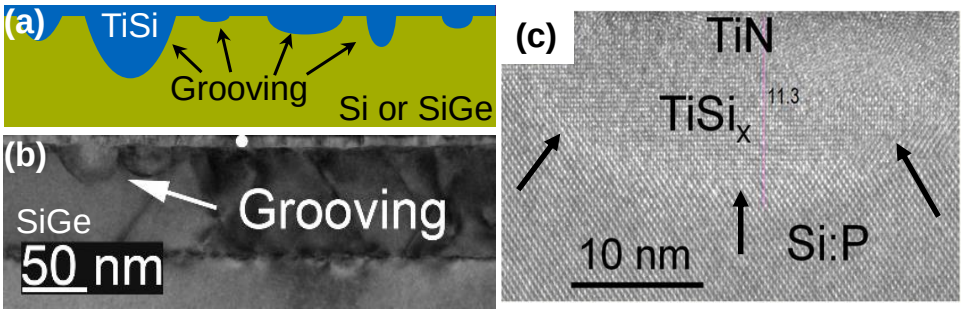

Figure 1.9: (a) A Schematic cross-section of a TiSi to Si or SiGe junction in which a localized grooving, because silicon was not consumed uniformly during crystallization, is depicted. (b) shows a TEM cross-section in which TiSi grooves are formed on a SiGe substrate already at an annealing temperature of 500 °C. In (c) is a TEM image of an uneven interface between TiSi and Si, formed at 600 °C, shown. The arrows should guide the eyes roughly to the boundary surface. (b) and (c) are reprinted with permission from Refs. [30, 92] © 2018, 2016 IEEE.

1.6 Carbon as a New Contact Material to Silicon

"Silicon will not realize its potential without the burden of development being carried out by carbon" [97]. When P. Atkins wrote these words, of course he meant that the organic human being (≙ carbon) is necessary for exploiting the full potential of silicon and the related devices. What he did not thought at that time is that this can be understood literally. Carbon (C) exists with different allotropes with outstanding characteristics and some can indeed be integrated into silicon devices, possibly exploiting the true potential of Si — with the help of humans, of course.

Carbon Exists in Various Forms

Carbon as the first group-IV element is located directly above Si in the periodic table, which makes an electrical compatibility of the two very likely. However, elemental C was known for a long time to exist basically in two forms: diamond and graphite. The difference between the two is essentially in the type of the bonding of individual C atoms. Diamond (see Fig. 1.10(a)) consists of a large mesh of sp^3-, whereas graphite (see Fig. 1.10(c)) has exclusively sp^2-hybridized atoms. Both have their unique electrical and mechanical properties [98–100].

Diamond forms a three-dimensional crystalline structure and is a wide band gap (5.5 eV) semiconductor and hence a good insulator. In contrast, graphite is referred to as semimetal because its conductivity lies between a conductor and a semiconductor with an electrical resistivity between 0.25 mΩ cm and 0.5 mΩ cm in-plane (along the individual sheets) and about 300 mΩ cm out-of-plane [100]. The main building block of graphite is the one-atom thick graphene (see Fig. 1.10(b)), which was ex-

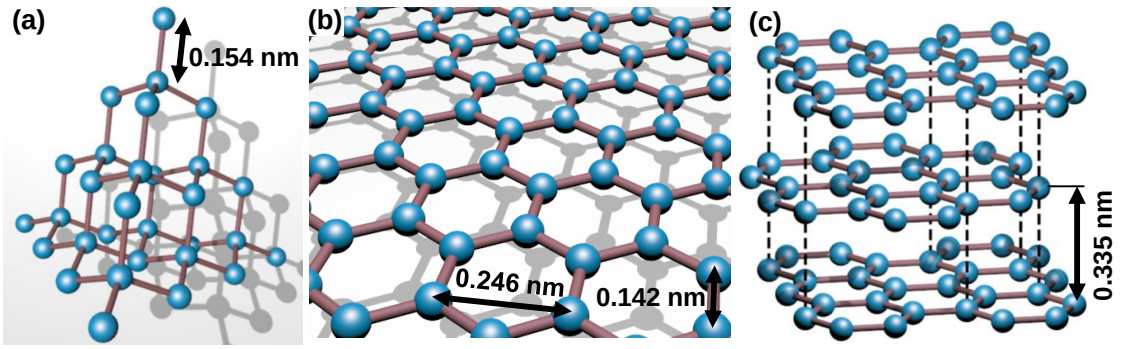

Figure 1.10: Lattice structure of different carbon allotropes. (a) Dimamond forms with the sp^3 bonded C atoms a tetrahedral with a bonding length of 1.54 Å. (b) The structure of a monolayer graphene is a two-dimensional hexagonal ("honeycomb") lattice formed by sp^2 bonded atoms. The bond length to each of the three covalent bonded neighbors is 1.42 Å. (c) Graphite is composed of stacked graphene layers with a spacing of 3.35 Å. The individual layers do not have any covalent bonds to each other and stick together purely by van der Waals force. The data for C-C bond lengths are taken from Ref. [100].

perimentally demonstrated the first time in 2004 by Novoselov and Geim [101]. If no defects occur, it is purely sp^2 bonded with an C atom having three neighbors. By 'loosely' stacking individual layers of graphene on top of each other, graphite is obtained. Therefore, graphene can be produced easily by the mechanical exfoliation of highly orientated pyrolytic graphite (HOPG).

The discovery of graphene was of great importance for the electronics industry in many fields of application: In photonics, bioelectronics, in sensor technology, for energy generation and storage and in (flexible) electronics for logic, analog and RF applications [102]. The European Union even started in 2011 a flagship project with a total funding of EUR 1 billion to promote research in this field [103]. The reason for this enthusiasm is mainly due to the extraordinary physical, electrical and mechanical properties. Graphene exceeds with a thermal conductivity of up to 5000 W/mK copper, a very good heat conductor, by about an order of magnitude [98] and of course also commonly used silicides [87]. In addition, it has a very high charge carrier mobility [104], shows a quantum Hall effect [105], a very high mechanical intrinsic strength [106], optical transparency [107], high thermal stability [108] and sublimates similar to graphite at temperatures above 4000 K [100, 109].

For the electronics industry, the first production of carbon nanotubes (CNTs) by Iijima in 1991 [110] was in addition of great significance. A CNT is like a sheet of graphene rolled up to a cylinder and is consequently purely sp^2 bonded. But it can even exceed the performance of graphene [98, 111].

In the meantime, other synthetic allotropes were discovered. C atoms cannot only form networks of pure sp^2 or sp^3 bonds, it is also possible to form materials containing both types, like the fullerenes observed in 1985 [112]. Heimann *et al.* [113] made a classification, as shown in Fig. 1.11, which defines different carbon forms based on their type and quantity of hybridization. It further shows that a sp^1 (or simply sp) hybridization is also possible.

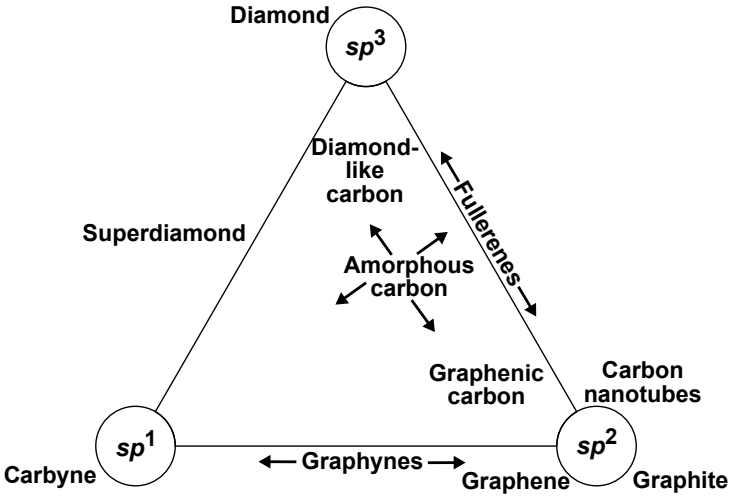

Figure 1.11: Ternary phase diagram to describe and classify different carbon allotropes based on their content of sp^1, sp^2 and sp^3 hybridized orbitals. Adapted from Ref. [113].

The fantastic characteristics of graphene render it a very attractive material for the integration to microelectronics. The focus of this work is on the metal-silicon contact and carbon/graphite with its Fermi level (or work function) at the mid-gap of silicon could give low barrier heights to n- and p-type silicon [114, 115]. The used carbon should be able to be integrated into the device process and meet the requirements for a silicide (or in general for the contact) listed in section 1.2. In the following is a short historical development of various carbon-silicon contacts given and whether they meet the requirements for a modern device.

1.6.1 The First Attempts with Amorphous and Diamond(-Like) Carbon

The presumably first carbon-silicon Schottky contacts were already produced at the end of the 1970s [116] — in the early years of the microchip. Amorphous carbon (a-C) was used, which was deposited by arc evaporation from graphite directly onto n-Si. a-C has an undefined ratio between sp^2 and sp^3 — also sp^1 is possible — bonded atoms, which are arranged in an irregular configuration [117, 118]. In addition, the contact was treated as a heterojunction, since the employed a-C probably has a non-negligible band gap and behaves as a semiconductor [119]. The resulting Schottky diode with Al on top of carbon shows rectifying properties, although apart from that rather worse forward conduction behavior, but this was not studied in detail. However, it has been shown that the carbon-silicon contact is photosensitive and that the resistivity of the carbon film can be improved by annealing about two to three orders of magnitudes down to 1 mΩ cm — clearly caused by a crystallization.

The fact that a photovoltage is generated during illumination was initially the driver that the C-Si heterojunction was further investigated for electronic applications after ten years. A polycrystalline diamond [120] or sp^3-rich diamond-like [121] film, which was deposited directly on silicon in a plasma-enhanced chemical vapor deposition (PECVD) process, was used there. The large band gap and the resulting large resistance, due to the high sp^3 fraction, render it mainly attractive only for photonics, as it is a transparent material.

Such a carbon film does not behave as a metal as it has a certain band gap. But it was demonstrated that it can be doped by ion implantation [122] or already during the deposition [123–125] to change its properties. Boron is used for p-type whereas nitrogen or phosphorus are used for n-type carbon.

It should be noticed, even if amorphous carbon is only partially suitable for high performance contacts, it recently has been shown that it is suitable as S/D contact in thin-film transistors because it is a very good barrier against chemicals and its thermal stability enables highly reliable devices [126].

Furthermore, the contact to silicon of fullerenes [127, 128] and CNTs [129] has been investigated. The main application might be in photonics as they have a band gap – CNTs exists also with metallic behavior [130]. However, since both allotropes have a circular or cylindrical surface, this leads to a non-ideal contact area to planar silicon and the integration of such a contact in other applications is rather unlikely.

1.6.2 Graphene as Contact Material to Silicon

Graphene could solve the problem because it can create a flat surface-to-surface contact, has no band gap [131] and the electron and hole concentration is equal at 300 K [132]. The superb properties mentioned in the previous section triggered a great rush in research and it was also very promising for the electronics industry because graphene was regarded as a wonder material. Despite the fact that a lot of money has already been invested, applications where the performance of graphene exceeds previous products at lower costs is restricted [133]. Also the use as the channel material MOS transistors poses several problems [134].

However, excellent on-chip inductors [135] can be manufactured and also the use as interconnect [136, 137], as highlighted by the IRDS 2018 Metrology report [138], is very promising, because it surpasses the properties of conventional materials such as copper in terms of electrical, thermal and reliability performance, especially in small dimensions. Beside its high *thermal stability*, it is also a distinguished *diffusion barrier* for common metals used in microelectronics [139] and Cu wires — still the primarily used interconnect — encapsulated by graphene show a significantly improved reliability [140].

Results of Graphene-Silicon Contacts in Literature

To connect device and interconnect, a good contact is needed. Di Bartolomeo [141] conducted an extensive review of graphene-semiconductor contacts, which helps to evaluate its potential. An essential prerequisite for achieving an ohmic contact is a *low SBH*, and a value around 0.4 eV is very likely for graphene/n-Si, even as low as 0.32 eV, but it should be noted that the extraction is prone to errors. Similar low values are found for highly oriented pyrolytic graphite (HOPG) on n-Si [142]. In addition, the barrier of graphene on p-Si may be less than 0.5 eV. The quality of the metal-semiconductor contact can be described by the so-called *ideality factor*, which is mainly deteriorated by recombination currents [114, 143]. A value of 1.1, close to the ideal value of unity, is possible with graphene and also the resulting diodes show high on/off-ratios.

If only these positive aspects are considered, graphene certainly appears to be a very promising candidate for contacts with silicon, as it enables high-performance ohmic contacts and can compete with the previously mentioned TiSi-Si contact. A closer look on the data in Ref. [141] shows that the measured SBHs can vary considerably and can approach values of 0.89 eV in the case of n-Si. Also, an ideality factor greater than two is often observed, which exceeds the theoretical boundary,

which indicates a large variation in the quality of the graphene sheet and non-ideal behavior of the interface [144].

Synthesis of Graphene

The reasons for poor performance can be manifold. The synthesis of graphene at first poses a considerable hurdle, as it affects the quality, purity, yield, scalability and cost of the final sheet. Raccichini *et al.* [145] and Novoselov *et al.* [102] qualified the most common production methods according to crystallite size (quality), scalability at reasonable costs and electrical mobility. Mechanical exfoliation [101], the method presented by Novoselov and Geim, undoubtedly produces graphene of high quality and performance for research and prototyping — a wafer-level production at low prices is hardly possible. Apart from this, several other methods have been proposed so far, such as liquid-phase exfoliation [146], which is very cost-efficient, but the quality and charge carrier mobility is low. The situation is similar for the chemical reduction of graphene oxide [147]. The sublimation of silicon carbide [148] is a wafer-scale method at low price and acceptable quality, but a transfer to other substrates is restricted. The growth of graphene by catalyst-assisted *chemical vapor deposition* (*CVD*) on metal substrates such as Cu or Ni [149] has been proposed as a promising approach with high quality and scalability. It even enables industrial-scale production, as recently demonstrated with an 30-inch sheet produced in a roll-by-roll process [150].

Drawbacks in the Integration of Graphene

Unfortunately, these methods usually require a transfer to the target substrate, whereby metallic or organic residues result in a deterioration of quality [151]. They can also contaminate the substrate, which in turn lead to a non-fulfillment of the desired electrical properties or function. Even a large roughness or the formation of wrinkles cannot be excluded [152]. Other synthesis methods that allow a transfer-free production of graphene [153, 154] are limited to SiO_2 (isolating) surfaces, preventing the direct formation of a graphene-silicon contact.

Furthermore, Graphene is a van der Waals material and forms only a negligible amount of covalent bonds to an underlying substrate or metallization above it, resulting in poor adhesion [155, 156]. This is a general problem of all defect-free 2D materials that have covalent bonds only in-plane and stick out-of-plane purely by van der Waals forces [157]. The consequence is that the sensitive metal-Si interface is not completely sealed, and exposure to the ambient atmosphere can create oxide traps, which in turn can lead to a long-term degradation of the electrical performance of the junction [158]. Also, the gap between graphene and substrate might be a diffusion path for the top metallization. Furthermore, the missing covalent bonds between the sheets in multi-layer graphene, similar to HOPG, results in an undesirable low interlayer conductivity of about 1500 times worse than in-plane [100].

1.6.3 Graphenic Carbon: The Ideal Contact Material to Silicon?

To really be able to integrate graphene as a contact material in a device, it must not only be possible to deposit it directly on insulators, but also on Si with covalent bonds to the substrate to ensure reliable operations. Recently, different approaches with conductive carbon at variable thickness directly deposited on Si have been investigated, mainly based on the *pyrolysis* of carbonaceous gases or solids [159–162]. The crystalline quality and morphology may well differ from ideal graphene and graphite, but covalent carbon-silicon bonds are formed due to the high temperature processing [163]. This lead to a good adhesion and a good electrical contact to the substrate, like shown in Fig. 1.12. This kind of carbon materials are called here, according to the nomenclature of Bianco *et al.* [164], *graphenic carbon* (GC) and is synonymous to the term graphitic carbon [165]. They belong to a broad class of solids with primarily sp^2 hybridized carbon atoms (see Fig. 1.11) and are based essentially on the graphite layer structure.

GC shows excellent mechanical and thermal properties, enabling the integration as membrane/window in x-ray detectors [166] or as heat spreader [167]. It is also very interesting for microelectronics, since it is electrically conductive, has a compatibility to high-k and silicon-based dielectrics, and a good CMOS processability [168]. The electrical resistivity of these GC films can be close to $1\,\mathrm{m\Omega\,cm}$, which equals the resistivity of n-type silicon at a doping concentration of roughly $8 \times 10^{19}\,\mathrm{cm^{-3}}$, and can be lowered to about $10\,\mu\Omega\,\mathrm{cm}$ by doping [168]. Applications include inter-

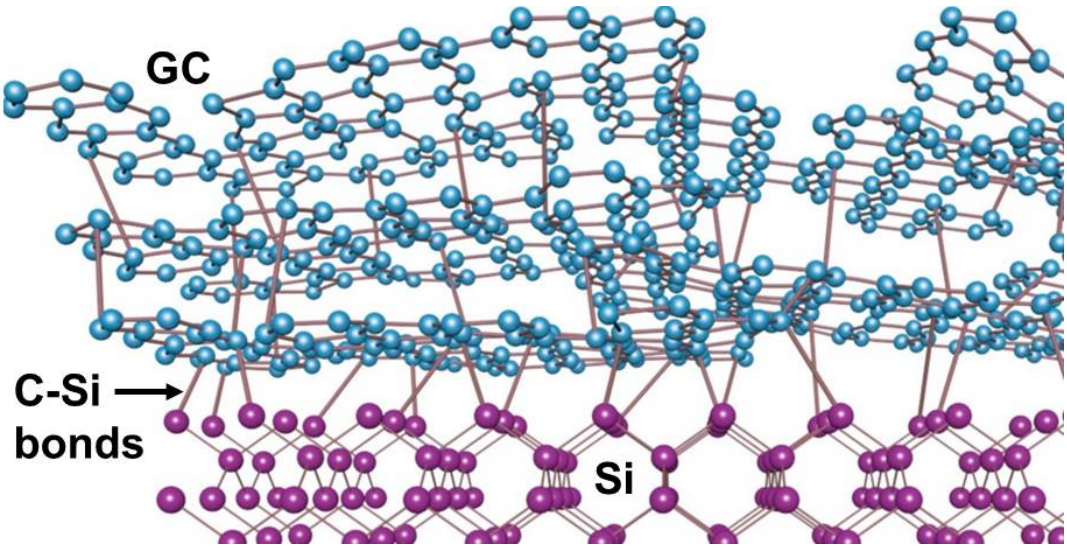

Figure 1.12: A schematic representation of a graphenic carbon to silicon contact (Si with (111)-surface). The individual GC sheets are not defect-free, thus not only sp^2 hybridization occurs and cross-links (bonds) between the stacked planes at lattice imperfections are formed. Covalent bonds between C and Si atoms are also formed, whereas the total number of interlayer bonds and defects shown here might differ from a real film.

connects and vias [169], gate electrodes [170], electrodes in metal-insulator-silicon capacitors [171], as a switchable element in non-volatile memories [172] and as electrodes in dynamic random access memory (DRAM) trench capacitors [173] because the CVD process allows a coating of structures with high aspect ratio.

The low resistivity and the work function of about 4.6 eV (mid-gap to Si) render it a potential candidate for metal-silicon contacts [168]. Recent studies show that GC is in addition capable of creating low-barrier Schottky contacts to n-Si with a barrier height of about 0.41 eV to 0.6 eV [142, 168, 174–176]. These values are comparable to those of common silicide contacts, but furthermore, Kreupl [168] has discovered in a first study that the C-Si contact is thermally highly stable and can withstand pulses with high current densities without damage. Furthermore, carbon has a very low diffusivity in Si which greatly reduces the probability of a short circuit of the junction. For example, the diffusion constant at 950 °C is 1500 times smaller than that of titanium in silicon [177, 178].

This robustness is very attractive for high-power devices where temperatures and currents are high, but also in CMOS devices to have an additional protection mechanism against overstress (like ESD) for the interface. Unfortunately, the temperature of over 800 °C required for the pyrolysis process is not always compatible with the temperature budget restrictions of around 400 °C to 500 °C for middle and back end of line (MOL/BEOL) at many applications, especially in advanced technology nodes [37, 179].

An alternative approach would be *radio frequency* (rf) *magnetron sputtering* — a physical vapor deposition (PVD) method and a standard process in the semiconductor fabrication. Investigations show that it is possible to produce sp^2-rich layers with a resistivity of $< 10\,\mathrm{m\Omega\,cm}$ at a low temperature [180, 181]. The labeling as graphenic carbon seems appropriate and the good adhesion to the substrate render it as another alternative for the substitution of conventional used silicides. Furthermore, it has been shown that sputtered carbon electrodes in memory devices with ovonic threshold switching (OTS) selectors are good diffusion barriers for titanium and could severely improve the reliability [182, 183]. This property might be the reason that carbon is also used as electrode in Intel's 3D XPoint memory [184].

1.7 Objective of the Thesis

The aim of this work is to deposit graphenic carbon directly onto silicon by

- the pyrolysis of a hydrocarbon gas source in a chemical vapor deposition (CVD) process; and
- a rf magnetron sputter deposition method.

The electrical properties of a GC-Si and a conventional TiSi-Si contact will be benchmarked with a commercial test vehicle substrate and especially the reliability against an ESD pulse with high current densities will be evaluated.

2 Characterization Methods and Theoretical Background

The essential theoretical basics of the electrical properties of graphenic carbon and the metal-semiconductor contact are discussed in this chapter. The methods used to evaluate the material and the produced diodes are also introduced.

2.1 Electrical Properties of Graphenic Carbon

Graphenic carbon (GC) is a material with no specific description, as it is rather a class of materials and is strongly influenced by the manufacturing conditions. Therefore, it is at first necessary to understand the basic electrical properties of solids. Then, by discussing graphite, the electrical properties of GC can be approximated.

2.1.1 Electrical Classification of Solids

A common way to visualize the differences between metals, semimetals, semiconductors and insulators is to look on the band theory of solids and especially on the band gap E_g between empty and electron occupied energy levels/bands. Such bands are formed due to the overlap of atomic orbitals in the crystal or lattice and valence electron spread over the whole structure. The number of states within particular energy levels in these bands, that are allowed to be occupied by electrons or holes, are called the density of states (DOS). They are not uniform across a band, as shown in Fig. 2.1, and get close to zero at the edges and outside [185].

Typical metals have a high number of conductive electrons per volume ($\geq 10^{22}\,\mathrm{cm}^{-3}$), therefore, they are also named as conductors. For semimetals, the number is in the range between $10^{17}\,\mathrm{cm}^{-3}$ and $10^{20}\,\mathrm{cm}^{-3}$ as the DOS in proximity to the Fermi level E_F is very low [186]. Graphite belongs to this class of solid and has a free carrier concentration of about $7 \times 10^{18}\,\mathrm{cm}^{-3}$ at 300 K, both for electrons and holes [187]. Intrinsic (non-doped) semiconductors, as shown in Fig. 2.1, generally have a band gap above 1 eV and a much lower mobile carrier concentration as the thermal energy is not sufficient to lift a reasonable amount of electrons to the conduction band. The number can be increased by doping to values similar to semimetals, but then one charge carrier type dominates. Insulators have a very high band gap (≥ 4 eV) and electrons are strongly bonded to the nucleus – hence, they are 'non-conductive', like diamond or SiO_2.

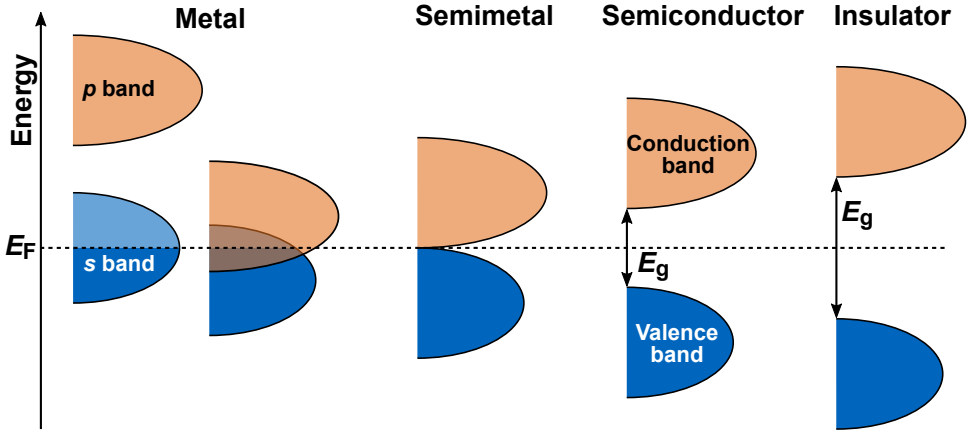

Figure 2.1: Schematic representation of the density of states of a typical metal, semimetal, semiconductor and insulator. Reference here is the Fermi level E_F. The s and p bands are bands built from s or p orbitals. In metals, single or overlapping bands are used for conduction. Electrical conduction can only occur at semimetals, semiconductors and insulators in the conduction band, which lies above E_F. Semimetals do not have a band gap or at least a very low one, but the DOS at E_F are reasonable low. Semiconductors and insulators do have a forbidden gap and the differentiation can be made by its magnitude E_g. Adapted from Ref. [185].

2.1.2 sp^2 Hybridization of Carbon

Elemental carbon consists of six electrons — four of them are valence electrons — and has the electron configuration $1s^2 2s^2 2p^2$. The $1s$ electrons are substantially inert and do not contribute to any chemical bonds. When a carbon atoms gets bonded to another atom, it changes to an energetically more favorable configuration – known as *hybridization*. The s and p orbitals combine into a new hybrid orbital with the energy level between the original orbitals [188]. As previously mentioned in section 1.6, sp, sp^2 and sp^3 hybridized orbitals are possible.

An sp^2 hybridized carbon atom, like shown in Fig. 2.2(a), has three identical sp^2 orbitals arranged in the same geometrical plane with an angle of 120° to each other. The remaining unhybridized p orbital is perpendicular to this plane. If the atom bonds to another C atom, the sp^2 orbitals overlap and form a very strong σ bond, as shown in Fig. 2.2(b), which is responsible for the strength of carbon crystals [119]. If all the remaining sp^2 orbitals bond to C atoms, graphite — to be more precise, graphene — with the honeycomb-like structure is obtained (see Fig 1.10(b),(c)). The unhybridized p orbitals can not really overlap and just form a π bond, with the shared electrons above and below the σ bond. This bond is very weak and the delocalized electrons can move more easily. They are responsible for the semimetal properties and the good conduction of graphite. Diamond in contrast is sp^3 hybridized and forms only σ bonds. Therefore, it is the hardest material, but it is a poor conductor (insulator) due to the lack of π electrons.

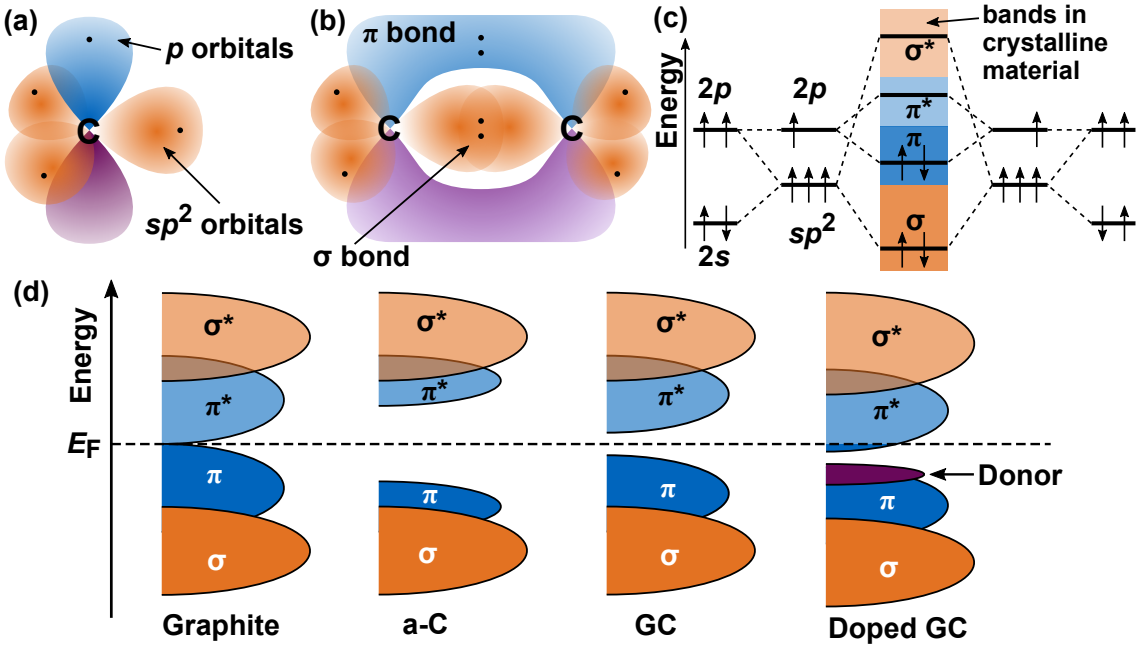

Figure 2.2: (a) A single sp^2 hybridized C atom. The lobes indicate the individual orbitals (sp^2 and p) and the propability of electrons to be at a certain location. The sp^2 orbitals have smaller lobes in opposite direction, which are omitted for clarity. (b) shows two C atoms with molecular orbitals formed. C-C double bonds consist of one σ bond (overlapped sp^2 orbitals) and one π bond (overlapped p orbitals) below and above the σ bond. The remaining sp^2 lobes can form bonds to further atoms and form a crystal. Adapted from Ref. [188]. (c) The corresponding molecular orbital diagram. If the bonds are in a crystalline structure, like graphite, energy bands are formed. (d) Schematic band structure with DOS of various carbon forms. Graphite as semimetal has no band gap, whereas a-C has a larger one. GC is expected to have a small band gap, idealy close to zero, but depends on the exact material form. A doping with foreign atoms can shift the Fermi level, which increases the carrier concentration. Adapted from Refs. [119, 189].

According to the chemical bonding theory, sp^2 carbon forms constructive interfering bonding orbitals (σ and π) and destructive overlapping antibonding orbitals (σ^* and π^*), as illustrated in Fig. 2.2(c). An electron is normally in the bonding orbital, as it has a lower energy. If it is excited to an antibonding state, it gets excluded from the nuclei region and can freely move. In case of a crystal structure, like graphite, the orbitals form bands and π and π^* touch each other.

But as can be seen in Fig. 2.2(d), the DOS are low at the intercept point, which is also the Fermi level, why it only has semimetal properties. This view is just valid within the crystal plane. The individual planes of graphite just stick together by van der Waals forces and the spacing between them is comparatively large (0.355 nm). Due to the lack of bonds, the electrons can hardly move from one plane to another and the material behaves there more like an insulator. Amorphous carbon is highly disordered and has a low amount of sp^2 bonds. Consequently, the band structure changes with altered π and π^* bands. A band gap with a magnitude between dia-

mond and graphite is obtained. Graphenic carbon is sp^2 rich and in its properties closer to graphite. It has most likely a small band gap, which depends on the process conditions but is expected to be below 0.25 eV [176]. GC is sometimes described as turbostratic carbon due to a certain degree of disorder [190]. This allows to form bonds between the planes and give rise to a better conductivity within this direction. A doping of these carbon materials furthermore changes the band structure. For example, nitrogen (N) acts as donor and shifts the Fermi level towards the conduction band (π^*), similar to semiconductors, and increases the electron concentration [189, 191, 192].

Compared to semiconductors, metals show a different behavior with regard to their electrical resistivity. If the temperature is increased, the atoms start to vibrate in the lattice and free electrons get more likely scattered (lower free mean path), which increases the resistivity. In semiconductors in contrast, additional electron-hole pairs are thermally generated. At a certain point, their amount is so high that their influence exceeds the negative impact of a lattice movement and the resistivity decreases. Graphite in turn shows also such a behavior with negative temperature coefficient (NTC). The resistivity decreases, independent of the crystal direction, up to a certain temperature and only at very pure HOPG the resistance always increases with the temperature [193].

2.2 The Metal-Semiconductor Contact

The metal-semiconductor (MS) contact is an inseparable part of all microelectronic devices and can be found at most of the terminals. It is quite essential for the performance and reliability of the device. When a metal and a semiconductor are brought into contact, a *Schottky barrier* get formed at this boundary layer, which is mainly responsible for its properties. This was named after Walter Schottky, who first described the nature and theory of such a contact in 1939 [194]. Depending on the application, the contacts may have rectifying current-voltage (I-V) characteristics, similar to a p-n junction, or ohmic (non-rectifiying) behavior. Schottky diodes, as used in high-frequency mixers, detectors and frequency multipliers, are becoming increasingly important due to the growing importance of mobile communications. This requires a sufficiently high Schottky barrier height (SBH) to obtain the necessary current or voltage rectification, which is also needed in power applications. In transistor in turn, it is desirable to have a very low SBH, as this results in a low contact resistance and a high on/off ratio.

Therefore, it is important to obtain a good understanding of the underlying physical and electrical properties of the MS systems in order to maintain future CMOS scaling and advance further technological developments. The following theoretical explanations and derivations are primarily taken from Refs. [114, 195, 196].

2.2.1 Formation of the Ideal Schottky Barrier

First, the case is considered where the metal and the semiconductor are still separated and electrically neutral. In addition, no surface states are present, called 'ideal', and therefore, the individual energies are constant across the material. As shown in Fig. 2.3(a) with an n-type semiconductor, the two solids are aligned with respect to the vacuum level. The average energy of the electrons differs from one material to another resulting here in the lower Fermi level of the metal $E_{\mathrm{F,m}}$ compared to the semiconductor $E_{\mathrm{F,s}}$. A related parameter is the work function of the metal $q\phi_{\mathrm{m}}$ and the semiconductor $q\phi_{\mathrm{s}}$, respectively, which represents the difference in energy between the vacuum and the Fermi level. q is an electric charge and represents here the elementary charge e ($q = e$).

When the metal and the semiconductor are joined together, a charge transfer occurs until a thermodynamic equilibrium is reached and the Fermi levels finally align to each other. Atoms (donor or acceptor) near the interface remain ionized in the semiconductor, resulting in a depletion region with a width W (a region almost free

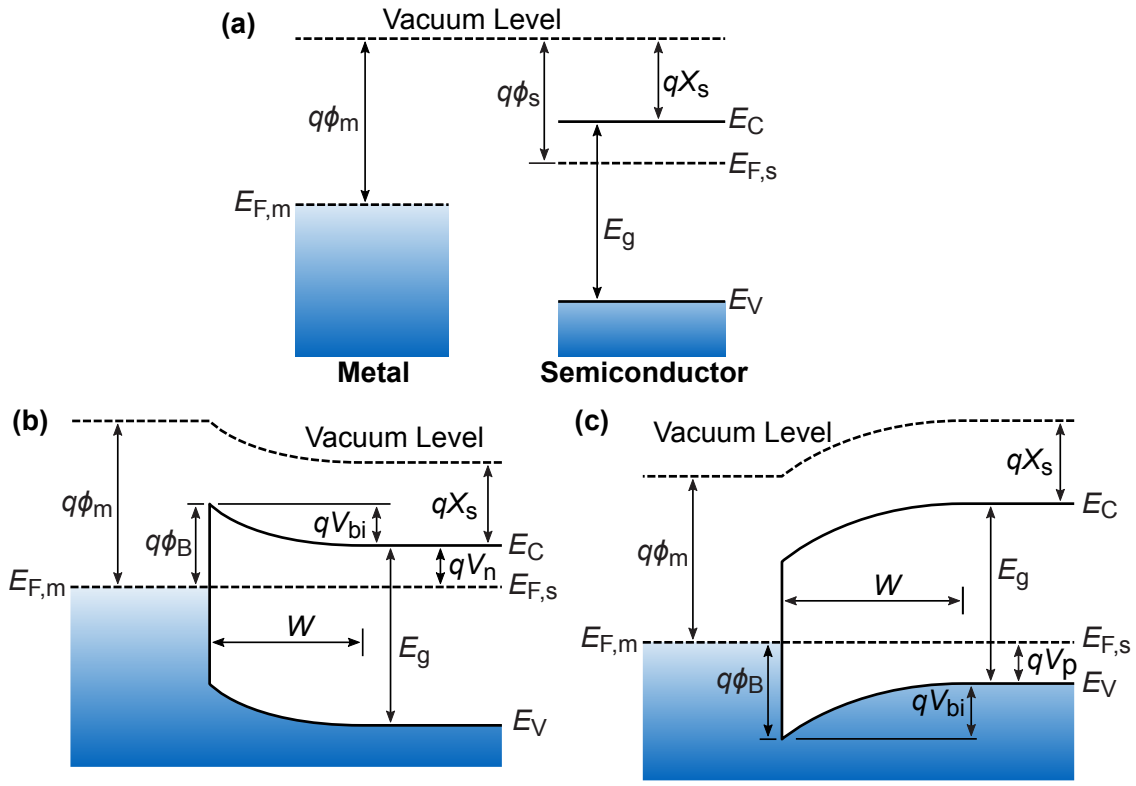

Figure 2.3: Energy-band diagrams of a metal-semiconductor system. (a) The metal and the semiconductor are electrically neutral, are still separated from each other and just show an alignment with respect to their vacuum level. The band diagram of an n-type in (b) and p-type semiconductor in (c) with an ideal contact to a metal in thermal equilibrium. The Fermi levels E_{F} of the two materials are aligned and the semiconductor bands are bent. Adapted from Refs. [114, 195].

of mobile charge carriers) and a parabolic bending of the lowest energy of the conduction band (E_C) and the highest energy of the valence band (E_V). The direction of the bending depends on the type of doping and is illustrated for an n-type semiconductor in Fig. 2.3(b) and a p-type semiconductor (not considered any longer) in Fig. 2.3(c).

The most important feature is the Schottky barrier, hence the name Schottky diode, which must be overcome by majority charge carriers coming from the metal. According to the Schottky-Mott theory [194, 197], is its height $q\phi_B$ a pure material dependent parameter with:

$$q\phi_B = q\phi_m - q\chi_s. \tag{2.1}$$

The electron affinity $q\chi_s$ (Si electron affinity $q\chi_{Si} = 4.05\,\text{eV}$ [114]) is the energy needed to move an electron from the bottom of the conduction band to the vacuum level. A rule of thumb for ideal contacts states for a given metal and semiconductor combination that the sum of the barrier heights on n- and p-type semiconductors equals the band gap E_g.

The depletion region also causes the formation of an electric field and the resulting potential difference is also called built-in potential V_{bi}, expressed as

$$V_{bi} = \phi_m - \phi_s = \phi_B - V_n. \tag{2.2}$$

V_n is the Fermi potential from the conduction-band to E_F:

$$V_n = \frac{E_C - E_F}{q} = \frac{k_B T}{q} \ln\left(\frac{N_C}{n}\right). \tag{2.3}$$

Here, N_C is the effective density of states in the conduction band (for Si at 300 K: $2.8 \times 10^{19}\,\text{cm}^{-3}$) and n is the free electron concentration, which is roughly equal to the donor doping density N_D at room temperature ($n \approx N_D$). From here it is clear, that not only the type of solids but also the doping concentration have a strong influence on V_{bi}.

The width W of the depletion layer can be altered at a fixed material combination mainly by the doping level and as shown in Fig. 2.4, the externally applied voltage V:

$$W = \sqrt{\frac{2\varepsilon_s\varepsilon_0}{qN_D}\left(V_{bi} - V - \frac{k_B T}{q}\right)}, \tag{2.4}$$

where ε_0 is the vacuum permittivity, ε_s is the semiconductor permittivity (11.7 for Si), k_B is the Boltzmann constant and T the temperature.

W is a quite important parameter as it is directly related to the junction or depletion-layer capacitance C_J, which consequently also affects the total device capacitance. As the depletion zone is free of mobile charge carriers, this acts like the

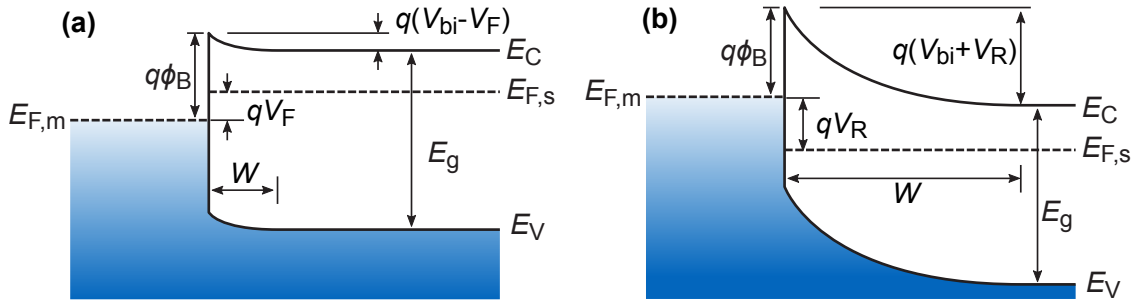

Figure 2.4: Energy-band diagrams of a metal-semiconductor contact under different biasing conditions. (a) When a positive (forward) voltage V_f is applied to the anode (metal) with respect to the cathode (semiconductor), $E_\mathrm{F,m}$ is lowered compared to $E_\mathrm{F,s}$ and the depletion width gets reduced. A reverse bias V_r shifts the Fermi levels vise versa and causes a larger W. Adapted from Ref. [114].

dielectric between a parallel plate capacitor, whereby the area-independent capacitance can be expressed as follows:

$$C_\mathrm{J} = \frac{\varepsilon_\mathrm{s}\varepsilon_0}{W} = \sqrt{\frac{\varepsilon_\mathrm{s}\varepsilon_0 q N_\mathrm{D}}{\left(2V_\mathrm{bi} - V - \frac{k_\mathrm{B}T}{q}\right)}}. \tag{2.5}$$

Schottky Barrier Lowering

Even with an ideal contact, it can be observed that the barrier does not behave as perfectly as shown in Fig. 2.3 and Fig. 2.4. The barrier height is slightly lowered, like illustrated in Fig. 2.5, due to a phenomenon called *image-force lowering*. The depletion zone is not fully free of mobile electrons and when it approaches the metal, it will induce a positive image charge at the same distance to the interface in the metal. As a result, a Coulomb potential forms perpendicular to the surface, which changes the potential energy of the electrons. This additional energy need to be added to the barrier energy and lowers $q\phi_\mathrm{B0}$ (barrier height without image force) by

$$q\Delta\phi = q\left[\frac{q^3 N_\mathrm{D}}{8\pi\left(\varepsilon_0\varepsilon_\mathrm{s}\right)^3}\left(\phi_\mathrm{B0} - V_\mathrm{n} - V - \frac{k_\mathrm{B}T}{q}\right)\right]^{1/4}. \tag{2.6}$$

As can be seen, essentially the donor density and the applied voltage have an impact on a lowering as they influence the field in the depletion region. For example, $\Delta\phi$ is about 25 mV at a doping levels of $10^{16}\,\mathrm{cm}^{-3}$, an ideal SBH of 0.5 eV and no external bias. Fig. 2.5 clearly shows that an applied forward bias leads to a smaller barrier lowering $q\Delta\phi_\mathrm{F}$, whereas a reverse voltage leads to a reduced effective barrier height (barrier is lowered by $q\Delta\phi_\mathrm{R}$). In the latter case, the electrons can overcome the barrier more easily, which results in an increased current flow at higher reverse bias voltage.

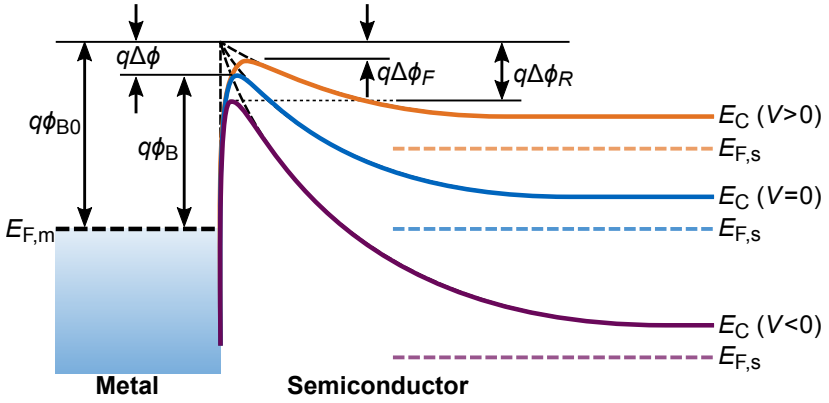

Figure 2.5: Energy-band diagrams of a metal-semiconductor contact with barrier lowering at different biasing conditions. The height would be intrinsically $q\phi_{B0}$ without considering a barrier lowering, but in reality it is lowered by $q\Delta\phi$ due to an image-force. The magnitude can be altered by applying a voltage to smaller (forward bias) or higher (reverse bias) values, which in turn changes the final barrier height. Adapted from Ref. [114].

2.2.2 Current Transport Mechanisms

A metal-semiconductor contact (e.g. Schottky diode) is, in contrast to the p-n junction, a 'majority carrier device', since the current flow is essentially caused by one type of charge carriers (electrons in the n-type semiconductor). However, minority charge carriers also have a minor contribution. The overall current transport has basically four mechanisms, as shown in Fig. 2.6, and can be described as follows:

(1) Thermionic emission of thermally excited majority carriers from the semiconductor over the barrier into the metal is the dominant mechanism in forward-biased junctions for lightly/moderately doped semiconductors ($\leq 10^{17}\,\mathrm{cm}^{-3}$) at room temperature;

(2) quantum mechanical tunneling (field emission or thermionic-field emission) through the barrier is important for ohmic contacts with high impurity concentrations;

(3) electron-hole recombination in the depletion region; and

(4) diffusion of minority carriers in the semiconductor and electron-hole recombination in the neutral region.

The Thermionic Emission Model

The term thermionic emission usually refers to the emission of an electron from a hot metal into vacuum [198]. This theory can be applied analogously to the metal-semiconductor contact. It essentially states that only charge carriers with an energy greater than the SBH are able to overcome it. The current flow of the diode can be

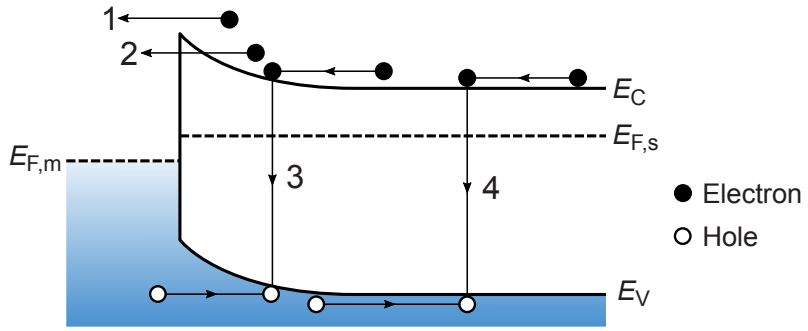

Figure 2.6: Energy band diagram of a forward biased Schottky junction on a n-type semiconductor showing four different transport processes. (1) Thermionic emission, (2) tunneling through the barrier, (3) electron-hole recombination in the depletion region, and (4) hole injection from the metal and recombination in the neutral region. Adapted from Ref. [195].

expressed as

$$J = A^{**}T^2 \exp\left(-\frac{q\phi_B}{k_B T}\right)\left[\exp\left(\frac{qV}{k_B T}\right) - 1\right]. \tag{2.7}$$

The pre-factor of this equation is also called saturation current density J_0:

$$J_0 = A^{**}T^2 \exp\left(-\frac{q\phi_B}{k_B T}\right). \tag{2.8}$$

It is associated to the current flow at high reverse bias and quite sensitive to the temperature, whereas a high barrier height leads to a lower current. A^{**} is a material-specific correction factor called the (reduced) effective Richardson constant, which is $112\,\mathrm{A\,cm^{-2}\,K^{-2}}$ for n-doped Si [199]. This coefficient also takes into account the diffusion of charge carriers, so Eq. 2.8 can be attributed to a so-called thermionic emission-diffusion theory [114]. The second term of Eq. 2.7 also depends on T but mainly refers to a current increase by an externally applied voltage V across the junction. It yields a semi-logarithmic plot under forward conduction a straight line when $V \gtrsim 3\frac{k_B T}{q}$.

However, the slope of the curve in a real Schottky diode deviates from the diode equation. This deviation is caused by second order effects and can be described by the ideality factor n. In general, n differs from unity with the commonly accepted sources being large surface leakage currents, recombination centers or trapping states at the interface region or in the semiconductor bulk, tunneling through the barrier, and a bias dependency of the SBH [24, 200]. Some of these mechanisms will be discussed later.

Furthermore, the individual components of the diode have a resistance that can be modeled as a resistor R_s (R_s is here area-normalized) in series to the diode. The main causes to it are the semiconductor bulk and metal resistance and the contact resistances R_c. The resistance between metal and semiconductor can be expressed

according to the thermionic emission theory (Eq. 2.7) for low/moderate doping levels as follows:

$$R_\mathrm{c} = \left(\frac{\mathrm{d}J}{\mathrm{d}V}\right)^{-1}_{V=0} = \frac{k_\mathrm{B}}{A^{**}\pi q T} \exp\left(\frac{q\phi_\mathrm{B}}{k_\mathrm{B}T}\right). \tag{2.9}$$

The total R_s leads together with the current flow through the diode to a voltage drop of $\Delta V = JR_\mathrm{s}$, reducing the applied voltage directly at the junction. In order to describe the J-V characteristics considering n and R_s, Eq. 2.7 can be modified to a semi-empirical equation:

$$\boxed{J = \underbrace{A^{**}T^2 \exp\left(-\frac{q\phi_\mathrm{B}}{k_\mathrm{B}T}\right)}_{=J_0} \left[\exp\left(\frac{q(V - JR_\mathrm{s})}{nk_\mathrm{B}T}\right) - 1\right].} \tag{2.10}$$

The corresponding curve, which also considers n and R_s, is shown in Fig. 2.7 as an illustrative example.

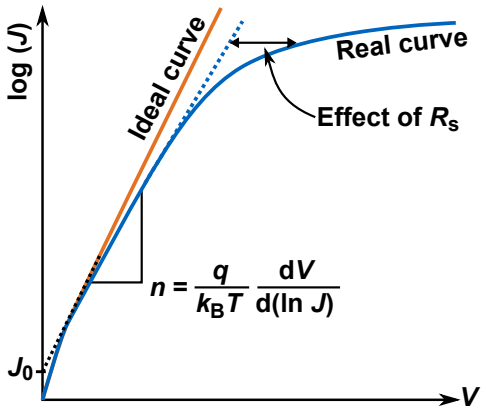

Figure 2.7: Schematic semi-logarithmic J-V curves according to the thermionic emission theory. The ideal curve, after Eq. 2.7, is a linear line when $V \gtrsim 3\frac{k_\mathrm{B}T}{q}$. If an ideality factor n, after Eq. 2.10, is taken into account, the slope gets flatter. In a real device, the series resistance causes a voltage drop, leading to a non-linear curvature at higher current density/voltage. The intersection of the extrapolated linear part of the curve with the y-axis yields J_0. It becomes clear that a change in slope also leads to a slightly different J_0.

Ohmic Contacts

For many devices, like transistors, it is essential to contact the semiconductor without rectifying, i.e. nearly linear I-V characteristic in forward and reverse direction. A low R_c is crucial to achieve the desired performance, like the fast transfer of charge within the circuitry and to reduce power dissipation. Two ways to establish an ohmic contact are possible:

- The SBH is negative, zero or close to the thermal energy $k_B T$ to easily allow emission across the barrier; and
- the semiconductor has a high doping density ($> 10^{18}\,\mathrm{cm}^{-3}$), which leads to a narrow depletion region and consequently to a narrower barrier allowing charge carriers to tunnel through it quantum mechanically in both directions.

As can be seen at Eq. 2.1, the metal work function must be close to or less than the electron affinity of the semiconductor to achieve a small SBH. Unfortunately, most of the metals, which are compatible to Si, only fulfill this requirement to a certain extent [201].

It is therefore essential to choose a high doping for an ohmic contact. The current transport is then no longer based only on the thermionic emission theory, but the larger part is based on the thermionic-field emission (see Fig. 2.8) [202]. At even higher doping densities ($\gtrsim 10^{19}\,\mathrm{cm}^{-3}$), the proportion of field emission current also increases. Consequently, the contact resistance is no longer only dependent on the SBH, as in the case of thermionic emission (see Eq. 2.9), but also on the doping concentration, which can be expressed in simplified terms as follows:

$$R_c \approx \frac{k_B}{A^{**}\pi q T} \exp\left[\frac{2\phi_B}{\hbar}\sqrt{\frac{\varepsilon_0 \varepsilon_s m_e^*}{N_D}}\right]; \tag{2.11}$$

$$\boxed{R_c \propto \exp\left(\frac{\phi_B}{{N_D}^{1/2}}\right).} \tag{2.12}$$

$\hbar$ is the reduced Planck constant and m_e^* is the effective electron mass. In summary, a good ohmic contact requires a highly doped semiconductor and a metal that gives a low barrier height.

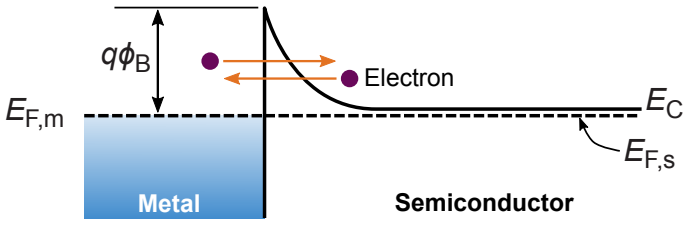

Figure 2.8: Energy-band diagram for a metal to a highly doped n-type semiconductor. The depletion region is very small in this case, which leads to a strong band bending. This allows electrons to tunnel through the narrow barrier very easily in both directions.

2.2.3 Non-Ideal Schottky Barrier

However, when considering a real Schottky contact, the barrier height theory most often does not agree with measured values. Most metals show a strong *Fermi level pinning* roughly at mid-gap of Si with a much weaker dependency on their work function [52]. For the involved mechanisms various theories are known [143,200,203].

One of the earliest concepts is the metal-induced gap states (MIGS) model [204]. Since the wave function of electrons in the metal is not abruptly terminated at the junction and penetrate a few Å into the semiconductor surface, interface states with energy levels within the band gap of the semiconductor are created. These states are charged and the Fermi level gets pinned at a charge neutral level at the semiconductor side. An interface region (see in Fig. 2.9) is created, which decouples the metal work function and the semiconductor electron affinity. It should be noted that imperfections and defects of the crystal near the contact can also cause such interface states.

Tung [205] proposed a more recent model, which is based on the formation of 'molecular electric dipoles'. The chemical bonds at the MS contact lead to a charge rearrangement as the number of effective bonds per number of semiconductor/metal atoms at the interface is not equal. Possible causes are a lattice mismatch, a structure incompatibility or the formation of tilted bonds. A similar interface specific region (causing a change in the SBH) as mentioned before is formed (see Fig. 2.9) but now caused by an interface polarization. In this model is the barrier height directly influenced by a change in the chemical or morphological form of the interface bonds. This is an important fact for reliability investigations of the MS contact as a change in the SBH after a stress condition is an indication of a possible modification of the bond system.

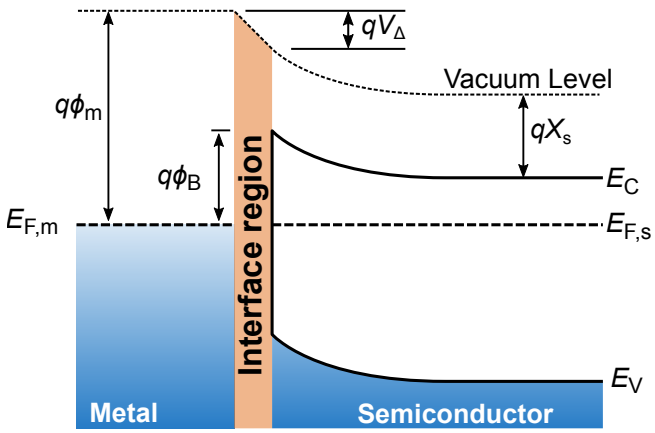

Figure 2.9: Energy-band diagram of a metal-semiconductor contact with a non-ideal contact. The interpretation of the interface region depends on the respective model and can be a layer caused by interface states or an interface specific region where a bond-polarization causes an interface dipole. Independent of the model, a potential drop V_Δ occurs, leading to a change in the SBH.

2.2.4 Schottky Diode Test Vehicle

It is well-known, that Schottky diodes can be used as a test vehicle to get a deeper understanding of the physical and electrical properties of a semiconductor or MS contact. It is used for example to study deep level bulk defects [206], interface effects [207] or as surface contamination monitor of individual process steps [208]. But especially for reliability tests, the Schottky diode is very interesting. A change in the SBH, in the leakage current, rectifying behavior or on-current can immediately provide evidence on a degradation of the junction without the need of a complex material analysis, e.g. through a device cross-section or secondary-ion mass spectrometry. Applications range from the investigation of diffusion barriers [209] or the analysis of the reliability of the contact metal towards high temperatures or an electrical overstress, like during an electrostatic discharge ESD pulse [210–214].

Especially rf Schottky diodes are very suitable [210,211,214], as they are designed to have a low series resistance to decrease the RC delay time, which allows the operation at high frequencies. The low R_s is achieved by a low doping level of the semiconductor only close to the contact region, normally realized by a few 100 nm thick epi-layer, whereas the rest of the substrate is highly doped. This thin layer is very susceptible to degradations in its electrical reverse bias characteristics when contaminations such as metal ions enter this epitaxial region. Such changes can be also detected with p-n junctions [215], but a Schottky diode is much more sensitive.

The *Infineon BAT15 Schottky diode* [216], based on an n-type silicon substrate with a thickness of 675 µm and a surface orientation of (111) is used as test vehicle in this thesis. It is a diode for detector and mixer applications up to 12 GHz as it has a low barrier height, a low forward voltage and a low junction capacitance. A schematic cross-section of the diode is illustrated in Fig. 2.10(a) and is mainly composed of an n^--Si epitaxial layer with a thickness of 150 nm on a highly doped substrate. The circular p^+-guard ring structure extends through the complete epi-layer and prevents the electrode sharp-edge effect, which cause a leakage current and a low breakdown voltage [217].

The test vehicle was provided from Infineon with the same dimensions and doping profile as the commercial version they sell — only without metallization, like shown in Fig. 2.10(b). Conventionally, a TiSi-Si contact — the exact crystal phase is confidential — is used in this diode because of the low SBH. The provided test vehicle allows to study an arbitrary 'metal', here graphenic carbon, towards its electrical characteristics and reliability properties and enables a direct comparison to the commercial TiSi-Si BAT15 diode. The backside metallization should be a metal which creates a low SBH, but the overall impact of the type of metal is assumed not to be very critical on the performance here. On the one hand, the substrate is highly doped, which reduces the contact resistance, and on the other hand, the area is very large compared to the active region, which also decreases the influence of R_c.

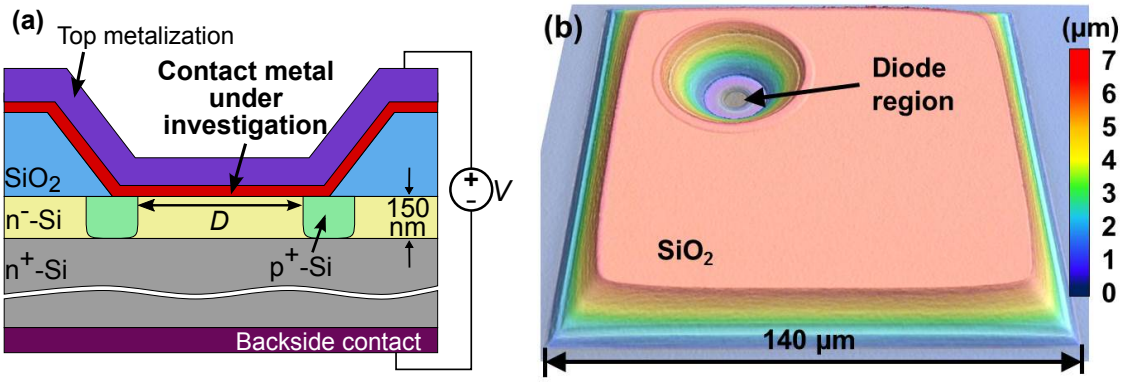

Figure 2.10: (a) A schematic cross-section of the Infineon BAT15 silicon-based Schottky diode with p-type guard ring structure and thin low-doped n-type epitaxial layer. The diode has a vertical structure, i.e. when a forward voltage is applied, the current flows towards the backside of the substrate. The junction is formed by the desired metal to investigate (TiSi in the commercial version) and an additional top metallization. The diameter D of the circular active region is 7.6 µm (area is 45.36 µm^2). (b) Microscope image of the BAT15 test vehicle structure without metallization with overlaid colored height profile. The quadratic oxide pad has a thickness of 6 µm to reduce the capacitance of a potential top metallization to the Si substrate.

2.3 Electrical Characterization Methods

The characterization of the device under test (DUT), here a Schottky diode, was measured in a shielded probe station (see Fig. 2.11(a)) in a two-wire measurement configuration [218]. The main disadvantage to a four-wire (Kelvin) measurement is that the current and voltage are not measured with different pairs of electrodes. As a result, especially with small device resistances, the lead and contact resistances can influence the measurement results. The advantage, however, is that the test setup can also be used for ESD stress tests without extensive modifications.

2.3.1 DC Measurement Setup

The dc device characterization of the fabricated diodes is performed in a Lake Shore TTPX probe station, as shown in Fig. 2.11(a). An Agilent model 2912A two channel source measurement unit (SMU) is used to execute the desired measurement tasks, mainly the acquisition of I-V curves, to characterize the MS contact. The SMU is controlled externally by a computer with MathWorks MATLAB to set individual source values and to acquire the measured data. The setup is suitable to be used with triaxial cable, but this is not necessary as the current to be measured is greater than 1 nA.

The measurement cables are feeded into the TTPX chamber, an inside view is shown in Fig. 2.11(b), and connected to a self-made probe. This consists of a probe tip mounted directly to a grid-style printed circuit board (PCB) with the needle's

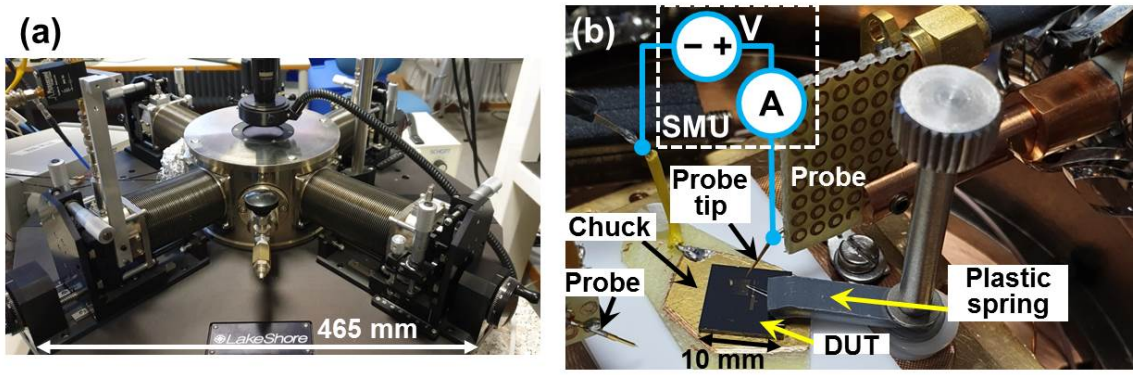

Figure 2.11: (a) shows a photograph of a Lake Shore TTPX probe station with microscope, which allows to measure a diode under a darkened and electrically shielded environment. It consists of four micro-manipulators (two are used) with cable feed-through to contact a DUT. (b) shows an inside view of the measurement chamber in which a 10 mm × 10 mm sample is pressed with a plastic spring onto a chuck — an FR4 PCB that is copper- and gold-plated on one side. The board also sits on 5 mm thick polytetrafluoroethylene (PTFE) to reduce capacitive coupling to the surrounding. An SMU, indicated schematically, is used to apply a voltage and sense the current in a two-wire configuration. It is connected with a coaxial cable to a probe needle, used to contact the anode of the diode (top side of the sample). The chuck acts as ground electrode, connected to the grounded shield of the coaxial cable. The second probe can alternatively be used for pulse-stress measurements discussed in section 2.3.3.

rear part soldered to an SMA connector. The substrate is pressed with a plastic spring on the gilded chuck to get a low-ohmic contact to the metallized substrate backside and the needle is still able to contact the anode of the diode.

2.3.2 Schottky Diode Parameter Extraction

In order to determine the quality of the MS contact compared to others, it is necessary to extract the critical parameters ($q\phi_\mathrm{B}$, R_s, n). The most common method is the extraction from current-voltage characteristics, as it allows to extract all three parameters. The obtained SBH by this methode involves barrier lowering, which can be circumvented by the capacitance-voltage (C-V) method [114, 195]. But the used test vehicle is only conditionally suitable for latter method because the epi-layer is very thin and the doping profile is not necessarily uniform within this region.

Cheung's Method Especially the extraction of R_s is tricky, for which the method of Cheung [219] provides very reliable solutions. Therefore, Eq. 2.10 can be rearranged as follows:

$$V = \frac{nk_\mathrm{B}T}{q} \cdot \ln\left(\frac{J}{J_0}\right) + R_\mathrm{s}J = \frac{nk_\mathrm{B}T}{q} \cdot \ln\left(\frac{J}{A^{**}T^2}\right) + n\phi_\mathrm{B} + R_\mathrm{s}J. \tag{2.13}$$

The derivative of V with respect to $\ln(J)$ with the aid of $\mathrm{d}J/\mathrm{d}\,(\ln J) = J$ results in

$$\frac{\mathrm{d}V}{\mathrm{d}\,(\ln J)} = R_\mathrm{s} J + \frac{n k_\mathrm{B} T}{q}. \tag{2.14}$$

A graphical representation of Eq. 2.14 with data measured at a C-Si diode is shown in Fig. 2.12(a). The curve is approximately linear whereas the slope represents R_s and the y-axis intercept can be used to determine n. The required temperature values are logged during every I-V measurement with the sensors of the used probe station. The SBH cannot be determined yet, therefore an auxiliary function $H(J)$ is introduced:

$$H(J) = V - \frac{n k_\mathrm{B} T}{q} \cdot \ln\left(\frac{J}{A^{**} T^2}\right). \tag{2.15}$$

Together with Eq. 2.13 follows:

$$H(J) = R_\mathrm{s} J + n\phi_\mathrm{B}, \tag{2.16}$$

which also leads to an almost linear line, as shown in Fig. 2.12(a), whereas the slope provides R_s. The intercept with the y-axis yields $n{\cdot}\phi_\mathrm{B}$ and with the previously determined value of n, ϕ_B can be obtained. The closer the two extracted R_s are, the more consistent is the approach. However, if the curve is not as linear as desired, determining the slope and extrapolating to the y-axis may cause deviations in the result.

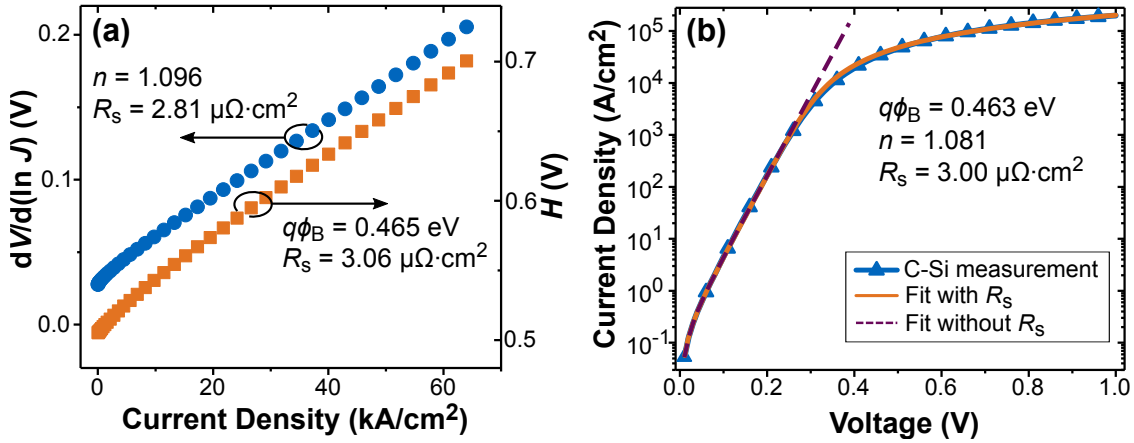

Figure 2.12: Diagrams for the extraction of diode parameters of a forward biased carbon-silicon diode with 7 nm thick C. For Cheung's method shown in (a), two different plots are needed to extract all parameters. By using Lambert W function as illustrated in (b), a numerical solver can be used with the measured J-V data as input values. The fitted curve matches here with the measured one quite well. If R_s is neglected, n and ϕ_B can be extracted without the need of the Lambert W function, just by the slope and the intercept with the y-axis.

Numerical Fitting with Lambert W Function However, it is not easy to check the correctness of the results obtained because an explicit expression for $J(V)$, given by Eq. 2.10, cannot be constructed with elementary functions. As shown by Jung *et al.* [220], an explicit solution can be found by using the Lambert W function. Taking only the principal branch W_0 of the Lambert W function, Eq. 2.10 can be represented with $\beta = \frac{q}{k_\mathrm{B}T}$ as follows:

$$J = \frac{n}{\beta R_\mathrm{s}} \cdot W_0 \left[\frac{\beta R_\mathrm{s} J_0}{n} \exp\left(\frac{\beta}{n} \cdot (V + R_\mathrm{s} J_0) \right) \right] - J_0. \tag{2.17}$$

The diode parameter can be extracted directly by solving the equation numerically by the least-squares method for non-linear curves. Such a solver is directly implemented in MATLAB as a function called 'lsqcurvefit', which provides a direct solution for all three variables. As shown in Fig. 2.12(b), the quality of the fit can be compared directly with the real measurement curve.

The solution for J_0 can be used to extract the SBH by rearranging Eq. 2.8 to

$$q\phi_\mathrm{B} = -k_\mathrm{B}T \cdot \ln\left(\frac{J_0}{A^{**}T^2} \right). \tag{2.18}$$

Both methods yield the SBH including the lowering effect, which is usually used in this work without correction. If a comparison with literature values extracted by the C-V method is necessary, the barrier height $q\phi_{\mathrm{B}0}$ without image-force lowering at zero electric field is required. Wagner *et al.* [221] have derived an expression which allows this by a correlation of the measured barrier $q\phi_\mathrm{B}$ and the ideality factor n:

$$q\phi_{\mathrm{B}0} = n \cdot q\phi_\mathrm{B} - (n-1) \cdot k_\mathrm{B}T \ln\left(\frac{N_\mathrm{C}}{N_\mathrm{D}} \right). \tag{2.19}$$

2.3.3 High Current Pulse Setups

A main task of this work is the investigation of the reliability of an MS contact against ESD pulses by using the BAT15 test vehicle. Basic requirements on the measurement setup are as follows. The device under test (DUT), here the Schottky diode in forward direction, can be subjected to an electrical overstress and can be examined for a change in the electrical properties by I-V measurements. A schematic drawing of the used setup is shown in Fig. 2.13, where an SMU and a pulse generator are simultaneously connected to the DUT via a high bandwidth (12 GHz) bias tee (Picosecond Pulse Labs model 5575A). The bias tee has a dc port which contains an ideal inductance in the equivalent circuit diagram and blocks ac signals, but adds a series resistance of 0.6 Ω. The ac or rf port contains in an idealized representation a capacitor with a low insertion loss (0.6 dB at ≤ 3 GHz). The length of the probe needle was kept as short as possible so that the wave impedance does not deviate too much from the 50 Ω of the transmission lines. The metallization of the chuck was also partly removed to get an effective size closer to the 1 cm × 1 cm sample. This reduces the capacitance of the chuck and avoids an impedance mismatch.

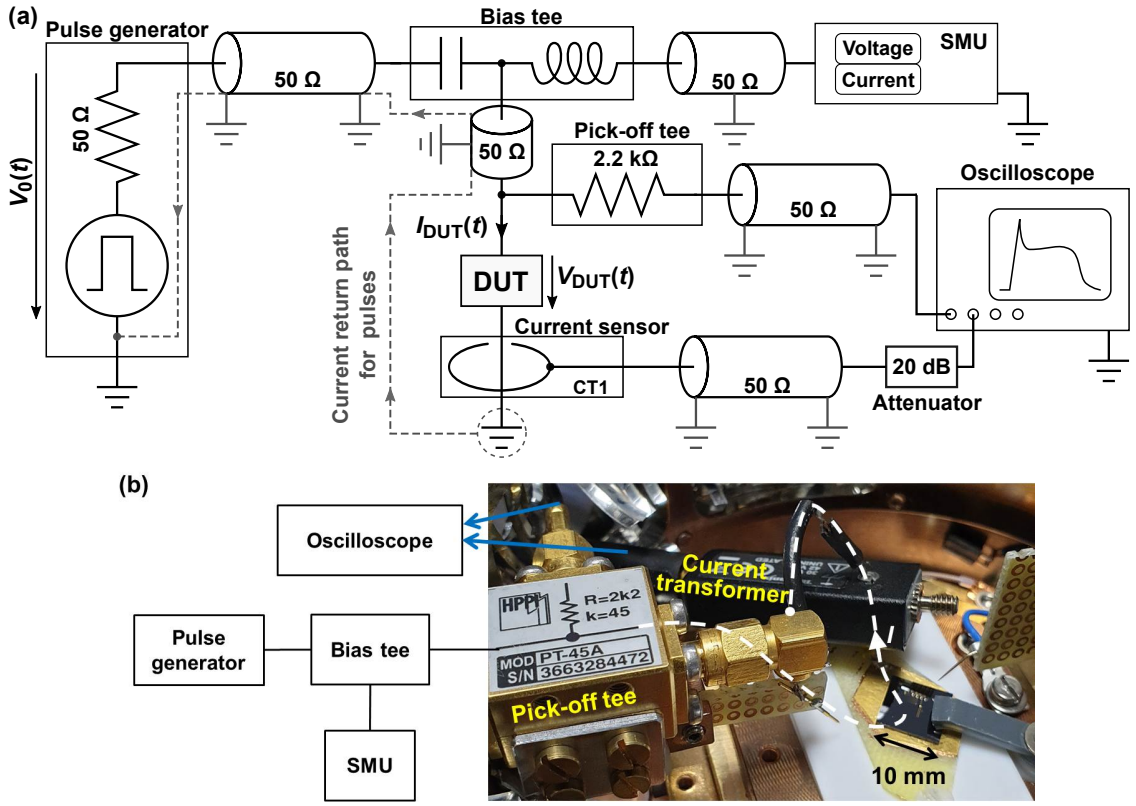

Figure 2.13: (a) Schematic overview of the used measurement setup to evaluate a DUT in dc and pulsed mode. To be able to perform both measurements task, a bias tee is connected before the DUT. The dc port is connected to an SMU to determine the *I*-*V* characteristics. Coaxial cables serve as transmission lines, mainly to reduce noise and the shield serves as a current return path. The drawn ground connection of the individual transmission lines is only shown in the circuit diagram to illustrate that the outer conductors are electrically connected and are at the ground potential of the source. A pulse generator is connected to the ac port of the bias tee. It is important that the impedance of the transmission lines Z_0 (50 Ω) matches the source impedance of generator to avoid signal reflections. The pulse passes a voltage pick-off tee (HPPI PT-45A) immediately before the DUT and afterwards a current sensor (Tektronix CT1). The CT1 sensor is connected with an additional 20 dB attenuator for protection to a 50 Ω input channel of an oscilloscope. The sample chuck is connected with a short copper braid — that also creates the magnetic field measured by the current sensor — to the coaxial cable shield, which acts as the least impedance current return path. (b) shows an inside view of the measurement chamber and a schematic of the connected components. The pick-off tee is mounted very close to the probe tip to accurately measure the effective voltage V_{DUT} applied to the DUT. The current transformer is placed in the return path to measure only the current I_{DUT} through the device. The copper return wire, which creates the field detected by the CT1, is soldered to the chuck and the body of the SMA connector.

An ESD event is commonly emulated with a rectangular voltage or current pulse with a width of 100 ns, measured at 50 % of the pulse height [222]. This is similar to the ANSI/ESDA/JEDEC JS-001-2012 Human Body Model [223] and the IEC61000-4-2 test standard [224]. Here, two different types of pulser schemes are used, the transmission line pulsing (TLP) technique [225, 226] and a pulse generator (Hewlett Packard 214B) with solid-state transistor as switch.

The latter is preferred because it is very versatile. The output voltage V_0 can be set to arbitrary values up to 50 V, the pulse width can be adjusted between 25 ns and 10 ms. Since it is a solid state pulse generator, it has a very good endurance behavior and can output an almost infinite number of pulses at a repetition period down to 250 ns. But the rise time is limited to about 10 ns to 15 ns — defined as the required time to rise from 10 % to 90 % of the pulse height.

In contrast, the home-made TLP system can output signals with an amplitude up to 300 V, but the used mercury-wetted reed switch might not switch that many events as it is a mechanical relay that is vulnerable to fatigue. But the switching operation is bouncing-free and can create a clearer waveform with rise times below 500 ps, which can be seen in the comparison of the waveforms of the two generators in Fig. 2.14(a). The pulses were terminated directly in the attenuated 50 Ω input of an oscilloscope (Rohde & Schwarz RTO1024 with a bandwidth of 2 GHz), so ideally all power is transmitted and no reflections occur at the load. In this case, the load or DUT voltage V_{DUT} equals V_0 ($V_{\mathrm{DUT}} = V_0$).

When a practical diode is tested, not all the power is transmitted as shown in Fig. 2.14(b). A mismatch in the terminating impedance Z_{DUT} of the load/DUT to Z_0 results in a partial reflection of the pulse. The reflection coefficient Γ can be used to determine the amplitude ($\Gamma \cdot V_0$) and polarity of the reflected wave at the DUT [226]:

$$\Gamma = \frac{Z_{\mathrm{DUT}} - Z_0}{Z_{\mathrm{DUT}} + Z_0}. \tag{2.20}$$

If $Z_{\mathrm{DUT}} > Z_0$, Γ is positive and the amplitude of V_{DUT} gets larger than the source value. But if $Z_{\mathrm{DUT}} < Z_0$, the reflected pulse has a negative amplitude, which leads to a decrease in the voltage applied to the device. With the measured data from Fig. 2.14(b), one can conclude with $Z_{\mathrm{DUT}} = \frac{V_{\mathrm{DUT}}}{I_{\mathrm{DUT}}} \approx 3.75\,\Omega$, a reflection coefficient of about -0.86.

The dc port of the employed bias tee can be used to operate the diode at certain operating point by applying a constant voltage or simply to record a I-V curve of the device. A damage or deterioration of the diode characteristics can be identified by monitoring the reverse current leakage at a given voltage, which shows up by an increased current. But also the observation of the series resistance, SBH or ideality factor is important because they indicate a change in the diode properties.

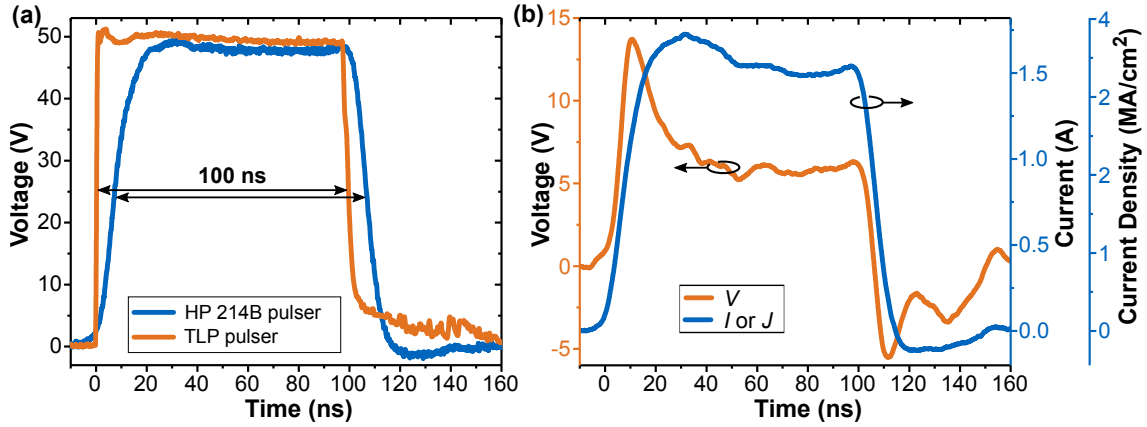

Figure 2.14: (a) Measured typical waveforms of 100 ns long pulses generated by the HP 214B (here the maximum possible value) and the TLP pulser directly terminated into an attenuated 50 Ω input of an oscilloscope. The pulse from the solid-state pulser has a rise time of < 15 ns while it is < 500 ps for the TLP setup . (b) Voltage and current characteristics from a pulse generated by the HP 214B generator sensed with a pick-off tee and current sensor at a C-Si diode. Since the DUT has a smaller resistance than the wave impedance of the transmission line, most of the pulse is reflected with a negative amplitude, resulting in a lower applied voltage V_{DUT}, which settles here at ~ 6 V. The voltage overshoot is mainly caused by capacitive and inductive parasitics in the setup. The measured current I_{DUT} or current density at the DUT has an average amplitude of about 1.6 A or 3.5 MA/cm^2, respectively. The negative current overshoot after the falling edge of the pulse is about 100 mA at a maximum voltage peak of 6 V.

SPICE Simulations

A SPICE simulation is helpful to get a more detailed insight in a measurement setup and to test the influence of circuit parameters. Here LTspice XVII from Analog Devices was used, since transmission lines can be considered for transient simulations and enables a realistic simulation of the setup. Fig. 2.15(a) shows the used schematic with a pulse source as stimulus. The propagation delay T_{d} is correlated to the length of a transmission line. The propagation velocity in a real cable with PTFE dielectric is about 0.2 m/ns [226], so for a length of 1.5 m the delay is 7.5 ns.

The probe used to contact the diode, the chuck and the copper return wire are also modeled by lossless transmission lines. Such a line is composed simplified by two-port elementary components, a series inductance L and a shunt capacitor C, representing infinitesimally small segments of the total length [227]. The characteristic impedance Z_0 is:

$$Z_0 = \sqrt{\frac{L'}{C'}}, \tag{2.21}$$

where L' and C' are per-unit-length values of L and C. For a single wire or the probe needle, the relation of L' to C' gets higher and Z_0 is assumed larger than 50 Ω. The chuck, which acts as capacitor, behaves vice versa.

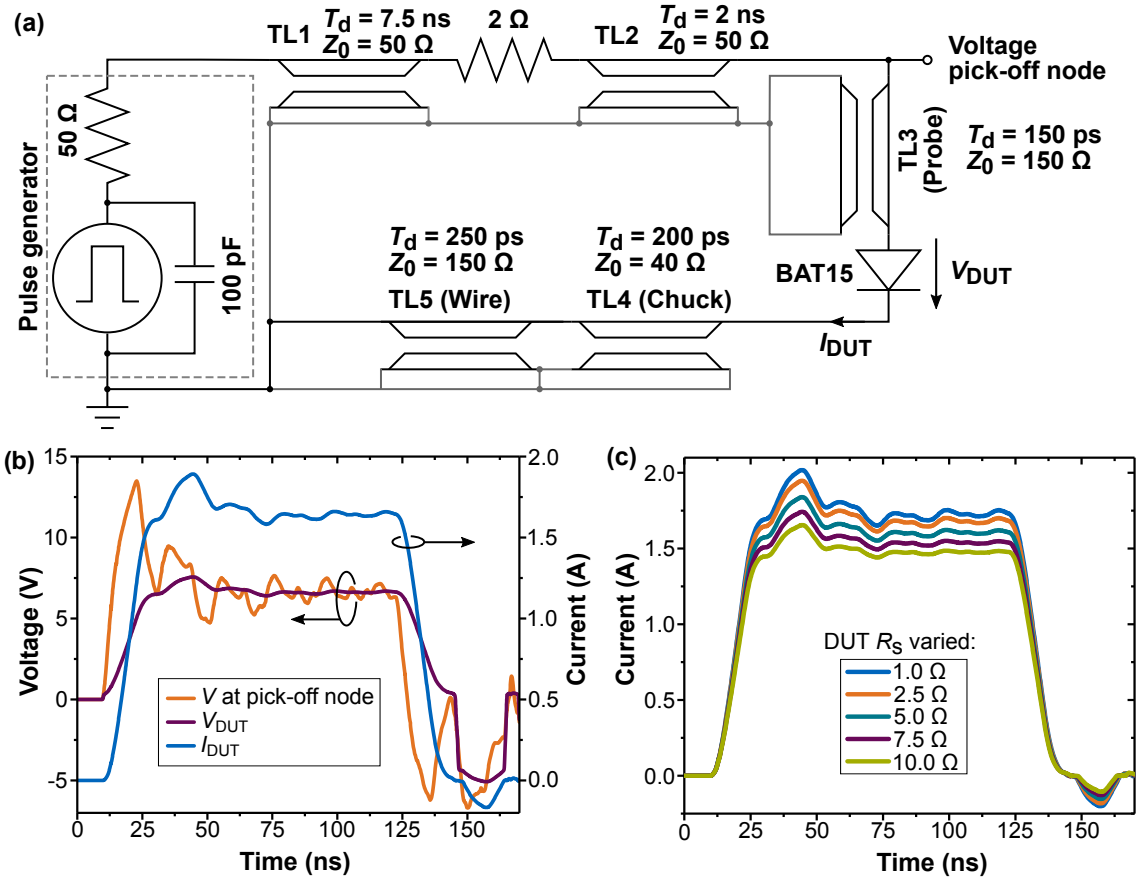

Figure 2.15: (a) LTspice schemtic of the pulse measurement setup. The pulse generator has internally a 50 Ω series resistance and is modeled with a 100 pF parallel capacitance. The output pulses have an amplitude of 47 V, a rise/fall time of 13 ns and a width of 100 ns, similar to a measured pulse. Transmission lines (lossless) TL1 and TL2 are coaxial cables of different length (indicated by the propagation delay T_d) with $Z_0 = 50\,\Omega$. The 2 Ω resistor represents the losses due to the bias tee, cables and connectors in the real setup. TL3 and TL5 act as the probe and return wire, which have a more inductive portion. TL4 represents the chuck with more conductive influence. The DUT is a SPICE model of the BAT15 diode from Infineon with $R_s = 3.75\,\Omega$. The destination of the pick-off tee in the real setup is indicated here as voltage pick-off node and measures the potential difference with respect to ground. (b) Simulated current and voltage characteristics as a function of time. Z_0 are T_d of TL3, TL4 are adjusted to get a pick-off voltage and I_{DUT} similar to the measured curves. V_{DUT} could not be measured in the real setup but can easily be extracted from the simulations and shows a similar shape as the I_{DUT} curve. (c) shows the impact of different R_s values of the BAT15 diode on I_{DUT}. The change in amplitude is not excessive, even if the resistance is changed by a factor of 10 from 1 Ω to 10 Ω.

The DUT is based on a SPICE model of the BAT15 diode without package from Infineon with all the parameters untouched, excepted the series resistance. Due to Joule heating during the pulse, the device gets more conductive and R_s is set to 3.75 Ω as previously discussed. Fig. 2.15(b) shows current and voltage characteristics of the simulation model. They behave very similar to measured curves like shown in Fig. 2.14(b), but it is obvious that the voltage at the pick-off point is not equal to the voltage drop V_{DUT} across the diode due to parasitic effects in the current return path. Different carbon deposition conditions or an altered GC thickness might lead to a change in R_s. The results of such a modification is plotted in Fig. 2.15(c), whereby the change in current is not very large.

2.3.4 Film Resistivity Measurements

The electrical resistivity of the deposited carbon films was evaluated with a four-point probing system based on a probe head connected to an RM3000 resistivity meter, both from Jandel. In such a setup, like schematically shown in Fig. 2.16(a), a constant current I is forced across the outer two electrodes, typically here 10 µA. The current flow causes a potential gradient across the film, which is measured as a voltage drop V with a high-impedance voltmeter at the two inner probes. The four individual probes have an equidistant spacing s of 1 mm, as shown in Fig. 2.16(b) for a low and in Fig. 2.16(c) for a high magnification. The individual probes are spring-loaded with a low load of 20 g each and the polished needle radius is with 500 µm quite large. This should prevent penetration into the carbon film and damage to the surface.

To accurately determine the sheet resistance R_s of the GC film, a silicon substrate with several hundred nanometer of SiO_2 is used to electrically isolate Si and GC from each other. R_s can be determined according to Smits [228] as follows:

$$R_s = \frac{V}{I} \cdot CF. \tag{2.22}$$

CF is a geometric correction factor, which depends on the lateral dimensions of the sample and the spacing of the probes. For an infinitely large sheet and a film thickness t much less than s, CF would be $\pi / \ln 2 = 4.5324$. In this work, exclusively rectangular substrates with an area of 10 mm × 10 mm ($a = d$) are used. The reduced dimensions confine the current, resulting in a larger measured potential difference at the inner electrodes. Smits provides a tabular overview in order to account for the impact of the different sizes. For $a/d = 1$ and $d/s = 10$, CF of 4.2209 was identified, which results in approximately 7 % lower values compared to an infinitely large sample.

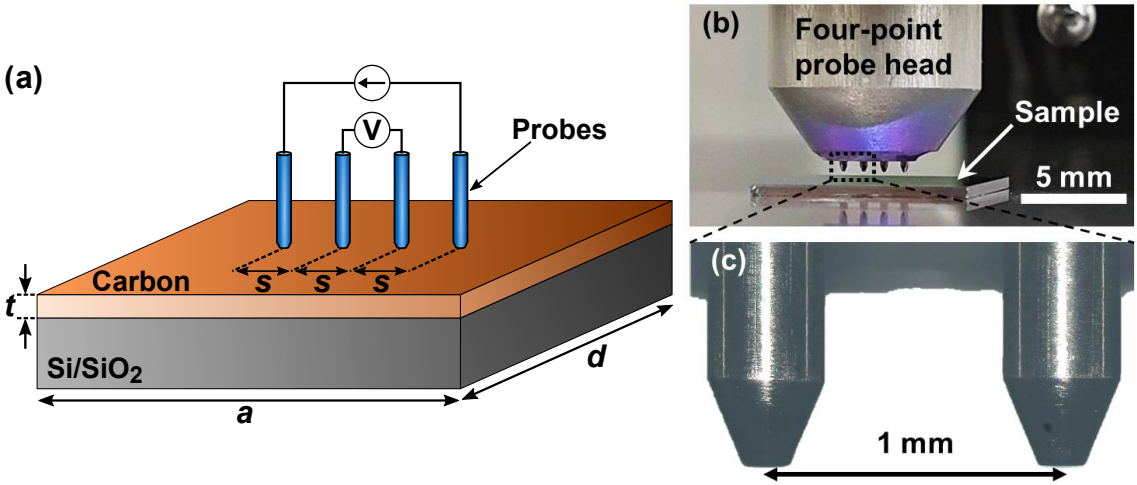

Figure 2.16: (a) A schematic illustration of the four-point probe resistivity measurement setup used. A fixed current is forced to the carbon film by the two outer probes and the subsequent voltage drop is measured across the two inner probes. The thickness of the carbon film is indicated by t and the lateral dimensions of the rectangular substrate (Si with SiO_2 on top) are given by a and d. (b) shows a photograph of the four-point probe head in close proximity to a sample, whereas a micrograph in (c) shows two probes with a higher magnification.

Further to be able to compare the individual carbon films with each other, it is necessary to specify a value independent of the film thickness t. The thickness need to be evaluated separately with other methods, like the measurement of a step height with an atomic force microscope (AFM), discussed in section 2.4. If t is known, the in-plane electrical resistivity ρ of the material can be calculated as follows:

$$\rho = R_{\mathrm{s}} \cdot t. \tag{2.23}$$

2.4 Non-Electrical Material Metrology of Graphenic Carbon

It is necessary not only to examine the deposited carbon films towards their electrical qualities but also to evaluate material properties for the individual deposition conditions and methods of the carbon materials. Key characteristics are the film thickness, surface roughness and structural configuration. Furthermore, it is crucial to evaluate with appropriate methods the individual process steps before and after the deposition of carbon and any changes to the device surface caused by an electrical stress.

2.4.1 Surface Analysis

Optical (3D Laser Scanning) Microscopy

A standard white-light optical and a confocal 3D laser scanning microscope (Keyence VK-X250) were used to evaluate the sample surface at a higher magnification. Latter allows a better resolution and measurements of the surface topology. They enable a quick and easy inspection and documentation of the surface for residues, particles, the quality of individual process steps and changes after electrical stress tests.

Scanning Electron Microscopy

The resolution of an optical microscope is limited roughly to half the wavelength of the used light — so about 200 nm to 250 nm. To overcome this limitation, electrons instead of visible light can be used. According to the de Broglie relation, they have a wavelength in the range of 10 pm (depending on their energy) [229]. The resolution gets independent of the wavelength but is rather determined by the quality of the electron optics and consequently the size of the electron spot on the sample.

Here, a scanning electron microscope (SEM) with field emission gun, a Hitachi S-4500, which allows a resolution below 10 nm, is used. The emphasis was mainly on the observation of the surface morphology after pulse stresses. Therefore, a low acceleration voltage in the range of 5 kV was used to prevent an interaction with bulk material. A low working distance between specimen surface and objective lens of 5 mm to 7 mm ensured a high resolution and the desired benefit against an optical microscope.

Atomic Force Microscopy

An atomic force microscope (AFM) is a very high resolution measurement technique to gather 3D information on a surface topography down to a sub-nanometer region [230]. A probe, which has a cantilever with a very sharp pyramidal tip at the end (see. Fig. 2.17), is scanned over the sample and traces its surface.

Common measurement modes are the contact and the tapping (non-contact) mode. Latter is used here as it provides more accurate evaluation of the surface roughness [231] and causes less damage to the tip and specimen as the tip touches the surface only for a very short time. The cantilever oscillates, stimulated by a piezoelectric actuator ('piezo'), close to its resonance frequency and interacts mainly by van der Waals and Coulomb forces between tip and surface atoms. The interaction causes a change in the amplitude of the oscillation, as the resonance frequency gets altered, and a phase shift occurs with respect to the drive frequency, even if there is only a very small variation in the surface height. A closed loop feedback control system evaluates the information and adjusts the height of the scanner accordingly to reach the set point amplitude again [232].

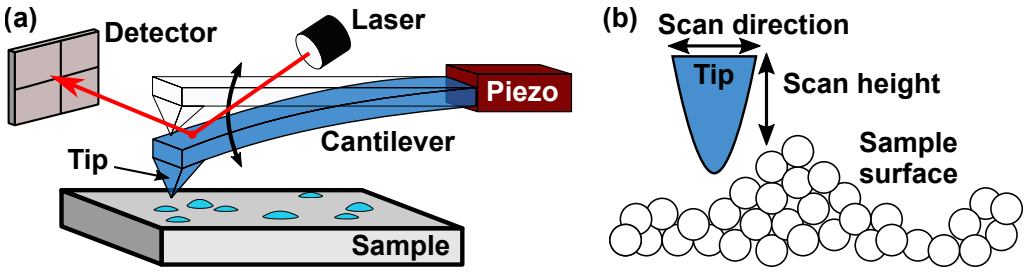

Figure 2.17: The schematic working principle of an AFM. (a) In tapping mode, an oscillating cantilever is moved in proximity across a sample. The interaction of the tip with the surface of the sample is sensed by a detector with laser light reflected from the cantilever. (b) A feedback loop alters the scanning height of the tip if a change in the surface profile, indicated schematically by atoms, is detected.

In this work, a Bruker Dimension Icon AFM was used to measure the surface roughness of deposited GC films and to get the thickness at steps where the carbon was scratched (like shown in Fig. 2.18) or etched away. The open source software Gwyddion was used for data visualization and analysis. To determine the quality of the surface and to compare it with other samples, the specimen are examined for their peak-to-valley height and for their areal root-mean-square surface roughness S_q. Latter is defined as follows:

$$S_\mathrm{q} = \sqrt{\frac{1}{mn}\sum_{y=1}^{m}\sum_{x=1}^{n}[z(x,y)-\bar{z}]^2}, \tag{2.24}$$

with n and m being the total number of data points in x- and y-direction with a certain height value z. $\bar{z}$ is the mean height.

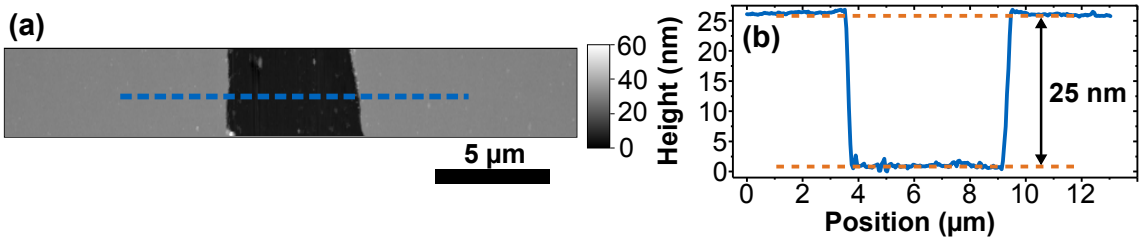

Figure 2.18: Thickness of a GC film measured with an AFM. (a) The surface morphology at a point where a narrow strip of carbon was scratched away with a test needle. The underlying silicon nitrite is almost undamaged. (b) The measured profile along the dashed line indicates a steep step with a height of 25 nm.

2.4.2 Raman Spectroscopy

Raman spectroscopy [233] is a very powerful technique to characterize semiconductors, especially carbon-based materials, like graphene, graphite, CNTs, diamond and amorphous carbon [234]. This method allows a quick — measurement time is low and no sample preparation is needed — and non-destructive analysis of a specimen in ambient condition with a high lateral resolution (spot size below 1 µm).

The basis for the so-called *Raman effect* is the inelastic scattering of photons by matter — from crystals to molecules. The incident light transmits energy and causes a vibration of the atoms/molecules and raises its energy level. The energy is finally released again in the form of a photon, but now with a slightly shifted wavelength, called Raman shift. This effect is very sensitive to the physical and chemical properties of the material under investigation and shows characteristic features in the spectrum.

The excitation source should be monochrome, like from a laser. A typical measurement setup is schematically shown in Fig. 2.19(a), which is similar to the used equipment, a B&W innoRam BWS445-532H with a 532 nm source and a more performant HORIBA XploRA PLUS with three different excitation wavelengths (532 nm, 638 nm and 785 nm). Many wavelengths from ultraviolet to near-infrared are suitable to investigate carbon [235], but typically a laser with green or red light, like 532 nm or 638 nm, is used.

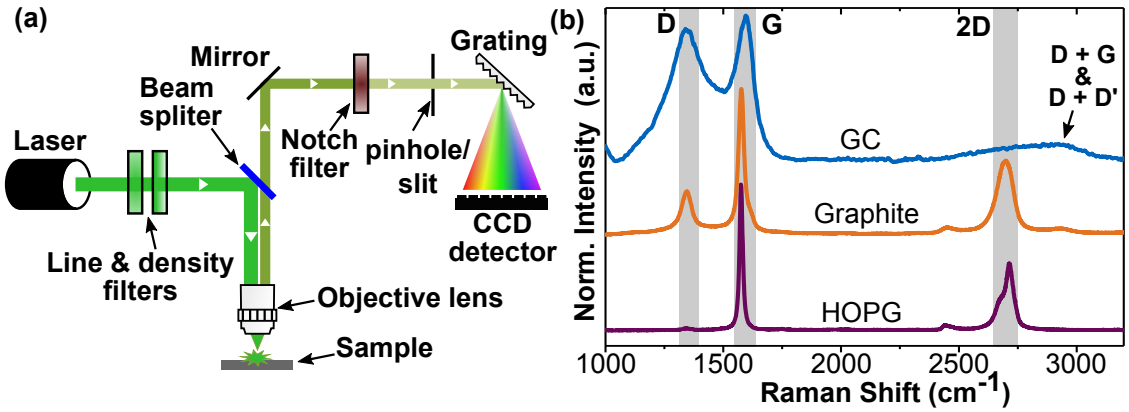

Figure 2.19: A schematic overview of the used Raman spectrometer setup in (a). A solid-state laser diode with an excitation wavelength of 532 nm, additionally filtered by a line band-pass and neutral density filter, is focused with a microscope objective lens on a sample with GC on top. The scattered and reflected light is notch filtered and in the detector spectrally split by a diffraction grating and detected by a CCD sensor. Measured Raman spectra, with offset for clarity, are in (b) for HOPG, graphite, and a typical GC film. The dominant graphitic features — D, G and 2D — are highlighted, but GC hardly shows the 2D band, instead shows also combination modes at higher Raman shift values.

In carbon allotropes, the specific vibration frequencies allow an evaluation of the characteristic structure in terms of sp^2 or sp^3 content, quality and doping of the material [236–239]. The most important feature in graphitic/graphenic materials is the G (graphite) band (or peak), which is related to the stretching of C-C bonds [240,241]. It is present in all sp^2 hybridized C systems and is located at $\sim 1580\,\mathrm{cm}^{-1}$, as shown in Fig. 2.19(b). The D (disorder) band ($\sim 1350\,\mathrm{cm}^{-1}$) appears when the lattice periodicity is broken by a disorder mechanism, like defects. HOPG exhibits nearly perfect crystallites of sp^2 bonded carbon atoms and hence does not show this feature, in contrast to a typical GC film.

The ratio between the D and G peak and their individual width is often used to interpret the quality of disordered or amorphous carbon [238, 242]. The determination of the correct height of the individual peaks by fitting is not straight forward and can lead to a misinterpretation [242–244]. In this work, if fitting is needed, the spectrum is deconvoluted with two Gaussian shaped curves. When the height is reliably extracted, even the crystallite size of nano-/polycrystalline carbon can be determined [245]. The 2D band (or named G') in the range $2500\,\mathrm{cm}^{-1}$ to $2800\,\mathrm{cm}^{-1}$ is a second-order sp^2 signature and is a two phonon process with opposite wave vectors and does not require defects [241]. Its position and intensity is sensitive to the 3D structure and the stacking of the graphitic layers [237]. GC in addition, shows a broad band at $2900\,\mathrm{cm}^{-1}$ to $3000\,\mathrm{cm}^{-1}$ (D+D' and D+G [241, 246, 247]), which are combined defect-induced modes.

2.5 Finite Element Simulations

The behavior of the diode during an ESD pulse can not be measured directly, as the event is very short and a look inside is not possible during this time. To get a deeper insight into the current and especially the heat distribution in the diode during the pulse, coupled time-dependent simulations based on the finite element method (FEM) were performed with *COMSOL Multiphysics*. The software allows the coupling of different physical domains. Relevant are here the electrical and thermal domain as the current generates Joule heat (see Eq. 1.4), while the temperature increase causes a change in the material parameters, which in turn lead to a change in the current distribution. A thermomechanical expansion was neglected in the analysis to reduce the simulation complexity and time effort.

Device Model

The geometry of the model used should be close to the real device, but not too detailed as this would increase the amount of mesh elements and the computing time. The BAT15 diode is a cylindrical diode with axial symmetry around the center of the active area. Therefore, not a complete 3D geometry need to be simulated, but COMSOL allows the simplification to an axisymmetric model. Only a half of the structure has to be built in 2D, based on the BAT15 structure with the same

dimensions, doping profile and metallization, as illustrated in Fig. 2.20(a). The boundary conditions are set in a way that the numerical solution of the problem is performed in 2D only, but the solution corresponds to a symmetrical 3D geometry, as shown in Fig. 2.20(b).

It is in addition not necessary to consider the complete bulk Si substrate of the real device because an ESD pulse is very short and the heat cannot spread far inside the materials during that time. As a good compromise between reliable results and short simulation time, a total height of 30 µm and a diameter of 40 µm was chosen.

A homogeneous doping profile for the highly doped substrate, the low/moderately doped epi-layer and the guard ring was set. Hence, the conductivity is constant within the individual regions at a fixed temperature. The top metallization is always Ti (50 nm) and Cu (1.35 µm). The contact material to Si is GC at a variable thickness. If it is 0 nm, titanium is in contact to Si, but as a simplification it is assumed that no silicidation to TiSi has occured — the TiSi thickness is 0 nm.

The backside of the device is at fixed ambient temperature and acts as heat sink and as electrical ground, whereas all surrounding boundaries are thermally and electrically isolated. An exception is the electrical terminal at the upper outer edge of the copper, where a current is applied symmetrically all around, unlike in the real device, where this is done at a particular spot by the probe needle. The waveform of the current is modeled very close to the measured pulse from the HP 214B through a diode, as can be seen in Fig. 2.21.

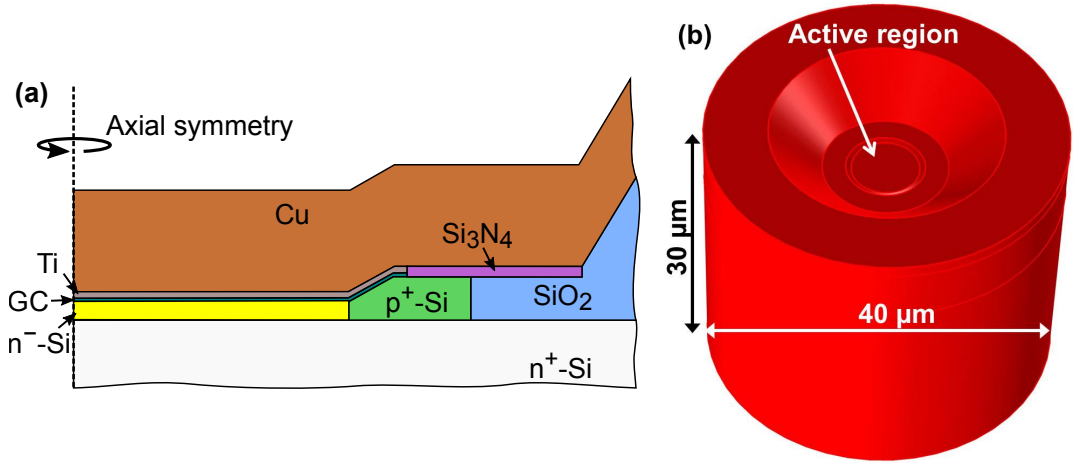

Figure 2.20: The geometric model of the BAT15 diode used in FEM simulations. (a) shows a section of the used 2D model of a BAT15 drawn in COMSOL. Geometric variations occur only in radial and vertical, but not in angular direction. The axial symmetry is around the center of the active region. (b) A rotation of the 2D model results in a cylindrical 3D solid. The height is set to 30 µm and the radius to 20 µm.

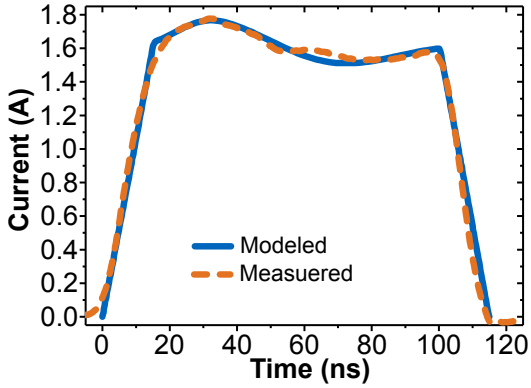

Figure 2.21: The modeled waveform in COMSOL in comparison to a real 100 ns long pulse. The modeled one matches with a measured curve. It has the same rise/fall time of 15 ns, a similar overshoot and 'ringing' behavior and the same average amplitude level of about 1.6 A (3.5 MA/cm^2).

Thermal Domain

As previously mentioned, the current flow generates Joule heat H, which is modeled and solved in COMSOL with the physics for *heat transfer in solids* [248]. The underlying equation is

$$\underbrace{\rho C_\mathrm{P}(T)\frac{\partial T}{\partial t}}_{Heat\ storage} \underbrace{-\nabla\cdot(-k(T)\nabla T)}_{Heat\ conduction} = \underbrace{H}_{Heat\ source}\quad, \tag{2.25}$$

with the material density ρ, the heat capacity C_P and the thermal conductivity k. These parameters change as the temperature increases, except ρ is assumed to be constant. SiO_2 and Si_3N_4 are modeled independent of temperature with values available in the software. Reported temperature-dependent parameters are used for Si, Ti, Cu and GC [249, 250]. The temperature characteristics for the individual solids are shown in Fig. 2.22.

The thermal properties of the used GC are strongly influenced by the deposition method and process conditions and do not have any distinct literature values. Instead, k and C_P of Acheson graphite were used as it is an artificial or rather polycrystalline graphite [100] and it is likely to have thermal properties close to the used graphenic carbon. However, the used film is very thin and it is expected that a deviation of the literature values to the real parameters only have minor impact on the results. It is further assumed in the simulation model that the GC film has the same values in- and out-of-plane, as it should be less anisotropic than Graphite.

Electrical Domain

The fundamental equation here is Ohm's law (Eq. 1.3), which leads to Joule heating and hence, it is necessary to consider a temperature-dependent electrical conductivity σ. Reported values are used only for Ti [251] and Cu [252]. If the temperature

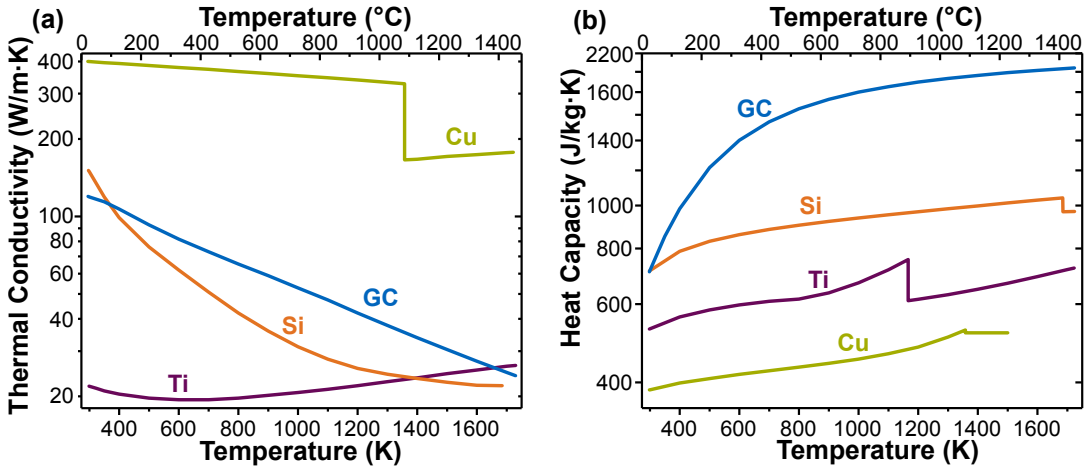

Figure 2.22: Temperature-dependent characteristics for the thermal conductivity k in (a) and heat capacity C_P in (b) for Si, Ti, Cu and GC. The values are taken from Refs. [249, 250]. A discontinuity in the curve in general indicates a transition from solid to liquid, except for Ti in (b) where only the crystal phase changes.

range of the electrical or thermal parameters are exceeded during the simulations, the values where extrapolated. The conductivity of silicon depends on the doping level and hence, no exact literature values can be used. According to Sze and Ng [114], σ can be expressed as a function of the charge carrier mobility μ and the free charge carrier concentration n (for electrons; in p-type Si with the hole density p) with only one charge type is present:

$$\sigma(T) = \frac{1}{\rho(T)} = \mu(T) \cdot q \cdot n(T). \tag{2.26}$$

The charge carrier density in silicon is determined by the doping concentration n_ext, under the assumption that all dopants are ionized, and the intrinsic charge density n_i:

$$n(T) = n_\mathrm{ext} + n_\mathrm{i}(T). \tag{2.27}$$

The temperature dependence of n_i is described with [114]:

$$n_\mathrm{i}(T) = 2 \cdot \left(\frac{2\pi k_\mathrm{B} T}{h^2}\right)^{3/2} \cdot (m_\mathrm{e}^* m_\mathrm{h}^*)^{3/4} \cdot \exp\left(-\frac{E_\mathrm{g}(T)}{2k_\mathrm{B}T}\right), \tag{2.28}$$

where h is the Planck constant and m_e^* and m_h^* are effective electron and hole masses, respectively. The latter can be expressed in terms of the electron rest mass m_0 as (a dependency on the temperature was neglected):

$$m_\mathrm{e}^* = 1.08 \cdot m_0, \tag{2.29}$$

$$m_\mathrm{h}^* = 0.55 \cdot m_0. \tag{2.30}$$

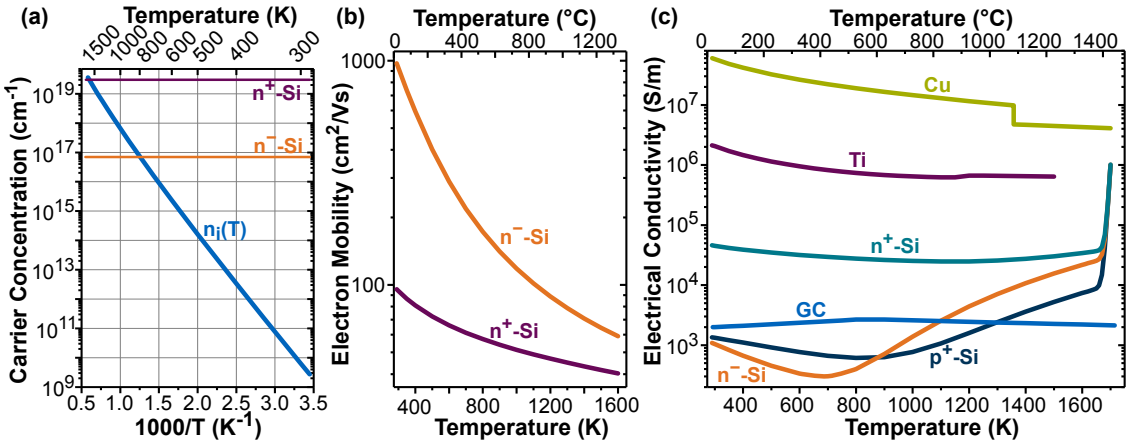

Figure 2.23: (a) Intrinsic carrier concentration as a function of reciprocal temperature. The doping level of the used Si substrate and epi are indicated. (b) Electron mobility as a function of temperature for high and low doped Si. (c) Electrical conductivity of Ti and Cu based on literature values [251, 252] and of the used n$^-$-, n$^+$-, p$^+$-Si and GC based on calculated values. A discontinuity in the curves and the strong increase of Si at $\sim$1650 K (melting point is 1685 K [250]) indicates the transition from solid to liquid.

The temperature dependence of the silicon band gap can be expressed by

$$E_{\mathrm{g}}(T) = E_{\mathrm{g}}(0) - \frac{\alpha T^2}{\beta + T}, \tag{2.31}$$

where $E_{\mathrm{g}}(0) = 1.169\,\mathrm{eV}$ is the band gap at absolute zero temperature and $\alpha = 4.9 \times 10^{-4}\,\mathrm{eV\,K^{-1}}$ and $\beta = 655\,\mathrm{K}$ are fitting constants [114].

Fig. 2.23(a) shows the calculated n_{i} as a function of temperature in comparison to the fixed n_{ext} of the utilized substrate and epi-layer. At roughly 800 K, Si becomes here intrinsic for a lower doping level, as now the number of thermally generated electron-hole pairs dominates, whereas a temperature over 1500 K is needed that the donor density does no longer dominate the carrier concentration at a higher donor density.

The carrier concentration increases with temperature, but the charge carrier mobility behaves in the opposite way. It depends also on the doping level and can be modeled according to Arora *et al.* [253]. The electron mobility μ_{e} is expressed as follows (the hole mobility is not shown here):

$$\mu_{\mathrm{e}}(T) = 88 \cdot \left(\frac{T}{300}\right)^{-0.57} + \frac{7.4 \times 10^8 \cdot T^{-2.33}}{1 + \dfrac{N_{\mathrm{D}}}{1.26 \times 10^{17} \cdot \left(\dfrac{T}{300}\right)^{2.4}} \cdot 0.88 \cdot \left(\dfrac{T}{300}\right)^{-0.146}}. \tag{2.32}$$

The corresponding curves of $\mu_e(T)$ for different doping levels are shown in Fig. 2.23(b). This equation was validated only up to 500 K but was used here for simplicity to much higher values as the general trend is assumed to be still valid.

The calculated values of σ as a function of temperature of Si with different doping densities are shown together with Ti, Cu and GC in Fig. 2.23(c). The sharp increase in σ at $\sim$1650 K for Si is due to the fact that molten silicon has a much lower resistivity [254].

For the characteristics of the electrical conductivity of GC, no direct reference can be made to literature values. As discussed later in chapter 4, the out-of-plane resistivity ρ is 50 mΩ cm (equal to 2000 S m^{-1}), according to measurements at room temperature of films deposited in a CVD process. The behavior of the resistivity at higher temperatures was assumed to behave like published data from Pierson [100] and Noyes [255]. For simplicity, these values were assumed for in- and out-of-plane resistivity as the layer is very thin. The conductivity is modeled in such a way that it increases linearly up to 800 K by 33 %. This is in contrast to conventional metals as GC becomes a better conductor at increasing temperatures. Nevertheless, σ is modeled to be constant between 800 K to 900 K and at higher temperatures, the behavior changes again. Because then the conductivity decreases until the room temperature value is reached at 2000 K. As can be seen in Fig. 2.23(c), GC is getting even less conductive than low doped silicon at $T > 1100$ K.

3 Graphenic Carbon Deposition and Diode Fabrication

This chapter deals with the preparation and cleaning procedures of the used substrates and the subsequent deposition of the graphenic carbon by chemical and physical vapor deposition. Basic theoretical considerations for these processes and the used individual parameters are discussed. Finally, the diode fabrication procedure after the GC deposition is presented.

3.1 Substrate Preparation and Cleaning

The used silicon substrate needs to be prepared appropriately before any carbon is deposited. The Infineon BAT15 test vehicle, described in section 2.2.4, is generally used in this work as substrate to deposit GC and to evaluate the resulting metal-semiconductor contact. The wafer was sawed with a blade dicing system into squared $1\,\mathrm{cm} \times 1\,\mathrm{cm}$ samples for ease of use and for the compatibility with the used equipment. The top side of the wafer was covered with photoresist to protect it during the sawing process from particle damages.

The cleaning of the substrate is essential to obtain an 'ultraclean' Si surface to enable the desired reliability tests and the comparison to a commercially manufactured diode. This means that the number of impurities on the semiconductor surface should be reduced as close to zero as possible. The contamination sources can be organic or metallic films, discrete particles (down to atomic size) or absorbed gas molecules [256, 257]. Highly mobile ions from alkali metals such as sodium (Na) or potassium (K) are among others very critical. They can cause device defects and yield losses due to increased leakage currents, shifted device characteristics and a reduced oxide breakdown voltage after a high temperature processing. But the most critical are heavy metals like copper (Cu), iron (Fe), nickel (Ni) and gold (Au) [257, 258]. They cause traps and generation/recombination centers, cause severe leakage currents and early junction breakdowns and influence the carrier lifetime. Especially Cu is very severe, as it diffuses very easily in Si [259], even at low temperatures [260]. But not just the cleaning, also handling and processing steps of the semiconductor samples need to be done with extreme care to avoid device degradation and reliability problems.

RCA Clean The cleaning procedure used in this work is essentially the so-called *RCA standard clean*. It was developed by W. Kern at the Radio Corporation of America (RCA) and is based on hot alkaline and acidic hydrogen peroxide solutions [256]. The two basic steps are called standard clean 1 and 2 (*SC-1* and *SC-2*).

The SC-1 is a solution of ammonium hydroxide (NH_4OH, 28 vol%), hydrogen peroxide (H_2O_2, 31 vol%) and deionized (DI) water (H_2O), here in a volumetric ratio of 1:1:6 at a temperature between 50 °C and 70 °C. It is effective in removing organic residues and forms amino-complexes with many metals, including Cu and Au. But also the removal of particles from the surface was reported [261].

The SC-2 is a solution of hydrochloric acid (HCl, 36 vol%), H_2O_2 (31 vol%) and H_2O, here in a volumetric ratio of 1:1:6 at a temperature between 60 °C and 75 °C. The intention is to remove ionic and metallic impurities and the complexes formed during the SC-1 step.

Special attention should be paid to the purity of the used DI water and chemicals — only 'semiconductor grade' solutions should be used as they contain a very low level of impurities. DI water is not only used to dilute chemicals but also used for rinsing between the individual steps to remove traces of chemicals from the surface. It is known that metal ions are easily deposited on the surface by DI water [262]. The used ultrapure water with a conductivity of 18.2 MΩ cm must also be treated with care. It has been reported, that residual contaminants can affect the reliability and the yield of devices [263].

But even this is not enough, the vessels used for the individual solutions must under no circumstances be made of borosilicate glass (popular trade names are Pyrex and Duran), as this contains boron, aluminum and alkali metals which can be leached out by the cleaning solutions [256]. Here, polytetrafluoroethylene (PTFE), perfluoroalkoxy alkanes (PFA) and quartz beakers with sample holders made of PTFE are used to minimize the risk of an unwanted contamination.

In the scope of this work the RCA cleaning procedure alone is not sufficient because the sawed samples are covered with protective photoresist. Before the resist is stripped, the samples are precleaned in an SC-2 solution in an ultrasonic bath (45 kHz) to remove Si particles and metal traces from the dicing process, especially Cu as it diffuses easily in Si at lower temperatures. The resist is subsequently removed in acetone and isopropyl alcohol (IPA) at 70 °C in an ultrasonicator. Afterwards the previously described RCA clean is executed.

On the test vehicle is an additional 20 nm thick protective SiO_2 layer on the backside and the active diode region, which has to be removed before carbon is deposited. This was etched in hydrofluoric acid (HF) with a concentration of 5 % for 2 min 30 s, leaving a hydrogen-terminated Si surface. Afterwards, the samples were rinsed in DI water to get rid of the chemicals. The subsequent drying of the substrate is a severe step. To do this only in air atmosphere can leave watermarks on the surface and the step would additionally be too time-consuming, which promotes

the formation of SiO_2. Blowing dry with compressed air or N_2 was discarded because it cannot be excluded that particles could get onto the sample at this step. Finally, the drying step after DI water rinsing was completed by a short dip in hot IPA as this dries very quickly without leaving residues and minimizes the risk of contaminations [264].

The samples must be transferred to the process chamber very quickly, as the terminated surface is only stable for a few minutes in ambient condition [265]. Otherwise, adsorbed moisture and oxygen from the air will cause a native oxide to form. This in turn would prevent the formation of a clean C-Si contact and could have a negative influence on the final device performance [266].

3.2 Chemical Vapor Deposition of Carbon

Chemical vapor deposition (CVD) is generally described as the deposition of a desired solid material on a surface of a substrate by a thermal reaction or decomposition of a gaseous precursor. It is a very versatile tool to deposit many materials at wafer scale with high uniformity, purity and a good control on thickness and crystallinity.

3.2.1 Theoretical Considerations

The CVD process to obtain carbon materials is based on the thermal decomposition of light hydrocarbons in the absence of oxygen — known as pyrolysis. The non-catalytic deposited carbon is frequently called pyrolytic carbon or pyrocarbon [267] and should not be misinterpreted with HOPG, which consists only of 'perfect' graphene layers. However, pyrolytic carbon films are dominated by sp^2 hybridizied C atoms and contain a certain fraction of hydrogen (H). Nevertheless, depending on the process condition, the films can also be sp^3-rich (diamond-like), especially when fabricated with enhanced CVD methods [268], such as rf-plasma CVD.

A ternary phase diagram of such hydrogenated amorphous and disordered carbon materials, as illustrated in Fig. 3.1, is frequently used to describe these based on the amount of H, sp^2 and sp^3 hybridized C atoms. The terminology used here is described by Silva [269] and shows a slightly more recent description than the often cited version of Ferrari *et al.* [238]. No matter which diagram is considered, it gets obvious that a high sp^2 content leads to a carbon or amorphous carbon (a-C) material of graphitic nature, whereas an increasing fraction of sp^3 bonds results in tetrahedral a-C (ta-C), which is more close to diamond-like carbon. An incorporation of hydrogen leads to the hydrogenated pendants a-C:H and ta-C:H. The hydrogen changes not only mechanical properties [117] — of higher importance for this work is the deterioration of the electrical conductivity, as demonstrated with a-C and a-C:H films [270]. A further increase in the H content, roughly higher than 50 %, causes a polymerization up to a content of 75 %. Afterwards, no films are possible anymore.

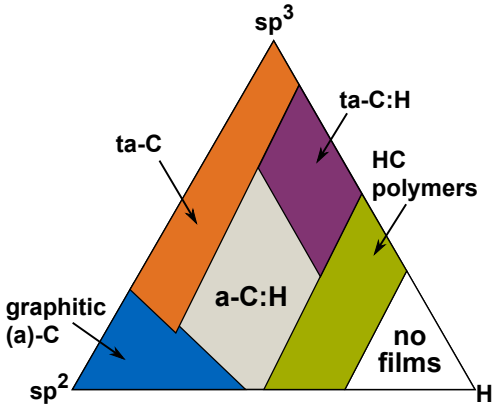

Figure 3.1: (a) Ternary phase diagram of different amorphous and disordered carbon-hydrogen alloys. The materials are classified on their ratio of sp^2 and sp^3 hybridized C bonds and the amount of incorporated H. Adapted from Ref. [269].

Understanding the chemistry and kinetics of the involved gas phase reactions is not straight forward and involves many reaction pathways. The group of K.J. Hüttinger [267,271,272], among others [273–275], made extensive investigations to give a better understanding.

However, some key requirements for the deposition of graphenic carbon on the BAT15 diode test vehicle (see section 2.2.4) are essential to make GC applicable for the usage in metal-semiconductor contacts:

- A low deposition temperature and time to prevent or minimize a diffusion of dopants in Si;
- a low resistivity parallel and perpendicular to the substrate surface, whereas latter is important for the diode;
- a high uniformity and smoothness to act as good diffusion barrier and enable a good contact to the top metallization; and
- a high adhesion to the substrate.

If the individual process parameters are chosen accordingly, the deposition is non-catalytic on all hot surfaces. The following parameters of the CVD process must be considered:

- The used type of hydrocarbon gas;
- the deposition temperature;
- the absolute pressure in the reactor as well as the partial pressure of the hydrocarbon gas;
- the gas flow and the residence time of the gas molecules in the hot reactor volume;
- the deposition time; and
- the ratio of the surface area of the substrate to the free volume in the deposition space and type of reactor.

Deposition Temperature

The choice of the precursor is mainly influenced by the desired temperature range. The doping profile of the BAT15 test vehicle allows temperatures up to 1000 °C for a few minutes without a reasonable change in the electrical properties of the used substrate, because the diffusivity of dopants in Si is still acceptable at this temperature [276].

Typical hydrocarbon gases used for the pyrolysis in a CVD process are methane (CH_4), acetylene (C_2H_2), ethylene (C_2H_4), ethane (C_2H_6) and benzene (C_6H_6). Latter is liquid at room temperature. Desirable is here a high C/H ratio, as a high H_2 content in the gas phase could lead to more incorporated hydrogen in the film.

From a thermodynamic point of view, the precursors can be differentiated with regard to their feasibility of a chemical reaction. The Gibbs energy of formation ΔG_f^0 provides a metric for measurement. Fig. 3.2(a) shows ΔG_f^0 per carbon atom as a function of temperature and simply indicates the thermal stability of the respective molecule against other hydrocarbons. All of them are unstable with respect to their elements at temperatures above room temperature except of CH_4 and C_2H_6, which are stable below ∼500 °C and ∼200 °C, respectively. C_2H_2 is very instable at low temperatures so that it must be dissolved in acetone but gets more stable at higher temperatures — but still has a high ΔG_f^0.

Acetylene and ethylene are very favorable for a usage because they are among the more unstable hydrocarbons and do have a good C/H ratio — H is undesirable. Fig. 3.2(b) and (c) show simulated gas phase analysis at the outlet of a reactor at different temperatures. C_2H_2 shows already a higher fraction of reaction products at 800 °C than C_2H_4. Consequently, a deposition of carbon is more likely. As can be

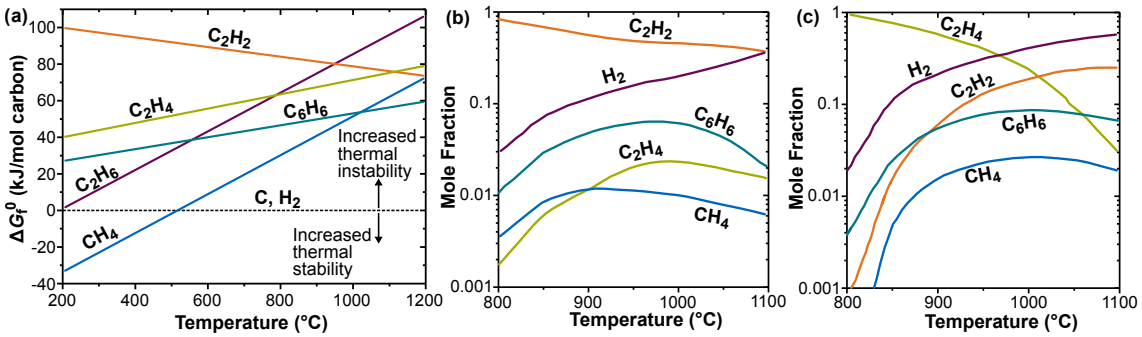

Figure 3.2: (a) Gibbs free energy of formation (ΔG_f^0) per C atom as a function of temperature for some hydrocarbons. For elements in their standard states applies $\Delta G_f^0 = 0\,\mathrm{kJ/mol}$. The higher ΔG_f^0, the more unstable is the molecule and it decomposes into other hydrocarbons. If the reaction time at high temperatures is long enough, the only products would be carbon and hydrogen. Adapted from Ref. [273]. Computational predictions from Ref. [277] of major gas phase reaction products as a function of temperature are shown in (b) for C_2H_2 and in (c) for C_2H_4 as initial precursor gas. An increase in temperature leads to a stronger decomposition and a raised fraction of reaction products. The simulation was performed at a gas pressure of 80 mbar and a residence time of 0.5 s.

seen in Fig. 3.2(c), the fraction of ethylene is progressively decreased at increasing temperatures and major reaction products are H_2 and C_2H_2.

The temperature in the reactor is responsible not only for the pyrolysis reactions but also for the crystallinity of the deposited carbon film as illustrated schematically in Fig. 3.3. The preferred orientation of graphitic films at low substrate temperatures is low-textured [278]. This means that the grain size is small and there is an increased misorientation between individual crystallites. So, a larger content of amorphous carbon can be assumed, but a higher defect density in the lattice promotes the formation of covalent C-C bonds between the individual layers and grains. Furthermore, the formation of Si-C bonds becomes more likely, which results in a good electrical contact and a strong adhesion to the substrate. Electrical, mechanical and thermal properties are more isotropic as discussed by Guellali *et al.* [279]. Higher deposition or heat treatment temperatures lead to a higher textured material with larger grain size and increased anisotropic characteristics. Especially the electrical conductivity in-plane gets closer to graphite or HOPG but deteriorates out-of-plane.

The graphenic carbon desired in this work should still have a certain degree of disorder because this results in more isotropic properties but at the same time have a high amount of sp^2 bonds to give a low film resistivity. It has been shown that a deposition or annealing temperature $\leq 1000\,°C$ is sufficient to achieve a resistivity (in-plane) of about $1\,m\Omega\,cm$ [169, 176].

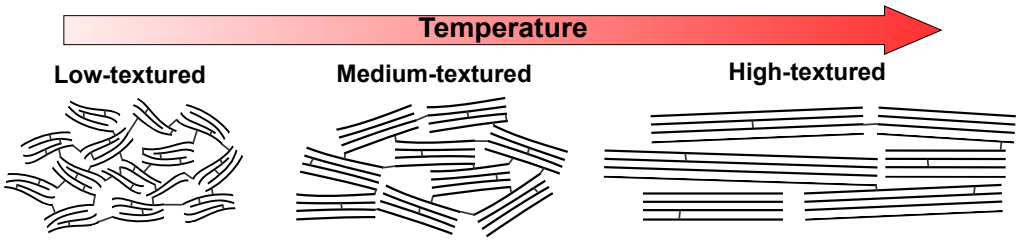

Figure 3.3: Schematic representation of the preferred orientation of deposited GC at different substrate temperatures after Ref. [280]. The carbon crystallites become larger and better orientated to each other at an increased temperature. It is further assumed that the defect density is reduced, which leads to a lower number of covalent bonds between the individual layers and crystal grains.

Pressure, Gas Flow and Residence Time

In order to evaluate the influence of different parameters on the pyrolysis of ethylene, the simplified reaction model in Fig. 3.4 is considered first. The formation of solid carbon originates only to a minor extent from C_2H_4 but rather results from the main reaction products C_2H_2 and especially C_6H_6. A higher partial pressure of the precursor gas is directly related to the amount of molecules and accelerates the conversion of hydrocarbons [281] similar to an increased temperature, which in turn

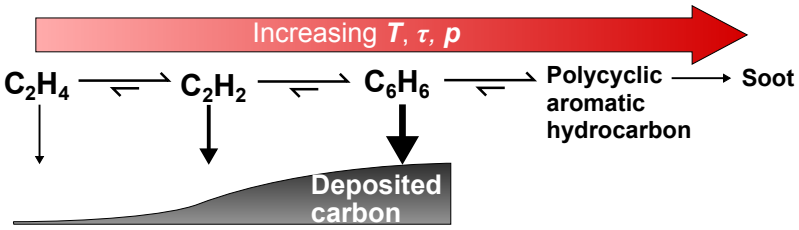

Figure 3.4: A simplified reaction scheme for the pyrolysis from ethylene (C_2H_4) to solid carbon. Only reaction products which contribute to the depostion of C are shown. The thickness of the arrows indicate the deposition rate of individual hydrocarbons (after Ref. [283]) and is more likely from acetylene (C_2H_2) and benzene (C_6H_6). The process is mainly driven by the temperature T, residence time τ and partial pressure of hydrocarbons p in the reactor. If they are chosen to high, undesired polycyclic aromatic hydrocarbons and soot partials can form. Based on figures from Refs. [271, 282, 284].

leads to a higher carbon deposition rate [272, 282]. For the sake of completeness, it should be mentioned that the absolute pressure can be increased by adding another gas, typically H_2, N_2 or Ar, which has an influence on the chemical reactions and deposition rate [282]. However, this will not be considered here.

The residence time τ is another important parameter to consider. This is the time the individual gas molecule has to flow through the hot reactor and it is consequently the time to react or decompose further [281]. τ depends directly on the reactor volume V and the set flow rate Q (in sccm). As the pressure p and temperature T in the hot zone differ from standard conditions ($p_0 = 1000\,\mathrm{mbar}$, $T_0 = 273.15\,\mathrm{K}$), they need to be considered as follows [285]:

$$\tau = \frac{V}{Q}\frac{p}{p_0}\frac{T_0}{T}. \tag{3.1}$$

A higher residence time does not only increase the deposition rate [282] but also impacts the texture of the grown film heavily [284–286]. Simplified, the longer τ, the better is the texture.

But if these parameters are chosen improperly (too high), the pyrolysis will not only lead to light hydrocarbons, but also the formation of large polycyclic aromatic hydrocarbon (PAH) molecules due to a gas phase nucleation can be observed [287]. Especially the pyrolysis of acetylene leads to large PAHs [277]. An accumulation of these molecules easily causes the formation of soot in the gas phase. They should be avoided as they are randomly hybridized [113] and hence, have unwanted electrical properties if deposited on the substrate. In addition, soot particles act as nucleation centers and alter the crystallite size of the film [100].

Deposition Time and Geometry

Beside the residence time, the total deposition time impacts the texture of the pyrolytic carbon film. De Pauw *et al.* [286] have shown that the growth of a carbon

film at 1100 °C starts with the formation of islands on the Si substrate. The surface still shows a granular structure after 5 min at a deposition rate of 11 nm/ min. Under the same process conditions, just for two hours now, the texture changes from a granular to a layered (high-textured) one.

The ratio of the substrate surface area to the volume area is another factor to be considered for the deposition of carbon as it impacts the reaction kinetics. Depending on the ratio, homogeneous gas phase or heterogeneous surface reactions will dominate the overall process and finally the deposition rate [271, 288].

3.2.2 Process Description

Two different CVD setups were used to deposit graphenic carbon on the substrates with a size of 10 mm × 10 mm. These furnaces are more suitable for experimental processes and not for industrial production on a wafer scale. Schematic illustrations of the setups are shown in Fig. 3.5. One was used for the pyrolysis of C_2H_2 while the other one was connected to C_2H_4 gas. However, both systems have in common that they are low pressure hot-wall reactors with resistive heaters and to a certain extent they allow a 'rapid thermal processing'. The samples can either be transferred directly into the hot reactor zone (Fig. 3.5(a)) or the heater can be moved over the substrates (Fig. 3.5(b)). This allows much steeper heating ramps than with simultaneous heating-up of the furnace and the substrate. Cooling works similarly, which reduces the total process time and a negative influence of a high temperature on the doping profile. Investigations by Reznik *et al.* [289] have shown that a very slow cooling rate releases more H_2 from the film, but this can cause undesired large pits in the film, which is not desired here. As the heating systems of the two furnaces did not touch the quartz tube, the measurement of the temperature in the free space between them is possible by a thermocouple.

It is important to thoroughly clean the utilized quartzware of the CVD setup to perform the desired reliability tests of the MS contact. For this purpose, organic residues from production and handling are removed first with acetone and IPA. Afterwards, an SC-2 cleaning step for about one hour and a short etching of the SiO_2 surface with diluted HF acid ($< 1\,\%$) were performed.

The RCA-cleaned and H-terminated test vehicle substrates should be loaded as fast as possible to the CVD equipment. This was done within $\sim$ 5 min after the HF dip, explained in section 3.1, to prevent the formation of a native oxide. The whole reactor volume was therefore vented with nitrogen and the sample was placed under N_2 flow on the quartz shovel at room temperature. After closing the chamber, it was immediately evacuated again. A typical base pressure was in the range of 7×10^{-2} mbar. The cold samples and also the chamber was subsequently purged under a hydrogen gas (99.9999 % purity) flow of 250 sccm at 0.6 mbar to remove air residues and moisture from the substrate and quartzware, which could promote the growth of SiO_2 on the Si substrate. In addition, they can also impact the growth

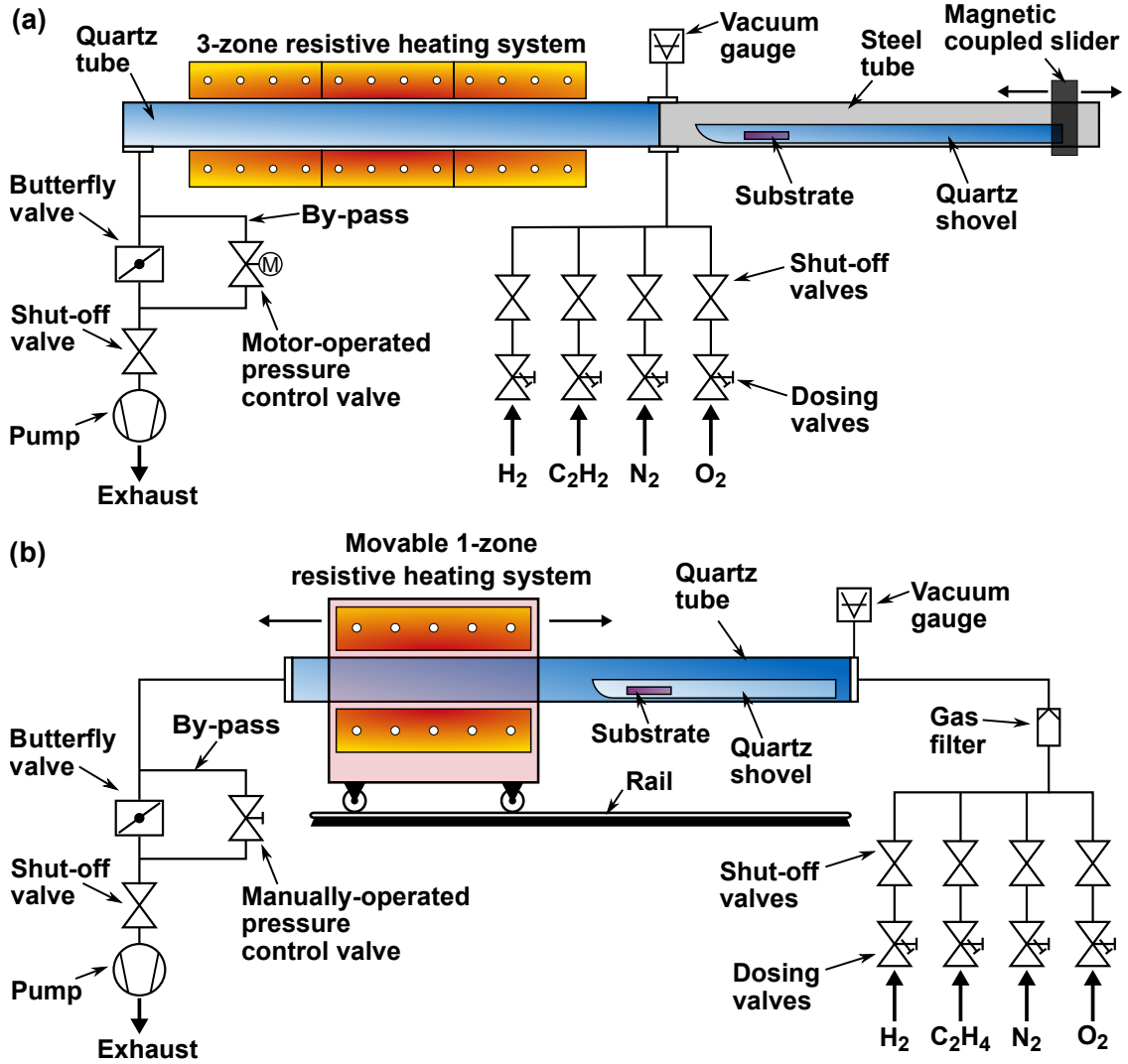

Figure 3.5: (a) A schematic illustration of the used low pressure hot-wall CVD system for the pyrolysis of acetylene. The system is divided into two main parts. A furnace with three-zone resistive heater (approx. up to 1300 °C) with quartz tube and a steel tube (both with an inner diameter of 40 mm) for the loading and cooling of the sample outside the hot zone. The substrates are placed on a quartz shovel and are transferred by a manually operated magnetic loading mechanism to the hot reactor zone. The gas flow of the individual gases is regulated by dosing and shut-off valves. A motorized throttling valve at the exhaust side is employed to control the pressure in the reactor automatically with feedback from the gauge meter. (b) A schematic overview of the used low pressure hot-wall CVD equipment for the pyrolysis of ethylene. The furnace, a single-zone heater (up to 1100 °C), can be moved on rails along a quartz tube with an inner diameter of 25 mm. The substrates can be loaded onto a quartz shovel by opening one side of the tube. A 3 nm gas in-line particle retention filter is employed before the entry to the tube to additionally clean the gas. The pressure inside the system is adjusted by a manually-operated throttling valve.

mechanisms, deposition rate and aid the formation of PAHs. Consequently, a soot particles formation during the pyrolysis process is promoted [290]. It is therefore essential to carry out a leakage check of the setup after purging and before starting the deposition procedure.

However, condensed PAHs are typically observed on the quartz tube after the gas leaves the hot zone, as shown in Fig. 3.6. But this does not imply that they are present in the whole volume of the reactor. The sample(s) is normally placed in the middle of the furnace. It is assumed that at appropriately chosen parameters, PAHs and possibly soot particles form only after the center of the hot zone and do not affect the GC deposition on the substrate.

During the deposition process, all hot surfaces get coated with GC including the inner side of the quartz tube, shovel and samples. A photograph of the latter two is shown in Fig. 3.7. After the process has been completed and the samples have been unloaded, air was used to remove carbon from the coated quartzware since graphite starts to oxidize at temperatures above 600 °C [291].

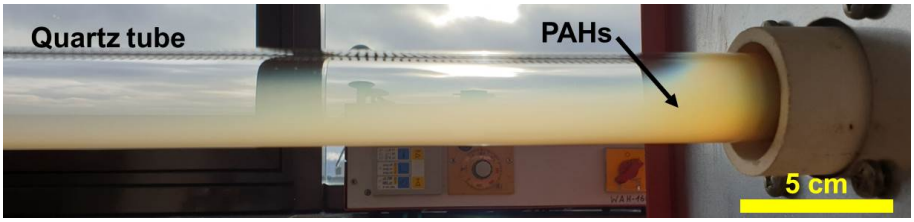

Figure 3.6: A photograph of the quartz tube during a GC deposition process at the pump/exhaust side of the furnace. Polycyclic aromatic hydrocarbons are formed in the gas phase and condense as film on the inner surface of the cooler quartz tube.

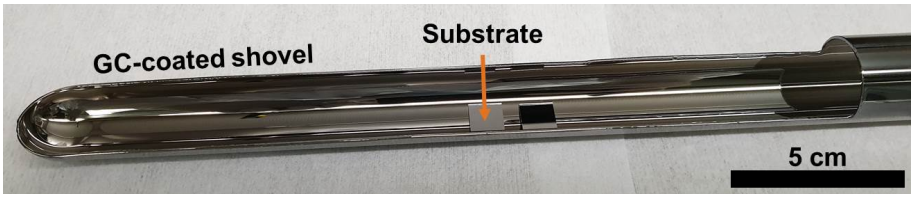

Figure 3.7: A photograph of a quartz shovel loaded with two samples, all surfaces are homogeneously coated with 40 nm thick graphenic carbon. It is very shiny with a high reflectivity, but still slightly transparent (hard to recognize here).

In the following is a process overview for the two used CVD setups and the two corresponding precursor gases, C_2H_2 and C_2H_4, given.

Acetylene Deposition Process

Since acetylene is thermodynamically very unstable, it polymerizes quite easily and since a high-texture is not required, lower temperatures can be used. In literature,

tests at temperatures between 850 °C and 900 °C are reported [159] and preliminary experiments on the used equipment show that GC films can be grown in this range that meet the requirements mentioned in the previous section.

The used C_2H_2 feedstock has a purity of 99.6 % — a higher pureness is hard to obtain as it is very reactive and needs to be solved in acetone. The employed pressure was in the range of 20 mbar, always at a gas flow of 20 sccm. The residence time can be estimated by Eq. 3.1. The length of the furnace is 90 cm, but it is assumed that only the inner 70 cm of the reactor are at the target temperature (no detailed evaluation was conducted). This results in an effective volume of 880 cm^3 as the quartz tube diameter is 4 cm. Using the previously stated gas flow, pressure and a temperature of 870 °C (1143.15 K), a residence time of 12.6 s can be calculated. The sample is placed approximately in the middle of the hot zone during the process. τ can therefore be halved to 6.3 s, since chemical reactions of the gas after the substrate no longer need to be taken into account. These values are much higher than those usually given in literature [282] but compensate for the lower temperature.

The samples were inserted slowly by a constant movement of the shovel within 20 s. Three process variations for the insertion of the sample in the hot zone were used:

- At the set target pressure of the precursor gas;
- while the C_2H_2 pressure was rising with slightly opened bypass valve (the desired pressure was reached between 2 min and 2 min 30 s); and
- while purging with H_2 — after fully inside, H_2 is turned off and pumped down, and C_2H_2 is turned on.

The advantage of heating the substrate under hydrogen atmosphere is that the H-termination of the surface is refreshed. In general, a different initiation has an impact on the first layer grown at the interface to the Si substrate and consequently on the MS contact properties. The processes were always completed by pumping down the precursor gas and removing the sample from the hot zone within 30 s while purging with H_2 (250 sccm, 0.6 mbar).

The electrical resistivity of the GC film is strongly influenced by the deposition temperature [176] and it is suggested that the incorporated hydrogen has a negative impact on the conductivity. Hence, the samples were subsequently annealed at 1000 °C under H_2 flow (250 sccm, 0.6 mbar) for 30 s (additional 30 s to insert the sample and 60 s to remove it) to improve the resistivity of the GC film [169]. This step releases hydrogen and can form additional sp^2 C-C bonds [292]. It is further assumed that the hydrogen gas does not react with already-deposited carbon during the annealing as the pressure in the reactor is very low [293].

The electrical resistivity in parallel to the surface, measured by the four-point probe method, was determined to be in the range between 2 mΩ cm and 3 mΩ cm. A detailed analysis of an improvement by an annealing step was not performed.

Depostion Rate It is necessary to evaluate the influence of the individual parameters on the growth rate in order to control the layer thickness of the deposited GC film reliably. As shown in Fig. 3.8(a), the rate depends for a specific parameter set nonlinearly on the temperature in the reactor. The same trend can also be observed when comparing two different pressures, here 20 mbar and 25 mbar. So, even small changes in temperature have a strong impact on the growth rate as C_2H_2 is very unstable. Fig. 3.8(b) illustrates that the pressure has also a nonlinear impact on the deposition rate — as far as the limited number of data allows an exact statement. However, it corresponds with trends reported in literature [282]. The influence of the deposition time shows a completely nonlinear behavior, as indicated by the trend line in Fig. 3.8(c). The deposition rate increases first with time but decreases here after 11 min again. It should be mentioned, that the substrate was inserted in the hot zone at the final pressure, here 24 mbar. However, the sample needed some time to reach the target temperature, which is a reason for the increase in the rate at first. The drop at a higher time might be related to some process deviations or measurement errors, but also a change in the growth mechanism is possible, as De Pauw *et al.* [286] has reported similar findings.

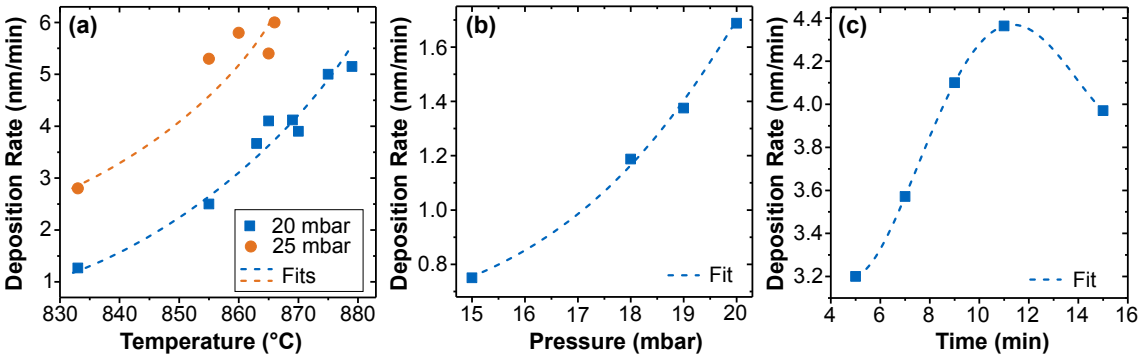

Figure 3.8: Carbon deposition rates at different process parameters for C_2H_2 with a gas flow of 20 sccm. (a) Growth rate as function of temperature at a pressure of 20 mbar and 25 mbar. The total time was always between 20 min and 30 min. (b) Deposition rate as function of pressure at 860 °C. (c) Growth rate as function of the deposition time at $p = 24$ mbar and $T = 860$ °C.

Surface Roughness A smooth surface is desirable, as this suggests a continuous/homogeneous film, which increases the quality as a diffusion barrier. In addition, a rough surface can lead to an electrical field enhancement locally, thereby negatively affect the reliability of the contact. Fig. 3.9 clearly shows that a 40 nm thick GC film has grown very smoothly with an areal surface roughness S_q of 0.4 nm. A variation of the process parameters caused a similar low roughness, nor did the subsequent annealing step lead to any measurable change.

An investigation of the influence of individual parameters on the GC films using a Raman spectrometer also showed no significant changes. A comparison to films deposited from C_2H_4 follows after the discussion of this process.

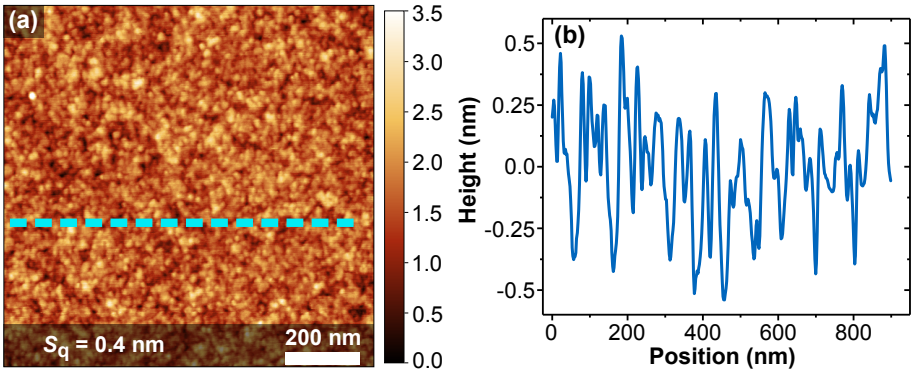

Figure 3.9: Surface roughness and corresponding height profile of a deposited GC film by pyrolysis from C_2H_2 gas measured with an AFM. The film was grown at 860 °C and 24 mbar for 9 min. (a) shows that the film is very smooth and does not show large particles (soot) or pits. (b) shows the surface profile along the dashed line. The average height is here set as zero height.

Even if the deposited film shows a desirable morphology, the use of acetylene has a decisive weakness. It can form copper acetylides in the presence of Cu [294]. The gas cylinder fittings (valve and pressure regulator) for C_2H_2 are typically made off brass, which contains a certain amount of Cu. But as mentioned in section 3.1, copper should be kept away from Si, especially at the high temperatures during the CVD process.

Furthermore, the CVD equipment used has a certain disadvantage. The cooling and loading position of the quartz shovel is in a steel tube. However, if the shovel is pushed towards the hot zone, it will grind along the metal surface and can scrape off traces of metal which will then be injected into the reactor. Steel is mainly composed of iron but also contains nickel. However, as discussed in section 3.1, these are known to cause reliability and yield problems in semiconductor products.

All this implies that not only the hydrocarbon precursor gas but also the equipment should be changed.

Ethylene Deposition

A different CVD setup is used for the deposition of GC by the pyrolysis of ethylene (C_2H_4), as previously schematically presented in Fig. 3.5(b). A major focus of this setup was to ensure that all components introduced into the hot reactor zone had no contact with any metals. The ethylene used is also available with a higher purity (99.995 %) than acetylene. However, the setup does not allow such steep heating ramps, because here the furnace is moved over the cold quartz tube with the shovel and sample inside. It is assumed that the substrate is at the final temperature after at least 6 min but no detailed analysis was carried out. Three different process variations were utilized after the furnace is moved over the sample:

- At the set target pressure of the precursor gas;
- H_2 is pumped down after 30 s and C_2H_4 is turned on (the desired pressure was reached between 30 s and 45 s); and
- while still purging with H_2 for 5 min before C_2H_4 is turned on.

The processes were always finished by pumping down the precursor gas and moving the furnace away from the sample within 40 s while purging with H_2 (200 sccm, 0.4 mbar).

The used dosing valves only allowed a minimum gas flow of 80 sccm, which in turn led to a very short residence time. In addition, ethylene is according to Fig. 3.2(a) thermodynamically more stable at temperatures up to 1100 °C compared to acetylene. A temperature of 1000 °C was chosen as a good compromise for an acceptable deposition rate as this also made an additional annealing step obsolete. However, according to Eq. 3.1, the process pressure must be increased to compensate the higher gas flow to achieve a larger residence time. First tests at $p = 50$ mbar showed good results and yielded in $\tau = 1.6$ s under the assumption of a 40 cm long constantly heated zone (the total furnace is 60 cm long) and an inner tube diameter of 2.5 cm. Taking into account that the sample is in the middle of the reactor, the time is halved to 0.8 s, which is much shorter than in experiments with C_2H_2.

A detailed investigation of the influence of temperature and pressure was not carried out here, but a total process time of 7 min (50 mbar, 80 sccm, 1000 °C) resulted in a layer thickness of 28 nm. The surface morphology of such a GC film is free of soot particles but showed a much higher roughness, as illustrated in Fig. 3.10(a),(d). In contrast to processes with C_2H_2, the residence time is very low and the growth is expected to be less laminar.

For a smoother growth it is necessary to increase the residence time, achieved by 'no-flow' of C_2H_4. To obtain better control on the process and the deposition time, the sample was heated for 5 min under H_2 flow before the hydrocarbon gas was introduced. This also has the advantage that the Si surface is then most likely H-terminated, but care must be taken as hydrogen can etch silicon at high temperatures [295]. After the precursor gas was introduced, the target pressure was reached after about 30 s. It can be assumed that the residence time thereafter increases almost constantly with the deposition time.

However, as discussed in the previous section, a high temperature, residence time and pressure increase the probability of soot formation. Comparing the surface roughness of a deposition at 20 mbar (see Fig. 3.10(b),(e)) and 10 mbar (see Fig. 3.10(c),(d)) to previous experiments with gas flow, it can be observed that no-flow conditions yield a smoother surface. For a higher pressure, soot particles are deposited on the surface, but the roughness is lower. Latter might be related to the total film thickness. The deposition time for both samples was 3 min, but at 10 mbar only 14 nm were grown in contrast to 39 nm at 20 mbar.

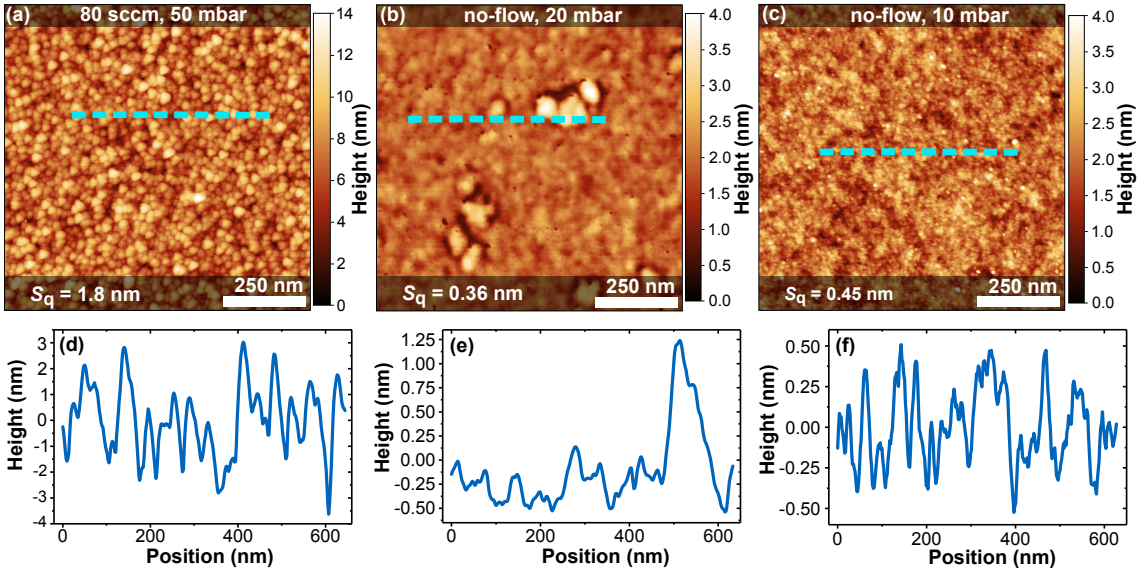

Figure 3.10: Comparison of the surface roughness and the corresponding height profile along the dashed line of GC films deposited by the pyrolysis of C_2H_4 at 1000 °C. All films were analyzed with an AFM. (a) and (d) show the surface and profile of a film grown at a gas flow of 80 sccm and a pressure of 50 mbar. It is very rough with $S_q = 1.8$ nm. The profiles of GC films grown at no precursor flow are illustrated for a pressure of 20 mbar in (b) and (e), and $p = 10$ mbar in (c) and (f). At a higher p, soot particles are formed and deposited on the surface, but a low surface roughness is observed. If only regions without particles are considered for the determination of the areal surface roughness, S_q is reduced from 0.36 nm to about 0.27 nm. The average height of each film is the zero height in (d)-(f).

At even a higher pressure, much more soot is formed in the gas phase. An analysis of the surface of a film grown at $p = 42$ mbar is shown in Fig. 3.11. The particles can reached a size of several micrometers and were distributed over the whole sample.

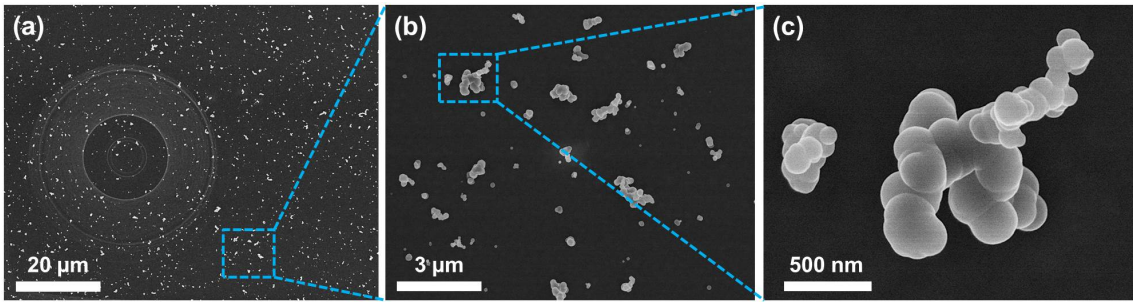

Figure 3.11: SEM images of a surface after a GC deposition process from C_2H_4 in no-flow conditions (1000 °C, 42 mbar). (a) shows an image in the region of the diode that is speckled with soot particles. Scans with higher magnification in (b) and (c) show that individual particles conglomerate and form larger objects. The images were obtained at an acceleration voltage of 4 kV and a working distance of 7 mm.

For the use as a MS contact, however, the electrical performance is a decisive factor. The films grown with C_2H_4 showed an electrical resistivity between 1 mΩ cm and 2 mΩ cm which is slightly better than those produced with C_2H_2. The reason could be the higher deposition temperature and that the annealing of films deposited from C_2H_2 was not as effective as desired.

Comparison of Raman Spectra

Raman spectroscopy allows a crystal characterization, which a pure surface analysis with an AFM could not provide. Fig. 3.12 compares two different C_2H_4 processes, no-flow at 10 mbar and a flow of 80 sccm at 50 mbar, with a film deposited from C_2H_2. Latter was grown at the lowest temperature and has the highest defect density (high D-peak), but the sharpest peaks as the valley between D- and G-band is the lowest. This might indicate a lower amount of amorphous carbon [246]. The films deposited from ethylene did not show such sharp peaks because the valley is higher. It is the highest without flow, probably due to different growth kinetics.

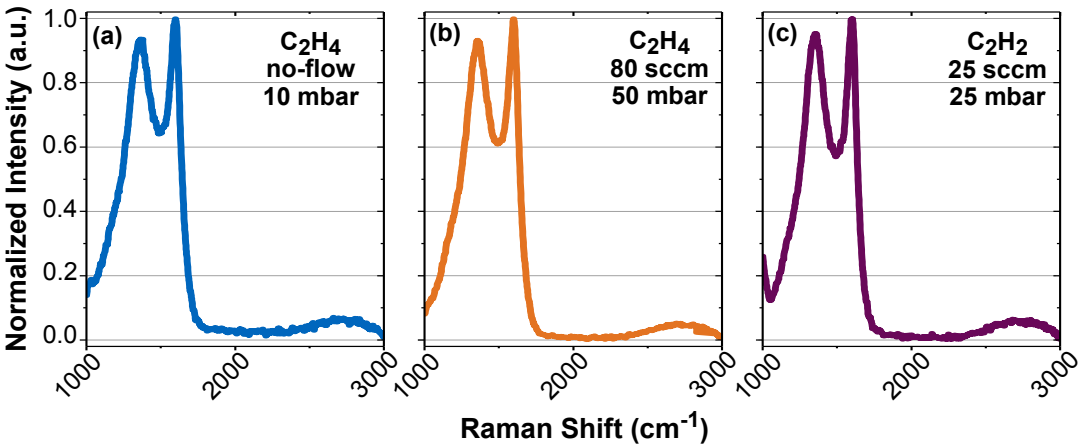

Figure 3.12: Comparison of Raman spectra of GC films deposited at different process conditions. All the y-axes have the same scaling. The used precursor gas in (a) and (b) is ethylene with no-flow and flow, respectively, whereas acetylene is used in (c). All have a higher G- than D-peak, only the height of the D-band is slightly different. A difference in the height of second-order peaks is hardly noticeable.

Parameters Used for Reliability Investigations

It should be noted that many samples have been prepared with a wide variety of parameters. These were mainly used to optimize the understanding of individual process and cleaning steps. Only very few were suitable for subsequent reliability tests. Table 3.1 lists the deposition parameters of the films where also the C-Si contact shows a high reliability. The films deposited in a CVD process are hereinafter referred to as CVD-C.

Table 3.1: The CVD parameters of the two setups used for the reliability analysis of graphenic carbon-silicon contacts.

Precursor gas	Deposition temperature	Gas flow	Pressure	Annealing temperature & time
C_2H_2	855 °C	20 sccm	25 mbar	1000 °C for 30 s
C_2H_4	1000 °C	80 sccm	50 mbar	—
C_2H_4	1000 °C	no-flow	10 mbar	—

3.3 Physical Vapor Deposition of Carbon

Physical vapor deposition (PVD) can be described simply as an atomistic process in which vaporized material is deposited on a substrate in vacuum or low-pressure gaseous atmosphere. One form of it is the so-called *sputtering* or *sputter deposition*. This method is widely used in semiconductor industries to deposit pure metals, alloys or dielectrics of high quality, uniformity, smoothness, film adhesivity and low level of contamination. These are all features which are also required for a reliable metal-semiconductor contact and in addition, the deposition temperature is much lower than in a CVD process.

3.3.1 Theoretical Considerations

Carbon can form a wide variety of allotropes ranging from graphitic/graphenic through amorphous to diamond-like formations when deposited in a PVD process [180,239]. It heavily depends on the method and deposition parameters. Carbon can not only form alloys with hydrogen like in the previously discussed CVD process, but it can also react with N and form nitrogenated or nitrogen-doped carbon. Fig. 3.13 shows a ternary phase diagram of such nitrogenated amorphous or disordered carbon materials (hydrogen-free) based on the content of incorporated N, and sp^2 and sp^3 hybridized C atoms. From here it is obvious that only sputtering can produce the desired films with graphitic properties.

Film Characteristics

The stoichiometry and the properties, especially the electrical characteristics, of the sputtered material are in the focus of this work. The growth of a film first begins with the impingement of a sputtered atom on the substrate. This adatom diffuses along the surface and nucleates there with other atoms. These nuclei capture others and finally form small islands that grow together at different rates to form a continuous film, depending on the surface mobility. The following parameters have a major impact on the final film morphology:

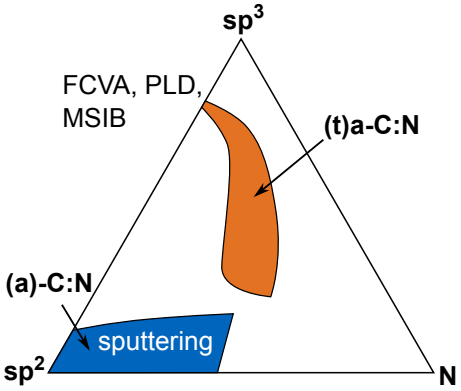

Figure 3.13: Ternary phase diagram of different amorphous carbon-nitrogen alloys. The materials are classified on their ratio of sp^2 and sp^3 hybridized C and the amount of incorporated N. Sputtering yields more graphitic carbon. Films with higher sp^3 content (ta-C:N) are produced by filtered cathodic vacuum arc (FCVA), pulsed laser deposition (PLD) and mass selected ion beam deposition (MSIBD). Adapted from Ref. [296].

- The substrate temperature;
- the partial pressure of the sputter gas;
- the partial pressure of an additional reactive sputter gas; and
- the ion energy.

Thornton [297] summarized the influence of the sputter parameters in a so-called *structure zone model*, as shown in Fig. 3.14. Messier [298] has added in an updated version the influence of the ion energy, which is inverse to the pressure.

Undesirable is the film from zone 1, which is formed at low temperatures, low ion energy and higher pressure. The film is rather porous or amorphous with voids between the crystallites and has unfavorable electrical properties. In zone 2, the substrate temperature is elevated to such an extent that the surface mobility of the adatoms is also increased. This finally leads to a dense and columnar growth of the crystallites, but the surface is very rough. At very high temperatures, starting at about 75 % of the melting point of the sputtered material, a smooth surface with a polycrystalline structure is obtained (zone 3). However, there is still a very desirable transition zone (zone T) between zone 1 and 2, which yields a low surface roughness and grows dense and fibrous, possibly even slightly polycrystalline. Only a moderately elevated temperature is necessary to obtain that kind of structure because a very low pressure or higher ion energy is already able to provide the necessary surface mobility.

For the deposition of carbon films, the pressure should be very low, ideally below 10 µbar. Estimating the required temperature for zone T is difficult because graphite has no melting point. Nevertheless, the vapor pressure might be used as a guide and is about 10 µbar at 2000 °C [300] and thus in the range of the working pressure.

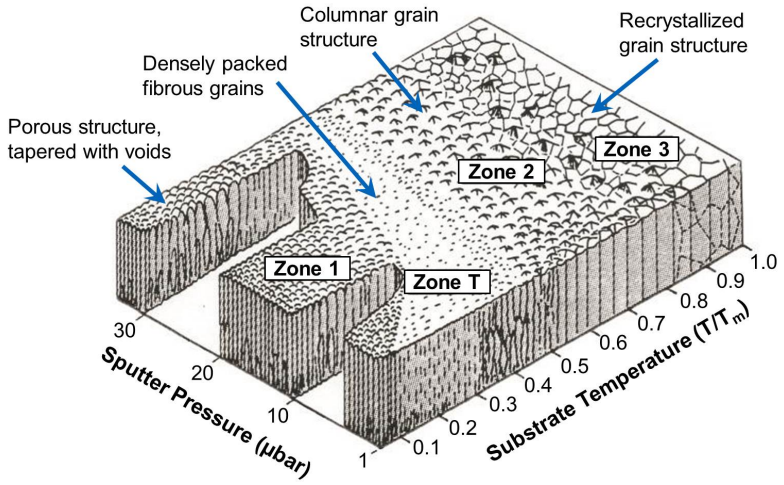

Figure 3.14: The structure zone model proposed by Thornton [297,299] for columnar thin films produced by sputter deposition. Three main and a transition zone between zone 1 and 2 are indicated. The relevant process parameters are the Ar pressure and the substrate temperature T (in Kelvin) which is normalized by the melting point T_m of the sputtered material. Reprinted from Ref. [297], with the permission of AIP Publishing.

Non-Doped Carbon Wyon *et al.* [301] and Kim *et al.* [302] have shown that the considerations made before also apply to sputtered carbon films, abbreviated here as SC. Micrographs of cross-sections clearly demonstrate that mainly a low pressure, ideally less than 10 µbar, and an increased substrate temperature towards 400 °C produces less porous structures, like for zone T. Furthermore, the surface roughness at a reduced argon pressure is also lower, since there are fewer unbound or badly bonded atoms/molecules [303]. In particular, a higher temperature leads to an increase in the sp^2/sp^3 ratio and nano-/microcrystalline structures are formed with fewer defects, which have the desired graphite-like properties [304].

It is essential that the film adheres well to the test vehicle for the use as MS contact. A high adhesion was demonstrated to Si and quartz. Peeling tests suggest the formation of covalent bonds to the substrates [180]. But also the electrical resistance has a decisive significance. It has been reported that the electrical resistivity of sputtered carbon films can be between $10^{-2}\,\Omega\,\mathrm{cm}$ and $10^{10}\,\Omega\,\mathrm{cm}$ [180, 270].

The electrical behavior has the same trend as the structural morphology discussed previously. A lower sputter pressure and a higher temperature increase the electrical conductivity [302,305–307]. This can be explained by the fact that the film becomes more graphitic (more sp^2 bonds) and gets a smaller band gap [306,307]. This changes the characteristics of the film from a semiconductor to a semimetal, resulting in more free charge carriers. Unfortunately, it has been reported that ρ increases at lower film thicknesses [180, 301] and when exposed to atmosphere it drifts to higher values [305, 307].

Nitrogen-Doped Carbon As mentioned before, carbon can be doped with nitrogen and is abbreviated here with CN. Compared to other atoms, a doping with N is preferable as its atomic size is similar to that of C. The content of incorporated nitrogen is hereby of decisive importance and can be adjusted mainly by the ratio of Ar to N_2 gas during the sputter process. Only if the content in the film is roughly below 5 %, graphitic structures are obtained in which a C atom in the hexagon is replaced by an N atom. A higher proportion tends to produce pentagons, which form fullerene-like structures [239, 308, 309].

Temperature and sputtering pressure also influence the amount of incorporated N, but also affect the crystal morphology similar to nitrogen-free layers [310]. Furthermore, the N-doping leads to a shift of the Fermi level towards the conduction band, that's why nitrogen acts as electron donor and is considered as weak n-type doping [189, 311, 312]. Broitman *et al.* [181] has reported an improvement of the electrical resistivity by an order of magnitude to values $< 10^{-2}\,\Omega\,\mathrm{cm}$.

3.3.2 Process Description

RF Magnetron Sputtering Basics and Setup

In a sputter process, ionized atoms are accelerated towards a target material and knock out atoms with an angular distribution according to the cosine-law [179]. These atoms can nucleate a thin film on a surface of a substrate. The gas commonly used is argon (Ar), here used with a purity of 99.9999 %. On the one hand it is inert and with a fraction of almost 1 % in the atmosphere very common. On the other hand, its atomic mass is in the range of the materials that are typically sputtered [179]. To accelerate the Ar^+ ions, a negative potential with respect to the potential of the plasma is necessary at the electrode (cathode) where the target is mounted.

A very common subgroup is rf sputtering, which is used here and therefore only this type will be considered further. The setup is schematically illustrated in Fig. 3.15. Typically, an rf power with a frequency of 13.56 MHz is used to form a plasma in the chamber. An impedance matching network is necessary to tune the impedance of the power source to that of the plasma to transmit maximum power. A magnetron, made out of permanent magnets, is placed behind the target material, here in a balanced configuration [313]. It enhances the efficiency (sputter rate) of the process, as the strong magnetic fields keep secondary electrons, ejected from the cathode, confined in this region. This method is called (*rf*) *magnetron sputtering* and yields locally a much denser plasma, which allows the working pressure to be reduced below 20 µbar.

The whole chamber is grounded and acts as the anode. As this surface area is much larger than the cathode area, a negative self-bias is created at the target, which attracts the positive Ar ions [314]. Here a 100 mm graphite target with a purity of 99.999 % was used. The sputtering process is overall very inefficient. When an ion

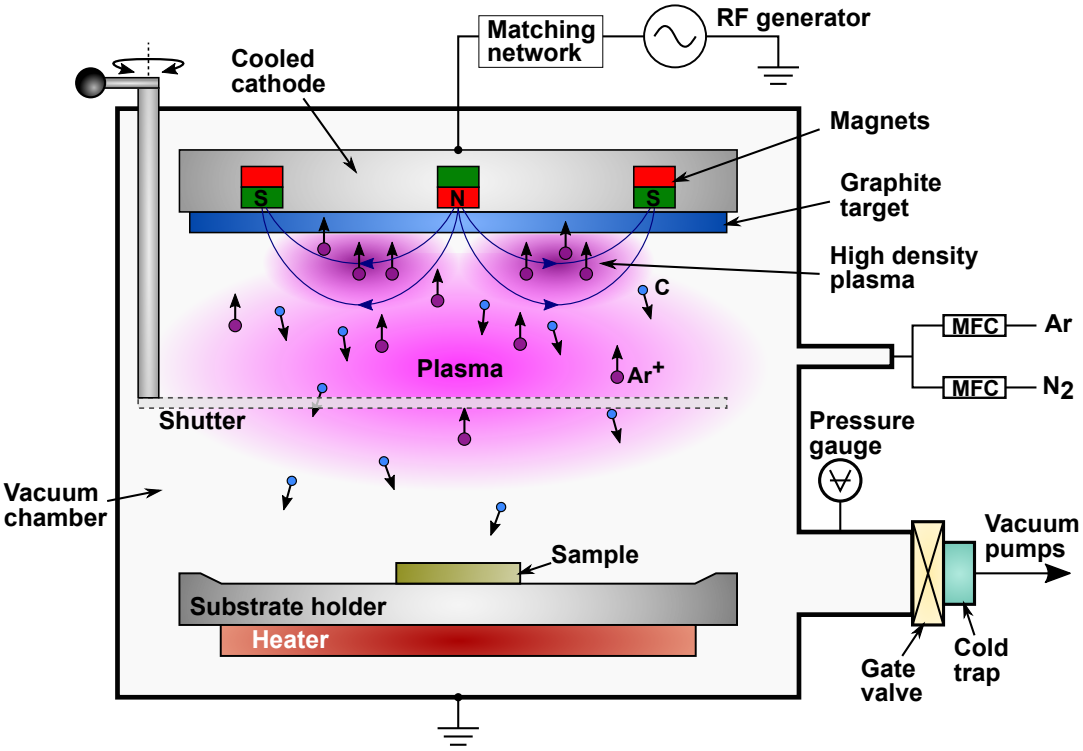

Figure 3.15: A schematic illustration of the used rf magnetron sputtering system and process. An rf power supply (13.56 MHz) is connected over an impedance matching network to the cathode. This contains the balanced magnetron and the iridium-bonded graphite target. The flow of the sputter gas (argon) and the optional reactive gas (nitrogen) is adjusted by mass flow controllers (MFCs). The pressure in the chamber can be controlled by a gate valve. A cold trap is available and can be filled with liquid nitrogen in order to improve the base pressure in the chamber. A hand-operated metal shutter, approximately centered between target and sample (target-substrate distance is 70 mm), conveniently stops the sputtering onto the substrate. The substrate holder was floating and can be heated to approximately 500 °C with a resistive heater underneath.

hits the target and kicks an atom out, most of the energy just heats the material or ejects secondary electrons. But the probability to release an atom is not the same for all materials. It is commonly described as the sputter yield, which is the number of sputtered atoms per bombing ions. In case of carbon, the yield is the lowest of all materials. At an Ar^+-energy of 200 eV, the yield is only about 3.5 %, whereas an energy of 600 eV increases the probability to approximately 14 % [315].

A reactive gas, such as O_2, N_2 or gaseous hydrocarbons, can be introduced together with Ar to react with the sputtered target atoms while they travel towards the substrate. This process is known as *reactive sputtering*. But, reactions also occur on the substrate and the target itself. Residual gases in chamber, especially water, can also cause similar effects. This can be prevented by keeping the base pressure as low as possible, for example by using an additional liquid nitrogen cold trap as it is equipped here. This allowed a pressure below 2×10^{-7} mbar in the chamber,

which is pumped by a turbomolecular and a scroll pump. To reduce the potential of contaminations, the samples are loaded through a load lock chamber directly after the HF-dip of the samples.

All the sputtered films showed very good adhesion to Si, SiO_2 and SiN, as if covalent bonds are formed. The adhesion of carbon to the metal parts in the PVD chamber is generally not very strong. However, in order to achieve films with a low level of contaminations, it is crucial that all parts near the sputtering source and especially the sample holder and shutter are well coated with carbon. Fig. 3.16(a) shows a shutter that was not well coated with carbon as the films adhered very poorly on the polished metal surface and a resputtering of the shutter material in a low pressure range is possible. In addition, a few milliseconds long exposure of a badly coated shutter to the plasma during the shutter operation from the closed to the opened position or if the shutter is left too close to the plasma source when opened could be enough to deposit unwanted contaminants on the diode active region or in the carbon film. A good adhesion is only achievable if the parts are glass bead blasted, like shown in Fig. 3.16(b), or a precoating with titanium might be useful.

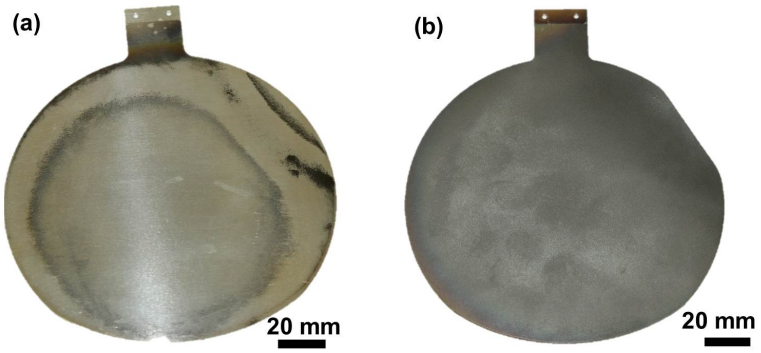

Figure 3.16: Photographs of different shutters after they were coated. In (a) the metal surface was polished and the carbon did not stick properly and could easily be wiped off. On the upper right part of the shutter is an arc visible because the shutter reached in the 'open' position slightly into the plasma . The shutter in (b) was glass bead blasted before it was sputtered with C on both sides while lying on the substrate plate. The part that protruded into the plasma was cut off.

Process Parameters for SC and CN Films

The above considerations suggest that carbon should be sputtered at a very low pressure and at a higher temperature. The plasma was hence operated at an Ar pressure between 2 µbar and 16 µbar. The substrates were heated on the heatable substrate holder to temperatures between 20 °C and 400 °C. The upper limit was chosen so that temperature budget restrictions for middle and back end of line of advanced nodes are maintained (see section 1.2). An additional heating of the sample due to plasma irradiation was not taken into account. The heating of the substrate

to 400 °C took about 20 min, which causes a delay between insertion and start of the deposition. It was assumed that almost no natural oxide grows on the surface because the sample is in a vacuum during heating. The aim of the first sputtering tests was to evaluate the influence of individual process parameters on the electrical resistivity and the film morphology, therefore polished silicon with 400 nm thermal SiO_2 on the surface was used as substrate.

Raman Spectra The Raman spectra in Fig. 3.17 highlight that a SC film sputtered at a temperature of 20 °C has no clearly distinguishable D- and G-band, which points to an amorphous structure [234]. In contrast, a film deposited at 400 °C (other parameters are kept the same) clearly shows sharper individual peaks with a dominating G-peak. This confirms previous considerations that graphenic sp^2-bonds are formed at these temperatures. To graphitize an SC film deposited at 20 °C by annealing (here in H_2), a temperature of at least 550 °C for 1 h was found to be necessary to get a Raman spectrum with similar features. All CN films showed a distinguishable D- and G-band — latter is always dominating independent of the substrate temperature because small amounts of incorporated nitrogen promote the formation of sp^2-bonds. The C≡N peak in the Raman spectra indicates that sp^1-bonded N is incorporated into the film, among other configurations [239]. But the CN sputtered at 400 °C shows more pronounced second order Raman peaks (D+G & D+D'), which are hardly recognizable at SC films.

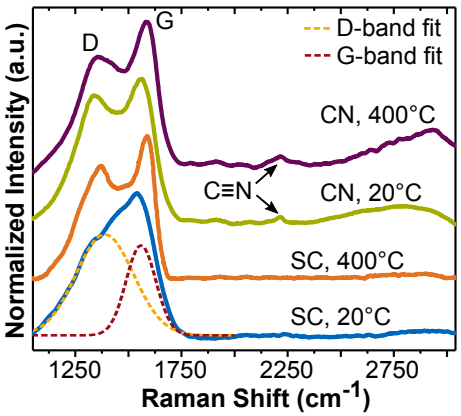

Figure 3.17: Raman spectra (offset for clarity) of SC and CN films sputtered at a substrate temperature of 20 °C and 400 °C, respectively. The used excitation wavelength was 532 nm. The spectrum of the SC film established at 20 °C is more of amorphous structure as indicated by the higher and wider D-peak than the G-peak of the Gaussian deconvolution of the spectrum. A higher temperature causes a graphitization, indicated by sharper Raman peaks. A ratio of ∼ 1 of the fitted D- and G-band was found for CN at 20 °C (not shown here). The pronounced G-peak is always higher than the D-peak for the films deposited at 400 °C, which indicates the prevalence of graphitic sp^2-bonds. Taken from Ref. [MS19].

Surface Roughness A surface analysis with an atomic force microscope (AFM), as shown in Fig. 3.18(a)-(f), highlights that an SC film sputtered at 20 °C has a very low surface roughness. The lack of recognizable grain boundaries points to a more amorphous structure. This is contrary to the structural zone model of Thornton because a zone 1 film should have a certain roughness (see Fig. 3.14). Either the film is already at the transition to zone 2, even if it was sputtered at room temperature, or it is due to the small film thickness of 35 nm, which behaves differently than the model. At a substrate temperature of 400 °C, the surface is rougher and polycrystalline graphitic clustering occurs (see Fig. 3.18(b),(e)).

The CN film grown at a temperature of 400 °C has a smoother surface, as shown in Fig. 3.18(c),(f). Together with the smaller grain size, one can conclude that the growth is nanocrystalline and better oriented. CN films sputtered at 20 °C exhibit a very similar surface compared to films deposited at higher temperatures. A 5 nm thick CN layer in contrast showed an almost two times lower surface roughness ($S_q = 0.35$ nm) than the 35 nm thick CN in Fig. 3.18(c),(f). It is very similar to the SC film shown in Fig. 3.18(a),(d), which was sputtered at 20 °C and implies that thinner films grow very homogeneously, without pinholes.

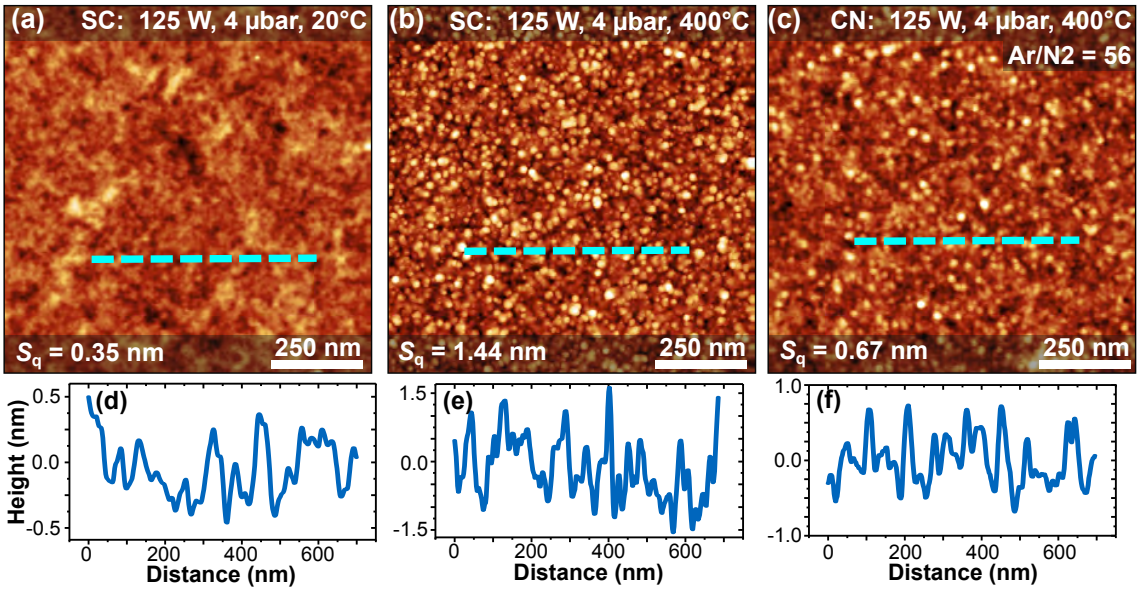

Figure 3.18: Comparison of the surface roughness and the corresponding height profile along the dashed line of SC and CN films measured with an AFM. (a) and (d) show the surface and profile of an SC film sputtered at 20 °C with a low surface roughness S_q of only 0.35 nm. The profiles of an SC film sputtered at 400 °C in (b) and (e) show a rougher surface and surface nuclei point to a polycrystalline texture. (c) and (f) illustrate the surface and height profile of a CN film deposited at 400 °C. It is smoother than the SC deposited at 400 °C as CN seems to grow more in a nanocrystalline fashion. Taken from Ref. [MS19].

Electrical Characteristics A main focus here was the investigation of the electrical film resistivity ρ by a four probe measurement as a function of the rf power P, working pressure p and substrate temperature T. For CN films, only the influence of the Ar/N_2 ratio was evaluated. To measure the film thickness required to determine ρ, a part of the carbon was previously always scratched off from the sample surface. This was no longer possible at all SC and CN layers manufactured. The determination of the thickness, which is need for the evaluation by scratching off a part of the carbon from the sample surface, was mostly not possible with sputtered films. As a result, it can be concluded that these films are very hard — sputtered carbon is also used as a protective layer for hard drive disks — and also have an excellent adhesion to the substrate. Instead, a part of the film was etched away in H_2 plasma (see section 3.4) while the other part was protected with photoresist to receive a step, which can be analyzed by an AFM.

The thickness should be in the same range for all samples (here $\sim 35\,\text{nm}$) to exclude possible errors, as a thickness-dependency of ρ — with a higher value for thinner films — was reported [180, 301]. However, at least with CN films it was discovered here that this dependence does not exist. So 5 nm thick CN has the same low resistivity as a 35 nm thick layer. It was not investigated whether the value becomes lower at much higher thicknesses.

Fig. 3.19(a) clearly illustrates that a higher power causes a lower ρ. As the slope is quite linear and does not converge to a minimum value within the displayed range, a further increase of P might lead to an even lower resistivity and an improved carbon film — but caution was taken not to overheat the target. The CN film exhibits a two times lower ρ at the same sputter conditions as nitrogen acts as an electron-donor and increases the Fermi level in GC. It even approaches the value of CVD-C ($\sim 1\,\text{m}\Omega\,\text{cm}$), which was deposited at 1000 °C. In addition, the rf power has in a quite linear impact on the sputter rate. A higher P linearly increases the self-bias potential at the cathode and consequently the Ar ions gain a higher energy, which increases the sputter rate. The (negative) potential measured at the cathode at 125 W was 220 V while it was 120 V at 50 W.

The resistivity of the sputtered film is quite sensitive to the pressure and increases for $p > 8\,\mu\text{bar}$ very rapidly and the minimum ρ might not be located much below 2 µbar, like illustrated in Fig. 3.19(b). The pressure is also directly connected to the sputter rate. The higher p, the denser is the plasma and more Ar ions are present, which can bombard the target. For later electrical investigations as a contact material to Si, 4 µbar instead of 2 µbar or lower was used, even if it would lead to a lower ρ. This is because surface analysis of films sputtered at 2 µbar showed a higher surface roughness.

An increase in the substrate temperature during the sputtering is very effective in the reduction of the electrical resistivity as a graphitization seems to occur at higher temperatures (Fig. 3.19(c)). The effect is quite high in the beginning, but tends to saturate at temperatures $> 400\,°\text{C}$. Surprisingly, the sputter rate also

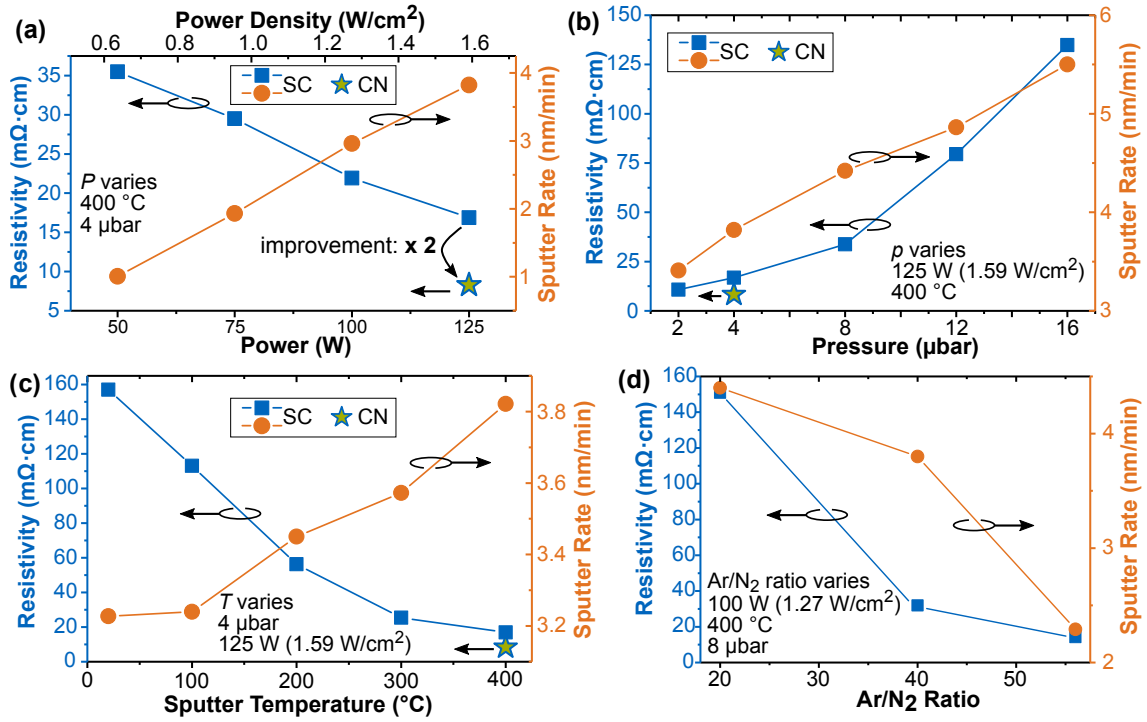

Figure 3.19: Dependence of the electrical resistivity ρ and the sputter rate of SC films in comparison with a CN film on the sputter condition are shown in (a)-(c). The CN film was sputtered at a power P, pressure p and substrate temperature T of 125 W (1.59 W cm^{-2}), 4 µbar and 400 °C, respectively. The ratio of the sputter gas flow was $Ar/N_2 = 56$. (a) shows ρ and the sputter rate of SC for different sputtering powers P and compares it to the CN film. (b) and (c) show them as a function of p and T. The influence of the ratio of the Ar and N_2 gas flows is shown in (d).

increases slightly with the temperature. One possible explanation is that the heat radiation from the substrate holder also heats the surface of the target a bit, thereby increasing the sputter yield. Similar findings are obtained with shorter sputtering durations, where the sputter rate is lower than with thicker films because the target is cooler in this case.

These results coincide with preliminary considerations and in summary it can be stated that an SC film with high electrical conductivity requires a high power density, low pressure and higher temperature. It is assumed that this is also true for CN films.

For CN, however, the ratio of Ar to N_2 in the plasma can be adjusted. The maximum available gas flow ratio of the used setup has been restricted in first experiments by the mass flow controllers to $Ar/N_2 = 56$. This resulted in an N concentration of 3.5 at.% in the plasma. The incorporated content of N in the CN films was measured by X-ray photoelectron spectroscopy (XPS) to be in the order of 11 at.%. This is different to experiments from Hellgren *et al.* [308] as they have

measured that it stays below 5 at.% at this gas ratio — at least for the setup they were using. In Fig. 3.19(d) is shown that a high ratio is needed to produce low resistive films, as the formation of graphenic carbon is promoted at very low incorporated N contents. Furthermore, the higher the proportion of N_2 in the sputter gas, the higher the sputter rate, since additional N atoms are added to the C atoms in the film.

CN as KOH Etch Mask It has been reported [AF19, 166] that CVD-carbon has been used as an etch mask for wet chemical etching of silicon with potassium hydroxide (KOH) because it is chemically very inert, is non-porous and forms many covalent bonds to Si. A similar experiment as described in Ref. [AF19] was performed here with a 35 nm thick CN film grown at 400 °C directly on a silicon substrate with (100) crystal surface. Different patterns, defined by laser lithography and subsequent plasma etching, were then used as etch masks for KOH etching. The used solution had a molar concentration of 5 M and was saturated with IPA. The etching process lasted for 7 min whereby about 6 µm of Si was etched in ⟨100⟩ direction. As shown in Fig. 3.20, the covalent bonds between CN and Si are abundant and strong enough to prevent the film from lifting off during the etching process. Also, the film seems to be dense enough, otherwise bubbles might have appeared between silicon and carbon. A more detailed analysis of the surface after the treatment was not carried out.

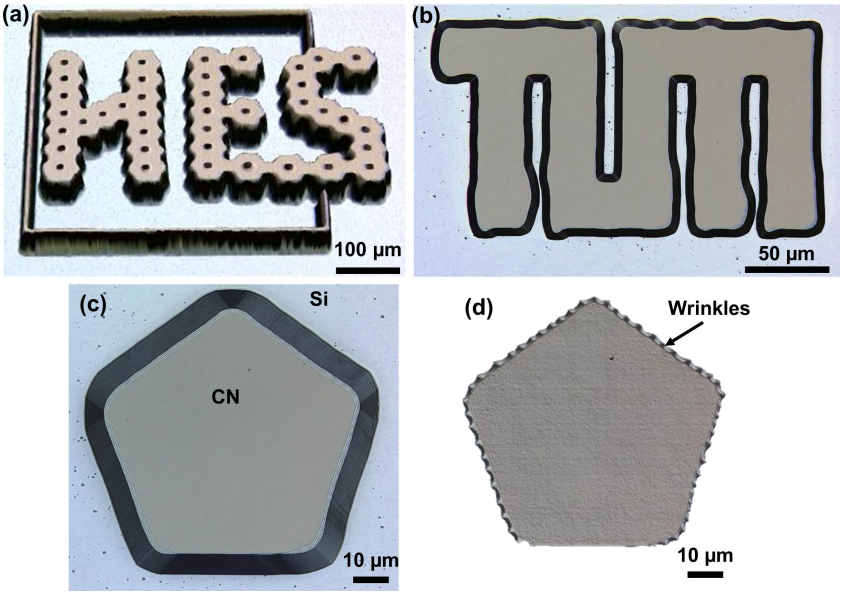

Figure 3.20: Micrographs of patterns etched with KOH using CN as etching mask. (a) shows a slightly tilted structure in a 3D view. The height is 6 µm and is shown enlarged by a factor of six compared to the indicated scale bar. (b) and (c) show a top view of two patterns indicating facets in the silicon. (d) shows the CN film from (c) with height information (enlarged by a factor of 20) to highlight the wrinkles at the edges where the carbon was undercut.

Sputtered carbon typically causes compressive stress on Si [305, 306, 308], which can be seen in Fig. 3.20(d) at the wrinkles in undercut CN. This type of stress is also observed at CVD-deposited carbon on silicon [166].

Parameters Used for Reliability Investigations

It should be noted that many samples have been prepared with a wide variety of parameters. Most of the depositions were performed on SiO_2/Si substrates to optimize the understanding and individual process steps. Only very few depositions were conducted for subsequent reliability tests. Table 3.2 lists the deposition parameters of the films which were used for investigations of the carbon-silicon contact.

Table 3.2: The sputtering parameters used for the electrical performance and reliability analysis of carbon-silicon contacts.

Type of film	Ar/N_2 ratio	Power	Pressure	Temperature
SC	no N_2	125 W	4 µbar	400 °C
CN	56	125 W	4 µbar	400 °C

3.4 Diode Fabrication Process

The essential part of the Schottky diode, the metal-silicon contact, is formed during the deposition of graphenic carbon, regardless of the method. A schematic cross-section of the BAT15 test vehicle after the GC deposition is shown in Fig. 3.21(a). Carbon grows in the CVD processes on all hot surfaces, so the substrates gets coated all around. GC on the SiO_2-free backside of the highly doped substrate is directly used as electrode for the backside contact without the need of an additional metallization. In contrast, the backside of the substrate remains free of carbon during the sputtering — so additional process steps for the metallization are necessary.

Metal Deposition A top metallization is required because the carbon films are typically very thin and the current needs to be transported from the test needle in the measurement setup to the active diode region. The metal should only be deposited on the active diode region and the thick oxide pad. The position of the metallization can be adjusted very precisely by photolithography and a subsequent lift-off process. However, the photoresist always leaves residues that deteriorate the contact resistance [316]. Instead, a shadow mask of 50 µm thick steel was used, which has lasered openings with the diode grid of the BAT15 substrate, as schematically shown in Fig. 3.21(b).

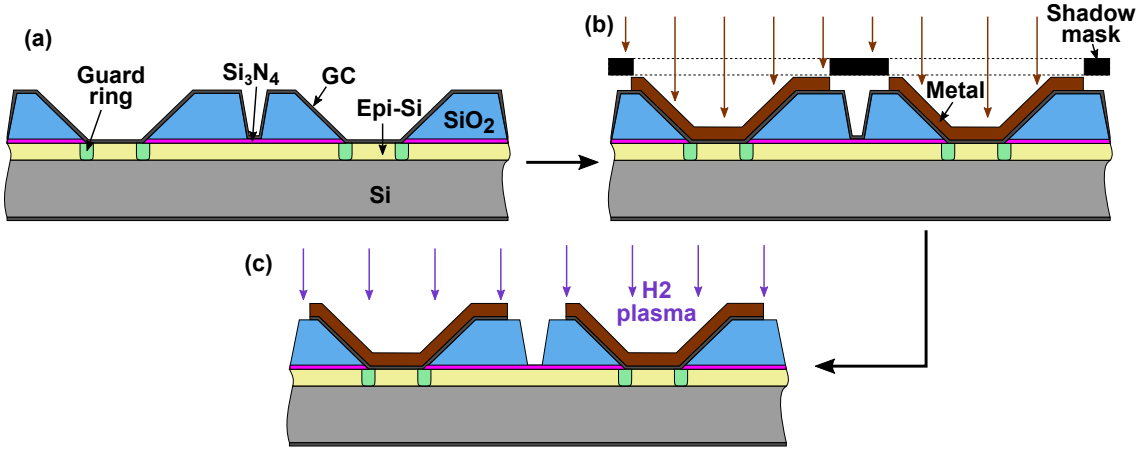

Figure 3.21: Schematic illustrations of the diode fabrication steps. (a) shows an exemplary cross-section of the BAT15 test vehicle directly after carbon deposition. In case of CVD-C all surfaces are coated, whereas in case of SC/CN films only the top face is coated. (b) A steel shadow mask is placed on top of the sample to define the areas to be metallized by e-beam evaporation. (c) The top metallization acts as a hard mask for an H_2 plasma etch so that the carbon is fully removed at non-covered regions.

However, the adjustment is not as easy as with a lithography mask. The samples, a maximum of four, were placed in a round holder with the shadow masks on top, as shown in Fig. 3.22. The spring which fixes the mask must be adjusted in such a way that the mask can still be moved, but does not slip during slight shaking. With the help of a camera and a micromanipulator with test needle, the shadow mask was adjusted to the diode grid until they matched as shown in Fig. 3.22(d).

The holder was then transferred directly into the process chamber for the metallization steps. This was done with an electron-beam (e-beam) evaporation process. The vacuum chamber with the samples to be metallized inside was pumped down overnight, resulting in a final pressure of about 2×10^{-7} mbar.

Titanium (Ti) with a thickness of 50 nm was the first metal to be evaporated. This was used because it provides a low specific contact resistance to graphene [316] — also assumed in case of graphenic carbon — and its high melting point makes it very suitable for subsequent reliability studies. If it reacts with carbon to form titanium carbide (TiC), this would not be a disadvantage because TiC has a very high melting point ($> 3000\,°C$) with excellent thermal stability. On top of Ti is copper (Cu) deposited with a thickness between 1.25 µm and 1.3 µm. Such a thick film is necessary to transport the current towards the diode and to prevent crowding during the device operations. But, Cu also acts as an additional heat sink to keep the temperature at the junction as low as possible. On top of this stack is 40 nm of gold (Au) deposited to prevent an oxidation of Cu. No additional annealing of the metal stack was performed after the deposition.

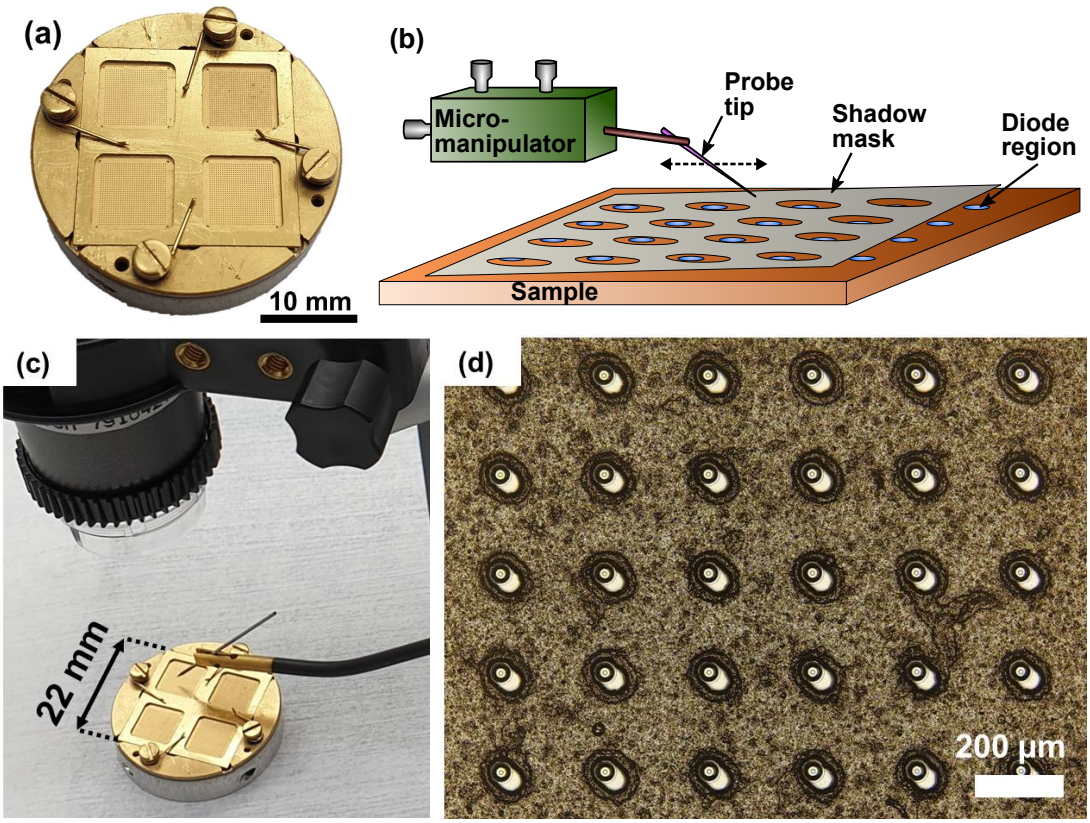

Figure 3.22: A photograph of the sample holder for up to four samples, which is used for the adjustment of the shadow mask and the subsequent metallization, is shown in (a). Each sample is assigned its own mask. A steel frame overlaps the samples and the shadow masks partially and is pressed on with springs. (b) shows a schematic representation of the alignment procedure of the shadow mask on the sample using the probe tip of a micromanipulator to move the mask. A part of the real measurement setup is shown in (c), whereby the alignment is carried out with the help of a microscope with a magnification rate of 140 and a high working distance of $\sim 30\,\mathrm{mm}$. (d) shows a shadow mask with an oval opening that is ideally aligned with the underlying substrate. The active diode region is below one part of the opening while the other part points toward the center of the oxide pad of the BAT15 test vehicle.

Graphenic Carbon Structuring As graphenic carbon still covers the whole surface, all diodes are connected by this film. To obtain isolated diodes on the substrate, the GC in between must be removed, whereby the existing metallization served as a hard mask. A wet chemical treatment is out of consideration as GC is chemically very inert and the metals would also react with the chemicals. Graphene is usually structured in oxygen plasma but there is a risk that the metallization would be oxidized during this process. Graphite also reacts with hydrogen [317], so the structuring can also be performed by H_2 plasma to remove GC on non-covered regions, as illustrated in Fig. 3.21(c).

The etching was performed here in a capacitively coupled plasma (CCP) system. The setup is simple and consists of a glass vacuum chamber with two electrodes connected to an rf generator, as shown in Fig. 3.23. The driving frequency of the source is 45 kHz at an output voltage and current of 990 V and 40 mA, respectively. The smaller electrode should create a higher self-bias and acts also as the substrate holder. A timer allowed to control the plasma-on duration. Typically, etching was done for 10 s followed by a 30 s to 50 s long pause period to avoid high substrate temperatures. The plasma was operated at a pressure of $\sim$3 mbar.

Finally, the process was stopped as soon as there was an optical change on the sample surface recognizable by visual inspection. The differences in color are illustrated in Fig. 3.24. However, a Raman spectrometer was then used to verify that the GC film has been thoroughly etched away. In this case, graphitic Raman features are not detectable anymore and only Si peaks are present. For samples with CVD-C, the carbon on the back is not removed during the etching process and the sample is ready for electrical characterization.

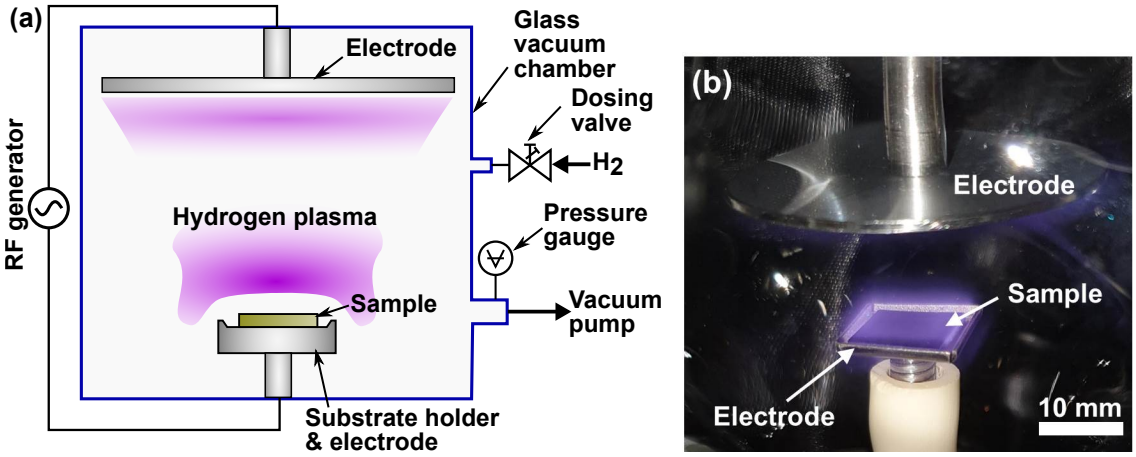

Figure 3.23: (a) A schematic representation of the CCP structure used for etching carbon with a hydrogen plasma. The pressure in the reactor can be adjusted by changing the gas flow with a needle valve. The photograph in (b) shows the real setup used, whereby the plasma is clearly recognizable around the sample.

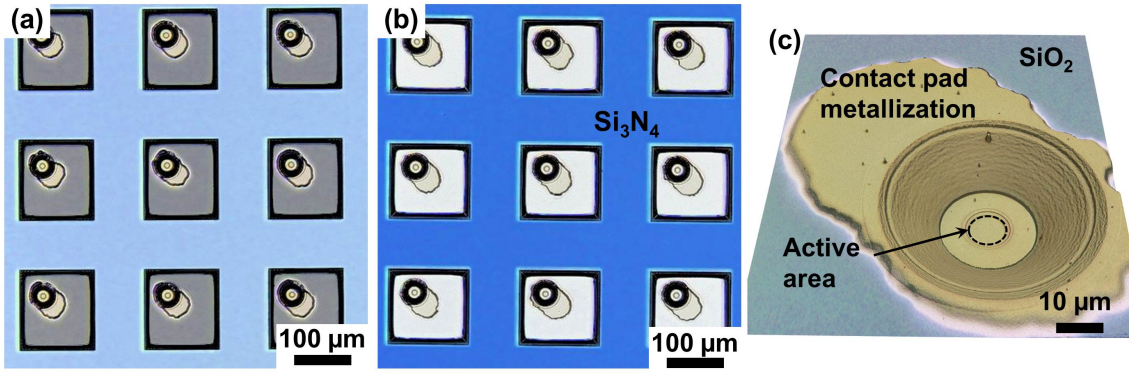

Figure 3.24: Micrographs of metallized BAT15 substrates with GC before etching in (a) and after GC was removed in an H_2 plasma in (b). The blueish color from the silicon nitride between the pads is sober as the 25 nm thick GC changes the reflection properties of the film stack an absorbs a certain fraction of light. A GC-free Si_3N_4 surface has a stronger blue. In (c) is a slightly tilted 3D image of a final diode at a higher magnification shown. The line edge roughness of the metallization is caused by the imperfect openings of the shadow mask.

Additional Steps for Diodes with Sputtered Carbon Sputterd films (SC and CN) do not have carbon films on the backside of the sample as only the top face was coated — to be more precise, the side face of the substrate might also get coated. During the process steps listed above, a natural oxide layer has formed on the backside of the substrate. Although this area is very large, it affects the contact resistance to a possible metal, which is why the thin SiO_2 must be removed with HF. To protect the front side from the attack of the chemical, it was covered with photoresist. After a 30 s long HF-dip (5 %) the sample was transferred directly into an ion-beam sputtering system. As contact material to silicon, 10 nm of Ti were deposited because of the low contact resistance to Si. 50 nm of Au were added subsequently because of the good electrical properties and to prevent an oxidation of Ti. Finally, the photoresist was stripped in acetone and IPA at 70 °C in an ultrasonic bath. No subsequent annealing step for the backside metallization was performed.

4 Electrical Evaluation of Graphenic Carbon as Contact

This chapter discusses the electrical properties of the TiSi-Si contact based on the commercial BAT15 diode and those of graphenic carbon-silicon contacts using the BAT15 test vehicle. The influence of different manufacturing methods and process parameters is presented for GC. All the shown J-V curves were measured at room temperature. Furthermore, additional electrical properties of GC films, which have not yet been presented in chapter 3, are discussed.

4.1 DC Characteristics of TiSi-Si Diodes as a Reference

In order to make a statement about the performance of a C-Si contact using the BAT15 test vehicle, it is first necessary to discuss the characteristics of the commercial version with TiSi-Si. The diode used here is based on the version listed in Ref. [216]. Typically, J-V characteristics are shown here in the voltage range from $-1\,\mathrm{V}$ to $1\,\mathrm{V}$ in a semi-log scale (see Fig. 4.1(a)), as this is within the device ratings. The current should not exceed $110\,\mathrm{mA}$ ($240\,\mathrm{kA/cm^2}$) when forward biased whereas the maximum voltage value for a reverase polarity is specified as $V_\mathrm{r} = 4\,\mathrm{V}$. Fig. 4.1 illustrated, that TiSi-Si creates an excellent contact with a very low SBH, an ideality factor close to the perfect value of one and due to the thin epitaxial layer a low series resistance of $5.7\,\Omega$ ($2.6\,\mu\Omega\,\mathrm{cm^2}$). A Ti-Si contact fabricated by rf magnetron sputtering of Ti onto the BAT15 test vehicle — without any heat treatment of the final metallization — showed similar result. In comparison, the barrier is slightly higher and the ideality factor is not as good but the series resistance is lower. Fig. 4.1(b) illustrates that the homemade diode drives a larger current at $1\,\mathrm{V}$ because the size of the substrate is $1\,\mathrm{cm} \times 1\,\mathrm{cm}$ and therefore larger than in the commercial one. The diodes are separated in the packaged version and the substrate is thinned back. But thinning does not fully compensate for the advantage of a larger substrate, as examined by FEM simulations.

In the following, only the commercial BAT15 diode will be considered for further comparisons with C-Si diodes. The diode parameters (barrier height, ideality factor and series resistance) extracted by the Lambert W method are summarized in Tab. 4.1.

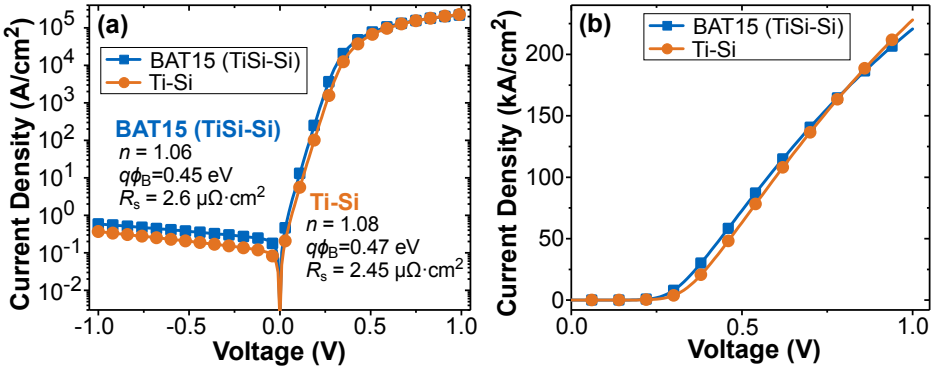

Figure 4.1: Comparison of the dc characteristics in a semi-log in (a) and fully linear scale in (b) of a commercial available BAT15 Schottky diode with TiSi-Si and a self-made Ti-Si contact by rf sputtering using the BAT15 test vehicle. Ideality factor n, SBH $q\phi_B$ and area-normalized series resistance R_s are displayed. They are very similar whereas the Ti-Si diode has a higher SBH and ideality factor but a slightly lower series resistance.

Table 4.1: Extracted TiSi-Si (BAT15) Schottky diode parameters. $q\phi_{B0}$ is the SBH without image-force lowering after Eq. 2.19.

$q\phi_B$	$q\phi_{B0}$	n	R_s
0.45 eV	0.47 eV	1.06	2.6 µΩ cm^2

4.2 DC Characteristics of CVD-C-Si Diodes

In order to be able to evaluate the fabricated CVD-C-Si diodes, a distinction must also be made between the two setups with the associated precursor gases. Apart from the gas used, the main difference is the deposition temperature and also the heating of the substrate.

Characteristics of Diodes Fabricated from C_2H_2 About 100 samples with GC deposited from acetylene were fabricated on the BAT15 test vehicle. The changes in the dc characteristics with altered process conditions were basically only minor. In Fig. 4.2(a),(b) are typical J-V curves of a C-Si diode — this diode also showed good reliability properties — in comparison with a TiSi-Si diode shown. Both have the same low Schottky barrier height of 0.45 eV and a low ideality factor < 1.1. Only the CVD-C-Si diode has a slightly higher R_s mainly due to the additional resistance of the 58 nm thick GC compared to TiSi. As shown in Fig. 4.2(c), the CVD-C-Si diode has a slightly higher reverse leakage current than the TiSi diode. A current density of 220 A/cm^2 (100 µA) is reached at a ~ 0.6 V smaller reverse voltage. The exact origin is not known as the two devices have the same SBH. It could be a consequence of the high temperature deposition of the GC as the dopants might start to diffuse and modify the epi-layer. The diode properties are furthermore very stable over time. A diode from the same substrate and deposition process showed

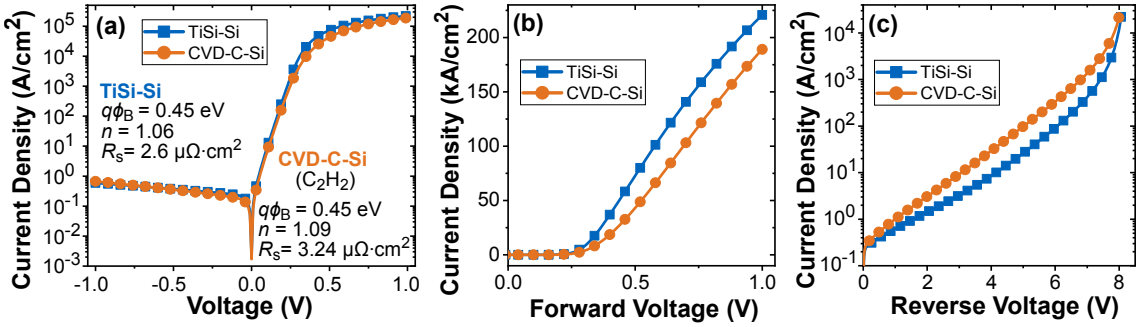

Figure 4.2: Comparison of the dc characteristics of a CVD-C-Si with a TiSi-Si diode. The GC has a thickness of 58 nm and was deposited from acetylene at 855 °C with a subsequent annealing step at 1000 °C. (a) shows the *J*-*V* curves in a semi-log and (b) in a fully linear scale. Ideality factor n, SBH $q\phi_B$ and area-normalized series resistance R_s are displayed in (a). The diodes are very similar and have the same SBH, only n and R_s of C-Si are not as good. (c) compares the reverse dc characteristics of a TiSi-Si and a C-Si diode. The C-Si diode has a lower blocking capability but the breakdown voltage is almost the same for both MS contacts (the last data point is where the breakdown occurred).

no change in the characteristics or a delamination of the GC from Si after more than four years after the fabrication.

It has been shown that GC grows layered [295] and has consequently anisotropic material properties. The in-plane resistivity can be determined quite easily by the four point method while the out-of-plane resistivity was extracted with help of the BAT15 test vehicle. For this purpose, GC was grown under the same process conditions from C_2H_2 only with different deposition times, which had a direct influence on the carbon thickness. The extracted series resistances are illustrated in Fig. 4.3 as a function of the film thickness and could be interpolated by linear regression. The slope of the data points yields the resistivity perpendicular to the surface to be about 50 mΩ cm, which is also used for FEM simulations. In contrast, the value in parallel to the surface was between 1 mΩ cm and 3 mΩ cm. This difference in the resistivity with a ratio of up to 50 suggests a layered growth, but is quite small compared to HOPG, which has a ratio of up to 1200 between the in- and out-of-plane electrical resistivity [100].

Characteristics of Diodes Fabricated from C_2H_4 Not as many samples were deposited from ethylene onto the BAT15 test vehicle by the second CVD setup. They fulfilled the desired reliability properties much better, as will be discussed in chapter 5. However, the initiation of the deposition process, as presented previously in section 3.2.2, had a greater impact on the resulting dc characteristics.

Typical *J*-*V* curves of C-Si diodes, deposited from C_2H_4, in comparison with a TiSi-Si diode are illustrated in Fig. 4.4(a),(b). The curves are quite similar but all the C-Si diodes have a lower SBH. A sample which was heated up in H_2 gas for 5 min before the precursor gas was turned on had only a barrier height of 0.41 eV.

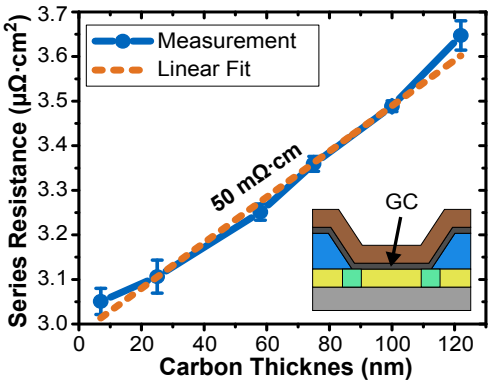

Figure 4.3: The area-normalized series resistance of the CVD-C-Si diode R_s as a function of the graphenic carbon thickness. All tested diodes have similar GC deposition parameters, only the growth time was altered, and the same metallization layers on top. The out-of-plane electrical resistivity is extracted to be 50 mΩ cm. Taken with permission from Ref. [MS17] © 2017 IEEE.

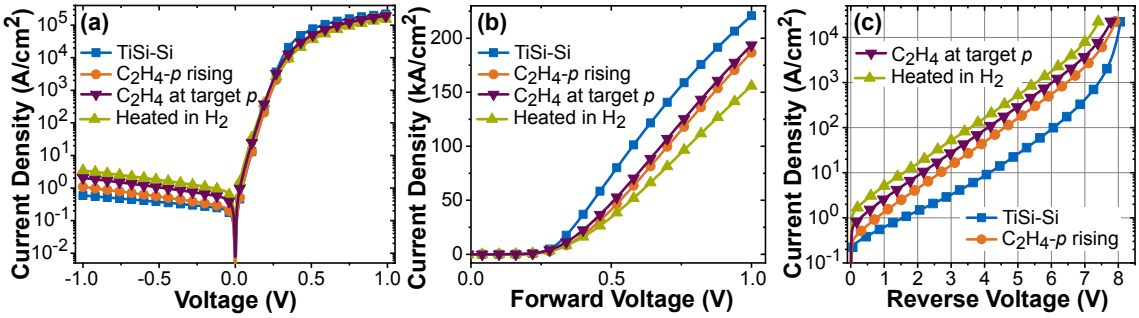

Figure 4.4: Comparison of the dc characteristics of CVD-C-Si with a TiSi-Si diode. (a) The graphenic carbon was deposited from ethylene with different process initiation procedures, but all at a temperature of 1000 °C. The J-V curves in a semi-log scale show that all the diodes are very similar, but the barrier height with carbon is always lower and ranges from 0.41 eV to 0.44 eV. The ideality factor is not as good as it is between 1.1 and 1.18. It is the highest for a sample heated in H_2, which also gives the lowest SBH. (b) shows the dc characteristics in forward direction in a fully linear scale. It becomes obvious that C-Si diodes have a higher series resistance. The sample heated at the target pressure of C_2H_4 just had a thickness of 11 nm compared to the other two samples which had a thickness of 37 nm (heated in H_2) and 28 nm (p rising), respectively. Taking this into consideration, it seems that samples with higher SBH have a lower R_s. (c) The reverse current characteristics are shown up to the voltage where the breakdown occurs. The higher the SBH, the higher is the observable reverse breakdown voltage. TiSi-Si has below 6 V a lower slope in the leakage current, but it increases afterwards. All CVD-C diodes have according to their SBH a similar breakdown behavior.

Unfortunately, these type of diodes have a higher ideality factor and series resistance compared to TiSi-Si and C-Si prepared with C_2H_2 — despite the carbon films here are thinner ($\leq 37\,\text{nm}$). One reason could be the higher growth temperature because the GC is better textured and consequently it has a higher out-of-plane resistance. Fig. 4.4(c) highlights that these type of C-Si diodes also have a higher leakage current when reverse biased compared to TiSi-Si. Nevertheless, the voltage points of breakdown seem to be in accordance with the lower barrier heights.

The SBH was also evaluated for CVD-C (C_2H_4, 1000 °C) on a high resistive p-type Si substrate. The diodes had no guard ring and just a circular contact region with top metallization. A sample heated in H_2 flow yielded a barrier height of about 0.72 eV, which is much higher than on n-Si where under similar process conditions an SBH of 0.41 eV was evaluated. Another experiment, with the sample heated directly in C_2H_4, showed a lower barrier on p-Si (0.68 eV), which is in turn consistent with the higher barrier height on n-Si (0.44 eV).

A rule of thumb states that the sum of the barrier heights of a metal on an n-type and p-type semiconductor should give the band gap E_g (1.12 eV for Si) [114]. Here, a sum of 1.13 eV and 1.12 eV, respectively, was calculated for the two process initiation procedures, which corresponds very well with the theoretical considerations. The used values are extracted directly from J-V measurements and consequently, they include the barrier height lowering. But even if some eV are added to compensate the lowering effect, the sum would be still very close to theory.

Overview of the Results Not all the fabricated diodes were considered furthermore. However, the essential dc characteristics (barrier height, ideality factor and series resistance) are summarized in Tab. 4.2 for diodes which showed desirable reliability properties, discussed in the following chapter.

Table 4.2: Extracted CVD-C-Si Schottky diode parameters for different deposition setups and conditions. The presented diodes showed the desired reliability properties. $q\phi_{B0}$ is the SBH without image-force lowering after Eq. 2.19.

Gas	$q\phi_B$	$q\phi_{B0}$	n	R_s	Thickness	Remarks
C_2H_2	0.45 eV	0.48 eV	1.09	$3.24\,\mu\Omega\,\text{cm}^2$	58 nm	—
C_2H_4	0.44 eV	0.47 eV	1.11	$3.31\,\mu\Omega\,\text{cm}^2$	28 nm	heated in C_2H_4 with flow
C_2H_4	0.41 eV	0.46 eV	1.19	$3.85\,\mu\Omega\,\text{cm}^2$	37 nm	heated in H_2 no flow

4.3 DC Characteristics of SC-Si and CN-Si Diodes

For sputtered films, not only their electrical resistivity is decisive, but rather the dc performance as a contact material to silicon. The dc characteristics in Fig. 4.5 illustrate that an SC-Si diode prepared at 20 °C reveals clearly non-ideal properties. It is hardly possible to extract the series resistance or ideality factor because the diode does not behave according to the thermionic emission theory. The reason for this is not evaluated in detail but previously presented analysis by Raman spectroscopy revealed that the carbon grows amorphous at room temperature. Usually, the conduction mechanism of amorphous carbon is described with the non-metallic Poole-Frenkel emission [318, 319], which might cause this undesirable behavior.

However, a substrate temperature of 100 °C was sufficient to fully change the forward conduction characteristics. The Schottky diode got a low ideality factor ($n = 1.17$) as the graphitization of SC led to properties more of a metal. A substrate temperature of 400 °C resulted in even improved characteristics, with a slightly better ideality factor ($n = 1.11$) and lower series resistance of 3.8 µΩ cm^2 compared to 4.95 µΩ cm^2.

Since it was expected that a higher temperature is also advantageous for CN-Si diodes, only samples prepared at 400 °C were used. However, the amount of incorporated nitrogen can be regulated by the sputtering conditions. Although it is known that a small content is desirable for low electrical resistivity, nevertheless, the amount of N can have a decisive influence on the contact properties. From Fig. 4.6 it is obvious that a high fraction yields a lower SBH but the forward conduction is far from ideal and does not behave according to the thermionic emission theory anymore. It is assumed that these type of films are less graphenic and tend to be

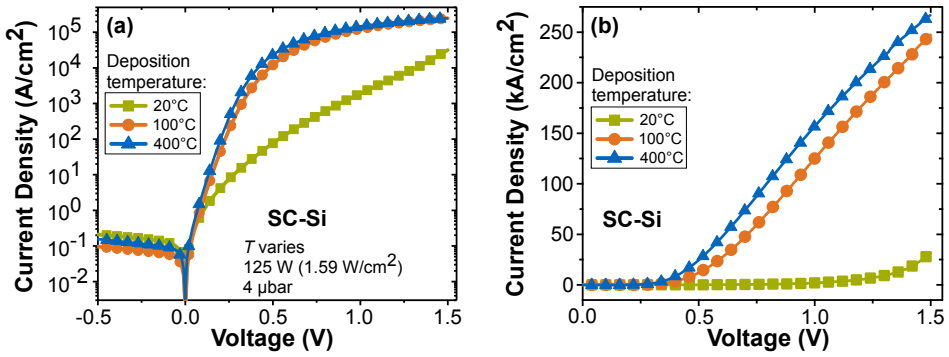

Figure 4.5: J-V curves of SC-Si diodes sputtered at different sputter temperatures whereas power (1.59 W/cm^2) and pressure (4 µbar) were kept constant. The diode sputtered at 20 °C has a lower SBH but the forward behavior is far from ideal. The barrier height of the shown diodes ranges from 0.45 eV to 0.48 eV and could also represent a certain process fluctuation. A substrate temperature of 100 °C was sufficient to change the conduction properties of the carbon-silicon interface and the diode shows electrical characteristics more close to a device sputtered at 400 °C. Taken from Ref. [MS19].

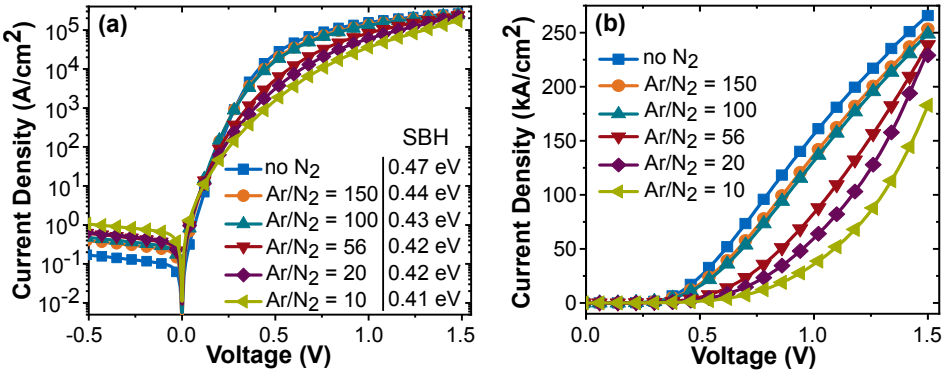

Figure 4.6: *J-V* curves of CN-Si diodes sputtered at different Ar/N_2 ratios in a semi-log in (a) and a fully linear scale in (b). The diode without N_2 is an SC-Si contact. The thicknesses of all films is in-between 5 nm and 7 nm. A higher content of incorporated nitrogen leads to a lower SBH (the respective values are given in (a) for all diodes) but the forward conduction is less ideal with higher R_s.

more fullerene-like with more sp^3 bonds. Sputtering in pure N_2 atmosphere was not tested but could provide an even smaller barrier, as long as the film can incorporate higher contents of nitrogen. With less N in the sputter gas in turn, the barrier gets higher and the overall dc characteristics approach that of an SC-Si diode.

To enable a better comparison of the CN-Si diodes presented before, the sputter time was 2 min for all films as this resulted in similar thicknesses. Nevertheless, Fig. 4.7 highlights that there is no change in the dc characteristics of a diode when the CN thickness was increased from 5 nm to 35 nm. The process conditions were all the same, except the sputtering time was 11 min instead of 2 min. Both curves are almost identical but there is hardly an improvement in the series resistance of the diode with thinner CN — even if they have the same electrical resistivity of 8.4 mΩ cm. A decrease of the CN thickness to 0.7 nm (not shown) did neither cause a reasonable improvement. A similar result was also observed when comparing SC-Si

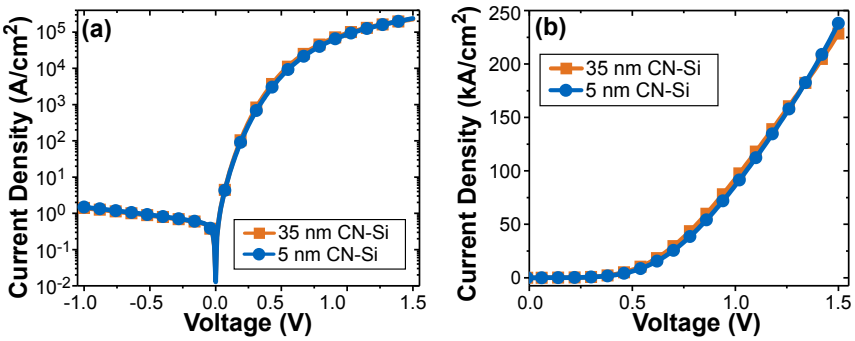

Figure 4.7: Comparison of the dc characteristics of CN-Si (400 °C) diodes with 5 nm and 35 nm thick CN in a semi-log in (a) and linear scale in (b). Both curves almost match each other and only the diode with the thinner CN drives more current at a voltage ≥ 1.5 V. Taken from Ref. [MS19].

diodes with carbon of different thicknesses. The reason is not known but it seems that R_s is mainly determined by the contacts and less by the thickness of SC or CN. In contrast, CVD-C-Si diodes show clearly a thickness dependence as previously presented in section 4.2.

Comparison of SC-Si and CN-Si with TiSi-Si and CVD-C-Si However, a fundamental question is how the sputtered carbon behaves in comparison to TiSi or CVD-C, which was deposited at much higher temperatures. Fig. 4.8(a) & (b) clearly illustrate that the electrical characteristics of an SC-Si diode grown at 400 °C is even close to a TiSi-Si and a CVD-C-Si diode. The SBH is with 0.48 eV slightly higher, as previously shown. However, if an ohmic contact is desired, the lower barrier height of 0.42 eV of a CN-Si diode is very beneficial even if the behavior in forward direction is less favorable. The Ar/N2 ratio during sputtering for CN-Si diode shown here was 56 as this was also used in subsequent reliability investigation. The reverse leakage behavior and the breakdown voltage depend on the one hand on the SBH of the contact and on the other hand on the used temperature budget, which can induce a diffusion of the dopants. Fig. 4.8(c) highlights that the CN-Si diode even performs better than a CVD-C-Si diode as they both have the same breakdown voltage but the CN creates a lower barrier. CN-Si has a lower leakage current at $V_r > 1$ V due to the lower deposition temperature of 400 °C in contrast to the 1000 °C used in the CVD process. This suggests that no dopant diffusion occurred at low deposition temperatures (the epi-layer thickness stayed constant) and consequently no change in the breakdown characteristics of the test vehicle can be observed.

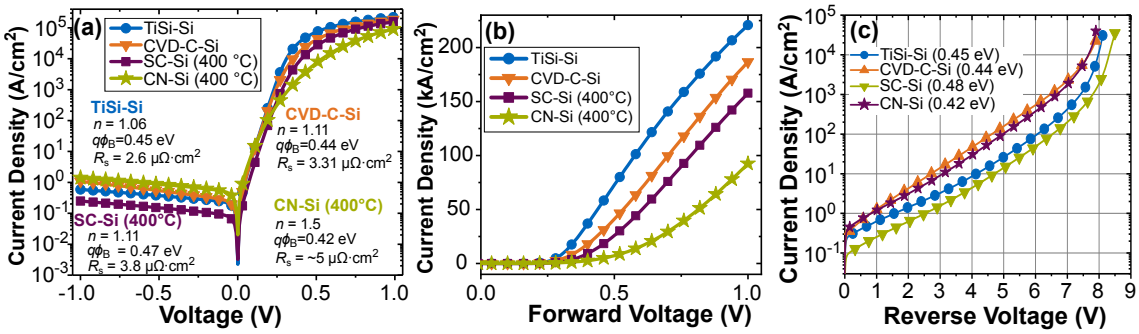

Figure 4.8: Comparison of the dc characteristics of a TiSi-Si, a CVD-C-Si, an SC-Si and a CN-Si diode. The thickness of CVD-C deposited, at 1000 °C is 28 nm, and of SC and CN is 35 nm. (a) shows the J-V curves in a semi-log scale and displays ideality factor n, SBH $q\phi_B$ and area-normalized series resistance R_s. The electrical characteristics of all the C-Si diodes are close to TiSi-Si. The CN-Si has a lower SBH but a higher ideality factor and series resistance. Latter is clearly illustrated with J-V curves in a fully linear scale in (b). SC creates a diode with a forward conduction behavior close to one with CVD-C. (c) The reverse current characteristics are shown close to the voltage where the breakdown occurs. It is necessary to have a high SBH to achieve a higher reverse breakdown voltage. Adapted from Ref. [MS19]

SBH-Shift by a High Bias It should be mentioned that the Schottky contact of sputtered carbon to silicon is not stable under all conditions. A dc voltage stress with high forward V_f or reverse bias V_r altered the interface properties of SC-Si and CN-Si, especially a change of the SBH was observed. The normal or safe operation area was defined to be within $V_r \leq 4\,V$ and $V_f \leq 1\,V$ because almost no changes in the pristine device properties are detectable if operated there. As illustrated in Fig. 4.9, dc sweeps to $V_r = 7.5\,V$ or $V_r = 7.3\,V$ of SC-Si or CN-Si, respectively, led to a decrease in the barrier height. The set voltage level was roughly about 0.5 V below the breakdown. After this sweep, a much smaller SBH can be measured at the CN-Si diode. It was even decreased to 0.39 eV, which is about 13 % lower than the TiSi-Si contact. The way for a 'zero-barrier height' is in fact paved by CN films with higher N content as they decreased their barrier height in a similar experiment from 0.41 eV to 0.36 eV, which could result according to Eq. 2.12 in very low contact resistance.

A device operation at higher forward bias ($V_f > 1\,V$) showed the opposite behavior as the SBH increased as consequence. After a dc sweep to 2.1 V, a $\sim$ 10 % lower SBH compared to the as-fabricated diode was obtained. Applying a constant high forward or reverse voltage for a much longer duration could even cause higher or lower values, respectively. The process hereby was fully reversible as a high SBH could be tuned to be smaller and vise versa.

However, a higher SBH is easier to achieve as the required voltage to force a change is lower. Also repeated dc cycles or a constant reverse bias were needed to retrieve the lower SBH. Without an applied bias the SBH was very stable over time even at temperatures up to about 85 °C (for 20 h) and did not recover back to the start value. The relative deviation to the as fabricated values is even after a treatment of 150 °C for 24 h still in average about 60 % (100 % deviation is directly

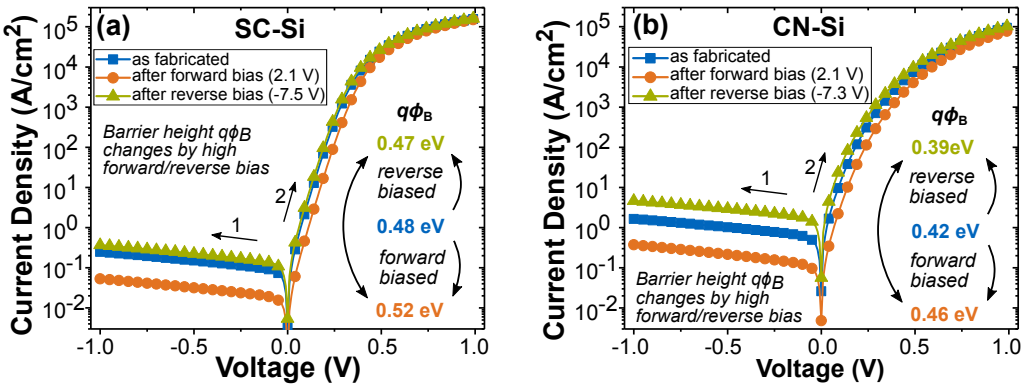

Figure 4.9: Comparison of the dc characteristics of a SC-diode (no N_2) in (a) and a CN-diode in (b) as fabricated, after being forward biased with 2.1 V and after being reverse biased with 7.5 V or 7.3 V, respectively. The reverse characteristics from 0 V to −1 V were measured first, followed by measurements in forward direction (0 V to 1 V). The SBH ϕ_B changes according to the applied polarity and is reversible by applying the opposite voltage direction. Taken from Ref. [MS19].

after the stress). The diode behaved as if an interface dipole was present, like the previously discussed molecular electric dipoles (see section 2.2.3), which arise by charge rearrangements at the interface. Similar phenomena have also been reported for graphene-silicon carbide Schottky junctions [320, 321].

Overview of the Results In Tab. 4.3 are basic dc parameters of the as-fabricated SC- and CN-Si diodes summarized, which had desirable reliability properties. The CN-Si with 0.7 nm of carbon has a slightly higher SBH but a lower ideality factor.

Table 4.3: Extracted SC-Si and CN-Si Schottky diode parameters. The presented diodes showed desired reliability properties. $q\phi_{B0}$ is the SBH without image-force lowering after Eq. 2.19 — the results must be considered with caution.

Ar/N_2	$q\phi_B$	$q\phi_{B0}$	n	R_s	Thickness	T
no N_2	0.47 eV	0.5 eV	1.11	3.8 µΩ cm^2	35 nm	400 °C
56	0.42 eV	0.55 eV	1.5	∼ 5 µΩ cm^2	35 nm	400 °C
56	0.42 eV	0.55 eV	1.5	∼ 5 µΩ cm^2	5 nm	400 °C
56	0.43 eV	0.54 eV	1.4	∼ 5 µΩ cm^2	0.7 nm	400 °C

4.4 Additional Properties of GC Films

An essential difference between graphenic carbon and conventional metals is the temperature behavior of the electrical resistivity ρ. Elementary metals usually have a positive temperature coefficient (PTC) of resistance, which means that their resistivity increases as the temperature rises. Graphite and also GC have a negative temperature coefficient (NTC) because ρ becomes lower as the temperature increases. Furthermore, as displayed in Fig. 4.10, this effect is independent of the production method (sputtering or CVD). At elevated temperatures more electrons fill the conduction band, which is more pronounced in samples with high resistivity as they probably have a higher band gap. The carbon film deposited at 20 °C exhibits an about 65 % higher conductivity at 200 °C. In contrast, the CVD-C is at room temperature already a good conductor with more free electrons available and this led only to an ∼ 15 % increase in conductivity at 200 °C.

It has been reported that especially nitrogen-free SC films, but also CN films, get a higher electrical resistivity ρ over time [181, 305]. It is assumed that humidity in the air is adsorbed and finally water diffuses into the film and deteriorates ρ. To verify this, a sample with an SC film was kept in atmosphere (the humidity was not monitored) and another one in DI water.

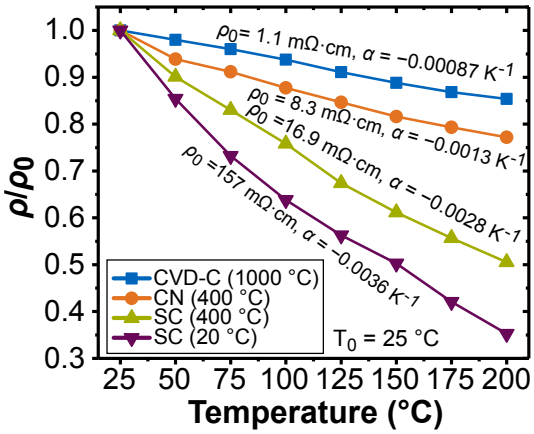

Figure 4.10: Measurement of the temperature-dependent relative electrical resistivity ρ/ρ_0 of CVD-C deposited at 1000 °C, CN deposited at 400 °C and SC deposited at 400 °C and 20 °C, respectively. ρ_0 is the initial resistivity at $T_0 = 25$ °C. All of them feature an NTC α, which was fitted for simplicity with a linear behavior over the measured temperature range. Taken from Ref. [MS19].

As can be seen in Fig. 4.11, both SC films show a very strong increase in ρ regardless of whether they were exposed to water or the atmosphere and have increased by at least 85 % after 62 days. Also a subsequent treatment with chemicals did not improve the resistivity again. Several treatments were tested, like hot (70 °C) acetone, IPA, SC-1 and SC-2 cleaning solutions, each of them for 10 min, but neither caused a reasonable change. A dip in HF or buffered HF (NH_4F with HF) for 5 min showed the same result. The same applies if the sample is stored in vacuum at a pressure of 1×10^{-6} mbar for several days. Only if the sample was heated in vacuum to 400 °C for one hour, a drop to $\rho/\rho_0 = 1.2$, but not the original start value, was observed.

In contrast, a CN film showed only an increase of 3 % after 44 days (see Fig. 4.11). A possible explanation is that CN is less sensitive to the presence of water or that the film is less porous compared to SC, which prevents the water from diffusing.

It gets obvious, that the time required to transfer the samples from the sputter chamber to the measurement setup could already lead to a considerable degradation. The measurement results, especially with SC films, are in general affected by a certain uncertainty. Therefore, it would be beneficial if ρ is already measured in vacuum to exclude errors. This phenomenon may also have a negative effect on the properties of the diode, hence a break in the vacuum should be avoided before GC is covered by the top metallization.

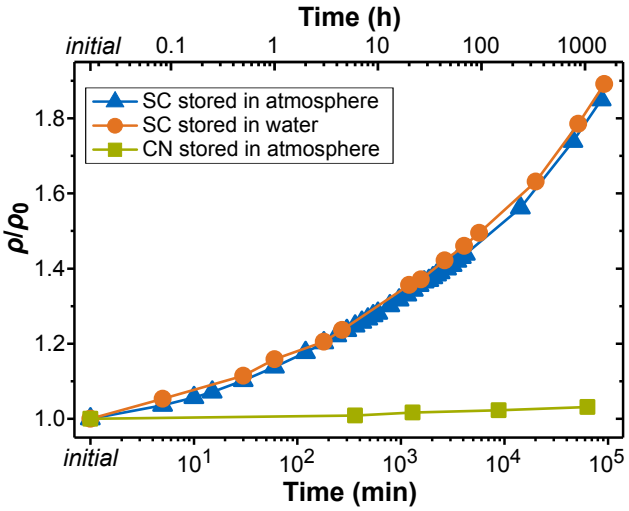

Figure 4.11: The change of the relative electric resistivity ρ/ρ_0 of SC and CN films on SiO_2/Si substrates after an exposure to atmosphere or storage in DI water. The initial resistivity value ρ_0 was measured by the four-point probe method within 5 min after removal from the sputter chamber and was 17 mΩ cm for SC and 8.5 mΩ cm for CN films. The SC sample that was stored in water was taken from the bath for periodic measurements whereas the other sample was analyzed automatically at fixed time intervals. The CN film was measured at arbitrary points in time.

5 Reliability Investigations of C-Si in Comparison to TiSi-Si

This chapter presents the obtained reliability results of the metal-silicon contact when stressed with ESD-like high current pulses. A comparison is made between TiSi, CVD-C and sputtered carbon (SC, CN) using the BAT15 diode/test vehicle. Before a detailed overview on the measurement results is given, the findings from FEM simulations are discussed.

The reliability tests were only carried out with positive pulses applied in the forward direction of the diode. Reverse pulse stress through the C-Si Schottky diode revealed a filamentary breakdown visible as burn marks in the top metallization, as shown in Fig. 5.1. During such a pulse, much more heat is generated as the depletion region is quite large, which increases the electrical resistivity at this area. As the applied electrical field is beyond the breakdown field of silicon, it is further assumed that a very localized mesoplasma is formed [322]. As a result, the temperature at these regions was increased to such an extent that the diode failed very quickly. Furthermore, it is expected that this happened regardless of the contact material used.

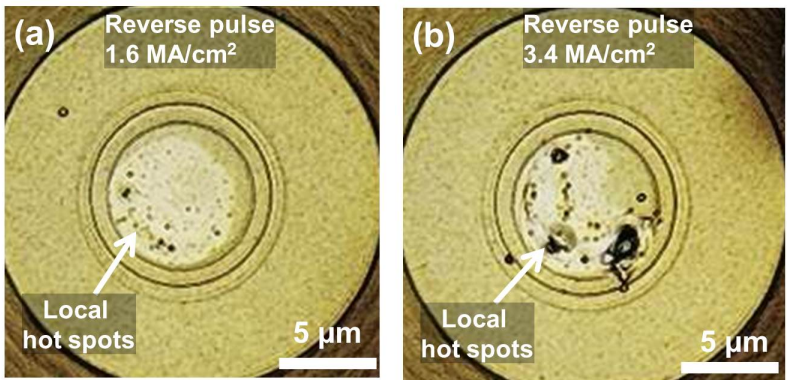

Figure 5.1: Micrographs of failed C-Si diodes after being stressed with a single current pulse applied in the reverse direction of the diode. A current density of (a) 1.6 MA/cm^2 and (b) 3.4 MA/cm^2 was used. A damage is clearly visible as burn marks on the 200 nm thick top metallization, which were caused by very localized high temperature hot spots. The higher the current density, the more severe is the damage.

5.1 Electro-Thermal FEM Simulations

It is not possible to visualize the exact current and especially the heat distribution during a short current pulse in the junction of a real device. Instead, to get a deeper insight, coupled time-dependent electro-thermal simulations based on the finite element method (FEM) with the model presented in section 2.5 were performed using COMSOL multiphysics.

The temperature distribution near the active region of a C-Si diode with 30 nm thick carbon, which had an electrical resistivity of 50 mΩ cm, is shown for different time steps in Fig. 5.2(a)-(d). The current density is in average 3.5 MA/cm^2 with a rise time of 15 ns. Such a pulse results in a power density of over 1 TW/cm^3 for silicon with a resistivity of 0.1 Ω cm.

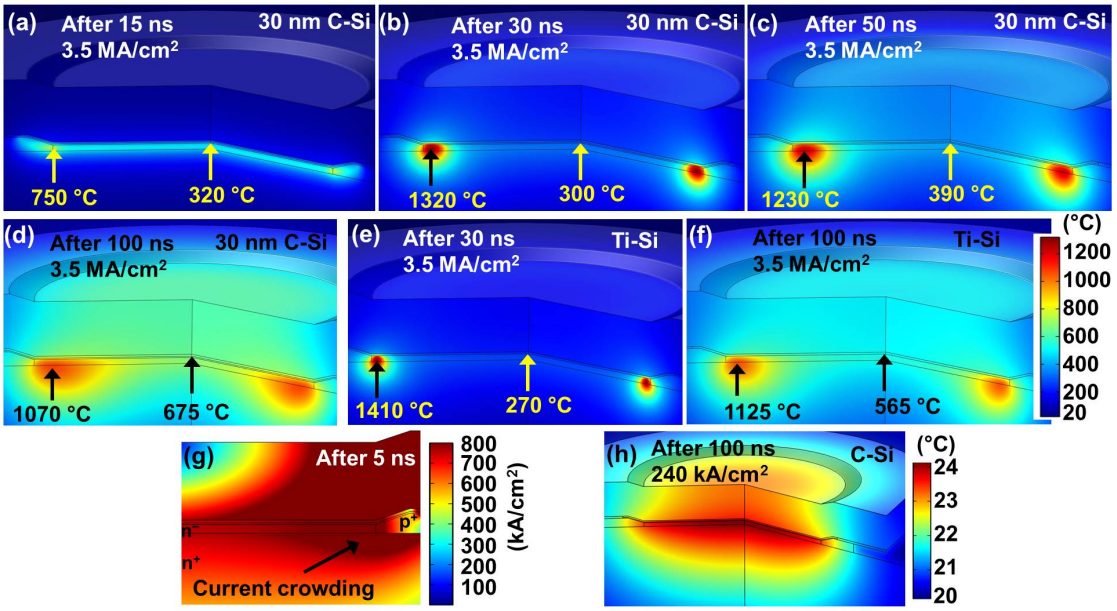

Figure 5.2: Coupled transient electro-thermal simulations of the used Schottky contacts. Images (a)-(f) share the same temperature color legend. (a)-(d) show the temperature distribution in a C-Si diode when stressed with a 3.5 MA/cm^2 current pulse. A peripheral hot spot is created in the epi-layer during the pulse at the region while the center part is much cooler. After the heat spreads out, the center of the active Si region gets more conductive and the hot spot cools down. In (e) and (f) is Ti (no GC) used as interface metal. The circular hot spot is also formed but it is hotter and the temperature remains higher after 100 ns. The image in (g) shows the normalized current density in a cross-section of a C-Si diode after 5 ns while the pulse is rising. Current crowding at the transition area between epitaxial layer and guard ring is visible. (h) shows the temperature increase at the junction of the device operated at normal conditions (240 kA/cm^2) with a small temperature increase at the junction whereby the center is the warmest.

After 15 ns (see Fig. 5.2(a)) it is already obvious that the active area close to the guard ring structure is heated more and reaches a temperature of 750 °C, which is more than twice the temperature compared to the center of the junction. As the resistivity at the warmer region of the low-doped Si becomes intrinsic and thus lower than at the center part, more current will consequently flow at the edges. After 30 ns — this is roughly the time when the temperature is the highest — the Joule heating creates a peripheral hot spot around the active area. This leads to a very high damage probability at this region as the maximum temperature even approaches the melting point of silicon (1412 °C).

Fig. 5.2(c) illustrates that the hot spot in the C-Si diode cooled down from 1320 °C to 1230 °C as the heat spread out to the periphery. The reason is the relative high electrical resistivity of GC, which is at these temperatures already higher than that of silicon. Therefore, it is not able to provide enough current to maintain the hot spot at such a high temperature. Consequently, more current flows through the cooler center part of the active region and heats it up. The exact shape of the temperature-dependent resistivity of GC has hereby a negligible influence on the temperature distribution and the absolute values within the diode. Even by assuming a temperature independent value of $\rho = 50\,\mathrm{m\Omega\,cm}$, a variation below 10 °C ($< 1\,\%$) in the heat distribution was observed.

Fig. 5.2(e),(f) illustrated that this circular hot spot is also formed in case of a Ti-Si contact. After 30 ns, the temperature is so high that the silicon might even start to melt. Additionally, it remains higher after 100 ns and does not spread out that much. As Ti or TiSi has an about 1000-times lower resistivity than the employed carbon, it provides enough current to keep the hot spot at high temperatures. In turn, this leads to a higher damage probability as an interdiffusion of silicon, metal or dopant atoms are more likely than at a device with GC-interface.

The origin of this phenomenon is guided by current crowding at the edges of the low doped epitaxial layer — despite the thick top metallization. Fig. 5.2(g) illustrates the current distribution in a C-Si diode after 5 ns while the pulse still rises. The diode is here still at a lower temperature but the current is already concentrated to the edges of the active region, which leads to an increased heating of this area and the silicon epi-layer becomes more and more intrinsic. Current crowding is no issue at normal operation conditions with low current densities ($240\,\mathrm{kA/cm^2}$). The diode is still cool and close to room temperature after 100 ns during such a pulse while the inner part of the active region is heated more, as shown in Fig. 5.2(h). The heat distribution is similar in a stationary simulation, where only the temperature increased to ~ 35 °C.

The concentration of the current at the edges was verified with a real C-Si diodes by stressing the diode with a thinner top metallization (120 nm). Fig. 5.3(a),(b) illustrate that a recrystallization of the metal occured at the transition region between active area and guard ring. Indeed, in a circular fashion, which points to a higher temperature at the edge region. Interestingly, the marks here are also visible at regions which are not just in the direct path of the current flow. However, a com-

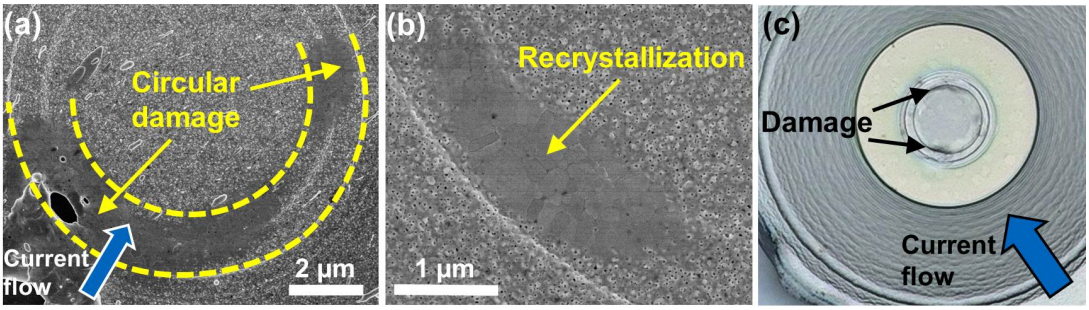

Figure 5.3: The SEM images in (a) and (b) show C-Si diodes with thinner metallization after several 3.5 MA/cm^2 pulses were applied. (a) The direct current path from the probe tip to the diode is indicated by the blue arrow. A recrystallization of the top metallization at the transition region between guard ring and active epi region occurs. A damaged region with recrystallized metal is highlighted in (b). In (c) is a micrograph of a failed C-Si diode shown after the copper has been removed wet-chemically. Damaged spots at the edges of the active region are visible through the Ti and GC. (a) and (b) are taken from Ref. [MS17].

parable damage scenario can be observed in diodes with a thicker top metallization. Fig. 5.3(c) shows a microscope image of a failed diode where the copper has been removed and opened the view to the active area. Damaged spots, maybe due to molten silicon or diffused metal, are visible at the edges of the active region and support or verify the simulation results. The edge burnout in Schottky diodes at short pulse durations at a high applied power has also been confirmed by Anand *et al.* [323].

Fig. 5.4(a) and (b) show the simulated maximal temperatures in the diode and the temperatures in the center of the active region over time for different carbon thicknesses. A thicker GC can also be treated simply as a film with higher electrical resistance at constant thickness and vice versa. But it becomes obvious that the maximum temperature in the diode decreases when a thicker film is used in the simulations, although this is an additional heat source. The reason for this is that the high-ohmic carbon prevents current corwding and more current is forced to flow through the center part.

However, if the layer thickness is greater than 100 nm, the maximum value does not drop as much because the total resistance is higher and the circular hot spot moves more to the center of the diode. As can be seen in Fig. 5.4(b), the temperature there almost corresponds to the maximum one. Furthermore, it indicates a drop in the temperature after about 18 ns before it rises again. The reason is that the circular hot spot is created at this point in time whereas the middle part is barely heated anymore.

It could already be seen in the previously shown Fig. 5.2 that copper — with its moderate heat capacity but excellent thermal conductivity — becomes very hot. Fig. 5.4(c) shows the temperature on top of Cu during the pulse at varied GC

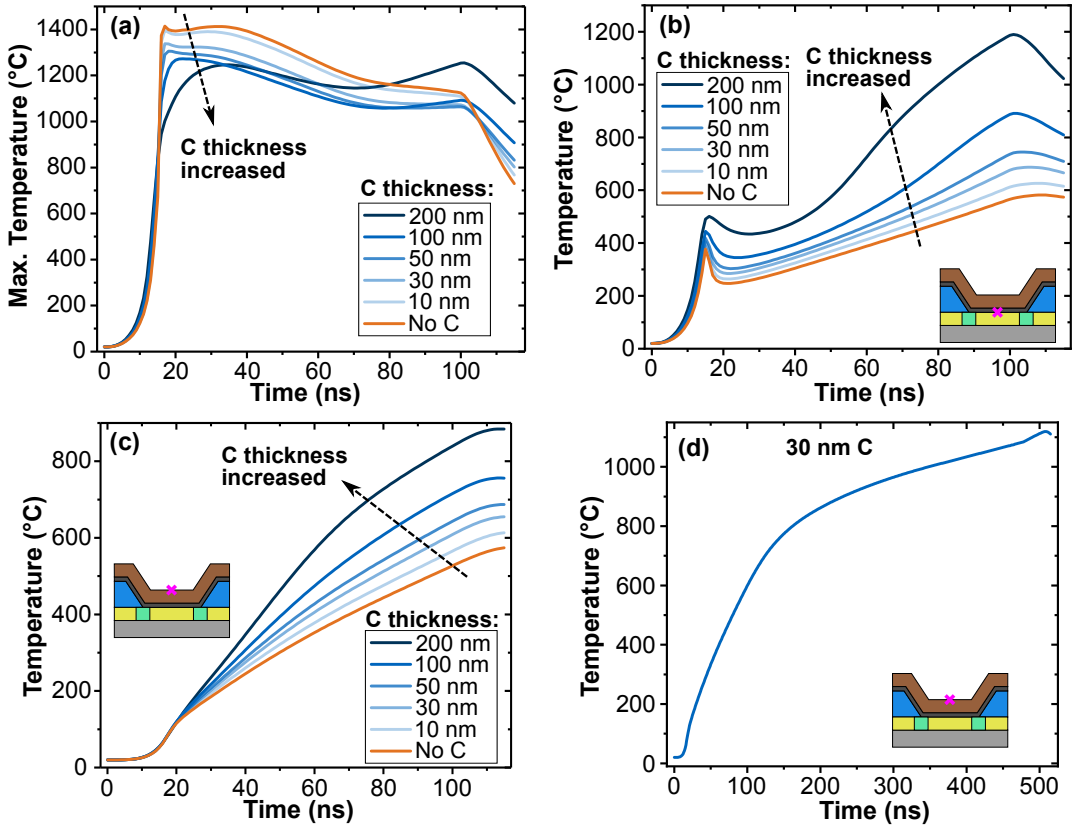

Figure 5.4: The maximum temperature during FEM simulations of the Schottky diode as a function of time for different thickness of carbon is given in (a). No C means that Ti is in contact to Si. The thicker the carbon layer, the lower is the maximum temperature and it is more constant during the whole pulse duration. (b) shows the simulated temperature profile at the junction in the center of the diode. A thicker carbon layer causes higher temperatures as the heat could spread better away from very hot regions. (c) shows the temperature profile in the center of the diode at the top of the metallization (copper) for different carbon thicknesses. The ticker the carbon, the higher the temperature at this point. The temperature on the copper surface for a diode with 30 nm thick carbon at a longer pulse duration is given in (d). Even the melting point of Cu is reached at the surface after 500 ns.

thickness. The ticker it is, the hotter the metal. In this case the heat is more equally distributed over the active region and of course, the carbon acts due to its high electrical resistivity as additional heat source.

Furthermore, the temperatures gets quite high within the materials, which would lead to thermal expansion. This was not considered in the simulation here, but in the real device it might lead to a pile-up of the metal in the middle, which would also change the current flow at the edges. A 500 ns long pulse at a 30 nm C-Si diode could heat the Cu even to its melting point (see Fig. 5.2(d)). This can cause very severe damage as the temperature in the active region must be much higher after such a long pulse.

5.2 Reliability of TiSi-Si BAT15 Diodes

It was previously shown that the GC-Si contact has similar electrical properties compared to TiSi-Si. However, in order to evaluate whether GC has an advantage in terms of reliability, this must first be discussed in the case of TiSi-Si. It is assumed, if an ESD-like pulse with high current density is applied to such a contact, the junction can be easily heated to temperatures above 1000 °C due to the dissipated power — as FEM simulations suggest. As indicated in Fig. 5.5, high temperatures (and additionally high electrical fields) can cause a diffusion of Ti or TiSi through the thin epi-layer towards the highly doped substrate.

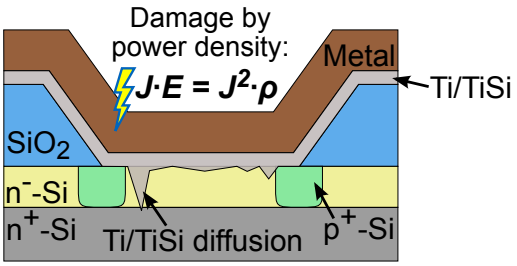

Figure 5.5: A schematic cross-section of a simplified TiSi-Si Schottky diode were a high current pulse was applied. The Joule heating (see Eq. 1.4) forces Ti or rather TiSi to diffuse into the n^--Si epitaxial layer, which could even reach the highly doped substrate.

The reliability tests were performed on commercially available BAT15 Schottky diodes with TiSi-Si contact at room temperature. At a current density J of $3.5\,\mathrm{MA/cm^2}$ and a pulse width of 100 ns, even a single pulse in forward direction can degrade the original behavior of the diode, indicated by the over 100-times increase of the reverse current at $V_\mathrm{r} = 1\,\mathrm{V}$, as highlighted in Fig. 5.6(a). This might signal the inter-diffusion of Ti or TiSi within the epitaxial layer. Further pulses incrementally deteriorated the device even more as a metal or silicide filament might be created as shown in Fig. 5.5. The diode is almost short-circuited after three pulses and a normal operation is not possible anymore.

The pulse number-dependent failure probability in Fig. 5.6(b) shows that a TiSi-Si contact typically fails between two and four pulses ($3.5\,\mathrm{MA/cm^2}$, 100 ns). Thereby, the failure of the diode was defined when the diode degrades to a reverse current larger than $220\,\mathrm{A\,cm^{-2}}$ (100 µA) at $V_\mathrm{r} = 1\,\mathrm{V}$. As the number of pulses is quite low, the diode was also tested at lower current densities, as shown in Fig. 5.6(b). It is evident that the maximum number of transient stress pulses depends on the used current density level. The duty cycle was below 0.0001 and it is assumed that the time between each pulse is sufficient to let the sample cool down to room temperature. The failure probability is spread over a wide range for $J = 1.35\,\mathrm{MA/cm^2}$, which is close to the permissible pulse load ($\sim 1\,\mathrm{MA/cm^2}$) specified by Infineon [216]. A diode could withstand 100 thousand events while another one failed only after up to a million pulses. But the current density was not that high and it gets obvious

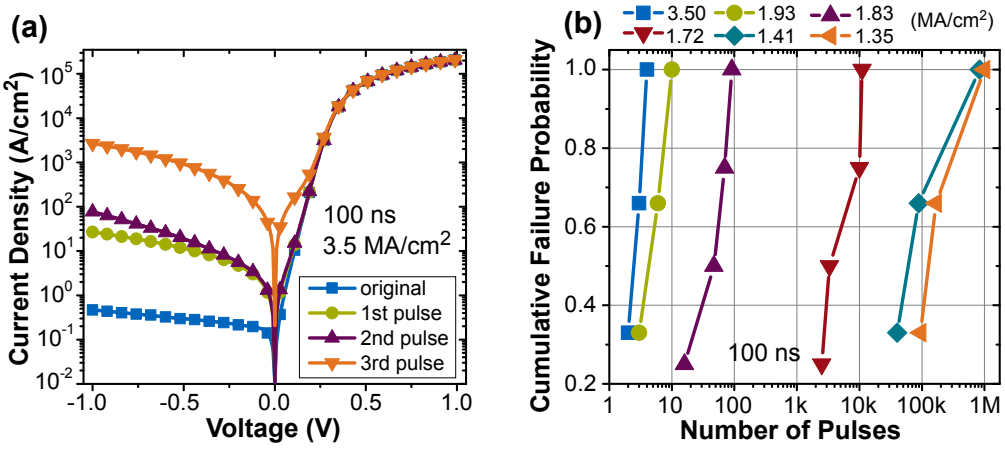

Figure 5.6: The J-V curves in (a) show the degradation of a TiSi diode pulsed with a current density of 3.5 MA/cm^2 and a pulse width of 100 ns. Every single pulse led to a deterioration of the reverse behavior of the diode and after the third pulse was the reverse current severely increased. (b) illustrates the failure probability versus the number of pulses at different current densities for commercial BAT15 diodes (TiSi-Si). At least three devices were stressed for a given pulse current density, a pulse width of 100 ns and a duty cycle < 0.0001. The failure of the diode was defined when the diode degrades to a reverse current $> 100\,\mu$A (220 A/cm^2) at $V_r = 1$ V. Adapted from Ref. [MS17].

(see Fig. 5.6(b)) that a higher J leads to an earlier failure as more heat is generated during the pulse. For example, raising J from 1.35 MA/cm^2 to 3.5 MA/cm^2 corresponds to an increase in power density of about 570 % because it is proportional to J^2.

The pulse endurance tests were also carried out with the Ti-Si diodes manufactured in-house. Even if the interface differs slightly, these devices also fail after 2–4 pulses. This provides an indication that it is not the package, the thinner substrate or, above all, another top metallization of the commercial BAT15 diode that is responsible for the early failure, but rather the contact itself.

5.3 Reliability of CVD-C-Si Diodes

5.3.1 Evaluation of Diodes with Carbon Deposited from C_2H_2

Reliability testing of samples deposited from C_2H_2 was accompanied by a long learning process. So, first the cleaning procedure of the used substrates and the setup itself had to be optimized. Most samples showed a stability against pulses with high current density in the range similar to TiSi-Si or up to 10 000 events. The failure of the diode was in general defined when the diode degrades to a reverse current ≥ 220 A/cm^2 at $V_r = 1$ V. However, it was known from preliminary tests that the C-Si should be much more stable. Finally, after chemical cleaning of the quartzware of the CVD equipment and an optimization of the substrate cleaning

procedure, the desired reliability could be demonstrated. For instance, a diode with 58 nm thick carbon showed a pulse endurance of at least 100 million stress events. Ten diodes were tested but the measurements were not continued until the contact failed. Instead, it was always stopped after 10^6, 10^7 or 10^8 pulses, respectively.

Fig. 5.7(a) shows on the basis of the J-V curves of a diode that no significant degradation occurred. The contact is very stable in its electrical properties after an increasing number of pulses have been applied to it. Only a continuous increase of the SBH from 0.45 eV to about 0.48 eV after 100 million pulses was observed. An increase of the barrier height leads in turn to a reduction of the reverse leakage current and a better blocking capability, as shown in Fig. 5.7(b). Similar findings were already presented for sputtered carbon diodes after they were stressed with a forward bias. The effect could also be related to an interface dipole, but it is less pronounced here. The new barrier height is stable over time, as long as no external voltage is applied.

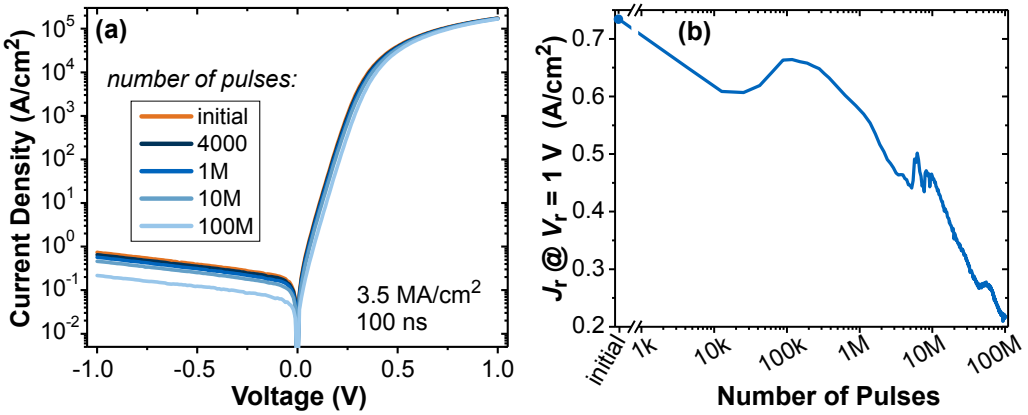

Figure 5.7: The J-V curves in (a) show the change in the dc-characteristics of a 58 nm CVD-C-Si diode (C_2H_2 as precursor gas) after several million current pulses (3.5 MA/cm^2, 100 ns) were applied. The forward conduction behavior is almost not affected after up to 100 M pulses. Only the SBH became larger, which leads to a lower reverse current. (b) shows that the reverse current density J_r at a reverse voltage V_r of 1 V decreases almost constantly with the number of pulses. A temporary increase in the current is associated with an initial burn-in behavior, mechanical vibrations at the setup and a change in the room temperature during day and night as the test took about 38 hours.

5.3.2 Evaluation of Diodes with Carbon Deposited from C_2H_4

Unfortunately, it turned out that the reliability decreased at subsequent carbon depositions, which is why no supplementary investigation of thinner carbon could be carried out by using this setup and precursor gas. Therefore, further deposition tests were accomplished with another CVD system and with ethylene as feedstock. Here, promising results could be generated very quickly and a diode with 28 nm thick carbon heated under process gas could easily endure over 400 million pulses,

as illustrated in Fig. 5.8(a). Before such a diode failed, it was still fully functional and did not show any reasonable deterioration after this high number of stress pulses (see Fig. 5.8(b)). The SBH only showed an increase of 0.01 eV after 500 million pulses, which is in contrast to the device discussed before much smaller. The C-Si interface layer is therefore very stable here and not prone to a dipole formation.

A first degradation was observed for this diode after 545 million pulses when presumably first atoms from the top metallization diffused through the carbon and changed the properties of the barrier. These atoms/ions might then be the origin of a further deterioration of the properties if the tests are continued until the device finally fails. The failure probability was here between 420 million and 548 million pulses. Under these test conditions, graphenic carbon can enhance the robustness against ESD-like high current events by a factor of over 100 million compared to the TiSi diode (Fig. 5.8(a)). The improvement might be attributed on the one hand to the about 1500 times smaller diffusivity of C in Si than Ti in Si at 950 °C [177, 178] and on the other hand due to the excellent diffusion barrier properties of sp^2-bonded carbon.

As an increase in the maximum current density was not possible with the so far used pulser setup, the pulse width was increased to force an earlier failure of the C-Si contact. Fig. 5.8(c) illustrates the pulse-number dependent failure probability for different pulse lengths. When the pulse width is doubled at the same current density of 3.5 MA/cm^2, the total applied energy is also doubled. However, the reliability is still excellent for 200 ns long pulses and a wear-out was observed between 150 million and 240 million pulses. It becomes obvious that a higher pulse width led to an earlier failure and for a width of 1 µs (the applied energy is increased by a factor of ten) a failure was observed between 5000 and 16 000 pulses. If this result is compared with the TiSi-Si contact, which has already failed after 2–4 pulses at a pulse length of only 100 ns, this is an amazing reliability. Furthermore, Fig. 5.8(d) shows the threshold number of pulses for a failure of the C-Si contact as a function of the pulse width and defines the 'safe-area' for operation. The curve looks very similar to the Wunsch-Bell [324] and Dwyer *et al.* [325] characteristics, which in contrast give a relation between power and pulse width.

Fig. 5.8(e) reveals that the tested diodes are no open-circuited devices. In fact, they have a greatly increased reverse leakage current with almost linear (ohmic) J-V characteristics, like if electrically shorted. In addition, the forward conduction is improved as no barrier to the low doped silicon exists anymore because it is assumed that the top metallization diffused through GC and the low doped epi-Si.

A closer look on the damage pattern of the surface of the top metallization of failed C-Si diodes reveals a different appearance depending on the pulse length used, as shown in the SEM analysis in Fig. 5.9. All the devices where stressed with the same current level of 3.5 MA/cm^2. The damage to the top metallization is hardly visible even after 548 million events at pulse width of 100 ns. The temperature in the copper during such a short pulse was not yet high enough to cause a reasonable thermomechanical deformation after each pulse and finally, only a small bump arised

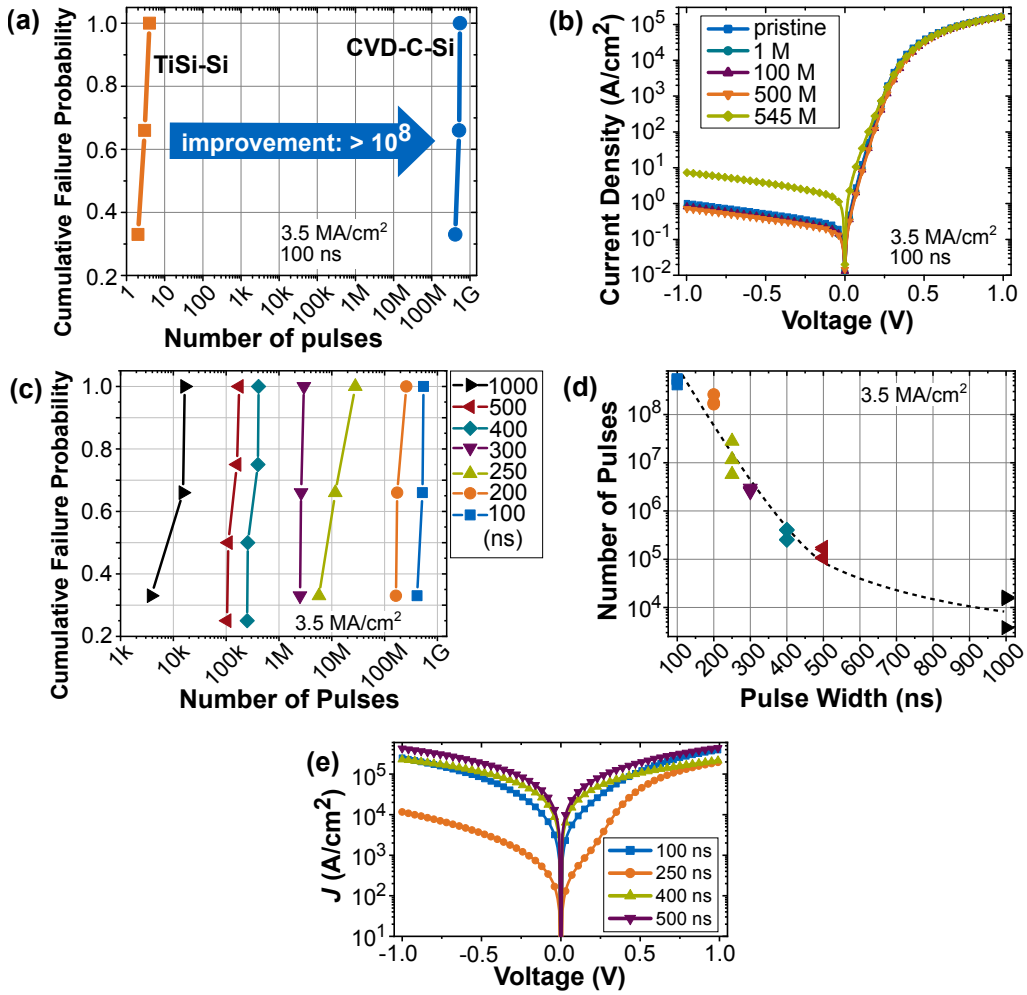

Figure 5.8: (a) Comparison of the stress pulse endurance of TiSi-Si (BAT15) and CVD-C-Si diodes with 28 nm thick carbon for a current density of 3.5 MA/cm^2 and a pulse width of 100 ns. The majority of the TiSi diodes were deteriorated below four pulses whereas the C-Si diodes could withstand more than 100 million pulses before they failed. The J-V curves in (b) show the change in the dc characteristics of a C-Si diode after several million current pulses were applied. The electrical behavior was almost not affected after up to 10^8 pulses. Only the SBH became slightly higher by about 0.01 eV, which led to a lower reverse current. The onset of a degradation after 545 M pulses is visible as an increased leakage current. Image (c) shows the failure probability as a function of the number of pulses at different pulse lengths for CVD-C-Si diodes with 28 nm thick GC. At least three devices were stressed with a given pulse current density of 3.5 MA/cm^2 and a duty cycle ≤ 0.0005. (d) shows the number of pulses the individual diodes could withstand as a function of the pulse width. (e) shows J-V characteristics of C-Si diodes after they reached the threshold for a failed diode. They are short-circuited and do not show a rectifying behavior anymore. For a pulse width below 300 ns the condition of the diode was checked at most every 50 000 pulses while at a higher pulse length the integrity was checked every 1000 pulses or even less. Consequently, many stress events may still have taken place before the J-V curves were recorded. Adapted from Ref. [MS17].

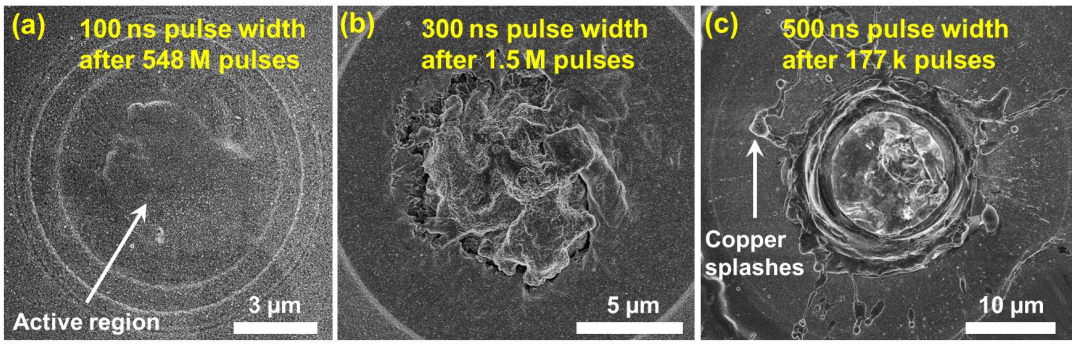

Figure 5.9: SEM image of the top view of failed CVD-C-Si diodes with a Ti/Cu/Au top metallization. All the devices where stressed at the same average pulse current density of 3.5 MA/cm^2 while only the pulse width was altered. In (a) is a diode after 548 million pulses (100 ns pulse length) shown where almost no damage in the top metallization is visible. The device in (b) demonstrates the damage after 1.5 million pulses (300 ns long), where the metal even started to melt and piled up. The temperature during the 500 ns long pulses rose in the copper of the diode shown in (c) to such an extent that some kind of volcano was created as molten copper was spit on the periphery and a circular crater was formed. Taken with permission from Ref. [MS17] © 2017 IEEE.

on the surface. For a longer pulse length was the copper heated to a point where it could have started to melt (1085 °C). This is in agreement with FEM simulations and caused a pile-up of the surface metal (Fig. 5.9(b)). As shown in Fig. 5.9(c), the temperature at 500 ns long pulses was so high that the metallization started to create a 'volcano' and Cu splashes were spit on the periphery of the substrate. Nevertheless, the C-Si contact could withstand up to 177 000 pulses before it fails, although the temperature at the interface must have been much higher. This underlines the excellent temperature stability of the graphenic carbon-silicon contact.

The reliability of CVD-C-Si contacts, where the substrate was heated in H_2 for 5 min, was investigated with the same test parameters (3.5 MA/cm^2, 100 ns). The carbon thickness was 37 nm and as discussed in the previous chapter, these samples yielded a very low barrier height of 0.41 eV. As shown in Fig. 5.10, the diode gradually obtained a smaller SBH (higher reverse current) and reached after one million pulses a value of 0.36 eV. This is in clear contrast to samples considered so far, where the pulses led to an increase of the barrier height (see Fig. 5.7 and 5.8). It could be related to some different interface reaction mechanism. After a total of ten million pulses, the SBH did not became smaller anymore — instead it started to increase. Stunningly, the diode could endure a total of four billion pulses and outperformed previous test results. The diode was still fully functional and only showed up an increase of R_s by 0.3 µΩ cm^2. A reason for the superior reliability might be the higher GC thickness of 37 nm compared to 28 nm from previously tested devices. The thicker carbon acts as a better diffusion barrier for the top metallization and the higher series resistance might be responsible for a more homogeneous heat

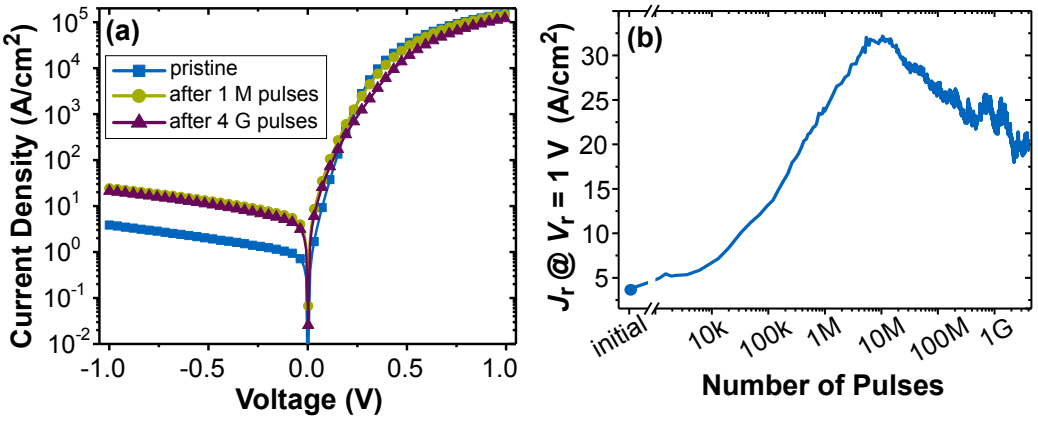

Figure 5.10: The J-V curves in (a) show the change in the dc-characteristics of a 37 nm CVD-C-Si diode (C_2H_4 as precursor gas, heated in H_2) after one million and four billion current pulses (3.5 MA/cm^2, 100 ns) were applied. The forward conduction decreased slightly with increasing number of pulses but the SBH became lower, which led to a higher reverse current. (b) shows that the reverse current density J_r at a reverse voltage V_r of 1 V increased first when up to ten million pulses were applied. Afterwards, the reverse current started to decrease almost constantly but the initial value was not reached after 4 billion pulses. A temporary fluctuations in the current are associated with an initial burn-in behavior, mechanical vibrations at the setup and a change in the room temperature during day and night as the test took about 32 days.

distribution in the junction. Furthermore, the carbon had a lower surface roughness, which could prevent an electrical field enhancement and consequently less localized stress spots with higher power density were present. The test was here only aborted due to the excessive testing time. Additional four samples were tested, not up to such high values, but one of them could endure one billion events without failure whereas others were stopped earlier. Tests with a longer pulse duration were not investigated for this type of diode.

The current density in a real world ESD event is not limited to 3.5 MA/cm^2 and can reach much higher values. This was evaluated here with the TLP setup at a pulse width of 100 ns. However, this setup produces pulses with a very short rise time, which negatively influences the probability of failure. To allow a better comparison to the previously used setup, the rise time of the pulse was set to 15 ns by a simple air core coil with about 400 nH, which was installed after the diode.

A typical waveform of a current pulse through a C-Si diode, here with an average current density of 9.3 MA/cm^2, is shown in Fig. 5.11(a). This was identified as the maximum applicable value for a CVD-C-Si diode with a carbon thickness of 58 nm. It is an increase of J by a factor of 2.66 compared to previous endurance tests. The power density, which is mainly responsible for possible damage to the device, is as a consequence increased by a factor of 7.1 as the current density has a squared dependency (see Eq. 1.4). Fig. 5.11(b) shows that the C-Si diode could withstand a

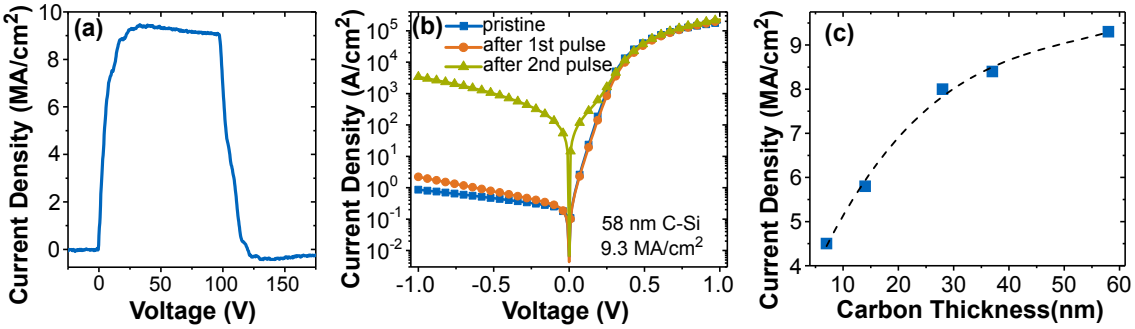

Figure 5.11: (a) shows a current pulse of the TLP setup, which was measured with the CT1 current coil at the cathode side of a C-Si diode. An additional 400 nH air-core coil was installed in the current return path after the diode to act as rise time filter (the rise time is 15 ns). The average amplitude height is 9.3 MA/cm^2. (b) J-V curves of a tested CVD-C-Si diode with a GC thickness of 58 nm. After a single pulse (100 ns long), the diode was still fully functional. The reverse behavior was slightly degraded but still close to the pristine curve. Only the second pulse was destructive. In (c) is the threshold current density value for a failure as function of the carbon thickness shown. Only very limited data is available but the diodes could withstand one pulse at the given J.

single pulse at this stress level wheras SBH, series resistance and ideality factor are hardly affected by the overstress. Only a slightly higher reverse current, as the slope changed, was observed — but the diode still fulfilled the BAT15 specifications. Only the second pulse was destructive to the interface and the diode completely failed as indicated by the about 500-times higher reverse leakage.

CVD-C-Si diodes — not necessary produced by the same setup or procedure — with thinner carbon films were also tested at a higher current density level. As can be seen in Fig. 5.11(c), the lower the GC thickness, the lower is the threshold current density for a failure. The test devices had the same electrical behavior as before. The first pulse was not yet destructive at the indicated value, but the second one was. It becomes obvious that a thicker carbon film acts as a better diffusion barrier for the top metallization, but the threshold value seems to saturate for even thicker GC. A reason might be the high dissipated power and the resulting Joule heating, which can cause a strong destruction of the Si substrate or force the diffusion through GC.

5.3.3 Overview of the Pulse Endurance of CVD-C-Si Diodes

Many CVD-C-Si diodes were fabricated but not all of them were tested with regard to their reliability or simply did not fulfill this property. The diodes, which showed an outstanding performance against high current density pulses (3.5 MA/cm^2, 100 ns), are summarized in Tab. 5.1. Nevertheless, other diodes also showed good results, but they were most often only tested up to one million pulses due the required excessive testing time and therefore, they are not further mentioned here. The reliability of diodes with thinner carbon was not fully evaluated. However, several tests with a film thickness < 25 nm did not show promising results in their pulse endurance and

failed below 10 000 stress events. But this could as well have been associated with some problems in the cleaning steps of the substrate.

Table 5.1: Summary of the pulse endurance (3.5 MA/cm^2, 100 ns) of tested CVD-C-Si. The carbon films were deposited by different setups and procedures.

Gas	Thickness	No. of tested diodes	No. of pulses	Remarks
C_2H_2	58 nm	10	1 M to 100 M	Test aborted; diodes did not fail
C_2H_4	37 nm	5	4 M to 4 G	Test aborted; diodes did not fail; heated in H_2
C_2H_4	28 nm	3	420 M to 548 M	Diodes failed; heated in C_2H_4

5.4 Reliability of Sputtered Carbon-Silicon Diodes

For the investigation of the reliability of sputtered carbon, only films deposited at 400 °C were considered as they are expected to have a less porous surface.

5.4.1 Preparation of the Setup

As previously discussed in section 3.3, it is important that all parts near the sputtering source and especially the shutter are well coated with carbon. In first experiments, the shutter was not well coated with carbon as the films adhered very poorly on the polished metal surface and a resputtering of the shutter material in this low pressure range is very likely. Far-reaching plasma interactions with a badly coated shutter, even for a very short time, might be sufficient to deposit metal contaminations onto the silicon active region or in the carbon film.

These trace amounts of metal can easily diffuse into the epi-layer only after a few 100 pulses and act as unwanted recombination centers. Fig. 5.12(a) shows a stressed SC-diode (35 nm thick carbon) which has a deteriorated behavior with strongly increased reverse current but hardly affected series resistance. After a continued stressing of the contact with pulses, two different scenarios are feasible. At first, the contaminations can diffuse further during the reliability test and form a local weak spot, which promotes the formation of a filamentary current. This in turn can create a short-circuit and consequently a failure. Second, the ions at the junction might react with silicon and become inactive or they diffuse into the highly doped substrate before a more severe failure can occur. As a consequence, the recombination centers would disappear again, which can be seen in the J-V curves in Fig. 5.12(a) after several million pulses.

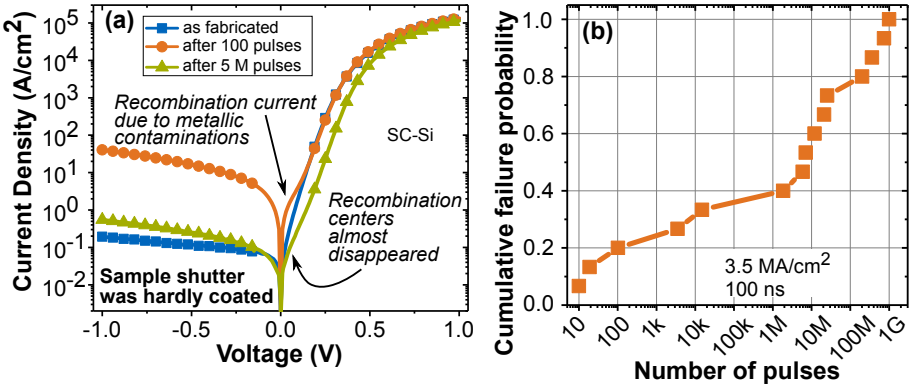

Figure 5.12: (a) shows J-V curves of SC-Si diodes were the shutter was not well coated with carbon and recombination currents become visible after a few hundred high current pulses (3.5 MA/cm^2, 100 ns). Depending on the degree of contamination, they can cause a short-circuit over time or they almost vanish again. Initially, the pulse endurance reliability had a wide distribution as indicated in (b). Only after a carbon coating of all sides of the shutter and all components in the proximity to the plasma, the contact is able to withstand up to one billion pulse events. Adapted from Ref. [MS19].

The failure probability of tested samples was distributed over a wide range of pulses. For badly carbon coated equipment, the diodes can even fail after ten pulses whereas an SC-diode can even withstand up to one billion pulses in better prepared setup, as shown in Fig. 5.12(b).

A precoating of the sputter equipment with carbon is essential, but even then an SC-Si contact typically showed an undesired increased reverse leakage current after a few pulses. Some of these diodes easily outperformed the stability of TiSi-Si and CVD-C-Si. Nevertheless, the reliability results were fluctuating on the same sample over a wider range. Possibly, poorly bonded C atoms act as additional recombination centers and were responsible for an early failure. However, these type of interface was not evaluated any further due to the uncertainty in the reliability of the SC-Si contact.

5.4.2 Reliability Boost of Sputtered Carbon by Nitrogen-Doping

The investigation of a diode with 35 nm thick nitrogen-doped carbon (CN) showed after a precoating of the whole sputter equipment J-V characteristics free of a recombination current, as illustrated in Fig. 5.13(a). Furthermore, a constant increase of $q\phi_B$ was observed during the stress tests. As a consequence, the contacts got even better blocking capabilities with reduced leakage current after one billion pulses (see Fig. 5.13(b)). The breakdown behavior did not deteriorate after so many pulses even they cause very high temperatures. This reveals that there was neither a diffusion of the interface metal nor of dopants from the highly doped substrate into the thin epi-layer, which could cause a filamentary current. A reason might be the high positive electrical field during the pulse at the junction of the diode. This could repel

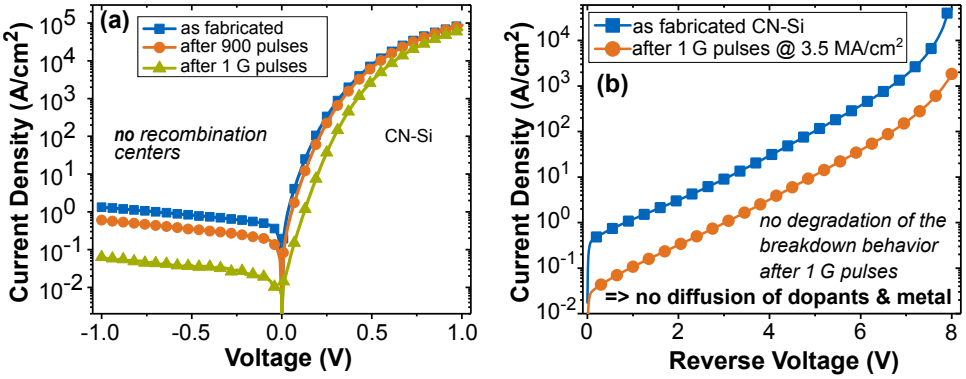

Figure 5.13: (a) illustrates J-V curves of an as-fabricated CN-Si diodes, which was stressed with pulses of $J = 3.5\,\mathrm{MA/cm^2}$ at a pulse width of 100 ns. The characteristics do not show a recombination current after 900 pulses, only a slightly higher SBH. The barrier continuously increased from 0.42 eV to 0.52 eV after one billion pulses due to interface reactions. (b) shows the reverse dc characteristics of the CN-Si diode as fabricated and after 1G pulses. The reverse blocking capability was improved as the SBH has increased and the onset of the reverse breakdown is not shifted to lower voltage. Adapted from Ref. [MS19].

positively charged donor ions and prevent them from diffusing into the epi-layer.

The change in the SBH might be similar to the findings that it can be altered by dc bias, as discussed in section 4.3. Here, the change is triggered at the CN-Si interface due to the high current density or the electrical field of the pulse. A reverse voltage of 7.5 V for about 1 min was sufficient to recover the SBH to the as-fabricated or an even lower value. This indicates that temperatures close to the melting point of silicon during billion of such ESD-like pulses did not lead to a permanent change of the CN-Si interface and just created a dipole.

Diodes with 35 nm of sputtered nitrogen-doped carbon showed in a benchmark of the failure probability with TiSi-Si and CVD-C-Si outstanding results, as highlighted in Fig. 5.14. The CN-Si diode outperformed the stability of the TiSi-Si contact at a current density of $3.5\,\mathrm{MA/cm^2}$ (100 ns) at least by a factor of one billion. The number of pulses were quite high and ranged from about 1.5 billion to 6.1 billion. But these values are just lower bounds as the devices did not fail the reliability tests. The diodes are still fully functional and only the SBH has increased after 6.1 billion pulses to ~ 0.55 eV, which is an increase of $\sim 30\,\%$. The tests were just aborted due to the excessive testing time of about four months for the four evaluated samples here. The test duration and thus the time between the individual pulses could not be reduced arbitrarily because the DUT needs a certain time to cool down to room temperature.

CN does not just exceed the reliability compared to TiSi on Si but also that compared to CVD-C deposited at 1000 °C by at least a factor of three (see Fig. 5.14(b)). These results underline, that the sputtered nitrogen-doped carbon is in its structure dense enough to act as an excellent diffusion barrier for metal. The reason for the

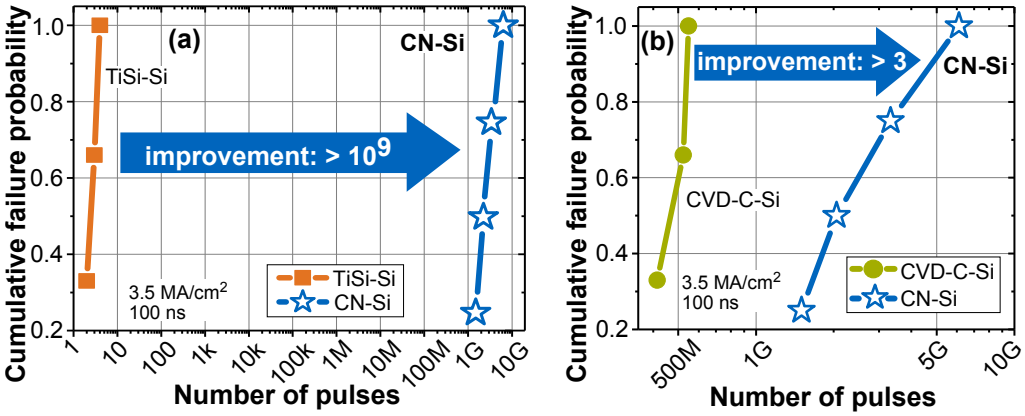

Figure 5.14: Pulse endurance comparison CN-Si with TiSi-Si (BAT15) and CVD-C-Si diodes for a current density of 3.5 MA/cm^2 and a pulse width of 100 ns. The CN-Si diodes can withstand at least over 1 billion pulses (at least nine orders of magnitude) more than the TiSi-Si diodes, as illustrated in (a). The CN-Si values are only lower bounds as the tests of the CN-Si contact have been aborted due to the excessive testing time. The diodes did not fail and were still fully functional. (b) shows that CN-Si (35 nm of CN) endures three times more pulses than the CVD-C-Si with 28 nm thick carbon. The duty cycle was always < 0.00015. Taken from Ref. [MS19]

enhanced reliability compared to the CVD-C-Si contact might be associated with the slightly higher thickness of 35 nm, which act as a better diffusion barrier than the 28 nm of CVD-C. In addition, the CN film has a higher electrical resistivity. According to results from FEM simulations presented in section 5.1, a higher resistivity and thickness of the interface metal leads to a more homogeneous heat distribution and a lower maximum temperature in the active region during the current pulse, which reduces the probability of degradation. But it should be mentioned, that also a CVD-C-Si diode with 37 nm thick carbon could withstand four billion pulses without a failure. At such a thickness range, the reliability seem to be similar independently of the deposition method.

Since the current density cannot be further increased with the used pulser, the pulse width was raised to 300 ns and 500 ns at the same current density of 3.5 MA/cm^2 to force an earlier failure of the diodes. An increase from 100 ns to 300 ns or 500 ns corresponds to a three-fold or five-fold larger applied energy. Fig. 5.15(a) illustrates that CN-Si is not as reliable as CVD-C-Si for longer pulse durations. The pulse endurance for 300 ns long pulses was between 150 000 and 500 000 and therefore, only one-tenth of the CVD-C-Si diodes. The deviation to CVD-C-Si contact became larger for pulses with a width of 500 ns but the contact could withstand at least 250 events. Nevertheless, the reliability is still superior to TiSi-Si, which was tested with 100 ns long pulses and failed after 2–4 stress events. Also, a much lower duty cycle of about 10^{-6} did not lead to any change in the pulse endurance. But Fig. 5.15(b) illustrates, that a degradation did not occur continuously. The highlighted diode

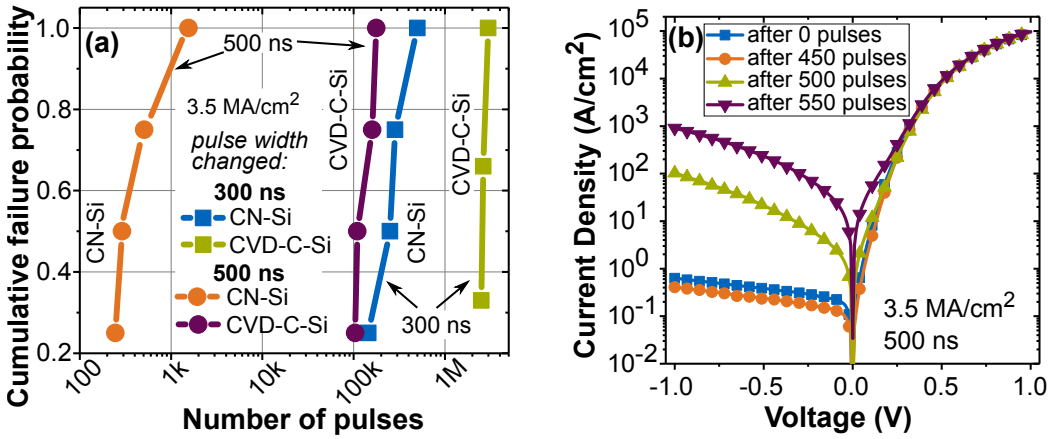

Figure 5.15: (a) shows the failure probability of CN-Si (35 nm thick C) and CVD-C-Si diodes (28 nm thick C) for a pulse width of 300 ns and 500 ns. The duty cycle was < 0.0001. In contrast to the reliability behavior at 100 ns long pulses, the CN-Si diodes failed at longer pulse durations earlier than CVD-C-Si diodes. The J-V curves in (b) show the degradation behavior in the dc characteristics of a CN-Si diode after several 100 current pulses (3.5 MA/cm^2, 500 ns) were applied. The electrical performance was hardly affected after up to 450 pulses, only the SBH was slightly increased. After 500 pulses, the diode showed a first deterioration with a strong increase in the reverse leakage and failed after additional 50 pulses. Taken from Ref. [MS19].

showed after 450 pulses almost no change in dc characteristics and was still fully functional. The pulses only caused a slight shift of the SBH to a higher value and consequently a lower reverse current. The next J-V curve was measured after 50 more pulses were applied. As can be seen, a degradation of the device took place as visible in the higher leakage current. Finally, the diode failed after a total of 550 pulses.

The reason for the reduced reliability compared to CVD-C is assumed to be the higher resistance of the contact and the CN film itself. As a result, the total temperature in the active region might be higher and also the temperature in the top metallization rises faster, according to FEM simulations. This can produce a stronger thermomechanical deformation of the copper and consequently a change in the current flow which in turn could enforce an earlier failure.

The impact of an altered pulse width on the top metallization of a diode after being stressed was analyzed with a scanning electron microscope (see Fig. 5.16(a)-(c)) and a confocal laser scanning microscope (see Fig. 5.16(d)-(f)). The temperature in the metallization does not seem to be so high during a 100 ns pulse to cause significant damage even after 1.7 billion pulses. The thermomechanical stress during each pulse only caused a slight pile-up of the metal. Nevertheless, the true color image shows a color change to a more blueish or rainbow-like appearance, which might indicate an oxidized surface even through the 50 nm gold capping layer. During a 300 ns long pulse, in contrast, the temperature in the metallization gets much

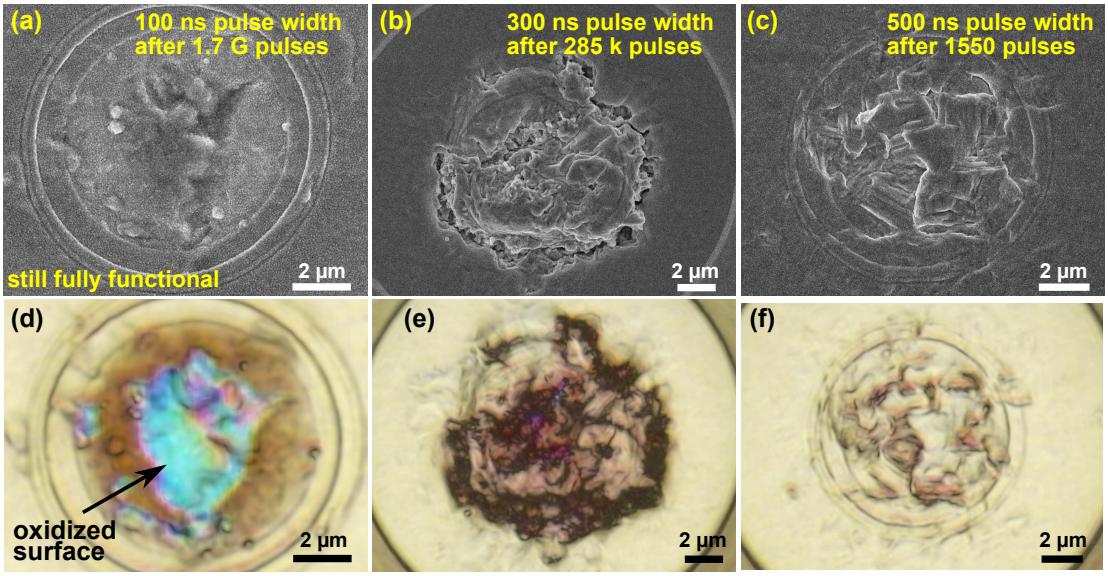

Figure 5.16: Images (a)-(c) are recorded by an SEM whereby (d)-(f) show the same CN-Si diodes in a top view with Ti/Cu/Au as metallization with true color microscope images. All the devices where stressed at a current level of 3.5 MA/cm^2 while only the pulse width was altered. The diode shown in (a) and (d) is after 1.7 billion pulses at a width of 100 ns still fully functional. Almost no damage in the top metallization is visible but the change in the color indicates most likely that the temperature on the surface was high enough to oxidize the Cu even through the Au capping during the two weeks of testing. The micrographs in (b) and (e) demonstrate the damage after 285 thousand 300 ns long pulses where the metal even started to melt because cracks and a pile-up are visible. The change in color is despite the strong damage quite low. (c) and (f) show the surface of a failed diode where the current-induced damage of 500 ns long pulses just slightly melted the surface as the total number of stress events (1550) was lower. Taken from Ref. [MS19].

higher. The thermomechanical forces caused after 285 000 pulses a cracked and piled up metal. Consequently, the CN-Si interface shows excellent temperature stability, as the temperature at the junction must have been much higher than in the top metallization. However, the metal surface showed less damage at a pulse length of 500 ns, possibly due to the lower number (1550) of pulses before the diode failed.

5.4.3 Scalability of Nitrogen-Doped Carbon down to 0.7 nm

The 35 nm thick CN films considered so far were relatively thick compared to the dimensions of aggressively scaled devices. As discussed in section 1.2, the contact critical dimensions are already below 20 nm and might even approach 10 nm. This in turn means that the narrow contact holes with high aspect ratio are very difficult to be coated with a metal by a PVD process. It might practically impossible to deposit carbon in the thickness range discussed before. In order to make CN a suitable candidate for a usage in aggressively scaled CMOS, the thickness of the carbon

must be significantly reduced.

CVD-C-Si contacts showed a strongly limited robustness against the high current density pulses at a GC film thickness of less than 25 nm. In contrast, CN-Si diodes with a much thinner carbon still have an excellent stability against such pulses, as highlighted in Fig. 5.17. Devices with a 5 nm thick CN film are superior to TiSi-Si by a factor of over 100 million and could withstand up to 1.28 billion pulses before they failed. Furthermore, the contact has still a better reliability than the previously discussed 28 nm CVD-C-Si diode. Nevertheless, this might still be too thick for the prevailing dimensions in modern devices and to prevent the resistance of the contact plug from skyrocketing, the thickness of the high-ohmic carbon must be reduced even further.

A film thickness of 5 nm was not yet the limit because even 0.7 nm thick CN still provides an excellent diffusion barrier for top metallization. The thickness was evaluated at steps with an AFM and was measured at different locations on the sample to be in average between 0.6 nm and 0.8 nm — the total average thickness was therefore set to 0.7 nm. This would be equivalent to only 2-3 layers of graphene, but still such a contact can survive up to 440 million ESD-like pulses, which easily beats TiSi. However, there might be regions in film were the layer is even thinner — even down to a single atom layers as the film is not perfectly smooth — but this seems still enough to hinder Ti or Cu from the diffusion during the pulses into silicon. In the worst case, the contact could still endure 14 million stress pulses.

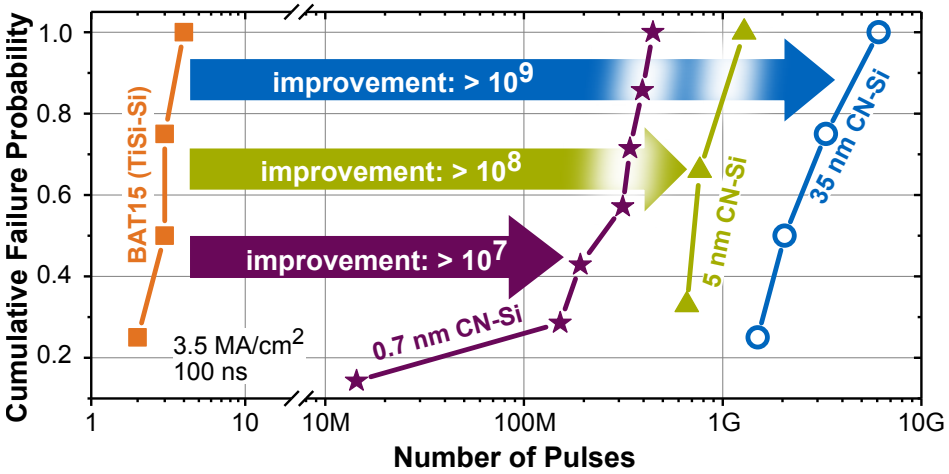

Figure 5.17: Pulse endurance comparison of TiSi-Si (BAT15) with CN-Si diodes of different CN thicknesses. All devices were tested under the same test conditions at a pulse width of 100 ns and $J = 3.5\,\mathrm{MA/cm^2}$. Samples with a 35 nm thick CN did not fail the test whereas diodes with thinner carbon failed. The 5 nm CN-Si showed a wear-out between 660 million and 1.28 billion pulses. A much thinner carbon film of only 0.7 nm showed still excellent diffusion barrier properties. The corresponding diode could withstand over 10 million more pulses more than the TiSi-Si diodes and failed between 14 million and 440 million pulses.

However, the majority of the testes devices could withstand over 100 million events.

It gets overall quite obvious from Fig. 5.17 that the quality as a diffusion barrier becomes 'weaker' with decreasing thickness because the number of applicable pulses scale with the carbon thickness. However, the results are remarkable for very thin films and one could conclude from this that even a thinner film — down to one atom layer — could be sufficient to obtain the desired reliability properties.

5.4.4 Overview of the Pulse Endurance of SC-Si and CN-Si Diodes

Not as many diodes with sputtered carbon (CN-Si and SC-Si) as from the CVD process were fabricated but even the few tested showed outstanding results. The diodes, which had an excellent stability against high current density pulses, are summarized in Tab. 5.2.

Table 5.2: Summary of the pulse endurance (3.5 MA/cm^2, 100 ns) of tested diodes for different types of sputtered carbon and varied thickness. All films were deposited at a substrate temperature of 400 °C. The ratio of Ar/N_2 for CN was always 56. The reliability of SC diodes cannot be specified accurately, since this was mainly used for the preparation of the setup.

Type	Thickness	No. of tested diodes	No. of pulses	Remarks
SC	35 nm	> 1	< 1 G	Used to prepare the setup
CN	35 nm	4	1.5 G to 6.1 G	Diodes did not fail
CN	5 nm	3	660 M to 1.28 G	—
CN	0.7 nm	7	14 M to 440 M	—

6 Summary and Outlook

This thesis demonstrated the successful deposition of graphenic carbon (GC) as electrical contact material to silicon as alternative to the widely used titanium silicide (TiSi). GC was identified as an attractive alternative due to its chemical and physical properties. Two different kinds of methods have been developed for the direct deposition of graphenic carbon on silicon. The films were synthesized by chemical vapor deposition (CVD) at temperatures between 850 °C and 1000 °C and by a sputter process at temperatures between 100 °C and 400 °C. These films formed the same low or even lower Schottky barrier height to n-type silicon as TiSi and adhered not only very well to Si but also to SiO_2, SiN and Ti. Moreover, the GC-Si contact showed a superior reliability, independent of the deposition method, and exceeded the robustness against high current density pulses by a factor of several million compared to a TiSi-Si contact. Finite element method simulations and investigations of the metal surface revealed that the temperatures during such an event can get quite high due to Joule heating. This in turn can lead to interdiffusion of the metal-semiconductor contact and finally to degradation or failure of the device.

A change in the CVD process conditions of the GC deposition could be used to alter the barrier height to even lower values, which would be very attractive for low contact resistance contacts. However, the high temperatures during the CVD process are not fully compatible with the temperature restrictions in modern CMOS devices. Nevertheless, this does not pose a problem for high-power switching devices, as the allowed temperature budget is higher there. The elevated temperature during the graphenic carbon deposition can even be used for dopant activation, which could save an additional process step. If a lower conductivity of carbon is required, a future work could dope GC with foreign atoms (e.g. P, B or N) to modify the electrical properties, which can also have an influence on the barrier height to silicon. The conformal step coverage of GC produced by CVD and the good diffusion barrier properties render it not just suitable as metal-silicon contact but also as a gate material because it aligns mid-gap to silicon. The conformal coverage of CVD-C is also very attractive for devices with trenches, which need to be contacted electrically. The good diffusion barrier properties are furthermore required at the liners/barriers for interconnects.

A drop in reliability has been observed for CVD-carbon film thicknesses below 25 nm, which is an obstacle for aggressively scaled devices. However, this was not further investigated and could also be related to the clean room infrastructure used. It was very difficult to ensure a consistently high level of cleanliness in a university

environment, which is the prerequisite for the carbon-silicon contact to withstand a high number of high current pulses. Only a small amount of unwanted atoms or ions at the junction region can be responsible for an early failure, especially if a high-temperature step follows.

In contrast to the CVD method, GC can also be produced in a sputtering process at much lower temperatures, which are also compatible with modern CMOS processes. The method is well established in the industry and it has been shown that the carbon film can be doped with nitrogen by simply adding nitrogen to the sputter gas. This improved not only the electrical conductivity, but also the stability against pulses with high current density. The reliability exceeds that of TiSi-Si by far and also shows better results than carbon from the CVD process. Probably the most important point, however, is that scaling is possible here and a contact with 0.7 nm thick carbon (about 2–3 graphitic atom layers) still has an extremely high pulse endurance. The attractivity of the material to achieve ohmic contacts is further increased by the fact that the incorporated nitrogen results in a lower barrier height on silicon.

Unfortunately, the nitrogen-doping leads to a deterioration of other electrical properties of the diode (series resistance, ideality factor) compared to an undoped carbon. The impact of the amount of incorporated nitrogen into the carbon need to be further investigated as a high reliability at good conduction properties is essential. To achieve this, the features of undoped and doped sputtered carbon could be combined in a future work. One atomic layer of the former could determine the contact properties while several atomic layers of the latter would provide the high reliability.

Graphene is also often proposed as a transparent and conductive electrode for photodetector applications with ultraviolet light. In this case, GC would also be a very attractive alternative, as it also has a certain transparency, a high durability and, if necessary, the band gap could also be slightly modified.

Commercially produced Schottky diodes usually use a guard ring structure to suppress high electric fields at the edges. Unfortunately, this increases the junction capacitance, which affects the signal integrity especially in high frequency applications. Since GC is chemically very inert, does not form silicides and does not react with dopant atoms, it can be used as an etch mask to produce a diode with mesa structure without a guard ring. A first work on this topic demonstrated the feasibility [AF19] and would enable very reliable devices with low capacitance.

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