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Design of a 9-50 GHz CMOS Integrated Readout Circuitry for Spin Wave Characterization

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Abstract

Most Complementary Metal-Oxide-Semiconductor (CMOS) based circuits consume very high-power at microwave frequencies. Emerging Spin Wave (SW) based devices may offer an alternative to CMOS in certain high-speed signal processing applications, e.g. the computation of the Fourier transform. SW devices inherently operate at frequencies in the range of tens GHz and carry very low energy. It makes the SW devices potentially energy efficient, but the challenge of an effective SW detection remains. Current SW detectors require Brillouin Light Scattering (BLS) equipment or external network analyzers connected to wave guides, but an on-chip SW characterization is still missing. However, it is needed for production ready applications.

Here, it is assumed that SWs will be detected using an on-chip loop antenna located below a thin, insulating magnetic Yttrium-Iron-Garnet (YIG) film. Micromagnetic simulations indicate that a near field loop antenna with an area of $1\,\mu m^2$ could recover a signal power of -80 to $-90\,\mathrm{dBm}$.

Starting with the model of an on-chip loop antenna as a sensing element for SWs, the readout circuitry is designed and simulated using 40 nm CMOS technology. This is done in order to characterize the detected SWs in regards to their frequency, amplitude and phase. The readout system covers operating frequencies of $9-50\,\mathrm{GHz}$ with a SW detection resolution of better than 20 MHz. The analysis shows that a signal power of less than $-90\,\mathrm{dBm}$, induced in the transducer, can be detected. The measurement resolution of the induced voltage in the antenna is below $2.5\,\mu V$. For the phase shift measurement, the deviation from an ideal curve is expected to be below 37.8°. The estimated power consumption of the readout circuitry ranges from 50 mW to 70 mW, depending on the operating frequency.

The presented readout circuitry is highly suitable for on-chip SW characterization and offers an integrated alternative to currently used SW detecting systems. Moreover, this readout system can be modified for other inductive sensing elements, such as microstrip lines or coplanar waveguides. A modification of the readout system for the Direct Current (DC) readout of the combined Spin Pumping (SP) Inverse Spin Hall Effect (ISHE) is also feasible.

Contents

Chapter 1

Introduction

Today, CMOS is the leading technology used in Integrated Circuits (ICs). The tremendous progress in downscaling CMOS technology nodes over the past few decades has enabled the development of new products, like smartphones or home automation systems, that were inconceivable $20 - 30$ years ago. Such innovative products have radically transformed both our society and the way we live, commute and communicate.

The leading companies in the semiconductor industry have already started with the production of the 7 nm node technology and $3 - 5$ nm nodes are expected to be production ready in the next 3 years [2, 3], providing even more computation power per unit area. However, such advanced technology nodes mean enormous costs for research and development. Moreover, the design costs (e.g. qualification, physical and software design, verification, prototype, validation) for advanced technology chips are rising as well [1]. Figure 1.1 shows the rising design costs of the advanced

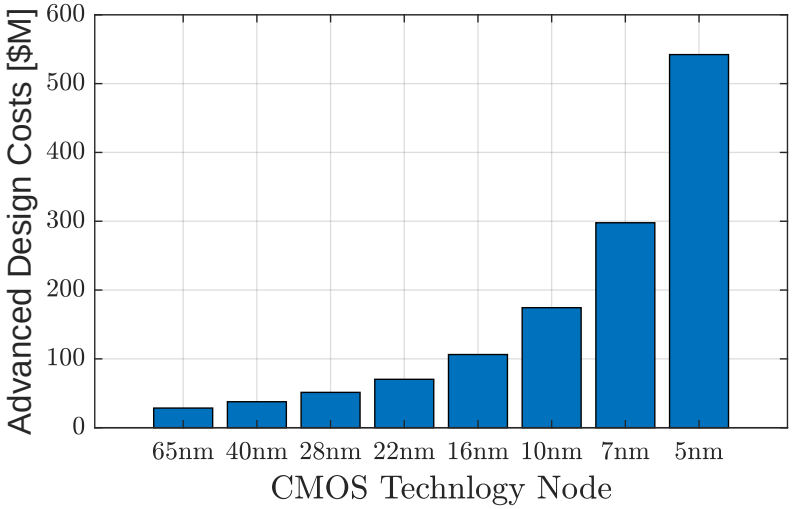

Figure 1.1: Rising design costs for the advanced technology nodes. Costs include Intellectual Property (IP) qualification, architecture, verification, physical and software design, prototype, validation. [1]

nodes, as a consequence the number of companies going to use these advanced technologies is limited. Hence, GlobalFoundries, one of the leading semiconductor companies, recently announced that they are ceasing from the production of the 7 nm technology due to high costs [4].

Experts also see a twilight of the Moors Law in the CMOS technology. Downscaling the size of transistors is becoming challenging due to quantum effects [5]. However, this does not mean the end of progress. Alternatives, like the Tunneling Field Effect Transistor (TFET), Nanomagnetic Logic (NML), SW devices and the recently introduced Magnetoelectric Spin-Orbit (MESO) devices [6], are considered as extension of the CMOS technology or even going beyond with promising performance in low power applications [5, 7]. Considering delays and energy per Arithmetic Logic Unit (ALU) operation, there are only few devices, such as TFETs, that could outperform CMOS in traditional Boolean computing [8], postulated by Shannon [9]. SW devices provide a possibility to execute both Boolean and non-Boolean computations. However, the experts see potential in SW devices especially for non traditional wave based computing, similar to optical computing [10], as they could perform more efficiently at image and video processing tasks [11, 12].

The general idea of SW devices (see Figure 1.2) is: (1) convert a charge current into a magnon current, in order to process the information in a magnonic domain and (2) convert back the SW signal into the electronic domain for post processing [13]. Transistors, as a key element in today's ICs, are also feasible in magnonics and could play a significant role for signal processing in emerging magnonic systems. In [14]

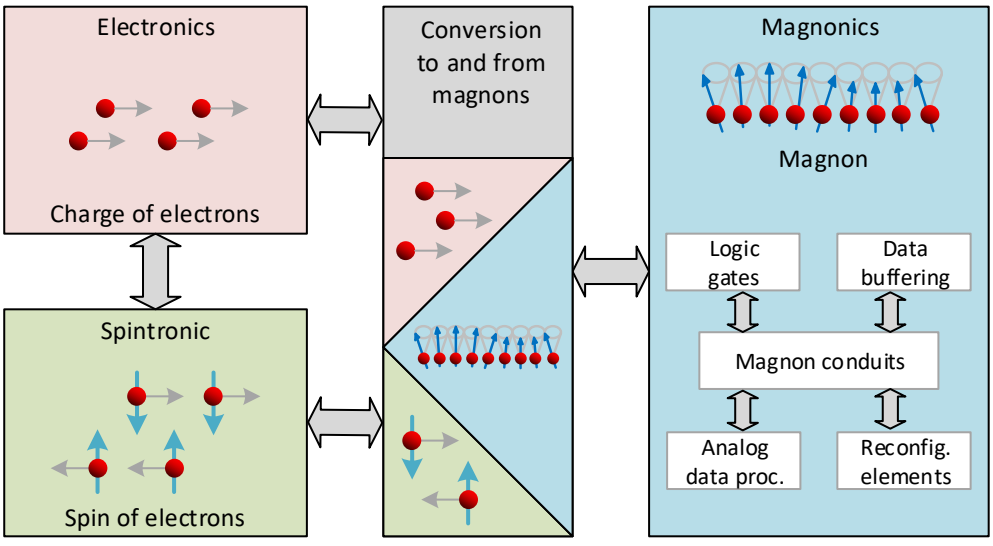

Figure 1.2: Schematical overview of the conversion between electronics, spintronics and magnonics with charge of electrons, spin of electrons and magnon, accordingly, as quanta for information processing. The electronic domain is used to control transducers converting the signal into the magnonic domain, where information is processed in an energy efficient way and is finally converted back into the electronic domain. Figure is adopted from [13, Figure 1].

Chumak describes the operational principle and physical mechanisms of a magnon transistor based on the four-magnon scattering mechanism. The theory and a prototype of the magnon transistor as a switch, based on SW interference, are published by Balynsky in [15, 16]. A majority gate, as another component in the magnonic system, is also experimentally proven [17–20]. From theoretical point of view Csaba and Papp show a SW device for computing Fourier transform, that could consume much less power than modern Central Processing Unit (CPU) performing the same Fourier transform operations [12, 21]. Similar to the Fourier transform calculation in optics, a magnetic lens can be used to manipulate propagating SWs [22].

The main advantage of spintronics, as compared to conventional electronics, is the energy efficiency due to the absence of an electrical current and the corresponding producing Joule heating. For signal processing the coupling between electron spins is used instead of electron transport, as a consequence no additional electromigration. [13, 23]

Besides, fast and power efficient data processing is made possible by the operation frequency of SW devices in a GHz to THz range at room temperature [24, 25]. It could play a significant role in analyzing huge amounts of data in a very short time in future applications such as autonomous driving or content searching and pattern recognition in video files.

One of the first SW related papers was published in 1963 by Schlömann, who investigated the conversion of electromagnetic power into SW power from a theoretical point of view [26]. Today, magnonics has become one of the most intense research areas worldwide as it is seen as a candidate for going beyond CMOS technology.

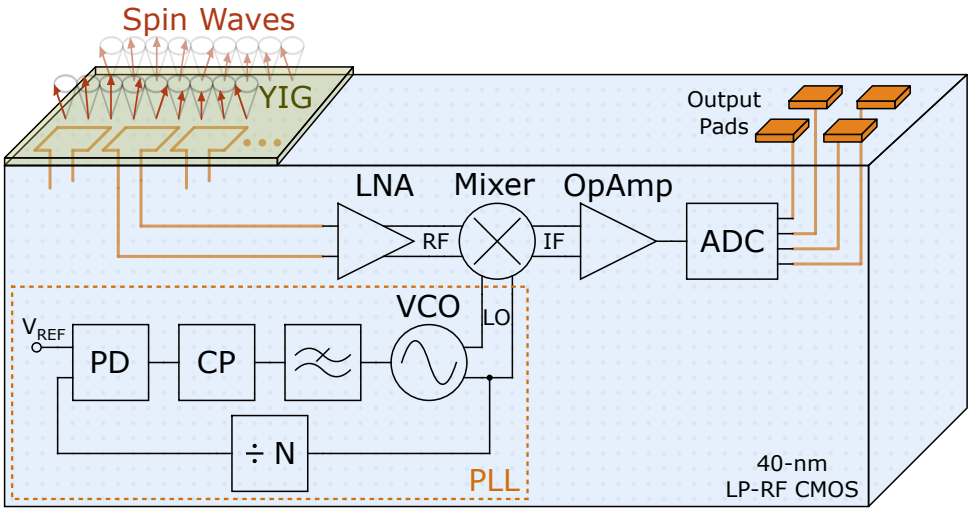

Figure 1.3: Conceptual schematic of Spin Wave (SW) on-chip detection. The SWs, propagating in the YIG film, are picked up with near field on-chip antennas. The transduced signal is processed in a CMOS Integrated Circuit (IC) (see Chapter 4). Information about SW frequency, amplitude change or phase difference between two SW signals is provided at the output pads in a digital form.

Nevertheless, the interface between a SW system and an electronic system remains one of the biggest bottlenecks to the integration of SW devices in consumer applications [21, 27, 28]. Producing SW devices on a single chip with CMOS technology is challenging, since efficient interfaces between a SW device and an electronic system are required.

There are several mechanisms for SW generation. A common way of SW excitation is a stripline with an AC current placed next to a SW propagating area [29]. Another possibility is usage of the Spin Hall Effect (SHE) [30, 31] or spin-torque nano-oscillators [32].

For the detection of the SWs Brillouin Light Scattering (BLS) [33] spectroscopy is often used [22, 32]. Picking up the SW signal with a small near field antenna is another method for the detection [13]. A brief overview of SW sensors is given in Chapter 2.

A single SW device or even a whole magnonic system integrated with a CMOS circuitry could look like the concept depicted in Figure 1.3. There is no integrated SW device to this date, enabling the characterization of propagating parameters of the SW such as the frequency, amplitude or phase. Instead, relatively bulky and expensive measurement setups are used for this purpose. But on the long run, if the trend goes to analyze SWs with low costs and to offer products with magnonic systems inside, it is obvious that SW devices have to be integrated together with electronics on a single chip or alternatively with a flip chip method.

In this work the concept for an on-chip SW device characterization is developed. Based on assumptions made for the near field loop antenna (see Chapter 2), the CMOS readout circuitry is designed. The operating principle is based on a heterodyne receiver, as depicted in Figure 1.3. The picked up SW signal is amplified by a Low Noise Amplifier (LNA) at Radio Frequency (RF) and millimeter Wave (mmW). Afterwards, the signal is down-converted by a mixer to Intermediate Frequency (IF). Local Oscillator (LO) signal, required for the mixer, is generated by a Voltage Controlled Oscillator (VCO), which is controlled by a Phase Locked Loop (PLL). Finally, an Operational Amplifier (OpAmp) additionally amplifies the IF signal, before it can be digitized by an Analog-to-Digital Converter (ADC).

In order to evaluate the performance of the designed circuitry (LNA, mixer, VCO, PLL and OpAmp) some fundamental parameters are described in Chapter 3. The operation principle of the CMOS building blocks, depicted in Figure 1.3, is explained in more detail in Chapter 4 and their simulation results are described in Chapter 5. In this thesis, the circuitry design is focused on the components affecting the output of the OpAmp, i.e. the design of an ADC is not considered. However, the ADC design at lower operating frequencies ($10 - 60\,\mathrm{MHz}$) is relatively straightforward. Hence, the SW characterization regarding its frequency, amplitude change and phase shift is done at the OpAmp output and is demonstrated in Chapter 6. For the first order approximation of the interconnect parasitics and their influence on the circuitry performance, the layout of the LNA is created and described in Chapter 7. Chapter 8 concludes the dissertation and proposes further development steps of the SW readout circuitry.

Chapter 2

Spin Wave Sensors

SWs are the propagating stimuli of electrons magnetization. Similar to the phonons as quasiparticles of lattice vibrations in a solid state, the SWs can be described by its quasiparticles, the magnons. While lattice vibrations are defined by the deflection of neighboring atoms from its equilibrium state, the SWs are described by the phase relation of precessing magnetic moments of neighboring electrons [34, pp. 12-13]. The visualization of a SW with its wave length is depicted Figure 2.1. The excitation of a spin results in the delayed deflection of the neighboring spins, which excite the next spins. Such propagation of the deflected spins forms the Spin Wave (SW). For more fundamental physical background of the SWs and the mathematical descriptions of its device models, the reader is referred to [13, 35–38] as well as to the recent magnetism roadmap [39].

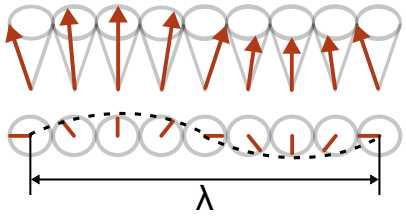

Figure 2.1: Sketch of the excited electron spins magnetized in same direction, forming the Spin Wave (SW). The wave length is defined as a distance of the excited spins with the same phase.

In order to analyze SWs, X-ray spectroscopy [40] or time-resolved Magneto-Optic Kerr Effect (MOKE) [41] can be used. However, the commonly used technique for detecting and characterizing the SW device probes is μ-BLS [33]. Especially, the possibility to visualize the spacial propagation of the SWs with high temporal resolution makes this equipment attractive for research. The SW frequencies up to 500 GHz with a resolution around 50 MHz can be measured [33]. The simplified operating principle of the BLS is sketched in Figure 2.2. A probe with propagating SWs is irradiated with a monochromatic laser light of certain energy hf_1 and momentum $\vec{p_1}$. Based on the spectrum analysis of the reflected light with energy hf_2 and momentum $\vec{p_2}$, a statement can be made about propagating SWs in the sample.

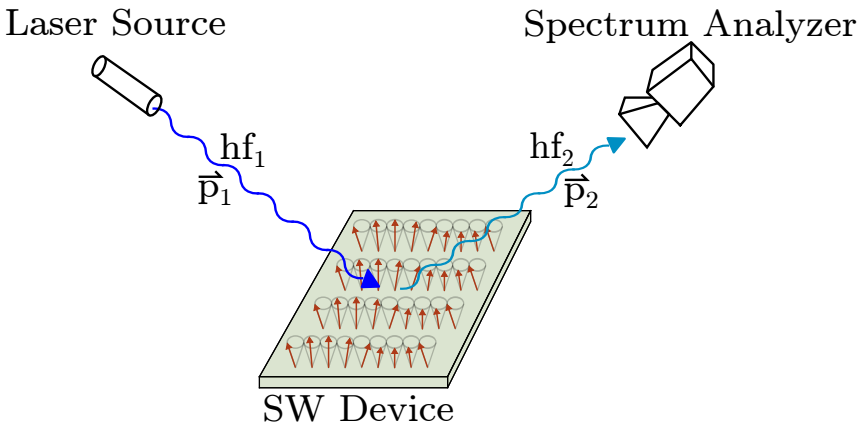

Figure 2.2: The principle of the BLS measurement technique for SW characterization. The frequency difference of the incident and scattered waves is used to analyze the SWs propagation in a sample. The spectrum analysis of the reflected electro-magnetic wave is performed with a Fabry–Pérot interferometer [33].

For more details of the μ-BLS measurement technique for SW characterization the reader is referred to [33].

There are several possibilities to transduce the SW signal into electronic domain. Each of them has right to exist for certain applications with their pros and cons. However, only some of the SW transducers with acceptable performance and lowest manufacturing costs will dominate the market or certain market niche. In this chapter SW sensors with a potential to be integrated with an electronic system [35, p. 36], directly or with flip chip method, are briefly described.

2.1 Combination of Spin Pumping and Inverse Spin Hall Effect

In order to understand the sensing principle of the SWs by the combination of the Spin Pumping (SP) and Inverse Spin Hall Effect (ISHE), each of the both processes is separately described in the following subsections.

2.1.1 Spin Pumping

In simple terms, the SP is a generation process of spin current from magnetization dynamics [42, p. 2]. This phenomenon occurs at the interface between a magnetic material and a metallic conductor, i.e. the SWs in magnetic material pump the spin current into the adjacent conductor. The corresponding theory of the SP is proposed by Tserkovnyak [43]. As depicted in Figure 2.3 the spin orientation in the magnetic material aligns the electron spins in the non-magnetic metal, resulting in the spin current I_S perpendicular to the spin orientation. Besides, the propagating torque of the magnetization precision decreases by entering the metallic region, due to enhanced Gilbert damping.

The reciprocal effect of the SP is the Spin Transfer Torque (STT), i.e. from the

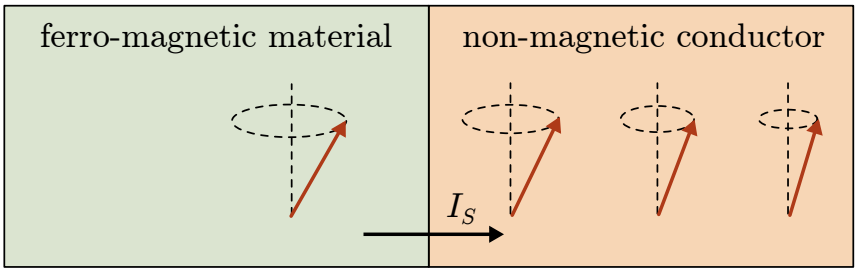

Figure 2.3: Spin Pumping (SP) effect by contacting the magnetic material with a non-magnetic metallic conductor. The magnetization dynamics in magnetic materials result in the spin current I_S flowing into the adjacent conductor.

spin current in the conductor the SW in the magnetic material like YIG can be excited. To generate the spin polarized current, the conventional charge current has first to be passed through the magnetic material with a certain magnetization direction. [42]

2.1.2 Inverse Spin Hall Effect

The Hall effect, discovered by Edwin Hall in 1879 [44], describes the movement of electrons in a conductor while applying an external magnet field. Due to the Lorentz force, the electrons deflect from their moving direction perpendicular to the current and the external magnetic field directions. This results in the Hall voltage at the appropriate conductor edges proportional to the strength of the applied magnetic field.

A similar effect is considered for the spin current, generated from the charge current, even without an external magnetic field. The SHE is postulated by Dyakonov and Perel [45, 46]. The first experimental proves of the ISHE and SHE are provided by Bakun [47] and Kato [48], respectively. The reciprocal effect to the SHE is the ISHE, that is used to convert the spin current into the electrical charge current [49, 50].

The schematic visualization of the ISHE is shown in Figure 2.4. From [49] we know,

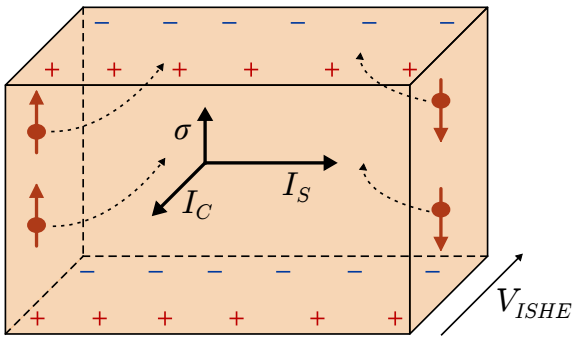

Figure 2.4: Sketch of the working principle of the Inverse Spin Hall Effect (ISHE). The spin current I_S with the spin polarization σ results in the electrical charge current I_C and the ISHE voltage V_{ISHE} [49].

that the electrical current I_C is proportional to the cross product of the spin current I_S and the spin polarization σ

$$I_C \propto I_S \times \sigma. \tag{2.1}$$

If we assume a spin current I_S from left to right and the spin-up polarization σ, then the electrons bend into the drawing plane [49]. Same happens with the spin-down electrons flowing from right to left. Consequently, the difference of the potentials, symbolized by plus and minus, results in between the front and the back of the sketched conductor. As shown by Chumak [50], the inversion of the spin current direction leads to the inversion of sign of the measured ISHE voltage V_{ISHE}.

2.1.3 Spin Wave Detection

The combination of the Spin Pumping (SP) and Inverse Spin Hall Effect (ISHE), described above, [37, 51] can be applied to detect Spin Wave (SW). The SWs, propagating in YIG, can used to generate the spin current in an adjacent conductor and consequently the ISHE voltage, that can be measured and analyzed by an IC. It is noted, that the frequency information is lost with this detection methodology and only DC voltage can be transduced to the electronic domain. However, it significantly relaxes the requirements for the IC readout circuitry.

For the nanoscale SW based spectrum analyzer, proposed by Papp [21], the combination SP-ISHE, as the SW sensing element, can be reasonably applied for the SW analysis, alternative to the loop antennas. The frequency information of the SWs is coded in the positions of the placed sensors.

2.2 Near Field Coplanar Waveguide Antenna

The inductive coupling of the magnetization dynamics can be realized with a coplanar waveguide, which is appropriately sized to the expected SW frequency. Such inductive detection is often called Propagating Spin Wave Spectroscopy (PSWS). Vlaminck [52] demonstrated the SW excitation and detection in $1 - 15\,\mathrm{GHz}$ frequency range with the coplanar antenna, as depicted in Figure 2.5. With the coplanar waveguide excited SWs propagate through the ferromagnetic thin film and are picked up by the identical coplanar antenna on the detection side. The signal path of the antenna is inside of two ground tracks serving as return conductors. The width of the signal track is twice of the ground track, in order to keep the sheet resistance of the whole signal path constant. Finally, the induced voltage V_S in the antenna has been analyzed with a Vector Network Analyzer (VNA) [52]. It is to be noted, that the output port of the proposed coplanar waveguide is suitable for the IC CMOS detection as well.

The folded structure of the coplanar waveguide, proposed by Vlaminck [52], allows precise adjustment of the SW frequency excitation and its detection. The antenna geometry also improves the transduction efficiency between the magnonic and electronic domains [52]. The frequency adjustment is realized by an appropriate sizing

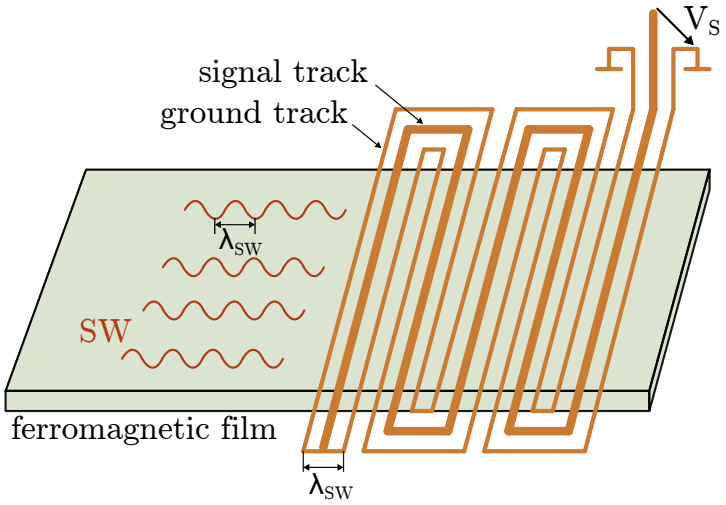

Figure 2.5: Coplanar waveguide as sensing element for SW detection propagating in a ferromagnetic thin film, e.g. YIG. The meander structure of the antenna improves the efficiency of the transduction [52]. The distance between two ground tracks of the waveguide should equal to the wavelength of the propagating SWs, in order to achieve high signal sensitivity (see also Figure 2.6).

of the distances between the signal and ground tracks. To understand this relationship, the spatial current density flow in the antenna is sketched in Figure 2.6. Here we can see, that the distance between two ground tracks of the waveguide results in from the SW frequency. From the assumed fact, that the width of the signal track is twice of the ground track, dimensions of the remaining geometric parameters can be calculated. A detailed analysis of the coplanar waveguide transducer with different geometries is described in [52]. An alternative inductive detection of the SWs

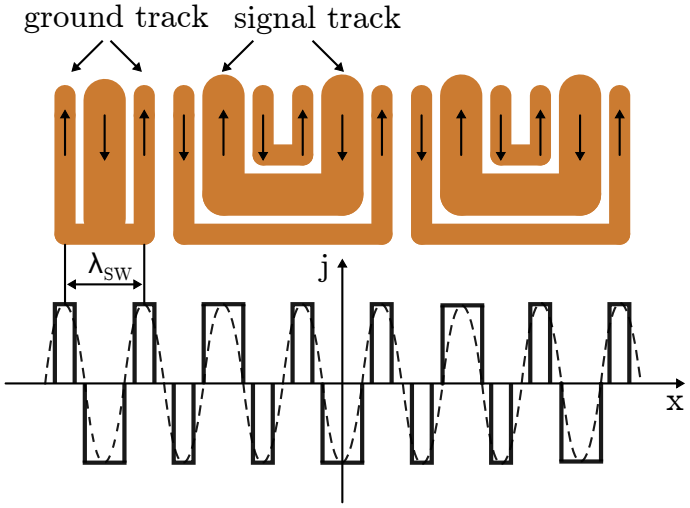

Figure 2.6: Spatial distribution of the current density flowing through the coplanar waveguide. The geometry of the waveguide is selected with the target for achieving a close approximation to a sinusoidal distribution as close as possible. Figure is adopted from [52].

with a U-form waveguide is reported in [53]. Besides, the Propagating Spin Wave Spectroscopy (PSWS) detection methodology is described in [29, 54–56].

2.3 Near Field Loop Antenna

To use the magnetic loop antenna, as a transducer from the SW signal into an electrical one, is the next possibility for the SW sensing [133]. It provides a low resistive and scalable sensing area. The on-chip antenna can be placed below the magnetic thin film with a low damping material, like YIG (see Figure 2.7a).

The model of the loop antenna is approximated by an ideal voltage source with the serial resistance and inductance, as depicted in Figure 2.7b. In addition, the noise source represents mainly the thermal noise, caused by the resistance. The thermal agitation of the magnetic moments is negligible compared to the thermal noise of the 50 Ω loop resistance. The equivalent resistance of the magnetic noise is in the range of 1 mΩ [133]. A relatively low magnetic noise originates from the damping of the YIG material. As shown by Scholz [57], the intensity of magnetic fluctuation is associated with the magnetic damping coefficient.

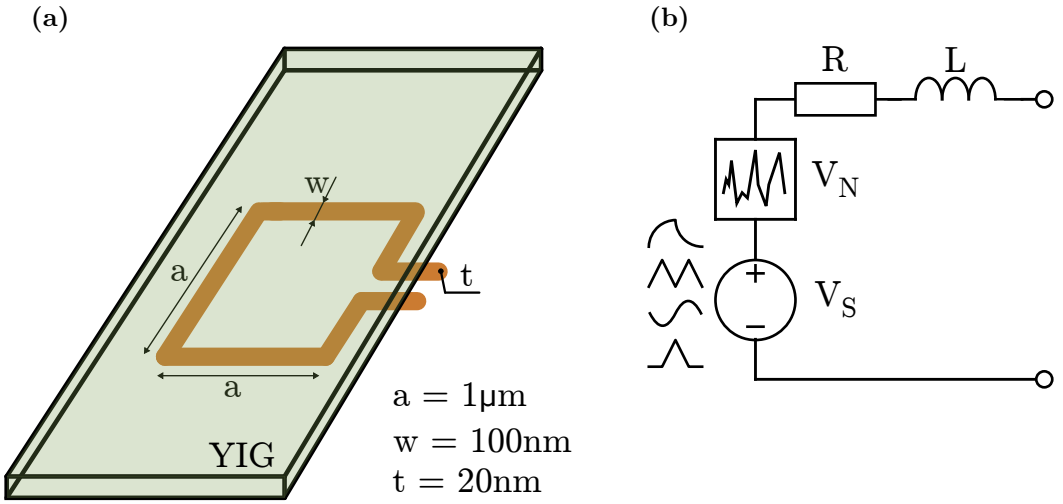

Figure 2.7: Sketch of the loop antenna placed below the non-conductive material YIG (a) and its equivalent circuit model (b). The squared loop antenna has the side length a, width of the wire w and thickness of the wire t. The resistance R and the inductance L result in from the geometry of the transducer. In addition, the model includes the voltage source V_S with the noise source V_N, originated mainly from the thermal noise of the conductor.

The integrated loop antenna as a sensor for electromagnetic near-field measurement has been extensively considered by Uddin [58] during his dissertation. Here, based on his work, the first order model of the loop antenna has been derived, i.e. neglecting the eddy currents, dielectric losses, radiation resistance and other second order effects [58, p. 27]. The resulted values for the resistance, the inductance and the voltage source are described below.

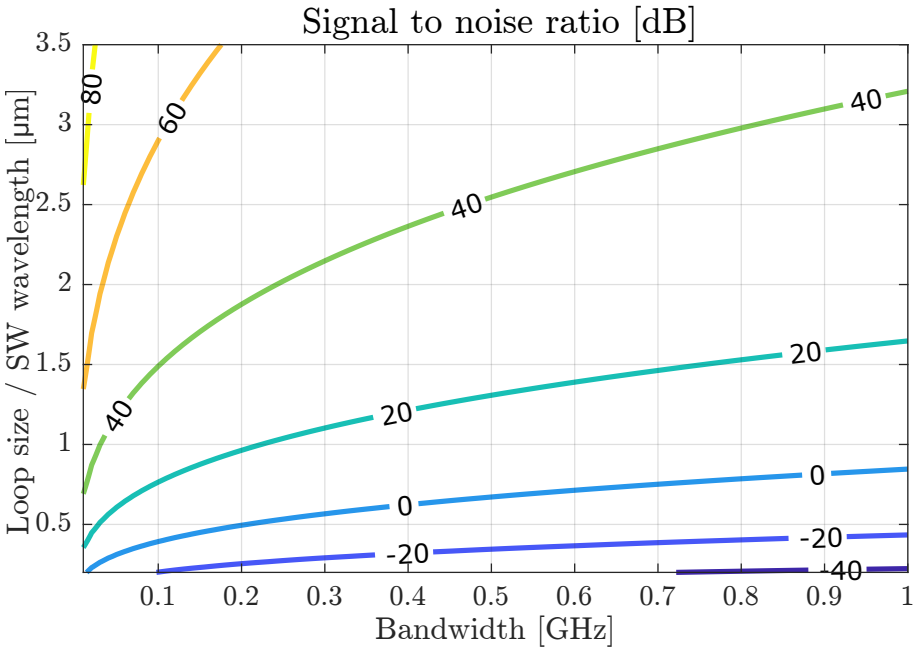

Figure 2.8: Simulated Signal-to-Noise Ration (SNR) of the squared loop antenna depending on its size and the considered bandwidth. The ordinate of the graph is normalized to the wavelength of the SW. As to expect, a larger area and a smaller bandwidth show a better SNR. [134]

As reported in [133], the considered squared loop antenna with an area of $1\,\mu m^2$ could induce signal with an amplitude in the range of tens microvolts. Besides, as depicted in Figure 2.8, the Signal-to-Noise Ration (SNR) is around $20 - 40\,dB$ with a restriction to a 100 MHz bandwidth.

2.3.1 Resistance of the Transducer Model

For the current flowing through a conductor at high frequencies the skin effect has to be kept in mind, i.e. the current density near the surface could be higher than near the middle of the wire's cross section. Thus, the skin depth (Equation 2.2) [58, p. 27] has to be considered for the resistance calculation of the loop antenna

$$\delta = \frac{1}{\sqrt{\pi f \mu_0 \mu_r \sigma}}, \tag{2.2}$$

where f is the considered operating frequency of the SW device ($9 - 50\,GHz$), σ is the gold conductivity ($4.47\,\frac{A}{Vm}$), μ_0 is the magnetic constant ($4\pi \cdot 10^{-7}$) and μ_r is the relative permeability of the medium.

At the highest considered frequency of 50 GHz the skin depth is around 350 nm. Thus, for the assumed dimensions of the squared loop antenna the skin effect can be neglected, i.e. the current fills the entire cross section. Consequently, the resistance of the transducer can be approximated by the standard formula in Equation 2.3

$$R = \frac{4a}{\sigma w t}, \tag{2.3}$$

where a is the side length of the loop antenna equal to $1\,\mu$m, w is the wirde width of 100 nm and t is the wire thickness of 20 nm. The resulted resistance of the loop antenna is equal to $49\,\Omega$. That fits very well to the transmission line standard of $50\,\Omega$.

2.3.2 Inductance of the Transducer Model

The inductance of a planar square loop antenna can be calculated with Equation 2.4 [58, pp. 27-28]

$$L = \frac{\mu_0 \mu_r 4a}{2\pi}\Big[\ln\Big(\frac{a}{r}\Big) - 0.77401 + \frac{\mu_r}{4}\Big], \tag{2.4}$$

where a is the side length of the loop antenna ($1\,\mu$m), r is the radius of the wire, μ_0 is the magnetic constant and μ_r is the relative permeability of the medium. The above formula for the inductance calculation is applied for a circular cross section. In order to estimate the inductance for a rectangular cross section, the equivalent radius can be approximated with Equation 2.5 [59]

$$r = \frac{w}{2(1 + 1.13\log(\frac{w}{t}))} \tag{2.5}$$

,

with the width of the wire w equal to 100 nm and the thickness of the wire t equal to 20 nm. With the assumed dimensions, listed above, the inductance of the loop antenna results in 2.44 pH. As reported in [133], the presence of the magnetic YIG film influence the inductance of the loop. Performing the Object Oriented Micro-Magnetic Framework (OOMMF) [60] simulations, the inductance of the transducer model is finally approximated to 25 pH, i.e. the YIG material is the main contributer to the inductance of the transducer.

2.3.3 Voltage Source of the Transducer Model

The induced voltage peak in the loop antenna can be estimated by Equation 2.6 [133]

$$V_S = a^2 f \mu_0 M_s M_{defl}, \tag{2.6}$$

where a is the side length of the loop antenna ($1\,\mu$m), f is the considered operating frequency of the SW device ($9 - 50$ GHz), μ_0 is the magnetic constant, M_s is the saturation magnetization of YIG ($1.4 \cdot 10^5$) and M_{defl} is the relative SW amplitude of 0.01.

Considering the lowest frequency of 9 GHz the induced voltage amplitude is around $16\,\mu$V. It is important to mention, that the induced voltage is dependent on the size

of the loop antenna and the frequency of the SW device. Besides, the non-considered imperfections at the interface between the YIG and the transducer would highly impact the picked up signal power. Nonetheless, the above considerations show the first estimation of the loop antenna's model, required as input for the readout circuitry, described in Chapter 4. Thus, the induced voltage amplitudes around $10 - 20\,\mu$V are considered for the $50\,\Omega$ transducer with the self-inductance around $25\,$pH.

Chapter 3

Fundamentals

This chapter briefly summarizes the parameters required to characterize circuit components like LNA, mixer and PLL with VCO described in Chapter 4. Here, only basic definitions and statements required for the design are mentioned. For more detailed information the reader is referred to the respective references mostly taken from Razavi [61], Lee [62], Nguyen [63] and Pozar [64].

It is obvious that it is impossible to design a circuit while having all parameters at best performance. Thus, trade-offs are required depending on an application. The RF design hexagon depicts this problem in Figure 3.1. In case of the designed spectrum analyzer the trade-offs are made especially between noise, power and frequency. Having a wide frequency bandwidth and, at the same time, high gain over the whole operating frequency is challenging. Thus, the compromises have to be made. Due to the relatively low voltage values, expected at the input of the LNA, the linearity provides less of a concern.

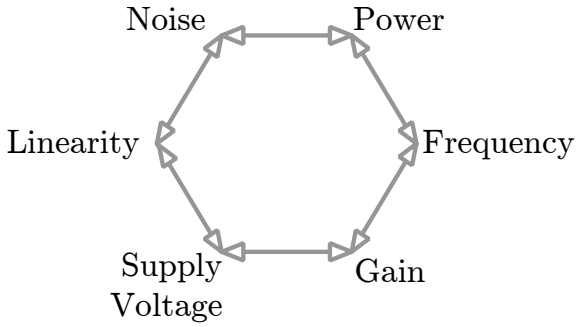

Figure 3.1: RF design hexagon representing trade-offs between parameters, e.g. the smaller the influence of the noise and the wider the operating frequency band, the more power is consumed by the circuit. [61, p. 4]

3.1 Matching

If the signal's wavelength reaches the range of device's physical dimensions, then the electronic components can no longer be modeled as lumped elements [64, p. 1], i.e.

poor matching leads to undesirable reflections and possibly voltage attenuations [61, p. 258]. The question arises, whether the matching technique is needed, if the targeted operating frequency of the IC is in the range of $9 - 50\,\text{GHz}$. If the half of the signal's rise or fall time approaches the one-way propagation time along the signal path, the impedance matching between two ports is required [65]. In low-κ (dielectric constant lower than 3.9) materials the propagation velocity v of the signal energy is estimated to be

$$v > \frac{c}{\sqrt{3.9}} \approx 15\,\frac{\text{cm}}{\text{ns}}. \tag{3.1}$$

The variable c denotes the speed of light in free space. The rise time t_R ($10 - 90\,\%$ change) of a sinusoidal signal can be approximated by

$$t_R = \frac{2\arcsin(0.9)}{2\pi f} \approx \frac{0.35}{f}, \tag{3.2}$$

$$7\,\text{ps} < t_R < 39\,\text{ps}, \quad f \in [9\,\text{GHz}, 50\,\text{GHz}]. \tag{3.3}$$

Consequently, for interconnect distances $d_{|9\,\text{GHz}} > 2.925\,\text{mm}$ and $d_{|50\,\text{GHz}} > 0.525\,\text{mm}$ transmission line terminations are required, i.e. for all RF and millimeter Wave (mmW) inputs and outputs connected to the pads of the chip.

The simplest way to match the LNA input to $50\,\Omega$ for a wide frequency band is to connect a resistor with $50\,\Omega$ in parallel to the source. However, as shown in [61, p. 51] this method dramatically deteriorates the Noise Figure (NF), such that values less than 3 dB cannot be achieved. Consequently, other techniques are required to achieve an input matching of the $50\,\Omega$ without the integration of the physical $50\,\Omega$-resistor with thermal noise. Some of these implemented methods are mentioned in Chapter 4. More details of other matching techniques, like the L-Match, π-Match or T-Match, are described in [62, pp. 94-104].

3.2 Scattering Parameters for Two-Port Network

In practice, measuring voltages and currents directly is more difficult than measuring power at high RF or mmW frequencies [64, p. 178], e.g. applying open- and short-techniques could lead to undesired oscillations [62, p. 225]. Thus, it is common practice to characterize RF and mmW devices, circuits or whole systems by parameters that can be obtained from power measurement [61, p. 71]. These parameters are called *scattering parameters* or *S-parameters*. Figure 3.2 visualizes the definition of the S-parameters of a two-port network. Mathematical definitions are stated in Equations 3.4-3.7 [61, pp. 71-73]

$$S_{11} = \frac{E_{r1}}{E_{i1\,|E_{i2}=0}}, \tag{3.4}$$

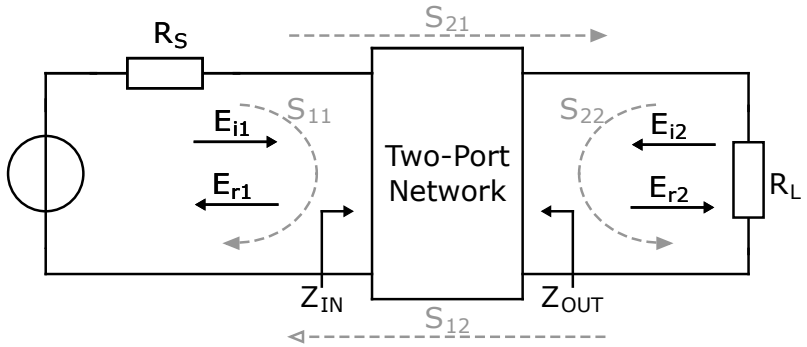

Figure 3.2: Illustration of the S-parameter definitions of a two-port network with source resistance R_S and load resistance R_L. E_i and E_r denote incident and reflected waves, respectively. Z_{IN} and Z_{OUT} represent input and output impedances of the two-port network.

$$S_{12} = \frac{E_{r1}}{E_{i2\,|E_{i1}=0}}, \tag{3.5}$$

$$S_{22} = \frac{E_{r2}}{E_{i2\,|E_{i1}=0}}, \tag{3.6}$$

$$S_{21} = \frac{E_{r2}}{E_{i1\,|E_{i2}=0}}. \tag{3.7}$$

S_{11} represents the accuracy of the input matching.
S_{12} represents the coupling of the output signal to the input signal.
S_{22} represents the accuracy of the output matching.
S_{21} represents the gain of the circuit.

E_{i1} is the incident wave at the input.
E_{r1} is the reflected wave at the input.
E_{i2} is the incident wave at the output.
E_{r2} is the reflected wave at the output.
$E_{i1,i2} = 0$ means that there is no reflection from the source or load, respectively.

The most relevant of the above mentioned parameters is S_{11}, as it describes the input matching accuracy of the designed spectrum analyzer (see Chapter 4). In order to test the designed receiver, the input of the LNA has to be connected with an external measurement setup, i.e. the cable length of the equipment is above the wave length of the input signal. Besides, the input of the LNA has to be matched to the standard $50\,\Omega$ termination.

Often S_{11} is expressed in dB and lower values mean better matching or less reflection at the input. A typically acceptable value is $-10\,\text{dB}$ [61, p. 259]. As shown in Chapter 5 the goal is set to design the LNAs with S_{11} parameter lower than $-10\,\text{dB}$, i.e. less than $10\,\%$ is reflected back.

Another relevant parameter is the *reflection coefficient* Γ defined as [62, p. 222]

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}, \tag{3.8}$$

with load impedance Z_L and reference impedance Z_0. Considering the reflection coefficient at the input of an LNA, S_{11} and Γ are one and the same. The variables Z_L and Z_0 from Equation 3.8 correspond to Z_{IN} and R_S from Figure 3.2, respectively.

3.3 Noise Figure

The Noise Figure (NF) is one of the key performance metrics in IC design. It shows the Signal-to-Noise Ration (SNR) degradation of the signal propagating from input to output of a circuit component and is defined as [61, p. 49]

$$\mathrm{NF} = \frac{\mathrm{SNR_{IN}}}{\mathrm{SNR_{OUT}}}. \tag{3.9}$$

An LNA, for instance, amplifies the signal and the noise at the input by the same factor. Thus, at the output the same SNR is expected, if the LNA is noiseless. In this case the NF is equal to 1. In practice, however, the NF is always greater than 1, due to the existence of noisy components inside the LNA. [64, pp. 502-503]

Input matching plays a significant role for the NF, too. Equation 3.10 shows the degradation of the NF in case of a mismatched circuitry. For a non-zero reflexion coefficient Γ the NF increases. $\mathrm{NF_M}$ denotes the NF of a perfectly matched input impedance. [64, p. 511]

$$\mathrm{NF} = 1 + \frac{\mathrm{NF_M} - 1}{1 - |\Gamma|^2} \tag{3.10}$$

An LNA is commonly designed with more than one stage. In this case the designer has to keep in mind that the most critical stage regarding the NF is the first one. The Friis formula [66] points out in Equation 3.11 that the NF of a cascaded circuit directly depends on the NF of the first stage. NFs of the following stages contribute to the whole NF as well, but are reduced by the power gains G_i of the previous stages. This fact is visualized in Figure 3.3.

$$\mathrm{NF} = \mathrm{NF_1} + \frac{\mathrm{NF_2} - 1}{G_1} + \frac{\mathrm{NF_3} - 1}{G_1 G_2} + \frac{\mathrm{NF_4} - 1}{G_1 G_2 G_3} \ldots \tag{3.11}$$

Since the NF is an expression of power at the input and output of a circuit component, it is often expressed in dB

$$\mathrm{NF_{|dB}} = 10 \log(\mathrm{NF}). \tag{3.12}$$

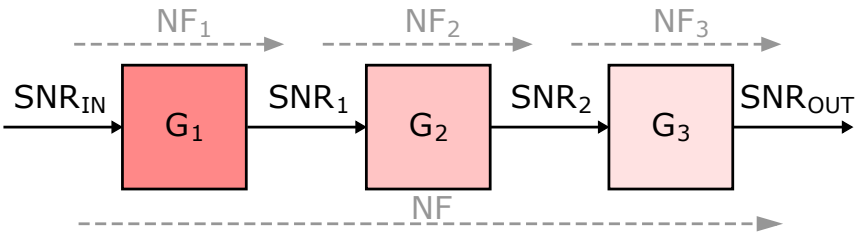

Figure 3.3: Schematical overview of a cascaded network with gain G_i and noise figure NF_i, calculated as ratio of the SNR at the stage input to the SNR at the stage output. NF_1 is the main contributor to the whole NF.

A receiver LNA typically has an NF of $2 - 3\,\text{dB}$ [61, p. 255], dependent on the operating frequency bandwidth of the LNA. Due to a relatively high bandwidth of the designed LNAs (see Chapter 4), the goal was to achieve NFs around 3 dB.

The definition of the NF for a mixer is the same as for the LNA, as stated in Equation 3.9. However, the NF is distinguished by two types, Single-Sideband (SSB) and Double-Sideband (DSB). The SSB NF is higher than the DSB by 3 dB in most cases, due to the additional noise from the image band [61, p. 344].

Figure 3.4 shows the noise contribution of the image band to the total noise at the output of the mixer, i.e. the noise at $\omega_{LO} + (\omega_{LO} - \omega_{RF})$ is also down-converted to the IF, same as the RF signal. Thus, it reduces the SNR at the output by a factor of 2, if the noise power at the image band is equal to the noise power in the signal band.

In case of a direct-conversion mixer, i.e. $\omega_{LO} = \omega_{RF}$, the signal power is also available in the image band. Hence, the SNR at the mixer output is not degraded and the DSB can be applied for NF quantization. However, for the SW spectrum analyzer the LO frequency is swept over a large frequency band and it is challenging to design a VCO with a sweep step size in Hz range. As described in Section 5.3, the step size is around 20 MHz. Consequently, the SSB definition for the NF consideration is used in this thesis.

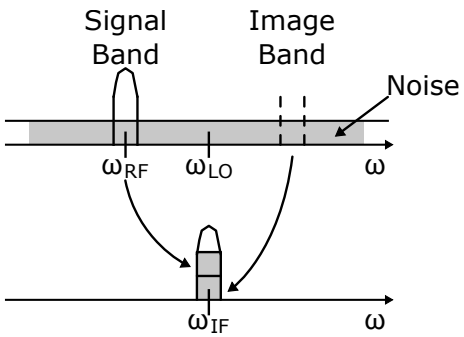

Figure 3.4: Noise contribution from the signal band and the image band to the total noise at the IF output of the mixer. By down-converting the RF signal to the lower IF signal, the additional undesired noise at $\omega_{LO} + (\omega_{LO} - \omega_{RF})$ is added to the noise from the signal band at $\omega_{LO} - \omega_{RF}$.

3.4 Gain

As already mentioned in the previous Section 3.3, the gain of the receiver LNA should be large enough in order to minimize the contribution of subsequent circuit components, like the down-conversion mixer, to the overall NF. There are several definitions for the power gain dependent on considered nodes of a two-port network with source and load matching blocks [64, pp. 558-561]. However, in ICs with an LNA driving a mixer directly, no matching between these two components is required, since the wavelength of the RF/mmWave signal is much larger than the physical dimensions of the interconnections between these two circuit components [61, p. 257], [67]. Thus, it is more convenient to consider the voltage gain A (see Equation 3.13), instead of the power gain, in order to characterize the performance of the LNA.

$$A = \frac{V_{OUT}}{V_{IN}} \tag{3.13}$$

As already mentioned in Section 2.3, the input voltage for the LNA is expected to be in the range of $10 - 20\,\mu$V. In order to have at least $200\,\mu$V at the input of the mixer, the voltage gain of the LNA has to be more than 26 dB.

The signal amplification by an active mixer is called *conversion gain*, the ratio of the voltage amplitudes of the IF signal to the RF signal. Typical values of the voltage conversion gain for a mixer are around 10 dB [61, p. 339].

3.5 Linearity

All practical amplifiers have a certain dynamic range for the minimum and maximum power that can be applied at the input in order to have a reasonable output signal. The applied minimum input power, that can be detected at the output, is limited by noise. The applied maximum input power is limited by saturation seen at the output due to the finite power supply of the circuit and non-linear effects of active devices, like transistors.

For the designed spectrum analyzer, relatively low input voltages of $10 - 20\,\mu$V are expected, so there is no risk for saturation at the output of the designed circuit components. However, in order to benchmark an LNA or a mixer regarding the dynamic range, the 1 dB compression point and the 3rd order intercept point are reasonable parameters to consider. The simulation results are presented in Chapter 5.

3.5.1 1 dB Compression Point

Figure 3.5 visualizes the definition of the 1dB compression point of a non-linear device. For an ideal amplifier the dependence between input power and output power always remains linear. In practice, the gain starts to reduce at a certain point. The deviation of the output power level from the ideal value by 1 dB is defined as *1 dB compression point*. For the compression parameter either the input or the output

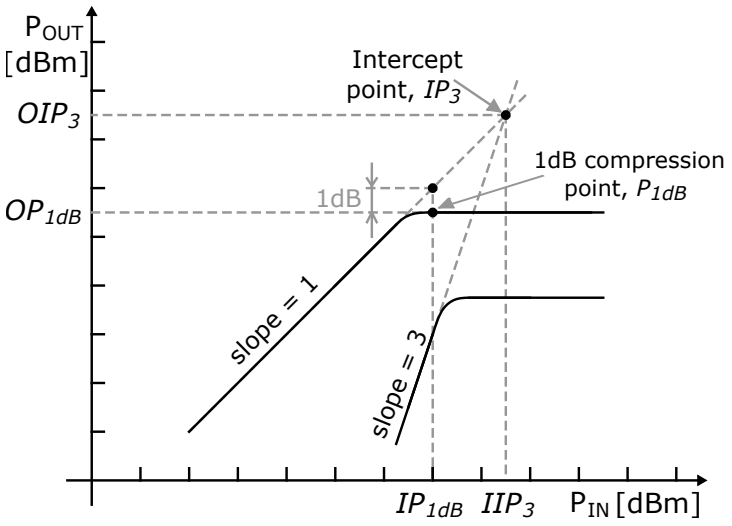

Figure 3.5: Definitions of the linear distortion parameters the *1 dB compression point* P_{1dB} and the *3rd order intercept point* IP_3. The curves represent the 1st and the 3rd order intermodulation products of the output power versus the input power in a log-log scale. Both responses indicate a compression at a certain input power. The ideal responses are extended with dashed lines.

power can be considered and defined as the Input referred 1 dB compression Point (IP_{1dB}) or as the Output referred 1 dB compression Point (OP_{1dB}), respectively. [64, pp. 512-513]

3.5.2 3rd Order Intercept Point

The definition of the 3rd order intercept point is visualized in Figure 3.5. Similarly to the 1 dB compression point, the input and the output power of a network is considered. Assuming an ideal device the output power, caused by the 3rd order terms of the Taylor series (see Equation 3.15), increases thrice as fast as for the 1st order, i.e. at a certain point, the Intercept Point (IP_3), these two curves intersect. The corresponding input and output powers are identified by the 3rd Order Input Intercept Point (IIP_3) and the 3rd Order Output Intercept Point (OIP_3), respectively.

In general, an input response of a non-linear system can be modeled using a Taylor series. For an input signal with a single frequency ω the system response has harmonics at $n \cdot \omega$, $n = 1, 2, 3, ...$, which can be easily filtered out in most cases. However, an input signal with two closely placed tones has also higher order frequency components at the sum and at the difference of the input frequencies. If we assume an input signal v_i with an amplitude V_0 and two tones at ω_1 and ω_2

$$v_i = V_0(\cos\omega_1 t + \cos\omega_2 t), \tag{3.14}$$

then the time response v_o at the output is equal to [64, pp. 513-514]

$$
\begin{aligned}
v_o = {} & a_0 + a_1 V_0 \cos\omega_1 t + a_1 V_0 \cos\omega_2 t \\
& + \frac{1}{2} a_2 V_0^2 (1 + \cos 2\omega_1 t) + \frac{1}{2} a_2 V_0^2 (1 + \cos 2\omega_2 t) \\
& + a_2 V_0^2 \cos(\omega_1 - \omega_2) t + a_2 V_0^2 \cos(\omega_1 + \omega_2) t \\
& + a_3 V_0^3 \left(\frac{3}{4} \cos\omega_1 t + \frac{1}{4} \cos 3\omega_1 t \right) + a_3 V_0^3 \left(\frac{3}{4} \cos\omega_2 t + \frac{1}{4} \cos 3\omega_2 t \right) \\
& + a_3 \boldsymbol{V_0^3} \left[\frac{3}{2} \cos\omega_2 t + \frac{3}{4} \cos(\boldsymbol{2\omega_1 - \omega_2}) t + \frac{3}{4} \cos(2\omega_1 + \omega_2) t \right] \\
& + a_3 \boldsymbol{V_0^3} \left[\frac{3}{2} \cos\omega_1 t + \frac{3}{4} \cos(\boldsymbol{2\omega_2 - \omega_1}) t + \frac{3}{4} \cos(2\omega_2 + \omega_1) t \right] + \cdots .
\end{aligned}
\tag{3.15}
$$

A special case occurs for the 3rd order, when the resulting frequency is close to the input frequency and thus cannot be filtered out properly. Especially with a rising input power the 3rd order terms of the Taylor series are not negligible, due to the power of 3 amplitude dependence. The undesired terms are marked with a bold font in Equation 3.15. The *3rd order intercept point* is therefore of great interest for the characterization of signal distortion. For the derivation of the above mentioned statements and for more detailed information on the non-linear signal distortion the reader is referred to [64, pp. 512-516].

3.6 Stability

Stability is indisputably the most important performance parameter for all electronic circuits and especially for RF and mmW circuit designs. Achieving a greater value for the gain or a lower NF of a circuit becomes irrelevant without a corresponding degree of stability. Thus, the stability parameters have to be verified continuously during the design flow, not only for the operating frequency band, but also for sufficiently wide range of frequencies.

In order to prove the circuit is *unconditionally stable*, i.e it does not start to oscillate under any conditions for source and load impedances at any frequency, the following conditions derived from Rollet stability [68] have to be met [63, p. 418-421]

$$
K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1, \tag{3.16}
$$

$$
B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0, \tag{3.17}
$$

where K and B_1 conventionally used stability parameters and $|\Delta|$ is the determinant absolute value of the scattering matrix, defined as

$$
|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|. \tag{3.18}
$$

An alternative way to prove unconditional stability with just one criterion was proposed by Edward [69]. The stability factor μ is defined as

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \Delta| + |S_{12} S_{21}|} > 1. \tag{3.19}$$

As already mentioned in Section 3.1 in ICs there is no need to match the LNA output to the mixer input, if the wire length between these two components is small enough. Besides, the load impedance of the LNA can be well controlled to avoid deviation from the nominal value. Thus, the above mentioned stability criteria are relatively pessimistic [61, pp. 259-260].

3.7 Port-to-Port Isolation

Capacitive coupling from one port to another is an issue in electronic components, especially in RF and mmW circuit design. Here, the port-to-port isolation of a mixer is considered. Figure 3.6 sketches the mixer with the input ports RF, LO and the output port IF. The port isolation is defined as the ratio of the voltages at one port to another port of the same frequency. In practice, four kinds of feedthroughs between the ports are used: LO-IF isolation, LO-RF isolation, RF-LO isolation and RF-IF isolation.

The most critical type is the LO-RF feedthrough, as it produces both a DC offset at the IF port and an undesirable propagation to the transducer (input of the LNA) with a consequent radiation of the signal. Besides, the LO signal is typically several orders of magnitude higher than the RF and IF signals. The LO-IF and RF-IF couplings are less critical since the LO and RF frequencies at the IF port are subsequently filtered out by an operational amplifier with a band pass characteristic. The RF-LO feedthrough deteriorates the spectrum of the LO signal. Due to the significant difference in magnitude (more than 40 dB) between the RF and LO signals this coupling issue is negligible. [61, p. 340], [63, pp. 637-638]

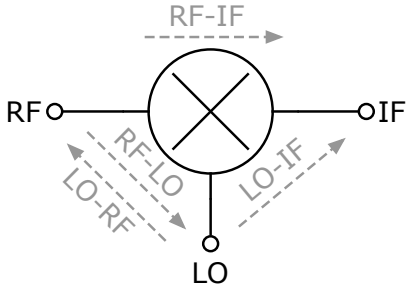

Figure 3.6: Port-to-port feedthroughs of a mixer with Radio Frequency (RF), Local Oscillator (LO) and Intermediate Frequency (IF) ports. The coupling between the ports is caused by parasitic capacitances of the used electronic devices.

3.8 Phase Noise

The spectrum of a practical Voltage Controlled Oscillator (VCO) is not an ideal Dirac delta function at the nominal oscillating frequency f_0, as it contains deviated frequency components next to f_0, due to thermal, flicker or other noise sources. This phenomenon is called *phase noise* or *jitter noise* in the time domain. Figure 3.7 visualizes the fluctuation of the frequency around the nominal value f_0, which causes an instability of the LO signal in time domain. Consequently, the precision of the SW frequency and phase detection suffer.

The phase noise (see Equation 3.20) is defined as the ratio of the noise power at offset frequency $f_0 + f_M$ with 1 Hz bandwidth and the carrier power (signal power at f_0) [63, p. 590].

$$\mathscr{L}(f_M) = 10 \log \frac{P_{Noise}}{P_{Signal}} = 10 \log \left(\frac{\text{Noise Power in 1 Hz at } f_0 + f_M}{\text{Carrier Power}} \right) \left[\frac{\text{dBc}}{\text{Hz}} \right] \quad (3.20)$$

Consider an offset frequency f_M at 1 MHz of an oscillator operating at the carrier frequency f_0 25 GHz. What does a phase noise of $-80 \frac{\text{dBc}}{\text{Hz}}$ mean? It means that the signal power at the frequency $f_0 + f_M = 25.001$ GHz in a 1 Hz bandwidth is 80 dB lower than the signal power at the frequency $f_0 = 25$ GHz. For more theoretical background on phase noise in oscillators, the reader is referred to a publication by Hajimiri [70].

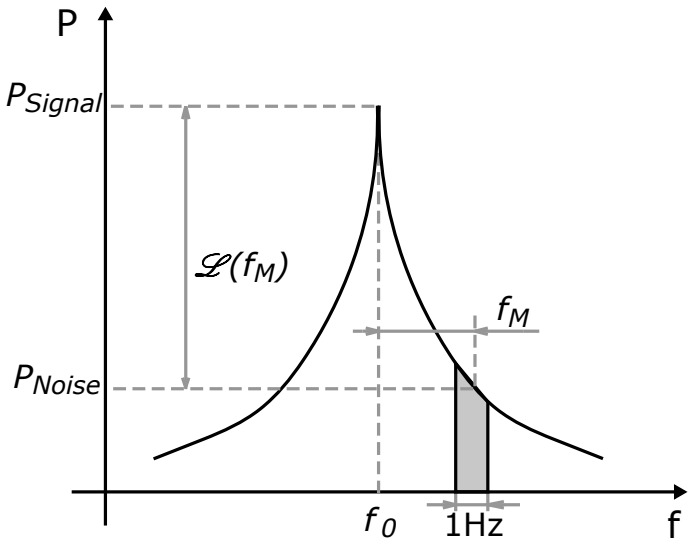

Figure 3.7: Phase noise $\mathscr{L}(f_M)$ defined by the ratio of the noise power P_{Noise} at the frequency $f_0 + f_M$ to the signal power P_{Signal} at the frequency f_0. The power is calculated for a frequency band of 1 Hz.

Chapter 4

Spin Wave Readout Circuitry Design

Based on the assumptions for the SW transducer presented in Chapter 2, the readout circuitry design is presented in this chapter. The development process of the circuitry is portrayed in Section 4.1 by referencing the author's related publications and emphasizing some currently known weak points of the presented results. After introducing the general concept of the SW characterization in Section 4.2, the readout circuitry components, such as the LNA, mixer, VCO, PLL and OpAmp are detailed in Sections 4.3-4.7, respectively.

4.1 Reference to the Author's Publications

The concept of the SW on-chip detection was first presented in [133]. The paper points out the need of an on-chip detection of SWs and consequently the necessity of dedicated CMOS circuitry. The loop antenna, as a possible SW transducer to the electronic domain, is described as well. The readout circuitry, presented in [133], enables a first approximation of the expected circuitry performance, based on previously published papers. Besides, it presents the three stage LNA that covers the frequency range of $10 - 40\,\mathrm{GHz}$ with the gain of $20\,\mathrm{dB}$. Details on the LNA are published in [132]. The main idea, to cover such a high frequency range with the single LNA design, is placing the resonant frequency of each amplifying stage at different frequency points.

The extension of the readout circuitry with the designed mixer and OpAmp in addition to the previously designed LNA is presented in [134]. Here, the SW spectrum analyzer was designed for the frequency range of $5 - 50\,\mathrm{GHz}$. The concrete methodology for the frequency, amplitude and phase detection of the SWs is described and substantiated with appropriate simulation results. However, for the LO signal an ideal voltage source has been used instead of a VCO. Besides, for the inductors an ideal Simulation Program with Integrated Circuit Emphasis (SPICE)-model was implemented.

In contrast to the topologies designed with 65 nm technology [132–134], fully differential LNAs, mixer and VCOs were implemented in the latest publication [135]. Based on the findings for the design in 65 nm CMOS technology, the design with 40 nm CMOS technology from GlobalFoundries is presented. The big advantage of the provided 40 nm CMOS technology is the presence of the RF and mmW libraries with devices modeled for up to 100 GHz. Moreover, it includes the Optimum Inductor Finder (OIF) kit as a lookup table with inductor models allowing faster design and more realistic representation compared to the previously used ideal model.

As mentioned in [134], it was attempted to design the circuitry covering the whole frequency range of $5 - 50$ GHz with a single receiver topology. The most relevant advantage of such an approach is a relatively low chip area and consequently lower manufacturing costs. However, the poor noise performance does not allow to pick up a relatively small transducer signal power of less than 90 dBm with respect to a $50\,\Omega$ impedance. Consequently, the frequency range $5 - 50$ GHz was split in several frequency bands in order to achieve a better NF of the LNA.

The SW readout circuitry published in [135] is further extended in the content of this thesis. PLL circuitry is additionally introduced. Besides, some optimizations regarding the power consumption of the readout circuitry have been achieved. It is also important to mention, that the LNA designed for $5 - 9$ GHz in [135], is not unconditionally stable, as recent analysis has shown. Relatively large inductor values were required for lower operating frequencies ($5 - 9$ GHz), i.e. a larger chip area and relatively poor modeling provided by the foundry. Thus, the frequency range for the SW characterization considered in this work is reduced to $9 - 50$ GHz. Table 4.1 shows the allocation of the $9 - 50$ GHz bands of the circuit components covering the corresponding frequency range with a single design topology.

Table 4.1: Frequency bands of the SW readout circuitry components. The check mark reflects a single topology of the LNA, mixer and VCO covering the corresponding frequency range, i.e. there are 6 different designs for the LNA, 1 for the mixer, covering the whole frequency range, and 6 for the VCO.

Bands	Freq. Range [GHz]	LNA	Mixer	VCO
1	$9 - 13$	✓		✓
2	$13 - 19$	✓		✓
3	$19 - 26$	✓	✓	✓
4	$26 - 33$	✓		✓
5	$33 - 39$	✓		✓
6	$39 - 50$	✓		✓

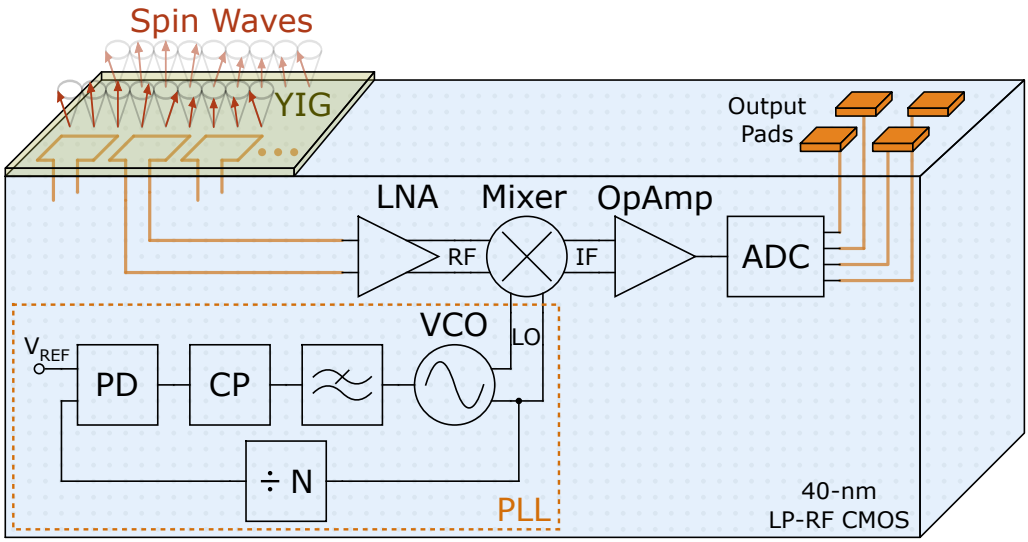

Figure 4.1: Concept of the SW detection with on-chip near field antennas placed below Yttrium-Iron-Garnet (YIG). The picked up signal is amplified and converted to lower frequencies with a circuitry realized in 40 nm CMOS technology. The digital information on the SW frequency, amplitude change and phase shift can be analyzed at the output pads.

4.2 General Concept of the Spin Wave Readout Circuitry

To convert magnetic excitations into an electrical signal, 50 Ω near field loop antennas can be placed below a dielectric thin film of yttrium iron garnet (YIG) with low damping (see Figure 4.1). The sensing system of the antennas can be placed in such a way that the SWs at higher frequencies propagate to the transducers with the readout circuitry operating at higher frequencies and the SWs at lower frequencies propagate to the lower ones. Similar to the idea published by Papp in [21, Figure 1].

As mentioned in Section 2.3, micromagnetic simulations show that the SWs induce an electrical signal power of -80 to -90 dBm in the transducer [133]. This periodic signal is amplified by a differential LNA. The ultra-wideband mixer converts the amplified signal to lower IFs in the range of $10 - 70$ MHz. In order to realize the conversion, the LO signal is required at the second input of the mixer. The LO signal is generated in the VCO. The PLL controls the frequency of the VCO. Subsequently, the OpAmp with a gain of 60 dB increases the IF signal to voltage values around 100-200 mV. Finally, the amplified and down-converted SW signal can be digitized by an ADC, that provides information about the SWs frequency, amplitude and phase change. The ADC is out of the scope of this thesis and is not described in the following Sections. The evaluation of the simulated frequency, amplitude and phase detection of the SWs is considered at the output of the OpAmp and described in Chapter 5.

4.3 Low Noise Amplifier

4.3.1 General Considerations

The LNA is the most critical part of the whole receiver circuitry regarding the noise contribution. Thus, a careful design is essential for achieving a low NF and consequently to be able to detect relatively low input voltages below $10\,\mu$V. In general, two transistor configurations are commonly used as inputs to the LNAs: *Common Source (CS)* and *Common Gate (CG)* circuits (see Figure 4.2).

On the one hand, the CG provides more accurate and broadband input matching, since the resistance looking into the source of the transistor is equal to the reciprocal of the transconductance g_m. Considering the small signal equivalent circuit of the CG in Figure 4.2c, the input resistance can be derived as shown in Equation 4.1. Subsequently, the $50\,\Omega$ input resistance can be adjusted with an appropriate selection of device dimensions. On the other hand, the CS is better for a lower NF. Depending on the application, if a NF greater than 4 dB is acceptable, than the CG configuration is a better choice [61, p. 293]. In our case, with a targeted NF around 3 dB or lower, the choice for the CS topology is obvious.

$$z_{in} = \frac{v_{in}}{i_{in}} = \frac{-v_{gs}}{-i_{ds}} = \frac{v_{gs}}{v_{gs} g_m} = \frac{1}{g_m} \tag{4.1}$$

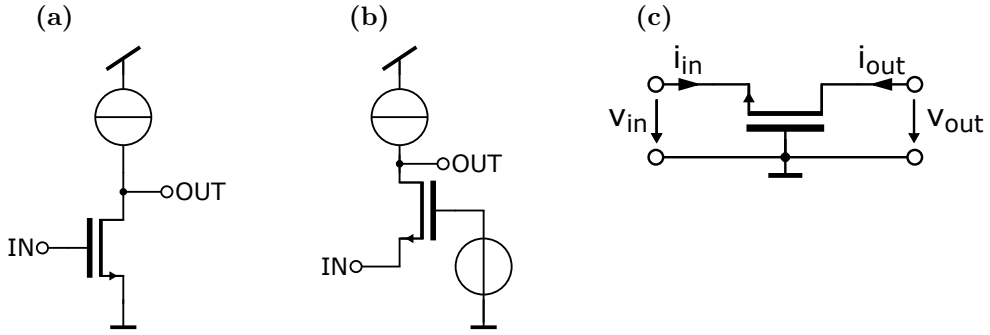

Figure 4.2: (a)Common Source (CS), (b) Common Gate (CG) and (c) the equivalent small signal circuit of the CG. In RF and mmW design the CS is used for a lower NF. For better input matching the CG is a better choice.

As mentioned in Section 4.1, the single-ended LNA was initially considered as a circuit part for the possible realization of the SW readout concept. However, the disadvantage of this topology is its high sensitivity to the parasitic ground inductance [62, p. 387]. It cannot be guaranteed that the ground of the transducer is at the potential as the ground of the source of the input CS transistor or rather at the bottom of the source degenerating inductor. Thus, the performance of the LNA can degrade significantly. Besides, undesirable noise in the signal bandwidth can couple from other building blocks, e.g. VCOs, through the ground plate to the transducer. An alternative is a fully differential LNA. It solves the above mentioned problem since the absolute potential of the sensor is not amplified. The fully differential

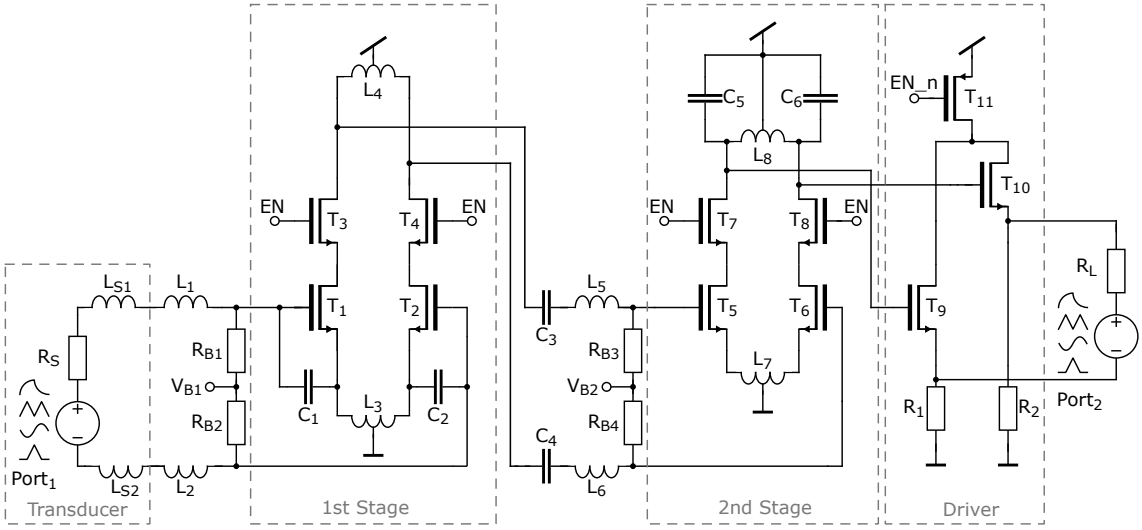

Figure 4.3: Topology of the LNA operating in the frequency range of $9 - 13\,\mathrm{GHz}$. The differential transducer signal is amplified in two stages, which is capacitively coupled with $C_{3,4}$. Each stage is implemented with a common-source and cascode circutiry. The load impedance of the LNA is driven by source followers. EN symbolizes *enable* signal, switching between ground $0\,V$ and supply voltage $1.1\,V$.

LNA also rejects common-mode disturbances [62, 388]. However, the advantages of a fully differential LNA come with an increased power consumption. To keep the NF at the same level, the total current has to be doubled.

4.3.2 Functionality of Implemented Topology

Figure 4.3 shows the topology of the fully differential LNA designed to operate in the frequency range of $9 - 13\,\mathrm{GHz}$. The LNA has two amplifying stages, the transducer model at the input (Port 1) and the impedance converter to drive the output load (Port 2).

Topologies of the LNAs designed for other frequency bands are very similar, except for the values of the electronic devices. In this Section, the function of all circuitry parts is explained and the relevant topological differences of the LNAs operating at frequencies higher than $13\,\mathrm{GHz}$ are mentioned as well. All LNA circuits with the parameter values of the electronic devices can be found in Appendix A.1.

$\mathbf{R_S}, \mathbf{L_{S1}}, \mathbf{L_{S2}}$ Source Impedance: The input of the LNA is the impedance model of the transducer. For all selected frequency bands the same model is assumed, i.e. $R_S = 50\,\Omega$ and $L_{S1,S2} = 12.5\,\mathrm{pH}$. As simulations have shown, the imaginary part of the input impedance is negligible. Consequently, the input matching of the LNA to the real part, equal to $50\,\Omega$, is more relevant. It is worth mentioning, that the LNA can be adopted to other input impedances. However, it is viable for the first approach, to design the LNA for a $50\,\Omega$ input, since most measurement setups are calibrated to a $50\,\Omega$ impedance.

$\mathbf{R_L}$ Load Impedance: The output of the LNA is the input of the mixer. As already mentioned before and explained in more detail in Section 4.4, the designed mixer covers the whole frequency range of $9 - 50\,\text{GHz}$ with a single topology, i.e. the load impedance R_L remains unchanged for all LNAs, operating in different frequency bands. During the design and optimization of the mixer, reasonable performance results have been achieved with an input impedance of the mixer equal to $140\,\Omega$. Thus, the load resistance R_L of the LNA is set to $140\,\Omega$ and the LNA is designed to match this value. Consequently, by connecting the LNA with the mixer, the achieved performance of the mixer remains almost unchanged.

$\mathbf{T_{1-2}}, \mathbf{T_{5-6}}$ Common-Source: CS is a standard circuit in analog design for amplifying the input voltage. Unfortunately, with a standard approach it has no gain at high frequencies (here $9-50\,\text{GHz}$), due to the poles in the transfer function from the load capacitance at the output and the parasitic overlap capacitances between the gate, drain and source nodes. Thus, other techniques, described below, are needed to achieve amplification by means of resonance effect at required higher frequencies. For that purpose, inductors have to be introduced in the circuitry.

$\mathbf{T_{3-4}}, \mathbf{T_{7-8}}$ Cascode Transistors: In the CS circuit the parasitic overlap capacitance between gate and drain produces a feedback between the input and the output nodes. Depending on the dimensions of the electronic devices it produces an input impedance with a negative real part at certain frequencies, i.e. the circuit becomes potentially unstable [61, pp. 266-269]. To overcome this issue cascode transistors can be introduced in order to increase the isolation between input and output [61, p. 284]. The cascode circuit is a combination of the CS with the CG. On the one hand, it improves the stability of the LNA. On the other hand, every additional electronic device, especially at the input of the LNA, contributes to the noise of the circuitry.

$\mathbf{L_3}, \mathbf{L_7}$ Inductive Source Degeneration: Degenerating inductors provide an additional possibility to improve the input matching (S_{11}) of the LNA. Starting from Kirchhoff's Voltage Law (KVL) (Equation 4.2) the small signal input impedance z_{in} is derived in Equation 4.3 [61, p. 284]. Finally, we see that z_{in} contains a real frequency-independent term, allowing better adjustment of the matching parameter S_{11} of the LNA.

$$v_{in} = \frac{i_{in}}{C_{gs} j\omega} + (i_{in} + v_{gs} g_m) L_3 j\omega = \frac{i_{in}}{C_{gs} j\omega} + (i_{in} + \frac{i_{in}}{C_{gs} j\omega} g_m) L_3 j\omega \tag{4.2}$$

$$z_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{C_{gs} j\omega} + L_3 j\omega + \frac{g_m L_3}{C_{gs}} \tag{4.3}$$

Here, C_{gs} stands for the parasitic overlap capacitance between gate and source nodes. g_m symbolizes the small signal transconductance of the transistor T_1. The relevant circuit parts of the LNA are depicted in Figure 4.4.

In order to achieve the best possible symmetry for the differential topology, center tap symmetric inductor has been implemented.

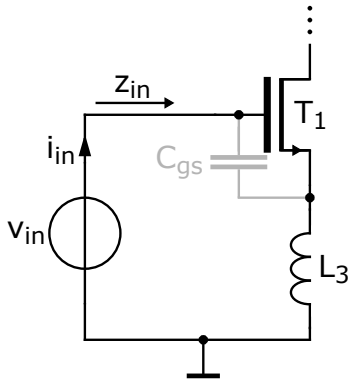

Figure 4.4: CS circuit with parasitic gate-source-capacitance and degenerating inductor. Small letters used for the input parameters mean small signal consideration.

C_{1-2} Increase of Gate-Source-Capacitance: Setting the frequency-independent part $\frac{g_m L_3}{C_{gs}}$ of the input impedance z_{in} (see Equation 4.3) equal to $50\,\Omega$ results in a relatively low value for the inductance L_3. The solution in this case would be to decrease the transistor transconductance g_m, i.e. an increase of the channel length and consequently a degradation of the NF [71]. The second possibility is to increase the gate-source-capacitance by placing an additional capacitor in parallel. [61, p. 285]

L_{1-2}, L_{5-6} Canceling Reactive Component: The input impedance derived in Equation 4.3 contains an imaginary part, that has to be zero for an appropriate input matching [61, p. 295]. Similar to the consideration made for inductive degeneration, we can introduce a serial inductor in the signal path as depicted in Figure 4.5. For the small signal voltage v_{in} and input impedance z_{in} we can write the following Equations

$$\begin{aligned} v_{in} &= i_{in}(L_1 j\omega + \frac{1}{C_{gs} j\omega}) + (i_{in} + v_{gs} g_m) L_3 j\omega, \\ &= i_{in}(L_1 j\omega + \frac{1}{C_{gs} j\omega}) + (i_{in} + \frac{i_{in}}{C_{gs} j\omega} g_m) L_3 j\omega, \end{aligned} \tag{4.4}$$

$$z_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{C_{gs} j\omega} + (L_1 + L_3) j\omega + \frac{g_m L_3}{C_{gs}}. \tag{4.5}$$

Finally, the parameter L_3 introduces an additional degree of freedom that can be treated to achieve a better input matching by finding the values for the electronic devices at the intended frequency, i.e. Equation 4.6 has to be valid.

$$\frac{1}{C_{gs}\omega} = (L_1 + L_3)\omega \tag{4.6}$$

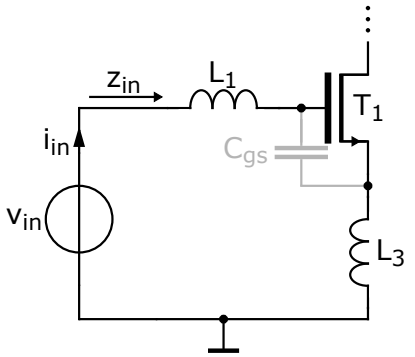

Figure 4.5: CS circuit with parasitic gate-source-capacitance, degenerating inductor L_3 and serial inductor L_1 for canceling the reactive component of the small signal input impedance z_{in}.

L_4, L_8 Inductive Loading: In RF and mmW circuit design it is common to replace resistive loading with inductive loading, as it provides better matching. Consequently, the time constant of the output node is reduced, due to a low inductor serial resistance. Moreover, the voltage headroom is increased for the cascode circuit, due to a low DC voltage drop at the inductor. The load inductors resonate with the total capacitance at the output nodes of each stage, allowing operation at much higher frequencies than with resistive loading. [61, pp. 266-267] To achieve a wider operating bandwidth of the LNA, the resonant frequencies at the output and input nodes have an offset [62, p. 384].

C_{5-6} Capacitive Load Increase: The capacitors C_{5-6} are only inserted in the LNAs operating up to 19 GHz, in order to increase the load capacitance at the output nodes of the second stage. The alternative is to implement a high inductance for L_8 to achieve resonance at the same required frequency. However, to fabricate inductor values higher than 2.5 nH in an IC with an acceptable quality factor is difficult. Besides, the provided inductor models in 40-nm CMOS technology from GlobalFoundries are limited to around 3 nH.

C_{3-4} Capacitive Coupling: The two stages of the LNA are coupled by capacitors, i.e. only high frequency components of the signal can propagate from the first stage to the second stage. This provides flexibility for adjusting the DC operating point of the transistors T_{5-6} and at the same time blocks undesired frequency components coming from the first stage.

T_{9-10}, R_{1-2} Impedance Converter: The *impedance converter* turns the impedance from a high resistive node to a low resistive node. The main drawback of the implemented circuit is the attenuation of the LNA gain. Depending on the operating frequency of the LNA the gain degrades by approximately 10 dB. However, the direct connection of the mixer to the output of the LNA's second stage reduces the gain of the stage as well. To create the above mentioned 140 Ω source impedance for a proper operation of the mixer, the impedance conversion is required. Moreover, this driver at the LNA output additionally isolates the mixer from the LNA, i.e. the LO-RF feedthrough of the mixer is suppressed.

$\mathbf{R_{B1}}, \mathbf{R_{B2}}$ Bias Resistors: Biasing is indispensable for adjusting the DC operating point of the transistors. Thus, it is important to have stable bias voltages over the whole operating temperature range and a resilience against supply voltage variations. Here, the bias voltage sources V_{B1} and V_{B2} are assumed to be ideal. However, the commonly used in IC design bandgap voltage references can be applied. Another possibility is the implementation of a current source with reduced Process, Voltage supply and Temperature (PVT) variation [74]. Bear in mind, that large enough resistor values for R_{B1} and R_{B2} have to be selected to avoid attenuation of the input signal and to minimize the equivalent noise current [62, p. 384].

$\mathbf{T_{3-4}}, \mathbf{T_{11}}$ Switches: The gates of the cascode transistors T_{3-4} are connected to the *enable* signal, i.e. during the operation period of the LNA, the gates are connected to the supply voltage $V_{DD} = 1.1\,\mathrm{V}$ and in the off-time to the ground 0 V. The same consideration holds for the Positive-Channel Metal-Oxide-Semiconductor (PMOS) transistor T_{11} with the inverted enable signal. Switching off the power supply of some building blocks obviously reduces the power consumption of the whole IC system. Additionally, the parasitic interconnect coupling to other circuits is reduced.

So far, the building blocks of the LNA operating in the frequency range $9 - 13\,\mathrm{GHz}$ has been explained. The schematics for other frequency bands are very similar, however the dimensions of the electronic devices are different. The sizes of the inductors and capacitors are reduced in order to shift the resonant frequency to higher values. The width of the transistors is reduced resulting in a lower DC power consumption.

To achieve a voltage gain greater than 26 dB, LNAs with 2 stages were sufficient as proven by the simulation results in Chapter 5. However, at the frequency band $39 - 50\,\mathrm{GHz}$ an additional stage was required to achieve a reasonable gain. The schematic of the LNA operating in $39 - 50\,\mathrm{GHz}$ is depicted in Figure 4.6. The third stage is identical to the second one and increases the resonance effect at frequencies around 50 GHz.

4.3.3 Recommended Publications

Fritsche [75] demonstrates an LNA with 3 dB bandwidth from 54.5 to 72.5 GHz. Details on the layout and considerations on the interconnects in case of mmW circuits are reported. A 2-stage cascode LNA is used as a topology.

A 3-stage Ultra-Wideband (UWB) LNA operating in $30 - 50\,\mathrm{GHz}$ is reported by Yang [76].

Another UWB LNA is presented by Seo [77]. The bandwidth of $18 - 32\,\mathrm{GHz}$ is achieved with 4 amplifying stages. Here, an unconventional approach with current-reuse is taken for the second and third stage of the LNA.

Kim [78] analyzes inductive peaking techniques for a transmitter. However, the ideas and insights can also be used for receiver circuits. Design methodologies for finding optimal inductive peaking structures are described.

A receiver front-end operating at $75 - 91\,\mathrm{GHz}$ is outlined by Khanpour [79]. The

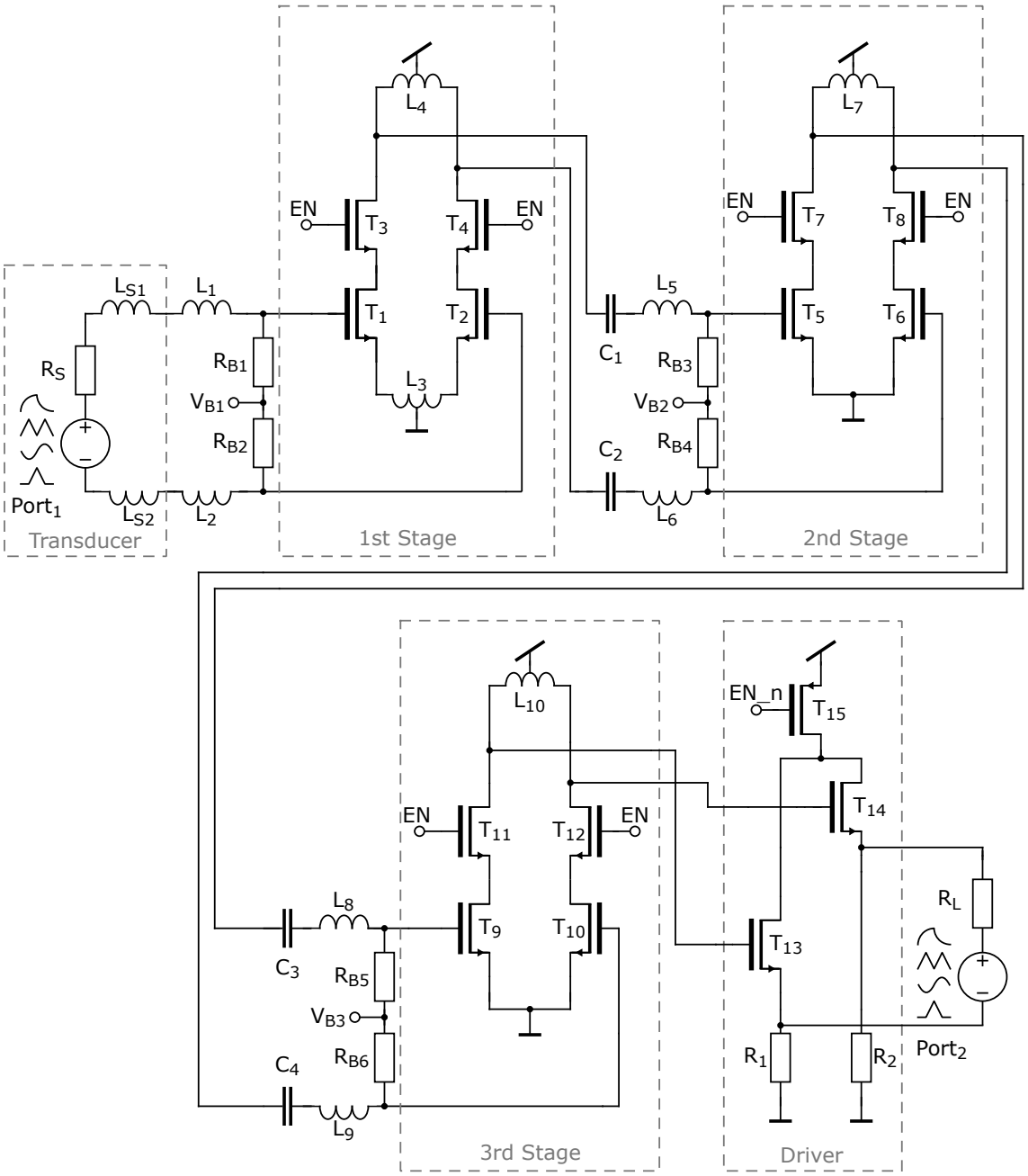

Figure 4.6: Schematic of the LNA operating in the frequency range of $39 - 50\,\mathrm{GHz}$ with the input signal picked up by an on-chip near field loop antenna. The LNA contains 3 amplifying stages in order to achieve a reasonable high voltage value for the RF input of the mixer (Port 2). Each stage consists of a cascode Common Source (CS) circuit with inductive loading. The first stage exhibits the inductive source degeneration L_3 needed for the $50\,\Omega$ input matching.

3-stage cascode LNA, as a first receiver circuit part, is described in-depth. An interesting approach is taken by replacing the commonly used degenerating inductors at the gate and source of the input transistor by a transformer, promising higher a

gain and a lower NF.

A useful approach to improve the NF and the gain at lower frequencies is described by Belostoski [72, 80–82]. The insertion of an LC-element between the common-source and the cascode transistors is introduced.

Noise optimization techniques, published by Goo [83], minimize the NF of the LNA, especially if something else than 50 Ω source impedances are allowed for the receiver input.

Some useful noise and power matching design techniques are also published by Nguyen [84].

4.4 Mixer

4.4.1 General Considerations

The mixer is a part of the on-chip readout circuitry for SW characterization. In general, it converts the signal from higher to lower frequencies or from lower to higher frequencies. For the SW readout a down-converting mixer is used. It shifts the high frequencies of tens of GHz to relatively lower frequencies in the MHz range. The down-conversion is realized by multiplying two input signals, RF and LO, in the time domain, i.e. convolution in the frequency domain. The resulting IF signal has two frequency components, one at lower frequencies and the second at higher frequencies, if two ideal sinusoidal signals are applied at the RF and IF inputs. Equation 4.7 reflects this working principle of the mixer [62, 405]

$$A\cos(\omega_1 t)B\cos(\omega_2 t) = \frac{AB}{2}[\cos((\omega_1 - \omega_2)t) + cos((\omega_1 + \omega_2))t]. \tag{4.7}$$

In general, down-converting mixers can be categorized into *single* or *double* balanced and into *active* or *passive*. While an active mixer has a conversion gain, the passive mixer has a conversion loss. The single balanced mixer has differential/balanced LO input and single RF input. While for the double balanced mixer both input RF and IF are differential/balanced. [61, pp. 348-349]

The double-balanced mixer results from an appropriate connection of two single-balanced mixers. The simplified topology of the two single-balanced mixers is depicted in Figure 4.7. Due to the small signal voltage v_{RF}^{+} is equal to $-v_{RF}^{-}$, the mixed voltages at the nodes A_1 and B_1 are equal to the negative voltages at the nodes A_2 and B_2. Thus, we can write $v_{A_1} = -v_{B_1} = -v_{A_2} = v_{B_2}$ which allows to short the nodes A_1 with B_2 and B_1 with A_2 [61, pp. 369-370]. The resulting parallel connection of two resistors results in a resistance of $\frac{R}{2}$, i.e. one resistor can be skipped.

The advantage of the double-balanced mixer is the fact that the odd harmonics of the LO signal, appearing at the mixer's output in the single-balanced case, are removed [62, p.417]. In the single-balanced mixer the undesired odd harmonics of the LO signal are mixed with the DC bias current. Due to the symmetry of the

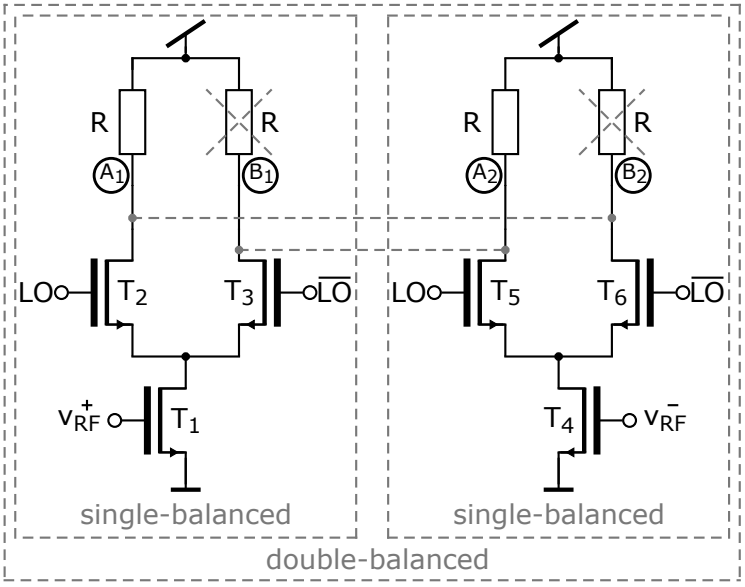

Figure 4.7: Topology of the double-balanced mixer as a combination of two single-balanced variants. The small signal voltage v_{RF}^{+} is equal to the negative voltage of v_{RF}^{-}. Consequently, for the double-balance configuration nodes A_1 can be connected with B_2 and B_1 with A_1. LO and $\overline{\text{LO}}$ represent complementary Local Oscillator (LO) signals.

double-balanced mixer, this distortion appears at both output nodes IF^{+} and IF^{-} and is consequently canceled out by considering the differential signal IF.

4.4.2 Functionality of Implemented Topology

The design topology of the realized UWB Gilbert cell down-conversion active mixer is presented in Figure 4.8. The parameter values of the electronic devices can be found in Appendix A.2 Figure A.8. The mixer covers the whole targeted frequency range $9 - 50\,\text{GHz}$. As can be seen, a double-balanced mixer is used. Compared to a single-balanced mixer, the critical LO-RF feedthrough of the double-balanced mixer decreases significantly because the port-to-port coupling appears at positive and negative IF nodes simultaneously. However, the absolute difference of the desired signal between IF^{+} and IF^{-} nodes is not affected. [61, pp. 348-349]

$\mathbf{R_{RF}}, \mathbf{R_{LO}}, \mathbf{R_{IF}}$ Source and Load Resistances: Both source resistances R_{RF} and R_{LO} are selected to have a reasonable conversion gain and NF. They do not have to be equal to $50\,\Omega$. It is essential, that the output of the LNA has the same impedance as the RF source impedance of the mixer. Consequently, the performance of the mixer is not influenced after connecting it with the LNA.

The load resistance R_{IF} is equivalent to the connected OpAmp. It is selected in such a way that the performance of the mixer remains almost unchanged, no matter the port or the OpAmp is connected.

$\mathbf{R_{B1-B2}}$ Bias Resistors: The DC operating points of the transconductance transistors $T_{4,5}$ and the switching transistors T_{6-9} are adjusted by the bias voltages V_{B1}

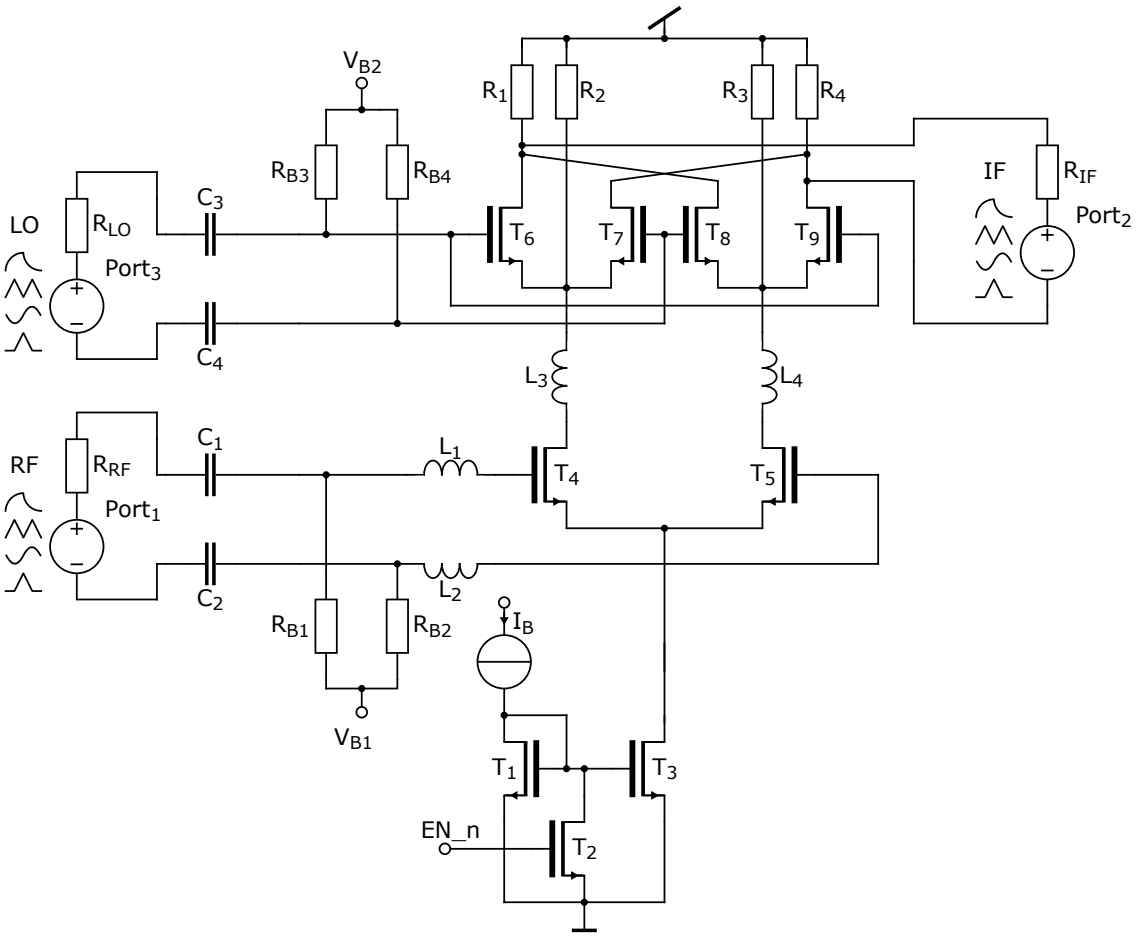

Figure 4.8: Topology of the double balanced Gilbert cell mixer, operating in the frequency range $9 - 50\,\text{GHz}$. The Radio Frequency (RF) signal is down-converted to the Intermediate Frequency (IF) signal by multiplication with the Local Oscillator (LO) signal. The topology is extended with inductors to achieve a better conversion gain and NF performance at around $30 - 50\,\text{GHz}$.

and V_{B2}, respectively. The direct connections to the gate of the transistor would create a short between differential nodes. Thus, the resistors R_{B1-B4} are required with large enough values to avoid RF and LO signal's deterioration. As already mentioned in Section 4.3, ideal sources are used for the bias voltage. However, a widely used bandgap voltage reference circuit can be implemented to have a stable bias voltage source for the mixer.

C_{1-2} Capacitive Signal Coupling: To separate the DC operating point of the LNA output nodes from the mixer's input nodes, the RF signal is capacitively coupled to the mixer. The capacitors C_{1-4} and resistors R_{B1-B4}, forming high pass RC filters, are sized according to the desired bandwidth of the mixer. A change of their parameter values is a trade-off between filtering out undesired low frequency components ($< 9\,\text{GHz}$) of the input RF signal and achieving an appropriate conversion gain, as well as a better NF of the mixer at lower operating frequencies ($9 - 20\,\text{GHz}$).

$T_{1,3}$ Bias Current with Current Mirror: The bias current provided by transistor T_3 is realized with a simple bias network consisting of an ideal current source I_B and a current mirror $T_3 : T_1$. The bias network can be extended to a circuit with a high robustness against process-voltage-temperature variations [74, 85] in case of an on-chip biasing. Alternatively, the current of I_B can be supplied from outside the chip by providing an additional pad.

$L_{1,2}$ RF Serial Inductors: The inductors L_1 and L_2 from Figure 4.8 are often used to match the input impedance to an appropriate real value by canceling reactive components [86–88]. This approach also improves the NF and conversion gain of the mixer [62, p. 421]. The values of the inductors were chosen to place the resonance frequency at approximately 40 GHz, in order to increase the conversion gain and improve the NF at high frequencies ($30 - 50$ GHz).

$L_{3,4}$ Interstage Inductors: To increase the conversion gain and decrease the NF at high frequencies ($30 - 50$ GHz), additional inductors $L_{3,4}$ are placed between the transconductance transistors $T_{3,4}$ and the switching transistors T_{5-8} [86, 87]. The interstage inductors compensate for the parasitic capacitances at the nodes between the drain of the transconductance transistors and the switching pairs. The LC resonance at these nodes contributes to the peaking of the conversion gain at higher frequencies [88].

$T_{4,5}$ Transconductance Transistors: As the name already indicates, the transistors operate as a voltage-to-current converter. To understand the mixing effect from a mathematical point of view, we consider a simplified version of the single-balanced mixer depicted in Figure 4.9. For the small signal drain-source current of the transistor T_3 follows Equation 4.8

$$i_{RF} = g_m v_{RF} = g_m a \cos(\omega_{RF} t). \tag{4.8}$$

Here, an ideal sinusoidal signal with the amplitude a is assumed for the RF input voltage.

T_{6-9} Switching Transistors: The switching quad transistors steer the converted RF current to the IF^+ or IF^- nodes. In Figure 4.9 the complementary switching transistors are symbolized with T_1 and T_2. Combined with Equation 4.8 for the currents I_1 and I_2 follow

$$I_1 = g_m v_{RF} S(t), \tag{4.9}$$

$$I_2 = g_m v_{RF} S(t - \frac{T_{LO}}{2}), \tag{4.10}$$

with T_{LO} the time period of the LO signal and $S(t)$ the unit-amplitude square wave function with values between 0 and 1.

$R_{1,4}$ Load Resistors: Resistors $R_{1,4}$ in Figure 4.8 form passive loads for the differential output of the mixer. They convert the mixed current back to a voltage.

Now, considering a simplified version of the mixer in Figure 4.9 and applying KVL it follows

$$V_{IF} = RI_2 - RI_1 = Rg_m v_{RF}[S(t - \frac{T_{LO}}{2}) - S(t)]. \tag{4.11}$$

The difference of the square wave functions can be replaced by a sign function and approximated by the fundamental component of the appropriate Fourier series [89, p. 1020]. Finally, for the output voltage, the following applies

$$V_{IF} = Rg_m v_{RF}\text{sgn}(\cos(\omega_{LO}t)) \approx Rg_m a\cos(\omega_{RF}t)\frac{4}{\pi}\cos(\omega_{LO}t). \tag{4.12}$$

Forming the multiplication of the cos functions in Equation 4.12 similar to Equation 4.7 shows that the mixer has low and high frequency components. The undesired high frequency part can be filtered out.

$$V_{IF} = \frac{2}{\pi}Rg_m a[\cos((\omega_{RF} - \omega_{LO})t) + \cos((\omega_{LO} + \omega_{RF})t)] \tag{4.13}$$

The above described derivation of the IF voltage demonstrates the working principle of the mixer [61, pp. 370-371]. It shows, how the periodic RF and LO signals are multiplied and how the down-converted IF signal at the mixer output is generated.

$R_{2,3}$ Current Injection/Bleeding : Resistors $R_{2,3}$ serve as current injection for transistors $T_{4,5}$ and guarantee that they remain in the saturation region during the

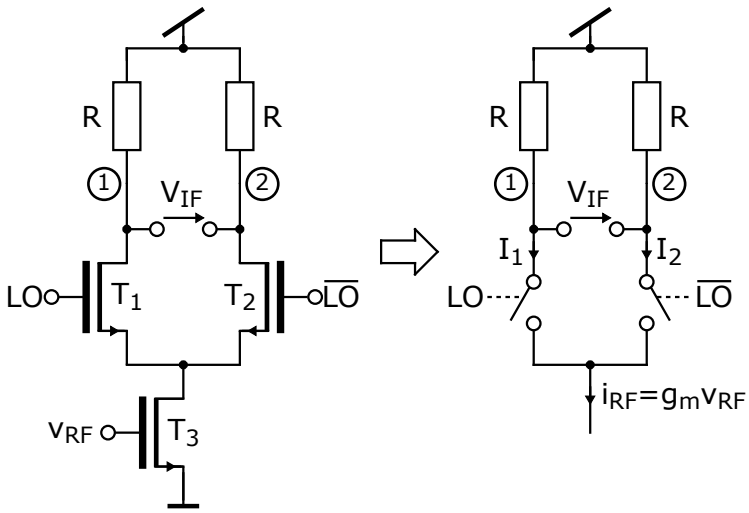

Figure 4.9: Simplified single-balanced mixer. Transistor T_1 and T_2 are replaced by two complementary switches. Transistor T_3 generates a small signal current $g_m v_{RF}$. The output IF voltage results from the multiplication of the RF current and square wave switch functions.

switching process of the transistors T_{6-9} [90]. It is a widely used technique to improve the conversion gain, the NF and the linearity of the mixer [87].

T_2 Switch: As previously mentioned the designed mixer covers the whole frequency range $9 - 50\,\text{GHz}$ with a single topology. However, there are 6 designs for the LNAs operating at different frequencies. To get the best chip area yield, a multiplexer has to be implemented between the LNA and the mixer. Unfortunately, such a multiplexer diminishes the RF signal significantly. The alternative is to connect one mixer to each LNA, which consumes more area, but delivers much better performance. In order to switch off currently unused mixers, the switch is realized with transistor T_2, pulling the gate voltage of the transistor T_3 to the ground.

4.4.3 Recommended Publications

Concluding the mixer Section, the reader is referred to read the following relevant publications. Kolios [87] shows simulation results of a 60 GHz Gilber cell mixer with extended topology. The interstage inductors between transconductance transistors and switching transistors are used for improving the NF and the conversion gain of the mixer. Besides, adjustable conversion gain versus bandwidth is proposed by variation of the gate voltage of the current bleeding transistors.

Zijie [88] proposed the mixer operating in $1 - 10$ GHz with crossed-coupled CG stage to achieve wideband input matching. Besides, the interstage inductors for conversion gain boosting are used, similar as in [86, 87].

A mixer covering an extremely high frequency range from $33 - 103\,\text{GHz}$ uses the distributed topology [91]. However, it has rather a conversion loss than a conversion gain.

Interesting approaches are demonstrated by Darabi [92] and Cheng [93] using a negative impedance, typically implemented in oscillators, in the current injection path of the mixer. The technique demonstrates the reduction of the flicker noise at lower frequencies.

Very similar Gilber cell mixers without using inductors are presented by Tsai [94] and Lin [90] covering $25 - 75\,\text{GHz}$ and $9 - 50\,\text{GHz}$, respectively.

Chang [95] demonstrated a folded Gilbert cell mixer with two PMOS transconductance transistor in addition to the standard NMOS ones. The mixer, operating in $0.2 - 16\,\text{GHz}$, shows a reduced power consumption.

As part of a $75 - 91\,\text{GHz}$ receiver front-end a Gilbert cell mixer is presented by Khanpour [79]. To achieve reasonable performance at such a high frequency, serial inductors in every path of RF and LO domain have been used.

4.5 Voltage Controlled Oscillator

4.5.1 General Considerations

The VCO is an indispensable part of RF and mmW receivers. In order to convert the RF signal to IF, the mixer requires the LO signal, that is generated by the VCO. In general, there are two types of VCOs: *ring oscillator* and *LC oscillator*. On the one hand, the ring oscillator consumes less chip area and is usually easier to design. On the other hand, the LC oscillator can operate at higher frequencies. Both types have been implemented and are described below.

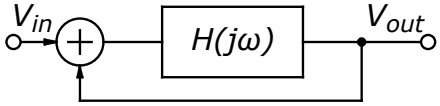

Figure 4.10: Feedback system with the transfer function $H(j\omega)$ and unity feedback gain. The subtraction of the output signal from the input means 180° phase shift of the output signal.

The VCO can be represented as a circuit with a feedback loop, depicted in Figure 4.10. It has to fulfill the Barkhausen criteria (see Equation 4.14) in order to be able to oscillate at the certain frequency ω_{osc} [96, p. 608].

$$\begin{aligned} |H(j\omega_{osc})| &\geq 1 \\ \angle H(j\omega_{osc}) &= 0^\circ \end{aligned} \tag{4.14}$$

Here, it is important to note, that the above conditions are necessary but not sufficient [97]. Thus, in practice the loop gain is typically chosen at least twice as required in order to compensate for temperature and process variations [96, p. 608].

The desired $9 - 50\,\text{GHz}$ range for the SW characterization cannot be covered by a single VCO topology. Thus, the frequency has been split in 6 bands (see Section 5.3). The first two designs are realized with ring oscillators, covering $9 - 13\,\text{GHz}$ and $13 - 19\,\text{GHz}$. The remaining frequency part is implemented with LC oscillators. Besides, all VCO topologies provide differential output signal LO. As described in Section 4.4, a double-balanced mixer has better conversion gain, less noise and less port-to-port feedthrough compared to a single-balanced one. Thus, to provide the required LO signal to the mixer, the VCO needs the differential outputs LO^+ and LO^-. The parameter values of the VCO topologies presented below can be found in Appendix A.3.

4.5.2 Functionality of Implemented Topologies

4.5.2.1 Ring Oscillator

The topology of the designed ring oscillator operating in the frequency range $9 - 13\,\text{GHz}$ is depicted in Figure 4.11. One of the possibility to adjust the oscillat-

ing frequency is defined by the odd number n of the inverter stages (see Equation 4.15) [98, p. 339].

$$f_{osc} = \frac{1}{n(t_{pLH} + t_{pHL})} \qquad n = 3, 5, 7, 9, ... \tag{4.15}$$

Here, the assumption of equal inverter stages is made. The parameters t_{pLH} and t_{pHL} denote the propagation delay time from low-to-high and from high-to-low, respectively. The highest frequency is achieved by selecting the minimum number of stages equal to 3. A ring oscillator with only one stage can not be realized due to an insufficient phase shift of 90°.

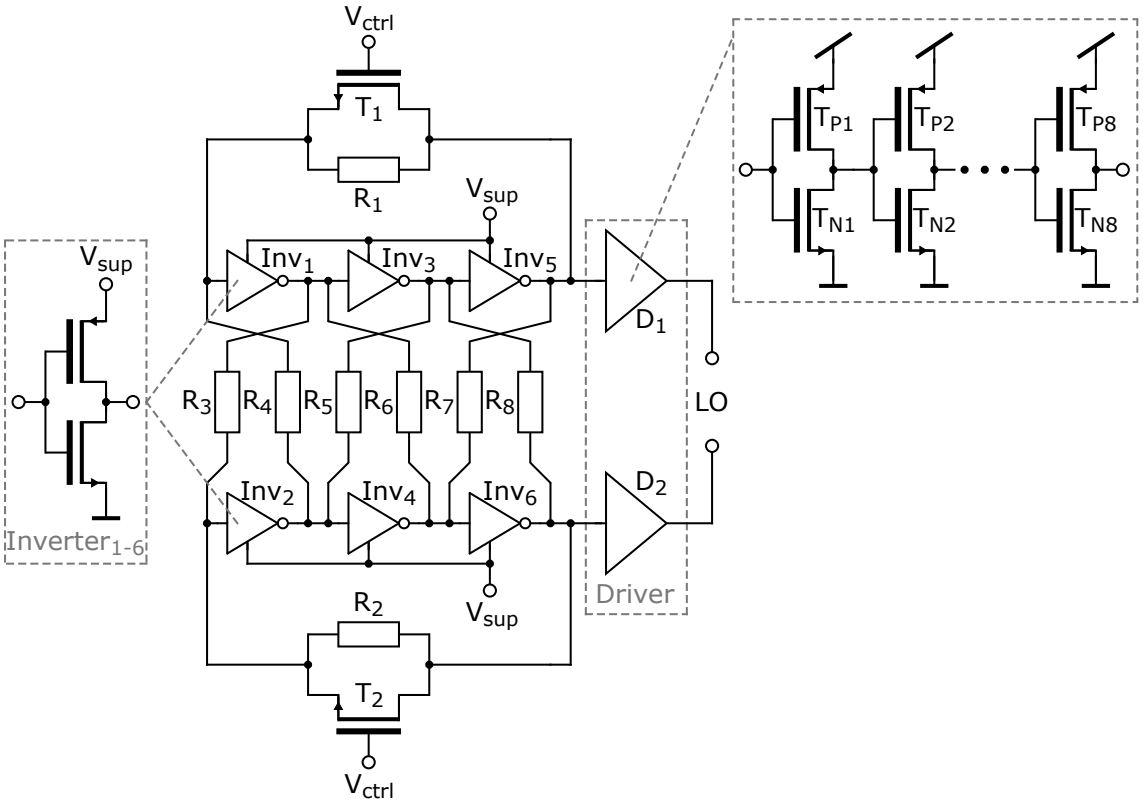

Figure 4.11: VCO operating in frequency range of $9 - 13$ GHz. The schematic includes the differential ring oscillator with three stages, the delay element in the feedback path, phase balancer resistors between two ring oscillators and the drivers at the output decoupling the oscillator from the load capacitance of the followed circuitry.

$\mathbf{Inv_{1-6}}$ Inverter: The inverter stage is build with PMOS and Negative-Channel Metal-Oxide-Semiconductor (NMOS) transistors for pulling the signal up and down, respectively. For understanding the oscillation of the ring oscillator we consider the simplified model depicted in Figure 4.12. For the small signal analyses we can write the transfer function $H(\omega)$ as follows [96, p. 610]

$$H(\omega) = -\frac{A}{1 + \frac{s}{\omega_0}}, \tag{4.16}$$

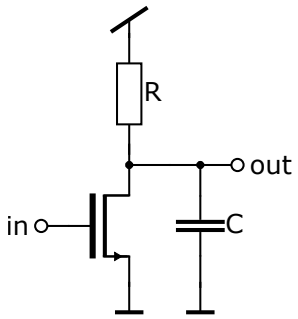

Figure 4.12: Simplified model of the inverter stage at the beginning of the oscillation. The input and the output are considered as small signal voltages.

with the amplification factor A. The minus sign takes the inversion of the signal into account. The load capacitance C introduces a pole in the transfer function at the frequency ω_0. Besides, for the frequency dependent phase shift $\phi(\omega)$ between the input and the output signals Equation 4.17 is applied [96, p. 610].

$$\phi(\omega) = \arctan\left(\frac{\omega}{\omega_0}\right) \tag{4.17}$$

Here, we can see, that the maximum phase shift of one inverter stage is equal to 90° at the frequency equal to infinity, i.e. at least three inverter stages are required to bring the ring VCO to an oscillation. Finally, for the total transfer function of the three inverter stages we write

$$H(\omega) = -\frac{A^3}{(1+\frac{s}{\omega_0})^3}. \tag{4.18}$$

Considering the Barkhausen criteria for the phase shift in Equation 4.14 and with an assumption of equally designed inverter stages, the phase shift of each stage has to be equal to 60° at the oscillating frequency ω_{osc}. Here, we have to consider the additional 180° phase shift, due to the inversion of the signal. Hence,

$$\arctan\left(\frac{\omega_{osc}}{\omega_0}\right) = 60° \quad \Rightarrow \quad \omega_{osc} = \sqrt{3}\omega_0. \tag{4.19}$$

Applying the resulted oscillating frequency ω_{osc} from Equation 4.19 into Equation 4.18 the minimum amplification of a single inverter stage results in

$$\frac{A^3}{\left(\sqrt{1+(\frac{\omega_{osc}}{\omega_0})^2}\right)^3} \geq 1 \quad \Rightarrow \quad A \geq 2. \tag{4.20}$$

The above statements show the oscillation conditions of the equal inverter stages with equal load capacitance at each stage. However, it is obvious that the especially load capacitance of the last stage is not equal to the first or to the second one. Thus, there is a trade-off between increasing the width of the inverter transistors

for lowering load resistance on the one side and decreasing the width of the same transistors for lowering the load capacitance of the previous stage on the other side.

At that point, it is important to note, that the above considerations have been made for the small signal analysis with linear functions. It shows, how the ring oscillator starts to oscillate whereas the signal changes are small enough in the beginning. After a certain period of time, if Barkhause criteria are filled, the voltage changes become large and the circuitry cannot be linearized at one single operating point any more. Finally, the voltage amplitude grows until each output node of the ring oscillator stages experience nearly rail-to-rail switching. Consequently, the oscillating frequency changes to

$$f_{osc} = \frac{1}{3(t_{pLH} + t_{pHL})}. \tag{4.21}$$

As depicted in Figure 4.11, the supply node of the inverters is not connected to V_{DD}. The supply voltage V_{sup} offers an additional possibility for coarse frequency tuning. For instance, with lower supply voltage less current is provided to charge and discharge the load capacitances at the inverter outputs. Consequently, the propagation delay from high to low t_{pHL} and from low to high t_{pLH} increases, i.e. the oscillating frequency f_{osc} decreases (see Equation 4.21).

$\mathbf{R_{3-8}}$ Phase Balancer: To realize the differential output signals LO^+ and LO^- with the phase shift of 180°, the resistors have been implemented between both ring oscillators in a cross configuration, as depicted in Figure 4.11. It allows charge transport between both ring oscillators in a way that the inverter inputs of the first oscillator are connected to the inverter outputs of the second one and vice versa. However, a closer look at the phase balancer resistors reveals that two serial resistors generate a feedback loop of two neighboring inverter stages. Thus, the values of the phase balancer resistors have to be high enough to prevent a latching.

$\mathbf{T_{1-2}}, \mathbf{R_{1-2}}$ Controllable Delay Element: The fine tuning of the oscillating frequency is realized by changing the on-resistances between drain and source of the transistors T_1 and T_2 (see Figure 4.11). For this purpose the control voltage V_{ctrl} has to be changed. As describe more detailed in Section 4.6, the control voltage is adjusted by the PLL circuitry. Additionally, the resistors R_1 and R_2 are inserted in parallel to the drain and source contacts of the transistors T_1 and T_2, respectively. The reason for this insertion is to keep the oscillation even if the control voltage V_{ctrl} decreases to 0 V.

The controllable delay element presented in Figure 4.11 shifts the whole frequency operating range to lower frequencies. Thus, it was difficult to cover the second frequency band $13 - 19$ GHz with this approach, as simulations in Cadence have shown. Consequently, another topology, depicted in Figure 4.13, was used. Here, the feedback path connects directly the output of the ring oscillator with the input. The delay element for frequency fine tuning is introduced with current starving technique, i.e. the insertion of the transistor T_C in the inverter stage. The frequency

is adjusted by the control voltage V_{ctrl}. The resistor R_C prevents the interruption of the oscillation in case V_{ctrl} decreases below the threshold voltage of the transistor T_C.

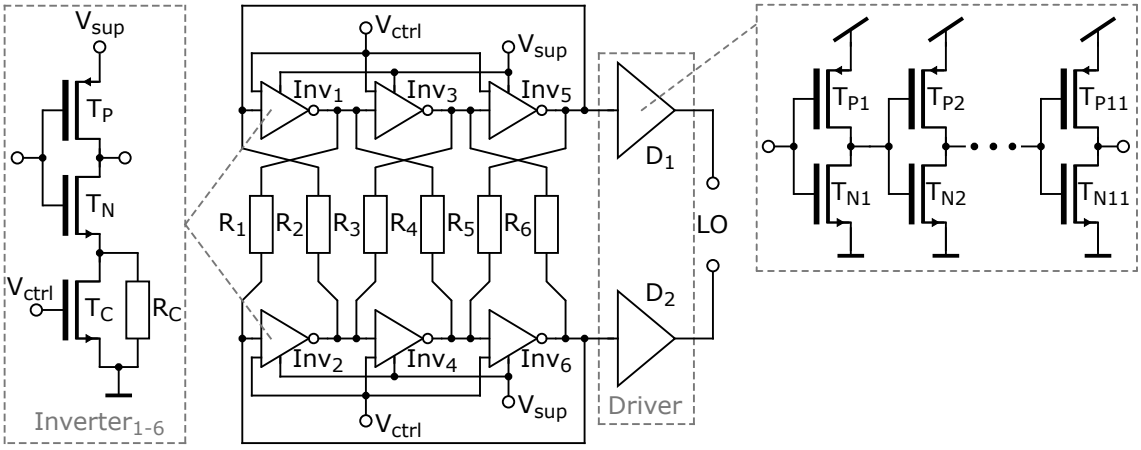

Figure 4.13: VCO operating in the frequency range $13 - 19\,\text{GHz}$. The topology is very similar to the design depicted in Figure 4.11. The difference is in the implementation of the delay element for frequency fine tuning, in order to achieve higher operating frequencies. Besides, the number of inverter stages in the drivers are higher for the same reason.

D_{1-2} Driver: The driver is a crucial part of the VCO to drive the capacitive load resulted by the inputs of the mixer and the frequency divider. Otherwise the oscillator could not operate at the desired frequency or oscillate at all. To drive a relatively large capacitive load at high frequencies, high enough current has to be provided, i.e. larger gate width of the transistors. However, the increased transistor size means larger capacitive load for the previous stage. Thus, it is counterproductive to use only one or two driver stages especially for RF VCOs. As depicted in Figures 4.11 and 4.13, eight and eleven driver stages have been implemented, respectively, in order to drive the mixer and the frequency divider.

4.5.2.2 LC Oscillator

In the previous section, the oscillator based on negative feedback system, having positive feedback at the oscillating frequency, has been considered. Here, the resonator based LC oscillator targeted to operate at higher frequencies is described.

We start with the topology operating in frequency range $39 - 50\,\text{GHz}$ (see Figure 4.14), due to easier understanding of the functional principle. Afterwards, based on these consideration, the extension in the schematic designed for $19 - 26\,\text{GHz}$ is explained. The remaining circuits, covering $26 - 39\,\text{GHz}$, have the same topology as $19 - 26\,\text{GHz}$ design, however with different parameter values. All VCO schematics including parameter values can be found in Appendix A.3.

T_{1-2} Cross-coupled transistors: A closer look at the cross-coupled transistors in Figure 4.14 reveals two in series connected CS circuits with a feedback loop from the output to the input. A simplified and redrawn circuit is depicted in Figure 4.15a.

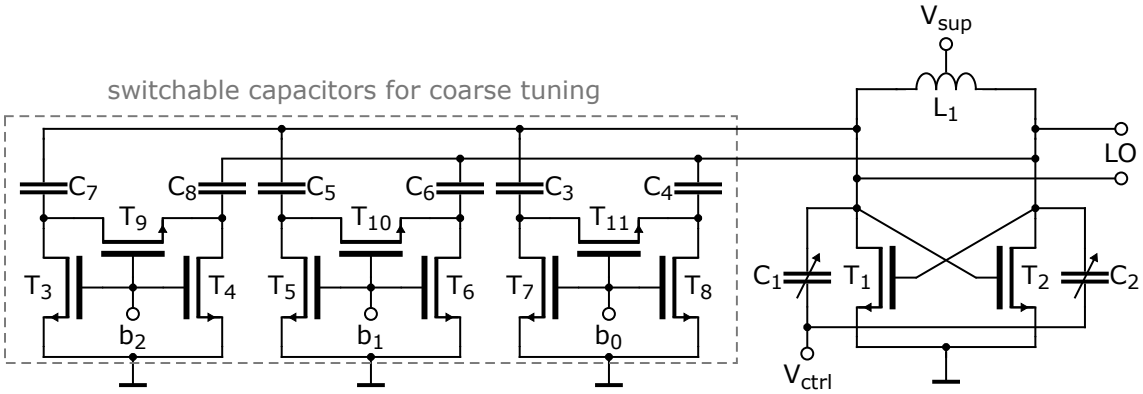

Figure 4.14: VCO operating in the frequency range $39 - 50\,\mathrm{GHz}$. The inductor and the capacitors at the LO output nodes build the core of the circuit. Crossed-coupled transistors generate a negative resistance to cancel out parasitic resistance of the LC block. Fine tuning of the frequency is made by control voltage V_{ctrl}. The coarse frequency tuning is adjusted by binary coded switches b_{0-2}.

In order to oscillate, the circuit has to fulfill the Barkhausen criteria mentioned in Equation 4.14, i.e. the phase shift of the circuitry has to be 0° or 360° and the loop gain greater than 1.

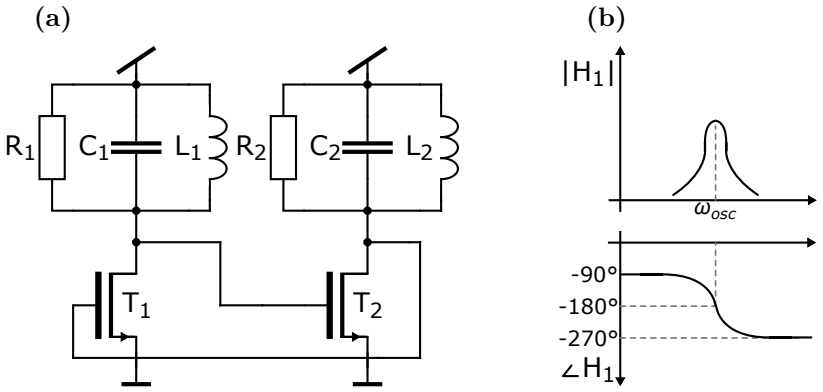

Figure 4.15: Simplified version of the LC oscillator (a) and the sketched gain and phase of the transfer function for the first stage. The cross-coupled transistors can be considers as two amplifying stages with a feedback loop. R_1 and R_2 represent equivalent parallel resistances at the resonant frequency ω_{osc} of the LC tanks. The required 180° phase shift per stage occurs at the resonance frequency ω_{osc}. [61, pp. 512-513]

At lower frequencies inductor L_1 from Figure 4.15a is dominant as load of the first stage. Thus, for the transfer function we can approximate [61, p. 512]

$$H_1(j\omega) = \frac{V_{out1}}{V_{in1}} \approx -g_{m1} \cdot j\omega L_1, \tag{4.22}$$

with the transconductance g_{m1} of the transistor T_1. Thus, the phase shift at lower

frequencies is equal to $-90°$. At the resonance frequency ω_{osc} the transfer function of the first stage is equal to

$$H_1(j\omega) = \frac{V_{out1}}{V_{in1}} = -g_{m1}R_1, \tag{4.23}$$

with equivalent resistance R_1 at the resonant frequency. It also means a phase shift of $-180°$ (see Figure 4.15b). At higher frequencies the load capacitance generates additional phase shift to $-270°$. Consequently, to achieve $360°$ phase shift at the resonance frequency, two stages can be cascaded. The adequate gain greater than 1 can also be achieved at the oscillating frequency ω_{osc} (see Equation 4.23. [61, pp. 512-513]

The main purpose of the cross-coupled transistor T_{1-2} is to cancel out the lossy part of the resonator, in order to prevent the attenuation of the oscillation. In order to achieve this, a negative resistance have to be created parallel to the oscillator tank. The standard LC oscillator with parasitic resistance R_p at the resonance frequency is depicted in Figure 4.16. Here, the negative resistance R_x created by cross-coupled transistors have to be $-R_p$ and consequently, $R_p||(-R_p) = \infty$ [96, p. 627]. To derive the resistance R_x we can write

$$i_x = g_{m1}v_{gs1} = g_{m1}(v_{gs2} - v_x) = g_{m1}(\frac{-i_x}{g_{m2}} - v_x), \tag{4.24}$$

$$i_x(1 + \frac{g_{m1}}{g_{m2}}) = -g_{m1}v_x. \tag{4.25}$$

With equally sized cross-coupled transistors, we have $g_{m1} = g_{m2} = g_m$ and for the resistance R_x follows

$$R_x = \frac{v_x}{i_x} = -\frac{2}{g_m}. \tag{4.26}$$

Hence, to keep the oscillation, it is necessary $R_p \geq \frac{2}{g_m} = |R_x|$. Above considerations are made for small-signal analysis. If $|R_x|$ falls below R_p, the oscillator generates large swings permanently switching off one of the cross-coupled transistors, i.e. degradation of the transconductance g_m and therefore increasing $|R_x|$. On average R_x remains equal to $-R_p$ in case of appropriately sized dimensions of the electronic devices. [96, p. 628]

L_1 Center-tapped resonance inductor: The key component of the LC oscillator is undoubtedly the inductor, responsible for the oscillation together with the node capacitors. In order to achieve as low as possible mismatch of the load inductors, instead of using two of them, one center-tapped inductor is implemented.

Here, it is important to note, the supply voltage of LC oscillator operating in $39 - 50\,\text{GHz}$ is not connected to the V_{dd} equal to $1.1\,\text{V}$. Otherwise, the voltages at the output nodes LO^+ and LO^- would exceed significantly the $1.1\,\text{V}$ and could

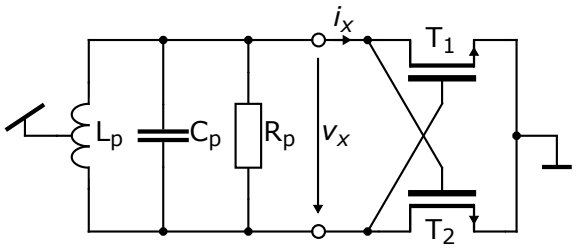

Figure 4.16: LC oscillator with equivalent parasitic resistance R_p at the resonance frequency. The cross-coupled transistors T_{1-2} generate a negative resistance in order to cancel out the lossy part of the tank.

cause damage of the transistors T_{1-2}. The generated peak voltages going above the supply voltage are caused by the induction in L_1. Hence, to avoid the stress for the transistors, the supply voltage has been reduced to 0.8 V (see also Figure A.16 in Appendix).

C_{1-2} Fine frequency tuning capacitors: The fine frequency tuning is adjusted by Metal-Oxide-Semiconductor (MOS) capacitors C_{1-2} (see Figure 4.14), i.e. the drain, the source and the bulk of the MOS transistor are connected together, building a capacitance to the gate node. Here, it is important to keep in mind, to place the device in a separated well, in order to isolate the control voltage node from the substrate of the chip. Besides, the connection of the gate node to the oscillating nodes is recommended, to avoid additional capacitive loading due to the junction between the n-well and the substrate [61, p. 519].

The control voltage V_{ctrl} can be varied between 0 and 1.1 V in order to have high or low capacitor values, respectively (see simulation results in Section 5.3). With an increased voltage drop on the varactor, the depletion or inversion of the region below the gate can be considered as increase of the distance between the plates of a capacitor. Hence, with the lower control voltage V_{ctrl} the capacitance increases. The mentioned dependence between the control voltage and the change of the capacitance is applied for high frequencies [99, p. 206]. However, in our case, all LC oscillators operate above 25 GHz, i.e. the frequency is high enough.

C_{3-8} Coarse frequency tuning capacitors: With the fine frequency tuning, described above, a frequency range around 2 GHz can be covered by sweeping the control voltage between gnd and V_{dd}. To cover larger frequency range around 10 GHz with single design, the discrete capacitors C_{3-8} have been implemented as depicted in Figure 4.14. The size of the capacitors is selected in a way that there are no blind zones in the frequency by switching between 8 possible switching states, i.e. there is always overlap in the frequency by increasing or decreasing to the next frequency range.

T_{3-8} Switches: The switches for the coarse frequency tuning are realized with simple transistors, digitally controlled by the binary coded nodes b_{0-2}. For setting the highest or the lowest frequency the signal b_{0-2} have to be equal to 000 or 111, respectively. The drawback of the transistor switches is the non-negligible on-resistance, degrading the quality factor of the oscillator tank [61, p. 534]. The

solution could be the increase of the transistors gate width. However, it increases the total capacitance at the LO output nodes, even if the transistors are switched off. Consequently, the frequency fine tuning range would diminish. Hence, the dimensions of the transistors T_{3-8} (see Figure 4.14) are set to the minimum sizes (see Figure A.16 in Appendix). This effect also limits the number of the implemented unit capacitors for the frequency coarse tuning. [61, pp. 534-535]

T_{9-11} Reducer of the switch's on-resistance: The problem regarding the on-resistances of the implemented switches described above can be solved by placing additional switch transistor T_{9-11} as depicted in Figure 4.14. Due to the differential operation of the VCO, the Alternating Current (AC) currents flowing for instance through the unit capacitors C_{3-4} are differently directed, i.e. the insertion of the transistor T_{11} do not influence the operating principle of the VCO. However, the on-resistances of the switches can be nearly halved. [61, p. 535]

For the VCO designs covering together the frequency range from 19 to 39 GHz, an additional component part has been inserted (see Figure 4.17). Two cross-coupled PMOS transistors connected between the V_{dd} and the output LO can be considered as two-stage amplifiers with the feedback loop, similar to the NMOS transistors described above. A closer look at the circuitry reveals two inverter stages with the feedback loop. The question arises, why should the topology depicted in Figure 4.17 be able to oscillate and a normal ring oscillator with two inverter stage not (see Section 4.5.2.1. The reason is, that the conventional ring oscillator has the required phase shift of 360° at the frequency near zero. However, the schematic proposed in Figure 4.17 has the required phase shift at the oscillating frequency ω_{osc}, which can be adjusted by the device parameters (see also Figure 4.15).

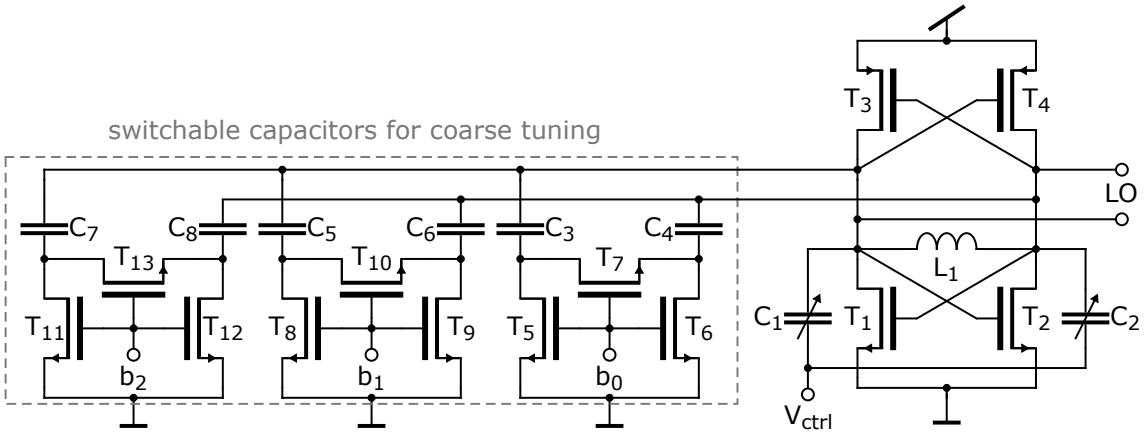

Figure 4.17: VCO designed to operate in the frequency range of $19 - 26$ GHz. The topology is very similar to the schematic presented in Figure 4.14. Here, cross-coupled PMOS transistor are implemented, to set the common-mode voltage of the LO output nodes to the half of the supply voltage V_{dd} and consequently, to use the full control voltage range to adjust oscillating frequency [61, p. 530].

The advantage of the VCO with additional cross-coupled PMOS transistors is the ability to use the full control voltage range between gnd and V_{dd}, in order to vary the

oscillating frequency [61, p 530]. Besides, the PMOS transistors avoid the output nodes LO^+ and LO^- increase above the supply voltage. Consequently, the reliability of the cross-coupled transistor T_{1-2} does not suffer [61, pp. 514-515]. Finally, it also means no additional supply voltage levels are required, as in the case of the VCO designed for the frequency range from $39 - 50\,\text{GHz}$.

4.5.3 Recommended Publications

The VCOs presented before have all an analog input voltage to control the frequency change in fine steps. Dalt shows an exampled of a digitally controlled oscillator with 1.03 MHz per one Least Significant Bit (LSB) operating at the center frequency 10 GHz [100], i.e. a digital PLL can be used to lock the frequency of the VCO. The achieved tuning range is 10 GHz. The topology could be used for narrow-band analyses of the SW. Alternatively, the circuitry can be extended with larger unit capacitors for coarse frequency tuning. However, it hast to be kept in mind, that additional components could significantly deteriorate the performance.

Schober and Choma [101] demonstrated a $0.8 - 28.2\,\text{GHz}$ differential ring oscillator based VCO fabricated in 40 nm CMOS process. The adjustment of the frequency is realized with current starving technique for fine tuning. For the coarse frequency tuning, a phase-coupled capacitor bank is used. The VCO is part of the PLL demonstrated in [102].

An influence of the commonly used bias current for cross-coupled LC oscillators is analyzed by Levantino [103]. It shows that the phase noise performance becomes better without the tail current generator.

4.6 Phase Locked Loop

The VCO described in previous Section, can be considered as one part of a PLL. Theoretically, the VCO can operate without the PLL. However, the frequency accuracy of a fabricated IC becomes better with the PLL, due to the self controlling mechanism for the frequency locking [61, p. 597]. The components of a typical PLL are depicted in Figure 4.18.

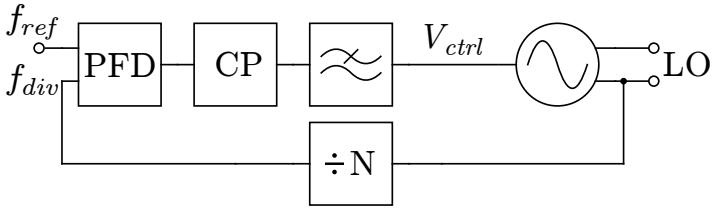

Figure 4.18: PLL building blocks: Phase Frequency Detector (PFD), Charge Pump (CP), Loop Filter (LF), Voltage Controlled Oscillator (VCO) and frequency divider. The feedback configuration allows to lock the LO frequency by a required multiples of the reference frequency f_{ref}.

Depending on the input control signals of the VCO, the LO signal with required oscillating frequency is generated. The frequency divider brings the signal to lower

frequency f_{div}. The PFD compares the divided signal with the reference one. In case of difference, up or down pulses are generated at the output of the PFD, which control the CP circuitry. Consequently, the CP generates current pulses, that are forwarded to the LF. Finally, the control voltage V_{ctrl} stabilizes the oscillating frequency f_{osc} dependent on set reference frequency f_{ref}. All mentioned building blocks of the PLL are described below. The functionality of the VCO is presented in Section 4.5.

4.6.1 Frequency Divider

It is not feasible to operate digitally clocked circuitry till 50 GHz with the state of the art CMOS technology. Same applies for the used 40 nm CMOS technology. Thus, to be able to control the oscillating frequency in the PLL with the PFD and the CP, the LO frequency is divided by factor of 128 to the lower frequencies, which is in the range of the reference clock $100 - 300$ MHz.

There are different approaches to divide the LO frequency. However, for the SW readout circuitry the primary focus is to be able divide the LO signal frequency of $5 - 50$ GHz. Here, the True Single-Phase Clocking (TSPC) divider and the Static Frequency Divider (SFD) topologies are considered, designed for the lower frequencies ($5 - 13$ GHz) and higher frequencies (up to 50 GHz), respectively.

4.6.1.1 True Single-Phase Clocking Divider

The TSPC dynamic logic has been initially introduced by Ji-Ren [104] and extended by Yuan [105]. The schematic of the TSPC divider is depicted in Figure 4.19. Similar to the standard edge-triggered D-Flipflop with a feedback, used to divide the clock frequency by factor of 2, the TSPC divider performs this function with dynamic logic.

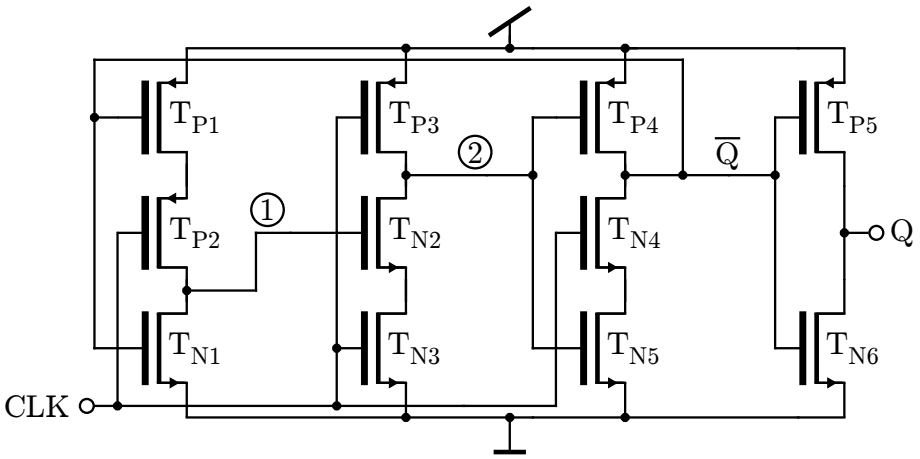

Figure 4.19: True Single-Phase Clocking (TSPC) frequency divider. The input clock signal CLK propagates to the output Q resulting in the frequency division by factor 2. The dynamic logic technique is used to achieve high frequency operations till 18 GHz.

For easier understanding the operating principle of the TSPC divider, the transient simulation results of the input and output nodes as well as of the inter-stage nodes $1, 2$ and $\overline{Q}$ are depicted in Figure 4.20. Before the detailed consideration of the signals flow in the TSPC divider, analyzed below, the general operating principle can be described with the following few sentences. Only at the rising edge in the clock signal the logical input signal $\overline{Q}$ is transfered to the inverted output of the flipflop (here $\overline{Q}$ as well). Subsequently, the next rising edge of the clock is required to propagate the inverted input signal to the output. Consequently, the output signal Q oscillates with the half of the frequency compared to the input clock signal.

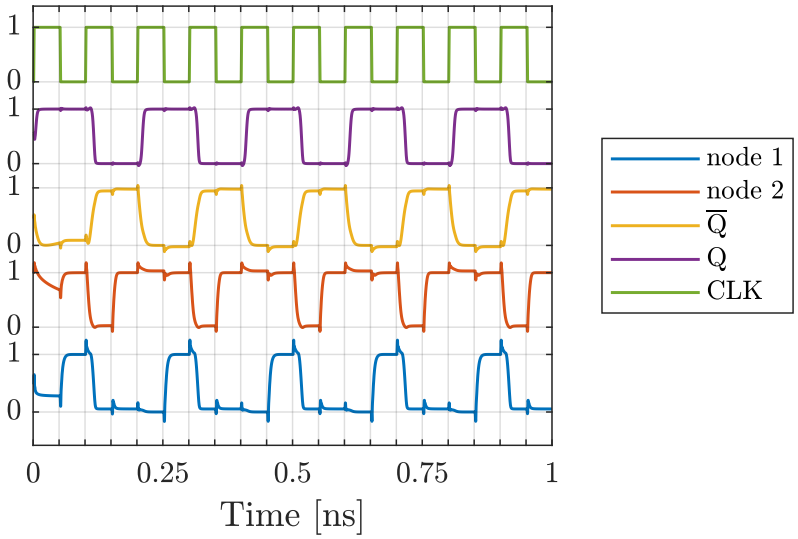

Figure 4.20: Transient simulation results of the TSPC divider with assumed clock frequency of 10 GHz. The voltage levels of the input and output nodes as well as the inter-stage nodes are normalized to the logical values 0 and 1. The observable small picks in the inter-stage node signals result from the parasitic capacitive coupling between the input and output of the respective stage.

- $\mathbf{CLK = 0 \nearrow 1; \overline{Q} = 0}$: With the rising edge of the clock signal the PMOS transistor T_{P2} is turned off and the node becomes floating with the logical value 1. Thus, the node 2 is going to be discharged through the NMOS transistors T_{N2} and T_{N3}. Consequently, the inverted output signal $\overline{Q}$ takes the logical value 1, i.e. the previously charged node 1 becomes 0. From now on, the transistor T_{N2} is turned off and the node 2 saves previous state equal to logical value 0.
- $\mathbf{CLK = 1 \searrow 0; \overline{Q} = 1}$: The falling edge of the clock signal results in the node 2 changes its state from 0 to 1. However, due to the turned off transistor T_{N4} the inverted output $\overline{Q}$ keeps its value by 1.
- $\mathbf{CLK = 0 \nearrow 1; \overline{Q} = 1}$: The next rising edge of the clock signal turns on the transistor T_{N4} and with the previously saved 1 at the node 2, i.e turned on transistor T_{N5}, the inverted output $\overline{Q}$ is going to be discharge to the ground. Due to the turned off PMOS transistor T_{P2} the node 1 keeps the previous values at 0.

- **CLK** $= \mathbf{1} \searrow \mathbf{0}; \overline{\mathbf{Q}} = \mathbf{0}$: Now, the second falling edge at the clock signal turns on the transistor T_{P2}. It connects the node 1 with the supply voltage V_{DD}. For the next action the first described step can be considered again.

The observation of the clock signal CLK and the inverted output signal $\overline{Q}$ in the above described 4 steps reveals the frequency of the output is the half of the input. The last stage of the divider topology in Figure 4.19 is a simple inverter, correcting the output signal of the divider and decoupling it from the load of the following circuitry.

The advantage of the TSPC divider is a relatively low power consumption, due to now static current flowing path from the supply voltage to the ground. However, for a proper operation a rail-to-rail input is required. Besides, as for all dynamic logic circuitries the minimum operating frequency has to be applied to keep the stored value in the latch. [61, pp. 697-698]

4.6.1.2 Static Frequency Divider

The Static Frequency Divider (SFD) is designed to divide the LO signal frequency from the range $13-50\,\text{GHz}$ to the frequencies lower than $18\,\text{GHz}$, in order to provide the signal to the TSPC divider. The schematic of the SFD is depicted in Figure 4.21. The circuitry contains two master slave D-latches, that alternated clocked with opposite-phase clock signals. The D-latch has three transistor pairs: *tracking* pair T_{N1-N2}, *latching* pair T_{N3-N4} and *clocking* pair T_{N5-N6} (see Figure 4.21b).

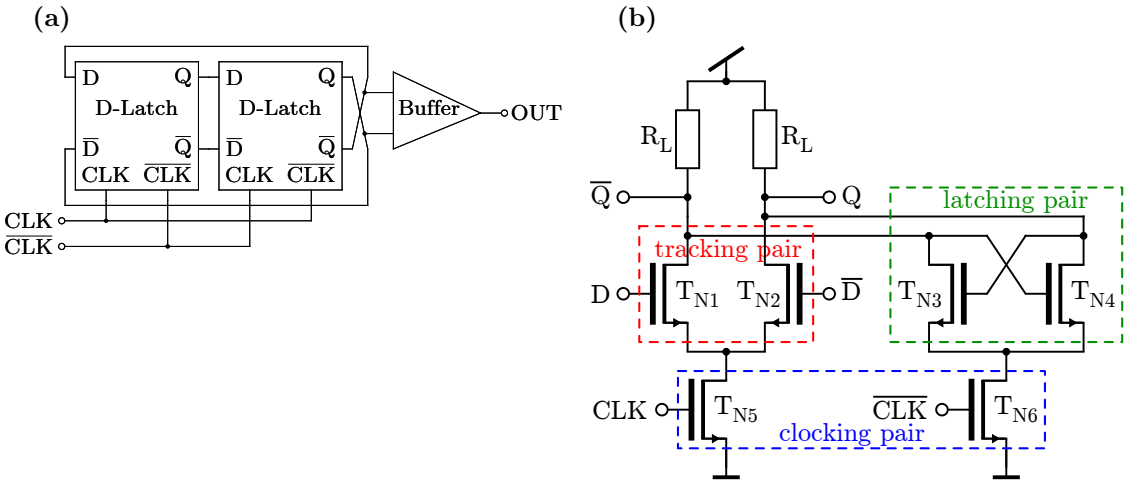

Figure 4.21: Static Frequency Divider (SFD) by factor 2 designed for the frequency range $18-40\,\text{GHz}$. The divider is realized by two alternated clocked D-latches (a). The transistor level schematic of the D-latch (b) contains the tracking, latching and clocking transistor pairs. The dimensions of the electronic devices are provided in Appendix Figure A.18.

The dimensioning of the tracking pair and the clocking pair depend on desired output swing and targeted power consumption. To find the optimum dimensions of the latching pair, the width ration of latching and tracking transistors have been

swept from $\frac{1}{16}$ to 1. Simulation results confirm the proposal of Cheema [106] the ration of $\frac{5}{8}$ as good trade of between speed and output swing.

The tracking pair is sensing the differential input signal $D - \overline{D}$, during the high phase of the clock signal CLK. The clocking pair operates as switches between the tracking and the latching pair. Besides, the clocking pair is dimensioned in way to provide the tail current. Thus, the circuitry can be classified into Current Mode Logic (CML) [107]. Both resistors R_L provide the resistive load for the output nodes Q and $\overline{Q}$. During the low phase of the clock signal the latching pair is active, i.e. the sensed signal D is saved at the output node Q. The second latch is opposite clocked to the first one. Thus, during the low phase of the clock the input signal is sensed and during the high phase it is latched. Consequently, two cycles of the clock are required to propagate the signal D of the first latch to the output Q of the second latch, i.e. dividing the clock frequency by factor of 2. The signal Q of the second latch is connected to the input $\overline{D}$ of the first stage and vice versa, in order to sustain the periodicity of the required signal. [108, p. 69]

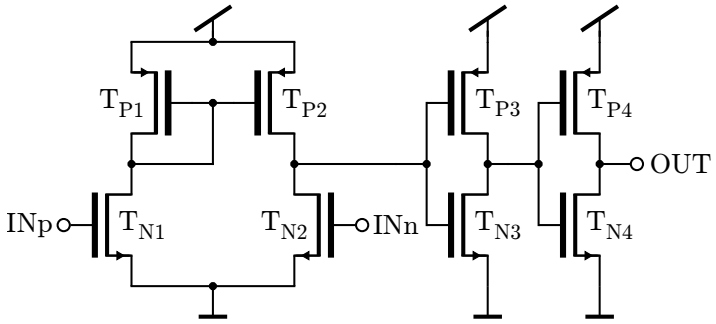

Figure 4.22: SFD divider buffer from the block diagram in Figure 4.21a. The circuitry includes differential comparator followed by two inverter stages. The dimensions of the circuitry are shown in Appendix Figure A.19.

In order to increase the amplitude of the output signal and to be able to drive the following circuitry, a buffer for the divider is required. The schematic of the buffer is shown in Figure 4.22. The differential input is converted by the current mirror transistor $T_{P1,P2}$ to the single output required for the TSPC divider, presented in previous Section 4.6.1.1.

The SFD schematic, described above, is used for the frequencies of the readout circuitry till 39 GHz. The limitation comes from the RC-time constant for charging and discharging the output nodes Q and $\overline{Q}$. It is also a trade-off between a low time constant for higher speed and a larger resistance for more gain of the tracking pair.

In order to achieve the division factor of four, two SFD dividers are used. They are connected in series with adjusted transistor dimensions and an addition buffer between both dividers. The circuitry with the electronic device dimensions is depicted in Appendix Figure A.20. The operating principle is the same, as described above.

To cover the remaining operating frequencies till 50 GHz, the inductive loading is

applied for the SFD divider (see Figure 4.23). Considered in the frequency domain, the introduction of the inductance generates a zero in the transfer function, that widens the operating frequency of the divider. From the time-domain prospective, the inductance increases the output impedance of the tracking pairs with increasing frequency. Consequently, it compensates for the decreasing impedance, resulted from the parasitic load capacitances at the output node. Due to serial connection of the resistors R and the center-tap inductor L, a high quality factor of the inductor is not necessary. [108, pp. 71-72]

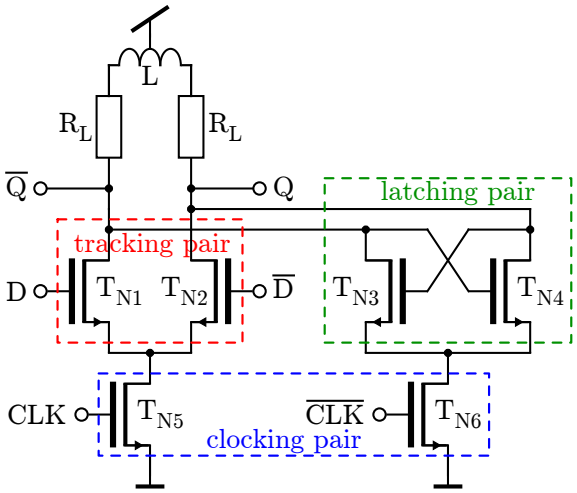

Figure 4.23: D-latch of the SFD operating till 50 GHz. The inductive loading is introduced to compensate for the capacitances at the output nodes Q and $\overline{Q}$. The whole circuitry of the SFD with parameter values of the electronic devices is attached in Appendix Figure A.21.

4.6.2 Phase Frequency Detector

The simplest implementation of a Phase Detector (PD) is an Exclusive Or (XOR) gate. In case of a phase difference of two periodic square wave signals, a logic 1 at the output is generated, that can be used to adjust the frequency of a VCO. The operating principle of the XOR gate as PD is described more detailed in [61, pp. 597-600]. The main drawback of the XOR gate PD, to use the topology for the SW readout circuitry, is inability to detect the frequency difference $f_{ref} - f_{div}$ between the reference and the divided signals. To be able to lock the LO signal with XOR gate PD its input signals' frequencies f_{ref} and f_{div} should be in same region [61, p. 611]. Thus, a PFD is required, that is able to correct simultaneously the phase and the oscillating frequency in a reasonable frequency range.

Instead of using the standard PFD [61, pp. 612-614], a design with dynamic logic is implemented. First, it was introduced by Kim [109] and a modified version proposed by Anushkannan [110]. The schematic of the dynamic PFD is depicted in Figure 4.24. The topology reduces the dead zone compared to the standard PFD, i.e. the resolution of the detectable phase difference between the reference and the divided LO signals is increased.

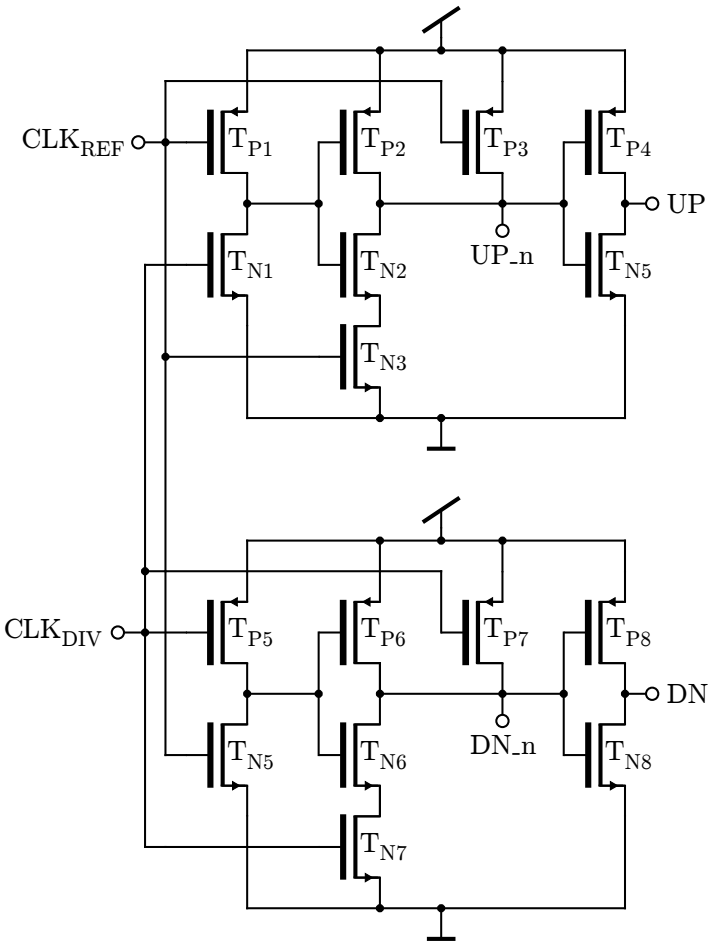

Figure 4.24: Topology of the implemented Phase Frequency Detector (PFD) operating in dynamic logic. Depending on the difference of the divided LO signal $\mathrm{CLK_{DIV}}$ and the reference clock $\mathrm{CLK_{REF}}$, the up and down pulses at the output are created to adjust the phase and the frequency of the VCO.

To understand the general working principle of the designed PFD, Figure 4.25 exemplary shows the curves of the input $(\mathrm{CLK_{REF}}, \mathrm{CLK_{DIV}})$ and output $(\mathrm{UP}, \mathrm{DN})$ signals. The circuitry detects rising edges of the both clock signals and generates up and down pulses for the charge pump, described in Section 4.6.3. The width of the pulses is equal to the time slot, when both clock signals are unequal.

To verify the functionality of the PFD (see the schematic in Figure 4.24), we consider the generation of the up pulses. The circuitry is build symmetrically, i.e. the down pulses are generated similar. The below described cases are also demonstrated in Figure 4.26.

- $\mathbf{CLK_{REF} = 0; CLK_{DIV} = 0}$: A digital signal 0 at the reference clock induces a logic 1 at the node UP_n, due to the open path to the supply voltage through the PMOS transistor T_{P3} and the closed path to the ground through the NMOS transistor T_{N3}, i.e. in all cases, as long as the reference clock is logical 0, the up pulses cannot be generated and the node UP is always at logical signal 0.

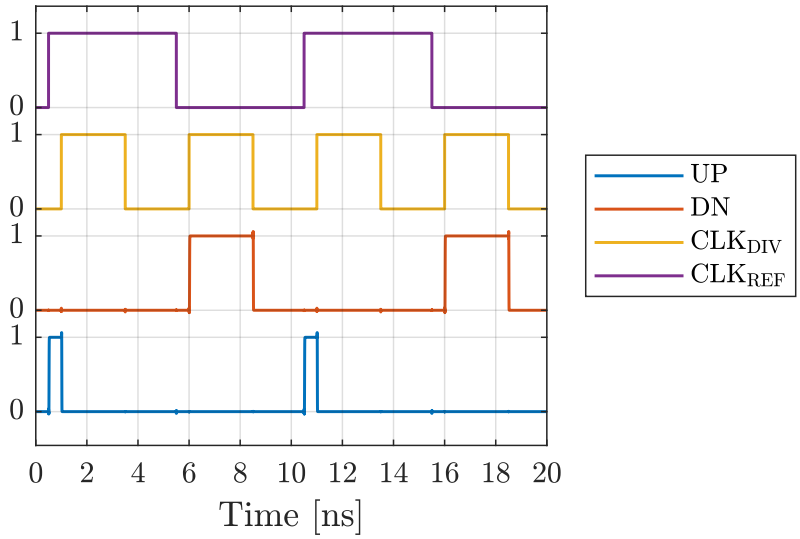

Figure 4.25: Input and output signal of the PFD (see schematic in Figure 4.24). If at the rising edge of $\mathrm{CLK_{DIV}}$ there is a difference to the reference clock, then the down pulse DN is generated. Equivalently, the up pulse UP is generated at the rising edge of the reference signal $\mathrm{CLK_{REF}}$.

Besides, both input signals at the logical signal 0, drive the output node of the transistors T_{P1} and T_{N1} to a logical 1.

- $\mathbf{CLK_{REF} = 1; CLK_{DIV} = 0}$: The rising edge of the reference clock closes the PMOS transistors T_{P1}, T_{P3} and opens the NMOS transistor T_{N3}. Consequently, the output node of the transistors T_{P1} and T_{N1} becomes floating. Due to the logical 1 at this node from the previous state ($\mathrm{CLK_{REF}} = 0; \mathrm{CLK_{DIV}} = 0$), the NMOS transistor T_{N2} is open. Thus, the node UP_n is discharged to ground and the up pulse at the output of the PFD is created. In general, it has to be kept in mind that the dynamic logic requires a minimum clock frequency for a proper operation. Otherwise, the floated nodes can be undesirably discharged due to the parasitic leakage current.
- $\mathbf{CLK_{REF} = 1; CLK_{DIV} = 1}$: At the rising edge of the divided LO signal $\mathrm{CLK_{DIV}}$ the NMOS transistor T_{N1} discharges the previously mentioned floated node to 0 V. Consequently, the node UP_n is charged to the supply voltage through the PMOS transistor T_{P2}. Finally, the previously generated up pulse goes back to the logical 0 value again.

4.6.3 Charge Pump

The task of the CP is to convert the up and down pulses, generated in the PFD, into control voltage, required for the frequency adjustment in the VCO. The implemented topology of the CP for the SW readout circuitry is depicted in Figure 4.27. The schematic was proposed by Schober [102]. Compared to the conventional CP topologies [111–113], the proposed CP consumes significantly less power, requires only 6 minimum-sized transistors and does not need the matching of the current mir-

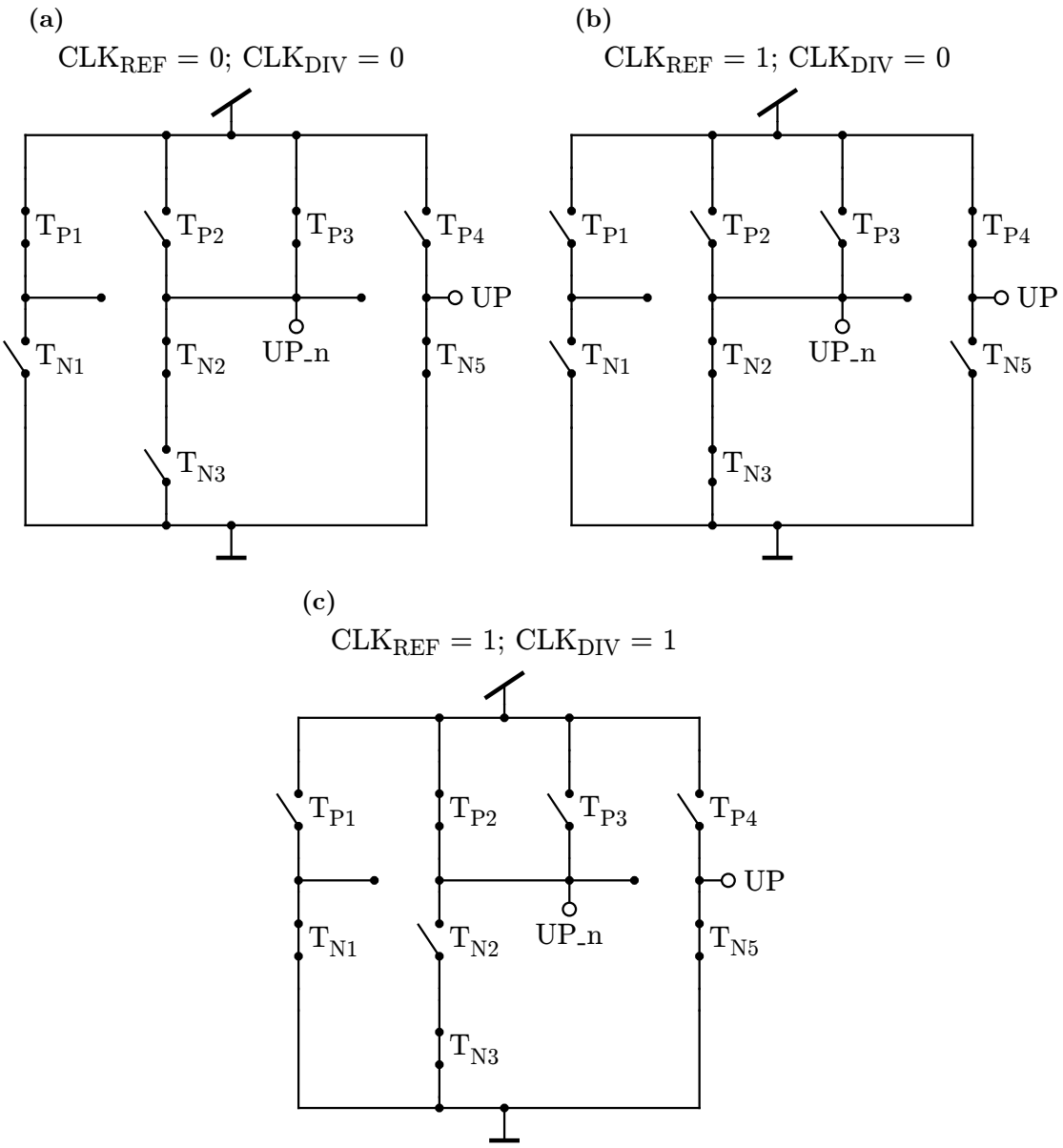

Figure 4.26: Demonstration of the operating principle of the PFD, presented in Figure 4.24. Three different states are considered, depending on the logical values of the reference clock $\mathrm{CLK_{REF}}$ and the divided LO signal $\mathrm{CLK_{DIV}}$. The transistors are replace by ideal switches.

rors. The 3 operating modes of the CP are depicted in Figure 4.28 and described more detailed below.

In **idle mode** the switches T_{N1} and T_{P1} are closed, as depicted in Figure 4.28a. At the same time, the transmission gate switches $T_{N2,N3}$ and $T_{P2,P3}$ are open. The idle mode of the CP is targeted for two different purposes. First, it is used to recharge the capacitor $\mathrm{C_1}$ to the supply voltage V_{DD} between up and down modes. Second, during the locked period of the PLL the control voltage V_{ctrl} is held at a constant value V_{ctrl0}. [102]

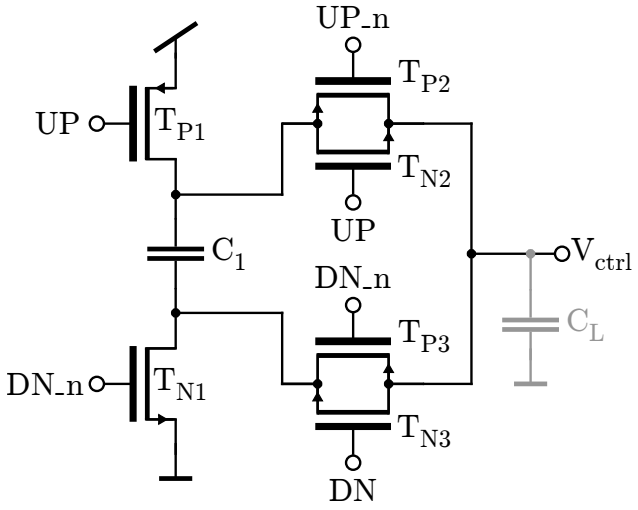

Figure 4.27: Charge Pump (CP) converting digital up and down pulses of the PFD (see Figure 4.24) into the analog control voltage V_{ctrl}. The charge transport from the supply to the output node is realized through the capacitor C_1. The gray marked capacitor C_L represents the load capacitance at the output node, resulted from the loop filter (see Section 4.6.4).

Compared to the conventional CP topologies [111–113], the proposed schematic uses a switched capacitor operating principle, i.e. there is no static current flow between supply and ground. It significantly improves the power efficiency. The dynamic power consumption can by estimated by Equation 4.27 [102]

$$P_{CP,dyn} \approx \alpha f_{REF} C_1 V_{DD}. \tag{4.27}$$

with activity factor α in the range from 0 to 1. The reference frequency f_{REF} varies between $100 - 300\,\text{MHz}$. The capacitance C_1 should be chosen high enough so that the parasitic capacitances of the transistors become negligible [102]. The capacitance C_1 is set to 100 fF (see Figure A.23 in Appendix). Consequently, with supply

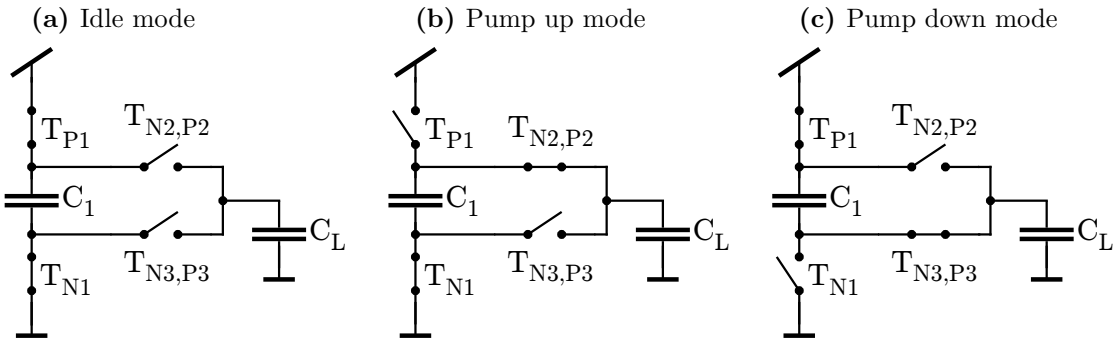

Figure 4.28: Operating modes of the CP. The idle mode (a) is required for pre-charging the capacitor C_1. The pump up (b) and down (c) modes are for increasing and decreasing the control voltage at the output node, respectively.

voltage V_{DD} equal to 1.1 V, the worst case power consumption is approximated to 33 μW.

During the **pump up** mode the transistor T_{N1} and the transmission gate $T_{N2,P2}$ are switched on, building a path to transport the stored charge in the capacitor C_1 to the load capacitor C_L. The simplified circuits for the pump up mode are depicted in Figure 4.29 at the time $t = 0$ (a) and during the charge transport $t > 0$ (b). The resistor R_{UP} originates from the on-resistance of the closed switch $T_{N2,P2}$. The transported charge to the load capacitor changes the control voltage V_{ctrl}, which is essential for the frequency adjustment of the VCO. Thus, the derivation of the time dependent control voltage, described below, is of a big interest.

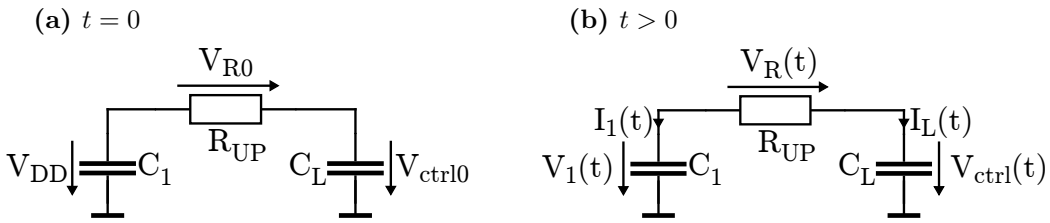

Figure 4.29: Simplified representation of the CP circuitry in the pump up mode. The resistor R_{UP} models the on-resistance of the closed transmission gate switch $T_{N2,P2}$ (see Figure 4.28b). The initial voltages across the electronic components at the beginning of the pump up mode ($t = 0$) are presented in (a). Figure (b) demonstrates the definitions for the time dependent voltages and currents.

First, we know the voltages at the start of the pump up mode across the capacitors. The capacitor C_1 is charged during the idle mode to the supply voltage V_{DD}. The initial voltage V_{ctrl0} across the load capacitor C_L represents the stored voltage value from the previous mode. Consequently, for the time dependent voltages Equations 4.28, 4.29 are applied

$$V_1(t) = V_{DD} - \frac{1}{C_1}\int_0^t I_L(t')\mathrm{d}t', \tag{4.28}$$

$$V_{ctrl}(t) = V_{ctrl0} - \frac{1}{C_L}\int_0^t I_L(t')\mathrm{d}t'. \tag{4.29}$$

The current I_L flowing at the time $t = 0$ is equal to

$$I_L(t=0) = \frac{V_{DD} - V_{ctrl0}}{R_{UP}}. \tag{4.30}$$

Applying KVL and substitution of Equations 4.28, 4.29 result in

$$V_1(t) = V_R(t) + V_{ctrl}(t), \tag{4.31}$$

$$V_{DD} - \frac{1}{C_1}\int_0^t I_L(t')\mathrm{d}t' = R_{UP}I_L(t) + V_{ctrl0} - \frac{1}{C_L}\int_0^t I_L(t')\mathrm{d}t'. \tag{4.32}$$

Taking the derivation of both sides of Equation 4.32 leads to a differential equation of the 1st order

$$-\frac{1}{C_1}I_L(t) = R_{UP}\frac{\mathrm{d}I_L(t)}{\mathrm{d}t} + \frac{1}{C_L}I_L(t), \tag{4.33}$$

$$R_{UP}\frac{C_1C_L}{C_1+C_L}\frac{\mathrm{d}I_L(t)}{\mathrm{d}t} + I_L(t) = 0. \tag{4.34}$$

Thus, for the current I_L, flowing in to the load capacitor C_L, it follows

$$I_L(t) = I_L(t=0)e^{-\frac{t}{\tau}} = \frac{V_{DD}-V_{ctrl0}}{R_{UP}}e^{-\frac{t}{\tau}}, \tag{4.35}$$

with

$$\tau = R_{UP}\frac{C_1C_L}{C_1+C_L}. \tag{4.36}$$

The required time dependent control voltage $V_{ctrl}(t)$ results from substitution of the derived current $I_L(t)$ into Equation 4.29 [114]

$$V_{ctrl}(t) = V_{ctrl0} + \frac{V_{DD}-V_{ctrl0}}{C_LR_{UP}}\int_0^t e^{-\frac{t'}{\tau}}\mathrm{d}t', \tag{4.37}$$

$$V_{ctrl}(t) = V_{ctrl0} + \frac{C_1}{C_1+C_L}(V_{DD}-V_{ctrl0})(1-e^{-\frac{t}{\tau}}). \tag{4.38}$$

The **pump down modus** occurs, when there is a phase difference between the reference clock and LO divided clock at the rising edge of the LO divided clock (see Section 4.6.2). For the period of time with phase difference of both clock signals, the switches T_{P1} and $T_{N3,P3}$ are closed, as depicted in Figure 4.28b. Consequently, the previously charged load capacitor C_L shares the charge with the capacitor C_1, i.e. the control voltage V_{ctrl} declines and the oscillating frequency of the VCO is reduced as well. The simplified circuitry of the CP during the pump down mode is depicted in Figure 4.30. It is very similar to the simplified circuitry for the pump up mode, presented in Figure 4.29, with the difference of capacitor C_1 connection.

In order to calculate the time dependent control voltage $V_{ctrl}(t)$ during the pump down mode, similar derivations as presented for the pump up mode can be applied. Here, the on resistance R_{DN} of the transmission gate switch $T_{N3,P3}$ has to be considered. The load current, flowing at the time $t = 0$, is equal to:

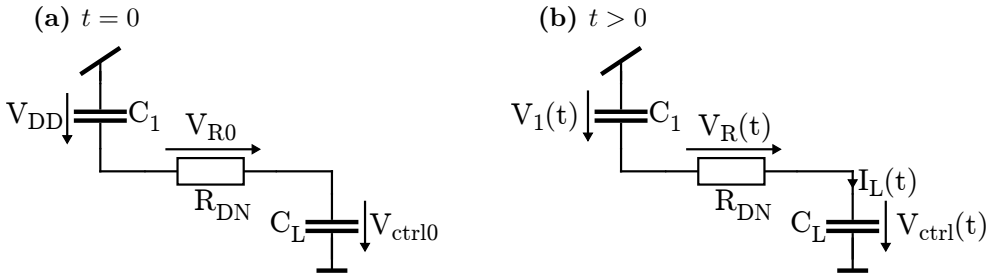

Figure 4.30: Simplified representation of the CP circuitry in the pump down mode. The resistor R_{DN} models the on-resistance of the closed transmission gate switch $T_{N3,P3}$ (see Figure 4.28b). The initial voltages across the electronic components at the beginning of the pump down mode ($t = 0$) are presented in (a). Figure (b) demonstrates the definitions for the time dependent voltages and currents.

$$I_L(t=0) = -\frac{V_{ctrl0}}{R_{DN}} \tag{4.39}$$

Equations 4.40 shows the final result of the time dependent control voltage in pump down mode

$$V_{ctrl}(t) = V_{ctrl0} - \frac{C_1}{C_1 + C_L} V_{ctrl0}(1 - e^{-\frac{t}{\tau}}), \tag{4.40}$$

with

$$\tau = R_{DN}\frac{C_1 C_L}{C_1 + C_L}. \tag{4.41}$$

As can be seen from the Equations 4.38 and 4.40, for the symmetric charge transitions in the pump up and pump down modes no extra matching circuitry is required [114]. Here, is important to keep the on-resistances of the transmission gates $T_{N2,P2}$ and $T_{N3,P3}$ as equal as possible.

4.6.4 Loop Filter

The PLL is a circuitry with a feedback loop, i.e. the issue with the instability could arise in case of an incorrect dimensioning of the electronic components. The loop filter of the PLL plays a significant role to fulfill the stabilization criteria, that are discussed below. Besides, the up and down pulses of the CP would modulate the VCO frequency and produce undesirable sideband in the frequency domain. Hence, a loop filter is required to prevent a relatively large sideband in the LO signal [61, p. 601].

Generally speaking, the PLL is a non-linear system in the voltage domain, as it is commonly known for an LNA or an OpAmp. However, the PLL system can be

linearized regarding the phase [61, pp. 606-607], i.e. considerations in the Laplace-transformed s-domain can be done for stability analyses. In this section, the whole PLL (see Figure 4.31) is considered in the s-domain to explain the need and the functional principle of the loop filter. The derivations, described below, essentially originate from [108, pp. 22-28].

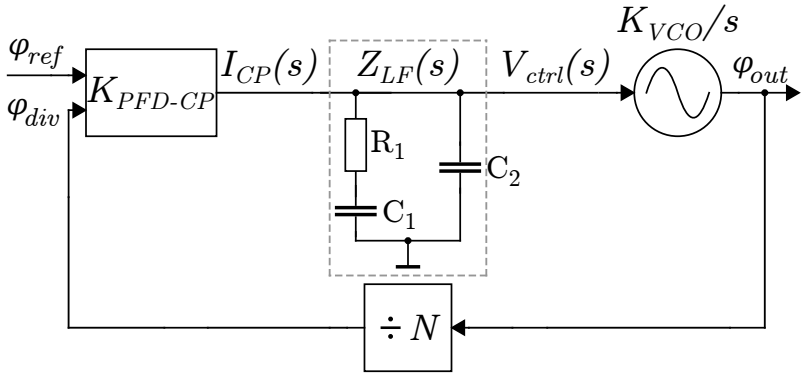

Figure 4.31: Block diagram of the PLL with its transfer functions. The PFD and the CP are combined to one block, due to a representation by a single transfer function. The loop filter is described by the impedance Z_{LF}.

The implemented CP (see Section 4.6.3) does not provide a constant current for charging and discharging the loop filter, as in traditional designs. However, to simplify the analysis of the open-loop transfer function of the PLL, the CP current is assumed to be constant. Hence, the phase difference $\Delta\phi = \phi_{ref} - \phi_{div}$ generates the pump up or pump down pulses, that deliver the constant current I_{CP} for a time fraction of the whole cycle. Thus, the transfer function K_{PFD-CP} of the combined PFD with the CP block is obtained as

$$K_{PFD-CP} = \frac{I_{CP}}{2\pi}. \tag{4.42}$$

The transfer function of the second order loop filter can be described with the impedance Z_{LF}, transforming the CP current $I_{CP}(s)$ into the control voltage $V_{ctrl}(s)$

$$Z_{LF} = \frac{1 + sR_1C_1}{s(sR_1C_1C2 + C_1 + C_2)}. \tag{4.43}$$

The frequency of the VCO is controlled by the control voltage V_{ctrl}. With a first order approximation, a linear behavior can assumed for the output frequency ω_{out} with the VCO gain K_{VCO}

$$\omega_{out} = \omega_0 + K_{VCO}V_{ctrl}(t). \tag{4.44}$$

Besides, the frequency in general can be expressed as time derivation of the phase

$$\omega_{out} = \frac{\mathrm{d}\phi_{out}}{\mathrm{d}t}. \tag{4.45}$$

Consequently, the phase is the integration of the frequency. With neglecting the initial condition of the output phase, the phase change at the output can be expressed with Equation 4.46

$$\phi_{out} = K_{VCO} \int V_{ctrl}(t)\mathrm{d}t. \tag{4.46}$$

Applying the Laplace transform to Equation 4.46, the transfer function of the VCO is equal to

$$\frac{\phi_{out}}{V_{ctrl}}(s) = \frac{K_{VCO}}{s}. \tag{4.47}$$

The presented steps for the derivation of the VCO transfer function originate from [61, pp. 577-581], where an interested reader can get more detailed information. Finally, taking the dividing factor N into account, the open loop transfer function of the PLL is formulated in Equation 4.48 as product of the above described transfer functions

$$H_{OL}(s) = \frac{1}{N}\frac{I_{CP}}{2\pi}\frac{1 + sR_1C_1}{s(sR_1C_1C2 + C_1 + C_2)}\frac{K_{VCO}}{s}. \tag{4.48}$$

For stability analysis of the PLL and for its lock time, the phase margin of the open loop transfer function plays a significant role. Based on selected loop filter parameters, the appropriate poles and zeros positions can be selected, in order to maximize the phase margin of the system. The example in Figure 4.32 demonstrates the bode plot of the transfer function H_{OL}. The assumed parameter values and the proposed MATLAB script for the PLL stability analysis can be found in Appendix C.

The implemented loop filter of the second order introduces a zero in the transfer function of the PLL, that increases the phase margin of the system. Besides, it has to be kept in mind, that the gain of other building blocks influence the stability of the PLL, as well. For instance, the assumed gain $2\,\frac{\mathrm{GHz}}{\mathrm{V}}$ of the VCO varies around $1-3\,\frac{\mathrm{GHz}}{\mathrm{V}}$, depending on the actual values of the control voltage V_{ctrl} and the implemented topology of the VCO in general. Consequently, the magnitude of the PLL transfer function (see Figure 4.32) increases or decreases with the gain variation, i.e. the frequency point with magnitude 1 shifts to the right or to the left, respectively. This fact leads to the reduction of the phase margins. Thus, the stability of the PLL has to be proved for each proposed VCOs at different frequencies (see simulation results in Section 5.4.2.

Finally, it is relevant to mention the rule of thumb approach to select the device dimensions of the loop filter, in order to achieve a reasonable stability of the PLL system:

- The ratio of the third pole and zero $\frac{\omega_p}{\omega_z}$ should be more than 10 [108, pp. 22-28].
- The loop bandwidth ω_c should be more than 10 time higher the reference frequency ω_{ref} [111].

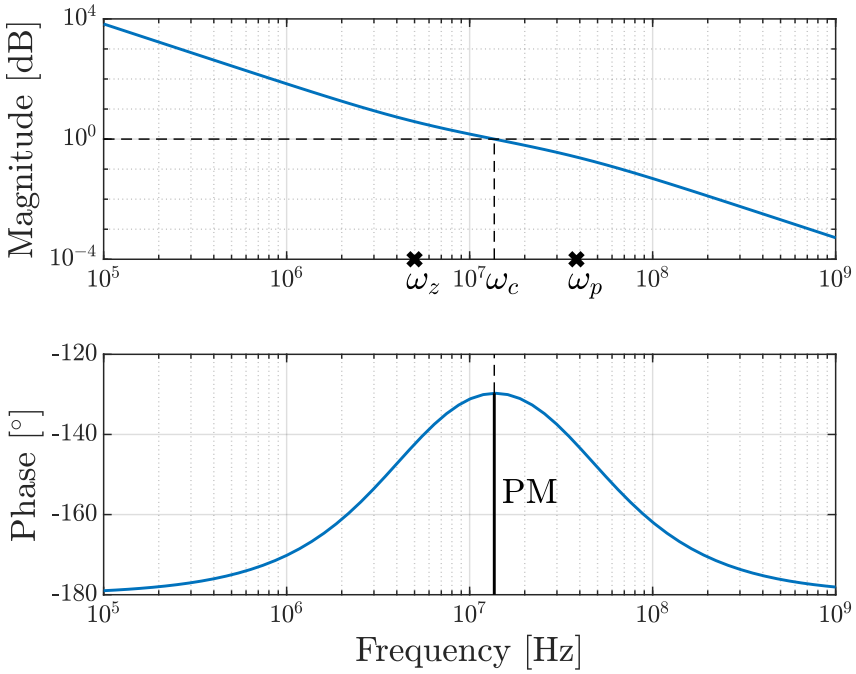

Figure 4.32: Bode plot of the PLL open loop transfer function H_OL. Two poles at frequency 0 Hz results in the phase shift of $-180°$ and the magnitude slope of $-40\,\frac{\text{dB}}{\text{dec}}$. The introduced zero ω_z of the loop filter decreases the slope of the magnitude to $-20\,\frac{\text{dB}}{\text{dec}}$ and increases the phase, making the phase margin of around 50° acceptable for the PLL stability. The third pole w_p decreases the phase and increases the absolute slope value of the magnitude. The bandwidth of the PLL is defined as frequency point ω_c at the magnitude equal to 1.

- The ratio $\frac{C_2}{C_1}$ of the filter capacitance C_2 (Figure 4.31) and the CP capacitance C_1 (Figure 4.27) should be in the range of 10 [114].

4.6.5 Recommended Publications

A handful ideas for the implemented topologies of the PLL components have been adopted from publications presented by Schober [102,114–116]. The summary of the whole PLL is elaborated in [101]. The PLL circuitry is fabricated in 28nm CMOS technology and covers the frequency range of $0.8 - 28.2$ GHz.

Another approach of the PLL design for 60 GHz is presented by Cheema [108]. Here, the circuitry is designed for a transceiver's frequency synthesizer. Especially, the considerations regarding the physical realization and verification offer precious information to be followed by design of mmW CMOS PLL circuit components.

A transceiver synthesizer operating in $26 - 32$ GHz and designed for 5G mobile communications is presented in [117]. A relatively low phase noise has been achieved with a cascaded PLL architecture. Here, the output LO signal of the first stage is used as reference signal for the second stage.

Another 5G PLL is proposed by Siriburanon [118]. The circuitry is designed for

a narrow band frequency $27.5 - 29.6\,\text{GHz}$. Instead of using the conventional PLL architecture, the frequency multipliers out of PLL are used for the reference signal and for the LO signal at the output of the VCO. This approach offers the reduction of the in-band and out-of-band phase noise.

4.7 Operational Amplifier

The final step of the SW readout circuitry is realized by the OpAmp with band-pass characteristic. It filters out undesired frequency components of the IF signal, coming from the mixer, and amplifies the signal in $10 - 60\,\text{MHz}$ range. Topology of the designed single-ended OpAmp with two stages is depicted in Figure 4.33. The schematic with parameter values of the electronic devices is attached in Appendix A.5 Figure A.24. The purpose and the functionality of each implemented electronic device are described in below.

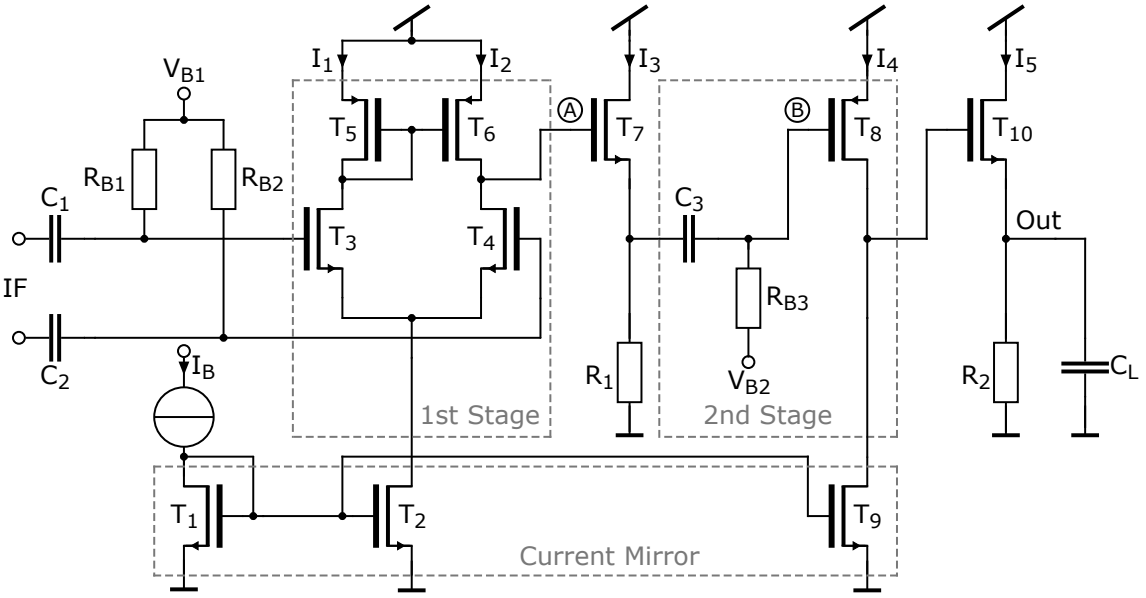

Figure 4.33: Topology of the differential single-ended Operational Amplifier (OpAmp) with two amplifying stages. Each stage is followed by a buffer to drive the high capacitive load. The DC current to the stages is provided by I_B. The DC gate voltages of the transistors T_{3-4} and T_8 are adjusted by bias voltage source V_{B1} and V_{B2}, respectively.

C_{1-3} High-Pass Capacitive Coupling: To be able to adjust DC operating point of the OpAmp, independent from the DC output voltage of the previous circuitry, e.g. mixer or first stage of the OpAmp, the capacitive coupling is often used. Additionally, the undesired low frequency components of the mixer's IF signal below 10 MHz can be filtered out. The IF signal propagating through the OpAmp to the output node Out is filtered twice by high-pass filters C_{1-2} and C_3, i.e. the attenuation of the noise below 10 MHz by $40\,\frac{\text{dB}}{\text{dec}}$.

R_{B1-B2} Bias Resistors: The DC voltage of the transistors T_{3-4} and T_8 is set by the bias voltages V_{B1} and V_{B2}, respectively. So that the AC signal can propagate to

the gates of the transistors, the bias resistors R_{B1-B2} and R_{B3} are inserted in the circuit. The resistances have to be properly chosen to set the corner frequency f_c of the high-pass RC-filter to the desired 10 MHz, i.e. the well-know Equation 4.49 has to be applied

$$f_c = \frac{1}{2\pi R_{Bi} C_i}. \tag{4.49}$$

$\mathbf{T_{1-2}}, \mathbf{T_9}$ Current Sources with Current Mirror: The DC current to the first and to the second stages is provided by transistors T_2 and T_9. For this, the constant bias current I_B is applied to the transistor T_1, that mirrors the current to the transistors T_2 and T_9. Here, it has to kept in mind, to size the transistors with a low as possible mismatch to each other. The constant current I_B can be provided from outside of the chip by generating an additional pad and thus having the flexibility for the trimming. The alternative is the generation of a current reference, independent from process, supply voltage and temperature variations [74, 85].

$\mathbf{T_{5-6}}$ Current Mirror: The applied current to the first stage of the OpAmp has to be evenly distributed to the both branches (see Figure 4.33). The current mirror, realized by equal transistors T_{5-6}, automatically adjust the current I_1 and I_2 to the same values. It mirrors the current I_1 to I_2 due to equal gate-source voltages of the PMOS transistors T_{5-6}

$\mathbf{T_{3-4}}$ Differential Pair: The differential IF signal, coming from the mixer, is applied to the differential pair transistors of the OpAmp, i.e. only voltage difference between to input nodes is amplified. To understand the functionality of the differential amplifier stage, we consider the small signal behavior of the circuit part.

If both input nodes rise by the same small signal value, the transistors T_3 and T_4 become more open and a higher drain current flows. The higher drain current through transistor T_4 reduces the voltage at the node A. However, the higher drain current through transistor T_3 is mirrored by transistor T_5, i.e. the equally increased drain current flows through transistor T_6, that increase the voltage at the node A by the same factor as it was reduced by the increased drain current of the transistor T_4. Consequently, the voltage at the node A remains unchanged and there is no amplification if both input nodes rise by the same voltage value. The same consideration can be done for the decreasing voltage values at both input nodes.

By considering the case that input voltage rises only at one node, then the higher drain current appear only in one branch of the first stage. Thus, the voltage at the node A can not be compensated anymore and it rises or falls depending on the differential input signal. For the small signal voltage amplification A_V from the differential input voltage v_{diff} to the node A voltage v_A following Equation 4.50 is applied

$$A_V = \frac{v_A}{v_{diff}} = g_{m4}(r_{ds4} + r_{ds6}), \tag{4.50}$$

with small signal parameter:
g_{m4}: transconductance of the transistor T_4
r_{ds4}: output drain-source resistance of the transistor T_4
r_{ds6}: output drain-source resistance of the transistor T_6

$\mathbf{T_7}, \mathbf{T_{10}}, \mathbf{R_{1-2}}$ Common-Drain Buffer: To decouple the first stage of the OpAmp from the second one and the second stage from the capacitive output load C_L, the common-drain circuits T_7 with R_1 and T_{10} with R_2 are implemented, respectively. The common-drain circuits have two functions. First, it drives high capacitive loads without changing the current in the amplifying stage. Second, the parasitic overlap capacitances of the common-drain transistors T_7 and T_{10} are significantly lower than the capacitances C_3 and C_L, i.e. the OpAmp can operate at higher frequencies without a degradation of the gain. However, the drawback of the common-drain circuit is a small attenuation A_{CD} of the gain as expressed in Equation 4.51 [96, pp. 68-69] for the first buffer and shown in Section 5.5.

$$A_{CD} = \frac{g_{m7}}{1 + g_{m7} R_1} \tag{4.51}$$

$\mathbf{T_8}$ Common-Source Amplifier: The second amplifying stage is realized by a common-source circuit with the PMOS transistor T_8. The realization with an NMOS transistor would require two PMOS transistors for the current source instead of one, as it is done with transistor T_9 (see Figure 4.33). Equation 4.52 applies for the gain of the common-source circuit A_{CS}.

$$A_{CS} = -g_{m8}(r_{ds8} + r_{ds9}) \tag{4.52}$$

$\mathbf{C_L}$ Load Capacitance: The load capacitance C_L plays a significant role for the bandwidth of the OpAmp. Dependent on the circuitry connected to the output of the OpAmp, different capacitances appears as the load. It can be relatively small in case of a direct connection to an integrated ADC, medium in case of an output pad connected to an external Printed Circuit Board (PCB) ADC or relatively large in case of an output pad connected to an extern measurement setup. In any cases, the output buffer circuitry has to be adjusted to be able to drive the load in the required frequency band. Here, the load capacitance is assumed to 0.5 pF (see Figure A.24).

The reader has to keep in mind, that the proposed OpAmp cannot operate in a closed-loop configuration, due to a low phase margin resulting in the instability of the circuit. Thus, the open-loop run is targeted, i.e. the trimming resistors between the differential pair T_{3-4} and current source T_2 are possibly required to compensate for the current difference in both branches of the first stage caused by the mismatch between the transistors T_3 and T_4.

Chapter 5

Simulation Results of the Readout Circuitry

This Chapter presents simulation results of the SW readout components performed in Cadence Virtuoso. For the simulations all real electronic device models, including integrated inductors, have been used. However, the interconnect parasitics, which will be impacted by the physical layout, have not yet been included in these simulations. This chapter provides simulation results of the parameters, characterizing the performance of each readout component: LNA, mixer, VCO, PLL and OpAmp.

5.1 Low Noise Amplifier

The principle goal in LNA design is high gain, low NF and appropriate input matching in the bandwidth of interest. Thus, the optimization of the LNAs has been especially geared to these three parameters, that are presented below. Besides, Table 5.1 summarizes achieved performance for the minimum NF, the maximum gain, the distortion parameters IP_{1dB} and IIP_3, and the DC power consumption. The IP_{1dB} and IIP_3 values confirm the rule of thumb, that the IP_{1dB} is typically 10 dBm lower than IIP_3 [119, p. 23]. The setup of the simulation tool Cadence Virtuoso for extracting typical LNA parameters is partially token from [120].

5.1.1 Gain

The estimated signal power in the loop antenna is in the range of -90 dBm [133], i.e. approximately $10\,\mu$V by the resistance of $50\,\Omega$. If we assume even less power of -95 dBm, expected voltage values will be in the range of $5 - 6\,\mu$V. In order to have at least $100\,\mu$V at the RF input of the mixer, the LNA gain of 200 is required (≈ 26 dB).

Figure 5.1 shows simulation results of the LNAs gain in 6 different frequency band, starting from frequency of 9 GHz till 50 GHz. All designed LNAs have gain of more than 26 dB. The bandwidth of an LNA is defined as frequency range with

Table 5.1: Summary of the achieved performance for each LNA operating in corresponding frequency range.

Frequency Range [GHz]	min. NF [dB]	max. Gain [dB]	IP_{1dB} [dBm]	IIP_3 [dBm]	DC Power [mW]
$9-13$	1.72	37.4	-40.5	-30.5	54.6
$13-19$	1.85	39.0	-33.9	-24.0	54.0
$19-26$	2.04	33.2	-15.3	-5.0	60.1
$26-33$	2.47	34.2	-6.1	3.8	32.8
$33-39$	2.72	30.6	-4.3	7.3	34.1
$39-50$	3.05	36.5	-2.0	8.4	36.2

a gain drop of maximum 3 dB. Here, we partially see more than 3 dB of the gain difference inside one band. Due to the fact, that for the frequency measurement of the SWs are not absolute values of the signal's amplitude required and for the amplitude measurement a relative change is targeted, so the requirements for the readout circuitry is more relaxed in this case. Today, it is in general very difficult to measure absolute amplitude of a signal at such high frequencies. Thus, to achieve a flat gain in the required bandwidth was not targeted for the LNAs. It was more relevant to cover the whole frequency range $9-50$ GHz without gaps.

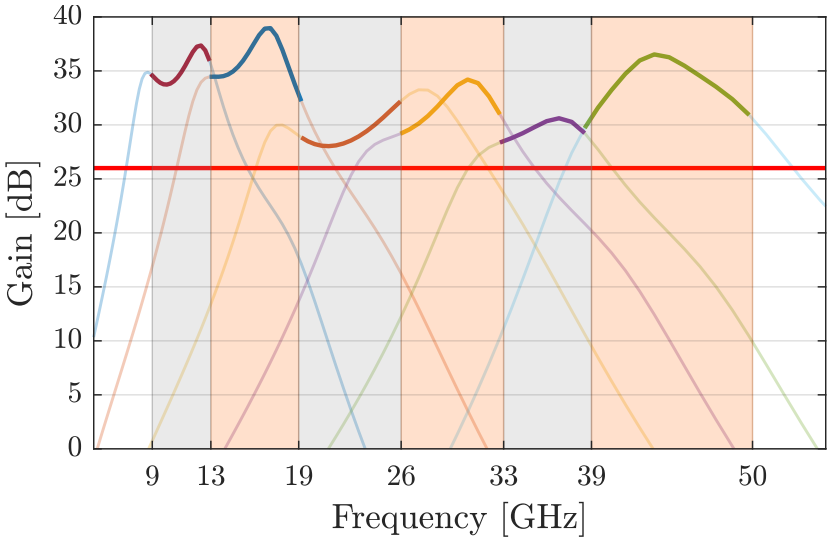

Figure 5.1: Voltage gain of the LNAs operating in 6 different frequency bands from $9-50$ GHz. The values at the abscissa correspond to limits of the bandwidths, that marked with alternating colors. The red horizontal line is sketched at 26 dB and shows that all LNAs achieve the amplification factor of at least 200.

5.1.2 Input Matching

In Chapter 3 the relevance of the scattering parameter S_{11} has been already elaborated. The simulation results of the S_{11} for all designed LNAs are depicted in Figure 5.2. Due to the fact, that to achieve at the same time a broad input matching and low NF is pretty difficult, a trade-off is required. The S_{11} value of less than $-10\,\text{dB}$ means the maximum reflection of 10 %, the value that also in practice still acceptable [61, p.259].

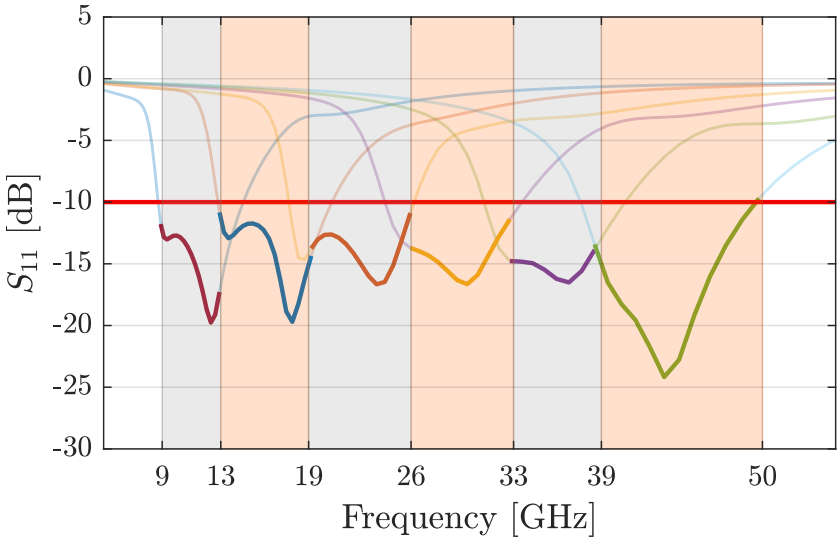

Figure 5.2: Scattering parameter S_{11} of the LNAs operating in 6 different frequency bands from $9 - 50\,\text{GHz}$. The red horizontal line corresponds to value of $-10\,\text{dB}$, i.e. less than 10 % of the LNA input signal is reflected back.

5.1.3 Noise Figure

Figure 5.3 shows the simulation results of the LNAs NF. As previously mentioned, less than 3 dB of the NF was targeted to achieve. 3 dB NF means the SNR at the input of the LNA degrades by factor of 2 compared to the SNR at the output of the same LNA. Except for the LNA operating in $39 - 50\,\text{GHz}$ range, the NF remains below 3 dB. For the designs between $9 - 26\,\text{GHz}$ the NF is even less than 2.5 dB.

Considering the minimum NF of each frequency band in Figure 5.3, the rising trend to higher frequencies is obvious. The reason for the increasing minimum NF is the gate resistance contributing more to the overall noise at higher frequencies [71, Figure 8a].

5.1.4 Stability

In Section 3.6 the stability parameter K and B_1 have been introduced. The LNA is unconditionally stable in case $K > 1$ and $B_1 > 0$. Figure 5.4 proves the stability of the LNA for the source (port 1) and the load (port 2) impedances equal to $50\,\Omega$ and $140\,\Omega$, respectively (see also Figure 4.3). Here, the curves of the parameters K and

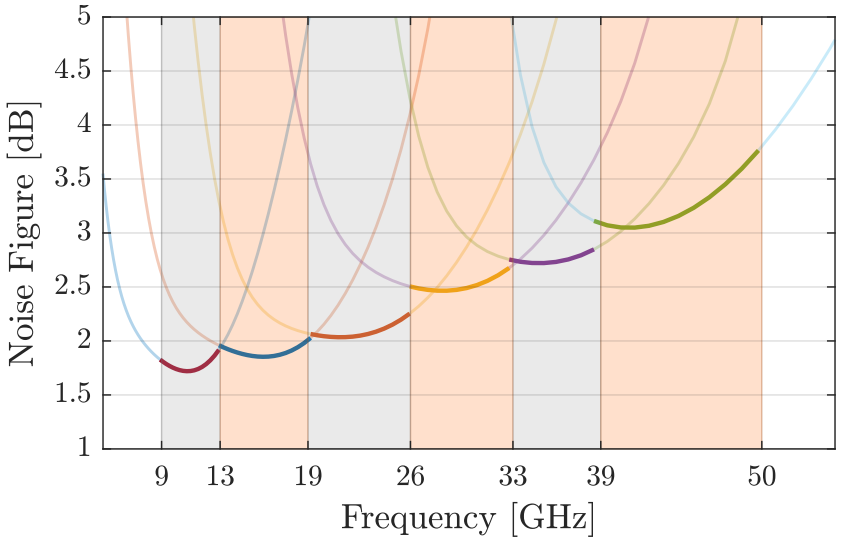

Figure 5.3: NF of the 6 LNAs operating at different frequency bands from $9 - 50\,\mathrm{GHz}$. The minimum achievable NF is rising with increasing frequency due to the higher contribution of the transistors' gate resistances [71].

B_1 have no particular meaning. It is crucial the curve do not run in to the *potentially* unstable regions. *Potentially* means, that the circuity could still be stable, even the above mentioned conditions are violated, but it cannot be guaranteed anymore.

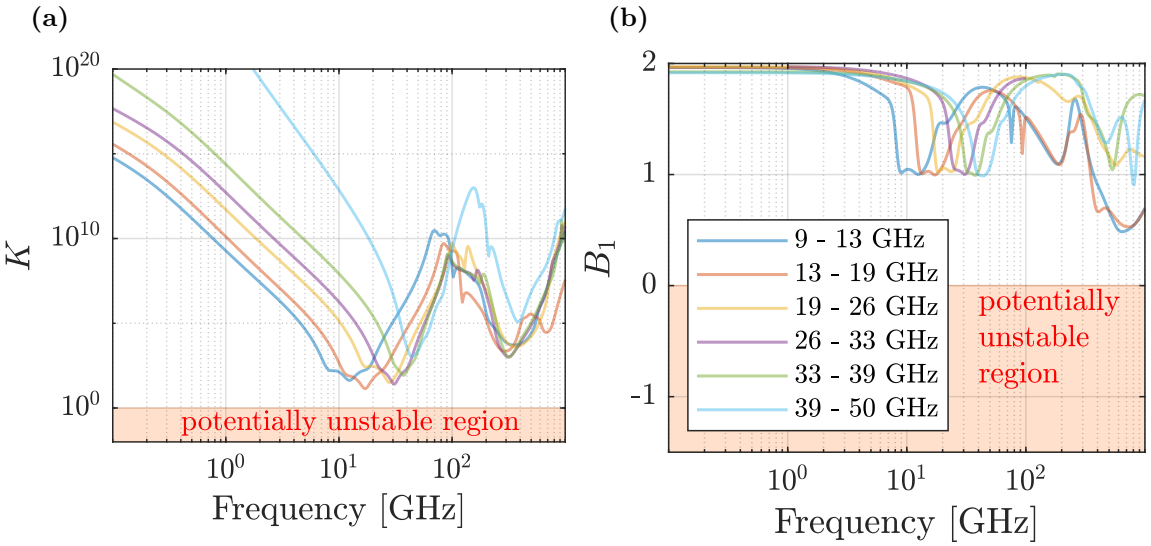

Figure 5.4: Stability parameters K (a) and B_1 (b). Parameters extracted from the simulation results of the LNAs operating in 6 different frequency bands. Legend in (b) also applies for (a). For *unconditional stability* the inequalities $K > 1$ and $B_1 > 0$ have to be hold.

5.2 Mixer

Here, the achieved performance of the mixer presented in Section 4.4 is described. It is quite obvious that the performance of the the design down-converting Gilbert cell mixer is highly dependent on the signal power applied at the LO input. Thus, to characterize the mixer, first the conversion gain versus input LO power has to be considered. It is essential in order to be able to compare different topologies with each other. Figure 5.5 depicts the conversion gain swept over the mixer's input LO power. The maximum achievable conversion gain is considered as reference, i.e. the 6 dBm LO power is used for all simulations presented below. For the designed mixer a relatively low power consumption of 3.5 mW has been achieved. For the simulation setup in software tool Cadence the reader is referred to the tutorials published in [121, 122].

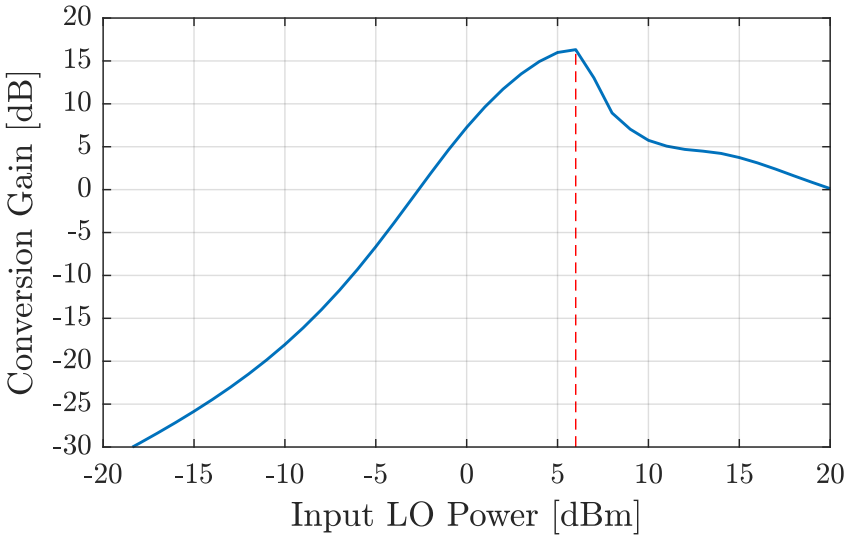

Figure 5.5: Conversion gain of the mixer versus input LO power. For this simulation the frequencies of the RF and LO signals are set to 25.02 GHz and 25 GHz, respectively. The maximum value of the conversion gain is achieved at 6 dBm.

5.2.1 Conversion Gain

The voltage conversion gain of the designed mixer is depicted in Figure 5.6. More than 16 dB in the desired frequency range $9 - 50$ GHz is achieved. For comparison only, a typical achievable conversion gain is around $10 - 15$ dB [61, p. 338]. The gain improvement at $30 - 50$ GHz is induced by inductors placed in the RF signal path. To filter out lower frequency components, the adjustment of the coupling capacitors and bias resistors in the LO path has been primarily done. To lower values of the bias resistors in the RF path would significantly diminish the conversion gain.

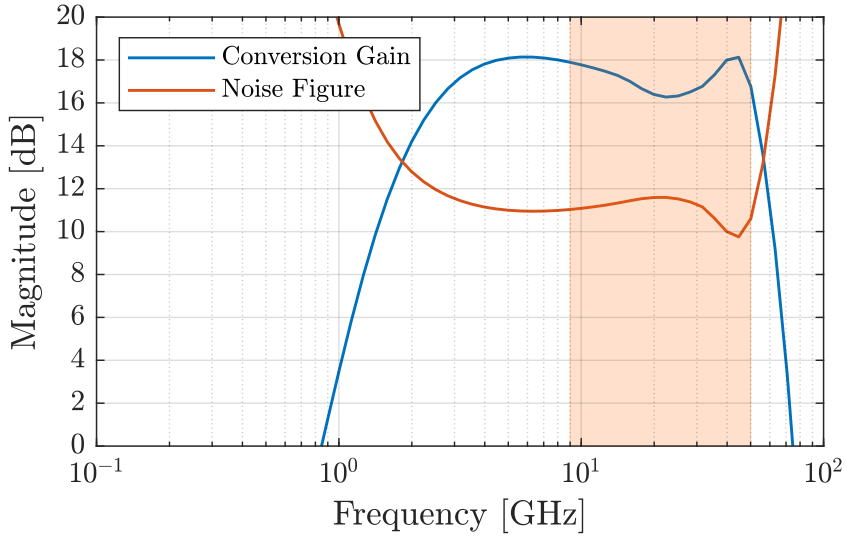

Figure 5.6: Conversion gain and NF of the designed mixer (see Figure 4.8). In the marked bandwidth of interest $9 - 50$ GHz the voltage conversion gain is more than 16 dB and the NF less than 12 dB.

5.2.2 Noise Figure

As mentioned in [61, p. 338], it is relatively seldom for a mixer to achieve a NF less than 8 dB. For UWB mixer is even hard to have less than 11 dB [79, 87, 88, 90]. As mentioned in [62, p.422], more frequently achieved NF values are around 15 dB. Thus, the simulated NF below 12 dB is a decent result (see Figure 5.6). The reader

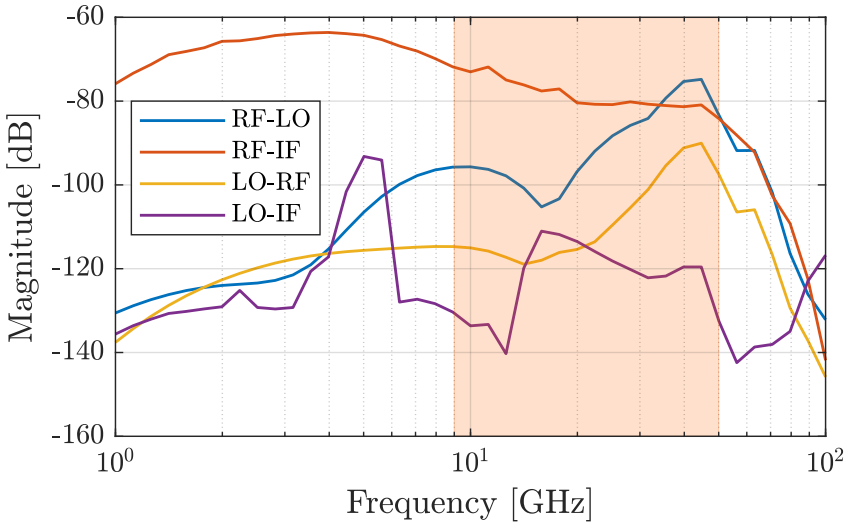

Figure 5.7: Characterization of the mixer's port isolation from RF to IF (RF-IF), from RF to LO (RF-LO), from LO to RF (LO-RF) and from LO to IF (LO-IF). A relatively low feedthroughs between all the port are achieved. The higher RF-IF feedthrough at lower frequencies is caused by amplified RF signal through transconductance transistors $T_{4,5}$ (see Figure 4.8), that is easily filtered out by the following OpAmp.

has to take into account, that sometimes the DSB NF is presented in publications in order to show better achievements. Here, the SSB NF is extracted, i.e. the DSB NF would be 3 dB lower.

5.2.3 Port-to-Port Isolations

The importance of the port-to-port isolations in a mixer is already described in Section 3.7. The simulation results of the 4 types feedthroughs are depicted in Figure 5.7. A relatively good isolation is achieved due to fully differential mixer topology. However, it has to be keep in mind, that the physical layout would play a significant role for the isolation, because the signal coupling from wire to wire is not included in the presented results. Typical values of the feedthroughs are around −60 dB [62, p. 420].

5.2.4 Distortion

The two commonly used parameters describing distortion of the mixer are 1 dB compression point and 3rd order intercept point. The simulated values are shown in Figure 5.8. The distortion parameters of the Gilbert cell mixer are bounded by the transconductance transistors $T_{4,5}$ (see Figure 4.8) [62, p. 422]. With rising voltage values at the input, the transconductance transistor leave the saturation regions and thus the distortion occurs. To achieve a better linearization, degenerating inductors can be implemented as proposed by Lee [62, p. 420].

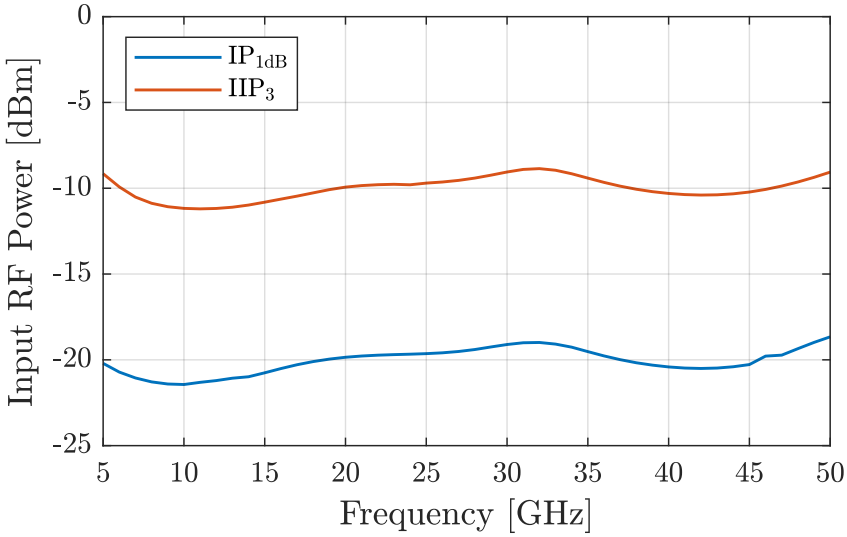

Figure 5.8: Input referred distortion parameters IP_{1dB} and IIP_3 extracted at different operating frequencies. The values remain relatively stable. The typical 10 dBm difference between IP_{1dB} and IIP_3 is apparent as well [119, p. 23].

5.3 Voltage Controlled Oscillator

Simulation results of the VCO designs, which described in Section 4.5, are presented below. Table 5.2 summarizes the performance of the six VCOs covering together $9 - 50\,\text{GHz}$. The achieved Phase Noise (PN) at the offset of 10 MHz is around $90 - 100\,\frac{\text{dBc}}{\text{Hz}}$. Unfortunately, the PN degrades with increasing tuning range [61, p. 501]. Thus, a trade-off have to be made regarding the PN and the number of the VCO designs covering the high frequency range of $9 - 50\,\text{GHz}$.

Each VCO produces a reasonable voltage swing around 1 V at the output, required for a proper LO signal level at the mixer. As mentioned in Section 5.2, the amplitude of the LO signal has direct impact on the conversion gain and the NF of the mixer (see also Figure 5.5).

The power consumption of the VCOs, listed in Table 5.2, is below 10 mW for all designs, except the VCO operating in $39 - 50\,\text{GHz}$. The higher power consumption of the $39 - 50\,\text{GHz}$ VCO is caused by the absence of the cross-coupled PMOS transistors, diminishing current flow, as it is the case of the VCO designs at lower frequencies (see Section 4.5).

Table 5.2: Summary of the achieved performance for each VCO operating in frequency bands between $9 - 50\,\text{GHz}$. The control parameters are set to values achieving highest frequency in the corresponding frequency band.

Frequency Range [GHz]	PN at 10 MHz $[\frac{\text{dBc}}{\text{Hz}}]$	Output Swing [V]	DC Power [mW]
$9 - 13$	-96	0.91	3.48
$13 - 19$	-96	0.88	7.19
$19 - 26$	-103	0.99	5.46
$26 - 33$	-93	0.97	7.26
$33 - 39$	-101	0.90	7.60
$39 - 50$	-98	1.0	19.2

5.3.1 Frequency Tuning

All designed VCOs have two possibilities to adjust the oscillating frequency, one for the fine frequency tuning and second for the coarse frequency tuning. It has to be kept in mind, to cover the targeted frequency range from $9 - 50\,\text{GHz}$ without blind zones, i.e. each frequency between $9 - 50\,\text{GHz}$ have to be adjustable with a reasonable precession. The achieved resolution of the VCOs is in the range of 20 MHz.

5.3.1.1 Ring Oscillator

The frequency adjustment of the VCO operating in $9 - 13\,\text{GHz}$ is depicted in Figure 5.9. The fine frequency tuning is realized by sweeping the control voltage V_{ctrl}

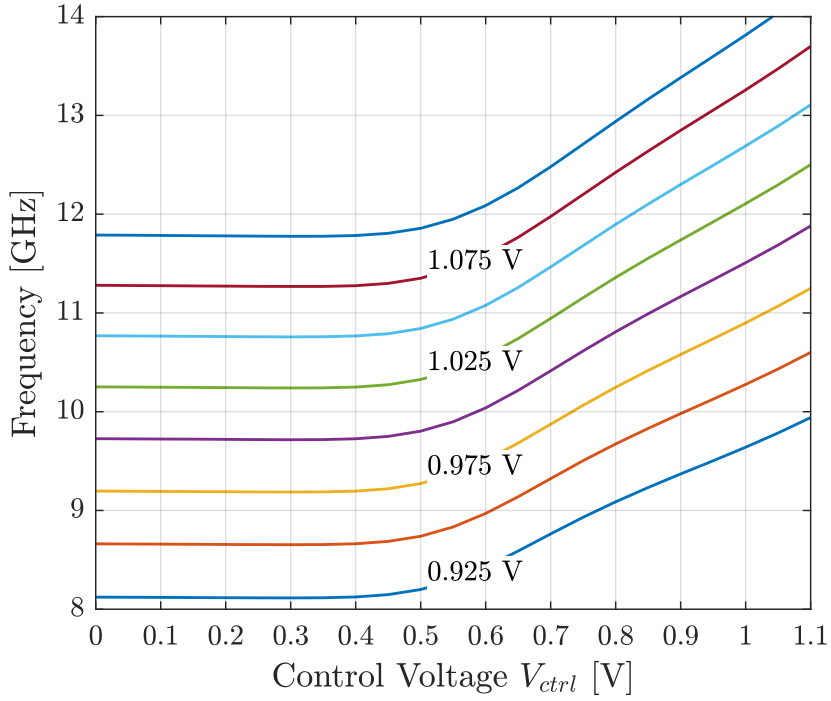

Figure 5.9: Frequency sweep of the VCO designed for $9-13\,\mathrm{GHz}$ and presented in Figure 4.11. The fine frequency tuning is achieved by the control voltage V_{ctrl}. The coarse frequency tuning is realized by sweeping the supply voltage of the inverter stages in steps of $25\,\mathrm{mV}$.

of the delay element in the feedback path ot the ring oscillator, presented in Figure 4.11. As shown in Figure 5.9, the oscillating frequency can be adjusted from $0.5-1.1\,\mathrm{V}$ of the control voltage. Below $0.5\,\mathrm{V}$ the delay transistors T_{1-2} (see Figure 4.11) are switched off and the current flows through the resistors, connected parallel to the transistors drain and source contacts. Thus, the frequency remains unchanged. The insertion of the parallel resistors are required, to sustain the oscillation of the circuitry. Otherwise, the PLL would not be able to control the frequency, if the VCO stops to oscillate.

The coarse frequency tuning is achieved with the variation of the supply voltage for the inverter stages. To avoid the blind zones, the voltage steps of approximately $25\,\mathrm{mV}$ are required. As depicted in Figure 5.9, the targeted frequency range of $9-13\,\mathrm{GHz}$ is covered with the proposed VCO design, presented in Figure 4.11.

A closer look at curves gradient in Figure 5.10 reveals a relatively flat region for the control voltage between $0.2-0.45\,\mathrm{V}$. However, the oscillating frequency should continue to increase with increasing control voltage values, due to decreasing output resistance of the control transistor, as depicted in Figure 5.11a. Below the threshold voltage the output resistance decreases exponentially.

The reason for the flattened gradient of the oscillating frequency curves is the increase of the drain capacitances. Figure 5.11b presents the drain-source and drain-gate capacitances of the control transistor $\mathrm{T_C}$. It is obvious, that in the range

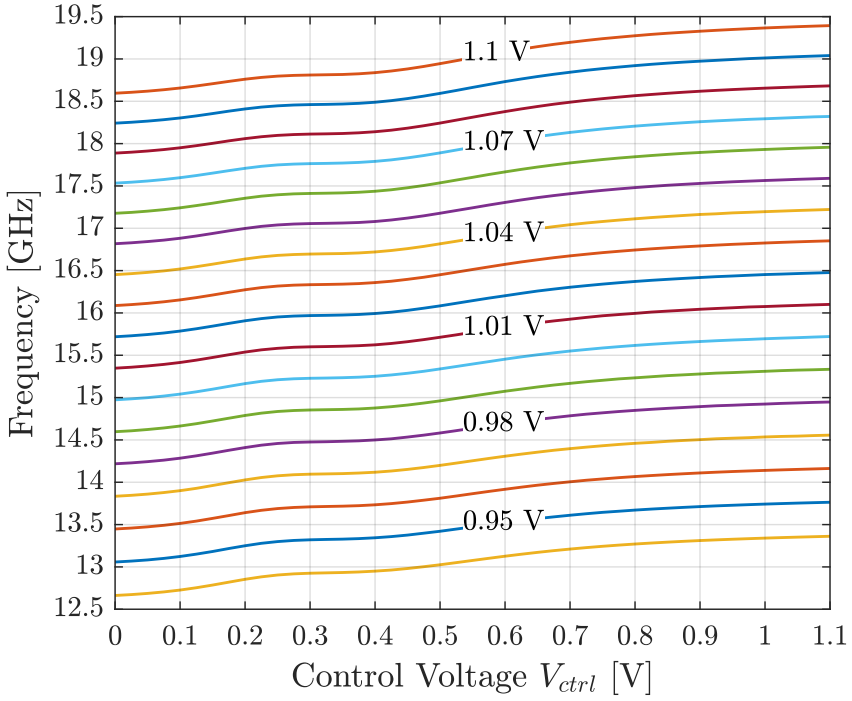

Figure 5.10: Frequency sweep of the VCO designed for 13 – 19 GHz. Schematic of the circuit is presented in Figure 4.13. The fine frequency tuning is adjusted by the control voltage V_{ctrl}. The coarse frequency tuning is realized by sweeping the supply voltage of the inverter stages in steps of 15 mV.

0.2 – 0.45 V the drain capacitances increase. Thus, the oscillating frequency can not rise with the same gradient, as it would be the case due to the decreasing output resistance of the control transistor.

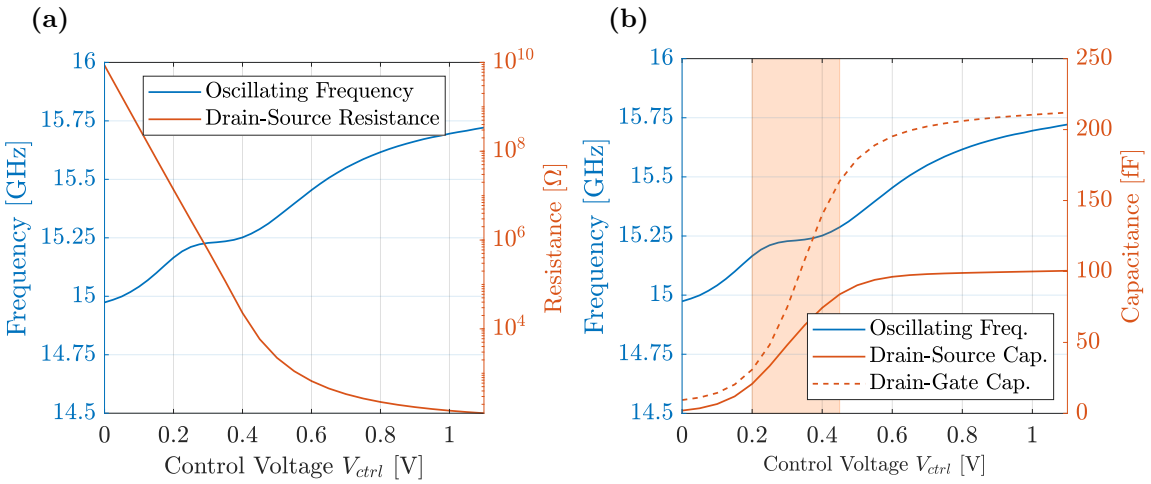

Figure 5.11: Frequency sweep of the VCO designed for 13 – 19 GHz. The selected curve for the oscillating frequency is for the supply voltage of 1 V. The red curves show the output resistance a) and the drain capacitances b) of the control transistor T_C (see Figure 4.13) for the fine frequency tuning.

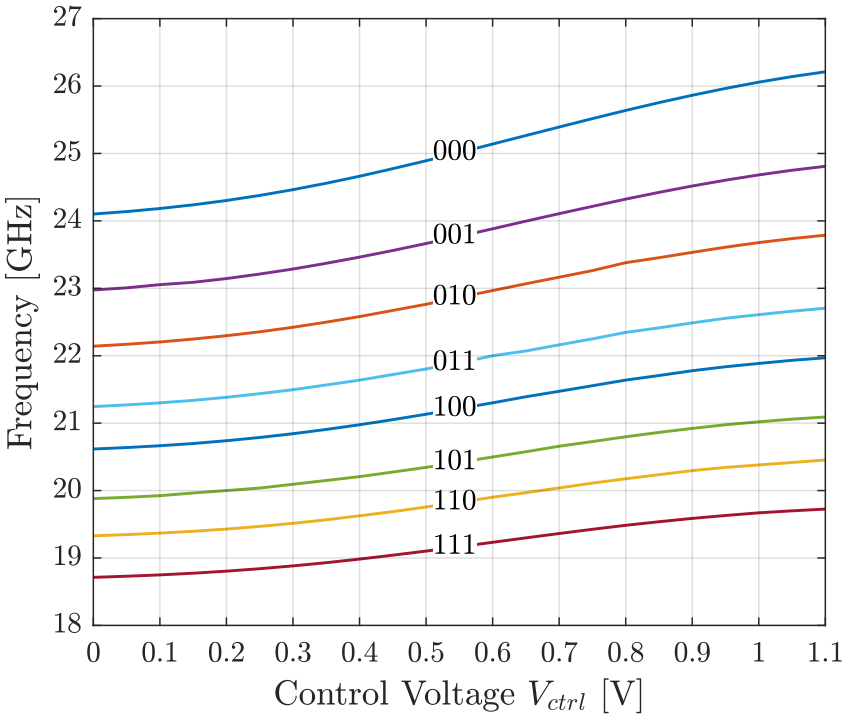

Figure 5.12: Adjustment of the VCO oscillating frequency in the range $19-26\,\text{GHz}$. The fine tuning of the frequency is made by the control voltage V_{ctrl} (see schematic in Figure 4.17). The coarse discrete tuning of the frequency is adjusted by digitally controlled input signals b_{0-2}.

5.3.1.2 LC Oscillator

The frequency sweep of the VCO designed for $19-26\,\text{GHz}$ is depicted in Figure 5.12. Comparing the slope of the curves, it becomes obvious that at lower frequencies the Δf_{osc} lessens. The reason is, the relative change of the capacitance by sweeping the control voltage V_{ctrl} becomes lower with increasing the unit capacitances by switching on the transistor responsible for the coarse tuning [61, pp. 533-534].

Compare to the ring oscillator topologies, where the coarse tuning can be flexibly adjusted by the supply voltage, the coarse frequency tuning by the designed LC oscillators is binary coded. Thus, it has to be kept in mind to avoid blind zones of the oscillating frequency. The example of the binary coded unit capacitances for the VCO operating in $19-26\,\text{GHz}$ are listed in Table 5.3. Topology of the circuitry can be found in Section 4.5 Figure 4.17.

Figure 5.12 reveals that the targeted frequency range is covered without blind zones. As expected, with increasing binary number, i.e. more switches for the unit capacitors are on, the oscillating frequency decreases.

The simulation results of the frequency tuning for the remaining designs covering $26-50\,\text{GHz}$ are attached in Appendix. The curves characteristics are very similar to the results presented in Figure 5.12.

Table 5.3: Binary coded unit capacitances for adjusting the frequency of the VCO operating in $19-26\,\text{GHz}$. C_0 indicates the load capacitance at one of the LO nodes whereas all switches b_{0-2} for the coarse frequency tuning are turned off (see Figure 4.17).

b_2	b_1	b_0	Capacitance
0	0	0	C_0
0	0	1	$75\,\text{fF} + C_0$
0	1	0	$137\,\text{fF} + C_0$
0	1	1	$212\,\text{fF} + C_0$
1	0	0	$261\,\text{fF} + C_0$
1	0	1	$336\,\text{fF} + C_0$
1	1	0	$398\,\text{fF} + C_0$
1	1	1	$473\,\text{fF} + C_0$

5.3.2 Phase Noise

The PN of the designed VCO at the offset frequency 10 MHz has been already presented in Table 5.2. The values around $-100\,\frac{\text{dBc}}{\text{Hz}}$ has been achieved, i.e. the signal power at the offset frequency of 10 MHz is 100 dB lower than the signal power at the carrier frequency. The consideration of the 10 MHz offset is chosen due to the targeted frequency measurement of the SW with a precision around 20 MHz.

The PN of the $9-13\,\text{GHz}$ VCO at other offset frequencies can be read from the Figure 5.13. The PN decreases with $20\,\frac{\text{dB}}{\text{dec}}$ with increasing offset frequency. Due to the fact, that other VCOs deliver similar results, the simulated PN plots are not depicted here.

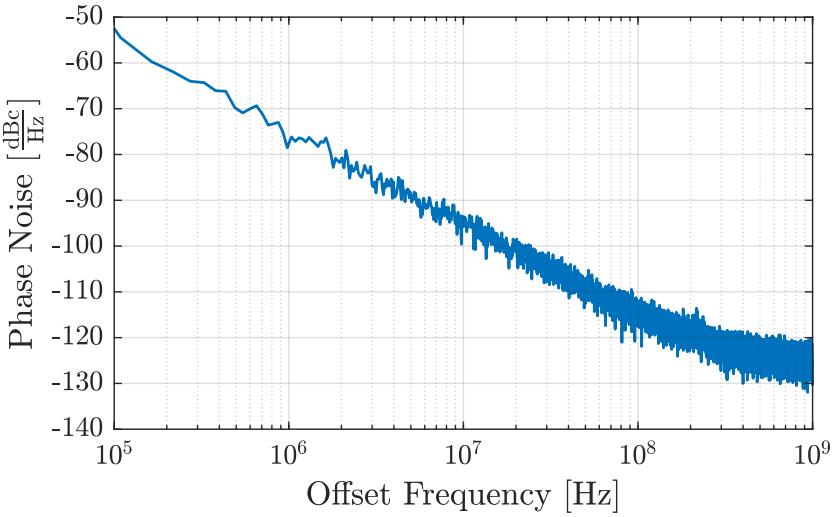

Figure 5.13: Phase Noise (PN) of the VCO operating in $9-13\,\text{GHz}$. The carrier frequency is set to the maximum adjustable values, i.e. the control voltage V_{ctrl} and the supply voltage V_{sup} are set to 1.1 V (see schematic in Figure 4.11).

Table 5.4: Power consumption of the PLLs at different frequency bands. The power consumption of the VCOs is listed in Table 5.2 and is not included in the results presented below.

Frequency Range [GHz]	Power Consumption [mW]
$9-13$	3.6
$13-19$	3.8
$19-26$	11.0
$26-33$	9.6
$33-39$	9.5
$39-50$	9.0

5.4 Phase Locked Loop

The simulation results of the PLL, described in Section 4.6, are presented below. Here, only the relevant parameters of the whole PLL block are considered. The simulation results of the single PLL components, like PFD, CP and divider, are omitted. The VCO, as a more relevant part of the PLL, has been separately presented in previous sections.

The power consumption of the PLL without the VCO is listed in Table 5.4. Here, we can see, that the needed power for PLL at frequencies higher than 19 GHz is larger than at lower frequencies by more than a factor of 2. The reason is the additional power consumption caused by the interstage buffer in the SFD divider, that is implemented in PLLs operating at frequencies higher than 19 GHz (see Figure A.20).

5.4.1 Phase Noise

The comparison of the LO signals regarding the PN is depicted in Figure 5.14. The simulated output signal of the VCO is presented with and without the PLL. As previously mentioned, the targeted precision of the SW frequency measurement is around 20 MHz, i.e. the PN at the offset above 20 MHz from the carrier frequency is more relevant than below. As Figure 5.14 shows, the PN becomes better for the offset frequencies higher than $10-20$ MHz after the PLL is applied to the VCO.

It is to be noted, that a PLL implemented in a fabricated chip normally improves the PN of the VCO more clearly, as it is shown in Figure 5.14. Here, by the extraction of the PN from the VCO without the PLL the control voltage has been applied from an ideal voltage source with a constant value. However, it will not be the case by a fabricated hardware. Hence, the deviation from the carrier frequency becomes larger, due to the variation of the VCO control voltage. Besides, the oscillating frequency of the VCO becomes unknown, if it is implemented without the PLL.

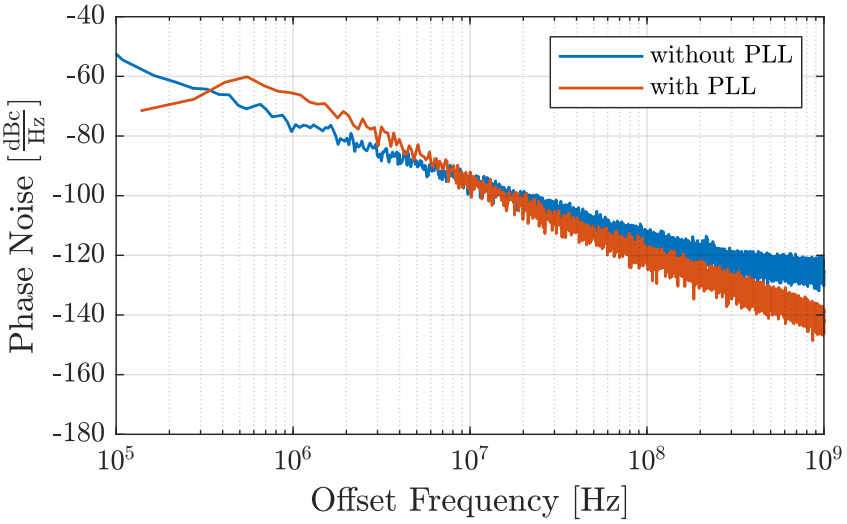

Figure 5.14: Phase Noise (PN) of the LO signal with and without the PLL. The carrier frequency is set in both cases to 10 GHz. The PN at the offset frequency around 10 MHz is almost equal for both cases. For the higher offset frequencies in case with the PLL the PN is improved.

5.4.2 Lock Time

For demonstrating the stability of the PLL, the locking behaviour is investigated. Figure 5.15 shows the transient simulation results of the VCO control voltage. As an example, the oscillating frequencies $14 - 19$ GHz are selected. For demonstrating reasons, the initial values of the control voltages are set to 0.5 V, in order to reduce the simulation time. Here we can see, that the control voltages of the VCO converge

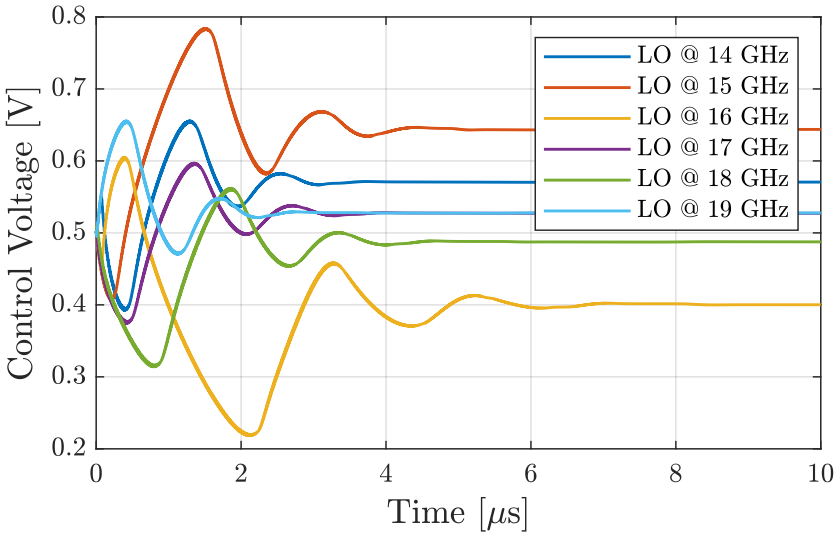

Figure 5.15: The transient simulation results of the VCO control voltage at different frequencies. Figure demonstrates the locking behaviour of the PLL. The reference frequency of the PLL is applied in way, in order to get the integer oscillating frequencies between 14 and 19 GHz of the LO signal.

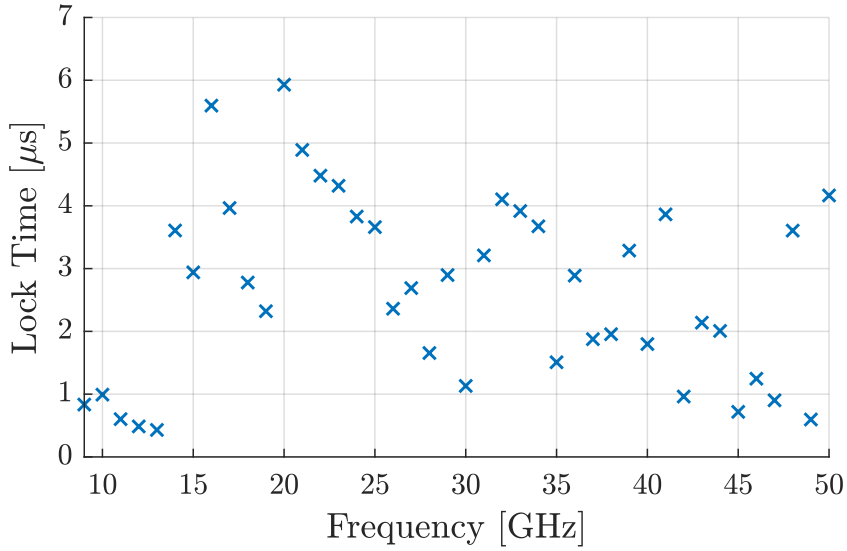

Figure 5.16: The simulated lock time of the PLL for integer oscillating frequencies of the LO signal. The tolerance of the control voltage is set to 5 mV, i.e. the variation of the control voltage is less than 5 mV after the lock time.

to a certain levels depending on the set reference frequency, i.e. the PLL is locked after a certain period of time.

Depending on the application and targeted performance of the PLL, the lock time is defined as the time period after that the control voltage does not exceed a specified voltage tolerance. Here, the tolerance for the control voltage is set to 5 mV, i.e. by a maximum VCO gain of 4 $\frac{\text{GHz}}{\text{V}}$ the targeted frequency resolution of 20 MHz remains valid. Under mentioned conditions, the lock time for the whole frequency range $9 - 50$ GHz with 1 GHz steps has been evaluated and is shown in Figure 5.16. The resulted absolute lock time is less relevant at this point. It is more important that the control voltage converges inside a reasonable time period. Here, the lock time varies in the range between 0.5 and 6 μs.

5.5 Operational Amplifier

To bring the IF signal at the output of the mixer, into the 100 mV range, it has to be amplified by the OpAmp with an appropriate gain and in the required frequency range. Figure 5.17 shows the resulted gain of the OpAmp presented in Section 4.7. The node A and B represent the output of the first stage and the input of the second stage, respectively (see Figure 4.33).

Considering the curve of the node A, it has obviously band-pass characteristic with 20 $\frac{\text{dB}}{\text{dec}}$ attenuation out the band of interest, i.e. band-pass filter of the first order. The high-pass part is realized by DC blocking capacitances C_{1-2}. The low pass component comes from the parasitic capacitance at the node A, generating a pole in the transfer function.

The OpAmp gain from the differential input to the input of the second stage (node B)

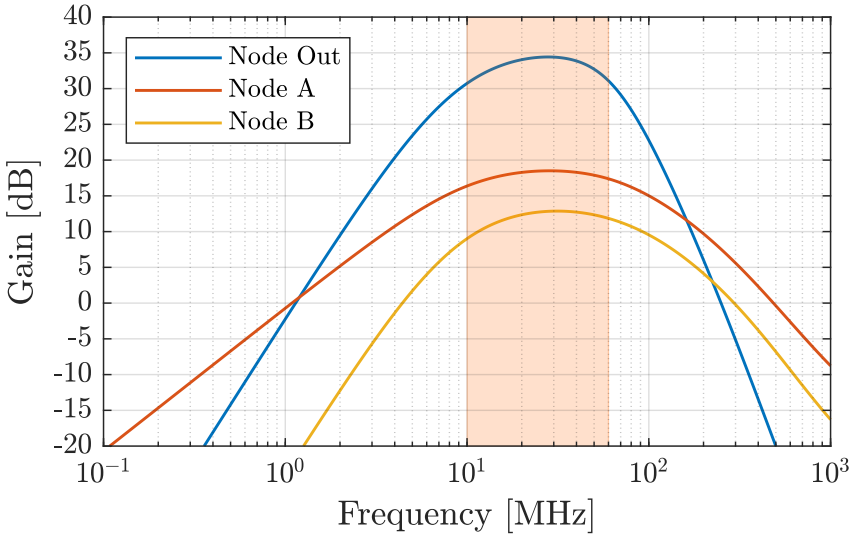

Figure 5.17: Gains of the OpAmp at nodes A, B and Out (see Topology in Figure 4.33). The band-pass characteristic of the second order is apparent. The reduction of the gain from node A to B is caused by the inter-stage buffer. In the desired frequency band $10-60\,\mathrm{MHz}$ the OpAmp achieves a gain higher than $30\,\mathrm{dB}$.

is presented in red. At lower frequencies the high-pass filter of the second order is apparent, i.e. attenuation of $40\,\frac{\mathrm{dB}}{\mathrm{dec}}$. It results from the signal's capacitive coupling through capacitor C_3 (see Figure 4.33). Besides, there is the gain reduction over the whole frequency range, caused by the buffer at the output of the first stage. This drawback of the common-drain circuit is mentioned in the Section 4.7, as well.

Finally, the whole gain of the OpAmp achieves more than $30\,\mathrm{dB}$ in the frequency range $10-60\,\mathrm{MHz}$. Due to the second dominant pole in the transfer function, caused by the parasitic gate-source capacitance of the CS transistor T_8, the low-pass part becomes a filter of second order.

Chapter 6

Spin Wave Characterization

This chapter shows the main goal of the performed research, i.e. the concept for the characterization of the SW devices with an IC in regards to the SW frequency, amplitude change and phase shift. The assumed model of the SW transducer is an on-chip loop antenna, sensing the magnetization coming from the SW device (see Section 2.3).

The simulation results, presented in the following sections, has been achieved with the CMOS circuitry described in Chapter 4. However, the regulating part of the PLL is omitted, due to enormous simulation time of several months without bringing additional insights for the SW characterization, i.e. only the VCO is used to generate the LO signal. Nevertheless, it has to be kept in mind, that the PLL is necessary part to adjust and regulate the frequency of the LO signal in a fabricated IC chip.

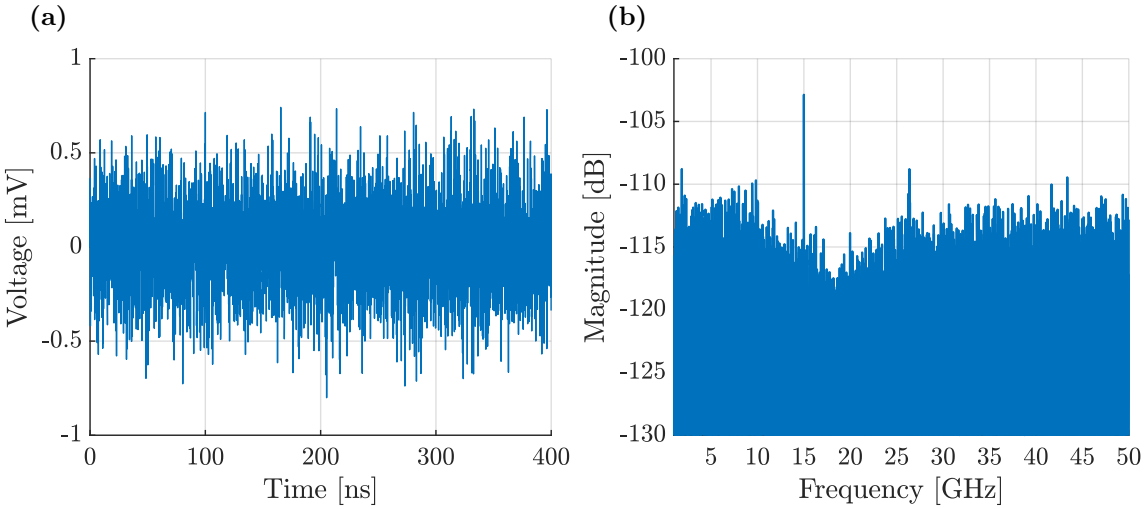

Figure 6.1: Voltage signal of the SW transducer model in time (a) and frequency (b) domain. The applied frequency is equal to 15 GHz. The amplitude is set to 10 μV. The thermal noise results in from the 50 Ω resistance of the loop antenna (see Section 2.3).

The simulation setups for the frequency, amplitude and phase represent a nominal case of electronic devices at room temperature of 27 °C and supply voltage of 1.1 V. Besides, Cadence Virtuoso tool provides the possibility to examine the effects of large signal noise on the designed circuitry, in order to see the impact of the noise in time domain simulations. For the simulations described in the following sections the noise between 1 Hz and 100 GHz has been activated, i.e. the thermal noise and 1/f noise of all electronic devices are considered in the presented results.

Figure 6.1 shows the voltage in time and frequency domain, generated by the model of the loop antenna with the thermal noise, caused by the 50 Ω resistance. The depicted input signal of the readout circuitry should demonstrate the challenge of the signal reconstruction and making statements regarding the frequency, amplitude and phase of the SW. It is quite obvious, that the bandpass filtering of the desired signal is indispensable.

6.1 Frequency

In order to verify the concept for the frequency measurement of the SWs with the proposed readout circuitry, freely selected frequencies at the circuitry input has been assumed. As mentioned in previous chapters, the targeted 9 − 50 GHz are subdivided in 6 frequency parts with its own circuitry. Thus, for each part a sinusoidal transducer signal with a certain frequency has been assumed: 10 GHz, 15 GHz, 20 GHz, 30 GHz, 35 GHz, 45 GHz. These transducer signals emulate the SWs with frequencies listed above. The amplitude of the applied signals are equal to 10 μV, i.e. the signal power of −90 dBm in case of 50 Ω impedance of the transducer.

The question arises, can the applied frequencies at the input be derived from the

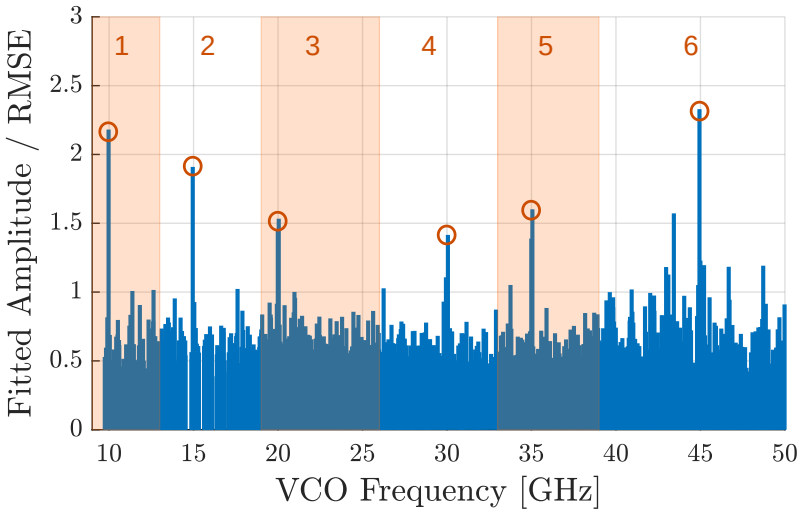

Figure 6.2: Simulation results for the SW frequency measurement. The output of the VCO signal, LO, is swept between 9 − 50 GHz with steps around 20 MHz. The maxima in each of the 6 frequency bands correspond to the applied frequencies of the input signals assumed in the loop antenna.

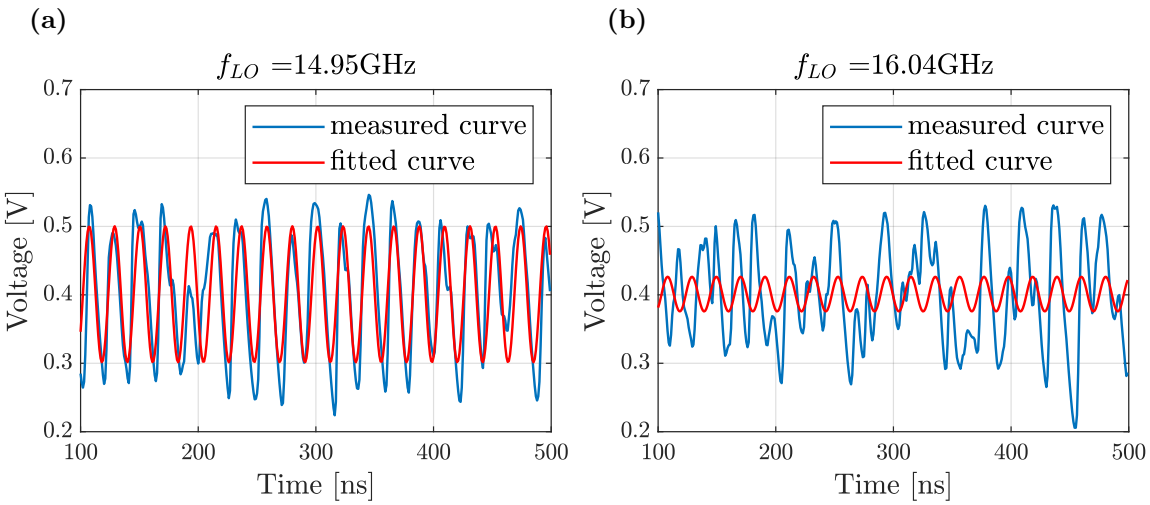

Figure 6.3: Transient simulation results for the readout circuitry outputs and its fitting curves resulted from post signal processing in MATLAB. Two frequencies of the LO signal 14.95 GHz (a) and 16.04 GHz (b) are considered. It demonstrates, that small frequency differences ($10 - 60$ MHz) between RF and LO signals can be recognized (a) by configured fitting tool. As targeted for larger frequency difference (b), the measured and the fitted curves do not match with each other.

signal measured at the output of the OpAmp. Through the mixing the RF and LO signals the IF signal can be generated at the lower frequencies and amplified by the OpAmp with bandpass characteristic. For that case, the frequency of the LO signal has to be swept from $9 - 50$ GHz. As soon as, the frequency difference between RF and LO signal is small enough ($10 - 60$ MHz), the required frequency measurement of the SWs can be achieved. For each frequency sweeping step of the LO signal the transient analysis has been applied for 500 ns.

Simulation result for the SW frequency measurement is depicted in Figure 6.2. For each of the 6 frequency bands the maximum peaks at the applied frequencies are obvious, showing the prove of the SW frequency reconstruction with used methodology. For the frequency reconstruction the transient signal at the output of the OpAmp has been additionally applied for the post signal processing in the software tool MATLAB. In the first step, the simulated output signal has been fitted to a sinusoidal curve of the first order with the limits for the frequency in the range $1 - 100$ MHz. After that, the amplitude of the fitted curve has been divided by the Root Mean Square Error (RMSE). The RMSE results from the difference between the original and the fitted curves. In other words, the ordinate in Figure 6.2 shows the quality of the fitting to the measured signal at the output of the OpAmp.

An example in time domain for the simulated and fitted curves of the output signals is depicted in Figure 6.3. Here, two different LO frequencies 14.95 GHz and 16.04 GHz have been applied to the readout circuitry. Due to the fact, the frequency of the transducer is set to 15 GHz, the case in Figure 6.3a generates the signal in

the expected frequency range ($1 - 100\,\text{GHz}$). Thus, the MATLAB algorithm can easily find an appropriate ideal sinusoidal curve of the first order. For the second case in Figure 6.3b the difference between the RF and LO signals is around 1 GHz, i.e. this frequency component is attenuated by the OpAmp with the band pass filter characteristic in $10 - 60\,\text{MHz}$ range. Consequently, there is no distinct frequency component with enough signal power to be recognized. Only, the amplified noise of the whole readout system is considered at the output of the OpAmp.

6.2 Amplitude

To measure the absolute amplitude of a detected signal is very difficult, i.e. for the SW readout circuitry the exact gains of the components (LNA, Mixer, etc.) have to be known. Due to the process variation of the IC, the DC operating point of the circuitry has to be calibrated after the fabrication. However, the change of the amplitude with respect to a reference signal can be detected easier. To visualize the performance of the designed readout circuitry, the change of the amplitude in the transducer is assumed and the fitted amplitude at the output is considered, as depicted in Figure 6.4.

For the fitting of the simulated transient signal at the output of the readout circuitry to an ideal sinusoidal curve, the same approach has been done as described in the previous Section 6.1. The frequencies of the RF and LO signals are set to 20 GHz and 20.04 GHz , respectively. Thus, the RF signal is down-converted to 40 MHz. The induced amplitude in the near field SW antenna is varied in the range $1 - 50\,\mu\text{V}$ or $-100\,\text{dBm}$ to $-76\,\text{dBm}$ signal power (see Figure 6.4). The detected amplitude of the fitted curve is plotted on the y-axis.

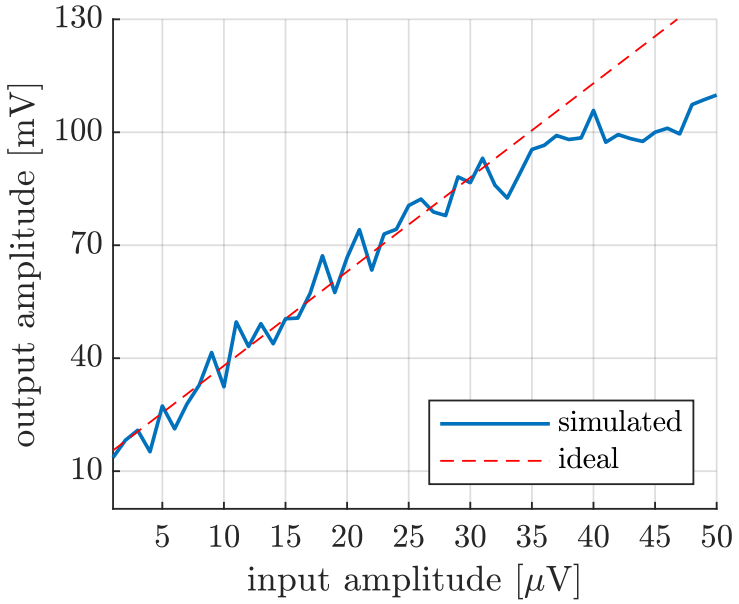

Figure 6.4: Amplitude change at the output of the SW readout circuitry due to the applied variation of the signal power at the input. The gain of the circuitry remains relatively linear till $30\,\mu\text{V}$, as the comparison with the ideal curve shows.

The important message of the simulation results is the fact, that the signal power below −90 dBm (below 10 μV amplitude) picked up by the antenna could be detected by the circuitry. Due to the noise of the whole system, the simulation results show a deviation from the ideal curve. The signal amplification remains relatively linear till 30 μV and saturates for higher input signal power due to the leaving the DC operating point of the OpAmp. However, the linearity of the readout circuitry can be easily adjusted for higher input signal power, as well. The simulated curve in the linear region is approximated by Equation 6.1

$$y = 2.5\frac{\text{mV}}{\mu\text{V}}x + 13\text{mV}. \tag{6.1}$$

The maximum deviation from the ideal curve in the linear region is around 10 mV, i.e. a detection of amplitude change in the antenna would be possible with the resolution of around 2.5 μV. It comes from the fact, that the voltage gain of the whole readout system is around 72 dB.

6.3 Phase

The same approach, as for the amplitude measurement, is applied for the SW phase shift measurement. Instead of amplitude change in the model of the SW transducer, the initial value of the phase is changed. The considered transient signal at the output of the readout circuitry is fitted to an ideal sinusoidal signal of the first order. The frequency of the input RF and LO signals are set to 20 GHz and 20.04 GHz, respectively.

The resulted phase shift of the simulated curves and an ideal one are depicted in Figure 6.5. Here, two different input amplitudes 10 μV and 20 μV are considered. Whereas, the maximum deviation of the phase for the 10 μV case is 37.8°, for the input amplitude of 20 μV improves the phase resolution to 24.2°. The reason is quite obvious, the SNR in the case with 20 μV amplitude at the input is higher than for the 10 μV one. Consequently, it results in a lower PN of the readout system. Besides, it is important to mention, that the phase shift, resulted from the signal propagation trough the readout circuitry, is subtracted from the presented results for better comparison with the ideal curve.

The proposed methodology for the phase measurement cannot deliver a real-time phase information of the signal induced in the loop antenna. Due to the down-conversion of the RF signal to the IF signal, the absolute phase information is going lost. However, the proposed approach can be used to compare the phase shift between two simultaneously measured signals coming from a SW device. In a SW readout system with two or more on-chip transducers the phase difference of two sinusoidal signals with the same frequency can be detected.

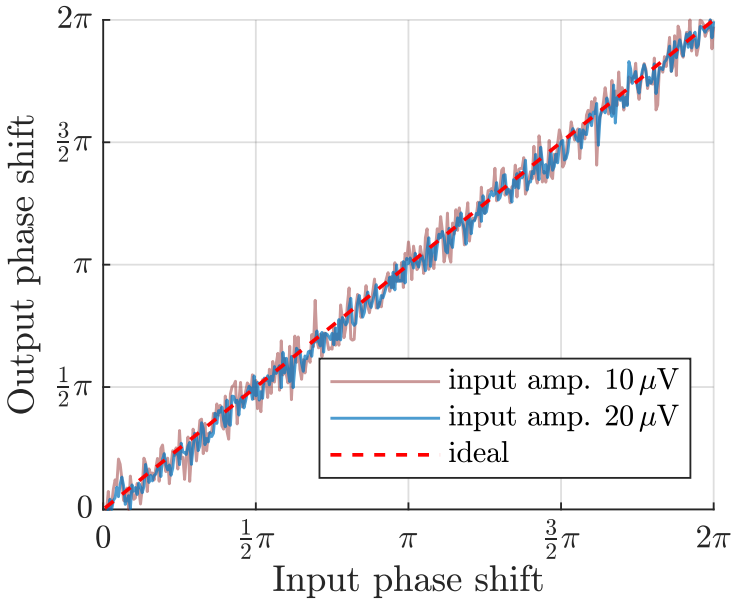

Figure 6.5: Phase shift measurement with the SW readout circuitry for two different input amplitudes 10 μV and 20 μV. The y-axes shows the phase shift considered at the output of the circuitry by applying a phase shift in the readout antenna. Comparison with the ideal curve reveals the deviation of the simulated results cause by the noise.

Chapter 7

Impact of Interconnect Parasitics

The simulation results presented in previous Chapter include the parasitics of all electronic devices. However, the parasitic capacitances and resistances originated from interconnects between the electronic devices have not been considered yet. Due to relatively high operating frequencies in tens of GHz range, the performance of the readout circuitry significantly depends on the parasitics of the wiring. In order to estimate the performance degradation due to non-ideal interconnects, the LNA designed for $19 - 26\,\mathrm{GHz}$ operation has been selected for the layout design.

Starting from the initial device dimensions achieved for the nominal case (see Figure A.4 in Appendix A.1), the resulted interconnect parasitics, extracted from the layout, deteriorated the performance of the readout circuitry too much. Hence, a redesign of the device dimensions was required. The redesigned version of the LNA operating in $19 - 26\,\mathrm{GHz}$ can be find in Appendix in Figure A.4. In general we can say, the additional interconnect capacitances shift the gain and input matching to lower frequencies. Thus, the dimensions of the transistors have been partly decreased, to compensate for the increased parasitic capacitance of the wiring by decreasing the parasitic capacitances of the electronic devices. Besides, the parasitic interconnect resistance in the signal path has a negative impact on the noise performance of the LNA. Thus, the wires have to be wide enough to lower the sheet resistance and small enough not to critically increase parasitic capacitance.

The voltage gain of the LNA for initial design and layouted version are compared in Figure 7.1. As expected, the gain of the layouted version of the LNA shows worse results. The maximum gain decrease is around $5\,\mathrm{dB}$. Nonetheless, the voltage gain still remains at an acceptable level above $23\,\mathrm{dB}$ between $19 - 26\,\mathrm{GHz}$. Besides, the filtering of the frequency components outside the bandwidth of interest becomes even better for the layouted design.

The targeted input matching of the LNA to the $50\,\Omega$ is $-10\,\mathrm{dB}$, as already mentioned in Section 3.2. Figure 7.2 shows that the S_{11} parameter of the layouted schematic version becomes higher, i.e. less input matching is achieved. However, the S_{11}

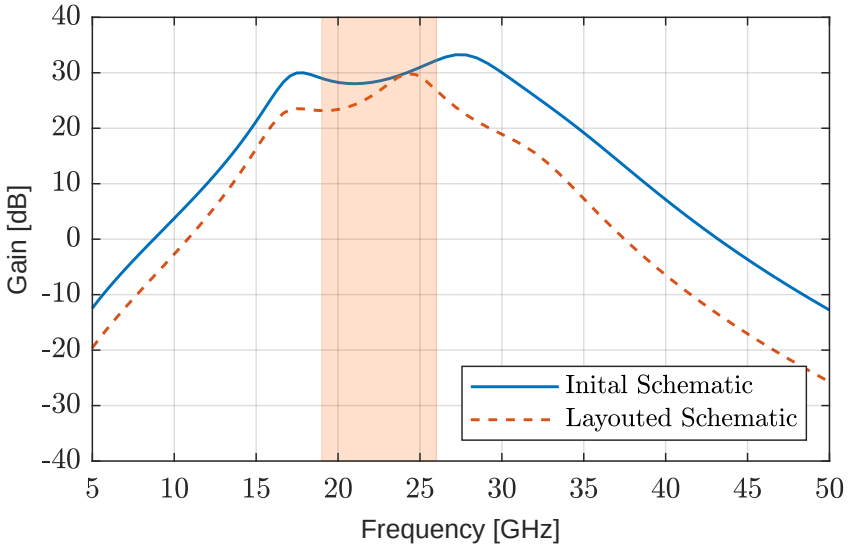

Figure 7.1: Voltage gain of the LNAs designed for the frequency range 19 − 26 GHz. The curve in blue shows the gain performance of the initial design. The redesigned version considering interconnect parasitics is depicted in the dashed curve.

magnitude remains below −10 dB in the almost whole frequency range of 19 − 26 GHz. A better input matching could be achieved, however at costs of worse gain and lower NF.

The most painful performance impairment of the LNA due to the interconnect parasitics is the NF. It becomes approximately 1 dB higher, as depicted in Figure 7.3. The NF has the most impact on the sensitivity in the detection of the SW signal.

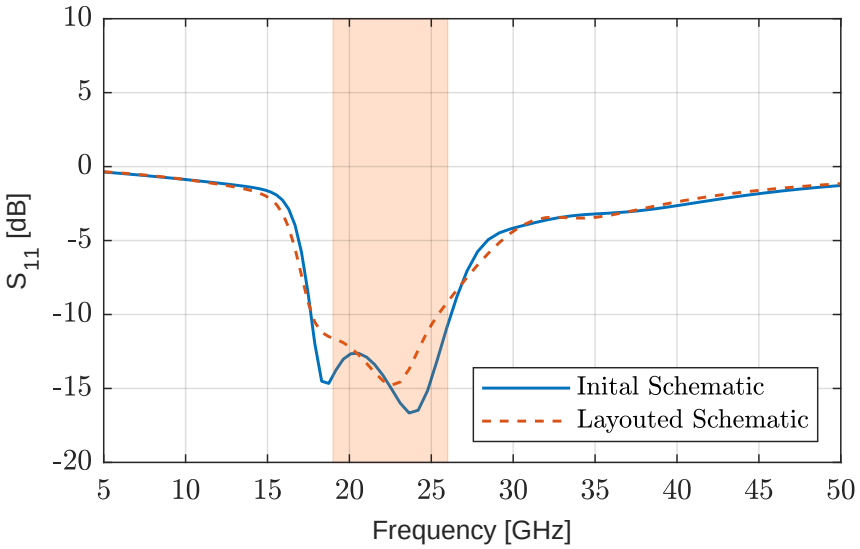

Figure 7.2: Pre- and post-layout simulation results of the input matching parameter S_{11}. The targeted performance below −10 GHz is almost achieved in the whole band of interest 19 − 26 GHz for both cases.

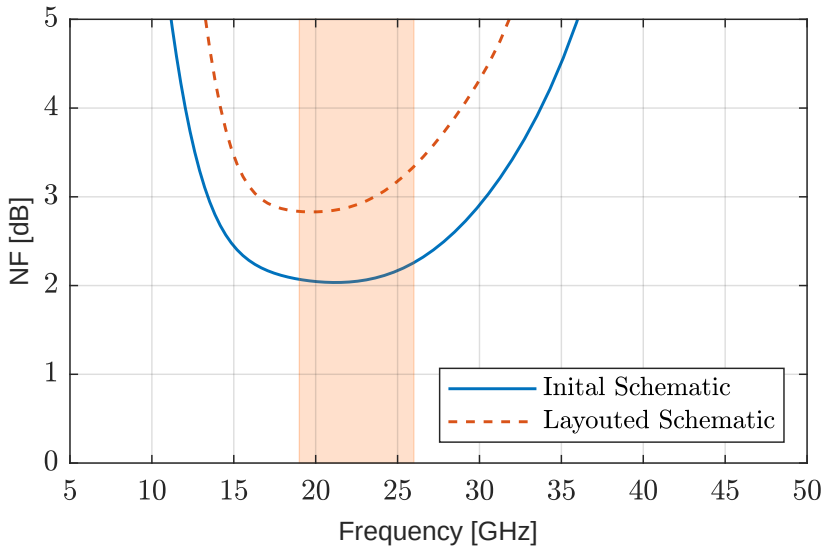

Figure 7.3: Noise Figure (NF) degradation of the LNA due to extracted interconnect parasitics resulted from the layout. The simulation results show 1 dB higher NF for the extracted schematic.

However, the resistance of the wires and vias between the electronic devices always remains one of the limiting factors for a better detection. One of the possibility to reduce the NF of the presented LNA is the lowering of the transducer's resistance in order to reduce its thermal noise.

For the sake of completeness, Figures 7.4 and 7.5 show the stability performance of the LNA. Here, it is important to see, that the stability parameters K and B_1 remains above potentially unstable regions for all frequencies, i.e. K and B_1 have to be greater than 1 and 0, respectively. The reader is referred to Section 3.6 for more background regarding the stability parameters.

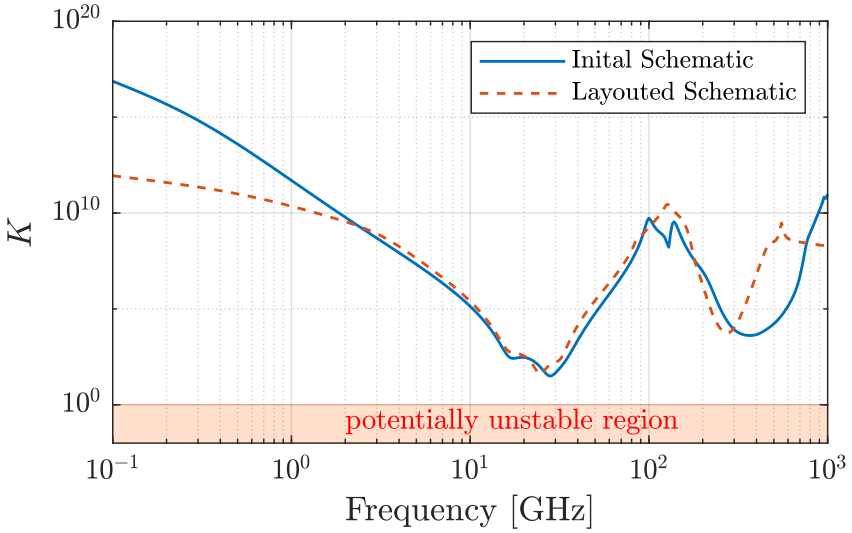

Figure 7.4: Stability factor K of the pre- and post-layout schematic. The simulation results show, the LNA still remains stable after the redesign.

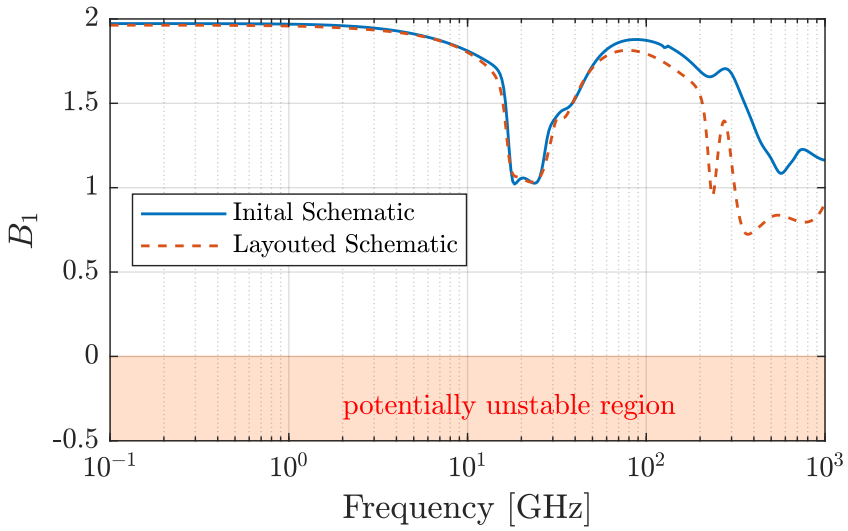

Figure 7.5: Stability factor B_1. The curves for both initial and layouted schematic are in the stable region.

The designed layout of the LNA operating in $19-26\,\mathrm{GHz}$ is visualized in Figure 7.6. It can be seen, that the most area is consumed by the seven inductors, taking more than 90 % of the used area. The wires of the positive supply voltage, vdd, and negative supply voltage, gnd, are chosen wide enough to decrease the sheet resistance of the wires. Besides, the top metal layer, having the largest metal thickness, have been used for the supply. The interface to the outside of the chip is not designed, i.e. there is no chip pads and the Electro Static Discharge (ESD) components. Thus, in the proposed layout only the interconnect parasitics between the electronic components of the LNA are included.

It is important to mention, that for the parasitic extraction from the layout, the minimum considered resistance and capacitance are equal to $1\,\mathrm{m\Omega}$ and $10\,\mathrm{aF}$, respectively. The extraction of the parasitic inductances, in order to estimate Electro-Magnetic (EM) losses, has not been included in the presented results above.

The presented simulation results in this chapter show first order estimation of the interconnect parasitics and its influence on the circuitry performance. The connection to the input and the power supply of the LNA is not assumed as a transmission line like microstip or co-planar waveguide. The 2.5- or 3-dimensional EM simulation of the passive electronic devices and of the whole layout are not included, as well. Consequently, the losses from the inductors to the silicon substrate and the undesired noise coupling from the substrate to the inductors are not considered. The software tools like Advance Design System (ADS) momentum from Agilent or High-Frequency Structure Simulator (HFSS) from Ansis could provide the required environment for EM simulations. Some insights regarding the LNA design at mmWave frequencies with applying the EM simulations are elaborated by Rashtian [123].

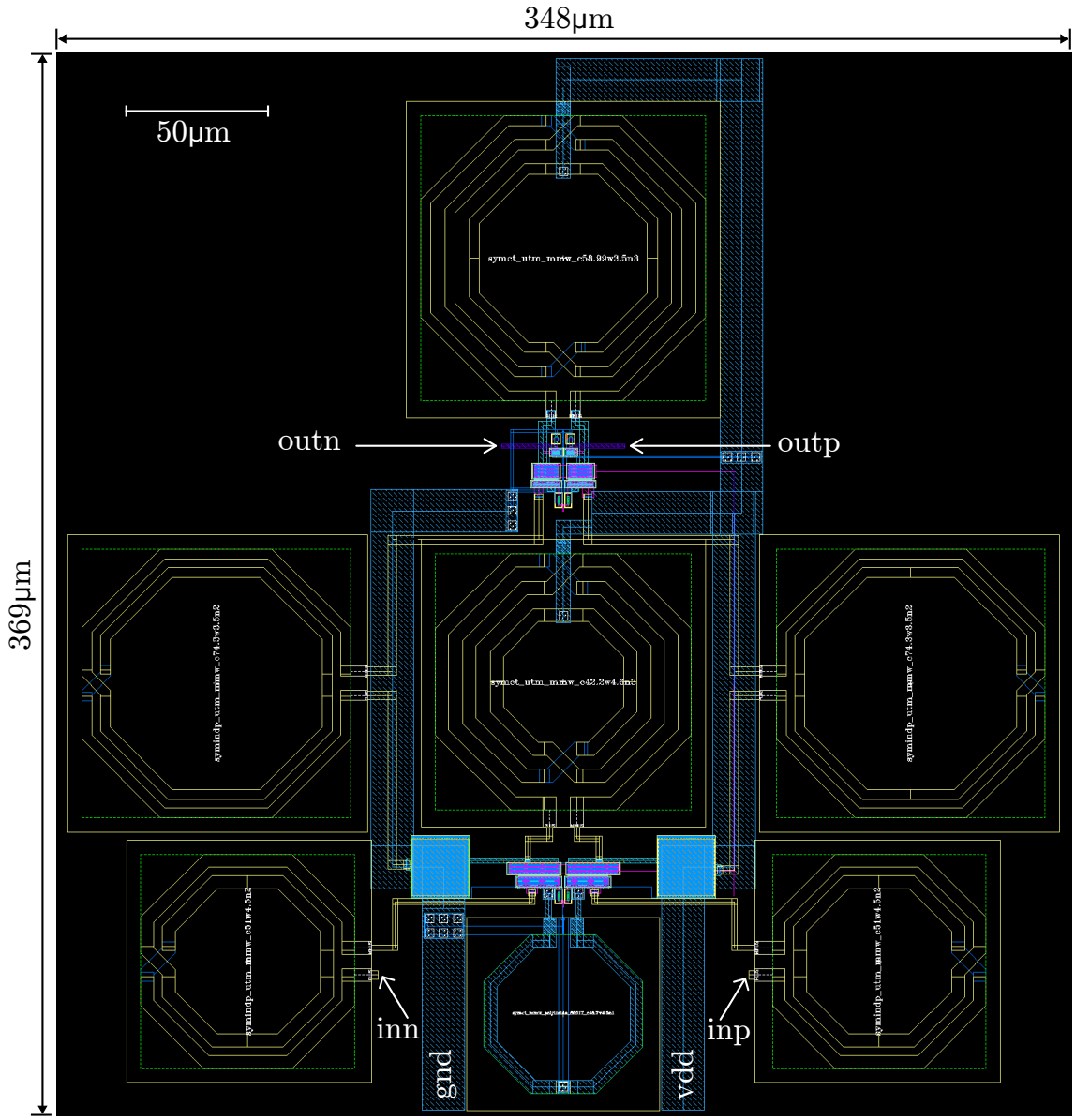

Figure 7.6: Layout of the LNA operating in the frequency range $19 - 26\,\mathrm{GHz}$. The negative and positive inputs are marked with *inn* and *inp*, respectively. Similarly, it is applied for the output of the LNA. The positive and negative supply voltage is indicated by *vdd* and *gnd*, respectively. The schematic of the circuitry with electronic device dimensions can be found in Figure A.4.

Chapter 8

Conclusion

8.1 Summary

The main motivation of this work was to find a solution for the on-chip characterization of SWs or SW devices, as additional alternative to currently known measurement setups with Brillouin Light Scattering (BLS) or Vector Network Analyzer (VNA). Moreover, the on-chip detection of SWs has not been demonstrated yet. However, the integration of SW devices with the widely-used CMOS technology will be definitely required, in order to bring magnonics from the labs into potential applications. The proposed CMOS readout circuitry in this work proves on simulation level the feasibility of characterizing SW devices regarding their frequency, amplitude change and phase shift. It offers a summary of some fundamentals, ideas and insights required for the on-chip SW characterization and should serve as a starting point towards the realization of an IC for SW devices.

The implementation of an effective interface between a SW device and electronic components remains the biggest challenge in bringing SW devices into production ready applications. Some of the commonly known SW receiver transducers have been briefly described. Each of the SW sensing elements has its pros and cons. However, for the on-chip detection the selected near-field loop antenna represents a relatively simple low-ohmic solution and can be scaled with steadily improving capabilities in chip manufacturing. Based on the derived model of the loop antenna, a readout circuitry has been developed for analyzing inductively coupled SW signals. Moreover, the proposed readout system can be modified for other magneto-resistive SW sensing elements.

The readout circuity is designed using the 40 nm CMOS RF technology provided by GlobalFoundries. The general working principle of the circuitry is firstly to amplify the transduced SW signal at RF and mmW frequencies ($9 - 50\,\mathrm{GHz}$), secondly, to down-convert to lower frequencies and finally, to digitize the amplified IF signal, in order to make a statement about the SW signal properties. The digitization of the electronic signal was not considered in this thesis. The analysis of the SW signal is done at the output of a low frequency amplifier (OpAmp).

To cover the targeted SW frequency range of $9 - 50\,\text{GHz}$, the readout circuitry has been divided into 6 frequency bands. For each frequency band the appropriate receiver components such as the LNA, mixer, VCO with PLL and OpAmp have been designed. The functionality of the building blocks and the whole SW characterization is demonstrated on the simulation level in design environment of Cadence Virtuoso. The proposed readout concept shows that the SW signal reconstruction is feasible, assuming an induced signal power of $-90\,\text{dBm}$ in the $50\,\Omega$ loop antenna.

Depending on the considered frequency band, the power consumption of the readout circuitry varies in the range of $50 - 70\,\text{mW}$ with the LNAs contributing around 90%. At first glance, the relatively high power consumption of the SW readout circuitry diminishes one of the main advantages of SW devices targeted for low power applications. However, by designing a SW readout circuitry for more narrow band applications, the power consumption can be significantly reduced. With an appropriate optimization effort, values below 10 mW for the whole readout circuitry are feasible.

The demonstrated simulation results of the receiver circuitry are achieved with realistic electronic component models, i.e. the parasitics of each device are included in the presented results. However, the interconnect parasitics between the devices are ignored. It is undeniable, that at high operating frequencies the wiring significantly impacts the circuitry performance. Hence, for one selected LNA, operating in $19-26\,\text{GHz}$, the layout of the circuitry has been done and the first order performance degradation is demonstrated.

8.2 Future Perspective

We should be aware, that the proposed circuits with all listed dimensions of the electronic components in Appendix A are not tape-out ready designs. Additionally, the control and supply electronics have to be developed before the submission for a Multi Project Wafer (MPW). As mentioned in Chapter 4, the bias circuitry [74, 85] for the designed SW readout components is still required. Besides, the common mode feedback for the proposed fully differential LNA [62, p. 389] is essential for the adjustment of the DC operating point.

The operating frequency of the readout circuitry has been fractioned into 6 frequency bands, that are covering $9 - 50\,\text{GHz}$. To avoid deterioration of the performance, the switches or multiplexers in the signal paths have been omitted. This also means, that the circuits operate separately from each other at different frequency bands. The introduction of multiplexers between the receiver components such as transducers, LNAs, mixer and VCOs could be considered, in order to reduce the chip area. However, a more careful design is required to avoid additional noise sources of the multiplexers. Thus, to reduce the effort and the design time, a focus on a single frequency band is advised. For instance, the K-band ($18 - 27\,\text{GHz}$) could be considered, due to relatively rare demonstrations of the SW devices operating at these frequencies. Besides, some know-how published for automotive radar applications

in K-band [125–127] could be adopted for the SW on-chip characterization.

Another essential IC development step are the Monte-Carlo (MC) and the corner simulations of the circuits. The simulation results presented in Chapter 5 show the typical performance of the designed SW readout components. However, manufactured integrated circuits exhibit a statistical variation of their performance due to temperature change, supply variation, geometric and doping mismatch, surface-state charges, oxide thickness imperfection and many more [128]. Statistical simulations of the circuits are crucial for the estimation and, if necessary, for increasing the yield of the ICs.

The layout of the readout circuitry is a necessary step towards manufacturing chips. After the extraction of the interconnect parasitics from the layout, a better estimation of the circuitry performance can be made. The influence of the parasitic inductances and capacitances are more significant at mmW frequencies than at lower frequencies, due to the fact that the parasitics reach the same order as values of the selected passive electronic devices of a circuit. Consequently, the resonant frequency of the LNA and mixer can be shifted to undesired frequencies. The same occurs for the oscillating frequency of the VCO. Thus, in addition to the typical RC extraction, known in traditional IC analog design, 2.5 and 3-D EM simulations are required when designing RF and mmW circuits. Besides, if the dimensions of the interconnects become greater than $\frac{1}{10}$ of the signal wave length, transmission lines have to be implemented for the signal propagation. Moreover, to avoid crosstalk, sensitive wires should be shielded. It has to be kept in mind, that after the first layout design, several redesign iterations are required to achieve the desired results. [108, pp. 36-41]

The resistivity of the substrate material significantly contributes to the signal losses of passive RF components such as transmission lines, transformers and inductors. A low resistivity of the substrate provides an undesired path for RF and mmW signals. Besides, a parasitic eddy current below the inductors can be induced [108, pp. 42-43]. To tackle this issue, the foundry provides boron fluoride implants, so-called BF-Moats, for the used 40 nm CMOS process, in order to increase the substrate resistivity. Thus, the noise coupling is reduced and the quality factor of inductors is improved. Another possibility to gain a highly resistive substrate is to use Silicon-on-Insulator (SOI) technology, which is often used for RF and mmW IC designs [1]. GlobalFoundries offers the 22 nm SOI process, that could significantly improve the performance of the SW readout circuitry [129]. However, the increased costs for manufacturing test chips should be taken into account.

By designing the layout for RF and mmW circuits, close attention has to be paid to the routing of the power supply. It is common practice, also at lower operating frequencies, to separate the power supply of the digital and analog circuitry parts, in order to avoid or minimize the cross-talk from the digital part to the analog part during switching events. However, at high frequencies the separation or shielding of the power supply inside the analog part of the chip is additionally required, in order to prevent EM coupling. Some of the RF grounding techniques are described by Cheema in [108, pp. 44-48]. Besides, the required bond wires for

the supply nodes influence the performance of the circuitry, especially the matching of the LNA, as addressed in [61, pp. 284-296], [123]. When using several supply domains, the IC designer should not forget to build in protection circuitry such as clamping diodes, which are dedicate to preventing transistor damage in case of a larger difference in the electrical potential at the interface of the two different supply domains. Similar considerations should be made for the ESD protection of all chip pads [130, 131].

It is finally to be noted, that the receiver part of the SWs has been considered in this work. However, the excitation of SWs could also be realized with an IC. On the long run, a system with electronic components for the on-chip generation and reception of SWs has to be demonstrated, in order to see the whole potential and competitive advantage of SW devices in certain applications compared to pure CMOS technology. To achieve this ambitious goal, a close cooperation of physicists from the magnonic community, IC circuit design institutes and the semiconductor industry is essential and unavoidable.

Appendix A

Schematics with Electronic Device Values

Schematics on transistor level of all implemented building blocks for SW characterization are presented below. The relevant electronic device dimension are listed as well, in order to facilitate the reproducibility of the achieve simulation results. The functionality of the presented circuits is described in Chapter 4. The acronyms used in the figures mean: **Length of Finger (LoF), Width of Finger (WoF), Number of Fingers (NoF), Multiplier (M)**.

A.1 Low Noise Amplifier

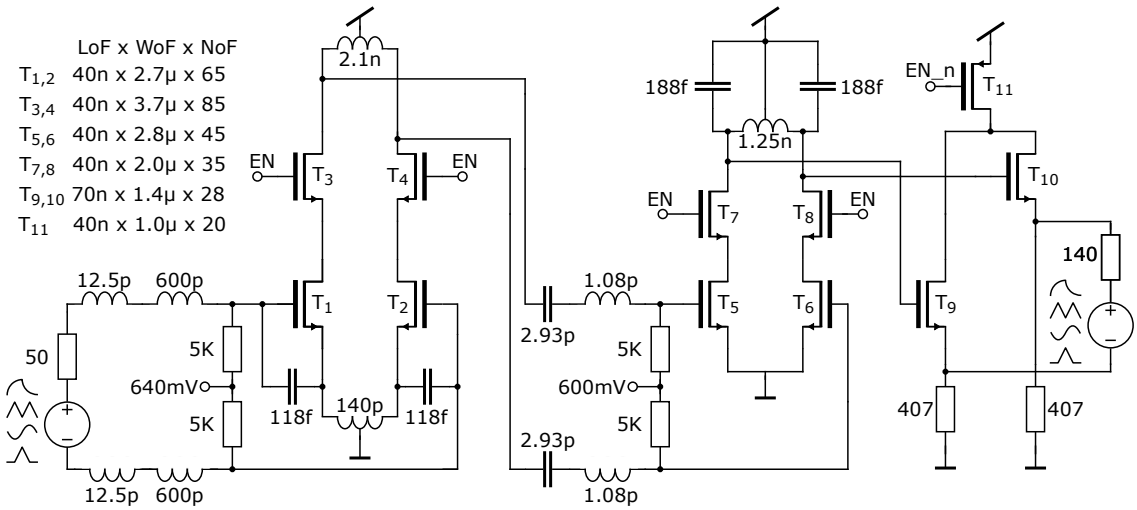

Figure A.1: LNA operating in the frequency range $9 - 13\,\mathrm{GHz}$.

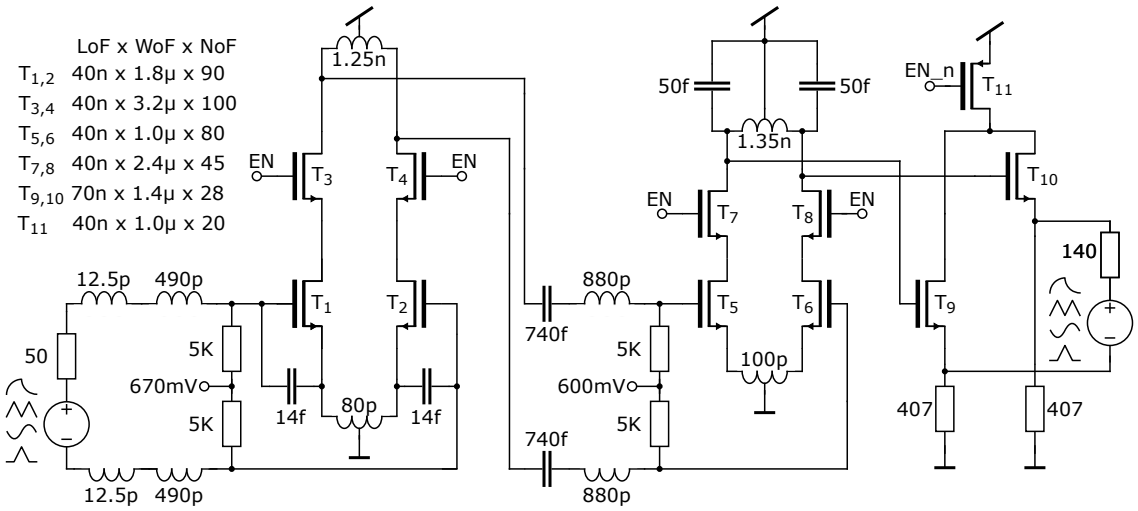

Figure A.2: LNA operating in the frequency range 13 – 19 GHz.

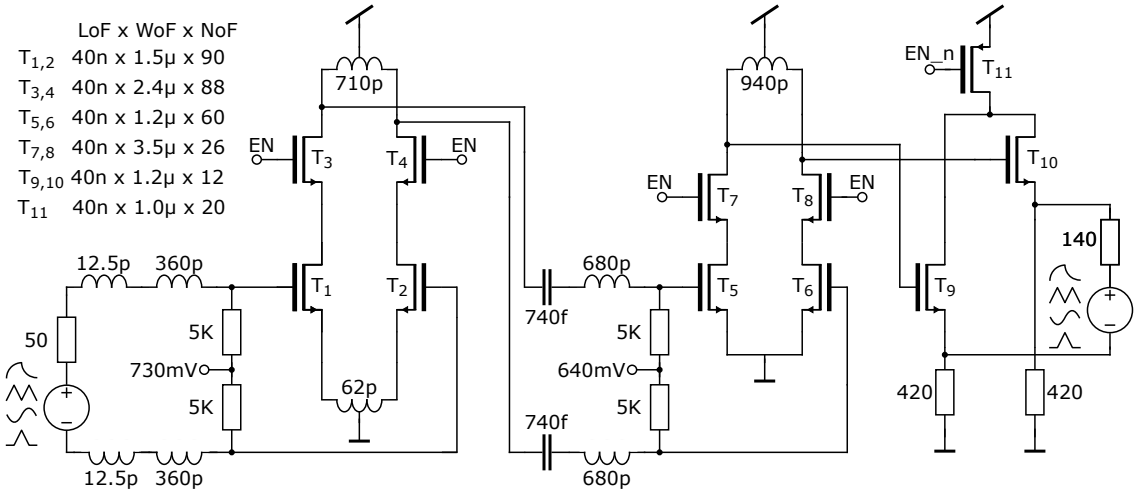

Figure A.3: LNA operating in the frequency range 19 – 26 GHz.

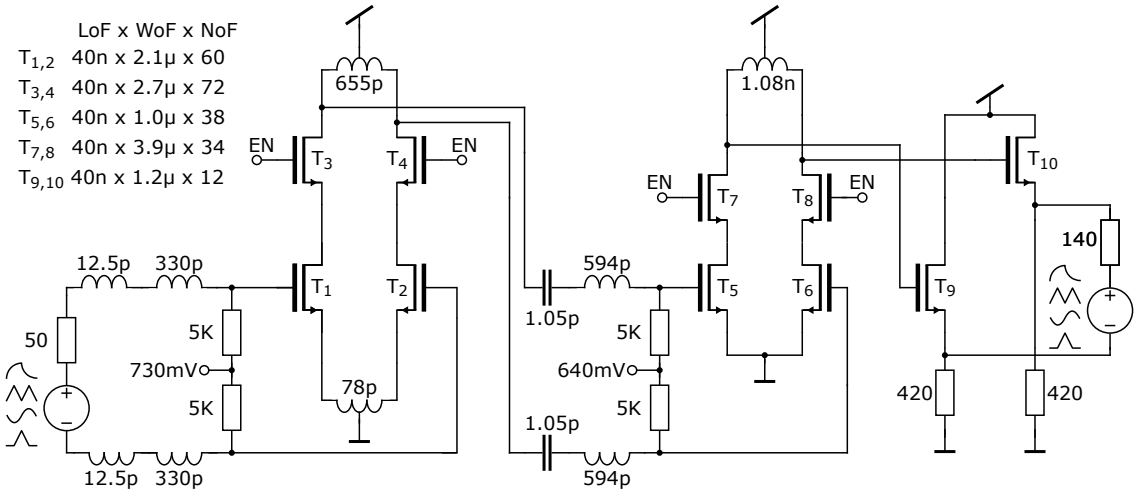

Figure A.4: Redesigned LNA operating in the frequency range 19 – 26 GHz taking into account resistive and capacitive interconnect parasitics.

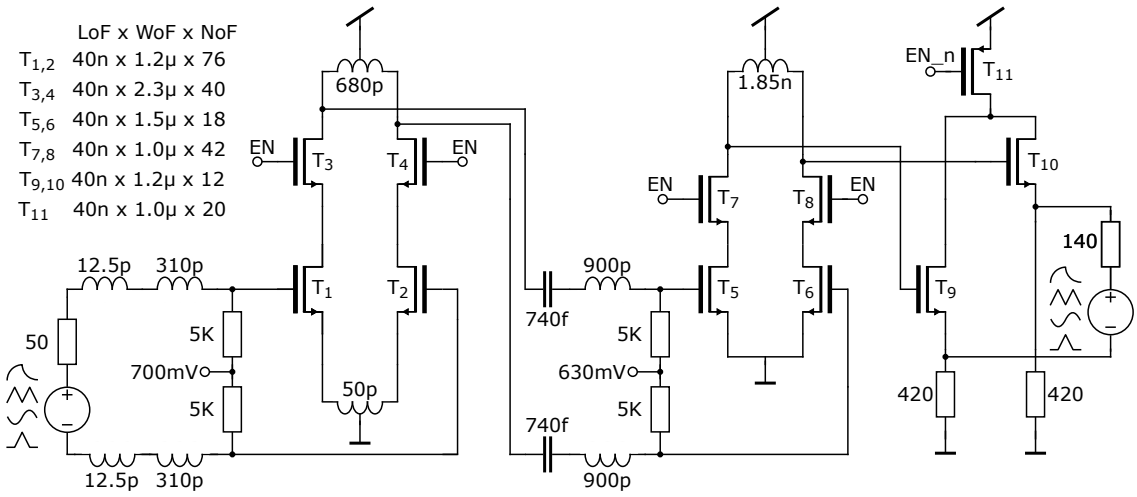

Figure A.5: LNA operating in the frequency range $26 - 33\,\mathrm{GHz}$.

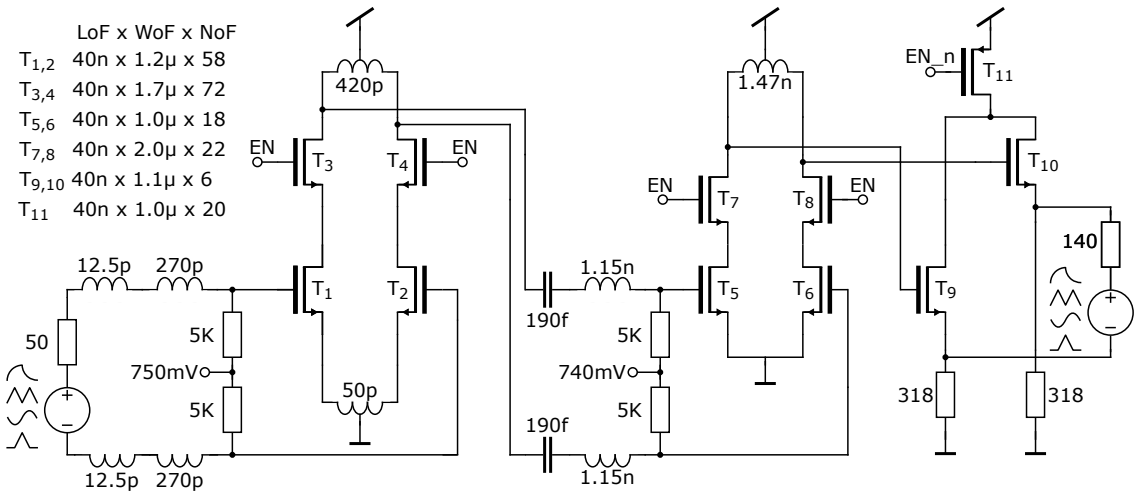

Figure A.6: LNA operating in the frequency range $33 - 39\,\mathrm{GHz}$.

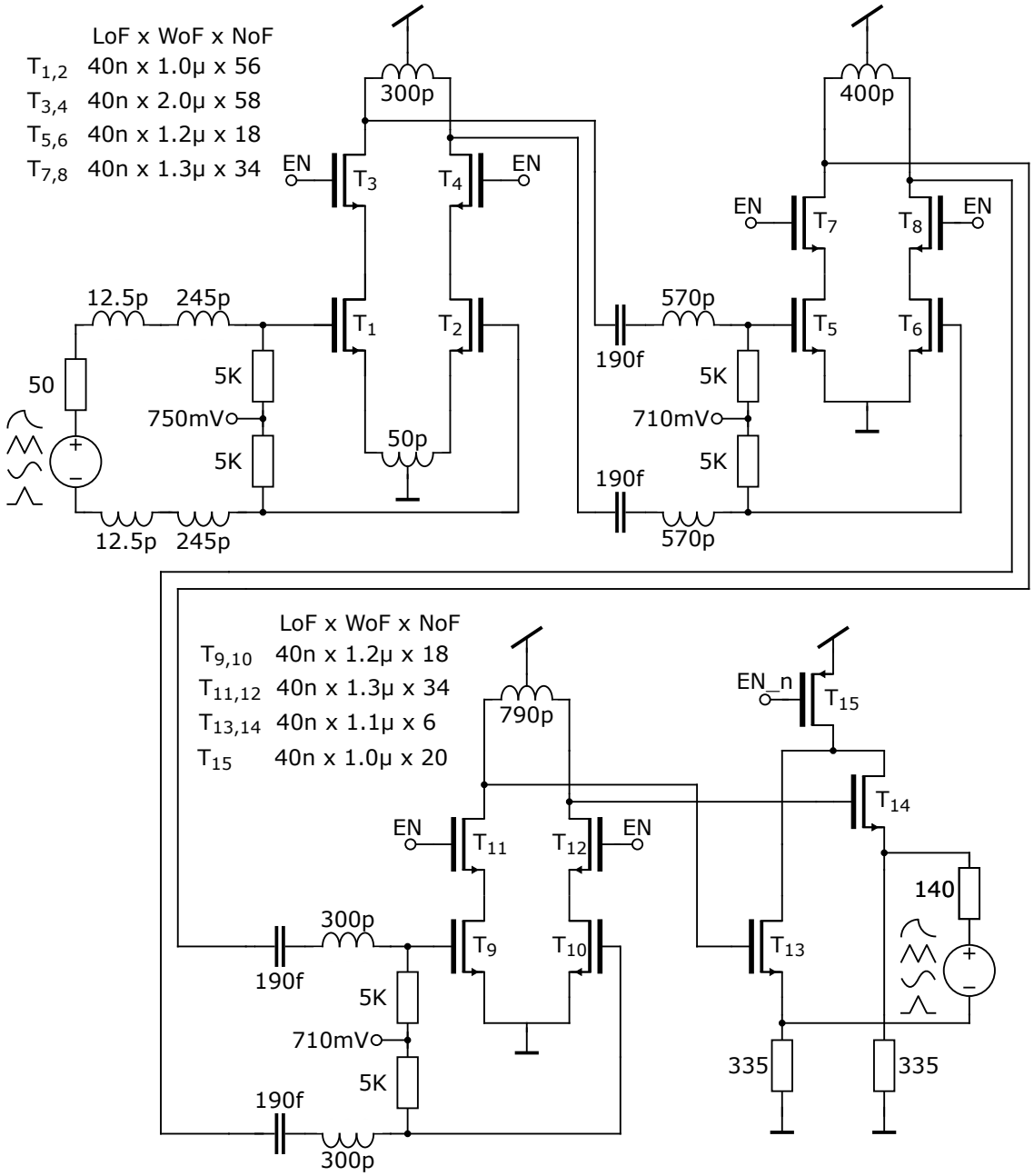

Figure A.7: LNA operating in the frequency range $39 - 50\,\mathrm{GHz}$.

A.2 Mixer

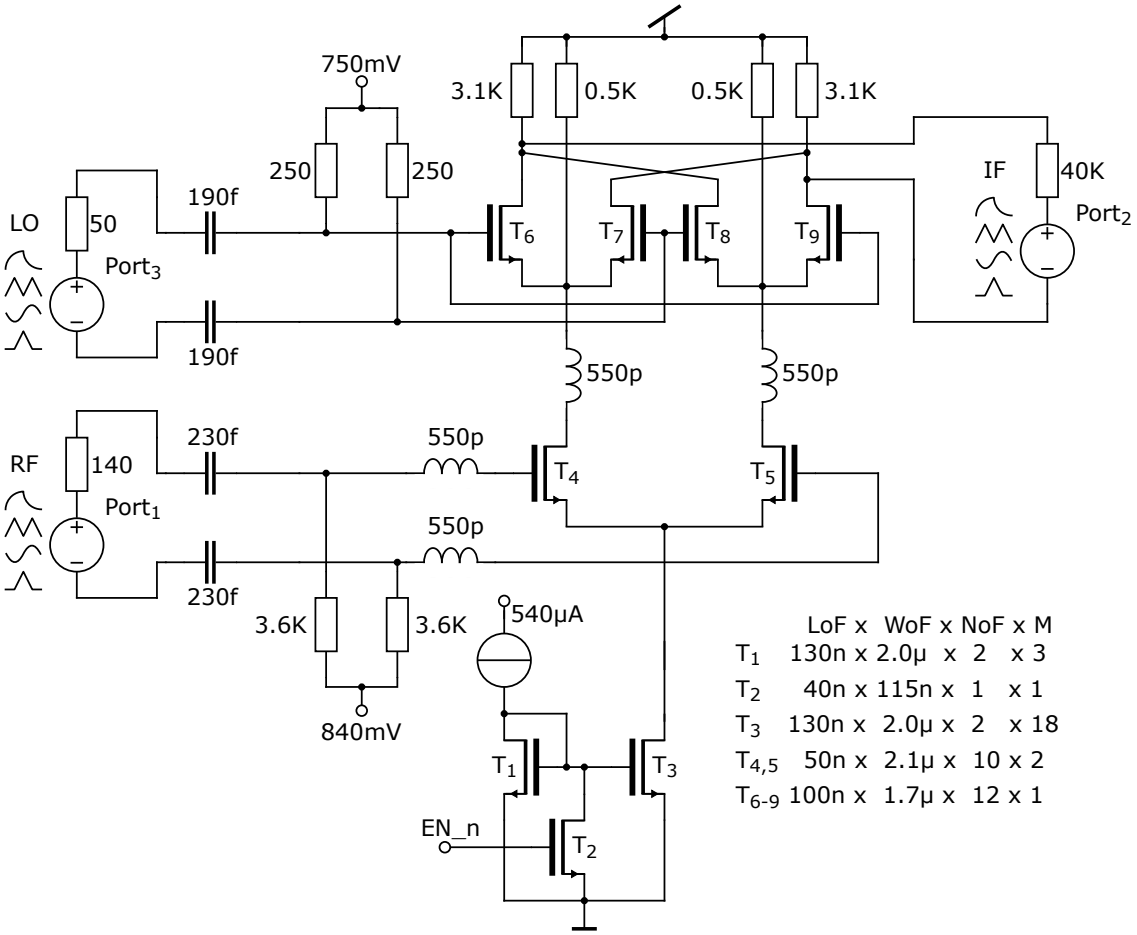

Figure A.8: Mixer operating in $9 - 50\,\mathrm{GHz}$ range.

A.3 Voltage Controlled Oscillator

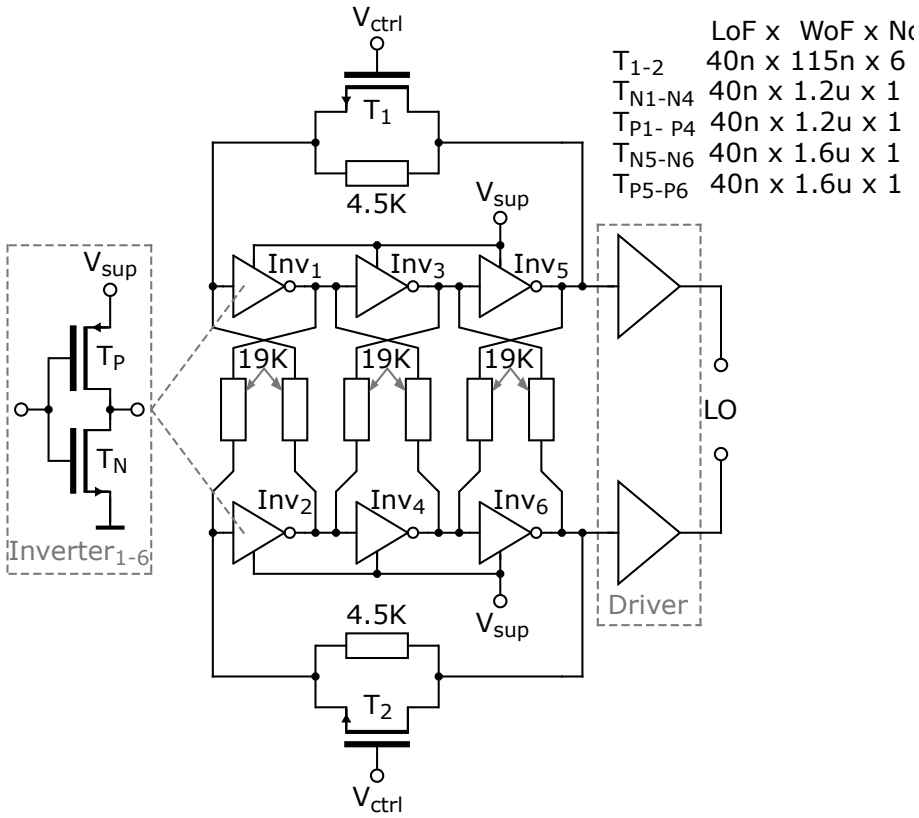

Figure A.9: VCO operating in the frequency range $9 - 13$ GHz. T_N and T_P symbolize NMOS and PMOS transistors, respectively.

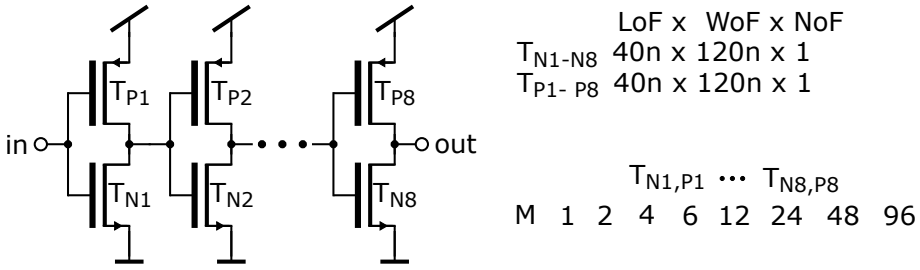

Figure A.10: Driver of the VCO depicted in Figure A.9. The finger dimensions of the NMOS and PMOS transistors are identical, except the multiplier M.

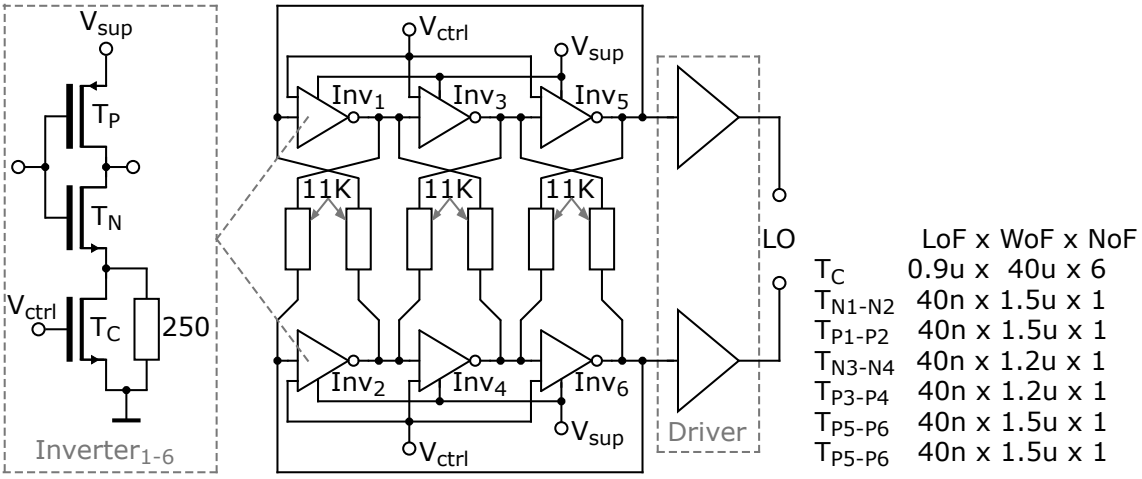

Figure A.11: VCO operating in the frequency range $13 - 19$ GHz. T_N and T_P symbolize NMOS and PMOS transistors, respectively.

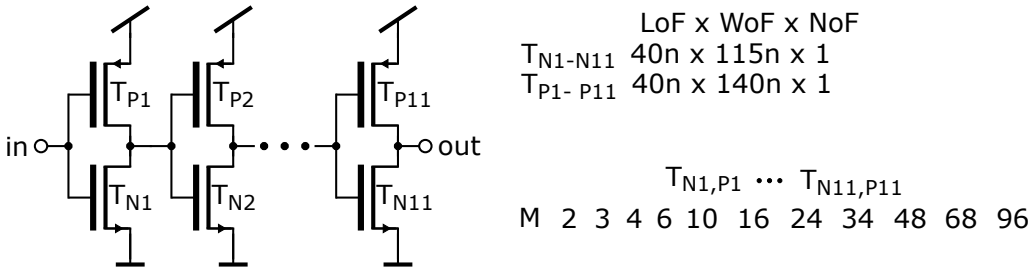

Figure A.12: Driver of the VCO depicted in Figure A.11. The eleven driver stages with increasing multiplier M is required to be able to drive the load at relatively high frequencies.

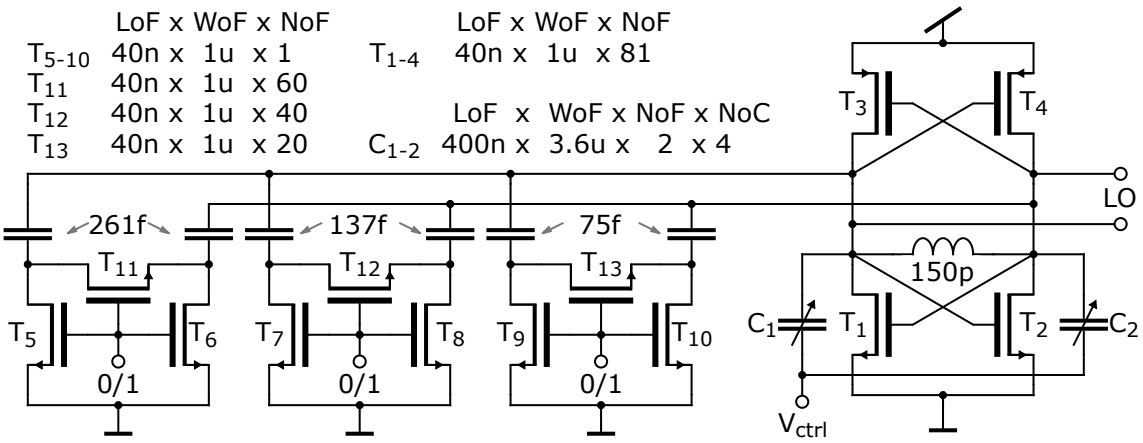

Figure A.13: VCO operating in the frequency range $19 - 26$ GHz. The varactors C_{1-2} are build with NMOS capacitors.

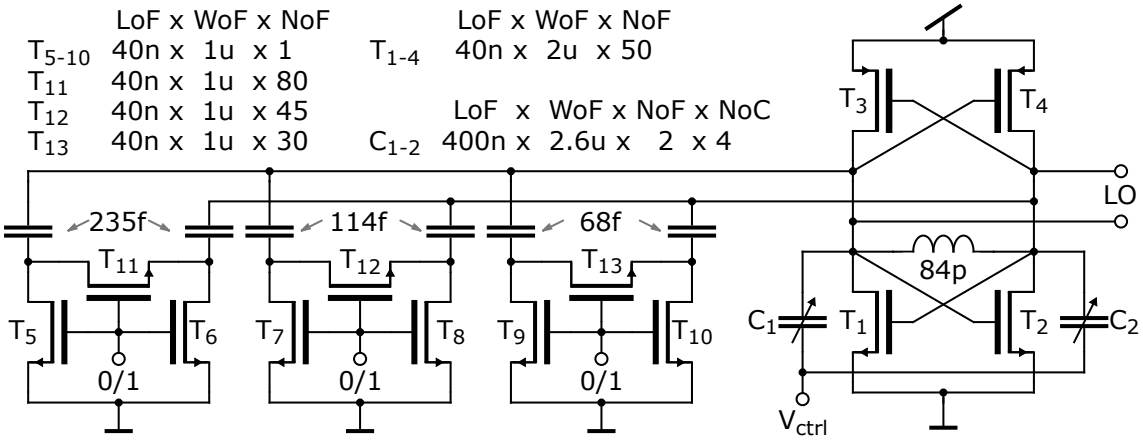

Figure A.14: VCO operating in the frequency range $26 - 33$ GHz.

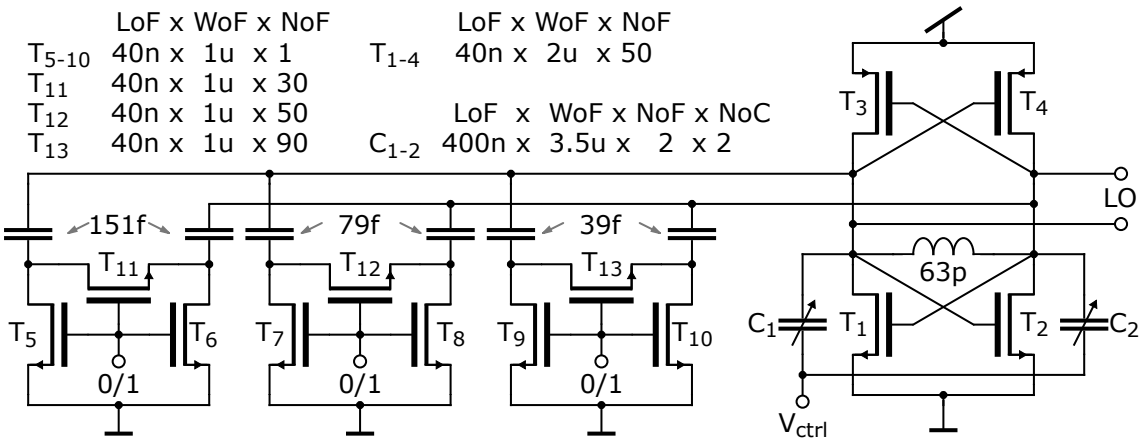

Figure A.15: VCO operating in the frequency range $33 - 39$ GHz.

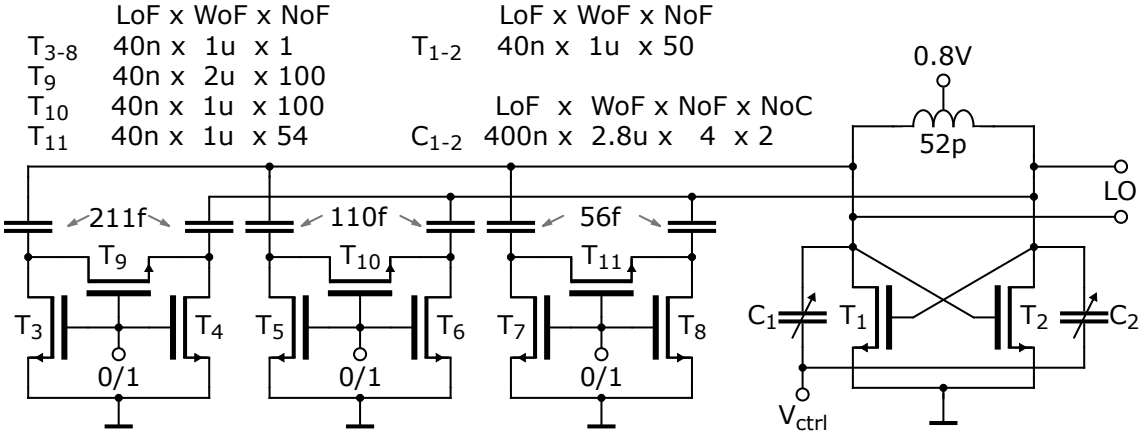

Figure A.16: VCO operating in the frequency range $39 - 50$ GHz.

A.4 Phase Locked Loop

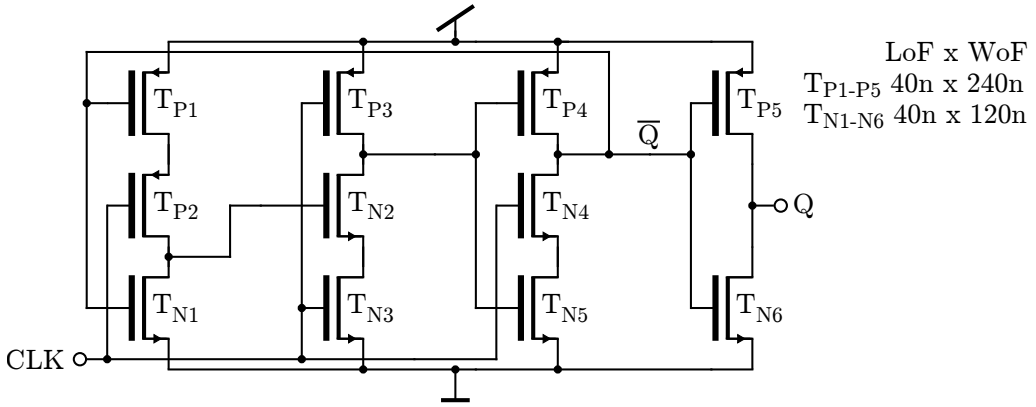

Figure A.17: TSPC divider operating till 18 GHz. Minimum sized NMOS and PMOS transistors are used.

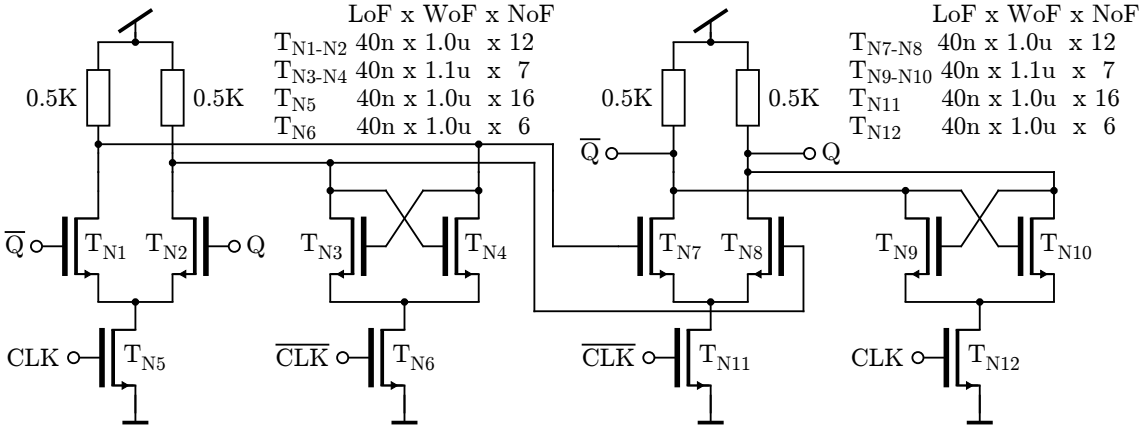

Figure A.18: SFD divider with dividing factor 2 operating till 40 GHz. The outputs Q and $\overline{Q}$ of the second flipflop are connected to the inputs of the first flipflop.

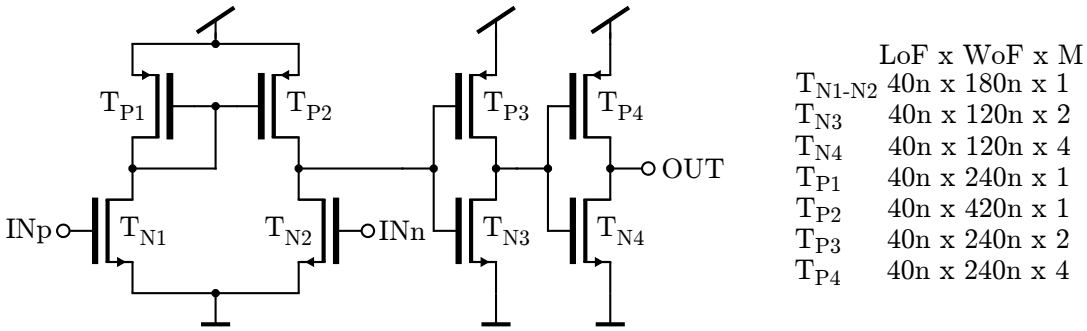

Figure A.19: Output buffer of the SFD divider.

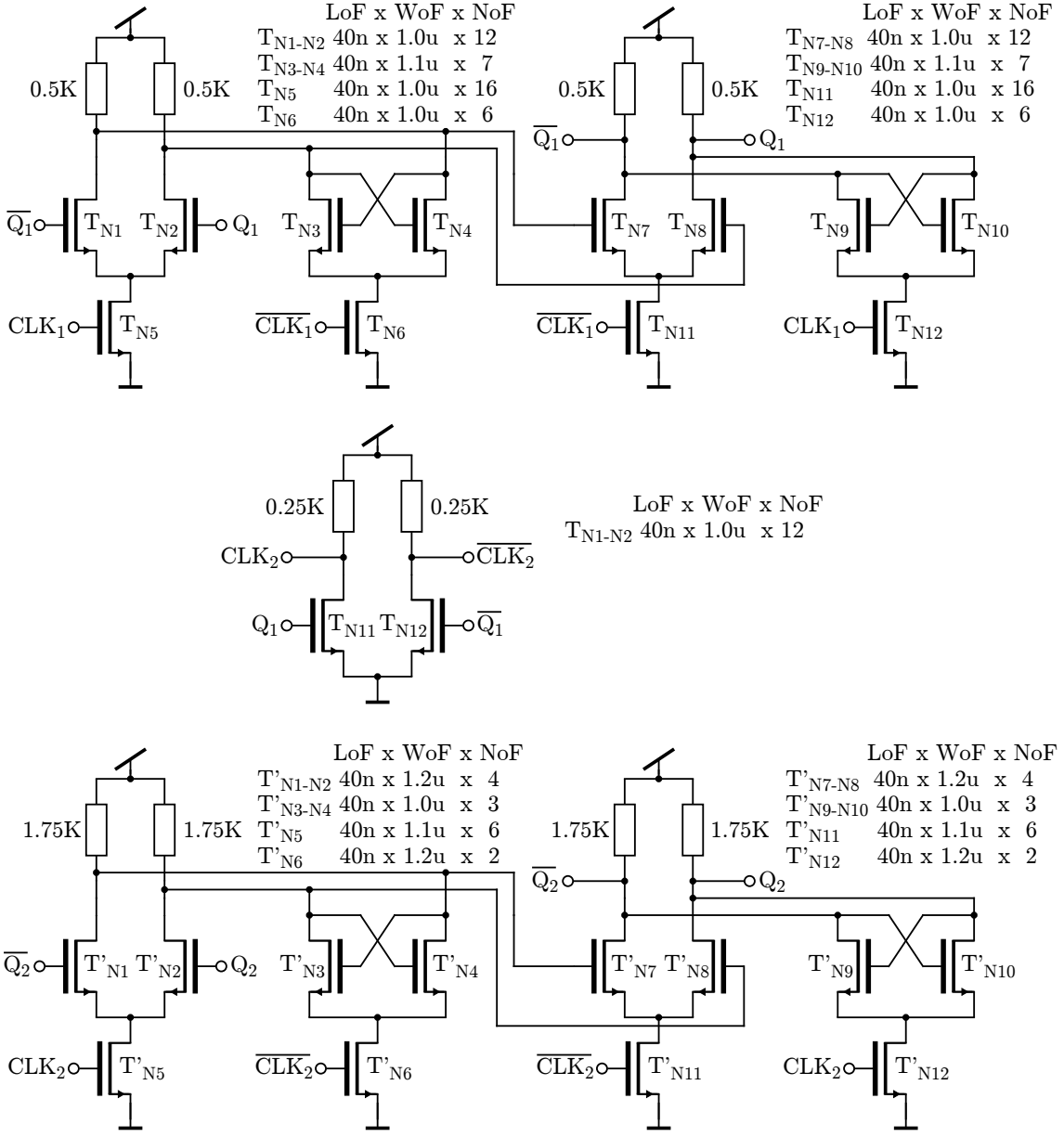

Figure A.20: SFD divider with dividing factor 4 operating till 40 GHz. The outputs $Q_{1/2}$ and $\overline{Q_{1/2}}$ of the second flipflops are connected to the inputs of the first flipflops. Inter-stage buffer recovers the divided clock signal CLK_1 and provides the clock signals CLK_2 and $\overline{\mathrm{CLK}_2}$ for the second divider.

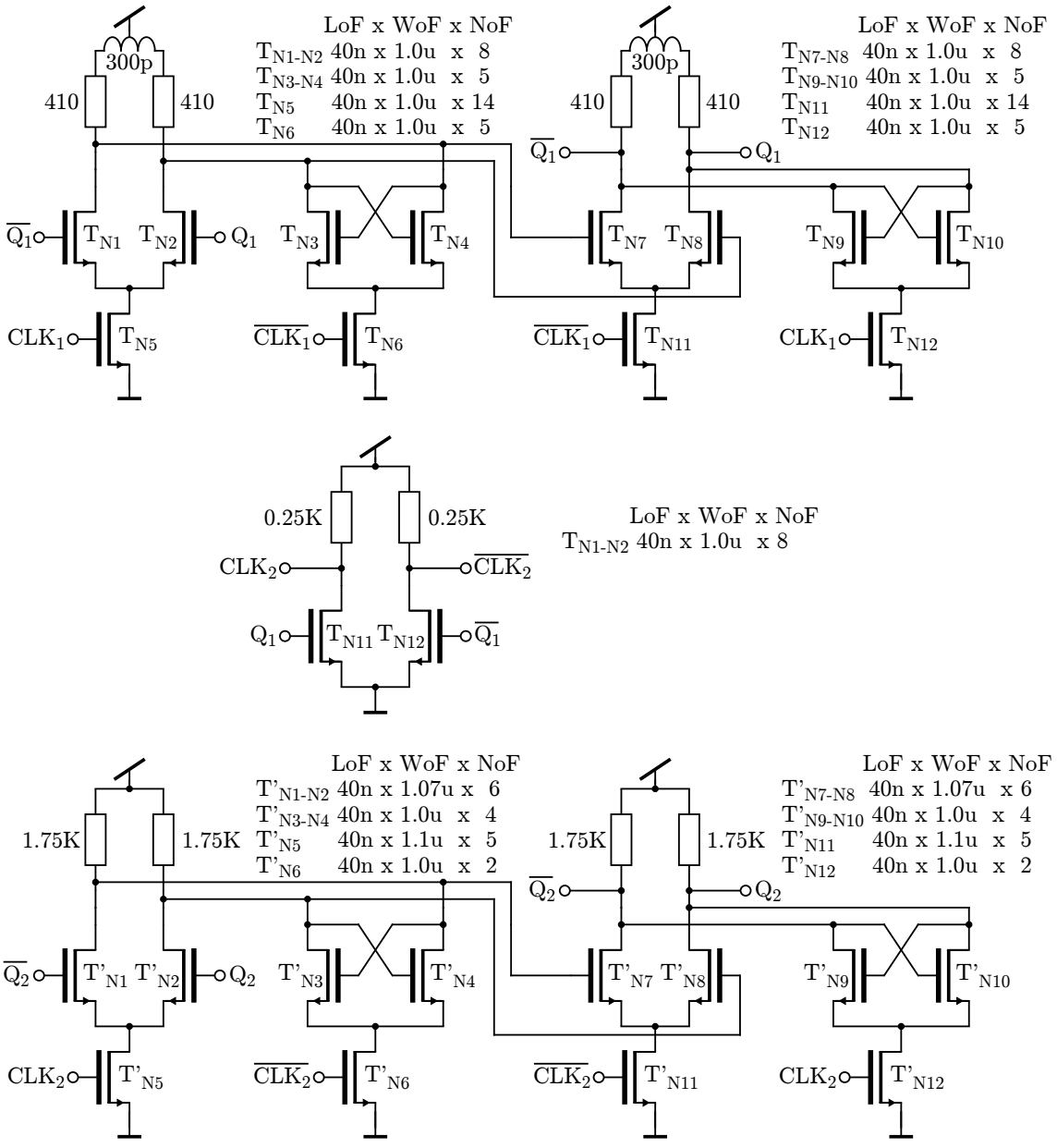

Figure A.21: SFD divider with dividing factor 4 operating till 50 GHz. The operation principle is similar to the topology depicted in Figure A.20. To achieve functionality above 40 GHz the inductive peaking technique is used in the first flipflop.

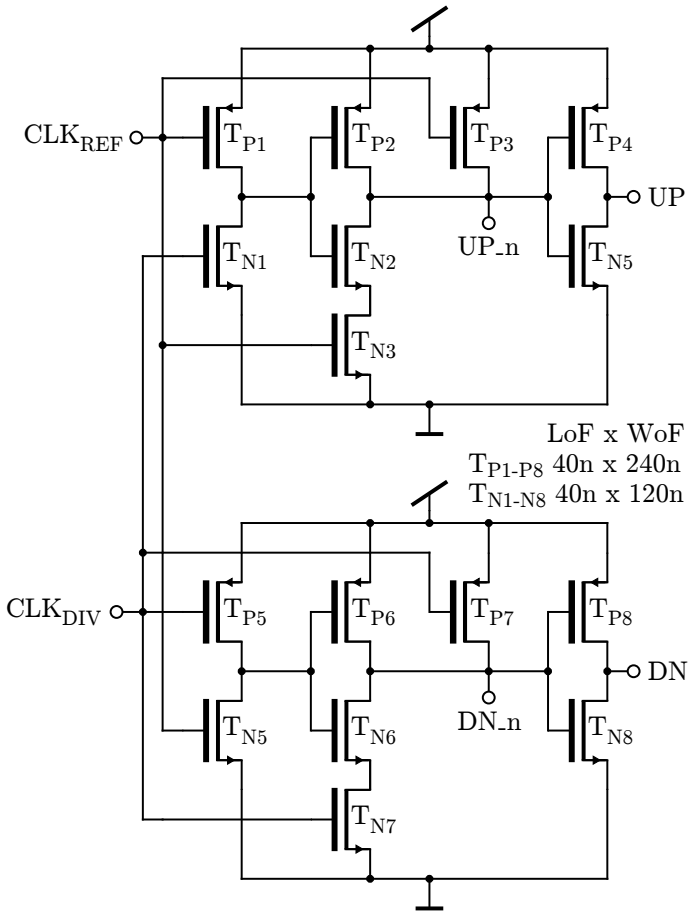

Figure A.22: Phase Frequency Detector (PFD) realized with dynamic logic. For the NMOS transistors minimal sizes of the gate length and width are used. The PMOS transistors have doubled gate width to have similar rising and falling time of the circuitry.

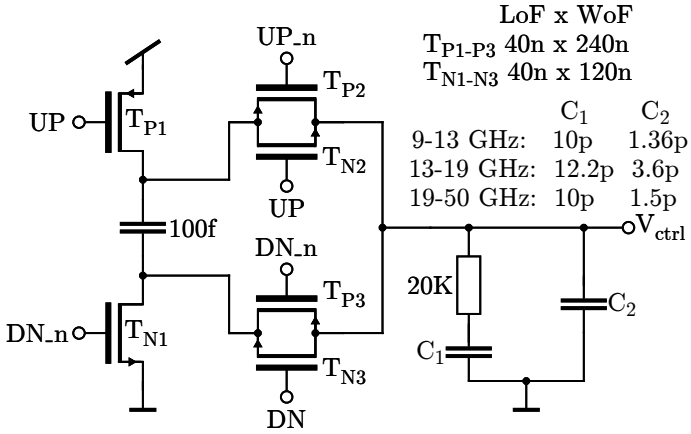

Figure A.23: Charge Pump (CP) with LF. For the NMOS transistors minimal sizes of the gate length and width are used. Depending on the VCO operating frequency, the filter capacitances C_1 and C_2 are adjusted due to stability reasons.

A.5 Operational Amplifier

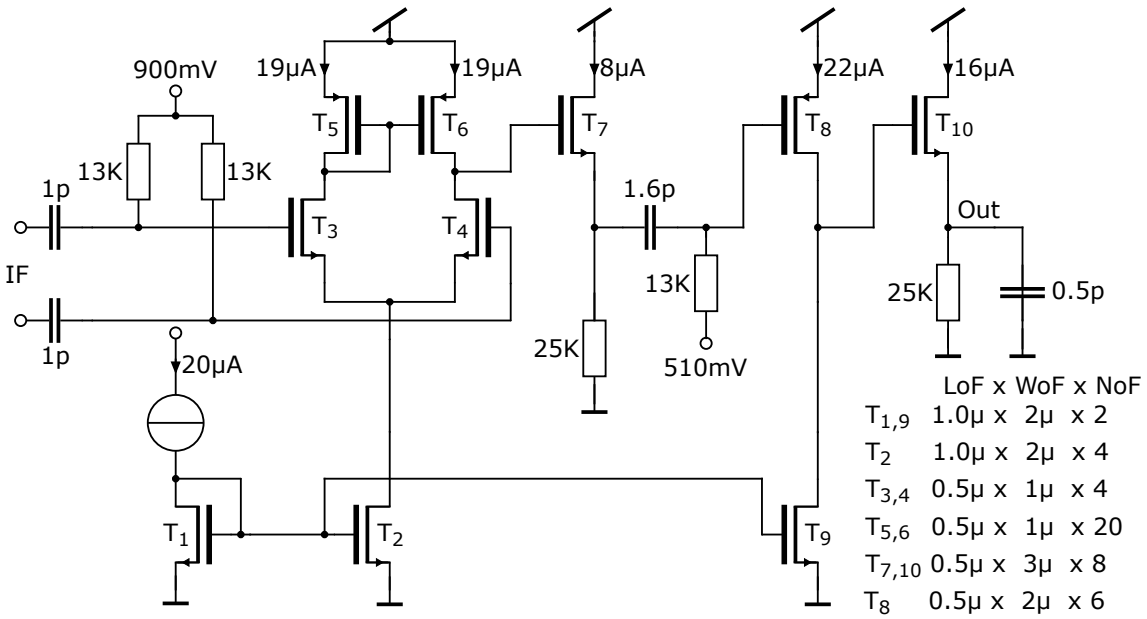

Figure A.24: OpAmp designed for the frequency range $10 - 60\,\mathrm{MHz}$.

Appendix B

Simulation Results

B.1 VCO frequency tuning

Figures presented below summarize the frequency adjustment of the VCOs. The functionality of the circuits is described in Section 4.5. The simulation results are discussed in Section 5.3.

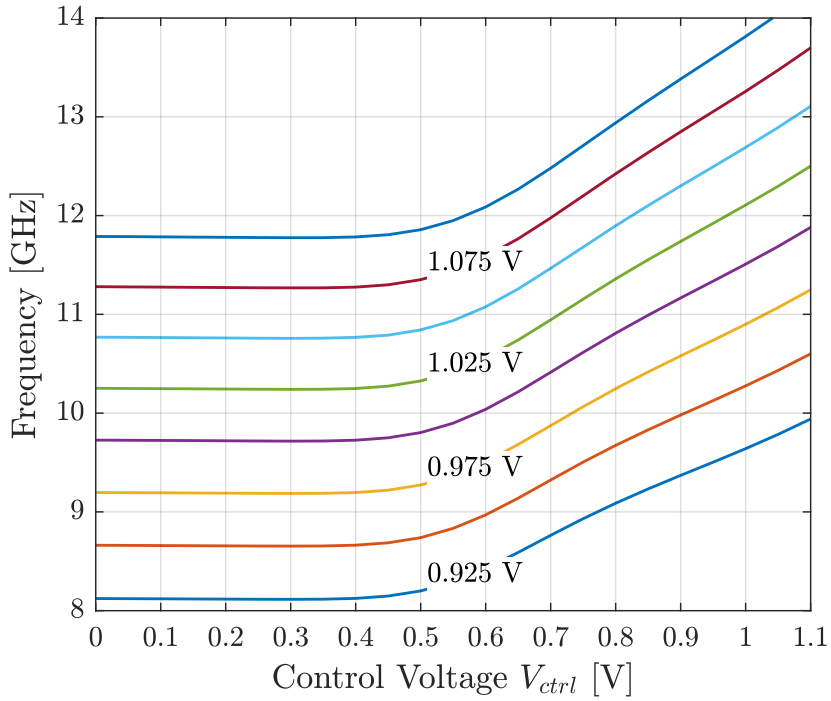

Figure B.1: Frequency tuning of the VCO designed for the frequency range $9 - 13\,\mathrm{GHz}$.

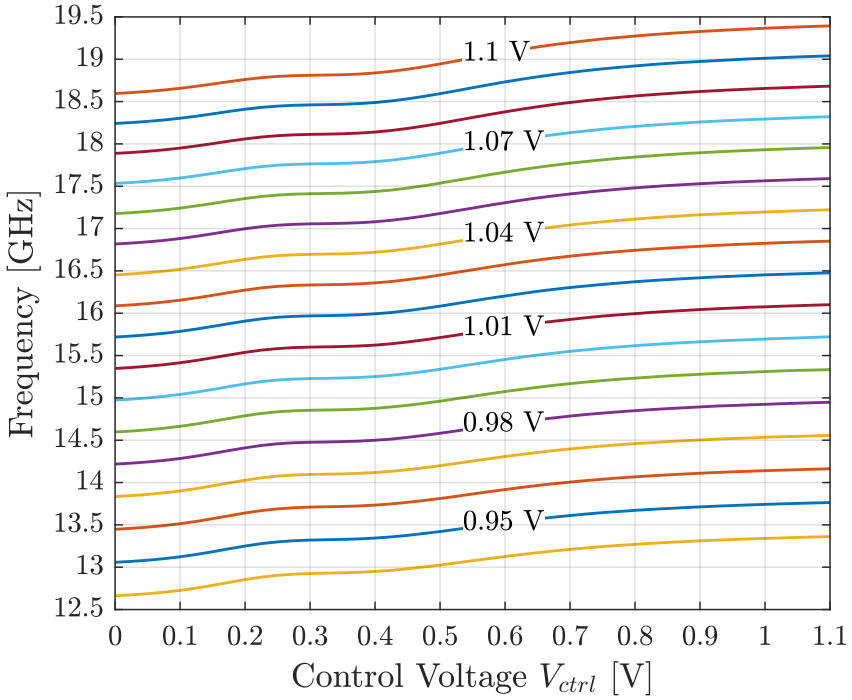

Figure B.2: Frequency tuning of the VCO designed for the frequency range $13 - 19\,\text{GHz}$.

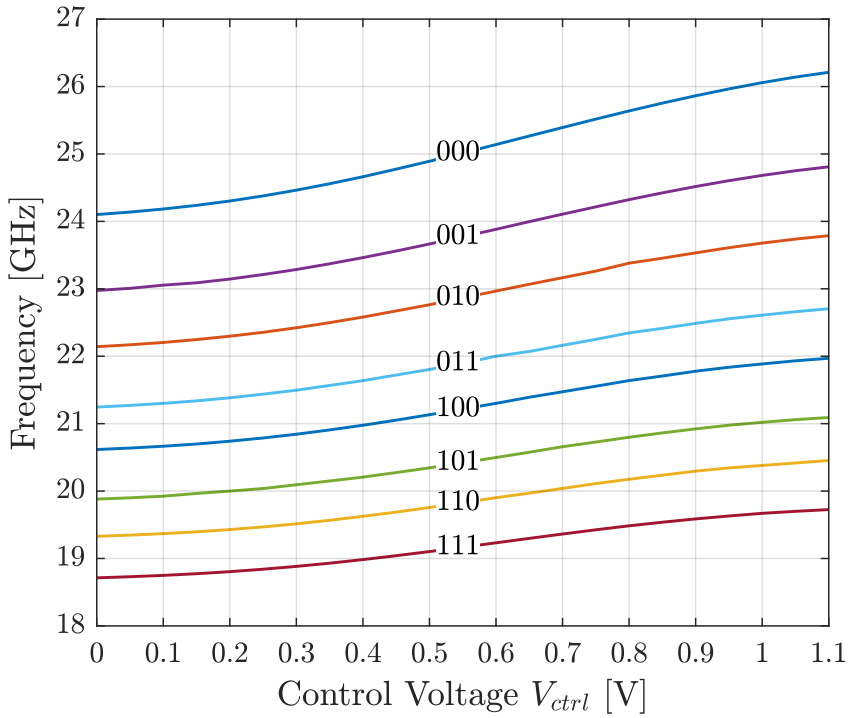

Figure B.3: Frequency tuning of the VCO designed for the frequency range $19 - 26\,\text{GHz}$.

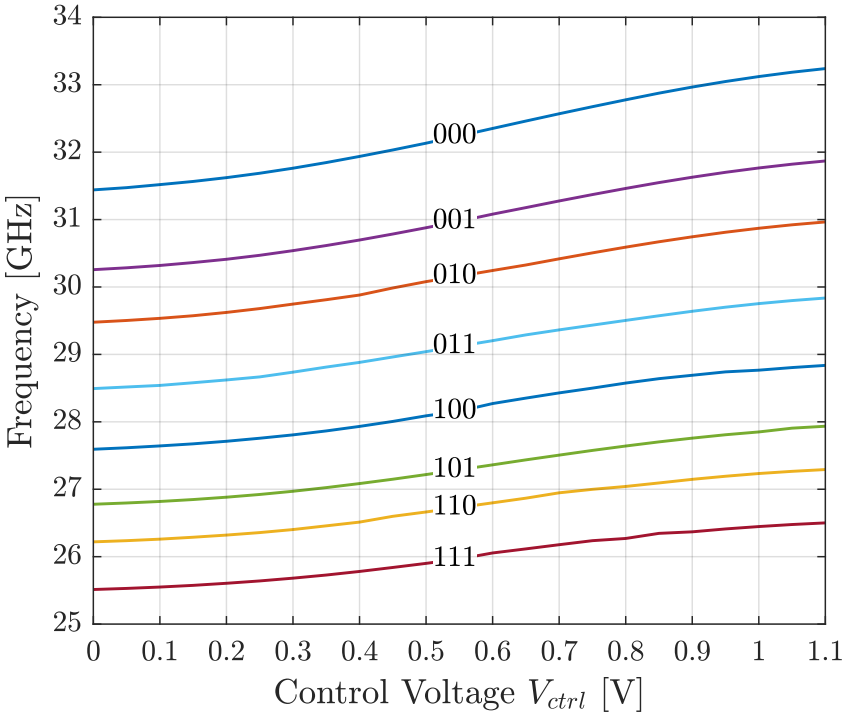

Figure B.4: Frequency tuning of the VCO designed for the frequency range 26 – 33 GHz.

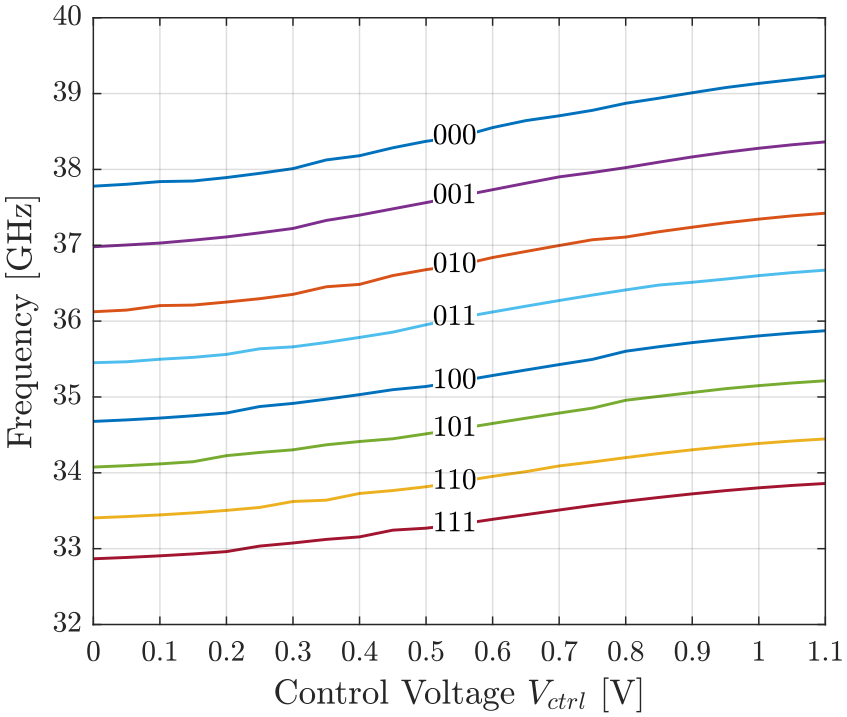

Figure B.5: Frequency tuning of the VCO designed for the frequency range 33 – 39 GHz.

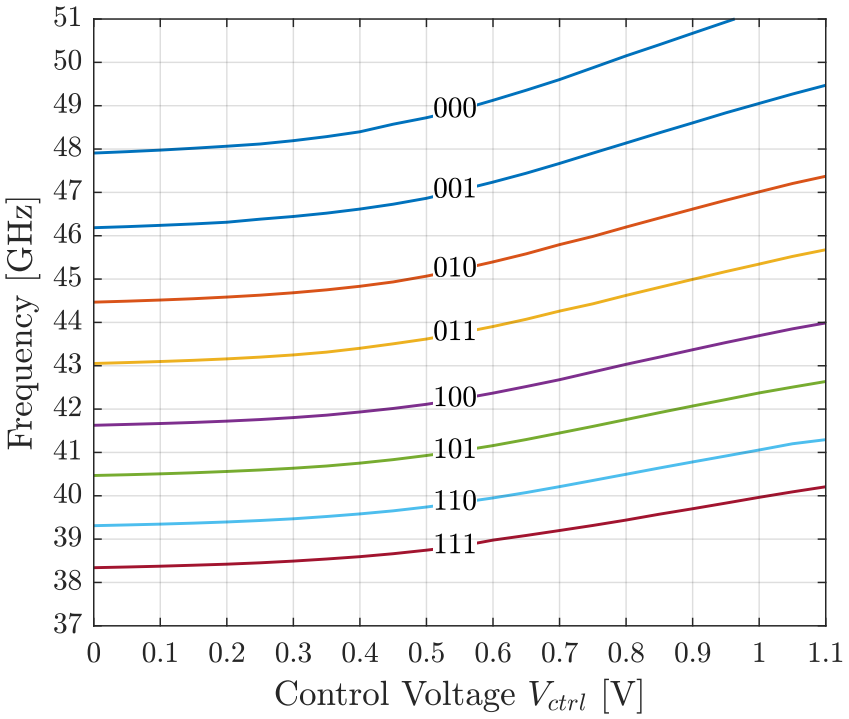

Figure B.6: Frequency tuning of the VCO designed for the frequency range $39 - 50\,\mathrm{GHz}$.

Appendix C

Matlab Code

The MATLAB script presented below has been used for stability analysis of the PLL described in Section 4.6.4.

```
clear;
close all;
dos('taskkill /F /IM acroRd32.exe')

% Input Parameters
R1 = 20e3;
C1 = 10e-12;
C2 = 1.5e-12;
K_VCO = 2*pi * 2e9;
K_PFD = 50e-6 / (2*pi);
N = 2^7;

% TF of Loop Filter
num_LPF = [R1*C1 1];
den_LPF = [R1*C1*C2 C1+C2 0];
TF_LPF = tf(num_LPF,den_LPF);

% TF of VCO
num_VCO = [K_VCO];
den_VCO = [1 0];
TF_VCO = tf(num_VCO,den_VCO);

% TF of PFD/CP
num_PFD = [K_PFD];
den_PFD = [1];
TF_PFD = tf(num_PFD,den_PFD);

% TF of Divider
num_N = [1];
den_N = [N];
```

```
31 TF_N = tf(num_N,den_N);
32
33 % TF of Open Loop
34 H_OL = TF_PFD * TF_VCO * TF_LPF * TF_N;
35
36 % H_OL parameters
37 [~, pm, ~, wpm] = margin(H_OL);
38 z = abs(zero(H_OL));
39 p = abs(pole(H_OL));
40 [mag, phase, w] = bode(H_OL);
41
42 %% Plot magnitude of H_OL
43 set(groot, 'defaultAxesTickLabelInterpreter','latex');
44 set(groot, 'defaultLegendInterpreter','latex');
45 subplot(2,1,1);
46 loglog(w, mag(:),'LineWidth',1);
47 ylim([1e-4 1e4]);
48 ylabel('Magnitude [dB]','FontSize',12,'Interpreter','latex')
     ;
49 set(gca,'YTick', [1e-4 1 1e4]);
50 grid on;
51 hold on;
52
53 % insert pole and zero
54 loglog(z,1e-4,'xk', 'LineWidth',2);
55 text(0.9*z, 0.2e-4, '$\omega_z$', 'FontSize',12, '
     Interpreter','latex');
56 loglog(p,1e-4,'xk', 'LineWidth',2);
57 text(0.9*p(3), 0.2e-4, '$\omega_p$', 'FontSize',12, '
     Interpreter','latex');
58
59 % Plot phase of H_OL
60 subplot(2,1,2);
61 semilogx(w, phase(:),'LineWidth',1);
62 xlabel('Frequency [Hz]','FontSize',12,'Interpreter','latex')
     ;
63 ylabel('Phase [$^\circ$]','FontSize',12,'Interpreter','latex
     ');
64 grid on;
65 hold on;
66
67 % insert phase margin
68 semilogx([wpm wpm], [-180 pm-180], '-k', 'LineWidth',1);
69 semilogx([wpm wpm], [pm-180 -120], '--k', 'LineWidth',0.5);
70 text(1.1*wpm, -155, 'PM', 'FontSize',12, 'Interpreter','
     latex');
```

```
71 subplot(2,1,1);
72 loglog([wpm wpm], [1e-4 1], '--k', 'LineWidth',0.5);
73 loglog([1e5 1e9], [1 1], '--k', 'LineWidth',0.5);
74
75 % insert loop bandwidth
76 text(0.9*wpm, 0.2e-4, '$\omega_c$', 'FontSize',12, '
     Interpreter','latex');
77
78 %% save figure as pdf
79 l_margin=-0.12;
80 r_margin=-0.45;
81 b_margin=0;
82 t_margin=-0.15;
83 fig_width=4.5;
84
85 fig_gca=gca;
86 fig_gca.Units = 'inch';
87 fig_ti=fig_gca.TightInset;
88 fig = gcf;
89 fig.PaperUnits = 'inch';
90 fig.PaperPositionMode = 'manual';
91 fig.PaperPosition=[l_margin b_margin fig_width 0.75*
     fig_width];
92 fig_pos = fig.PaperPosition;
93 fig.PaperSize = [fig_pos(3)+r_margin fig_pos(4)+t_margin];
94 print(fig,['pll_bode_plot'],'-dpdf');
95 open pll_bode_plot.pdf
```

Acronyms

AC	Alternating Current
ADC	Analog-to-Digital Converter
ADS	Advance Design System
ALU	Arithmetic Logic Unit
BLS	Brillouin Light Scattering
CML	Current Mode Logic
CMOS	Complementary Metal-Oxide-Semiconductor
CP	Charge Pump
CPU	Central Processing Unit
CG	Common Gate
CS	Common Source
DC	Direct Current
DSB	Double-Sideband
EM	Electro-Magnetic
ESD	Electro Static Discharge
HFSS	High-Frequency Structure Simulator
IC	Integrated Circuit
IF	Intermediate Frequency
$\mathbf{IIP_3}$	3rd Order Input Intercept Point
IP	Intellectual Property
$\mathbf{IP_{1dB}}$	Input referred 1 dB compression Point
$\mathbf{IP_3}$	Intercept Point
ISHE	Inverse Spin Hall Effect
KVL	Kirchhoff's Voltage Law

LNA Low Noise Amplifier

LoF Length of Finger

LSB Least Significant Bit

M Multiplier

MC Monte-Carlo

MESO Magnetoelectric Spin-Orbit

mmW millimeter Wave

MOKE Magneto-Optic Kerr Effect

MOS Metal-Oxide-Semiconductor

MPW Multi Project Wafer

NF Noise Figure

NML Nanomagnetic Logic

NMOS Negative-Channel Metal-Oxide-Semiconductor

NoF Number of Fingers

LF Loop Filter

LO Local Oscillator

OIF Optimum Inductor Finder

OIP_3 3rd Order Output Intercept Point

OOMMF Object Oriented MicroMagnetic Framework

OP_{1dB} Output referred 1 dB compression Point

OpAmp Operational Amplifier

PCB Printed Circuit Board

PD Phase Detector

PDK Process Design Kit

PFD Phase Frequency Detector

PLL Phase Locked Loop

PMOS Positive-Channel Metal-Oxide-Semiconductor

PN Phase Noise

PSWS Propagating Spin Wave Spectroscopy

PVT Process, Voltage supply and Temperature

RF Radio Frequency

RMSE	Root Mean Square Error
SFD	Static Frequency Divider
SHE	Spin Hall Effect
SNR	Signal-to-Noise Ration
SOI	Silicon-on-Insulator
SP	Spin Pumping
SPICE	Simulation Program with Integrated Circuit Emphasis
SSB	Single-Sideband
STT	Spin Transfer Torque
SW	Spin Wave
TFET	Tunneling Field Effect Transistor
TSPC	True Single-Phase Clocking
UWB	Ultra-Wideband
VCO	Voltage Controlled Oscillator
VNA	Vector Network Analyzer
WoF	Width of Finger
XOR	Exclusive Or
YIG	Yttrium-Iron-Garnet

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