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Design and Implementation of a 17-Level Cascaded H-Bridge Inverter for Battery Energy Storage Systems in the Low Voltage Grid

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Abstract

Renewable energy sources are connected to the public grid using power electronics circuits. The increase of these power sources has led to specific requirements on the power electronics circuits and grid stability. However, the power generation is fluctuating during the day. This fluctuation in the power generation can be bypassed using energy storage systems. Grid connected stationary storages represent an important research topic, which has grown rapidly in recent decades accompanied by the growth of power generation from renewable sources. Nowadays, conventional grid connected battery energy storage systems use single- and three-phase conventional topologies. The power limitation of single-phase inverters is bypassed using the three-phase B6-bridge inverters. Further power increase can be achieved using multilevel inverters. However, the usage of these topologies in stationary battery energy storage systems in the low voltage grid provides a high degree of efficiency, scalability, and promises particular advantages compared to the conventional topologies.

This thesis examines the usage of multilevel inverters to connect battery energy storage systems to the low voltage grid. The basic multilevel topologies are introduced, compared to each other, and a 17-level cascaded H-bridge inverter topology is selected to be further designed and implemented in hardware. The discussed methodology simplifies the design of such complex power inverters containing higher number of components, owing a complex switching behavior, and operating for long-time periods. Therefore, the design is divided into the analysis on different abstraction levels.

The deepest abstraction level studies one submodule used in the multilevel inverter to reduce the system complexity and calculate its efficiency. These simulations on component-level consider an H-bridge inverter and deliver high accuracy compared to the hardware measurements.

The next higher level focuses on the dynamic operation of the whole 17-level cascaded H-bridge inverter. On circuit-level, the used simulation model is divided into a hardware- and software-part and is used to design the grid parameters, the system modulation technique, the power filter, and the controller parameters using conventional methods as well as the one adapted for the cascaded H-bridge inverter. Finally, the inverter's operation is validated using simulation and measurement results.

The highest level uses behavioral models of the selected inverter for long time operation. On system-level, the used behavioral models of the conventional single-phase, three-phase, and cascaded H-bridge inverter neglect the switching behavior of the inverter and allow simulating the inverter for long time periods. The system-level is especially interesting for cascaded H-bridge inverters due to the usage of split independent battery modules to analyze their states of charge for long simulation times in hours-range

Zusammenfassung

Erneuerbare Energiequellen werden über leistungselektronische Schaltungen an das öffentliche Versorgungsnetz angeschlossen. Die Zunahme solcher Energiequellen führt zu besonderen Anforderungen in Bezug auf leistungselektronische Systeme und auf Seiten der Netzstabilität. Die erneuerbare Energieerzeugung schwangt jedoch stark im Laufe des Tages und abhängig von der Jahreszeit. Um diese Schwankungen in der Stromerzeugung umgehen zu können, werden Energiespeichersysteme eingesetzt, um damit eine dezentrale Energieerzeugung und -verbrauch zu ermöglichen. Netzgebundene stationäre Speicher stellen daher ein wichtiges Forschungsthema dar, das in den letzten Jahrzehnten stark an Wichtigkeit gewonnen hat. Heutzutage werden herkömmliche netzgebundene Batterie-Energiespeichersysteme mit konventionellen einphasigen und dreiphasigen Umrichter-Topologien verbunden. Die Leistungsbegrenzung von Einphasenwechselrichtern wird mit dreiphasigen B6-Brückenwechselrichtern überwunden. Die weitere Leistungserhöhung kann mit mehrstufigen Wechselrichtern erreicht werden. Die Verwendung solcher Topologien in stationären Batterie-Energiespeichersystemen im Niederspannungsnetz bietet einen hohen Grad an Effizienz und Skalierbarkeit und verspricht dabei besondere Vorteile gegenüber herkömmlicher Topologien.

Diese Dissertation untersucht die Verwendung von mehrstufigen Wechselrichtern, um Batteriespeichersysteme an das Niederspannungsnetz anzubinden. Die grundlegenden mehrstufigen-Wechselrichter-Topologien werden miteinander verglichen. Weiter wird ein kaskadierter 17-stufiger H-Brückenwechselrichter ausgewählt und in Hardware umgesetzt.

Die besprochene Entwurfsmethodik vereinfacht das Design von komplexen Wechselrichtern, die eine höhere Anzahl an Komponenten sowie ein komplexes Schaltverhalten besitzen und gleichzeitig für lange Zeiträume betrieben werden. Daher wird der Entwurf in verschiedene Abstraktionsebenen unterteilt. Diese Ebenen sind nach dem bottom up Ansatz gestaffelt.

Die unterste Abstraktionsebene untersucht ein Submodul des Multilevel-Wechselrichters, um die Systemkomplexität zu reduzieren und die Effizienz zu ermitteln. Diese Simulation auf Komponentenebene berücksichtigt einen H-Brückenwechselrichter und bietet im Vergleich zu den Hardwaremessungen eine hohe Genauigkeit.

Auf der Schaltungsebene ist das verwendete Simulationsmodell in einen Hardware- und Softwareteil unterteilt. Darüber hinaus werden drei Netzmodelle untersucht und deren Auswirkungen auf den Betrieb des Wechselrichters diskutiert. Die Netzparameter, das Energiesystem und die Reglerparameter werden mit herkömmlichen Methoden sowie mit dem kaskadierten H-Brückenwechselrichter entworfen. Schließlich wird der Betrieb des Wechselrichters anhand von Simulations- und Messergebnissen validiert.

Die oberste Abstraktionsebene verwendet Verhaltensmodelle der ausgewählten Wechselrichter für den Langzeitbetrieb. Einphasige, dreiphasige und kaskadierte H-Brückenwechselrichter vernachlässigen das Schaltverhalten des Wechselrichters und ermöglichen damit die Simulation für längere Zeiträume.

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Many thanks to all projects partners during the projects EEBatt and MBatt, especially the colleagues from other departments at the Technical University of Munich, VARTA Storage GmbH, Fine Power GmbH, and Mixed Mode GmbH for their friendly and technically cooperation to research and develop the multilevel inverters technology to be used in battery storage systems.

Many thanks for all students and their appreciable theses under my supervision related to the topic of the thesis.

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My biggest thank goes to my family for its huge support. My Mother, my wife, my sisters, and my brothers helped me to come and study in Germany and provided me with ongoing financial and moral support.

Finally, I would like to dedicate this thesis to my wife, Vanya Dimitrova, who has been a constant source of support and encouragement all the time. She was always there for me as a loving wife and a dear friend. Furthermore I dedicate this thesis to my children Asma and Nora Lahlou. I am grateful to all the beautiful moments I share with them. I am truly thankful for having all them in my life.

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1 Introduction

In this chapter an introduction to the present work is given. The motivation and goals are defined followed by the list of publications related to this work. At the chapter's end, the structure of the thesis is summarized and the content of the individual chapters is initiated.

1.1 Motivation and Goals

In recent years, a great attention has been paid to renewable energy sources [25]. They produce a fluctuating power and influence the power quality and the stability of the power grid. Therefore, the energy storage systems should be installed close to these resources to overcome the power quality problem and solve the stability issues on the grid [14]. The requirements of stationary BESSs are high efficiency, scalability, and modularity to enable an energy transition to compensate the unequal renewable energy production during the day. The conventional BESSs operate using two-level inverters and require therefore high DC-link voltages and a big sized power filter or they operate at higher switching frequencies which leads to higher inverter losses. Multilevel inverters offer several advantages over their two-level counterparts such as smaller grid power filters, smaller voltage ratings for semiconductors with reduced stress on switches, lower switching frequencies, less power losses, higher efficiency, low electromagnetic compatibility (EMC) concerns [116], and higher modularity. Nowadays, multilevel inverters are not often used in low voltage BESSs. They are mostly used in medium and high voltage power range. Whenever, higher efficiency and redundancy are required, the multilevel inverters represent a good opportunity due to their topology. Fig. 1.1 gives the actual electricity generation from renewable and nonrenewable energy sources in the German power grid in 2017. According to this figure, the renewable energy sources, which mostly use power inverter, produce about 40 % of the total generation. It means that the energy and average power produced are 210 TWh and 24 GW, respectively. The fluctuation in the power generation of these power sources shows the future importance of stationary energy storage systems on a large scale.

Assuming a conventional inverters' efficiency of 97 %, the power losses produced by the inverters in Germany are about 720 MW. The efficiency of the multilevel cascaded H-bridge inverter studied in this thesis is 2 % higher than conventional inverters. This is the equivalent of 482 MW.

1.2 Scientific Contributions

This thesis examines the usage of multilevel inverters to connect battery energy storage systems to the low voltage grid, which leads to higher efficiency and offers several advantages in comparison with the conventional inverter topologies.

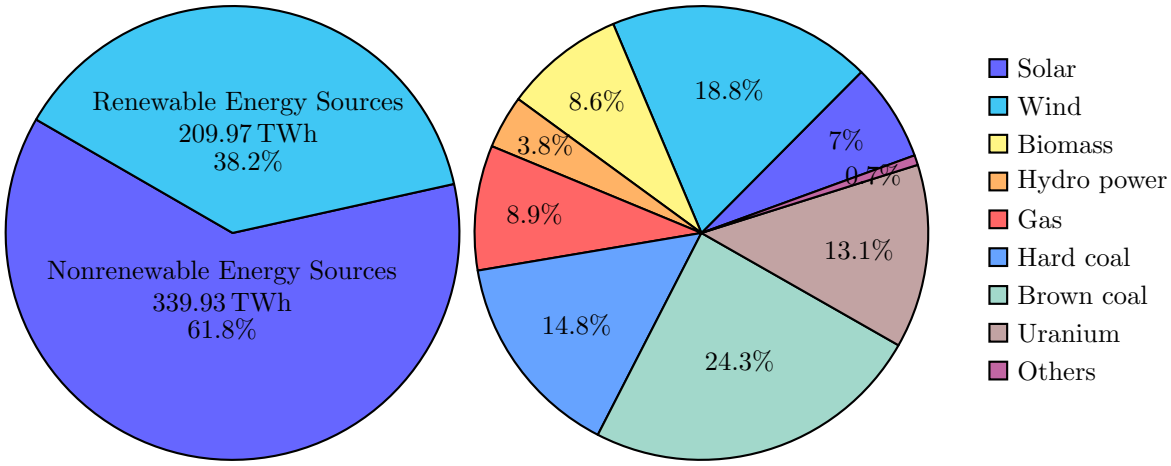

Figure 1.1 – Electricity generation and detailed power sources and their net generation of power plants for public power supply in Germany in 2017 [26].

The presented design methodology simplifies the design of such complex power inverter's topologies containing higher number of components, owing a complex switching behavior, and operating for long-time periods. Therefore, the design is divided into the analysis on different abstraction levels. The deepest abstraction level studies one submodule used in the multilevel inverter. The next higher level focuses on the dynamic operation of the whole inverter. The highest level considers the operation using behavioral models for long time periods.

The results of the inverter's operation using the presented abstraction levels serve as the basic of the design of the system modulation techniques, the power filter, and the controller parameters using conventional methods and the one adapted for the CHB inverter to finally validate the inverters operation using simulation and hardware results.

1.3 List of Publications

Lahlou, T.; Abdelrahem, M.; Valdes, S.; Herzog, H.-G.: "Filter Design for Grid-Connected Multilevel CHB Inverter for Battery Energy Storage Systems". In: 2016 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM). IEEE, 2016, pp. 831–836. ISBN: 978-1-5090-2067-6.
Lahlou, T.; Aslam, M. A.; Bolvashenkov, I.; Kammermann, J.; Herzog, H.-G.: "Grid Models for Use with Cascaded H-Bridge Inverter Based Battery Energy Storage System: Accepted for Publication". In: 2018 AEIT International Annual Conference.
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Schimpe, M.; Becker, N.; **Lahlou, T.**.; Hesse, H. C.; Herzog, H.-G.; Jossen, A.: "Energy Efficiency Evaluation of Grid Connection Scenarios for Stationary Battery Energy Storage Systems". In: Energy Procedia (2018).

1.4 Outline and Methodology

This thesis deals with the simulation-based design of cascaded H-bridge inverter for stationary battery storage system on the low voltage grid with hardware assessment.

In Chapter 2, the state of the art of grid connected battery energy storage systems is given and the fields of application are explained. The different components, such as the storage units, the energy and battery management systems, the power electronics, and the power grid as well as the related power quality are presented. Thereby, the focus is given to the power electronics part.

In Chapter 3, the grid connected BESSs using the single- and three-phase conventional topologies are introduced. The basic operation of the single-phase H-bridge inverter using bipolar and unipolar pulse width modulation techniques is presented. The usage of single-phase inverters is limited in the power given by the inverter. Therefore, the three-phase B6-bridge inverter is presented and its operation is shown using an example of BESS. The different effects of the DC-link capacitance sizing are shown for both inverter circuits.

In Chapter 4, further power increase is reached using multilevel inverters. Therefore, the main topologies are introduced and their advantages and disadvantages are compared with each other. The basic three topologies for multilevel inverters are shown and at the chapter's end the cascaded H-bridge multilevel inverter topology is selected to be further designed and used in battery energy storage systems.

In Chapter 5, three different circuits used in the submodules of the cascaded H-bridge inverters are presented. The one- and two-stage topologies offer different advantages and disadvantages. The related simulation results lead to the selection of the submodules topology to be used in BESS.

In Chapter 6, the design of the multilevel inverter starts on component-level to reduce the system complexity and introduce calculation methods for their efficiency. These simulations are then validated using hardware measurements on the H-bridge inverter used in the one-stage CHB inverter.

In Chapter 7, the inverter design on the next higher abstraction level is introduced. On circuit-level, the inverter's hardware- and software-parts are defined. The grid models used influence the inverter operation. Therefore, three grid models are studied and only one is selected for the further simulations. After this, different modulation techniques for the cascaded H-bridge inverter are explained and followed with the power filter design. The next design-step is related to the definition of the used controller parameter using the step response analysis. At the chapter's end, the simulation results are presented and the hardware as well as the measurements' results are shown.

In Chapter 8, the long-term modeling of the cascaded H-bridge inverter used in BESS is done on the highest abstraction level. The system-level and the used behavioral models of the power inverter are introduced. First, the conventional single- and three-phase inverter's behavioral models are shown followed by the corresponding model of the 17-level CHB inverter. The modulation techniques discussed on circuit-level are implemented using behavioral models to show the effects in the long-term operation of the BESS. Finally, the simulation performances using the average models are compared to those when the simulations on circuit-level is used.

In Chapter 9, the results are summarized and concludes the above points. Finally, further research field and recommendations are provided.

The structure of the presented work is summarized in Fig. 1.2.

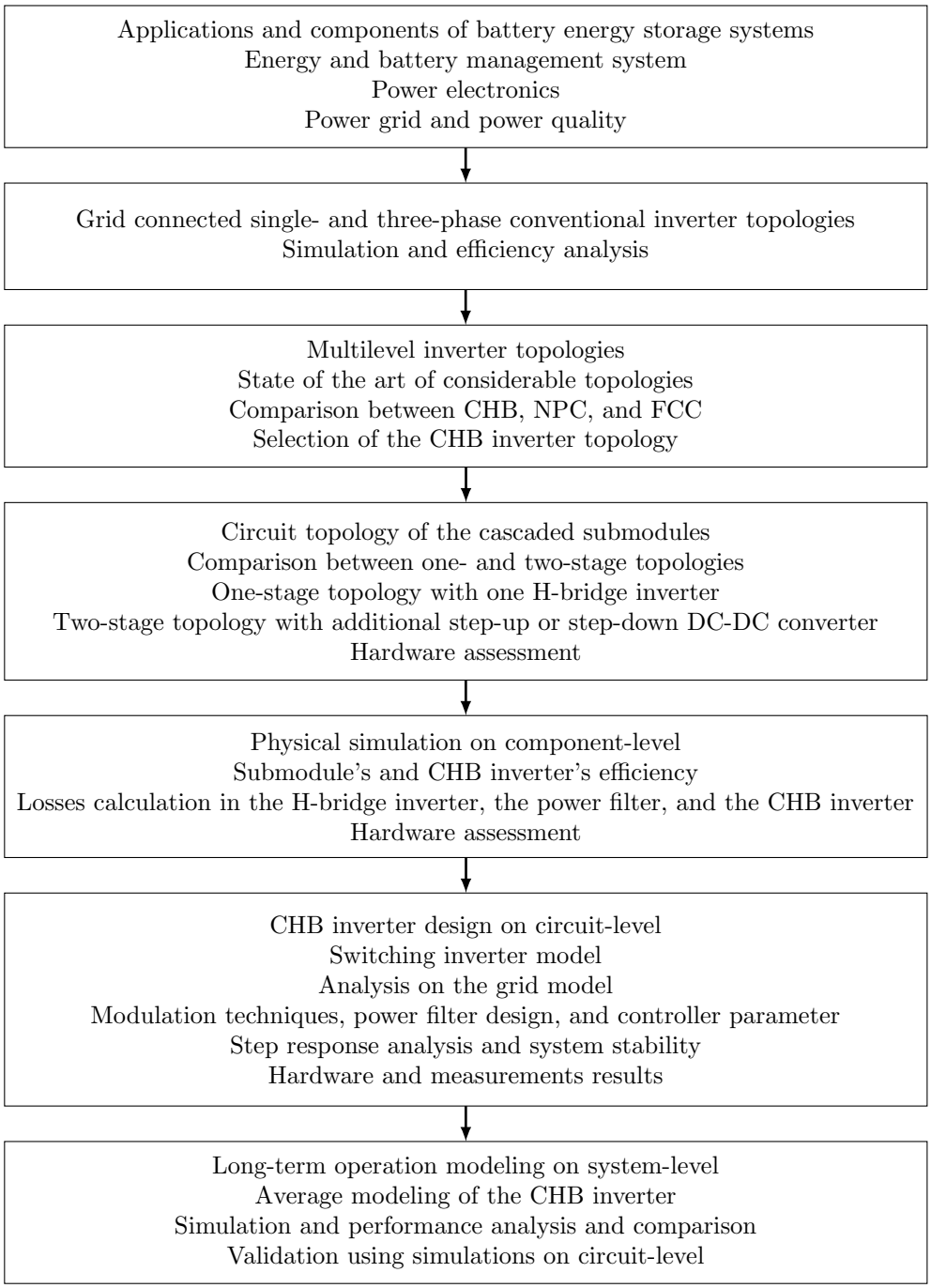


Figure 1.2 – Summary and structure of the Thesis.

2 Grid Connected Battery Energy Storage Systems

The components of the Battery Energy Storage Systems (BESSs) are introduced and explained in this chapter. The major components of grid connected BESSs and their fields of applications are presented in Section 2.1. The possible storage units and actual research projects are presented in Section 2.2. Furthermore, the energy and battery management systems are introduced and their tasks are explained in Section 2.3 and 2.4, respectively.
At the end of this chapter, the required power electronics for BESSs is presented in Section 2.5, while the power quality and grid effects are introduced in Section 2.6.

2.1 Fields of Application

Interest in stationary energy storage systems continues to increase since the last decade. In general, stationary BESSs are enclosed in a container and are isolated from the external environmental conditions. Only the grid connection power port and energy management system port are accessible as shown in Fig. 2.1. The BESS also contains a communication part to the user interface for debugging and operating the system.
The batteries' operating temperature differs from that of an inverter. For this purpose, it is recommended to separate the power inverter and battery modules' heat zones. Using bigger BESS, smart power meters are usually used to calculate the overall BESS energies and allow transferring the data to the Energy Management System (EMS). An intelligent BESS also uses dedicated hardware for communication with other available storage systems.
The BESS sector is still increasing due to the battery technology development and the need for peak shaving of the generated power by the Renewable Energy Sources (RES) during the day. In Germany, "Energiewende" (Energy Transition) speeds up the development of methods for decentralized energy. One main possibility to save renovation on the power grid is the

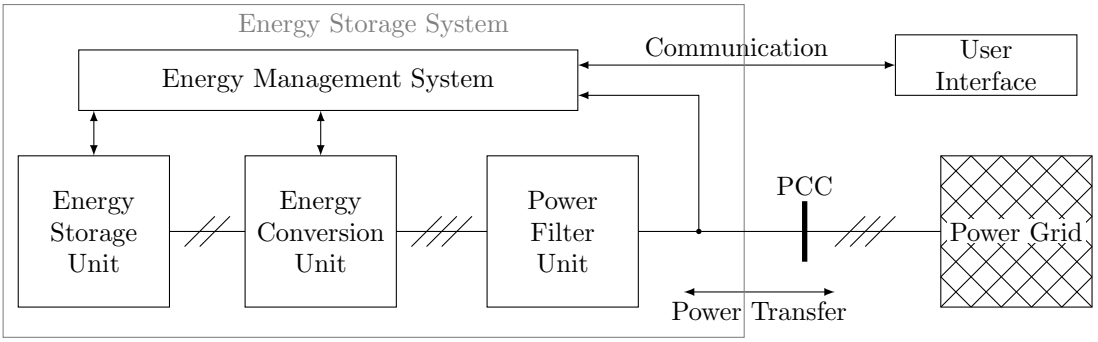


Figure 2.1 – Schematic diagram of the main components of grid connected energy storage systems.

usage of decentralized stationary BESS.
Fig. 2.1 shows the main components of grid connected energy storage systems. They consist of an energy storage unit connected to a voltage grid via power conversion and filter unit. The EMS is the interface between the user interface and the intern components of the energy storage system and is detailed in Section 2.3. The shown energy storage system in Fig. 2.1 is connected to the power grid and the required measurements for its operation are made on the Point of Common Coupling (PCC).
The expansion of renewable energy requires intelligent storage concepts to compensate the fluctuations in energy production and consumption caused during the day. A good alternative is the usage of stationary battery energy storage systems based on lithium-ions batteries.
Nowadays, the main usage of batteries is in the Uninterrupted Power Supply (UPS) due to the importance of power supply security in case of power grid failure. The scope of BESS is expanding due to the increase of energy density and decrease of battery-cells' prices. BESSs are used in multiple applications to increase the own-consumption of Photovoltaic (PV) systems. The energy produced during the day is stored to be used at night. BESSs are also used for island mode operation, whenever the power grid fails or misses, and supporting micro grids to become more independent from the main power grid.

2.1.1 Integration of Renewable Energy Generation Systems

In [63], it is shown, that the decentralized PV battery systems are an important contributor in integration of fluctuating renewable generation systems to power grids and in the implementation of smart grid concepts. When equipping two thirds of the PV systems with a battery storage, a load shift to midday peak can occur up to approximately 40 %.

2.1.2 Primary and Secondary Frequency Control

The primary and secondary frequency control is used in different grid voltage ranges: in low, medium, and high voltage. The RESs are usually connected to low-voltage grids. The storage for grid stabilization can be used for grid frequency control or support active power exchange with the grid. The reactive power is used for grid voltage control. In [22], it has been shown that even small scale storage units are sufficient to provide continuous and reliable primary and secondary frequency control reserves to the grid.
In [9], a BESS is used for voltage control by supplying reactive power to the grid. An apparent power 150 kVA and 30 kW is fed to the low-voltage grid to stabilize the grid voltage.
Since PV systems strongly feed back active power into the grid, the grid voltage increases. With the feedback of the reactive power using BESS, the voltage can be maintained within the certain limits.

2.1.3 Peak Shaving and Industrial Applications

The electric public utility applies different prices for companies with high peak electricity consumption based on the highest required current. It leads to higher costs for the accounting period. Therefore, BESSs are used to shave the peak current and reduce the electricity costs. As an example, in [90] a 1 MW battery storage is presented and algorithms for peak shaving are built to mainly reduce the costs.

2.1.4 Island Operation

In [22], BESSs are used in island grids for companies or industrial enterprises as well as for schools and hospitals in developing countries. In [61], a concept for a decentralized village power supply in islanding operation is given. Nowadays, island systems have also higher numbers and a variety of consumers.
PV home supply systems are widely used in off-grid regions in Africa, Asia and Latin America. The island systems usually have their electricity from hybrid plants that combine various renewable power sources and an additional diesel generator. Whenever renewable sources generate excess energy, it should be stored in battery storage systems. Likewise, the diesel generator can run in a more optimal operating point and pass the excess energy to the storage. Therefore, smart EMS plays an important role here.
According to the estimations for 2030 from the European Photovoltaic Industry Association (EPIA), the share of autonomous PV systems will increase by 30 % worldwide with a steadily rising trend.

2.2 Storage Units

The energy can be stored in different ways. In this section, the pumped hydro storage plants, the electrochemical batteries, and the redox flow storages are presented and their usage is described.

2.2.1 Pumped Hydro Storage Plants

Pumped hydro storage plants are actually one of the best possible storage units. The pumped hydro storage represents a promising storage technique. It has been widely applied to mitigate the variable output of renewable energy plants [179]. This can be achieved with naturally intermittent renewable energy, such as wind farms and solar power stations, by reduced costs [77]. The application of pumped hydro storage allows to increase the flexibility and better track the volatility of the renewable energy generation [82]. Those plants can ensure the power supply reliability, e.g. in Netherlands' electricity supply by supplying the emergency reserve of the power grid. The investment for such storages' costs are higher than conventional generation resources, e.g. coal- or nuclear- fired power plants [87] [186].
However, this type of storage depends on the geographical location. They consist of a higher and a lower water basin. In case of an energy overshoot the water is pumped to the top basin. Whenever the energy is needed, the water flows to the lower basin and rotates the turbines to deliver energy. Such storage has a theoretical self discharge close to zero and due to its high power, it is mostly used for grid support. In sunny days, whenever the renewable energy sources deliver more power than required, the water is pumped up. In the evening, the water is pumped down.
The disadvantages of such systems are their low efficiency and their higher response time.

2.2.2 Electrochemical Batteries

Due to the increase of the energy density and the decrease of battery-cells prices, the application of battery based energy storage systems is increasing. In [57], a Li-Ion based BESS with nominal power of 560 kW and nominal energy content of 560 kWh with a discharge rate of 2C is described. The C-rate is the rate, at which the batteries are being discharged. 2C discharge rate means the BESS will be discharged in half an hour.
The round trip efficiency is greater than 90 % and the system is able to operate for 4500 cycles (charge and discharge periods). It is made in a container with a length of 6 m, width of 2.4 m, and height of 2 m. It provides an energy density of 19.4 kWh/m^3.
Batteries are the main energy source, which is stored in form of DC voltage. The connection of battery storage units in series increases the system voltage and the connection in parallel increases the current.
The BESSs are used in peak shaving applications, voltage or frequency control, and islanding operation.

2.2.3 Redox Flow Storage

Furthermore, in [57], a vanadium Redox flow battery storage with nominal power of 200 kW and energy content of 1200 kWh connected to the grid is presented. This Redox flow based storage offers lower power density and lower efficiency. The round trip efficiency of this example is more than 70 % and it needs a much higher construction length of 28 m, width of 7.5 m, and height of 4 m. It offers an energy density of 1.4 kWh/m^3. The used electrolyte represents 30 % of the system's cost and offers a lifetime of more than 10000 cycles at 100 % Depth of Discharge (DoD).

2.3 Energy Management System

The energy management system is defined as foresighted, organized and systematized production, distribution and use of energy under ecological and economic objectives [42].
The energy management system is responsible for the energy and power flows coordination between the power grid and the storage system. The main goal is to ensure maximum reliability and high economic wins. The energy management is an intelligent link between the power grid and the battery storage and it prescribes the battery storage operating strategy [131]. The charging and discharging process is managed using the EMS. It represents the central BESS's unit managing the storage and its security. It ensures a secure BESS operation and controls the batteries' State of Charge (SoC). This unit also operates the storage economically to maximize the economical wins. The EMS communicates with internal BESS components and with other possible components outside the BESS. It operates with other users or with neighboring storage systems [130]. One important communication is established with the battery management system to obtain the batteries' SoC and get further information related to the batteries' state. The EMS is required to be intelligent enough to avoid disturbing or damaging the batteries. It is responsible for the whole energy and power management inside of the BESS and it contributes to the enhancement of the system's reliability.

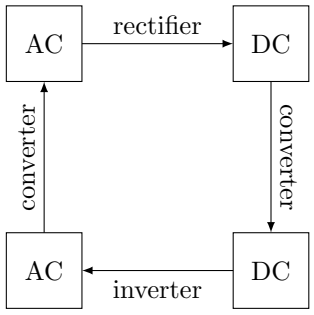


Figure 2.2 – Operation mode of power conversion.

2.4 Battery Management System

A Battery Management System (BMS) is an electronic circuit that monitors the battery-cells, measures, and calculates the most important data. It measures the individual battery-cells' voltages, currents, and temperatures. From these measured data further information about the battery-cells are estimated or calculated, e.g. the SoC and State of Health (SoH). The calculated and measured data are sent to the EMS using bus communication systems, e.g. CAN-bus.
In case of using multilevel inverters with split battery storage units, higher number BMSs are used and communicate with each other. The BMS must be able to protect the battery-cells and disconnect it in some critical operating cases. Therefore, it is responsible for the security of the batteries. Some active BMSs are also able to balance the battery-cells whenever different cell voltages or SoC are measured or calculated respectively.

2.5 Power Electronics

Converters are used for converting a given AC voltage to another AC voltage with a different amplitude or frequency.
They use a DC-link unit consisting of a capacitor or an inductor. The converters with DC-link capacitance are the most widely used topology in electric drives and grid connected inverters. For converting a given DC voltage level to another higher or lower DC voltage, DC-DC converters are used.
For DC to AC energy conversion, rectifiers and inverters are used. Rectifiers transform AC to DC voltages and are mostly not bidirectional and do not use active switches. An inverter is the bidirectional device transforming from DC to AC using active switches. Since the battery voltage is DC and the grid AC, inverters are used to invert the DC- into AC-voltages. For single-phase grids, one H-bridge inverter can be used e.g. as PV-inverter and for three-phase power grids B6-bridge inverters are used. The different names of the operation mode of power conversion presented are summarized in Fig. 2.2. The inverter is used for charging and discharging the storage units, as shown in Fig. 2.1. The power electronics, which are connected between the energy storage unit and the power grid, are able to control the energy transfer.
The power electronics have benefited from recent development of modern software, such as FPGA technology and real-time systems. They are compatible with simulation softwares and

thus can reduce the time required for system design and speed up the implementation phase. For three-phase system, the B6-bridge inverter is used and will be explained later.

2.6 Power Grid and Power Quality

Nowadays, decentralized power generation units using power inverters as a grid interface are increasing. Therefore, the power quality is playing a more important role. Inverters represent non-linear loads for the power grid. The current is not ideal sinusoidal due to the inverter switching voltage waveform. The power generation quality, as in [33], is based on three main pillars. The continuity of supply and commercial quality are not technical terms and depend on the power providers and their organization. The third term is about the power quality and depends on the grid connected power generation units. The power quality defines the accordance of physical terms and the used norms in national and international level at the PCC. The Total Harmonic Distortion (THD) and the harmonic spectrum based on the Fourier series describe the inverter effects on the power grid and are explained in the following section.

2.6.1 Fourier Series

To describe the effect of the non-sinusoidal behavior of an inverter and its effects on the grid, Fourier series are used. They allow to describe any periodic signal with a sum of sine wave signals. For this, using Fourier series Eq. (2.1), any signal could be described as the sum of DC-part $n = 0$, the fundamental waveform $n = 1$ and infinite individual harmonic [153].

$$\begin{aligned} f(t) &= \frac{a_{(0)}}{2} + \sum_{n=1}^{\infty} a_{(n)} \cdot \cos(n\omega t) + \sum_{n=1}^{\infty} b_{(n)} \cdot \sin(n\omega t) \\ &= \frac{a_{(0)}}{2} + \sum_{n=1}^{\infty} \sqrt{a_{(n)}^2 + b_{(n)}^2} \cdot \sin(n\omega t + \varphi_n) \end{aligned} \tag{2.1}$$

Whereby $\omega = 2\pi/T$, $a_{(n)}$ and $b_{(n)}$ are the Fourier coefficients represented as peak values and are defined in Eqs. (2.2)−(2.4). They represent the amplitudes of the sine and cosine functions generated by the Fourier series. Using Fourier series, signals could be regenerated from a given harmonic spectrum.

$$a_{(n)} = \frac{1}{T} \cdot \int_0^T f(t) \cdot \cos(n\omega t) dt \quad (n = 0, 1, 2, ...) \tag{2.2}$$

$$b_{(n)} = \frac{1}{T} \cdot \int_0^T f(t) \cdot \sin(n\omega t) dt \quad (n = 0, 1, 2, ...) \tag{2.3}$$

$$\varphi_n = \arctan\left(\frac{a_{(n)}}{b_{(n)}}\right) \tag{2.4}$$

Using non-linear loads, the possible harmonic could be predicted using Eq. (2.5). Using a single-phase system, e.g. B2-bridge inverter ($m = 2$) switching power supply, only the uneven harmonics (3, 5, 7, 9,...) could be measured. For B6-bridge inverter ($m = 6$), the uneven pairwise harmonics (5, 7, 11, 13, 17, 19,...) could be measured. The third harmonics disappear in three-phase system since the harmonics are in phase to each other using a three-phase system in star. In three-phase systems harmonics could be measured and grouped into positive ($3n$), negative ($3n + 1$), and zero ($3n - 1$) sequence [79].

$$h = (n \cdot m) \pm 1 \tag{2.5}$$

2.6.2 Total Harmonic Distortion

To evaluate the harmonics generated by an inverter, the Total Harmonic Distortion (THD) is introduced. It is calculated from the sum of each harmonic v_{n} relative to the fundamental v_{fund} and uses the square root function as in Eq. (2.6) i.e. of the voltage THD_v. The current THD_i is calculated in a similar way.

$$THD_v = \sqrt{\sum_{n=2}^{\infty} \left(\frac{v_n}{v_{\mathrm{fund}}} \right)^2} \tag{2.6}$$

The THD is generally measured only until the 40^{th} harmonic ($n = 40$) as given by the norm VDE0938-4 and IEC1000-3-4 [71] and is introduced as $THD_{v,40}$ [119]. This value is calculated by power analyzers using Eq. (2.7) for the measured voltages and currents.

$$THD_{v,40} = \sqrt{\sum_{n=2}^{40} \left(\frac{v_n}{v_{fund}} \right)^2} \tag{2.7}$$

Using VDE0839-4-2, EN61000-2-4 [72], and IEEE-standards [18], the THD should be considered and calculated until the 50^{th} harmonic ($n = 50$). The difference to the $THD_{v,40}$ is minimal since the amplitudes of higher harmonic are not high compared to the lower order harmonics. In the norm DIN EN50160, the limits for the harmonics in low voltage grid are as shown in Table 2.1. The $THD_{v,40}$ should not be bigger than 8 % throughout the inverter's operation range and 5 % at nominal operation.

2.6.3 Effects of Nonlinear Loads on the Power Grid

To describe the grid harmonic distortion in a single-phase system, the Thevenin grid model with internal impedance is presented in Fig. 2.3. A quick power exchange between the inverter and the grid causes variation on the grid voltage amplitude. Due to the dynamic inverter operation and a quick power reference change, the grid current i_{g} is changed with an additional load current Δi_n. The grid power changes in short time and causes an additional voltage drop over the grid impedance $v_{\mathrm{g,imp}}$ as shown in Fig. 2.3.
Using the Kirchhoff's voltage law (KVL) or mesh equation, the load voltage is calculated as in Eq. (2.8). It can be seen from this equation that the grid voltage depends on the grid current.

$$v_{\mathrm{load}} = v_{\mathrm{g}} - R_{\mathrm{g}} \cdot i_{\mathrm{g}} - L_{\mathrm{g}} \cdot \frac{\mathrm{d}i_{\mathrm{g}}}{\mathrm{d}t} \tag{2.8}$$

Table 2.1 – Maximum harmonic voltage distortion as a percentage of the fundamental as in IEEE-standard and DIN EN50160 [38] [68].

Odd harmonics				Even harmonics	
Not multiple of 3		Multiple of 3			
h	V_{rel} in %	h	V_{rel} in %	h	V_{rel} in %
5	6.0	3	5.0	2	2.0
7	5.0	9	1.5	4	1.0
11	3.5	15	0.5	6 to 24	0.5
13	3,0	21	0.5		
17	2.0				
19	1.5				
23	1.5				
25	1.5				

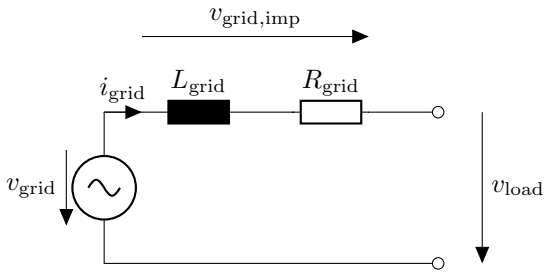


Figure 2.3 – Grid model to explain the voltage drop over the grid impedance by changing the load.

By grid connection of non-linear loads v_{load} with a non-sinusoidal current i_{g} , the grid voltage v_{g} is influenced and is also non-sinusoidal.
EN50160 [38], IEC1000-3-5 [71], and DIN VDE0838 part 3 (EN61000-3-3, IEC1000-3-3) [72] include limits for quick changes of the voltage.
To explain the non-sinusoidal load influence and the harmonics generated, an example is shown in Fig. 2.4. It represents the addition of the 3^{rd} ($v_{3\text{rd}}$), 5^{th} ($v_{5\text{th}}$), and 7^{th} harmonic ($v_{7\text{th}}$) to an ideal sine wave ($v_{1\text{st}}$) and the resulting distorted signal (v_{dist}). The amplitudes of the 3^{rd}, 5^{th}, and 7^{th} harmonics are one third, one fifth, and one seventh, respectively. In the harmonic spectrum, the amplitudes are given as shown in Fig. 2.5 and the THD of the resulting signal v_{dist} is more than 41 %. The resulting waveform represents the possible grid distortion by loading it with non-linear load.
Furthermore, recommendations for the harmonic voltage and current limits are given by IEEE-standard [68]. The voltage limits are shown in Table 2.2. For the currents, the limits are derived from the IEEE-standard and are shown in Table 2.3. The relevant voltage range for analyzing the current distortion limits is from 120 V to 69 kV [68]. Even harmonics are limited to 25 % of the odd harmonics shown in Table 2.3.
The low voltage grid delivers a root mean square (rms) line-to-line voltage of $v_{\text{LL,rms}} = 400\,\text{V}$. For devices with input current higher than 16 A, the standards EN61000-3-4 or EN61000-3-12 must be applied [29]. Grid with higher voltages until 50 kV are defined as the middle voltage grids while voltages over 110 kV correspond to the high voltage grid. The selection of grid voltage level depends on the power required by the customer.

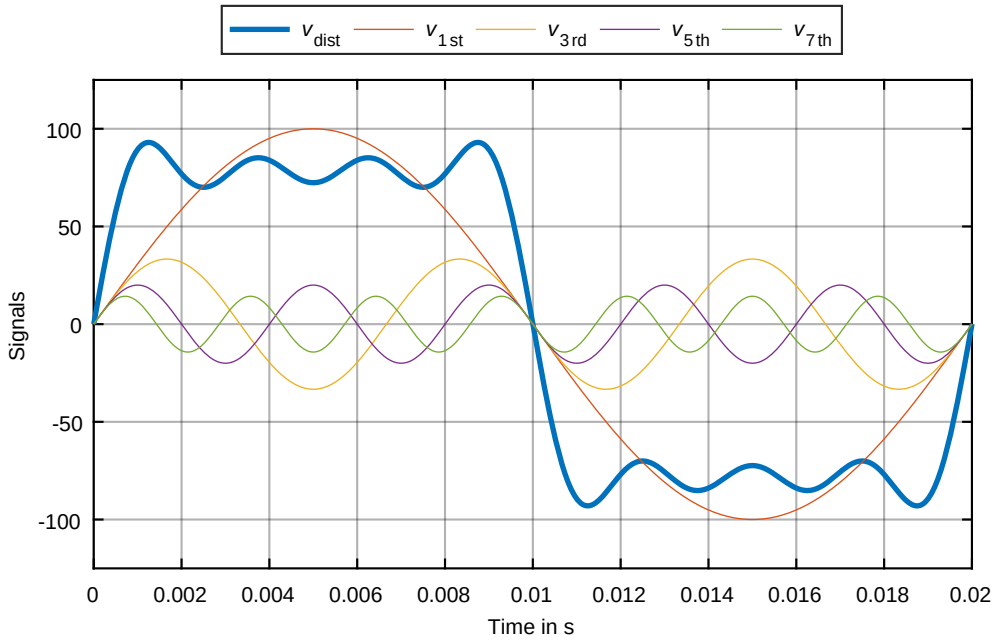


Figure 2.4 – Addition of the 3rd, 5th, and 7th harmonic to an ideal sine wave and the resulting signal.

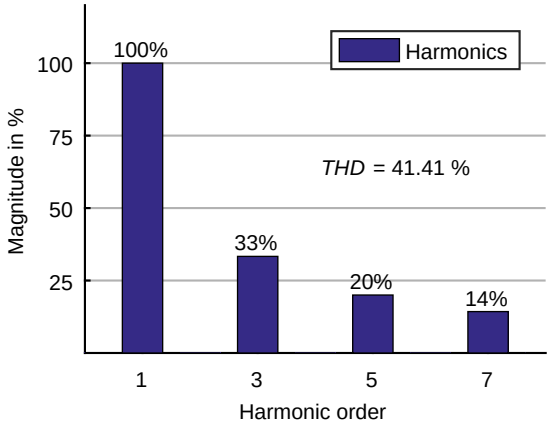


Figure 2.5 – Harmonic spectrum and THD of the resulting distorted signal v_{dist} in Fig. 2.4.

Table 2.2 – Maximum harmonic current distortion as a percentage of the fundamental [68] [93].

	Bus voltage v at PCC	Individual harmonics in %	THD in %
Low voltage	$v \leqslant 1.0\,\mathrm{kV}$	5.0	8.0
Middle voltage	$1\,\mathrm{kV} < v \leqslant 69\,\mathrm{kV}$	3.0	5.0
High voltage	$69\,\mathrm{kV} < v \leqslant 161\,\mathrm{kV}$	1.5	2.5
Highest voltage	$161\,\mathrm{kV} < v$	1.0	1.5

Table 2.3 – Recommended harmonic current distortion as a percentage of the fundamental given by IEEE-standard 519 [68].

Odd harmonics	Distortion limit in %
3^{rd} - 9^{th}	4
11^{th}–15^{th}	2
17^{th}–21^{st}	1.5
23^{rd}–33^{rd}	0.6
35^{th}–	0.3

2.6.4 Grid Connected Inverters' Norms and Standards

The grid regulations or rather requirements from the local power grid operators must ensure a safe and reliable grid with a given power quality. They promote the grid extension and integration of other renewable energy sources such as PV, BESS, or wind turbines.
The norm EN50160 [38] is an European norm for the power producers which defines the characteristics of the public power grid voltage. Whereby, the norm EN61000 [72] is applied for the consumers connected to the power grid.
In Germany, the regulations are defined by the DKE (Deutsche Kommission Elektrotechnik Elektronik Informationstechnik im DIN und VDE, German Commission for Electrical, Electronic and Information Technologies of DIN and VDE). At European level, the norm for low voltage grids are given in VDE-AR-N 4105:2011-08 [175]. This norm, which came in effect on August 2011, represents the low voltage directive and reference while connecting inverters to the low voltage grid. The main voltage parameters and their permissible deviation ranges at the customer's point of common coupling in public low-voltage electric distribution systems under normal conditions are as in [93]:

- Frequency range: The permissible frequency band is 47.5 Hz to 51.5 Hz. The plant must only disconnect if it reaches 51.5 Hz, but over 50.2 Hz the power is curtailed.
- Normal voltage operating range: The allowed voltage range is between $-10\,\%$ and $+10\,\%$ of the nominal grid voltage.
- Voltage quality: The voltage harmonics limits are given in Table 2.1, where h represents the voltage harmonic order. Inverter output voltage has high distortion due to its steps waveform behavior and affects the grid voltage even when a power filter is used. The voltage harmonics depend on the power grid model and its parameter.
- Current harmonics: The current harmonic levels limits are given in Table 2.3 [166].

The grid distortions caused by inverter have negative effects on the power grid operation and must be filtered and kept within the given limits. Those effects cause deviations in the grid voltage amplitude, the current form, and the grid fundamental frequency [88]. In Table 2.4, the inverter effects on the power grid are listed. The non-linear load of the grid causes periodic harmonics.
Harmonics are integer multiples ($n \cdot f_{\text{g}}$, $n \in \mathbb{N}$) of the fundamental frequency, whereby inter-harmonics are non-integer multiples of the fundamental frequency and are higher than the fundamental frequency ($\frac{n}{m} \cdot f_{\text{g}};\ m < 1$).
The sub-harmonics are also non-integer frequencies but smaller than the fundamental frequency ($\frac{n}{m} \cdot f_{\text{g}};\ m > 1$) [80].

Table 2.4 – Inverter effects on the power grid and their causes [36].

Parameter	Reason type	Reason
Grid voltage changes, flicker	Periodic	Power exchange variation
Transients	Non periodic	Inverter switching behavior
Voltage drop, voltage failure	Non periodic	Grid faults
Asymmetric grid voltage	Periodic and non periodic	Asymmetric load, asymmetrical inverter operation

By charging a BESS with only active power the inverter operates as a load and decrease the grid voltage amplitude at the PCC. The other way around, while discharging the BESS, the grid voltage at PCC increases. Furthermore, the inverter switching operation causes transients in the power grid by applying a reference value change.
Asymmetric loads, e.g. one or two phase operation of the power inverter, cause a grid voltage amplitude difference between the loaded and non-loaded phases. The limits for the grid effects depend on the ratio ($ratio_{S_{\mathrm{sc}}}$) of the grid short circuit apparent power $S_{\mathrm{sc,grid}}$ and the actual inverter apparent power $S_{\mathrm{nom,i}}$ as in Eq. (2.9). To vary the grid frequency, the ratio of the grid power to the inverter power should be close to one. In general, the power grid is a spatial decentralized system and contains power generation sources, transmission lines, power transformers, and loads [161].

$$ratio_{S_{\mathrm{sc}}} = \frac{S_{\mathrm{sc,grid}}}{S_{\mathrm{nom,i}}} \tag{2.9}$$

The standard EN6100-2-2 defines a maximum voltage THD_v of 8 % at the PCC of public power grid connection without defining the current harmonics limits. Whereby, the IEEE-standard 519 [68] describes the current and voltage harmonic content and is used as a comparison criteria and reference in further analysis. The first example shown is the single-phase inverter to analyze the explained effects.

2.7 Conclusion

The decentralized BESS represents a future opportunity to be used in combination with renewable energy generation. The different fields of application of BESSs are presented within this chapter. The different battery storage units are presented and actual projects in this field are shown. The electrochemical battery storage technology based on lithium-ions promises high power and energy density.
The required EMS and BMS are introduced and their function is explained. They represent an important part of any battery based storage system.
The grid connection of BESS is made using power electronic inverters and must consider the given standards and limitations. Therefore, the power quality is described and the related norms and standards are defined.

In the next chapter, single- and three-phase grid connected BESSs are simulated and their effect on the power grid are analyzed.

3 Grid Connected Single- and Three-Phase Conventional Inverter Topologies

This chapter presents an introduction to BESS based on single- and three-phase grid connected inverter topologies. Section 3.1 describes the single-phase H-bridge inverter. The uni- and bipolar pulse width modulation techniques are shown and compared to each other in Section 3.1.1. The inverter operation is validated using physical simulations in Section 3.1.2. In BESS, the effects of the DC-link capacitor's sizing are shown using different capacitances in Section 3.1.3. To conclude the usage of the conventional single-phase inverters, their efficiency is studied using measurements in Section 3.1.4.
Using single-phase inverters, the exchanged power is limited by the nominal phase current. Therefore, three-phase conventional B6-bridge inverters are introduced in Section 3.2. Based on a realized BESS, a conventional three-phase inverter topology is introduced in Section 3.2.1, simulations are done to explain their functionality in Section 3.2.2. However, using this topology in BESS leads to current ripple on the DC-link, which are shown using different DC-link capacitances in Section 3.2.3.
Finally, while still increasing the power, three-phase systems are limited due to the higher voltage range required. Therefore, multilevel inverter topologies are introduced.

3.1 Single-Phase H-Bridge Inverters

To connect a DC voltage source to an AC-power grid with minimum number of components, the H-bridge and B6-bridge inverters are used for single- and three-phase power grid, respectively. The inverter allows the batteries connection to the AC-power grid with a given amplitude, frequency, and a given shift to the grid voltage to control the active and reactive power transfer. The H-bridge inverter, also known as full bridge or B2-bridge inverter, consists of four power switches and is used in single-phase battery energy storage system as shown in Fig. 3.1. This inverter topology could be used in home storage systems to simplify their integration. The power and capacity ranges of such storage system are in kW and kWh-range, respectively [173].
Fig. 3.1 shows the conventional single-phase H-bridge inverter to be used in BESS applications. This topology is compatible with any other DC voltage source such as PV panel with Maximum Power Point Tracker (MPPT) or fuel cells. The DC voltage sources are connected to the grid through an H-bridge inverter and power filter for harmonics mitigation. In same BESS applications intermediate DC-DC converters are used to maintain the H-bridge inverter DC-link voltage at constant value. The H-bridge inverter, shown in Fig. 3.1, operates as a two and three-level voltage inverter, depending on the modulation scheme used, and has four useful switching states of the 16 possible states. Those switching states are shown in the Table 3.1. When T1 and T4 are switched on (state S3), the inverter output voltage is equal to the positive battery voltage. The negative battery voltage is measured at the inverter output

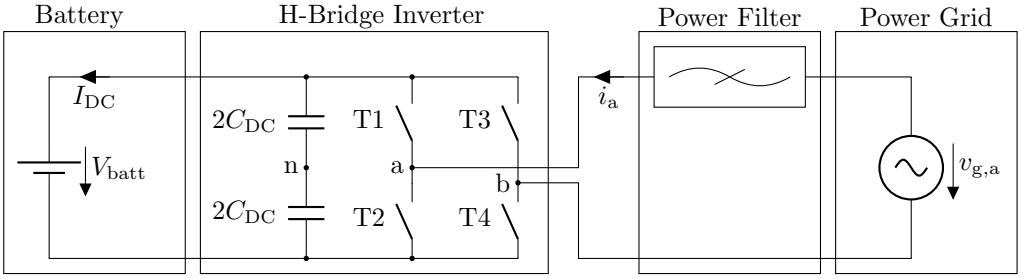


Figure 3.1 – System overview of conventional H-bridge inverter to be used in single-phase battery energy storage system.

Table 3.1 – Switching states of an H-bridge inverter and the resulting voltage.

Switching state	**T1**	**T2**	**T3**	**T4**	$\boldsymbol{v_{ab}}$
S1	0	1	0	1	0
S2	0	1	1	0	$-V_{DC}$
S3	1	0	0	1	$+V_{DC}$
S4	1	0	1	0	0

by switching the switches T2 and T3 (state S2). The other two possible switching states are the output voltage 0 V and the inverter phases are short circuited. In this case T1 and T3 (state S4) or T2 and T4 (state S1) are simultaneously active.

Grid connected inverters control the active and reactive power exchange by changing the shift between the grid phase voltage and current while keeping the grid effects as small as allowed by the standards. For grid-compliant operation, the inverter modulates the controller reference signal output using modulators. There are two possible sine based Pulse Width Modulation (PWM) techniques. The bipolar and unipolar modulations are introduced and explained in the next section.

3.1.1 Bipolar and Unipolar Pulse Width Modulation Techniques

There are different methods to control the power switches of power electronic inverters [46] [147]. The selection of those methods is based on different inverter operation parameters such as the switching frequency, inverter power losses, and harmonic distortion [64].

Inverters are generally modulating a sinusoidal reference signal during their grid connected operation. The amplitude of this reference signal affects the current flow values to or from the power grid. This reference signal is generally generated by the controller during the inverter operation. PWM is the most used modulation strategy for power inverters [64]. Especially, the sine based PWM is the most chosen modulation due to its simplicity. The modulation of a sinusoidal signal for an H-bridge inverter is possible in two ways: bipolar and unipolar.

To modulate a sinusoidal signal the bipolar and unipolar modulation techniques are represented using an ideal sinusoidal signal with a fundamental frequency of $f_{ref} = 50\,\text{Hz}$ and using a carrier-signal of frequency of $f_{cr} = 1\,\text{kHz}$. The peak to peak values of the sinusoidal and triangular signals are identical. The reference signal, described with Eq. (3.1) is compared to a carrier-signal with the same amplitude.

$$v_{ref} = \hat{V} \cdot \sin(2\pi t + \varphi) \tag{3.1}$$

The Sine-Sawtooth modulation is not studied due to the improved harmonic performance of Sine-Triangle modulation [64]. To describe a sine based modulation technique, two terms are relevant namely the amplitude modulation index m_{amp} which is defined in Eq. (3.2) and the frequency modulation index m_{f} shown in Eq. (3.3).

$$m_{\text{amp}} = \frac{\hat{V}_{\text{ref}}}{\hat{V}_{\text{cr}}} \tag{3.2}$$

$$m_f = \frac{f_{\text{cr}}}{f_{v_{\text{ref}}}} \tag{3.3}$$

By increasing the amplitude modulation index m_{amp} the mean inverter voltage increases. During the normal inverter operation m_{amp} is $0 < m_{\text{amp}} < 1$ and for values bigger than one, the inverter is over modulated. The frequency modulation index is used to describe the ratio of the carrier frequency over the fundamental inverter frequency.

Bipolar PWM The bipolar PWM modulation controls the inverter and generates the pulses for its gate driver by comparing the reference signal with the carrier-signals as shown in Fig. 3.2. The fundamental frequency or the reference signal, also known as modulating frequency, corresponds to the desired output voltage frequency [181] and is 50 Hz for a grid connected inverter. In the bipolar PWM scheme the two switches of each leg are switched in a complementary way. Using this modulation technique in the H-bridge inverter shown in Fig. 3.1, the switch pairs T1, T4 (state S3) and T2, T3 (state S2) are switched simultaneously, Table 3.2. When the reference signal is higher than the carrier-signal $v_{\text{ref}} > v_{\text{cr}}$, the first pair is switched on, otherwise the other pair is switched on as shown in Table 3.2. The H-bridge inverter output voltage contains only two levels $\pm V_{\text{batt}}$, therefore it is called bipolar PWM [126].

Table 3.2 – Switching states of an H-bridge inverter using bipolar PWM.

Condition	Switching state	T1	T2	T3	T4
$v_{\text{ref}} < v_{\text{cr}}$	S2	0	1	1	0
$v_{\text{ref}} > v_{\text{cr}}$	S3	1	0	0	1

Unipolar PWM When unipolar PWM is used, under similar conditions as the previous bipolar PWM, the resulting switching states are shown in Table 3.3. Unlike the bipolar PWM, the power semiconductors are not switched simultaneously [126].

Fig. 3.3 represents the unipolar PWM function principle in an H-bridge inverter. Two signals are required and are compared to one other signal [181]. Even the sinusoidal reference signal or the carrier-signal can be inverted.

Fig. 3.3 shows that by using the unipolar PWM similar inverter operation is reached when the carrier-signal or the sinusoidal reference signal are inverted. The carrier-signal inversion is achieved using the multiplication with -1 (mirrored, $|v_{\text{ref}} - 100|$) or by shifting it with an offset of 180°, which is practically not easy to implement because modulators are generally implemented in one hardware component. The inversion of the reference signal is easier for possible implementation and is further followed. The second and third plot in Fig. 3.3

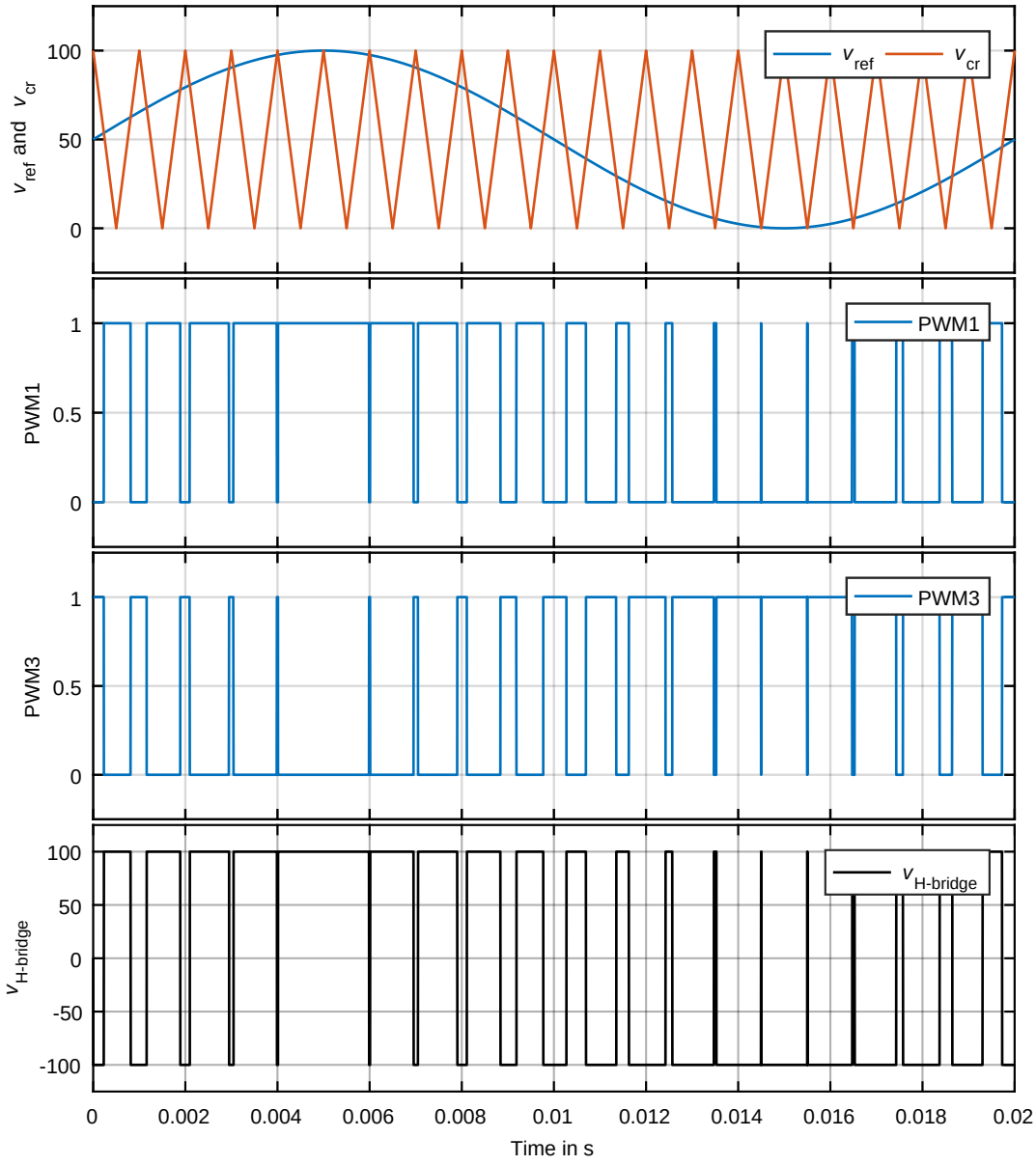


Figure 3.2 – H-bridge inverter bipolar PWM function principle using ideal sinusoidal signal with fundamental frequency $f_{\mathrm{ref}} = 50\,\mathrm{Hz}$ and carrier-signal with switching frequency of $f_{\mathrm{sw}} = 1\,\mathrm{kHz}$ (top plot). Both plots in the middle represent pulse signals for switches S1 and S3. The bottom plot shows the resulting two-level H-bridge inverter output voltage using bipolar PWM [16] [126] [181].

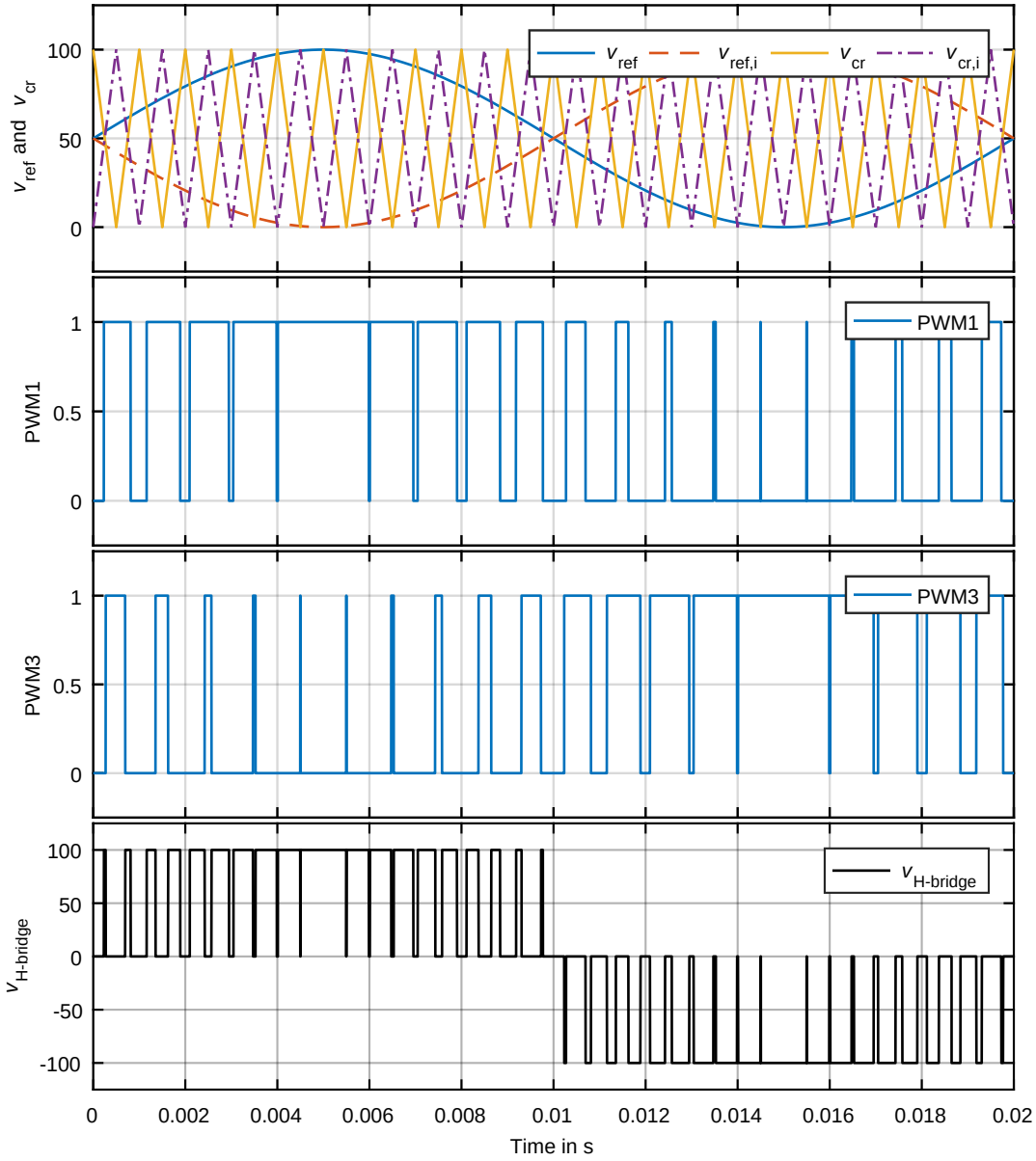


Figure 3.3 – H-bridge inverter unipolar PWM function principle using ideal sinusoidal signal with fundamental frequency $f_{\mathrm{ref}} = 50\,\mathrm{Hz}$ and carrier-signal with switching frequency of $f_{\mathrm{sw}} = 1\,\mathrm{kHz}$ (top plot). Both plots in the middle represent pulse signals for switches S1 and S3. The bottom plot shows the resulting three-level H-bridge inverter output voltage using unipolar PWM [16] [126] [181].

Table 3.3 – Switching states of a H-inverter using unipolar PWM.

Condition	Switching state
$v_{\mathrm{ref}} > v_{\mathrm{cr}}$	$T1 = 1;\ T2 = 0$
$v_{\mathrm{ref}} < v_{\mathrm{cr}}$	$T1 = 0;\ T2 = 1$
$-v_{\mathrm{ref}} + 100 > v_{\mathrm{cr}}$	$T3 = 1;\ T4 = 0$
$-v_{\mathrm{ref}} + 100 < v_{\mathrm{cr}}$	$T3 = 0;\ T4 = 1$

represent the PWM signal for the power switch T1 and T3 respectively. The signal in the second plot is similar to the signal using the bipolar PWM. The H-bridge inverter output voltage is shown in the fourth plot and contains three voltage steps at the AC-side while using unipolar PWM.
The resulting inverter switching frequency, using unipolar PWM, is twice as high compared to the bipolar PWM. The resulting inverter voltage also has three levels instead of two as shown in Fig. 3.3. Therefore, this modulation technique is used to present the operation of single-phase grid connected inverter.

3.1.2 Simulation of H-Bridge Inverter's Operation

The operation of a single-phase grid connected inverter, as in Fig. 3.1, is presented in order to discuss its advantages and disadvantages. The simulation parameter used are shown in Table 3.4 and are similar to the hardware of the used inverter parameters and are not discussed further. The simulation results are shown to validate its operation. Fig. 3.4 shows the current and phase voltage of the inverter and the grid in charging operation.
Using single-phase inverter, the DC-link current oscillates with the double of the nominal AC current frequency. Therefore, in the following section the effect of sizing the DC-link capacitor on single-phase application is explained.

Table 3.4 – Simulation model's parameters of the H-bridge inverter.

Parameter	Nomenclature	Value
Grid phase voltage	$v_{\mathrm{g,a}}$	230 V
Grid short circuit power	S_{short}	1 MVA
Ratio of grid impedance over grid inductance	$X_{R/L}$	2
DC-link battery voltage	V_{batt}	512 V
Inverter switching frequency	$f_{\mathrm{sw,B2}}$	8 kHz
Inverter nominal current	i_{n}	25 A
Power filter inductance	L_L	10 mH
Power filter internal resistance	R_L	12 mΩ
Low DC-link capacitance	$C_{\mathrm{DC,low}}$	4 mF
Internal resistance of $C_{\mathrm{DC,low}}$	$R_{C,\mathrm{DC,low}}$	258 µΩ
High DC-link capacitance	$C_{\mathrm{DC,high}}$	20 mF
Internal resistance of $C_{\mathrm{DC,high}}$	$R_{C,\mathrm{DC,high}}$	52 µΩ

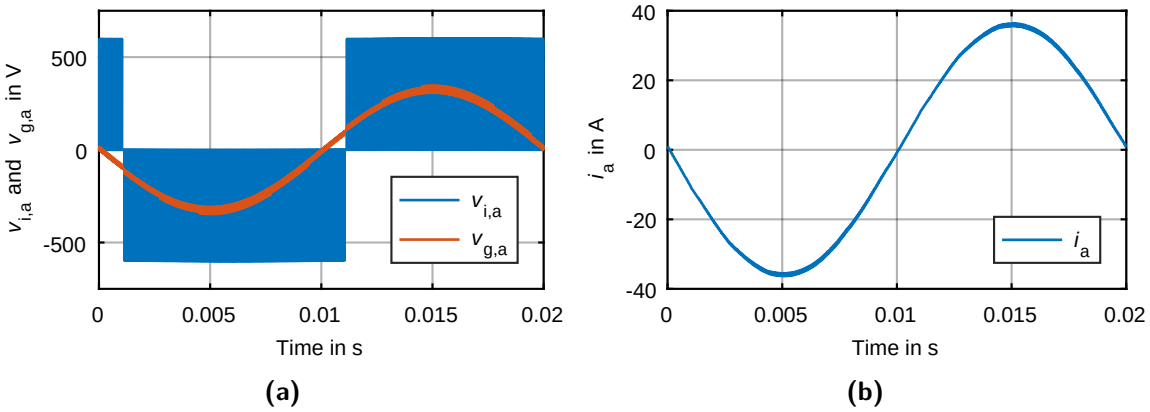


Figure 3.4 – H-bridge (a) inverter $v_{\mathrm{i,a}}$ and grid voltages $v_{\mathrm{g,a}}$ (b) and AC current i_{a} during the charging operation of the BESS.

3.1.3 DC-Link Circuit for the H-Bridge Inverter

A DC-link in the power electronic is a circuit used between the DC voltage source and the inverter power switches [183]. It represents a filter and an energy storage [16]. Two main DC-link circuits are used in power inverters: DC-link chokes store magnetic energy and DC-link capacitors store the electric energy [16].
Only the DC-link capacitor based inverters are further studied due to their wide usage. The capacitor used in DC-AC inverters is mainly used to minimize the voltage ripples on the DC-side and allows the inverter to operate with a constant DC voltage. In case of batteries, the DC-link capacitor should absorb the current ripple from the inverter to unburden the battery storage. The inverters' DC-link circuit practically contains more capacitors connected in parallel to increase the capacitance of the DC-link circuit and decrease the total resistance of the DC-link. Mostly aluminum electrolytic capacitors are used due to their high capacity and low price. Their main disadvantage is temperature dependency.
The higher order current ripples are filtered using DC-link capacitors. The low order ripples, 100 Hz as shown in Fig. 3.6, are not totally filtered, even by using DC-link capacitors. Those low frequency current ripples do not damage the studied battery and do not shorten the battery lifetime [43].
The study in [172] analyzed the high current ripple with different frequencies and their effect on 15 similar batteries using five different current frequencies for 1200 charge and discharge cycles. The results using the frequencies, 0 Hz (only DC-discharge), 10 Hz, 55 Hz, and 256 Hz at the test end show that the inner resistance is mostly similar and the batteries' ageing are similar and the batteries are not affected negatively. Using 14.8 kHz shows that the batteries inner resistance is higher and the ageing process is quicker. The "spread of values was found to be 10 times greater" for cells cycled with an AC ripple current of 14.8 kHz [172]. Therefore, it is highly recommended to use DC-link capacitors even if batteries are used.
In some applications DC-DC converters are used between the battery and the H-bridge inverter DC-link. The inverter DC-link capacitance should not be designed too large, because DC-DC converters already include high output capacitance. This connection allows a DC-load on the batteries since DC-DC converters usually contain big input and output capacitors. This case will be further studied later in Section 5.3.
In the following, the DC-link capacitance sizing is studied and its effect on the inverter

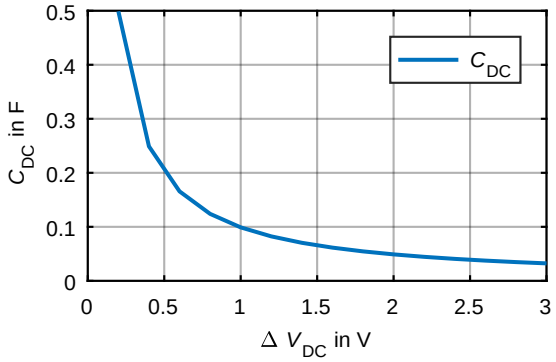


Figure 3.5 – Sizing the DC-link capacitance to decrease the voltage ripple ΔV_{DC} around a nominal voltage of 50 V.

operation and battery loading is shown. The DC-link current is a positive oscillating current with the double frequency of the AC-current, i.e. 100 Hz.
This behavior is not damaging the battery and its variation (peak to peak values) depends on the DC-link capacitance sizing. Increasing the DC-link capacitance decreases also the low order current ripple and helps avoiding these effects.
The capacitance C is defined as in Eq. (3.4) and the energy E_C stored in a capacitor is given in Eq. (3.5). This equation can be written as in Eq. (3.6) in case of voltage variation on the DC-link capacitor [183]. Therefore, the decreasing of the voltage ripple ΔV highly influences the size and the capacitance value used in the DC-link as shown in Fig. 3.5.

$$C = I \cdot \Delta t / \Delta V_C \tag{3.4}$$

$$E_C = \frac{1}{2} \cdot C V_C^2 \tag{3.5}$$

$$\Delta E_C = \frac{1}{2} \cdot C \cdot ((V_C + \Delta V_C)^2 - V_C^2) \tag{3.6}$$

$$C = 2 \cdot \Delta E_C / (\Delta V_C \cdot (2V + \Delta V_C) \tag{3.7}$$

Highly increasing the DC-link capacitance leads to higher charging current when the capacitor is fully discharged, ie.e at operation start. Furthermore, the charging resistor muss be highly dimensioned to slowly charge the capacitor and avoid high currents.
To show the DC-capacitance's sizing effect in single-phase inverters, an example is presented using the capacitances mentioned in Table 3.4. The AC current shown in Fig. 3.4a when using a capacitance $C_{\mathrm{DC,low}} = 4\,\mathrm{mF}$ leads to the DC-link current ripple shown in Fig. 3.6a. Whenever the capacitance is increased to e.g. $C_{\mathrm{DC,high}} = 20\,\mathrm{mF}$, the DC-link current oscillation is decreased as shown in Fig. 3.6. The current ripple decreases from 19 A to about 10 A due to the increased DC-link capacitance.
In [145], a detailed capacitor Equivalent Series Resistance (ESR) model is shown. However, only the simplified model is further used and consists of a capacitor and its ESR.

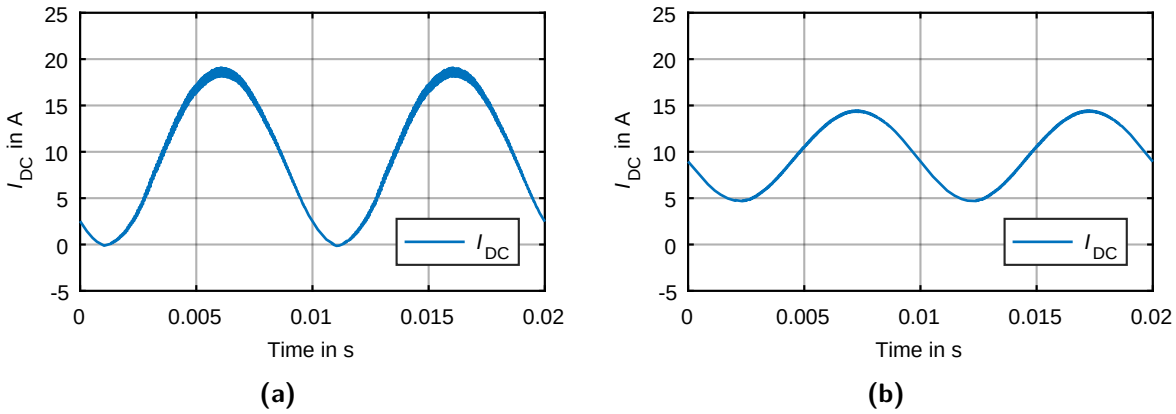


Figure 3.6 – H-bridge inverter DC-link currents using different capacitance values of (a) 4 mF and (b) 20 mF.

3.1.4 Efficiency of Conventional Single-Phase Inverters

Fig. 3.7 represents measurements assessment of DC-AC conversion efficiencies as a function of DC input power for eleven micro-inverters with single PV module inputs done in [37]. The measured DC-AC conversion efficiencies of different inverters are shown. Based on those measurements, the European Union (EU) efficiencies η_{EU} and the California Energy Commission (CEC) efficiencies η_{CEC} for the micro inverters have been calculated according to Eq. (3.8) and (3.9). The resulting values for η_{EU} are between 88.7 % and 95.4 %, whereby the η_{CEC} is between 90.9 % and 95.6 % [37].

$$\eta_{\mathrm{EU}} = 0.03\ \eta_{5\,\%} + 0.06\ \eta_{10\,\%} + 0.13\ \eta_{20\,\%} + 0.1\ \eta_{30\,\%} + 0.48\ \eta_{50\,\%} + 0.2\ \eta_{100\,\%} \tag{3.8}$$

$$\eta_{\mathrm{CEC}} = 0.04\ \eta_{10\,\%} + 0.05\ \eta_{20\,\%} + 0.12\ \eta_{30\,\%} + 0.21\ \eta_{50\,\%} + 0.53\ \eta_{75\,\%} + 0.05\ \eta_{100\,\%} \tag{3.9}$$

3.1.5 Motivation for Three-Phase Inverters

Single-phase energy storage systems are used as home storage since low power and energy content are required. By increasing the capacity of these storages and their power, the connection is done to the three-phase inverter.
The higher power requirement obligates the change to three-phase systems, which is mainly the use case for big houses and industrial applications and emergency power. An inverter also enables alternative power generation for low voltage applications in case of an off-grid system or in case of unavailability of the main power grid. In standard houses, 16 A fuses in the phases are built. Therefore, the power for a single-phase is limited to a maximum of 3.7 kVA. If more power is required, generally more than 3 kVA, [16] three-phase inverters are used.

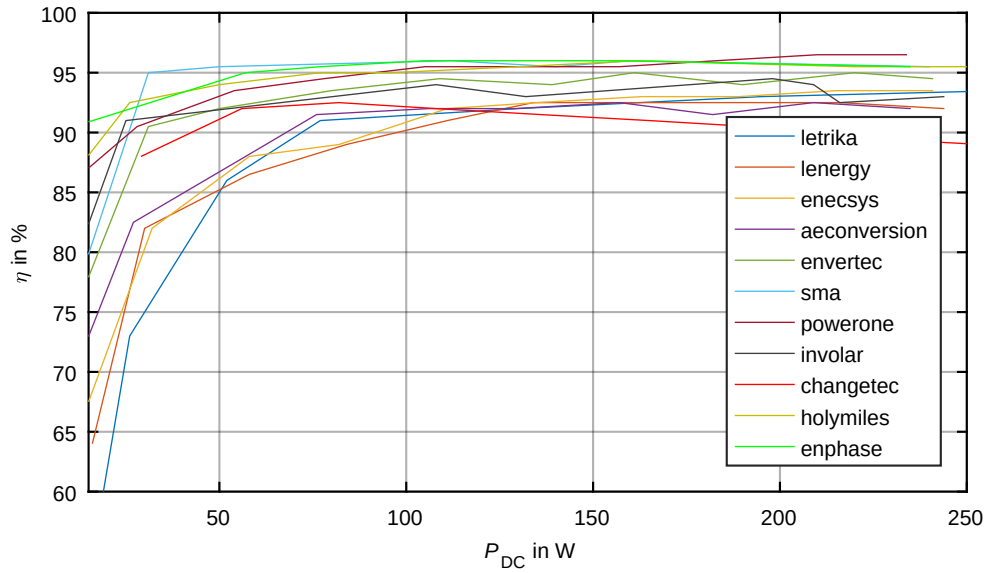


Figure 3.7 – Measured DC-AC conversion efficiencies as a function of DC input power for eleven micro-inverters with single PV module inputs [37].

3.2 Three-Phase B6-Bridge Inverters

B6-bridge inverters are the most common classical and conventional topology used in grid connected applications and also in three-phase electric drives. B6-bridge inverter contains, as from their name, six components. If these six components are diodes, the inverter is called B6U (uncontrolled B6-bridge) and is used only as a rectifier for power conversion in one side. There is also another topology using three active switches and three diodes which is called B6H (half controlled B6-bridge). The B6-bridge inverter with six active switches is known as fully controlled bridge, B6C. The switching frequency using standard silicon semiconductors is in the range from 4 kHz to 20 kHz. This range is a compromise between switching losses and system's dynamics and depends also on the switch semiconductors used and the inverter's power range.

3.2.1 Example of BESS based on B6-Bridge Inverter

A B6-bridge inverter, used in an energy storage demonstrator, is described in [99] and [130]. For three-phase system, the B6-bridge inverter is used with the minimum possible number of switches, which is six. It is simple to control and uses the least number of power switches, which is mostly relevant for industrial applications to reduce the costs. It uses the B6C inverter topology which consists of six Insulated-Gate Bipolar Transistors (IGBTs) and uses a switching frequency of 8 kHz. The B6-bridge inverter is on the AC-side connected through the power filter, an LCL-filter, to the power grid.
The Energy Neighbor [130] is an example of BESS using the topology shown in Fig. 3.8. The energy storage system comprises a plurality of AC-side parallel-connected units of battery-cells and power electronics. Therefore, the installed units enable a modular expandability and a scaling of the maximum amount of storable energy [132]. An example of this topology is

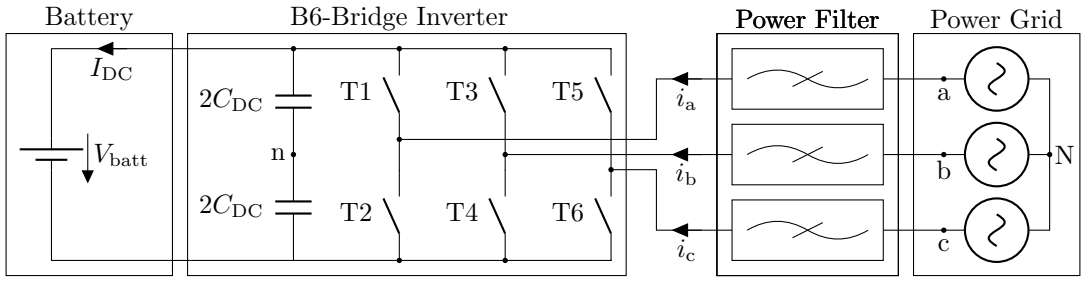


Figure 3.8 – System overview of conventional three-phase B6-bridge inverter for battery energy storage system.

presented in EEBatt-project [130] where a prototype with nominal power of 200 kW and nominal energy content of 250 kWh is implemented to be connected to the low voltage grid. The battery-rack used consists of 208 LiPo-cells connected in series to guarantee the DC-link voltage required by the inverter in the range from 580 V to 750 V. The BESS consists of eight racks, each one contains 13 battery modules connected in series. The battery storage developed in [129] consists of eight battery-racks and is used as a reference for a typical battery storage system based on the B6-Bridge inverter topology. The modularity and scalability of this system is done on the AC-side.

The battery modules in [129] consist of 192 battery-cells connected in parallel and series. To increase the battery module voltage and keep its maximal voltage under the safe low voltage limit of 60 V, 16 cells are connected in series.

The nominal battery modules voltage in [129] is $V_{batt} = 51.2\,V$. Whereby, the maximal and minimal voltages are $V_{batt,max} = 57\,V$ and $V_{batt,min} = 44.6\,V$. To increase the battery modules' capacity, 12 cells are connected in parallel. The battery module uses the cells combination of 16s12p, which means that 16 cells are in series and 12 in parallel. Using 3 Ah cells results in a capacity of 36 Ah of each submodule. Therefore, the modules energy content at nominal voltage is 1.84 kWh.

The battery-cell's voltage is variable and depends on its SoC. Fig. 3.9 represents the measured open-circuit voltage of a lithium-ions battery-cell, which is constant in a wide SoC-range. The DC-link voltage is similar to the cell's voltage shown in Fig. 3.9 because all cells are stacked in series and connected without DC-DC converter to the B6-bridge inverter. Therefore, the system costs are low and the efficiency is increased.

For connection of DC sources to the three-phase grid, a minimal DC-link voltage of $\sqrt{2}\cdot 400\,V = 565\,V$ is required. In [132], the inverter DC-link voltage range required is 580 V–750 V [151]. Therefore, the battery-racks shall consist of 13 battery modules connected in series. The required high voltage power switches must be able to switch on and off the DC-link voltage. The actual semiconductor voltage range limits the further increasing of the B6-bridge inverter's DC-link voltage and power.

3.2.2 Simulation of B6-Bridge Inverter's Operation

A physical simulation model is used to explain the operation of a BESS using the B6-bridge inverter topology connected to the low voltage grid using an LCL power filter. To operate on the low voltage power grid with line-to-line rms voltage $V_{LL,rms} = 400\,V$, the DC-link voltage must be higher than $400\,V \cdot \sqrt{2} = 565\,V$ in addition to the voltage drop over the power

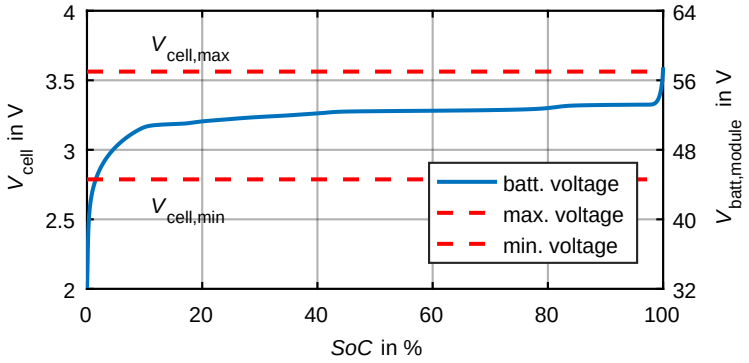


Figure 3.9 – Measured cell open-circuit voltage and operation range limits.

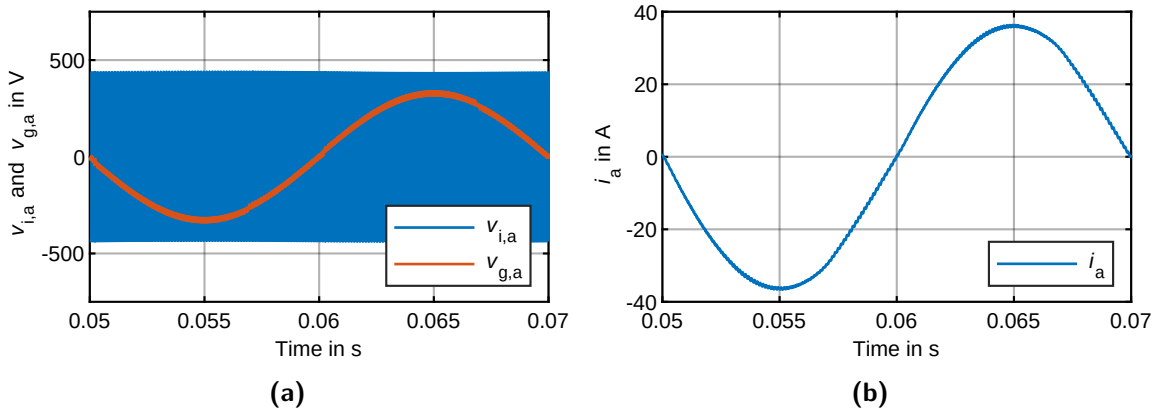


Figure 3.10 – B6-bridge (a) inverter $v_{\mathrm{i,a}}$ and grid voltages $v_{\mathrm{g,a}}$ (b) and AC current i_{a} during the charging operation of the BESS.

filter. The maximum value of the DC-link voltage is limited by the voltage rating of the used power semiconductors. The inverter switches the whole DC-link voltage on and off during its operation.
Fig. 3.8 shows the conventional topology of a three-phase B6-bridge inverter based battery energy storage system. The BESS presented in [130] is used for the simulations as a reference. On the DC-side, a battery stack, containing a high number of battery packs connected in series, is connected to the inverter DC-side. The used power filter is always an LCL-filter, with a main inductance and an LC-part for filtering the low and high order harmonics respectively. Fig. 3.10 shows grid and inverter voltages. The inverter phase voltage has only two levels $\pm\frac{V_{\mathrm{batt}}}{2}$. In this case, the AC current is also synchronized to the power grid voltage, since the BESS is in charging phase. The power grid and filter parameters are similar to the parameters in Table 3.5.

3.2.3 DC-Link Circuit for the B6-Bridge Inverter

Similar to the DC-link capacitance sizing effect on the single-phase inverter, the sizing of the DC-link of a B6-bridge inverter is explained. Fig. 3.11 shows the capacitance value effects in grid connected B6-bridge inverter using capacitance values of 1.4 mF [151] and its tenths to

Table 3.5 – Simulation model's parameters the B6-bridge inverter.

Parameter	Nomenclature	Value
Line-to-line grid voltage	v_{ab}	400 V
DC-link battery voltage	V_{batt}	750 V
Inverter switching frequency	$f_{\mathrm{sw,B6}}$	8 kHz
Low DC-link capacitance	$C_{\mathrm{DC,low}}$	0.14 mF
Internal resistance of $C_{\mathrm{DC,low}}$	$R_{C,\mathrm{DC,low}}$	7400 µΩ
High DC-link capacitance	$C_{\mathrm{DC,high}}$	1.4 mF
Internal resistance of $C_{\mathrm{DC,high}}$	$R_{C,\mathrm{DC,high}}$	739 µΩ

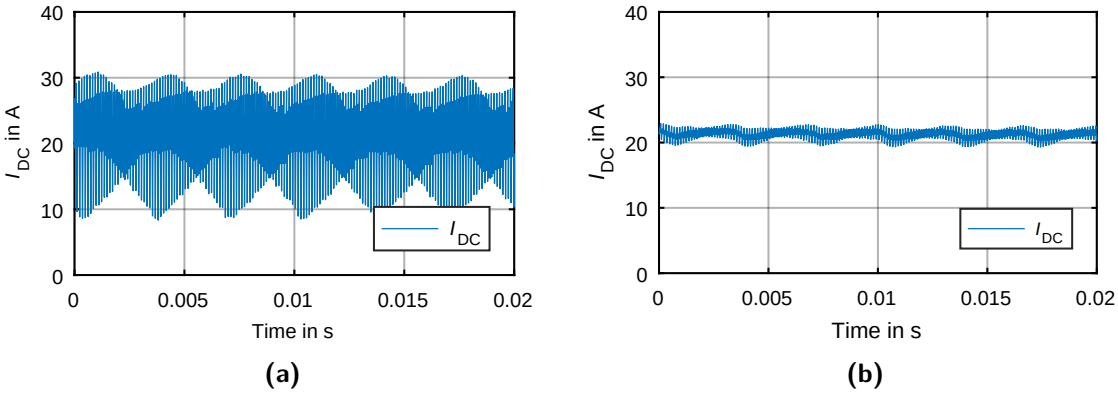


Figure 3.11 – B6-bridge inverter DC-link current using different capacitance values of (a) 0.14 mF (b) and 1.4 mF.

show the capacitor sizing effect.
The current oscillation in B6-bridge inverters is low compared to the H-bridge inverter, since it uses three half-bridges. B6-bridge inverters require smaller capacitance to reach similar current oscillation compared to the H-bridge inverter. Fig. 3.11 shows the B6-bridge DC-link current using different capacitance values with low order oscillations of 300 Hz, because it uses six switches during the inverter operation in one period. The current ripple on the B6-bridge inverter using a small capacitance, e.g. $C_{\mathrm{DC,low}} = 0.14\,\mathrm{mF}$ is $\Delta I_{\mathrm{DC}} = 22.2\,\mathrm{A}$ as shown in Fig. 3.6a. By increasing the capacitance to e.g. $C_{\mathrm{DC,high}} = 1.4\,\mathrm{mF}$, the current ripple on the DC-link current is reduced to $\Delta I_{\mathrm{DC}} = 3.5\,\mathrm{A}$, as shown in Fig. 3.6b.
The efficiency of the used B6-bridge inverter in [130] at nominal operation point is 96 %. Therefore, the round trip efficiency is 92 %. To minimize the losses and increase the BESS efficiency, multilevel inverter topologies can be used.

3.3 Conclusion and Motivation for Multilevel Inverter Topologies

The three-phase two-level inverter is presented and simulation results are given, using an example of a BESS. The DC-link capacitance sizing effect on the DC-link current ripple is shown. The B6-bridge inverter topology represents the widely used topology in grid connected and electric drive inverters. To summarize, the B6-bridge inverter topology advantages and disadvantages are listed in Table 3.6.

Table 3.6 – Advantages and disadvantages of B6-bridge inverter topology.

Advantages	**Disadvantages**
The simplest possible topology for three-phase systems	LCL-filter or sine filter is required for norm compliant grid operation
Low component and development costs and available by many suppliers in the market	Large sized power filter is required
Reliable and experimented power switches	Limited scaling of the inverter power
Simple inverter control	Connection to the middle voltage only over transformer is possible
Robust structure due to the used components	Lowest number of components leads to lowest failure probability
More compact design	High voltage at centralized DC-link
Easier diagnosis of errors due to its less complexity	Isolation and security required due to the high voltage used
Simpler modulation technique	Largely sized DC-link capacitance
Proven technology	Higher switching frequencies, higher switching losses and therefore lower efficiency
Lowest possible number of components	

BESSs are continuously evolving due to the increase of the irregular power generated by renewable energy sources. To increase the energy exploited, efficient power conversion devices are required for grid connection.
Increasing the BESS power range, B6-bridge inverters, that actually dominate the low voltage grid connected inverters' market, face limitations due to their maximum DC-link voltage. The power inverter is the main key component for efficient energy conversion in grid connected BESS. Actually major projects are using standard two-level inverter, due to the advantages shown in this chapter.
The power increase could be reached by developing higher voltage semiconductors with higher voltage blocking capability or by using multilevel inverter topologies. The usage of multilevel inverters allows a direct inverter connection up to the medium voltage power grid [149].

4 Multilevel Inverter Topologies

The B6-bridge inverter topologies are limited in their power while increasing their output voltage. Multilevel inverters allow to increase the power by switching more voltage level steps. In this chapter, the multilevel inverter topologies are introduced in Section 4.1. The application of those topologies is detailed in Section 4.2. The first traceable single-phase three-level inverter is presented in Section 4.3. The mainly used three-phase multilevel inverter topologies, the cascaded H-bridge, the neutral point clamped, and the flying capacitor clamped inverters, are presented in Section 4.4, 4.5, and 4.6, respectively.
After comparing their main advantages and disadvantages, the suitable topology to be used in BESS is selected in Section 4.7.

4.1 Introduction to Multilevel Inverter Topologies

The B6-bridge inverters are suitable for low voltage applications due to limited voltage range of the power semiconductors. However, in the recent years, the demand for high power inverters has increased. Multilevel inverters present great advantages compared to conventional and very well-known two-level inverters [46] [148] [149]. They are suitable for high and medium voltage electric drives [108] [142] [168] and BESS [107].
However, in low voltage applications, multilevel inverters with low voltage power semiconductors for increased efficiency are not often used, e.g. in grid connected BESSs.
The name of multilevel describes their operation principle and their functionality. They use multiple voltage steps to generate alternating voltage levels. Multilevel means that the inverter voltage output consists of multiple steps (three or higher number of positive and negative voltage steps). Fig. 4.1 and Fig. 4.2 [183] represent an explanation of the voltage level increase using one half-bridge inverter and four of them connected in series. The half-bridge inverter generates two output voltage levels as shown in Fig. 4.1. The output voltage of the circuit shown in Fig. 4.2 contains five-level steps. All inverters with more than two output voltage levels are called multilevel. The corresponding output voltages are shown in Fig. 4.1 and Fig. 4.2. For the multilevel inverter operation, an array of power semiconductors and capacitors are used.
While increasing the power of a given electrical system, the current should not be increased, due to the quadratic rise of the conduction losses in the inverter. Therefore, the power increase is done by using more voltage levels, which is also limited by the capability of actual power semiconductors. The voltage increase can be reached by increasing the number of voltage steps by connecting higher number of power semiconductors in series. The concept of multilevel inverters first appeared as the demand for high power applications at more voltage levels was raised [108].
There are two main categories of multilevel inverter: the centralized and decentralized topologies, depending on the used voltage sources.

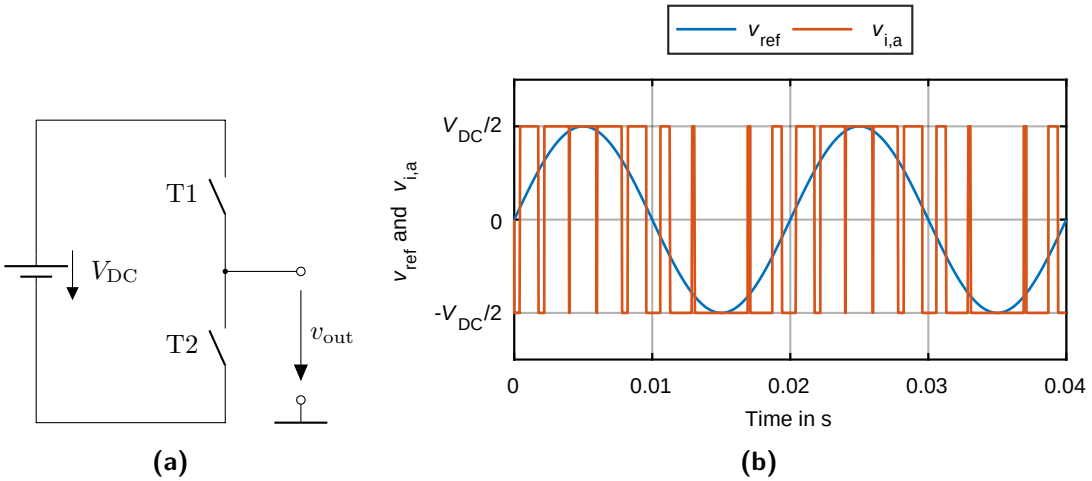


Figure 4.1 – Schematic circuit for two-level inverter and its output voltages [183].

4.1.1 Advantages of Multilevel Inverters

Multilevel inverters, as in [46] [148], allow a reduction of the voltage stress on the power switches, due to their series connection. They use less expensive components with lower voltage range, e.g. Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) instead of IGBTs. Increasing the number of components leads to the increase of availability through redundancy and allows the reduction of the harmonic distortion which leads to the usage of smaller passive power filters with reduced cost and weight.
Additionally, multilevel inverters operate at lower switching frequencies and the switching losses decrease. Therefore, the system efficiency is higher and the acoustic noise and electromagnetic interference is lower, when compared to two-level topologies. The Electromagnetic Compatibility (EMC) properties and capabilities are better.

4.1.2 Disadvantages of Multilevel Inverters

Using higher number of components, compared to B6-bridge inverters, multilevel inverters require higher control power and synchronized operation of high number of power switches, which means higher cost. Furthermore, by increasing the number of components of any system, its failure probability increases.
Additionally using multilevel inverters requires multiple DC voltage sources or banks of series connected DC-capacitors, which leads to complex control systems for higher number of component and voltage levels.

4.2 Applications of Multilevel Inverters

The multilevel inverters are used in RES e.g. in PV applications[15] and can be used in VAR-generator systems as in [141] [8]. They are scalable and theoretically could be connected to diverse power grid voltage ranges. They allow connecting the used system to the medium voltage grid without using an expensive medium voltage transformer.

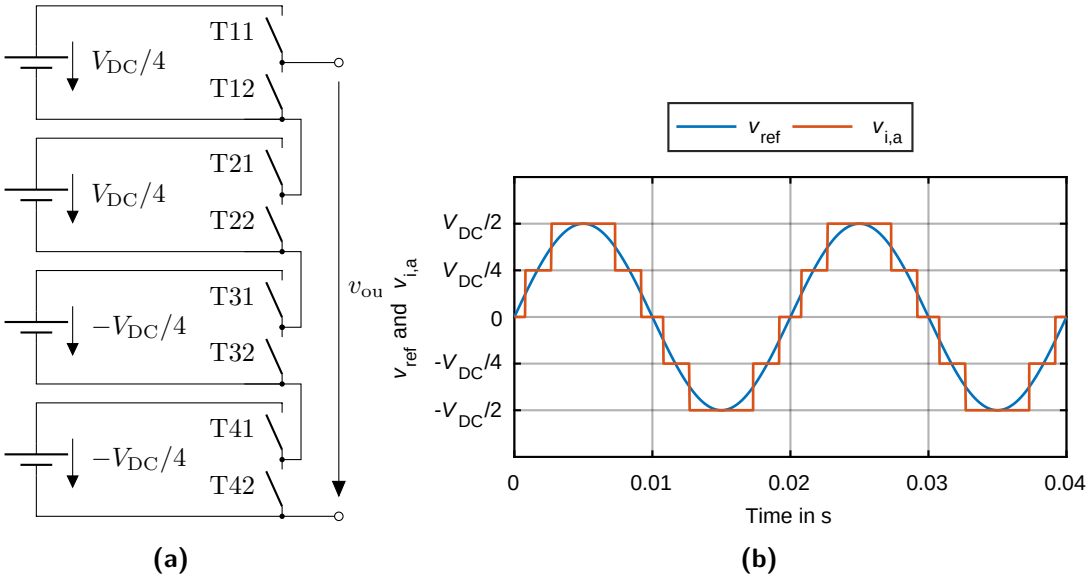


Figure 4.2 – Schematic circuit for multilevel inverter and its output voltages [183].

The high costs of this transformer represent a big part of the inverter system cost in medium voltage applications. Furthermore, multilevel inverters generate a voltage output with less distortion and the switches' stress is lower compared to conventional two-level inverters with medium voltage transformer.
The multilevel inverters are often used in electric drives and electric vehicles [178] [169], motor drive and utility applications [56] [141], regenerative type motor drive applications [55] [7], laminators mills, conveyors, pumps, fans, blowers, and compressors.
The active researches on multilevel inverter are, as in [46], to simplify the control schemes, reduce THD using optimization algorithms, reduce the current ripples, and further to eliminate specific harmonics.
The design application while constructing a higher level inverter (i.e. more than 7-levels [19]) has resulted in bulky and large inverters. The system complexity still represents a drawback of those inverters and increases their development cost.
Using multilevel inverters in 400 V applications, e.g. in a BESS, increases the system efficiency, compared to the conventional B6-bridge inverters. The use of several extra-low voltage power semiconductors in series, e.g. 100 V, with better switching behavior and lower conduction resistances is possible. The idea of using more power switches in series started in medium and high voltage applications, since nowadays power electronic semiconductors are not reliable for high voltage [108] [148]. However, the tolerance of the components leads mostly to problems and failure, while connecting power switches directly in series. Therefore, multilevel inverters are used.
Further industry application for medium voltage power inverters are summarized in Table 4.1. In the next section, the history of multilevel inverters is explained using one phase system. However, the further studied inverters are mainly used in the three-phase configuration.

Table 4.1 – Industry application for medium voltage power inverters [89].

Application	**Industry Sector**	**Power Range**
Turbo compressors (export gas, LNG gas, pipelines, gas storage, air separation), reciprocating compressors, centrifugal pumps	Oil and Gas	1–100 MW
Hot rolling mill drives (rougher, plate mill, CSP mill, finishing mill), cold rolling mill (single stand reversing mill, cold tandem mill, skin pass mill), sectional steel mill (beam line), blast furnace converter	Metals	2–25 MW
Pumps (boiler feed pump, cooling medium pumps), coal mills, conveyor belts, blowers. fans, startup converters for gas turbo generators and storage pump generators, static var compensators, HVDC-links, Static frequency changers, power converters for wind turbines	Power	2–25 MW
Ore mills, mine hoists, conveyor bells, pumps. crushers, blowers, compressors, bucket wheel excavators	Mining	2–15 MW
Pumps, blowers	Water	0.5–40 MW
Propulsion drives, booster-generators, thrusters, winders, dredge pumps	Marine	2–20 MW
Extruders, pumps, compressors, blowers, cement mils, fans, mixers, presses	Chemical, Cement, Pulp, and Paper	0.5–4 MW

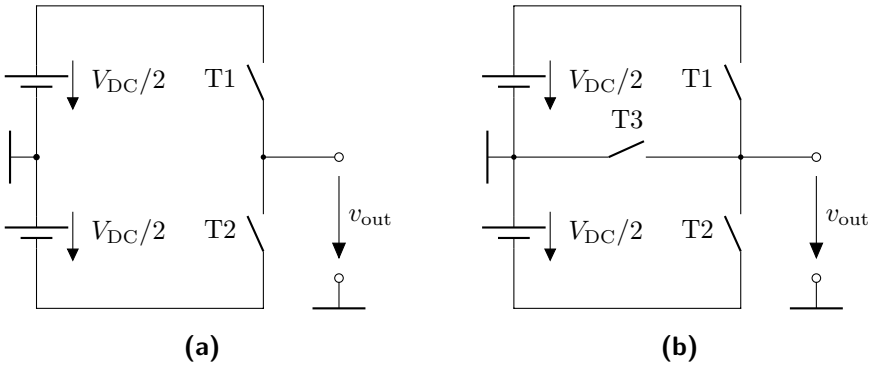


Figure 4.3 – Two- and three-level inverter topologies.

4.3 Three-Level Single-Phase Inverters

In 1973, the patent [67] presented the first traceable and possible three-level inverter, using a connection to the DC-link middle point. It allowed the inverter, shown in Fig. 4.3, to generate three levels. The three-level PWM control was presented by Prof. Holtz in Germany in 1982, after his patent [67]. It discussed the extension of a half-bridge topology as shown in Fig. 4.3a using a middle bidirectional switch as shown in Fig. 4.3b. However, this suggested topology still has the disadvantage, that the used switches must be able to block the whole DC-link voltage range V_{DC}. Whenever the second power switch T2 is on, T1 should be able to block the whole voltage V_{DC} [66]. Therefore, the switches used must be in the voltage range of V_{DC}.

4.4 Cascaded H-Bridge Inverter

History The first patent [11] related to the CHB multilevel inverter was introduced in February 18, 1975. "The device inverts from direct to alternating current" [11] using seven H-bridge inverters connected in cascade. A submodule of this inverter consists of an H-bridge inverter and its DC-link capacitor. The usage of seven submodules allows to generate seven positive, seven negative steps, and the zero voltage. In total, the output voltage contains 15 steps and the inverter called 15-level CHB inverter. In the American regions, steps of the line-to-line voltage are counted. In the case of using seven H-bridge inverters, the line-to-line voltage contains 29 levels.
The patent [11] is the earliest invention of multilevel inverter using cascaded H-bridges to generate more level steps. This topology did not get much attention after its patent until the mid of the 1990^{th}. Due to the high demand for medium voltage high power inverters, CHB got more attention. The CHB has become inevitable for motor drive and utility applications with two major patents [141] [56].
In order to use CHB inverters in regenerative type motor drive applications, two more patents [7] [55] were published. The probable application, suggested in the patents, are fuel cells, solar cells, thermal electric devices, which involve conversion of chemical, radiation, and thermal energy into electrical energy. One submodule of the presented patent is shown in Fig. 4.4. After these patents, further patents were published in 1997 [141] [8] to be used in VAR-generator systems. Many hybrid inverters emerged out of this topology, but are not

discussed further.
The CHB inverter is the most modular inverter topology discussed, since it is easy to maintain, even during its operation mode. Its three-phases can be connected in star or delta [142]. Using the star connection, the number of phases is at least one and can be varied and increased. For single-phase operation of the star connected topology, the neutral point must be connected to the power grid ground.
The modularity of this topology allows cascading low voltage rating components to be connected to medium voltage electric drives or power grids using three to ten H-bridge inverters connected in series [34]. CHB inverters are established in the market of medium voltage drives and are able to synthesize a medium output voltage based on a series of power cells using standard low-voltage components [116].
In combination with RES, cascaded multilevel inverter uses PV modules as a DC-link voltage source and consists of several in series connected cells [27] [46] [81] [112]. The CHB inverter can be used for motor drive and utility applications [141] [56] and in regenerative type motor drive applications [7] [55].
Due to the modularity of this topology, the inverter can be used for high power application up to 31 MVA [83]. For BESS, CHB multilevel inverters offer the capability of embedding small energy storage units in a split manner, given the existence of several submodules operating at lower voltages [107]. From its early development, the CHB multilevel inverter was designed as a battery charger and discharger to store energy from other generation units [114]. A transformer-less energy storage system based on a multilevel CHB inverter with star configuration used for medium grid voltage connection. For this, three different power switches were recommended, depending on the total output voltage levels [114].
The three CHB inverter's phases can be connected in star or triangle. The star topology is the widest used topology and is here further analyzed. It is also possible to connect a B6-bridge inverter to the star point of the CHB inverter to double the number of levels as discussed in [96]. However, here only the star connected CHB inverter is discussed and further analyzed to be used in BESS.

Operation The operation of the CHB inverter is similar to the presented H-bridge inverter operation. A submodule is active when it is involved in the AC current (MOSFET-states 1010 or 0101). A passive submodule has not been switched on and only forwards the current (state 1100 or 0011). The submodules are switched on one after the other.
Table 4.2 represents the states of the five-level CHB shown in Fig. 4.4. Only the states of the upper switches of each H-bridge inverter are presented in Table 4.2 with the assumption, that each half-bridge switches complementary (when T11 is switched on, T12 is directly switched off). The switch states presented lead to a five-level output voltage using two H-bridge inverters with split battery modules. The five-level CHB inverter output voltage with the corresponding switching states is represented in Fig. 4.5.

The split DC-power sources are mainly realized using a transformer with multiple output windings and represent generally a main disadvantage for this topology. The CHB inverters require isolated DC-sources such as PV panels or battery modules. The number of required components for an n-level output voltage are $2(n-1)$ power switches in each phase. Since each H-bridge inverter needs one DC capacitor, $\frac{1}{2}(n-1)$ capacitors are required.

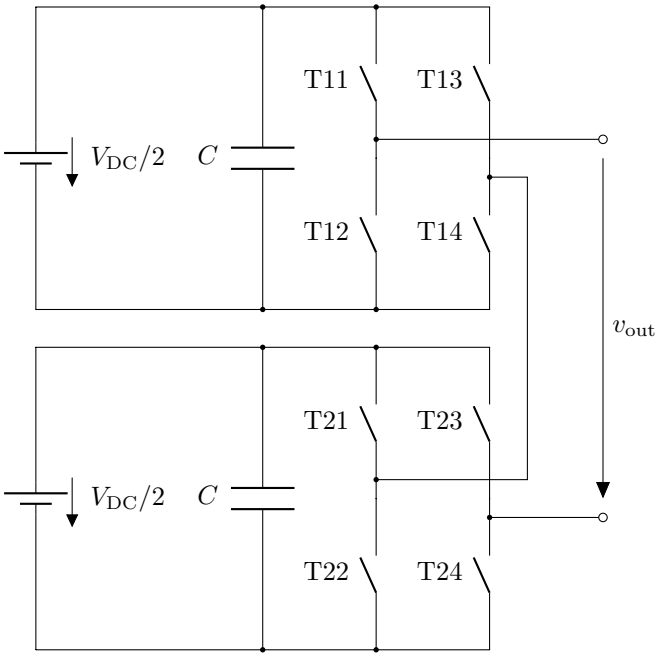


Figure 4.4 – Basic circuit of the CHB inverter.

Table 4.2 – Switching states of a five-level CHB inverter and the resulting voltage.

Switching state	T11	T13	T21	T23	Output
S1	1	0	1	0	V_{DC}
S2	1	0	1	1	$\frac{1}{2}V_{DC}$
S3	1	1	1	1	0 V
S4	1	1	0	1	$-\frac{1}{2}V_{DC}$
S5	0	1	0	1	$-V_{DC}$

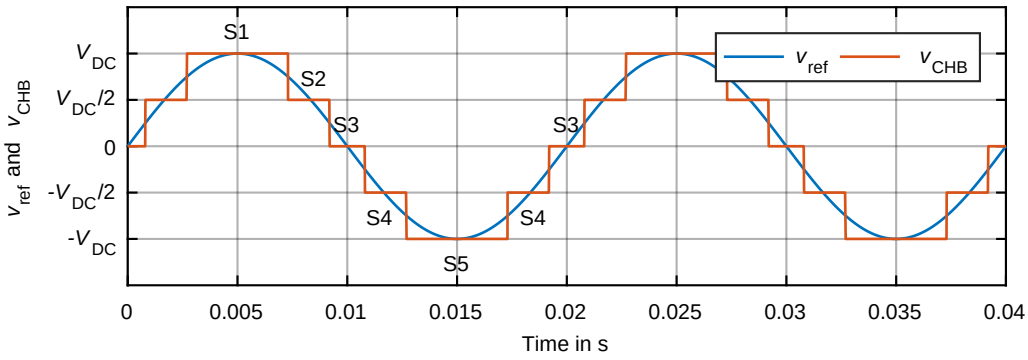


Figure 4.5 – Output voltage of the circuit in Fig. 4.4 with the switching states in Table 4.2.

Advantages Using split battery modules as a DC voltage source for the H-bridge inverter allows the usage of power switches with low voltage range. This leads to increased inverter efficiency. Using more voltage steps, the harmonic distortion caused by the inverter operation

decreases significantly.
"One of the major limitations of the multilevel inverters is the voltage unbalance between different levels when a transformer is used" [108]. Using DC battery sources solves this problem, since they offer almost constant voltage. The idea of using more small power inverters with low voltage steps in series allows a multilevel output voltage, as shown in Fig. 4.1 and Fig. 4.2 [183].
Whenever the voltage range of the used power switch is lower than the inverter output voltage, the losses are lower than in the conventional two-level inverter.
Increasing the number of submodules, using e.g. the phase shifted PWM at constant H-bridge inverter switching frequency, leads to increased CHB inverter switching frequency. While keeping the CHB inverter switching frequency constant, the switching frequency of the submodules decreases. Therefore, the switching losses of the components are lower compared to other multilevel inverters.
Furthermore, the components used in multilevel inverters are well researched. Compared to other multilevel topologies, CHB inverter needs the lowest number of components while increasing the number of voltage levels and it offers highest modularity. Using higher number of voltage steps, multilevel inverter topologies decrease the THD, which leads to small power filter for harmonic mitigation and grid-compliant operation. Furthermore, at higher number of levels, the DC voltage sources could be designed to avoid exceeding the low voltage limits.
The IEC60364 defines any AC-voltage higher than 1 kV range as an high AC voltage and low voltages are between 50 V and 1000 V. The extra-low AC-voltage is less than 50 V.
In [176], the DC voltage is defined as high for values higher than 1500 V. The low DC voltages are between 120 V and 1500 V. The extra-low DC voltage is less than 120 V. In EN61140 [177], the AC voltage level is similar to the IEC-standard [176]. However, the extra low voltage DC voltage is set to 75 V. The German norm VDE0140-1 is similar.

Disadvantages Multilevel inverters contain a high number of power switches compared to the B6-bridge inverter. Therefore, the control system is more complex. One special disadvantage of CHB inverters is the usage of decentralized power source units (submodules), which means more cables for the batteries and more complex battery management systems. In BESS, when using split battery modules, the requirements of their BMS are higher. Each submodule operates with its own BMS and all BMSs are connected to each other e.g. while using master slave configuration. The ground of each submodule is different from the other ones. Therefore, the signal ground of the BMSs must be galvanic isolated from the submodule's ground.
The BMS normally needs to measure the current from and to the battery modules and needs therefore a current sensor in each submodule. This means higher system costs by increasing the number of levels. Using the cascaded structure, the switches inner resistance is summed and this increases the conduction losses.
Using this topology, the battery load is similar to the one using a single-phase inverter as shown in Section 3.1. The low order current ripples are an exception while using batteries and as shown before, it does not represent a special disadvantage [172].
Conventionally, the individual isolated voltage sources are realized using multi-winding transformer with the same number of isolated secondary winding as used submodules. This leads to a huge and expensive system. [121].

4.5 Neutral Point Clamped Inverter

History As an idea to expand the half-bridge inverter using a middle switch, the first three-level inverter was introduced and published by Prof. Nabae from Japan in 1981 [133]. This inverter uses an "auxiliary switch device in to clamp the output terminal potential to the neutral point potential" and is called the first Neutral Point Clamped inverter (NPC) or Neutral Point Diode Clamped (NPDC) inverter. Actually, Siemens [159] [160] and ABB [1] [3], and General Electric [49] use the three-level NPC topology in PWM medium voltage drives for the power range 1–28 MVA. The inverters consist of medium voltage IGBT and IGCT and are connected to 2–4 kVA voltage grid.
The five-level NPC used from ABB [2] is to be connected to the 6 kV voltage grid.

Operation As shown in Fig. 4.6, four power transistors are connected in series and the diodes are used as clamping elements to generate a three-level alternating output voltage. Using this topology, the switches could be designed only for the half of the DC-link voltage $\frac{V_{\mathrm{DC}}}{2}$, which represents a main advantage against the topology presented in [67]. The NPC inverter is used in voltage ranges of 2.3 kV to 4.16 kV, and in some applications up to 6 kV [149] and represents the most used topology in industrial applications. In the patent [12], NPC inverters are used in high power and voltages (higher than 600 V) switching and motor drive applications. The operation of the NPC inverter can be explained using the states shown in Table 4.3. When the switches T1 and T2 are switched on, the output voltage is equal to $\frac{1}{2}V_{\mathrm{DC}}$. Switching T1 off and T3 on leads to a 0 V output voltage.
Finally, T2 is turned off and T4 on. It leads to an output voltage of $-\frac{1}{2}V_{\mathrm{DC}}$. Using this switch scheme, the power semiconductors never switch the whole DC-link voltage and lower voltage range of the power switches can be selected. By increasing the number of levels, the voltage range decreases by increasing the number of required diodes.
The three-level NPC inverter's output voltage with the corresponding switching states is represented in Fig. 4.7.

Table 4.3 – Switching states of an NPC inverter and the resulting voltage.

Switching state	T1	T2	T3	T4	Output
S1	1	1	0	0	$\frac{1}{2}V_{\mathrm{DC}}$
S2	0	1	1	0	0 V
S3	0	0	1	1	$-\frac{1}{2}V_{\mathrm{DC}}$

Advantages The NPC inverter is easy to control and since it uses passive elements for clamping, the costs are lower. To synthesize a waveform with n voltage levels, $(n-1)$ DC-link capacitors are required. Each phase requires $2(n-1)$ power switches and $(n-1)(n-2)$ diodes. Therefore, the costs are lower compared to other multilevel inverter topologies. Using lower voltage rated power switches, the efficiency is higher than using two and three-level inverter topologies. Therefore, it is easy to control, when compared to other topologies.

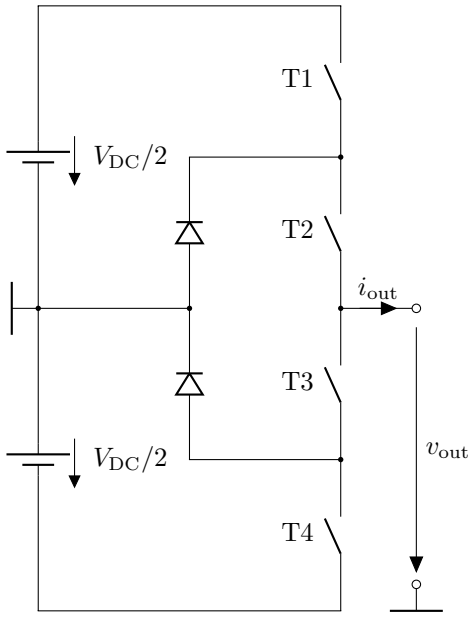


Figure 4.6 – Basic circuit of the neutral point clamped inverter.

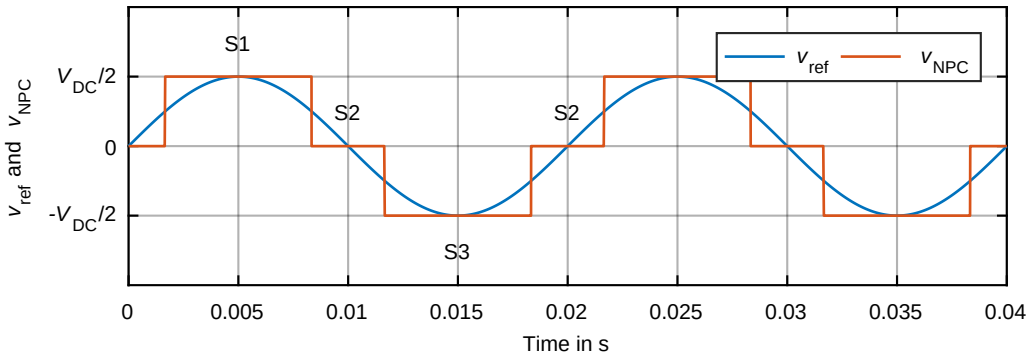


Figure 4.7 – Output voltage of the circuit in Fig. 4.6 with the switching states in Table 4.3.

Disadvantages There is an unbalanced stress on power semiconductors during the operation of the NPC inverter. Furthermore, its modularity is limited, when the system is already designed for a given number of levels. It needs a high number of diodes and it contains a higher number of components, at more than three-level output voltage, than other multilevel inverter topologies.
Moreover, this topology requires one central and high DC-link voltage while increasing the inverter power.

4.6 Flying Capacitor Clamped Inverter

History Floating capacitors could be used instead of the diodes as proposed in [133]. This inverter topology was presented for the first time as capacitor-clamped inverter (flying capacitors) in [62] [108] [122]. This topology was introduced by Prof. H. Foch in France in

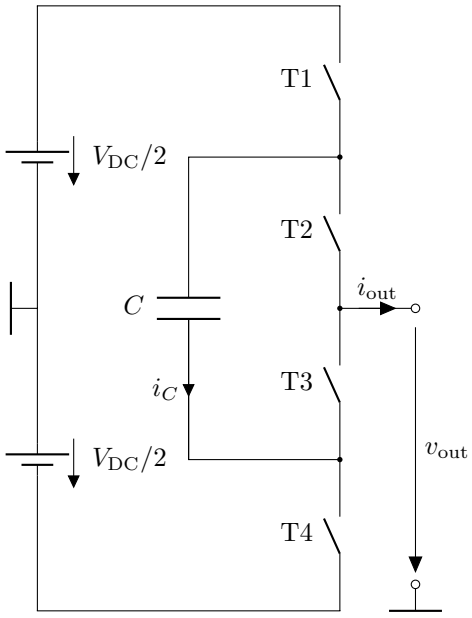


Figure 4.8 – Basic circuit of three-level flying capacitor clamped inverter.

1992 [123] and uses flying capacitors instead of clamped diodes and it is "safer and more simple to control and delivers purer output waveform" [123]. The first patent about Capacitor Clamped Converter (FCC) was published in September 16, 1997 [109]. This topology inverts from DC to AC using capacitors as clamped elements. It is compatible also for high voltage power conversion. It is recommended to be used in higher operating frequencies [109]. Single-phase of this inverter is shown in Fig. 4.8 using four power switches, mostly IGBTs, and one clamping capacitor to generate a three-level inverter output voltage. This topology requires $n-1$ capacitors on the DC-side and $2(n-1)$ power switches for each phase and $\frac{1}{2}(n-1)(n-2)$ clamping capacitors.

Operation The operation of the FCC inverter can be explained using the states shown in Table 4.4. When the switches T1 and T2 are switched on, the output voltage is equal to $\frac{1}{2}V_{DC}$ and no current flows through the capacitor. Switching T2 off and T3 on leads to a 0 V output voltage and the capacitor is charging. The switches T1 and T3 are then turned off while T2 and T4 on. The capacitor is discharging and the output voltage is still equal to 0 V. Finally, the T2 is turned off and T3 on. It leads to an output voltage of $-\frac{1}{2}V_{DC}$. Using this switch schemes, the power semiconductors never switch the whole DC-link voltage and lower voltage range of the power switches can be selected. By increasing the number of levels, the voltage range decreases.
The three-level FCC inverter's output voltage with the corresponding switching states is represented in Fig. 4.9.

Advantages The FCC inverter topology is also easy to control because it uses passive clamping elements. The power dissipation in this multilevel inverter topology is equally divided among all power semiconductors.

Table 4.4 – Switching states of a FCC inverter and the resulting voltage and capacitor current.

Switching state	T1	T2	T3	T4	Output	i_C
S1	1	1	0	0	$\frac{1}{2}V_{\mathrm{DC}}$	0
S2	1	0	1	0	0 V	$+i_{\mathrm{out}}$
S3	0	1	0	1	0 V	$-i_{\mathrm{out}}$
S4	0	0	1	1	$-\frac{1}{2}V_{\mathrm{DC}}$	0

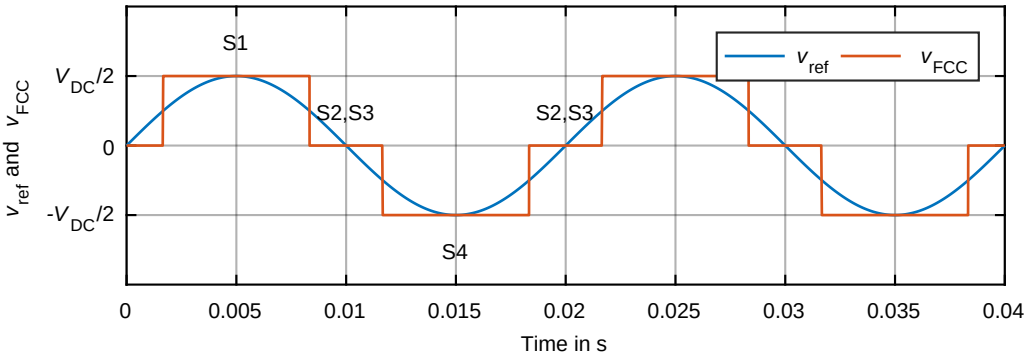


Figure 4.9 – Output voltage of the circuit in Fig. 4.8 with the switching states in Table 4.4.

Disadvantages The FCC inverter requires higher switching frequencies and balanced clamped capacitor voltages at a high DC-link voltage. Since the capacitors are more expensive than diodes, the costs of this inverter are higher when compared to the NPC inverter.

4.7 Conclusion and Selection of the CHB Multilevel Inverter Topology

The three main multilevel inverter topologies are presented and compared to each other in this chapter. In the following, one multilevel inverter topology is selected to be used in an efficient and modular BESS.
The multilevel inverters presented in the literature are mostly mixes or with minimal changes of the three main multilevel inverter topologies (CHB, NPC, FCC).
The number of required components for one phase of the discussed multilevel inverter topologies is summarized in Table 4.5. For comparison, Fig. 4.10 is a graphical equivalent of Table 4.5 with the total required components using the three main multilevel inverter topologies at different output voltage levels. To achieve the same number of voltage levels (higher than 7-levels), the CHB inverter needs less number of components as shown in [20] and [108]. The CHB inverter will need the minimum number of components if compared to other multilevel inverter with the same output voltage levels [20]. The multilevel inverter topologies losses are compared in [171]. It is shown that the CHB inverter reaches efficiencies up to 99.07 %, the NPC inverter 99.09 %, and the FCC inverter 98.44 % using 6.6 kV power switches and different switching frequencies (NPC and FCC inverter 1050 Hz and CHB inverter 550 Hz). BESS needs inverters with modular structure. To increase the capacity of the BESS or its power, CHB inverters offer highest modularity when compared to other main multilevel inverter topologies.

Table 4.5 – Number of required components in the three main multilevel inverter topologies for each phase.

Component	**CHB inverter**	**NPC inverter**	**FCC inverter**
Power switches	$2(n-1)$	$2(n-1)$	$2(n-1)$
Clamping diodes	0	$(n-1)(n-2)$	0
Clamping capacitors	0	0	$\frac{1}{2}(n-1)(n-2)$
DC-link capacitors	$\frac{1}{2}(n-1)$	$n-1$	$n-1$

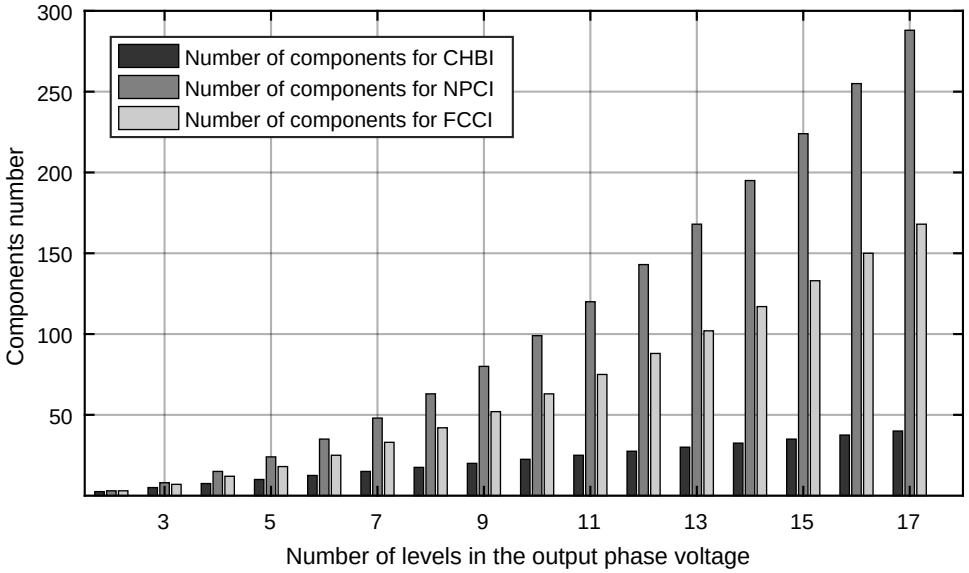


Figure 4.10 – A comparison between the number of components in different multilevel inverter topologies [20].

It offers flexibility and is fault tolerant.
Due to its efficiency and modularity, the CHB inverter is best compatible to be used in BESS and is further analyzed. This topology consists of cascaded submodules. Those have three different possible circuit topologies and are further discussed.

5 Circuit Topology of the Cascaded Submodules

The CHB multilevel inverter is selected to be the topology used in the BESS, which is connected to the low voltage power grid. Its submodule's circuit is discussed in this chapter. In general, the submodules deliver the output voltages $+V_{\mathrm{DC}}$, $-V_{\mathrm{DC}}$, or 0 V using at least one H-bridge inverter.
There are two main CHB inverter topologies depending on their submodule's circuit, presented in section 5.1. The one-stage topology contains only H-bridge inverters in the cascaded submodules and is shown in section 5.2.
The two-stage variant uses an additional intermediate DC-DC converter and is further divided into two possible cases. The DC-DC converter delivers constant DC-link voltages higher or lower than the battery voltage as shown in sections 5.3 and 5.4, respectively. Since the battery voltage is not constant, DC-DC converters are used in the two-stage topology to maintain the DC-link voltage for the H-bridge inverter at constant value. For this, the battery voltage is converted up or down using step-up or step-down DC-DC converters respectively.
At the chapter's end, the submodule's topology used for further analysis is selected in section 5.5.

5.1 Introduction to the Submodule's Circuit Topologies

In this section, a comparison between three different topologies of the CHB inverter's submodules is discussed. In the one-stage topology, the submodule consists of only an H-bridge inverter. The two-stage topologies use an additional DC-DC converter, a step-up or step-down, to keep the H-bridge inverter's DC-link voltage at constant value.
To implement a BESS based on the CHB inverter topology, split battery modules are required. The main property of the CHB inverter's submodules is their maximum voltage, which is lower than the extra-low safe voltage limit given by the standards [176][177]. This voltage range keeps the batteries under the low voltage range and can be handled easily and securely. Those battery modules consist of 192 LiFePo4 cells. The cell's nominal voltage is $V_{\mathrm{cell}} = 3.2\,\mathrm{V}$ and the nominal capacity is $E_{\mathrm{cell}} = 3\,\mathrm{Ah}$. 16 cells are connected in series and 12 cells are connected in parallel to increase the capacity to 36 Ah [129]. The measured cell's open-circuit voltage and operation range limits of one cell are shown in Fig. 3.9. The normal operation range of the batteries is defined by the battery management system (BMS). At $SoC = 100\,\%$, the maximum battery voltage is $V_{\mathrm{batt,max}} = 57\,\mathrm{V}$, at $SoC = 20\,\%$ the nominal battery voltage is $V_{\mathrm{batt,nom}} = 51.2\,\mathrm{V}$, and at $SoC = 0\,\%$ the minimum battery voltage is $V_{\mathrm{batt,min}} = 44.6\,\mathrm{V}$ (the battery modules are not deep-discharged at this SoC).

5.1.1 One-Stage Topology using H-Bridge Inverter

The one-stage topology consists of multiple H-bridge inverters connected on the DC-side to the battery modules. On the AC-side, the submodules are connected to each other in series. This topology offers the highest possible efficiency because the batteries are directly connected to the H-bridge inverter's DC-link. Furthermore, cascading multiple power switches allows the usage of lower voltage range power semiconductors. They usually offer the advantage of very low internal resistance and dissipate less power in conducting operation than power switches with higher voltage range.
Since the number of required submodules is calculated based on the minimum DC-link battery voltage, this topology provides more redundancy and higher fault tolerance at higher values of the batteries' SoC.
On the other hand, the disadvantage of this topology is the number of active submodules. Depending on the actual SoC of the battery modules, the number of voltage steps changes. This leads to variation in the number of CHB inverter's output voltage levels. Therefore, the voltage and current THD at the PCC are not constant.

5.1.2 Two-Stage Topology using additional DC-DC Converter

Through embedding an additional stage between the H-bridge inverter and the battery modules, the DC-link voltage is kept constant while the battery voltage changes. Furthermore, the second stage allows the use of different kinds of storage chemistry or same storage with different ageing. The two-stage topology allows to unequally discharge the battery modules using different DC-link currents and offers a new point of freedom. By changing the DC-link voltage of one submodule, the battery module connected to the DC-DC converter delivers more or less power by similar DC-link current and is quicker discharged or charged. A five-level CHB inverter operates on the grid e.g. with a nominal current of $I_{\mathrm{rms}} = 10\,\mathrm{A}$. The submodule with the DC-link voltage of 60 V delivers lower power and is less discharged than the submodule with the DC-link voltage of 80 V. This degree of freedom can be used for further balancing strategies used in the EMS to balance the SoC during the inverter operation.
Furthermore, using the two-stage topology allows an operation at constant number of output voltage levels at the PCC. This leads to a stable and grid-compliant operation.
Using higher number of power switches (for the DC-DC converter) increases the submodule failure probability but on the other hand also increases the fault tolerance of the system.
One main drawback of the two-stage topology is the lower efficiency compared to the one-stage topology. Using an additional power converter stage decreases the submodule efficiency [97]. The power flow is bidirectional and therefore the round trip efficiency highly decreases. It is reported in [170], that the efficiency of DC-DC converter using matching modulation techniques allows efficiencies of about 99 % (in 300 kW range). The realized hardware's efficiency is less than 97 % (while charging or discharging), as shown in the following sections. The round-trip efficiency is therefore approximately 94 %.
Furthermore, using more components in the two-stage topology, two additional power switches, one high current inductor, and the corresponding voltage and current measurement, increases the system costs and requires more space in the submodule. The DC-DC converter volume is higher than the used H-bridge inverter, due to its main inductor and the required voltage and current measurement sensors. The additional two MOSFETs increase the cost factor of each submodule and also need their own control unit.

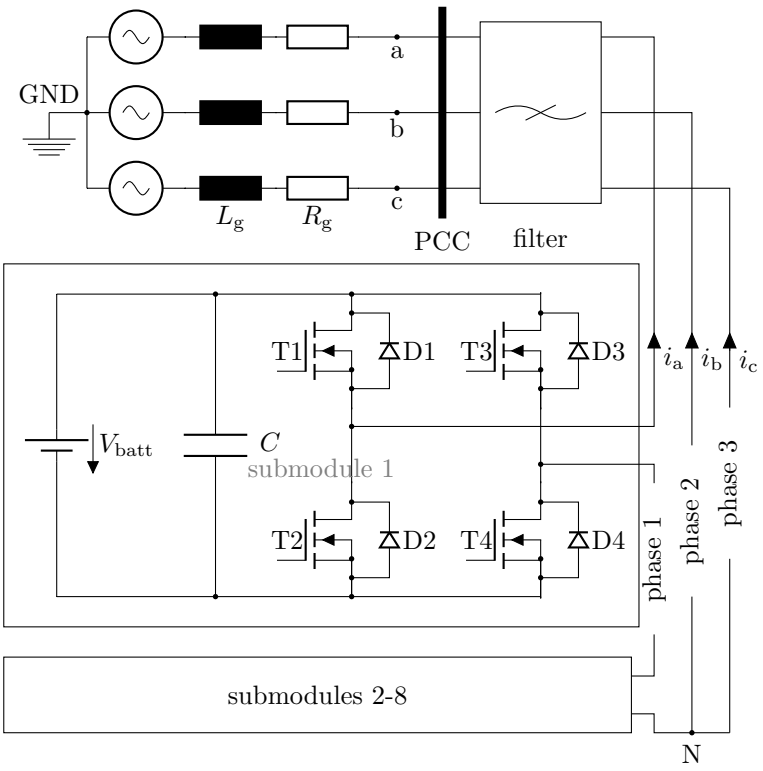


Figure 5.1 – Circuit of the one-stage CHB inverter topology [100].

To minimally size the inductor used in the DC-DC converters, high switching frequencies (higher than 50 kHz) are used. However, possible electromagnetic interference (EMI) problems may appear. In [110], the EMI is divided into two main parts. One part is the power caused EMI which is usually avoided using filters. The second part, the radiating/emitting EMI, is filtered using shielded power connection. This negatively affects the system complexity.
In the following sections, the two possible two-stage topologies using step-up and step-down DC-DC converter are presented and their specific advantages and disadvantages are discussed. Their operation and control are shown and the hardware implementation is discussed to finally select the recommended topology to be used in BESS.

5.2 One-Stage Topology using Cascaded H-Bridge Inverters

In the one-stage topology, the submodules contain one H-bridge inverter and one battery module as shown in Fig. 5.1.

5.2.1 Number of Voltage Levels

The number of required submodules for the one-stage topology is designed using the worst case scenario. To calculate the number of submodules, the AC grid voltage peak value $\hat{V}_a$ is divided by the minimum battery voltage $V_{batt,min}$, so that the inverter is still able to charge and

discharge the BESS at full battery operation voltage range. The ±10 % grid voltage tolerance is neglected. The minimal number of submodules is calculated using Eq. (5.1) [100].

$$\frac{\hat{V}_\mathrm{a}}{V_\mathrm{batt,min}} = \frac{\sqrt{2}\cdot 230\,\mathrm{V}}{44.6\,\mathrm{V}} = 7.3 < n_\mathrm{submodule} = 8 \tag{5.1}$$

The number of levels is an integer number and must be higher than 7.3. Therefore, each phase consists of eight series-connected submodules in the one-stage topology. Using eight submodules, the batteries can theoretically be discharged until 40.5 V if the voltage drop on the power filter is neglected.
In CHB inverters, it is possible to use more cascaded submodules than required. The energy content of the storage increases and the BESS is more fault tolerant.
By using the minimal number of submodules, the output voltage of the three-phase one-stage CHB inverter based BESS contains 17-levels, since it uses in each phase eight submodules connected in series as shown in Fig. 5.1.

5.2.2 Operation of One-Stage CHB Inverter

The one-stage CHB inverter topology and its operation and control are presented in [100].
During the CHB inverter operation, the number of the output voltage levels depends on the battery modules' *SoC*. Fig. 5.2 represents the number of the required inverter output voltage level when the batteries are fully charged, at their nominal voltage, and when the batteries are fully discharged.
The inverter is still able to charge the batteries using six submodules at $V_\mathrm{batt,max}$. In this case, the inverter voltage only has 13-levels. The charging operation is theoretically possible, whenever the AC peak voltage is higher than one DC-link voltage.
At a battery voltage of $V_\mathrm{batt,nom} = 51.2\,\mathrm{V}$, the CHB inverter output voltage consists of 15-levels to keep the grid current at zero, to charge or to discharge the battery modules.
At $V_\mathrm{batt,min}$, the inverter is able to discharge the BESS using all eight submodules using 17-level output voltage.
There is no extra unit required to control the number of the inverter's output voltage levels. The controller increases the duty cycle given to the modulator until reaching the desired inverter voltage. Thereby, the BMS and EMS are monitoring the battery voltages and the energy content of the BESS to avoid any overcharging or deep discharging.

5.3 Two-Stage Topology using additional Step-Up DC-DC Converter

The two-stage CHB inverter uses bidirectional step-up DC-DC converters for both charging and discharging operation modes. They maintain the DC-link voltage constant at 60 V or any other reference DC voltage. It also allows using batteries with different nominal voltages or currents as a degree of freedom. Assuming a symmetrical grid voltage, the three inverter phases need to generate the three-phase currents with the fundamental grid frequency. In order to overcome the DC-link current waveform found in the one-stage topology, the two-stage topology using DC-DC converters to connect the batteries to the H-bridge inverters' DC-links is proposed in [51] [170] [174]. For DC-link current ripple cancellation, a dual active bridge

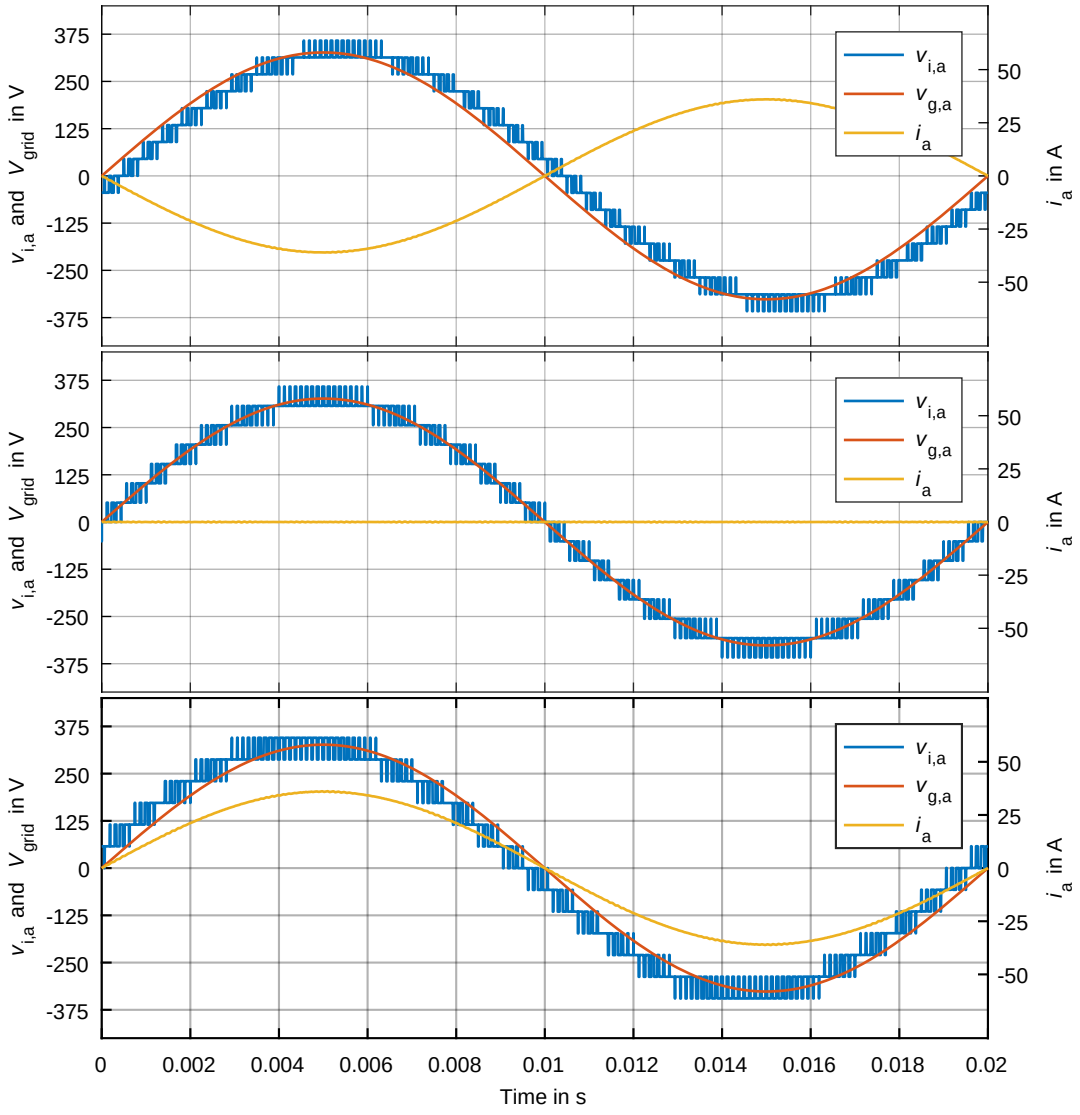


Figure 5.2 – One-stage CHB inverter and grid voltages and current at different battery voltages. The CHB inverter requires 17 levels at $V_{\mathrm{batt,min}}$ while discharging the BESS (top). It requires 15 levels at $V_{\mathrm{batt,nom}}$ to keep the grid current at zero (middle) and 13 voltage levels at $V_{\mathrm{batt,max}}$ while charging the BESS (bottom). [100].

derived galvanic isolation is used in a CHB multilevel topology for automotive applications [51]. This topology uses medium frequency transformer to provide galvanic isolation between the batteries and the H-bridge inverters and therefore eliminates the DC-link current oscillations. However, this addition leads to increased costs and additional submodule weight.
In [170], a CHB multilevel inverter with bidirectional DC-DC converters for energy storage is presented. The used structure solves the disadvantages of the one-stage topology such as the DC-link current oscillation and the resulting DC voltage fluctuation. The proposed system is based on a resonant controller to control the average DC-link voltage for each phase independently. However, the DC-link voltage is still suffering from fluctuations.
In [174], balancing control actions for CHB inverters with integrated battery energy storage using a non-isolated DC-DC stage in between the split storage elements and the H-bridge inverter are presented. The inherent second-order DC-link current harmonic in either star and delta configuration has been eliminated. The module voltage still contains the fluctuations in star case. This voltage fluctuation is studied in the following and eliminated.

5.3.1 Number of Voltage Levels

In Fig. 5.3, each submodule contains a bidirectional half-bridge DC-DC converter for maintaining the DC-link voltage constant at all batteries' SoC. Using DC-DC converters between the storage and the H-bridge inverter enables a full control on the batteries charge or discharge currents independently from the grid current by changing the DC-link voltage as explained before. The number of required submodules in the two-stage topology depends on the DC-Link voltage of each submodule V_{DC} and is calculated as in Eq. (5.2). Using a DC-link voltage under the extra low voltage limit standards of 60 V, reduces the number of submodules as shown in Eq. (5.2) to only six submodules in each phase. The SoC dependent battery voltage variation between 44.6 V and 57 V is eliminated and the DC-link voltage is kept constant. Therefore, the CHB inverter operates in the two-stage topology with 13-levels in its output voltage.

$$\frac{\hat{V}_{\mathrm{a}}}{V_{\mathrm{DC}}} = \frac{\sqrt{2} \cdot 230\,\mathrm{V}}{60\,\mathrm{V}} = 5.4 < n_{\mathrm{submodules}} = 6 \tag{5.2}$$

The operation and control of the submodules' step-up DC-DC converter is shown in the next section. The control for the step-down converter is made in a similar way.

5.3.2 Advantages and Disadvantages using Step-Up DC-DC Converter

The two-stage CHB inverter topology using bidirectional step-up DC-DC converters, as presented in Fig. 5.3, is studied. The control algorithm for its DC-DC converters eliminate the DC-link voltage fluctuation under all operation conditions as proposed in [107]. Using a variable DC-link voltage, the failure of one submodule could be overcome using a low number of submodules and higher DC-link voltages. However, to implement this, the voltage range of the power switches in the H-bridge inverter and DC-DC converter should be designed higher than needed, which decreases the submodule's efficiency. The control of the DC-DC converter and CHB inverter presented in this section is previously published in [107]. Furthermore, the fluctuation in the voltages using the two-stage topology is removed using a feed forward control strategy as proposed in [107].

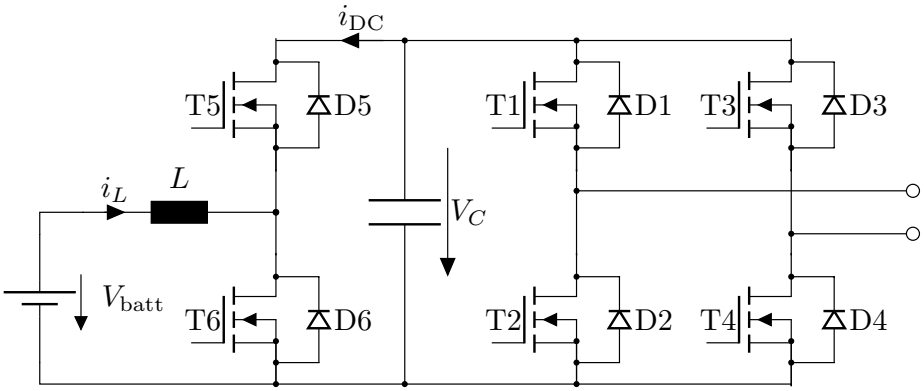


Figure 5.3 – Circuit of the two-stage CHB inverter's submodule including the bidirectional step-up DC-DC converter.

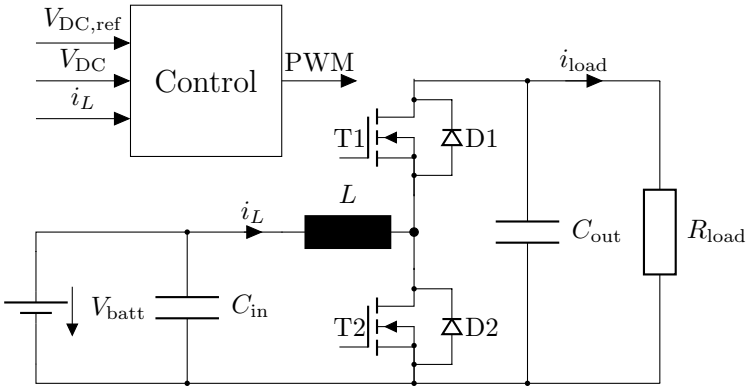


Figure 5.4 – Circuit of the used bidirectional step-up DC-DC converter between the H-bridge inverter and the battery modules in the CHB inverter.

5.3.3 DC-DC Converter's Parameter and Modeling

The circuit of the used DC-DC converter is shown in Fig. 5.4. Table 5.1 contains the parameter of the components used in considered step-up DC-DC converter. It has two possible operation states. Fig. 5.5 and Fig. 5.6 represent the final circuits when T1 and T2 are switched on, respectively.

The internal resistances of the inductance and capacitance are considered by modeling the DC-DC converter while applying Kirchhoff´s voltage law (KVL) and current law (KCL) for the circuit and are given in Eq. (5.3).

$$\begin{aligned} L \cdot \frac{\mathrm{d}i_L}{\mathrm{d}t} &= V_{\mathrm{batt}} - V_C - R_L \cdot I_L \\ C \cdot \frac{\mathrm{d}V_C}{\mathrm{d}t} &= I_L - \frac{V_C}{R_C} - i_{\mathrm{load}} \end{aligned} \tag{5.3}$$

Table 5.1 – Step-up DC-DC converter parameters.

Parameter	Nomenclature	Value
Input voltage range	V_{batt}	44.6 V–57 V
Output voltage	V_{out}	60 V
DC-DC converter switching frequency	$f_{\text{sw,DC}}$	50 kHz
Inductance	L	15 μH
inductance internal resistance	R_L	2.2 mΩ
Input capacitance	C_{in}	820 μF
Input capacitance internal resistance	$R_{C\text{in}}$	26 mΩ
Output capacitance	C_{out}	7.2 mF
Output capacitance internal resistance	$R_{C\text{out}}$	6.25 mΩ

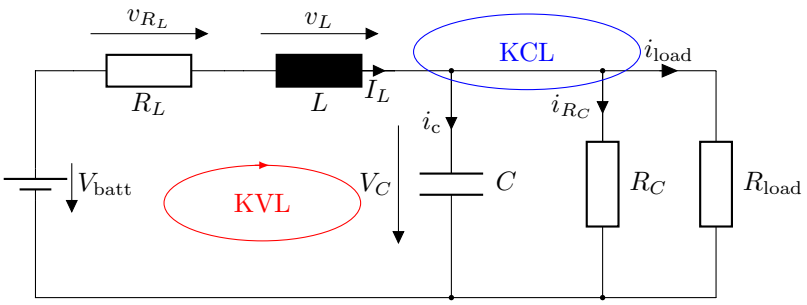


Figure 5.5 – Equivalent circuit of the step-up DC-DC converter: T1 ON and T2 OFF.

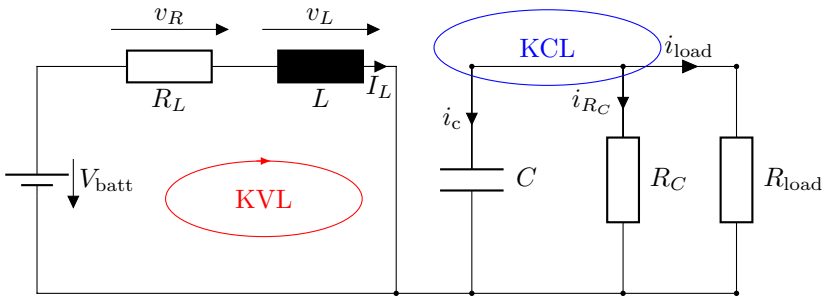


Figure 5.6 – Equivalent circuit of the step-up DC-DC converter: T1 OFF and T2 ON.

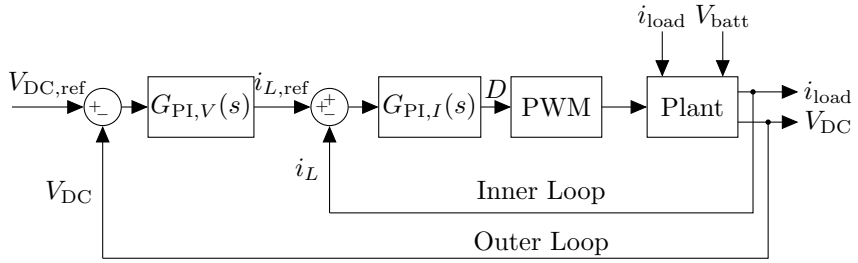


Figure 5.7 – General cascaded control structure of step-up DC-DC converters [10] [107].

In the second state as in Fig. 5.6, KVL and KCL results to Eq. (5.4).

$$\begin{aligned} L \cdot \frac{\mathrm{d}i_L}{\mathrm{d}t} &= V_{\text{batt}} - R_L \cdot I_L \\ C \cdot \frac{\mathrm{d}V_C}{\mathrm{d}t} &= -\frac{V_C}{R_C} - i_{\text{load}} \end{aligned} \tag{5.4}$$

In the normal operation of a half-bridge, the power switches T1 and T2 are operating complementarily. Therefore, Eq. (5.3) and (5.4) can be summarized to Eq. (5.5), where S_w is the switching control signal and has the value 1 or 0 [10].

$$\begin{aligned} L \cdot \frac{\mathrm{d}i_L}{\mathrm{d}t} &= V_{\text{batt}} - S_w \cdot V_C - R_L \cdot I_L \\ C \cdot \frac{\mathrm{d}V_C}{\mathrm{d}t} &= S_w \cdot I_L - \frac{V_C}{R_C} - i_{\text{load}} \end{aligned} \tag{5.5}$$

Operating the DC-DC converter in current continuous-conduction mode allows a bidirectional current flow. Therefore, the control signal S_w is replaced by the duty cycle D and its complementary $1 - D$ [10]. Eq. (5.3) can be written as Eq. (5.6).

$$\begin{aligned} L \cdot \frac{\mathrm{d}i_L}{\mathrm{d}t} &= V_{\text{batt}} - D \cdot V_C - R_L \cdot I_L \\ C \cdot \frac{\mathrm{d}V_C}{\mathrm{d}t} &= D \cdot I_L - \frac{V_C}{R_C} - i_{\text{load}} \end{aligned} \tag{5.6}$$

Using the DC-DC converter model from Eq. (5.6) shows, that two state variables should be controlled. The inductor current I_L and the DC-link voltage V_{DC} can be controlled in a cascaded structure using PI controllers [10].

5.3.4 Plant Identification

Fig. 5.7 represents the cascaded control structure of the DC-DC converter. The outer loop controls the DC-link voltage V_{DC} to be equal to the reference value $V_{\text{DC,ref}}$ using a PI controller $G_{\text{PI},V}(s)$. The inner loop is used to control the inductor current I_L to follow the reference value $i_{L\text{ref}}$ using the PI controller $G_{\text{PI},I}(s)$ [10]. In steady state, Eq. (5.6) can be linearized with the following steady state $(, \infty)$ assumptions in Eq. (5.7).

$$\begin{aligned} V_C &= V_{C,\infty} \\ I_L &= i_{L,\infty} \\ D &= D_{,}\infty \\ i_{\text{load}} &= i_{\text{load},\infty} \end{aligned} \tag{5.7}$$

and written as Eq. (5.8).

$$L \cdot \Delta i_L = V_{\text{batt}} - V_{C,\infty} \cdot \Delta D - R_L \cdot \Delta I_L \tag{5.8}$$

Eq. (5.9) represents the transfer function of the inner loop control. It is a first order delay and is calculated from Eq. (5.8).

$$G_{\text{plant,inner}}(s) = \frac{\Delta I_L(s)}{\Delta D(s)} = \frac{\frac{-V_{C,\text{ref}}}{R_L}}{1 + s\frac{L}{R_L}} \tag{5.9}$$

The dynamic of the inner control loop is higher than the outer control loop. From the perspective of the outer loop, the change of the inductor current ΔI_L is equal to zero [10], [84], [135]. The duty cycle D can be calculated from Eq. (5.6) (when neglecting the inductor power losses by setting $R_L = 0$) as shown in Eq. (5.10). The DC-DC converter generates output voltages greater than or equal to the battery voltage [125].

$$D = \frac{V_{\text{batt}}}{V_C} \tag{5.10}$$

Inserting Eq. (5.10) into Eq. (5.6) gives Eq. (5.11). After a multiplication by V_{DC} results to Eq. (5.12).

$$C \cdot \frac{\mathrm{d}V_C}{\mathrm{d}t} = \frac{V_{\text{batt}}}{V_C} \cdot I_L - \frac{V_C}{R_C} - i_{\text{load}} \tag{5.11}$$

$$C \cdot V_C \cdot \frac{\mathrm{d}V_C}{\mathrm{d}t} = V_{\text{batt}} \cdot I_L - \frac{V_C^2}{R_C} - i_{\text{load}} \cdot V_C \tag{5.12}$$

Linearizing Eq. (5.12) around the operating point leads to Eq. (5.13).

$$C \cdot V_{C,\infty} \cdot \Delta V_C = V_{\text{batt}} \cdot \Delta I_L - \frac{2 \cdot V_{C,\infty} \cdot \Delta V_C}{R_C} - i_{\text{load},\infty} \cdot \Delta V_C - V_{C,\infty} \cdot \Delta i_{\text{load}} \tag{5.13}$$

The output voltage transfer function, as a function of the inductor current I_L (controlled value) and the load current i_{load} (disturbance), can be calculated using Laplace transformation as in Eq. (5.14).

$$\Delta V_C = \left(\frac{V_{\text{batt}}}{CV_{C,\infty}s + \frac{2V_{C,\infty}}{R_C} + i_{\text{load},\infty}} \right) \Delta I_L - \left(\frac{V_{C,\infty}}{CV_{C,\infty}s + \frac{2V_{C,\infty}}{R_C} + i_{\text{load},\infty}} \right) \Delta i_{\text{load}} \tag{5.14}$$

Dividing Eq. (5.14) by the steady state load current $i_{\text{load},\infty}$ gives Eq. (5.15):

$$\Delta V_C = \left(\frac{V_{\text{batt}}}{i_{\text{load},\infty}} \cdot \frac{1}{\frac{CV_{C,\infty}}{i_{\text{load},\infty}}s + \frac{\frac{2V_{C,\infty}}{i_{\text{load},\infty}}}{R_C} + 1} \right) \Delta I_L - \left(\frac{V_{C,\infty}}{i_{\text{load},\infty}} \cdot \frac{1}{\frac{CV_{C,\infty}}{i_{\text{load},\infty}}s + \frac{\frac{2V_{C,\infty}}{i_{\text{load},\infty}}}{R_C} + 1} \right) \Delta i_{\text{load}} \tag{5.15}$$

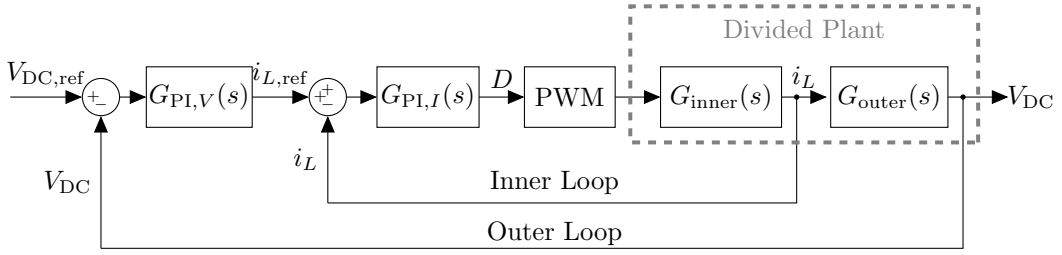


Figure 5.8 – Detailed cascaded control structure of the step-up DC-DC converter.

Assuming higher value of the capacitor's internal resistance R_C, the term $\frac{\frac{2V_{C,\infty}}{i_{\mathrm{load},\infty}}}{R_C}$ can be neglected. Therefore, Eq. (5.15) can be simplified to Eq. (5.16).

$$\Delta V_C = \left(\frac{V_{\mathrm{batt}}}{i_{\mathrm{load},\infty}} \cdot \frac{1}{\frac{CV_{C,\infty}}{i_{\mathrm{load},\infty}} s + 1} \right) \Delta I_L - \left(\frac{V_{C,\infty}}{i_{\mathrm{load},\infty}} \cdot \frac{1}{\frac{CV_{C,\infty}}{i_{\mathrm{load},\infty}} s + 1} \right) \Delta i_{\mathrm{load}} \tag{5.16}$$

The inductor current transfer function I_L to the capacitor voltage V_{DC} can be determined from Eq. (5.15) by neglecting the effect of the load current i_{load} ($\Delta i_{\mathrm{load}} = 0$) as in Eq. (5.17).

$$G_{\mathrm{plant,outer}}(s) = \frac{\Delta V_C(s)}{\Delta I_L(s)} = \frac{\frac{V_{\mathrm{batt}}}{i_{\mathrm{load},\infty}}}{1 + s\frac{CV_{C,\infty}}{i_{\mathrm{load},\infty}}} \tag{5.17}$$

5.3.5 Controller Design

After defining the transfer function of the DC-DC converter, the cascaded control loop shown in Fig. 5.8 is concluded. To control the inductor current I_L, the inner current control loop is based on a PI controller, as in Eq. (5.18).

$$G_{\mathrm{PI},I}(s) = K_{\mathrm{p},I} \left(1 + \frac{1}{sT_{\mathrm{i},I}} \right) \tag{5.18}$$

The transfer functions of the DC-DC converter and its controller are defined. The transfer function of the closed inner loop $G_{cl,inner}(s)$ is therefore derived as in Eq. (5.19).

$$G_{cl,inner}(s) = \frac{T_{\mathrm{i},I} s + 1}{\frac{T_{\mathrm{i},I} T_I}{K_{\mathrm{p},I} K_I} s^2 + T_{\mathrm{i},I} \left(1 + \frac{1}{K_{\mathrm{p},I} K_I} \right) s + 1} \tag{5.19}$$

Usually the inner control loop's response time is at least set five times faster or more than the outer control loop. For improved system dynamic, the selected value of the bandwidth of the inner control loop is chosen ten times smaller than the bandwidth of the outer control loop ($T_{0,I} = T_{0,V}/10$), as shown in Table 5.2. The inner closed control loop dynamic is described by a bandwidth of $1/T_{0,I}$ and a damping factor $\zeta_{0,I}$. The outer control loop is described by

Table 5.2 – Bandwidth and damping coefficient.

Parameter	Nomenclature	Value
Bandwidth of the voltage control loop	$T_{0,V}$	1 ms
Damping factor for voltage loop	$\zeta_{0,V}$	0.9
Bandwidth of the voltage control loop	$T_{0,I}$	0.1 ms
Damping factor for current loop	$\zeta_{0,I}$	0.9

the bandwidth $1/T_{0,V}$ and the damping factor $\zeta_{0,V}$ with $10 \cdot T_{0,I} \geq T_{0,V}$.
The proportional part of inner loop PI current controller $K_{\mathrm{p},I}$ is calculated using T_I, K_I, $\zeta_{0,I}$, and $T_{0,I}$ as shown in Eq. (5.20). Thereby is $K_I = \frac{-V_{C,\mathrm{ref}}}{R_L}$ and $T_I = \frac{L}{R_L}$.

$$K_{\mathrm{p},I} = \frac{T_I}{K_I T_{0,I}^2} \left(2\zeta_{0,I} T_{0,I} - \frac{T_{0,I}^2}{T_I} \right) \tag{5.20}$$

The integral part of the inner loop PI current controller $T_{\mathrm{i},I}$ is calculated using $\zeta_{0,I}$, $T_{0,I}$, and T_I as shown in Eq. (5.21).

$$T_{\mathrm{i},I} = 2\zeta_{0,I} T_{0,I} - \frac{T_{0,I}^2}{T_I} \tag{5.21}$$

For the outer control loop, the PI controller transfer function, as in Eq. (5.22), is similar to Eq. (5.18), but uses different index.

$$G_{\mathrm{PI},V}(s) = K_{\mathrm{p},V} \cdot \left(1 + \frac{1}{T_{\mathrm{i},V} s} \right) \tag{5.22}$$

In a similar way to the inner control loop, the outer loop PI controller parameters are calculated in Eq. (5.23).

$$\begin{aligned} K_{\mathrm{p},V} &= \frac{T_V}{K_V T_{0,V}^2} \left(2\zeta_{0,V} T_{0,V} - \frac{T_{0,V}^2}{T_V} \right) \\ T_{\mathrm{i},V} &= 2\zeta_{0,V} T_{0,V} - \frac{T_{0,V}^2}{T_V} \end{aligned} \tag{5.23}$$

Fig. 5.9 summarizes the circuit topology of the step-up DC-DC converter with cascaded control structure. Using the steady state values of the DC-DC converter ($V_{\mathrm{batt}} = 51.2\,\mathrm{V}, i,\infty = 36\,\mathrm{A}, V_{C,\infty} = 60\,\mathrm{V}$), the PI controller parameters of the inner and outer loop are calculated and summarized in Table 5.3. The simulation results, using the calculated parameters, are shown in the following.

5.3.6 Simulation Results without Feed-Forward Control

To validate the control of the DC-DC converter, it is connected to a linear load to operate at nominal load. Fig. 5.10 represents the corresponding results. To test the step response of the control system, the reference voltage is changed from 60 V to 65 V at $t =$ 15 ms and from 65 V back to 60 V at $t = 40$ ms. The results are satisfying and the controller succeeded in tracking the reference DC voltage, when connected to a linear load.

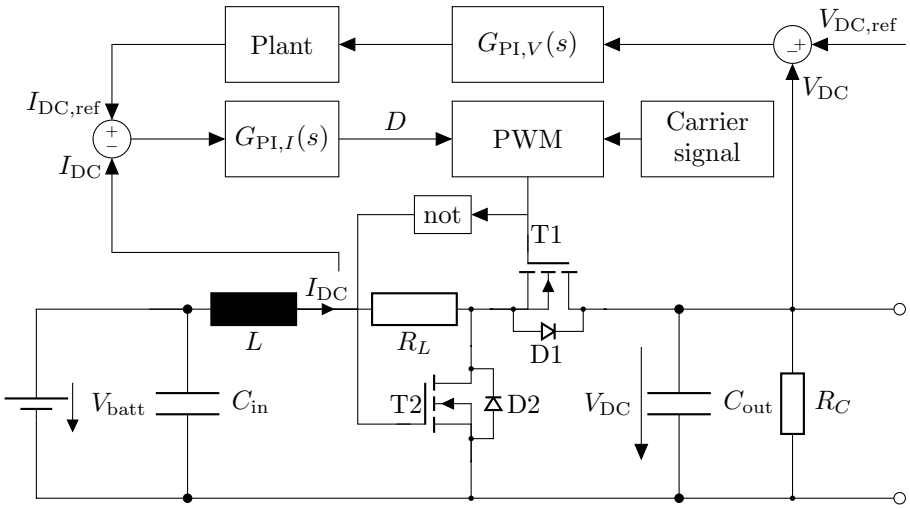


Figure 5.9 – Bidirectional step-up DC-DC converter with cascaded control structure [10].

Table 5.3 – DC-DC converter controller parameters.

Parameter	Nomenclature	Value
Proportional gain of the voltage regulator	$K_{\mathrm{p},V}$	13.3
Time constant of the outer loop	$T_{\mathrm{i},V}$	1.7 ms
Integral gain of the voltage regulator	$K_{\mathrm{i},V}$	7872
Proportional gain of the current regulator	$K_{\mathrm{p},I}$	-0.0045
Time constant of the inner loop	$T_{\mathrm{i},I}$	0.18 ms
Integral gain of the current regulator	$K_{\mathrm{i},I}$	-25

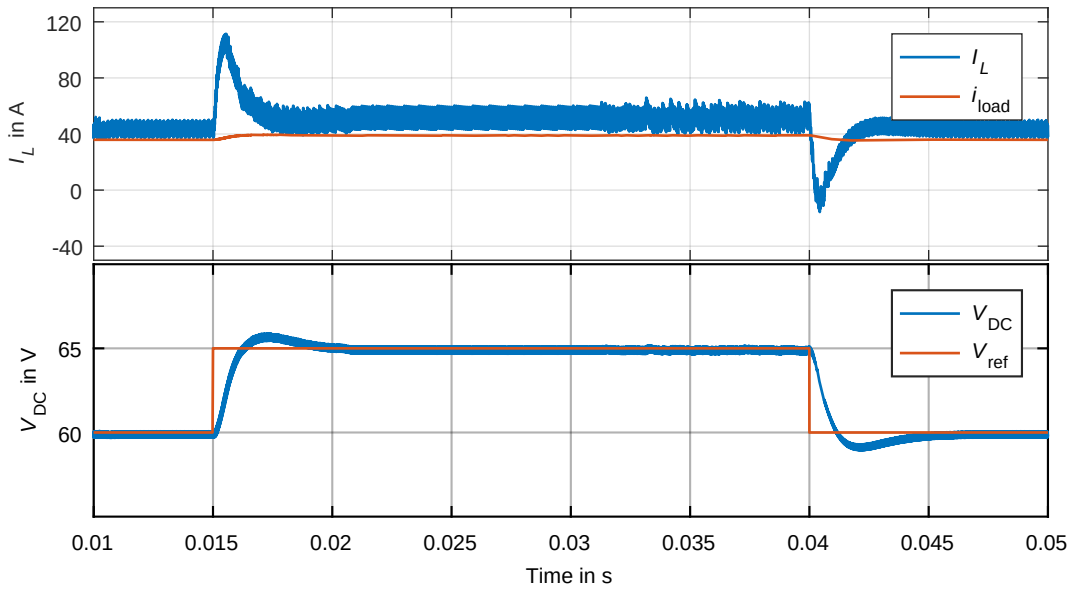


Figure 5.10 – Step-up DC-DC converter's inductor current I_L and DC-link voltage V_{DC} in case of linear load without feed-forward control [107].

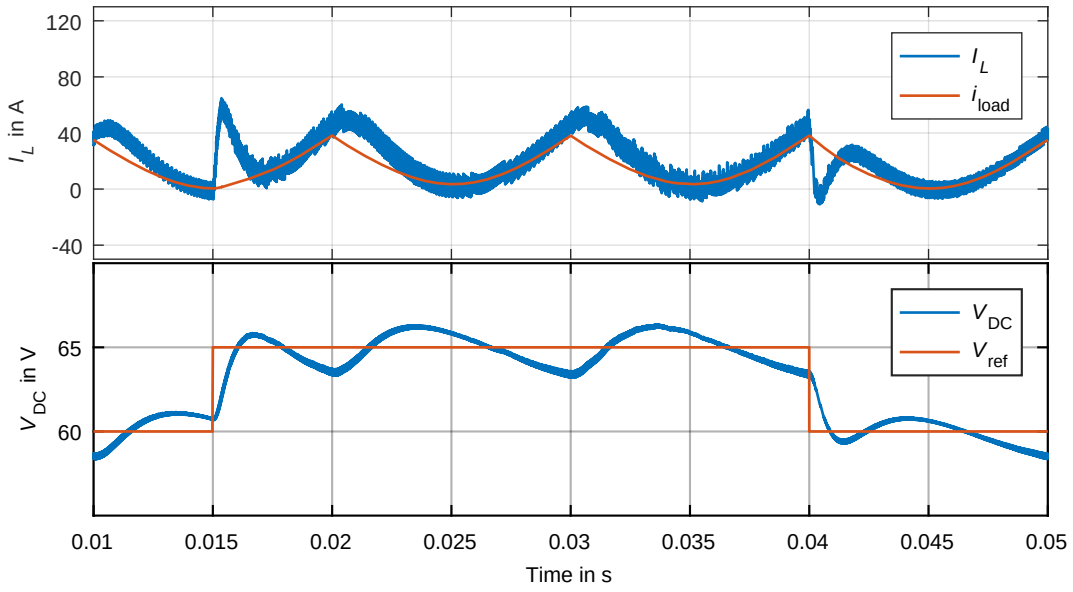


Figure 5.11 – Step-up DC-DC converter's inductor current I_L and DC-link voltage V_{DC} in case of non-linear load without feed-forward control [107].

In the two-stage topology, the DC-DC converter is connected between the battery module and the DC-side of the H-Bridge inverter. It operates with an AC current at its output which leads to DC-link voltage fluctuating around the reference voltage. Therefore, the DC-DC converter control system is not suitable for tracking the reference value exactly in this case. The DC-DC converter operation by connection to the non-linear load is presented in Fig. 5.11. To eliminate those fluctuations, a proposed control system for the DC-DC converter using feed forward control is presented in the next section for a suitable converter operation with non-linear load [107].

5.3.7 Simulation Results using Feed-Forward Control

In the two-stage CHB multilevel inverter, DC-DC converters are connected to the H-bridge inverters which represent a non-linear load. Therefore, as shown previously, the DC-link voltage is influenced by fluctuations with double of the nominal current frequency. These fluctuations also affect the DC capacitors lifetime and influence the power quality of the CHB inverter output voltage and current. Therefore, the feed-forward control is used to suppress this fluctuation by considering the effect of the load current on the DC-link voltage, which is illustrated in Eq. (5.17). The transfer function, or the quotient of the DC-link voltage and the load current, is written in Eq. (5.24). To consider this, the block diagram of the detailed cascaded control structure, using feed forward control, is modified by including the effect of the disturbance i_{load}, as shown in Fig. 5.12.

$$G_{\mathrm{CFF}}(s) = \frac{\Delta V_C}{\Delta i_{\mathrm{load}}} = \frac{\frac{-V_{C,\infty}}{i_{\mathrm{load},\infty}}}{\frac{C \cdot V_{C,\infty}}{i_{\mathrm{load},\infty}} s + 1} \tag{5.24}$$

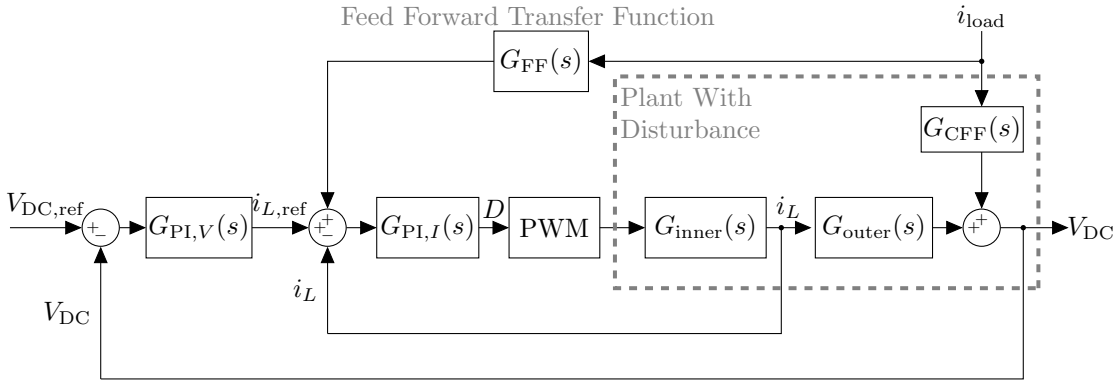


Figure 5.12 – Detailed cascaded control structure using feed forward control and considering the plant with disturbance [107].

The compensation of the disturbance effect, using a feed-forward control, is generated as in [135] in Eq. (5.25) and Eq. (5.26).

$$\Delta V_C(s) = G_{\text{CFF}}(s) \cdot \Delta i_{\text{load}} + G_{\text{plant,outer}}(s)(\Delta I_L + G_{\text{FF}}(s) \cdot \Delta i_{\text{load}}) \tag{5.25}$$

$$\Delta V_C(s) = G_{\text{plant,outer}}(s) \cdot \Delta I_L + \Delta i_{\text{load}}(G_{\text{plant,outer}}(s) \cdot G_{\text{FF}}(s) + G_{\text{CFF}}(s)) \tag{5.26}$$

For the absolute value functions to compensate each other, the condition in Eq. (5.27) should be valid. It reflects the value of added current to the reference value of the inductor current to counterbalance the disturbance as presented in Fig. 5.12.

$$G_{\text{plant,outer}}(s) \cdot G_{\text{FF}}(s) + G_{\text{CFF}}(s) \stackrel{!}{=} 0 \tag{5.27}$$

The load current i_{load} is multiplied with the transfer function G_{FF} and summed with the difference of reference and actual inductor current $\Delta I_L = i_{L,\text{ref}} - I_L$ considering Eq. (5.28). Thereby the controller calculates the additional current value, which should be driven through the inductor L to keep the output DC-link voltage constant.

$$G_{\text{FF}}(s) = \frac{\Delta I_L}{\Delta i_{\text{load}}} = \frac{-G_{\text{CFF}}(s)}{G_{\text{plant,outer}}(s)} \tag{5.28}$$

Fig. 5.13 shows the simulation results of the step-up DC-DC converter in case of a non-linear load by using the feed-forward control. The DC-link voltage is constant and does not fluctuate even if the current oscillates due to the use of an H-bridge inverter at the DC-DC converter output. The proposed control eliminates the fluctuations on the DC-link voltage of the H-bridge inverter and of the DC-DC converter output.

5.3.8 Operation using Step-Up DC-DC Converter

The CHB inverter operation is shown in Fig. 5.14. The inverter operates at all operation points using 13 voltage levels. The inverter can charge, and discharge the battery submodules using only six submodules in each phase. The DC-link voltage of each submodule is set to 60 V and is in the limit for ELV voltage. However, it is possible to higher boost the voltage e.g. in case of one submodule failure. This requires higher voltage range of the used power semiconductors and the passive elements must be designed for this possible operation.

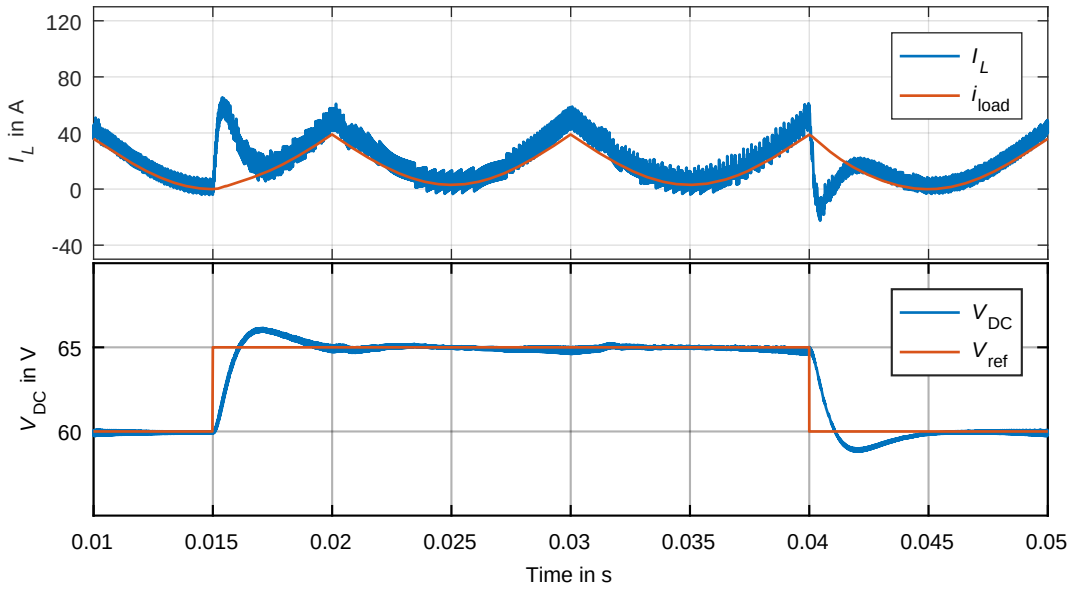


Figure 5.13 – Step-up DC-DC converter's inductor current I_L and DC-link voltage V_{DC} in case of non-linear load with the proposed feed-forward control [107].

Table 5.4 – Measured step-up DC-DC converter efficiency at different battery voltages.

Parameter	Nomenclature	Value
Maximal efficiency at maximal battery voltage	$\eta_{\mathrm{max},V_{\mathrm{batt,max}}}$	97.12 %
Maximal efficiency at nominal battery voltage	$\eta_{\mathrm{max},V_{\mathrm{batt,nom}}}$	97.01 %
Maximal efficiency at minimal battery voltage	$\eta_{\mathrm{max},V_{\mathrm{batt,min}}}$	96.95 %
Nominal efficiency at maximal battery voltage	$\eta_{\mathrm{nom},V_{\mathrm{batt,max}}}$	92.64 %
Nominal efficiency at nominal battery voltage	$\eta_{\mathrm{nom},V_{\mathrm{batt,nom}}}$	91.32 %
Nominal efficiency at minimal battery voltage	$\eta_{\mathrm{nom},V_{\mathrm{batt,min}}}$	91.10 %

5.3.9 Hardware Implementation and Efficiency

Furthermore, to analyze the efficiency of the DC-DC converter, a prototype is built and its efficiency is measured. The parameter related to the step-up DC-DC converter hardware are listed in Table 5.1. The maximal reached efficiency is up to 97.12 % and can be increased if interleaved DC-DC converter are used. However, this will lead to increased submodule's volume. At all three battery voltages ($V_{\mathrm{batt,min}}, V_{\mathrm{batt,nom}}, V_{\mathrm{batt,max}}$), the maximal efficiency is more than 96 %. At nominal operation point, the efficiency at maximum battery voltage is the smallest. The lowest efficiency of 91.10 % is reached at nominal operation point and minimal battery voltage. At this operation point, the round trip efficiency of the step-up DC-DC converter is 82.99 %. The measured efficiencies are listed in Table 5.4. The feed-forward control method for the 13-level inverter with step-up DC-DC converter in the submodules eliminates the DC-link voltage fluctuations during all the operation conditions [107]. The simulation results confirmed the ability of the proposed control to keep the DC-link voltage constant. In the next section, the usage of step-down DC-DC converter is integrated in the submodules of the CHB inverter and analyzed.

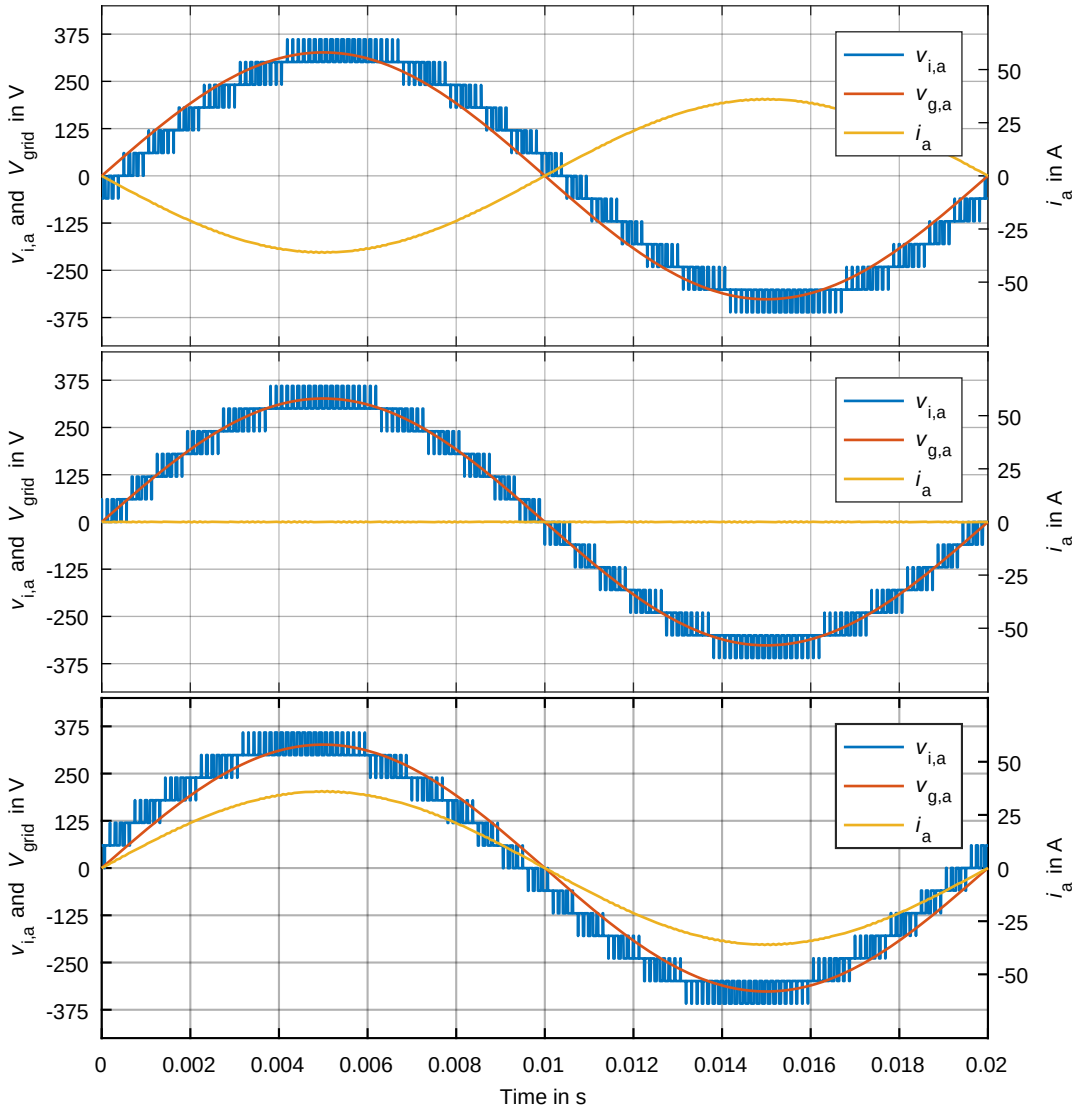


Figure 5.14 – Two-stage CHB inverter and grid voltages and current using the step-up DC-DC converter. The CHB inverter requires 13 voltage levels while charging and discharging the battery modules and when the phase current is set to zero.

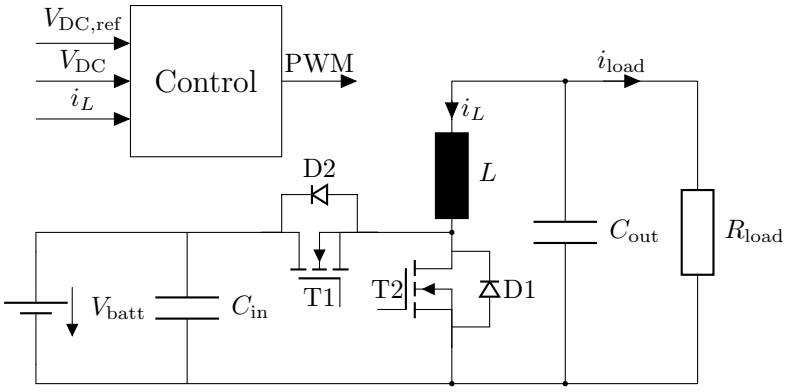


Figure 5.15 – Circuit of the used bidirectional step-down DC-DC converter between the H-bridge inverter and the battery modules in the CHB inverter.

5.4 Two-Stage Topology using additional Step-Down DC-DC Converter

The two-stage topology using step-down DC-DC converters works with the similar principle as discussed previously using step-up DC-DC converters. The circuit for this converter is presented in Fig. 5.15.

5.4.1 Advantages and Disadvantages using Step-Down DC-DC Converter

Using a step-down DC-DC converter in the two-stage topology allows more voltage level and therefore the grid effects are smaller than the one-stage and the two-stage using step-up DC-DC converter topologies. Using higher number of H-bridge inverters, the system fault tolerance increases.
The disadvantage of using the step-down DC-DC converter consists in the system efficiency, which is a general disadvantage while using the two-stage topology. Moreover, using additional components leads to increased system costs.

5.4.2 Number of Voltage Level

The step-down DC-DC converter delivers a lower voltage for the H-bridge inverter than the battery voltage. As example with the used battery modules, the chosen DC-DC converter voltage is set to 40 V. Therefore, the number of output voltage levels is increased as shown in Eq. (5.29) to 9 submodules in each phase instead of eight in Fig. 5.1. It offers the advantage to use lower voltage range power switches in the H-bridge inverters and offers also the possibility to deliver a CHB inverter voltage output with higher number of levels.

$$\frac{\hat{V}_{\mathrm{a}}}{V_{\mathrm{DC}}} = \frac{\sqrt{2} \cdot 230\,\mathrm{V}}{40\,\mathrm{V}} = 8.12 < n_{\mathrm{submodules}} = 9 \tag{5.29}$$

Table 5.5 – Step-down DC-DC converter parameters.

Parameter	Nomenclature	Value
Input voltage range	V_{batt}	44.6 V – 57 V
Output voltage	V_{out}	40 V
DC-DC converter switching frequency	$f_{\text{sw,DC}}$	50 kHz
Inductance	L	16.5 μH
Inductance internal resistance	R_L	1.2 mΩ
Input capacitance	C_{in}	820 μF
Input capacitance internal resistance	$R_{C\text{in}}$	26 mΩ
Output capacitance	C_{out}	7.2 mF
Output capacitance internal resistance	$R_{C\text{out}}$	6.25 mΩ

5.4.3 Parameter and Control of the Step-Down DC-DC Converter

Table 5.5 shows the circuit's components parameters of the step-down DC-DC converter. The DC battery voltage variation between 44.6 V and 57 V is eliminated and the DC-link voltage is kept constant at 40 V. The control and operation described in the section 5.3 is similar for the step-down DC-DC converter. The feed forward control is also used in the operation. The control of the step-down DC-DC converter can be achieved in a similar way as previously shown using the step-up DC-DC converter and is not further discussed. However, the operation of the two-stage CHB inverter using step-down DC-DC converter is presented in the next section.

5.4.4 Operation using Step-Down DC-DC Converter

The CHB inverter operation is shown in Fig. 5.16. The inverter operates at all operation points using 17 voltage levels. The inverter can charge, and discharge the battery submodules using eight submodules in each phase. The DC-link voltage of each submodule is set to 40 V and is under the ELV voltage limit.

5.4.5 Hardware Implementation and Efficiency

Efficiency plays an important role while designing the CHB inverter to be used in BESS. Therefore, a hardware prototype of the presented step-down DC-DC converter is built and its efficiency is determined. The parameter related to the step-up DC-DC converter hardware are listed in Table 5.5. The hardware is used to measure the maximum reachable efficiency of this topology. Its efficiency at different operation points is measured. At all three battery voltages ($V_{\text{batt,min}}, V_{\text{batt,nom}}, V_{\text{batt,max}}$), the maximal efficiency is more than 97.98 %. The lowest reached efficiency at nominal operation point and maximum battery voltage is 90.64 %. At this operation point, the round trip efficiency of the step-down DC-DC converter is 82.16 %. The relevant efficiencies are shown in Table 5.6.

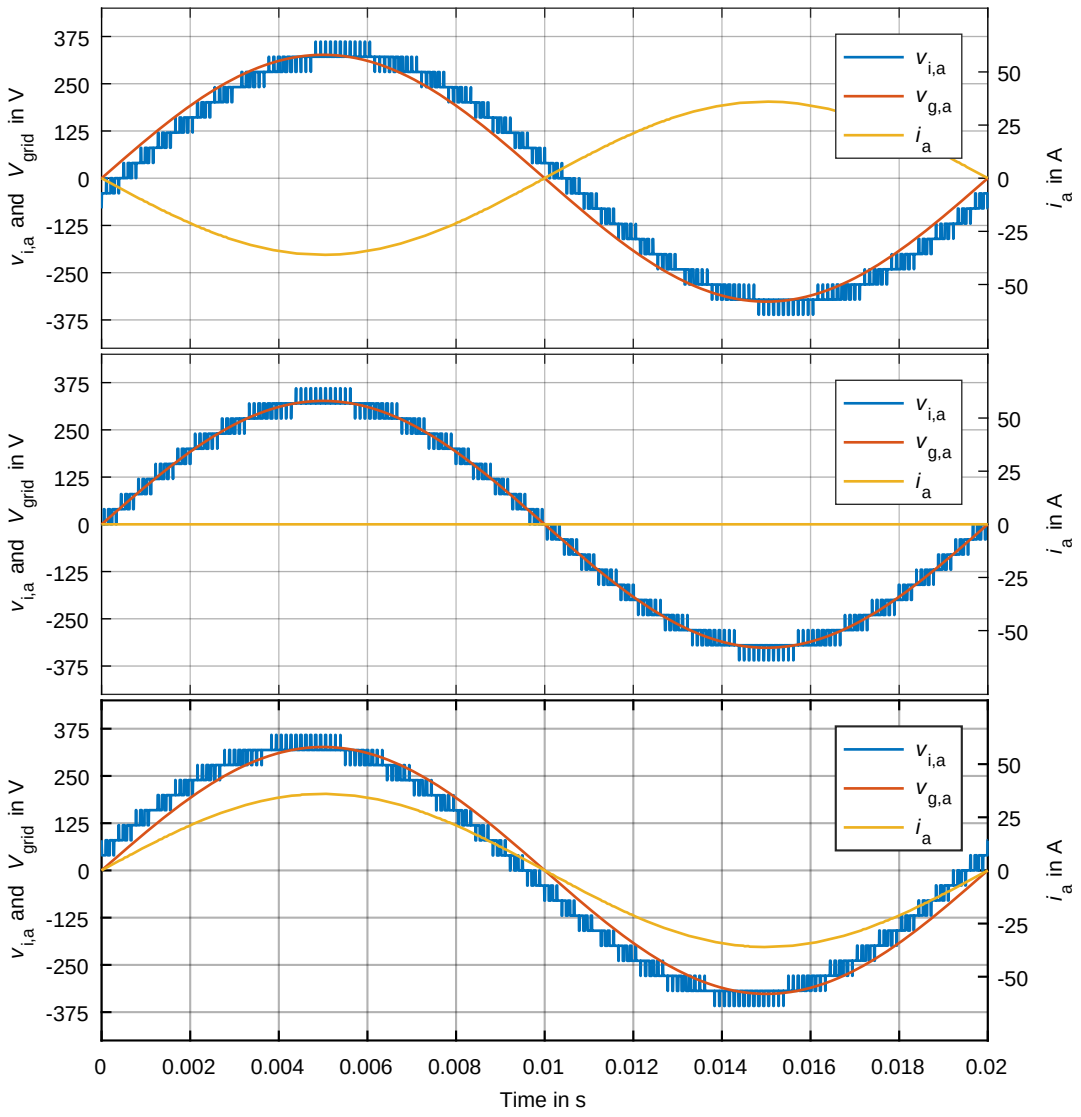


Figure 5.16 – Two-stage CHB inverter and grid voltages and current using step-down DC-DC converter. The CHB inverter requires 17 voltage levels while charging and discharging the battery modules and when the phase current is set to zero.

Table 5.6 – Measured step-down DC-DC converter efficiency at different battery voltages.

Parameter	Nomenclature	Value
Maximal efficiency at minimal battery voltage	$\eta_{\max,V_{\text{batt,min}}}$	97.98 %
Maximal efficiency at nominal battery voltage	$\eta_{\max,V_{\text{batt,nom}}}$	97.54 %
Maximal efficiency at maximal battery voltage	$\eta_{\max,V_{\text{batt,max}}}$	97.30 %
Nominal efficiency at minimal battery voltage	$\eta_{\text{nom},V_{\text{batt,min}}}$	94.29 %
Nominal efficiency at nominal battery voltage	$\eta_{\text{nom},V_{\text{batt,nom}}}$	92.73 %
Nominal efficiency at maximal battery voltage	$\eta_{\text{nom},V_{\text{batt,max}}}$	90.64 %

5.5 Selection of the Submodule's Topology

The CHB inverter consists of several submodules connected in series, which defines the inverter output voltage levels. The three possible circuits for the submodules are compared and the one-stage topology is selected. The one-stage CHB inverter topology offers advantages in terms of the lower number of components, which means higher CHB inverter efficiency, which plays an important role in BESS. The power electronic is used to charge and discharge the batteries, which highly influence the round-trip efficiency.
Without using DC-DC converters, the system complexity is lower and the additional EMI is removed. The failure safety from the additional DC-DC converter could be balanced in the one-stage topology by using additional submodules to keep the CHB inverter operating.
Considering the discussed one- and two-stage topologies, it is clear that the advantages of using step-up or step-down DC-DC converter are not big enough, and for an efficient system, the one-stage topology is more relevant. It offers similar submodules using similar battery modules and H-bridge inverters for higher efficient BESS, hence it is preferred and selected. The used CHB inverter topology shown in Fig. 5.1 with eight series connected submodules is further studied.
After the selection of the one-stage CHB inverter topology, the simulations are used to design and validate the inverter operation before starting with the hardware implementation. The required next steps and the inverter design methodology are done at multilevel abstraction and depth as presented in the next section. The physical modeling of CHB multilevel inverter on multilevel abstraction is introduced. The abstraction levels are the component-, circuit-, and system-level accompanied with hardware assessment.
The system simulation and modeling plays an important role during the design process. It saves time and allows a possible inverter component design. Due to the complexity of the multilevel inverter, the high number of components and the split battery modules, the simulation is necessary to design and validate the inverter operation. Only one inverter model is insufficient to simulate the power electronics of the BESS. Therefore, the simulation on multilevel abstraction is necessary and is divided into three levels by partially accompanied hardware assessments. The simulation part is divided in component-, circuit-, and system-level.
These simulation levels use different models of the inverter and are mutually dependent and mutually complementary during the design phase of the BESS. The difference to lower simulation levels is in the preciseness of modeling the BESS's components.
The inverter's efficiency is investigated on component-level and validated with hardware measurements. The simulation of the exact power semiconductors allows an exact prediction of the inverter efficiency as presented in the next section.

6 Inverter's Efficiency Using Physical Simulation on Component-Level with Hardware Assessment

To design a power inverter with higher complexity and number of components such as the selected one-stage CHB inverter, the system can be reduced to one H-bridge inverter. The main goal of this restriction is to study the inverter's efficiency as introduced in Section 6.1. The calculation of the power losses on component-level is introduced in Section 6.2. The submodule's losses are simulated on component-level and compared to hardware measurements in Section 6.3. The deepest simulation level, defined here as component-level, represents the power semiconductor dynamic model behavior and focuses on its efficiency. Therefore, it allows to define the power losses and delivers the efficiency curves during the inverter operation by modeling the power MOSFET's dynamic switching-on and -off as shown in Section 6.2. The results from simulations on component-level are validated with hardware using oscilloscope measurements of the switch-on and -off waveforms of the power semiconductor. Furthermore, a power analyzer is used to measure the H-bridge inverter efficiency at different operation points.
Finally, in addition to the power filter losses presented in Section 6.4, the whole CHB-inverter's efficiency is calculated and shown in Section 6.5.
This simulation level and the results presented in this chapter are previously published in [105] and [21].
After the inverter design on component-level, the results are transferred to the simulation on higher abstraction levels, such as circuit- and system-level in the following chapters.

6.1 Introduction to the Inverter's Design on Component-Level

To accelerate the development process of power inverters and shorten the design time, a physical simulation on component-level is introduced. It allows an elaboration of a real system using causal models with higher similarity to the measurement results. Using modern simulation software allows to exactly predict the losses in power switches during their operation. It allows to study the H-bridge inverter's thermal effects such as the design of its heat sinks. On component-level, the H-bridge inverter's efficiency prediction is achieved to be used in the selected one-stage CHB inverter topology. The inverter model is reduced to one of its submodule for efficiency analysis and only one H-bridge inverter is simulated as shown in Fig. 6.1.
The H-bridge inverter switching frequency is set to 1 kHz. Increasing this frequency decreases the H-bridge inverter efficiency as shown in [21].
The power MOSFET's dynamic switch-on and -off is used to find out the H-bridge inverter efficiency at different operation and load points, which represents the focus of simulations on

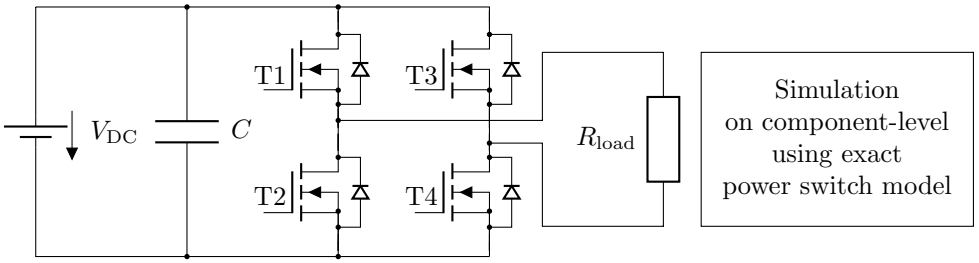


Figure 6.1 – Simulation on component-level using an exact H-bridge inverter's model [105]

component-level. Exact switching process modeling allows the exact calculation of all power losses simultaneously and permits the analysis of thermal effects. The required heat sink is designed and the PCB thickness and the power lines width are defined on component-level. The H-bridge inverter losses are defined and calculated using Shichman-Hodges physical models on component-level.
Furthermore, to get results close to the reality, parasitic elements are simulated on component-level. The total CHB inverter efficiency is defined as the sum of the power filter losses and the H-bridge inverter power losses. The batteries power losses are not addressed.

6.2 Power Losses Calculation on Component-Level

To describe the power dissipation in active power semiconductors, there are four categories presented as shown in [105].
A power switch operates in on- or off-state and therefore produces conduction and blocking losses respectively. Between both states, it produces switching losses. Furthermore, to change its state, controller losses occur, which are required to charge the power MOSFET's gate capacitance.
In the following blocking, controlling, conduction, and switching power loss categories are described and their calculation is presented.

6.2.1 Blocking Power Losses

When a power MOSFET is switched off, there is still a low leakage-current flowing in the blocking region when a drain-source voltage is applied (blocking state). However, the blocking losses are small and can be neglected. For a possible MOSFET in the studied power range, the blocking losses caused by a leaking-current of around 20 nA [70] and at 50 V are approximately 1000 nW.

6.2.2 Controlling Power Losses

The controlling losses result from the MOSFET's gate current and the losses that the DC-DC converters cause when providing supply energy for the driver and the logical circuits. At low

H-bridge inverter operation power, the controlling losses should not be neglected, because they are independent from the transmitted power.

6.2.3 Conduction Power Losses

The conduction losses are generated by the ohmic voltage drop on the drain-source resistance $R_{\mathrm{DS,on}}$ while the power MOSFET conducts current. $R_{\mathrm{DS,on}}$ depends on the power semiconductor temperature and the used gate-driver voltage. Assuming a constant $R_{\mathrm{DS,on}}$ over the used current range, the conduction losses P_{cond} are expressed as in Eq. (6.1). The conduction losses depend mainly on the semiconductor's inner resistance and temperature.

$$P_{\mathrm{cond}} = \frac{1}{T} \int_{t_1}^{t_1+T} R_{\mathrm{DS,on}} i^2(t) \cdot \tau(t) \mathrm{d}t \tag{6.1}$$

In Eq. (6.1), $i(t)$ is the periodical current with a period T and $\tau(t)$ is a function which is always equal to 1 when the MOSFET is in the conduction region, otherwise it is equal to 0. It usually correlates with the PWM signal which drives the power semiconductor and is controlled by the gate driver. Assuming a sinusoidal grid current, which normally flows through all submodules by certain modulation scheme, Eq. (6.1) is simplified as in [181] to Eq. (6.2).

$$P_{\mathrm{cond}} = 2 \cdot \frac{1}{T} \int_{t_1}^{t_1+T} R_{\mathrm{DS,on}} i^2(t) \mathrm{d}t \tag{6.2}$$

When inserting the current rms value I_{rms}, Eq. (6.2) can be further simplified to Eq. (6.3).

$$P_{\mathrm{cond}} = R_{\mathrm{DS,on}} \cdot I_{\mathrm{rms}}^2 \tag{6.3}$$

During the CHB inverter operation, the MOSFETs are always conducting and there is no current flowing in the free-wheeling diodes. Therefore, the diodes' losses are neglected. The two MOSFETs of each H-bridge inverter leg are switched complementary. Using eight submodules in each phase means that always 16 MOSFETs are conducting current while the other 16 are in blocking state. By considering the whole 17-level CHB inverter three-phases, 48 MOSFETs are permanently conducting current and all H-bridge inverters conduction losses are calculated as in Eq. (6.4).

$$P_{\mathrm{cond}_{24\ \mathrm{H-bridge\ inverters}}} = 2 \cdot n_{\mathrm{submodules}} \cdot R_{\mathrm{DS,on}} \cdot I_{\mathrm{rms}}^2 = 48 \cdot R_{\mathrm{DS,on}} \cdot I_{\mathrm{rms}}^2 \tag{6.4}$$

The device acts as a resistive load and produces conduction loses during the MOSFET turn on time. Fig. 6.2 draws the results by applying Eq. (6.1) on the CHB inverter line rms current. Where $I_{\mathrm{on}} = 36$ A is the peak current during the on state and $R_{\mathrm{DS,on}} = 2.3$ mΩ is the used MOSFET resistance [69].

6.2.4 Switching Power Losses

The H-bridge inverter switches DC voltage on and off. Whenever, during the transition times, the voltage and current are not equal to zero, as in Fig. 6.3, power dissipation occurs as in Eq. (6.5).

$$P = V \cdot I \tag{6.5}$$

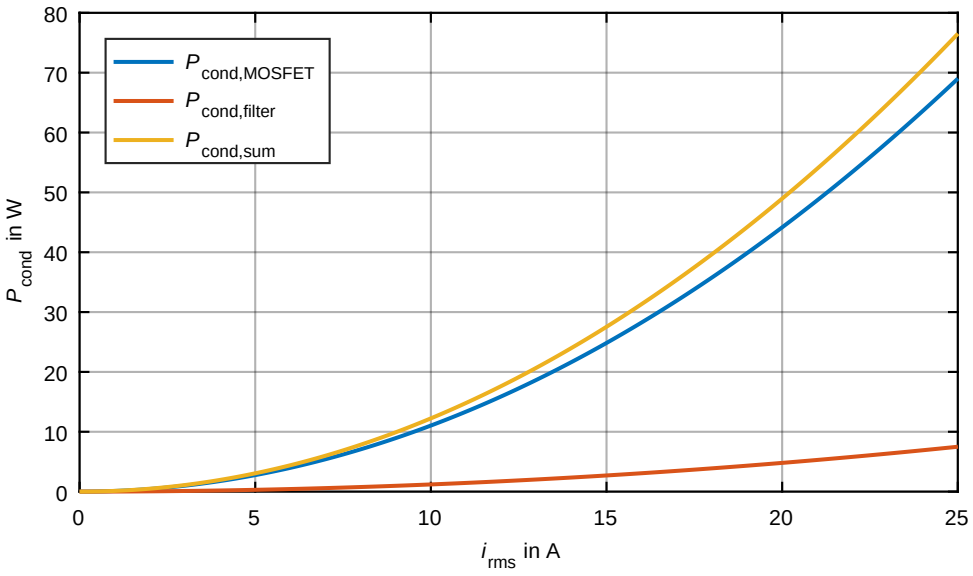


Figure 6.2 – Conduction power losses for the internal resistance of the power switches and the power filter depending on the current rms value.

The usage of a dynamic power switch model allows an exact prediction of the switches' operation under different conditions, since the conduction losses are easier to be defined. Fig 6.3 represents the power losses for simplified power semiconductor switching. It shows the idealized voltage and current curves for one MOSFET during the switch-on and -off time operations for one switching period T_{sw} from t_{on} to t_{off}. It shows a given time delay while the MOSFET changes its state for the current rising and the voltage decreasing. During this time, the multiplication of both signals gives the resulting switching power losses. During the switch-on time and off time conduction and blocking losses happen, respectively. In contrast to Fig. 6.3, the real MOSFET switch-on and -off, considering parasitic effects, looks different. Fig. 6.4 represents a realistic MOSFET drain-source voltage waveform during the switch-on time. Simulations on component-level are done using LTspice and Simscape physical model and are highly accurate to each other and to the hardware measurements. The parameter used in the MOSFET simulation model are obtained from its data-sheet. By comparing the MOSFET transient time, the switching process is well simulated and is close to the measured drain-source voltage during the switch-on time [105]. The shown overshoot could be used for snubber circuit design to protect the power semiconductors from possible damage due to over-voltage. The transition from the conduction to the blocking region and the other way round occurs with a given time delay as shown in Fig. 6.3. During this time, switching losses occur due to charging or discharging of the MOSFET's gate source capacitance. The integral of the current and voltage multiplication gives the lost switching energy E_{sw}. During one switching period T_{sw}, the switch-on energy losses $E_{\mathrm{sw,on}}$ and the switch-off energy losses $E_{\mathrm{sw,off}}$ occur. Thus the total switching energy losses per switching period are equal to E_{sw}. The switching power losses P_{sw} are calculated as a product of the switching frequency $f_{\mathrm{sw}} = \frac{1}{T_{\mathrm{sw}}}$ and the switching energy losses E_{sw} as represented in Eq. (6.6). The higher the switching currents and voltages, the higher the switching losses.

$$P_{\mathrm{sw}} = E_{\mathrm{sw}} \cdot f_{\mathrm{sw}} \tag{6.6}$$

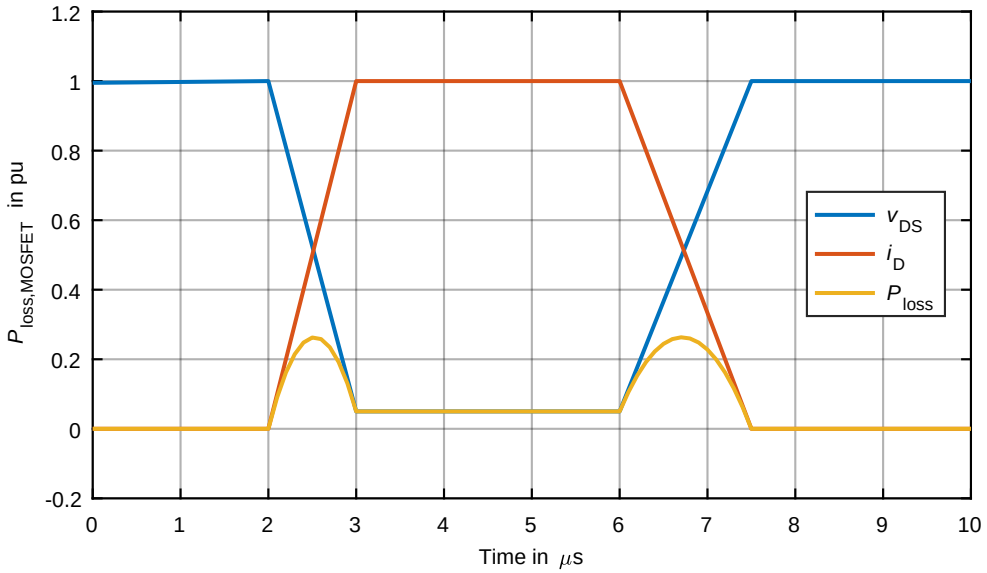


Figure 6.3 – Idealized power semiconductor dynamic switch-on and -off behaviors [105].

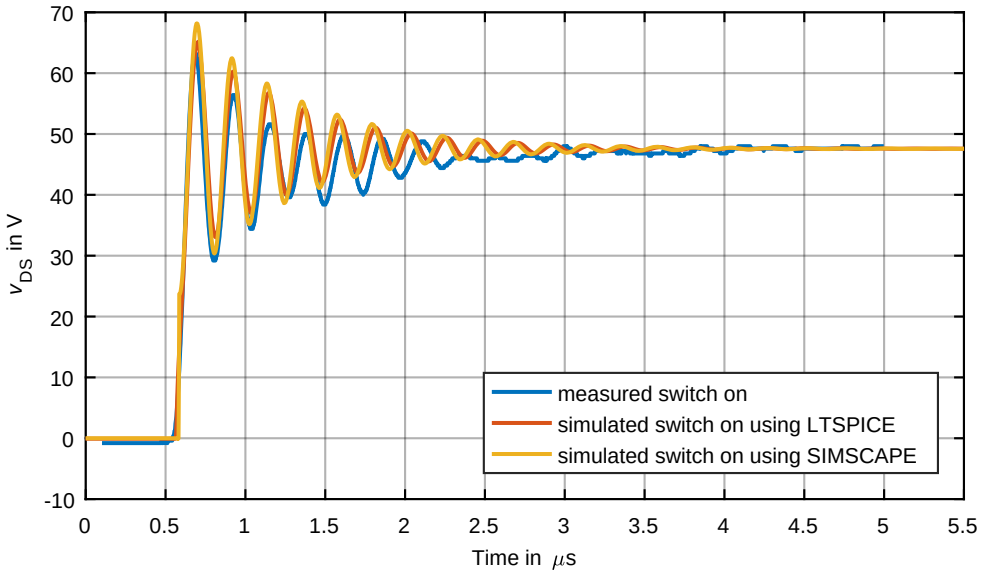


Figure 6.4 – Drain-source voltage V_{DS} during MOSFET switch-on time using physical simulations and measurement result [100].

The voltage needs time to fall to zero or to the desired drain voltage level in the switch-on and -off states, respectively. Similarly, there is a delay in the current rise and fall time.
The power losses during switch-on and -off times $P_{\mathrm{sw},on/off}$ are the product of switch-on and -off energy losses $E_{on/off}$, the grid frequency f_{g}, and the number of switch-on and -off states $n_{\mathrm{sw},on/off}$ in one time period (20 ms) as presented in Eq. (6.7).

$$P_{\mathrm{sw,on/off}} = E_{\mathrm{on/off}} \cdot f_{\mathrm{g}} \cdot n_{\mathrm{sw,on/off}} \tag{6.7}$$

To find out the power semiconductor losses, models on component-level are used to simulate the power switch dynamic behavior. For this purpose, the Shichman-Hodges model is introduced and parametrized using real component data-sheet values.

6.2.5 Shichman-Hodges Model

There are several models that describe a MOSFET on different levels. By increasing the physical description depth, the number of levels increases [163].
The simulation on component-level uses the most accurate MOSFET-model based on the Shichman-Hodges model. It does not contain the MOSFET body diode and therefore it is necessary to use an external one [44]. The Shichman-Hodges model is on level 1. By increasing the modeling depth it comes close to the semiconductor's physics part. Using the MOSFET-level-i model at higher depth of levels ($i > 1$), geometry based and semi empirical model are used as in [158]. These models at higher depth of levels are not further analyzed.
The Shichman-Hodges model requires data-sheet values to perform a dynamic switch-on and -off in µs-range. Therefore, the time-range of simulations on component-level is in the range of µs and is used only to analyze the MOSFET dynamic operation.
The calculated losses are then stored for further use in higher abstraction simulation levels. The switch-on result using the Shichman-Hodges model is close to the measurement switch-on behavior and allows the exact calculation of power semiconductor losses and H-bridge inverter efficiency.
The Shichman-Hodges model based on threshold voltage [156] on level 1 is used for simulations in Simscape. Fig. 6.5 represents the simulated n-channel MOSFET circuit diagram and is used in the physical simulation on component-level. This circuit contains the MOSFET main drain source C_{DS} and gate source C_{GS} capacitances. The current source between the drain and source pin delivers the current flowing through the MOSFET in its on-state. Parallel to the current source is the drain source on-resistance $R_{\mathrm{DS,on}}$, which represents the power MOSFET's equivalent resistance during the on-state. Furthermore, this circuit contains the MOSFET's pin resistances R_{D}, R_{G}, and R_{S}. The parameters used for the considered power MOSFET are listed in Table 6.1.
The circuit operates in three different cases. In the first state, assuming a smaller gate source voltage V_{GS} than threshold voltage V_{th} ($V_{\mathrm{GS}} < V_{\mathrm{th}}$), the drain source current in the off region is described in Eq. (6.8).

$$I_{\mathrm{DS}} = 0\,\mathrm{A} \tag{6.8}$$

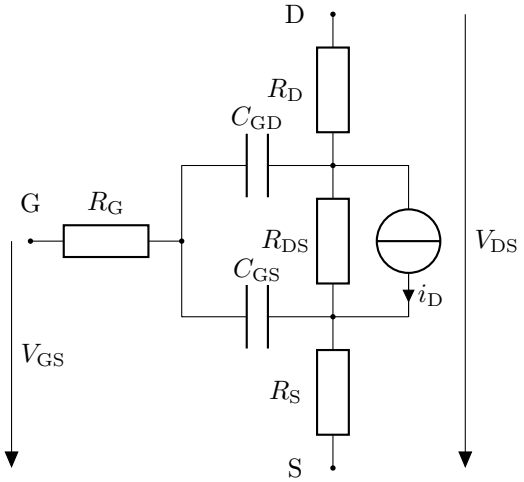


Figure 6.5 – Circuit diagram used to simulate a MOSFET with the Shichman-Hodges' equations in Simscape.

Table 6.1 – MOSFET's parameters used in the Shichman-Hodges circuit.

Parameters	**Nomenclature**	**Value**
Drain Resistance	R_D	1 mΩ
Drain Source on Resistance	$R_{DS,on}$	2.3 mΩ
Drain Current	i_D	120 A
Gate Source Voltage	V_{GS}	10 V
Gate Source threshold Voltage	V_{th}	3.1 V
Drain Source Voltage	V_{DS}	75 V
Source Resistance	R_S	1 mΩ
Gate Resistance	R_G	2.1 Ω
Gate Drain Capacitance	C_{GD}	53.3 pF
Gate Source Capacitance	C_{GS}	5.4 nF

In the second state, the linear region, at a positive drain source voltage V_{DS}, which is smaller than the difference between gate source and threshold voltage ($0 < V_{DS} < V_{GS} - V_{th}$), the drain source current I_{DS} is described by Eq. (6.9).

$$I_{DS} = K \cdot ((V_{GS} - V_{th}) \cdot V_{DS} - \frac{V_{DS}^2}{2}) \cdot (1 + \lambda \cdot |V_{DS}|) \tag{6.9}$$

K describes the transistor gain and λ the channel modulation [162].
In the third state, when $0 < V_{GS} - V_{th} < V_{DS}$, the MOSFET is in the saturation region and I_{DS} is described by Eq. (6.10).

$$I_{DS} = \frac{K}{2} \cdot (V_{GS} - V_{th})^2 \cdot (1 + \lambda \cdot |V_{DS}|) \tag{6.10}$$

The presented Shichman-Hodges equivalent MOSFET circuit does not contain the body diode. Normally real power MOSFETs have an integrated free-wheeling diode, also called body diode. In some cases, the body diode is eliminated when the substrate and the source gate are short-circuited at production [183]. For the used MOSFET model, the external diode model

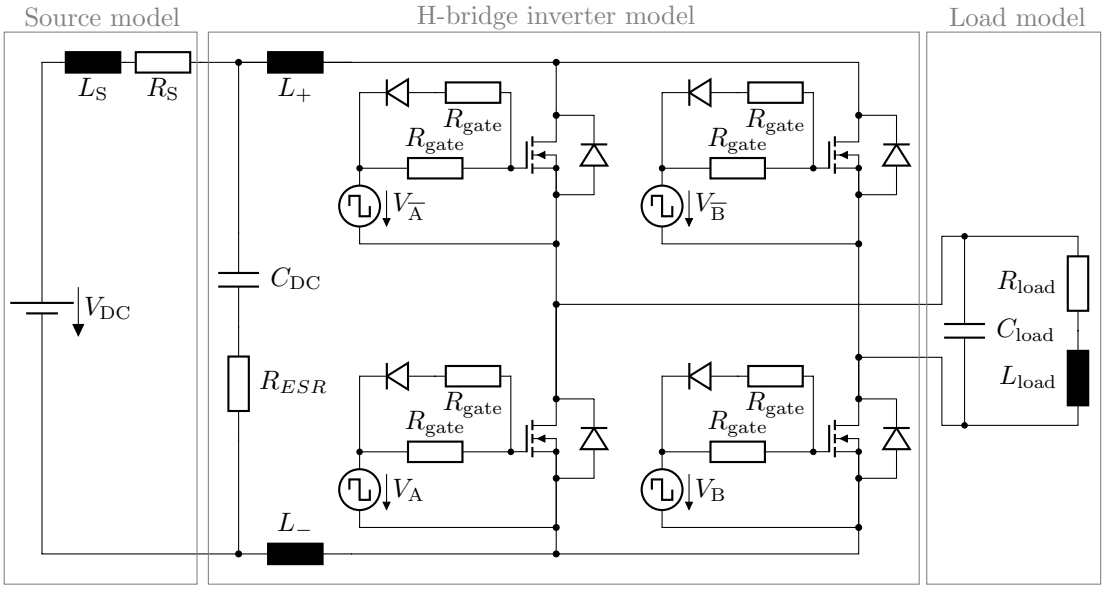


Figure 6.6 – Circuit used for efficiency simulations on component-level. It considers the PCB parasitic inductances L_+, L_-, the source inductance and resistance L_S, R_S, and the load model represented by a power resistor R_{load} with its parasitic components L_{load} and C_{load} [105].

uses an exponential current-voltage-curve with its internal resistance. Adding this feature results in the VDMOS power MOSFET model.
The simulation results achieved with LTspice are similar to those from Simscape as presented in Fig. 6.4. Using this model, it is possible to exactly model the switching and conduction losses on component-level. To achieve those results, the circuit parasitics, used for H-bridge inverter efficiency measurement, are further studied.

6.2.6 Parasitic Elements

The simulation results of the H-bridge inverter efficiency are validated on the test bench, which is modeled considering its parasitic elements and an exact resistive load model. To operate the H-bridge inverter at different load points, a power resistor with big geometric dimensions is used and modeled using its parasitic inductance and capacitance. Their values are derived from measurement series.
To achieve simulation results close to the hardware, test bench parasitic elements are implemented using several measurements on the DC- and AC-side as shown in Fig. 6.6. The circuit shown considers the gate circuit connected to the gate driver output and the power MOSFET input. It uses one gate resistor R_{V1} to switch on the MOSFET by charging its gate capacitance. To switch-off the MOSFET faster, a diode and resistor are connected in parallel to the gate resistor to halve the discharge resistance.
Furthermore, the current and voltage gradients during the switching times are influenced by the parasitic elements in the circuit-board, which are represented in Fig. 6.6 with L_+ and L_- and are found out from the H-bridge inverter PCB data. These are given as parasitic inductances on the DC-side based on a constant inductance value per meter of line length, 1 μH/m.

Table 6.2 – Simulation model's parameter on component-level used in Fig. 6.6 [105].

Parameters	**Nomenclature**	**Value**
DC-Link voltage	V_{DC}	47.6 V
Switching frequency	f_{sw}	1 kHz
Source inductance	L_{S}	25 nH
Source resistance	R_{S}	8 mΩ
DC-link capacitance	C_{DC}	1.64 mF
DC-link ESR	ESR	28 mΩ
Parasitic inductance	L_+ and L_-	5 nH
Gate driver voltage	V_{A},$V_{\overline{\mathrm{A}}}$,$V_{\mathrm{B}}$,$V_{\overline{\mathrm{B}}}$	12 V
Gate resistor	R_{gate}	10 Ω
Load resistance	R_{load}	1.422 Ω
Load capacitance	C_{load}	120 nF
Load inductance	L_{load}	196 µH

6.3 Efficiency Assessment for One Submodule

The simulation based on the presented circuit and parameters is built and the results are compared to the measurements at different operation points. The H-bridge inverter efficiency η_H during the discharging operation is defined as the AC to DC input power quotient. Those powers are not measured directly, but rather calculated from certain measured quantities. For the H-bridge inverter, the measurements of two voltages V_{in} and v_{out}, and of two currents I_{in} and i_{out}, are required during the discharging operation as shown in Eq. (6.11).

$$\begin{aligned} P_{\mathrm{in}} &= I_{\mathrm{in}} \cdot V_{\mathrm{in}} \\ p_{\mathrm{out}} &= i_{\mathrm{out}} \cdot v_{\mathrm{out}} \\ \eta &= \frac{p_{\mathrm{out}}}{P_{\mathrm{in}}} \cdot 100\,\% \end{aligned} \tag{6.11}$$

The H-bridge inverter efficiency comparison at different load currents between Simscape and LTspice simulation results and measurements with Power Analyzer PA4000 [105] are done and shown in Fig. 6.7. Despite the power analyzer's high precision, the measured efficiencies reach a deviation up to 0.7 % [105].
The maximum H-bridge inverter efficiency is 99.4 % in the measurement and around 99.6 % in the LTspice and Simscape simulation. At nominal power the efficiency is 98.6 % in the measurement and approximately 99 % in the LTspice and Simscape simulation as shown in Table 6.3. The simulated H-bridge inverter efficiency is, as expected, slightly higher than the measurements, because not all parasitic elements are modeled and approximations are made.
The CHB inverter consists in addition to the H-bridge inverters of a power filter, which also produces losses that are further studied.

6.4 Power Filter Losses

A grid connected CHB inverter usually consists of several components aside from the H-bridge inverters. Due to the decentralized structure of CHB inverter, cables are required to connect

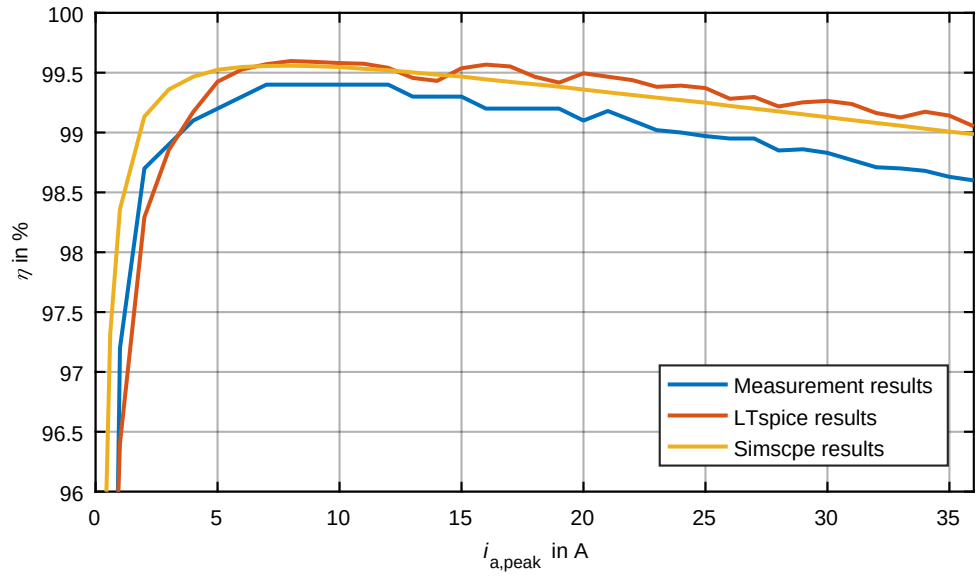


Figure 6.7 – H-bridge inverter efficiency at different load current using Simscape and LTspice simulations and measurements with power analyzer PA4000 [105].

Table 6.3 – H-bridge inverter efficiency.

Parameter	Nomenclature	Value
Maximal efficiency in measurements	$\eta_{\text{max,meas}}$	99.4 %
Maximal efficiency in LTspice	$\eta_{\text{max,LTspice}}$	99.65 %
Maximal efficiency in Simscape	$\eta_{\text{max,Simscape}}$	99.56 %
Nominal efficiency in measurements	$\eta_{\text{nom,meas}}$	98.60 %
Nominal efficiency in LTspice	$\eta_{\text{nom,LTspice}}$	99.05 %
Nominal efficiency in Simscape	$\eta_{\text{nom,Simscape}}$	98.99 %

the H-bridge inverters with each other. Those losses are neglected.
The main loss sources are the power filter and the H-bridge inverters. The inductor losses are categorized as iron and copper losses [13]. The power filter contains an internal resistance and its conduction losses represent the main power loss source when compared to other categories and depend on the nominal grid current as shown in Fig. 6.2. Using a power filter in the studied power range gives an internal resistance value of about 12 mΩ. Therefore, the losses in this filter at nominal current are in Eq. (6.12). The power filter losses at nominal operation point represent 0.04 % compared to the CHB inverter nominal power.

$$P_{\text{cond,filter}} = R_L \cdot I_{\text{rms}}^2 = 7.8 \text{ W} \tag{6.12}$$

6.5 CHB Inverter Efficiency on Component-Level

As described in the previous sections, the CHB inverter based BESS consists of 24 battery modules and full bridge-inverters and is connected to the grid using an inductor with internal resistance.

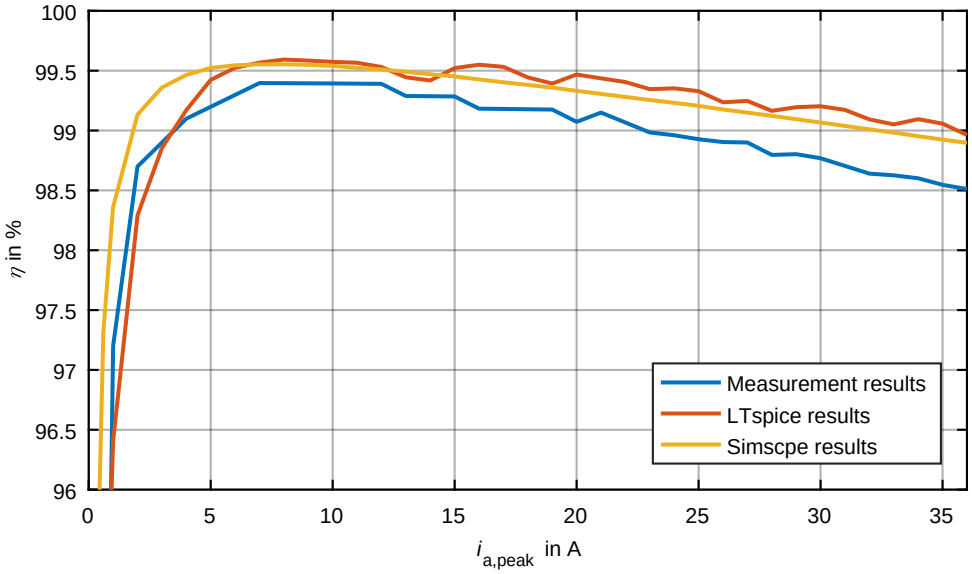


Figure 6.8 – CHB inverter efficiency considering the power losses in all H-bridge inverters and the power filter used.

Table 6.4 – CHB inverter efficiency.

Parameter	Nomenclature	Value
Maximal efficiency in measurements	$\eta_{\mathrm{max,meas}}$	99.36 %
Maximal efficiency in LTspice	$\eta_{\mathrm{max,LTspice}}$	99.55 %
Maximal efficiency in Simscape	$\eta_{\mathrm{max,Simscape}}$	99.51 %
Nominal efficiency in measurements	$\eta_{\mathrm{nom,meas}}$	98.56 %
Nominal efficiency in LTspice	$\eta_{\mathrm{nom,LTspice}}$	99.01 %
Nominal efficiency in Simscape	$\eta_{\mathrm{nom,Simscape}}$	98.94 %

Fig. 6.8 shows the whole CHB inverter efficiency. It reaches a maximum of 99.36 % in the measurement and 99.5 % in the LTspice and Simscape simulation. At nominal power, the efficiency is 98.56 % in the measurement and approximately 99 % in the LTspice and Simscape simulation as shown in Table 6.4.

6.6 Summary

This section outlines the possibilities for H-bridge inverter's power losses calculation on component-level. The simulation is used to study the CHB inverter components and considers the power switches' losses using dynamic power MOSFET physical model such as the Shichman-Hodges model.
The simulation results are validated with measurements using a power analyzer. The implemented hardware assessment shows high accuracy between the efficiency results of different simulation programs and measurements. Whereby the efficiency in the simulation is slightly higher than measured.
The presented simulation results show high accuracy to the measurements of up to 0.1 %. This

is important for the high efficiency application such as the case of a 17-level CHB inverter. The exactness of those results allows an effective and compact heat sink design before the implementation phase. Therefore, it is highly recommended to start using simulations on component-level before going into the implementation phase.
The conduction power losses of the used filter are also added to the H-bridge inverter losses. The simulation results on component-level support the simulations on higher abstraction levels, such as circuit- and system-level. Those results are transferred to the next upper abstraction level in form of lookup Tables to enable the prediction of the CHB inverter efficiency at different operation points, to allow the usage of ideal switches for faster simulation, and to permit the design of several parameters and other components for the whole BESS before going up to the simulation on system-level.

7 Inverter Design on Circuit-Level and Hardware Implementation

In the last chapter, the simulations on component-level are introduced and validated using hardware measurements. The efficiency of the H-bridge inverter and the whole CHB inverter is simulated and validated.
In this chapter, the inverter design on higher abstraction level is discussed and implemented in hardware. The design is based on physical models on circuit-level, which are introduced in Section 7.1. The inverter design using physical simulations on circuit-level allows to simulate the inverter as a circuit describing its dynamic behavior and operation on the grid. The grid connected CHB inverter physical modeling on circuit-level is introduced and use cases are shown in Section 7.2. The different simulation model parts are presented and parametrized. The inverter operation on circuit-level is explained and the relevant physical model parameter, such as the grid model, the modulation techniques, the power filter, and the current controller are presented.
Since the inverter is grid connected, different grid simulation models are introduced in Section 7.3. These models are compared to each other and the one to be used for further simulations on circuit-level is selected.
Since the inverter switches different voltage levels, the modulation carrier-signals used can be placed differently. For the CHB inverter, different modulation techniques are possible. Those are presented, implemented, and compared to each other to be used in BESS. The modulation techniques influence the submodules and the whole inverter's switching frequency as shown in Section 7.4. At the section's end, one modulation technique is recommended to be used in BESS.
Due to the inverter switching behavior, distortions on the grid occur. For grid distortion limitation, a power filter is required for proper and standard-conform inverter operation. Generally, the CHB inverters require smaller filters with low inductance values compared to the two-level inverters. To fulfill the grid requirements, the power filter is designed in Section 7.5.
To design the current controller for the CHB inverter, the switching frequency and the power filter parameter must be defined. Therefore, the plant to be controlled is fully defined and the used control method is shown and explained in Section 7.6. At the section's end, the control method is adapted for the CHB inverter to be used in BESSs.
The power filter and the switching frequency represent two first order delays. Therefore, the plant is a second order system. The suitable inverter current controller is designed, studied, implemented in the physical simulations on circuit-level, and the results such as the system stability, step response, and steady state operation are presented in Section 7.7. Finally, the simulations are validated with hardware measurements on the 17-level CHB inverter in Section 7.8.

7.1 Introduction

In the simulations on component-level, the losses and rather the inverter efficiency are studied and validated with hardware measurements.
The next higher abstraction is the circuit-level. On this level, the CHB inverter switching model is described by ideal power switches and connected to a power grid model. On circuit-level, the simulations are done to discuss the possible modulation techniques and the power filter design for the selected one-stage CHB inverter. Furthermore, on this level the controller used for the grid connection is designed and validated in hardware. The efficiencies calculated on component-level are implemented as look-up tables. In addition, the inverter dynamic operation and its controller can be simulated on circuit-level.
The switching model of the inverter is made to analyze its dynamic operation on the grid. Therefore, different modulation techniques can be examined and compared to each other. The multi-carrier-signal modulation is becoming increasingly important as the number of voltage levels increases. The placement of the carrier-signals influences the discharging of the battery modules for the multilevel CHB inverter based BESS.
The inverter model on circuit-level is also known as switching model. Using ideal switches leads to the representation of the inverter's dynamic operation and allows therefore the power filter (Section 7.5) as well as the current controller design (Section 7.6).
From this level, the software-part for further hardware implementations in a test bench is generated.

7.2 CHB Inverter Model on Circuit-Level

On circuit-level, the simulation model is divided into two main parts using significantly different simulation sampling-times to represent the software- and hardware-parts as shown in Fig. 7.1. The hardware-part uses higher simulation sampling frequency. The software-part sampling-time is limited due to the hardware used for this purpose. Those simulation model parts are further explained.

7.2.1 Inverter's Hardware Modeling

Fig. 7.1 shows the simulation model of the selected one-stage CHB inverter as implemented on circuit-level. The simulation contains models of the power MOSFETs or rather the H-bridge inverters, the battery modules, the power grid, the power filter, and the PWM modulators.
In the used models on circuit-level, the power MOSFET dead times during switching-on and -off are neglected to shorten the simulation duration, when compared to the previous models on component-level. The power MOSFET model used before focuses on the exact representation of the real switching-on and -off. The results are stored in datasets to be used in simulations on higher abstraction levels. This allows calculating the whole inverter efficiency at different operation points on circuit-level. Using idealized switches in simulations on circuit-level simplifies the switching transitions. The used model considers only the states on or off. Therefore, larger simulation steps are possible and shorter run-time is reached.

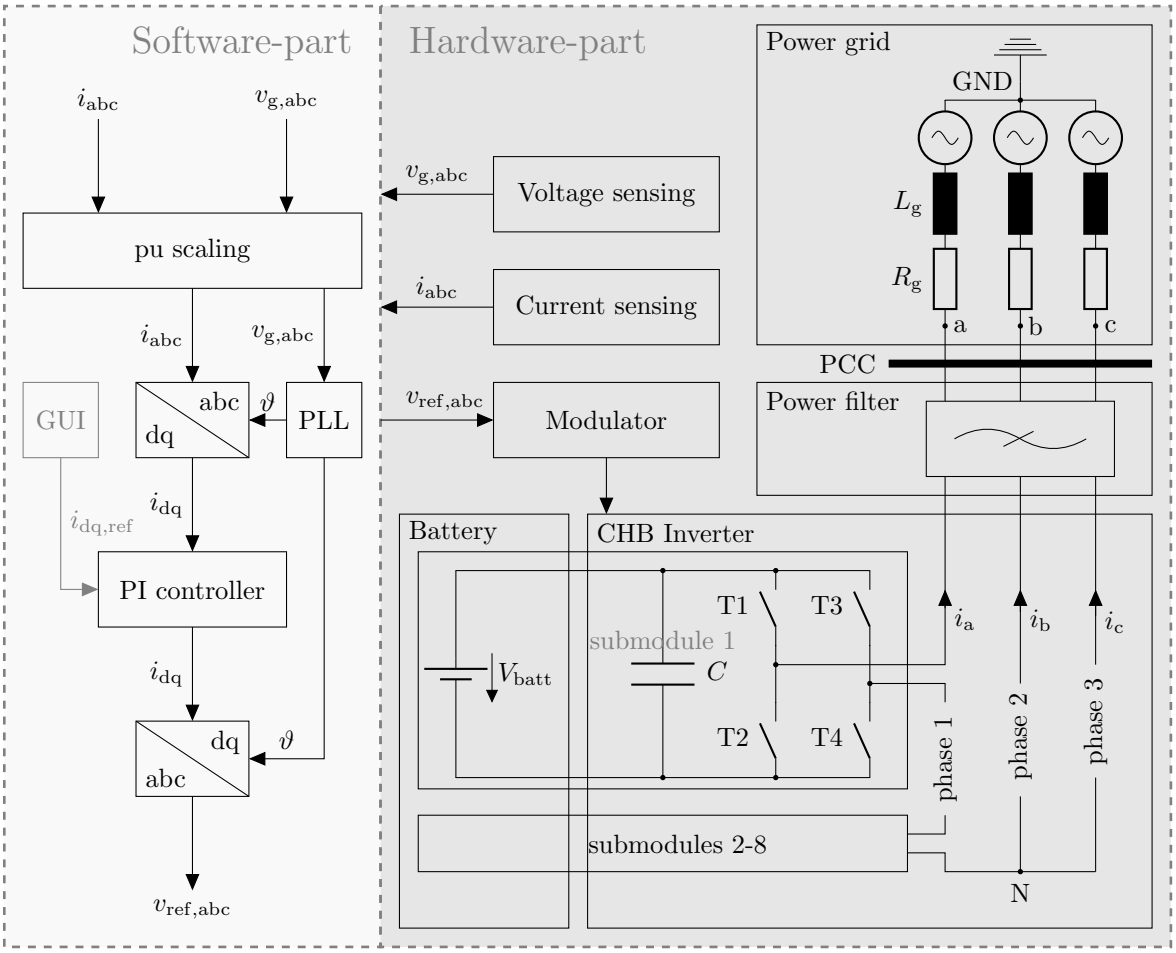


Figure 7.1 – Simulation model of the CHB inverter on circuit-level.

The simulated time-range is in second-range and is higher than simulations' time-range on component-level.
The used battery model consists of a controlled voltage source with an internal resistance. It includes an SoC calculator and look-up table with the cell voltage from open circuit measurements as presented in Fig. 3.9. However, the battery model does not affect the inverter operation. Therefore, the battery model is not further studied.
The used power filter model consists of only an inductor with a given inner resistance and is further studied in the Section 7.5. As shown in Fig. 7.2, the power grid can be modeled in different ways using ideal voltage source, weak and strong grid model [95] and is further discussed in Section 7.3.
The PWM modulators are placed in the model's hardware-part. They modulate the reference signals generated by the software-part. These modulators are presented within the physical model due to their high sampling frequency.
The modulator used to generate the required PWM signals for the inverter operation runs with higher sampling frequency than the real-time system. It is mostly realized as a device with a given PWM switching frequency f_{sw} and needs at its input the reference signal v_{ref}. Therefore, the modulators are represented in the simulation model on circuit-level using higher sampling frequency. This enables the representation of the carrier-signals to use a sine carrier

comparison and generates the pulses.
The voltage and current sensing blocks are modeled as factors of the measured signals.

7.2.2 Inverter's Software Modeling

The inverter's hardware-part presented in the previous section is controlled by a mathematical part, which is used as a software in the implementation phase and is lower sampled than the hardware model. The software-part's sampling frequency is usually set equal to the switching frequency. The inverter's software runs in a real-time system to control the BESS's operation. The software-part represented in Fig. 7.1 is explained block-wise in the following.
The block *pu scaling* is used to scale the measured signals to per unit (pu) values. The usage of normed values simplifies the description of the signals during the control process.
The block *abc to dq* contains the Clarke- and Park-transformations as presented later in Section 7.6. Those mathematical calculations allow a comprehensive representation of the measured and controlled currents. Their usage allows a comprehensive and decoupled control of the active and reactive power exchange.
The Phase Locked Loop (PLL) delivers the transformation angle ϑ used to transform the measured currents into dq-frame using the block *abc to dq*. This angle is also used in the inverse transformations. This method is presented in Section 7.6.2.
The Graphical User Interface (GUI) represents the communication between the user controlling the BESS and its EMS. It delivers the reference values for the inverter's controller.
The software-part consists of PI-controllers for the active and reactive power exchange between the battery storage units and the grid. The main inverter software-part is its controller. It controls the difference between the actual and reference current values and delivers the inverter duty cycle to the modulators. In-between, mathematical transformations are required and are delivered by the blocks *abc to dq* and *dq to abc*. This model-part is further explained in Section 7.6.
This block contains the inverse transformations used in the block *abc to dq*. It contains the inverse Clarke- and Park-transformation using the angle ϑ. This part is further explained in Section 7.6.
In the further design steps, the hardware-parts, such as the power grid model, the modulation techniques, and the filter design are further separately discussed. The software-part and the controller design are nearly explained. Finally, the simulation results on circuit-level are presented and validated with hardware measurements on the 17-level CHB inverter.

7.3 Grid Modeling on Circuit-Level

The low voltage grid model on circuit-level presented in this section is a part of the publications [95] and [100]. Different types of grid models, their effect on the inverter operation, and the judgment of their effects on the grid are presented within this section.

7.3.1 Introduction to Grid Models

The grid and its parameter are important factors for simulating grid connected inverters. The simulation results analysis shows a difference depending on the used grid model parameter, which is generally represented by its Thevenin equivalent circuit [78].
An ideal voltage source with and without an internal impedance is used as a grid model in the simulations on circuit-level. Fig. 7.2 shows the ideal single-phase grid model represented by a voltage source. The strong and the weak grid models contain an internal resistance and inductance.

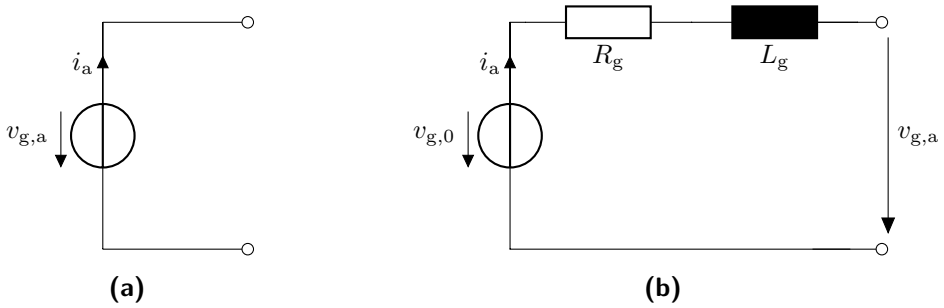


Figure 7.2 – Single-phase (a) ideal grid model represented by a voltage source, (b) strong, and weak grid models containing internal resistance and inductance.

7.3.2 Grid Models' Parameter

The grid model parameters define the inverter effects in terms of harmonic content in voltage and current. For this purpose, three grid models with different parameters are presented in Table 7.1.
As shown in Fig. 7.2a, the first ideal power grid model is represented by an ideal voltage source with a phase voltage of $v_a = 230\,\mathrm{V}$ and a frequency of $f_g = 50$ Hz. The second and third grid

Table 7.1 – Grid model parameters for ideal, strong, and weak grid [95], [100].

Parameter	**Nomenclature**	**Value**
Line-to-line voltage	v_{LL}	400 V
Line-to-ground voltage	v_a	230 V
Grid frequency	f_g	50 Hz
Short circuit apparent power for the weak grid	$S_{sc,weak}$	1 MVA
X/R-ratio for the weak grid	$ratio_{X/R,weak}$	2.0
Inductance of the weak grid	$L_{g,weak}$	8.4 mH
Resistance of the weak grid	$R_{g,weak}$	26.5 mΩ
Short circuit apparent power for the strong grid	$S_{sc,strong}$	100 MVA
X/R-ratio for the strong grid	$ratio_{X/R,strong}$	2.6
Inductance of the strong grid	$L_{g,strong}$	84.2 µH
Resistance of the strong grid	$R_{g,strong}$	0.2 mΩ

models use the same circuit containing a resistor and an inductor as shown Fig. 7.2b. By changing the values of the short circuit apparent power S_{sc}, the internal grid resistance R_{g}, and inductance L_{g}, the grid is defined as strong or weak. The grid's internal resistance and reactance represent the physical grid elements such as the internal power plant generator's line resistance and inductance, the power transmission lines, and the transformers seen from the PCC's point of view.
The short circuit apparent power S_{sc} and the reactance to resistance ratio X/R in the weak grid are lower than in the strong grid. Moreover, the strong grid's internal resistance is smaller than that of the weak grid. Therefore, the voltage drop over this resistance is small, which leads to small voltage fluctuation on the PCC while loading the grid. Weak grids, as the name contains, are highly affected by the inverter operation.
Different definitions of strong and weak grids are mentioned in [32], [52], [154], and [187]. The strong and weak grid definition, as in [58], depends on the ratio $ratio_{S_{\mathrm{sc}}}$ shown previously in Eq. (2.9) in Chapter 2. Whenever the $ratio_{S_{\mathrm{sc}}}$ is higher than 50, the grid is defined as strong grid. By $ratio_{S_{\mathrm{sc}}}$ values of less than 15, the grid model is defined as weak grid as summarized in Table 7.2.

Table 7.2 – Relation of the grid model type and the ratio of the grid and inverter power.

Grid model type	$\boldsymbol{ratio_{S_{\mathrm{sc}}}}$
Strong grid model	$\gg 50$
Weak grid model	< 15

7.3.3 Simulation Results Using Different Grid Models

To clarify the difference in the inverter grid effects, simulations are made using, as an example, the selected one-stage 17-level CHB inverter topology using the parameter shown in Table 7.3. The inverter operates with 17-level output voltage because the submodules' DC-link voltage is set to 40 V. It uses a phase shifted pulse width modulation (PSPWM), which will be presented later in Section 7.4.1. The simulation results using the three different grid models are shown in Fig. 7.3 for the ideal, the strong, and the weak grid. The harmonic distortion on the ideal and strong grid is almost negligible. However, using the weak grid model, the inverter effects on the grid are higher. Table 7.4 represents the THD values for the current and voltage by

Table 7.3 – CHB inverter parameters used to represent its effects on different grid models in simulations on circuit-level [95].

Parameter	**Value**
Number of voltage levels	17
Modulation technique	PSPWM
Nominal inverter power	17.5 kVA
Inverter voltage switching frequency	8 kHz
Power filter resistance	12 mΩ
Power filter inductance	0.98 mH
Submodules' DC-link voltage	40 V

Table 7.4 – Voltage and current THD using different power grid models [95].

Grid model	THD_v in %	THD_i in %
Ideal grid model	0	0.85
Strong grid model	0.03	0.87
Weak grid model	3.37	2.73

considering all harmonics order to highlight the effect of the grid parameter on the inverter's operation. All these values are under the standards' limits given by [68].

Using an ideal grid model, the THD_v is equal to zero and the THD_i is less than 1 %. Using the strong grid model, the THD_v slightly increases 0.03 % in comparison with the usage of the ideal grid and the THD_i is 0.02 % higher.
Using the weak grid model by decreasing the values of the internal grid resistance and inductance, the THD_v and THD_i increase significantly to values around 3 % and are still under the standards limits. As shown in Fig. 7.3, the inverter and grid voltages are then higher distorted. Using the weak grid model, the THD_v and THD_i significantly increase from 0.03 % to 3.37 % and from 0.87 % to 2.37 %, respectively. This effect can be seen in the distorted waveforms as in the bottom-part of Fig. 7.3. The weak grid shows high distorted results and is therefore selected to be used in further models. It shows the nearest results to the five-level inverter's hardware implementation presented in [106].
There are different further possible approaches for grid modeling not mentioned within this section. Three basic categories are shown in [94].
Finally, the real grid voltage can vary in a tolerance band of up to ±10 % of its nominal voltage as given by the grid standards. However, this variation is not further studied in the simulations.

7.4 Modulation Techniques for Multilevel Inverters

The particularity of multilevel inverters is the usage of multiple carrier-signals. An n-level CHB inverter generally uses $n_{\text{submodules}} = \frac{1}{2}(n-1)$ submodules and requires therefore the same number of carrier-signals $n_{\text{carrier-signals}} = n_{\text{submodules}}$. The modulation techniques for multilevel inverters have been introduced in [100], [124], and [150].
Fig. 7.4 represents the studied modulation techniques, which are explained using an ideal sine signal to modulate the CHB inverter voltage with an amplitude modulation index of $m_{\text{amp}} = 1$ and frequency modulation index of $m_f = 20$. This sine signal represents an idealization of the PI-controllers' output signals at a given operation point.
Generally, the modulation techniques can be divided into two categories as shown in Fig. 7.4. The first category is carrier based. It uses a modulator and the inverter operates at constant switching frequency. As an example, the Phase Shifted Pulse Width Modulation (PSPWM) and Level Shifted PWM (LSPWM) are mentioned. To compare the multi-carrier based modulation techniques, the switching frequency of the CHB inverter output voltage is set to $f_{\text{sw,CHB}} = 8$ kHz.
The second category operates without modulators with a variable or rather non defined

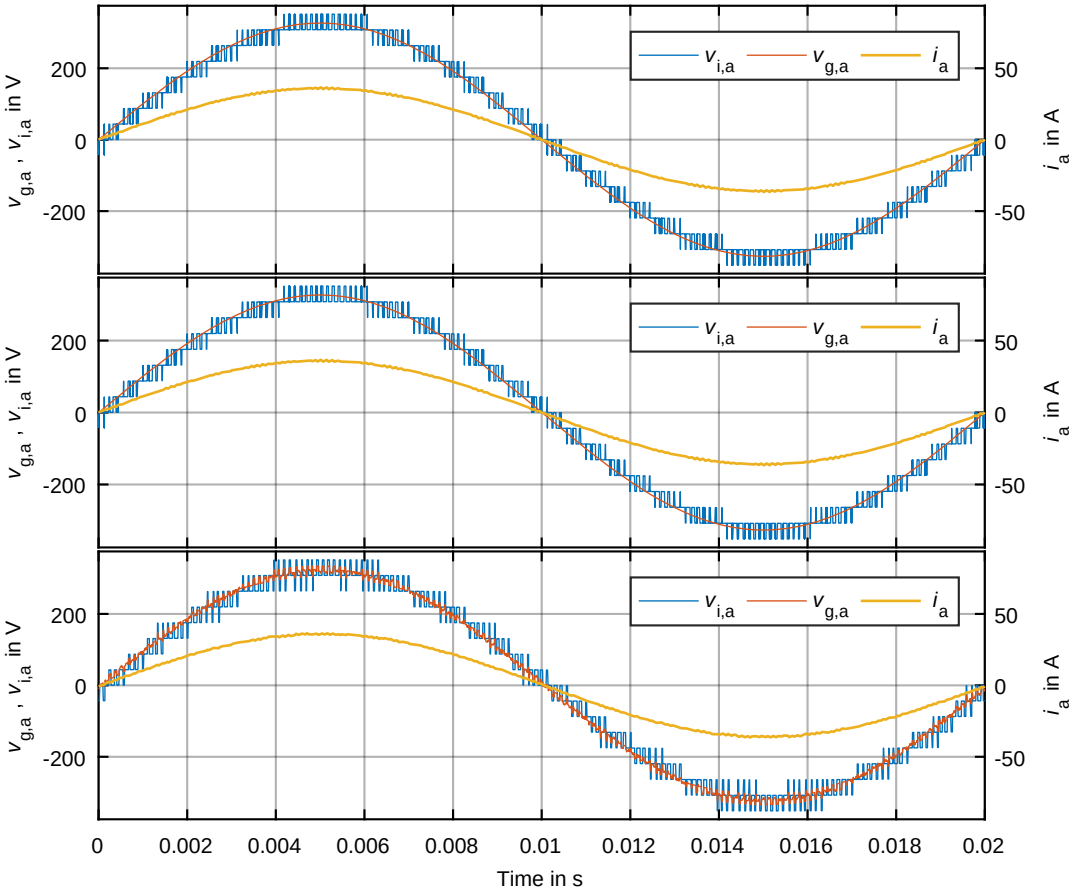


Figure 7.3 – Grid and inverter voltages and current using ideal, strong, and weak grid model.

switching frequency, such as the Nearest Level Control (NLC) or Hysteresis Control (HC). For the selected 17-level CHB inverter, both of the modulation technique categories are discussed, implemented, compared to each other, and finally one modulation technique is recommended.
The main evaluation criteria is the BESS's or rather the inverter's efficiency. However, the harmonic content, which describes the inverter grid effects, is studied and analyzed using the mentioned modulation techniques.
As discussed in the previous section, the grid parameter influences the normative operation of the inverter. For the following analysis, the weak grid model is used due to the better compliance with the later shown hardware measurements.

7.4.1 Phase Shifted PWM

In [91], it is shown, that all CHB inverters available in the industry are using the PSPWM as modulation technique. No new modulation technique has found its way into industrial application when CHB inverter is used. This is due to the proven PSPWM and its simplicity over other methods. To modulate one ideal sine wave signal using the CHB inverter topology, the same number of carrier-signals and submodules is required $n_{\mathrm{carrier-signals}} = n_{\mathrm{submodules}}$.

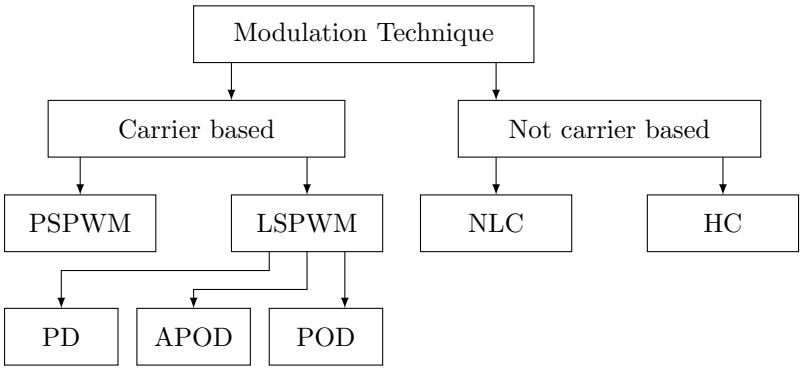


Figure 7.4 – Modulation techniques for the CHB inverter on circuit-level.

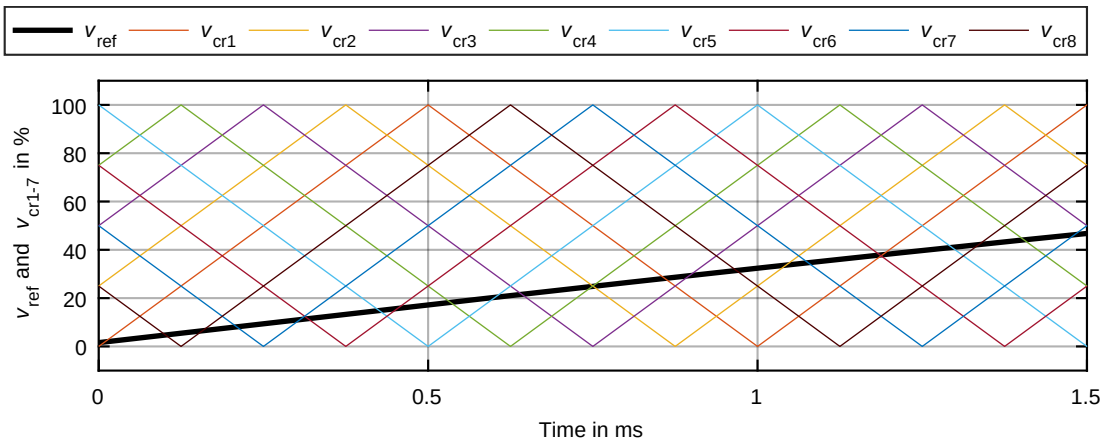


Figure 7.5 – Reference voltages and carrier-signals for the 17-level CHB inverter using PSPWM.

The PSPWM's name means, the carrier-signals are shifted in their phase to each other. This shifting leads to an increased switching frequency of the inverter. In case of the selected one-stage 17-level CHB inverter, the submodule's switching frequency is set to $f_{\mathrm{sw,SM}} = 1$ kHz using a bipolar PWM as shown in Eq. (7.1). If a unipolar PWM is used, the resulting inverter switching frequency is double the frequency when a bipolar PWM is used.

$$f_{\mathrm{sw,i,PSPWM}} = f_{\mathrm{sw,SM}} \cdot n_{\mathrm{submodules}} \tag{7.1}$$

The carrier-signals are shifted from each other depending on the submodule switching frequency $f_{\mathrm{sw,SM}}$ as shown in Eq. (7.2).

$$T_{\mathrm{shift}} = \frac{1}{f_{\mathrm{sw,SM}} \cdot n_{\mathrm{submodules}}} \tag{7.2}$$

Using $f_{\mathrm{sw,SM}} = 1$ kHz and $n_{\mathrm{submodules}} = 8$, the angular phase shift is $\vartheta = 45°$ and the time shift is $T_{\mathrm{shift}} = 125\,\mu\mathrm{s}$ between the carrier-signals v_{cr1}–v_{cr8} as presented in Fig. 7.5. The frequency of the reference sinusoidal signal's v_{ref} is set to $f_{\mathrm{ref}} = 50\,\mathrm{Hz}$.
The resulting inverter output voltage is represented in the top-part of Fig. 7.6 for a half time period. It consists of eight positive steps, eight negative steps, and the zero voltage step, which means 17 voltage levels. The switching frequency of the output voltage is $f_{\mathrm{sw,CHB}} = 8$ kHz, where the switching frequency of all submodule is $f_{\mathrm{sw,SM}} = 1$ kHz as shown in the bottom-part of Fig. 7.6 and later in Table 7.6.

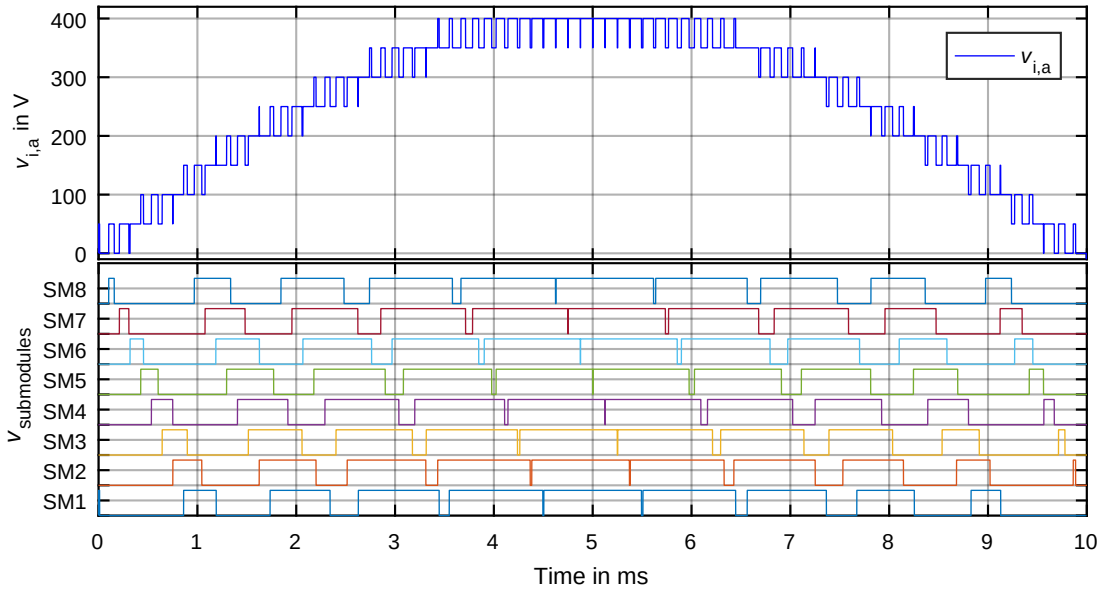


Figure 7.6 – CHB inverter and submodules voltages using PSPWM.

Advantages Using PSPWM, the reduced submodule switching frequency leads to decreased switching losses. Power semiconductors with low inner resistance $R_{\mathrm{DS,on}}$ can be used to increase the inverter efficiency as discussed in the last chapter. At $f_{\mathrm{sw,SM}} = 1$ kHz, the maximum efficiency of 99.4% of each submodule is simulated and validated with measurements as previously shown. The CHB inverter's efficiency is equal to the efficiency of one of its submodules in addition to the power filter losses. However, at a constant inverter rated current, the filter and its losses remain the same in all discussed modulation techniques.
Using PSPWM, all H-bridge inverters operate at the same switching frequency and conduction time [181]. Furthermore, low switching frequencies lead to decreased EMI effects and represent a main advantage of the multilevel inverters.
When the battery modules are fully charged, the inverter operates using only 13 voltage levels. Using the PSPWM, all submodules operate even at reduced number of levels.

Disadvantages The DC-link capacitance sizing depends on the inverter's switching frequency. In case of PSPWM, the decreased submodule's switching frequency implies the usage of higher DC-link capacitance. The submodules' size and costs increase.
The realization of the PSPWM requires exact shifting of the carrier-signals. This means higher complexity by implementation in hardware compared with the LSPWM presented in the next section. In failure case, the new shift angle for the carrier-signals must be calculated online and the BESS operation can disturb the power grid. New synchronization using the new shifting angle between the carrier-signals is required.

7.4.2 Level Shifted PWM

Using multi-carrier PWM, the carrier-signals can be shifted to each other in the time or in their level. If the carrier-signals are placed over each other, the modulation is called LSPWM.

Table 7.5 – THD and V_{rms} using the three different types of LSPWM at different modulation indexes.

	PD-LSPWM		POD-LSPWM		APOD-LSPWM	
m_{amp}	THD_v	V_{rms}	THD_v	V_{rms}	THD_v	V_{rms}
0.10	60.90 %	40.41 V	60.85 %	40.20 V	60.85 %	40.20 V
0.20	31.40 %	69.63 V	31.44 %	69.44 V	31.45 %	69.77 V
0.30	19.04 %	100.51 V	19.05 %	100.11 V	19.04 %	100.28 V
0.40	12.89 %	132.27 V	12.90 %	132.23 V	12.90 %	132.73 V
0.50	10.61 %	163.34 V	10.60 %	163.60 V	10.60 %	163.43 V
0.55	10.35 %	181.02 V	10.35 %	180.21 V	10.35 %	180.86 V
0.60	9.68 %	196.61 V	9.68 %	195.99 V	9.68 %	196.08 V
0.65	8.10 %	213.17 V	8.09 %	212.41 V	8.10 %	213.01 V
0.70	8.56 %	228.55 V	8.55 %	228.76 V	8.56 %	229.30 V
0.75	7.15 %	244.45 V	7.15 %	244.01 V	7.15 %	244.84 V
0.80	7.10 %	261.88 V	7.10 %	261.48 V	7.11 %	260.93 V
0.85	6.80 %	276.85 V	6.80 %	276.72 V	6.80 %	276.72 V
0.90	5.91 %	293.94 V	5.91 %	292.92 V	5.91 %	293.00 V
0.95	6.25 %	308.75 V	6.25 %	309.19 V	6.24 %	309.81 V
1.00	5.40 %	325.59 V	5.38 %	325.58 V	5.40 %	325.56 V
1.05	5.17 %	335.31 V	5.17 %	334.26 V	5.18 %	334.99 V
1.10	5.88 %	343.01 V	5.87 %	341.94 V	5.89 %	342.76 V
1.15	7.07 %	349.84 V	7.07 %	349.18 V	7.07 %	350.21 V
1.20	8.41 %	355.64 V	8.38 %	354.71 V	8.42 %	355.35 V

The LSPWM offers a degree of freedom in the placement of the carrier-signals. It is divided into three main sub-categories depending on the carrier-signals placement and their phase shift. Therefore, Phase Disposition PD-, Phase Opposite Disposition POD-, and Alternative Phase Opposite Disposition APOD-LSPWM are possible as shown in Fig. 7.7. These three simple positioning possibilities are presented in [30]. Fig. 7.7 represents the three different types of LSPWM for two submodules of the 17-level CHB inverter using the carrier frequency of 8 kHz.
Placing all carrier-signals in phase to each other delivers the PD-LSPWM or PH-disposition, described in [30] and shown in Fig. 7.7a.
The POD-LSPWM is reached whenever the carrier above the middle line of the sine wave are in phase among them but in opposition to those below the line (POD-LSPWM) as shown in Fig. 7.7b. The carrier-signals are in POD-LSPWM generally mirrored around the time-axis.
Placing all carrier-signals alternatively in opposition leads to the APO disposition (APOD-LSPWM) as shown in Fig. 7.7c. The carrier-signals are alternating between 0 and 180°.
However, the resulting difference in the output voltage is minimal due to the high carrier frequency used in this modulation. The difference in the voltage's THDs of the presented sub-categories is negligibly small.
In [5], the PD method is presented as superior compared to the other LSPWM modulation techniques. In contrast, in the case of the 17-level CHB inverter, the THD and V_{rms} difference is negligibly minimal as shown in Table 7.5. It can be seen, while increasing the number of levels, the THD of the inverter voltage decreases. In the over-modulation area, the THD increases.

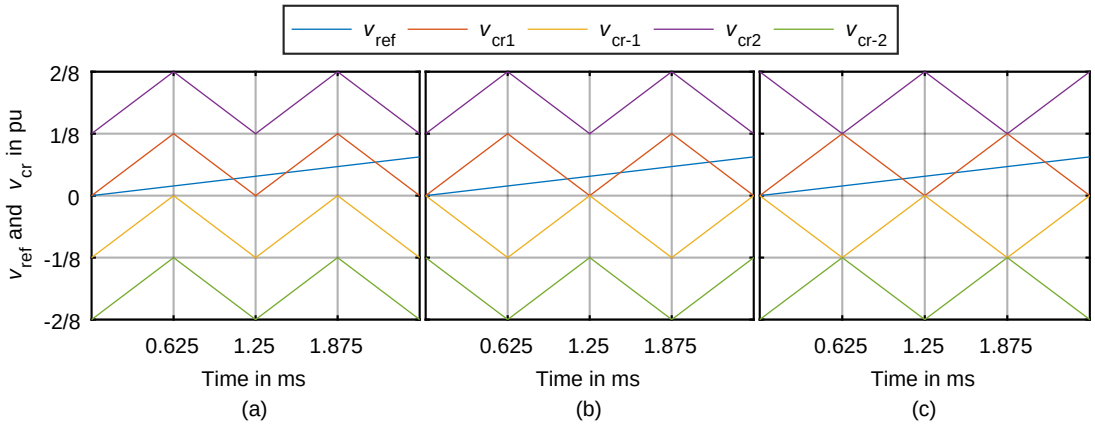


Figure 7.7 – Reference voltages and carrier-signals for the 17-level CHB inverter using (a) PD-, (b) POD-, and (c) APOD-LSPWM.

Proposed implementation While controlling the inverter, the reference voltage contains positive and negative values. Moreover, the PWM modulators deal only with positive values. To implement this, the absolute value of the sine signal is calculated and compared to the carrier-signals. The modulation is then similar to the POD-LSPWM, which represents the simplest possible modulation to be implemented for the multilevel CHB inverter. All carrier-signals must be synchronized to each other and only shifted in their level. The reference signal of the controller is multiplied by the number of used submodules to reach all carrier-signals. This implementation can be reached using the following possibility to reduce the number of required carrier-signals.
Instead of shifting the carrier-signals in their levels, the presented method for the implementation is based on POD-LSPWM and uses only one carrier-signal while multiplying the reference signal with the number of used submodules. The POD-LSPWM allows a shifting in reference signals by using only one carrier-signal as presented in Fig. 7.8.
The carrier-signal's value range is between $0 - 100\,\%$. The usage of only one carrier-signal avoids any possible synchronization fault between the carrier-signals.
One the other side, the reference signal is segmented in sections depending on the number of submodules. In the case of the selected 17-level CHB inverter, the reference signal is multiplied by eight. The reference signal is then cut in different levels and placed in the carrier-signal's values range as shown in Fig. 7.8. The different submodules' reference signals $v_{\mathrm{ref1-8}}$ are compared with the carrier-signal to generate the pulses for the H-bridge inverters. The signal v_{ref1} is compared to the carrier-signal and the PWM signals are forwarded to the first submodule. The other submodules are controlled in similar way. From the submodules' reference signals, it can be seen, that the H-bridge inverters operate for different time periods. The proposed modifications made in the reference signal are easy to implement in the simulation and the hardware. It is the simplest compared to other discussed carrier based modulation techniques and delivers similar CHB inverter voltage using the multiple carrier-signals shown in Fig. 7.7.
Using the proposed method, the resulting CHB inverter output voltage is presented in the top-part of Fig. 7.9. It is comparable to the output voltage using PSPWM, hence the switching frequency is $f_{\mathrm{sw,CHB}} = 8$ kHz. In the bottom-part of Fig. 7.9, the submodules' output voltages are shown. The first submodule switches at the start of the period and stays on

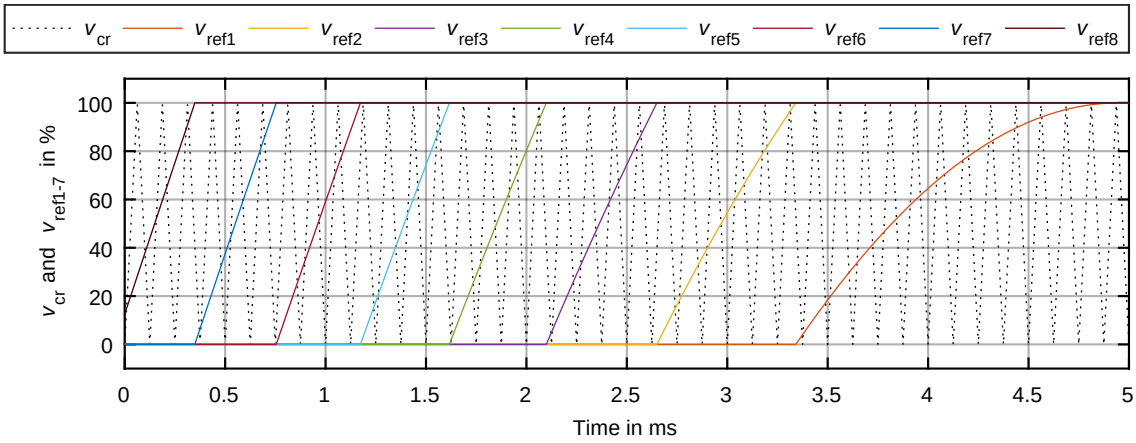


Figure 7.8 – Reference voltages and carrier-signals for the 17-level CHB inverter using the proposed method to implement POD-LSPWM.

when the reference signal is higher than its carrier-signal. This leads to a variable submodules' switching frequency during the whole inverter operation time. The first submodule operates in over-modulation and operates for longer time period than all upper submodules. Therefore, its battery module is discharged quicker.

Advantages The implementation of POD-LSPWM using a shifting in the reference signal represents the most easy implementable modulation technique. It requires one modulator at high number of PWM outputs, which is related to the number of power switches used in the inverter. For this method, there is no limits for the number of used submodules. The limitation is only given by the used control unit, which generates the PWM signals.

Disadvantages The unequal on and off switching times of each submodule leads to significantly different discharging of the battery modules. This effect is detailed in the next chapter while using simulations on system-level. However, it can be seen from the bottom-part of Fig. 7.9 that the voltage-time surface of each submodule is different. The surfaces under the voltages in the bottom-part of Fig. 7.8 are different. The battery modules operate for different time periods and are unequally discharged. The requirements in the used EMS are higher compared to the PSPWM.
Furthermore, the carrier frequency required to be used with LSPWM is higher than the PSPWM to reach similar inverter voltage frequency.
The implementation of APOD-LSPWM requires similar performances in terms of shifting the carrier-signal as the PSPWM and is then the most sophisticated. The requirements on the control unit are the highest compared to PD-, POD-LSPWM, and PSPWM.
In the hardware implementation, the power inverter requires gate drivers to switch on and off the power devices. The bottom power semiconductor of each half-bridge is switched simultaneously with the upper one. To switch the upper MOSFET, a bootstrap circuit is required. One of its parts is the bootstrap capacitor. Its size depends on the switching frequency. Using a non-constant switching scheme as shown e.g. in the output voltage of submodule one, one upper and one lower MOSFET are switched on during the on time where the H-bridge inverter is over-modulated. To switch the upper MOSFET, the control voltage needed is delivered

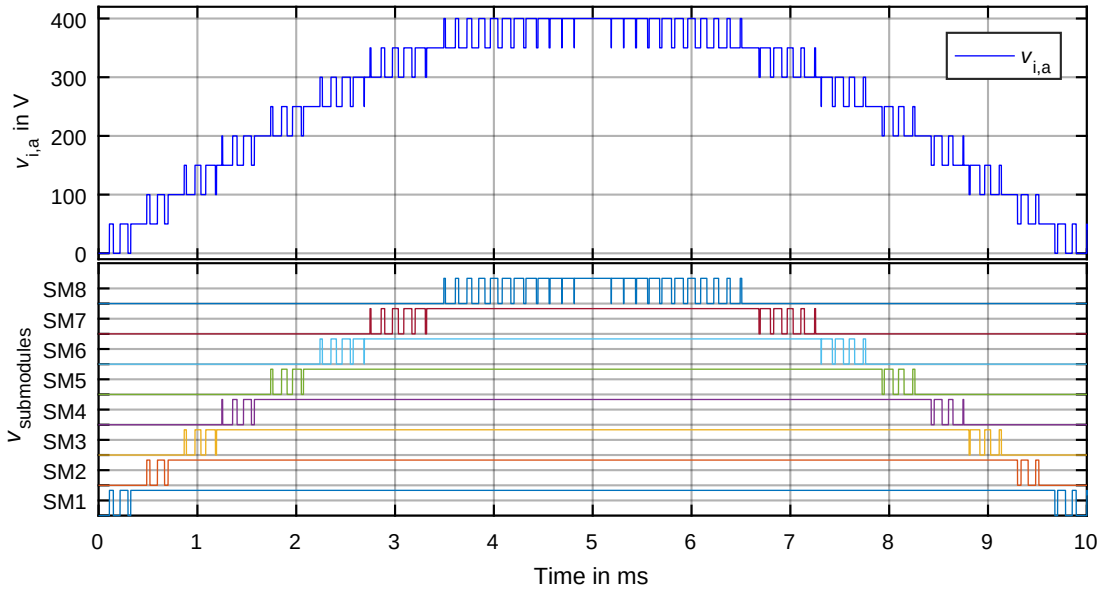


Figure 7.9 – CHB inverter and submodules voltages using LSPWM.

by the bootstrap capacitor. Therefore, the sizing and the design of this bootstrap capacitor should consider this worst case scenario and the capacitor should be designed big enough. The other possibility to operate the hardware of the H-bridge inverter is the usage of independent and galvanic isolated voltage sources for the upper power switch's gate driver which leads to increased submodule volume and costs.
Using LSPWM, the submodules operate at different frequencies as shown in Table 7.6. The different switching schemes lead to unequal power dissipation and therefore different efficiencies of each submodule. The resulting CHB inverter efficiency calculation gets more complex. Table 7.6 represents the counted switching frequencies of the submodules in the state shown in Fig. 7.6 and Fig. 7.9. In case of PSPWM, all submodules are switching at 1 kHz. Using LSPWM, the eighth submodule's switching frequency is 2.5 kHz where the first submodule's switching frequency is 0.5 kHz. These frequencies are derived by counting the switching of each H-bridge inverter presented in Fig. 7.5 and Fig. 7.8. However, these equivalent switching frequencies significantly vary in case of LSPWM depending on the amplitude modulation index m_{amp} and the battery modules' voltages.
The carrier-based modulation techniques are presented and compared to each other. In the next section, the modulation techniques shown operate without modulators.

7.4.3 Nearest Level Control

The NLC method generates the pulses or rather the inverter switches' states depending on the actual value of the reference signal. In contrast to PSPWM and LSPWM, the NLC operates without the need of carrier-signals. Its operation is comparable to the SVM, but based on the time domain. This method is known as round method and uses a rounding operator which compares the input signal and rounds it to switch on or off the next voltage level steps as shown in Fig. 7.10. The function $roundx$ delivers the closest integer number to x. As its names indicates, NLC computes the switching states depending on the value of the reference signal.

Table 7.6 – Equivalent switching frequencies of the CHB inverter and its submodules using PSPWM and LSPWM.

	$f_{\mathrm{sw,PSPWM}}$	$f_{\mathrm{sw,PD-LSPWM}}$
Inverter	8 kHz	8 kHz
Carrier frequency f_{cr}	1 kHz	8 kHz
SM1	1 kHz	0.5 kHz
SM2	1 kHz	0.5 kHz
SM3	1 kHz	0.7 kHz
SM4	1 kHz	0.7 kHz
SM5	1 kHz	0.7 kHz
SM6	1 kHz	0.9 kHz
SM7	1 kHz	1.1 kHz
SM8	1 kHz	2.5 kHz

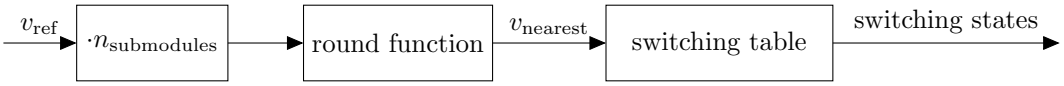


Figure 7.10 – Block diagram of NLC.

During its operation, NLC selects the nearest voltage level to the reference value. Fig 7.10 represents the block diagram of the NLC. The controller's reference signal v_{ref} is multiplied with the number of submodules to scale its amplitude as done in the case of the LSPWM. Whenever the reference signals reach a certain value, the next submodule is switched on to deliver the DC-link voltage. Therefore, the modulation is called nearest level control.

In Fig 7.10, the round function rounds its input values and delivers the signal v_{nearst}, which is forwarded to a switching look-up table already placed in the software. Finally, the state of all CHB inverter's switches is changed or rather updated once every sampling period.
In case of the 17-level CHB inverter, the NLC multiplies the reference signals with eight. The output is rounded into an integer value and changes the switching states of the whole inverter. The switching table is stored in a look-up table to change the switching state of the inverter. Using NLC, the resulting 17-level CHB inverter voltage $v_{\mathrm{i,NLC}}$ is shown in Fig. 7.11. Thereby, the reference signal v_{ref} is an idealized sinusoidal. Depending on the reference signal's amplitude, the times for switching the voltage steps significantly differs. This behavior is similar to that using the LSPWM.

Advantages The main advantage of NLC is its conceptual and implementation simplicity and the inverter efficiency.

Disadvantages The working principle of the NLC leads to similar results regarding the discharging of the battery modules as in the case of LSPWM.
The operation at low switching frequency, the DC-link capacitance should be high sized as

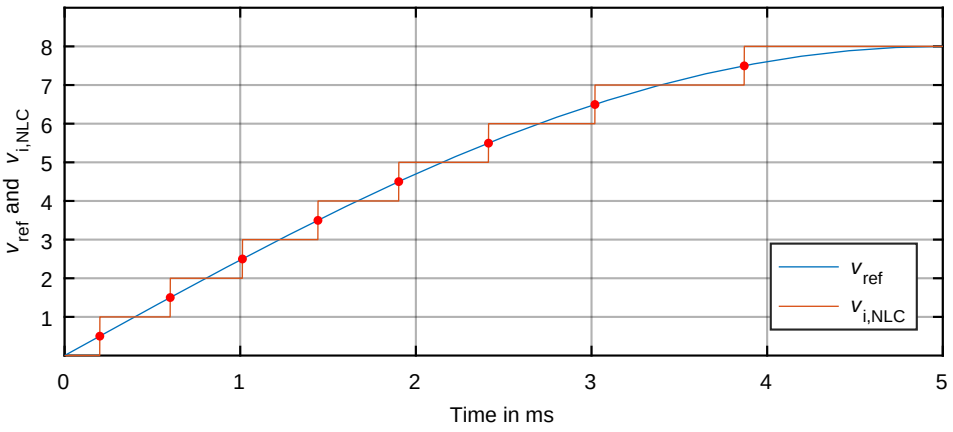


Figure 7.11 – Output inverter voltage at a given reference signal using NLC.

discussed in the case of PSPWM.
Since no modulator is used, the switching frequency of the CHB inverter's voltage is not constant. The CHB inverter voltage's switching frequency depends on the PI-controller parameters and the sampling frequency of the software.

7.4.4 Space Vector Modulation

The results discussed in this section are published previously in [102]. The space vector modulation is a form of PWM proposed in the mid- 1980s [64]. It offers significant advantages over the classical PWM in terms of performance, ease of implementation, and higher DC-link voltage utilization [64]. For multilevel inverters, carrier based modulation techniques are mostly used. Whenever, high DC-link voltage utilization is required, the space vector modulation can be used. However, this feature is not important in grid connected application due to the given AC voltage by the power grid.
As its name indicates, the SVM operates with the principle of representing the three-phase system in one vector in the space. When the reference vector falls into a hexagon, the corresponding vectors will be generated by the inverter as shown in Fig. 7.12.
Fig. 7.12 represents the space vector diagram of the selected 17-level CHB inverter. Generally, the inverter's reference voltage is represented as a vector. The SVM generates the reference vector as a combination of the three closest possible switching inverter's voltage vectors. The SVM generates the reference signal v_{ref} using a linear combination of the closest state space vectors marked in red in Fig. 7.12. In order to achieve the reference signal, Eq. (7.3) describes the switching times of the used space vectors to achieve the reference voltage. Thereby, $T_{\mathrm{sw}} = t_1 + t_2 + t_3$ is a switching period.

$$v_{\mathrm{ref}} = \frac{1}{T_{\mathrm{sw}}} \cdot (t_1 v_1 + t_2 v_2 + t_3 v_3) \tag{7.3}$$

Using the SVM in an n-level inverter leads to n^3 switching states, $6 \cdot (n-1)$ triangles, and $1 + 6\Sigma_{i=1}^{n-1} i$ switching vectors in the space vector diagram [31],[35]. Table 7.7 represents the switching data for different inverter output voltage levels. By increasing the number of levels,

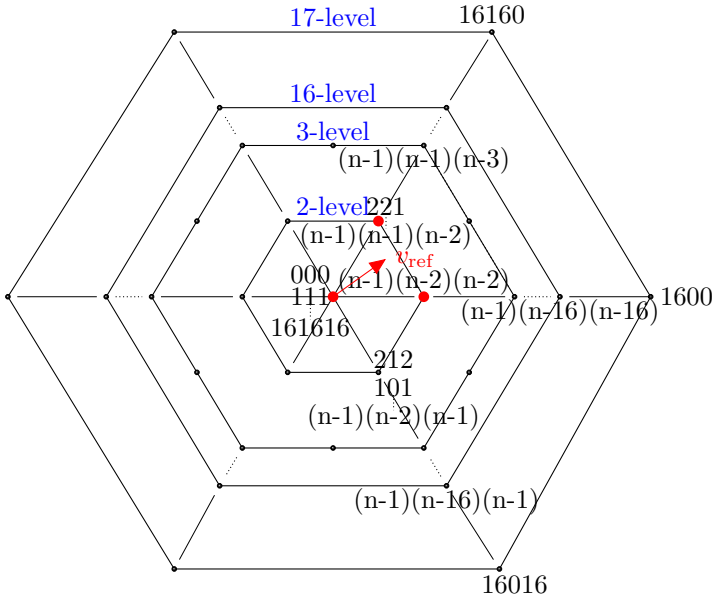


Figure 7.12 – Space vector diagram of the 17-level CHB inverter.

Table 7.7 – Switching values for different inverter output voltage levels using SVM.

	2-level	3-level	5-level	7-level	17-level
Switching states	8	27	125	343	4913
Switching vectors	7	19	61	127	817
Triangles	6	24	96	216	1536

the switching states and vectors significantly increase compared to the two-level inverter. Instead of eight switching states and seven switching vectors in the two-level inverter, the 17-level CHB inverter needs 4913 switching states and 817 switching vectors. The number of triangles required increase from six to 1536 when 17 levels instead of two levels are used. Therefore, the system complexity using the SVM for the 17-level inverter increases.
The switching vectors are lower in comparison to the switching states, because when increasing the level number, the rest of switching vectors are redundant vectors. As a result, the inverter using higher number of levels contains a large number of space vectors. The greater redundancy offered can impose massive computational overheat if not optimized [65].
SVM algorithms have been introduced in [6]. They are categorized into three parts. The first one selects the switching states or vectors for modulation. Usually, these are the vectors closest to the reference. The second category computes the duty cycles of each vector to achieve the desired reference over a modulation period. The third category decides the sequence, in which the vectors are generated.
The presented categories differ mainly in how the vectors are chosen, how the on and off times are computed, which are the sequences used to generate the vectors, and finally in the computational effort required while implementing the SVM.

Advantages The SVM treats the whole converter as one unit. This technique directly controls the CHB inverter's line-to-line voltages in a two-dimensional $\alpha\beta$-reference system [117], while carrier-based PWM deals with the phase voltages.
The SVM delivers the same results in terms of THD_i compared to carrier based PWM in three-phase inverters [6] and [144].
The SVM has different advantages against the carrier based modulation techniques. Therefore, it is desirable in many industry applications, where higher fundamental output voltage is needed. It offers better utilization of the DC-link voltage and higher fundamental output voltage compared to the carrier-based PWM [6], better dynamic response [76], and reduced switching losses [137]. Furthermore, it extends the flexibility to utilize switching states for minimizing switching frequency, harmonics and current ripples [120].

Disadvantages Generally, the SVM is characterized by a more complex implementation than carrier based modulation techniques [117].
The usage of SVM promises different advantages against carrier based PWM. However, using this method for the selected 17-level inverter, the switching tables used contain a high number of vectors and the system complexity increases.
The implementation of the SVM leads to similar results concerning the SoC of the used battery modules in the CHB inverter as in LSPWM and NLC. The battery modules are unequally discharged due to the space vector diagram structure [102]. This affects not only the battery lifetime, but also the operation time of the inverter if no EMS is used. In the case of the selected 17-level CHB inverter, the shift in the modules' SoC leads to an interruption of the BESS operation because the first submodule's SoC reaches 0 % where the eighth submodule's SoC is at 100 % as nearly discussed in the next chapter. Furthermore, the usage of more complex balancing algorithms is required.

Table 7.8 – Comparison of the presented modulation techniques for CHB inverter.

Modulation technique	Switching frequency	Conduction period	Switching losses	Total switching losses
PSPWM	low	same for all submodules	same for all submodules	low
LSPWM	high	Different	Different	High
SVM	High	Different	Different	High
NLC	Low	Different	Different	Low

7.4.5 Conclusion

Within this section, the modulation techniques to be used in the selected one-stage 17-level CHB inverter are presented and their advantages and disadvantages are shown. The extension of traditional modulation techniques to be used in multilevel inverter topologies increases their complexity and allows an extra degree of freedom provided by having more power semiconductors and additional switching states. The presented modulation techniques differ in their features and drawbacks.
In [92] an analysis of the modulation methods used in CHB inverters in terms of their losses is presented. Table 7.8 shows a brief comparison derived from [92]. It is clear, that the PSPWM offers superior advantages compared to the LSPWM, NLC, and SVM.
Generally, the carrier based modulations are preferred, due to the resulting constant inverter switching frequency and easy implementation.
All presented modulation techniques, except the PSPWM, lead to an unequal discharge of the battery modules, unequal switching schemes for the H-bridge inverters, and different power dissipation in the submodules. However, they are simple to implement compared to the PSPWM. Especially, the LSPWM using the proposed implementation method is the easiest in the implementation and represents a good opportunity to shorten the realization time.
In contrast, the PSPWM uses lowest carrier frequency and therefore the CHB inverter's efficiency increases. For efficient BESS, the PSPWM offers more advantages against the LSPWM. Moreover, losses are found to be 96 % lower compared to the LSPWM as shown in [136] with the recommendation of the usage of this modulation because its overall performance is superior.

Because the efficiency of BESS is important, the PSPWM overall performance is superior and recommended to be used in BESS.
In the next section, the power filter is designed to minimize the grid distortion based on the recommended modulation technique. After this, all modulation techniques presented within this section are simulated using the weak grid model and compared to each other.

7.5 Power Filter Design

The inverter voltage is non sinusoidal due to the inverter switching operation. The inverter voltage contains a wide range of harmonics at an integer multiple of the fundamental frequency. These distortions bring undesirable effects to electrical equipments connected to the voltage

source inverter and should be filtered and kept under given norm-limits. The power filter is used to minimize the effects of the inverter's pulse width modulated voltage on the grid. It's necessary for all grid connected inverters including multilevel inverters.
The power filter design presented in this section is partially published previously in [93]. The results here are different due to the different grid parameter, which are a very important part for harmonic spectrum calculation by investigating the results. The used grid model is a weak grid as selected before.
Furthermore, this section differs from the publication [93] in terms of switching frequency of 8 kHz and the nominal power of the studied inverter due to the current limitation of the used battery modules. The inverter nominal power is 17.64 kW instead of 36 kW in [93].
Using simulations on circuit-level, the inverter dynamic is modeled. Therefore, it is possible to design the power filter. The field of active power filter is increasing and gives better results than using passive filters. However, the usage of CHB inverter minimally affects the grid compared to the two-level topology. Hence, only passive filters are considered.
In [93], an algorithm to minimize the size of the filter's inductance is proposed. The design is made using the current ripple method and the filter's inductance is minimized using an iteration design algorithm. Within this section, only the current ripple method is discussed.
For the CHB inverter, an LCL-filter design is previously presented in [93] and [139]. In [93], the filter design for an L and LCL-filter for both of B6-bridge and CHB inverter is discussed. There are many strategies presented to design an LCL power filter. The current ripple calculation method is presented in [111], the iterative algorithms as in [41], [75], [140], and [146], and the power losses optimization as shown in [128]. The main disadvantage of using more than one non-linear element in the filter is the resonance frequency. To avoid these resonances, the high order filters, like LC-, LCL-, and LLCL-filter, require damping. For this purpose passive methods are well suited for stiff grid applications [182], [184]. These methods offer good performance with low complexity and cost. Furthermore, using additional components increases the losses in the power filter as shown in [140] and [181].
In [93], it is found out that only an inductor is enough for standard-conform inverter operation on the power grid. Therefore, in this section only the L-filter design is pointed out and discussed to be used in the selected 17-level CHB inverter and to compare the multilevel topology advantages against the two-level inverter.
The grid code presented previously allows certain maximal values for the THD. At nominal power, the maximal allowable current and voltage THD is 5 %. In the entire inverter operation range, it must be kept less than 8 %.
An inductor is the simplest configuration of a possible passive power filter to be used for harmonics mitigation. The filtering is made using an inductor, which contains an internal resistor due to its windings. The equivalent circuit of the power filter is shown in Fig. 7.13 and contains the equivalent series resistance R_L.
As a first order filter the attenuation is ideally 20 dB/decade. By increasing the switching frequency, the inductors become smaller and the losses in the inverter's power switches increase. Therefore, a compromise between switching frequency and filter size should be found. Due to its internal resistance, a voltage-drop over the filter exists. Using Kirchoff's voltage law gives Eq. (7.4).

$$v_{\mathrm{g,a}}(t) = v_{\mathrm{i}}(t) - (R_L + jwL_L) \cdot i_{\mathrm{a}}(t) \tag{7.4}$$

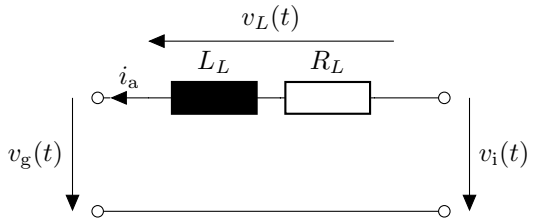


Figure 7.13 – Equivalent circuit of a power filter.

At high frequencies, the grid can be seen as a short circuit [111]. Therefore, from Eq. (7.4), the transfer function of the power filter can be expressed as in Eq. (7.5).

$$G_L = \frac{I_\mathrm{a}(s)}{V_\mathrm{i}(s)} = \frac{\frac{1}{R_L}}{s\frac{L_L}{R_L} + 1} \tag{7.5}$$

At high frequencies, the filter impedance rises and can be seen as an open circuit, so that the higher order frequencies are filtered.

The filter's inductance determines the current ripple produced by the inverter. These current ripples depend on the inverter operation and control. They are defined by the difference between the peak volt-seconds and the average volt-seconds applied to the inductor. As the filter is not an ideal inductance, it contains an inner resistance. The inductor's internal resistance depends on a series of factors such as the core material or operating temperature. In [165] and [180], two filter's inductance values of 3 mH and 1.8 mH with internal resistances of 30 mΩ and 16 mΩ are used, respectively. In this section the value of the internal filter resistance is set to $R_L = 12\,\mathrm{m\Omega}$, which is measured in a real inductor with an inductance of $L_L = 0.98\,\mathrm{mH}$, which is used later in the hardware validation section. While designing the power filter, both inverter topologies are considered, with the aim of comparing both topologies in size and grid effects and to highlight the requirement of the 17-level CHB inverter against the two-level B6-bridge inverter topology. To get similarity in the comparison, the inverter switching frequency at the connection point to the power filter is kept at 8 kHz using both inverter topologies.
In order to define the ripple on the filter, Fig. 7.14 represents the current ripple in the inductor in case of the B6-bridge and CHB inverter. Thereby, T_on is the switch on time, T_sw is the switching period, $v_\mathrm{g,a}$ is the grid voltage, v_B6 is the B6-bridge inverter voltage, and v_CHB is CHB inverter's voltage.
In the worst case scenario, the DC-link voltage is at its maximum. Furthermore, the maximum ripple occurs when the duty cycle is set to 50 % ($D = 0.5$). In this case, the average volt-seconds is equal to zero. In order to define the filter inductance value using the worst case, the voltage drop across the inductor is given by Eq. (7.6).

$$L \cdot \frac{\Delta I_L}{T_\mathrm{on}} \;=\; v_\mathrm{CHB} - v_\mathrm{g,a} \tag{7.6}$$

The definition of the allowed current ripple ΔI_L is shown in Eq. (7.7).

$$\Delta I_L \;=\; \frac{(v_{CHB} - D \cdot v_\mathrm{CHB}) \cdot D \cdot T_\mathrm{sw}}{L_L} \tag{7.7}$$

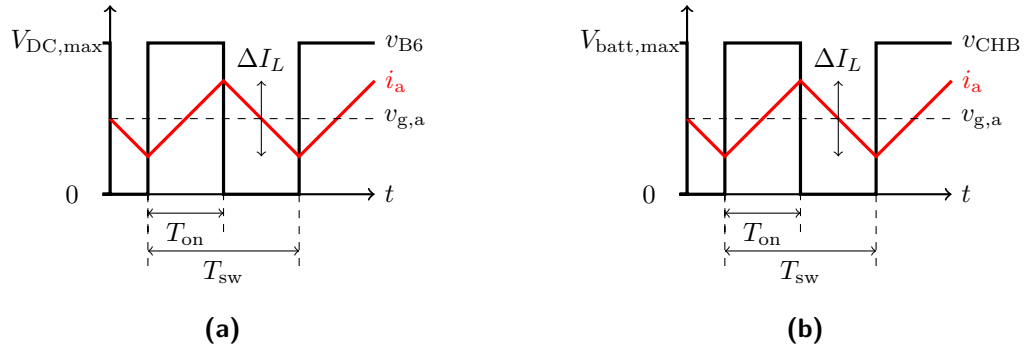


Figure 7.14 – Inductor's current ripple in case of (a) the B6-bridge and (b) CHB inverter [93].

Finally, the power filter's inductance can be calculated using Eq. (7.8).

$$L_L = \frac{v_{\mathrm{CHB}} \cdot D \cdot (1-D)}{f_{\mathrm{sw}} \cdot \Delta I_L} \tag{7.8}$$

In the worst case scenario, the peak current ripple on the inductor $\Delta I_{L,\mathrm{max}}$ is at its maximum. This value is defined by the difference between the peak volt-seconds and the average volt-seconds applied to the inductor [139].
Using stacked battery modules in the B6-bridge inverter's DC-link and the CHB inverter, the voltage depends on the battery modules' SoC. The current ripple method considers the fully charged state where the battery module's voltage is at its maximum. Therefore, as shown in Fig. 7.14, the B6-bridge and CHB inverter's voltage ripples are at $D = 0.5$ and $V_{DC,max}/2$ and $V_{\mathrm{batt,max}}/2$, respectively.
The maximal peak current ripple on the inductor $\Delta I_{L,\mathrm{max}}$ is set at 5 % of the peak current. Considering the battery maximal current of $I_{\mathrm{batt,max}} = 36\,\mathrm{A}$, the current ripple of 5 % is equal to $\Delta I_{L,\mathrm{max}}$ of 1.8 A.
The Eq. (7.9) gives a filter's inductance of 13 mH for the B6-bridge inverter by considering a maximal DC-link voltage of 750 V. Using Eq. (7.10), the inductance of the CHB inverter's filter is 0.99 mH, considering a maximal submodules' battery module voltage of 57 V.

$$L_{\mathrm{B6}} = \frac{T_{\mathrm{sw}}}{2} \cdot \frac{V_{\mathrm{DC,max}}}{2} \cdot \frac{1}{\Delta I_{L,\mathrm{max}}} = 13\,\mathrm{mH} \tag{7.9}$$

$$L_{\mathrm{CHB}} = \frac{T_{\mathrm{sw}}}{2} \cdot \frac{V_{\mathrm{batt,max}}}{2} \cdot \frac{1}{\Delta I_{L,\mathrm{max}}} = 0.99\,\mathrm{mH} \tag{7.10}$$

The CHB inverter's filter inductance is lower than that of the B6-bridge inverter due to the low voltage steps of the CHB inverter. Using the internal resistance of the hardware reference filter gives an internal resistance of 159 mΩ and 12.1 mΩ for the B6-bridge and CHB inverter, respectively. The increased internal resistance of the used B6-bridge inverter's filter leads to higher losses.
One other method to design the power filter presented in [86] and [113]. It considers a filter's inductance of 10 % of the inverter's base inductance. This is calculated using Eq. (7.11) and Eq. (7.12).

$$Z_{\mathrm{b}} = \frac{V_{\mathrm{rms}}}{I_{\mathrm{rms}}} \tag{7.11}$$

Table 7.9 – Power filter parameter designed with the current ripple method.

Parameters	B6-bridge inverter		CHB inverter	
Switching frequency f_{sw} in kHz	8		1	
Reference value for I_{d} in pu	0.5	1	0.5	1
Inductance L_L in mH	13		0.99	
Resistance R_L in mΩ	159		12.1	
THD_v in %	0.09	0.12	0.03	0.03
THD_i in %	1.56	1.06	0.20	0.11

$$L_{\mathrm{b}} = \frac{10\,\% \cdot Z_{\mathrm{b}}}{2\pi \cdot f_{\mathrm{n}}} \tag{7.12}$$

The calculated resistance of the power filter is given in Eq. (7.13).

$$R_{\mathrm{b}} = 0.05 \cdot Z_{\mathrm{b}} \tag{7.13}$$

A similar method presented in [185] uses 5 % of the inverter's base inductance. However, these methods show higher values for the filter's inductance and resistance and are therefore not further followed.
Table 7.9 represents the results using the filter parameters calculated, using the current ripple method and an inverter voltage switching frequency of 8 kHz. The THD is given at two inverters operation points, at half and at nominal active power. The slightly higher THD using the CHB inverter is due to the usage of smaller power filter compared to the B6-bridge inverter. However, both of the THDs are under the norm-limits. Using the filter parameter of the CHB inverter with the B6-bridge inverter leads to THD_i and THD_v of 13.05 % and 5.22 %, respectively. These values are higher than the norms-limits.
Within the above section, the design of an inductor as a power filter for the grid connected B6-bridge and 17-level CHB inverter is presented. The filter requirements for the CHB inverter are lower than the usage of B6-bridge inverter. Further, the current ripple method represents a simple but reliable method to calculate the inductance of the power filter. The current ripple method delivers satisfying and standard-conform results. The results have shown that the L-filter succeeded in mitigating the harmonics for both inverters.
In the next section, the CHB inverter's controller design is discussed because the parameter required, the filter and switching frequency, are defined in the previous sections.

7.6 Control Schemes

In the recent research, a stack of current control methods for grid connected inverter has been proposed in [84] and [155]. It concludes to the point, that the controller design is a trade-off between different requirements related to the system.
Within this section, two control schemes for the selected 17-level CHB inverter are shown and discussed. The well known hysteresis control, which is a modulation and control scheme, is introduced and its implementation in the 17-level CHB inverter is discussed. Furthermore, the Vector Oriented Control (VOC) for the CHB inverter is introduced. After determining the modulation and filter parameters, the controller for the VOC can be designed and the inverter operation is described and the system stability is studied. The simulation results

using different modulation techniques are then shown and compared. The inverter operation's stability using the designed controller is validated using the zero pole map. Furthermore, the system step response is analyzed using physical models on circuit-level and is validated with measurements. Even with a good controller design, the inverter responds with a current overshoot while abruptly changing the current reference value. Therefore, a simple method to totally eliminate the overshoot is proposed and validated in simulation and hardware. At the section's end, one control method to be used in BESS is recommended.

Hysteresis Control The hysteresis control represents the easiest possible control and modulation technique. It is a method used to control the current in a given hysteresis band. It operates as a modulator and controller in one. The hysteresis control is a type of non-linear control. It is based on an on-off controller for each phase [85]. The two-level hysteresis current control is based on the idea to switch on the inverter output voltage between the positive and negative DC-link voltage. The current must follow the reference current in a given hysteresis band. Whenever the current crosses or touches the hysteresis band, the inverter voltage is reversed to keep the current within the specified range. The current errors resulting from the comparison between the measured current and the reference value are controlled using hysteresis comparators. In multilevel inverters, the switching happens for each submodule in the determined current regions. The operation area of each submodule is predefined. Multi-band hysteresis modulation used to control the multilevel inverters are presented in [48], [53], [54], and [157].
In the case of the 17-level CHB inverter, 16 hysteresis bands are required to control the current. Whenever the current crosses the boundary of a submodule, the next voltage step is switched on or off when the upper or lower band limit is crossed, respectively. During the CHB inverter's operation at nominal active power, the inverter phase voltage is used as a reference value and is multiplied with the current peak value desired. This reference is divided in operation areas for each submodule. The only parameter to be set is the hysteresis band width, which defines the variation allowed in the current deviation from the reference value. Therefore, this control method is very dynamic, stable and easy to implement. The inverter operation depends significantly on the hysteresis band width. To keep the actual current in the defined hysteresis band, the inverter switching frequency can not be influenced. By connecting the inverter to the weak grid, the current variation is higher and the inverter switches often than when the strong grid model is used. It depends also on the size of the power filter used. Since the filter limits the current increase, the operation also depends on the filter's inductance value. By increasing the width of the hysteresis band, the current distortion increases. On the counter part, the switching losses increase at small hysteresis band.

The hysteresis control is simple and offers outstanding robustness. It provides extremely good dynamics, which is only limited by the switching speed and the load time constant [85].
Using grounded CHB inverter, the control of each phase current can be done independently. The hysteresis control is easy to be adapted to systems with higher number of phases such as multiphase electrical machines.

The usage of the hysteresis control leads to an undesirable variable inverter switching frequency, especially for high power applications where the multilevel inverter are usually used. The

variable switching frequency leads to a spread harmonic spectrum and different THDs at the PCC. However, efforts were made to achieve a constant switching frequency by modulating the hysteresis band as in [23] and [115]. Furthermore, the resulting switching frequency using hysteresis control depends largely on the load parameter and the comparator's hysteresis band [85]. The inverter's operation highly depends on the selected band width.
The inverter operation is somewhat rough due to the inherent randomness in parameters and comparator hysteresis band [85]. Therefore, inverter protection is required and is difficult to implement [118].
The hysteresis control is suitable for single phase systems. The control of three-phase inverter with floating neutral point leads to difficulties described in [24].
The implementation of the hysteresis control gets more complex in terms of defining the angle between the voltage and current in the case of reactive power exchange between the inverter and the grid.
Using this control and modulation technique, the battery modules are, similarly to all studied modulation techniques except PSPWM, unequally discharged. Therefore, the usage of an EMS unit is highly required.

7.6.1 Vector Oriented Control

The controller design presented within this section is published previously in [100] and [107]. The core of the operation of a grid connected inverter is its controller. The inverter's performance and operation rely primarily on the quality of the current controller. Its main function is to maintain the current through the filter at a desired value. It must be dynamic, stable, simple, and maintain the grid distortion in the given limits.
In [91], it is shown, that all CHB inverter available in the industry use the VOC also known in electric drives fields as Field Oriented Control (FOC) as control method.

The VOC requires low sampling frequency. Therefore, low cost hardware can be used [16]. The PI-controller can be easily calculated based on different approaches and delivers good performance concerning the steady-state accuracy [155]. The operation is robust against controller's parameter changes.
The VOC enables to separately control the required active and reactive power using simple mathematical transformations. The mathematical calculations allow a comprehensive representation of the measured and controlled currents.

From the control point of view, the system to be controlled consists of the power filter and the inverter time delay due to its switching operation. The system's plant is fully defined after the definition of the inverter switching frequency and its power filter parameter in Section 7.4 and 7.5, respectively. Therefore, the controller can be further designed.
On circuit-level, the controller's parameter are mathematically designed to control the current while charging or discharging the BESS. The controller design quality is important for the inverter performance. It minimizes the distortion and increases the inverter stability.
The vector oriented control method is derived from the field oriented control of electric drives, since the grid is mostly a rotating synchronous machine operating as generator. It considers several mathematical calculations to simplify the understanding of the rotating AC system's

currents and voltages. Furthermore, the VOC separately controls the active and reactive power using the Clarke- and Park-transformation. These transformations allow the control of the d- and q-components separately. Using the inverse Park- and Clarke-transformation, the reference signals for the modulators are generated. All these transformations are made using one unique transformation angle.

7.6.2 Transformation Angle

In the field oriented control, the transformation angle ϑ represents the rotor position and is given by incremental encoders. In grid connected applications, the angle ϑ delivers the actual position of the rotating dq-coordinate axes and is used to synchronize the inverter voltage to the grid voltage.
The grid synchronization plays an important role to operate the inverter using the VOC. In the field of grid connected power inverters, the power transfer requires continuous monitoring of the grid parameters such as the grid's frequency, phase angle between voltage and current, and voltage magnitude [47]. An ideal grid synchronization must precisely track the grid's phase angle, effectively detect frequency deviations, and quickly respond to the grid parameter changes [74].
The three-phase grid synchronization methods are classified as open and closed loop systems. Whereby the open loop systems detect the magnitude, frequency, and phase angle of the input signal, the closed loop systems update their results adaptively by using certain loops containing controllers.
The first proposed scheme for synchronization to the grid is an open loop phase angle estimation using Zero Cross Detector (ZCD) as introduced in [45]. However, its performance is deteriorated under polluted grid conditions. The weak grid power quality issues leads to malfunction of the ZCD based controllers [45]. Therefore, Phase Locked Oscillator (PLO) i.e. Phase Locked Loop (PLL) is introduced and developed. In recent years, many modifications and researches are invested to improve and enhance the performance of PLL to handle with polluted grid voltages. In practical implementations, the PLL is still the most employed synchronization method due to its simplicity, frequency adaptation features and versatility [47].
There are several ways to calculate the transformation angle ϑ. The comparison of the advantages and drawbacks of various synchronization methods leads to the highlighting of PLL and arctan-methods.

Phase Locked Loop The Phase Locked Loop PLL is a method commonly used to obtain the angle for the Park-transformation and the grid angular velocity ω, as i.e. in [185]. The angle ϑ is expressed as in Eq. (7.14).

$$\vartheta = \int_0^t \omega(t)dt + \vartheta_0 \tag{7.14}$$

The PLL is simple to implement, robust in its operation, and effective under various and polluted grid conditions. Nowadays, the well known PLL is widely used in industrial application, grid connected inverters, and electric drives. The main function of the PLL is based on the synchronization to the input signals in frequency or phase [50], [127]. For this purpose, it uses a

non-linear closed loop control as shown in the basic structure of a PLL in Fig. 7.15. It consists of three main components. The phase detector first detects the grid signal, mostly the grid voltage, and the output signal of the PLL. Both signals are compared to each other and the error signal is filtered using a low-pass filter. Its output signals drives the Voltage Controlled Oscillator (VCO), which delivers the required phase angle ϑ. This closed loop operates to minimize the phase angle error $\delta\vartheta = \vartheta_{\text{ref}} - \vartheta_{\text{out}}$ shown in Fig. 7.15 to zero. Whenever the zero-error is reached and $\delta\vartheta = 0$, the phase is locked.
Recent researches improved and modified the PLL to increase its reliability and exactness.

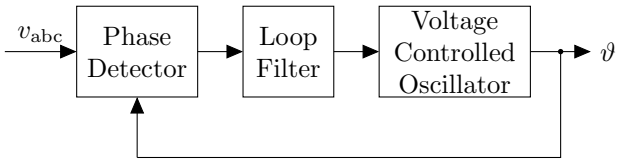


Figure 7.15 – Structure of non-linear closed control loop in PLL.

Further methods like enhanced PLL, synchronous reference frame PLL, fixed reference frame PLL, and variable sampling period filter PLL are presented in [73]. These methods differ in the implementation of the phase detector block. However, the additional improvement are not required in the field of grid connected inverters. Therefore, the classical PLL is used for further transformation angle's calculation.

Low-Pass Transformation Angle Detector The next method, which is simpler to be implemented in the hardware of grid connected inverter is the $\alpha\beta$-filter algorithm. However, the low-pass transformation angle detector operates as an open loop system. This method enables the synchronization with the positive sequence fundamental vector of the three-phase input signal and was firstly introduced in [164].
This method represents a good digital alternative to the PLL in good grid conditions. As mentioned before, the open loop methods offers limited performance under polluted grid conditions. Under good grid conditions, the voltage distortion is low and the operation is possible without low-pass filtering using only the arctan-function.
The low-pass transformation angle detector uses the Clarke-transformation of the three-phase system. This transformation and its equations are explained later within this section.
Eq. (7.15) shows the arctan-function used. The data points of this function are stored in look-up tables in the microcontroller. It is also possible to use the four-quadrant inverse tangent function atan2 presented in [45].

$$\vartheta = \arctan\left(\frac{v_\beta}{v_\alpha}\right); \quad \vartheta \in [-\pi, \pi] \tag{7.15}$$

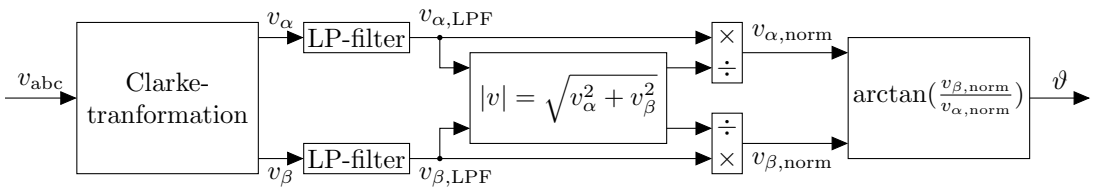


Figure 7.16 – Low pass transformation angle detector scheme [164].

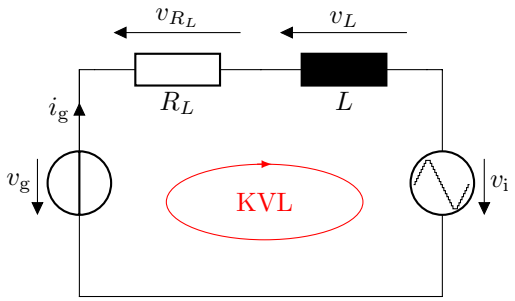


Figure 7.17 – Single phase equivalent circuit of the CHB inverter connected to the grid through L-filter.

The used low-pass filter helps in case of possible grid distortion on the grid. However, using the low-pass filtering, the system response of the controller gets slower. Therefore, this filter must be designed carefully to limit this resulting delay. Ideally, this delay should be compensated, which increases the system complexity while implementing the low-pass filter.
This method operates without sequence decoupling. Whenever a good decoupling and filtering scheme are used, the Low-Pass Transformation Angle Detector (LP-TAD) with atan2 function seems to be a good alternative to the PLL. Using the filtering, the dynamic response of the LP-TAD can be enhanced using various types of filter i.e. stochastic and or recursive filter such as space vector filter- or enhanced Kalman filter-TAD mentioned in [164] and [167]. Finally, this method can be extended to deal with unbalanced grid conditions [45] using the normalized positive sequence synchronous frame proposed in [28].

Recommendation The ZCD represents the simplest and easiest method in the implementation. However, it operates with reduced exactness under polluted grid conditions. PLO based controller are more robust against distorted grid voltage and operate with higher reliability. However, their design remains complex and requires higher computational power compared to ZCD methods.
In the implementation of the 17-level CHB inverter, the transformation angle ϑ is calculated using both of the two methods. The PLL and the arctan-function allow a synchronization and grid operation during the simulations and measurements without any difference between the quality of the voltage and current.
In the further controller design step, the plant is mathematically defined and the required transformations are further explained to enable the controller parameter calculation.

7.6.3 Plant Definition

The CHB inverter is connected to the grid using a power filter. Fig. 7.17 shows a single phase representation of the CHB inverter to explain the plant identification using Kirchhoff's Voltage Law (KVL) and initiate the controller design. Thereby v_g represents the grid voltage of one phase, v_i the CHB inverter output voltage, i the three-phase current, and L_L the filter inductance considering its internal resistance R_L.

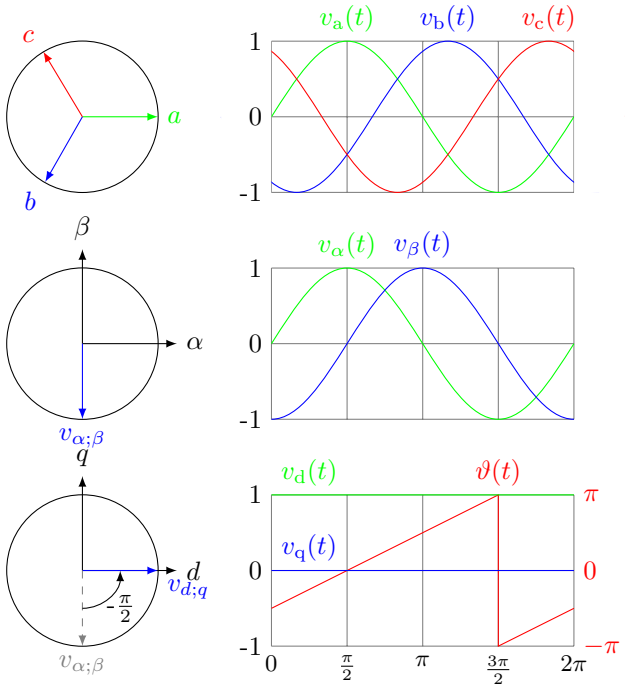


Figure 7.18 – Clarke- and Park-transformation in space and time domain.

Coordinate Transformations Applying the KVL in Fig. 7.17, the voltage mesh delivers the relation shown in Eq. (7.16).

$$v_\mathrm{g} = v_\mathrm{i} - L_L \frac{\mathrm{d}i_\mathrm{g}}{\mathrm{d}t} - R_L i_\mathrm{g} \tag{7.16}$$

The coordinate transformations are used to simplify the expression of the value in the abc-frame and therefore simplify the analysis of three-phase systems, such as electrical machine and grid connected three-phase circuits. These transformations describe the system using $\alpha\beta$– and dq–coordinate system using the Clarke and Park-transformations, respectively.

Overview The mentioned transformations can be summarized in space and time domain in Fig. 7.18. On the left side, the space vectors are shown in the abc-, $\alpha\beta$-, and dq-reference frames. On the right side are the corresponding time value to the vectors.

The Clarke-Transformation The Clarke-transformation describes the abc-reference values, i.e. voltage, current or flux in $\alpha\beta$-reference frame as shown in Eq. (7.17). It is used to transform the abc-reference frame in a stationary $\alpha\beta$-reference frame [39].

$$\begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix} = \frac{2}{3} \begin{bmatrix} \cos(0) & \cos(\frac{-2\pi}{3}) & \cos(\frac{2\pi}{3}) \\ \sin(0) & \sin(\frac{-2\pi}{3}) & \sin(\frac{2\pi}{3}) \end{bmatrix} \begin{pmatrix} x_\mathrm{a} \\ x_\mathrm{b} \\ x_\mathrm{c} \end{pmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{pmatrix} x_\mathrm{a} \\ x_\mathrm{b} \\ x_\mathrm{c} \end{pmatrix} \tag{7.17}$$

Using the factor 2/3, the amplitudes of $\alpha\beta$-components and the abc-values remain identical. Using $\sqrt{2/3}$ instead of this the powers in the AC- and DC-side are similar. The resulting values of $\alpha\beta$-components have a shift of 90° and are rotating with the grid frequency.

The Clarke-Transformation Using Line-to-Line Values In practical applications, three-phase inverters use only three wires. Therefore, the calculation shown in Eq. (7.17) can not be used. The alternative is shown in Eq. (7.18) [161] and uses only two ac-values due to the assumed symmetric grid voltages. Using line-to-line values, sensing voltage in the grid connected inverter requires less voltage sensors (two instead of three). However, the reduction of the system component increases the failure probability and decrease the system reliability.

$$\begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix} = \begin{bmatrix} \frac{2}{\sqrt{3}} & \frac{1}{\sqrt{3}} \\ 0 & 1 \end{bmatrix} \begin{pmatrix} x_{\mathrm{ab}} \\ x_{\mathrm{bc}} \end{pmatrix} \tag{7.18}$$

To normalize the resulting vector, a multiplication with the factor $\frac{2}{3\sqrt{3}}$ is needed.

The Inverse Clarke-Transformation

$$\begin{pmatrix} x_{\mathrm{a}} \\ x_{\mathrm{b}} \\ x_{\mathrm{c}} \end{pmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix} \tag{7.19}$$

The inverse Clarke-transformation is represented in Eq. (7.19).

The Park-Transformation The rotating and time variant $\alpha\beta$-components are transformed using the transformation angle ϑ into time invariant dq-components. The Park-transformation can be used to express the $\alpha\beta$-components in the rotating reference frame, i.e. dq-components [138] as shown in Eq. (7.20).

$$\begin{pmatrix} x_{\mathrm{d}} \\ x_{\mathrm{q}} \end{pmatrix} = \begin{bmatrix} \cos(\vartheta) & \sin(\vartheta) \\ -\sin(\vartheta) & \cos(\vartheta) \end{bmatrix} \begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix} \tag{7.20}$$

$$\tag{7.21}$$

There is also a possibility to transform the abc-frame directly into the dq-frame using the matrix in Eq. (7.22) as mentioned in [17].

$$\begin{pmatrix} x_{\mathrm{d}} \\ x_{\mathrm{q}} \end{pmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\vartheta) & \sin(\vartheta) \\ -\sin(\vartheta) & \cos(\vartheta) \end{bmatrix} \begin{bmatrix} \cos(0) & \cos(\frac{-2\pi}{3}) & \cos(\frac{2\pi}{3}) \\ \sin(0) & \sin(\frac{-2\pi}{3}) & \sin(\frac{2\pi}{3}) \end{bmatrix} \begin{pmatrix} x_{\mathrm{a}} \\ x_{\mathrm{b}} \\ x_{\mathrm{c}} \end{pmatrix} \tag{7.22}$$

$$\begin{pmatrix} x_{\mathrm{d}} \\ x_{\mathrm{q}} \end{pmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\vartheta) & \cos(\vartheta - \frac{2\pi}{3}) & \cos(\vartheta - \frac{4\pi}{3}) \\ -\sin(\vartheta) & -\sin(\vartheta - \frac{2\pi}{3}) & -\sin(\vartheta + \frac{4\pi}{3}) \end{bmatrix} \begin{pmatrix} x_{\mathrm{a}} \\ x_{\mathrm{b}} \\ x_{\mathrm{c}} \end{pmatrix} \tag{7.23}$$

The Inverse Park-Transformation The inverse Park-transformation corresponding to Eq. (7.20) is represented in Eq. (7.24).

$$\begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix} = \begin{bmatrix} \cos(\vartheta) & -\sin(\vartheta) \\ \sin(\vartheta) & \cos(\vartheta) \end{bmatrix} \begin{pmatrix} x_{\mathrm{d}} \\ x_{\mathrm{q}} \end{pmatrix} \tag{7.24}$$

Applying the transformation during the controller design Applying the discussed Clarke-transformation on Eq. (7.16) delivers the voltage mesh equation in the $\alpha\beta$-reference frame shown in Eq. (7.25).

$$v_{\alpha\beta} = v_{\mathrm{i},\alpha\beta} - L_L \frac{\mathrm{d}i_{\alpha\beta}}{\mathrm{d}t} - R_L i_{\alpha\beta} \tag{7.25}$$

After the Park-transformation, Eq. (7.25) can be rewritten in the dq-reference frame as Eq. (7.26).

$$\begin{aligned} V_{\mathrm{g,d}} &= v_{\mathrm{i,d}} - R_L i_{\mathrm{d}} + \omega L_L i_{\mathrm{q}} - L_L \frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} \\ V_{\mathrm{g,q}} &= v_{\mathrm{i,q}} - R_L i_{\mathrm{q}} - \omega L_L i_{\mathrm{d}} - L_L \frac{\mathrm{d}i_{\mathrm{q}}}{\mathrm{d}t} \end{aligned} \tag{7.26}$$

Projecting the Laplace transformation for Eq. (7.26) delivers Eq. (7.27).

$$\begin{aligned} V_{\mathrm{g,d}}(s) &= V_{\mathrm{i,d}}(s) - R_L I_{\mathrm{d}}(s) + \omega L_L I_{\mathrm{q}}(s) - s L_L I_{\mathrm{d}}(s) \\ V_{\mathrm{g,q}}(s) &= V_{\mathrm{i,q}}(s) - R_L i_q(s) - \omega L_L I_{\mathrm{d}}(s) - s L_L I_{\mathrm{q}}(s) \end{aligned} \tag{7.27}$$

To describe the CHB inverter reference voltage, the Eq. (7.27) can be rewritten as Eq. (7.28).

$$\begin{aligned} V_{\mathrm{i,d}}(s) &= \overbrace{(R_L + sL_L)I_{\mathrm{d}}(s)}^{\text{d axis dynamics}} + \overbrace{V_{\mathrm{g,d}}(s) - \omega L_L I_{\mathrm{q}}(s)}^{\text{compensating term}} \\ V_{\mathrm{i,q}}(s) &= \overbrace{(R_L + sL_L)I_{\mathrm{q}}(s)}^{\text{q axis dynamics}} + \overbrace{V_{\mathrm{g,q}}(s) + \omega L_L I_{\mathrm{d}}(s)}^{\text{compensating term}} \end{aligned} \tag{7.28}$$

Eq. (7.28) describes the relationship between the CHB inverter's output voltage and current in the dq-reference frame. It can be divided into two main parts. The compensating term in this equation is treated in the control diagram as a feed-forward term and is added after the control to the controller output. Therefore, the filter transfer function can be simplified as in Eq. (7.29).

$$G_{\mathrm{f}}(s) = \frac{I_{\mathrm{d}}(s)}{V_{\mathrm{i,d}}(s)} = \frac{I_{\mathrm{q}}(s)}{V_{\mathrm{i,q}}(s)} = \frac{\frac{1}{R_L}}{1 + \frac{L_L}{R_L} s} \tag{7.29}$$

BESSs are able to provide active and reactive power. However, mainly active power is transferred from and to the grid. The simulation and hardware results focus only on the active power transfer.
The apparent power is generally defined as in Eq. (7.30).

$$S = v_{\mathrm{a}} i_{\mathrm{a}} + v_{\mathrm{b}} i_{\mathrm{b}} + v_{\mathrm{c}} i_{\mathrm{c}} = P + jQ \tag{7.30}$$

Applying the Park-transformation to Eq. (7.30) delivers Eq. (7.31).

$$S = \frac{3}{2} \cdot V_{\mathrm{dq}} \cdot I_{\mathrm{dq}} = \frac{3}{2} \cdot (V_{\mathrm{g,d}} + jV_{\mathrm{g,q}}) \cdot (I_{\mathrm{d}} - jI_{\mathrm{q}}) \tag{7.31}$$

The active and reactive power can then be defined in terms of the dq-reference frame as in Eq. (7.32).

$$\begin{aligned} P &= \frac{3}{2}(V_{\mathrm{g,d}} I_{\mathrm{d}} + V_{\mathrm{g,q}} I_{\mathrm{q}}) \\ Q &= \frac{3}{2}(V_{\mathrm{g,q}} I_{\mathrm{d}} - V_{\mathrm{g,d}} I_{\mathrm{q}}) \end{aligned} \tag{7.32}$$

For easier working on the dq-frame, the reference frame's d-axis is aligned along the grid voltage position $V_{\mathrm{g,q}} \stackrel{!}{=} 0$ and $V_{\mathrm{g,d}}$ is constant [181]. Therefore, Eq. (7.32) can be rewritten as Eq. (7.33).

$$\begin{aligned} P &= \frac{3}{2} V_{\mathrm{g,d}} I_{\mathrm{d}} \\ Q &= -\frac{3}{2} V_{\mathrm{g,d}} I_{\mathrm{q}} \end{aligned} \tag{7.33}$$

As shown in Eq. (7.33), the active and reactive power can be controlled independently using the d- and q-components of the current. Therefore, the control of the active and reactive power can be done using Eq. (7.34).

$$\begin{aligned} I_{\mathrm{d,ref}} &= \frac{2 P_{\mathrm{ref}}}{3 V_{\mathrm{g,d}}} \\ I_{\mathrm{q,ref}} &= -\frac{2 Q_{\mathrm{ref}}}{3 V_{\mathrm{g,d}}} \stackrel{!}{=} 0 \end{aligned} \tag{7.34}$$

P_{ref} and Q_{ref} are the reference values for the active and reactive power, respectively. During the operation of the selected CHB inverter, the reference reactive power is kept to zero ($Q_{\mathrm{ref}} \stackrel{!}{=} 0$) by setting $I_{\mathrm{q,ref}} \stackrel{!}{=} 0$. Therefore, the power factor is kept at $cos(\varphi) = 1$ and only active power is transferred during charging and discharging the BESS.

7.6.4 Controller Parameter

In Fig. 7.19, the VOC block diagram using the decoupled d- and q-components of the currents is represented.
The PLL is connected to the grid voltage. It delivers the transformation angle ϑ used for the discussed Clarke-, Park-transformations, and their inverses. The grid voltages are transformed into the dq-reference frame and are used for the feed forward control as shown in the compensating term in Eq. (7.28).
The currents reference values are calculated based on the required active and reactive power. These reference currents are compared with the actual measured current (after transformation from abc- to dq-reference frame) and the error is proceeded by two PI-controllers. In addition to the compensating term, which consists of the grid voltages in the dq-frame and the feed forward terms from Eq. (7.28), the reference inverter voltages in the dq-frame are then calculated as presented in Fig. 7.19. The usage of weak grid model shows higher distortion in the grid voltage. Therefore, the dq-components of the grid voltages are fluctuating and negatively influence the controller operation in the simulation and hardware. Furthermore, the second part of the compensation term is equal to zero because the q-component of the current is set to zero. Therefore, in the implementation, the compensation term is neglected which leads to lower dynamics in the inverter operation as shown later in Section 7.7. It is recommended to disable the compensation term when the grid voltages are polluted and has big noises.
Using the transformation angle ϑ, the inverter reference voltages $V_{\mathrm{i,d,ref}}$ and $V_{\mathrm{i,q,ref}}$ are transformed back using the inverse Clarke- and Park-transformations. The reference signals

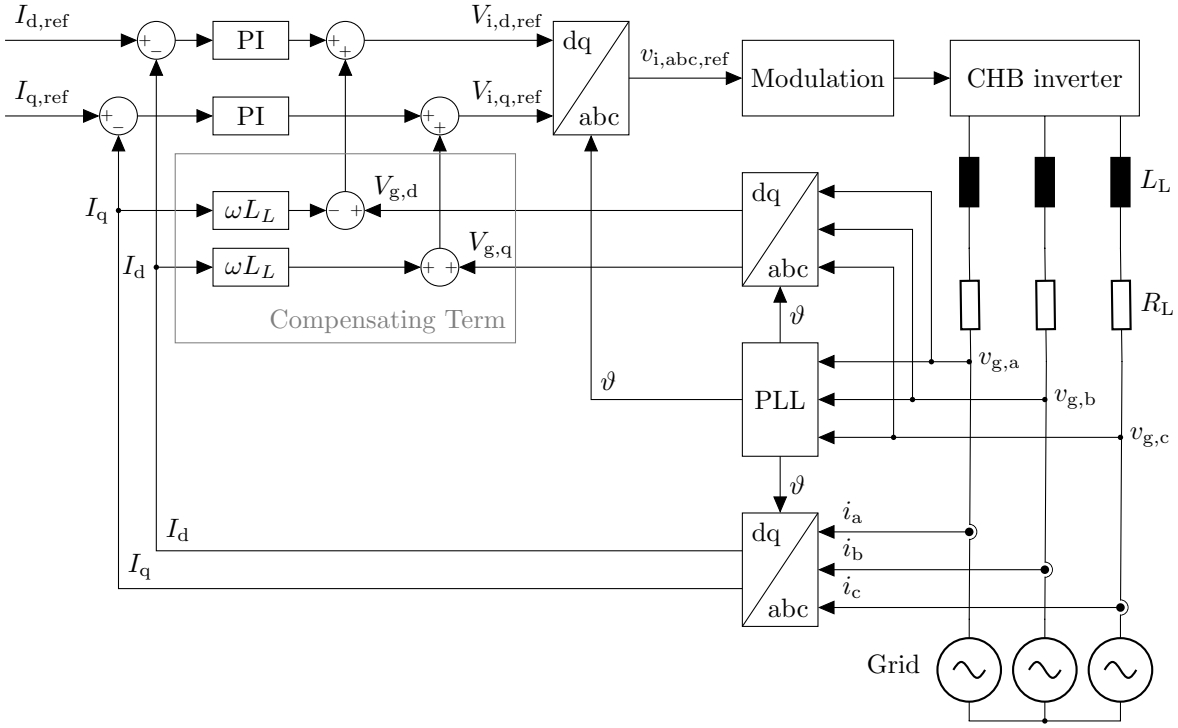


Figure 7.19 – Vector oriented control block diagram [107].

$v_{i,abc,ref}$ for the modulator are then generated in the abc-frame. Finally, the switching pulses for the CHB inverter are generated.
Further blocks shown in Fig. 7.19 are described from the control point of view to provide the controller's parameter.

CHB inverter block The time delay related to the switching behavior of the CHB inverter can be represented with the transfer function shown in Eq. (7.35).

$$G_{PWM}(s) = \frac{1}{1 + sT_\sigma} \tag{7.35}$$

The PWM signals for the H-bridge inverters are generated by comparing the reference voltage with a carrier-signal. Therefore, the delay in the system can be between zero and a maximum of one carrier period. Since this depends on the current value, the average value is used. The pulse width modulation average dead time is thus given in Eq. (7.36) [152].

$$T_\sigma = \frac{T_{sw,CHB}}{2} = \frac{1}{2 \cdot f_{sw,CHB}} \tag{7.36}$$

Power Filter Circuit The output filter dynamics are derived in Eq. (7.29) and can be expressed as Eq. (7.37).

$$\begin{aligned} G_{\mathrm{f}}(s) &= \frac{V_{\mathrm{S}}}{1+T_1 s} \\ V_{\mathrm{S}} &= \frac{1}{R_L} \\ T_1 &= \frac{L_L}{R_L} \end{aligned} \tag{7.37}$$

PI-Controller blocks The PI-controller parameters are designed using the Symmetrical (SO) and Modulus Optimum (MO) approaches recommended in [152]. The proportional part and the controller time constant using SO are calculated as shown in Eq. (7.38).

$$\begin{aligned} V_{\mathrm{R,SO}} &= \frac{T_1}{2T_\sigma V_{\mathrm{S}}} \\ T_{\mathrm{n,SO}} &= 4 \cdot T_\sigma \end{aligned} \tag{7.38}$$

The usage of MO leads to the parameter shown in Eq. (7.39).

$$\begin{aligned} V_{\mathrm{R,MO}} &= \frac{T_1}{2T_\sigma V_{\mathrm{S}}} \\ T_{\mathrm{n,MO}} &= T_1 \end{aligned} \tag{7.39}$$

The controller output voltages $V_{\mathrm{i,dq,ref}}$ are inverse transformed to the abc-coordinates $v_{\mathrm{i,abv,ref}}$ and build the reference signals for the modulator. The values for the proportional $K_{\mathrm{P,SO}}$ and integral $K_{\mathrm{I,SO}}$ of the PI-controller can be written as in Eq. (7.40) [152].

$$\begin{aligned} K_{\mathrm{P,SO}} &= \frac{L_L}{T_{\mathrm{sw}}} \\ K_{\mathrm{I,SO}} &= \frac{L_L}{2 \cdot T_{\mathrm{sw}}^2} \end{aligned} \tag{7.40}$$

Using MO, The values for the proportional $K_{\mathrm{P,MO}}$ and integral $K_{\mathrm{I,MO}}$ of the PI-controller can be written as in Eq. (7.41) [152].

$$\begin{aligned} K_{\mathrm{P,MO}} &= \frac{L_L}{T_{\mathrm{sw}}} \\ K_{\mathrm{I,MO}} &= \frac{R_L}{T_{\mathrm{sw}}} \end{aligned} \tag{7.41}$$

The PI controller parameters using MO and SO are listed in Table 7.10 and the step response is illustrated in Fig. 7.20a. The SO and MO provide quick reaction time accompanied with overshoot. Using the SO, this overshoot is higher compared to the MO.

In Table. 7.11, the performances and robustness of the PI controllers using the SO and MO is shown. The rise time in the SO is smaller than that of MO because is reacts quicker. However, the overshoot is 45.1 % and higher than that of the MO approach which is 4.9 %. The step response shows that in both cases the system is stable. Due to the lower overshoot, the MO is preferred.

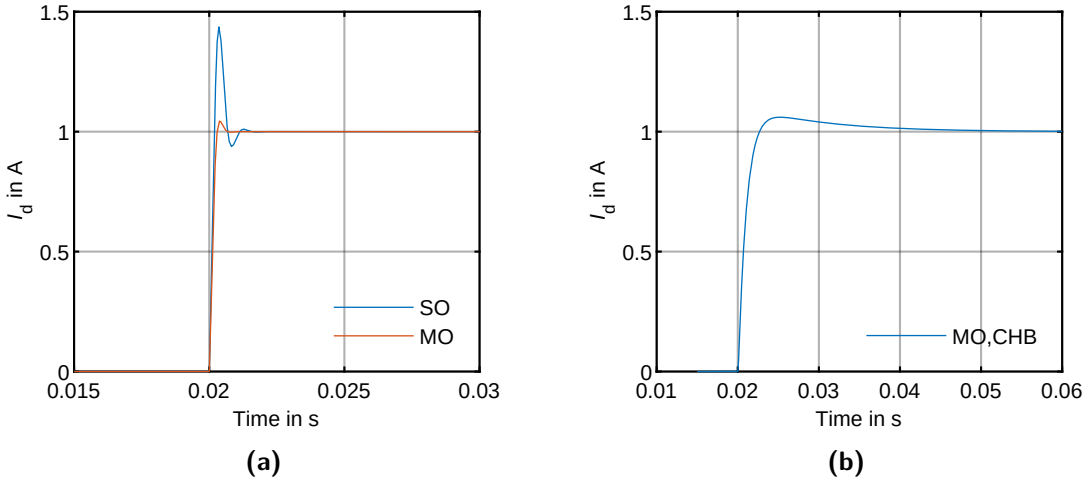


Figure 7.20 – Step responses of the closed loop using (a) SO, MO, and (b) MOCHB.

Table 7.10 – PI-controller parameter using symmetrical and modulus optimum from [152] and adapted to the CHB inverter.

Description	Variable	Value	Unit
K_P using the SO-approach	$K_\mathrm{P,SO}$	8.01	V/A
K_I using the SO-approach	$K_\mathrm{I,SO}$	32056	V/As
K_P using the MO-approach	$K_\mathrm{P,MO}$	8.01	V/A
K_I using the MO-approach	$K_\mathrm{I,MO}$	98.13	V/As
K_P using the MO-approach for the CHB inverter	$K_\mathrm{P,MO,CHB}$	1	V/A
K_I using the MO-approach for the CHB inverter	$K_\mathrm{I,MO,CHB}$	98.13	V/As

The usage of these values are optimized for two-level inverter. The selected CHB inverter with eight submodules reacts abruptly in the simulation while using the controller parameter from Eq. (7.41) and shown in Table 7.10. Therefore, the $K_\mathrm{P,MO}$ is divided by the number of the submodules used in the CHB inverter as shown in Eq. (7.42). Fig. 7.20b shows the step response using the proposed parameter for the PI-controller in Eq. (7.42). The time axes in the Fig. 7.20a and 7.20b are different due to the reduction of the $K_\mathrm{P,MO}$. The usage of the $K_\mathrm{P,MO,CHB}$ using the MO-approach for the CHB inverter (MOCHB) leads to good operation in the simulation as shown in Section 7.7.

$$K_\mathrm{P,MO,CHB} = \frac{L_L}{n_\mathrm{submodules} \cdot T_\mathrm{sw}} \tag{7.42}$$

The PI-controller parameter using SO, and MO, and MOCHB are summarized in Table 7.10. Finally, from the control point of view, the PI-controller block shown in Fig. 7.19 can be represented as the transfer function in Laplace-domain as shown in Eq. (7.43).

$$\begin{aligned} G_\mathrm{PI}(s) &= K_\mathrm{P,MO,CHB} \cdot \left(1 + \frac{1}{sT_\mathrm{n,MO,CHB}}\right) \\ &= \frac{sK_\mathrm{P,MO,CHB} + K_\mathrm{I,MO,CHB}}{s} \end{aligned} \tag{7.43}$$

Table 7.11 – Performances and robustness of the PI-controllers using the SO, MO, and MOCHB.

Optimization method	Rise time	Settling time	Overshoot	Closed-loop stability
SO	0.13 ms	1.04 ms	45.1 %	Stable
MO	0.19 ms	0.53 ms	4.9 %	Stable
MOCHB	1.7 ms	16.5 ms	6.04 %	Stable

7.7 Simulation Results

7.7.1 System Stability

The transfer function solution of a linear system provides whether the system is dynamically stable or not. In order to have a stable system, all poles have to be on the left half of the complex plane. The system response is fast when the poles are more to the left of the imaginary axis. While in an unstable system, the poles have positive real parts and lie on the right plane. A pole lying on the imaginary axis has undamped oscillations and is known as marginally stable [134]. The plant's transfer function includes the inverter switching delay (Eq. (7.35)), the power filter (Eq. (7.37)), and the PI-controller (Eq. (7.43)) as shown in Eq. (7.44) or Eq. (7.45).

$$G(s)_{\text{Plant}} = G(s)_{\text{PWM}} \cdot G(s)_{\text{f}} \cdot G(s)_{\text{PI}} \tag{7.44}$$

$$G(s)_{\text{Plant}} = \frac{(1/R_L)(sK_{\text{P,MO,CHB}} + sK_{\text{I,MO,CHB}})}{s(1+sT_\sigma)(1+s(L_L/R_L))} \tag{7.45}$$

The transfer function delivers the system response characteristics without the need to solve its complete differential equations. The plant's transfer function $G(s)_{\text{Plant}}$ is used to plot the pole zero map for the inverter at the calculated filter value, the given voltage switching frequency, and the adapted PI-controller parameters. From Eq. (7.45), the feedback control transfer function is derived. Its poles and zeros are then mapped on the imaginary and real axis of the complex s-plane as shown in Fig. 7.21. The CHB inverter's pole zero map determines the system stability. Thereby, the crosses 'x' represent the poles and the circle 'o' the zero of the feedback control transfer function and are located in the left half of the complex plane. The system has one real zero and three real poles and is therefore fourth order. Their exact coordinates are shown in Table 7.12 and leans on the real axis. The real poles define an exponentially decaying components in the homogeneous response. The pole1 decay rapidly compared to pole2 and pole3. Therefore, the system is stable.

Table 7.12 – Data related to the pole zero map.

Type	Value
Pole1	$-14\,935\,\text{s}^{-1}$
Pole2	$-969\,\text{s}^{-1}$
Pole3	$-108\,\text{s}^{-1}$
Zero	$-98\,\text{s}^{-1}$

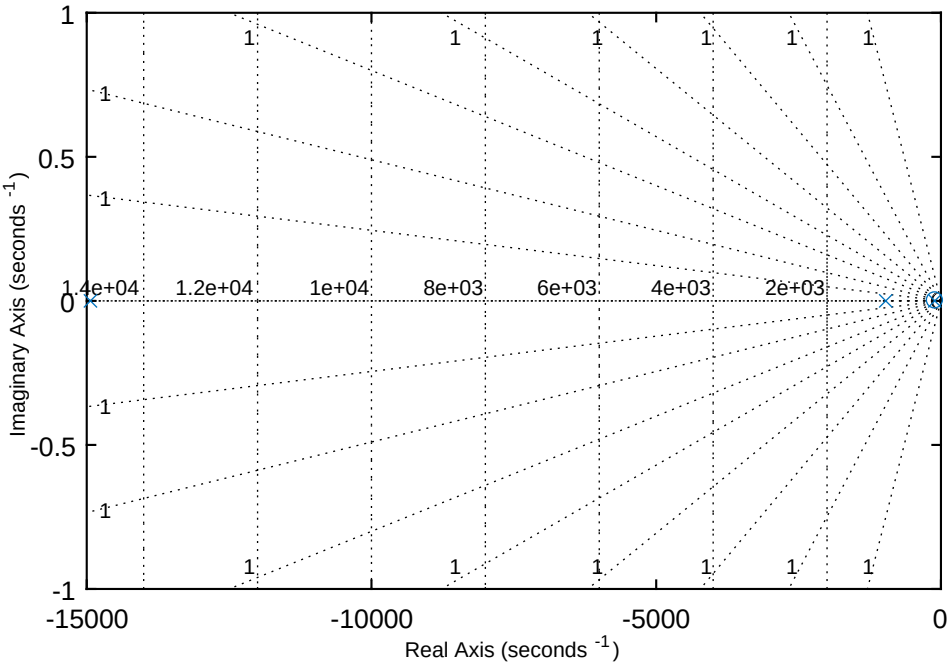


Figure 7.21 – Pole zero map for the feedback control transfer function $G(s)_{\mathrm{Plant}}$ of the filter, the inverter, and the PI-controller.

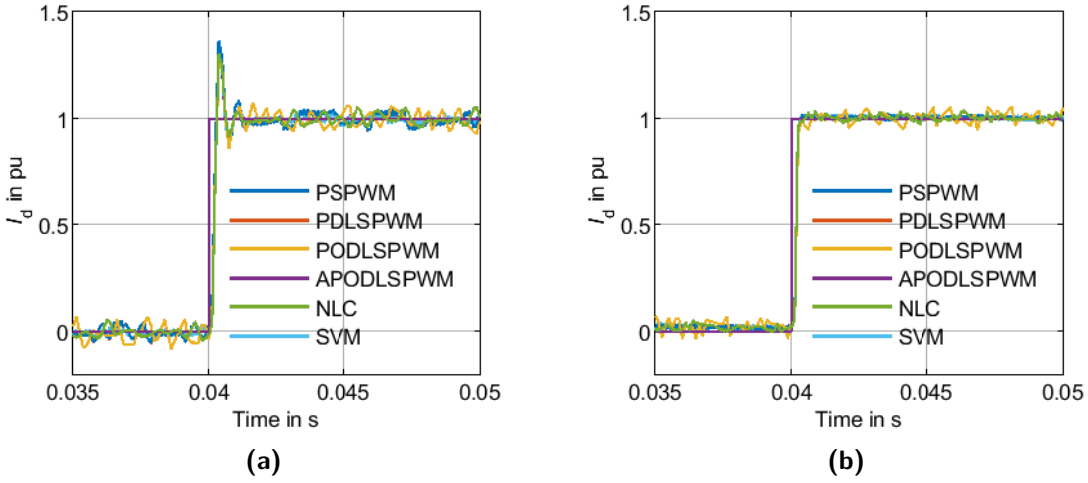


Figure 7.22 – Step responses using the simulations on circuit-level (a) with and (b) without considering the compensating term.

7.7.2 Step Response Analysis

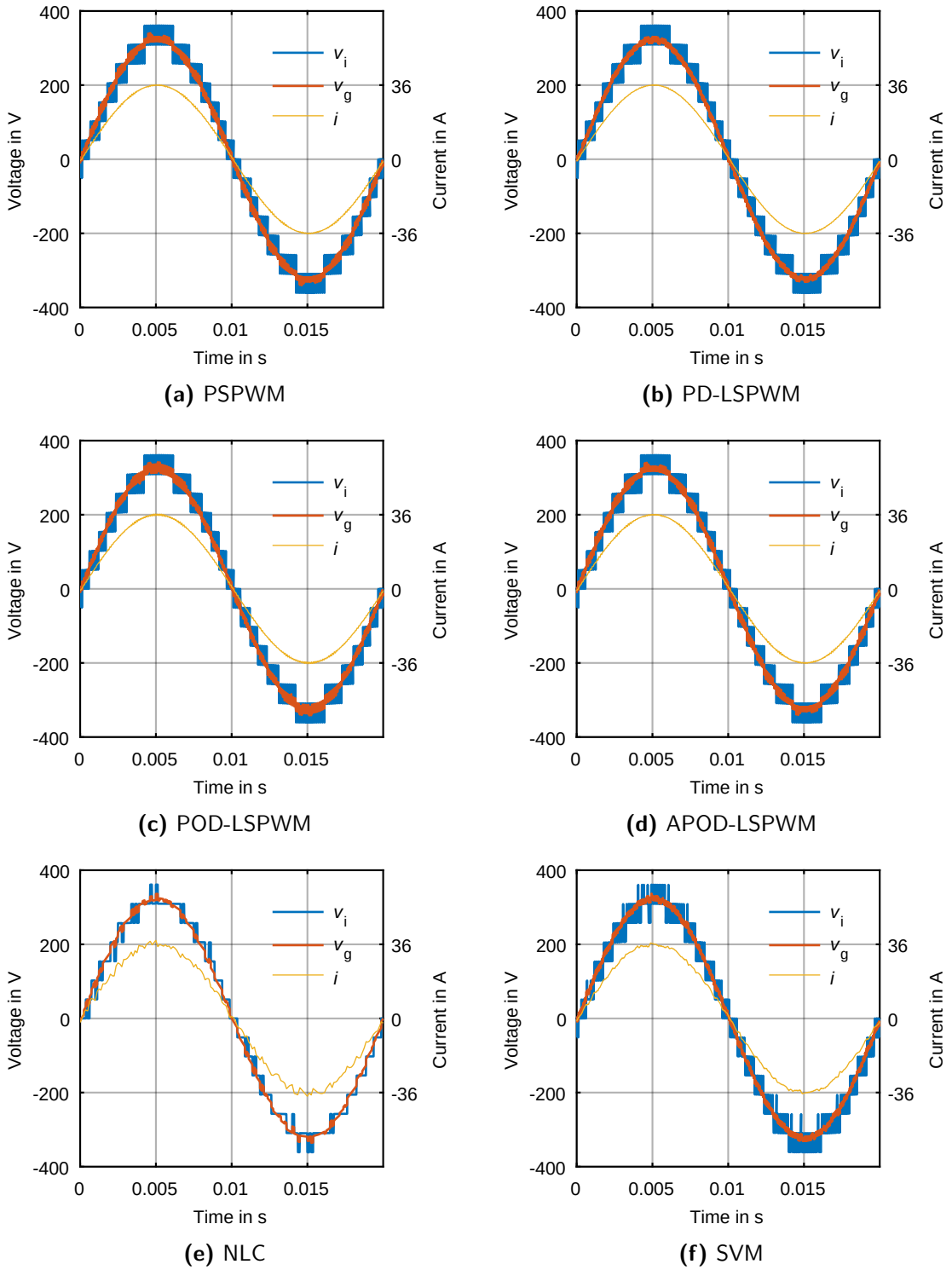
In order to validate the CHB inverter's operation using the calculated parameter, the step response of the current's d-component is investigated in the simulation and later in the implemented hardware. Fig. 7.22 shows the CHB inverter step response in the simulation

using the discussed modulation techniques. Using the compensating term with the weak grid model leads to the results shown in Fig. 7.22a. Using the weak grid model, the grid voltage is distorted and the coupling of the distorted signals and the coupling of this value at the controller outputs leads to higher distortions in the inverter reference voltages. Moreover, the coupling of the d- and q-components of the voltages leads to higher system dynamic and higher overshoot. The implementation of Eq. (7.28) leads to an overshoot shown in Fig. 7.22a of 36 % using PSPWM, 36 % using LSPWM methods, 25 % using NLC, and 30 % using SVM. In order to avoid the overshoot in the actual current value, a slew ramp can be used to limit the abruptness of the reference current change for a half time period (10 ms) [100]. For BESS's operation, high dynamic response is not required. Furthermore, the operation without compensating term leads to better performance in the simulation when a weak grid is used as shown in Fig. 7.22b where all the overshoots are eliminated. Therefore, further steady state simulations focus on the operation without using the compensating term.

7.7.3 Steady State Operation

In the last section, the controller design is parametrized and the system's stability and step response show a stable system without overshoot. Within this section, the simulation results during the steady state operation are presented.
The current, grid, and inverter voltages of one phase while charging the BESS using the modulation techniques discussed in Section 7.4 are shown in Fig. 7.23. The d-component of the current is set to $I_\mathrm{d} = 1$ and q-component is set to $I_\mathrm{q} = 0$. Therefore, only active power is fed from the grid while keeping the reactive power at zero. The current i is therefore in phase with the grid voltage v_g.
Using the carrier based PWM techniques, the inverter voltage switching frequency is set to 8 kHz. Using the NLC, the switching frequency depends on the sampling-time of the used controller and the used controller parameter. The sampling frequency of the controller is also set to 8 kHz.
The THD using the carrier based modulation techniques show higher performance and lower THD in comparison to the NLC and SVM.
The current and voltage THDs are the highest using the NLC. However, they are under the standards limits.

In Table 7.13, the corresponding THDs during the charging operation shown in Fig. 7.23 in addition to the operation using the coupling term and for both of the charging and discharging operation are listed. The distortion of the voltages and currents using the different modulation techniques are under the limits given by the grid standards. Compared to the two-level inverter, the distortion caused by the CHB inverter is lower. Table 7.13 also shows the corresponding THDs while discharging the BESS. The grid distortion is almost similar to that measured during the charging operation. The usage of NLC leads to the highest current and grid voltage distortion.
Furthermore, Table 7.13 also provides the simulation results considering the compensation term. The grid voltage and current THDs are higher compared to the results without compensating term. The addition of the distorted grid voltage leads to additional fluctuation in the reference voltage for the modulators.



(a) PSPWM **(b)** PD-LSPWM

(c) POD-LSPWM **(d)** APOD-LSPWM

(e) NLC **(f)** SVM

Figure 7.23 – CHB inverter and grid voltages and phase current using different modulation techniques during the charging operation.

Table 7.13 – Voltage and current THDs of the simulation results using different modulation techniques during the BESS's charging and discharging operation on circuit-level.

Grid model	**Without coupling term**				**With coupling term**			
Operation	Charging		Discharging		Charging		Discharging	
Modulation	THD_v	THD_i	THD_v	THD_i	THD_v	THD_i	THD_v	THD_i
PSPWM	0.03	0.11	0.03	0.20	1.37	4.11	1.19	3.97
PD-LSPWM	0.04	0.09	0.05	0.20	0.66	1.56	0.60	1.27
POD-LSPWM	0.04	0.10	0.04	0.23	0.75	1.80	0.70	1.91
APOD-LSPWM	0.03	0.11	0.03	0.20	1.18	3.79	1.08	3.46
NLC	1.2	2.78	0.98	2.37	1.47	3.30	1.44	3.5
SVM	0.67	1.49	0.52	1.28	1.17	2.73	1.01	2.5

Within this section the simulation results are shown and compared to each other. It is found, that the operation at the weak grid requires neglecting the compensating term. However, all results shown are under the standards limits. The simulation on circuit-level allows to study the dynamic and steady state operation of the CHB inverter to be designed and prepared for hardware implementation. In the next section, the implemented CHB inverter hardware is shown and measurements are done to validate the simulation results.

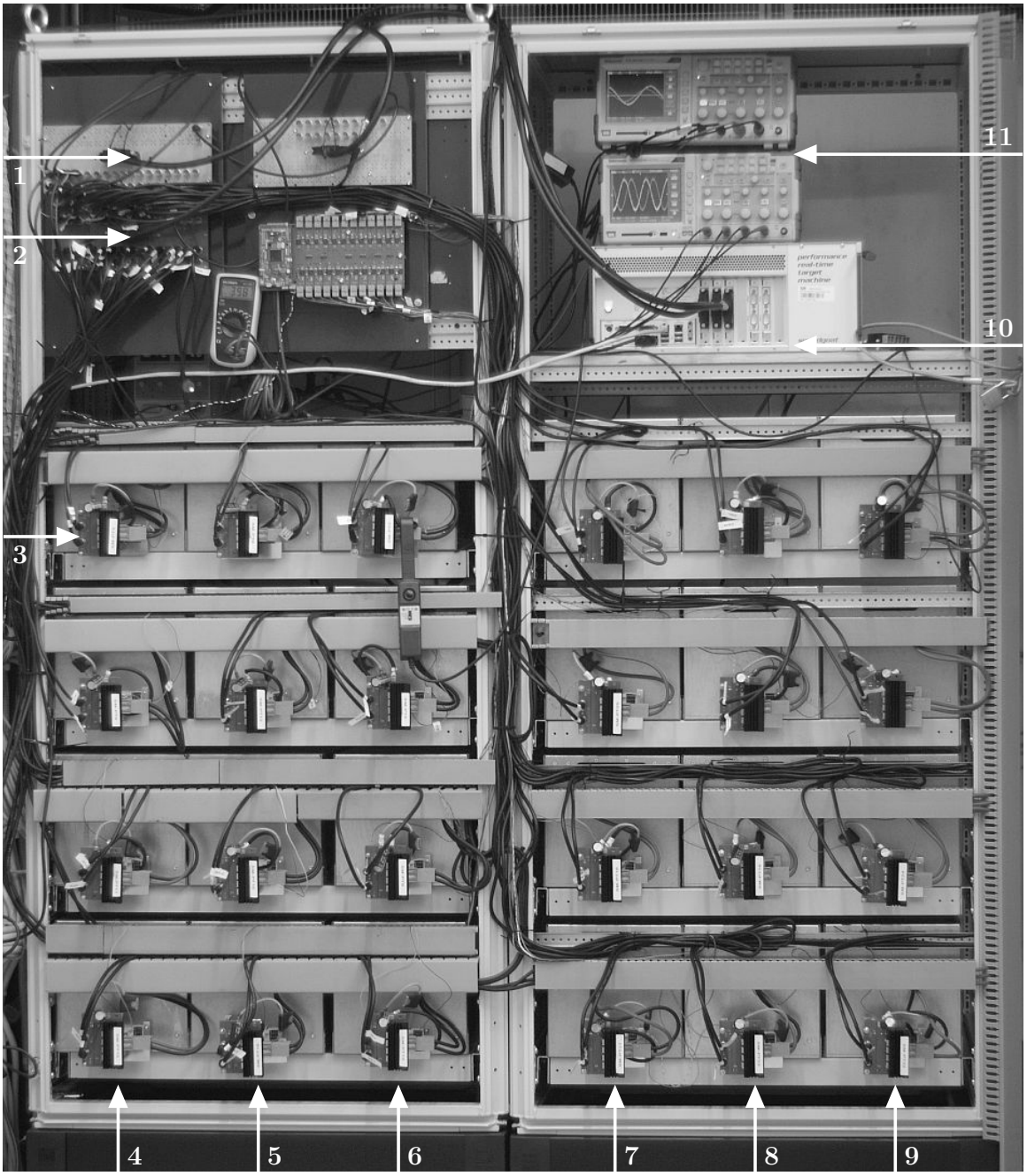
7.8 Hardware Assessment

The simulation results show a satisfying and standard-conform 17-level CHB inverter operation while charing and discharging the BESS using the weak grid model. Thereby the usage of the coupling term gives highest THD values. In this section, the hardware and measurement results are shown and compared to the previous simulations.

7.8.1 Hardware

In Fig. 7.24, the implemented three-phase 17-level CHB inverter with a maximal efficiency of 99.36 % is shown. For its power range of 17.6 kVA, it is the most efficient connected power inverter to the low voltage grid. It consists of 24 submodules. In each phase, eight of them are connected in series.

The submodule's hardware is designed and tested on component-level. The focus is given to one component of the CHB inverter. It shows higher efficiency and higher overload capability during its operation as discussed in [20].
Due to the complexity of the CHB inverter and its high number of components, the three-level three-phase inverter is firstly connected to the grid using a variable output voltage transformer. The next submodules are successively connected meanwhile increasing the grid voltage depending on the sum of the submodules' DC-link voltages. The connection of the CHB inverter including all submodules using similar parameter as in the simulation leads to high distortions. Therefore, to reduce the noises, the switching frequency or the filter inductance must be increased. The increase of the switching frequency is simpler and leads to better inverter's performance on the grid and is followed in the further results. The power filter used is an inductor with an inductance of 0.98 mH and internal resistance of 12 mΩ. The



Number	Description	Number	Description
1	Analog inputs	5 and 8	Phase b
2	Digital outputs	6 and 9	Phase a
3	H-bridge inverter	10	Control unit
4 and 7	Phase c	11	Oscilloscopes

Figure 7.24 – The implemented three-phase 17-level CHB inverter.

usage of this small filter value is given by the current ripple method shown in Section. 7.5. The used control unit shown in Fig. 7.24 reads the analog voltages and currents required for

the software-part shown in Fig. 7.1 and then generates the PWM for all H-bridge inverters. The usage of a centralized system is preferred due to its simplicity. Therefore, the increase of the switching frequency suggested to reduce the distortion is easily implemented. Decentralized control methods are suggested in [104] and [106].
The oscilloscopes shown in Fig. 7.24 are used to monitor the grid and inverter line-to-line voltages amplitudes and phase synchronization before connecting the inverter with the grid. They are also used to record the measurements shown within this section.

7.8.2 Step Response Analysis

In order to validate the CHB inverter's operation using the parameter calculated, the step response of the current's d-component is investigated in the implemented hardware. The implementation in the hardware shows also similar overshoot. After a reference value change from zero to one, 16 % current overshoot is measured. The measurement's step response is shown in Fig. 7.25.
In order to avoid the current's overshoot, a slew ramp can be used to limit the abruptness of the reference current change for a half time period (10 ms) [100].

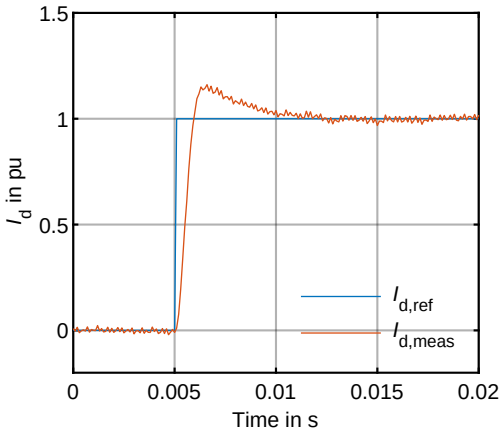


Figure 7.25 – CHB inverter's step response in the hardware.

7.8.3 Steady State Operation

The inverter steady state operation is presented within this section. For the measurements, the POD-LSPWM is used due to its implementation's simplicity as described in Section 7.4. The measurement results are shown in Fig. 7.26 using POD-LSPWM during the charging, at zero current, and discharging operation of the BESS using the switching frequencies 16 kHz and 32 kHz. The used filter has an inductance of 0.98 mH. The design of the filter using the current ripple method leads to low inductance and shows high distortions while connecting the hardware to the grid using the switching frequency of 8 kHz. One possibility to eliminate the noises is the increase of the filter's inductance by decreasing the allowed current ripple. The second possibility is by increasing the switching frequency. The second possibility is easier to implement but leads to higher switching losses. The inverter is then connected to the grid

Table 7.14 – Voltage and current THDs of the measurements shown in Fig 7.26 using POD-LSPWM.

Modulation	Switching frequency f_{sw}	THD_v	THD_i
Fig. 7.26a	16 kHz	2.45	4
Fig. 7.26c	16 kHz	2.24	-
Fig. 7.26e	16 kHz	2.04	3.78
Fig. 7.26b	32 kHz	2.12	3.53
Fig. 7.26d	32 kHz	1.76	-
Fig. 7.26f	32 kHz	1.67	3.49

and using the switching frequencies of 16 kHz and 32 kHz and the corresponding measurement results are shown in Fig. 7.26. This increase from the switching frequency 8 kHz to 16 kHz and 32 kHz is similar to the decrease of the current ripple to 2.5 % and 1.25 %, respectively. The usage of 16 kHz shows higher distortions near to the standards' limits. The THD of the current while charging and discharging the battery is 4 %. The usage of the switching frequency of 32 kHz decreases both of the THDs.

In Table 7.14, the THDs of the grid voltage and current are shown. They are higher than those from the simulation on circuit-level. In comparison to the simulation results shown in Table 7.13, the measurement shows higher distortions. However, the simulation's goal is the design, the system operation, and concept functionality tests. It provides the possibility to test cases, which can not be tested in real hardware due to the possible damages. The difference can be justified by the parasitic effects and additional components which can not be determined and modeled. The voltage and current sensors also have a given tolerance. The parametrization of a real grid, to which the inverter is connected, requires complex measurements and can not be performed.

It can be concluded, that the power filter design delivers a low inductance, which leads to increasing the switching frequency to compensate the small filter.

7.9 Summary

Within this section, the circuit-level is introduced and the CHB inverter design and operation are presented.

The simulations on circuit-level allow to study important components of the BESS. Assuming the inverter operation using ideal power switches highly reduces the simulation time while keeping the dynamic operation in the CHB inverter. The shown inverter's model on circuit-level is divided into two parts. The software- and hardware-parts are introduced and the difference in their modeling and sampling frequencies is explained. This allows to nearly model the reality and the hardware measurements.

Since the inverter dynamic and switching behavior are modeled on circuit-level, the grid is influenced during the inverter operation. The influence depends on used grid model's parameter. Therefore, the ideal, the strong, and the weak grid are introduced and parametrized. The different simulation results operating at different grid models are shown and compared to each other. The weak grid is selected to be used for further analysis during the simulation of the CHB inverter on circuit-level.

The modulation techniques for multilevel inverters are presented. Both of the carrier based techniques such as the phase shifted and level shifted PWM and not carrier based such as the

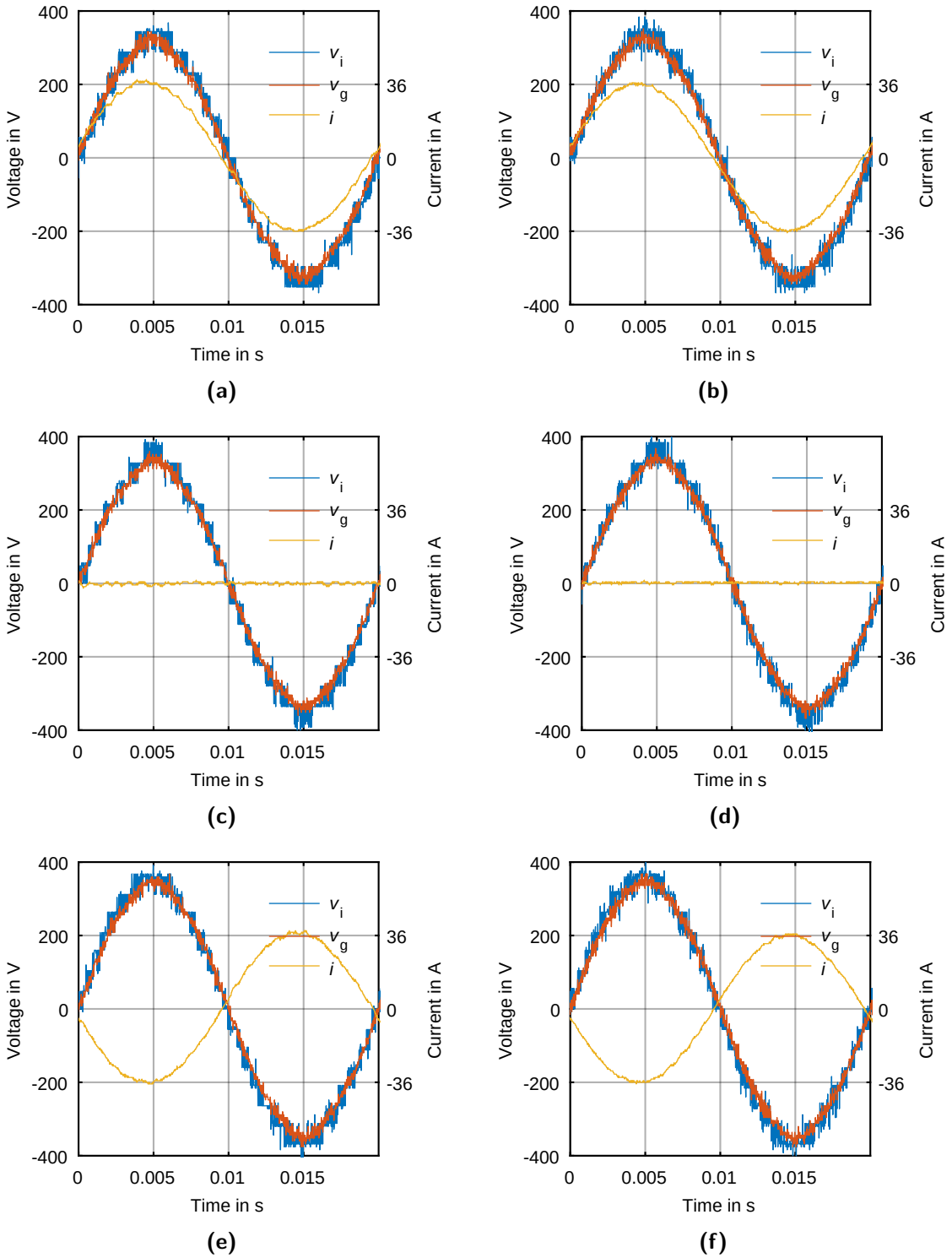


Figure 7.26 – Inverter v_i and grid v_g voltages and current i measurement results using the CHB inverter prototype at $f_{sw} = 16\,\mathrm{kHz}$ (a) while charging, (c) at zero current, (e) while discharging, at $f_{sw} = 32\,\mathrm{kHz}$ (b) while charging, (d) at zero current, and (f) while discharging at constant filter value of $0.98\,\mathrm{mH}$.

nearest level control and the space vector modulation are explained and adapted to be used in the selected 17-level CHB inverter. Due to its overall superior advantages in the field of BESS, the PSPWM is recommended.
To design the power filter for distortion mitigation, the state of the art of the design methods is shown. The current ripple method is then applied on the L-filter to be used in the CHB inverter and the filter parameters are compared to the classical two-level B6-bridge inverter. It concludes that the filter inductances of the 17-level CHB inverter is much lower than the two-level B6-bridge inverter even if both inverters operate at the same switching frequency at the PCC.
The definition of the CHB inverter switching frequency and the filter parameters allows to fully describe the plant to be controlled. The vector oriented control is used and the PI-controller parameters are calculated. It allows a fully decoupled control of the active and reactive power while charging and discharging the BESS.
After the controller design, the simulation results are shown to verify the system stability and to analyze the step response of the plant. Furthermore, the steady state operation of the BESS during charging is shown and the distortions in voltages and currents are derived. It is concluded, that the inverter operates stably without overshoot and without exceeding the standards' limits.
Finally, the implemented 17-level CHB inverter prototype is shown and measurement results are presented. The hardware measurements contain more noises than expected and the grid effects and distortions are higher than the simulations. The CHB inverter is centrally controlled and the pulses are generated using the software-part from the simulation model on circuit-level implemented in the centralized control unit.
The inverter operation shown on circuit-level can be used for short times to analyze the dynamic behavior of the BESS in transient and steady state cases. However, the BESS operates normally in hours-ranges to deliver all its energy content or to be charged to and from the grid, respectively. For this analysis, the system-level is introduced in the next chapter. Increasing the abstraction degree of the BESS modeling opens a new area to study the BESS operation for hours-range. The average models used are introduced and validated using the results from the simulations on circuit-level.

8 Long-Term Operation Modeling on System-Level

To analyze the BESS's operation for long periods of time, simulations are done on system-level using the inverter's average models. The behavioral model is applied for hours-range simulation. The usage of simulations on system-level is especially interesting for CHB inverters due to the utilization of separated batteries, which are unequally discharged depending on the used modulation technique.
The simulations on system-level are introduced in Section 8.1 and the behavioral modeling of power inverter is given in Section 8.2. Special attention is given to the H-bridge, B6-bridge, and 17-level CHB inverter.
The simulations on system-level use non-switching models. Therefore, the modulation techniques for the 17-level CHB inverter are also averaged and introduced in Section 8.3.
These simulations on system-level allow the calculation of the inverter efficiency, as presented in Section 8.4, to study or rather optimize the long-term BESS's operation to increase its efficiency.
Finally, the simulation results on system-level are presented in Section 8.5. The simulation's performance in terms of simulation duration is mentioned to represent the main advantage of using an average model. The DC-link currents waveforms are presented to explain the loading of the submodule's battery modules and the resulting different discharging time using different modulation techniques. Furthermore, the states of charges of the submodules and the remaining energy contents are compared to recommend and select the modulation technique on system-level.
The simulation results on system-level are compared to the previous results on circuit-level.
The discussed simulations on system-level and results are previously partially published in [101].

8.1 Introduction to Simulations on System-Level

The modern physical simulation shortens the design time and accelerates the study of the BESS. The simulation on system-level, on the highest abstraction level, of the power conversion unit uses averaged (non switching) models. It is used to analyze the BESS's long-term operation and is therefore suitable for testing different BESS operation strategies.
This simulation is especially interesting for CHB inverters due to the usage of split independent battery modules in the submodules. In order to investigate the inequalities between the charging and discharging closely, the models are done on system-level in order to analyze the BESS's SoC for long simulation times (hours-range) by means of averaged models.
Increasing the simulation abstraction up to the system-level reduces the simulation duration by a factor of up to 370 compared to the simulation on circuit-level and it allows long-term prediction of the behavior of the storage system in short time.

This allows the usage of the models in hardware in the loop system to test e.g. the EMS without implementing the hardware. Only average models are used in this case.
Moreover, the efficiency curves of the inverter from lower simulation-level, as presented in the past chapters, can be used on this level. This leads to e.g. increased efficiency of the BESS if additional intelligence is implemented in the EMS.

8.2 Behavioral Model of Power Inverters

Using physical simulations on system-level allows the elaboration of a system before realizing it in hardware. Physical models save time and accelerate the development process. For simulation time-range of hours, as in the case of analyzing the operation strategies for BESS, average models of the power inverters on system-level are used. They need lower sampling-time and progress quicker than the inverter's models on circuit-level.
The simulations on system-level are used for investigating the interaction between the inverter and other BESS components. Their main objective is to design an effective EMS and to study the effects of modulation techniques on the SoC behavior of the different battery modules.
Further averaged models of the power electronics are deeper presented and studied in [10]. "Averaged model focuses on capturing the low-frequency behavior of power electronic converters while neglecting high-frequency variations due to circuit switching" [10]. However, on system-level only behavioral models are introduced and used. Neglecting the switching behavior and using average models make the simulation faster due to the lower sampling-time required. The inverter's average model uses ideal voltage sources to represent the inverter's AC-side. On the DC-side, the battery modules are connected to controlled current sources as shown later e.g. in the H-bridge inverter in Fig. 8.1.
This simulation on system-level is suitable to simulate the BESS's operation in hours-range. On circuit- and component-level, the simulations duration are in seconds and milliseconds range, respectively.

8.2.1 Average Modeling of H-Bridge Inverters

The average model of a single-phase DC-AC inverter, e.g. of an H-bridge inverter, is presented in Fig. 8.1. This model can be used to explain the simplifications done at system-level and further be used to represent one CHB inverter's submodule. On the left DC-side, it is represented using a controlled current source which is connected to the battery module. On the right side, the average model uses a controlled voltage source.
When only active power is exchanged between the grid and the inverter (using $cos(\varphi) = 1$ or $I_\mathrm{q} = 0$), the DC-link current source is controlled by the absolute value of the AC current and the quotient of the grid and battery voltages ($I_\mathrm{DC} = |i_\mathrm{a}| \cdot \frac{v_\mathrm{i,a}}{V_\mathrm{batt}}$). Whenever the reactive power is considered, the DC-link current depends additionally on the d-component of the grid current as in Eq. (8.1), where $sgn(I_\mathrm{d})$ the sign function of the d-component of the current.

$$I_\mathrm{DC} = |i_\mathrm{a}| \cdot \frac{v_\mathrm{i,a}}{V_\mathrm{batt}} \cdot sgn(I_\mathrm{d}) \tag{8.1}$$

The AC voltage source is controlled by the controller's output. In the simulations on circuit-level, this signal is forwarded to the modulator. However, the models on system-level consist

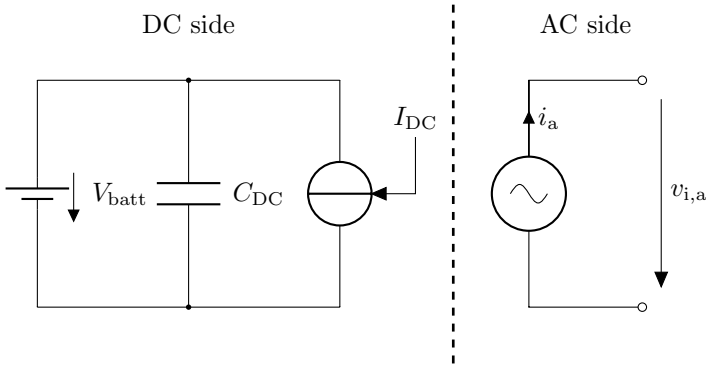


Figure 8.1 – Average model of a single-phase DC-AC inverter, e.g. H-bridge inverter.

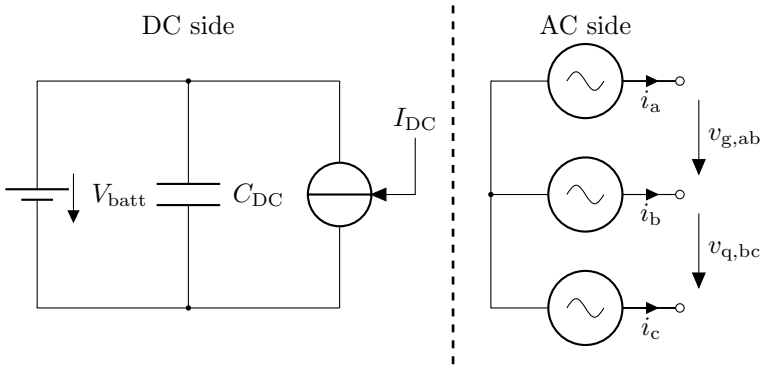


Figure 8.2 – Average model of a three-phase DC-AC inverter, e.g. B6-bridge inverter.

of average models and no switching units are present. The controller varies the amplitude and the shift angle to the grid voltage of the reference signals to control the grid current and therefore the active and reactive power exchange with the grid.

8.2.2 Average Modeling of B6-Bridge Inverters

To introduce the average model of the CHB inverter on system-level, the model used for two-level B6-bridge inverters is introduced and its function is explained. For a three-phase DC-AC Inverter, the AC-side is represented by three controlled voltage sources and the DC-side using one controlled current source. Fig. 8.2 shows the average model of a conventional DC-AC inverter. A representation on the AC-side with two voltage sources, that represent the line-to-line voltage, is also possible. However, the representation of the AC-side using three controlled voltage sources is preferred because the control presented in the previous section delivers the three-phase reference signals.
On the DC-side, a representation using a variable resistor or a controlled voltage source is possible. The DC-part of this average model is not similar to this of the H-bridge inverter. It is controlled by the peak value of the current and the d-component of the grid current ($I_{\mathrm{DC}} = \hat{I}_{\mathrm{a}} \cdot \frac{I_{\mathrm{d}}}{I_{\mathrm{d,nom}}}$). The usage of controlled current sources is preferred because the grid connected inverters are current controlled on the AC-side. Thus the calculation of the DC-link currents becomes much simpler.

8.2.3 Average Modeling of 17-Level CHB Inverters

In the case of modeling a three-phase 17-level cascaded H-bridge inverter on system-level, 24 controlled current sources on the DC-side and three voltage sources on the AC-side are required as shown in Fig. 8.3.
All current sources are controlled depending on the 24 battery modules voltages, the AC-currents, and the controller reference signals. Efficiency tables from simulations on component-level or measurements can be implemented to analyze the efficiency of the BESS in its long-term operation. The implementation of the modulation techniques while modeling the CHB inverter on system-level differs only on its DC-side.
The inverter's AC-side using three controlled voltage sources and the control remain the same in all implemented models. It is similar to the AC-side used in B6-bridge inverter. Using average models, the inverter generates a non switching output voltage on the AC-side using the reference signals at the controller's output after the inverse Clarke- and Park-transformations. The vector oriented control delivers the abc-reference voltages for the modulator after applying the inverse Clarke- and Park-transformations when simulating on circuit-level. The modulator then generates the pulses for the power switches. On system-level no modulators are used and the inverter's switching behavior is neglected. Therefore, the reference signals at controller output are multiplied with the magnitude of the grid phase voltage ($\hat{V}_{\mathrm{g,a}} = \sqrt{2} \cdot v_{\mathrm{g,a}}$) and fed to the controlled voltage sources.
The DC-side operates in a similar way as using the average model of the H-bridge inverter. In combination with the actual current i_{a} and the sum of the battery voltages, the reference signals are used to calculate the reference currents for the controlled current sources.
The 17-level CHB inverter can be modeled on system-level using 24 average models of each H-bridge inverter separately. This leads to higher number of voltage sources in the system on the AC-side. However, the resulting AC-voltage waveform is identical to the approach proposed using less number of AC-voltage sources as shown in Fig. 8.3.
On system-level, the inverter's DC- and AC-side are physically independent from each other. The current on the AC-side is measured and in combination with the battery modules' SoC and their voltages is fed to the DC-side in a similar way as presented in the H-bridge inverter. Depending on the used modulation, different current multiplications are required and discussed in the next section.

8.3 Behavioral Modeling of the Modulation Techniques

The behavioral modeling of the modulation techniques PSPWM, PD-LSPWM, NLC, and SVM is discussed and compared to each other in this section. On system-level, no modulators are used and their behavioral modeling of the modulation's effects is introduced. The effect of the modulation techniques can be recognized only on the inverter's DC-side. Its AC-side remain in all modulation techniques on system-level identical.

8.3.1 Implementing PSPWM on System-Level

The PSPWM allows an equal discharging of the battery modules due to the shifting of the carrier-signals on circuit-level as shown in the last chapter.

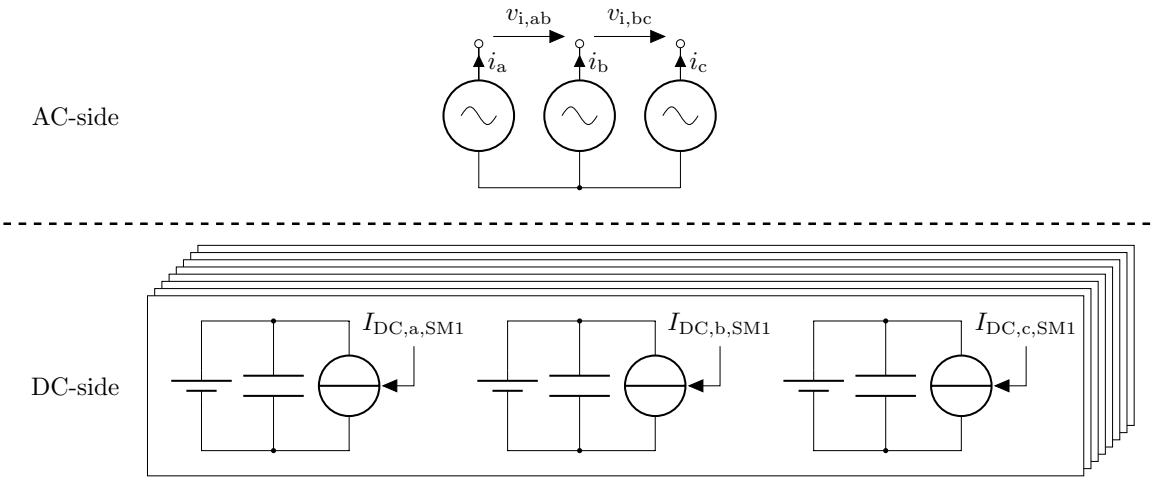


Figure 8.3 – Average model of the 17-level CHB three-phase inverter on system-level.

The carrier-signal's shifting leads to equal surfaces under the DC-link current curves and may be neglected. On system-level, the reference signal for the controlled current sources on the submodule's DC side is calculated by dividing the AC power by the sum of the battery modules' voltages in each phase. For the charging and discharging operation, the final results are multiplied with the actual d-component of the grid current I_{d} in per unit as shown in Eq. (8.2).

$$I_{\mathrm{DC,a,SM1-8}} = \left| \frac{i_{\mathrm{a}} \cdot v_{\mathrm{a}}}{\sum V_{\mathrm{SM1-8}}} \right| \cdot \frac{I_{\mathrm{d}}}{I_{\mathrm{d,nom}}} \tag{8.2}$$

To explain the different discharging of the submodules when average modeling are used, the surfaces under the DC-link currents generated on system- and circuit-level are compared to each other.

8.3.2 Implementing PD-LSPWM and NLC on System-Level

Due to the inverter's switching frequency using LSPWM, the results using the three different modulation's types (PD, POD, and APOD) are almost similar. Therefore, only one, the PD-LSPWM, is followed.
The effect of the PD-LSPWM and NLC modulation techniques on the battery modules' side is similar. Therefore, both modulations are modeled in the same way on system-level. Furthermore, both modulation techniques lead to an unequal discharge of the battery modules of the 17-level cascaded H-Bridge inverter.
Using PD-LSPWM or NLC on circuit-level, the reference signals at the controller output are divided into levels. The number of voltage steps in a 17-level CHB inverter varies from 13 to 17 depending on the *SoC* of the battery modules as shown in [100].
Depending on the sum of the DC-link voltages, only several submodules are active and the current flows through their batteries. This operation leads to inactive battery modules, e.g. submodule seven and eight. In 13-level operation using PD-LSPWM and NLC, the battery modules of the last two submodules are not discharged because the controller's reference signal is lower than 6 pu. Therefore, in the case of PD-LSPWM or NLC, the reference signal

for the DC-link current sources is divided by the sum of the DC voltages and then multiplied by the actual current value.

8.4 Efficiency Modeling on System-Level

The assessment of the simulation on system-level is done using simulations on circuit-level. Furthermore, the inverter efficiency can be implemented using characteristic diagrams between the measured AC current and the reference signal for the DC-link current sources. The efficiency data are imported from simulations on component-level, as done on circuit-level.
The inverter's efficiency in charging η_{charging} operation differs from the discharging $\eta_{\text{discharging}}$ operation. On the AC-side, the current is controlled and is therefore always constant in models on system-level. During the charging operation of the BESS, losses occur in the inverter. Therefore, the DC-power stored in the battery modules is slightly lower than the AC-power as described in Eq. (8.3).

$$I_{\text{DC}} = \eta_{\text{charging}} \cdot |i_{\text{a}}| \cdot \frac{I_{\text{d}}}{I_{\text{d,nom}}} \tag{8.3}$$

During the discharging operation, slightly higher DC-power is required as shown in Eq. (8.4).

$$I_{\text{DC}} = \frac{|i_{\text{a}}| \cdot \frac{I_{\text{d}}}{I_{\text{d,nom}}}}{\eta_{\text{discharging}}} \tag{8.4}$$

The characteristic diagrams of power inverters differ between the charging and discharging operation. Using efficiency curves of the inverter allows the design of an energy management system for an efficient operation with equally discharged BESS even if different modulation techniques are used. In further analysis, no characteristic diagrams of the inverter's efficiency on system-level are implemented. Applying those diagrams increases the system operation's complexity and represents a challenge for the design of balancing algorithms for the proposed 17-level CHB inverter.

8.5 Simulation Results on System-Level

The results of the simulations on system-level are presented and compared to that from the circuit-level. The relevant comparison data for both simulation levels are the discharging time, the simulation time, the DC-link current waveforms including the surface under those curves, the SoC of each submodule's battery during a full discharging operation until at least one submodule reaches $SoC = 0\,\%$, and the remaining energy content of the BESS using PSPWM, PD-LSPWM, and NLC.
For all further simulations, the start SoC of all submodules is set to 100 %. The simulations are stopped whenever at least one submodule reaches the $SoC = 0\,\%$. Furthermore, no EMS unit is used at this stage to compare the effects of different modulation techniques on the BESS using 17-level CHB inverter. For the simulations on system- and circuit-level, the solver Euler is used at fixed simulation's time steps of 1 µs on system-level and 100 µs on circuit-level.

Table 8.1 – Simulation duration on system- and circuit-level [101].

Simulation duration	PSPWM	PD-LSPWM	NLC
System-level	0.97 h	1.65 h	1.58 h
Circuit-level	320.88 h	391.2 h	283.92 h

8.5.1 Simulation Duration

The validation of the results on system-level and comparison of the simulation duration are done using models from the circuit-level. The validation using models on circuit-level leads to simulation duration of up to 18 days. It shows that switching models are not suitable to be used for long-term simulations. Table 8.1 summarizes the simulation durations on system- and circuit-level. The difference in the simulations at the same level is due to the model complexity and the implementation of the modulation techniques. Using the highest abstraction level shortens the physical simulation duration in all modulation techniques. Using PSPWM, PD-LSPWM, and NLC the simulation is more than 330, 237, and 179 times faster than the simulation on circuit-level, respectively.
Increasing the abstraction to the simulation on system-level reduces the simulation durations up to 330 times compared to the simulation on circuit-level and allows long-term operation's prediction of the behavior of the storage system. However, the discharging time using e.g. PSPWM in system- and circuit-level are similar. The simulation of one discharging period of more than two hours is achieved in less than two hours (0.97 h, 1.65 h, and 1.58 h using PSPWM, PD-LSPWM, and NLC respectively.). Therefore, a real-time operation can be achieved using such average models on system-level.
In addition to the comparison of the simulation duration, the DC-link current waveforms, the discharging time, the SoC, and the remaining energy content using different modulation technique are further handled.

8.5.2 DC-Link Current Waveforms

DC-link current waveform on system-level Using simulation on system-level leads to the DC-link currents shown in Fig. 8.4. The current waveform using PSPWM is identical for all submodules. Using PD-LSPWM and NLC, the submodules seven and eight are not discharged as in simulations on circuit-level.

DC-link current waveform on circuit-level The DC-link currents of the battery modules are analyzed and compared in simulations on system- and circuit-level. In Fig. 8.4 and 8.5 (a), the submodules' DC-link currents using simulations using PSPWM are shown on system- and circuit-level, respectively. All submodules are discharged at the rated current. Due to the operation of this modulation technique as explained in the Chapter 7, the battery modules are equally discharged. In Fig. 8.4 and 8.5 (b), the submodules' DC-link currents at system- and circuit-level using PD-LSPWM at nominal operation are shown. In this case, the submodules seven and eight are not discharged until the battery voltages of other submodules drop down. This behavior is similar using NLC as shown in Fig. 8.5 and 8.4 (c).
Furthermore, the current-time surfaces on system- and circuit-level are calculated and compared to each other.

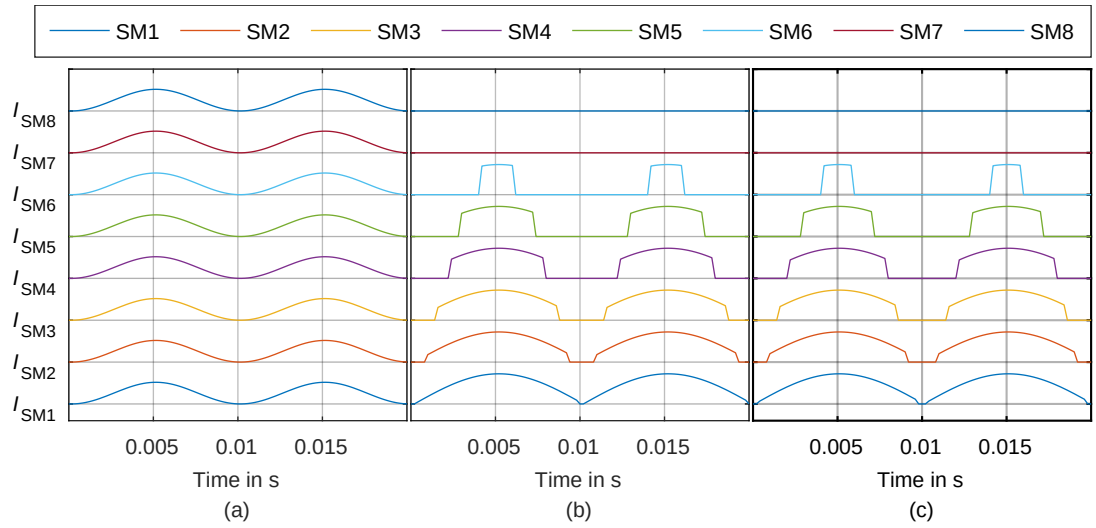


Figure 8.4 – DC-link current of the submodules of phase a using simulation on system-level using: (a) PSPWM, (b) PD-LSPWM, and (c) NLC.

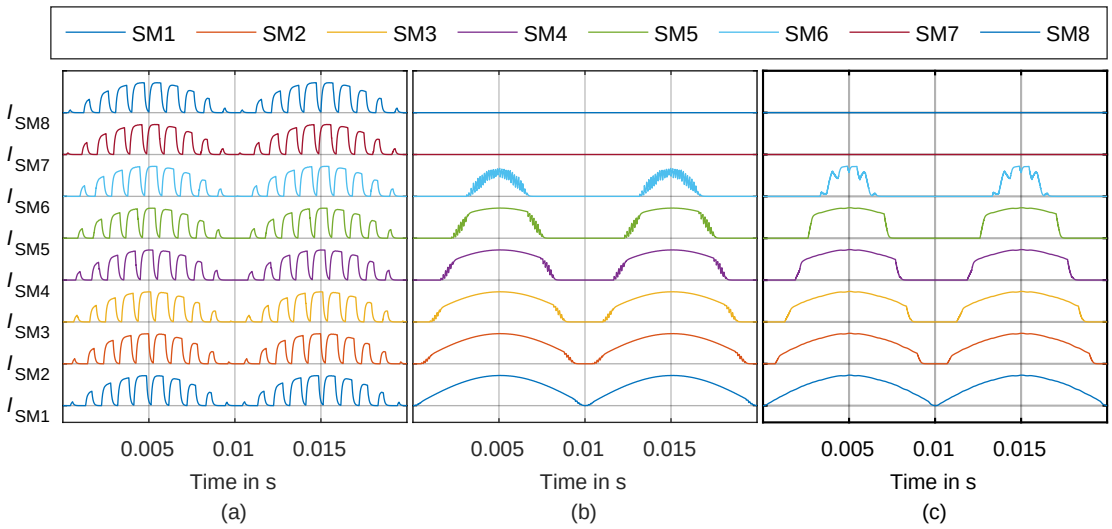


Figure 8.5 – DC-link current of the submodules of phase a using simulation on circuit-level using: (a) PSPWM, (b) PD-LSPWM, and (c) NLC.

Table 8.2 – DC-link current-time surface using different modulation techniques on system-level [101].

Submodule	**Surface in As**		
	PSPWM	PD-LSPWM	NLC
SM1	0.258	0.457	0.456
SM2	0.258	0.443	0.440
SM3	0.258	0.414	0.408
SM4	0.258	0.353	0.362
SM5	0.258	0.292	0.281
SM6	0.258	0.142	0.128
SM7	0.258	0.000	0.000
SM8	0.258	0.000	0.000
Total	2.0616	2.1025	2.0752

DC-link current-time surface on system-level Using the modulation techniques on system-level explained before, the DC-link current-time surfaces are summarized in Table 8.2.
Using PSPWM on system-level leads to exactly equal DC-link current waveform and therefore the same current-time surface. All submodules are equally discharged.
Using PD-PSPWM on system-level leads to DC-link current-time surfaces almost identical to those from the simulation on circuit-level. The current-time surfaces of submodules seven and eight at the given operation point are equal to zero.
The DC-link current-time surfaces for the NLC on system-level are similar to those of the PD-LSPWM and to those on circuit-level. The sum is also similar to the other results.

DC-link current-time surface on circuit-level Table 8.3 represents the DC-link current-time surfaces of the curves shown in Fig. 8.5 and 8.4. Using PSPWM, the DC-link current-time surfaces on circuit-level are almost equal to each other ($\approx 0.264\,\mathrm{As}$).
In the operation with PD-LSPWM the submodules seven and eight are not discharged and therefore the surface is equal to zero. The DC-link current-time surface of submodule one is three times higher than this of submodule six. Therefore, submodule one operates in each time period three times longer than the submodule six. Therefore, both submodules are not equally discharged.
The DC-link current-time surfaces using NLC are almost similar to those of the PD-LSPWM. They slightly differ from each other on circuit-level. However, the ratio of the operation between e.g. submodule one and six is similar.
The sum of the DC-link current-time surfaces using the different three modulation techniques is similar, because the inverter delivers the same rated power on the AC-side.
In the next step, the unequal discharging of the battery modules is explained by analyzing the long-term simulation results such as the BESS's discharging time and the resulting difference in the SoC.

8.5.3 Discharging Time

The time required for discharging the whole BESS calculated by dividing the nominal energy content of the storage $E_{\mathrm{BESS,nom}}$ by the nominal inverter power $P_{\mathrm{BESS,nom}}$ is studied and later

Table 8.3 – DC-link current-time surface using different modulation techniques on circuit-level [101].

Submodule	Surface in As		
	PSPWM	**PD-LSPWM**	**NLC**
SM1	0.262	0.456	0.457
SM2	0.263	0.442	0.441
SM3	0.263	0.414	0.409
SM4	0.263	0.367	0.361
SM5	0.265	0.292	0.295
SM6	0.265	0.142	0.151
SM7	0.263	0.000	0.000
SM8	0.264	0.000	0.000
Total	2.110	2.112	2.115

compared to the discharging time from the simulation on system- and circuit-level.
The three-phases nominal BESS's AC-power using the 17-level CHB inverter $P_{\mathrm{BESS,nom}}$ is calculated as in Eq. (8.5).

$$\begin{aligned} P_{\mathrm{BESS,nom}} &= 3 \cdot v_{\mathrm{g,a}} \cdot i_{\mathrm{a}} \\ &= 3 \cdot 230\ \mathrm{V} \cdot \frac{36\ \mathrm{A}}{\sqrt{2}} \\ &= 17564.5\ \mathrm{W} \end{aligned} \tag{8.5}$$

The rated energy content $E_{\mathrm{BESS,nom}}$ of the whole BESS is the sum of the energy contents of each submodule's battery ($E_{\mathrm{batt,nom}} = 36\,\mathrm{Ah}$) and is given in Eq. (8.6)

$$\begin{aligned} E_{\mathrm{BESS,nom}} &= n_{\mathrm{submodules}} \cdot E_{\mathrm{batt,nom}} \cdot V_{\mathrm{batt,nom}} \\ &= 24 \cdot 36\ \mathrm{Ah} \cdot 51.2\ \mathrm{V} \\ &= 44236.8\ \mathrm{Wh} \end{aligned} \tag{8.6}$$

Discharging the BESS at nominal power (discharge at 1C) leads to a discharging time of $t_{\mathrm{discharging}}$ as given in Eq. (8.7).

$$\begin{aligned} t_{\mathrm{discharging}} &= \frac{E_{\mathrm{BESS,nom}}}{P_{\mathrm{BESS,nom}}} \\ &= \frac{44236.8\ \mathrm{Wh}}{17564.5\ \mathrm{W}} \\ &= 2.52\ \mathrm{h} \end{aligned} \tag{8.7}$$

Using 1C discharge rate, the BESS needs 2.52 h to be fully discharged. This value is correct only with the assumption that all battery modules are equally discharged. Table 8.4 shows the simulation's stop-time on system- and circuit-level using different modulation techniques. Using a physical model for simulation on system-level, the first battery module reaches the $SoC = 0\,\%$ in case of PSPWM, PD-LSPWM, and NLC after 9113 s = 2.53 h, 5672 s = 1.58 h, and 5674 s = 1.58 h, respectively. The discharging time is defined in the simulation whenever at least one submodules's battery reaches $SoC = 0\,\%$. Using PSPWM on system- and circuit-level, the discharging times are 2.53 h and 2.5 h, respectively.

Table 8.4 – Simulation's stop-time using different modulation techniques on system- and circuit-level [101].

Simulation stop-time	PSPWM	PD-LSPWM	NLC
System-level	9113 s	5672 s	5672 s
Circuit-level	8995 s	5684 s	5688 s

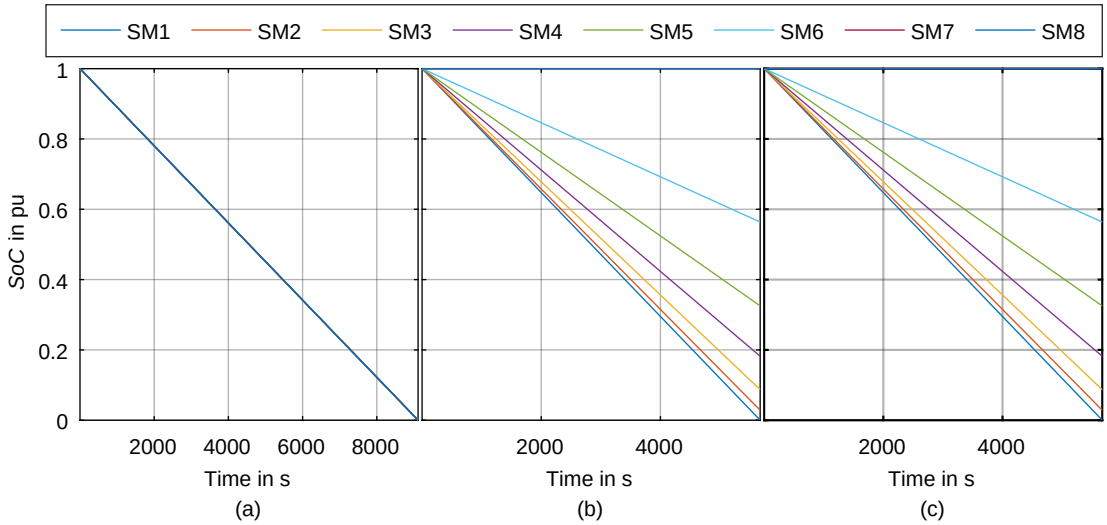


Figure 8.6 – State of charge of the battery modules of phase a using simulation on system-level using: (a) PSPWM, (b) PD-LSPWM, and (c) NLC.

8.5.4 State of Charge

In this section, the SoC of each submodule during one full discharging period until at least one submodule reaches $SoC = 0\,\%$ is analyzed.
Fig. 8.6 represents the SoC of the battery modules in one phase using (a) PSPWM, (b) PD-LSPWM, and (c) NLC on system-level. Those results confirm the simulations on circuit-level. The SoCs of all submodules are exact the same using PSPWM. Using PD-LSPWM and NLC on system-level leads to the same results when compared to each other. In contrast to the circuit-level, two submodules are not discharged ($SoC = 100\,\%$) due to the simplification of the model used. Fig. 8.7 represents the SoC of the battery modules in one phase using (a) PSPWM, (b) PD-LSPWM, and (c) NLC on circuit-level. The simulations are set to stop whenever one submodule reaches the $SoC = 0\,\%$.
The stop-time using PSPWM is higher than using PD-LSPWM and NLC. Using PSPWM, the SoC of all submodules are lower than $1\,\%$ and all submodules are discharged almost equally to each other at the simulation's stop-time. The usage of PD-LSPWM and NLC leads to fully discharged submodule one ($SoC = 0\,\%$) while the last one's $SoC = 100\,\%$.
The analysis of the SoC of the battery modules on system- and circuit-level shows that the BESS stops its operation while some submodules are still fully charged and the available BESS energy content is not exploited effectively.

Balancing methods Therefore, it is not recommended to use the PD-PSPWM and NLC without a balancing algorithm which, e.g. changes the sequence of the battery modules. Management algorithms for CHB inverters are suggested in [60], [59], and [40]. A periodic

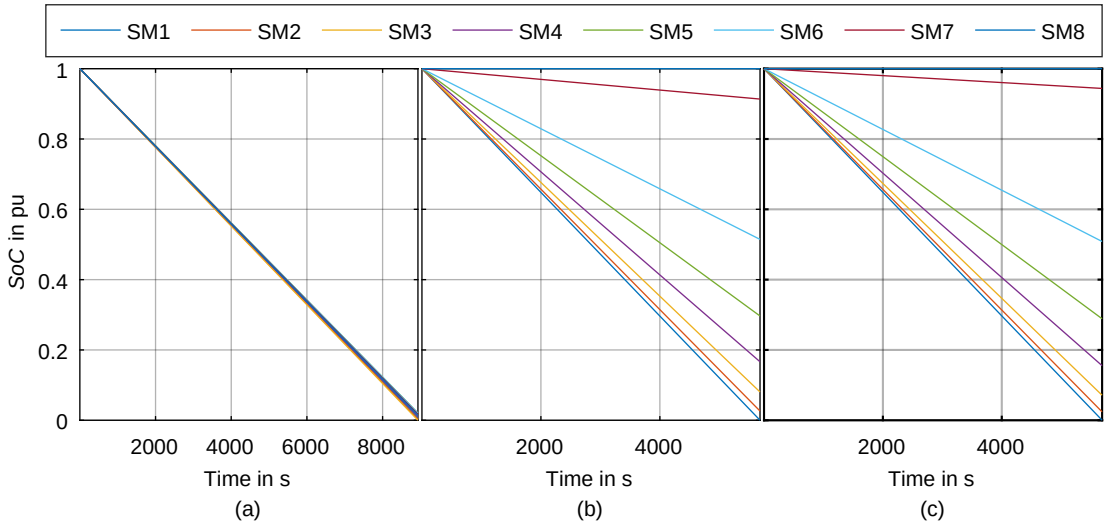


Figure 8.7 – State of charge of the battery modules of phase a using simulation on circuit-level using: (a) PSPWM, (b) PD-LSPWM, and (c) NLC.

rearrangement of the operation range is used to reach balanced SOCs between the submodules over time. Using such intelligent balancing methods, the PD-LSPWM and NLC get more interesting due to their easy hardware implementation.

Furthermore, one commonly used balancing method uses the sorting of the DC-link voltages. The submodule with the highest voltage or SoC is selected to be first discharged as in [121], [4], and [143].

The literature [121] presents also a simplified method for balancing based on sorting the submodules' voltages.

Furthermore, using different modulation techniques, the performance and requirements on the EMS differ. In the next section, the remaining SoC related energy content in each submodule is presented.

8.5.5 Energy Content

At the simulation's stop-time on system-level, the remaining energy content of the battery modules of phase a using PSPWM, PD-LSPWM, and NLC are presented in Table 8.5. Similar to the resulting SoC, the energy content remaining in the BESS is the lowest using PSPWM. Only 6 mAh are remaining in each submodule. The usage of PSPWM leads to fully discharging the whole BESS. The remaining BESS's energy content at the stop-time is negligibly small $E_{\text{end}} = 48\,\text{mAh}$. This value represents less than 0.01 % of the nominal energy content of the BESS.
The both right rows of Table 8.5 are similar. The remaining energy content of each submodule using PD-LSPWM on system-level is similar to the one when NLC is used.

Table 8.5 – Remaining energy content of the battery modules in one phase on system-level.

Submodule	**remaining energy content in Ah**		
	PSPWM	PD-LSPWM	NLC
SM1	0.006	0.012	0.012
SM2	0.006	1.03	1.03
SM3	0.006	3.14	3.14
SM4	0.006	6.56	6.56
SM5	0.006	11.71	11.71
SM6	0.006	20.3	20.3
SM7	0.006	36	36
SM8	0.006	36	36
Total	0.048	114.74	114.74
%	0.017	39.84	39.84

Table 8.6 – Remaining energy content of the battery modules in one phase on circuit-level.

Submodule	**remaining energy content in Ah**		
	PSPWM	PD-LSPWM	NLC
SM1	0.28	0.01	0.01
SM2	0.12	0.95	0.86
SM3	0.01	2.9	2.57
SM4	0.4	6	5.6
SM5	0.74	10.68	10.4
SM6	0.73	18.52	18.31
SM7	0.61	32.89	33.98
SM8	0.51	36	36
Total	3.4	107.95	107.72
%	1.1	37.48	37.40

The corresponding results from the simulations on circuit-level are shown in Table 8.6.

In the table's last line, the percentage value relative to the nominal energy content of the battery modules $E_{\text{batt,nom}}$ is shown.
Using PD-LSPWM or NLC, the remaining energy content at the simulation's stop-time is about $E_{\text{end}} = 40\,\%$ without using any balancing unit.
The submodules seven and eight still contain the nominal energy content while submodule one is at $E_{\text{SM1}} = 0\,\%$.

Using PD-LSPWM and NLC on circuit-level, the 7^{th} submodule is discharged until $SoC = 91.4\,\%$ due to the slightly higher DC-link current-time total surface. The small difference leads to higher discharging the whole BESS on circuit-level as shown in Table 8.6. The BESS's SoC at the simulation end is $SoC_{\text{BESS}} = 37.48\,\%$. It is lightly higher than the BESS's SoC on system-level where $SoC_{\text{BESS}} = 39.84\,\%$. However, the average model is used for approximating the inverter's operation and its effect on the BESS's discharging.
The simulations on circuit-level can be used as a comparison, however it also depends on the

exactness of the simulation as previously shown in the last chapter. The hardware implementation shows difference to the simulation on circuit-level during the inverter operation.

8.6 Summary

Using the introduced three simulation abstraction levels, on component-, circuit-, and system-level, the design of the inverter is done and enables the opportunity to analyze the system from different points of view. Those abstraction levels are helpful for different use cases during the implementation phase. The different simulation levels are presented and categorized for different use cases and complement each other. This chapter focuses on the highest abstraction level for long-term operation modeling of the BESS. Using average models shortens the simulation duration and allows the design of other BESS components, mainly the EMS balancing algorithm in case of CHB multilevel inverters.
The simulations on the highest system-level reduces the simulation duration by a factor of up to 370 compared with simulations using the switching models of the inverter. The simulations on circuit-level are used as a reference to validate the results of the models on system-level.
The behavioral modeling of power inverter is presented in this chapter and its goals are shown. The model of an H-bridge inverter is used to introduce the average modeling and its function. The inverter's AC-side is represented by a controlled voltage source and the DC-side by a controlled current source.
Furthermore, the average model of the B6-bridge inverter is shown. It uses three controlled AC voltage sources and one unique DC-link controlled current source.
The modeling of the 17-level CHB inverter combines both mentioned average models. On its DC-side, it is similar to the single-phase H-bridge inverter and on its AC-side to the three-phase B6-bridge inverter. The reference signals for the controlled voltage sources on the AC-side are independent from the used modulation techniques on system-level. The DC-link current highly depends on the used modulation technique. This is why the simulations on system-level are highly interesting to be used in CHB multilevel inverter to investigate the unequal discharging of the battery modules in long-term operation.
The modulation techniques PSPWM, PD-LSPWM, and NLC are implemented and introduced on system-level and their effects on the battery modules are analyzed. Since no switching behavior and no modulator is used on system-level, the signals for the controlled current sources are generated depending on the AC current.
Behavioral modeling allows to analyze the inverter efficiency. Furthermore, the efficiency of the CHB inverter depends on its operation and the actual AC current. It can be represented on system-level using characteristic diagrams from component-level.

To validate the models presented on system-level, the simulations implemented on circuit-level are used. The DC-link current waveforms and the DC-link current-time surfaces using simulations on circuit-level show a small difference to the results using average models. This leads later in long-term simulation to differences in the results. However, the average models enable implementing EMS algorithms, which are able to handle or rather eliminate those inequalities.
The BESS's discharging time is calculated by dividing the nominal energy content and the nominal power and compared to the simulation results on system-level. The BESS's operation time calculated is similar to the discharging time when PSPWM is used.

Since the simulations stop whenever at least one submodule reaches $SoC = 0\,\%$, there is a difference between the PSPWM and both of the PD-LSPWM and NLC. With both modulation techniques, this is the case after shorter time and before the BESS is totally discharged. Therefore, the total energy content of the BESS is not effectively used without using an EMS for balancing and correcting this difference.
Furthermore, the SoCs and the remaining energy content at the simulation's stop-time on system- and circuit-level are compared to each other.
Only using the PSPWM, total energy content of the BESS is used and at the simulation's stop-time the SoC is lower than $1\,\%$. Using other modulation techniques leads to total BESS's SoC of about $40\,\%$.
The exactness of the presented average models is not totally identical to the models on circuit-level. However, the exactness is enough to represent the operation of the BESS based on 17-level CHB inverter. Using average models of PSPWM, PD-LSPWM, and NLC leads to small differences in the DC-link current-time surface which by itself leads to deviation in the results in the long-term simulation. However, those models are suitable for testing EMS algorithms to balance the battery modules in the 17-level CHB inverter.

9 Conclusions

9.1 Summary and Results

A cascaded H-bridge inverter to be used in a battery energy storage system and connected to the low voltage grid is designed based on simulations at different abstraction levels.
Stationary and mobile energy storage systems are increasing revolutionary in recent years. Therefore, the research and development of efficient power electronics systems, such as inverters, is becoming more crucial. In grid connected stationary storage systems, the efficiency should be kept as high as possible because it is bidirectional and losses occur by charging and discharging the storage units. Therefore, their round trip efficiency highly decreases.

The usage of energy storage systems will play a bigger role in the future of low voltage power grids. The state of the art in the field of battery energy storage systems is presented and the components of such system are explained. The diverse application fields of grid connected battery energy storage systems indicate that their efficiency must be increased.

The focus is thereby given to the power electronics and their efficiencies, scalability, fault tolerant operation, decentralized storage modules, and redundancy.

The grid connected classical topologies show several advantages while connecting the BESS to the low voltage power grid. The power range limitation given by the usage of single phase systems can be bypassed using three-phase power inverters. However, the efficiency of these systems is limited by the development of the power semiconductors technology. The failure of one component leads to a total power inverter's failure and immediate disconnection from the power grid.
The usage of multilevel inverters for the low voltage application promises higher efficiency and reliability compared to the classical topologies. They use a higher number of smaller devices for transferring higher power instead of using a lower number of high power devices. The resulting multilevel inverter's higher costs must be compensated by the system benefits.

Multilevel inverter topologies are usually used in medium and high power systems, where the power of three-phase B6-bridge inverters is limited and the voltage range can not be further increased. Using serial connection of power semiconductors, multilevel inverters offer the possibility to operate with power semiconductors of the low voltage range in applications with higher voltage range. Different topologies offer different advantages and are suitable for difference use cases at different voltage ranges. For stationary energy storage systems, different multilevel inverter topologies are compared to each other. The CHB inverter topology shows superior advantage for the usage in BESS in low voltage grid applications. This topology is further selected to be used with split battery modules which use a voltage range lower than

the standards' extra low voltage.
The selected multilevel CHB inverter's number of voltage levels depends on its DC-link voltages. Using battery modules, the DC-link voltage varies in a given range and therefore the number of levels delivered by the CHB inverter differs. To avoid this voltage change, different submodules' topologies are studied. The single-stage topology uses only one H-bridge inverter in each submodule. The two-stage topology uses additionally DC-DC converters. The topology using a step-up DC-DC converter increases the DC-link voltage and therefore decreases the levels of the CHB inverter's voltage. The second two-stage topology uses step-down DC-DC converter and allows higher number of voltage levels. Therefore, more submodules are required and the system's reliability increases.
However, additional DC-DC converters in the submodules decrease the CHB inverter's efficiency. Therefore, the one-stage topology is preferred and selected.

The selected submodule topology consists of an H-bridge inverter and offers the highest possible efficiency using the selected multilevel inverter topology and is further simulated on component-level.
The simulation on the first and depth abstraction level focuses on the modeling of the losses of the power switches. In the case of the selected CHB inverter topology, power MOSFETs are most suitable. Their losses are calculated using dynamic models of the power semiconductors. The efficiency of one submodule is calculated and validated using hardware measurements. Furthermore, the power filter's losses are added to calculate the total CHB inverter's efficiency. The hardware validation shows a maximal efficiency of the used H-bridge of 99.4 %. In addition to the filter losses, the CHB inverter maximum efficiency is 99.36 %.
The results from component-level serves, inter alia, the efficiency studies on the next higher abstraction level such as the circuit- and system-level.

The simulation on component-level requires higher computation power and is therefore suitable for power loss calculation of the power semiconductors during the switching-on and -off time. The next abstraction level is called circuit-level. The whole CHB inverter is simulated using H-bridge inverters with ideal switches to speed up the simulation run-time while keeping the system dynamism and switching behavior.
The effects of the inverter depend on the used power grid model used on circuit-level. Different grid models are presented and show different behavior while connecting the CHB inverter. The weak grid model delivers nearest results to the measurement and is selected to be used in further simulations.
The CHB inverter model used on circuit-level is called switching model. Therefore, the modulation techniques are studied and compared to each other on this level. The PSPWM shows superior results in terms of efficiency and an equal discharge of the battery modules.
The definition of the modulation technique or rather the inverter switching frequency allows the power filter's design on circuit-level. For this purpose different filter circuits and topologies are analyzed and compared to each other. The filter design methods are shown and the current ripple method is used to calculate the filter's inductance. For CHB inverters, only the simplest L-filter is needed to fulfill the grid requirements as shown in the physical simulations. The filter internal resistance is then selected using the power filter hardware as a reference.
The definition of the switching frequency and filter inductance is followed by the controller design. Different methods show that the controller design is a trade-off between different criteria depending on the system. The vector oriented control is used due to its simplicity

and independent control of the active and reactive power of the BESS.
The simulation model of the CHB inverter on circuit-level is used to validate the system stability and its step response for a reference value change. Furthermore, the steady state operation using the discussed modulation techniques is presented and the results are compared to each other.
Finally, the hardware and measurement results are shown to validate the shown simulations on circuit-level.

BESSs operation is generally in hours-range and can not be simulated using the inverter's switching model on circuit-level. The simulations on system-level are suitable for the long-term operation modeling of the selected CHB inverter topology using split battery modules.
Especially for the selected topology, the split battery modules can be differently discharged depending on the modulation technique used. The simulations on system-level use average models of the inverter and neglect the switching behavior of the inverter. The simulation's run-time is up to 370 times shorter than the simulation on circuit-level.
The average models are also used to predict the inverter behavior at different conditions and to design possible energy management system's algorithms. The results presented using average models are finally validated using simulations on circuit-level.

To conclude, the usage of simulation on different abstraction levels allows reducing the complexity of the CHB inverter and to study different aspects regarding the efficiency, the system dynamism, and long term BESS's operation. The presented simulation levels cover the CHB inverter operation from the switching analysis of one MOSFET in µs and its losses produced up to the operation in hours-range of the whole studied 17-level CHB inverter on system-level using averaged models. On circuit-level, the inverter model provides the software-part used to control the inverter while implementing the hardware.

9.2 Future Work and Recommendations

The research on multilevel inverter used to connect the BESS to the low voltage grid can be done on a wide scale and the aspects shown can be further expanded.

Switching frequency reduction and different MOSFET-packaging In the shown simulations and hardware measurements, the frequency modulation index m_f is set to 20. The usage of a switching frequency of a multiple of three and 50 leads to elimination of the odd harmonics. However, the THD increases due to the higher amplitudes of the uneven harmonics.
Furthermore, the switching frequency can be further reduced to achieve higher efficiencies. The power filter size will then increase.
Furthermore, the packaging of the used power semiconductors can be changed to reduce the internal resistance of the power switches and therefore further increase the inverter efficiency.
Furthermore, the usage of parallel connected power MOSFETs will decrease the conduction losses of the H-bridge inverters.

Voltage amplitude fluctuation In the norms, the grid voltage is allowed to vary in a tolerance band of up to ±10 % [72]. The simulations and operation shown assume a symmetric grid voltage. Whenever the CHB inverter operates at different grid voltage amplitudes, the control method must be updated to handle the different phase voltage amplitudes. One method is shown in [103]. The grid voltage fluctuation also affects the number of submodules required and the topology must be adapted for this BESS's operation.

Asymmetric current operation The extension of the presented symmetric vector oriented control to operate with different current amplitudes offers an additional degree of freedom, which can be considered by the design of new balancing algorithms. To operate the inverter with different phase current, the asymmetric current control using three-phase three-wire CHB inverter is shown in [98]. To operate the inverter with independent different phase currents, the star point of the inverter must be grounded and the operation using three-phase four-wire CHB inverter is also presented in [98]. The operation of these inverter configurations is simulated and validated in hardware [98]. Whenever the star point of the CHB inverter is used, one method propose the usage of Level Doubling Network to generates double number of levels using six additional power switches can be followed as suggested in[96]. The extension of the asymmetric current control using the single phase active and reactive power decoupled control is a further extension of the asymmetric operation [103].

Grid modeling The grid modeling approaches proposed using the ideal, the strong, and the weak grid models can be extended using the suggestions shown in [94]. The effects of different grid models on the inverter's operation can then be studied to reach nearest results to the hardware measurements.

Standards conform simulation The system complexity of the CHB inverter gets more interesting in failure cases. The simulations presented can be extended for a standards-conform operation in case of failure due to internal faults such as one switch damage. In case of external faults, the grid phase failure can be analyzed i.e. in case of short circuits. These failure analysis probably leads to damages if tested on the hardware.

Redundant submodules and reliability The CHB inverter can be used with a higher number of submodules than required to increase the system reliability and fault tolerance. On the other hand, the usage of redundant submodules increases the system failure probability.
The reliability of the multilevel inverter in combination with multiphase machine is shown in [20]. This study can be further analyzed in terms of using this topology for critical applications.

Different number of levels The suggested number of levels is optimized for DC-link voltage under the extra low voltage limits and to be connected to the low voltage power grid. Further optimization possibilities in a multilevel inverter for stationary energy storage in terms of the number of module and the control techniques can be studied using the methodology presented. The different abstraction-levels reduce the system complexity. A multi-criteria optimization problem is given by the selection of the power electronics topology and number of submodules.

The scalability of the inverter allows to scale the power and energy content of the inverter to be adapted for the different use cases.

Electromagnetic compatibility Due to its decentralized structure, the electromagnetic compatibility (EMC) of the CHB inverter must be kept in mind while implementing in hardware and using the centralized PWM generation. The decentralized hardware structure of the CHB inverter make it sensible for EMC problems.
The usage of fiber optic cables helps to increase the system robustness against EMC distributions.

Decentralized PWM generation The used control method proposed consists of a central unit, which delivers the pulses for all power switches. It offers high implementation simplicity but lowest fault tolerant possible. The usage of decentralized system to i.e. locally generate the pulses can be followed to increase the system modularity and scalability. The suggestions shown in [104] and [106] can be further followed and examined.

EMS balancing algorithms The realized hardware can be used as a platform to implement EMS's balancing algorithms to equally discharge the BESS and optimize the usage of its energy content. A possible algorithm to be followed is published in [60].

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