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Markets for Technology in the Semiconductor Industry – The Role of Ability-Related Trust in the Market for IP Cores

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List of abbreviations

AM	Additive Manufacturing
ARM	ARM Holdings PLC
ASIC	Application Specific Integrated Circuit
CAGR	Compound Annual Growth Rate
CPU	Central Processing Unit
EDA	Electronic Design Automation
ERP	Enterprise Resource Planning (software), e.g. by SAP
FPGA	Field Programmable Gate Array
GPU	Graphics Processing Unit
HHI	Herfindahl-Hirschman Index – a measure of industry concentration
IDM	Integrated Device Manufacturers
IP	Intellectual Property
IPR	Intellectual Property Rights
MfT	Market(s) for Technology
PCB	Printed Circuit Board
PPA	Power, Performance, Area, the primary statistics of a computer chip
PPE	Plant, Property, Equipment – also known as tangible fixed assets in a balance sheet
R&D	Research and Development
RTL	Register Transfer Level
SCPA	Semiconductor Chip Protection Act
SoC	System on a Chip
TCE	Transaction Cost Economics
TRIPS	Trade-Related Aspects of Intellectual Property Rights
WTO	World Trade Organisation

Abstract

The iPhone is one of the most popular products of our time with sales exceeding 230 million units and associated revenue of more than 155 billion USD in 2015. It is a showcase of the power of Markets for Technology (MfT) with both its processing (CPU) and graphics unit (GPU) delivered as blueprints, so-called IP Cores, by companies that do not deal in products but instead focus exclusively on developing and licensing technology. Considered strong enablers for the global innovation landscape, MfT—such as the market for IP Cores—are also quite elusive. The market for IP Cores is an interesting research subject specifically because it is representative of the understudied MfT that deal in blueprints rather than patents and fulfills a vital role for the entire semiconductor industry. Most importantly, it functions well, yet has received little attention due to its secretive nature.

Due to the limited prior research into the stability of this type of market, this study used 38 semi-structured interviews with leading managers of buyers and sellers of technology combined with datasets on market shares and patenting intensity to analyze the market.

The research revealed several unexpected aspects of the market for IP Cores. First, despite being stable and experiencing continuing growth, the market is still subject to one of the difficulties associated with MfT, extreme volatility of price. However, results show this issue does not bear the same destructive potential in the market for IP Cores as in other MfT since customers do not use it as their primary evaluation criterion. Rather, when faced with the high-risk choice of technology, which buyers are unable to evaluate prior to purchase and which has potentially disastrous consequences when flawed, buyers of IP Cores choose a provider based on trust. Additionally the market for IP Cores features high transaction costs along several dimensions, most notably uncertainty and asset specificity, which should lead to internalization but do not. Finally this research finds that while patent protection—which is considered crucial by the prior literature in facilitating the technology transaction—is available to sellers of IP Cores, sellers do not connect it to the licensing transaction in any way, nor do they exhibit a higher patenting intensity than comparable companies dealing in products. This may be due to the widespread use of alternative protection mechanisms such as third-party verified encryption.

This thesis extends the theory by highlighting the importance of trust in transactions involving *ex ante* difficulty to evaluate the quality and high cost of reversal, the robustness of MfT in the face of high transaction costs, and the substitutability of patent protection by technological means.

1 The Market for IP Cores – A Market for Technology at the Core of the Semiconductor Industry

One of the most popular products of our time, with sales exceeding 230 million units and associated revenue of more than 155 billion USD in 2015 (Apple 10-K, 2015), the Apple iPhone uses a Central Processing Unit (CPU) by ARM Holdings PLC (ARM) for the calculations and a Graphics Processing Unit (GPU) by Imagination Technologies for the visualization (arstechnica, 2016; wccftech.com, 2016). These companies are unique in that they do not deal with products, but rather they sell blueprints for parts of computer chips—so-called IP Cores—to other companies that subsequently integrate them into their overall computer chips and sell these to their customers. Furthermore, this example is representative of a major trend in the semiconductor area where, by current estimates, some 75% to 80% (interviewee K and interviewee M[1]) of all computer chips contain third-party IP Cores, up from about 50% four years ago (interviewee M). This proliferation of the integration of third-party IP Cores has made ARM so successful that even Intel, a longstanding rival in mobile computing that is following the traditional model of selling physical chips, has recently announced that it will provide support for ARM processors in its foundry[2] division due to ARM's success (EE Times Europe analog, 2016; fortune.com, 2016a, 2016b; pcworld.com, 2016).

1.1 Motivation

The strong adoption of third-party provided technology through IP Cores in the semiconductor industry is in line with a large volume of academic literature that acknowledges the benefits of MfT in general (e.g., Arora et al., 2001a; Arora, 1995; Arora and Gambardella, 2010; Cockburn et al., 2010; Gans and Stern, 2010; Hicks and Hegde, 2005; Teece, 1986).

Nonetheless there is an increasing number of scholars asking why MfT "are relatively uncommon" (Gans and Stern, 2010, p. 806), even wondering whether MfT are

[1] All information citing "interviewee X" stems from the interviews performed as part of this thesis. Appendix A2 provides a short overview of the role of the anonymized interviewees quoted throughout the thesis.

[2] The term foundry refers to providers of manufacturing capacity to enable outsourcing of production. In the case of Intel, it uses its manufacturing division to produce its own chips, and makes excess capacity available to external chip manufacturers.

"prone to failure" (Agrawal et al., 2014, p. 1) or if MfT "carry the seeds of their own destruction" (Arora and Gambardella, 2010, p. 795).

The market for IP Cores presents an exceptional research object because it enables a clean observation of the opportunities and limitations of being a seller of technology because the majority of providers of IP Cores are dedicated technology providers, unlike the majority of companies that license patents. This dedication to technology development also provides a unique setting for studying multiple aspects of technology providers such as revenue generation and the objective observation of the role of patent protection through analysis of the company-level filings rather than through surveys, thus eliminating multiple possible sources of bias and error.

Due to the limited amount of prior literature on this question and on the setting of technology licensing not based on patents but on blueprints, this study employed an exploratory qualitative analysis following a multiple case study approach building on an extensive set of 38 semi-structured interviews across providers, intermediaries, and buyers of IP Cores. Quantitative insights gained through examining the only long-term dataset on the performance of this market enhance these finding. The qualitative nature of the research enabled the gathering of rich, contextual information on the research questions and the identification of new patterns in MfT that promote their viability and provide the basis for quantitative verification in future research. Triggered by unexpected insights on the role of patents through the interviews, I conclude with a quantitative study that compares the patenting intensity of similar companies that operate on opposite sides of the divide between MfT and product markets.

This research contributes to the understanding of MfT in a number of areas. Through the systematic evaluation of the proposed sources of non-viability of MfT (Agrawal et al., 2014; Arora and Gambardella, 2010; Gans and Stern, 2010). The inherent uncertainty of the technology being traded—an understudied element of MfT according to Arora and Gambardella (2010)—is identified as a potent enabler. The importance of the encountered technological risk, not accounted for in the established, relational trust-model, highlights the role of ability-related trust for transactions in the market for IP Cores. In short, the primary burning question of buyers of IP Cores is not whether the seller of an IP Core CHOOSES to not deliver the required quality, but whether it is at all ABLE to do so. Using the unique setting of an MfT dealing in blueprints rather than patents, the study investigates the role of patent protection for facilitating technology

transfer without the distorting influence of transactions realized through patents.

1.2 Research question

The research questions started off as being very broad "How does the market for IP Cores work" since it represented a somewhat secretive[3] representative of the understudied MfT that do not deal in patents but rather perform technology transactions via blueprints, which are akin to computer programs. This was refined by the question "how does it manage to remain stable" followed by "how do buyers of IP Cores evaluate and choose their supplier," and eventually concluded with the final question of "how do sellers of IP Cores build trust into their product and what is the risk that buyers are concerned about" (Chapter 5). During the research, several interesting side topics opened up, two of which are also addressed in this dissertation, namely: "What role does patent protection play in this non-patent based Market for Technology" (Chapter 6) and "how does the market structure differ compared with a reference product market" (Chapter 4). Finally, the findings of the market for IP Cores made it possible to answer the question "which theoretical insights beyond the market for IP Cores can be generated based on the findings of this market?"

1.3 Structure

The dissertation continues as follows: Chapter 2 provides an overview of the existing literature on MfT and provides an overview of the market for IP Cores including a deep dive on the technological peculiarities required to understand the market performance. Chapter 2.3 discusses the available methods for performing exploratory research and details the two most common frameworks of qualitative research by Eisenhardt and Gioia before discussing this study's approach. Chapter 4 contains bespoke analysis of market and provider characteristics including concentration and revenue variance in comparison with an adjacent product market based on the only database available on the market for IP Cores by Gartner (2007 - 2015a). Chapter 5 introduces the concept of technological risk and the resulting ability-related trust as an enabler for MfT

[3] A senior scholar knowledgeable about the industry used these words to describe his experience with the market, "The main challenge is (I think) getting access to data about this market, which is generally private and considered sensitive."

followed by a brief consideration of a transaction cost perspective on the market for IP Cores and the resulting implications. Chapter 6 addresses the question of the role of formalized patent protection in a market where such protection is clearly applicable but not mandatory to facilitate technology transfer. Finally, Chapter 7 sums up the various insights generated into the market for IP Cores and contains an outlook on areas for future research.

2 Literature review

Before discussing the research and findings of this study, overviews of prior literature for the relevant topics of MfT (2.1), the object of observation, the market for IP Cores (2.2), as well as of the prior literature on organizational trust (2.3) are set forth.

2.1 Markets for Technology

Technology as the object of trade of MfT is broadly defined by Arora and colleagues (2001a) as covering concrete 'technology packages' (such as blueprints) and also patent licensing and the trading of abstract ideas (Arora et al., 2001a; Gans and Stern, 2010) with the majority of research into MfT focusing on patent licensing (Arora, 1997; Cockburn et al., 2010; Fosfuri, 2006; Gans and Stern, 2010; Grindley and Teece, 1997; Hall and Ziedonis, 2001) due to the high incidence of patent licensing and a relatively good data availability. Arora, Fosfuri, and Gambardella (2001a) further distinguish between markets where buyers and sellers are rivals (horizontal market) or upstream/downstream companies (vertical market), as well as the timing with a distinction between existing technologies and those for future technologies. In the case of IP Cores, the most frequent case is that of existing technologies traded in a vertical market. Horizontal market transactions are rare due to the high cost of cannibalization since IP generally only achieves a low price compared with physical products (Arrow, 1962) (see also profit dissipation effect in Section 2.1.2). Transactions regarding future technologies are rare since one of the key reasons for sourcing IP Cores is the omission of development time for the technology (Tuomi, 2009). The only exception to this rule is a new entrant with an unrivaled technology that will partner with an established company as a primary customer in order to bring their technology to market readiness.

Prior to the conceptualization of MfT (Arora et al., 2001b) and the concept of Open Innovation (Chesbrough, 2006), the common understanding was that companies needed to combine institutionalized in-house research and development (R&D) with complementary assets for commercialization of technological innovations, a concept for managing innovations that was spearheaded in the early twentieth century by German chemical companies that dominated the next decades (Arora et al., 2001a). There are strong advantages to combining in-house R&D with investments in complementary assets like marketing and manufacturing (Chandler, 1990) such as the ability to differentiate on the developed technologies due to exclusive access. Therefore, some of the largest

companies still follow this approach.

However, in the last two decades several researchers started investigating the possibility of licensing externally developed technologies as an alternative model for gaining access to innovations (including Arora et al., 2001a; Arora, 1995, 1997; Bresnahan and Gambardella, 1997; Gans and Stern, 2010). Both theoretical considerations and observations of increasing technology exchange across firms drove this research into MfT.

Theoretical considerations include technology transfer being seen as a key variable in determining the rate of economic growth (Rosenberg et al., 1992) and, therefore, technology licensing, as an important means for transferring technology, should be seen as being in the interest of society as a whole (Arora, 1995). Additionally, in the spirit of the division of labor (Smith, 1776; Stigler, 1951), MfT have the potential to increase the efficiency of innovation through specialization and distribute the cost of development across an entire industry, reducing duplicate innovation efforts at the firm level (Arora et al., 2001a; Bresnahan and Gambardella, 1997; Hicks and Hegde, 2005). MfT also increase competition in markets by lowering entrance barriers, helping to shorten product life cycles by making technologies available to all companies that require them (Arora et al., 2001a; Arora, 1997), improving the allocation of funds across industry participants, and assisting in the promotion of efficiency at the firm level (Gans and Stern, 2010). Additionally, the availability of a market is seen as a significant enrichment of the strategic choices available to firms that no longer have to develop their own innovations but can rely on outside inventors or generate additional rents by licensing out their own technology (Arora et al., 2001a). This aspect is especially important for small research-focused institutions that lack downstream assets for commercializing technology and therefore are reliant on a MfT to generate rents from past innovations to fund future innovations (Arora, 1995; Hicks and Hegde, 2005; Teece, 1986)

Several researchers further substantiate these conceptual advantages by analyzing the impact of MfT on major economic revolutions driven by so-called general purpose technologies (e.g., the steam engine, computers). These technologies were so broad in their applicability that no single firm could reasonably fully exploit them leading to them being shared and licensed between firms, and even industries, long before the concept of MfT had been established (e.g., (Arora et al., 2001a; Arora and Gambardella, 2010; Bresnahan and Gambardella, 1997; Hicks and Hegde, 2005). For such technologies a market mechanism that helps connect them with the corresponding complementary assets

benefits both society as a whole and the individual firm providing the technology by generating licensing revenues on top of the revenues derived from internal utilization of the technology (Arora et al., 2001a; Gans and Stern, 2010).

Despite these advantages and areas of application, MfT are fraught with several difficulties. Technology providers need to strike a compromise between the economies of scale of the specialized organization and the lack of adaptation to the specific end user's needs (also called localization) (Bresnahan and Gambardella, 1997), thereby providing an upper limit to the size of these markets. Furthermore, the transfer of technology frequently requires additional transfer of tacit know-how, which gives rise to dual opportunism. Sellers of technology can reduce the amount of tacit know-how being transferred (due to quality of transfer being impossible to verify for outside parties) while buyers can reduce (or stop) payments upon transfer of the technology or know-how (Arora, 1995). While the first problem of localization vs. generalization is inherent in technology and cannot be solved, the issues around opportunism are addressable by spreading payments across the integration horizon (to increase the incentive of the seller to continue transfer) and combining them with patent protection (to stop the buyer from stealing technology) (Arora, 1995; Cockburn et al., 2010; Cohen et al., 2000; Fischer and Henkel, 2013; Hall and Ziedonis, 2001). In an effort to better understand why MfT are rare despite their apparent benefits, Arora and Gambardella (2010) and Agrawal et al. (2014) identified several reasons for non-viability for MfT that are evaluated in detail in Section 5.1.

Detailed discussions of two topics specifically relevant in connection with the MfT and this dissertation appear in the following subchapters: the role of patents in the MfT and the Transaction Cost Economic (TCE) perspective on technology transactions.

2.1.1 The role of patents in the Markets for Technology

The role of patents differs substantially between discrete and cumulative products (Anand and Khanna, 2000; Arora, 1995; Cockburn et al., 2010). Additionally, semiconductors are among the "strongest examples of cumulative system technologies" (Grindley and Teece, 1997, p. 10) . Analyses are as follows: the role of patents in cumulative industries in general, a closer analysis of the role of patents in safeguarding the licensing process, a short discussion of the potential drawbacks of relying overly on patent data when investigating technology transfer in MfT, and an overview of the alternative legal mechanisms available to protect IP applicable to the market for IP Cores.

Patents are traditionally considered an incentive to innovate for the individual inventor at the cost of a slower technology diffusion to society (Arora, 1995). Due to the plethora of existing literature on the general advantages and drawbacks of the patent system, this research will not elaborate on these (see e.g., (Fischer and Henkel, 2012; Gallini and Scotchmer, 2002; Hall and Ziedonis, 2001; Jell et al., 2016; Shapiro, 2001) and instead will focus on the literature investigating the role of patents in high technology markets and in MfT.

The Yale survey (Levin et al., 1987) found patent protection to be a weak means of appropriating rents in many high-tech industries which poses a challenge to licensors (Arora, 1997; Hall and Ziedonis, 2001). One reason for the low appropriability is the difficulty of monitoring and detecting patent infringement in industries where the technology is deeply embedded in the product (Gallini and Scotchmer, 2002; Grindley and Teece, 1997) rendering patent protection useless in cases where infringement cannot be proven or would be prohibitively expensive to detect, such as, for example, for algorithms optimizing the path length of the various connections on the semiconductor chips. Another issue regarding appropriability is the overlapping nature of patent claims in many cumulative high-tech industries where there is no clear primary owner leaving mutual infringement claims to be settled in court and frequently resulting in counter-lawsuits in reaction to an infringement suit (Shapiro, 2001). At the same time, the number of patents filed for in the semiconductor industry soared between 1979 and 1995, a phenomenon referred to as the 'patenting paradox.' While at first glance contradictory, two additional benefits of owning patents that do not rely directly on a strong appropriability mechanism explain this phenomenon. In cumulative[4] high-tech industries such as semiconductors, a large patent stock has been identified as a prerequisite to gaining access to competitors' technology through cross-licensing, which is essential due to frequently overlapping intellectual property rights (IPR) (Arora, 1997; Grindley and Teece, 1997). Another factor increasing the number of filings of patents is their use as a defense against hold-up in areas of highly fragmented technology markets (Hall and Ziedonis, 2001; Ziedonis, 2004).

Despite the detailed shortcomings of patents, the literature on MfT considers patents an effective means of facilitating licensing by reducing the threat of expropriation during

[4] I.e., industries in which many patents cover products, rather than just one, as would frequently be the case for novel molecules in chemistry.

exposure of technology to potential future licensees (Arrow, 1962; Gans et al., 2000). Other research identifies patents as a means to simplify contracts involving the need to exchange tacit know-how (Arora, 1995).

While patents are attractive to market participants as instruments for safeguarding their innovations, the usage of patents as a proxy for measuring the extent of technology exchange, as is done by a significant share of the literature on MfT, is not without issues. These issues include the substantial share of cross-licensing or *ex post* licensing after independent reinvention, which does not constitute technology transfer but rather ensures 'freedom-to-manufacture' (Fischer and Henkel, 2013; Grindley and Teece, 1997; Linden and Somaya, 2003; Somaya and Teece, 2001), the failure of monetary evaluations of patent licensing to capture large segments of cross licensing for which no money is being exchanged (Grindley and Teece, 1997), and the fact that negotiations do not take place in true arm's-length market settings but frequently under a 'bilateral monopoly' where both parties to the deal lack alternative trade partners and the valuation of the technology is highly context specific (Gans and Stern, 2010). Finally, and perhaps most strikingly, Feldman and Lemley (2015, p. 174), found that "ex post patent demands are not serving much of an innovation promotion function at all, even in the industries in which we would expect significant technology transfer. That does not mean technology transfer never happens; it does. But it may mean that technology transfer happens early in the life of a technology, and that secrets, collaborations, and informal know-how, not patents, are the primary focus of real technology licensing agreements." I therefore distinguish in this thesis between primarily patent-based technology transactions, where the primary object being licensed is a patent (and which is therefore possibly affected by the aforementioned shortcomings), and non-patent-based technology transactions where the primary object of the interaction is something other than a patent such as a blueprint or the transfer of tacit knowledge which strictly serves the proliferation of an innovation

The IP Cores that are the focus of the subsequent analysis are also subject to various other means of protecting the IP including copyright, industrial design, trademark, and a sui generis (Latin: of its own, unique) protection of the layout which is discussed in the next paragraph. For a detailed discussion please refer to Yeo et al. (2010).

The sui generis protection, initially established in the United States in 1984 with the Semiconductor Chip Protection Act (SCPA), rolled out globally via the Trade-Related Aspects of Intellectual Property Rights (TRIPS) agreement to which all members of the World Trade Organization (WTO) are bound. These agreements met the need for a

protection of the layouts of computer chips since the final chips are relatively easy to copy compared with their huge development effort and are neither well protected through patents nor copyright. Therefore, the new legislation effectively banned direct copying of existing chip topologies, similar to what copyright laws have achieved for literary works (Yeo et al., 2010). It does not, however, prohibit reverse engineering and building on the discovered working mechanisms, which is why secrecy and patent protection remain important to the semiconductor industry.

The existing literature in the field concludes that patents in general are an important means of protecting innovation in cumulative high-technology markets and that patents should be of added attractiveness to participants in markets for technologies due to their ability to safeguard and simplify the licensing process.

2.1.2 Transaction cost perspective on technology licensing

Transaction Cost Economics (TCE) affected the economics literature by shifting the view of companies as production functions to organizations and, thus, to their interactions (Macher and Richman, 2008; Williamson, 1998). TCE deals with the various factors that determine the efficiency of these interactions (transactions) and considers different means of governance ranging from a market mechanism relying solely on social forms of governance (where actors are part of social networks that would penalize opportunism in the absence of such formal mechanisms), to a market mechanism relying on (incomplete) contracts to internalization (vertical integration) if market transactions are perceived as unsatisfactory based on the economic environment in which they take place (Argyres and Mayer, 2007; Barney and Hansen, 1994; Macher and Richman, 2008; Williamson, 1979).

The proposition that market transactions between companies bear a cost is based on the conception that the partners to these transactions are subject to three shortcomings (Macher and Richman, 2008):

- Human actors involved in both organizations are subject to bounded rationality, meaning they are not able to mentally conceive and account for all possible future outcomes (Simon, 1957).
- Even if human actors were able to fully consider all possible future outcomes, it would be difficult for them to negotiate between organizations due to the lack of a

common business language on these future events (Hart, 1995).

- Even if both of these obstacles could be overcome, it would be difficult for a third party lacking the inside knowledge to enforce the agreement.

These three factors in combination imply that contracts between organizations are, by definition, incomplete. This incompleteness means that partners may need to engage in costly renegotiation in the case of an event not considered in the original agreement. Even more concerning, however, is that the incompleteness enables both parties to opportunistically exploit the shortcomings of the contracts governing the interaction and exposes each party to the other's ability to do so since it is impossible to *ex ante* identify a contract partner's inclination to exploit that incompleteness (Williamson, 1996).

To mitigate the risks of both renegotiation and opportunistic behavior, the parties select different governance regimes with the aim of minimizing the expected total cost of the interaction (or maximizing the net benefit of the interaction). The regimes differ with regard to the incentives they set, the contract-based legal framework, and the control mechanisms (Williamson, 1991). The decision to interact in a market-type framework yields significantly stronger incentives while being subject to transaction costs compared with a hierarchical (internalized) setting, which allows for more control over the interaction partner while being burdened with the administrative cost of hierarchies (Coase, 1937). Multiple varieties exist of an intermediate arrangement between these two polar opposites—frequently called a "hybrid" model—such as joint ventures (Klein et al., 1990) or the exchange of equity as a "hostage" between firms engaged in market-style transactions (Arora et al., 2001a; Pisano, 1990; Pries and Guidl, 2007).

While screening the literature, two consistent sets of transaction costs became apparent. The first set consists of generally applicable factors found to shift the balance toward either internalization or market mechanisms. The second set is an amendment to these factors based on work by Somaya and Teece (2001), which specifically explores factors believed to be most salient with regard to component and technology licensing that closely fit the licensing of IP Cores. Section 5.4 sets forth the evaluation of these combined factors with regard to the expected preferred governance mode of companies seeking to source IP Cores.

First set of transaction costs

The general literature review yielded the following five sources of transaction cost that make the market mechanism less attractive and therefore increase the likelihood of internalization when high:

1) Weak appropriability regime for developed technology (Arora et al., 2001a; Pisano, 1990) and inability to specify applicability of property rights between partners of technology development projects leading to potential loss of valuable information (Fosfuri, 2006; Pisano, 1990).

2) Difficulty of monitoring and enforcing contractual agreements (Fosfuri, 2006). It would be possible to address many of the abovementioned transaction costs if an objective way of measuring the impact of a technology on an invention and the licensor (e.g., the profit dissipation) was available. In many cases the impact of the technology simply cannot be measured (Somaya and Teece, 2001) and therefore a fair compensation is difficult to conceive and other less sophisticated means of limiting the usage are implemented such as restrictions by region or technology type, reducing the flexibility of both licensor and licensee that constitute a transaction cost.

3) Small-numbers bargaining, meaning that the number of alternative transaction partners is limited (Pisano, 1990), is a transaction cost.

4) Need for co-specialized assets since these put companies at a disadvantage if contracts need to be renegotiated (Pisano, 1990; Teece, 1986). Williamson (1985) distinguishes six types: physical specificity, human asset specificity, temporal specificity, dedicated assets, site specificity, and brand-name capital. This effect is especially salient when combined with small-numbers bargaining where few outside options exist to replace the current partner (Pisano, 1990).

5) High environmental uncertainty since this, in turn, increases the incompleteness of contracts (Pisano, 1990).

Of these factors, asset specificity and uncertainty are regarded as the primary drivers toward internalization (Walker and Weber, 1984).

Since the role of uncertainty in internalization is of particular interest to this

dissertation, elaboration on the various types of uncertainty that have been considered according to the extensive literature review by Macher and Richman (2008) is called for. Possible sources of uncertainty include fluctuations of demand (Heide and John, 1990), and supply (Walker and Weber, 1987), behavioral uncertainty (Anderson, 1985) and, most importantly to this work, technology (Balakrishnan and Wernerfelt, 1986; Walker and Weber, 1984). The verdict on the impact of technological uncertainty on the decision of the governance mode is unclear as Walker and Weber (1984) and Balakrishnan and Wernerfelt (1986) argue in opposite directions based on different operationalization of the concept of technological uncertainty.

Walker and Weber (1984) operationalize technological uncertainty as the expected number of changes in the design of simple manufactured parts based on a sample of contracts within one division. They hypothesize a negative correlation between high uncertainty and reliance on market transactions, but find no significant correlation between technological uncertainty and governance mode.

Balakrishnan and Wernerfelt (1986) look at aggregate industry data and operationalize technological uncertainty by the frequency of technological change—that is, the inverse of the number of years until any one technology would become obsolete—and find that internalization is lower for industries in which technological change is higher. They argue that this could be because licensors are aware of the lower value of a technology soon to become obsolete to licensees and hence they reduce their bargaining, making the market mechanism comparatively more attractive than pursuing vertical integration.

While the theoretical literature on the impact of technological uncertainty on internalization is clear, the empirical verdict on uncertainty (technological and other) is mixed. Harrigan (1986) argues that one reason for this is that uncertainty only becomes salient when combined with high asset specificity. Therefore, theory predicts that instances of high uncertainty coupled with high asset specificity should be primary candidates for internalizations.

Second set of transaction costs

Somaya and Teece (2001) propose an additional set of eight transaction costs that they deem especially relevant for technology transactions and which shift the balance toward internalization when high and toward market mechanisms when low, some of

which overlap with the above framework and therefore are not listed here to avoid duplication.

1) Effort for matching buyers and sellers (also called search cost) addresses the difficulty of finding a buyer and/or a seller for a certain technology.

2) Difficulty of negotiating and executing a transaction encompasses the drafting of a contract, which contains many of the elements considered by Macher and Richman (2008) that are not detailed more closely by Somaya and Teece (2001), as well as the physical exchange of the technology transfer.

3) Strategic isolation of rents captures the idea that patents may enable a company to safeguard monopoly rents for an entire product, thereby having a value far higher than that for the individual technology and therefore will not be licensed.

4) Diffuse entitlement problems when many different parties have applicable patent claims to a given technology or the validity of such claims with regard to a technology are difficult to evaluate. Negotiating for licenses to their patents (or deciding not to do so) is time-consuming and costly. In the IP Core industry, this is not really an issue due to the high incidence of cross-licensing.

5) Transfer of tacit know-how addresses how transferring tacit know-how without transferring the people involved is difficult and time-consuming.

6) Extent of dynamic transaction cost results from the need to frequently coordinate multiple stakeholders and contributors in technology development to contribute their respective share (Robertson and Langlois, 1995). Teece defines this kind of innovation as ‘systemic innovation’ which can be best handled internally (as opposed to ‘autonomous innovation’) (1996, p. 205).

7) Technological interconnectedness specifies the need to adapt multiple interdependent elements of technology to each other.

8) Valuation problems with technological assets concerns how high uncertainty regarding technological and commercial prospects, both of the overall product and also the share of a potential success, to be attributed to any single technology subsumed in a multi-invention product leads to strong discrepancies in value to be

attributed to a given technology (Somaya and Teece, 2001). The availability of a market with multiple alternatives to choose reduces the transaction cost associated with this factor.

While Linden and Somaya (2003) categorized all of the factors identified by Somaya and Teece (2001) as significant obstacles to licensing of IP Cores, this review of the applicable transaction costs reaches beyond their analysis in a number of areas. First, the attribution of relative strength of the impact of each of the transaction costs in the market for IP Cores and the observation of a mature market in contrast to the nascent stage they described where many transaction cost mitigating efforts such as technological development (e.g., encryption of the IP Cores to address Arrow's information paradox [1962]) were at an early stage.

One caveat raised by Fosfuri (2006) is that traditional TCE focus primarily on individual transactions and run the risk of not sufficiently considering the strategic background of the licensing companies, which may lead to a failure to explain why in some cases licensing is not pursued despite the individual transaction featuring low cost (although the strategic isolation of rents factor above will capture at least part of this concern).

To consider the strategic dimension of technology licensing, Arora and Fosfuri (2003) highlight the need to consider the two antagonistic effects of revenue generation and profit dissipation in addition to the traditional transaction costs to evaluate companies' overall attractiveness to enter into a licensing agreement.

The revenue generation effect captures the primary motivation for licensing of generating additional revenue through licensing contracts for developed technology. This positively correlates with the expected profits generated through the technology by the licensee and the bargaining power of the licensor, and negatively correlates with transaction cost.

The profit dissipation effect encompasses the reduced profit achievable with the products containing the technology due to the increased competition by the licensee. This effect can arise either through a reduced number of products sold or a lower price per product. This effect is also termed "cannibalization" and is only applicable for companies operating in both technology licensing and downstream product market.

Companies decide on the extent and scope (geographic or volume restrictions) of their licensing programs based on a careful deliberation of these two effects; licensing stops entirely when the revenue effect is lower than the transaction costs, even in the case

of no profit dissipation as would be the case for pure play technology providers (Fosfuri, 2006).

Having discussed the various literature on MfT and the specific focus topics of the role of formal IP in the form of patents and the verdict that TCE has had on transactions involving high asset specificity and uncertainty, the discussion of the object of observation, the market for IP Cores, appears in the next subchapter.

2.2 Market for IP Cores

This thesis focuses on the provision of technology packages in the form of IP Cores because non-patent-based technology licensing lacks study compared with patent-based transactions. While this can be explained with the relative small size of these markets—the market for IP Cores was worth 2.7 billion USD in 2014 (Gartner, 2015a) compared with an estimated market size of the total MfT of 90–100 billion USD[5] in 2000 (Arora and Gambardella, 2010; Athreye and Cantwell, 2007)—these considerations fail to account for the vital role these technology markets can serve for adjacent, significantly larger markets. In the case of the market for IP Cores, they serve as essential enablers for the semiconductor industry as a whole, an industry worth in excess of 320 billion USD in 2015 (IC Insights, 2016) as supported by the statement of Nenni and McLellan (2013, p. 93) describing the IP Core providers as "not so much the tail that wags the dog, rather they are like the heart of an elephant, tiny in comparison but without which there is no elephant."

2.2.1 Technology

This section focuses on the attributes of IP Cores required for understanding the conclusions in the subsequent sections. Reference is made to other publications for further details into the technological side (Bergamaschi and Cohn, 2002; Hurtarte et al., 2007; Linden and Somaya, 2003), the history and evolution of the market (Nenni and McLellan, 2013; Tuomi, 2009), the licensing contracts (FSA, 2004; Hurtarte et al., 2007), and the applicable IP protection (Oshima, 2003; Yeo et al., 2010).

[5] This figure includes technology interactions among related entities with the interaction of unrelated entities estimated at one third of this volume. Additionally, this sum would also capture *ex post* patent licensing where no knowledge is exchanged but freedom to manufacture is maintained (Grindley and Teece, 1997). The actual value of the MfT where technology exchanges between unaffiliated companies is likely substantially lower, although no precise measurement is available.

The rapid increases in processing power and decreases in transistor size driven by Moore's law, now makes it possible to integrate entire computer systems that used to be spread out across various, dedicated silicon chips connected through a Printed Circuit Board (PCB) into a single silicon chip—a so-called System on a Chip (SoC) (Nenni and McLellan, 2013). Just as one company did not necessarily provide the multiple dedicated chips, this technological evolution gave rise to another type of provider who now provided the individual designs of the dedicated chips to the manufacturer of the SoCs for integration prior to manufacturing. These designs are called 'IP Cores' or occasionally referred to as 'Macros' or Silicon IP (short: SIP) and represent a distinct function that is being integrated into the SoC. Examples of IP Cores include CPUs (e.g., provided by ARM), GPUs (e.g., provided by Imagination Technologies) or the analog and digital proportions of the USB port (e.g., provided by Synopsys). The IP in the context of IP Core stands for intellectual property and signifies that an IP Core essentially constitutes codified intellectual property.

IP Cores are available in a variety of formats. The highest-level description is called source code, or register transfer level (RTL), written in either Verilog or VHDL, and is comparable to a programming language in software development (Hurtarte et al., 2007). The advantage of source code is that it is relatively quick and easy to understand, which helps in troubleshooting, customizing the IP Core, and in connecting the IP Core to the remaining SoC. This accessibility is also the greatest disadvantage since the entire know-how and all contained trade secrets are easily decipherable, therefore, source code is rarely given. The next step is translating this source code into a Gate Level Netlist, which basically breaks the logic down into a number of switches and the connections between these switches. The name comes from the graphical representation of this item, which represents a "net" connecting the various gates. This breaking down obfuscates the underlying logic through its sheer complexity. One interviewee states that it should be technically feasible for a major company to reverse-engineer the code, but the effort is huge and serves as a practical means of protection; thus, it is comparable to assembly code in software. If an IP Core is provided either in source code/RTL or in netlist it is called a Soft Core because it is still processing technology independently and can be

easily inserted into an EDA tool,[6] which then incorporates and optimizes it with the remaining parts of the SoC. Typically, all digital components of an IP Core are in Soft Core format.

The alternative to Soft Cores are so-called Hard Cores that are completely finalized in terms of geometry and performance and are specific to a processing technology (e.g., TSMC 16nm FinFet), so cannot be easily ported from one processing technology to the other (e.g., between TSMC 16 nm and Samsung 16 nm) or between technology nodes (transistor sizes – e.g., 21 nm, 14 nm). A Hard Core is akin to plugging a black box into an otherwise final design and is unalterable by the EDA software. This specificity is the largest disadvantage because each Hard IP Core being specific to each processing technology and node hugely increases the design effort. However, for all computer components involving analog parts (the counterpart to the digital), Hard Cores are the only option because the analog proportion cannot be customized to various processing technologies through the EDA tools; the processes involved here being complex and not fully understood – two interviewees (H and C) referred to designing analog IP Cores as "black magic."

One of the most peculiar attributes of IP Cores is that it is impossible to say whether any given one is free of defects, as summarized by a researcher from a European university developing own IP Cores "*It is not possible to show that it works or that it doesn't work. I can show in specific areas that it does not work, but I cannot show that it works. […] It is technologically not possible in a limited time. Complexity is very high. We generally have billions of transistors on a chip*." (Quote interviewee X). Additionally, a representative of one of the largest IP Core providers stated that a full verification of an IP Core in order to prove it contains no defects is possible "*in exceptional, rare cases only*" (Quote interviewee G).). The difficulty associated with performing a satisfactory verification therefore scales with the number of transistors on a chip.

Regarding the functionality of the IP Cores and their respective value shares of the overall market for IP Cores, the 'Semiconductor Design Intellectual Property' reports by Gartner (2007-2015a) are highly insightful. Almost half of all revenues in 2014 were generated by processors with the majority of revenues stemming from microprocessors

[6] EDA stands for Electronic Design Automation and is a summary for all tools used to translate the programming-language-like source code (also called Register Transfer Level – RTL) into concrete paths for the wiring of an integrated circuit. Due to the complexity of these tools, there is an entire industry that focuses on their delivery.

(CPUs fall into this category) at 42.7% and Digital Signal Processors,[7] DSPs for short, capturing another 4.5%. The second largest segment is so-called physical IP with the largest share being Wired Interface IP (e.g., USB, PCI Express), which is typically highly standardized making it difficult for providers to differentiate. All IP Cores, in the "Physical IP" category would typically be delivered as hard cores due to the contained analog proportions. The final category of "Other Digital IP" is mainly composed of Graphics IP (which contains GPUs, so adding this element to the Processor IP would lead to a total processor-related share of IP Cores of 56.1%) and Fixed-Function Signal Processing IP (e.g., Codecs). One further interesting feature are the libraries of standard building blocks—these were the first IP Cores to be made available by dedicated IP Core providers since they are the processing technology-specific building blocks required during place and route (Nenni and McLellan, 2013). Today most foundries offer these basic libraries for free; therefore their revenue market share is low despite their relevance (Nenni and McLellan, 2013). Figure 1 contains a graphical representation of these findings.

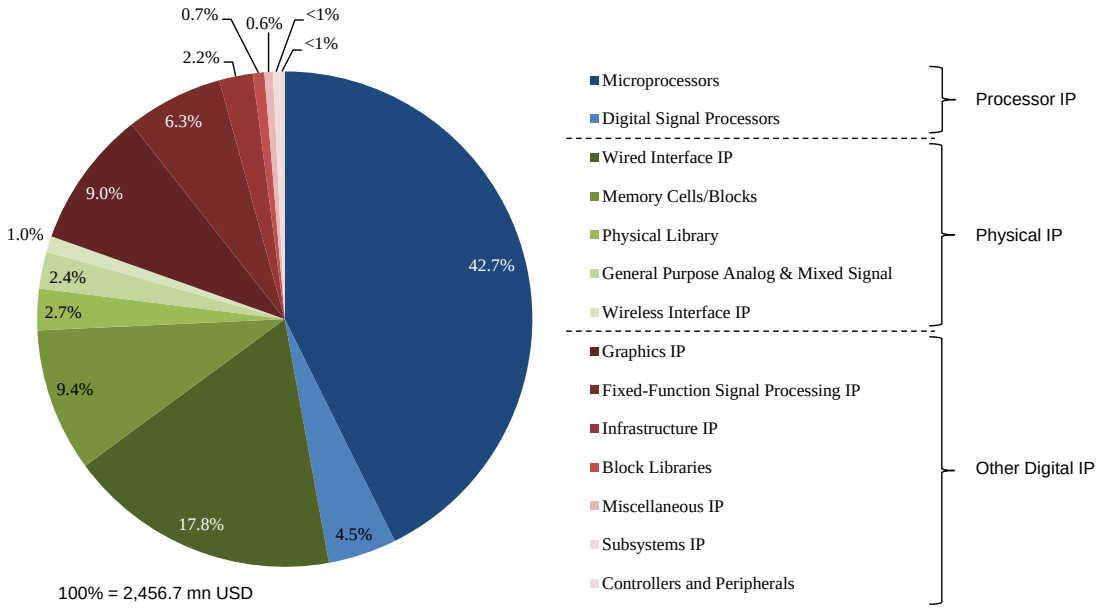


Figure 1: IP Core licensing revenue volume by function 2014; Source: Gartner 2015a

2.2.2 Market participants

The market for IP Cores features a variety of sellers, buyers, and intermediaries,

[7] DSPs are optimal for performing computations based on real life analog signals such as audio.

briefly categorized in the next paragraphs. Every single company developing computer chips will develop IP Cores for internal use; however, the focus of this thesis is on commercial transactions of IP Cores that transcend the boundaries of the firm.

The **providers** can be grouped into two categories, those whose primary business is the transaction regarding the IP Cores (called **dedicated IP Core providers**) and those for which IP Cores serve as an enabler for another, complementary service or product (called **enabler IP Core providers**).

The **dedicated IP Core providers** generate the majority of their revenue through sales of IP Cores for which they also provide support to facilitate integration into the SoC of the client. Some, especially smaller, companies see the provision of integration support as core to their offering and therefore operate as design services companies where IP Cores are only included in the bundle of a project or not even explicitly sold but rather are utilized internally to speed up recurring implementation routines. The larger companies try to minimize the support required for their IP Cores due to the low scalability of these services. Dedicated IP Core companies operate somewhere between this continuum of using pre-codified knowledge and individualized services and also frequently move from being pure design services companies to IP Core providers over time. The largest dedicated IP Core providers are ARM and Imagination Technologies (Gartner, 2015a).

The three **enabler IP Core provider** types are foundries, FPGA providers, and EDA tool providers.

The term foundry refers to contract manufacturers in semiconductors that produce silicon chips for both Fabless companies and IDMs (see detailed description in discussion of buyers of IP Cores that follows). Foundries produce so-called ASIC (Application Specific Integrated Circuit) chips, which are optimized to one specific use case in terms of performance (e.g., speed of the chip, noise of a signal), power (how much power the chip consumes during operation), and area (how much space the chip occupies in silicon)—in the industry these criteria are summarized as PPA based on the initial letters of power, performance, and area. Since every foundry has somewhat different processing technologies, each foundry provides the basic building blocks—so called foundational IP—to their respective processing technology to chip creators. This IP is required to translate a Soft Core into a Hard Core and is typically provided free of charge to the foundry's customer. For all requirements exceeding the basic offering, the foundries maintain an ecosystem of providers of IP Cores and design services certified on their

respective processing technology. The largest foundries in 2015 were TSMC and GLOBALFOUNDRIES (IC Insights, 2016).

Field Programmable Gate Array (FPGA) providers produce re-programmable computer chips. An FPGA consists of a hard-coded section that contains all the frequently used components, such as a CPU, and some interconnect and additionally contain a programmable area that customizable to the customer's wishes. The advantage of FPGAs compared with the ASICs is that FPGAs are patchable—for example, in case of a bug in the chip design or to update the chips in the field (used for telecommunications base-stations). The disadvantage is that due to the flexible nature of the wiring, the full utilization of all elements is not possible in terms of PPA so that an FPGA is more expensive on a per-unit level than an ASIC; however, the upfront development cost is significantly lower. This makes FPGAs the preferred choice for prototyping and lower volume charges, whereas the high to very high volume chips develop as ASIC chips.[8] One interesting side effect of the programmability of FPGAs is that it allows cloud computing providers such as Amazon to enable customers to not only rent generic computing performance and memory but also allow customers to upload their own FPGA designs onto Amazon's FPGAs and thereby customize the very hardware they are renting to their specific requirements. This enables effectively combining the advantages of flexible, easily scalable computing resources and increased utilization of cloud computing with the performance increases of a dedicated specialized hardware design (Amazon Web Services, 2016; Armbrust et al., 2010). Since many customers do not develop all missing functions themselves, FPGA providers nurture an ecosystem of function providers, comparable to that of foundries, which they audit, certify, and also promote during client meetings. Two large FPGA providers are Altera (acquired by Intel in 2015) and Xilinx.

Electronic Design Automation (EDA) tool providers are a hybrid between enabler-providers and dedicated providers. They are dedicated in the sense that the IP Core business is separate from the EDA tools organizationally with the expectation of contributing significantly to the company revenue and profits. The enabler characteristic stems from the strong synergies between the provision of EDA tools, which enable a large number of IP Core developers to work with the latest (and occasionally pre-release) versions of the tools free of charge while at the same time providing valuable, unfiltered

[8] This research does not consider ASSPs (application specific standard products), which are basically ASICs not designed based on a customer request but rather based on market forecasts by semiconductor providers.

feedback to the tool developers. These financial and technological advantages contribute to enabling EDA tool providers to succeed in the challenging segment of standards based IP (see Section 4.6 for a more detailed discussion). The EDA tool providers most active in IP Core licensing are Synopsys and Cadence (Gartner, 2015a).

Having considered the various providers of IP Cores, the focus now shifts to the **buyers** of IP Cores, which comprise Integrated Device Manufacturers (IDMs) and so-called Fabless manufacturers of chips.

IDMs are the original business model that dominated the semiconductor industry in the 1980s and early 1990s and basically means that all tasks from R&D through manufacturing to (after) sales are available from a single organization. Due to the increasing complexity and corresponding cost of developing and manufacturing IP Cores, only a small number of companies still follow this model exclusively and many companies utilize foundries to handle production peaks. While there is a trend toward dis-integration of the value chain leading to the multitude of different providers and consumers of IP Cores, this by no means implies the imminent demise of the established IDMs, which have adapted to the new participants and can use their coverage of the entire value chain to realize strong synergies. They are therefore likely to co-exist with the specialized providers going forward (Kapoor, 2013). A prominent example of an IDM is Intel.

The name for the Fabless model stems from the word “fab” (short version of semiconductor fabrication plant) and signals that these providers do not own any plants but rather utilize chips produced by foundries. These companies develop some parts of the SoC themselves in the form of IP Core, which they use internally. Subsequently, these IP Cores integrate with commercially licensed IP Cores from dedicated IP Core providers using EDA tools. After verification of the entire integrated SoC, the chip design goes to a foundry for manufacturing. Finally, the produced physical chips are available for sale to electronic system companies. Prominent examples of Fabless companies are Qualcomm and AMD (which used to be an IDM).[9]

In terms of **intermediaries,** there is a distinction between resellers and market places of IP Cores.

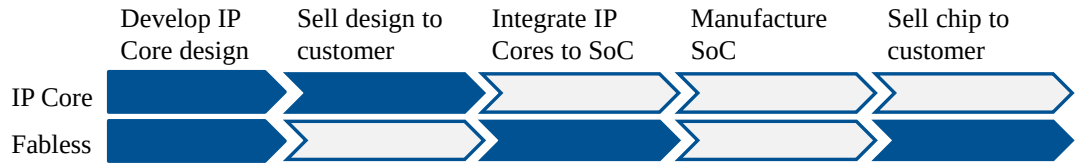
[9] There is an (in)famous quote by the former head of AMD W.J. “Jerry” Sanders: “Real men have fabs,” which he said just a couple of years before AMD decided to sell their own fabs (http://www.bloomberg.com/news/articles/1994-04-10/real-men-have-fabs)

Resellers serve as sales channels without own development either for small dedicated IP Core developers that are too small to maintain a dedicated sales team or represent large corporations that deal in silicon chips and lack the will or capabilities to directly license out their technology. Typically these providers partner with design service companies or maintain an own set of field application engineers who can deeply engage on the technical details with potential customers and subsequently support them in adapting the technology. Examples of resellers are T2M and Missing Link Electronics.

Market places provide IP Core developers with an easily searchable product catalogue of all available IP Cores. These market places typically provide only high-level information including a data-sheet on the IP Core. They then forward potential customers to the respective developer's homepage for further information and support. Prominent examples of market places are Design & Reuse and ChipEstimate.

The comparison of the R&D aspect of Fabless and IP Core companies receives further attention in later chapters. Here, more detail on the common and distinguishing features of the two company types are given. The initial step in developing a new chip, the development of a soft core with the desired functionality, is the same for both companies. IP Core companies develop the IP Core to sell on to other companies, while Fabless companies use their in-house developed IP Core as their distinguishing proprietary contribution to the SoC they assemble. The integration of the proprietary IP Core and the third-party IP Cores is a distinguishing feature since only Fabless companies need to do it; however, the aforementioned third-party EDA tool providers heavily support it and the IP Core providers are able to ensure smooth integration of their IP Cores for their customers. Fabless providers outsource the manufacturing so it is not in scope for either Fabless or IP Core. Subsequently, Fabless companies sell the physical chips directly to the end customers instead of licensing their blueprints, as is the case for IP Core providers. While the integration of the proprietary and third-party IP Cores could potentially be subject to R&D, this impact is likely small since it is primarily facilitated by a third party (EDA tool provider) and is also pre-conceived by IP Core providers. Finally, the sales processes are not the subject of significant research and patenting and therefore do not distort the comparability of the R&D footprints of Fabless and IP Core companies. It is therefore concluded that, in terms of R&D footprint, Fabless providers are similar to IP Core providers because neither owns manufacturing sites and the most R&D intensive task of developing IP Cores is common to both. This leads to repeated

make or buy decisions as supported by a manager active in the procurement of IP Cores who said that "*we always make the decision of make or buy, we make it again and again*" (Quote interviewee A, translated). Figure 2 visually represents these considerations with the R&D intensive tasks highlighted in bold blue font.



IP Core

- **Designs IP Cores for sale**
- Customers are Fabless companies, IDMs[2] and some electronic systems companies developing own chips (e.g., Apple)
- **Ensure IP Cores are integrable** in close cooperation with 3rd party EDA tool providers
- No manufacturing required

Fabless

- **Designs IP Cores for internal, proprietary usage**
- Customers are electronic systems companies integrating the chips into their devices
- **Integrate both own and 3rd party IP Cores into SoC**, heavily relying on 3rd party EDA[1] tools
- Manufacturing is done by foundry

1 Electronic Design Automation 2 Integrated Device Manufacturer

Figure 2: Comparison of R&D intensive tasks between Fabless and IP Core company type

Having discussed the various participants in the market for IP Cores, the next section focuses on the reasons for sourcing IP Cores.

2.2.3 Reasons for sourcing IP Cores

Tuomi (2009) lists 10 factors that potential customer of IP Cores consider when deciding on whether to make or buy an IP Core.

These factors are rearranged into three categories, depending on whether they advocate the "make" option, the "buy" option, or whether their impact depends on more deliberate consideration. Table 1 provides an overview of the 10 factors.

Table 1: Considerations influencing a make or buy decision for IP Cores; Source: Adapted from Tuomi 2009

Make	Neutral	Buy
- Dependence on vendor - Need for support by vendor - Differentiation benefits from proprietary design	- Technical risks - Legal risks - Product lifecycle management	- Time to market - Preexisting IP ecosystem - Development cost and commercial risk - Need for skilled engineers

The three factors **Dependence on vendor**, **Need for support by vendor**, and **Differentiation benefits from proprietary design** all shift the decision toward internal production.

Dependence on vendor[10] addressees the concerns of buyers of IP Cores of becoming locked into their relationship with an individual IP Core provider in case of repeated purchase, and increasing reliance on the vendor's know-how in the development of this specific chip component, which the vendor could ultimately exploit in follow-on negotiations. This is especially true if dedicated software that is required to operate the IP Core (such as drivers) has been written, the development effort for which will make switching much less attractive and facilitate a lock-in, or if the buyer of the IP Core has laid off the internal teams able to build the respective IP Cores.

Need for support by vendor captures the need to be able to rely on the vendor's proprietary know-how if issues arise during the integration. Since IP Cores are highly complex and are frequently delivered in formats that are not readable by the buyer (to protect against risk of loss of IP), the developers of the IP Cores are, due to their intimate knowledge of the source code, the fastest and sometimes only way to address any issues. If the vendor's support is required, its priorities and incentives may not align with the buyer's, again giving rise to opportunism on the side of the vendor. Therefore, if a Fabless or IDM company anticipates commercially available IP Cores to contain many flaws, they are more likely to develop in-house.

Differentiation benefits from proprietary design captures the concern of Fabless companies and IDMs that ultimately they need to differentiate themselves from their competition—a need that is directly opposed to the interests of the IP Core sellers who earn licensing fees and royalties with every additional sale of their technology and therefore are interested in distributing their IP Core to as many customers as possible.

The three factors **Technical risks**, **Legal risks**, and **Product lifecycle management** do not clearly favor either make or buy and therefore need to be carefully evaluated.

The existence of **Technical risks** is one of the primary concerns of customers of IP Cores since "designs almost always have design errors and bugs" (Tuomi, 2009, p. 45). The advantage of buying an IP Core is that these IP Cores are recognized and accepted in the market at another company and in mass production—a state termed 'silicon proven.' However when no proven technologies exist in the market, an internal development has

[10] Tuomi (2009) terms this factor as a 'sourcing risk,' which this researcher believes to be too generic.

the advantage of being better able to control the technicians and of creating less incentive to hide design flaws as supported by Williamson's (1985) argument that greater managerial ownership helps limit opportunism.

Legal risks mostly arise through inadvertent infringement of another company's patents. This risk is lower for suppliers of IP Cores that have a long history of providing a certain type of IP Core compared with a novel internal development. This is because the IP Core seller in this case is likely more familiar with the IP landscape and less likely to inadvertently infringe. If both companies have similar experience in a field and have equally thorough patent monitoring processes, the legal risks are comparable. One advantage of sourcing from a third party is the possibility of including indemnity clauses in the contract that transfer part of the damage to the IP Core seller. One disadvantage of relying on a third party follows the moral hazard issue described for 'technical risk' of hiding a possible infringement, which is more likely to occur with a third party.

The consideration behind **Product lifecycle management** is that when buyers of IP Cores use the IP Cores for multiple generations of products, they will be able to benefit from an IP Core seller's autonomous efforts to continuously refine and improve upon their IP Core offering. This allows the buyer to achieve increased performance across generations without dedicating any development resources. The downside to this consideration however is that buyers of IP Cores become locked-in and weaken their bargaining position if they are reliant on an IP Core provider for multiple generations. Additionally the improvements will necessarily change part of the IP Core, which might result in compatibility issues and subsequent adaptation efforts. Therefore, it is not clear whether this factor works in favor of making or buying IP Cores.

The four factors that drive companies to buy rather than to make IP Cores are **Time to Market**, **Preexisting IP ecosystem**, **Development cost and commercial risk**, and **Need for skilled engineers**.

The **Time to Market** factor captures the fact that IP Core companies will continuously develop chips containing various functionalities and of various power, performance, and area specifications. This in turn implies that when a Fabless or IDM company discovers that it needs a chip at a given PPA, a chip that exactly or closely matches the requirement is likely to be available in a fully developed and potentially even silicon proven state on the market. This will save the company several months' worth of time required for development and, more importantly, verification of the chip. This need becomes especially apparent when considering the compression of time to market that the

full SoC experiences. As expressed by Stube Kengeri, Vice President of GLOBALFOUNDRIES: “An IoT chip in the past was brought to market in about 3-4 years, but future requirements will be closer to 1-2 years with simultaneous reduction in cost to below one dollar per chip” (Nenni and McLellan, 2013, p. 199).

The **Preexisting IP ecosystem** aims at the large area of complementary services and software required to fully utilize an IP Core. In the case of ARM, independent companies develop a huge number of drivers and dedicated software in order to make their services run smoothly on ARM CPUs. If a company selling SoCs currently running on ARM CPUs decides to switch to a proprietary CPU, its customers will not only expect the CPU to match the performance of ARM CPUs (which is challenging in itself) but also will require the company to provide all the corresponding software that it would have access to for free for an ARM. This added expense of the software provided to ARM free of charge is prohibitively expensive and helps to cement the position of ARM in the CPU area. While complementary software is one such example (and the case of ARM is probably the most extreme case), there are many similar cases such as independent developers who can support the integration and are familiar with ARM but would not be with a proprietary CPU, the existence of verification IP, and processes and development tools.

Development cost and commercial risk closely relate to the previous point in that one of the advantages of relying on a third-party IP Core is that the cost of development spreads across multiple customers. Additionally, in the case of an already silicon proven IP Core, the commercial risk of it not being up to market expectations is reduced since it has already been accepted in a different end-product. These benefits are in contrast to developing an IP Core internally where difficult to predict costs need to be fully borne by the developing company while the product lacks an established presence in the market. The cost aspect is especially salient considering the increasing productivity gaps in design and verification, which highlight the fact that the number of transistors on a given chip or IP Core is increasing faster than the speed at which designers can design and verify a given number of transistors. This results in an ever increasing number of hours required to develop an IP Core and thereby increases development cost with each technology node (FSA, 2004; Linden and Somaya, 2003). The primary reason why these effects have not brought the semiconductor industry to a standstill is “the emergence of an IP reuse strategy” (Foster, 2013, p. 584).

Finally, the salience of **Need for skilled engineers** strongly depends on whether a

potential buyer of an IP Core has been actively developing IP Cores in the area of concern. If the company has not recently done so, the high level of specialization combined with the high speed of technological change and improvement make it difficult to find the required, qualified staff for a given project internally. This is because of high demand for this kind of expertise in the industry and the fact that these developers are expensive, specialized talent who tend to quickly leave the firm upon cessation of development activities in a certain technological area. In contrast, IP Core companies have the required number of staff with the required up-to-date know-how since they continuously develop IP Cores in a given domain.

2.3 Trust

Trust, the subject of detailed analysis for many decades, has been studied in a multiple number of fields as diverse as psychology, sociology, economics, and marketing (Doney and Cannon, 1997). There is a "confusing potpourri" of definitions (Shapiro, 1987, p. 625) regarding the exact content and nature of trust. Rather than discuss the various alternatives, hereinafter is a brief (and necessarily incomplete) overview of the reasons trust is required in market transactions, followed by an overview of the evolution of the concept of trust in the academic literature and the definition of trust as used in this thesis.

The definitions of trust in economics and marketing strongly focus on the existence of risk and vulnerabilities to which participants expose themselves when engaging with other parties in the market place due to possible "adverse selection…moral hazard…[or] hold-up" (Barney and Hansen, 1994, p. 176), especially in cases involving asymmetric information and investments that are specific to an exchange partner (Williamson, 1979) (see Section 2.1.2 for a more detailed discussion). This thesis follows the definition of risk by Sitkin and Pablo (1992, p. 10) as "a characteristic of decisions that is defined here as the extent to which there is uncertainty about whether potentially significant and/or disappointing outcomes of decisions will be realized." The nature of the risk focused on by researchers in these settings is the possibility "that one's exchange partner will act opportunistically" (Bradach and Eccles, 1989, p. 104) and has been the subject of extensive study in the respective literature (see e.g., (Andaleeb, 1995; Barney, 1991; Barney and Hansen, 1994; de Ruyter et al., 2001; Geyskens et al., 1998; Gulati and Nickerson, 2008; Kramer, 1999; Ring and Van de Ven, A. H., 1992). For this thesis, the description of this specific risk focusing on the possibility of opportunistic behavior by

the exchange partner is ‘relational risk’ following Nooteboom et al. (1997).

Shapiro (1987) has considered trust in the context of principal-agent settings where the principal (trustor) cannot fully evaluate the actions of the agent (trustee) and hence faces a risk through adverse actions of the agent. Bradach and Eccles (1989, p. 104) extended trust to the context of governance choices and found trust essential for market-style interactions to prevail over internal hierarchies and defined it as an “expectation that alleviates the fear that one's exchange partner will act opportunistically” – a finding that is especially significant in light of the vertical disintegration introduced through MfT. Ring and Van de Ven (1992, p. 487) further expand this concept to repeated buyer-seller type transactions between companies and specifically define trust as a means to overcome the risk of not “accomplishing tasks that require sustained cooperation with others, particularly when they represent difficult or novel ventures.”

Mayer et al. (1995) contributed to the discussion around trust by reviewing which elements determine the level of trust between organizations and identified *ability*, *integrity*, and *benevolence* as the sources of trustworthiness. Their corresponding definition of trust, which I follow for this thesis, is “the willingness of a party to be vulnerable to the actions of another party based on the expectation that the other will perform a particular action important to the trustor, irrespective of the ability to monitor or control that other party” (p. 712), so in contrast to previous definitions it is not directly contingent upon opportunism and thereby contains the risk arising from a trade partner who involuntarily is unable to fulfill its obligations due to a lack of ability (on top of containing the established risk of opportunistic behavior). This definition of trust has been widely adopted and tested in the field including for international Buyer-Seller relationships (e.g., Bell et al., 2002) and has received some 14,000 citations to date according to Google Scholar.

Building on Mayer et al.’s (1995) framework on trust, McKnight et al. (1998; 2002; 2004) analyzed antecedents of initial trust in an effort to explain why some organizations, despite never having interacted previously, exhibit high levels of trust in one another. His antecedents include *disposition to trust* (general readiness to trust others independent of their characteristics), *structural assurances* (third-party mechanisms that can be used to penalize lack of integrity), *reputation* (information on the trustworthiness of a company provided by third parties), *perceived quality* (decision on trustworthiness based upon any available cues due to limited information being available (Meyerson et al., 1996) such as the attractiveness of a person or visual appeal of a homepage) and *third-party certificates*

(representing an endorsement by the issuing organization). McKnight et al. (2004) also find that reputation is important for initial transactions but is readily replaced with personal experience in settings of repeat interactions. Another significant contribution of McKnight et al. (1998) is the separation of trustworthiness (the belief that the other party has high integrity, benevolence, and ability) and trusting intention (the intention to make oneself vulnerable to the other party) that constitute separate dimensions according to the theory of reasoned action (Fishbein and Ajzen, 1975) of the complex trust construct.

The final mechanism of achieving trust is the possibility of transferring trust from a highly reputed organization to another organization that has less trust (Doney and Cannon, 1997; Stewart, 2003). There are various ways trust can be transferred, either through individuals, through a place, or through an organization (Stewart, 2003). Trust is also transferable deliberately through communication from the trustee or by a trusted third party actively reaching out, or through cognitive processes based on the perceived similarity or relationship of the trustee and the trusted third party in the eyes of the trustor.

The topic of trust has received little attention in the context of Markets for Technologies with the only prior research performed by Jensen et al. (2015) who highlight the role of trust in future technology transactions through a survey of technology intermediaries. In contrast, this study analyzes the underlying risks in a market for current technologies and further embeds its findings with the existing theories around trust.

To sum up, while there is a huge variety of differing definitions of trust used in various research streams, the economics and marketing literature focuses on trust as a means of mitigating the relational risk of opportunism in interactions that rely on the market mechanism. The trust model by Mayer et al. (1995) is a good fit for the context of MfT because of its being proven in the literature, including for buyer-seller interaction, its orientation toward organizations, the consideration of initial trust, and the inclusion of ability as an element of trust (see Section 5.35.3 for an elaboration on this element).

Now, having laid out the relevant prior literature and details on the technological concepts required to fully understand those set forth herein, the following chapters detail the methodology employed to investigate the market for IP Cores.

3 Methodology

This chapter describes the methodologies applied in answering the research questions as well as why they are best suited for doing so. Section 3.1 details the deliberation involved in choosing a qualitative vs. hybrid vs. quantitative research approach. Section 3.2 follows up by outlining the two most commonly employed qualitative approaches by Eisenhardt and Gioia before elaborating on the qualitative methodology used in this thesis. Section 3.3 contains a description of the secondary data employed throughout the dissertation

3.1 Decision on approach

In accordance with Edmondson and McManus (2007), the first step of the dissertation was to narrow down the research questions and investigate the relevant prior literature.

There is an abundance of previous research into the working mechanisms on MfT, yet most of it rests on patent-based observations and analysis; therefore, early stage interviews aided in determining whether the working mechanisms of the market for IP Cores were comparable to the patent transactions pre-eminent in the discussions of MfT. When several of the interviewees stated that these are two completely distinct phenomena, I pivoted to approaching the market in an exploratory way by asking, in general terms, the questions "how does the market for IP Cores function" and following up more precisely by asking IP Core sellers "what enables you to sell IP Cores and which obstacles do you face" while directing the inquiry of "when do you chose to buy vs make an IP Core and what obstacles do you face in sourcing IP Cores from a third party" at buyers of IP Cores. These questions are fundamental because of the lack of prior literature on the working mechanism of non-patent-based technology transactions [11] and call for a qualitative, interview-based approach to provide the rich perspective and elaborate context inaccessible in large database-focused econometrical approaches (Masten and Saussier, 2000). Additionally, the wide scope enabled me to avoid missing any relevant insights and concepts that could have been the case when approaching the topic with a predefined, narrow research question or hypothesis (Edmondson and McManus, 2007; Eisenhardt, 1989; Gioia et al., 2013). For one sub-area of this research, the role of

[11] The only research in this area (Linden and Somaya, 2003) focuses on the criteria determining the organization mode and undertaken at a time when the market for IP Cores was still in a nascent stage.

formalized IP protection in the market for IP Cores, preconceptions existed in the MfT literature, albeit for a setting based purely on patents to facilitate the technology transfer. Approaching this question via a hybrid method of qualitative evidence from interviews combined with an empirical analysis based on a large dataset made it possible for this study to both address a clearly defined hypothesis and explore the context of why the results come out as they do.

3.2 Qualitative research

In the domain of qualitative research, I distinguish two major approaches that have gained considerable traction in large shares of the qualitative research published in high-ranking journals—highlighted by the *Strategic Management Journal* in its primer on qualitative research (Strategic Management Journal, 2014)—the Eisenhardt and the Gioia methodologies, before outlining the approach chosen for this research.

3.2.1 Eisenhardt

The Eisenhardt methodology was conceived to provide researchers with a clear pathway to ensure their research was rigorous and defensible amid "concerns of validity and reliability in experimental research" (Eisenhardt, 1989, p. 534). Her method rigorously focuses on iteratively developing theory based on a well-sampled set of multiple cases and triangulating inputs from multiple data sources and investigators. Researchers deliberately ignore existing theory and hypotheses at the beginning of a research project to avoid biases in observation and only receive consideration at a later stage. Table 2 summarizes the key steps and activities of the Eisenhardt methodology.

Table 2: Steps and key features of the Eisenhardt methodology; Source: Eisenhardt (1989)

Step	*Activity*	*Reason*
Getting Started	Definition of research question	Focuses efforts
	Possibly a priori constructs	Provides better grounding of construct measures
	Neither theory nor hypotheses	Retains theoretical flexibility
Selecting Cases	Specified population	Constrains extraneous variation and sharpens external validity
	Theoretical, not random, sampling	Focuses efforts on theoretically useful cases-i.e., those that replicate or extend theory by filling conceptual categories
Crafting Instruments and Protocols	Multiple data collection methods	Strengthens grounding of theory by triangulation of evidence
	Qualitative and quantitative data combined	Synergistic view of evidence
	Multiple investigators	Fosters divergent perspectives and strengthens grounding
Entering the Field	Overlap data collection and analysis, including field notes	Speeds analyses and reveals helpful adjustments to data collection
	Flexible and opportunistic data collection methods	Allows investigators to take advantage of emergent themes and unique case features
Analyzing Data	Within-case analysis	Gains familiarity with data and preliminary theory generation
	Cross-case pattern search using divergent techniques	Forces investigators to look beyond initial impressions and see evidence thru multiple lenses
Shaping Hypotheses	Iterative tabulation of evidence for each construct	Sharpens construct definition, validity, and measurability
	Replication, not sampling, logic across cases	Confirms, extends, and sharpens theory
	Search evidence for "why" behind relationships	Builds internal validity
Enfolding Literature	Comparison with conflicting literature	Builds internal validity, raises theoretical level, and sharpens construct definitions
	Comparison with similar literature	Sharpens generalizability, improves construct definition, and raises theoretical level
Reaching Closure	Theoretical saturation when possible	Ends process when marginal improvement becomes small

3.2.2 Gioia

In contrast to that of Eisenhardt, the Gioia methodology rests much more strongly on the belief that interview sources are “knowledgeable agents” (Gioia et al., 2013, p. 17) who are ideally positioned to inform the researcher on the realities of their environments because a large share of the world is socially constructed (Berger and Luckmann, 1966; Schutz, 1967; Weick, 1969). Gioia therefore puts great emphasis on using the very words used by the interviewees in the early stages of research to avoid missing out on new concepts that might result from approaching a subject with preconceived constructs.

The Gioia methodology is best-suited for understanding processes in a given environment due to the close interaction with and the importance placed on the people most knowledgeable about these processes through semi-structured interviews. Table 3 summarizes the approach for the Gioia methodology.

Table 3: Steps and key features of the Gioia methodology; Source: Gioia et al. (2013)

Step	*Key Features*
Research Design	Articulate a well-defined phenomenon of interest and research question(s) (research question[s] framed in ‘‘how’’ terms aimed at surfacing concepts and their inter-relationships)
	Initially consult with existing literature, with suspension of judgment about its conclusions to allow discovery of new insights
Data Collection	Give extraordinary voice to informants, who are treated as knowledgeable agents
	Preserve flexibility to adjust interview protocol based on informant responses
	"Backtrack" to prior informants to ask questions that arise from subsequent interviews
Data Analysis	Perform initial data coding, maintaining the integrity of 1st-order (informantcentric) terms
	Develop a comprehensive compendium of 1st-order terms
	Organize 1st-order codes into 2nd-order (theory-centric) themes
	Distill 2nd-order themes into overarching theoretical dimensions (if appropriate)
	Assemble terms, themes, and dimensions into a ‘‘data structure’’
Grounded Theory Articulation	Formulate dynamic relationships among the 2nd-order concepts in data structure
	Transform static data structure into dynamic grounded theory model
	Conduct additional consultations with the literature to refine articulation of emergent concepts and relationships

One of the biggest differences between the Gioia and the Eisenhardt methodologies is the proposition of a structured data model by Gioia et al. to support abstracting from the 1st Order Concepts that are strongly based on interviewee feedback via 2nd Order Themes that are built based on the insights of the knowledgeable researcher and finally consolidated to Aggregate Dimensions where appropriate (Step Data Analysis). Additionally Gioia et al. recommend consulting the existing literature upfront to inform the approach but refrain from hypothesizing about the object of observation based on this literature. Their requirement for multiple data sources, multiple investigators, and triangulation of results is less strict compared with Eisenhardt (1989). Gioia et al. (2013, p. 22) correspondingly report with regard to the reporting of intercoder reliability or agreement percentages that “we certainly do not consider such a step to be necessary, however, because the data structuring procedures themselves lend the requisite rigor to the analyses.”

For a list of exemplary papers using the methodology, see Appendix B of Gioia et al. (2013).

3.2.3 Own methodology

Due to the scarcity of prior literature on the role of trust in the context of technology licensing and the focus on the sales process I followed a qualitative approach to investigate the working mechanisms of the market for IP Cores and employed a hybrid approach with an additional panel dataset of patenting data to analyze the role of formal IPR in a MfT that does not use patents for licensing deals (Edmondson and McManus,

2007).

For the qualitative section of my research I performed a multiple case study analysis that enabled me to more robustly identify new concepts and constructs along with the rich context in which they appear by triangulating the feedback of the multitude of participants to and stakeholders of the market for IP Cores (Eisenhardt, 1989). Following the advice of Anteby et al. (2014) of posing 'How' questions rather than 'Why' questions I initially explored the question "How does the market for IP Cores work." This was refined by the question "how does it manage to remain stable (or become viable in the first place)" followed by "how do buyers of IP Cores evaluate and choose their supplier," and concluded with the final question "how do sellers of IP Cores build trust into their product and what is the risk that buyers are concerned about."

The exploratory nature of this research required significant flexibility regarding adjusting the research questions to unexpected interviewee feedback. The primary object of observation was the sourcing process of IP Cores, where potential market failures both on supply and demand sides are most apparent. Performing semi-structured interviews following the Gioia methodology with knowledgeable observers of this sourcing process from both the supply and demand side, as well as with independent experts, made it possible to safeguard against biased reporting of interviewees due to social desirability.[12]

I sampled cases theoretically rather than randomly in order to ensure a best possible fit between the selection and the phenomenon to be studied (Eisenhardt, 1989, 2014). The chosen cases cover all relevant perspectives along the dimensions of transaction participant type, size, region, and life cycle enabling the identification of important differences between the perceived obstacles faced by large and small companies. In addition, it was possible to more closely identify the source of risk by comparing two sub-segments of the market for IP Cores, that for FPGAs and that for ASICs. I distinguish transaction participants along the categories of buyers, intermediaries, independent industry experts, and sellers. Sellers were further separated into dedicated IP Core sellers, EDA tool companies, and foundries (the interviews from the FPGA companies appear separately since these companies are active as both buyers and intermediaries of IP Cores). In terms of size, I spoke with both large sellers (4 of the top 10 IP Core providers according to Gartner [2015a]) employing thousands of people with annual revenues of several hundred million Euros and small providers, some of which employed two people

[12] There was no evidence for this; during interviews the answers of experts and buyers/sellers aligned.

with a few hundred thousand Euros of sales per year. Region-wise, I primarily spoke with European (28 interviews) and American (eight interviews) companies. Asian companies (two interviews) were harder to identify and far fewer (as well as less responsive to my requests for interviews). I did not identify fundamental regional differences when interviewing and do not believe that my research is subject to a strong bias in the identified mechanisms because "*semiconductor is very global [because] it doesn't cost a lot to ship such a small thing [the chip] around the world*" (Quote interviewee A) and information exchange across vast distances is no longer an issue due to the Internet. The companies I interviewed were diverse in terms of life cycle, some having been involved in the licensing of IP Cores since the beginning in the late 1980s and others being only a couple of years old and still trying to find their first customer.

Initially, it was difficult to arrange interviews with managers at the larger IP Core providers and on the customer side with a 0% initial success rate of e-mails (and calls) to publicly available company addresses. Only through personal connections and significant support from senior leadership of the Global Semiconductor Association were the first interviews arranged. These initial interviewees were able to arrange further interviews with other IP Core providers based on their own reputation, unlocking the otherwise closed world of IP Cores.

Each interviewee received the questionnaire upfront. A short section introducing the general research topic was included so that interviewees could prepare for the questions and understand the overall direction in mind. This enabled the highlighting of missing points that were relevant to the overall understanding yet not contained in the interview questionnaire. All interviewees received the assurance of anonymity. Therefore, it was necessary to partially redact selected quotes where anonymity would have been at risk in order to reduce social desirability biases and to enable interviewees to speak freely without the worry of possible repercussions for their employer (regardless, one company did refuse to permit their employee to engage in this research). All interviews were performed in either English or German and audio recorded for future reference. The recordings were transcribed in the respective language of the interview and a second researcher independently verified each. The interview questionnaire was continuously refined based on evolving understanding from previous interviews (Gioia et al., 2013) (see Appendix A 1 for early and late stage interview questionnaires). As a follow-up, after completion of the interviews initial interviewees answered new questions to gather a complete picture.

In total, I performed 38 interviews, not counting two follow-up interviews, and received additional input per mail from five contacts, of which three subsequently agreed to an interview. I collected 36 hours of interview material. Table 4 contains an overview of the performed interviews per transaction participant type.

Table 4: Overview of interviews performed

Category	*Type*	*# of interviews*
Experts	Independent industry expert	7
Sellers	Dedicated IP Core provider	17
	EDA-Tool provider	2
	Foundry	1
Buyers	Buyer	7
	FPGA provider	1
Intermediaries	Sales channel for IP Core provider	2
	Market Place	1
Grand Total		**38**

During the interviews, I asked interviewees about the perspective of their current company and for general trends in the industry. Interviewees included relevant insights from previous placements, which helped generate understanding regarding failed companies. Many of the managers and founders of IP Core companies had been previously involved in setting up or running other IP Core providers, some of which ultimately did not succeed. They frequently agreed to share their ideas on the reasons for these failures. Additionally, I was able to clarify statements that contradicted feedback from earlier interviews to advance my understanding of the limits of my developing concepts.

Interviews were coded iteratively using Nvivo, starting with an initial coding scheme that was cyclically refined as new themes emerged through continuing interviews and previous interviews were re-coded to capture all comments befitting of the coding tree, a process termed ‘open coding’ by Strauss and Corbin (1998). Ultimately, I coded along four levels and 91 individual coding items and allocated close to 1.000 interview passages to the coding items in total (see Appendix A 2 for an overview of the interviewees quoted throughout this thesis and Appendix A 3 for an overview of the coding tree).

3.3 Secondary data

In line with the requirements for rigorous case study research (Eisenhardt, 1989; Gioia et al., 2013) I use substantial amounts of secondary data to substantiate and triangulate the information received during the interviews. The following subchapters detail the various sources of data and the data gathered.

3.3.1 Gartner

Gartner, Inc. is a leading market research company with a focus on information technology and high-technology sectors of the economy (Source: Gartner.com homepage) and was described as the "*typical go-to analyst for semiconductor IP*" (Quote interviewee Y). For this thesis, I use Gartner's annual report of the IP Core industry called *Market Share: Semiconductor Design Intellectual Property, Worldwide*, which is considered the "*most credible market research*" (Quote interviewee K) and "*the only one I know*" (Quote interviewee Z) on this particular market.

I had access to reports from the years 2007 through 2015 capturing the years 2006 through 2014 (Gartner, 2007-2015a). Each report contains aggregate revenue information on the top 50 companies including ranking, market share, and relative growth to last year, the same information on a top-10 ranking per product segment (see Figure 1 for a breakdown of the segments and their relative sizes), per revenue type (licensing fee vs. royalty), and, up until the 2013 report (2012 data), also by geography. All analysis on market share information in the IP Core industry relies on this data. Importantly, the Gartner datasets only contain the revenue generated through the licensing of IP Cores, not of other business units. This is especially relevant for companies like the EDA tool providers who generate income from a number of different sources.

Additionally, I had access to a report that tracks all private companies in the semiconductor space (unfortunately no IP Core-specific cut is available and no identifier is included to enable a quick identification of IP Core startups; therefore, the corresponding analysis is not IP Core specific) and provides a view of the number of new entrants to a market as detailed in Section 4.4 (Gartner, 2015b).

3.3.2 IC Insights

IC Insights, another major provider of market research on the high-technology sector, provides several reports on the semiconductor industry. For this thesis, I used the McClean Report (IC Insights, 2007 – 2016) that provides several league tables such as an overall size of the semiconductor industry and of the Fabless sub-segment, again

including market shares. This enables me, in turn, to compute the same analysis I perform for the IP Core industry for the Fabless industry and allows me to compare the results yielding comparative statements regarding market stability, concentration, and revenue variance.

3.3.3 Patstat

For patent data, I use the Patstat offline dataset provided on DVD including the INPADOC database of autumn 2015 by the European Patent Office (EPO).

For identification of the relevant patents, I took the top 25 rankings for both IP Core (Gartner, 2014) and Fabless (IC Insights, 2014) of the year 2013 and performed a name search using tls206 (PERSON_NAME, which contains either the name of the individual or the name of the company that is filing) and manually eliminated non-applicable names (e.g., a text-based search for *ARM* retrieved a large number of non-applicable entries) and created a new table of the corresponding DOC_STD_NAMES and IDs (due to various spelling mistakes in names and the multitude of different organizational units filing patent applications for large multinational corporations, the EPO maintains a directory of standardized names in their DOCDB database that link the names back to a reduced number of families). Using these DOC_STD_NAMES I collected all Person Names again to catch all entries, including those with spelling mistakes (basically using the DOCDB as an intermediate step to ensure the capture of all patents, even those that contain spelling mistakes).

Next, I collected all application IDs of the type “PI” (patents) for the respective firms, yielding a total of 266,106 patent applications across all geographies, as summarized in Figure 3.

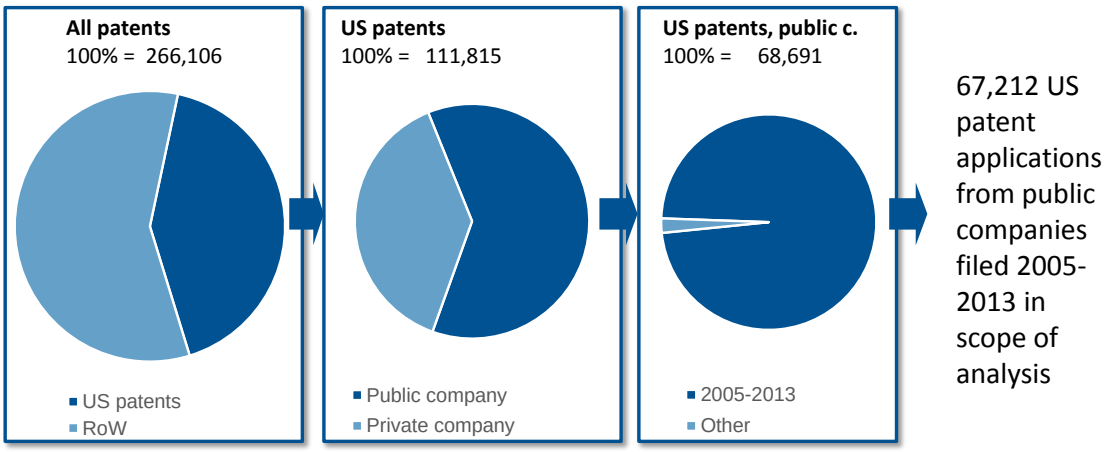


Figure 3: Overview of number of patents captured during analysis; Data: Patstat (2015)

To decide on the scope of the analysis I computed which authority contributed which share of patents. I found that 84% of all patents were filed with six authorities providing the bulk of all patent applications, with by far the largest being the United States with 42% of applications, followed by Japan, China, Europe, Taiwan, and Korea (see Figure 4).

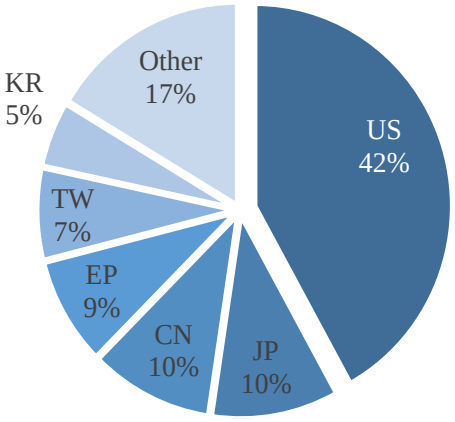


Figure 4: Share of patent applications by Fabless and IP Core companies per filing authority, 1925 – 2015; Source: Patstat (2015)

In order to evaluate whether focusing on only one of these authorities is justifiable (taking out the complexities of considering different patent systems impacting ease of application and underlying cost structures and the risk of double-counting patents that were simply replicated into other geographies) I computed the size of the potential blind spot by calculating the share of patents that were part of patent families that did not contain any patents filed in the United States. I summarize the values of this analysis in Table 5.

So, while for China, for example, a total of 26,872 patents were identified for the full time period and all companies in scope, only 9,020 of these did not contain a single US-filed patent in their patent family. I therefore calculated the share of patents that would be omitted from China for my analysis as 33.6 % since I consider patents that have a family member filed in the United States as technologically closely related (and potentially duplicate) and therefore as captured by my analysis. The total column for the patent applications (showing 222,756 patents) is simply a sum of the patent counts of the six authorities above. For the patent families, the analysis of the individual markets works

the same as for patents, however, the total is not the sum of the lines above, since a patent family with one patent in China and one in Europe (EP) would be counted in both lines, while only being counted once in the total line.

In total, I found that only 16.4% of patents and 29.0% of patent families fall outside the scope of a US-only analysis with the remainder of patents being linked to at least one US patent through a joint patent family. Therefore I decided to focus exclusively on patents filed in the United States.

Table 5: Overview of US coverage of patents filed with top 6 authorities; Data: Patstat (2015)

	Patent applications			Patent families		
Authority	Total Count	Count not US	Share non-US	Total Count	Count not US	Share non-US
CN	26,872	9,020	33.6%	24,306	8,490	34.9%
EP	22,886	2,235	9.8%	19,895	2,073	10.4%
JP	27,763	19,048	68.6%	26,453	18,842	71.2%
KR	13,907	1,235	8.9%	11,831	1,176	9.9%
TW	19,513	4,922	25.2%	18,743	4,827	25.8%
US	111,815	-		74,448	-	
Total	222,756	36,460	**16.4%**	104,844	30,396	**29.0%**

After focusing on US patents, I further limited the sample to publicly held companies since I required data on size and R&D expenditure to control for these influences in my regressions, which were only available for publicly listed companies.

Data availability is also the reason my analysis is limited to the years 2005–2013. The cutoff in the year 2005 was determined by the data availability through Orbis (the Compustat equivalent licensed by Technical University of Munich), which only contains information reaching back 10 years. The cutoff in 2013 was mandated by the patent data where 2014 data on patent applications was scant and potentially subject to a selection bias since patent applications have to be made public after 18 months at the latest, but can be published earlier by the author (United States Patent Office, 2015). Hence, using the fall 2015 Patstat release I could only reasonably assume that all patent applications up until the end of 2013 would be contained. Confirmation for this approach is found from the fairly steady trends of application numbers over the years contrasted by a significant drop in 2014 as depicted in Figure 5 for both Fabless (left axis) and IP Core (right axis). This chart additionally reveals that the number of patents applied for by Fabless companies is almost by the factor 10 higher than that of IP Core companies, although this difference can be partially explained by the behavior of a single company – Qualcomm, which filed 43 % of all patent applications of the Fabless companies in scope in the years 1995 to 2014 (equivalent to three times the patents of all IP Core companies in scope combined).

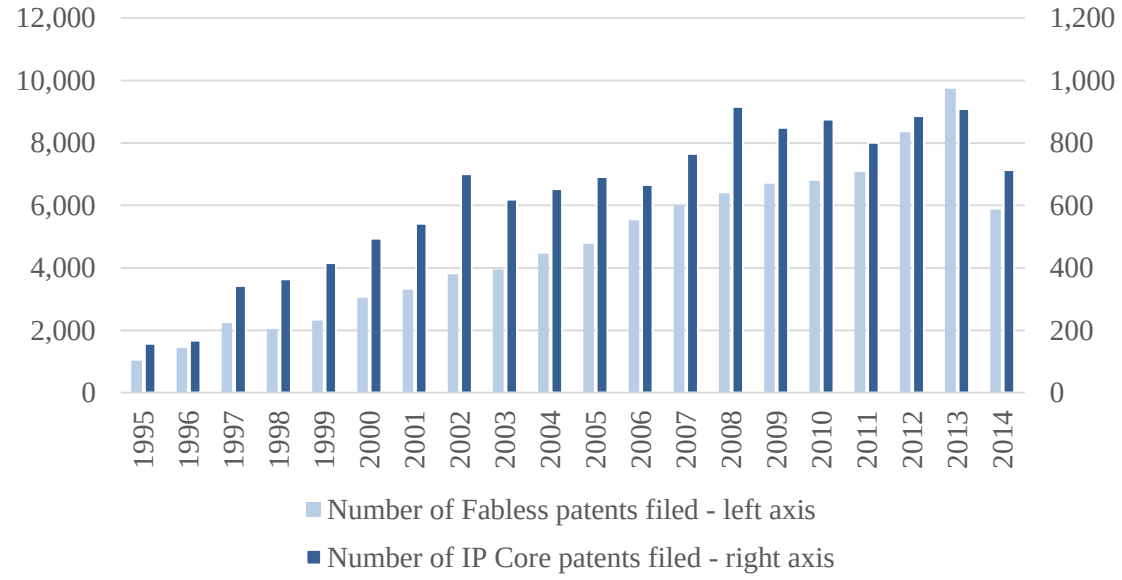


Figure 5: Patent applications per year - IP Core and Fabless; Data: Patstat (2015)

3.3.4 Orbis - Public company information

Orbis is a database by Bureau van Dijk that collects and standardizes publicly available information from various filings for a large number of international companies. The choice for Orbis was made due to the availability of a TUM subscription for the database and a good coverage of the relevant Fabless and IP Core companies.

Due to the large amount of consistent data required for the regression analysis, I focus on publicly listed companies in the top 25 of both Fabless and IP Core charts. The information available on Orbis reaches back 10 years from last filing, so data was available from 2005 to 2015.

I collected the following information for the public companies: *R&D Intensity (percentage of operating revenue spent on R&D)*, *Operating Revenue*, *Number of employees, Profit margin*, *Gross margin*, *Profit per employee*, *Operating revenue per employee*, *Year of inception, Net Assets turnover*. Since I was not able to break out R&D for the business units tasked with creating IP Cores from other business units (which would have been required to use the revenue information provided by Gartner), I used the information for the entire firm and control for the EDA firms (active in developing and selling EDA tools) and for Qualcomm (actively licensing their patent portfolio in addition to licensing IP Cores) via dummies and robustness tests in Chapter 0.

I excluded from this analysis all companies that did not provide information on R&D expenditure since this information was required to calculate the dependent variable.

Descriptive statistics of the firm-year data of companies in scope of this analysis is provided in Table 6 (see Appendix A 4 for a more detailed summary including Quartile

information).

Table 6: Descriptive statistics of companies included for patent analysis; Data: Orbis, Patstat

	IP Core			Fabless		
	Avg	Min	Max	Avg	Min	Max
Revenue (in thsd 2005 USD)	451,626	7,736	1,676,855	1,868,237	82,752	21,249,816
R&D (in thsd 2005 USD)	151,568	2,755	571,875	401,567	10,108	4,244,651
PPE (in thsd 2005 USD)	65,086	464	343,431	319,961	906	4,434,418
Employees	2,030	105	8,573	3,601	195	31,000
Age	18.4	6.0	32.0	18.7	3.0	53.0
Patents filed (per year)	78	0	364	311	0	5,405
Patents granted (per year)	48	0	196	165	0	1,483
R&D intensity	37%	21%	67%	20%	2%	41%
Profit margin	5%	-97%	64%	10%	-158%	44%
Gross margin	83%	50%	118%	51%	8%	77%
Patenting intensity	0.71	-	4.70	0.78	-	4.35

I combined the annual public company information from Orbis with patenting information from Patstat to build a panel dataset containing 255 full firm-year observations from 32 firms.

3.3.5 Analyst reports / online sources

Several analyst reports and online Internet pages and blogs were used in preparing for the interviews and for cross-checking with interviewees on industry dynamics, although they did not find direct access into this dissertation. The most notable sources used were semiwiki.com for background reports and blogs by industry experts on industry trends and firm characteristics, chipworks.com for teardown reports of actual products (such as iPhones) and background information on design wins and losses, and Anandtech.com for company profiles.

In order to identify smaller companies for interviews I utilized the homepages of Xilinx and Altera, the two principal manufacturers of FPGAs that maintain and certify a sizable network of IP Core developing partners.

3.3.6 Design&Reuse

Design&Reuse, one of the largest market places, invited me to their 2015 IP SoC conference in Grenoble, providing another valuable source of contacts to IP Core providers. The keynote speakers provided a profound view into both demand and supply side concerns regarding the provision of IP Cores that were subsequently verified during the interviews.

After summarizing the methodology used for the qualitative proportion of this thesis and outlining the secondary data used to triangulate and substantiate my findings, the next chapter details several bespoke analyses of the market for IP Core.

4 Analysis of Market and Provider Performance

A large part of the findings in later chapters and of the contribution of this thesis to the understanding of MfT hinges on the market for IP Cores actually constituting a well-functioning market. Therefore, in the following sections I describe the performance of the market as a whole and of the various stakeholders active in this industry. To allow for claims with regard to stability and viability, which are difficult to substantiate due to the lack of a generally accepted definition, I frequently employ comparisons with the Fabless market (introduced in Section 2.2.2); Fabless companies are considered the "prevailing business model [of the semiconductor industry] today" (Nenni and McLellan, 2013, p. vii) and are accepted as well-functioning and significant contributors to that industry (e.g., Nenni and McLellan, 2014; Tuomi, 2009). From a theoretical point of view, this chapter is relevant because it is one of the first quantitative explorations of the performance of dedicated, specialized technology providers, the enablement of which is considered one of the key benefits of MfT (Arora et al., 2001a). The vast majority of prior research focuses on technology interchanges such as patent licensing, which are typically not the core function of the firms performing them. The few papers that look into specialized technology providers are based on qualitative case studies and do not contain quantitative data and therefore are unable to answer the question of how well the specialized technology providers perform compared with the alternative business model of selling products.

In order to make a claim with regard to the stability of the market for IP Core, I first I investigate the market as a whole (Section 4.1) by analyzing the total revenue growth of the observable market (top 50 providers by revenue through Gartner ranking), the share of revenue that stems from companies that were not in the ranking the year before, and the stability of the rankings to make claims regarding stability on the overall market level. To understand whether these findings are only applicable for a few large dominating firms, I shift my focus to the concentration of the market and the three main technological subclasses of the IP Core market (Section 4.2). To answer the question from an individual firm's perspective, I analyze the revenue variance (Section 4.3) to gain an insight into whether design companies are subject to a higher variance than product companies and to understand whether the companies at the top or at the bottom of the ranking are subject to higher fluctuations; the continuity of revenue has serious implications on the ability to finance the next round of innovations. As a complement to the analysis of the share of revenue from companies outside the ranking, I next use a separate dataset to analyze the

number of new entrants to the market since the focus on the top 50 companies typically excludes new entrants who have not yet reached a size to fit in these rankings, however, they serve as an early indicator for the overall attractiveness of the market to new entrants over time (Section 4.4). In Section 4.5, I analyze the patenting success rate of the top 25 IP Core and Fabless companies since ownership of patents is highly important to the ability of semiconductor companies to remain competitive (see, e.g., Hall and Ziedonis, 2001), but at the same time constitutes a significant strain on company resources. In Section 4.6, I distinguish the underlying business models into three types, which provides further insights into why some company types are predestined to offer certain types of products. Section 4.7 closes the analysis with a discussion of limitations of the analysis performed and Section 4.8 summarizes the findings and implications of this chapter for the market for IP Cores.

4.1 Market dynamics

The market for IP Cores is an interesting object of study because it is well-established, growing, and has achieved a degree of stability comparable to a product market. While the computation of growth in terms of sales is straightforward, I measure stability by identifying 1) the share of revenue that stems from companies new to the ranking, 2) the share of firms that are in the top 50 ranking in 2014 that were already present for each of the previous years (i.e., a measure of longevity of firms in the ranking), and 3) the number of companies that dropped out of the top 50 ranking by drop-out reason of the market for IP Cores. I compare each of these stability indicators to the respective values for the Fabless industry.

The size and growth of the market for IP Cores is reported as part of the annual *Semiconductor Intellectual Property Report by Gartner* (2007-2015) and shown in Figure 6[13]. It shows that the market stagnated around 1.3 billion USD of revenue between 2007 and 2009 but has since regained momentum and has grown steadily with a compound annual growth rate (CAGR) of about 15% between 2009 and 2014. Additionally the graph reveals that while the level of revenue of the Fabless market is significantly higher, the change in revenue over the years closely mirrors the change in revenue of the IP Core

[13] Tuomi (2009, p. 43) has a different version of this based on the same reports, which show continuous growth of the IP Core industry from 1999 to 2008. This difference is due to Tuomi reporting the sum of the categories ‘technology licensing’ and ‘Design IP’ as available in the Gartner reports up to the year 2008. Since the ‘technology licensing’ category is no longer reported as of 2009 and I am primarily interested in the trading of IP Cores, I only show the revenues associated reported as ‘Design IP.’

market, thus showing a comparable reaction to the financial crisis of the years 2008 and 2009.

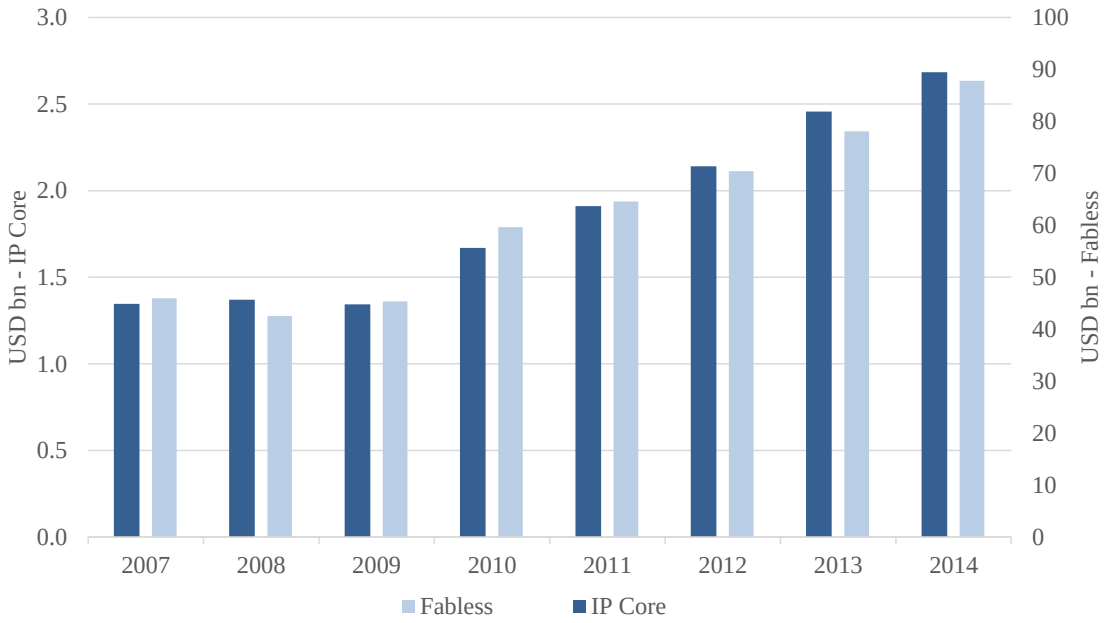


Figure 6: Annual total 'Design IP' market revenue of the IP Core – left axis - and total revenue of the Fabless industry – right axis - in billion USD; Data: Gartner, IC Insight

To understand whether the growth stems from a volatile environment with a large number of companies entering and exiting the market or from a stable set of companies that are continuously expanding their revenue, I analyze the percentage of revenue that stems from companies that are new to the top 50 in a given year (light blue) compared with revenues generated by companies that were already present in that ranking the year before (dark blue) in Figure 7. The low share of revenues of companies that were not in the ranking the year before (consistently between 2% and 5% across all 7 years of analysis) reveals that growth of the incumbent firms, and not that of new entrants to the ranking, is what primarily drives the growth shown in Figure 6.

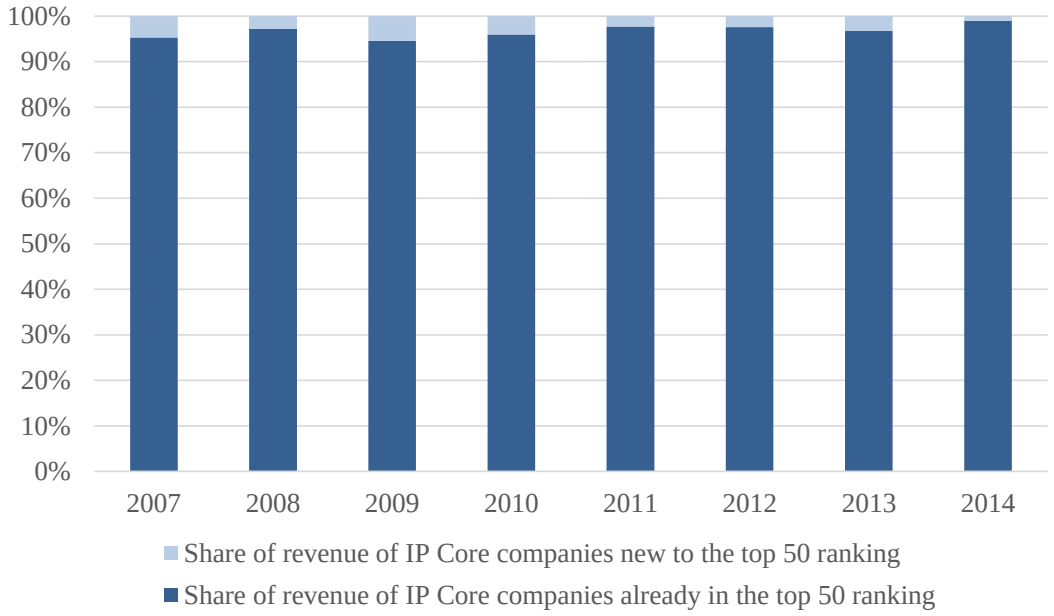


Figure 7: Share of revenues from companies new to the top 50 rankings vs. companies already in the top 50 ranking the year before for the IP Core market; Data: Gartner

Comparing this share of the revenue of companies that were not in the top 50 ranking the year before with the respective values for the Fabless market, reveals that both markets feature a similar share of revenue of new entrants, with the exception of the year 2009 (see Figure 8). This is due to the entry of AMD into the Fabless rankings after carving out the manufacturing business. The data is only compared between 2008 and 2014 because the corresponding top 50 Fabless ranking is only available as of 2007 (the previous year only contains the top 40, which would distort our analysis). Therefore, the first statement made with regard to new vs. old firms is as of the 2008 ranking.

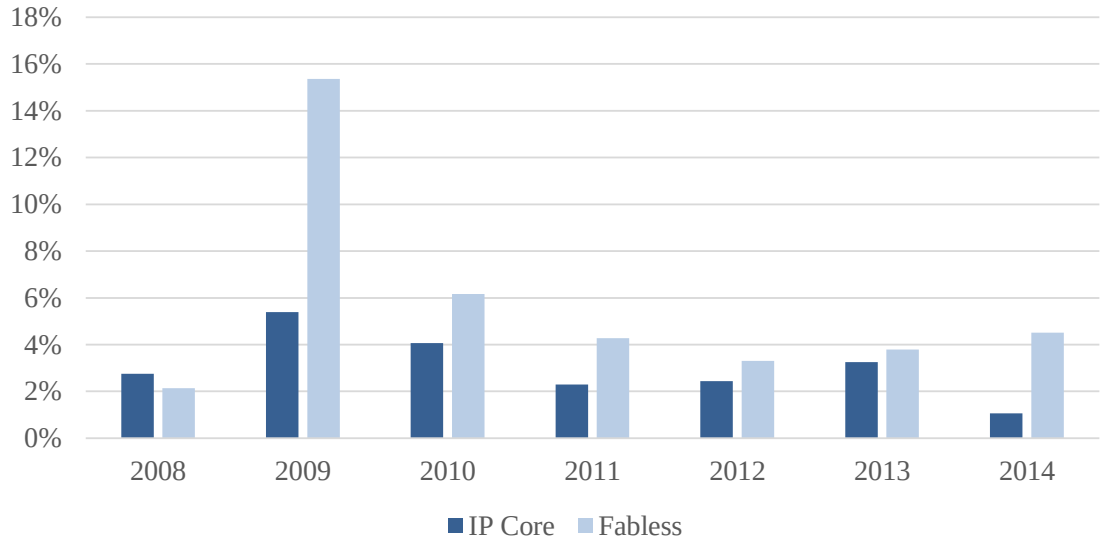


Figure 8: Share of revenues from companies new to the top 50 ranking - IP Core vs. Fabless; Data: Gartner, IC Insight

To develop a perspective on the total number of new entrants to the top 50 ranking over time, I compare the companies of the 2014 top 50 ranking with the companies constituting the top 50 rankings of the previous years and calculate the share of 2014 companies that were already present in the top 50 ranking of each vintage. To allow for a qualitative evaluation of these fluctuations, I additionally compare them to the stability of the top 50 ranking of Fabless companies using the McClean report on Fabless companies provided by IC Insights (2007-2015) using the same approach and find that the longevity of companies in the top 50 rankings is comparable for our observation period as visualized in Figure 9. I therefore conclude that the market for IP Cores is stable in both the short term and medium term on a comparable level with the Fabless market.

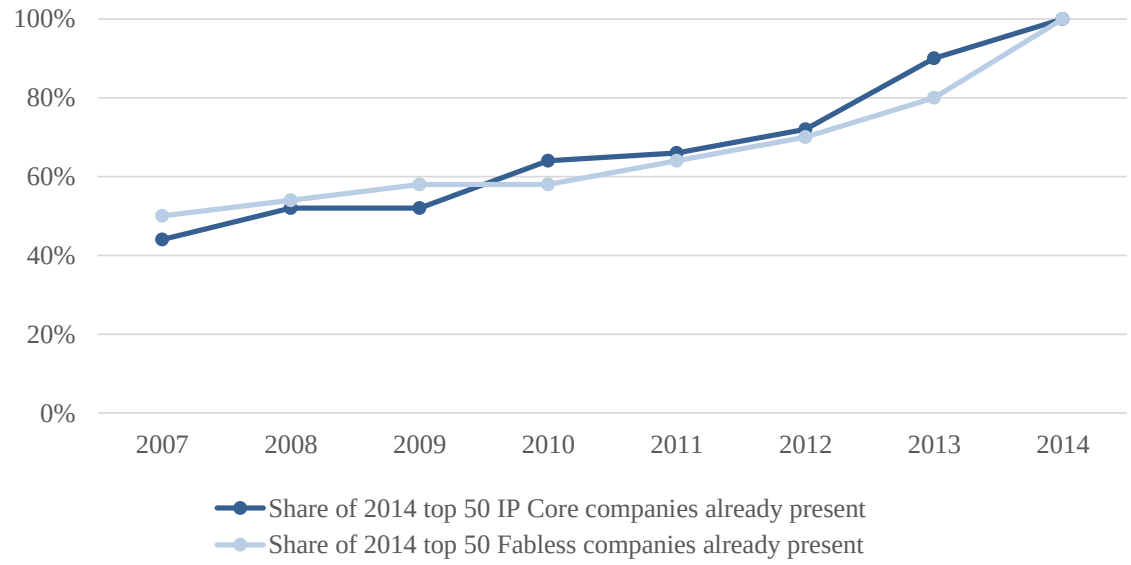


Figure 9: Comparison of stability between IP Core and Fabless top 50 rankings between 2007 and 2014; Data: Gartner, IC Insight

Finally, an analysis of the reasons for the firms dropping out of the top 50 rankings between 2006 and 2014 [14] (Baumeister, 2016; Wolz, 2016) as summarized in Table 7 reveals two things. On the one hand, the number of companies permanently exiting the top 50 ranking for Fabless firms is comparable to the respective number of companies for the market for IP Cores (and correspondingly of new companies entering the ranking). However, the share of companies exiting the ranking because of having been acquired is substantially higher for IP Core companies compared with Fabless companies. Not a single IP Core company dropped out due to bankruptcy and only two companies dropped out of the Fabless ranking for this reason. This indicates that companies either tend to shrink in revenue for a long time, thereby disappearing off the rankings before they go bankrupt, or another company acquires them.

[14] I consider a firm drop-out only when it does not subsequently reappear in the rankings. A company that dropped out in 2009, reappeared in 2010, and dropped out again in 2011 qualifies as a drop out only once, in the year 2011.

Table 7: Summary of reasons for drop-out of Top 50 ranking 2006 – 2014 - IP Core and Fabless

	IP Core		Fabless	
M&A	31	61%	18	40%
Bankruptcy		0%	2	4%
Decline in Revenue	16	31%	22	49%
Change in Business Model	4	8%	3	7%
Total	51		45	

The similarity of market stability as exhibited by the number of companies disappearing from the Fabless top 50 ranking and the corresponding figure for IP Core is further reinforced by the resemblance of the relative revenue share contributed by new firms (firms that have not been in the ranking the year before, thus, the data contained in Figure 8).

These findings suggest that the product and the technology market under observation are of similar stability. This is surprising considering the substantially lower barriers to entry into the market for IP Cores in terms of skill and capital required. Three interviewees contrasted the prospects of entering the market for IP Cores with entering the Fabless market: "*Entering the [IP Core] market is easy. Any unemployed engineer and a couple of friends with knowledge in a particular application space (e.g., video processing or PCI express communications) can start an IP company. Little more capital is needed than what is required to pay salaries*" (Quote interviewee L); "*being a Fabless provider or a Fabless startup is very difficult these days of course. Mask costs are very high, also packaging*" (Quote interviewee Y), and "*The last Fabless semicon company in which I was involved was 2007. We underestimated how much money we would need. To get a somewhat reasonable foothold that would have been a 100 million USD trip. ROI [return on investment] combined with the likelihood of success was too low for any investors to take on that risk. […] Therefore there are practically no startups anymore in Fabless*" (Quote interviewee S, translated).

4.2 Concentration analysis

Besides the new entrants into the Top 50 rankings, I was interested in how the remainder of the ranking is composed structurally—are there a few very large companies (or even one) at the top with the rest being comparatively small companies, or is the Top 50 ranking more evenly distributed with a lot of large companies vying for dominance of

the market.

To answer this question I compute the Herfindahl-Hirschman Index (HHI) by squaring the relative market share of each company and then adding it up (thus either ranging from 0-1 in case absolute values are used (as in this thesis) or from 0-10,000 in case percentage values are used) as detailed in Equation 1.

Equation 1: Herfindahl-Hirschman index

$$HHI = \sum_{i}^{N} s_i^2$$

s: Market share of firm i

N: number of firms in market

Due to the squaring of the market shares, markets with few dominant firms with high market shares and a long tail of very small firms will result in a higher HHI than markets with many firms with equal market share. Accordingly the HHI can be used as a measure of industry concentration with an HHI of below 0.15 considered 'unconcentrated,' between 0.15 and 0.25 'moderately concentrated,' and above 0.25 as 'highly concentrated' by the US Department of Justice in their *Horizontal Merger Guidelines* (U. S. Department of Justice, 2010).

A comparison of the annual HHI of the Top 50 companies of the market for IP Cores and the Fabless market reveals that while the Fabless market is unconcentrated and the trend is flat. The market for IP Cores has a higher concentration and has been classified as moderate since 2011; it is approaching a state of high concentration with an unbroken positive trend up to 2014, the last year the data was available (see Figure 10). The 2006 HHI value for the Fabless market is based on a top 40 ranking.[15]

[15] This fact has no impact on the HHI since a robustness check estimating the increase in HHI if all companies were included in the computation of the HHI and if all remaining companies were the same size as the 40th ranked company reveals that this would only change the total HHI by 0.00067, a negligible amount.

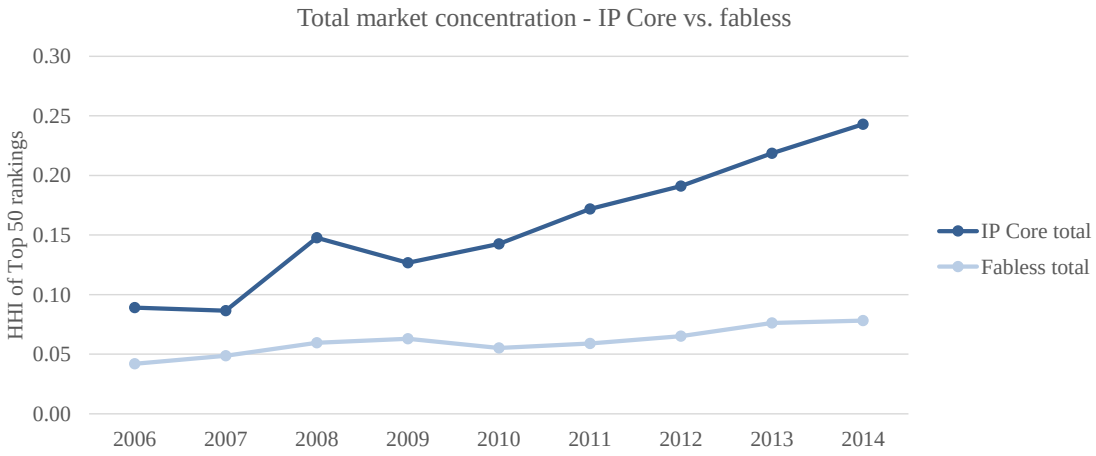


Figure 10: HHI of Market for IP Core and Fabless; Data: Gartner, IC Insight

For a deeper understanding of the extraordinary trend of the market for IP Cores, I utilize the detailed reporting in sub-segments of Processor IP, Physical IP, and Other Digital IP using the segments detailed in Figure 1 in Section 2.2.1. Because the reports on these sub-segments only detail the Top 10 market participants and their respective market shares in these subcategories, I cannot compute the HHI based on the entire population. Since the market share report is based on the total market size (and not just relative to the Top 50 companies), I can compute a lower bound to the HHI since several small elements of the sum detailed in Equation 1 are missing, but the individual quotients are not distorted. A robustness check of the difference between upper and lower bounds of the HHI values reveals that the gap is, in most cases, very small[16] (see Appendix A 5, Table 24).

I split our analysis by looking separately at each of the three segments 'Processor IP,' 'Physical IP,' and 'Other IP' and discuss the impacts of the sub-segments for each of these three segments.

Probably the most conclusive segment in trying to understand the increasing concentration is the Processor IP segment. The charts for the segments always contain the technology sub-segments (such as Microprocessors and DSP) and the overall, combined segment concentration (such as Processor IP – Total). In this segment both sub-segments of Microprocessors and DSPs are highly concentrated. However, while the concentration

[16] Only two years in the sub-segment 'Controllers and Peripherals' within the 'Other IP' segment show a substantial possible difference of 0.03 driven by a low number of market participants identified and a substantial share of market captured by participants classified as 'Other,' which, in combination leads to the possibility of few large companies constituting the rest of the market and thereby having a large impact on the HHI.

of DSP is decreasing, the trend for Microprocessors is steadily positive and the HHI reaches values of 0.84 in 2014, as shown in Figure 11 (see Appendix A 5 for all concentration figures). That is the result of one company capturing 82.9% of the market, the second largest being 5.2%, with the sixth largest provider in this market already having only 1.0% of market share. In short, this graph captures the success story of one company that has achieved a dominant position in the IP Core market for microprocessors —ARM.

Since the sub-segment for microprocessors also happens to be the largest sub-segment in the market for IP Cores, with a revenue based market share of 42.7% of the overall IP Core market in 2014, the high concentration in this relevant sub-segment contributes strongly to the increasing concentration in the overall HHI of the market for IP Cores.

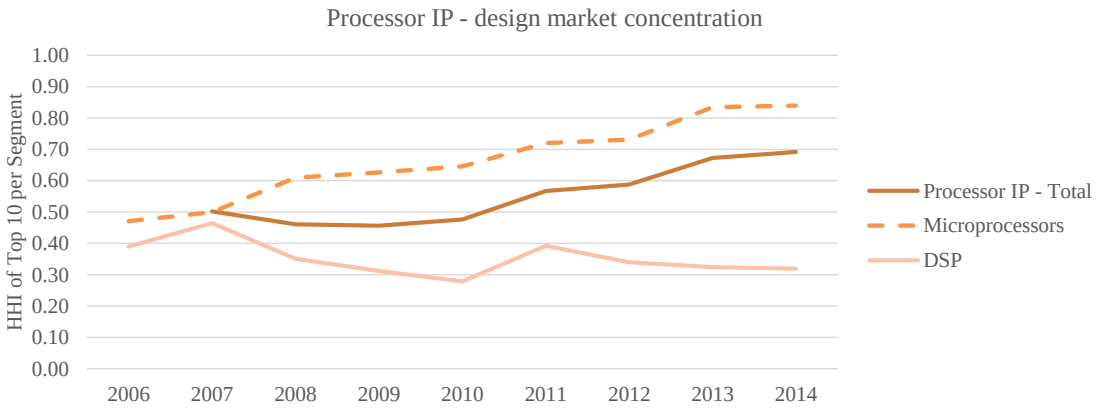


Figure 11: HHI of Market for IP Core, Processor IP segment; Data: Gartner

For the other two segments, the observations are not as clear-cut. In the segment for physical IP (Figure 12), most segments are low to moderately concentrated with only the Physical Library sub-segment being in the area of high concentration. However the level of concentration for this sub-segment (and the others, as well) is stable and is a very small sub-segment at 2.7 % market share. The two more sizable markets of Wired and Wireless Interface (separated in Figure 1, but reported jointly here due to variations in the reporting of Gartner over the years) at 18.8% and Memory Cells/Blocks at 9.4% are both moderately concentrated at around 0.2 in the year 2014 with a modest increase in concentration for the overall market driven by the largest sub-segment of Wired and Wireless Interface, yet nowhere close to strong enough to explain the overall trend on its own.

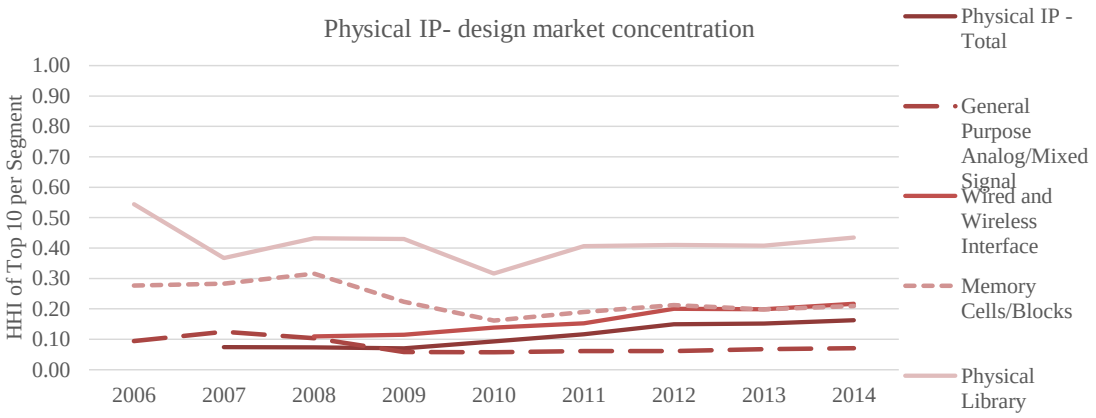


Figure 12: HHI of Market for IP Core, Physical IP segment; Data: Gartner

The last segment, Other IP (detailed in Figure13), contains the largest heterogeneity in terms of concentration between the sub-segments. The most obvious line at basically full concentration around a single firm is the Block Libraries sub-segment, however at 0.7 % market share it is too small to impact the overall concentration to any significant amount; additionally, it stagnates as of 2007 and therefore cannot explain the continuously increasing trend. The Fixed Function Signal sub-segment, which also contains Graphics IP in this chart (again due to differences in reporting of this segment over the years in the Gartner reports), is the only sub-segment sizable enough to have a potential impact on the overall trend. Indeed, I do see a steady increase from 0.12 in the year 2006 to 0.28, or high concentration in 2014 thereby contributing to the overall increase in concentration.

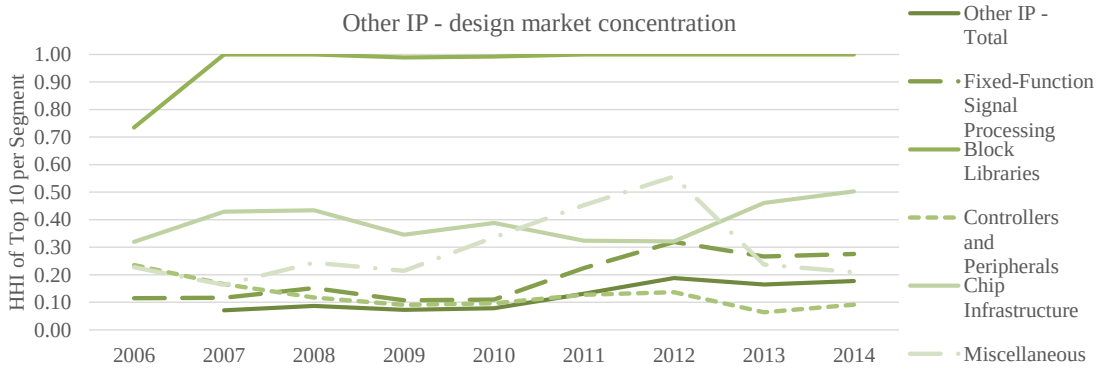


Figure 13: HHI of Market for IP Core, Other IP segment; Data: Gartner

One final element that cannot be captured by splitting the market into its sub-segments is that some of the most successful companies have added to their product offerings over the years and expanded into new segments of IP Cores. Since the full-market ranking (Figure 10) is captured on a combined firm level, this effect additionally

contributes to an increasing market concentration. As summarized by one manager, "*So an SoC vendor like Texas Instruments or Qualcomm whoever was building a chip, would license the CPU from company A* (name confidential) *and then would license the graphics and the video from company B* (name confidential). *That kind of lasted for probably about a decade until both company A and company B decided that actually it would be beneficial to expand their portfolio and add more product lines*" (Quote interviewee E).

4.3 Revenue variance

Prior literature on IP Cores lists a multitude of business models available to IP Core providers with the prominent distinction between companies charging one-time licensing fees and those that additionally charge running royalties (Linden and Somaya, 2003; Tuomi, 2009). The reliance on one-time licensing fees would result in significant discontinuity in revenue generation and could make it difficult for companies to fund the development of the next generation of IP Cores. This opinion is supported by one interviewee who described the impact of exclusive one-time licenses (which are an extreme form of the business model around one-time licensing fees) with the words, "*Basically that killed a lot of companies in the IP [Core] industry. They get money once for their Core and after that there is no new money anymore. But they need money to fund the development of their future Cores. […]A successful IP business depends on the business model. You need to get reasonable amounts of money for your IP and that regularly*" (Quote Interviewee J, translated). Through an analysis of the variance of revenue and comparing it between the IP Core and Fabless companies (who as sellers of products are not subject to one-time licensing fee revenue variance), I test my hypothesis that technology providers are subject to a significantly more discontinuous revenue generation compared with product providers. Additionally, this analysis shifts the focus from the entire market to the individual company by asking the question "how volatile is the revenue" for IP Core companies compared with Fabless companies. To answer this question, I again use the rankings of Top 50 companies for both IP Core (Gartner 2007 – 2015) and Fabless (IC Insights 2007 – 2015) and calculate the change in revenue between consecutive years. Due to the limited data availability for the Top 50 companies, I cannot compute the revenue change for any companies that have not been in the ranking for the year before; I will discuss the possible impacts of this limitation at the end of this section.

I perform three variations of this analysis that compare the revenue variance between IP Core and Fabless companies (Figure 14 and Table 8), between the top and

bottom halves of the ranking for both IP Cores (Figure 15 and Table 9) and the top and bottom halves of the Fabless ranking (Figure 16 and Table 10).

I explain the analysis using the example of comparison between IP Core and Fabless companies for the year 2007. I first compute the change in revenue for all companies contained in the Top 50 ranking for the year 2007 that were also present in the Top 50 ranking for the year 2006 separately for IP Core and Fabless companies. For the two vectors containing the revenue growth values for both IP Core and Fabless firms, I compute the mean value and the standard deviation. I then aggregate this information into a chart containing two bars (one for IP Core and one for Fabless companies) representing the mean values of each vector via the height of the bar chart and the standard deviation by error bars. I repeat this approach for every year and ultimately compute an overall bar for IP Core and Fabless by aggregating the revenue growth values of all the individual years.

Subsequently, I employ a two-sided t test for both vectors of growth values to check for (non-)equal means of the distributions of revenue growth of IP Core and Fabless companies. I report the p values in a table below each figure (IP Core vs. Fabless companies—Figure 14 and Table 8; top 25 and bottom 25 in IP Core rankings—Figure 15 and Table 9; top 25 and bottom 25 Fabless rankings—Figure 16 and Table 10).

Considering the mean values of the revenue growth figures of IP Core companies compared with Fabless companies over the years, no structural difference between the two company types is apparent. IP Core companies' average revenue growth is higher for 3 years and Fabless companies' average growth is higher for 4 years. Also, the size of the standard deviation is not systematically greater for one of the two company types with IP Core companies having a higher standard deviation with regard to revenue growth for 4 years compared with 3 years for Fabless companies. These observations are confirmed by the summary statistics for all years, which put average revenue growth for IP Core vs. Fabless companies at 6.6% and 9.2%, respectively, with standard deviations of 32.0% and 31.8%, respectively, showing that the difference of means between populations is way smaller than the standard deviations within populations.

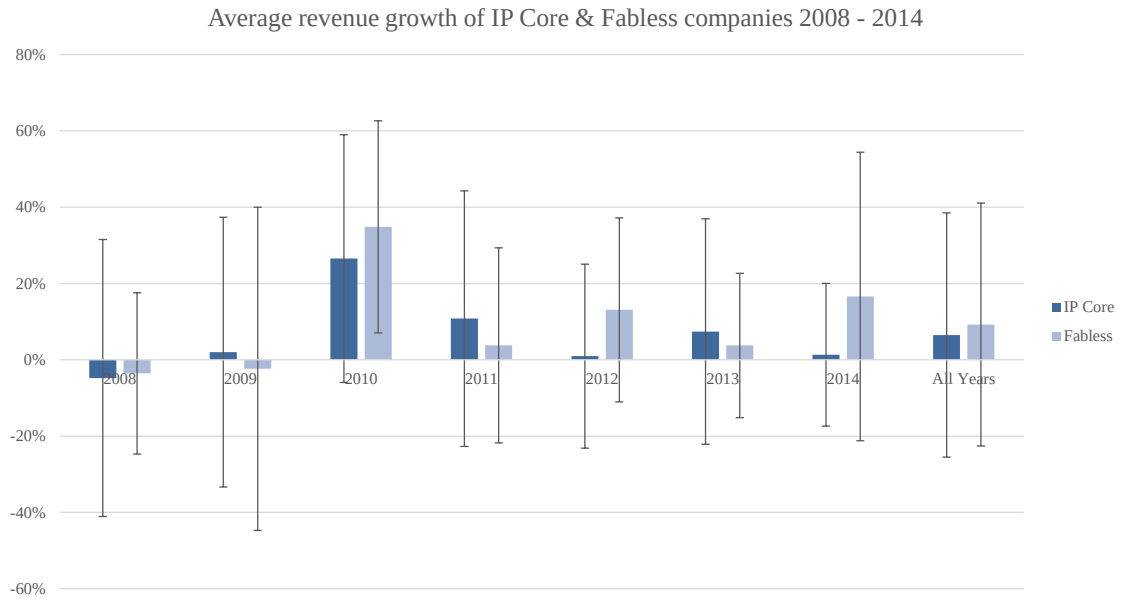


Figure 14: Average revenue growth of IP Core & Fabless companies; Data: Gartner, IC Insight

This similarity between IP Core and Fabless company growth prospects over the years translates into a high p-value of the two-sided t-tests of 31.3 % (see Appendix A 6 for detailed information on mean values, standard deviations, and number of observations per period), as detailed in Table 8.

These observations and statistical tests lead me to conclude that the comparison of the revenue variance between individual IP Core and Fabless companies reveals no significant differences with regard to revenue variance between technology and product firms. However, there is an exception for the years 2011 and 2013 when the null hypothesis that the distribution of IP Core companies' and Fabless companies' revenue growth follows the same distribution could be rejected at statistically significant levels ($p = 0.0\%$ in 2011 and $p = 2.6\%$ in 2013). The difference between the mean values between IP Core and Fabless companies in 2014 is driven by two outliers in the Fabless rankings that exhibited revenue increases of 138% and 196%, which explains why the significance of the difference in revenue variance is small despite strong differences in the mean values (one extreme outlier of a medium-sized IP Core company growing by 814% between 2012 and 2013 due to M&A activity was eliminated from the data). When considering the growth values over all the years of the two sets of companies, the null could not be rejected at any acceptable significance level.

Table 8: Two sided t-test of average revenue growth of IP Core & Fabless companies; Data: Gartner, IC Insight

		2008	2009	2010	2011	2012	2013	2014	All Years
IP Core	Mean Rev Growth	-4.8%	2.0%	26.5%	10.8%	1.0%	7.4% *	1.4%	6.5%
	Observations	41	39	43	45	41	40	45	294
Fabless	Mean Rev Growth	-3.6%	-2.3%	34.9%	3.8%	13.1%	3.8%	16.6%	9.2%
	Observations	45	42	41	43	42	41	42	296
	P-value of 2-sided t-test	**85.3%**	**62.0%**	**21.5%**	**0.0%**	**27.9%**	**2.6%**	**51.6%**	**29.4%**

** 1 outlier eliminated*

Diving deeper into the respective markets, I next look at the question of whether there are any systematic differences between the growth prospects of small companies compared with large companies. In order to answer this question, I split my Top 50 ranking in half and compare the average revenue growth experienced by the Top 25 of the Top 50 ranking with the average revenue growth of the Bottom 25 of the Top 50 ranking (i.e., ranks 26 to 50). Since this analysis again requires information on revenue from the current and the previous year, not all entries will be available for analysis.

The single most interesting result in the analysis of the IP Core industry is that the Top 25 exhibit a higher average revenue growth than the Bottom 25 in six out of the seven years with the exception of 2009 as shown in Figure 15. This translates into an average growth of 12% across all years for the Top 25, contrasted by 0% or no growth for the Bottom 25. There appears to be no obvious trend with regard to standard deviation being higher in the Top 25 or Bottom 25 resulting in pretty comparable standard deviations across all years of 33% for Top 25 and 30% for Bottom 25.

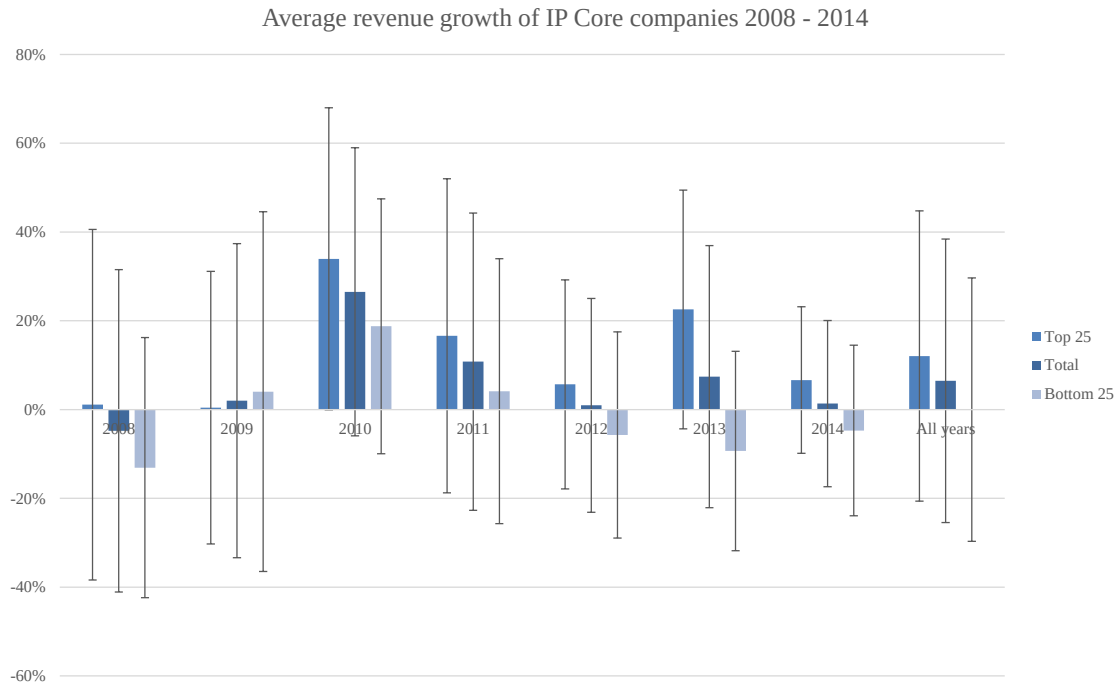


Figure 15: Average revenue growth of IP Core companies, top 25 vs. bottom 25; Data: Gartner

I employ a two-sided t-test to quantify whether there are any systematic differences between the growth rate of the top and bottom halves, and reveal that while the resulting p-values are small for each year (potentially due to the low number of observations between 17 and 24 per year and group), except for 2013 I do find that I can reject the null hypothesis of both distributions having the same mean to a high significance level of 1% ($p = 0.11\%$), as summarized in Table 9. This somewhat surprising result suggests that not only do the large firms grow faster than the small firms in absolute terms (for which equal percentage-based growth rates would suffice) they even grow faster in relative terms leading to an increasing concentration of the market in the absence of exits of high-ranking firms.

Table 9: Two sided t-test of average revenue growth of IP Core companies, top 25 vs. bottom 25; Data: Gartner

Two-sided t-tests of revenue growth Top 25 vs. Bottom 25 - IP Core

		2008	2009	2010	2011	2012	2013	2014	All years
Top 25	Mean Rev Growth	1.1%	0.4%	33.9%	16.6%	5.7%	22.6% *	6.7%	12.1%
	Observations	24	22	22	24	23	20 *	23	158
Bottom 25	Mean Rev Growth	-13.1%	4.0%	18.8%	4.1%	-5.7%	-9.3%	-4.7%	0.0%
	Observations	17	17	21	21	18	20	22	136
	P-value of 2-sided t-test	**20.6%**	**76.9%**	**13.0%**	**21.6%**	**14.4%**	**0.1%**	**6.8%**	**0.1%**

** 1 outlier eliminated*

Next, I compute the comparison of the Top and Bottom 25 for the Fabless industry to enable comparison of the results with the IP Core industry in an effort to disentangle whether the effect of faster growth of large companies is a common characteristic of the semiconductor market or specific to the market for IP Cores. Figure 16 summarizes the results.

I do observe the same pattern for the IP Core companies that the Top 25 grow faster than the Bottom 25, and it is even more pronounced for the Fabless companies with the Top 25 growing faster in every single year analyzed. The resulting mean revenue growth across the years is comparable to IP Core companies both in individual size and difference between large and small companies at 14% and 3%, respectively (IP Core: 13% and 1%). One difference is that the standard deviation is higher for the larger firms than for the smaller firms at 36% compared with 25%, which in itself is surprising since this implies that there does not appear to be an inertia in revenue related to company size.

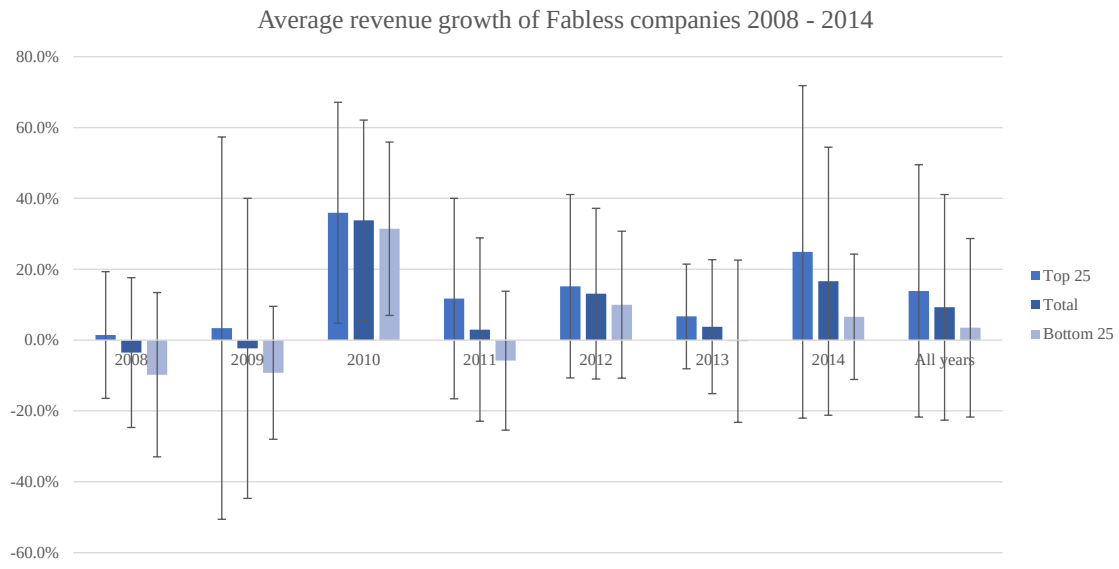


Figure 16: Average revenue growth of Fabless companies, top 25 vs. bottom 25; Data: IC Insight

Just as with the IP Core companies, I find that the p-values of the two-sided t-tests of the individual years of the Fabless companies are not significant with the exception of 2011 (not the same year as it was for IP Cores). Yet, when combining all observations from the various years, I can again reject the null of equal mean values at a high significance level of 1% (see Table 10).

Table 10: Two sided t-test of average revenue growth of Fabless companies, top 25 vs. bottom 25; Data: IC Insight

		2008	2009	2010	2011	2012	2013	2014	All Years
Top 25	Mean Rev Growth	1.4%	3.4%	36.0%	11.7%	15.2%	6.7%	24.9%	13.9%
	Observations	25	23	22	22	25	24	23	164
Bottom 25	Mean Rev Growth	-9.8%	-9.3%	33.6%	-4.5%	10.0%	-0.3%	6.6%	3.5%
	Observations	20	19	19	21	17	17	19	132
	P-value of 2-sided t-test	**9.1%**	**31.4%**	**78.9%**	**3.7%**	**48.6%**	**29.2%**	**10.2%**	**0.4%**

To further substantiate the finding that large companies grow faster than small companies, I compute Spearman's rank correlation coefficients between the rank and the revenue growth for IP Core and Fabless companies using the Spearman correlation coefficient (see Appendix A 6 for a graphical representations of the data as support regarding the required monotony of the datasets). To allow for a more granular analysis of the phenomenon, I split the analysis by year (*all years* plus 7 individual years 2008 – 2014), by position in the ranking (*full ranking*, *top 25*, *bottom 25*), and by company type (*IP Core*, *Fabless*) resulting in the 48 subsets of analysis contained in Table 11.

Table 11: Spearman's rank correlation coefficients for IP Core and Fabless companies; Data: Gartner, IC Insight

			All years	2008	2009	2010	2011	2012	2013	2014
IP Core	Full ranking	Rho	-0.25	-0.21	-0.02	-0.25	-0.26	-0.36	-0.57	-0.51
		p-value	0.0%	19.9%	90.9%	10.6%	8.3%	2.0%	0.0%	0.0%
		Obs	*295*	*41*	*39*	*43*	*45*	*41*	*41*	*45*
	Top 25	Rho	-0.13	-0.14	-0.04	-0.03	-0.25	-0.27	0.02	-0.38
		p-value	9.8%	52.6%	86.5%	88.5%	23.6%	19.4%	92.3%	6.6%
		Obs	*164*	*24*	*24*	*22*	*24*	*24*	*22*	*24*
	Bottom 25	Rho	-0.23	-0.15	-0.34	-0.42	-0.20	-0.16	-0.23	-0.28
		p-value	0.9%	57.3%	21.1%	5.9%	37.8%	54.8%	34.8%	22.5%
		Obs	*131*	*17*	*15*	*21*	*21*	*17*	*19*	*21*
Fabless	Full ranking	Rho	-0.18	-0.27	-0.25	-0.09	-0.46	0.01	-0.12	-0.27
		p-value	0.1%	7.3%	11.4%	56.2%	0.2%	94.8%	46.6%	8.4%
		Obs	*298*	*45*	*42*	*42*	*44*	*42*	*41*	*42*
	Top 25	Rho	-0.07	-0.06	-0.14	0.14	0.02	0.09	-0.14	-0.35
		p-value	34.3%	76.5%	52.3%	54.3%	91.9%	67.4%	50.4%	9.9%
		Obs	*164*	*25*	*23*	*22*	*22*	*25*	*24*	*23*
	Bottom 25	Rho	-0.22	-0.02	-0.45	-0.48	-0.59	0.02	0.01	-0.15
		p-value	1.2%	91.7%	5.1%	3.1%	0.4%	94.8%	97.0%	53.8%
		Obs	*134*	*20*	*19*	*20*	*22*	*17*	*17*	*19*

The table provides three insights (see Appendix A 6 for a color-coded version of the chart that is visually more accessible). First, the rho values of all 18 subsets of analysis where the p-value is below the 10% significance level are negative and therefore confirm my earlier findings of winner takes all markets for both IP Core and Fabless companies

where a higher (i.e., less revenue) rank is correlated with a lower percentage-based revenue growth. Second, I find that this phenomenon is mostly driven by companies in the Bottom 25 ranking where the negative correlation between ranking and revenue growth is stronger compared with the Top 25 companies in the 'All years' column both in terms of magnitude (IP Core rho-values of -0.23 vs. -0.13 and Fabless rho-values of -0.22 vs. -0.07), as well as significance (IP Core p-values of 0.9% vs. 9.8% and Fabless p-values of 1.2% vs. 34.3%) over all the years. Finally, I find that the negative correlation for the technology providers is stronger than the one for the product providers for the full ranking and both subsets.

When considering all years, the high significance of the results highlights that the weak significance in the majority of the individual years (30 of 48 subsets are non-significant) is likely due to the low number of observations rather than the phenomenon not being true.

As mentioned at the beginning of this chapter, one possible cause for concern of these analysis (revenue variance and rank correlation) is that I cannot observe growth amid companies that just entered (or exited) the ranking of the 50 largest companies since there is no data available for these companies. Since I also compare growth of the Top 25 compared with the Bottom 25 of the Top 50 ranking, I face a potential structural difference in the composition of the firms available for the analysis. This is due to the fact that the nature of the ranking by company size means that this dropping out and re-entering is more frequent for the bottom 50% that are closer to the drop-out threshold.

However, I do not see any reason why companies that are just entering the Top 50 ranking market should grow faster in the year prior to their entry compared with companies in the Bottom 50% of this ranking that have been there the year before. I would expect the growth of companies that are in this ranking to be larger than that of companies outside of it due to the added visibility and publicity brought to these companies through their very position in ranking.

Following the assumption that the companies for which growth information is available represent the overall performance of the companies in these rankings, I find that revenue growth in the MfT companies (IP Core) and the corresponding product market companies (Fabless) are comparable with neither market exhibiting systematically higher growth or higher variance of revenues, meaning I fail to reject the null hypothesis.

I additionally identify that both markets exhibit stronger percentage-based revenue growth for larger companies than for smaller companies. Since I am not able to

distinguish organic from non-organic growth, an increase in merger and acquisition activities of the large players that would, in the absence of exits of large players from the rankings, lead to an increasing market concentration over time may drive these results.[17] From a theoretical point of view, it is interesting that companies dealing in technology for which the one-time licensing fee forms a significant part of the revenue generated do not suffer from stronger fluctuation in revenue than product companies that are not subject to this peculiarity. These findings support my interview-based evidence that companies actively aim to stretch the revenue generation over time, either by charging royalties or by spreading the payments of the licensing fees across several milestones in the development process (which also is in the interest of the buyer of the IP Core since it helps align incentives of IP Core seller and buyer during the integration). I therefore conclude that based on my observation, technology providers are not subject to a significantly higher detrimental revenue variance compared with product companies.

4.4 Startup analysis

The final element of the market for IP Cores that I want to highlight is the number of new startups to the market since my focus on the Top 50 ranking leaves a potentially large blind spot regarding a possibly vibrant ecosystem of small startup firms. To address this question, I again use a proprietary dataset of Gartner on the number of private companies operating in the semiconductor industry (Gartner, 2015b). Unfortunately, this dataset has two key drawbacks that I cannot negate:

1) The dataset covers the entire semiconductor industry and does not have an identifier allowing distinction of IP Core companies, Fabless companies, or any of the various other company types active in this industry, which makes this a necessarily blunt instrument to reach conclusions on the IP Core industry.

2) The database contains only companies that were active and private at the time of the report. I was only able to obtain the 2015 version of the *Market Insight: Private Semiconductor Vendors and Startups Report* (Gartner, 2015b), leading to a large selection bias regarding survival and firms going public, meaning that both the worst and best performing companies of past years would no longer be part of this dataset. The further I

[17] This theory is anecdotally supported by the large number of acquisitions by the three largest providers of IP Cores, ARM, Synopsys, and Imagination Technologies, who have acquired 9, 29, and 3 companies, respectively, between 2004 and 2016 according to Crunchbase.com (2016a, 2016b, 2016c). The exceptionally high number of acquisitions by Synopsys needs to be considered against the backdrop of it being an EDA provider for which acquisitions are quite frequent (see, e.g., Henkel et al., 2015).

look into the past, the fewer firms I expect to see due to these two drawbacks worsening over the lifetime of a firm.

Despite these two serious drawbacks of the data, it nonetheless reveals trends. A clustering of firms still operating today by five-year vintage reveals that the largest share of companies were started in 2005-2009, as shown in Figure 17 (see Appendix A 7 for information on regional shares over time). The lower number of the earlier vintage private companies still in existence is no surprise, however the decreasing number of private companies founded in the period 2010-2014 is. One interesting regional trend is the decreasing share of companies founded in the Americas over the years, from 60% in the 1995-1999 window to 40% in the 2010-2014 window. This reduction contrasts with the share of Asian startups increasing in the same time window from 18% to 37%, Europe staying more or less stable from 18% to 23%, and Oceania not playing any significant role.

Over the entire time horizon, the most frequent country of origin by far is the United States, accounting for the founding of 47% of private companies. Surprisingly, the second largest contributor is the United Kingdom at 7% followed by China and India at 5% each.

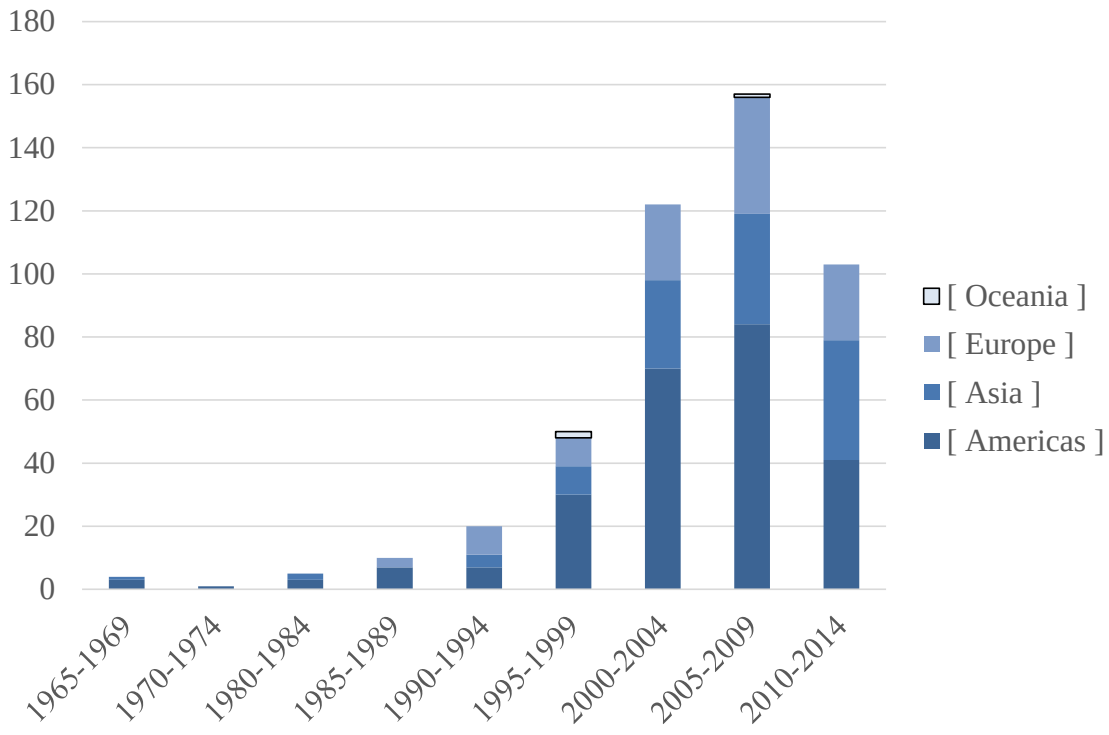


Figure 17: Number of private firms still active in 2015 per region and 5-year-window 1965 - 2014; Data: Gartner 2015b

Zooming into the time around the peak of company inceptions reveals that the highest number of companies contained in the dataset (and again, this may deviate substantially from the actual number of companies founded in a given year due to death or going public of companies in the meantime) originated in the year 2005. Ever since, with the exception of 2010, the number of companies per vintage has followed a downward trend reaching a dramatic low at just four companies in 2014 (see Figure 18).

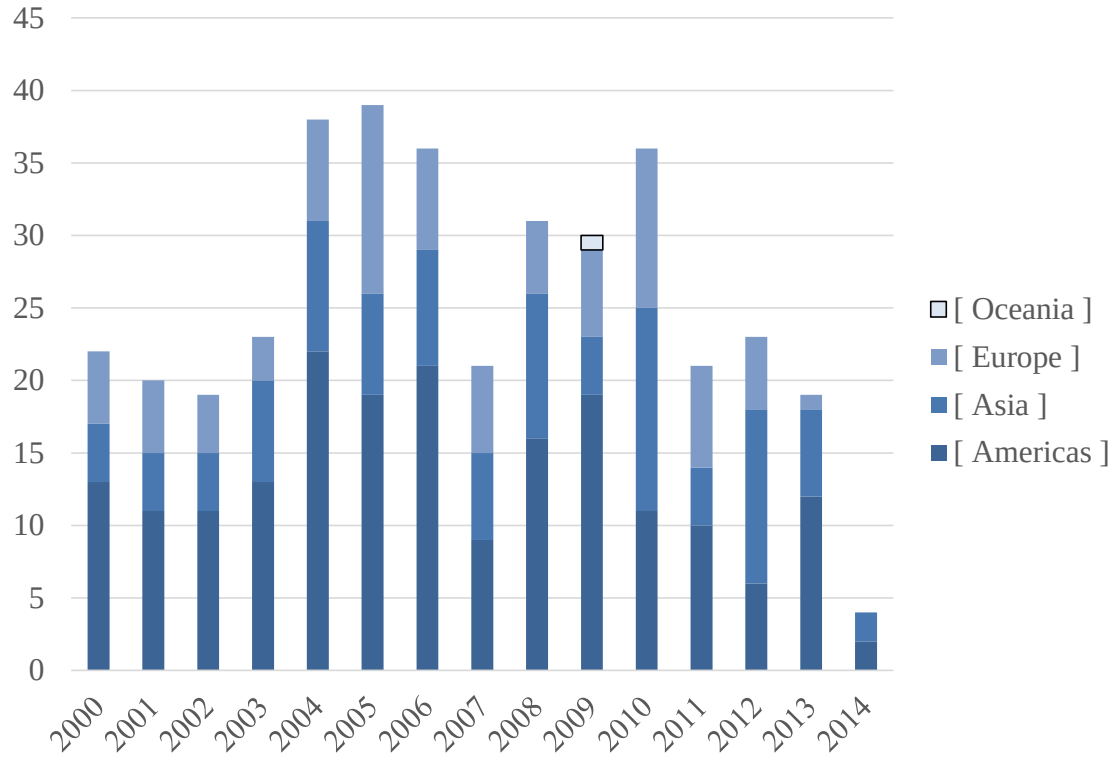


Figure 18: Number of private firms still active in 2015 per region and year 2000 - 2014; Data: Gartner 2015b

While the 50% share of IP Core companies in 2014 is high (two IP Core companies, one design services company [which is basically a contractor that supports the development of a chip], and one company that focuses on sensor development) the low total number indicates that the attractiveness of entering both the semiconductor market and the market for IP Cores has dramatically decreased.

While this data is biased—old companies may have encountered bankruptcy or gone public, and discovery of young companies may yet to happen—the downward trend of the recent vintages is nonetheless remarkable. Possible explanations provided in the report include “the market has matured, and as chip complexity becomes denser, the costs have risen and the ROI has not been as great as in earlier years” (Gartner, 2015b, p. 38), as well as “high production costs” (Gartner, 2015b), which match the evidence from my

interviews including "*There are not a lot small IP companies getting in the market these days, because the barrier to entry in terms of the expectation of quality is so high and the complexity of IP is getting so high*" (Quote interviewee K) and "*if you want to be successful in the IP business, you really have to find a corner of the market, where nobody else is playing. I think that is incredibly difficult these days*" (Quote interviewee G).

4.5 Patenting success

In the course of the analysis of patenting behavior, further detailed in Chapter 0, I also took a look at the share of patent applications across the years 1995–2014 that were ultimately granted due to the high impact of patent ownership on the success of individual companies and by extension to the stability of the market as a whole.

The realization that some companies filed much higher numbers of patents relative to their R&D investments triggered this analysis. One company, Qualcomm, especially stood out by filing for 43% of the patents of the Fabless firms in the scope of this analysis (see Section 3.3.3 for a detailed discussion) despite only investing around 30% of total R&D spending. Considering that Qualcomm is also quite active in directly licensing its patent portfolio,[18] one assumption is that Qualcomm files more aggressively than other companies since it generates money directly from patents rather than only through products. This is an effect that I was hoping to observe in a lower share of patents granted (following the assumption that a higher incentive to patent will, at the margin, result in patents of lower success probability being filed and therefore a higher share of patent applications being rejected by the patent evaluators). I cannot distinguish between patents that failed to be granted and those that are still in the process of negotiations between applicant and patent examiner. Therefore, I additionally compute the share of patents that were filed in 2012 or later as a proxy for the share of patents filed across all years that possibly were not rejected but rather are still in the process (see Section 3.3.3 for a discussion of the disclosure period of up to 18 months). I chose the year 2011 as the cut-off based on an analysis of the overall grant rates per vintage of patents. Figure 19 shows that while the grant rate decreases steadily over time, as of 2012 the curve displays a distinct kink downward for both Fabless and IP Core companies.

[18] This is particularly the case in the context of communication standards such as long-term evolution (LTE) (with a focus on standard-essential patents).

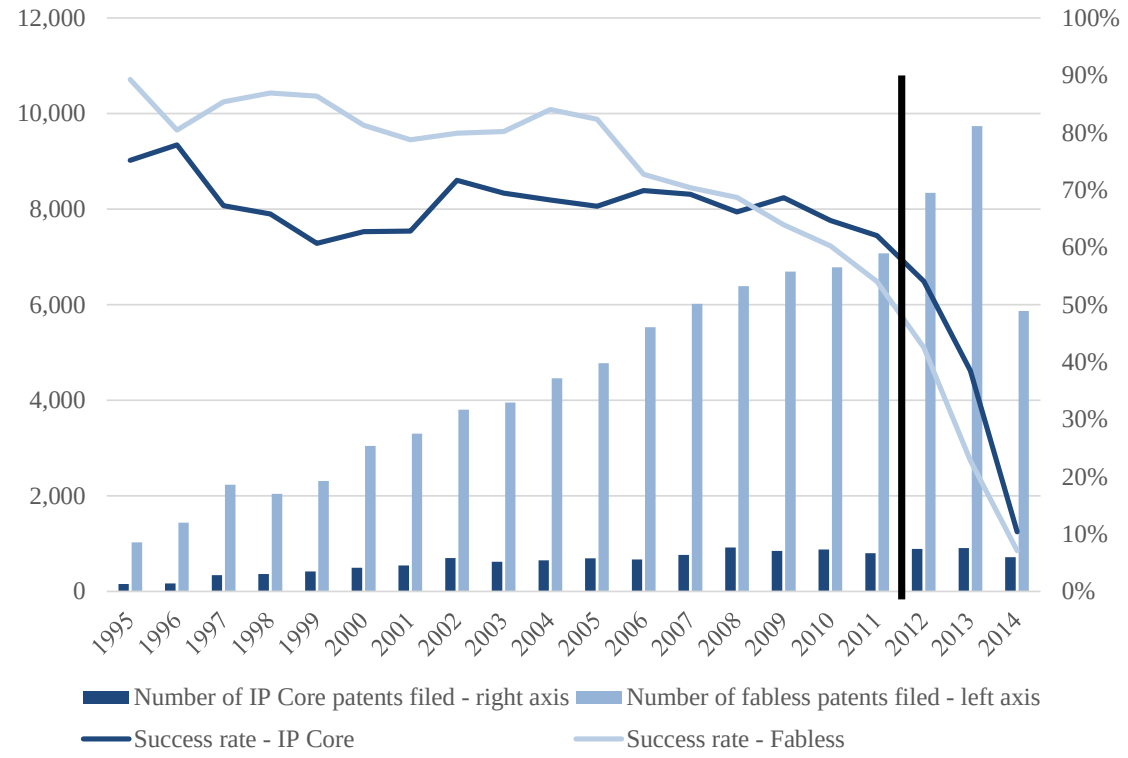


Figure 19: Patent grant rates by vintage; Data: Patstat (2015)

When charting the share of patents granted (as of October 2015, the retrieval date of the patenting data) over the share of patents possibly still in process of negotiation, a rather diverse picture appears (see Figure 20).[19]

[19] Only companies that had applied for at least 20 patents in the years 1995–2014 were included for the graphical representation in Figure 20. See Appendix A 8 for a full table of all companies that had filed for patents in the United States.

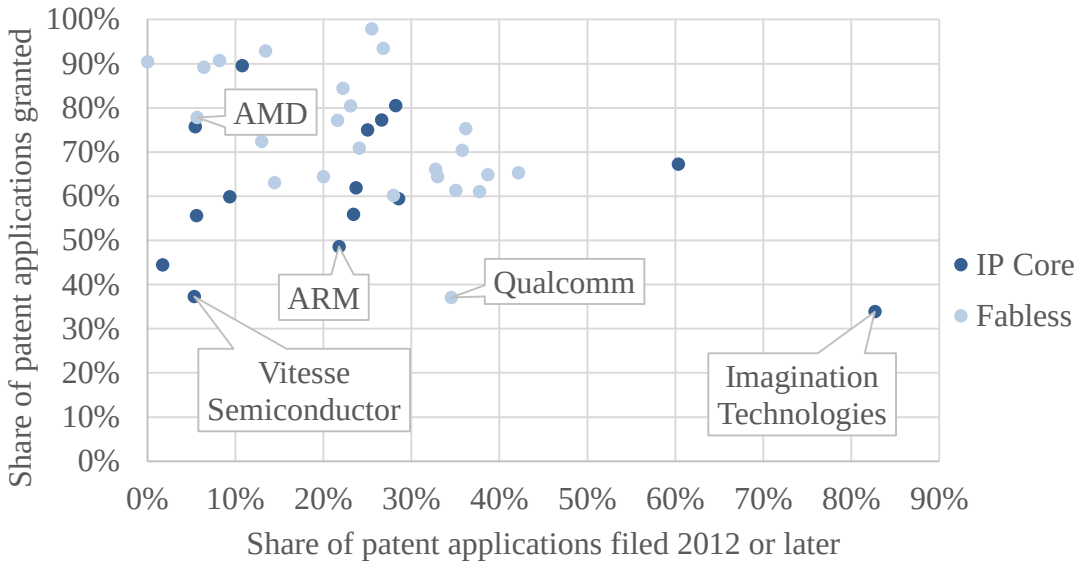


Figure 20: Share of patents granted over share of recently filed patents; Data: Patstat (2015)

Remarkably, the two companies with the most patents filed, Qualcomm for Fabless and ARM for IP Core, have low success rates considering the share of recently filed patents, which is in line with the originally stated assumption that these large companies may file patents with lower chances of success for strategic reasons. This factor appears to more than offset the advantage of having a professional patenting office that should increase their odds of successfully filing a patent (Hall and Ziedonis, 2001) compared with the smaller companies.

The second largest company, AMD, has quite a high rate of success that can at least partially be attributable to the fact that it has few patents that are still in the process. This is in contrast to Imagination Technologies that has quite a low grant rate, which in turn may be due to a high share of patents that could still be in the process. The IP Core company on the bottom left side of Figure 20, Vitesse Semiconductor, has filed only 94 patents compared with ARM's 4,349 and could be a result of less experience.[20]

My finding of an exceptionally low success rate at Qualcomm of 39%—20 percentage points less than the second lowest Fabless operator without an exceptional high share of recent patents (see Appendix A 4 for a detailed table of all IP Core and Fabless companies in scope)—is in line with the interpretation that Qualcomm files patents more aggressively than other providers due to the nature of its business model of generating revenue by actively licensing its patents. However, this is not proof since the

[20] Microsemi acquired Vitesse Semiconductors in April 2015.

patenting success is subject to many different drivers of which the intention to commercialize patents is only one. This, in turn, implies that any patent analysis would have to account for possible differences in the patenting behavior of this impactful company by introducing a dummy variable to avoid distorting the overall results.

4.6 Provider types

During interviews with senior managers of IP Core sellers and buyers, I was able to distinguish three provider types of IP Cores: 1) the pure-play sellers, 2) the complementary sellers, and 3) the combined IP Core and chip sellers. I describe each of these distinct types based on interviewee feedback and distinguish the respective product portfolios. Understanding the respective underlying business model is key to understanding why, for example, EDA tool providers primarily provide standards-based IP Cores, and why ARM is so successful in selling its CPUs.

Type A: Business model built around creation and monetization of IP Cores

This segment subsumes all dedicated IP Core providers that do not create own chips but rather develop partial layouts and trade with these. In short, these are the companies that generate revenue primarily through development and licensing of their IP Cores (e.g., ARM, CEVA). The technology provided by these companies ranges from high-end CPUs selling for millions of dollars in upfront licensing fees and significant royalties, to small-scale video-codec modules with four to five digit licensing fees and no royalty payments. Companies engaged in these segments "*are really focused on a niche. They focus on one specific feature, or function, or even CPU like the ARM architecture*" (Quote interviewee W). They enhance their offering by parameterizing their IP Cores allowing the customer to adapt the core to its specific requirements and by providing adjacent services such as integration support and bespoke software facilitating the design, as described by one manager, "*we also help with the engineering work in addition to the reference manual and the standardized test to make sure that their product is compliant with our architecture*" (Quote interviewee E). This company type also primarily aims to provide soft cores since the flexibility inherent in this provision format increases the size of the addressable market due to being portable to any foundry and technology node and being highly integrable with the buyer's own designs. This flexibility, however, also mandates that IP Core providers work closely with EDA tool companies to ensure that the integration of their IP Cores into the overall SoC work smoothly. As expressed by one IP Core manager, "*Our design services are complementary to our core, which is IP licensing.*

In certain cases we actually partner with EDA companies. We have, for example, a (name confidential) *design service kit […]. Those service kits will help a customer get to market faster or optimize for a specific performance or power or area target*" (Quote interviewee E).

Regarding the type of IP Cores provided by the dedicated pure-play IP Core sellers I find that one quite successful strategy is to focus on Cores that are reliant on ecosystems or linked to software stacks in order to create customer stickiness that ensures long-term survival. This is reinforced by an IP Core manager who stated that "*our main driver comes from the handheld market, which is naturally a really sticky space, because you have decades of legacy software*" (Quote interviewee Z).

Type B: Business model focused on a closely related, complementary good [diagonal integration] with provision of IP Cores at a low or even zero price

Both foundries and EDA tool providers earn their primary revenues with the sale of their core-product (EDA tool or ordered wafers) and use the provision of IP Cores to enhance customer value or provide an enhanced solution to the customer (e.g., TSMC, Synopsys) making them both active developers of IP Cores. Foundries focus their development offers on basic building blocks required to translate the Soft Cores into technology-specific Hard Cores. A foundry offers the basic versions of these IP Cores for free since this acts as a facilitator in getting customers to purchase wafer capacity, the clear priority for foundries. A manager at a foundry described this as "*IP Cores help a lot to enable new SoC design wins and tape-outs at foundry's processes. […] However, the commercial value of IP core licensing income is not foundry's business focus*" (Quote interviewee M). They may choose to sell more advanced versions of these IP Cores to their customers if required, but will mostly leave the field of developing advanced IP Cores to certified, partner companies of Type A that are able to pass the development cost on to the customers through dedicated licensing contracts. I have received anecdotal evidence that some foundries will scan their customers' layouts and collect royalties for any proprietary designs of third-party IP Core companies contained therein addressing the issue of monitoring the number of chips produced. According to interviewee M, "*If it's a process based IP, GDS delivered IP [i.e., delivered as a hard core], like mixed-signal IP or a standard cell library, they will be scanned-out in the foundry when the customer tapes out. They will have some information.*"

EDA tool companies operate somewhere between the Type A and the foundry models detailed above. They sell their IP Cores and the IP Core segment is treated as a

profit center (compared with the cost center approach of foundries), yet the close tie-in with the EDA tool development creates synergies for both business units. There are primarily three sources for synergies. On the one hand, the IP Core business unit benefits by being able to use the latest versions of the EDA tools, sometimes even before these are sold in the open market and at significantly lower to no cost as outlined by one EDA manager who stated that they, "*don't charge for EDA tools from cross chargers [i.e. internal users]. So there is a cost advantage of having the IP division within the larger EDA company*" (Quote Interviewee K) and can use the contact to foundries to ensure the ideal modelling of IP Cores to the specific processing technology and the various contact points to customers of the EDA tools to pitch their IP Cores. That same manager stated, "*In general, we want to provide cores that go onto a very wide range of chips, because it takes advantage of some our core strengths as a company. Our channel, our reach, and our distribution*" (Quote interviewee K). The EDA tool business unit benefits from having a sizable number of IP Core developers who can beta test the latest versions of the EDA tool and provide valuable feedback on required functionality and bugs during the development process as the EDA manager verified by stating, "*We are a very large user of the tools and can provide some very strong and focused feedback that improves the overall tools significantly*" (Quote interviewee K). Ultimately, both business units benefit from being able to provide an integrated solution to customers' needs by providing the two complementary facets of software to facilitate the integration of the SoC and building blocks that work smoothly with the EDA software to fill the gaps in the SoC design. The same manager sums up this aspect with, "*If you think about EDA tools: What is their primary purpose? Their primary purpose is to take ideas at various levels of abstraction and implement them quickly […]. If you think about it from that perspective, IP is almost, in some ways, like the ultimate tool, because instead of having to translate it through abstraction layers, it's already pre-existing*" (Quote interviewee K).

I find that EDA tool providers offer a high share of standards-based interface IP Cores that are typically provided as Hard Cores and will focus on the mass market as summarized by one independent expert stating that "*if you look at Synopsys, which is market leader in this IP segment with more than 50% market share - Synopsys is providing the solution for the mainstream market. If you look at the interface IP market it is based on standards, protocol standards*" (Quote interviewee V). This focus on non-differentiating IP also enables EDA companies to avoid being seen as competition by the Type A companies that are customers of their EDA tools, thus avoiding a possible conflict

of interest as expressed by the EDA executive who stated "*Think about your phone. It has a USB port on it. Do you ever buy your USB phone, because it has a USB port on it? Of course you don't! […] It's a classic example of something that is necessary and required, but doesn't differentiate the product. So our customers are saying: '[…] We can design it ourselves using Synopsys tools or we can just buy the whole thing from Synopsys and implement it in our chips. Our customers don't view, in any meaningful way, us competing with them'* " (Quote interviewee K). During my interviews, I heard that this was due to the fact that EDA companies are well positioned to capture this market since they are able to quickly implement new standards due to their intricate knowledge of the EDA tools, as described by the EDA executive "*as a leading EDA tool supplier we use our best in class tools to design our IP*" (Quote interviewee K), and are able to fund the expensive large teams with the required high level of expertise over extended periods of time required to develop these Cores. Finally, EDA tool companies are able to bundle their offering of EDA tools and IP Core into attractive packages as described by one interviewee who stated, "*Synopsys defines the price in a bundle with tools, the licenses, the service level agreements. […] Of course there is a list price for an IP Core, but that is somehow factored into the bundle price*." (Quote interviewee S, translated), all of which combined enabled "*Synopsys, for example, in the area of USB achieve a market share of 80-90%*" (Quote interviewee J, translated).

Type C: Business model that involves both sale of final products, as well as IP

This provider type incorporates both Fabless providers and IDMs (e.g., Intel, Infineon). In the semiconductor industry, the special circumstances of high price differences between physical products and IP, the competitive non-cooperative mindset, and globally integrated markets lead to a strong concern about cannibalization as summarized by an independent expert "*there is more 'protectionism around designs.' A belief that I'm going to enable a competitor, therefore I'm not going to make it available. Particularly given the relative value I get for it compared to what I would get if I had made the winning tool and try to get the market share*" (Quote interviewee AA). IDMs face the additional risk of owning a manufacturing site that rapidly depreciates, so that any lost chip sales due to out-licensing of the technology will additionally reduce utilization of the manufacturing plant with a corresponding bottom-line impact due to the high fixed-cost share of these fabs. Therefore, out licensing by these providers is rare and usually triggered by specific end-customer requests to do so (usually in order to enable a dual-source strategy based on one technology).

A final market participant type of a somewhat different nature is market places focused on matching supply and demand of IP Cores.

The market place providers do not add to the amount of IP but have a very relevant role of matching supply and demand, especially for smaller IP Core providers that are not present in chip designer's minds (e.g., IPExtreme, Design&Reuse).

4.7 Limitations of research

It is difficult to derive causal statements based on the analysis presented in Chapter 0. While I can observe the outcome, I can only speculate with regard to the underlying mechanisms leading to these observations. Even where I have reason to speculate on the underlying mechanisms I can only really speak of correlation due to the manifold opportunities of reverse-causality and omitted variables that could drive the results.

More concretely, the analysis suffers from the non-observability of the companies outside the Top 50 rankings for IP Core and Fabless, yet I believe that since both sets of analysis are subject to the same observation limitations and exhibit similar characteristics in terms of stability of the rankings (see Figure 9), in terms of new revenue entering the rankings each year (see Figure 8), and in terms of revenue growth for the individual firms contained in the rankings (both large and small – see Figure 14, Figure 15 and Figure 16) that I do not suffer from significant systematic errors when comparing the two datasets. My analysis only captures the largest companies that are more likely to be able to both receive royalties (many customers prefer not to pay royalties since they prefer not to disclose the produced volume of products and are more willing to face a one-off charge as part of the R&D budget than a continuous variable cost impacting the profitability of the product) and to be able to manage the effort to monitor the buyers of the IP Cores in order to ensure fair payments. Therefore, take the findings with caution when thinking of the various small IP Core providers that may be subject to strong fluctuations of revenue (as I have heard anecdotally during the interviews).

The startup analysis is probably the one where it is most difficult to derive specific insights for the market for IP Cores. However, since it does reveal a strong downward trend for all submarkets of the semiconductor industry and lines up with the findings from the interviews, I consider it worthwhile while being cautious in its interpretation.

4.8 Discussion of Market and Provider Performance

Summing up I find that the relative revenue development (also not in absolute terms) over time and the composition of the Top 50 ranking over the observation period (both in terms of share of revenue of companies new to the ranking per year and the longevity of companies in the ranking) is comparable to that of the Fabless market. This makes it possible to state that the market for IP Cores as a whole is of comparable stability to the adjacent product market.

The one major difference I encounter is the dramatic difference in concentration with the Fabless industry being unconcentrated and the market for IP Cores being close to highly concentrated, which is to a significant degree the result of the success of ARM dominating the market for IP Cores based on their strong performance in the largest segment of microprocessors (see Appendix A 5, Figure 33).

On an individual provider level, I find through an analysis of the revenue variance that the level of fluctuation is comparable between Fabless and IP Core companies, further substantiating the claim of comparable stability at the individual firm level. Additionally, both markets feature stronger growth among the Top 25 of the Top 50 ranking than the Bottom 25, revealing winner takes all in both Fabless and IP Core markets due to the already larger firms growing stronger in relative terms. The reduced number of new entrants to the semiconductor industry since 2005 due to high quality expectations and lack of unoccupied niches reinforces this finding.

With regard to patenting success, an area crucial for achieving long-term success on an individual firm level, my analysis highlights that while both IP Core and Fabless companies overall have a comparable patent grant rate of 61% for both markets, the largest company has a significantly lower grant rate that cannot be solely explained by patents that are still in the process. This, therefore, raises the possibility that these large companies file strategically for patents that have a lower chance of success than some of their smaller counterparts.

Finally the analysis of the archetype reveals that the extraordinary success of ARM is supported by the ability to create a lock-in through the software stack that is specialized to the ARM CPUs, and that the reason EDA tool providers are quite successful in the difficult setting of standards-based IPs is that internal synergies can be realized between the EDA tool and the IP Core division.

In the next chapter, using the results of my interviews, I analyze the reasons why

the market for IP Cores is so well-functioning despite the evidence toward sources of systematic non-viability for MfT (see Chapter 1).

5 The role of Ability-Related Trust in an Environment of Technological Risk

As described in the Introduction and in Section 2.3, the majority of the literature on risk involved in strategic alliances and that on technology transactions has focused on the possibility of future opportunistic behavior of the other party and the role of trust in overcoming this risk. Starting with a systematic evaluation of sources of non-viability of MfT raised in the prior literature (5.1), I identify an alternative source of risk that is of importance to the market for IP Cores, that is the technological risk inherent in the technology being traded (5.2), which has implications for the nature of the trust required to overcome this risk (5.3). I subsequently address the question of the salience of the two types of risk to discern the importance of the newly identified risk compared with the established risk (5.4) and follow up with a discussion of the transaction costs involved in the market for IP Cores to address the question of viability of MfT from a second perspective (5.5). I conclude this chapter with a discussion of possible limitations of this analysis (5.6) before summarizing the key findings (5.7).

5.1 Sources of non-viability

During their discussion of the current state of the literature on MfT, Arora and Gambardella (2010) investigate potential instabilities of these markets and identify four key issues that were frequently mentioned as key concerns during my interviews: **The inability of downstream buyers of technology to differentiate** when technology is made available to all competing market participants; the **'Not Invented Here' (NIH) syndrome,** which excludes viable external technology from consideration; the **loss of technology as a strategic asset** to providers of technology; and, finally, the issues around **pricing** IP. Additionally, based on the market design literature of Roth (2007; 2008), Agrawal et al. (2014) identified the factors of **market thickness** and **market congestion** (the element of market safety[21] is subsumed in the loss of technology as a strategic asset factor). In the next section, I discuss the applicability of these six concerns, based on evidence garnered through interviews, as to how these instabilities are dealt with in the market for IP Cores.

Based on their prior research Arora and Gambardella (2010) argue that MfT will

[21] Operationalized by Agrawal et al. (2014, p. 5) as the share of IP that is "protectable by patents, trade secrets…"

typically make their technologies available to all market participants of a downstream market (in order to maximize the number of licensees and rents) and thereby remove the 'inimitable' attribute of the VRIN categorization used within the resource-based view of the firm (Barney, 1991; Conner and Prahalad, 1996). They argue that this will remove the **ability of buyers to differentiate** and therefore force them into smaller niches, which ultimately reduces the customer base of MfT. While this point may be applicable for discrete technologies where a technology being traded subsumes the entire product, the rationale of the argumentation needs to be questioned in general for the context of complex technologies (which include IP Cores) since upstream markets could simply be used to provide parts of the product considered to be non-differentiating while the downstream companies focus their resources on complementary yet differentiating parts of the final product. This is exactly what I find in the market for IP Cores where only those technologies are provided as IP Cores, which are mutual to many customers and the downstream buyers of IP Cores, differentiate on the elements of technology that are not provided by MfT. Vice versa, IP Core sellers are aware of this limitation and therefore do not enter certain areas where customers will not buy due to the need for differentiation. Hence, an equilibrium has been established that caters to the need for spreading development cost for non-differentiating parts while allowing for differentiation of the buyer of IP Cores, a tendency reinforced by one buyer of IP Cores who stated (regarding the need to differentiate) that, "*When you say 'this is my core competency and very important' and you find 4,5,10 others who say 'look, you could buy this directly off the shelf from me' then you need to ask yourself whether this core competency is sustainable*" (Quote interviewee B follow up– translated). There are two major types of IP Cores that are considered to be non-differentiating: the IP is really commodity and no customer will be willing to fund the redevelopment since it is not possible to differentiate against competitors based on this IP (this is the case for foundational IP provided by foundries and standards-based IP); or, the IP is difficult to develop and there is a large value to interoperability or stability in the provider (this is the case for CPUs that have a huge dedicated software stack that can simply be adopted free of charge when using the established provider as well as for the latest implementations of interconnect). An option to achieve differentiation compared with competitors' products while relying on IP Cores is the usage of so-called architectural licenses that allow the customer to adapt and optimize the source code and therefore differentiate on the base of an IP Core. One interviewee described this stating, "*You have the option of licensing the architecture,*

which is slightly more expensive, but gives you the opportunity to either differentiate or build a custom solution for a certain application" (Quote interviewee E). Another option for IDMs is to use their proprietary processing technology, which according to one interviewee, was an important source of differentiation for IDMs. To sum up, I found that managers are fully aware of the need to differentiate, and perceive various ways in which differentiation can be achieved despite the use of a (non-differentiating, since generally available) IP Core leading to a fruitful cooperation between IP Core providers and buyers. One interviewee stated that his customers "*are happy when they have somebody who takes some of the workload off their shoulders*" (Quote interviewee H, translated).

Another potential source of non-viability to the market for IP Cores is the so called **Not Invented Here syndrome (NIH).** Especially in the early days of MfT and for providers who have no history of using outside knowledge, this focus on internally developed technology effectively hinders initial growth. The findings of Katz and Allen (1982), whereby the NIH syndrome is dynamic as it increases the longer project teams work together, constitute an additional complication that could spell trouble for both nascent and established MfT. On the topic of NIH, interviewees were evenly split with seven reinforcing that it was a significant obstacle to licensing technology and seven stating that the NIH syndrome could be overcome by convincing through hard facts such as price and development time. NIH was considered to be an ongoing concern by small companies as described by one interviewee who stated, "*Your biggest competitor is always your customer. 'Oh we could do this ourselves'"* (Quote interviewee AB). NIH is even a concern of large companies of IP Cores. As stated by a representative of one of the largest IP Core companies, NIH presents a "*particular obstacle for us. There are instances we have seen where customers want to do their own thing even though we could license an equivalent solution to them. Sometimes it's a pride thing on the part of our customers*" (Quote interviewee G follow up). Several other interviewees, however, found NIH to be manageable, highlighting the key advantages of having a lower price due to development cost spread across several companies combined with earlier availability by resorting to a fully developed external solution compared to commencing in-house development. One reason why the NIH is manageable in the setting of IP Cores could be due to the fact that the syndrome is significantly weaker with suppliers than with competitors (Hussinger and Wastyn, 2015). This effect also adds a possible explanation besides the concern for cannibalization of why so few buyers of IP Cores try to sell their internally developed IP Cores to their competitors.

One of the most frequent issues cited in connection with supplying technology is the risk of losing control of the technology during negotiation, a concern summed up in the formulation of Arrow's information paradox (1962). This risk was extended by the interpretation that the very creation of a MfT renders the technology non-strategic to the firms (Dierickx and Cool, 1989) in the sense that it can no longer be used to out-compete competitors even in the presence of patent protection since competitors are able to build upon the now disclosed technology to the same degree as its creator (Arora and Gambardella, 2010). I term these combined factors the **loss of technology as a strategic asset**. In the market for IP Cores, I found that while six interviewees stressed that the above concerns regarding disclosure were applicable, 14 interviewees perceived them to be addressable through acquiring patent protection, encrypting the IP Cores, and signing corresponding contracts such as NDAs that were generally well respected throughout the industry up to the point that "*it's all a contractual mechanism backed by the ability to do audits*" (Quote interviewee K). The reason contracts work so well in this industry is that the end-customers are quite conscious of the risk of being drawn into IP litigation when one IP Core provider steals IP from another provider because "*the risk is too large because it (IP theft) is traceable. The last thing you want to do is steal. Steal for half a million and then pay billions – no chance. […] All sides are basically forced to be honest because the end-customer, for whom everything is at stake, forces them*" (Quote interviewee S, translated). This risk to end-customers is quite real as described by another interviewee who shed light on who is being sued in case of IP infringement by stating, "*They go where the money is. Sometimes they even sue our customers or both our customers and us, but rarely they sue an IP vendor itself*" (Quote interviewee C). This risk is further exacerbated by the limited effectiveness of indemnification clauses, as highlighted by another interviewee, "*indemnification is probably not worth a great deal, because you'll bankrupt the company anyway by taking them to court.*" (Quote interviewee T). On top of the utilization of patents and the effectiveness of the contractual protection, a large number of providers rely on an additional level of technological protection that is enabled through the providers of the software tools used for designing chips (EDA tools). Providers of IP Cores are able to encrypt their Cores so that only the EDA tool can decrypt it in the process of integrating the IP Core into the overall SoC. This additional protection is broadly pursued by providers of IP Cores, especially when dealing with new customers and it provides an alternative solution to the Arrow information paradox (1962) by enabling the evaluation of the technology in the specific context of the SoC without needing to disclose

the information at hand—a feature that is a function of IP Cores being a market for current, highly codified technology rather than abstract future technology. Finally, there is the perception that some markets are too uncertain in terms of IPR protection. One interviewee stated that he had partner companies that "*generally are very reluctant to sell IP to China at all. Simply because they believe that there is no possibility to protect it as soon as you sell to China. Regardless of copyright, encrypted netlists and whatever*" (Quote interviewee D, translated). But apart from these extreme examples, the prevalent mix of patents for novel technologies and widespread use of well-respected contracts and encryption appears to have stabilized the issue around loss of IP.

The final and most contentious mechanism with potential for causing non-viability is the setting of the **price**. In the literature, this topic has received considerable attention in the context of future technologies where cost cannot be taken as basis of pricing and where valuation is hindered by high amounts of information asymmetry (Arora and Gambardella, 2010). However, I find that even in the context of a current technology where cost is a possible basis for pricing, and with comparably low amounts of information asymmetry due to codification and possibility to test/evaluate the technology, the price level is volatile and was mentioned by 13 interviewees as a source of non-viability. The non-viability in this market for current technology stems from a number of factors. First, IP Cores are fully developed by the time they hit the market and replication costs in terms of filling in the licensing contract are extremely low as the technology is fully codified and can be sent as a data file ready for implementation, leading to a scenario where each additional sale is almost purely profit to the bottom line. This implies that unlike with physical products there is no real lower threshold to the prices competitors may set as "*there is a certain point where you can't, you can't sell a chip, below a certain point because you start shipping money with the chip. But with […] IP, […] you do an FTP-transfer*" (Quote interviewee T). Secondly, the barriers to entry from a skill perspective are fairly low as described by one interviewee who stated, "*entering the market is easy. Any unemployed engineer and a couple of friends with knowledge in a particular application space […] can start an IP company. Little more capital is needed than what is required to pay salaries*" (Quote interviewee L). In combination with a volatile semiconductor industry that regularly sheds highly skilled developers, this accounts for a large number of small companies that continuously enter into and exit from the market, each of which is flexible in terms of pricing, to either get a foothold in the market or to extract final rents prior to leaving. This leads to the situation described by an

interviewee where "*the price of an IP is extremely flexible, in the market. If it is in competition, so if you're talking about standards and we specialize in standards, then, companies will come in and, yeah, the price can be extremely flexible you can see price-reduction 50 to 60% during a negotiation*" (Quote interviewee T). Finally, when using cost-based pricing, the price to be charged fully depends on the expectation of how many licensees a particular technology will acquire, a decision that is strongly endogenous and further works to drive prices down in the sense of Bertrand competition. However, not all interviewees were so critical with respect to pricing, especially the largest ASIC providers that were considered to be able to achieve sustainable prices as described by one interviewee, "*with AISCs it is thank God the case that they know what they have to pay in the end. [...] They don't look only at the money but for the Americans time to delivery (i.e., market window) is important, too*" (Quote interviewee H, translated). Another interviewee, referring specifically to ARM, added "*I think they price very well. Their revenues keep going, their margins are phenomenal, they are a $2 bn dollar company, with a $20 bn market cap. Can you get any more? I'm sure they can, but I think they have done a very nice job of balancing demand and supply to keep that going*" (Quote interviewee AF). Summing up, the pricing of IP is one of the most difficult issues faced by both small and large companies in the market for IP Cores. It could harbor the seeds of a price war between rivalling IP Core providers competing for the same customers; however, it does not seem to negatively affect all providers and the largest ASIC providers seem to be exempt.

Switching the focus to the factors identified by Agrawal et al. (2014), I find that the **market thickness** is no longer an issue since for most IP Cores there are multiple broadly equivalent suppliers available, while sellers of IP Cores have multiple customers whom they are able to sell to. This is exemplified by the multitude of competing offerings listed on the marketplace of Design&Reuse (see Section 3.3.6) that contained offerings of 477 providers across all IP Core types; for the subsection of 'Processor and Microcontroller IP Cores' alone it listed 27 Coprocessors, 48 CPUs, 250 Digital Signaling Processors, 148 Microcontrollers, and 161 Microprocessors. One of the interviewees confirmed this finding by answering that the number of providers of analog digital converters (a standard part required in most SoCs) was "*I would say 20, at least*" (Quote interviewee B, translated) and another interviewee (interviewee A) likened it to the automotive industry in terms of substitutability. The lack of thickness therefore likely was a major obstacle to the creation of the market for IP Cores (see discussion of the NIH factor), but is no longer

a major issue in the steady state of the market. Looking into the future, this factor will again gain some relevance due to the increasing consolidation of the demand side and the corresponding increase in bargaining power of the customers of IP Cores combined with a reduction of the number of companies who pay one-time licensing fees. This was explained by one interviewee who stated, "*because now we have fewer customers to negotiate with and fewer potential licensing bills. We need to try to charge you a higher price. So it is general consolidation of the existing semiconductor companies […] that results in fewer customers.*" (Quote interviewee L).

The second factor of Agrawal et al. (2014), **market congestion**, does not apply to technology licensing outside of exclusive licenses. The idea behind congestion is that in order for market mechanisms to function, potential buyers need sufficient time to evaluate the quality of the product on offer while simultaneously being able to conclude their evaluation in a timely manner to allow the market to clear. The examples analyzed by Roth (2007; 2008) include the market for kidneys and that for medical students, where the competitive nature of the bidding led to increasingly early offers effectively undermining the ability to evaluate. While a similar situation can happen in the case of exclusive licenses with multiple bidders rushing to ensure exclusive access to a potentially superior technology, in the case of non-exclusive licenses such a rush is not to be expected. Rather, the opposite is true as one interviewee described the process of introducing a new IP Core to the market, "*I'm dealing with that right now with a new product that we have. […] We have three customers with early access and nobody wants to be first! There is always one person that says: 'I really need this, maybe I WILL go first.' You have to figure out, who that is. It is all about pain, finding the pain.*" (Quote interviewee AB).

Summing up, I found that the **need for differentiation**, the **NIH syndrome**, the **loss of technology as a strategic asset**, **market thickness,** and **market congestion** while all being relevant for the MfT at hand, were well addressed and a steady state had developed affording the technology providers a stable position in the value chain. There is one source of non-viability that was most prominent, yet was not able to be addressed in a straightforward fashion. This is the setting of prices in the market for IP Cores since all the ingredients for aggressive competition based on price are present but do not appear to materialize for the large ASIC providers. The reasons for this appear in the next section.

5.2 Risk of sourcing technology

Based on feedback from interviewees, prices are stable due to the fact that prices are not the primary criteria based upon which IP Cores are selected. The primary concern is the large risk involved.

During the interviews, I encountered the relational aspect of risk that is well and extensively covered in the literature on trust in the marketing field (see Section 2.3) including the risk that the exchange partner, in this case the provider of IP Cores, may choose to behave opportunistically during the exchange and act against the interests of the buyers.

Additionally, I found a second source of risk that was not connected to opportunism but to the inherent uncertainty of the underlying technology—an area highlighted by Arora and Gambardella (2010) as requiring further research. This uncertainty revolves around whether the purchased IP Cores are technically sound and free of violations of third parties' IP rights, absent any opportunism. It focuses on whether the provider of the technology has the ability—beyond the will—to provide a working technology. This dual source of risk is nicely captured in the statement by a founder of a semiconductor company who said "*it was a very painful process in the sense that we didn't just have to convince him about technology, We also had to convince him that we are a decent company to work with*" (Quote interviewee N) and is shown in Figure 21 with the corresponding first- and second-order concepts.

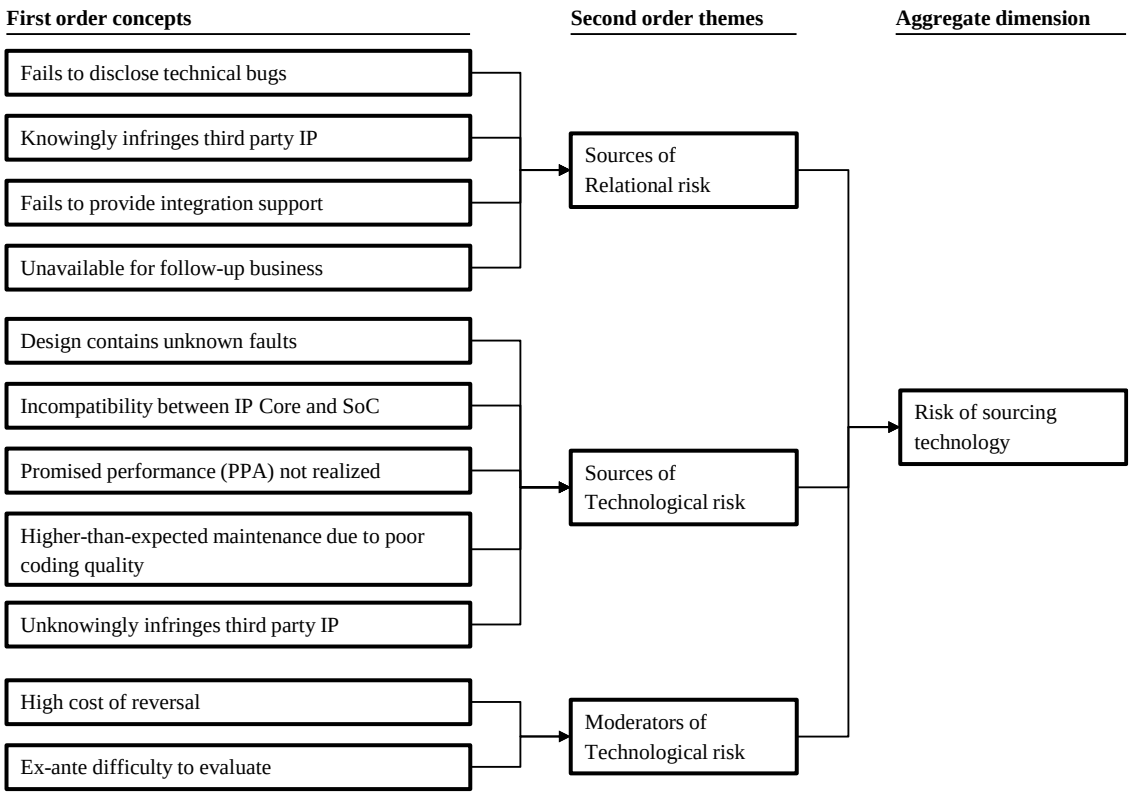


Figure 21: Overview of risk model incorporating relational and technological dimensions of risk

5.2.1 Relational risk

Commencing with the established, relational risk theme, concerns were encountered regarding the technology provider's failure to disclose technical bugs, deliberate IP infringement, failure to provide integration support, and the unavailability for follow-up business.

The size of the risk and the fact that the failure to disclose is a serious concern, is nicely summed up by one interview who stated, "*there are a lot of competitors with incomplete products selling for low prices and giving the entire semiconductor IP business a bad reputation*." (Quote interviewee L). This results in the need for buyers of IP Cores to "*do a lot of verification yourself*" (Quote interviewee L) when sourcing IP that has not yet been proven in the market—a huge waste of resources considering that verification amounts to between 70–80 % of the total design effort (Tuomi, 2009). But the fact that companies would rather take on this effort than just integrate the Cores speaks volumes to the size of risk IP Cores pose.

The issue around infringing third-party IP is of primary concern to the customers of IP Core companies due to the risk described in Section 5.1 regarding IP infringers suing the revenue-strong customers of IP Core companies rather than the provider of the IP Core

to maximize the rent extraction. The awareness of this particular risk is exemplified by a manager responsible for procuring IP Cores of a leading semiconductor manufacturer who stated, "*Small companies always struggle with Legal risk*" (Quote interviewee C) and considered legal challenges as the biggest risk involving small companies in a presentation during a conference of providers of IP Cores.

Failure to provide integration support appears to be one of the primary sources of concern for large companies contracting from small companies. An interviewee who provided the example of the company Evatronix in Poland, the first and best on the market with a USB 3.0 Core, highlights the scale of this concern. He said, "*Intel had them* [Evatronix] *on their Radar but did not touch them. One day after the takeover through Cadence Intel called 'When can we have that IP Core?' The perceived risk of buying from such a small company is just too large*." (Quote interviewee S, translated). He also provided the case where a developer "*broke his ankle and all of a sudden a 300 million USD project was at a stand-still*" (Quote interviewee S, translated) because he was the single provider knowledgeable about an IP Core. The frequency of need of support during the integration is also very high, going so far that some interviewees offered the opinion, "*With the IP you need this (design support), if you don't have that you are not able to use it*" (Quote interviewee U). Other companies are actively addressing this by seeing it as a need to differentiate, as described by another manager, "*I think our support […] clearly differentiates us from the competition*" (Quote interviewee K). Overall, the perception in the market is that the concerns regarding the willingness and ability of small providers to provide significant support in time-critical situations appears to be a major obstacle to their securing business.

Finally, the risk that IP Core providers will disappear and be unavailable for future business is relevant in cases involving a large, dedicated development effort for a certain IP Core (such as the software stack for CPUs described in Section 4.6). This is also true in cases where buyers of IP Cores have long maintenance obligations to their respective customers and also not infrequently, as described by one intermediary, "*There are many people we work with who say 'I earned 500.000 with that thing, I will now stay in Thailand at the beach"*" (Quote interviewee S, translated). In these settings, the longevity concerns regarding small companies are paramount as detailed by a manager active in the procurement of IP Cores for the automotive industry where long support for parts is expected: "*I have to say I always have my doubts when I need to support something for 10 years and then need to rely on a company that has 20 people and was founded 2 years*

ago. I need to ask - can that work? I rather rely on a company that exists for 10 years or has 20 years of track record" (Quote interviewee A, translated). The validity of these considerations can be derived from Figure 9, which shows that after only 8 years almost 60% of IP Core companies in the Top 50 have vanished from the ranking.

Combined, all these issues were concerned with elements where the providers of the IP Cores have the choice and may behave opportunistically to exploit the vulnerability of the buyer of the IP Core. Some facets of these issues were raised in all interviews, which speaks to the relevance of the relational aspect in dealing with technology, also described by Jensen et al. (2015). However, the relational risks only partially cover the risks described by the interviewees and especially fail to explain some of the mitigating actions taken by buyers of IP Cores (which are described in detail in the next section). The uncertainty in the quality of the technology is a significant additional source of risk that has not as yet been discussed in the literature.

5.2.2 Technological risk

The focus on technological risk when deciding to source IP Cores was noted by a board member of a buyer of IP Cores who stated, "*The contract rather comes last and technology comes first, second and third*" (Quote interviewee B follow-up, translated). Considering that the contracts serve primarily as protection against relational risks such as failure to provide integration support, this statement powerfully underlines the primacy of technological risk over relational risk in the market for IP Cores. Further support for this is provided by the concerns among buyers of IP Cores regarding the presence of undiscovered faults in the designs. This was described by the interviewees stressing that "*design quality*" was even more important than "*time-to-market*" (Quote interviewee V). This is remarkable considering that time-to-market is the primary reason for sourcing IP Cores (overview of reasons for sourcing IP Cores is provided at the end of this section in Table 12). The gravity of this concern was additionally highlighted by a representative of a foundry, who stated that they chose not to sublicense IP Cores because, "*If we sell it or sublicense it, we have to bring some liability to the customer. That would be very complicated*" (Quote interviewee M). Another interview source identified the low level of quality control provided by small players as the reason "*why there has been such a massive wave of consolidation across the entire IP industry. It's because all of those guys were small guys […] really weren't fundamentally meeting the need of the semiconductor manufacturers*" (Quote interviewee K) in terms of fault-free delivery of IP Cores. For some buyers of IP Cores this concern goes beyond the initial delivery, having a dynamic

component aimed at the need for "*ongoing functionality*" (Quote interviewee J). Again, this concern is distinguished from the relational risk by the absence of opportunism—providers don't **choose** to deliver poor quality, they are simply **unable** to deliver good quality.

Another concern was that even when the IP Core in itself is working flawlessly, issues frequently arise during the integration of the IP Core with the SoC due to the context-specific nature of the technology. The IP Core will interact with the multitude of remaining SoC components on the computer chip both in terms of data exchanged and physical environment, which can occasionally lead to unforeseen issues as highlighted by interviewees who said, "*any one prototype is unlikely to accurately characterize the results for a customer's usage*" (Quote interviewee L) and "*just because it works in one cell phone it doesn't mean that it will work in the next phone [generation]*" (Quote interviewee S, translated). This context specificity is also the reason why most providers stressed that "*IP Cores always come with support*" (Quote interviewee R, translated) and that if "*you leave them (the customers) alone, chances are there they probably fail with your product and they'll look to go to another direction.*" This need for support during integration also explains why the relational risk of a provider failing to provide integration support is such a serious concern for buyers of IP Cores.

Besides outright faults of the chips, sometimes IP Cores end up not delivering the performance as initially promised. This is partly due to the context specificity described in the paragraph above, but also to limitations of the EDA tools used to design the computer chips—especially when IP Cores have not yet been realized in silicon and only exist as simulations. One interview source stated that in the context of an increasing relevance of mobile devices and big data, power consumption plays an increasingly important role where "*real power values can only be provided to the customer when they were measured in silicon. […] (Otherwise) they are off by orders of magnitude, not like by factor of two*" (Quote interviewee O, translated). The same issues also hold true for all analog chips (which is why it was referred to as 'black magic,' see Section 2.2.1), which mandates the need for test chips as described by one interviewee stating, "*the EDA tools may not be able to fully verify those (analog chips), because in that area of domain, you do not completely understand what happens in the silicon, unless you can actually see that. For hard IP, suppliers usually have to do a test chip. Unless they do a test chip, they are simply not credible, not being looked at credibly. When we engage with hard IP guys, we mandate that there will be a test chip*." (Quote interviewee C).

One element that was something of a surprise was that a large focus was placed by large buyers of IP Cores on the coding quality (code being well structured and commented) exhibited by small providers. I cannot say for certain whether coding quality is a source of risk because poorly developed IP Cores are inherently more at risk of failure and make the frequently required post integration support more difficult. Nor can I confirm whether the coding quality is used as a proxy by the customers of the IP Core providers for the other sources of technological risk such as contained bugs or integration difficulty since coding quality is considered a good predictor of overall quality and thereby risk of the IP Core as such. One interviewee who provided source code to potential ASIC customers stated, "*one [of my customers] said 'I looked at the code and looked at another code and liked your code better' It was simply better structured, we were able to convey that a lot of thought went into it*" (Quote interviewee H, translated). Another interviewee, a vendor for IP Cores, confirmed that, "*source code reviews*" (Quote interviewee O, translated) are a relevant element of how they choose their new technology providers.

The final element of technological risk, the risk of *unknowingly infringing IP*, is closely related to the relational risk of knowingly infringing IP. A large volume of scientific literature exists on patent thickets, their adverse effects on innovation, and the difficulties that ensue for individual companies navigating this terrain (see e.g., Jell et al., 2016; Jell and Henkel, 2012; Shapiro, 1987; Ziedonis, 2004). Since IP Core providers are active in the area of semiconductors, where patents are frequently filed and actively enforced (Hall and Ziedonis, 2001), the risk of inadvertently infringing on a patent is of prime concern to all customers of IP Cores. This risk of being sued by the owner of the infringed patent is so significant that buyers of IP Cores go to considerable lengths to prevent their suppliers from infringing IP. This was described by one interviewee who said, "*All sides are factually forced to play fair because there is too much at stake for the end-customer. When you sell an IP Core to Apple which was stolen from me, then Apple has a problem. Therefore they are fiendishly careful that the IP Core is really from you. There will be an engineer who says 'Hang on, we have this* [IP Core] *by person A and this by person B and they look absolutely the same'. Then he will immediately say 'We stop talking to both of you' "* (Quote interviewee S, translated). These considerations also explain why providers with corresponding patents are well received, according to a senior manager of a buyer of IP Cores, stating that patents are a "*sign that the technology is innovative and unlikely to be infringing others' IPR, or if it does, that there is ample prior*

art in the company to try & invalidate 3rd party IPR" (Quote interviewee C). This consideration needs to be taken into account by smaller providers of IP Cores that choose not to patent their inventions due to the fact that "*patenting really is a drain on the company resources*" (Quote interviewee L). This, in turn, leads to less exposure to the patent market and therefore an increased risk that relevant patents cannot be found or considered due to the rarity of search for prior art and that, in the case of IP infringement and subsequent legal procedures, there are fewer patents to launch a retaliatory lawsuit.

5.2.3 Moderators of technological risk

Beside these factors constituting the sources of technological risk, I encountered two variables that moderated the gravity of these risks, the e*x-ante* difficulty to evaluate and the cost of reversal of the decision to buy an IP Core.

The *ex-ante* difficulty to evaluate the technology is a critical element considering MfT. In contrast to relational risks, which are frequently based on potential for opportunistic behavior in the future (such as the failure to provide integration support after the purchase) and therefore cannot be evaluated, the technological risks considered here are already contained in the purchased technology and could, therefore, theoretically be protected against through elaborate testing (this is an important distinction of markets for current technologies vs. markets for future technologies—for future technologies the dominant type of risk is relational risk). Therefore, the difficulty to fully evaluate an IP Core at the time of purchase is a critical moderator of technological risk. If technology could be fully evaluated the technological risk would disappear. In the case of IP Cores, the difficulty to perform these tests becomes apparent by the heretofore mentioned facts that full verification is impossible due to the complexity of current chip layouts that accounts for some 70-80% of the development time (see Section 2.2.1). If a company were to try to re-perform a full verification on every purchased IP Core, it would lose a significant proportion of the key advantage of immediate availability associated with sourcing externally. It is important to conceptualize the difficulty to evaluate as a continuous variable ranging between the two extremes of complete, instantaneous, free, and low-skill ability to evaluate the quality on the one end and a complete inability to evaluate the quality, regardless of time, money, and skill, employed on the other side. Examples for markets where quality is easy (and therefore inexpensive) to determine include crude oil and soy beans (Barney and Hansen, 1994). When evaluating where the IP Core industry falls on this spectrum it helps to consider what quality is. According to ISO 9001, the international norm governing quality management systems, one of the main

benefits is "the ability to consistently provide products and services that meet customer and applicable statutory and regulatory requirements" (ISO 9001, 2015, art. 0.1). IP Cores are highly difficult to evaluate for several reasons. Even when IP Cores are flawlessly working in a competitor's product and are internally flawless, they might still create a flaw in a new SoC and, in turn, the high number of products usually built of each SoC would assure that even rare flaws will be encountered by a sizable number of customers and the sheer complexity (see Section 2.2.1) and skill required for testing is considerable. This factor combined with the fact that "designs almost always have design errors and bugs" (Tuomi, 2009, p. 45) leads me to conclude that it is highly difficult to evaluate the IP Core industry.

Regarding the high cost of reversal, I compare two sub-markets of the market for IP Cores—the market for ASIC-directed IP Cores and the market for FPGA-directed IP Cores. Technologically these IP Cores are similar; neither of them is significantly harder or faster to develop. The one key difference between the two, as described in Section 2.2.2, is that in the case of an error on the chip, the FPGA is repairable with a patch post-production and even post-sales in the field since, "*you can change or update the hardware without any issues. This new implementation […] takes a couple of hours*" (Quote interviewee D, translated). Whereas for an ASIC, a new mask layer has to be developed, which is a significant investment of "*more than a million*" (Quote interviewee S, translated) and "*when the ASIC does not work, and that is not uncommon, you need to do a complete second re-run*" (Quote interviewee D, translated) with the corresponding time implications of some "*3 months*" (Quote interviewee S, translated). This results in the verification efforts for ASIC being substantially higher as confirmed by an interviewee who stated that for his small company it would be impossible to perform "*an ASIC-type of verification […]. There is just no way that amount of verification would be […] done" accompanied by the fact that "for the ASIC market, you would need to provide some more expensive tools.*" A closer deliberation of the performance differences of these two markets and the corresponding conclusions of the relevance of this factor is presented in Section 5.4.

5.2.4 Possible negative outcomes of sourcing decision

The final aspect of risk that still requires discussion is the possible outcome of a poor sourcing decision, that is, the potential downside. As previously described, these differ dramatically for FPGAs vs. ASICs. Where it is possible to fix and even repair FPGAs with an effort of a couple of hours and correspondingly little cost, the impact for

an ASIC developer is rather different. If a bug is identified at the IP Core developer during verification, it typically takes a matter of hours to address the issue, and would be unknown to any outside party, as the corresponding effort is already considered a normal part of the development of a chip. If a flaw is identified during simulation-based verification of the combined SoC by the customer of an IP Core (soft Cores are loaded into a simulation program on a computer and joint functionality is simulated), the error correction requires the formal filing of an error report to the providing company and fixing that mistake typically takes a few days with limited cost to either company. This begins to change dramatically as soon as the SoC is transferred into the mask set and sent to the foundry for a production run. In case a flaw is detected after this step, the entire mask set is obsolete (costing in excess of 1 million USD). Additionally, this sets the project back by a couple of months since the process of identifying the flaw, re-running the entire verification, and generating a new mask set is time-consuming, and, as stated by one of my interviewees, leads to significant tension before a mask run, "*Even for large companies […] everybody will be shaking before the tape out whether it will work. Those are sleepless nights*" (Quote interviewee X). If the project is already running against a tight deadline and is intended for a specific end-product whose release schedule cannot or will not be shifted, the entire project could be at risk and result in a typical project value in the range of 100-300 million USD. However, even this scenario pales in comparison with the cost and loss in reputation when a design flaw is discovered after the product has been introduced to the market. In such a case, depending on the severity of the flaw, a product recall is required and the potential exists for the scrapping of all the products that the computer chips went into. In this worst-case scenario, the cost is entirely context specific and has simply no upper bound (while rare, this is by no means a hypothetical scenario as shown by the 'Pentium FDIV bug').

These very serious adverse results of the decision to source an IP Core for an ASIC in combination with the fact that this so-called outcome potential is, regardless of its rarity, often overrepresented in the considerations of decision makers (Kahnemann and Tversky, 1979; Sitkin and Pablo, 1992) leads to buyers of IP Cores choosing not to engage with the multitude of small, aggressively pricing providers that are perceived to represent a high risk. This, in turn, enables the large providers for whom the risk is perceived to be low to charge higher prices.

When comparing these outcomes to the reasons why IP Cores are used in the first place, as summarized by the literature (see Section 2.2.3) and according to the feedback

during interviews, as summarized in Table 12, the risk consciousness of buyers of IP Cores becomes understandable. After all, taking bold risks regarding quality leading to potential delays and cost increases is not advisable when reduction of the time to market, cost, and risk overall are the prime reasons for buying an IP Core rather than developing internally.

Table 12: Most frequently cited reasons for sourcing IP Cores from interviews

Reason for sourcing IP Core	Number of interview sources
Reduce time-to-market	18
Reduce cost	13
Reduce risk	12
Increase performance	11
Lack of required capabilities/resources	11

According to one of the interviewees, "*the reason IP exists is time-to-market*" (Quote interviewee T). I heard through various interviews from both the supply and demand side of IP Cores that meeting the fixed time-tables, especially in consumer products, was absolutely paramount and one of the key drivers for the market for IP Cores. Since development of IP Cores frequently takes many months and the odds of success are notoriously difficult to predict, customers assign a high value to having a completely developed IP Core immediately at their disposal.

In combination with the time-to-market consideration, the importance of the role of de-risking is made clear in the words of a leading manager who stressed, "*the whole purpose for buying is to accelerate your time to market and de-risk your IP*" (Quote interviewee K). The aforementioned point of the difficulty of IP Core development and the multitude of elements required for building an IP Core result in IP Core integrators carefully evaluating where to develop in-house and where to resort to IP Cores that are already proven in the market.

The motivation behind cost reduction was nicely summed up by one of the interviewees who stated that "*they are more likely to buy rather than to develop their own, because their resources would be more efficiently used on developing their differentiation than on […] something where the licensing would spread the cost among their competitors*" (Quote interviewee L). During my interviews, I heard that IP Core sellers aim for at least 3-4 licensees for each product. This implies that in-house development

from scratch is routinely going to be more expensive, unless a similar product is available that needs only to be adapted.

Another, albeit less often cited, reason for licensing IP Cores is performance, specifically in areas where the reasons for the high performance are patent protected and where it is difficult to design around the patents, as highlighted by one of the interviewees: "*For us to compete in low-power we had basically no choice but to license from them*" (Quote interviewee W). Performance is frequently treated as a minimum requirement that needs to be met, but where exceeding the requirements is not rewarded and occasionally even seen viewed negatively because higher performance is usually associated with higher chip area, which in turn, translates into higher cost.

Finally, there are clear concepts within semiconductor companies as to which features are core to their offering, differentiating the market offering from the competition's, and which features are not. The high degree of specialization and the corresponding gaps in capabilities and resources in other areas were described by one interviewee with, "*TI was good at DSPs at the time. They simply don't have enough resources to create another IP (sic)*" (Quote interviewee W).

Summing up, the decision to source IP Cores involves risks from a relational perspective of the buyer-supplier relationship and is also subject to significant technological risks magnified by the difficulty to evaluate *ex ante* and the high cost to reverse the decision.

5.3 Importance and role of trust

Considering that buyers of IP Cores in the ASIC area faced with the serious risks and the distorted perception of the outcome potential do not source their IP Cores from the cheapest bidder, the question arises as to which other criteria they primarily select. As described in the marketing literature on relational risk, the answer to this question is trust, which, according to Mayer et al. (1995), is considered a means of "uncertainty reduction."

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In this section I detail how technological risk factors into the trust model and close with the provision of a comprehensive model on trust in MfT. The section is focused on the ASIC market due to the higher risk involved.

Before I introduce the trust model, I highlight one finding from the interviews that was extremely unexpected. Eleven interviewees clearly stated that trust is more important

to them than price. The feedback ranged from "*This market lives primarily from trust*" (Quote interviewee J) via "*Cost […] is rather a secondary topic*" (Quote interviewee A, translated) to "*without trust in the beginning you can be as cheap as you want*" (Quote interviewee H, translated) because "*Any small amount you could save by going to a low cost IP supplier is waaaaay offset by the increased risk to your project or your schedule of marketing or you […] missing a market window*" (Quote interviewee K). This finding directly contradicts the findings of Doney and Cannon (1997, p. 45) who investigated the importance of trust in buyer-seller relationships and found that "supplier selection is not influenced by trust of the supplier firm or its salesperson. In the industrial buying context of this study, the key criteria for supplier selection are delivery performance and relative price/cost." A possible explanation for the difference in importance of trust in the market for IP Cores relative to price/cost stems from the two moderators of technological risk, *ex-ante* difficulty to evaluate delivery performance and the relative cost of reversal, which is much higher when purchasing technology.

As detailed in Section 2.3, I follow the definition of trust by Mayer et al. (1995, p. 712) as trust being "the willingness of a party to be vulnerable to the actions of another party based on the expectation that the other will perform a particular action important to the trustor, irrespective of the ability to monitor or control that other party" – or shorter " 'willingness to take risk,' and the level of trust is an indication of the amount of risk that one is willing to take" (Schoorman et al., 2007, p. 346).

The corresponding trust model proposed by Mayer et al. (1995) and subsequent refinements by McKnight et al. (1998) consists structurally speaking of several elements: *antecedents of trust*, which then load onto *dimensions of trustworthiness* (also referred to as trusting beliefs), which translate into a *trusting intention,* which is subsequently subjected to a comparison to the *perceived risk,* and finally leads to *risk taking* if the level of trust is sufficient to satisfy the demand caused by the perceived risk. The model represents the trust that is bestowed upon the seller of IP Cores by the buyer of IP Cores.

In line with the identification of a risk element that is based on the technological uncertainty, I **that buyers of IP Cores attach great importance to the** *ability* **dimension of trustworthiness** which captures the ability of the provider to produce the IP Core at the required quality level in order to engage in the risk-taking activity of sourcing the IP Core. While the trust model proposed by Mayer *et al.* (1995) already includes 'ability' as one of the dimensions of trustworthiness, I extend upon their model by identifying a corresponding, dedicated antecedent of trust. This is a pre-purchase Audit—another

reference to the importance of both the technological risk and the corresponding role of ability-related trust and an additional factor that eliminates the need for trust—the state of technology. The model is depicted in Figure 22 and the individual elements are described below.

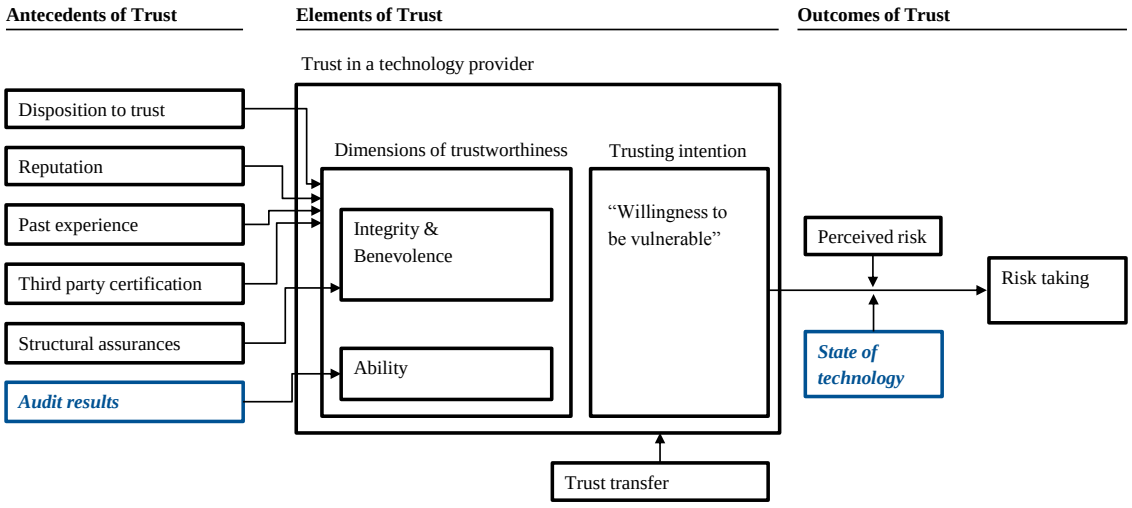

Figure 22: Model of trust

Dimensions of trustworthiness:

The Trust model proposed by Mayer et al. (1995) contains two groups of dimensions of trustworthiness, *integrity and benevolence,* which constitute the moral dimension (Hosmer, 1995) expectations toward the exchange partner and *ability*, sometimes also referred to as competence. This duality of dimensions of trustworthiness is well matched to the dual risk of relational and technological risk, with the former being addressed through the moral dimension of trust and the latter through ability. Since the literature exploring risks involved in business interactions has focused on issues around long-term partnerships and strategic alliances, the primary risk involved was the potential of future opportunistic behavior and the ensuing trust was focused around the elements of integrity and benevolence. For example, McKnight et al. (2002) investigate how trust is established in a novel online store, which revolves around the trust in the integrity of the vendor, not his ability to deliver. I expand on this concept by outlining a trust model that is focused on addressing a technological risk and hinges much more on ability. Due to ability being the essential dimension of trustworthiness in the context of IP Cores I term the resulting trust ability-related trust. I consider integrity and benevolence jointly, but mention them individually as there are contradictory findings regarding their

separability (Geyskens et al., 1998; Schoorman et al., 2007).

During the interviews, I identified six relevant antecedents to trust, four of which had an impact on both integrity/benevolence and on ability (*Disposition to trust*, *reputation*, *Past experience,* and *Third party certificates*), one item each which had an impact on the moral factors (*Structural assurances*) and one for ability (*Audit results*). These antecedents are analyzed individually and in detail in the following paragraphs.

As introduced in Section 2.3 the *Disposition to trust* is an attribute that is specific to each company and is well established in the literature. This antecedent is independent of the provider of IP Core and represents the amount of trust the trusting organization would bestow upon a trustee absent any other information. This element is exemplified by one interviewee who said regarding willingness of buyers of IP Cores to take major risks, "*There are, surprisingly, a few people who just say 'Well, then do it. If you think you can do it then go do it'* " (Quote interviewee H, translated). Due to its generic nature, *Disposition to trust* is a general construct affecting all trusting believes.

One of the most frequently reported antecedent was *Reputation,* which is based on information from third parties (McKnight et al., 1998) and is also confirmed by the literature in the context of Buyer-Seller relationships (Ganesan, 1994). Reputation is perceived as vital in the market for IP Cores and is supported by the statement, "*You need references or a name that is known in the market. In the beginning it was quite important to get references*" (Quote interviewee H, translated). However, the importance of reputation is a double-edged sword as reported by another interviewee who stated, "*You are dead. Once delivered broken IP you never again need to go anywhere. The word spreads immediately*" (Quote interviewee O, translated). For startups, the way to achieve reputation was to hire experienced senior executives as an interviewee noted, "*for new company it's word-of-mouth, it is not a relationship with a certain company, it is a relationship to people"* (Quote interviewee I) as *"people develop reputations very quickly*" (Quote interviewee T) in the market for IP Cores. An important part of reputation is based on the so-called 'track record' that captures the perception by potential buyers of the success of past IP Core integrations governed by the quality of the technology and services provided as expressed by one interviewee who stated, "*I have to say I always have doubts when I need to support something for 10 years and have to rely on a company that employs 20 people, has been founded two years ago [...]. I rather rely on a company that has been around for 10 years or has 20 years of track record*" (Quote interviewee A, translated). Another important element of reputation, especially as companies grow in

size, is a strong brand fueled by a strong reputation, which is "used as a badge or emblem that bestows credibility and attracts attention in new markets, be it a new country, a new category, or a new industry. Hence, a strong brand can reduce risks[22] a company faces in introducing new products, because customers may be less vigilant about examining the specifics" (Mohr, 2001, pg. 407). However, during the interviews I found that even the largest IP Core companies cannot rely on the branding mechanism and are subject to "*multi day review, where they really look at every single aspect of our development process*" (Quote interviewee K). A positive (or negative) effect of reputation also affects all trusting believes since third- party opinion will include both elements.

While reputation is hugely important for partners who have not yet worked together, the *Past Experience* becomes increasingly more important and substitutes reputation as companies form impressions of their counterparts based on own interactions (Gulati and Nickerson, 2008). Interviewees gave strong feedback on this point, especially those from smaller companies who stated that the personal and long- standing relationship with their customers is one of their sources of success. One interviewee stated, "*And then it's really the case that they do come back because they know 'Okay, they have done well in a project' and we really have projects running for 5-6 years, where we always get involved for the new generation*" (Quote interviewee H, translated). On the other hand, the customers appreciate this long-standing cooperation because "*they can basically see your quality. Because they know that something that is running in an FPGA is now put into an ASIC. That is proven. We have a certain safety. We can trust it*." (Quote interviewee H, translated). This kind of past experience is also sticky because even when people change companies as presented by one interviewee, "*if people have experience with you from some kind of other company, they will stick with you. We have people who have [gone] through many different companies but kept the relationship with us. Typically it is, because they know that our stuff works*." (Quote interviewee I).

Another relevant way to establish trust in the market for technologies is through *Third party certificates*. I distinguish two cases of certificates, those that are awarded upon successful qualification for membership of an alliance or group of organizations, which are typically arranged around and funded by a focal firm (e.g., Xilinx Alliance Program, TSMC OIP), and those that are awarded to products for passing certain tests and/or corresponding to a defined standard (such as SATA hard-drives or USB Cores).

[22] This is the risk of the seller of an IP Core that his novel product does not sell.

The alliance membership is an antecedent to both moral and ability-related dimensions of trustworthiness. The ability-related trust is based on the fact that the organizations awarding the certificates invest part of their reputation so they have an incentive to ensure that the corresponding IP is working. This notion is supported by one customer stating, "*TSMC accredits IP. […] So we want accredited IP and not somebody who says that it should work*" (Quote interviewee B, translated). Additionally, membership in an alliance is seen as an additional indicator for integrity; other members of the alliance, especially the focal firm, would be negatively impacted by a lack of integrity by a single organization and therefore are expected to exert pressure on individual firms to conform to the expected behavior. This assumption is supported by the close interaction and representation of alliance members through the focal firm as supported by a representative who replied to the question of how much of their reputation was at stake that, in the cases where most reputation was at stake "*We do joint customer visits, we transfer business leads from A to B, mutually promote each other*" (Quote interviewee D, translated). However the relevance of this aspect of a membership of an alliance appears to be heterogeneously perceived as described by the same representative, who stated that being a member of an alliance "*doesn't do any harm, but I doubt that because of the certificate 'member of* (name confidential) *alliance' anybody will win a design*" (Quote interviewee D, translated). The relevance of the second type of certificate that is awarded for products is paramount for products that need to conform to standards as supported by one manager who described that "*If you want to bring a CAN interface to market there is a testing body in Germany offering a conformity test. You basically need to perform this test and get the certificate before you can pitch at any automotive company*" (Quote interviewee D, translated). Correspondingly, for another interface IP Core it was reported that "*When you take a USB Core [or] an interface IP Core, it has to adhere to a certain standard, it has to go through a Plugfest, it has to get a compliance certificate*" (Quote interviewee S, translated). So in the area of standards-based interface IP, these certificates create trust in the product being bought and thereby substitute for trust in the ability of the provider of the IP Core because a neutral third party has provided direct support to the quality of the IP.

Important for determining the behavior with potential providers of IP Cores are so-called *Structural assurances*. These factors consider all means put in place by third parties that set a frame within which exchange partners are expected to operate; these include regulations, warranties, and legal framework (McKnight et al., 1998). A frequently

mentioned example for regulations is contracts governing the usage of source codes in case of bankruptcy or otherwise discontinuation of the provider of the technology. There were two options provided – either the customers directly got "*access to the code*" (Quote interviewee H, translated) or the interviewees "*worked with an escrow agent, it was part of the deal. We put the RTL, so the source code, on an escrow agent, so that they feel secure and when we get out of business, they get access to it*" (Quote interviewee N). Regarding warranties, the most relevant and frequently sought after was indemnification of the buyer of IP Cores through the provider in case of IP infringement. The effectiveness of this tool is, however, limited in terms of truly covering the expenses of a lawsuit as can be seen from the statement of a buyer of IP Cores who stated, "*At the end of the day there will be limited indemnification in the contract anyway […], because you'll bankrupt the company anyway by taking them to court*" (Quote interviewee T). Therefore, the idea intends to ensure that providers of IP Cores strictly avoid knowingly infringing IP due to the risk to their own company and therefore aims at the integrity component. The final element of the legal framework was truly relevant in the context of China where the general respect for IP and the corresponding enforceability of IP was perceived to be so low, that an interviewee responded to the question of how they protect their know-how when dealing with such countries with, "*Let's put it that way - there are certain countries where we would simply not sell to*" (Quote interviewee F). Summing up the structural assurances are ways to build trust into the integrity of a provider due to the existence of control through a third party, which can be either a respected focal firm or a government actor.

The final antecedent to trust, which I found to be relevant during my interviews, was the performance of *Audits*. These in-depth examinations take place prior to a purchase and were described as, "*We do a kind of due diligence, if you like, we have a questionnaire, you could call it, consisting of 30-35 questions along the 4 sources of risks*[23] *I mentioned in my presentation at IP-SOC*" (Quote interviewee C). These dimensions match up closely with the sources of technological risk described in Section 5.2.2 and are all elements that concern the ability of the supplier, whether it is able to do it, not whether it is willing to do it. One element that is also frequently reviewed is the "*coding style*" (Quote interviewee H, translated) which, as discussed in Section 5.2.2, may be used as a proxy for the overall quality of the coding of the IP Core. Another

[23] Risk of delivering the IP, risk of integrating the IP with the SoC, risk of (lack of) market adoption that is linked to performance, and risk of legal challenge based on (involuntary) infringement of IP.

interviewee described the elements that are audited in more detail with, "*We look at what do they have in terms of documentation? Is that properly documented so that it is comprehensible […]? We do source code reviews, […] verification reviews, look at the test cases*" (Quote interviewee O, translated) and upon purchase they will re-run the test cases based on the promised performance data and the target company will only be paid if all criteria are met. These audits are not only performed for small or young companies but also for the largest providers as described by a senior manager of one of the major IP Core companies in stating, "*it is not unusual for these big companies to come in and do a day or multi day review, where they really look at every single aspect of our development process*" (Quote interviewee K). Some aspects of the audit also go beyond the pure technical delivery and look at whether a company is able to fulfill the contract in terms of support as described by another interviewee who said, "*they wanted to evaluate the company itself. Its viability. At the end of the day, you know, that We are able to do a deal with them […] they wanted to see, what the size of the company in terms of check count in revenues and such and we, being a startup at that point, we were only 5 people and we had no past history of revenues*" (Quote interviewee N). The relevance of these audits is also apparent by their usage in marketing materials, where ARM advertises their ARM Approved Program with "Audited quality and management procedures" (ARM Ltd., 2016). Summing up, these audits are the way buyers try to satisfy their need for trust in the ability of the provider of the product by evaluating the economic situation, the internal processes, and the technical capabilities.

For some small companies that do not manage to meet the above criteria, *trust transfer*, that is, to work through or closely with an established, trusted third party, is the only other option to achieve success in the market. One example described by an interviewee referred to the ways to gain trust as "*you actually look at an investor, who can help you develop your business either through networking or by […] introducing you to major customers*" (Quote interviewee N). In the case of an alliance where the focal firm served as an "*enabler for us. […] So they have been the one that has been pushing us, asking us and kind of have vouched for us, I would say*" (Quote interviewee Q). In some cases being *"approached or asked by our customer to directly deliver certain IP because they do not want to have the extra step to the third party provider. That is also a little bit of a trust issue*" (Quote interviewee D, translated) regarding the availability of the source code and the viability of the smaller, unknown IP Core company. In order to be able to benefit from trust transfer, the new company, or startup, needs to have

unrivalled technology in order for the larger trustworthy partner to accept the risk of vouching for another company. This was stressed by many interviewees who said, "*For a startup it is always more difficult […] you need something pretty unique. […] If they do only a me-too, that doesn't help*" (Quote interviewee B, translated) with a leading provider of IP Cores seconding "*you really have to find a corner of the market, where nobody else is playing*" (Quote interviewee G).

The overall level of trust that is formed based on the above antecedents and trust transfer are subsequently compared to the risk level that is applicable for each decision. The elements of risk are described in Section 5.2 and are affected by one more element—the state of technology. This element basically captures whether an IP Core exists only as a simulation with the discussed inaccuracies of the translation into silicon, whether it has been built as a test chip, or whether it is already in commercial mass production in the desired processing technology. The last mentioned state is referred to as being "silicon proven," the ultimate sales argument for any IP Core as described by a buyer of IP Cores who described the importance of being silicon proven by the confidence this created in his respective customer "*When I say I used the USB Core by Synopsys, then my customer knows okay, that is silicon proven, there is no risk*[24]" (Quote interviewee A, translated). So basically, the state of technology is a moderator that has a direct effect on the risk overall since being silicon proven significantly increases the information available on the likelihood and gravity of a potential flaw, thereby significantly de-risking a purchase (except for the context specificity).

Finally, this comparison of level of risk with level of trust culminates in the final decision of whether to engage in the risk-taking decision and make oneself vulnerable (Mayer et al., 1995).

5.4 Deliberation between technological and relational risk

One question regarding the risk model developed based on my interviews, is how relevant is the new proportion of technological risk compared with the established relational risk.

Three points showcase the relevance of the technological risk: the *terminology used*

[24] Technically there will always be some risk that remains such as context specific flaws that are only observable in the setting of the specific SoC, but being silicon proven implies that a potential flaw within the IP Core itself would at least be very rare since it has not been encountered by the large number of customers using the technology

to describe the concern of the interviewees, the *remedies and coping mechanisms including the role of being 'silicon proven'* employed to address the risks involved in the transactions, and the *relative price sensitivity of the FPGA and the ASIC market*.

Regarding the terminology, a vivid description of the impact on firm success of not focusing on the technological risk of IP Cores was given by a leading manager of a provider of IP Cores "*Far more than anything that they [buyers of IP Cores] evaluate […] on is the quality of the IP. Because the whole purpose for buying is to accelerate your time to market and de-risk your IP. If you're buying buggy low quality IP, then you're not getting at the fundamental value, so why you're buying IP? That's why actually in the earlier days, like 10 years ago, of the IP there were a whole bunch of small IP providers that were like 'Great, we can design a digital core. All we need is a PC, something to enter VeriLog code into, a cheap simulator and we can go to market. Isn't that great?' That model just fell by the wayside really, really fast, because it didn't address the fundamentals customers care about. They needed to accelerate and de-risk. When you're buying low quality IP, you are just simply not getting that*." (Quote interviewee K). This statement was reinforced by a board member of a purchasing company who noted "*The contract rather comes last and technology comes first, second and third*" (Quote interviewee B follow-up, translated). These two quotes are exemplary of a host of quotes that contain explicit reference to the need to control the risk of designs containing undiscovered bugs. These are clearly separate from concerns of risk doing business with small companies because of their potential inability to provide required integration services *ex post*, etc. Managers I spoke with perceive the primary risk to be contained in the piece of technology they are buying rather than the dependence on the seller.

Looking at the remedies encountered as antecedents of trust—certifications, audits of internal processes and coding style, reputation in the market for delivering flawless IP Cores, and most importantly the role of being silicon proven reinforces this point. All of these elements mitigate the technological element of the risk and do not account for the potential future risks of opportunistic behavior on the side of the seller of the IP Core (see Section 5.2.2 for more detail). Most revealing is the role of being silicon proven. The statement by one of the interviewees is quite revealing, "*It is sometimes even marketing. When I say 'I have the USB Core of Synopsys inside', then my customer XY knows, 'Okay, that is silicon proven, there is no risk'* " (Quote interviewee B, translated). The most important information to the customer is that the product is silicon proven not that it is made by Synopsys, the second largest provider of IP Cores with a huge reputation in the

industry. Another manager described the startup phase of his company as, "*[we] did the classical crossing the chasm thing, because you have to be silicon proven, before anybody is going to buy you*" (Quote interviewee AB). Again, being silicon proven was the critical step to gaining market traction, not some other aspects of brand or reputation. And even in the situation where a product is not silicon proven, the technological risk is considered the primary risk when deciding on whether to engage with a company providing a superior, unrivaled new technical solution as supported by the head of IP procurement by a major semiconductor company, "*In fact the smallest company we've done a license agreement with, an IP deal, consisted of 2 people. One of the 2 was not even full time. That was a deal we did in Australia. The reason why we dealt with these guys is because they had a very innovative solution. It wasn't silicon proven, but it was not a hard IP, it was a soft IP, so RTL. You understand the difference between soft and hard IP? […] When it's hard IP, you are usually more risk averse, because if there is a bug, it takes a very long time. While for a soft IP, like ARM sells in the most part, you could probably debug the IP much faster. So we are a little bit more willing to take risk there*" (Quote interviewee C).

The final observation substantiating this claim that it is really the technological risk that is in the focus and not the brand-based reputation is that even large and highly reputed companies with long track records of successful integrations are subject to audits when their chips are not yet silicon proven. A leading manager stated, "*In terms of us getting into new areas and how new customers evaluate that: It is very, very common for us to have very deep technical dives with our customers about the quality of the IP. It is not unusual for these big companies to come in and do a day or multi day review, where they really look at every single aspect of our development process. How we design it, how we architect it, how we support it, how we insure designing quality, what our verification environment looks like, what does our regression environment look like, what does our certification environment looks like… Once we have silicon, do we take it to the standards body, in case of USB, and get it certified or go to these plug tests and do a lot of interoperability testing*" (Quote interviewee K).

The final observation that underscores the importance of technological risk in determining the buyers' behavior is the difference in market dynamics of FPGA and ASIC markets. The FPGA and ASIC chips for the same technological function are identical in terms of technology and complexity. Additionally, a soft core chip that is provided for an ASIC can also be used for an FPGA and vice versa (some adaptations are required, but it

is possible) making the companies offering the chips theoretically interchangeable. For both ASIC and FPGA, the chips may contain yet undiscovered flaws since the available verification environments are equivalent. Yet, the market dynamics are fundamentally different for these two markets. For the FPGA market, I find that "*with FPGA customers it is very bad. […] People want to get IP from the libraries but don't want to pay for it. That unfortunately destroyed the market a little*" (Quote interviewee H, translated) leading to "*the FPGA [market] is governed by price pressure. […] That market is basically broken*" (Quote interviewee S, translated) because firms operating in this market have a difficult time recovering their development cost. On the other side, interviewees stated that for the ASIC market "*Cost […] is rather secondary*" (Quote interviewee A, translated) and "*Without trust you [as a provider] cannot get in, you can be as cheap as you want*" (Quote interviewee H, translated). The only one real difference between these two markets is the cost of reversal, which is low for FPGA because "*the customers frequently think: because it is a programmable gate array I can always repair it. Therefore the perceived risk is relatively low*" (Quote interviewee S, translated), contrasted with the massive sunk cost and time in case of a defect for an ASIC mask layer (see Section 5.2.3 for a more detailed discussion) as summarized in Figure 23. The high cost of reversal primarily loads on the technological risk since the risk that a supplier will behave opportunistically in the future is independent of this item, and the strong impact resulting from a change in this moderator further supports the importance of the underlying risk for the final purchasing decision.

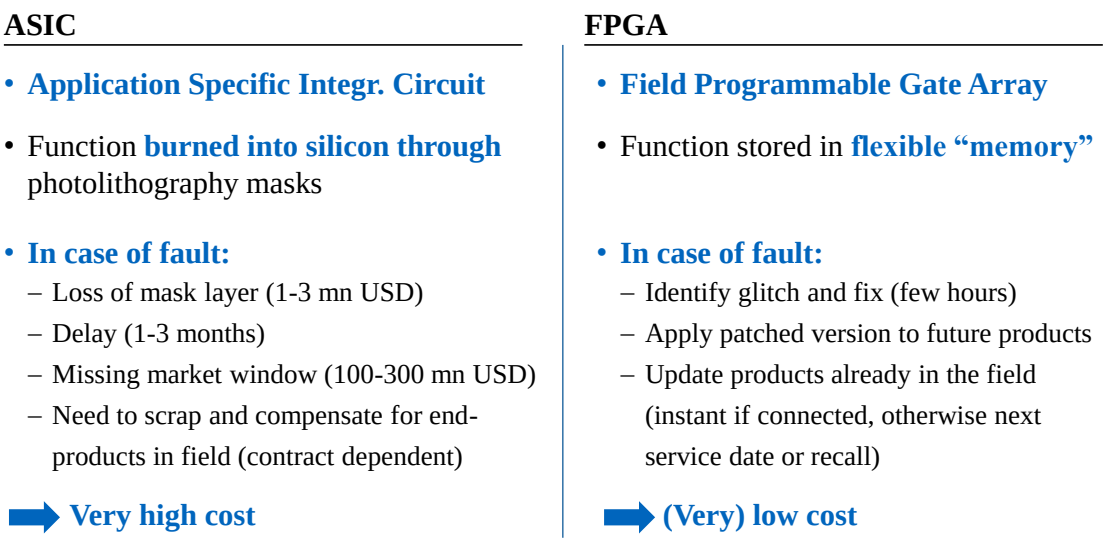

Figure 23: Comparison of FPGA and ASIC

An interesting question with regard to this last comparison between FPGA and ASIC is the question of why the market for FPGA IP Cores exists at all. One reason is the significantly lower barrier to entry that continuously creates new providers as described by one interviewee who stated, "*When you talk about startups - purely via the FPGA market. The half-life period there is similar to the Android app market. Very low barriers to entry*" (Quote interviewee S, translated). The reason the barriers are so low is that the development tools required, which can cost in the region of six digits annually for a single work space, are provided for free by the provider of the FPGA for which the IP Core is destined. Additionally, these FPGA providers maintain their own "*third party alliance networks*" (Quote interviewee U) with whom they closely interact in development and dissemination of their IP Cores. Therefore, this industry is heavily cross-subsidized by the downstream FPGA providers that benefit from having IP Core developers provide additional functionality for their chips. At the same time, there is no distinction between ASIC and FPGA providers in the rankings. However, based on my interviews, I find that none of the large companies focuses on FPGAs—they might produce an FPGA derivative of their chip for evaluation purposes of a potential large customer, but will earn the majority of their revenues through ASICs. I, therefore, conclude that the FPGA IP Core market survives due to subsidization from FPGA companies and the ability to benefit from new developments in the closely related ASIC business.

5.5 Evaluation of Transaction Costs in the market for IP Cores and implications on governance mode

Based on the analysis already detailed in the market for IP Cores, it seems to be both subject to a high level of uncertainty (due to the difficulty of evaluating whether the design contains any flaws combined with the seriousness of possible outcomes, detailed in Section 5.2.4) and a high level of asset specificity (verification is based on the specific SoC design and needs to be redone in case of change of a single component). This should, according to the literature on TCE outlined in Section 2.1.2, lead to internalization. A flourishing market exists, based on arm's-length market transactions. Therefore, this study includes a full review of transaction costs involved in the technology transaction to analyze the conflict between observed market performance and the existing literature.

Based on the market literature, I consider five types of transaction costs that are of particular relevance to the efficiency of market transactions introduced in Section 2.1.2:

weak appropriability regime, **difficulty of monitoring and enforcing contractual agreements**, **small-numbers bargaining**, **need for co-specialized assets,** and **environmental uncertainty**.

With respect to **weak appropriability regime,** as I described in Section 2.1.1, IP Cores are protected not only by patents but also by a whole set of IPR (patents, copyright, industrial design, trademark, and a sui generis protection of the layout). In the majority of cases, interviewees were quite confident that they could pursue infringement in court and were not overly concerned with competitors or end-customers stealing their technology, and relied on strong contracts, as highlighted by one interviewee stating, "*You typically will enforce the IP usage through one or two things. No 1 is: specifying the use scenarios through the contract, that's the most important. In a way making sure your IP is being used appropriately. The second way is that for all contracts we, and this is true across the board of every IP company, we all have audit rights and we can go in and audit our customers*" (Quote interviewee K). However, I repeatedly encountered real concern with regard to dealing with Chinese customers due to the perceived weak enforceability of patent protection and contracts and the corresponding risk of losing control over the technology. This was described by one interviewee who stated, "*There is a pretty strong restraint when it comes to dealing with China. We have many partners who generally are reluctant to sell anything to China. Simply because they are of the opinion that as soon as you sell to China you no longer have any possibility to protect it in any way. Despite copy protection and encrypted netlists and god knows what else they more or less settled on refraining from this topic [doing business in China]*" (Quote interviewee D), which, however, contrasts with the view of another interviewee's comments that, "*Even in China, foreign companies are pretty much on an equal footing, if you look at the statistics, in terms of getting patents allowed and even enforcing those patents*" (Quote interviewee L). So (apart from China), the appropriability regimes appear to be pretty strong and, even in the few cases where the reputation of IP protection is weak, the evidence appears to be mixed. Additionally, I collected evidence pointing to customers of IP Cores being very aware of the risk of being sued. Therefore, they take great care to select only providers with whom they felt comfortable that did not infringe on anyone else's patent rights. This opinion was included in their evaluation of possible providers of IP Cores, as one interviewee's statement that, "*Small companies always struggle with Legal risk [...]. These guys [the IP Core seller's competitors] send many, many letters [alleging infringement]. The vast majority of these letters, we just respond back and say 'You must*

be out of your mind, because not only we are not using that but etc. etc.' Most of the time with the letters it goes nowhere, but still we are getting letters every week and even multiple times a week. We have a legal team in the US mostly spending their lives challenging these letters" (Quote interviewee C). These customers have not invested any money in the development of IP Cores at this point, and therefore have no incentive to engage with developers of IP Cores that are at risk of infringing on others' IP, This is in contrast to an internalized scenario where the cost of a lawsuit would be weighed against the loss of R&D budget in case the innovation was shelved or against the potential licensing fees to be paid. I believe that the strength of the appropriability regime of patents is even stronger in market mechanism settings compared with internalized settings due to the lack of an incentive on the part of the customers of IP Cores to risk a lawsuit as supported by one interviewee who highlighted, "*[a bigger company] sued us for infringement of their patents. [...] I think anyone looking objectively at their case would agree that it was a baseless lawsuit.* […] *But as a small company, the bigger chip companies who were looking at our product saw too much risk in us disappearing. Lawsuit are generally used by the larger competitors to put risk in the eyes of potential customers when it comes to using a smaller competitor's product*" (Quote interviewee L). Therefore, the negative effect of this type of transaction cost on the market mechanism is classified as **low**.

The need for **monitoring and metering** is relevant for both buyer and seller. Buyers need to ensure that they actually receive a product meeting the performance (which can be measured on the chip upon completion of the development) and quality criteria (which cannot be measured even upon completion and can best be identified by observing the internal processes of an IP Core developer). Sellers need to insure that customers do not use the chip outside the settings granted by the licensing agreement and that customers state the correct number of products produced to compute royalties. With regard to buyers, they can quite easily evaluate the performance of a chip upon delivery. They can even evaluate a chip prior to purchase via a simulation in cases of a soft core if the IP Core is already silicon proven, by buying the competitor's SoC or by requesting a test chip, as is routinely done for hard cores. As one interviewee tasked with sourcing IP Cores for a major IDM stated, "*For hard IP, suppliers usually have to do a test chip. Unless they do a test chip, they are simply not credible, not being looked at credibly. When we engage with hard IP guys, we mandate that there will be a test chip*" (Quote interviewee C). With regard to quality requirements, customers will perform multi-day audits engaging closely

with the development team on the seller's site to gain confidence in the development and verification processes in place at their supplier because they ultimately cannot observe the adherence to agreed programming practices and conformance to agreed verification routines. For sellers, the need to monitor and meter the usage of their IP Cores as specified in the licensing agreements is ensured by conducting audits at the customer's site (see quote in previous paragraph on appropriability regimes). Sellers may additionally cooperate with foundries to identify the actual number of chips produced based on the scan of designs that foundries routinely perform (see Section 4.6). Additionally, a large share of IP Cores is not royalty bearing (one-time licensing fee only) and therefore not subject to the need to monitor the number of chips produced by the customer. Summing up, monitoring and metering is a concern to customers of IP Cores (discussed at length in Section 5.2), yet is well addressed in terms of contractual obligations and audit rights It is, therefore, classified as having **medium** negative impact on transaction costs and, in turn, on the effectiveness of the market mechanism.

The impact of **small numbers bargaining** and the extent of **co-specialization of assets** highly depends on the stage of the development that is considered. In the initial phases of an IP Core development, the effect is low since a sizable number of competitors will typically provide equivalent products allowing for choice between providers and limiting the bargaining power of the suppliers. The sellers of IP Cores are typically significantly smaller than their customers, leading to a stronger bargaining power on the buyer's side. According to one interviewee, "*IP core companies are, they are more exposed. They need to make the sale. And for them losing a deal just means losing revenue. For a bigger company like an ARM and Imagination technologies etc. then, they can set the prices very differently, because they can walk away from business*" (Quote Interviewee T). This changes rapidly, however, as soon as an IDM or Fabless company decides to do business with an IP Core company and integrate the IP Core into its SoC. The verification and the mask sets created are fully specialized to every, single component. Replacing a single component would mean re-developing a significant proportion of the chip, re-running parts of the verification (due to the interdependence of the components and the issue of context-specific bugs), and effectively losing months of development time and millions of dollars leading to extremely small numbers bargaining. The reason this dependency of buyers of IP Cores on their respective seller does not frequently lead to exploitation through the IP Core company in case of a bug is that IP Core companies' reputations are also on the line; word of failure travels quickly,

effectively prohibiting opportunism. Regardless, the issue of being unable to quickly switch suppliers of an IP Core in case of failure serves to magnify the issues around the possibility of contained bugs and, therefore, has a **high** negative impact on the attractiveness of the market mechanism.

The discussion of the final source of transaction cost, the **environmental uncertainty**, will be limited to the technological component herein due to the high importance of this factor as described in Section 5.2. The uncertainty in this regard stems from the inability to account for the sheer number of possible failure scenarios having significant difficulties in establishing who is at fault and whether compensation is required (especially in the case of context-specific bugs where each part fulfills the specification but in combination do not). Additionally, in cases of failure, it is completely unpredictable how much support is required and how to calculate the corresponding damages incurred due to a defect. This factor, combined with the frequent occurrence of bugs (Tuomi, 2009) leads to a multitude of different scenarios with varying degrees in the gravity of impact (see Section 5.2.4 for a summary of the possible consequences). The relevance to IP Core buyers' decision making can be observed via the vastly different sourcing preferences of ASIC compared with FPGA IP Cores (see Section 5.4). The described timing-dependence of the impact of flaws, combined with the impossibility of identifying all design flaws deterministically (see Section 2.2.1) and the difficulty of determining who is at fault in case of context-specific bugs (where no single company is at fault) creates significant uncertainty with regard to the completeness of contracts. This results in a **high** negative impact of this factor on the attractiveness of the market mechanism.

The findings with regard to which transaction costs are salient in the market for IP Cores is summarized at the end of this section in Table 13.

Next, I discuss the factors identified by Somaya and Teece (2001) for combining multi-invention products, which are especially relevant to the market for IP Cores: **effort for matching buyers and sellers**, **difficulty of negotiating and executing a transaction**, **strategic isolation of rents**, **diffuse entitlement problems**, **transfer of tacit know-how**, **extent of dynamic transaction cost**, **technological interconnectedness,** and **valuation problems with technological assets**.

The market is fully established and features dedicated market places that contain searchable databases of all the major IP Core providers and their respective products

including datasheets (see Section 4.6). Therefore, the impact of the factor **matching supply and demand**, along with clearly established, standardized input/output interfaces between the various elements of an SoC for matching buyers and sellers (search cost) is **low**.

Next, I consider the **difficulty of negotiating and executing a transaction**. Since the number of licensing transactions is high, 75 to 80% of all computer chips contain third-party IP Cores (see Chapter 1), the licensing agreement contracts are highly standardized. This is described by one interviewee with, "*if I am smart I will go and take the [licensing contract] of Synopsys or Cadence, copy it, because it is not protected, because Apple, Sony, Samsung they all have signed that already. They will say 'Is that the one of Synopsys? Right, then we can sign it'* " (Quote interviewee S, translated). The execution of transaction involves a simple transfer of a piece of software that is enabled by the Internet and implementation is facilitated by the widespread use of EDA software. Therefore, in line with the expectations for an established market this factor is well addressed and presents a **low** obstacle to the market mechanism.

The **strategic isolation of rents** is only salient when the companies observed also compete in the product market and is closely tied to the profit dissipation argument by Arora and Fosfuri (2003). For dedicated technology providers, these factors are not applicable since all patents filed by IP Core providers are filed with future licensing in mind since this is the primary commercialization path for IP Core providers. Therefore this factor is considered to have **low** bearing on the market mechanism.

The **diffuse entitlement problems**, which refers to the fragmented ownership of patent rights, is a major concern to any cumulative product and is very much an issue for semiconductors and, therefore, also for IP Cores. One interviewee stated, "*I think when you're being really honest today nobody can say anymore that they're not infringing IP. NOBODY can say that for any product*" (Quote interviewee B, translated). However, because it has been such a significant issue in the IP Core industry this is not really an impediment to their business; the players have developed strategies to deal with issues such as cross-licensing and patent pools (for a detailed discussion, see Hall and Ziedonis, 2001). Sourcing an IP Core from a well-connected and established IP Core developer yields the advantage of not needing to negotiate for all the cross-licenses but rather being able to rely on the IP Core developer's expertise in doing so (and being able to trigger contractual indemnification clauses in case the IP Core company fails to do so). Thus, the impact of this mechanism on the market mechanism is considered to be **low**.

The **transfer of tacit know-how** is limited for IP Cores since the knowledge transfer happens through pieces of computer code (soft core) or design files (hard core) within which the knowledge required is completely codified. The tacit knowledge required evolves around integration that is heavily supported by the EDA tools and around identifying and addressing flaws in the design. In this latest case, that transfer of tacit knowledge will be required because the knowledge of possible sources of error of an IP Core is likely to be tacit in nature and situated with the developers of that IP Core. This knowledge needs to be partially transferred to the buyer of IP Core for troubleshooting since the buyer will be reluctant to hand over its proprietary source code to the provider for holistic troubleshooting (even more so than the IP Core seller for whom it is part of doing business). Therefore, it is usual for engineers from the provider to be brought in to the overall project team (if they are not collocated already) to swiftly address these issues. Since IP Cores themselves are highly codified but some transfer of tacit knowledge may be required, this effect is considered to have a **medium**- sized, negative effect on the attractiveness of the market mechanism.

The extent of **dynamic transaction costs** and **technological interconnectedness** is considered jointly since they both hinge on the number of parties involved in the creation of an IP Core. As described in Section 2.2.2, the number of participants to be coordinated is significant and involves: the buyer of the IP Core as the focal firm; various third-party IP Cores (since bugs may be context-specific rather than contained in a single IP Core); the EDA tool company whose tools take care of integrating the various IP Cores; the foundry tasked with manufacturing the SoC (potentially outside design firms supporting in improving the SoC); and the customer of the ASIC that intends to integrate it into its customer product. The customer has to make sure the SoC meets its requirements and is compatible with any software required to run on it and may have various requirements. One IDM manager stated that his end-customers might even mandate him to "source from two fabs [by different foundries]," which, again, has implications on the parts to be included since it bars the SoC integrator from relying on parts by one of the foundries who will not make them available to the competing foundry. Especially in cases of a faulty production run, multiple stakeholders need to be involved (and contracted) in order to rapidly identify and solve the issue. This high level of interconnectedness, not only between the different providers of IP Cores but also of the other stakeholders involved in the SoC production, renders this issue one of the most significant obstacles to the market mechanism and has a **high** negative impact compared with an internal

organization where such alignments can be more efficiently organized with lower risk of opportunistic behavior.

Finally, the **valuation problem** with technological assets has already been discussed at length in Section 5.1; multiple interview sources stated that valuation is an ongoing major concern and therefore has a **high** negative impact on the attractiveness of the market mechanism compared with a vertically integrated governance structure. These points are summarized in Table 13.

Table 13: Summary of relevant transaction costs and respective salience for the market for IP Cores

First set of general Transaction Costs according to literature review

Transaction Cost Factor	**Salience in market for IP Cores**
Poor appropriability regimes	*Low*
Difficulty of monitoring and enforcing contractual agreements	*Medium*
Small-numbers bargaining	*High*
Need for co-spezialized assets	*High*
Environmental uncertainty	*High*

Second set of Transaction Costs focused on technology transactions

Transaction Cost Factor	**Salience in market for IP Cores**
Effort for Matching buyers and sellers	*Low*
Difficulty of negotiating and executing a transaction	*Low*
Strategic Isolation of Rents	*Low*
Diffuse Entitlement Problems	*Low*
Transfer of Tacit Know-how	*Medium - Low*
Extent of dynamic transaction cost	*High*
Technological Interconnectedness	*High*
Valuation Problems with Technological Assets	*High*

It is quite astonishing that the IP Core industry exists despite the significant transaction cost with which it is fraught. The literature on this subject agrees that transactions fraught with uncertainty and valuation problems should be internalized, especially when both factors are salient as they are for the market for IP Cores (see Section 2.1.2). To identify the driving force against internalization, a look at Table 11 listing the primary reasons for sourcing IP Cores is illustrative. The primary reasons are reductions

of time to market, cost, risk, performance, and lack of required capabilities and resources. The time to market, performance, and lack of required capabilities and resources motivations could arguably be addressed through increased investments in additional teams of developers who going forward would simply develop all these IP Cores currently being bought in-house. Doing this to a high standard on a continuous basis (not once an urgent need for a component occurs) would take care of the time to market, performance, and lack of required capabilities factors. However, this option directly conflicts with the aim of reducing cost, which is a pressing matter due to the increasing design cost with each chip (see Section 2.3.3 for an elaboration of design and verification productivity gaps). One interviewee summarized this point by stating, "*When there is a non-differentiating feature, for example a well-defined standard, like USB or Ethernet, there is no differentiation for the big guys. So they are more likely to buy rather than to develop their own, because their resources would be more efficiently used on developing their differentiation than on licensing something where the licensing would spread the cost among their competitors for developing a standard*" (Quote interviewee L). Also, reducing risk is only possible by resorting to an IP Core that has already entered mass production via a competitor's SoC, since internalization would necessarily require one of a company's own products to take the risk of promoting an unproven chip to 'silicon proven' status. The product market alternative of dealing in physical chips and combining them using a printed circuit board also is not attractive due to the significant disadvantages regarding processing speed, power consumption, and area required to implement a given functionality of a PCB compared with an SoC (Linden and Somaya, 2003).

The finding of high transaction costs, however, stresses the role of trust in these interactions even further. Significant literature points to trust as a way to reduce transaction costs (Aulakh et al., 1996; Dodgson, 1993; Gulati and Nickerson, 2008; Gulati and Singh, 1998; Jensen et al., 2015; Nooteboom et al., 1997; Zaheer et al., 1998; Zaheer and Venkatraman, 1995).

Despite several of the identified transaction costs having a strong negative impact on the attractiveness of market interactions, including high uncertainty and high asset specificity, which according to Harrigan (1986) should lead to internalization, I observe a functional market with frequent market mechanism governed transactions between unaffiliated parties. Based on interviews, I conclude that the advantages of the market mechanism (as described in Section 2.2.3) outweigh the transaction costs in an

environment of constantly increasing pressure regarding cost and time to market of the computer chips. The risk of internally developing a flawed product (see Section 5.2.3), which in turn increases the relative attractiveness of buying a mass market proven (silicon proven) product, enhances these pressures. These trends, especially the technological risk, are not unique to the IP Core industry and, therefore, merit consideration when evaluating the attractiveness of market transactions instead of purely analyzing the applicable transaction costs.

5.6 Limitations of research

One of the most obvious drawbacks in this study is the perceived risk of ex-*post* rationalization and the lack of generalizability, which I try to address by triangulating my findings through the diverse backgrounds of my interviewees from both buy and sell side, as well as independent industry experts.

The lack of large scale datasets is one of the most contentious issues this kind of research faces since the Trust-construct is typically only accessible via surveys that require a large number of respondents to allow for disentanglement of the closely related mechanisms described in Section 5.3. This approach is not possible in the semiconductor industry due to its generally private nature and the especially high sensitivity around the purchasing/sales process of IP Cores (see Section 3.2.3 for an overview of some of the difficulties involved). The attempt of a professional industry organization to conduct a survey on this topic among its several hundred members demonstrates this difficulty; it received only a handful of responses from mostly small companies.

Finally, the analysis is subject to a survival bias since it is difficult to find employees of failed companies. I addressed this concern by explicitly inquiring about past placements with failed companies during my interviews. This contributed many valuable lessons on the salience of the requirement for trust and, particularly, the role of being 'silicon proven.'

Another source of possible bias is that of social desirability, leading interviewees to over or understate the difficulties involved in IP Core transactions. I compared the feedback of active transaction participants to that of various independent industry experts who had no vested interest in IP Core transactions and to that of a founder in the process of selling the remains of its IP Core company, but found no evidence of systematic differences between these two groups.

5.7 Key findings of qualitative research

Since the previous sections of this chapter are quite lengthy, I have distilled the key findings from the qualitative research in the following paragraphs.

Result 1: While the *inability of downstream buyers of technology to differentiate*, the *'Not Invented Here' (NIH) syndrome*, *loss of technology as a strategic asset*, lack of

market thickness, and lack of *market congestion* are well-addressed in the market for IP Cores, *pricing* remains a significant difficulty for some companies; other, especially large ASIC providers, do not appear to suffer from this difficulty.

Result 2: The reason large providers do not suffer from the pricing difficulty is that buying an IP Core is a high-risk situation due to both the established relational risk and the technological risk inherent to the IP Cores. This leads customers to be willing to pay a premium to secure the technology from a highly reputable provider.

Result 3: This technological risk is moderated by the difficulty to evaluate the product prior to purchase and the cost of reversal, the former is dependent on the complexity of the product and therefore generally high for IP Cores, whereas the latter is significantly higher for ASIC IP Cores than for FPGA IP Cores, which can be patched in the field. This explains why the risk associated with buying an ASIC IP Core is substantially higher than the risk of sourcing an FPGA IP Core, which leads to ASIC IP Core companies being able to charge sustainable rents.

Result 4: Trust needs to overcome the technological risk in the *ability* of the provider, not only in its *integrity and benevolence,* since the primary question is not whether the provider wants to deliver an IP Core without flaws, but whether it is able to. This makes a track record highly important when judging a provider's eligibility, the performance of audits at the seller's development site by potential buyers, and the attractiveness of the membership of alliances that is conditional on passing an audit by the focal firm of the alliance.

Result 5: The market for IP Cores is subject to both high uncertainty and high asset specificity (in addition to several other sources of significant transaction cost) but is still highly functional due to the intense time and cost pressure to which the semiconductor industry is subjected, which mandates the sharing of components between competitors in order to spread the cost and risk of non-differentiating components.

After outlining the risk and trust framework prevalent in the IP Core industry based on the interview results, I next look at the results of an analysis of the patenting behavior of IP Core companies compared with that of Fabless companies. This analysis is especially interesting since it addresses the open question of the role of formal IPR in MfT not directly based on patent transactions (i.e., where patents are not the primary object being licensed).

6 The Role of Patent Protection in a Non-Patent-based Market for Technology

Despite research pointing to the relative weakness of patents in semiconductors compared with, for example, chemicals and pharma (Anand and Khanna, 2000), the analysis of patenting activity nonetheless is highly relevant in the semiconductor sector since it has seen a steady increase in patenting activity, a phenomenon coined "patent paradox" (Hall and Ziedonis, 2001).

Additionally, as described in Section 2.1, a large body of literature studying MfT relies on insights from patent data, further increasing the importance of the market participants understanding the application of this tool.

One important assumption underlying the following analysis is that companies actually exercise judgment regarding how many patents to file and for which inventions. This is in contrast to the belief that there are simply certain innovations that require patents, essentially leaving companies with little leeway on patenting. I find support for this assumption based on my interviews. One interviewee responsible for patent strategy at a semiconductor company stated that, "*I even still struggle to convince the company to care about the value, to care about truly what inventions to patent towards some rational decision making process behind it. To a certain extent, at* (name confidential)*, the board of directors wants the CEO to provide a report at the end of the year showing that we filed a certain number of patents that year. […] we're still patenting by the numbers, more than we probably should*" (Quote interviewee L).

In the following chapter, I assume a novel perspective in two ways: First I observe an industry that does not deal in patents, but primarily[25] in blueprints and, second, I compare the patenting activity of the technology providers with a company type that is similar with the exception that they deal in products—the Fabless companies (see Section 2.2.2 for a description of the company types). The similarity of the companies (both develop IP Cores, one for internal use, the other for commercialization; neither has a manufacturing footprint; the differing sales process is of no relevance to this analysis since it is neither R&D nor patenting relevant) renders them an ideal observation setting to analyze the impact of being a member of a MfT on patenting intensity—defined in this dissertation as the number of patents applied for per million USD in the R&D budget.

[25] I use the word 'primarily' because the licensing contract will include a provision on all impacted patents, but this is not perceived to be the focus of a transaction by market participants.

6.1 Hypotheses

To understand the level of patenting observed in the market for IP Cores compared with the Fabless market, two contributing factors need to be distinguished.

The first is an average industry-specific propensity to patent derived from operating in the semiconductor industry. This is high despite a weak appropriability attested to patents, a situation referred to as the 'patenting paradox' (see Hall and Ziedonis, 2001 and Section 2.1.1 for an elaboration of reasons) and is the same for both IP Core companies and Fabless companies. It, therefore, should have no impact on the comparative analysis of patenting behavior.

The second factor is based on the MfT literature's unanimous description of patents as an essential tool to make these markets viable by ensuring that theft and infringement of ideas are pursuable in courts and that technology can be disclosed prior to sale. This increases and protects innovative activity by companies and individuals (Arora et al., 2001b; Arora and Ceccagnoli, 2006; Arrow, 1962; Gans and Stern, 2010). This effect is, by definition, only salient for IP Core companies and not for Fabless companies due to the peculiarities of dealing in technology. Accordingly, I expect both companies to have a high patenting intensity but to observe a significantly higher intensity for IP Core companies (controlling for other determinants of patenting intensity such as size, research intensity, and capital intensity) due to the added incentive of patenting to safeguard the technology licensing process.

> H1: IP Core firms exhibit a higher patenting intensity compared with Fabless companies

Another interesting element of this analysis is the question of which influencing factors determine patenting intensity for technology companies compared with product companies. Hall and Ziedonis (2001) consider the R&D expenditure, the company size (operationalized via number of employees), capital intensity (operationalized via tangible assets) and, firm age as the primary explanatory variables.[26] Despite Hall and Ziedonis (2001) considering both Fabless firms and IP Core firms 'technology firms,' I expect their

[26] They further included a *post 1982* dummy variable due to changes in the efficiency of the patenting system and a *TI* dummy due to the dominant patent position of Texas Instruments at the time – both variables are not relevant for this dissertation since the year and the company are not in scope of the analysis

findings comparing IDMs with Fabless and IP Core firms to also hold when comparing Fabless firms with IP Core companies. Fabless firms are located between IDMs and IP Core companies when considering capital intensity (need for integration and cost-intensive physical distribution of chips to end-customers, but no need for own manufacturing sites) and comparable to IDMs when considering the underlying R&D effort in developing proprietary IP Cores (see Section 2.2.2).

H2: Capital intensity is more strongly positively correlated with patenting intensity for Fabless companies than for IP Core companies.

H3: R&D expenditure (per employee) is positively correlated with patenting intensity for both Fabless and IP Core companies.

H4: Firm size is positively correlated with patenting intensity for both Fabless and IP Core companies.

H5: Firm age has no significant effect on the patenting intensity for both Fabless and IP Core companies.

Before looking into the regression results based on the large panel dataset of publicly listed IP Core and Fabless companies, I summarize the various interviewee feedback collected on the role and importance of patenting for IP Core companies.

6.2 Qualitative findings

During my interviews, I received ambiguous feedback on the importance of patenting primarily because the interviewees did not disentangle the two motivations for patenting described in the introduction of this chapter. The responses stressing the importance of patents fall broadly into the categories of i) preventing infringement (10

responses), ii) keeping competition at bay[27] (8 responses), iii) usage as defensive bargaining chip (6 responses), and iv) signaling of product uniqueness (5 responses). While ii) and iii) have no relation to the process of technology transactions, i) and iv) possibly could. Looking closer at the responses in section i) I find that these concerns of infringement are not aimed directly at customers stealing know-how but rather at competitors. One interviewee stated, "*there is basically no theft [by competitors], because for a company like Qualcomm, Samsung [...] the risk is way too big, it can be proven. The last thing you want to do is steal. Steal for half a million and pay billions, not a chance. […] All our products and implementations are supported by unique patents and we're proud of that and that helps differentiate us against our competition and helps protect and fortify our competitive position"* (Quote interviewee S, translated). The final factor, iv), is related to the transaction, but there is no reason for the uniqueness of an innovation to be more important for a product sourced as an IP Core compared with one sourced as a physical SoC. Therefore, I find no direct evidence that those interviewees stressing the significance of patents were highlighting that importance during licensing rather than simply confirming the expected overall importance of patents in the semiconductor industry.

Several interviewees spoke directly to the importance of patents in the licensing process and their feedback was unanimous; patents are not a primary consideration. Answering the question of whether a lack of patents is an issue with regard to out licensing, a patent attorney of a large IDM said, "*I would say with IP Cores the transfer of know-how is the priority. I.e., you provide know-how and get paid for that. And patents are really only […] secondary. So I would not have any difficulties to out license an IP Core even if there is not a single patent on it*" (Quote interviewee AC, translated). Interviewee K also separated the two usages of patents in his statement that "*We do have patented features in our IP and of course we list those features as part of our technology. But we are not in the business of licensing patents to our customers. That's just not a business model that we support. It's not a business model that ARM, who is one of the*

[27] An interesting account of this approach was provided by one interviewee stating that one of the competitors of an earlier company he had worked at "*started their systems with a much larger patent portfolio than I had. Basically I had none. And they sued us for infringement of their patents: maybe I'm a little bit biased, but I think anyone objectively looking at their case would agree that it was a baseless lawsuit. […] They sued us and it basically made it impossible for us to sell. It could have dragged on for years, but as a small company, the bigger chip companies who were looking at our product saw too much risk in us disappearing. Lawsuits are generally used by the larger competitors to put risk in the eyes of potential customers when it comes to using a smaller competitor's product*" (Quote interviewee L).

leaders, support. Imagination, cadence, CEVA, kind of the top 5 people in the semiconductor IP space, none of them really have a patent licensing portfolio. Do they have patents to protect a unique innovation? Absolutely they do. But we are not in the business of going into patent licensing." And a reseller of IP Cores highlighted that the risk of IP Core abuse by customers is low because they are acutely aware of the risks involved in overstepping their rights according to the licensing contract, stating, "*there is less of a need to protect your IP Core as a seller, other than via a sensible licensing contract, than as a user to protect against using more than you should*" (Quote interviewee S, translated).

During the interviews, I encountered three reasons why patents are not perceived to be of particular importance in safeguarding the licensing process. Patents are not very effective because:

- infringement can be difficult (to impossible) to detect and requires reverse-engineering of competitors' and customers' products,[28] which is prohibitively expensive;
- much of the patentable technology for the interface IP segment of IP Cores is already patented as part of the standard and beyond these elements customers explicitly do not want proprietary technology since they perceive it as a risk to compatibility; and
- better, cheaper technology-based options are available to designers of IP Cores to protect their innovations.

I encountered three distinct technology-based protection mechanisms: Encryption, provision of Gate-level Netlists, and inclusion of time bombs.

The most frequently cited method to protect an IP Core during the transaction is encryption (mentioned by 12 interviewees), which ensures that IP Cores can only be read by the EDA tools of the large providers (or the tools provided by the FPGA providers) who, in turn, verify that the user of the EDA tool also has the license to use the respective IP Core. When asked how he protects against the overuse of his IP Cores, one interviewee stated, "*There is a very convenient solution from the FPGA-providers. A developer specific key is inserted into the source code which can be linked to a timer. [...] The product can then be provided for free to even Chinese customers for e.g., 30 days, after which it can no longer be compiled and is useless without payment. There are specific*

[28] I am considering only infringement of patented technology, not 1:1 copies of the entire IP Core, which can be detected by inserting watermarks (Linden and Somaya 2003).

IEEE standards for evaluation and comprehension. The effort for cracking this encryption is so high that it is difficult even for large firms" (Quote Interviewee AD, translated). This means that during the evaluation process, IP Core providers can give the code in an encrypted format and include time bombs to a possible future customer who can then load the blueprint into the EDA tool and run simulations of the performance of the joint SoC directly out of the EDA suite. This approach provides both comfort to the customers, since they are able to work and evaluate the IP Core directly in their target environment, and safeguards the seller of the IP Core from reverse engineering and usage without purchase. Even after the transaction concludes, the IP Core does not have to be provided as source code (except for architectural licenses), thus offering protection against theft of the contained technology across the entire lifetime of the IP Core. Compared with the provision of IP Cores as gate-level-netlists, which provide protection through obfuscation of the source code (see Section 2.2.1). Provision of encrypted source code enables IP Core companies to provide their customers with a configurable product that customers can alter to their needs, thus eliminating frequent, time-consuming interactions between supplier and customer. As described by one interviewee, "*These IP [Core]s can be configured and are delivered in the so-called encrypted source code format. I.e. the Xilinx-Tools know the source code and can, depending on the configuration, then select specific parts of the source code and insert them into the FPGA. With a gate-level-netlist, the customer only gets one configuration, if that needs to change just a little bit he would need to get a new gate-level-netlist. This would imply a huge interaction between our support and the customer. [...] With the encrypted source code format he can configure it himself*" (Quote interviewee AE, translated). Finally, the encryption does not require a lot of effort. One interviewee described the effort as "*something that is not comparable to the development effort you need for a core. It is something you do in a matter of hours or in worst cases days, a few days*" (Quote interviewee N). Due to the high relevance of third-party guaranteed encryption to the functioning of the market for IP Cores, it has been formalized in the IEEE Standard 1735-2014 (IEEE 1735, 2014).

The provision of netlists is basically standard procedure since it obfuscates the underlying source code and presents a significant obstacle to reverse engineering. As described by one interviewee, "*In general we rely on the belief that nobody will bother to*

reverse engineer a netlist. we have confabulators [29]for the code which we use that make it more or less illegible prior to generating the netlist so that, when you go into the first level, you still do not understand what we do. But when a major company invests, I will say, 5 man years, then they would indeed be able to reverse engineer our IP" (Quote interviewee F, translated).

The inclusion of time bombs in evaluation licenses, which shuts down the IP Core every couple of hours, ensures that potential customers do not simply integrate the test IP Core provided with an evaluation license into their product. Frequently, the combination of this option with other technological means prevents reverse engineering since source code access would enable quick removal of time bombs.

To sum up, I find that while several interviewees report the importance of patents, none of them explicitly stresses the importance of patents in connection with the out-licensing process. Furthermore, several interviewees reported that patenting was not an element of their licensing consideration and that there were alternative, more effective and efficient means to achieve the protection of know-how during and after the sale of an IP Core. This is in direct contradiction to the relevant literature's claims with regard to the importance of patents in facilitating licensing in MfT.

The qualitative findings run contrary to the existing literature, which directly connects the activity of outbound technology licensing with a need for strong patent protection. Instead, the interviews highlight the efficiency of technology-enabled secrecy as an alternative to patenting, which is highly effective in combination with contractual protection outside of China. The qualitative evidence, therefore, supports the finding in Section 5.5 that the appropriability regime is quite strong even without patent protection (due to the multitude of formal, applicable protection mechanisms, well-functioning legal systems in case of non-compliance, inclusion of audit rights in contracts, and buyers of IP Cores scrutinizing for technology theft due to concern about being a target of infringement law suits).

To further substantiate the phenomenon of the lower-than-anticipated importance of patent protections for technology providers, I next detail a quantitative model which I

[29] These are, basically, scramblers for the code that rearrange the sequence of functions within the source code thereby hiding the hierarchical logic in which the code is written and making it more difficult to comprehend.

use to compare the patenting intensity of Fabless and IP Core companies to identify systematic differences in their patenting behavior.

6.3 Quantitative model

To answer the hypotheses formulated in Section 6.1, I first compare the patenting values of Fabless and IP Core companies through univariate analysis comparing their variances and the mean of the distribution for the overall time period and individual years.

To control for the influences of other explanatory variables than being a technology provider I next use a panel dataset that combines patenting information (see Section 3.3.3) with publicly available company information (see Section 3.3.4) for both IP Core and Fabless companies. I analyze this using two different sets of regressions, the first set utilizes clustered standard errors on the firm level for the combined IP Core and Fabless company datasets, the second set uses firm-level fixed effects for the IP Core and Fabless company datasets separately. The unit of observation is a firm-year combination. I was not able to investigate Hypothesis 1 through a random effects panel regression since the Hausman test for correlation between the error terms and the independent variables rejected the Null (i.e., there was correlation between the error terms and the independent variables) requiring a fixed effects regression. This, however, would have eliminated my dummy variable 'IP Core' that is perfectly collinear with the firm-specific dummy variables since no firm changed from being IP Core to Fabless or vice versa. Therefore, I utilize an ordinary least squares (OLS) model with clustered standard errors since the panel character of the data is not essential to answering the first hypothesis (patenting characteristics are not likely to be dependent on the patenting characteristics of the previous year but rather to be determined by firm characteristics).

I compute for the regressors, in accordance with Hall and Ziedonis (2001), the decadic logarithm of R&D spending, number of employees, plant and property equipment (PPE), the firm age (Year – Year of Inception), and the year (to capture time trends). I use logarithms because they capture the decreasing changes in firm behavior for a given absolute change of a variable as the starting position of the variable increases (i.e., the patenting behavior of a firm is likely to change more as it grows from 100 to 200 employees than from 1100 to 1200 – a difference better captured by the logarithm) and also reduce the influence of outliers (Cohen et al., 2014). Herein, number of employees serves as a proxy for firm size and PPE as a proxy for capital intensity. Additionally, all monetary values are discounted to 2005 USD using the US gross domestic product

deflator (US Bureau of Economic Analysis, 2016). See Table 22 in Appendix A 4 for detailed per-company information of the explanatory variables.

As the dependent variable I use the decadic logarithm of the patenting intensity, which equals the number of patents filed in a given year divided by million dollars of R&D investment for that year in 2005 USD, plus one to enable computation of the log for firms that have not filed for a single patent in the respective year ($y_{i,t} = \frac{Patentsfiled_{i,t}}{R\&D\ spending_{i,t}} + 1$). This variable has also been used by Hall and Ziedonis (2001), termed as propensity to patent in their analysis of the patent paradox. I deviate from this terminology since I follow past scholars (e.g., Brouwer and Kleinknecht, 1999; Jell et al., 2016) in their description of two distinct, subsequent process parameters. The first process parameter, termed R&D efficiency, describes the number of patentable innovations generated per million dollars R&D budget. The second process parameter, termed propensity to patent, captures how many patents a company files given a certain set of patentable innovations. The described measure of number of patent applications divided by million dollars R&D budget (i.e. the product of the two process parameters introduced before) is called patenting intensity.

I further include a dummy for the three EDA companies due to their different business models (see Section 2.2.2) and create additional robustness tests excluding Qualcomm from the regressions due to its size and corresponding high patenting activity (see Section 3.3.3 and Section 4.5). A Qualcomm dummy with a coding of 1 for Qualcomm is not possible for the models using clustered standard errors on the firm level since this would have led to only one firm cluster exhibiting a '1' while all the rest would have exhibited '0' for this independent variable, which in turn leads to Stata no longer computing an F statistic and p-value for the entire distribution (see last entry of STATA help file 'help j_robustsingular' for details). Instead, I recalculate the regressions without the Qualcomm data as robustness tests and receive similar results (see Appendix A 11 for the corresponding figure).

Finally, it is important to stress that the regressions I run are not able to generate statements with respect to causality; they merely allow for the identification of correlations between dependent and independent variables. One illustrative example of this issue would be a positive correlation between firm size and patenting intensity. On the one hand, a company could start pursuing a more aggressive R&D agenda of hiring new researchers, which would, in turn, lead to a higher patenting intensity; thereby, the

increase in size causes an increase in patenting intensity. On the other hand, this same company could have had a breakthrough innovation using the existing staff some two years earlier and then began both filing a higher number of patents to exclude competitors from exploiting this innovation and hiring more staff to prepare for internal exploitation of the new technology. In this case, I would also see a rise in number of employees and patenting intensity, yet they would not be causally linked one way or another; rather, both would be due to the independent event of having a breakthrough innovation. Since my data does not allow distinction between these various scenarios (and the plethora of alternative imaginable scenarios leading to the same outcomes), I refrain from making statements with regard to causality in most cases, except where one decision clearly precedes the other (like choice of business model).

To investigate the first hypothesis, whether being an IP Core provider leads to a significantly higher incentive to patent, I compute four regressions including different dependent variables using regressions and clustered standard errors on firm level since I believe that the patenting intensity of year t does not depend so much on the patenting intensity of year t-1 itself, but rather that the driver of patenting behavior is the underlying firm. I therefore decided to address this firm heterogeneity by clustering standard errors on the firm level and treating the individual years as independent observations (see Equation 2). To account for overall time trends, I include Year as a regressor.

Equation 2: OLS regression of R&D expenditure, capital intensity, size, year and age on patenting intensity using clustered standard errors on firm level

Model 1:

$$y_{i,t} = \beta_0 + \beta_1 * IPCore_i + \beta_2 * LogRnD_{i,t} + \varepsilon_{i,t}$$

Model 2:

$$y_{i,t} = \beta_0 + \beta_1 * IPCore_i + \beta_2 * LogRnDperEmpl_{i,t} + \beta_3 * LogPPEperEmpl_{i,t} + \beta_4 * LogEmpl_{i,t} + \beta_5 * Year_t + \varepsilon_{i,t}$$

Model 3:

$$y_{i,t} = \beta_0 + \beta_1 * IPCore_i + \beta_2 * LogRnDperEmpl_{i,t} + \beta_3 * LogPPEperEmpl_{i,t} + \beta_4 * LogEmpl_{i,t} + \beta_5 * Year_t + \beta_7 * EDA_i + \varepsilon_{i,t}$$

Model 4:

$$y_{i,t} = \beta_0 + \beta_1 * IPCore_i + \beta_2 * LogRnDperEmpl_{i,t} + \beta_3 * LogPPEperEmpl_{i,t} + \beta_4 * LogEmpl_{i,t} + \beta_5 * Year_t + \beta_6 * Age_{i,t} + \beta_7 * EDA_i + \varepsilon_{i,t}$$

To investigate the second hypothesis regarding determinants of patenting behavior, I split my dataset into IP Core and Fabless datasets and perform panel regressions using firm-level fixed effects for each separate dataset since I am not concerned about losing the IP Core dummy for this inquiry. As I did for the clustered standard errors, I build corresponding models to increase comparability but omit the EDA control variable since it is collinear with the firm fixed effects (see Equation 3).

I also perform robustness tests removing individual years and individual companies, the two crisis years (2008 and 2009), and the two largest Fabless companies (Qualcomm and AMD whose average R&D budgets over the years 2005-2013 eclipse those of the next smaller company, NVidia, by a factor of 3 and 1.7, respectively, and can be assumed to operate differently due to their scale).

Equation 3: Firm-level fixed effects regressions of R&D expenditure, capital intensity, size, year and age on patenting intensity

Model 1:

$$y_{i,t} = \beta_0 + \beta_1 * LogRnD_{i,t} + \nu_i + \varepsilon_{i,t}$$

Model 2:

$$y_{i,t} = \beta_0 + \beta_1 * LogRnDperEmpl_{i,t} + \beta_2 * LogPPEperEmpl_{i,t} + \beta_3 * LogEmpl_{i,t} + \beta_4 * Year_t + \nu_i + \varepsilon_{i,t}$$

Model 3:

Omitted since additional variables collinear with firm-level fixed effects

Model 4:

$$y_{i,t} = \beta_0 + \beta_1 * LogRnDperEmpl_{i,t} + \beta_2 * LogPPEperEmpl_{i,t} + \beta_3 * LogEmpl_{i,t} + \beta_4 * Year_t + \beta_5 * Age_{i,t} + \nu_i + \varepsilon_{i,t}$$

Finally, during separate robustness tests I find that, in contrast to the clustered standard error regressions where no quadratic terms were significant, the PPE per Employee exhibits a significant quadratic relationship in the fixed-effects regressions. Therefore, I also compute a third set of regressions.

Equation 4: Firm-level fixed effects regressions of R&D expenditure, (quadratic) capital intensity, size, year and age on patenting intensity

Model 1:

$y_{i,t} = \beta_0 + \beta_1 * LogRnD_{i,t} + \nu_i + \varepsilon_{i,t}$ (same as Model 1 in Equation 3)

Model 2:

$$y_{i,t} = \beta_0 + \beta_1 * LogRnDperEmpl_{i,t} + \beta_2 * LogPPEperEmpl_{i,t} + \beta_3 * LogPPEperEmpl_{i,t} * LogPPEperEmpl_{i,t} + \beta_4 * LogEmpl_{i,t} + \beta_5 * Year_t + \nu_i + \varepsilon_{i,t}$$

Model 3:

Omitted since additional variables collinear with firm-level fixed effects

Model 4:

$$y_{i,t} = \beta_0 + \beta_1 * LogRnDperEmpl_{i,t} + \beta_2 * LogPPEperEmpl_{i,t} + \beta_3 * LogPPEperEmpl_{i,t} * LogPPEperEmpl_{i,t} + \beta_4 * LogEmpl_{i,t} + \beta_5 * Year_t + \beta_6 * Age_{i,t} + \nu_i + \varepsilon_i, t$$

The next section details the regression results for the models described in this chapter and provides robustness tests.

6.4 Regression results

The first set of regressions aims at identifying structural differences between companies dealing in technology and those dealing in products.

A univariate analysis comparing the variances within the log transformed patenting intensities for IP Core companies on the one side and Fabless companies on the other side reveals that the variance within the IP Core dataset is higher compared to the Fabless company dataset at the 5% significance level as detailed in Figure 24.

```
end of do-file

. sdtest PatFiledperRnD, by (IPCore)

Variance ratio test
```

Group	Obs	Mean	Std. Err.	Std. Dev.	[95% Conf.	Interval]
0	173	.2189636	.0118415	.1557509	.1955902	.242337
1	82	.1849375	.0212737	.1926412	.1426096	.2272654
combined	255	.2080219	.0105747	.1688638	.1871967	.2288471

```
    ratio = sd(0) / sd(1)                                     f =   0.6537
Ho: ratio = 1                             degrees of freedom =  172, 81

    Ha: ratio < 1               Ha: ratio != 1                 Ha: ratio > 1
  Pr(F < f) = 0.0107         2*Pr(F < f) = 0.0215          Pr(F > f) = 0.9893
```

Figure 24: Variance-comparison test for equal variance of patenting intensity of IP Core and Fabless companies over years 2005-2013

Next I test for equal means of the IP Core and Fabless datasets using two-sided t-tests for groups with unequal variances companies. I find that for all companies and for most years (with the exception of the year 2005 which features very few IP Core observations) the hypothesis of different means for the patenting intensities of IP Core companies and Fabless companies cannot be confirmed as seen in Table 14 (see Appendix A 11 for a histogram visualizing the underlying patenting intensities of Fabless and IP Core companies across all years from 2005 to 2013 and for a recomputation of Table 14 without the where the patenting intensity is not log transformed). While the mean of the patenting intensities across all years is higher (albeit not statistically significantly) for Fabless companies compared to the IP Core companies at 0.22 vs. 0.18 this small difference disappears when eliminating the EDA companies from the IP Core dataset leading to both company types displaying a mean of 0.22 and results in a p-value of the t test of 0.91.

Table 14: Two-sided t-tests assuming unequal variances for patenting intensities of Fabless vs. IP Core companies

	Observations Fabless	Mean Fabless	Observations IP Core	Mean IP Core	p-Value
All Years	*173*	0.22	*82*	0.18	**0.16**
All Years, no EDA	*173*	0.22	*58*	0.22	**0.91**
All Years, no Qualcomm	*165*	0.21	*82*	0.18	**0.29**
Only 2005	*10*	0.23	*3*	0.03	**0.00**
Only 2006	*19*	0.25	*10*	0.21	**0.59**
Only	*19*	0.25	*10*	0.21	**0.71**
Only	*19*	0.24	*10*	0.22	**0.80**
Only	*21*	0.23	*10*	0.20	**0.68**
Only	*22*	0.20	*10*	0.18	**0.82**
Only	*22*	0.20	*10*	0.16	**0.51**
Only	*22*	0.20	*10*	0.19	**0.91**
Only	*19*	0.19	*9*	0.15	**0.44**

To investigate whether the failure to confirm the first hypothesis based on the univariate analysis is due to other influences than the provision of technology vs. products I next perform a multivariate OLS regressions using clustered standard errors on firm level detailed in Equation 2. While Model 1 in Table 15 does not reveal any significant correlations between total R&D expenditure and patenting intensity, Models 2, 3, and 4 reveal a significant negative correlation between the R&D expenditure per employee and the patenting intensity as well as between firm age and patenting intensity. The dummy variable for EDA companies is significant and negative in Model 3, but the significance disappears as soon as firm age is considered. Most relevant to this analysis, however, is the fact that the first line containing the dummy variable for IP Cores is non-significant in all models (see Table 15).

Table 15: OLS regression results using clustered standard errors on firm-level according to Equation 2

Patenting intensity estimates
Panel data set of 32 companies (22 fabless, 10 IP Core) 2005 - 2013
US patents only, Clustured Std Err on Firm level
255 observations

Variable Name	Model 1	Model 2	Model 3	Model 4
Dummy for IP Cores	-0.05	-0.02	0.05	0.05
Log R&D ($2005)	-0.06			
Log R&D per employee ($2005)		**-0.3****	**-0.38*****	**-0.35*****
Log PPE ($2005) per employee		0.14	0.13	0.13
Log firm size (employees)		-0.06	0	0.02
Year		0	0	0
Log firm age				**-0.29*****
Dummy EDA companies			**-0.21***	-0.16
Constant	**0.52***	7.68	9.15	-1.91
F	1.06	2.46	4.19	9.31
Prob>F	0.36	0.06	0.00	0.00
R_sq	0.05	0.16	0.22	0.34
Observations	255	255	255	255

Signficance levels: *** p<0.01, ** p<0.05, * p<0.10

To check whether the non-significance is introduced by a single firm or an exceptional year, I run the same regression multiple times omitting each individual firm and the two largest firms (Qualcomm & AMD) iteratively, detailed in Table 16, and perform the same computation for all individual years and the two crisis years jointly (2008 and 2009), detailed in Table 17. All coefficients that had a p-value lower than the 10% significance level pointed in the same direction as the regression results presented above. Therefore, I only report the significance levels. The tables are constructed as follows: I first eliminate company A from the dataset and re-run models 1 and 4 of the regressions outlined in Equation 2. If the coefficient for the IP Core dummy is significant at the 0.05% level, I add 1 to the respective field. I then repeat this operation for all other coefficients contained in Models 1 and 4. After this step, every row contains one entry (except for the *Dummy for IP Core* and *Constant* columns, which are identical to both models and therefore feature two entries). Next, I repeat this process by reloading the full dataset (including company A) and subsequently, beginning with company B, eliminate each individual company. In total, I perform 34 iterations of company eliminations: the full dataset, 32 individual company eliminations, and the simultaneous elimination of AMD and Qualcomm.

After having performed the robustness test for companies, I perform the same for

the time periods, resulting in 11 iterations: the full dataset, the nine individual years (2005-2013), and the two crisis years 2008 and 2009 jointly.

Table 16: Robustness tests of OLS regression for individual firms

	Model 1 (basic)				Model 4 (full)			
	Non-sign	* (<0.1)	** (<0.05)	*** (<0.01)	Non-sign	* (<0.1)	** (<0.05)	*** (<0.01)
Dummy for IP Cores	34	0	0	0	34	0	0	0
Log R&D ($2005)	33	1	0	0				
Log R&D per employee ($2005)					0	0	0	34
Log PPE ($2005) per employee					32	1	1	0
Log firm size (employees)					34	0	0	0
Year					34	0	0	0
Log firm age					0	0	4	30
Dummy EDA companies					33	1	0	0
Constant	3	19	11	1	34	0	0	0

Table 17: Robustness tests of OLS regression for years

	Model 1 (basic)				Model 4 (full)			
	Non-sign	* (<0.1)	** (<0.05)	*** (<0.01)	Non-sign	* (<0.1)	** (<0.05)	*** (<0.01)
Dummy for IP Cores	11	0	0	0	11	0	0	0
Log R&D ($2005)	11	0	0	0				
Log R&D per employee ($2005)					0	0	0	11
Log PPE ($2005) per employee					11	0	0	0
Log firm size (employees)					11	0	0	0
Year					11	0	0	0
Log firm age					0	0	0	11
Dummy EDA companies					11	0	0	0
Constant	0	7	4	0	11	0	0	0

I find that the non-significance of the Dummy for IP Core is highly robust to all permutations The p-values of the IP Core dummy for the firm exclusions (Table 16) range between 12% and 61% (average of 40%) for Model 1 and 29% and 97% (average of 55%) for Model 4. The p-values for the IP Core dummy for year exclusions (Table 17) range between 35% and 43% (average of 38%) for Model 1 and 48% and 60% (average of 55%) for Model 4. This shows that the non-significance identified for the full dataset is not due to the inclusion of some outliers but, rather, is truly based on the overall data analyzed. Furthermore, I find that the significance levels for the various independent variables are quite robust, with the exception of the constant for the basic model (which is skipping between significance at the 10% and the 5% level).

The second set of panel regressions are fixed-effects regressions run separately for

the IP Core and the Fabless datasets in order to identify whether the constituting factors of the patenting intensity are comparable in accordance with Hypothesis 2.

In accordance with Equation 3, I omit Model 3 since the introduction of firm-level fixed effects eliminates the EDA tool dummy variables and, therefore, the regression results are identical to Model 2. The regressors and the dependent variable are the same as for Equation 2 based on the clustered standard errors except that the dummy for IP Core companies no longer exists, see Table 18.

Table 18: Firm-level fixed effects regression results according to Equation 3

Patenting intensity estimates
Panel data set of 32 companies (22 fabless, 10 IP Core) 2005 - 2013
US patents only, Panel w/ Fixed Effects on Firm level
255 observations

Variable Name	Model 1 Fabless	Model 2 Fabless	Model 4 Fabless	Model 1 IP Core	Model 2 IP Core	Model 4 IP Core
Log R&D ($2005)	**-0.26*** **			**-0.2*** **		
Log R&D per employee ($2005)		**-0.32*** **	**-0.36*** **		**-0.23*** **	**-0.22*** **
Log PPE ($2005) per employee		0.02	0.04		-0.06	-0.06
Log firm size (employees)		**-0.2*** **	**-0.17*** **		-0.05	-0.06
Year		0	**0.02*** **		0	0
Log firm age			**-0.66*** **			0.08
Dummy EDA companies			N/A			N/A
Constant	**1.57*** **	7.25	**-28.71*** **	**1.15*** **	1.39	5.73
R_sq (within)	0.26	0.28	0.36	0.25	0.29	0.30
F	53.62	14.22	16.53	23.42	7.09	5.62
Prob>F	0.00	0.00	0.00	0.00	0.00	0.00
Observations	173	173	173	82	82	82

Signficance levels: *** p<0.01, ** p<0.05, * p<0.10

In general, I find that a higher number of variables are highly significant in the fixed-effects regression compared with the OLS regression that uses clustered standard errors. This reveals a significantly negative correlation between higher R&D expenditure and patenting intensity in Model 1, as well as a significant negative correlation of R&D per employee and patenting intensity in Models 2 and 4 for both company types. Both Fabless and IP Core companies exhibit no significant correlation between capital intensity (operationalized as Log PPE per employee) and patenting intensity. However, this is where the similarities between the two company types end. Firm size (proxy is number of employees) has a significant and negative correlation with patenting intensity for Fabless companies while no such correlation can be confirmed for IP Core companies. Interestingly, the time component, in terms of year and age, does not have a significant

effect on patenting intensity for IP Core companies while having a highly significant effect in Fabless firms, where patenting intensity has increased over the years but decreases with firm age.[30]

A check for the existence of significant quadratic terms for the regressors reveals that an inclusion of capital intensity as a quadratic variable is highly significant for IP Core companies, yet non-significant for Fabless firms, see Table 19.

Table 19: Firm-level fixed effects regression results with squared capital intensity influence according to Equation 4

Patenting intensity estimates
Panel data set of 32 companies (22 fabless, 10 IP Core) 2005 - 2013
US patents only, Panel w/ Fixed Effects on Firm level
255 observations

Variable Name	Model 1 Fabless	Model 2 Fabless	Model 4 Fabless	Model 1 IP Core	Model 2 IP Core	Model 4 IP Core
Log R&D ($2005)	**-0.26*** **			**-0.2*** **		
Log R&D per employee ($2005)		**-0.32*** **	**-0.37*** **		**-0.23*** **	**-0.22*** **
Log PPE ($2005) per employee		0.01	-0.1		**-0.63*** **	**-0.67*** **
Log PPE ($2005) per employee, squared		0	0.04		**0.21*** **	**0.22*** **
Log firm size (employees)		**-0.19*** **	**-0.16*** **		-0.03	-0.04
Year		0	**0.02*** **		0	-0.01
Log firm age			**-0.69*** **			0.22
Dummy EDA companies			N/A			N/A
Constant	**1.57*** **	7.22	**-31.14*** **	**1.15*** **	6.03	18.08
R_sq (within)	0.26	0.28	0.37	0.25	0.40	0.40
F	53.62	11.30	13.97	23.42	8.76	7.44
Prob>F	0.00	0.00	0.00	0.00	0.00	0.00
Observations	173	173	173	82	82	82

Signficance levels: *** p<0.01, ** p<0.05, * p<0.10

The regression, including the quadratic term for PPE, reveals that PPE is significantly correlated with the patenting intensity for IP Core companies (both linear and quadratic terms are insignificant for Fabless companies) with an inflection point[31] at Log PPE ($2005) per employee = 1.595, which equals 39.400 USD of tangible assets per employee in 2005 USD. Therefore, I find a negative correlation of PPE per employee and patenting intensity up to a PPE per employee of 39.400 USD followed by a positive correlation of

[30] The difference in magnitude likely stems from years being coded in absolute numbers while age is coded as a logarithm, so the age variable for a 10 year old firm would increase by 0.04 in the next year while the year variable would increase by 1.

[31] Computed by setting the derivative of the quadratic formula of the PPE equal to zero:

$$\frac{d(ax^2+bx+c)}{dx} = 0; x = \frac{-b}{2a} = \frac{-(-0.67)}{2*0.21} = 1.595; 10^{1.543} \approx 39.400$$

PPE per employee and patenting intensity beyond this value (while on average only two IP Core companies, Rambus and Cadence, are to the right of this inflection point, a total of 21 individual periods by five IP Core companies are to the right).

In the next chapter, I discuss my findings and the implications with regard to the hypothesis, the qualitative findings, and the existing literature on the role of patents for companies active in MfT.

6.5 Discussion

While the non-significance of the univariate t-tests and the IP Core dummy of the OLS regressions using clustered standard errors on the firm level is always harder to interpret than a highly significant result due to the possibility that the dataset simply does not include enough observations to detect a weak effect, I can definitely conclude that the effect of being an IP Core provider does not have a strong, systematic impact on the patenting intensity and I therefore fail to reject the null hypothesis of Hypothesis 1.

Failure to demonstrate the increased patenting intensity is contradictory to established academic literature on this subject, which stresses the importance of patents to enable licensing. Findings are, however, in line with the suspicion highlighted by Gallini and Scotchmer (2002) that formal IP protection may be foregone if costs associated with the alternative protection are low (see Section 6.2 for a discussion of the alternative protection mechanisms). Indeed, social costs for the encountered encryption appear to be low as no significant deadweight loss is associated with it since neither price nor quantity provided is severely impacted (beyond the impact of the independently existing sui generis protection of the chip layout) and the risk of imitation is strongly reduced compared with providing unprotected source code.

The widespread and well-established availability of alternative means of protection, markedly the possibility of encryption safeguarded by large, trusted third-party companies, could constitute such an alternative protection mechanism. This would explain both why patents are not perceived to be vital to the licensing interaction (see Section 6.2) and why the patenting intensity is not significantly higher for IP Core companies compared with Fabless companies, regardless of the choice of regressors and robust to the exclusion of both firms and years (see Table 16 and Table 17).

Due to the similar coefficients resulting from the regressions and the higher

accuracy of Table 19 compared to Table 18, I only discuss the results contained in the set of regressions including the quadratic PPE term.

I reject Hypothesis 2 because the effect of capital intensity on patenting intensity is non-significant for Fabless companies; additionally, for companies with a large capital base, patenting intensity is positively correlated with capital intensity for IP Core firms. The insignificance of the correlation between capital intensity and patenting intensity for Fabless companies is noteworthy because Hall and Ziedonis (2001) identify an effect that was highly positive and larger than that of R&D expenditure. However, they note that for design firms this correlation should be weaker. For IP Core companies, the negative correlation of PPE per employee (which is strongly positively correlated with R&D investment, Revenue and number of employees, all size proxies, and age see Figure 40 in Appendix A 9) with patenting intensity for companies with a lower capital intensity could be explained by companies with a lower PPE per employee footprint being capital constrained. This capital, therefore, is subject to a trade-off between investing in tangible assets or in patents. The positive correlation between PPE per employee and patenting intensity for companies with higher capital intensity due to the quadratic term is in line with the positive correlation identified by Hall and Ziedonis (2001). However, this contradicts their finding that this element should be less important for design firms than for firms dealing in products (the coefficients for PPE per employee and PPE per employee squared for Fabless companies are close to 0 and have p-values of 0.96 and 0.94 respectively, while the coefficients for PPE per employee and PPE per employee squared for IP Core companies both have p-values of less than 0.01).

I also reject Hypothesis 3 with respect to total R&D spending and R&D expenditure per employee with both sets of firms exhibiting negative correlations. A possible explanation for this fact (considering that both the dependent variable and the research intensity are normalized) is that companies that exhibit a high R&D intensity may be doing so because they are working on technologies that require higher investments to achieve the inventive step required, and therefore also yield fewer patents per R&D investment. This argument may explain the contradiction to the positive correlation identified by Hall and Ziedonis (2001) while observing a nascent state of the Fabless and IP Core companies through observation of the years 1979-1995 when higher R&D expenditure may have resulted in more innovations rather than being a sign of companies researching more expensive areas.

I finally also reject both Hypotheses 4 and 5 due to the discrepancy between Fabless companies and IP Core companies with regard to the correlation between firm size and patenting intensity, and between age and patenting intensity. While these correlations are both highly significant and negative for Fabless companies, I do not see any significant correlation on the IP Core side. A possible explanation for this observation aiming at the R&D efficiency would be that while Fabless companies become less and less productive in their R&D efforts and produce fewer patentable innovations per R&D budget as they grow larger and older, the technology providers have found ways to break these negative trends and continue to create innovations at a high pace even as they grow larger and older (assuming the patenting propensity remains constant). However, there are also at least two alternative explanations that would cast IP Core providers in a less favorable light. First, IP Core providers could be subject to the same negative trends with regard to R&D efficiency, but make up for it with an increased patenting propensity that results in a stable patenting intensity masking the reduced innovative efficiency. Alternatively, it could be that Fabless providers at some point simply own a sufficient stock of patents to safeguard their innovative position and rely more on complementary assets such as their sales channels and customer contacts to safeguard their position and hence are able to reduce their patenting efforts, while IP Core providers lacking these complementary assets need to continue to rely on the patent system to maintain their competitive position.

I ultimately cannot disentangle the underlying mechanisms driving this different behavior with regard to patenting intensity, yet find the implications of this discrepancy interesting and therefore recommend further research in this direction.

Summing up, I surprisingly could not confirm Hypothesis 1 of having a significant and positive impact of being a technology provider on the patenting intensity. I had to reject all four further hypotheses based on the previous literature either because no effect could be observed where one would have been expected or because the effect pointed in the opposite direction. The patenting behavior exhibited by both IP Core companies and Fabless companies with regard to capital intensity, age, and size does not conform to the expected effect direction and size.

6.6 Limitations of research

One possible challenge to this analysis is that patents are found to be a weak means of protecting know-how in the semiconductor industry (Hall and Ziedonis, 2001) and,

therefore, potentially do not play a central role in the context of licensing. This argumentation, however, fails to account for the strategic importance of patenting (see Section 2.1.1) and additionally should not significantly skew the results since both companies are active in similar fields of the semiconductor industry and cover similar elements of the value chain (see Section 2.2.2). Therefore, my exclusive focus on the differential element of increased patenting intensity due to the reliance on licensing should alleviate this concern.

The most significant limitation that I cannot address is the number of observations contained in my sample. Since, due to the data availability I am limited to the Top 25 ranking in both the IP Core industry and the publicly listed companies, and to the timeframe 2005-2013, the only way I could have extended the dataset is by loading additional Fabless companies outside of the Top 25 into my dataset. This, however, would have skewed the balance further to the direction of the Fabless companies which were already contributing 22 companies compared with the IP Cores' 10.

Regarding data quality, one limitation is that the revenue is not only linked to IP Cores or chips but may also involve patent licensing, fees for integration support and tools, thereby distorting the observations by including sizable sections of the business that are not IP Core related. I addressed this concern by adding dummy variables for those companies where this was likely to be a significant proportion, namely Qualcomm and the EDA companies. Additionally, the analysis would have been cleaner if I had the number of R&D employees to control the R&D intensity; however, since I assume that IP Core companies and Fabless companies essentially perform similar tasks and any structural differences due to a larger sales staff for Fabless companies, for example, would have been taken care of by the dummy variable or the firm-fixed effects, I do not believe this effect to strongly distort my results.

One challenge regarding the observed variable of patenting intensity is that patents filed to prevent infringement cannot be distinguish from patents filed to facilitate licensing. Therefore, it could be the case that the entire need for patents to facilitate licensing is already fulfilled by the patents that are filed to protect against infringement and for other strategic reasons leading to no observable increase in patenting intensity of the technology providers. While this is theoretically a fair point, I believe the additional incentive to patent due to the proposed licensing effect should have tipped the balance toward patenting at the margin and, therefore, should have resulted in an increased patenting intensity for IP Core firms.

Having concluded looking at the quantitative aspects of patenting behavior for IP Core companies relative to the Fabless companies and finding confirmation for my qualitative statements in the database-driven empirical analysis, the next chapter closes with a summary of this dissertation and an outlook to potential future research.

7 Summary and Outlook

The market for IP Cores is a fascinating object of observation because it is an extreme market in that there are many attributes that should make the market non-viable. On the one side are the high transaction costs (Section 5.5) and price uncertainty as a source of non-viability (Section 5.1), which push the equilibrium of a make-or-buy decision toward internalization. On the other hand, the market for IP Cores exhibits low barriers to entry, which should foster entry by new providers of IP Cores able to compete aggressively on price deteriorating profitability of the incumbents to the point where new developments are no longer feasible (as is the case for parts of the FPGA market and some components of the ASIC market such as libraries of foundational IP). Torn between these two extremes, I nonetheless find a remarkably stable market that is comparable in almost all characteristics (except for size in terms of revenue and concentration) to the corresponding product market of Fabless providers, which is not fraught with these issues (Chapter 0).

With regard to the risks of market entrants or firms dropping out of the market pricing aggressively, I discover that this source of non-viability does not realize its destructive potential because customers of ASIC IP Cores do not evaluate primarily based on price but rather on minimizing the risk of acquiring a defective IP Core. I detail the various relational and technological elements of risk (Section 5.2) and identify the two elements of 'High cost of reversal' and '*ex-ante* difficulty to evaluate' as critical moderators for the role of the technological risk. Finally, I support that it is really the reliance on minimizing technological risk and exploiting the corresponding ability-related trust (Section 5.4) that is required to understand the performance and structure in this market.

The drive toward internalization (Section 5.5) is overcome by the combined pressures of required performance increases, price reductions (on a per transistor level), life cycle compressions, and the need to minimize technological risk. These factors mandate the use of third-party design components for non-differentiating parts in order to spread the corresponding development cost over a wider customer base and enable the use of market-proven components that have been demonstrated in the market and are therefore more likely to be free of flaws and ready to be immediately integrated into the overall design. This eliminates the cost, a large share of the risk, and probably most importantly, the significant time investment of internal development.

The future prospects for the market as a whole seem attractive. The combined

pressures described above are set to further increase as both cost and design effort are expected to rise with future technology nodes. This would lead to both unprecedented levels of consolidation on the side of the customers of IP Cores (the semiconductor industry had a record M&A year in 2015 with more than 100 billion USD in deals announced compared with 37.7 billion in 2014 (*Wall Street Journal*, 2015)) and also increased use of third-party designed IP. This consolidation, however, has detrimental effects for the IP Core providers. Having fewer potential customers for their IP Cores and being larger, they have more bargaining power during negotiations. This also means that even if the number of royalty-bearing products does not decrease, the number of licensees and the associated license fee volumes are expected to decrease.

In terms of market participants, the outlook is attractive for the established incumbents that can use their track record and the trust established over the years to continue outgrowing new entrants. The flip side is the case for startups and new entrants that face a tough time entering the market and only stand a chance when offering new, unrivalled technology. One possible inflection point in this regard is the rise of the Internet of Things (IoT), which may create new technological niches and thereby enable new companies to prosper.

Products that provide an interesting offering for major corporations are architectural licenses, which are currently offered by the likes of ARM and Imagination Technologies and are used by Apple in their iPhone (Tech Spark, 2016). They are an attractive option since they allow IDMs and Fabless providers to continue relying on third-party developers while differentiating themselves on top of this base offering. A downside is that the risk reduction is achievable only to a lower extent since the resulting chip is necessarily different to that of the competitors and, therefore, not silicon proven.

To better understand possible alternatives to commercial IP Cores, I also performed a joint investigation with Daunhauer (2016) into the attractiveness of Open Source IP Cores for commercial applications. I found that because the majority of Open Source IP Cores were developed by universities and hobbyists who were more interested in developing new functionality than the tedious fool-proofing and verification, most products failed to meet the high quality expectations due to the inherent technological risk; therefore, uptake by commercial players is limited, although not unheard of. Daunhauer finds that two of the key advantages of Open Source software, the price and the continuous improvement via the community, cannot be realized since commercial players need to painstakingly redo the verification on their own; no private person or

company is willing or able to create a sufficiently rigorous and complete verification for the open source IP Cores, which also inhibits iterative improvements. In contrast to Open Source software, the significantly higher cost of reversal in case of a flaw results in significantly higher risk aversion by potential customers. One interesting recent development is the adoption of an Open Source CPU by Samsung for its IoT applications in the wake of the acquisition of ARM by Softbank, which might signal a development toward large customers taking on the extra work of verification in order to minimize dependence on a no longer independent supplier (*Electronics Weekly*, 2016). It remains to be seen whether this is an isolated case under specific circumstances or the beginning of a serious disruption of the commercial IP Core industry.

Looking beyond the market for IP Cores, joint research with Petersen (2016) has identified the area of design trading in the context of Additive Manufacturing (AM) as potentially attractive. While currently there is not yet a true market to speak of, I encountered various pilot projects in this regard. I identify the lack of standards specifying how to build the products described in the blueprint as one of the key road blocks—an issue that is similar to one of the three vital ingredients required for the market for IP Cores to flourish, the availability of standard-cell libraries for computer chips (Nenni and McLellan, 2013). Considering the benefits the IP Core industry has brought to the semiconductor industry (reduction in lead time, cost and risk – see Section 2.2.3), the creation of corresponding standards for the AM industry are seen as a potentially significant contributor to realizing the benefits of decentralized production and to a breakthrough in the proliferation of design trade for additive manufacturing (Petersen, 2016).

I believe that the developed risk and trust frameworks are quite informative, especially for the small and medium players in the market to whom it provides a clearer perspective on reasons for limited demand for their solutions and possible ways to address these. With regard to public policy, I believe the creation of these markets can be supported by providing funding for some of the institutions that help generate trust, such as certification bodies, and by maintaining the legal framework that helps safeguard innovations. While I did not see an increased patenting intensity of participants of the MfT compared with participants of product markets, I did hear from various IP Core providers that a reliable legal system (with regard to enforcing nondisclosure agreements, contracts, and patents) was mandatory for them to do business with a client. This led to multiple interviewees stating that they did not do business with Chinese customers at all

and some stating they only provided Hard Cores, which is detrimental to the development of the Chinese Fabless and IDM companies.

I am cautious regarding the generalizability of my findings because the semiconductor industry and the IP Core sector are unique. I do believe that the trust mechanism is salient in industries where the technology is sufficiently complicated to be difficult to evaluate *ex ante* and to feature high, specific investments leading to high costs of reversal. Additionally, the need for trust to overcome the high uncertainty involved in technology transactions should contribute to a general importance of this factor in the context of MfT in line with the findings of Jensen et al. (2015). Potential interesting candidates could be the purchasing of new drug candidates for further development, or the selection of a consultancy for high-risk projects such as an ERP-software implementation, or post-merger integrations that cannot be repeated or easily switched mid-project.

I believe relevant next steps would be an evaluation of my qualitative findings around risks and trust using a large dataset of companies, a systematic scan of alternative markets that could be subject to the same trust-mechanism and evaluation under which conditions it is salient, and finally a further analysis of the root causes whether (and why) IP Core companies do not suffer from diminishing returns to R&D compared with Fabless companies. With regard to patenting intensity, it would be interesting to identify further pairs of technology and product company types and evaluate whether the patenting intensity is generally not higher for specialized technology providers or, if this is not the case, only with respect to the semiconductor industry due to the attractive alternative means of protecting the codified know-how.

Appendix

A 1 Interview questionnaires

Early stage interview:

Dear interview partner,

We would like to start the interview with a short introduction of ourselves, followed by a brief description of what we are exactly looking at. After this introduction we would like to ask you to describe your function in the company and your exposure to technology licensing, specifically to the licensing of Cores. After that we would like to get your opinion on a couple of questions that will help us generate insights into the licensing decision making at your company. If you agree we would like to record this conversation for ensuring proper scientific conduct.

1) Question 1:
   What do you license?
   - For which products/categories are IP Cores available?
   - How does the supplier landscape look like? Do you usually have multiple options to choose from, or is there only one provider for your specific needs?
   - Who starts the interaction on licensing possibilities? Is it the Core provider, or your company?
2) Question 2:
   Why do you license?
   - Which are the reasons for licensing?
   - What are the main benefits you get out of licensing?
   - Which are issues/drawbacks of licensing? How do they affect your licensing decisions?
   - How strong would you say are these factors when deciding whether to license (or not) on a scale of 1 (weakest) to 7 (strongest):
     i. Corporate strategy
     ii. Technology/product considerations
     iii. Individual project manager (or other) attitude towards licensing
   - Which steps/developments would be necessary to make licensing easier/more widespread?
3) Question 3:
   How do you license?
   - How do you decide whether to license or build in-house?
   - At which point of the product development process do you decide on licensing a product?
   - Who decides on whether to license and which supplier to use?

- How well would you say that the licensing process works (on a scale of 1-7, 1 being not at all and 7 being perfect)
- Who facilitates the licensing deal? Do you use external legal counsel?

4) Question 4:
What is the role of patents? What is the role of "sui generis" semiconductor topology rights?
   - How essential are patents to back up/secure the technology deals?
   - What role do patents play in your search for potential licensors?
   - Do any of the issues associated with patents (paten thickets, patent trolls, royalty stacking) negatively affect your licensing intentions?
5) Wrap up:
   - Are there any third-party data providers you use to keep an eye on your competitors' licensing activities?
   - Who else would you recommend we talk to on this behalf?
   - Would you be willing to serve as a reference?

Late stage interview guide:

Dear Madam or Sir,

I would very much appreciate the opportunity to conduct a phone interview with a representative from [Company] to broaden the scope and explanatory power of my PhD thesis.

All answers will be treated anonymously and only reported in aggregated way. If I would like to explicitly cite you for one of your statements I will contact you beforehand for approval.

1) What is [Company]'s long-term strategy and how do the product lines fit into it? Are there significant synergies between the three lines, or are they rather separate?
2) When do your customers decide to build their own chips rather than use your IP Cores?
3) Do you also offer design services on your own IP Cores, or do you focus on standardized off-the-shelf products? Do you internally use a modular product setup where you have a stable core and then an "interface wrapper" that you customize to the clients requirements?
4) How do you generate value from the IP offering? Is it primarily through IP Cores, related services or other sources?
5) How do you come up with prices for new products? Cost based vs. value based? How does price discrimination work? Do you get royalties on your chips, or are they licensing fee only? Does this depend on customer/geography?

6) Looking at the other provider types (EDA tool providers and foundries/FPGA providers) - how do you interact with them? Are they natural complements to your offering, or are they competitors? In case both arise - can you distinguish for what type of IP a complementary vs. a competitive scenario would arise?

7) Do you need to protect your IP? If so, how do you do so? Do you file patents, rely on NDAs or do you rely on secrecy? Are there settings when the importance of one of these elements is more important than the others?

8) Is "trust" a kind of soft currency in the market for IP Cores that is essential to doing business? How do you prove your trustworthiness (e.g., certifications, patents, PlugFests, references, "silicone proven" status, …)? What happens if trust is lost? Does trust constitute a major hurdle to entering the market for IP Cores for startups? Does this "trust" currency replace some of the need for law-based intellectual property rights?

9) Are there strong norms among members of the IP Core community (e.g., no copying, non-compete clauses etc.)? How are they enforced?

10) Do you also use M&A to acquire new IP Cores/technology? If not - why does this make sense for [Company] but not for you?

A 2 Interviewee overview

Table 20: Anonymized list of quoted interviewees

Full name	Role	Company	Location
Interviewee A	Head of IP Core procurement	IDM	European
Interviewee B	Member of board	IDM	European
Interviewee C	Head of IP Core procurement	IDM	European
Interviewee D	Senior marketing manager	FPGA provider	European
Interviewee E	Senior marketing manager	IP Core provider	European
Interviewee F	CEO & founder	IP Core provider	European
Interviewee G	Senior marketing manager	IP Core provider	European
Interviewee H	CTO	IP Core provider	European
Interviewee I	CTO	IP Core provider	American
Interviewee J	Senior marketing manager	EDA tool provider	European
Interviewee K	Vice President for IP	EDA tool provider	American
Interviewee L	Patent Portfolio develop	IP Core provider	American
Interviewee M	Director of IP Strategy	Foundry	Asian
Interviewee N	CEO & founder	IP Core provider	European
Interviewee O	CEO	IP Core provider	European
Interviewee P	CEO & founder	IP Core provider	American
Interviewee Q	CTO	IP Core provider	European
Interviewee R	CEO & founder	IP Core provider	European
Interviewee S	CTO & founder	Distributor of IP Cores	European
Interviewee T	CEO	Distributor of IP Cores	European
Interviewee U	Senior marketing manager	Market place for IP Cores	European
Interviewee V	Expert	Consultancy	European
Interviewee W	Expert	Consultancy	American
Interviewee X	Expert	University	European
Interviewee Y	Director for Strategic Investment	IDM	European
Interviewee Z	Senior marketing manager	IP Core provider	European
Interviewee AA	Expert	Consultancy	American
Interviewee AB	Senior marketing manager	IP Core provider	American
Interviewee AC	Patent attorney	IDM	European
Interviewee AD	CEO & founder	IP Core provider	European
Interviewee AE	Sales director	IP Core provider	European
Interviewee AF	Expert	Consultancy	American

A 3 Coding tree

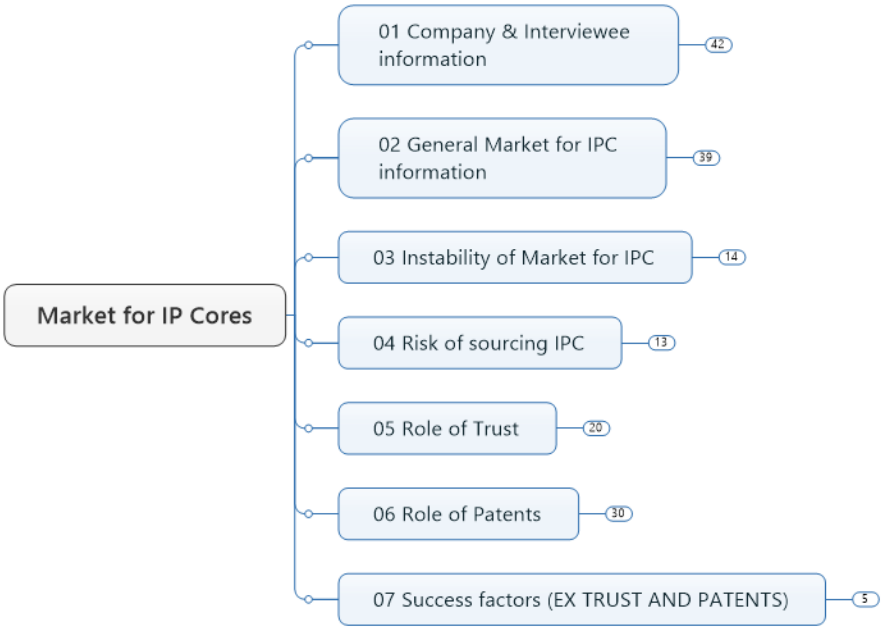

Figure 25: Top level overview of coding tree

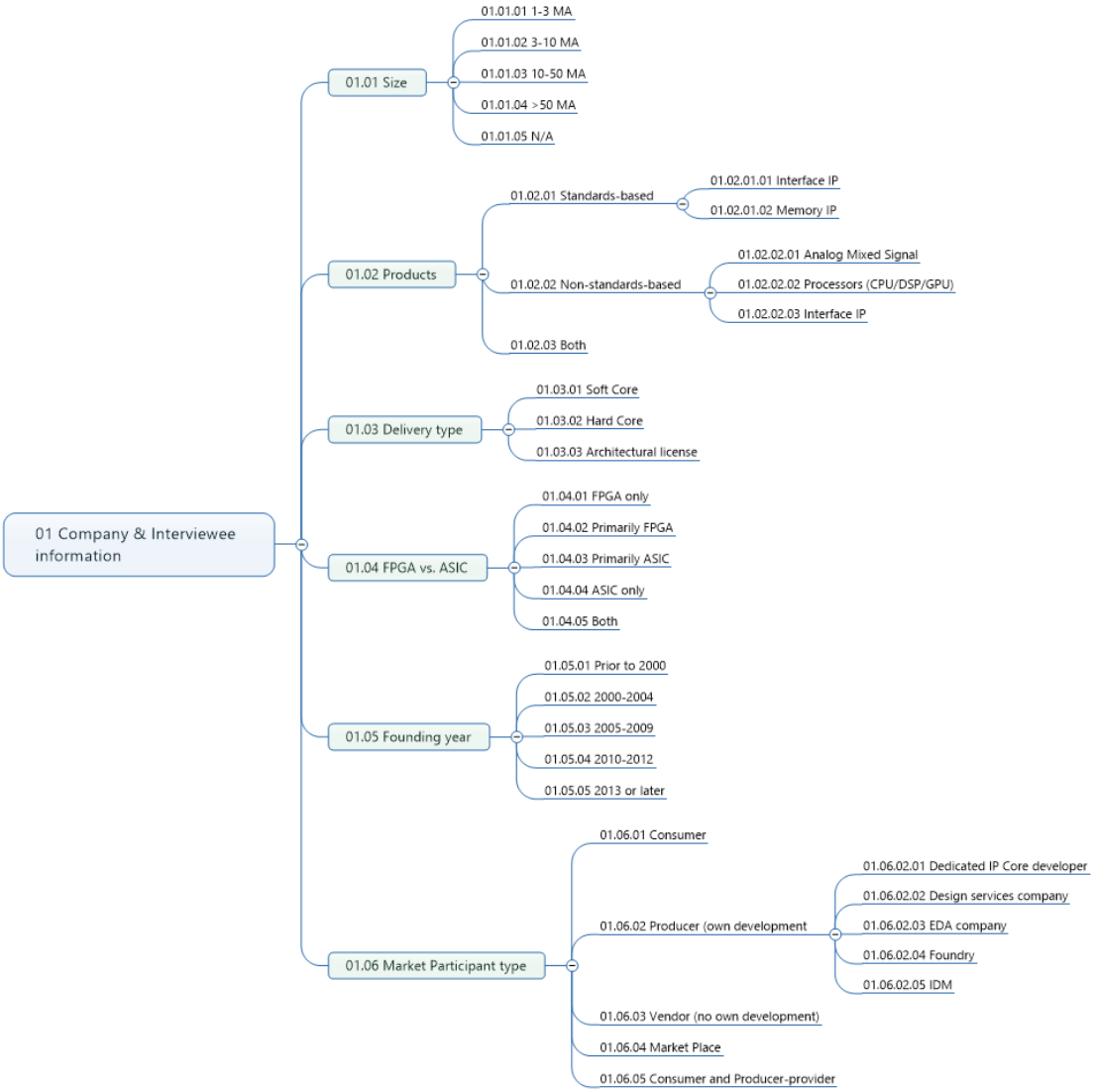

Figure 26: Coding Tree - 01 Company and interviewee information

Figure 27: Coding tree - 02 General Market for IPC information

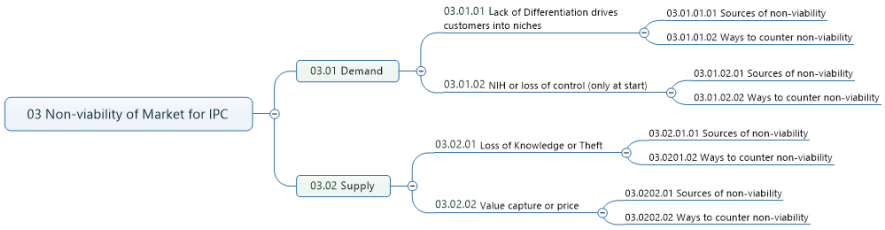

Figure 28: Coding tree - 03 Non-viability of market for IP Cores

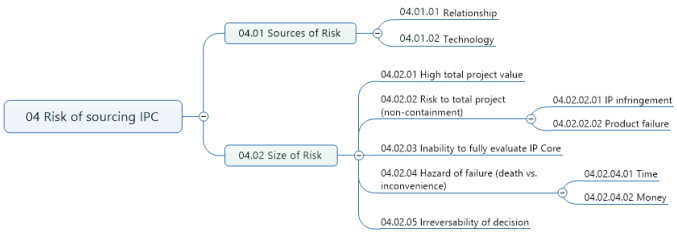

Figure 29: Coding tree - 04 Risk of sourcing IP Cores

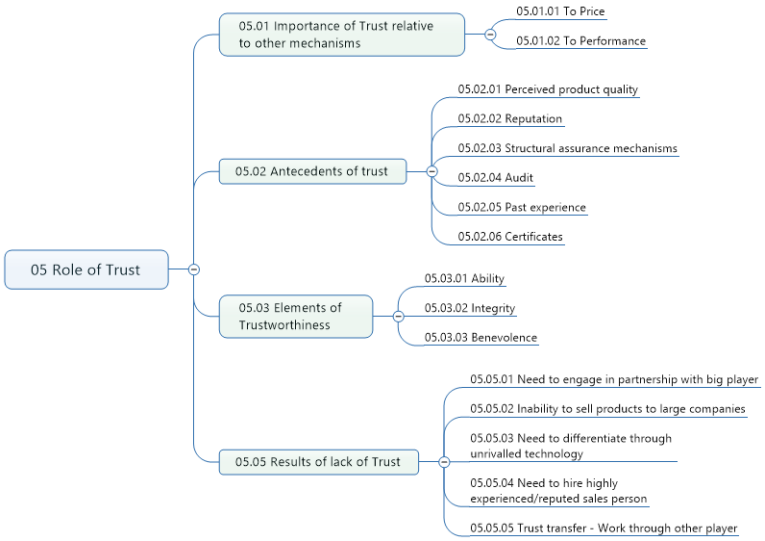

Figure 30: Coding tree - 05 Role of Trust

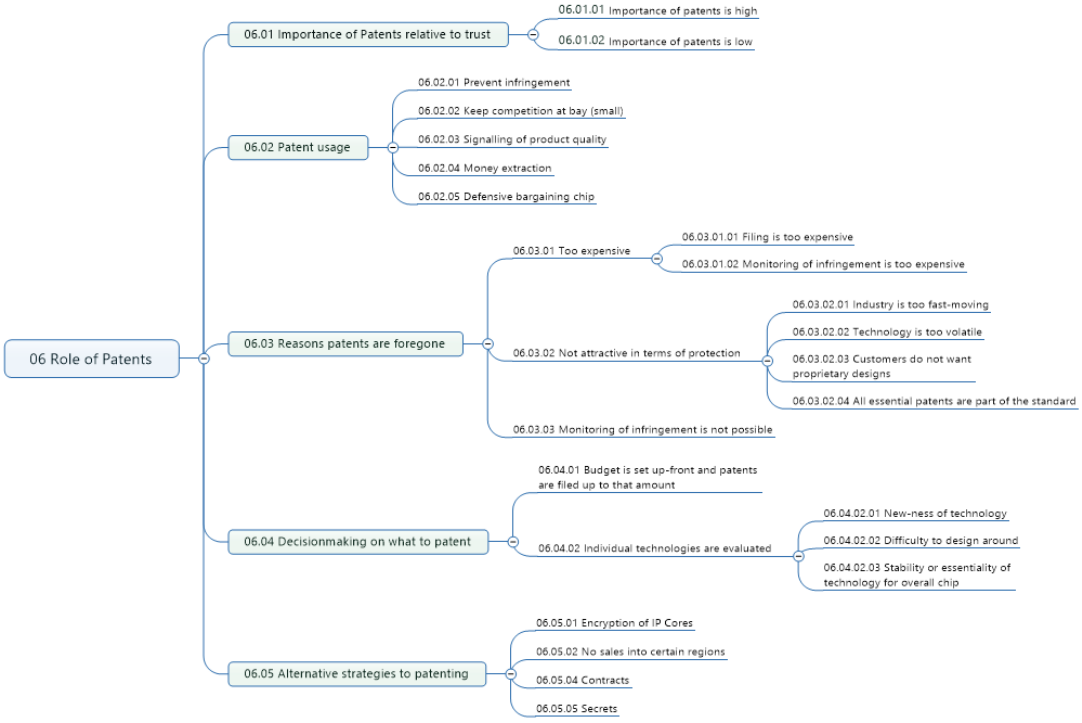

Figure 31: Coding tree - 06 Role of Patents

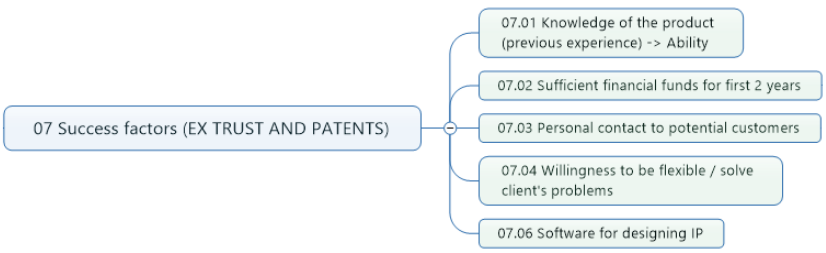

Figure 32: Coding tree - 07 Success factors (excluding trust and patents)

A 4 Company descriptive information

Table 21: Aggregate descriptive statistics of companies included for patent analysis; Data: Orbis, Patstat

	IP Core				
	Avg	Min	1st Quartile	3rd Quartile	Max
Revenue (in thsd 2005 USD)	451,626	7,736	102,967	818,274	1,676,855
R&D (in thsd 2005 USD)	151,568	2,755	43,008	261,182	571,875
PPE (in thsd 2005 USD)	65,086	464	7,422	106,573	343,431
Employees	2,030	105	363	4,400	8,573
Age	18.4	6.0	12.0	23.8	32.0
Patents filed (per year)	78	0	4	125	364
Patents granted (per year)	48	0	2	93	196
R&D intensity	37%	21%	31%	43%	67%
Profit margin	5%	-97%	-2%	21%	64%
Gross margin	83%	50%	68%	93%	118%
Patenting intensity	0.71	0.00	0.09	1.21	4.70

	Fabless				
	Avg	Min	1st Quartile	3rd Quartile	Max
Revenue (in thsd 2005 USD)	1,868,237	82,752	467,463	2,060,105	21,249,816
R&D (in thsd 2005 USD)	401,567	10,108	70,151	509,005	4,244,651
PPE (in thsd 2005 USD)	319,961	906	29,323	295,682	4,434,418
Employees	3,601	195	806	4,324	31,000
Age	18.7	3.0	11.0	24.0	53.0
Patents filed (per year)	311	0	28	246	5,405
Patents granted (per year)	165	0	18	187	1,483
R&D intensity	20%	2%	15%	25%	41%
Profit margin	10%	-158%	6%	22%	44%
Gross margin	51%	8%	42%	65%	77%
Patenting intensity	0.78	0.00	0.26	1.10	4.35

Table 22: Per company descriptive statistics of companies included for patent analysis; Data: Orbis, Patstat

	IP Core	EDA	Years contained	Average Revenue [$2005 mn]	Average R&D exp. [$2005 mn]	Average R&D exp. per empl. [$2005 thd]	Average PPE [$2005 mn]	Average PPE per empl. [$2005 thd]	Average employees	Average age [years]	Average profit margin	Average gross margin	Average patents filed	Average patenting intensity
Altera			9	1,392.8	245.1	89.1	165.4	60.47	2,750	12	32%	70%	227.0	0.9
AMD			8	5,271.2	1,357.8	109.9	2,233.0	163.09	12,649	40.5	-11%	50%	290.8	0.2
Broadcom			5	1,909.7	277.7	74.8	355.4	93.38	3,720	6	18%	53%	993.0	3.6
Cirrus Logic			9	325.7	62.5	109.5	38.5	62.77	554	11	15%	57%	51.3	0.9
CSR			4	771.1	182.3	247.3	14.3	19.28	742	12.5	5%	46%	60.3	0.3
Dialog			9	317.6	58.1	122.7	21.0	44.79	467	28	1%	42%	18.9	0.3
HiMax			8	678.5	67.9	54.4	46.3	36.68	1,281	8.5	8%	24%	82.3	1.2
IDT			9	553.3	138.0	68.2	72.4	34.93	2,073	22	-13%	62%	51.2	0.4
LSI			9	1,835.8	501.7	98.6	185.5	35.59	5,119	23	-17%	54%	307.3	0.6
Marvell			9	2,641.6	798.7	140.3	339.6	63.90	5,706	14	11%	56%	379.9	0.5
Mediatek			9	2,730.3	523.7	110.4	223.3	50.41	4,701	12	29%	54%	215.3	0.6
MegaChips			9	415.0	18.3	53.2	4.8	9.76	349	14	8%	20%	18.2	1.2
Mstar			3	1,073.8	175.0	61.6	60.7	21.58	2,829	4	18%	46%	98.3	0.6
Novatek			8	990.1	92.9	78.2	44.5	40.85	1,151	12.5	16%	28%	102.3	1.2
Nvidia			8	3,376.4	807.0	130.2	462.3	75.21	6,267	11.5	11%	49%	306.9	0.4
Phison			7	730.3	22.3	46.4	23.2	47.00	458	9	8%	13%	40.1	2.0
PMC Sierra			9	456.8	153.2	124.5	20.5	15.99	1,248	25	-1%	72%	16.2	0.1
Realtek			8	558.7	120.8	56.8	87.2	42.64	2,068	22.5	12%	43%	92.9	1.0
Semtech			8	361.8	64.2	61.7	53.5	51.56	1,001	49.5	10%	60%	8.6	0.1
Silicon Labs			8	406.1	105.8	129.6	46.2	52.93	822	13.5	13%	67%	0.9	0.0
Xilinx			9	1,849.5	364.2	111.7	349.4	107.40	3,261	19	26%	67%	201.6	0.6
Average Fabless ex Qualcomm				*1,374.4*	*300.0*	*97.5*	*234.8*	*54.6*	*2,855.9*	*18.4*	*0.1*	*0.5*	*159.0*	*0.7*
Qualcomm			8	12,054.0	2,496.0	131.7	2,075.9	115.39	18,975	24.5	36%	73%	3,443.6	1.4
Average Fabless				**1,868.2**	**401.6**	**99.1**	**320.0**	**57.4**	**3,601.3**	**18.7**	**0.1**	**0.5**	**310.9**	**0.8**
ARM	TRUE		8	611.1	182.4	94.4	27.2	13.73	1,908	19.5	24%	98%	313.9	1.9
CEVA DSP	TRUE		8	39.7	17.6	92.0	1.3	6.72	191	10.5	21%	92%	0.1	0.0
eMemory	TRUE		7	16.1	5.9	35.7	6.1	32.41	161	9	31%	89%	13.4	2.5
Imagination Technologies	TRUE		9	139.3	73.1	99.9	27.6	29.09	745	15	5%	76%	6.9	0.1
RAMBUS	TRUE		8	199.7	85.0	206.4	46.9	112.24	409	19.5	-23%	103%	139.8	1.7
Silicon Image	TRUE		9	223.8	61.7	116.2	14.3	26.83	535	10	-1%	61%	28.7	0.5
Vitesse Semiconductor	TRUE		9	158.6	51.4	106.0	8.6	16.36	481	25	-15%	58%	1.4	0.0
Average IP Core ex EDA				*200.2*	*68.9*	*108.5*	*19.0*	*33.4*	*638.6*	*15.7*	*0.1*	*0.8*	*69.9*	*0.9*
Cadence	TRUE	TRUE	8	1,119.6	400.3	79.8	272.5	54.96	5,000	22.5	6%	91%	111.5	0.3
Mentor Graphics	TRUE	TRUE	8	747.3	231.0	49.0	114.7	24.49	4,655	28.5	-8%	87%	45.6	0.3
SYNOPSYS	TRUE	TRUE	8	1,310.7	422.7	65.1	142.3	22.18	6,521	23.5	13%	86%	134.9	0.3
Average EDA				*1,059.2*	*351.3*	*64.6*	*176.5*	*33.9*	*5,391.8*	*24.8*	*0.0*	*0.9*	*97.3*	*0.3*
Average IP Core				**451.6**	**151.6**	**95.6**	**65.1**	**33.6**	**2,029.8**	**18.4**	**0.0**	**0.8**	**78.0**	**0.7**

A 5 Concentration of IP Core industry

Table 23: Concentration of IP Core industry, HHI values 2006 to 2014 and market share information; Data: Gartner

	2006	2007	2008	2009	2010	2011	2012	2013	2014	Market Share 2014
Processor IP - Total		0.50	0.46	0.46	0.48	0.57	0.59	0.67	0.69	47.1%
Microprocessors	0.47	0.50	0.61	0.63	0.65	0.72	0.73	0.83	0.84	42.7%
DSP	0.39	0.46	0.35	0.31	0.28	0.39	0.34	0.32	0.32	4.5%
Physical IP - Total		0.07	0.07	0.07	0.09	0.12	0.15	0.15	0.16	33.3%
General Purpose Analog/Mixed Signal	0.09	0.12	0.10	0.06	0.06	0.06	0.06	0.07	0.07	2.4%
Wired and Wireless Interface	0.08		0.11	0.11	0.14	0.15	0.20	0.20	0.22	18.8%
Memory Cells/Blocks	0.28	0.28	0.32	0.22	0.16	0.19	0.21	0.20	0.21	9.4%
Physical Library	0.54	0.37	0.43	0.43	0.32	0.41	0.41	0.41	0.43	2.7%
Other IP - Total		0.07	0.09	0.07	0.08	0.13	0.19	0.17	0.18	19.6%
Fixed-Function Signal Processing	0.12	0.12	0.15	0.11	0.11	0.22	0.32	0.27	0.28	15.3%
Block Libraries	0.73	1.00	1.00	0.99	0.99	1.00	1.00	1.00	1.00	0.7%
Controllers and Peripherals	0.24	0.17	0.12	0.09	0.10	0.13	0.14	0.06	0.09	0.4%
Chip Infrastructure	0.32	0.43	0.43	0.35	0.39	0.32	0.32	0.46	0.50	2.2%
Miscellaneous	0.23	0.16	0.24	0.21	0.34	0.45	0.56	0.24	0.21	0.6%

Table 24: Robustness check, difference between upper and lower bound of concentration of IP Core industry, HHI values 2006 to 2014; Data: Gartner

	2006	2007	2008	2009	2010	2011	2012	2013	2014
Processor IP - Total		0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Microprocessors	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
DSP	0.00	- 0.00	0.00	-	0.00	0.00	-	-	0.00
Physical IP - Total		0.01	0.01	0.01	0.01	0.01	0.00	0.00	0.00
General Purpose Analog/Mixed Signal	0.01	0.00	0.00	0.01	0.01	0.01	0.01	0.01	0.01
Wired and Wireless Interface	0.00		0.01	0.01	0.01	0.00	0.00	0.00	0.00
Memory Cells/Blocks	0.00	-	-	0.00	0.00	0.00	0.00	0.00	0.00
Physical Library	0.00	0.00	0.00	-		0.00	0.00	0.00	0.00
Other IP - Total		0.01	0.01	0.01	0.01	0.01	0.01	0.00	0.00
Fixed-Function Signal Processing	0.00	0.00	0.00	0.01	0.01	0.00	0.00	0.00	0.00
Block Libraries	0.00	-	-	-	-	-	-	-	-
Controllers and Peripherals	0.03	0.00	0.00	0.01	0.01	0.00	0.00	0.03	0.02
Chip Infrastructure	0.00	0.00	0.00	0.00	0.00	0.00	0.00	-	0.00
Miscellaneous	0.01	0.00	0.00	0.00	0.00	0.00	-	0.00	0.00

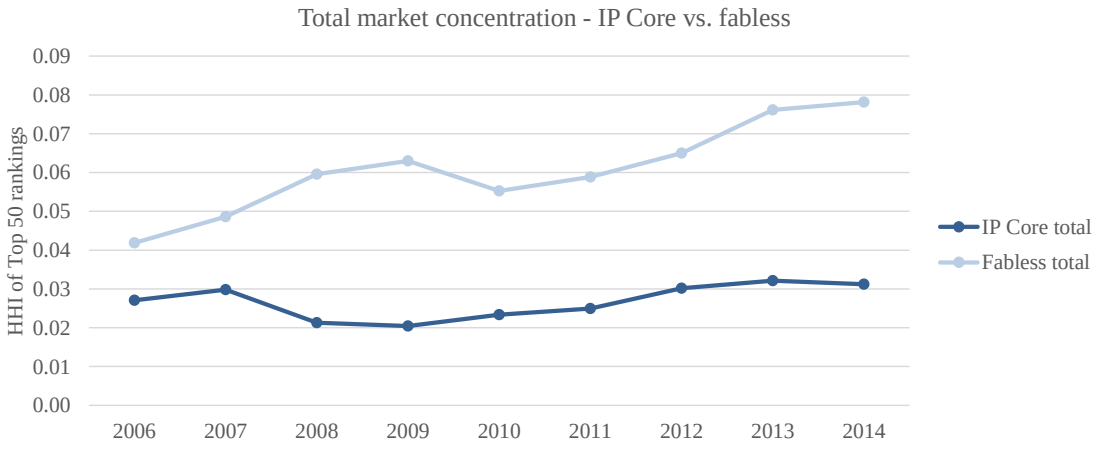

Figure 33: Robustness check HHI of Market for IP Core without ARM and Fabless; Data: Gartner, IC Insight

A 6 Revenue variance of IP Core companies vs. Fabless companies

Table 25: Descriptive statistics revenue variance, IP Core and Fabless; Data: Gartner, IC Insights

		2008	2009	2010	2011	2012	2013	2014	All Years
IP Core	Average	-4.8%	2.0%	26.5%	10.8%	1.0%	7.4% *	1.4%	6.5%
	Std. Dev	36.3%	35.4%	32.4%	33.5%	24.1%	29.5% *	18.7%	32.0%
	Observations	41	39	43	45	41	40	45	294
Fabless	Average	-3.6%	-2.3%	34.9%	3.8%	13.1%	3.8%	16.6%	9.2%
	Std. Dev	21.2%	42.4%	27.8%	25.6%	24.1%	18.9%	37.8%	31.8%
	Observations	45	42	41	43	42	41	42	296

** 1 outlier eliminated*

IP Core:

Table 26: Descriptive statistics revenue variance, IP Core, top 25 vs. bottom 25 of top 50 ranking; Data: Gartner

		2008	2009	2010	2011	2012	2013	2014	All years
Total	Average	-4.8%	2.0%	26.5%	10.8%	1.0%	*7.4% **	*1.4%*	6.5%
	Std. Dev	36.3%	35.4%	32.4%	33.5%	24.1%	*29.5% **	*18.7%*	31.9%
	Observations	41	39	43	45	41	*40 **	*45*	294
Top 25	Average	1.1%	0.4%	33.9%	16.6%	5.7%	*22.6% **	*6.7%*	12.1%
	Std. Dev	39.5%	30.7%	34.0%	35.4%	23.6%	*26.9% **	*16.5%*	32.7%
	Observations	24	22	22	24	23	*20 **	*23*	158
Bottom 25	Average	-13.1%	4.0%	18.8%	4.1%	-5.7%	-9.3%	-4.7%	0.0%
	Std. Dev	29.3%	40.5%	28.7%	29.8%	23.2%	22.5%	19.2%	29.7%
	Observations	17	17	21	21	18	20	22	136

** 1 outlier eliminated*

Fabless:

Table 27: Descriptive statistics revenue variance, Fabless, top 25 vs. bottom 25 of top 50 ranking; Data: IC Insight

		2008	2009	2010	2011	2012	2013	2014	All years
Total	Average	-3.6%	-2.3%	33.8%	3.0%	13.1%	3.8%	*16.6%*	9.2%
	Std. Dev	21.2%	42.4%	28.3%	25.9%	24.1%	18.9%	*37.8%*	31.8%
	Observatio	45	42	41	43	42	41	*42*	296
Top 25	Average	1.4%	3.4%	36.0%	11.7%	15.2%	6.7%	*24.9%*	13.9%
	Std. Dev	17.9%	54.0%	31.2%	28.3%	25.9%	14.8%	*47.0%*	35.6%
	Observatio	25	23	22	22	25	24	*23*	164
Bottom 25	Average	-9.8%	-9.3%	31.4%	-5.8%	10.0%	-0.3%	6.6%	3.5%
	Std. Dev	23.2%	18.8%	24.5%	19.6%	20.8%	22.9%	17.7%	25.2%
	Observatio	20	19	19	21	17	17	19	132

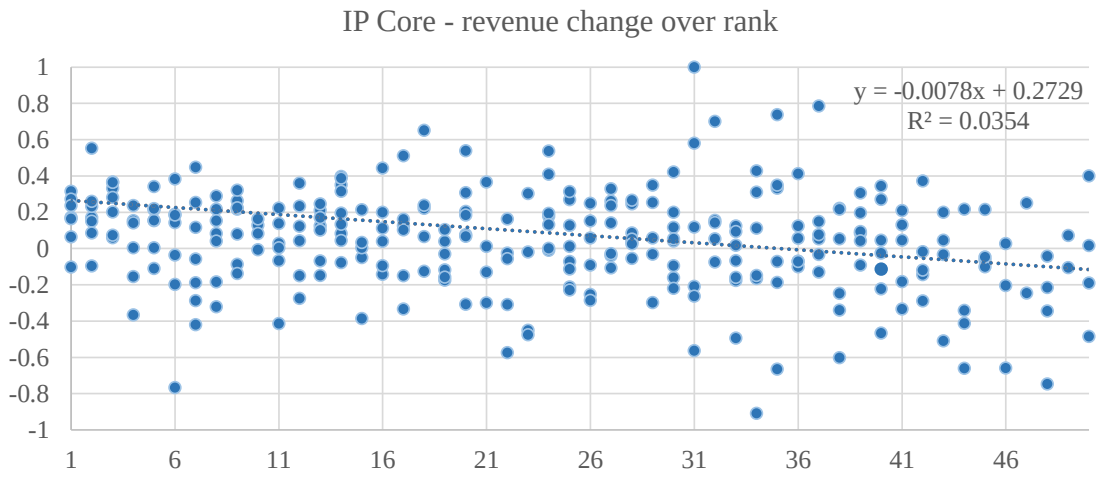

Figure 34: Monotony analysis for Spearman rank correlation coefficient - IP Core companies; Data: Gartner

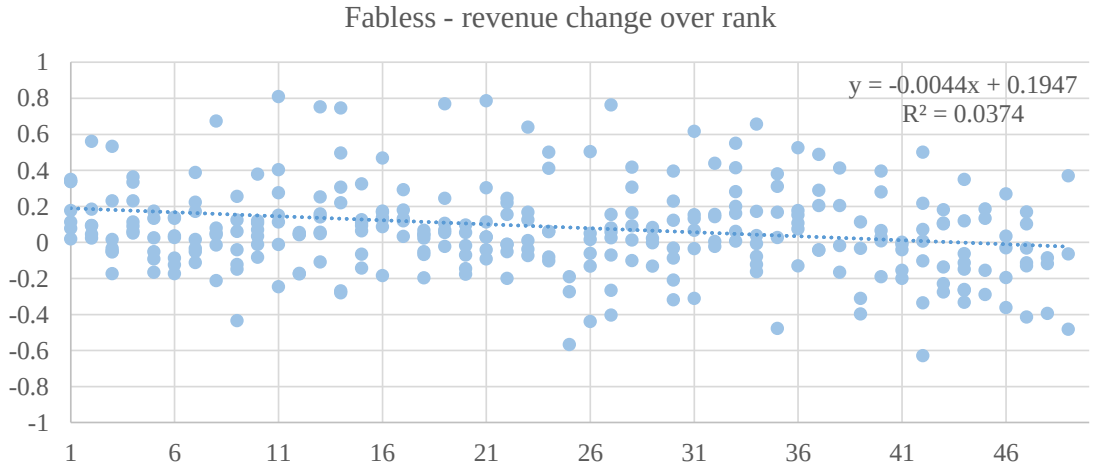

Figure 35: Monotony analysis for Spearman rank correlation coefficient - Fabless companies; Data: IC Insight

Table 28: Color-coded Spearman's rank correlation coefficients for IP Core and Fabless companies; Data: Gartner, IC Insight

			All years	2008	2009	2010	2011	2012	2013	2014
IP Core	Full ranking	Rho	-0.25	-0.21	-0.02	-0.25	-0.26	-0.36	-0.57	-0.51
		p-value	0.0%	19.9%	90.9%	10.6%	8.3%	2.0%	0.0%	0.0%
		Obs	295	41	39	43	45	41	41	45
	Top 25	Rho	-0.13	-0.14	-0.04	-0.03	-0.25	-0.27	0.02	-0.38
		p-value	9.8%	52.6%	86.5%	88.5%	23.6%	19.4%	92.3%	6.6%
		Obs	164	24	24	22	24	24	22	24
	Bottom 25	Rho	-0.23	-0.15	-0.34	-0.42	-0.20	-0.16	-0.23	-0.28
		p-value	0.9%	57.3%	21.1%	5.9%	37.8%	54.8%	34.8%	22.5%
		Obs	131	17	15	21	21	17	19	21
Fabless	Full ranking	Rho	-0.18	-0.27	-0.25	-0.09	-0.46	0.01	-0.12	-0.27
		p-value	0.1%	7.3%	11.4%	56.2%	0.2%	94.8%	46.6%	8.4%
		Obs	298	45	42	42	44	42	41	42
	Top 25	Rho	-0.07	-0.06	-0.14	0.14	0.02	0.09	-0.14	-0.35
		p-value	34.3%	76.5%	52.3%	54.3%	91.9%	67.4%	50.4%	9.9%
		Obs	164	25	23	22	22	25	24	23
	Bottom 25	Rho	-0.22	-0.02	-0.45	-0.48	-0.59	0.02	0.01	-0.15
		p-value	1.2%	91.7%	5.1%	3.1%	0.4%	94.8%	97.0%	53.8%
		Obs	134	20	19	20	22	17	17	19

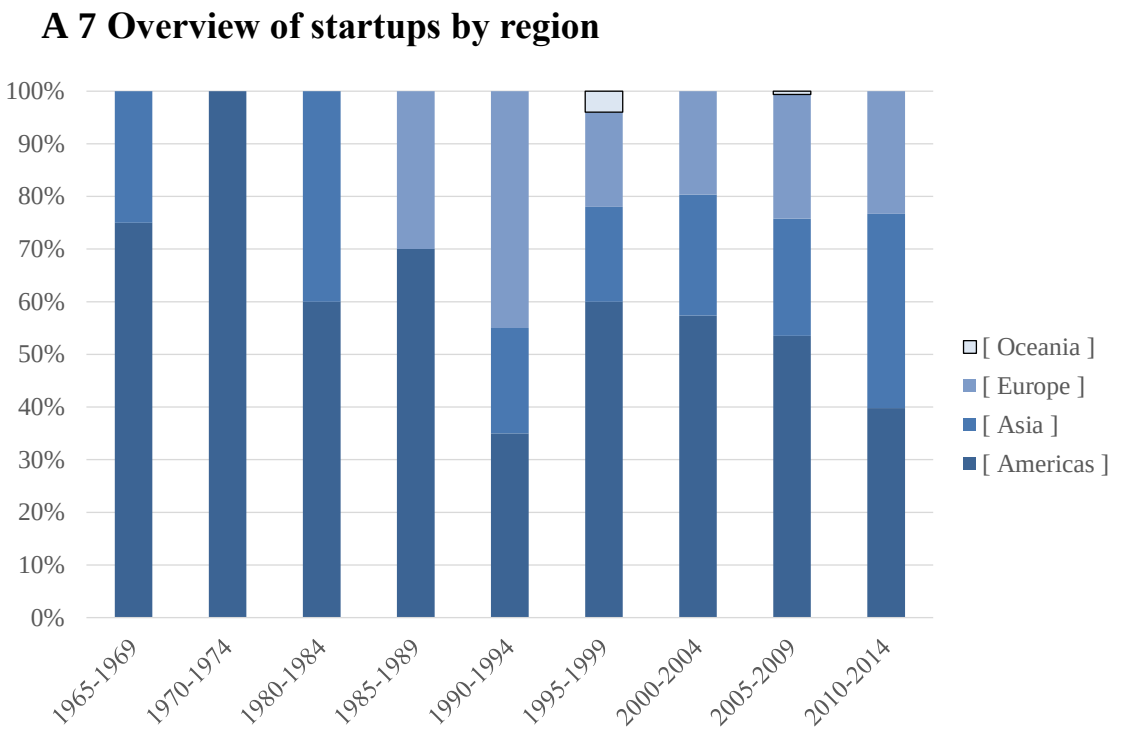

Figure 36: Share of private firms still active in 2015 per region and 5-year cluster 1965-2014; Data: Gartner 2015b

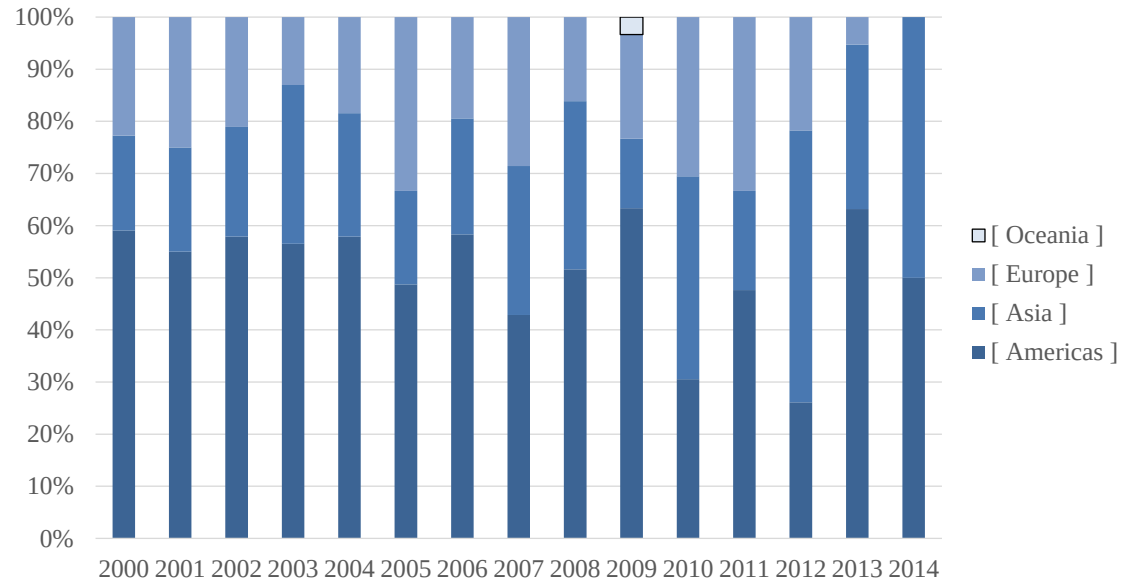

Figure 37: Share of private firms still active in 2015 per region and year 2000-2014; Data: Gartner 2015b

A 8 Patent grant success rate by company

Table 29: Patent grant success rate 1995 - 2014 by company

Firm	Number of patent applications	Number of patents granted	Success rate	Share of patents 2012 and later
Qualcomm	40,371	14,967	37%	35%
AMD	12,056	9,382	78%	6%
Broadcom	12,477	9,622	77%	22%
Marvell	4,067	3,979	98%	25%
Xilinx	3,613	3,276	91%	8%
Nvidia	3,638	2,404	66%	33%
Altera	3,388	3,147	93%	13%
LSI	3,186	2,399	75%	36%
Mediatek	2,515	1,512	60%	28%
Cirrus Logic	1,540	1,115	72%	13%
Avago	1,508	1,273	84%	22%
Realtek	1,127	906	80%	23%
IDT	921	821	89%	6%
Novatek	951	580	61%	38%
Mstar	773	501	65%	39%
HiMax	776	489	63%	14%
Phison	411	252	61%	35%
CSR	377	246	65%	42%
Dialog	341	240	70%	36%
PMC Sierra	321	300	93%	27%
MegaChips	191	123	64%	33%
Semtech	158	112	71%	24%
Silicon Labs	52	47	90%	0%
Spreadtrum	45	29	64%	20%
Average Fabless (weighted with number of patent applications)			**61%**	**26%**
Average Fabless excl. Qualcomm (weighted with number of patent appl			**79%**	**19%**
ARM	4,349	2,113	49%	22%
Rambus	1,967	1,217	62%	24%
Synopsys	1,658	1,280	77%	27%
Cadence	1,606	1,438	90%	11%
Sarnoff Corp.	1,119	497	44%	2%
Mentor Graphics	613	364	59%	29%
Silicon Image	444	248	56%	23%
eMemory	195	157	81%	28%
Imagination Technologies	127	43	34%	83%
Vitesse Semiconductor	94	35	37%	5%
Sonics	107	64	60%	9%
Faraday Technology	72	40	56%	6%
IPGoal	58	39	67%	60%
Kilopass	37	28	76%	5%
Verisilicon	20	15	75%	25%
Memoir Systems	19	11	58%	47%
Sidense	13	9	69%	54%
Discretix	8	4	50%	0%
CEVA DSP	7	5	71%	0%
Dolphin	5	3	60%	0%
Chips&Media	1	-	0%	0%
Vivante Corp	1	-	0%	0%
Chips&Media	1	-	0%	0%
Average IPCore (weighted with number of patent applications)			**61%**	**20%**

A 9 Patent regressions - correlation tables

The figures included in this section of the Appendix contain pairwise-correlation matrixes from various cuts of the data. The variables *Patens filed per R&D* and *Patents granted per R&D* are not non-logarithmic.

All entries that are significant at the 5% level are marked in bold. Entries that are not significant at the 5% level are non-bold and italicized. The color-coding is based on the value of the correlation coefficient with a +1.00 being a dark green, a 0.00 being white and a -1.00 being dark read to allow for rapid visual interpretation of correlation matrixes.

Figure 38: Pairwise correlation table, all firms, 2006-2013

	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)	(13)	(14)	(15)
(1) IPCore	-														
(2) Year	- *0.01*	-													
(3) Revenue, Log	- **0.53**	**0.15**	-												
(4) R&D, Log	- **0.28**	**0.18**	**0.89**	-											
(5) RnD per Employee, Log	- *0.08*	*0.10*	**0.27**	**0.44**	-										
(6) PPE per Employee, Log	- **0.37**	*0.06*	**0.56**	**0.56**	**0.30**	-									
(7) Employees, Log	- **0.28**	**0.16**	**0.88**	**0.94**	*0.11*	**0.51**	-								
(8) Age, Log	*0.04*	**0.25**	**0.18**	**0.32**	*0.10*	**0.14**	**0.31**	-							
(9) Profit margin	- *0.11*	**0.12**	**0.16**	*0.05*	*0.00*	*0.02*	*0.06*	- **0.21**	-						
(10) Gross margin	**0.67**	*0.04*	- **0.23**	**0.13**	**0.19**	- *0.03*	*0.08*	**0.23**	*0.06*	-					
(11) Patents filed	- **0.17**	*0.09*	**0.50**	**0.50**	**0.18**	**0.32**	**0.49**	*0.09*	**0.21**	*0.08*	-				
(12) Patents granted	- **0.24**	- *0.02*	**0.58**	**0.57**	**0.20**	**0.41**	**0.56**	- *0.00*	**0.22**	*0.08*	**0.85**	-			
(13) New patent families filed	- **0.18**	*0.06*	**0.52**	**0.51**	**0.18**	**0.33**	**0.50**	*0.11*	**0.21**	*0.08*	**0.99**	**0.87**	-		
(14) Patents filed per R&D	- *0.03*	- *0.09*	- *0.04*	- **0.21**	- **0.30**	*0.06*	- *0.12*	- **0.43**	**0.16**	- *0.07*	**0.25**	**0.33**	**0.24**	-	
(15) Patents granted per R&D	- *0.09*	- **0.20**	- *0.07*	- **0.26**	- **0.34**	*0.06*	- **0.16**	- **0.47**	**0.14**	- **0.14**	*0.10*	**0.26**	*0.09*	**0.93**	-

Figure 39: Pairwise correlation table, all firms excl. Qualcomm, 2006-2013

	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)	(13)	(14)	(15)
(1) IPCore	-														
(2) Year	- *0.01*	-													
(3) Revenue, Log	- **0.52**	**0.15**	-												
(4) R&D, Log	- **0.25**	**0.18**	**0.87**	-											
(5) RnD per Employee, Log	- *0.06*	*0.10*	**0.23**	**0.42**	-										
(6) PPE per Employee, Log	- **0.35**	*0.06*	**0.53**	**0.53**	**0.27**	-									
(7) Employees, Log	- **0.25**	**0.16**	**0.86**	**0.93**	*0.06*	**0.47**	-								
(8) Age, Log	*0.06*	**0.25**	**0.14**	**0.29**	*0.09*	*0.11*	**0.28**	-							
(9) Profit margin	- *0.09*	**0.13**	*0.09*	- *0.03*	- *0.03*	- *0.03*	- *0.02*	- **0.25**	-						
(10) Gross margin	**0.69**	*0.04*	- **0.29**	*0.11*	**0.18**	- *0.05*	*0.05*	**0.22**	*0.04*	-					
(11) Patents filed	- **0.22**	*0.12*	**0.56**	**0.55**	**0.15**	**0.38**	**0.55**	- **0.16**	*0.12*	*0.01*	-				
(12) Patents granted	- **0.25**	- *0.03*	**0.54**	**0.54**	**0.14**	**0.39**	**0.53**	- **0.21**	*0.12*	- *0.01*	**0.91**	-			
(13) New patent families filed	- **0.25**	*0.08*	**0.60**	**0.59**	**0.14**	**0.39**	**0.59**	- *0.11*	*0.11*	- *0.02*	**0.96**	**0.82**	-		
(14) Patents filed per R&D	- *0.02*	- *0.10*	- *0.10*	- **0.29**	- **0.33**	*0.03*	- **0.18**	- **0.46**	**0.13**	- *0.08*	**0.44**	**0.39**	**0.40**	-	
(15) Patents granted per R&D	- *0.09*	- **0.19**	- *0.08*	- **0.28**	- **0.35**	*0.06*	- **0.17**	- **0.47**	**0.14**	- **0.14**	**0.40**	**0.44**	**0.34**	**0.94**	-

Figure 40: Pairwise correlation table, IP Core only, 2006-2013

	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)	(13)	(14)	(15)
(1) IPCore	.														
(2) Year	.	-													
(3) Revenue, Log	.	*0.15*	-												
(4) R&D, Log	.	*0.16*	**0.98**	-											
(5) RnD per Employee, Log	.	*0.09*	*0.19*	*0.21*	-										
(6) PPE per Employee, Log	.	*0.12*	**0.37**	**0.42**	**0.34**	-									
(7) Employees, Log	.	*0.12*	**0.90**	**0.91**	- **0.22**	**0.27**	-								
(8) Age, Log	.	**0.38**	**0.68**	**0.70**	*0.01*	**0.30**	**0.70**	-							
(9) Profit margin	.	*0.18*	*0.02*	- *0.08*	- *0.10*	- **0.29**	- *0.04*	- **0.24**	-						
(10) Gross margin	.	*0.21*	*0.12*	*0.18*	- *0.00*	**0.24**	*0.18*	*0.13*	*0.20*	-					
(11) Patents filed	.	*0.12*	**0.54**	**0.53**	*0.17*	*0.17*	**0.46**	**0.34**	*0.12*	**0.54**	-				
(12) Patents granted	.	- *0.01*	**0.63**	**0.63**	*0.10*	**0.24**	**0.58**	**0.37**	*0.11*	**0.53**	**0.91**	-			
(13) New patent families filed	.	*0.08*	**0.53**	**0.52**	*0.11*	*0.09*	**0.47**	**0.31**	*0.16*	**0.49**	**0.99**	**0.91**	-		
(14) Patents filed per R&D	.	- *0.08*	- **0.29**	- **0.31**	- *0.16*	*0.02*	- **0.24**	- **0.24**	*0.10*	**0.46**	**0.44**	**0.36**	**0.43**	-	
(15) Patents granted per R&D	.	- *0.12*	- **0.35**	- **0.37**	- **0.25**	*0.05*	- **0.27**	- **0.30**	*0.13*	**0.43**	**0.32**	**0.31**	**0.31**	**0.95**	-

Figure 41: Pairwise correlation table, Fabless only (incl. Qualc.), 2006-2013

	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)	(13)	(14)	(15)
(1) IPCore	.														
(2) Year	.	-													
(3) Revenue, Log	.	**0.19**	-												
(4) R&D, Log	.	**0.19**	**0.88**	-											
(5) RnD per Employee, Log	.	*0.11*	**0.34**	**0.58**	-										
(6) PPE per Employee, Log	.	*0.02*	**0.53**	**0.57**	**0.26**	-									
(7) Employees, Log	.	**0.19**	**0.90**	**0.96**	**0.32**	**0.57**	-								
(8) Age, Log	.	**0.21**	*0.04*	**0.21**	**0.16**	*0.11*	**0.19**	-							
(9) Profit margin	.	*0.09*	**0.19**	*0.08*	*0.07*	*0.15*	*0.07*	- **0.20**	-						
(10) Gross margin	.	- *0.00*	**0.24**	**0.55**	**0.53**	**0.36**	**0.45**	**0.32**	**0.16**	-					
(11) Patents filed	.	*0.10*	**0.62**	**0.54**	**0.22**	**0.35**	**0.56**	*0.10*	**0.25**	**0.29**	-				
(12) Patents granted	.	- *0.03*	**0.66**	**0.60**	**0.25**	**0.44**	**0.61**	- *0.02*	**0.25**	**0.34**	**0.84**	-			
(13) New patent families filed	.	*0.07*	**0.63**	**0.55**	**0.22**	**0.36**	**0.57**	*0.12*	**0.25**	**0.29**	**0.99**	**0.87**	-		
(14) Patents filed per R&D	.	- *0.11*	*0.09*	- **0.18**	- **0.42**	*0.07*	- *0.06*	- **0.52**	**0.19**	- **0.33**	**0.29**	**0.40**	**0.28**	-	
(15) Patents granted per R&D	.	- **0.24**	- *0.02*	- **0.26**	- **0.43**	*0.02*	- **0.15**	- **0.53**	*0.14*	- **0.32**	*0.08*	**0.27**	*0.07*	**0.93**	-

A 10 Patent regressions - variable descriptions

Table 30: Regression variable descriptions and sources

Variable	Description	Source
Patents filed per R&D, Log	The decadic logarithm of the number of patent applications filed in the US by a given company as identified via DocDB database divided by the firm-wide R&D expenditure in million 2005 USD plus one	Patstat, Orbis
IPCore	Dummy variable capturing whether a company deals in technology (IP Cores, coding "1") or in products (fabless, coding "0")	Gartner, IC Insight
Year	The calendar year of the firm-year observation	Orbis
R&D, Log	The decadic logarithm of the total firm-wide R&D expenditure in thousand 2005 USD	Orbis
RnD per Employee, Log	The decadic logarithm of the total firm-wide R&D expenditure in thousand 2005 USD divided by the number of total employee	Orbis
PPE per Employee, Log	The decadic logarithm of the total firm-wide tangible assets (property, plant, equipment - PPE) in thousand 2005 USD divided by the number of total employee	Orbis
Employees, Log	The total number of employees	Orbis
Age, Log	The decadic logarithm of the firm age as computed by year of observation minus year of inception of the firm	Orbis, company homepages

A 11 Patent regressions - backup regressions

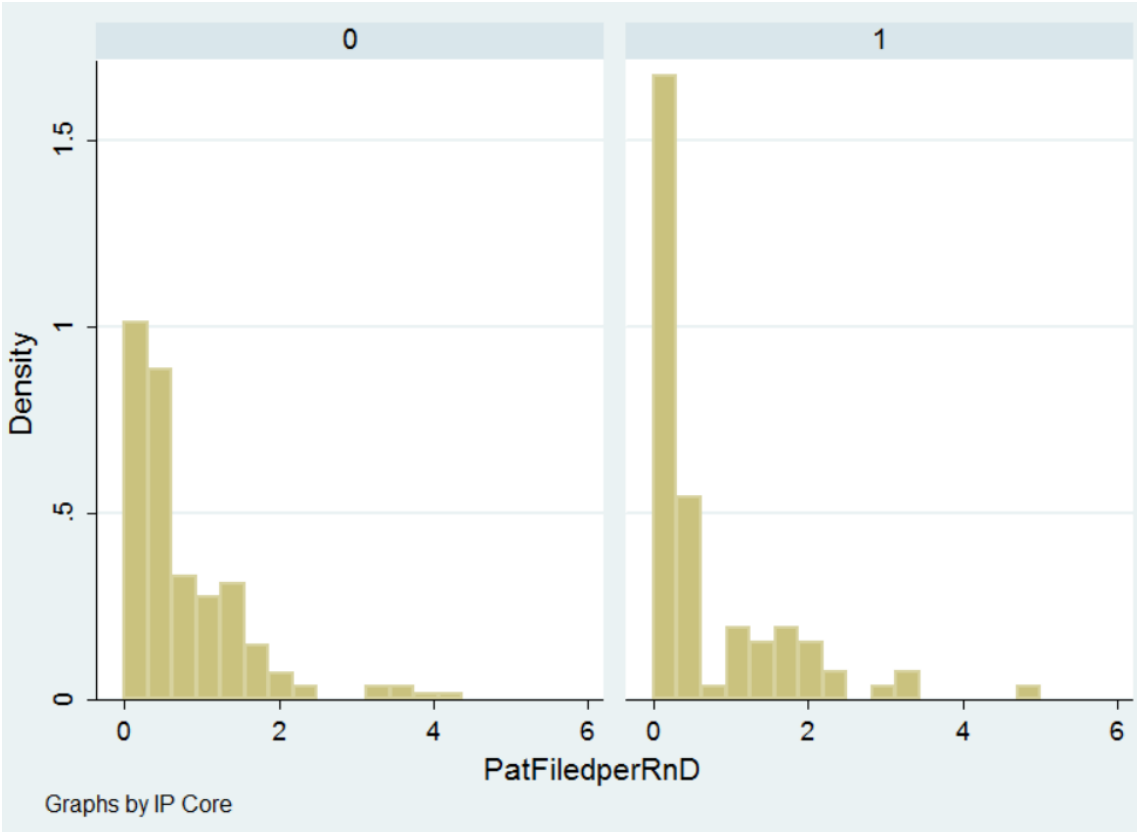

Figure 42: Histogram of patenting intensity for IP Core (right side) and Fabless (left side) 2005-2013

	Observations Fabless	Mean Fabless	Observations IP Core	Mean IP Core	p-Value
All Years	*173*	0.78	*82*	0.71	**0.58**
All Years, no EDA	*173*	0.78	*58*	0.88	**0.50**
All Years, no Qualcomm	*165*	0.75	*82*	0.71	**0.76**
Only 2005	*10*	0.73	*3*	0.08	**0.00**
Only 2006	*19*	0.92	*10*	0.84	**0.83**
Only 2007	*19*	0.90	*10*	0.93	**0.95**
Only 2008	*19*	0.89	*10*	0.92	**0.95**
Only 2009	*21*	0.85	*10*	0.77	**0.80**
Only 2010	*22*	0.70	*10*	0.67	**0.93**
Only 2011	*22*	0.69	*10*	0.52	**0.50**
Only 2012	*22*	0.68	*10*	0.73	**0.88**
Only 2013	*19*	0.66	*9*	0.48	**0.45**

Figure 43: Two-sided t-tests assuming unequal variances for patenting intensities of Fabless vs. IP Core companies, patenting intensity not log transformed

Patenting intensity estimates
Panel data set of 31 companies excl. Qualcomm (21 fabless, 10 IP Core) 2005 - 2013
US patents only, Clustured Std Err on Firm level
247 observations

Variable Name	Model 1	Model 2	Model 3	Model 4
Dummy for IP Cores	-0.05	-0.02	0.04	0.04
Log R&D (2005)	**-0.09***			
Log R&D per employee (2005)		**-0.32****	**-0.39*****	**-0.35*****
Log PPE (2005) per employee		0.13	0.13	0.13
Log firm size (employees)		-0.09	-0.03	-0.01
Year		0	0	0
Log firm age				**-0.3*****
Dummy EDA companies			-0.18	-0.12
Constant	**0.66*****	6.27	7.64	-4.26
F	2.34	2.92	4.43	10.20
Prob>F	0.11	0.03	0.00	0.00
R_sq	0.08	0.19	0.24	0.37
Observations	247	247	247	247

Signficance levels: *** p<0.01, ** p<0.05, * p<0.10

Figure 44: OLS regression results using clustered standard errors on firm-level according to Equation 2; Excluding Qualcomm

Variable Name	Fixed Effects Fabless + IP Core	Random Effects Fabless + IP Core
Log R&D ($2005)		
Log R&D per employee ($2005)	**-0.29*****	**-0.28*****
Log PPE ($2005) per employee	0.01	0.02
Log firm size (employees)	**-0.15*****	**-0.09****
Year	**0.01****	**0.01***
Log firm age	**-0.47*****	**-0.36*****
Dummy Qualcomm	N/A	**0.38*****
Dummy EDA companies	N/A	-0.02
Constant	**-19.66****	-9.54
R_sq (within)	0.31	0.30
F	19.22	101.26
Prob>F	0.00	0.00
Observations	255	255

Signficance levels: *** p<0.01, ** p<0.05, * p<0.10

Figure 45: Hausman test of Fixed effects and Random effects models, regression results

```
. hausman fixed ., sigmamore

                 ---- Coefficients ----
                |      (b)          (B)            (b-B)     sqrt(diag(V_b-V_B))
                |    fixed            .       Difference          S.E.
----------------+----------------------------------------------------------------
           Year |   .0104341     .0054005       .0050336        .0031851
RnDperEmpl~g    |  -.2934323    -.2770928      -.0163395        .0173496
PPEperEmpl~g    |    .014881     .0166024      -.0017214        .0076897
        EmplLog |  -.1560251    -.0936913      -.0623338        .0327491
         AgeLog |  -.4660158    -.3555584      -.1104574        .1086037
------------------------------------------------------------------------------
                           b = consistent under Ho and Ha; obtained from xtreg
            B = inconsistent under Ha, efficient under Ho; obtained from xtreg

    Test:  Ho:  difference in coefficients not systematic

                  chi2(5) = (b-B)'[(V_b-V_B)^(-1)](b-B)
                          =       11.53
                Prob>chi2 =      0.0418
```

Figure 46: Hausman test of Fixed effects and Random effects models, STATA output

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