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Advanced Control Techniques of Impedance Source Inverters for Distributed Generation Applications

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To my wife Noura and my little son Elarion

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Abstract

Distributed generation systems based on renewable energy sources, such as photovoltaic, wind power, fuel cells, and etc. have remarkably increased world wide as alternatives to the conventional generation systems. The primary energy of the aforementioned sources widely vary in nature, where it depends on the temperature, irradiation level, wind speed, stored Hydrogen, etc. Therefore, power electronic interfaces as power conditioning units are required. These units must assure output power with high quality. In this thesis, the newly proposed impedance source inverters are used to substitute the conventional two-stage inverters (dc-dc converter and voltage source inverter). It is confirmed that the proposed topologies come with higher efficiency and reliability as well as lower cost and complexity.

In distributed generation applications, the control algorithm play a crucial role in stabilizing the whole system under normal operation and fault conditions. This thesis aims to examine some of the advanced control techniques for the impedance source inverters used in such applications. In order to improve the output voltage quality, the proportional-resonant controller is designed instead of the classical PI controller. In addition, a main part of this work deals with the application of direct model predictive control (MPC) with the impedance source inverters. First, direct MPC with long horizon prediction is introduced as a current controller. As a next step, MPC is examined as a voltage controller when the impedance source inverters are connected with linear/nonlinear load via an intermediate LC filter. Finally, a variable switching point predictive current control strategy is proposed and compared with the classical MPC schemes. It is proven that the performance of the proposed control techniques outperforms the ones of the conventional linear controllers for the same application.

Zusammenfassung

Dezentrale Energieerzeugungssysteme auf Basis erneuerbarer Energiequellen wie z.B. Photovoltaik, Windenergie und Brennstoffzellenhaben als attraktive Alternative zu konventionellen Systemen weltweit deutlich zugenommen. Die Primärenergie der genannten Quellen variiert stark, da sie von Natureinflüssen wie Temperatur, Bestrahlung, Windgeschwindigkeit, gespeichertem Wasserstoff usw. abhängen. Deshalb werden Leistungselektronische Schaltungen als Power-Conditioning-Einheiten benötigt. Diese Einheiten müssen Ausgangsleistung hoher Qualität sicherstellen. In dieser Arbeit wird der Impedance Source Inverter verwendet, um die konventionellen zweistufigen Wechselrichter (DC-DC-Wandler und Wechselrichter mit Zwischenkreisspannung) zu ersetzen. Es wird gezeigt, dass die vorgeschlagenen Topologien mit höherer Effizienz und Zuverlässigkeit arbeiten, sowie geringeren Kosten und Komplexität aufweisen.

Bei dezentralen Energieerzeugungssystemen spielen Regelungsalgorithmen eine entscheidende Rolle zur Stabilisierung des Gesamtsystems unter üblichen Betriebs- und Störbedingungen. Das Ziel dieser Dissertation ist es, hochentwickelte Regelungsalgorithmen einschlieich Model Predictive Control für Impedance Source Inverter, im Hinblick auf die Systemleistung und Effizienz zu untersuchen. Zunächst wird direktes MPC mit langem Prädiktionshorizont als Stromregler eingeführt. Im nächstem Schritt wird MPC als Spannungsregler untersucht, wenn der Impedance Source Inverter über einen LC-Filter mit linearer / nichtlinearer Last verbunden ist. Schlieich wird eine prädiktive Stromregelungsstrategie mit variablem Schaltzeitpunkt vorgeschlagen und mit den klassischen MPC-Schemata verglichen. Es wird gezeigt, dass mit den vorgeschlagenen Regelungsalgorithmen die Performanz von konventionellen Linearregler für dieselbe Anwendung übertroffen wird.

Table of Contents

CHAPTER 1

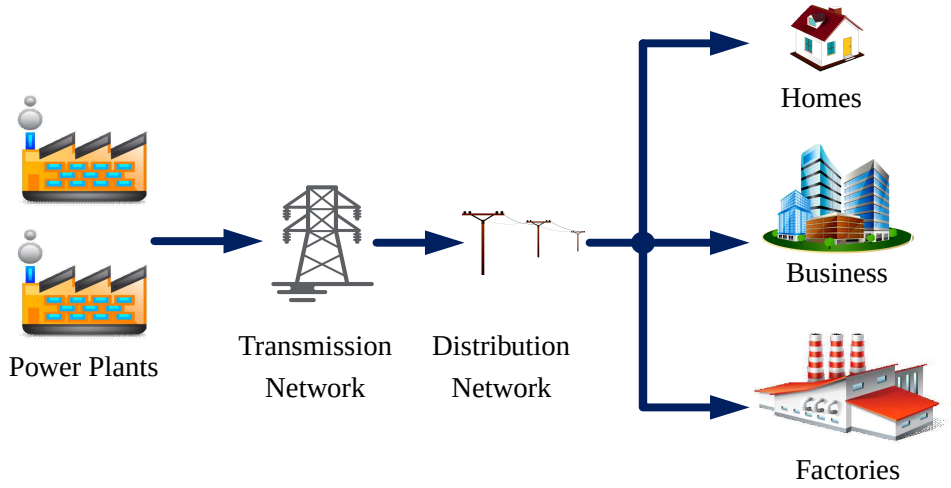
Introduction

1.1 Overview and Motivation

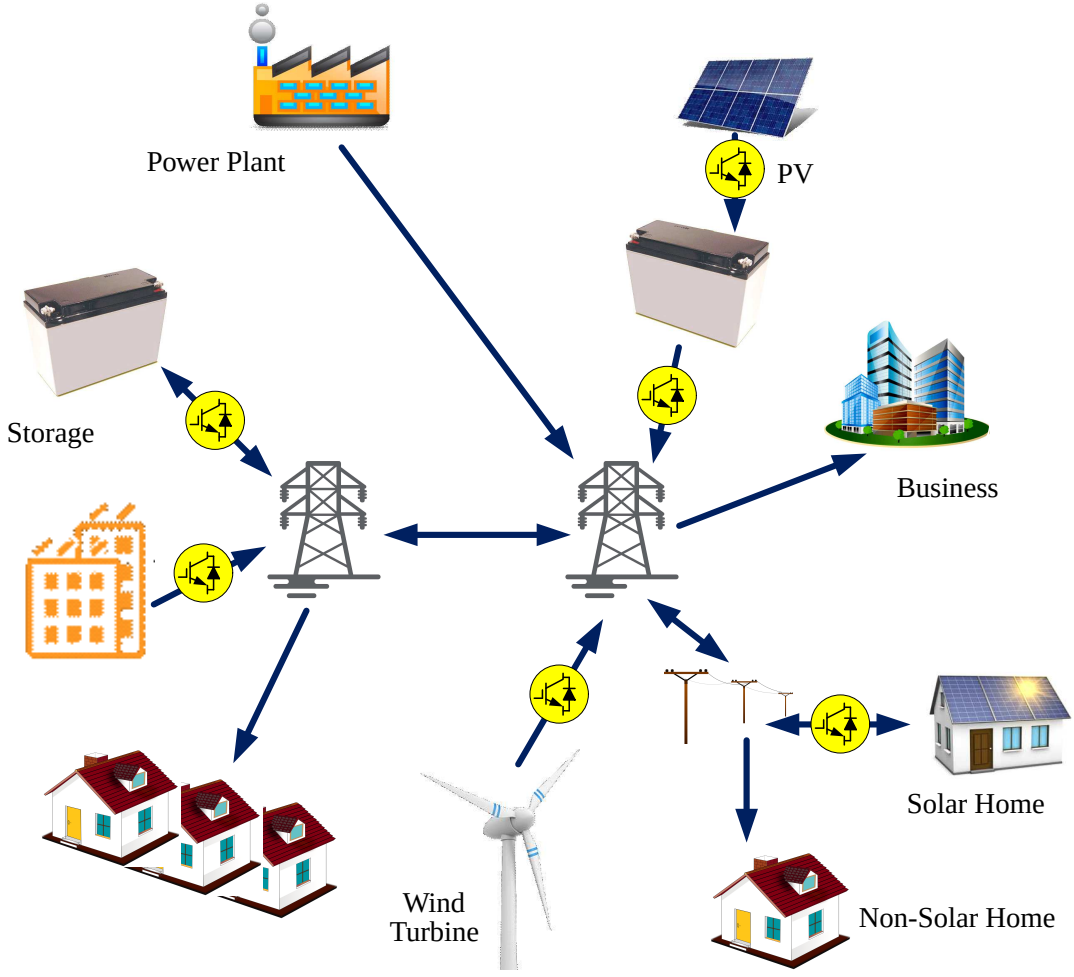
Nowadays, power electronic converters are considered as the enabling technologies necessary to realize many benefits of distributed generation (DG) systems. In order to increase the output power quality and the reliability of the generation systems, modern control algorithms are required to be proposed. This dissertation aims to investigate some of these techniques for the newly proposed family of impedance source inverters utilized in DG applications.

In recent years, DG systems based on renewable energy sources (RESs), such as photovoltaic (PV), wind power, and fuel cells (FC), have remarkably increased world wide as alternatives to the conventional generation systems [1–5]. The main reason is the huge increase of the energy demand in addition to the increased concern about global environmental problems. The DG systems are able to generate reliable, high quality, and low-cost electrical power because it saves the cost of the grid expansion and line losses [6–8]. DG technologies yield power in capacities that range from a fraction of a kilowatt [kW] to about 100 megawatts [MW]. Figure 1.1 shows the structure of both the conventional central power generation and DG system. As can be observed, unlike the centralized generation systems, the DG can make the whole grid more secure as there is less reliance on any particular part of the system, i.e. when a failure occurs in one energy source, the others can be used to fill the gap without shutting down the whole system. Moreover, being based on RESs, the DG systems are considered as environment friendly.

The main characteristic of RESs is that the primary energy widely varies in nature, where it depends on the temperature, irradiation level, wind speed, stored hydrogen, etc. Therefore, power electronic interfaces functioning as power conditioning units are required. These units must assure an output power with high quality that is able to cope with wide input voltage variations and meet the required IEEE standards [9]. The cost of power electronic systems represents a substantial portion of the overall installation cost of the DG applications. Thus,



(a) Central power generation.



(b) Distributed generation.

Figure 1.1: Power generation systems.

these systems should work with a high efficiency in order to reduce the energy cost.

Voltage source inverters (VSIs) have been extensively used in various power electronic applications, including among others, distributed generations, energy-storage systems, and uninterruptable power supplies (UPS) [10, 11]. However, VSIs feature some limitations and constraints [12]. First, the ac output voltage is lower than the input dc voltage, and for that reason they can be characterized as buck converters. In order to boost the input dc voltage to the desired dc-link voltage, an additional dc-dc boost converter is needed. Adding the dc-dc boost converter increases the complexity of the controller, decreases the overall efficiency, and increases the overall cost of the inverter [13–16]. Moreover, to avoid a shoot through (i.e. a short circuit) between the upper and the lower dc-link rails, a dead time is inserted between the pulses which in turn increases the distortion in the output current/voltage waveforms.

To overcome the aforementioned limitations of the VSIs, the impedance source inverters (ISIs) were proposed. The first topology of the ISIs is Z-source inverter (ZSI) which was proposed in 2002 as an alternative to the conventional VSI. The ZSI fulfills the buck-boost function in a single-stage converter by utilizing a Z-source network which consists of two identical inductors, two identical capacitors, and a diode [12, 17]. By employing an extra switching state, called *shoot-through state*, the ZSI can boost the input dc voltage to the desired dc-link voltage [18]. This in turn increases the inverter operating range and improves its reliability since the mis-gating resulting from electromagnetic interference (EMI) does not affect its operation. In comparison with the traditional two-stage inverter (consisting of a dc-dc boost converter and a voltage source inverter), the ZSI comes with a better efficiency, simpler design, and reduced cost [19, 20].

The quasi-Z-source inverter (qZSI) was presented as an improved version of the classical ZSI [21]. It has many additional advantages such as continuous input current and joint earthing of the dc source and the dc-link bus. Moreover, the voltage of one of the quasi-Z-source network capacitors is significantly reduced resulting in a smaller passive components size [22]. Taking into account the aforementioned characteristics, the qZSI can be considered as an attractive candidate for several DG applications [23–26]. Later on, other advanced topologies of ISIs have been proposed in order to improve the overall performance and efficiency, see e.g. [27–32]. Although the efficiency of the latter might be improved, the inverter circuit is more complicated which requires advanced and sophisticated control algorithms. An experimentally-based comparison between the conventional two-stage inverter and qZSI is required to show the latter's advantages for the DG applications.

In the last few years, many control algorithms have been presented and implemented with different topologies of the ISIs, most notably ZSI and qZSI. Most of these control methods are based on conventional linear control schemes that are combined with pulse width modulation (PWM) techniques [24, 25, 33–38].

Using conventional linear control techniques such as proportional-integral (PI) controllers to control the ISIs appears to be a challenging task. Although the ISIs are considered as single-stage buck-boost converters, they require two separate controllers for both sides. On the dc side of the converter, the dc-link voltage is indirectly controlled by adjusting the capacitor voltage (and the inductor current when needed) of the impedance network. Because of its natural form as a pulsated voltage, the dc-link voltage can not be directly controlled. At the same time, the

output current/voltage on the ac side has to be controlled [24,35–37]. This necessitates the presence of multiple control loops (an outer voltage control loop and an inner current control loop) which during transients may start interacting with each other. This implies that the controller parameters have to be carefully tuned in order to avoid a significant limitation in the system performance in terms of bandwidth, i.e. a considerable engineering effort is required [24, 25]. In addition, the dc side of the qZSI exhibits a nonminimum phase characteristic which requires much attention in the controller design in order to minimize its effect on the converter operation at different operating points.

As an alternative, nonlinear control algorithms such as sliding mode control [39, 40], fuzzy control [41], and neural network control [42, 43] have been applied to ZSI/qZSI. In comparison with the traditional proportional-integral (PI) based controllers, these algorithms exhibit fast dynamic behavior at the expense of the increased design complexity.

A control strategy that allows to significantly reduce the control effort involved in the design stage is model predictive control (MPC) [44]. MPC can handle multiple—and frequently competing—objectives simultaneously by incorporating the different control loops in one computational stage. Moreover, MPC can successfully tackle constraints that can be explicitly imposed on the variables of concern and thus allows the system to operate at its physical limits. Thanks to these characteristics, MPC is particularly effective when multiple-input multiple-output (MIMO) systems with complex dynamics are considered, such as many power electronic systems [45, 46]. To further simplify the controller design, MPC in power electronics is usually implemented as a direct control strategy (also known as finite control set MPC—FCS-MPC), i.e. the switches of the converter are directly manipulated without requiring a modulator [47–49]. As a result, its implementation is considered to be straightforward, as verified by numerous works published in the last decade [47, 50–56].

Motivated by the above-mentioned advantages of direct MPC, one of the main objectives of this dissertation is to introduce different direct MPC strategies for one of the ISIs topologies, namely qZSI. The goals of applying these advanced techniques are to overcome the previously stated problems of the conventional linear controllers and to improve the converter's overall performance.

1.2 Dissertation Contributions

Considering the advantages of the qZSI as an attractive example of the ISIs, this dissertation aims to propose some advanced control techniques that can comply with the DG requirements. The main contributions of the dissertation can be divided into two main parts as follows. The first part is concerned with conventional inverters and control as follows.

- In order to evaluate the newly proposed qZSI, a thorough experimentally-based comparison with the conventional two-stage inverter is carried out. The comparison includes the analysis of the voltage stress on the inverter switches, required active and passive components, steady-state and transient performance, and inverter efficiency. In this comparison, the conventional PI-based controllers are designed for both inverters.

- In UPS systems, regardless the load type, linear or nonlinear, a high quality output voltage

is desirable. However, the nonlinear output current, introduced by nonlinear loads, results in a highly distorted output voltage. This is typically the case when PI control is utilized. To improve the quality of the output voltage, a proportional-resonant (PR) controller is designed which compensates for selected low-order harmonics. Thus, a regulated sinusoidal output voltage is obtained not only for linear loads, but also for nonlinear loads. In this dissertation, the design and digital implementation of the PR controller are presented in detail.

The second part of the dissertation contributions deals with the application of direct MPC with the qZSI by considering the following topics.

- Direct MPC–as a current controller–is designed for the qZSI connected with an RL load. To improve the closed-loop performance of the converter, a long prediction horizon is implemented. However, the underlying optimization problem may become computationally intractable because of the substantial increase in the computational power demands, which in turn would prevent the implementation of the control strategy in real time. To overcome this and to solve the problem in a computationally efficient manner, a branch-and-bound strategy is used along with a move blocking scheme. These techniques facilitate the implementation of a long-horizon MPC in real time. It is proved that the performance of the long-horizon MPC outperforms the performance of both the classical single-step MPC and the conventional PI control.

- Direct MPC–as a voltage controller–for qZSI connected with linear/nonlinear loads via an intermediate LC filter is designed. The proposed MPC strategy simultaneously controls both sides of the converter by controlling the output voltage of the LC filter and the capacitor voltage and inductor current on the dc side. To address time-varying and unknown loads as well as to reduce the number of measurement sensors required, a Kalman observer is added to estimate the load current which appears to be immune to noise. As it is shown, the proposed algorithm represents an attractive alternative for the conventional linear controllers.

- A variable switching point predictive current control (VSP^{2}CC) strategy for the qZSI is proposed and implemented. Unlike the previously presented MPC strategies for the ZSI/qZSI, with the proposed control scheme, the optimal switch position can be changed at any time instant within the sampling interval. By doing so, the shoot-through switching states can be applied for a shorter period of time than the sampling interval. This results in lower output and inductor currents ripples. It is concluded that the proposed method results in lower inductor current ripples and output current THD compared to the conventional MPC when operating the converter at the same switching frequency.

All the proposed control methods in this dissertation are experimentally validated in the laboratory based on a low-cost and a low-power field programmable gate array (FPGA) Cyclone III-EP3C40Q240C8. Moreover, only with minor modifications, all control techniques proposed for the qZSI can be applied to other ISI topologies.

1.3 Dissertation Organization

The upcoming chapters of this dissertation are categorized into four main parts as follows. Part I includes chapter 2 as a general background on the system under investigation. Firstly, it addresses the different topologies of the ISIs which have been widely used. In addition, it introduces the utilized modulation techniques with the ISIs including sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) strategies. Then, the conventional linear control and MPC techniques are introduced.

Part II includes two chapters as follows. A thorough comparison is done in chapter 3 between the qZSI and the conventional two-stage inverter. Chapter 4 proposes the design and the digital implementation of the proportional-resonant (PR) controller for the qZSI that can be used with UPS applications.

Chapters 5, 6, and 7 compose the third part of this dissertation. These chapters present the application of different MPC algorithms with the qZSI. In chapter 5, the MPC with long prediction horizon is introduced as a current controller, where the qZSI is connected with an RL load. Chapter 6 presents the MPC as a voltage controller for the qZSI connected with linear/nonlinear loads via an intermediate LC filter. The variable switching point predictive current control (VSP^{2}CC) is introduced and discussed with the qZSI in chapter 7.

Chapter 8 provides a brief summary of the whole dissertation and discusses some extended ideas that can be carried out in the future. Finally, the appendices are introduced in part IV.

Part I

Theoretical Background

CHAPTER 2

Theoretical Background

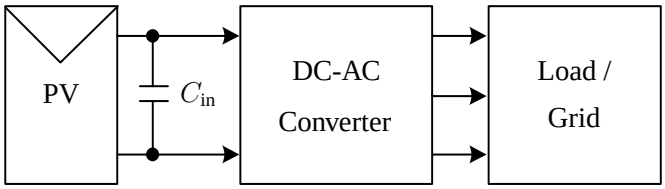
This chapter introduces the impedance source inverters as attractive alternatives to the conventional voltage source inverters (VSIs). First, the limitations of the conventional VSIs will be discussed. Then, the different topologies of impedance source inverters will be presented. Moreover, the modified modulation techniques for the proposed inverters will be introduced and compared with each other. Finally, the conventional control and the advanced control strategies for the impedance source inverters will be highlighted.

2.1 Impedance Source Inverters

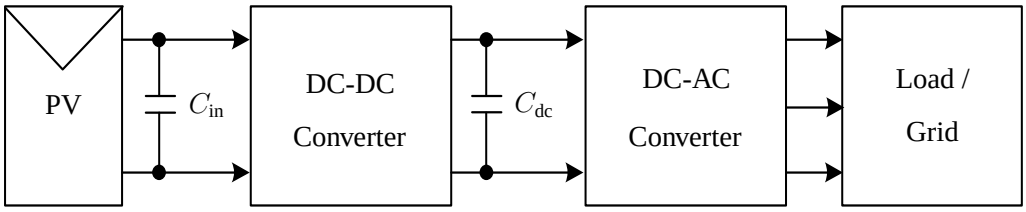
Modern DG systems employ several power electronic converters in order to provide ac power to loads/grid [10, 11]. Based on the number of power processing stages, converters in DG systems (i.e. PV) can be divided into two main types; single- and two-stage converters [57], shown in Figure 2.1. In the first configuration, the dc-ac converter, commonly VSI shown in Figure 2.2(a), performs all the control functions, i.e. maximum power point tracking (MPPT) and/or current/voltage control. However, VSIs feature some limitations and constraints [12]. First, the ac output voltage is lower than the input dc voltage, and for that they can be characterized as buck converters. Moreover, to avoid a shoot through (i.e. a short circuit) between the upper and the lower dc-link rails, a dead time is inserted between the pulses which in turn increases the distortion in the output current/voltage waveforms. In order to boost the input dc voltage to the desired dc-link voltage, an additional dc-dc boost converter is needed as shown in Figures 2.1(b) and 2.2(b). However, the dc-dc boost converter increases the complexity of the controller, decreases the overall efficiency, and increases the overall cost of the inverter [13–16].

2.1.1 Z-Source Inverter

As alternative to the traditional two-stage inverters, ISIs have been paid much attention from the researchers in the area of power electronics [58]. These inverters are considered as one-stage

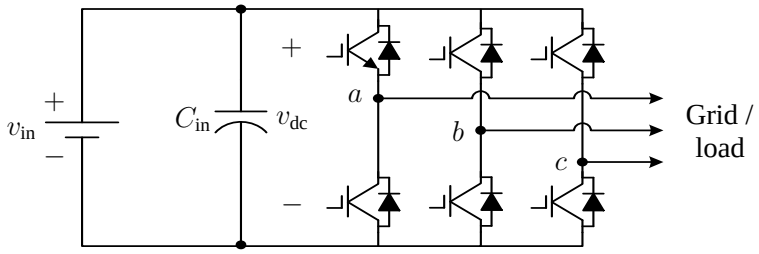


(a) Single-stage converter.

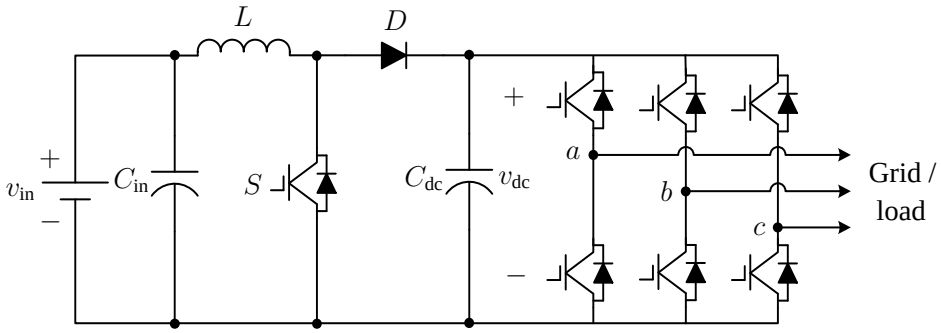


(b) Two-stage converter.

Figure 2.1: PV system configuration.



(a) Voltage source inverter



(b) Two-stage inverter

Figure 2.2: Single- and two-stage inverters for DG applications.

buck-boost converters. The first topology of the impedance-source inverters is called Z-source inverter (ZSI) displayed in Figure 2.3 [12, 59, 60]. By using an impedance network, consisting of two capacitors and two inductors, and a diode, and including an extra switching state, called *shoot-through state*, the input dc voltage can be boosted to the desired dc-link voltage. The shoot-through state is carried out during a part of the zero state time. The output voltage during the shoot-through state is still zero; therefore, it does not affect the operation of the PWM inverter. It is well known that VSI has eight switching states; six active states and two zero states. However, the ZSI has nine switching states; six active states, two zero states, and the

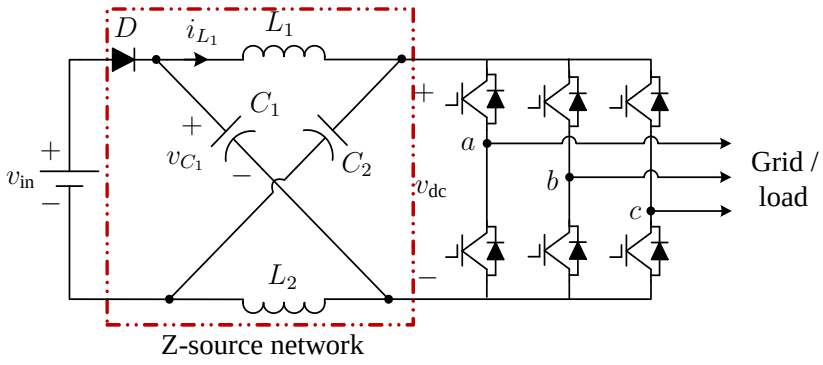


Figure 2.3: The classical Z-source inverter topology.

shoot-through state.

Considering these characteristics, the reliability of the inverter is notably improved because the shoot-through resulted from mis-gating can no longer damage the inverter devices. The approach of Z-source network can be used for all power conversion methods, namely dc-ac, ac-dc, ac-ac, and dc-dc conversion.

ZSI has been tested with different DG applications; such as PV [17, 61, 62]. In these studies, the one-stage ZSI successfully replaces the traditional two-stage inverter, where the ZSI can boost dc voltage when needed, perform MPPT, and interface the PV with the grid. In [63], the ZSI is used with electric vehicle (EV) applications as a bidirectional one-stage converter based on FC and battery sources.

At steady-state operation, the voltages of the capacitors C_1 and C_2, v_{C_1} and v_{C_2}, respectively, are deduced as follows (assuming that $C_1 = C_2$).

$$v_{C_1} = v_{C_2} = \frac{1-d}{1-2d}\, v_{\text{in}}\,, \tag{2.1}$$

where d is the shoot-through duty cycle and i_{load} represents the input current to the inverter bridge. Moreover, the peak value of the dc-link voltage during the non-shoot-through period is given by

$$\hat{v}_{\text{dc}} = 2v_{C_1} - v_{\text{in}} = \frac{1}{1-2d}\, v_{\text{in}} = b\, v_{\text{in}}\,, \tag{2.2}$$

where $b \geq 1$ is the boost factor resulting from the shoot-through period.

2.1.2 Switched Inductor Z-source Inverter

Applying switched-capacitor or switched-inductor or hybrid switched-capacitor/inductor structures to dc-dc conversion provides the high boost in cascade and transformerless structures with high efficiency and high power density [64]. In order to increase the boost factor of the ZSI, the concept of the switched inductor (SL) technique is integrated into the Z-source network. This in turn results in producing a higher dc-link voltage for the main power circuit from a very low input dc voltage. Consequently, a new switched inductor Z-source inverter (SL ZSI) is obtained as depicted in Figure 2.4 [65].

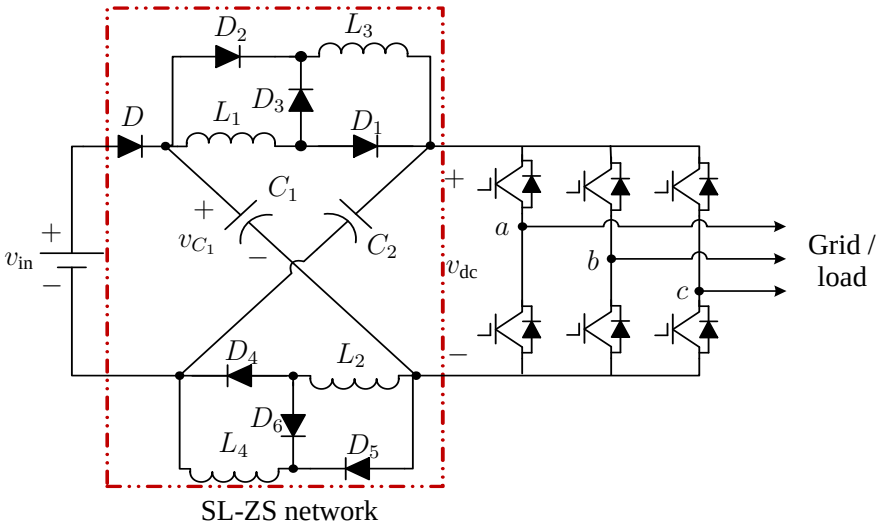


Figure 2.4: The switched inductor Z-source inverter.

In steady state, the average capacitor voltages and the peak dc-link voltage (during the non-shoot-through period) are calculated by

$$v_{C_1} = v_{C_2} = \frac{1-d}{1-3d}\, v_{\text{in}}\,, \quad \hat{v}_{\text{dc}} = 2v_{C_1} - v_{\text{in}} = \frac{1+d}{1-3d}\, v_{\text{in}} \tag{2.3}$$

From (2.3), it is pointed out that the boost factor highly increases and the capacitor voltage significantly decreases in comparison with the classical ZSI (see (2.2) and (2.3)). This means that by utilizing a very short time for the shoot-through state, high voltage conversion ratios can be obtained. However, the main drawbacks of this topology are the high voltage stress across the switches and the very high inrush current [60, 66].

Due to the drawbacks of the SL ZSI topology, the improved SL ZSI is presented. This topology has the same components of SL ZSI, but the SL Z-source network is moved to be in series with the three-phase inverter as shown in Figure 2.5 [60]. The improved SL ZSI has the same boost factor of the SL ZSI in addition to high reduction in the voltage stress across the switches and in the inrush current. The steady state equations for this topology are defined as follows.

$$v_{C_1} = v_{C_2} = \frac{2d}{1-3d}\, v_{\text{in}}\,, \quad \hat{v}_{\text{dc}} = 2v_{C_1} - v_{\text{in}} = \frac{1+d}{1-3d}\, v_{\text{in}} \tag{2.4}$$

Nonetheless, in order to achieve some control algorithms such as the MPPT for PV, the output current of the PV should be continuous [67], otherwise an input LC filter is required. Because of the diode D located in the input circuit of the ZSI, SL ZSI, and improved SL ZSI, the input current is discontinuous. This leads to a non-efficient power tracking and short PV life time.

2.1.3 Quasi-Z-Source Inverter

The quasi-Z-source inverter (qZSI), shown in Figure 2.6, was presented as an improved version of the classical ZSI [21]. It has many additional advantages such as continuous input current and

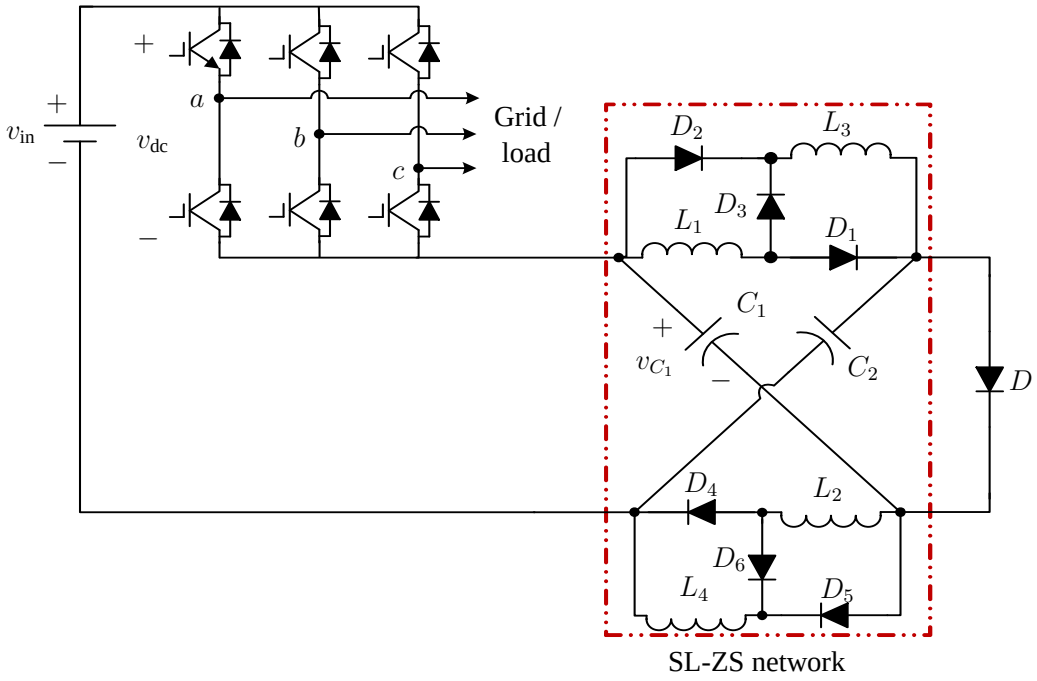


Figure 2.5: The improved switched inductor Z-source inverter.

joint earthing of the dc source and the dc-link bus. Moreover, the voltage of one of the quasi-Z-source network capacitors is significantly reduced resulting in a smaller passive components size [22, 24]. Taking into account the aforementioned characteristics as well as its enhanced efficiency, reduced cost, and simpler design [19, 20], the qZSI can be considered as an attractive candidate for several DG applications, including PV systems [25].

In steady state, the capacitor voltages and the peak dc-link voltage are given by

$$v_{C_1} = \frac{1-d}{1-2d}\, v_{\text{in}}\,, \quad v_{C_2} = \frac{d}{1-2d}\, v_{\text{in}}\,, \quad \hat{v}_{\text{dc}} = v_{C_1} + v_{C_2} = \frac{1}{1-2d}\, v_{\text{in}} \tag{2.5}$$

As can be noted from (2.5), the qZSI has the same boost factor of the ZSI. However, the capacitor voltage v_{C_2} is highly reduced. The only limitation of the qZSI is that the boost factor is low in comparison with the previously mentioned topologies, such as SL ZSI and improved SL ZSI (compare (2.5), (2.3), and (2.4)).

In order to increase the boost factor of the qZSI, an SL cell is integrated into its impedance network. The SL cell, which consists of two inductors and three diodes, replaces the output side inductor as illustrated in Figure 2.7. Thus, the switched inductor quasi-Z-source inverter (SL qZSI) has been obtained [28]. In steady state, the following equations are obtained.

$$v_{C_1} = \frac{1-d}{1-2d-d^2}\, v_{\text{in}}\,, \quad v_{C_2} = \frac{2d}{1-2d-d^2}\, v_{\text{in}}, \tag{2.6a}$$

$$\hat{v}_{\text{dc}} = v_{C_1} + v_{C_2} = \frac{1+d}{1-2d-d^2}\, v_{\text{in}} \tag{2.6b}$$

As can be seen, the SL qZSI has the same advantages of the qZSI along with higher boost

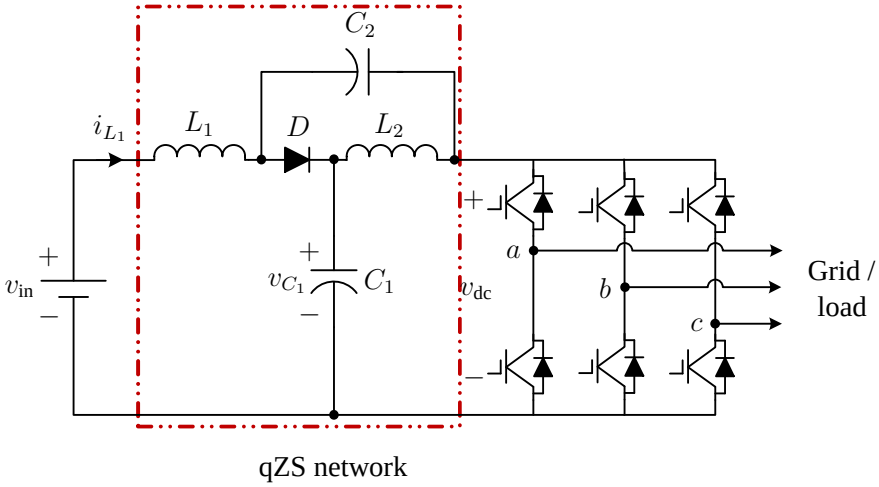


Figure 2.6: The quasi-Z-source inverter.

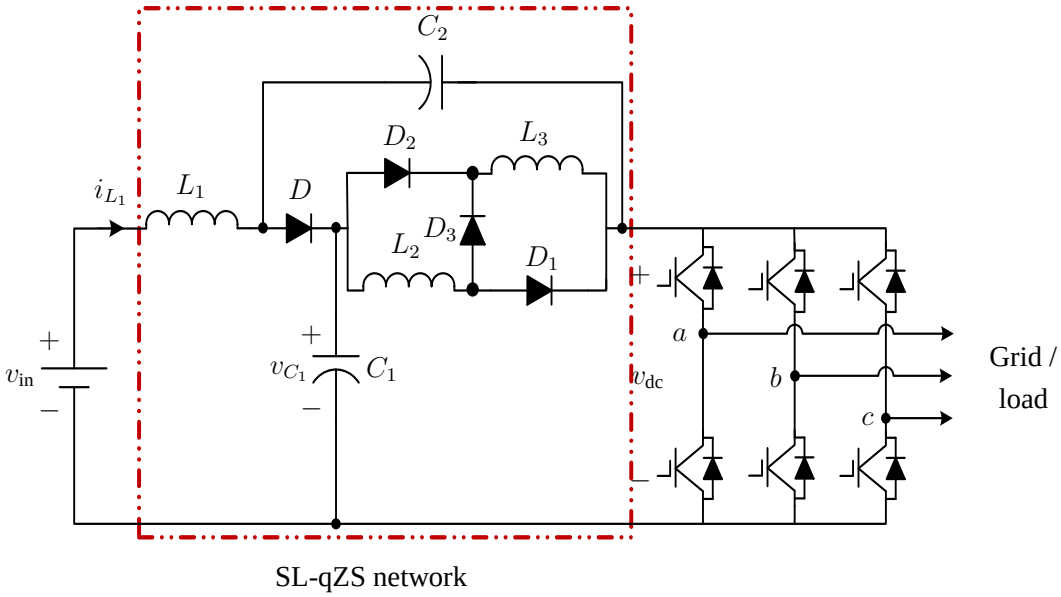


Figure 2.7: The switched inductor quasi-Z-source inverter.

factor; therefore, a wide range of voltage gain can be achieved to fulfill the requirements of the DG-based RES applications.

Based on the same operation principle, other topologies of the ISI have been proposed to increase the boost factor and/or the overall efficiency, see [27–32].

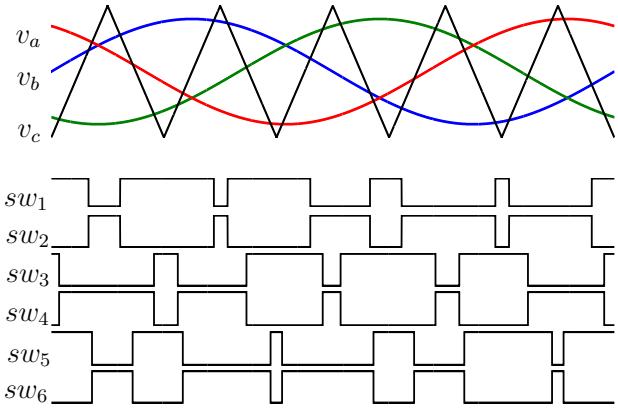
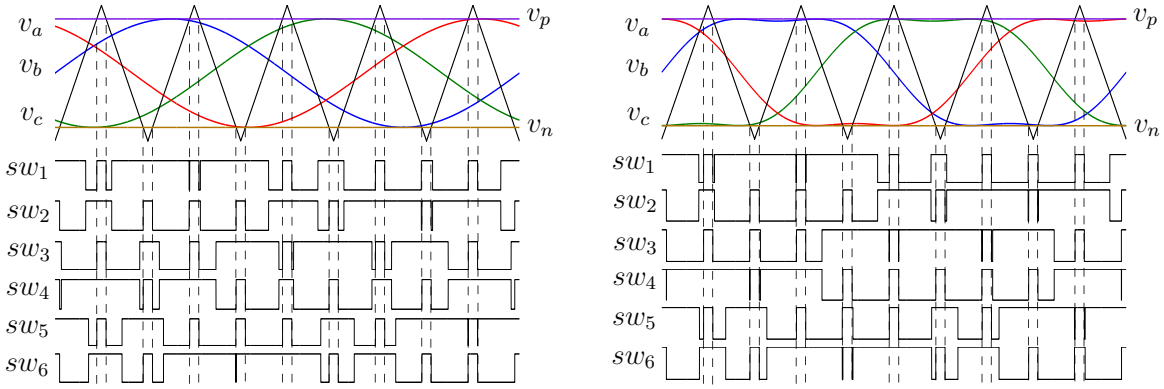


Figure 2.8: Conventional sinusoidal PWM.



(a) Simple boost PWM.

(b) Simple boost PWM with THI.

Figure 2.9: Simple boost PWM.

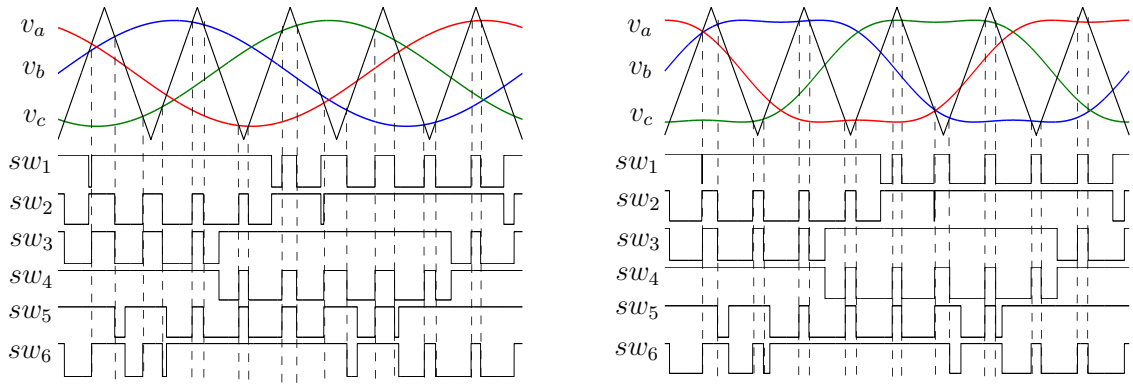
2.2 Pulse Width Modulation Techniques

2.2.1 Sinusoidal Pulse Width Modulation

As previously stated, the ISI has an extra switching state; shoot-through state. Accordingly, the conventional sinusoidal pulse width modulation (SPWM) used with the conventional VSI, shown in Figure 2.8, needs to be modified in order to insert the shoot-through state into the switching pattern. According to the literature, there are three SPWM techniques for the ZSI/qZSI, namely Simple Boost PWM (SBPWM), Maximum Boost PWM (MBPWM), and Maximum Constant Boost PWM (MCBPWM).

2.2.1.1 Simple Boost PWM

In the SBPWM method, two straight lines are utilized to insert the shoot-through state within the other switching states. As can be see in Figure 2.9(a), the triangular carrier waveform is



(a) Maximum boost PWM. (b) Maximum boost PWM with THI.

Figure 2.10: Maximum boost PWM.

compared with these two lines (v_p and v_n) in order to generate the shoot-through states. When the carrier waveform is greater than or lower than v_p or v_n, respectively, the inverter switches turn into shoot-through states. Apart from that, the inverter works with the conventional active and zero states.

In order to efficiently utilize the dc-link voltage, third harmonic injection (THI) is added to the reference signals v_a, v_b, and v_c as shown in Figure 2.9(b). By doing so, the inverter modulation index range is extended to $2/\sqrt{3}$ instead of 1. This results in a higher boost range as will be shown in the next chapters.

2.2.1.2 Maximum Boost PWM

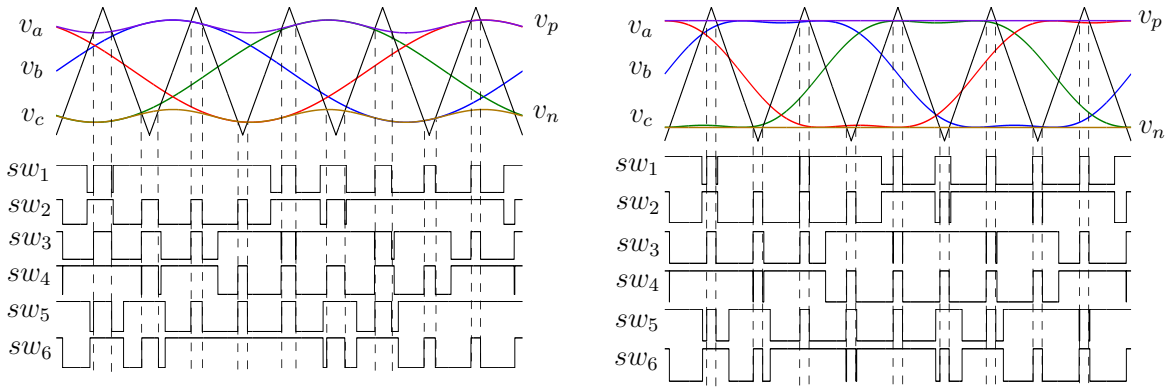
In this method, all zero states are turned into shoot-through states, see Figure 2.10(a). As a result, the voltage stress across the devices can be highly minimized. In addition, Figure 2.10(b) shows the MBPWM with THI.

The main disadvantage of this method is that the shoot-through duty cycle changes during the inverter operation which in turn results in high current ripple. In this case, a bigger passive components size is needed which increases the volume, weight, and cost of the inverter.

2.2.1.3 Maximum Constant Boost PWM

To overcome the problems of the above modulation technique, the MCBPWM technique is presented, see Figure 2.11(a). This method achieves the maximum available boost while keeping the shoot-through duty cycle fixed. In Figure 2.11(b), the THI is inserted to fully utilize the dc-link voltage.

As can be noted from Figures 2.9(b) and 2.11(b), the SBPWM and MCBPWM both with THI are typically the same and result in similar switching patterns. Table 2.1 shows a comparison of the SPWM methods. Note that m denotes the inverter modulation index, G_{max} is the maximum inverter gain, and $\hat{v}_{\text{dc}/v_{\text{in}}}$ represents the voltage stress on the inverter switches.



(a) Maximum constant boost PWM. (b) Maximum constant boost PWM with THI.

Figure 2.11: Maximum constant boost PWM.

Table 2.1: Comparison of different SPWM techniques for the ZSI/qZSI.

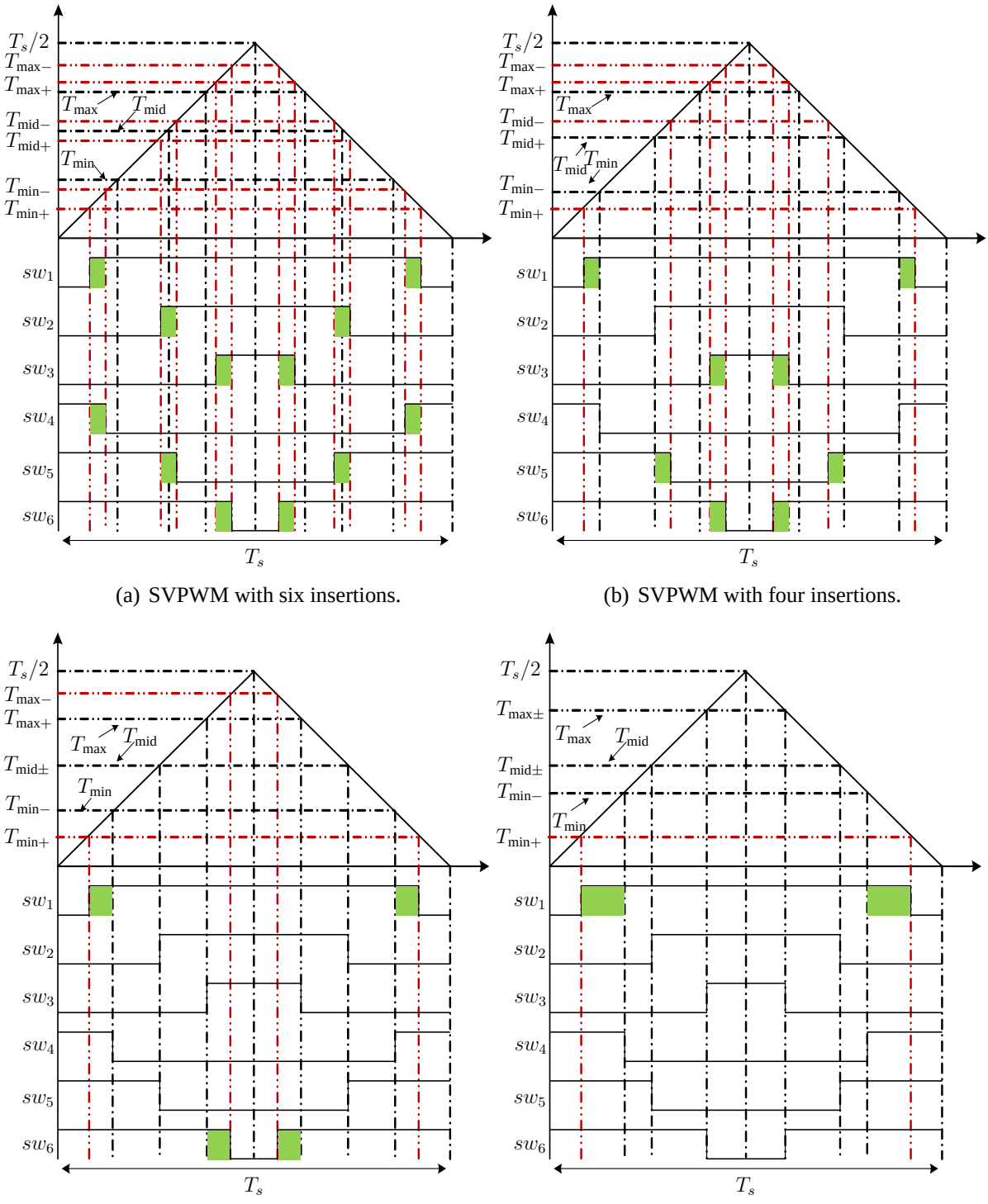
	SBPWM	MBPWM	MCBPWM
Maximum shoot-through duty cycle d_{max}	$1-m$	$1-\frac{3\sqrt{3}}{2\pi}m$	$1-\frac{\sqrt{3}}{2}m$
Maximum boost factor b_{max}	$\frac{1}{2m-1}$	$\frac{\pi}{3\sqrt{3}\,m-\pi}$	$\frac{1}{\sqrt{3}\,m-1}$
Maximum gain G_{max}	$\frac{m}{2m-1}$	$\frac{\pi\,m}{3\sqrt{3}\,m-\pi}$	$\frac{m}{\sqrt{3}\,m-1}$
Voltage stress $\hat{v}_{\text{dc}/v_{\text{in}}}$	$2G_{\text{max}}-1$	$\frac{3\sqrt{3}\,G_{\text{max}}}{\pi}-1$	$\sqrt{3}\,G_{\text{max}}-1$

2.2.2 Space Vector Pulse Width Modulation

Motivated by its advantages, such as lower current harmonics, full dc-link voltage utilization, and high modulation index, space vector pulse width modulation (SVPWM) has been applied with impedance source inverters [68–70]. For the SVPWM of the ZSIs/qZSIs, the shoot-through time is equally divided into several parts per the sampling interval. According to the literature, there are four main SVPWM techniques as follows.

The first one called SVPWM with six insertions (SVPWM6). In this technique, the shoot-through vector is equally divided into six parts in one sampling interval and inserted into the transition moment of switching states, as shown in Figure 2.12(a). Thereby, only one phase-leg is short-circuited in one switching cycle, where every inverter leg has two shoot-through states in each switching cycle. In comparison with the traditional SVPWM, there is no additional switching transitions, no need of dead time in phase legs, and invariant action time of effective vectors. These features lead to switching losses identical to that of the conventional VSI and higher reliability.

In the second technique, SVPWM with four insertions (SVPWM4), the the shoot-through time is also divided into six parts in one sampling interval as in SVPWM6, but it only modifies four switching signals as shown in Figure 2.12(b). The third method is called SVPWM with two insertions (SVPWM2). This modulation method divides the desired total shoot-through



(a) SVPWM with six insertions.

(b) SVPWM with four insertions.

(c) SVPWM with two insertions.

(d) SVPWM with single insertion.

Figure 2.12: The modified SVPWM techniques for the ZSI/qZSI. T_{max}, T_{mid}, and T_{min} are the maximum, medium, and minimum switching times of the three-phase switches, respectively. Moreover, the six switching times $T_{\text{max}+}$, $T_{\text{mid}+}$, $T_{\text{min}+}$, $T_{\text{max}-}$, $T_{\text{mid}-}$, and $T_{\text{min}-}$ are the shoot-through times resulting from the shoot-through duty cycle d.

Table 2.2: Comparison of different SVPWM techniques for the ZSI/qZSI.

	SVPWM6/2	SVPWM4	SVPWM1
d_{max}	$1-\frac{3\sqrt{3}}{2\pi}m$	$\frac{3}{4}(1-\frac{3\sqrt{3}}{2\pi}m)$	$\frac{1}{2}(1-\frac{3\sqrt{3}}{2\pi}m)$
b_{max}	$\frac{\pi}{3\sqrt{3}m-\pi}$	$\frac{4\pi}{9\sqrt{3}m-2\pi}$	$\frac{2\pi}{3\sqrt{3}m}$
G_{max}	$\frac{\pi m}{3\sqrt{3}m-\pi}$	$\frac{4\pi m}{9\sqrt{3}m-2\pi}$	$\frac{2\pi}{3\sqrt{3}}$
$\hat{v}_{\text{dc}}/v_{\text{in}}$	$\frac{3\sqrt{3}G_{\text{max}}}{\pi}-1$	$\frac{9\sqrt{3}G_{\text{max}}}{2\pi}-2$	$\frac{2\pi}{3\sqrt{3}m}$

time into four parts and it only needs to modify two switching signals as shown in Figure 2.12(c).

Finally, the SVPWM with single insertion (SVPWM1) is proposed. Compared with the traditional and former SVPWM methods, this technique just modifies one control signal that is the upper switch of minimum timing control signal or the lower switch of maximum control signal. Figure 2.12(d) illustrates the switching pattern for changing the upper switch control signal.

Based on the maximum boost factor, maximum overall gain of the inverter, and maximum voltage stress, Table 2.2 summarizes a comparison among the different SVPWM methods.

2.2.3 Comparison

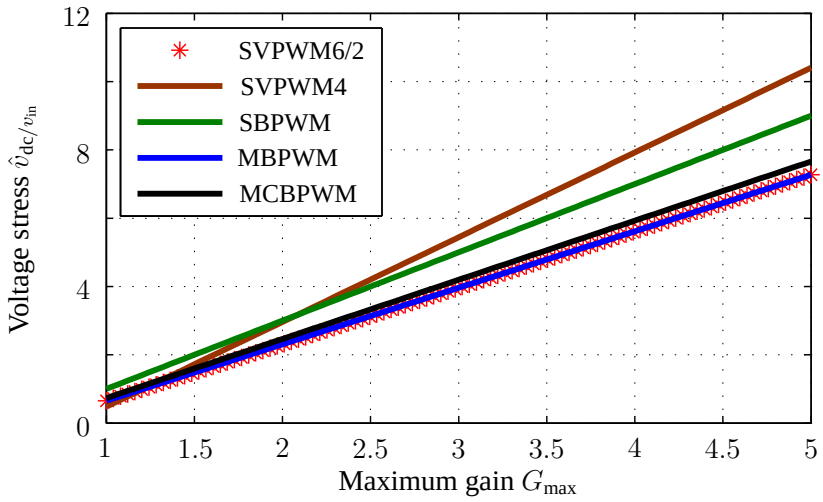
Figures 2.13(a) and 2.13(b) illustrate the difference in performance among the different modulation techniques. As can be seen, SVPWM6/2 and MBPWM provide the highest maximum shoot-through duty cycle in comparison to the other techniques. This in turn allows SVPWM6/2 and MBPWM to provide the highest boost factor.

At the same time, both SVPWM4 and SBPWM exhibit higher overall voltage stress on the inverter switches for most of the gain range. In addition, as shown in Table 2.2, the maximum overall gain of the inverter with SVPWM1 method is constant as it is independent either on the inverter modulation index or on the shoot-through duty cycle.

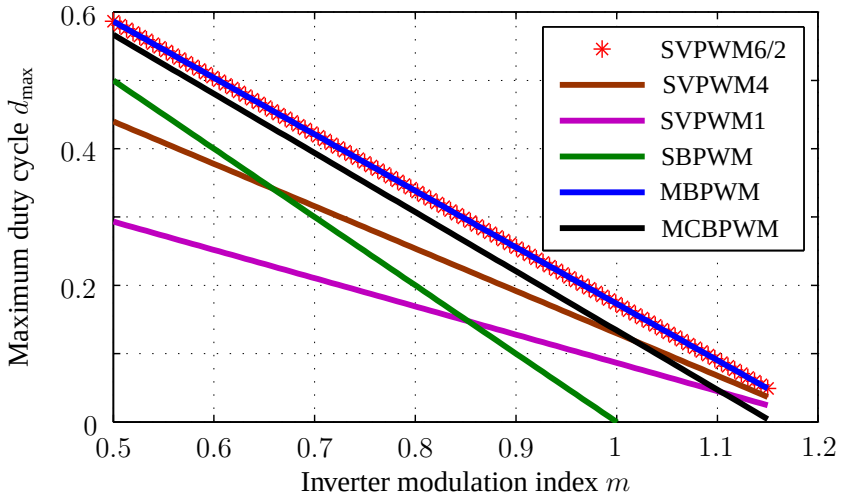
In this dissertation, with the linear controller, I employ both SVPWM6 and THI-SBPWM in order to result in reduced inductor current ripple and fully utilization of the dc-link voltage.

2.3 Conventional Linear Control Schemes

Although the ISIs are considered as single-stage buck-boost converters, both sides of them have to be separately controlled. On the dc-side, the dc-link voltage is indirectly controlled by adjusting the capacitor voltage (and/or the inductor current) of the impedance network. The dc-link voltage can not be directly controlled because it is a pulsated voltage as shown in Figure 2.14. In addition, the ac output current/voltage has to be simultaneously controlled. Thus, multiple control loops of linear controller (an outer, voltage control loop, and an inner, current loop) are required for both sides of the ISIs. The output of both dc- and ac-side controllers



(a) Voltage stress versus maximum gain.



(b) Maximum shoot-through duty cycle versus inverter modulation index.

Figure 2.13: Comparison of different modulation techniques for the ZSI/qZSI.

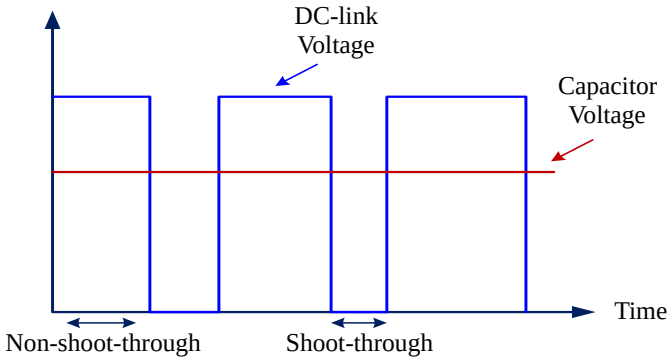


Figure 2.14: Dc-link voltage of the impedance source inverters.

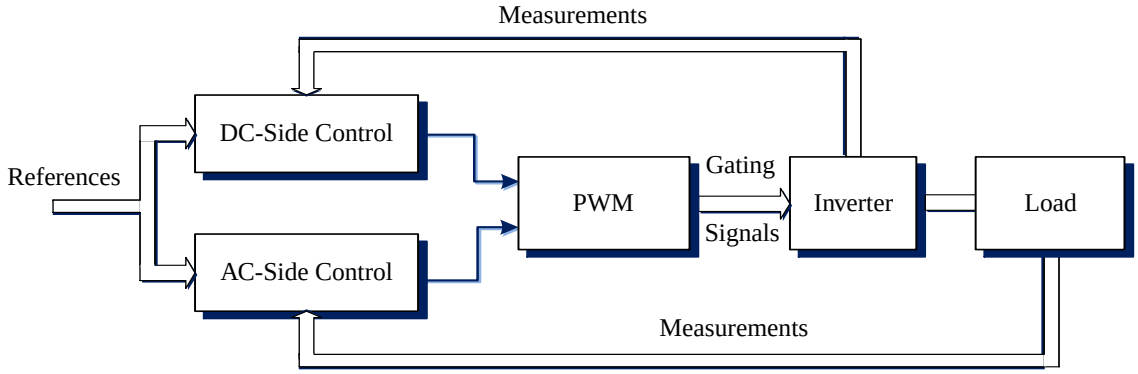


Figure 2.15: Linear control scheme for impedance source inverters.

are provided to the PWM technique to produce the gating signals to the inverter. The overall block diagram of linear controller for the ISIs is highlighted in Figure 2.15. Most of these linear schemes are based on PI controllers [24, 25, 33–38].

There are some crucial points that have to be taken into account when designing controllers for ISIs. First, the output of the dc- and ac-side controller are correlating to each other which accentuate a kind of limitation for the control designer. In other words, the shoot-through duty cycle (from the dc-side controller) and the inverter modulation index (from the ac-side controller) are related to each other, where their summation should not exceed the highest available modulation factor (1.15 in case of SVPWM). The interacting between the dc- and the ac-side controllers should be avoided in order to ensure a satisfying performance for both sides of the inverter. This implies that the controller parameters have to be carefully tuned in order to avoid a significant limitation in the system performance in terms of bandwidth, meaning that considerable engineering effort is required [24, 25].

Moreover, the impedance network of the ISI exhibits a nonminimum phase characteristic which requires much attention in the controller design in order to minimize its effect on the converter operation at different operating points. This characteristic means that the system exhibits a reverse-response behavior during transients. For example, when the output power demands increase then the ac side needs to be instantaneously short circuited for a non-negligible time for the dc-link voltage to remain at the desired level. This prolonged short-circuit situation of the ac side (which can be interpreted as an instantaneous increase in the shoot-through duty cycle) causes the capacitor voltage to initially drop and diverge from its reference value. A controller should be able to bring the voltage back to its predefined value in order to keep the system stable [71].

2.4 Direct Model Predictive Control

Predictive control is an advanced control method that relays on the physical model of the system under control in order to predict its future behavior. Based on the future predictions and an optimization criteria, the controller decides a sequence of appropriate control actions to be applied [72]. Although predictive control has a relatively long history with chemical and process engineering, it has been recently applied in power electronics and electrical drives ap-

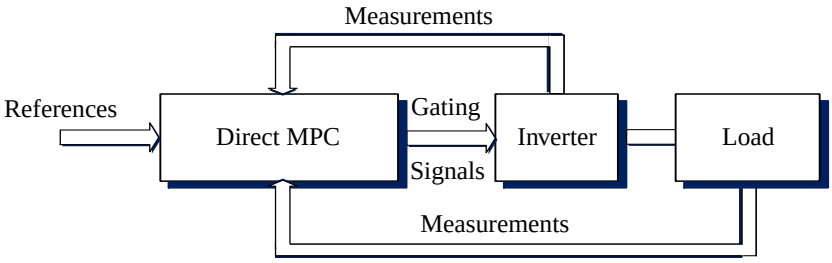


Figure 2.16: Direct model predictive control scheme for the impedance source inverters.

plications [73–75]. Predictive control is mainly classified into three techniques: trajectory-based predictive control, hysteresis-based predictive control, and model-based predictive control (MPC) [45].

Over the last decade, model predictive control (MPC) [44] has been established as an attractive control algorithm for power electronics applications [46, 75]. Particularly, the so called *direct* MPC—also referred to as finite control set (FCS) MPC—has been extensively used, thanks to its design simplicity; the switches of the converter are directly manipulated without requiring a modulator [45, 76–78]. Moreover, MPC, in general, and direct MPC, in particular, have been proved to be particularly effective when multiple-input, multiple-output (MIMO) systems with nonlinear, complex dynamics are concerned. The reason is that all the control objectives can be tackled in one stage since they are incorporated in one performance criterion, i.e. the cost function.

Considering the complexity of the ISIs and the above mentioned problems of the conventional control schemes, MPC can be considered as an efficient alternative control strategy. The block diagram of direct MPC for the ISI is presented in Figure 2.16.

2.5 Summary

In this chapter, different topologies of the impedance source inverters are proposed. Among others, qZSI is considered as one of the most efficient converter that can be utilized with DG applications. In addition, the modulation techniques proposed for ISI are discussed and compared with each other. It is found that space vector PWM with six insertions and simple boost PWM with THI are the most appropriate techniques for the qZSI. Hence, both techniques will be utilized with PI and PR controllers in the next chapters.

Furthermore, the conventional control methods for the ISIs are presented and discussed, where the control challenges are highlighted. As an alternative to the conventional linear control schemes, MPC strategy is introduced.

Part II

Conventional Inverters and Control

CHAPTER 3

Comparison of qZSIs and Conventional Two-Stage Inverters

This chapter presents a thorough comparison between the single-stage qZSI and the conventional two-stage inverter when used in DG-based PV applications. The comparison includes the analysis of the voltage stress on the inverter switches, required active and passive components, steady-state and transient performance, and inverter efficiency.

3.1 Motivation

Recently, the qZSI has been widely used with RES, especially with PV generation systems [17, 21, 23, 24]. Few research works found in the literature focusing on the comparison between the ZSI and the conventional two-stage inverter based on simulation studies, i.e. [19, 79]. These works do not consider the performance of each inverter neither the measured efficiency. Nevertheless, the comparison between the qZSI and the conventional two-stage inverter has not been yet done. Considering the advantages of the qZSI as a single-stage inverter for PV application, this chapter aims to investigate and compare it with the conventional two-stage inverter.

The comparison is carried out based on stand-alone PV application, where the inverters are connected with a resistive inductive RL load via an intermediate LC filter. In order to assure the system stability, both dc and ac sides of both inverters are simultaneously controlled by the PI-based control. The dc-side controller manages the boost operation, while the ac-side controller achieves the dc-ac conversion. The modeling, the theoretical concepts, and the control design for both inverters are presented and discussed. Moreover, the passive components requirement and the inverters losses analysis are introduced. Experimental investigations are conducted to verify the proposed inverter. In order to get high performance with low control volume, the control algorithms, the transformation, and modulation techniques are implemented on an FPGA.

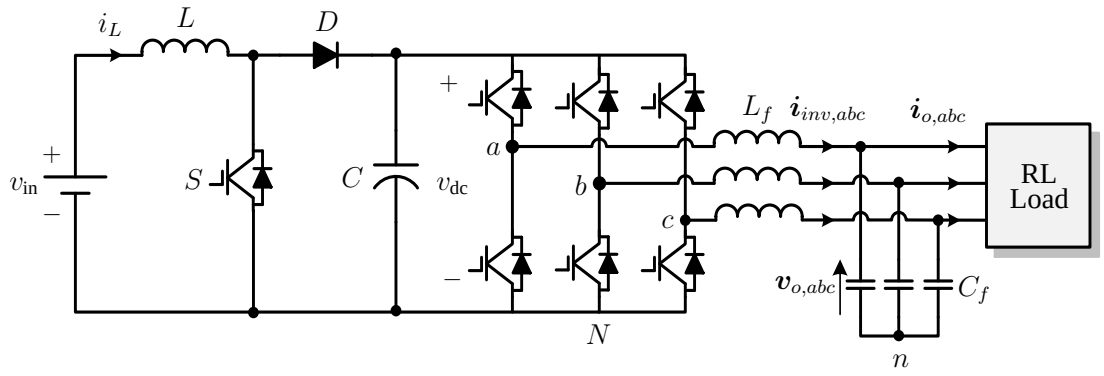
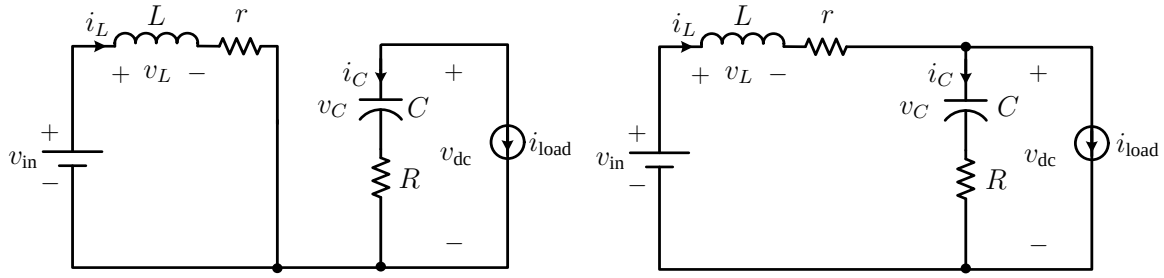


Figure 3.1: The conventional two-stage inverter connected with an LC filter and RL load.



(a) ON state. (b) OFF state.

Figure 3.2: Operation states of the dc-dc boost converter.

This chapter is organized as follows. Section 3.2 introduces the conventional two-stage inverter. In Section 3.3, the qZSI configuration and modeling are presented. Section 3.4 discusses the required passive and active components as well as the inverter efficiency, while the controller design is described in Section 3.5. In Section 3.6, experimental results are provided and analyzed. Finally, the summary is given in Section 3.7.

3.2 Conventional Two-stage Inverter

The configuration of the conventional two-stage inverter is shown in Figure 3.1. It consists of a dc-dc boost converter and a three-phase two-level VSI. The two-stage inverter is connected with an RL load throughout an LC filter. The mathematical model of the dc and ac side of the inverter are derived as follows.

3.2.1 DC-Side Model

As shown in Figure 3.2, the dc-dc boost converter has two operation states; ON and OFF state when the switch S is closed and open, respectively. Note that the three-phase inverter is approximated by a current source with dc current $i_{\text{load}} = \frac{p_{\text{vsi}}}{v_{\text{dc}}}$ (VSI instantaneous power divided by dc-link voltage). As the system model is concerned, the system state vector includes the inductor current and capacitor voltage, i.e. $\boldsymbol{x} = [i_L \ v_C]^T \in \mathbb{R}^2$. The system input consists of

the inverter input current and input voltage, i.e. $\boldsymbol{u} = [i_{\text{load}}\ v_{\text{in}}]^T \in \mathbb{R}^2$. Moreover, the capacitor voltage and the inductor current compose the output vector, i.e. $\boldsymbol{y} = [v_C\ i_L]^T \in \mathbb{R}^2$.

During ON state (see Figure 3.2(a)), the input voltage charges the inductor, while the capacitor voltage feeds the load. Accordingly, the following model is obtained

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \boldsymbol{A}_1\boldsymbol{x}(t) + \boldsymbol{B}_1\boldsymbol{u}(t) \tag{3.1a}$$

$$\boldsymbol{y}(t) = \boldsymbol{C}\boldsymbol{x}(t)\,, \tag{3.1b}$$

where,

$$\boldsymbol{A}_1 = \begin{bmatrix} -\frac{r_s}{L_s} & 0 \\ 0 & 0 \end{bmatrix},\ \boldsymbol{B}_1 = \begin{bmatrix} 0 & -\frac{1}{L_s} \\ -\frac{1}{C_s} & 0 \end{bmatrix},\ \boldsymbol{C} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix},$$

with r_s and R_s being the internal resistance of the inductor L_s and the equivalent series resistance of the capacitor C_s, respectively.

In OFF state (see Figure 3.2(b)), the input voltage and the inductor voltage charge the capacitor and supply energy to the load. Thus, the system model is given as

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \boldsymbol{A}_2\boldsymbol{x}(t) + \boldsymbol{B}_2\boldsymbol{u}(t) \tag{3.2a}$$

$$\boldsymbol{y}(t) = \boldsymbol{C}\boldsymbol{x}(t)\,, \tag{3.2b}$$

where,

$$\boldsymbol{A}_2 = \begin{bmatrix} -\frac{r_s+R_s}{L_s} & -\frac{1}{L_s} \\ \frac{1}{C_s} & 0 \end{bmatrix},\ \boldsymbol{B}_2 = \begin{bmatrix} \frac{R_s}{L_s} & -\frac{1}{L_s} \\ -\frac{1}{C_s} & 0 \end{bmatrix}.$$

By utilizing the state-space averaging method, models (3.1) and (3.2) can construct one model that describes the behavior of the dc-dc boost converters as follows.

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \boldsymbol{A}\boldsymbol{x}(t) + \boldsymbol{B}\boldsymbol{u}(t) \tag{3.3a}$$

$$\boldsymbol{y}(t) = \boldsymbol{C}\boldsymbol{x}(t)\,, \tag{3.3b}$$

where,

$$\boldsymbol{A} = \begin{bmatrix} \frac{R_s(d_s-1)-r_s}{L_s} & \frac{d_s-1}{L_s} \\ \frac{1-d_s}{C_s} & 0 \end{bmatrix},\ \boldsymbol{B} = \begin{bmatrix} \frac{(1-d_s)R_s}{L_s} & -\frac{1}{L_s} \\ \frac{d_s-1}{C_s} & 0 \end{bmatrix},$$

with d_s being the conduction duty cycle of the switch S, i.e. $d_s = T_{\text{ON}}/T_s$, where T_{ON} is the conduction time and T_s is the sampling interval.

In order to obtain the small-signal model of (3.3), perturbations are introduced to the system variables. Thus, the following model is obtained.

$$\frac{\mathrm{d}\hat{\boldsymbol{x}}(\boldsymbol{t})}{\mathrm{d}t} = \tilde{\boldsymbol{A}}(\bar{\boldsymbol{X}} + \hat{\boldsymbol{x}}) + \tilde{\boldsymbol{B}}(\bar{\boldsymbol{U}} + \hat{\boldsymbol{u}}) \tag{3.4a}$$

$$\hat{\boldsymbol{y}}(t) = \boldsymbol{C}\hat{\boldsymbol{x}}\,, \tag{3.4b}$$

where $(\bar{\boldsymbol{X}} + \hat{\boldsymbol{x}}) = [\bar{I}_L + \hat{i}_L \;\; \bar{V}_C + \hat{v}_C]^T \in \mathbb{R}^2$ and $(\bar{\boldsymbol{U}} + \hat{\boldsymbol{u}}) = [\bar{I}_{\text{load}} + \hat{i}_{\text{load}} \;\; \bar{V}_{\text{in}} + \hat{v}_{\text{in}}]^T \in \mathbb{R}^2$. Note that the variables with capital letters represent the average dc values, while the small letters denotes the small-signal values. Moreover,

$$\tilde{\boldsymbol{A}} = \begin{bmatrix} \frac{R_s(\bar{D}_s + \hat{d}_s - 1) - r_s}{L_s} & \frac{\bar{D}_s - 1}{L_s} \\ \frac{1 - \bar{D}_s - \hat{d}_s}{C_s} & 0 \end{bmatrix}, \; \tilde{\boldsymbol{B}} = \begin{bmatrix} \frac{(1 - \bar{D}_s - \hat{d}_s)R_s}{L_s} & \frac{1}{L_s} \\ \frac{\bar{D}_s + \hat{d}_s - 1}{C_s} & 0 \end{bmatrix},$$

where $\bar{D}_s$ is the average value of the duty cycle, while $\hat{d}_s$ represents the small-signal value. By rearranging the state variables in (3.4a), the following system model results

$$\frac{\mathrm{d}\hat{\boldsymbol{x}}(\boldsymbol{t})}{\mathrm{d}t} = \begin{bmatrix} \frac{R_s(\bar{D}_s - 1) - r_s}{L_s} & \frac{\bar{D}_s - 1}{L_s} \\ \frac{1 - \bar{D}_s}{C_s} & 0 \end{bmatrix} \hat{\boldsymbol{x}}(\boldsymbol{t}) + \begin{bmatrix} \frac{R_s(\bar{I}_{L_s} - \bar{I}_{\text{load}}) + \bar{V}_{\text{in}}}{L_s} \\ \frac{\bar{I}_{\text{load}} - \bar{I}_{L_s}}{C_s} \end{bmatrix} \hat{d}_s + \begin{bmatrix} \frac{1}{L_s} \\ 0 \end{bmatrix} \hat{v}_{\text{in}} + \begin{bmatrix} \frac{R_s(1 - \bar{D}_s)}{L_s} \\ \frac{\bar{D}_s - 1}{C_s} \end{bmatrix} \hat{i}_{\text{load}}\,. \tag{3.5}$$

Then, by applying Laplace transform on (3.5), the transfer function of the capacitor voltage and the converter duty cycle is obtained as

$$G(s) = \frac{\hat{v}_C(s)}{\hat{d}_s(s)} = \frac{(1 - \bar{D}_s)\bar{V}_{\text{in}} + (r_s + L_s s)(\bar{I}_L - \bar{I}_{\text{load}})}{L_s C_s s^2 + (R_s C_s(1 - \bar{D}_s) - r_s)s + (1 - 2\bar{D}_s)^2} \tag{3.6}$$

where s is the complex frequency in the Laplace domain. The transfer function (3.6) is used to design and tune the voltage controller of the dc-dc boost converter in Section 3.5.

3.2.2 AC-Side Model

Considering one phase from the ac side, the output LC filter can be represented by the equivalent circuit shown in Figure 3.3.

By applying Kirchhoff's Law to the circuit shown in Figure 3.3, the governing differential equations for phase a can be written as

$$L_f \frac{\mathrm{d}i_{\text{inv},a}(t)}{\mathrm{d}t} = S_a\, v_{\text{dc}} - (i_{\text{inv},a}\, r_f + v_{o,a} + v_{nN}) \tag{3.7a}$$

$$C_f \frac{\mathrm{d}v_{o,a}(t)}{\mathrm{d}t} = i_{\text{inv},a} - i_{o,a}\,, \tag{3.7b}$$

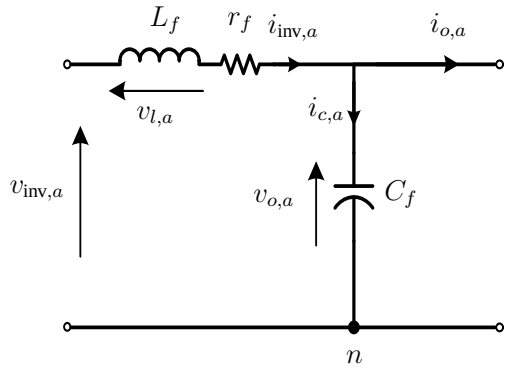


Figure 3.3: Ac-side equivalent circuit of phase a, with r_f being the internal resistance of the filter inductance L_f.

where S_a represents the switching signal for the upper switch in phase a and v_{dc} is the dc-link voltage. Similarly, phases b and c can be expressed by

$$L_f \frac{\mathrm{d}i_{\text{inv},b}(t)}{\mathrm{d}t} = S_b\, v_{\text{dc}} - (i_{\text{inv},b}\, r_f + v_{o,b} + v_{nN}) \tag{3.8a}$$

$$C_f \frac{\mathrm{d}v_{o,b}(t)}{\mathrm{d}t} = i_{\text{inv},b} - i_{o,b}\,, \tag{3.8b}$$

$$L_f \frac{\mathrm{d}i_{\text{inv},c}(t)}{\mathrm{d}t} = S_c\, v_{\text{dc}} - (i_{\text{inv},c}\, r_f + v_{o,c} + v_{nN}) \tag{3.9a}$$

$$C_f \frac{\mathrm{d}v_{o,c}(t)}{\mathrm{d}t} = i_{\text{inv},c} - i_{o,c}\,, \tag{3.9b}$$

where S_b (S_c) represents the switching signal for the upper switch in phase b (c). Assuming that the three-phase load is balanced, the following equations apply.

$$i_{\text{inv},a} + i_{\text{inv},b} + i_{\text{inv},c} = 0\,, \quad v_{o,a} + v_{o,b} + v_{o,c} = 0 \tag{3.10}$$

By summing up (3.7a), (3.8a), and (3.9a), and then substituting (3.10), the voltage v_{nN} can be described in terms of S_a, S_b, and S_c as following:

$$v_{nN} = \frac{v_{\text{dc}}}{3}(S_a + S_b + S_c) \tag{3.11}$$

Substituting (3.11) in (3.7a), (3.8a), and (3.9a) results in

$$L_f \frac{\mathrm{d}i_{\text{inv},a}(t)}{\mathrm{d}t} = -i_{\text{inv},a}\, r_f - v_{o,a} + v_{\text{dc}}(S_a - \frac{1}{3}(S_a + S_b + S_c)) \tag{3.12a}$$

$$L_f \frac{\mathrm{d}i_{\text{inv},b}(t)}{\mathrm{d}t} = -i_{\text{inv},b}\, r_f - v_{ob} + v_{\text{dc}}(S_b - \frac{1}{3}(S_a + S_b + S_c)) \tag{3.12b}$$

$$L_f \frac{\mathrm{d}i_{\text{inv},c}(t)}{\mathrm{d}t} = -i_{\text{inv},c}\, r_f - v_{o,c} + v_{\text{dc}}(S_c - \frac{1}{3}(S_a + S_b + S_c)) \tag{3.12c}$$

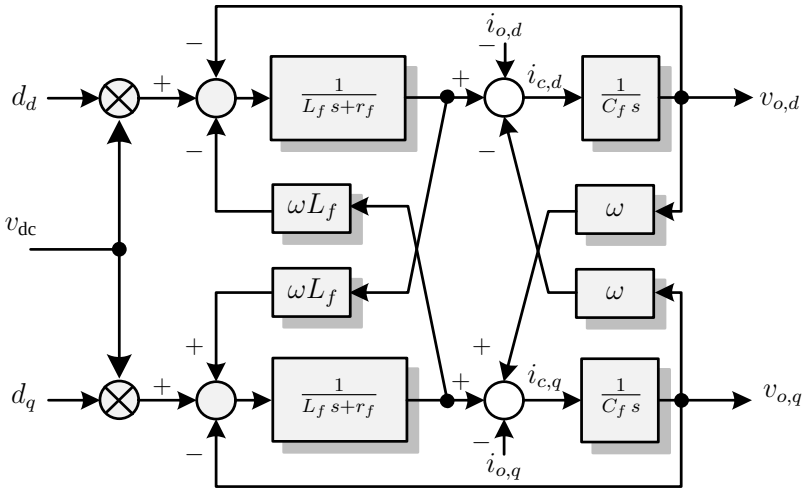


Figure 3.4: Ac-side mathematical model in the dq frame.

When the switching frequency is much higher than the output voltage fundamental frequency, the switching signals S_a, S_b, and S_c can be replaced with their respective duty cycles d_a, d_b, and d_c [80]. In order to simplify the model, the three-phase system (abc) is transformed to the stationary reference system $(\alpha\beta)$, and then to the rotating reference frame (dq) by using Clarke and Park transformation matrices, respectively, i.e. $\boldsymbol{\xi}_{\alpha\beta} = \boldsymbol{K_C}\boldsymbol{\xi}_{abc}$ and $\boldsymbol{\xi}_{dq} = \boldsymbol{K_P}\boldsymbol{\xi}_{\alpha\beta}$, where $\boldsymbol{\xi}_{abc} = [\boldsymbol{\xi}_a\ \boldsymbol{\xi}_b\ \boldsymbol{\xi}_c]^T$ is a variable in the abc system, $\boldsymbol{\xi}_{\alpha\beta} = [\boldsymbol{\xi}_\alpha\ \boldsymbol{\xi}_\beta]^T$ is a variable in the $\alpha\beta$ system, and $\boldsymbol{\xi}_{dq} = [\boldsymbol{\xi}_d\ \boldsymbol{\xi}_q]^T$ is a variable in the dq system.

$$\boldsymbol{K_C} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}, \quad \boldsymbol{K_P} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix}, \tag{3.13}$$

where $\omega = 2\pi f$ is the angular frequency of the output voltage, with f being the fundamental frequency. Performing $\alpha\beta$ and dq transformations to (3.7b), (3.8b), (3.9b), and (3.12), the following mathematical model in the dq rotating reference frame is obtained.

$$L_f \frac{\mathrm{d}i_{\text{inv},d}(t)}{\mathrm{d}t} - \omega\, L_f\, i_{\text{inv},q} + r_f\, i_{\text{inv},d} = v_{\text{dc}}\, d_d - v_{o,d} \tag{3.14a}$$

$$L_f \frac{\mathrm{d}i_{\text{inv},q}(t)}{\mathrm{d}t} + \omega\, L_f\, i_{\text{inv},d} + r_f\, i_{\text{inv},q} = v_{\text{dc}}\, d_q - v_{o,q} \tag{3.14b}$$

$$C_f \frac{\mathrm{d}v_{o,d}(t)}{\mathrm{d}t} = i_{\text{inv},d} + \omega\, v_{cq} - i_{o,d} \tag{3.14c}$$

$$C_f \frac{\mathrm{d}v_{o,q}(t)}{\mathrm{d}t} = i_{\text{inv},q} + \omega\, v_{cd} - i_{o,q}\,, \tag{3.14d}$$

The final mathematical model of the ac side (3.14) is drawn and presented in Figure 3.4.

3.2.3 Steady-State Analysis

During the steady-state operation and according to the inductor volt-second balance, the average voltage of the inductor is zero over one complete sampling interval T_s. Accordingly, the dc-link voltage v_{dc} is deduced as

$$v_{\text{dc}} = \frac{1}{1-d_s}\, v_{\text{in}} \tag{3.15}$$

Moreover, the peak ac output voltage is calculated by

$$\hat{v}_o = m_s\, \frac{v_{\text{dc}}}{2} = \frac{m_s}{1-d_s} \cdot \frac{v_{\text{in}}}{2} = G_s\, \frac{v_{\text{in}}}{2}\,, \tag{3.16}$$

where m_s and G_s are the inverter modulation index and the overall voltage gain of the conventional two-stage inverter, respectively.

The minimum voltage stress on the inverter switches is defined as the relationship between the dc-link voltage and the input voltage when the inverter modulation index is maximum. Assuming that the sinusoidal PWM is employed with the THI, the maximum achievable modulation index is $2/\sqrt{3}$. Accordingly, the minimum voltage stress is given by

$$\frac{v_{\text{dc}}}{v_{\text{in}}} = \frac{2\,G_s}{\sqrt{3}} \tag{3.17}$$

3.3 Quasi-Z-Source Inverter

Figure 3.5 shows the configuration of the qZSI. It includes an impedance network, a three-phase two-level VSI, an LC filter, and an RL load. The qZSI uses the impedance network and the shoot-through state in order to boost the input voltage to the desired dc-link voltage. Accordingly, the qZSI has two different operating states, namely shoot-through and non-shoot-through state as shown in Figure 3.6. The model of the dc side will be introduced in detail; however, the ac-side model is the same as the one derived previously for the conventional two-stage inverter in Section 3.2.2.

3.3.1 DC-Side Model

The models of the qZS network will be separately derived for each case, and then averaged in one model. The state vector includes the inductors current and capacitor voltages, i.e. $\boldsymbol{x} = [i_{L_1}\ i_{L_2}\ v_{C_1}\ v_{C_2}]^T \in \mathbb{R}^4$. The inverter input current and input voltage are considered as the system inputs, i.e. $\boldsymbol{u} = [i_{\text{load}}\ v_{\text{in}}]^T \in \mathbb{R}^2$, while the capacitor voltage and inductor current compose the output vector $\boldsymbol{y} = [v_{C_1}\ i_{L_1}]^T \in \mathbb{R}^2$. Due to the symmetry of the quasi-Z-source network, only one inductor current and one capacitor voltage are chosen as output variables.

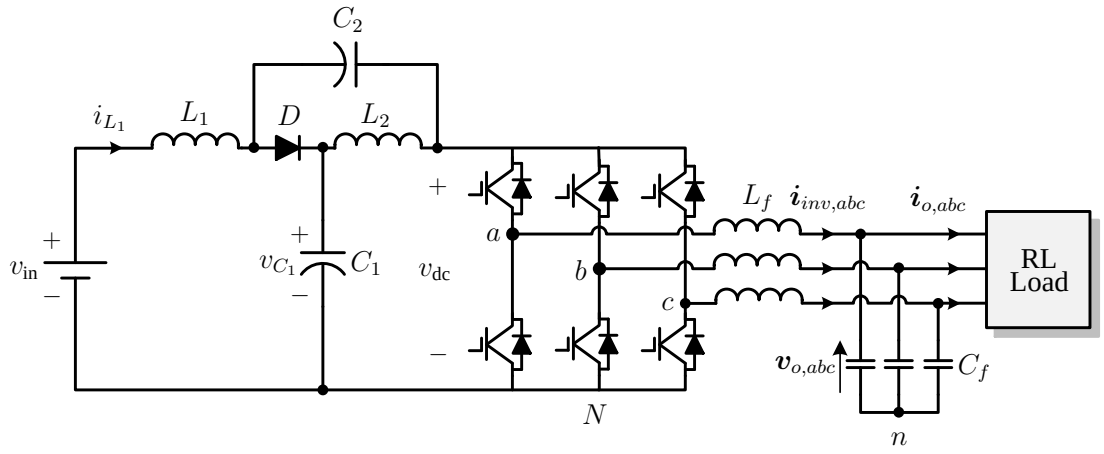
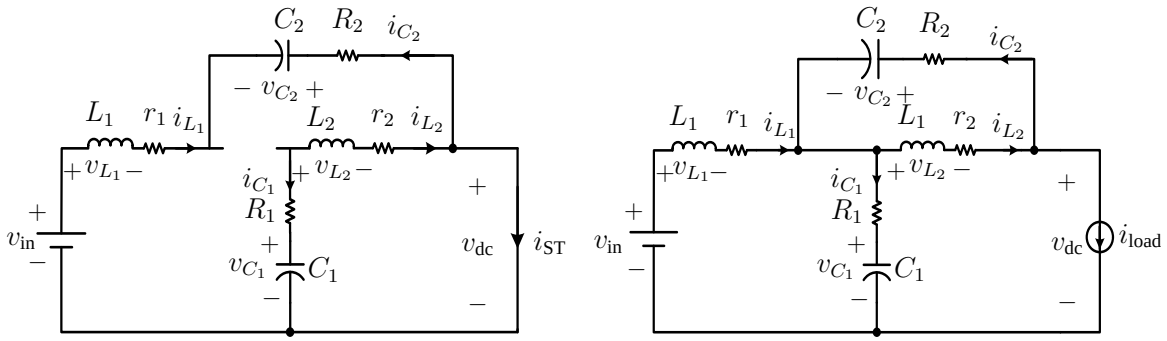


Figure 3.5: The quasi-Z-source inverter connected with an LC filter and RL load.



(a) Shoot-through state.

(b) Non-shoot-through state.

Figure 3.6: Operation states of the qZSI.

3.3.1.1 Shoot-Through State

At shoot-through state, as can be noted in Figure 3.6(a), the capacitors charge the inductors, while the diode is cut off. Thus the system model is expressed as

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \boldsymbol{F}_1\boldsymbol{x}(t) + \boldsymbol{G}_1\boldsymbol{u}(t) \tag{3.18a}$$

$$\boldsymbol{y}(t) = \boldsymbol{E}\boldsymbol{x}(t)\,, \tag{3.18b}$$

where,

$$\boldsymbol{F}_1 = \begin{bmatrix} -\frac{r_1+R_2}{L_1} & 0 & 0 & \frac{1}{L_1} \\ 0 & -\frac{r_2+R_1}{L_2} & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ -\frac{1}{C_2} & 0 & 0 & 0 \end{bmatrix},\ \boldsymbol{G}_1 = \begin{bmatrix} 0 & \frac{1}{L_1} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix},\ \boldsymbol{E} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix}.$$

where r_1, R_1, r_2, R_2, L_1, L_2, C_1, and C_2 are the resistances, inductances, and capacitances of the qZS network, respectively.

3.3.1.2 Non-Shoot-Through State

During the non-shoot-through state, the input voltage and the inductors charge the capacitors and supply the load as shown in Figure 3.6(b), where the diode turns on. Accordingly, the system model is written as

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \boldsymbol{F}_2\boldsymbol{x}(t) + \boldsymbol{G}_2\boldsymbol{u}(t) \tag{3.19a}$$

$$\boldsymbol{y}(t) = \boldsymbol{E}\boldsymbol{x}(t)\,, \tag{3.19b}$$

where,

$$\boldsymbol{F}_2 = \begin{bmatrix} -\frac{r_1+R_1}{L_1} & 0 & \frac{-1}{L_1} & 0 \\ 0 & -\frac{r_2+R_2}{L_2} & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 \end{bmatrix},\ \boldsymbol{G}_2 = \begin{bmatrix} \frac{R_1}{L_1} & \frac{1}{L_1} \\ \frac{R_2}{L_2} & 0 \\ \frac{-1}{C_1} & 0 \\ \frac{-1}{C_2} & 0 \end{bmatrix}.$$

3.3.1.3 Average State-Space Model

Using state-space averaging, the models (6.5) and (3.19) can be combined in one model. Note that to simplify the model, we assume that $C_1 = C_2 = C$ and $L_1 = L_2 = L$. Also, the internal resistances of the inductors and the capacitors are assumed as $r_1 = r_2 = r$ and $R_1 = R_2 = R$. Consequently, the model of the qZS network is given by

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \boldsymbol{F}\boldsymbol{x}(t) + \boldsymbol{G}\boldsymbol{u}(t) \tag{3.20a}$$

$$\boldsymbol{y}(t) = \boldsymbol{E}\boldsymbol{x}(t)\,, \tag{3.20b}$$

where,

$$\boldsymbol{F} = \begin{bmatrix} -\frac{r+R}{L} & 0 & \frac{-1+d}{L} & \frac{d}{L} \\ 0 & -\frac{r+R}{L} & \frac{d}{L} & \frac{-1+d}{L} \\ \frac{1-d}{C} & -\frac{d}{C} & 0 & 0 \\ -\frac{d}{C} & \frac{1-d}{C} & 0 & 0 \end{bmatrix},\ \boldsymbol{G} = \begin{bmatrix} \frac{(1-d)R}{L} & \frac{1}{L} \\ \frac{(1-d)R}{L} & 0 \\ \frac{-1+d}{C} & 0 \\ \frac{-1+d}{C} & 0 \end{bmatrix}.$$

with d being the shoot-through duty cycle, i.e. $d = T_0/T_s$, where T_0 is the shoot-through interval.

In order to drive the small-signal model of the qZS network needed for the controller design, perturbations are introduced to the system variables. Accordingly, the following expression is given.

$$\frac{\mathrm{d}\hat{\boldsymbol{x}}(\boldsymbol{t})}{\mathrm{d}t} = \tilde{\boldsymbol{F}}(\bar{\boldsymbol{X}} + \hat{\boldsymbol{x}}) + \tilde{\boldsymbol{G}}(\bar{\boldsymbol{U}} + \hat{\boldsymbol{u}}) \tag{3.21a}$$

$$\hat{\boldsymbol{y}}(t) = \boldsymbol{E}\hat{\boldsymbol{x}}\,, \tag{3.21b}$$

where $(\bar{\boldsymbol{X}} + \hat{\boldsymbol{x}}) = [\bar{I}_{L_1} + \hat{i}_{L_1} \;\; \bar{I}_{L_2} + \hat{i}_{L_2} \;\; \bar{V}_{C_1} + \hat{v}_{C_1} \; \bar{V}_{C_2} + \hat{v}_{C_2}]^T \in \mathbb{R}^4$ and $(\bar{\boldsymbol{U}} + \hat{\boldsymbol{u}}) = [\bar{I}_{\text{load}} + \hat{i}_{\text{load}} \;\; \bar{V}_{\text{in}} + \hat{v}_{\text{in}}]^T \in \mathbb{R}^2$. Moreover,

$$\tilde{\boldsymbol{F}} = \begin{bmatrix} -\frac{r+R}{L} & 0 & \frac{-1+\bar{D}+\hat{d}}{L} & \frac{\bar{D}+\hat{d}}{L} \\ 0 & -\frac{r+R}{L} & \frac{\bar{D}+\hat{d}}{L} & \frac{-1+\bar{D}+\hat{d}}{L} \\ \frac{1-\bar{D}-\hat{d}}{C} & -\frac{\bar{D}+\hat{d}}{C} & 0 & 0 \\ -\frac{\bar{D}+\hat{d}}{C} & \frac{1-\bar{D}-\hat{d}}{C} & 0 & 0 \end{bmatrix}, \; \tilde{\boldsymbol{G}} = \begin{bmatrix} \frac{(1-\bar{D}-\hat{d})R}{L} & \frac{1}{L} \\ \frac{(1-\bar{D}-\hat{d})R}{L} & 0 \\ \frac{-1+\bar{D}+\hat{d}}{C} & 0 \\ \frac{-1+\bar{D}+\hat{d}}{C} & 0 \end{bmatrix}.$$

where $\bar{D}$ is the average value of the shoot-through duty cycle, while $\hat{d}$ represents the small-signal value. By rearranging the small-signal model (3.21a), the following model is obtained

$$\frac{\mathrm{d}\hat{\boldsymbol{x}}(\boldsymbol{t})}{\mathrm{d}t} = \begin{bmatrix} -\frac{r+R}{L} & 0 & \frac{\bar{D}-1}{L} & \frac{\bar{D}}{L} \\ 0 & -\frac{r+R}{L} & \frac{\bar{D}}{L} & \frac{\bar{D}-1}{L} \\ \frac{1-\bar{D}}{C} & -\frac{\bar{D}}{C} & 0 & 0 \\ -\frac{\bar{D}}{C} & \frac{1-\bar{D}}{C} & 0 & 0 \end{bmatrix} \hat{\boldsymbol{x}}(\boldsymbol{t}) + \begin{bmatrix} \frac{\bar{V}_{C_1}+\bar{V}_{C_2}-R\,\bar{I}_{\text{load}}}{L} \\ \frac{\bar{V}_{C_1}+\bar{V}_{C_2}-R\,\bar{I}_{\text{load}}}{L} \\ \frac{\bar{I}_{\text{load}}-\bar{I}_{L_1}-\bar{I}_{L_2}}{C} \\ \frac{\bar{I}_{\text{load}}-\bar{I}_{L_1}-\bar{I}_{L_2}}{C} \end{bmatrix} \hat{d} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_{\text{in}} + \begin{bmatrix} \frac{R(1-\bar{D})}{L} \\ \frac{R(1-\bar{D})}{L} \\ \frac{\bar{D}-1}{C} \\ \frac{\bar{D}-1}{C} \end{bmatrix} \hat{i}_{\text{load}} \tag{3.22}$$

Accordingly, the transfer functions of the capacitor voltage and the inductor current with the shoot-through duty cycle are given by

$$G_1(s) = \frac{\hat{v}_C(s)}{\hat{d}(s)} = \frac{(1-2\bar{D})(\bar{V}_{C_1} + \bar{V}_{C_2} - R\,\bar{I}_{\text{load}}) + (Ls + r + R)(\bar{I}_{\text{load}} - \bar{I}_{L_1} - \bar{I}_{L_2})}{LCs^2 + C(r+R)s + (1-2\bar{D})^2} \tag{3.23}$$

$$G_2(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{(\bar{V}_{C_1} + \bar{V}_{C_2} - R\,\bar{I}_{\text{load}})Cs + (2\bar{D}-1)(\bar{I}_{\text{load}} - \bar{I}_{L_1} - \bar{I}_{L_2})}{LCs^2 + C(r+R)s + (1-2\bar{D})^2} \tag{3.24}$$

The transfer functions (3.23) and (3.24) are used to design and tune the dc-side controller of the qZSI in Section 3.5.

3.3.2 Steady-State Analysis

At steady-state operation and according to the inductor volt-second balance, the average voltage of the inductors over one complete sampling interval T_s is zero. Therefore, the voltages of the capacitors C_1 and C_2, v_{C_1} and v_{C_2}, respectively, as well as the currents i_{L_1} and i_{L_2} of the inductors L_1 and L_2, respectively, are deduced as follows.

$$v_{C_1} = \frac{1-d}{1-2d}\, v_{\text{in}}, \;\; v_{C_2} = \frac{d}{1-2d}\, v_{\text{in}}, \;\; i_{L_1} = i_{L_2} = \frac{1-d}{1-2d}\, i_{\text{load}} \tag{3.25}$$

Moreover, the peak value of the dc-link voltage during the non-shoot-through period is

$$\hat{v}_{\text{dc}} = v_{C_1} + v_{C_2} = \frac{1}{1-2d}\, v_{\text{in}} = b\, v_{\text{in}} \tag{3.26}$$

With regards to the ac-side of the qZSI, the peak phase voltage is given by

$$\hat{v}_{\text{o}} = m\,\frac{\hat{v}_{\text{dc}}}{2} = m\,b\,\frac{v_{\text{in}}}{2} = \frac{m}{1-2d}\cdot\frac{v_{\text{in}}}{2} = G\,\frac{v_{\text{in}}}{2}, \tag{3.27}$$

where m and G are the modulation index and total voltage gain of the qZSI, respectively. It can be noted from (3.27) that the output voltage of the qZSI can be stepped up or down based on both d and m.

In order to define the voltage stress on the inverter switches, the simple boost control PWM for the qZSI is assumed to be utilized in this work. In this case, the relationship between the modulation index m and the maximum shoot-through duty cycle d_{max} is given by [81]:

$$d_{\text{max}} = 1 - m \tag{3.28}$$

By inserting the THI to the PWM technique, the limitation between m and d_{max} can be reduced as follows

$$d_{\text{max}} = 1 - \frac{2}{\sqrt{3}}\,m \tag{3.29}$$

Accordingly, the maximum boost factor b_{max} and the maximum overall gain G_{max} can be presented as

$$b_{\text{max}} = \frac{1}{1-2\,d_{\text{max}}} = \frac{1}{\sqrt{3}\,m-1}\,, \quad G_{\text{max}} = m\,b_{\text{max}} = \frac{m}{\sqrt{3}\,m-1} \tag{3.30}$$

Based on (3.30), m can be written as

$$m = \frac{G_{\text{max}}}{\sqrt{3}\,G_{\text{max}}-1} \tag{3.31}$$

Thus, the minimum voltage stress on the inverter switches can be deduced from (3.26), (3.30), and (3.31) as follows

$$\frac{\hat{v}_{\text{dc}}}{v_{\text{in}}} = \sqrt{3}\,G_{\text{max}} - 1 \tag{3.32}$$

The voltage stresses of the conventional two-stage inverter and the qZSI are compared based on (3.17) and (3.32). The result is illustrated in Figure 3.7. The result highlights that up to voltage gain of 2, the voltage stress is lower in case of the qZSI. However, if the voltage gain is higher than 2, the voltage stress is lower with the conventional inverter.

3.4 Required Components and Efficiency

Both inverters are mainly composed of active switches (semiconductor devices) and passive components (capacitors and inductors). As for the active components, the conventional two-stage inverter uses an extra active switch in comparison with the qZSI, compare Figures 3.1 and 3.5. This section deals with the required passive components and the losses analysis of both topologies under investigation.

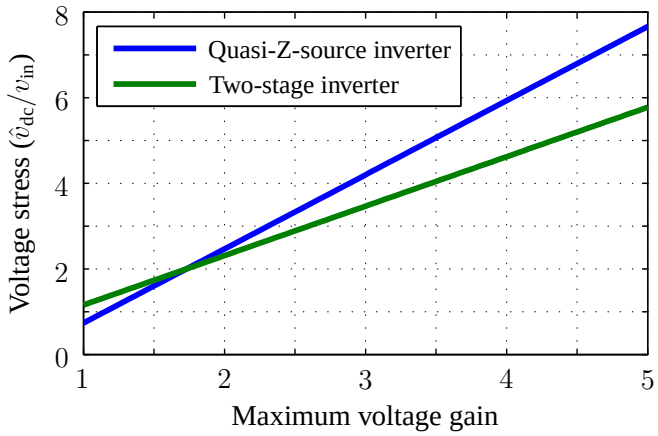


Figure 3.7: The relationship between the voltage stress and the overall gain of the inverters.

3.4.1 Passive Components Requirement

Passive components required for each converter represent significant parts which determine the inverter size, weight, and cost. In this section, the passive components for both topologies are designed based on the desired inductor current and capacitor voltage ripples as follows.

3.4.1.1 Two-Stage Inverter

The maximum capacitor voltage ripple occurs in two cases; during the longest zero state and when the instantaneous output power reaches its peak value. When the longest zero state occurs, the inverter input current i_{load} is zero. Throughout this case, if the dc-dc boost converter in its ON state, the capacitor current is zero (see Figure 3.2(a)). However, during the OFF state, the capacitor current equals to the inductor current, i.e.

$$i_{C_{\text{a}}} = i_L = \frac{P_o}{v_{\text{in}}}\,, \tag{3.33}$$

where P_o is the output power. On the other hand, the maximum output power occurs in an active state and when the output voltage of one of the three-phases reaches its maximum value. In this case, the capacitor current equals to the inverter input current as follows

$$i_{C_{\text{b}}} = i_{\text{load}} = \hat{i}_o\, \cos\varphi = \frac{4\,P_o}{3\,m_s\,v_{\text{dc}}}\, \cos\varphi\,, \tag{3.34}$$

where $\hat{i}_o$ is the peak phase current and $\cos\varphi$ is the system power factor. From (3.33) and (3.34), the capacitor voltage ripple is given by

$$\Delta v_C = (1-d_s)\frac{P_o\,T_s}{C_s\,v_{\text{in}}} - (\frac{3}{4}m_s - d_s)\frac{4\,P_o\,T_s}{3\,m_s\,C_s\,v_{\text{dc}}}\cos\varphi \tag{3.35}$$

In order to design the inductance for the dc-dc boost converter, the current ripple is given by

$$\Delta i_L = \frac{v_{\text{in}}\,\bar{D}_s\,T_s}{L_s} = \frac{v_{\text{in}}(v_{\text{dc}} - v_{\text{in}})\,T_s}{L_s\,v_{\text{dc}}} \tag{3.36}$$

Table 3.1: System requirements

Parameter	Value
Input voltage v_{in}	$160\,\text{V}$
Dc-link voltage v_{dc}	$240\,\text{V}$
Capacitor voltage v_{C_1}	$200\,\text{V}$
Peak dc-link voltage $\hat{v}_{\text{dc}}$	$240\,\text{V}$
Desired capacitor voltage ripple	$< 3\,\%$
Desired inductor current ripple	$< 10\,\%$
Output power P_o	$2\,\text{kW}$
Load power factor $\cos\varphi$	0.9
Modulation index for the conventional inverter m_c	$2/\sqrt{3}$
PWM carrier frequency for dc-dc-converter	$50\,\text{kHz}$
PWM carrier frequency for three-phase inverter	$20\,\text{kHz}$

Both (3.35) and (3.36) are utilized to design the required capacitance and inductance for the dc-dc boost converter.

3.4.1.2 Quasi-Z-Source Inverter

As for the qZSI, during the shoot-through time, the capacitors charge the inductors. As a result the same current flows through both of them. Hence,

$$\Delta v_C = \frac{\bar{I}_L\, T_0}{C} = \frac{P_o\, T_0}{C\, v_{\text{in}}}\,, \tag{3.37}$$

where Δv_C represents the desired capacitor voltage ripple. Again, in the shoot-though interval, both voltages on the capacitors and inductors are equal, then

$$\Delta i_L = \frac{\bar{V}_C\, T_0}{L} \tag{3.38}$$

where Δi_L is the desired inductor current ripple and $\bar{V}_C$ denotes the average capacitor voltage. Since the currents passing through the two inductors of the qZSI are identical and the voltages across them are the same, they can be built on one core with the same size of one inductor and doubled inductance. By doing so, the weight and the size of the qZS network can be highly reduced.

Table 3.2: Passive components requirements

Parameter	Value
qZS inductance L_1, L_2	$500\,\mu$H
qZS capacitance C_1, C_2	$470\,\mu$F
dc-dc converter inductance L	$1000\,\mu$H
dc-dc converter capacitance C	$780\,\mu$F

3.4.1.3 Case Study

Based on the previous analysis and the system requirements presented in Table 3.1, the passive components for both inverters are designed. The required inductors and capacitors for the conventional two-stage inverter and qZSI are summarized in Table 3.2. As can be seen, the qZSI uses comparable inductance and capacitance values with the two-stage inverter for the same input voltage and output power rating. At the same time, the two-stage inverter uses an extra active switch as previously mentioned.

3.4.2 Inverters' Losses

The efficiency of any power converter is basically related to its losses. The losses of an inverter include semiconductor devices losses, passive components losses, gate driver and controller losses. However, the semiconductor devices losses are considered as the significant part of the total losses. The latter mainly compose of two types, namely conduction and switching losses that will be deduced as follows [82]. The voltage drop on the semiconductor device and the conduction losses are given by

$$V_{ce} = A_{ce} + B_{ce}\, i_{con} + C_{ce}\, i_{con}^2\,, \tag{3.39a}$$

$$P_{con} = \frac{1}{2\pi}\int_{\gamma_1}^{\gamma_2} V_{ce}(\omega t)\, i_{con}(\omega t)\, d_{con}(\omega t)\, d\omega t\,, \tag{3.39b}$$

where A_{ce}, B_{ce}, and C_{ce} represent the coefficients of the conduction losses of the semiconductor device derived from its data sheet. Moreover, i_{con} is the conduction current and d_{con} expresses the conduction duty cycle of the device. On the other hand, the average switching losses in one cycle is given by

$$P_{sw} = \frac{f_{sw}}{2\pi}\int_{\alpha_1}^{\alpha_2} E_{sw}(\omega t)\, d\omega t\,, \tag{3.40}$$

where

$$E_{sw} = (A_{sw} + B_{sw}\, i_{con} + C_{sw}\, i_{con}^2)\frac{v_{\text{dc}}}{v_{\text{ref}}}\,, \tag{3.41}$$

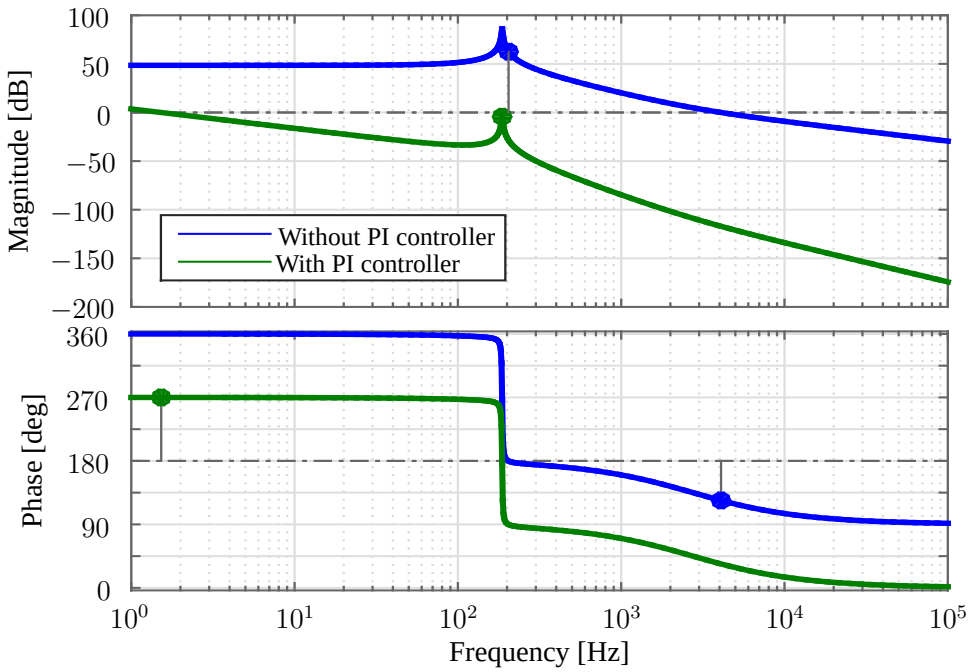


Figure 3.8: Bode plot of the dc-dc boost converter with and without PI compensation.

with A_{sw}, B_{sw}, and C_{sw} denoting the switching losses coefficients obtained from the device data sheet. Moreover, f_{sw} is the inverter switching frequency and v_{ref} is the reference voltage used for parameters calculation in the device data sheet.

Based on (3.39) and (3.40), the losses of both inverters can be calculated using the data sheet of the semiconductor devices as will be shown in Section 3.6.2. For this work, the Powerex IPM PM300CLA060 module is used as a three-phase bridge for the qZSI and VSI. In addition, the Powerex PM300DSA060 switch is utilized for the dc-dc boost converter. The diodes of the dc-dc converter and the qZS network are represented by RURG3060.

3.5 PI-Based Controller Design

Both the conventional two-stage inverter and qZSI require two separate controllers for the dc and ac side. For the dc side, based on (3.6) and (3.23), PI controllers are designed to regulate the dc-link voltage of the two-stage inverter as well as the capacitor voltage of the qZSI. Figures 3.8 and 3.9 show the Bode responses of the dc-dc boost converter and the qZS network, respectively. As can be noted, by adding the PI controllers, the systems are stable with sufficient phase margins.

With regard to the ac-side control, the conventional multi-loop PI controller, shown in Figure 3.10, is utilized for the inverters under consideration. The inner loop is a feedback current loop (P controller) that provides compensation for the input voltage disturbances and for the phase delay caused by the output LC filter. The outer voltage loop, PI controller, generates

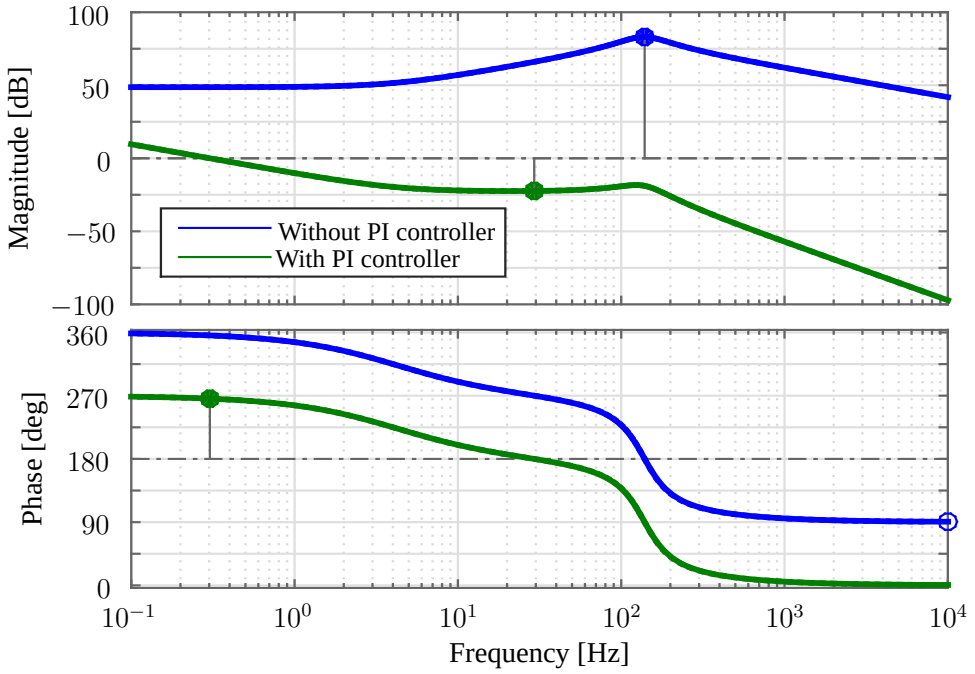


Figure 3.9: Bode plot of the dc side of the qZSI with and without PI compensation.

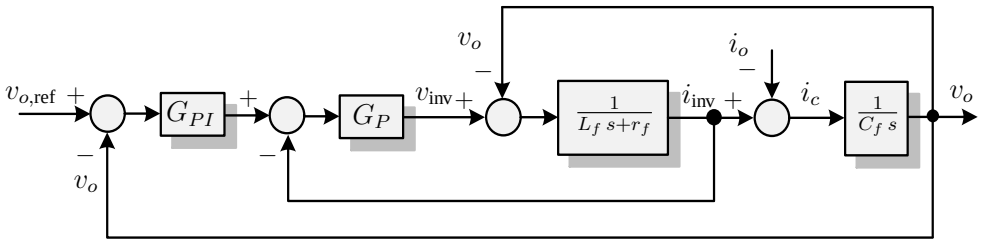


Figure 3.10: Ac-side controller scheme.

the reference current for the inner current control. Since the PI current control in stationary $\alpha\beta$ coordinates presents non-zero steady state error due to the lack of an integral component at frequencies different from zero, the PI control in rotating synchronous dq coordinates is implemented instead. Hence, a phase-locked loop (PLL) is used to compute the instantaneous angular position θ of the output voltage required for the transformation from the abc to the dq frame, and vice versa.

The voltage control schemes of the two-stage inverter and qZSI are shown in Figures 3.11 and 3.12, respectively. The output of the dc-side controller (d_s) of the two-stage inverter is fed to the PWM to generate the switching signal for the switch S of the dc-dc boost converter. Moreover, the inverter modulation index m_s is input to the PWM to output the switching signals for the VSI. With the qZSI, both the shoot-through duty cycle d and the modulation index m are delivered to the PWM block in order to generate the switching signals.

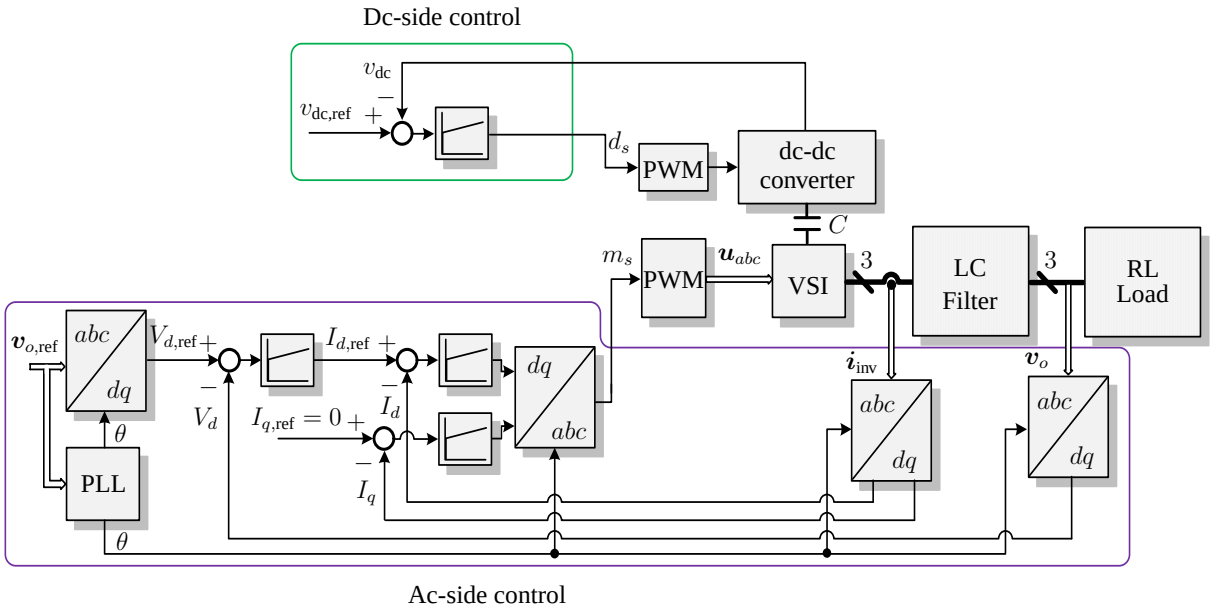


Figure 3.11: Voltage control scheme based on PI controllers for the two-stage inverter.

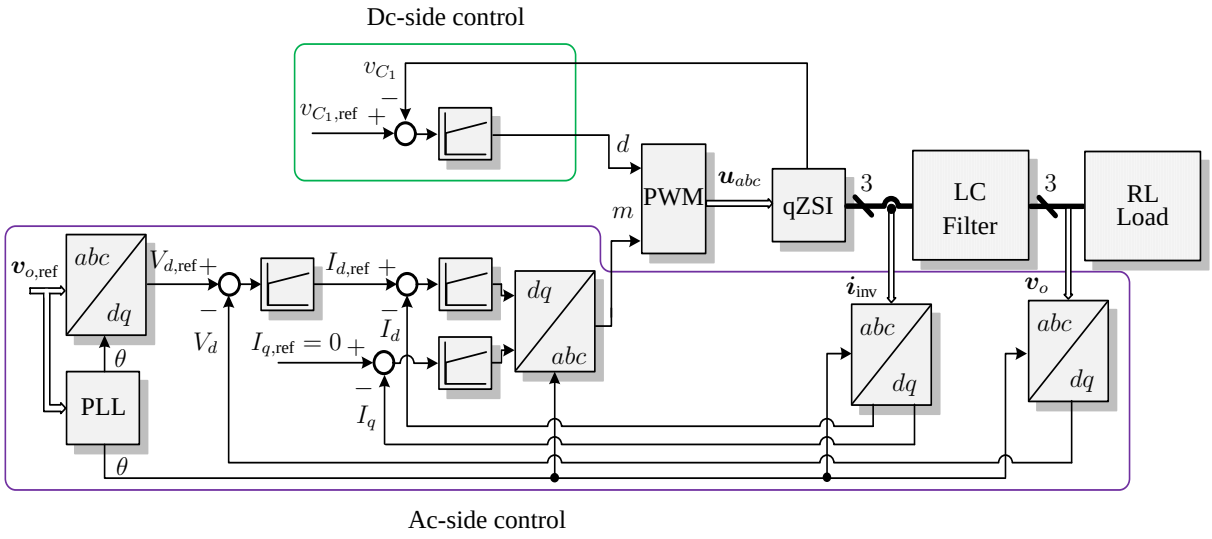
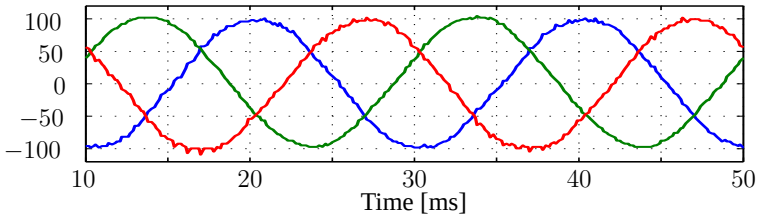


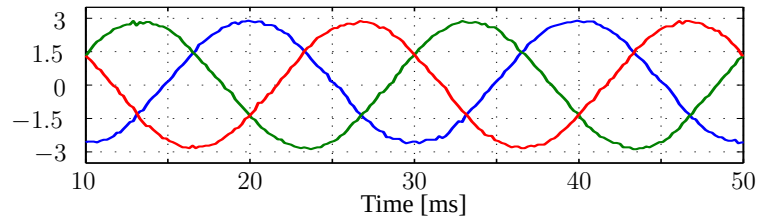
Figure 3.12: Voltage control scheme based on PI controllers for the qZSI.

3.6 Experimental Evaluation

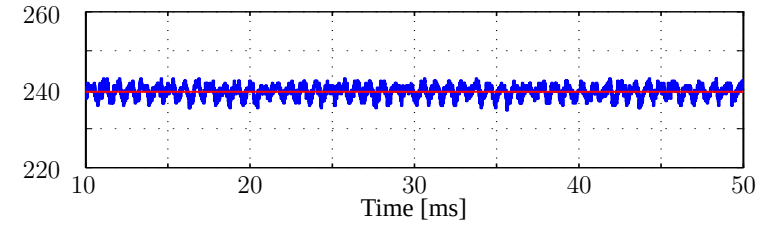
In order to examine the performance of both inverters under discussion in steady-state and transient operations, experimental work is conducted at the laboratory. 2 kW prototypes of both the qZSI and the conventional two-stage inverter are designed based on the system parameters in Tables 3.1 and 3.2. Both inverters are fed from a variable dc power supply (represents the PV source) and connected with an RL load ($35\,\Omega, 2.5\,$mH) via an LC filter ($10\,$mH, $50\,\mu$F) as shown in Figures 3.1 and 3.5. The input dc voltage v_{in} is adjusted to $160\,$V. The control algorithms are implemented on FPGA Cyclone III-EP3C40Q240C8. For more details about the test bench, please refer to appendix C.



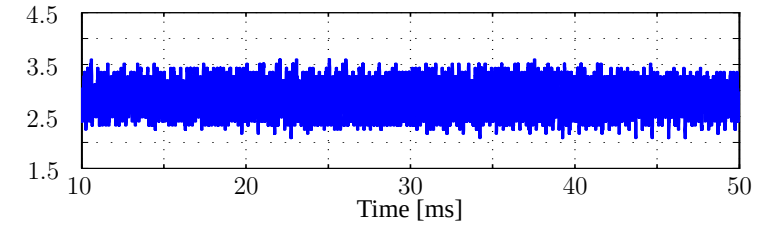
(a) Three-phase output voltage $\boldsymbol{v}_{\text{o,abc}}$ in [V].



(b) Three-phase output current $\boldsymbol{i}_{\text{o,abc}}$ in [A].



(c) DC-link voltage v_{dc} and its reference in [V].



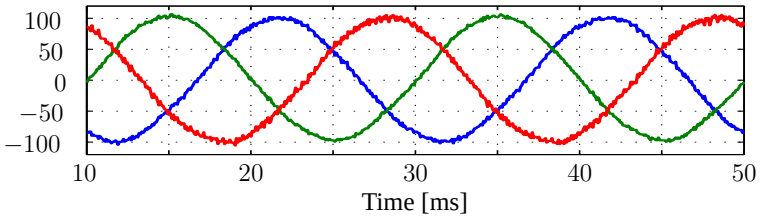
(d) Inductor current i_L in [A].

Figure 3.13: Experimental results of the conventional two-stage inverter. The output voltage THD $= 2.01\%$.

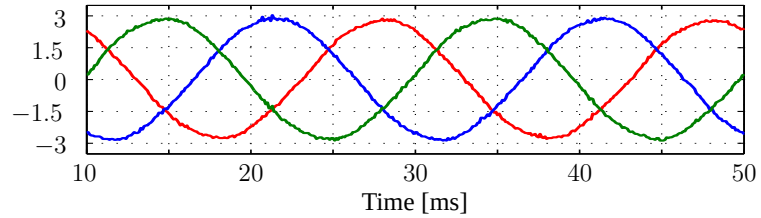
The output voltage reference $v_{o,\text{ref}}$ is set to $100\,\text{V}$. In order not to affect the sinusoidal waveform of the output voltage and avoid the interacting between the ac and dc sides of the qZSI, the capacitor voltage reference $v_{C,\text{ref}}$ should be equal to or higher than double the output voltage reference [24]. Hence, the capacitor voltage reference is chosen to be $200\,\text{V}$ which results in a $240\,\text{V}$ peak dc-link voltage (see steady-state analysis presented in Section 3.3.2). As for the two-stage inverter, the dc-link voltage reference is adjusted to $240\,\text{V}$ in order to be comparable with the dc-link voltage of the qZSI.

3.6.1 Steady-State Operation

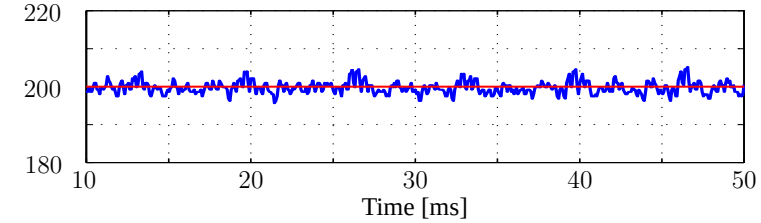
The experimental ac- and dc-side results for the conventional two-stage inverter and qZSI are shown in Figures 3.13 and 3.14, respectively. As can be observed in Figures 3.13(a) and 3.14(a),



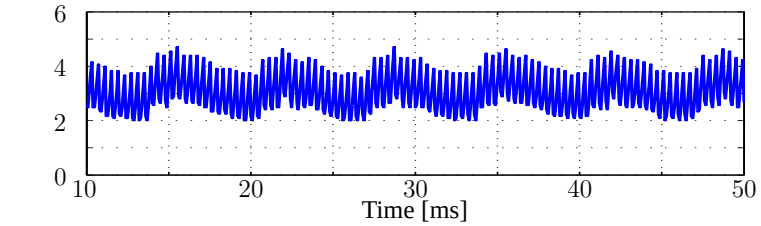
(a) Three-phase output voltage $\boldsymbol{v}_{\text{o,abc}}$ in [V].



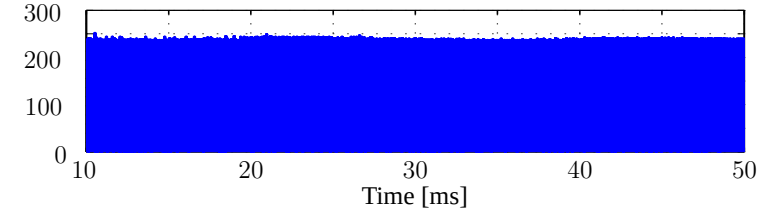
(b) Three-phase output current $\boldsymbol{i}_{\text{o,abc}}$ in [A].



(c) Capacitor voltage v_{C_1} and its reference in [V].



(d) Inductor current i_{L_1} in [A].



(e) Dc-link voltage v_{dc} in [V].

Figure 3.14: Experimental results of the qZSI. The output voltage THD $= 0.63\%$

both the two-stage inverter and the qZSI generate fully regulated sinusoidal output voltage waveform. However, the qZSI generate voltage THD of $0.63\,\%$ which is lower than that of the two-stage inverter ($2.01\,\%$). This thanks to the qZS network, the output distortion is highly reduced.

As for the dc-side results, Figure 3.13(c) shows that the dc-link voltage of the two-stage inverter is well tracked. On the other hand, the capacitor voltage of the qZSI is successfully regulated along it reference value at $200\,\text{V}$ (see Figure 3.14(c)) resulting in a peak dc-link volt-

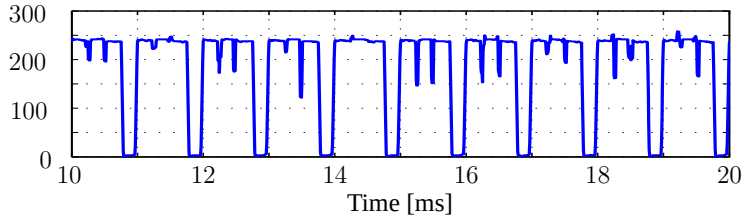


Figure 3.15: Zoomed-in dc-link voltage v_{dc} of the qZSI.

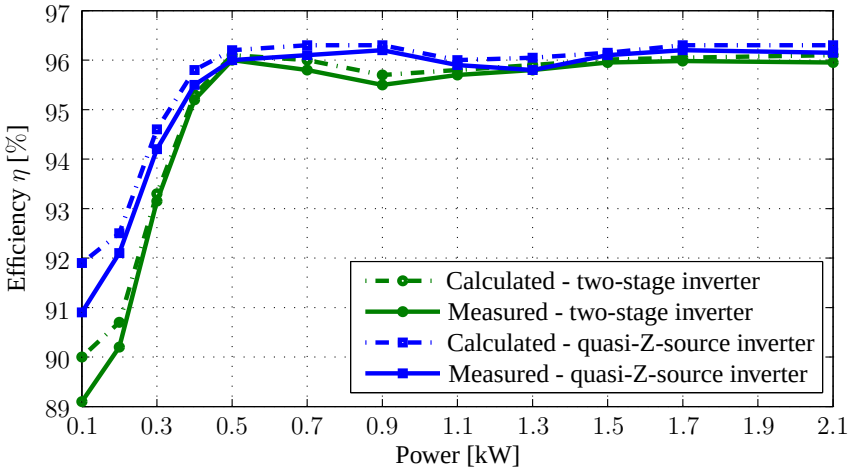


Figure 3.16: Calculated and measured efficiencies of both presented inverters.

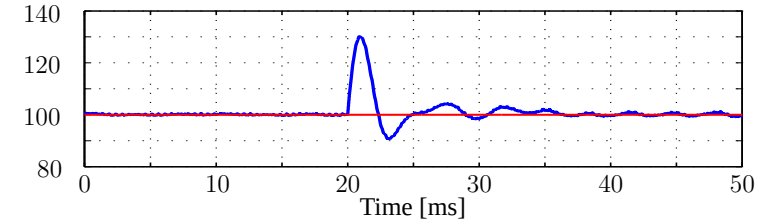
age of $240\,\text{V}$ (see Figure 3.14(e)). Moreover, Figure 3.15 zooms in on the time axis of the dc-link voltage of the qZSI. As can be noted, the dc-link voltage is not fixed, where it switches between a peak value (during the active or zero state) and zero value (during the shoot-through state). These results are inline with the theoretical analysis introduced in Section 3.3.2.

3.6.2 Inverters Efficiency

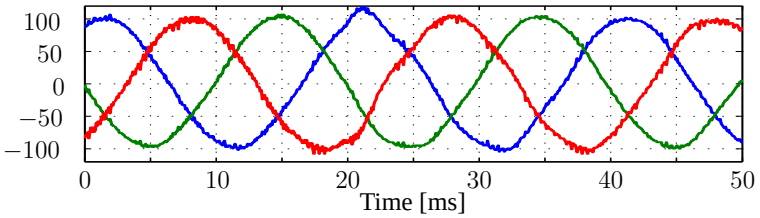
In fact, the efficiency test is very crucial in the evaluation process for any power converter. Based on the losses model presented in Section 3.4.2, the efficiency of both proposed inverters are calculated. Moreover, some experiments are conducted in the laboratory on both inverters to measure the efficiency under the same input and output operating conditions. In order to get different output power values, the RL load is changed while keeping the output voltage fixed at $100\,\text{V}$ and the input voltage constant at $160\,\text{V}$. The efficiencies of the inverters are computed with different output load by

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{3/2\, v_o\, i_o\, \cos\varphi}{V_{\text{in}}\, I_{\text{in}}}\,. \tag{3.42}$$

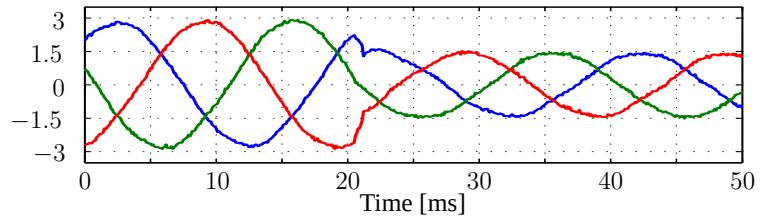
Figure 3.16 highlights the calculated and measured efficiencies for the conventional two-stage inverter and qZSI. As can be concluded from the comparison results, the qZSI shows higher efficiency than the two-stage inverter for the whole operating power range (up to $2.1\,\text{kW}$). This result claims that the single-stage qZSI represents an attractive alternative with reduced cost and higher reliability and efficiency.



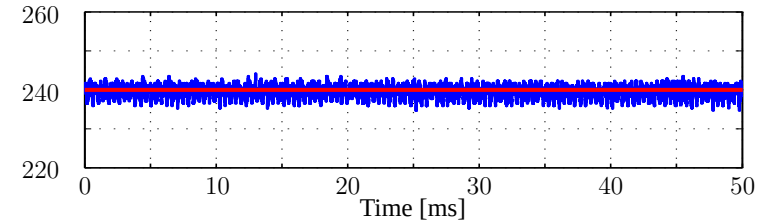
(a) d-component of the output voltage and its reference in [V].



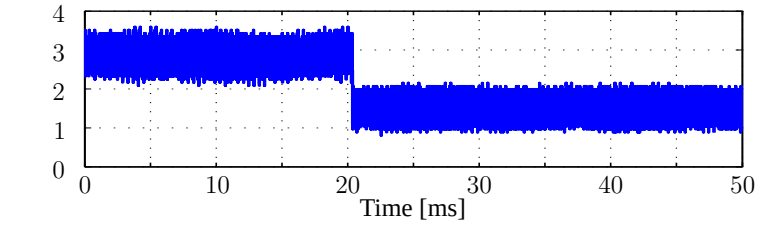
(b) Three-phase output voltage $\boldsymbol{v}_{\text{o,abc}}$ in [V].



(c) Three-phase output current $\boldsymbol{i}_{\text{o,abc}}$ in [A].



(d) Dc-link voltage v_{dc} and its reference in [V].

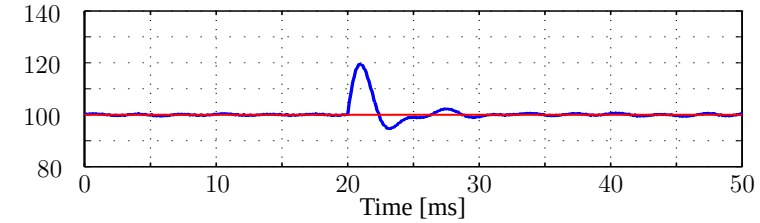


(e) Inductor current i_L in [A].

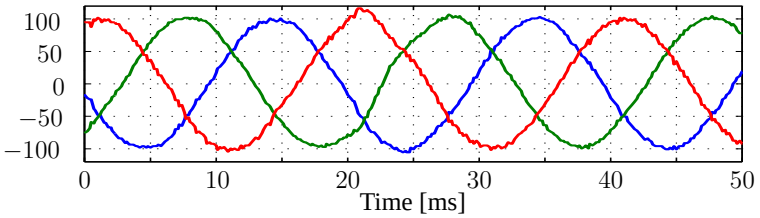
Figure 3.17: Experimental results of the two-stage inverter under load step-down change.

3.6.3 Transient Operation

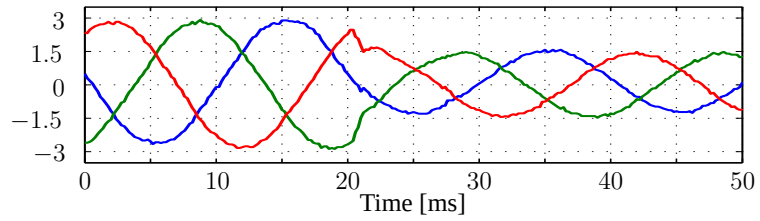
The transient performance of both the conventional two-stage inverter and qZSI are tested with an RL load. The reference value of the output voltage is kept constant to $100\,\text{V}$, regardless of the input dc voltage and load value. The transient response of both inverters are examined under step change in the load value and in the input dc voltage level.



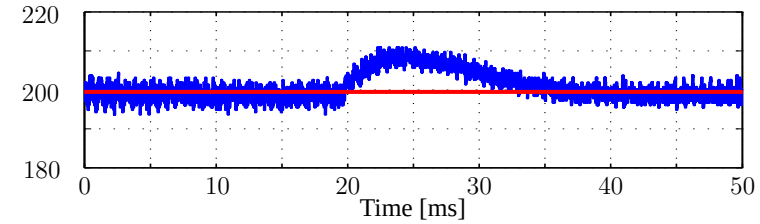
(a) d-component of the output voltage and its reference in [V].



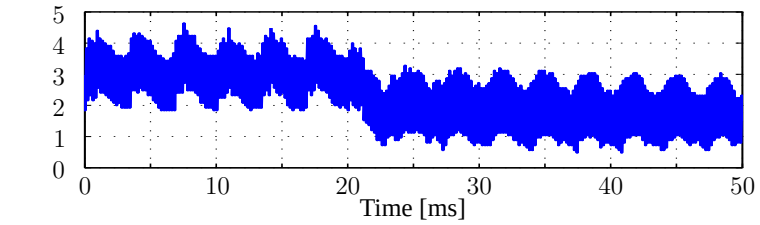
(b) Three-phase output voltage $\boldsymbol{v}_{\text{o,abc}}$ in [V].



(c) Three-phase output current $\boldsymbol{i}_{\text{o,abc}}$ in [A].



(d) Capacitor voltage v_{C_1} and its reference in [V]



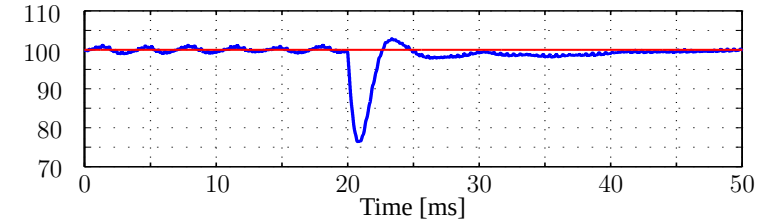
(e) Inductor current i_{L_1} in [A]

Figure 3.18: Experimental results of the qZSI under a load step-down change.

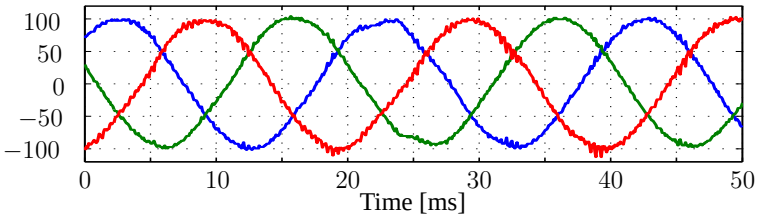
3.6.3.1 Load Step Change

In this test, the the resistive part of the RL load is step changed from full load ($35\,\Omega$) to half load ($70\,\Omega$), and vice versa, while keeping the input voltage constant at $160\,\text{V}$.

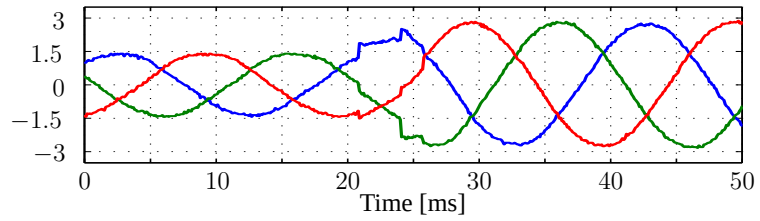
When the load is step changed from full to half load, the corresponding ac- and dc-side results



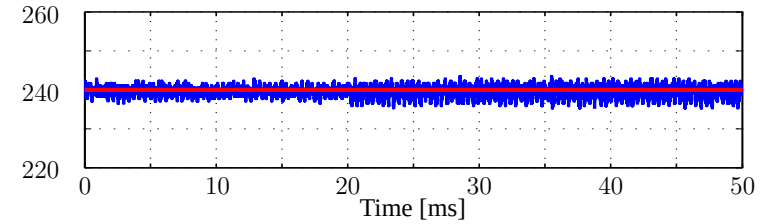
(a) d-component of the output voltage and its reference in [V].



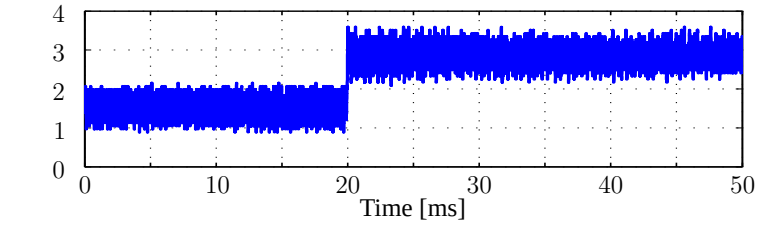
(b) Three-phase output voltage $\boldsymbol{v}_{\text{o,abc}}$ in [V].



(c) Three-phase output current $\boldsymbol{i}_{\text{o,abc}}$ in [A].



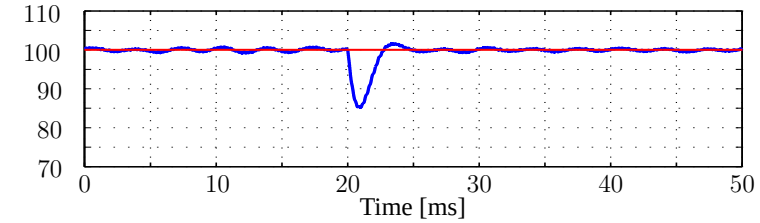
(d) Dc-link voltage v_{dc} and its reference in [V].



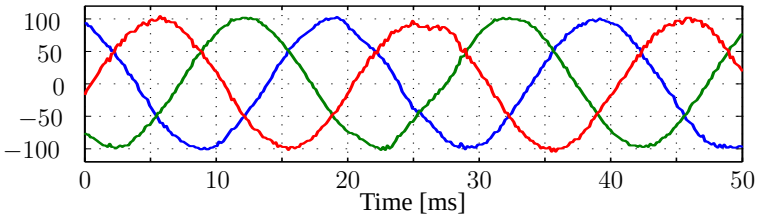
(e) Inductor current i_L in [A].

Figure 3.19: Experimental results of the two-stage inverter under load step-up change.

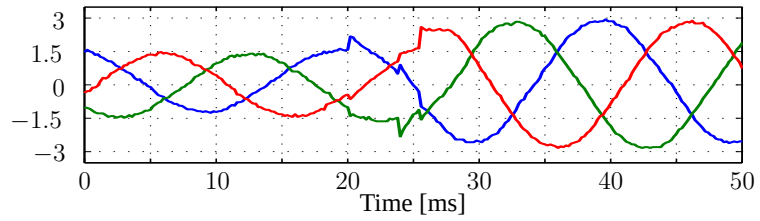
are displayed in Figures 3.17 and 3.18 for the two-stage inverter and qZSI, respectively. With both inverters, the output voltage is well tracked with a small variation during the transient time as demonstrated in Figures 3.17(b) and 3.18(b). According to the d-component of the output voltage shown in Figures 3.17(a) and 3.18(a), the output voltage stays within its nominal value before and after the step change. In the dc side of the two-stage inverter and the qZSI, the dc-



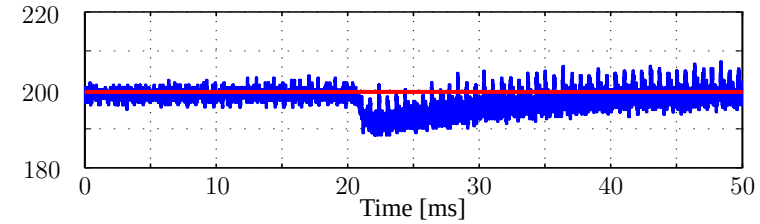
(a) d-component of the output voltage and its reference in [V].



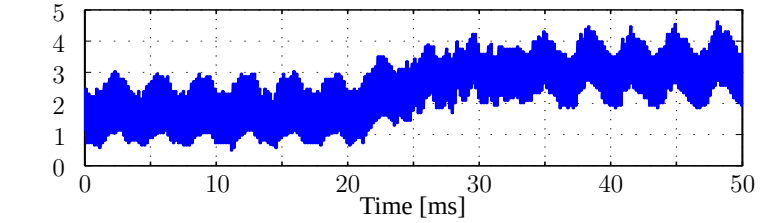
(b) Three-phase output voltage $\boldsymbol{v}_{\text{o,abc}}$ in [V].



(c) Three-phase output current $\boldsymbol{i}_{\text{o,abc}}$ in [A].



(d) Capacitor voltage v_{C_1} and its reference in [V].

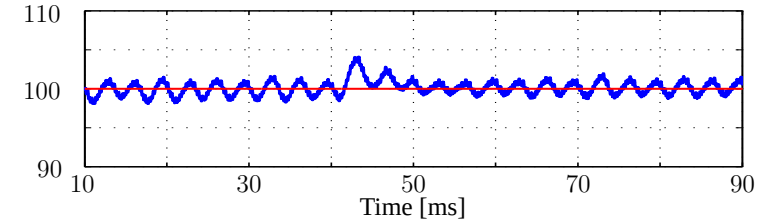


(e) Inductor current i_{L_1} in [A].

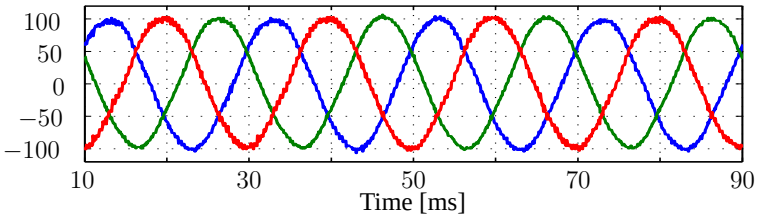
Figure 3.20: Experimental results of the qZSI under a load step-up change.

link voltage and the capacitor voltage are regulated along their references before and after the step change as can be seen in Figures 3.17(d) and 4.9(a).

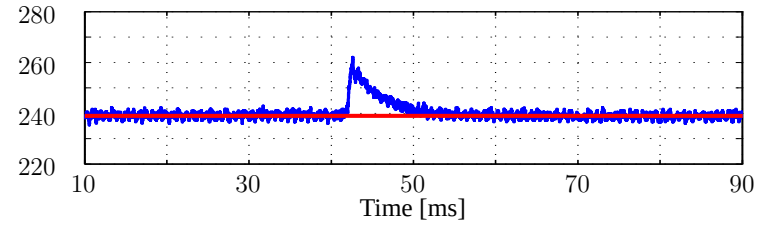
Afterwards, the load is step changed from half to full load. The experimental results for the two-stage inverter and qZSI are shown in Figures 3.19 and 3.20, respectively. It can be observed



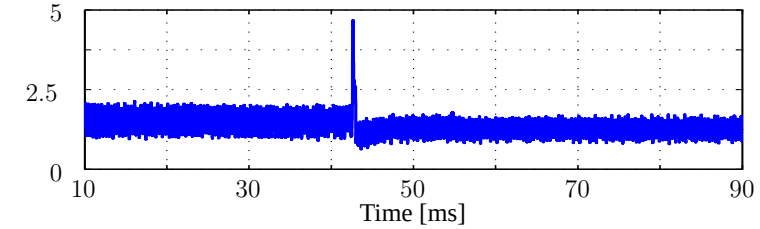
(a) d-component of the output voltage and its reference in [V].



(b) Three-phase output voltage $\boldsymbol{v}_{\text{o,abc}}$ in [V].



(c) Dc-link voltage v_{dc} and its reference in [V].



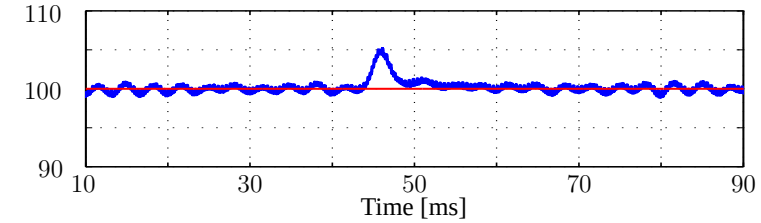
(d) Inductor current i_L in [A].

Figure 3.21: Experimental results of the two-stage inverter under input voltage step change.

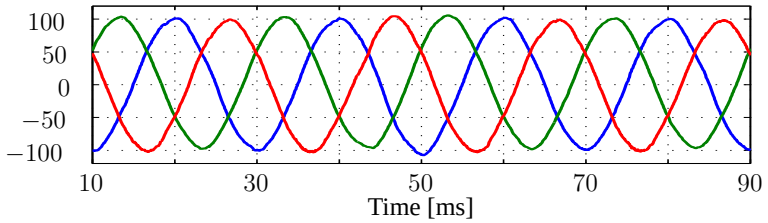
that the ac-side performances of the both inverters are comparable; however, the qZSI shows smaller voltage undershoot as can be seen in Figures 3.19(a) and 3.20(a).

3.6.3.2 Input Voltage Step Change

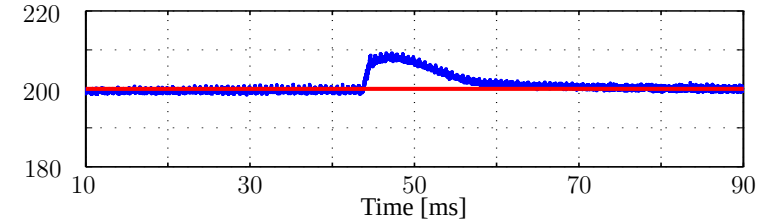
As previously mentioned, the qZSI proposes an attractive solution for the PV systems. In such a case, the resulting dc voltage from the PV is not constant, where it changes with the temperature and the solar radiation level during the day. In order to examine the performance of both inverters under this condition, the input voltage is step-changed from $160\,\text{V}$ to $190\,\text{V}$, while keeping the output voltage reference at $100\,\text{V}$, the capacitor voltage reference at $200\,\text{V}$, the dc-link voltage at $240\,\text{V}$. The dc- and ac-side results of the two-stage inverter and qZSI are shown in Figures 3.21 and 3.22, respectively.



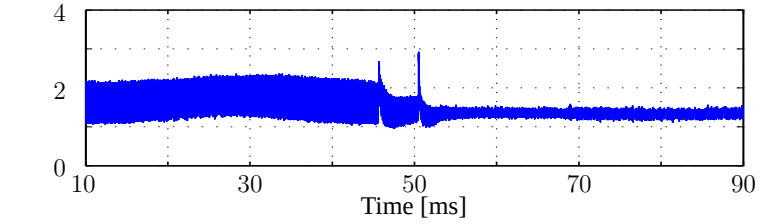
(a) d-component of the output voltage and its reference in [V].



(b) Three-phase output voltage $\boldsymbol{v}_{\text{o,abc}}$ in [V].



(c) Capacitor voltage v_{C_1} and its reference in [V].



(d) Inductor current i_{L_1} in [A].

Figure 3.22: Experimental results of the qZSI under input voltage step change.

According to Figures 3.21 and 3.22, the dc-side variables of both inverters have comparable performances. However, the inductor current shows lower overshoot in case of the qZSI than the two-stage inverter, see Figures 3.21(d) and 3.22(d). As for the ac-side, both inverters show very good transient responses with very short transient times as displayed in Figures 3.21(b) and 3.22(b). These results highlight the effectiveness of the qZSI as a single-stage inverter for PV systems.

3.7 Summary

This chapter conducts a comparison between the conventional two-stage inverter and the newly proposed qZSI in terms of the voltage stress on the inverter switches, passive components requirements, steady-state and transient responses, and efficiency. In this comparison, both inverters are connected to an RL via an intermediate an LC filter. Multi-loop linear PI controllers are designed in order to achieve output voltage regulation and disturbance rejection.

As it is shown, the qZSI results in lower voltage stress on the switches than the traditional inverter when the operating voltage gain is in the range of (1-2). The experimental results demonstrate that the qZSI exhibits lower output voltage THD and higher efficiency than the traditional two-stage inverter. The results also point out the ability of the inverters to respond quickly to the load and the input voltage change, where the transient and steady state response are comparable for both inverters. Thus, these results verify the proposed qZSI as an alternative inverter for DG applications combined with many advantages.

CHAPTER 4

Proportional-Resonant Controller Design

This chapter proposes the design and digital implementation of a PR controller of the qZSI for UPS applications as an alternative to the classical PI control. The main goal is to improve the output voltage quality when the inverter is connected to nonlinear loads.

4.1 Motivation

In UPS systems, regardless the load type, linear or nonlinear, a high quality output voltage in desirable. However, the nonlinear output current, introduced by nonlinear loads, results in a highly distorted output voltage. The conventional PI controller designed in the previous chapter can not solve this problem.

One of the promising control techniques that is recently established for UPS systems is the PR controller [4, 83–86], in which the classical integral (I) controller is replaced by a resonant (R) one. First, at the resonant frequency, the PR controller does not exhibit a phase delay. In addition, by having an infinite gain at the fundamental frequency, the PR controller achieves robust reference tracking, zero steady-sate error, and fast disturbance rejection [87–89]. One more advantage of the PR controller is that it is designed in the stationary $\alpha\beta$ reference frame without a need for multiple transformations from/to the rotating dq reference frame, as this is the case for PI controller. This in turn results in a reduction of the controller computational demand. In order to compensate for selective low-order harmonics, multiple R controllers are added in parallel to the fundamental control algorithm [90–92]. Thus, in addition to the stated characteristics of the PR controller, the output voltage distortion can be canceled.

Recently, the PR controller has been applied with the ZSI, i.e. [93, 94]. A point to note is that in these works the PR controller has been investigated only with linear loads. In this chapter therefore the PR controller is designed to control the output voltage of the qZSI that subject to linear/nonlinear load currents. In addition, the capacitor voltage of the qZS network is adjusted by a PI controller. In order to fully utilize the dc-link voltage while keeping the

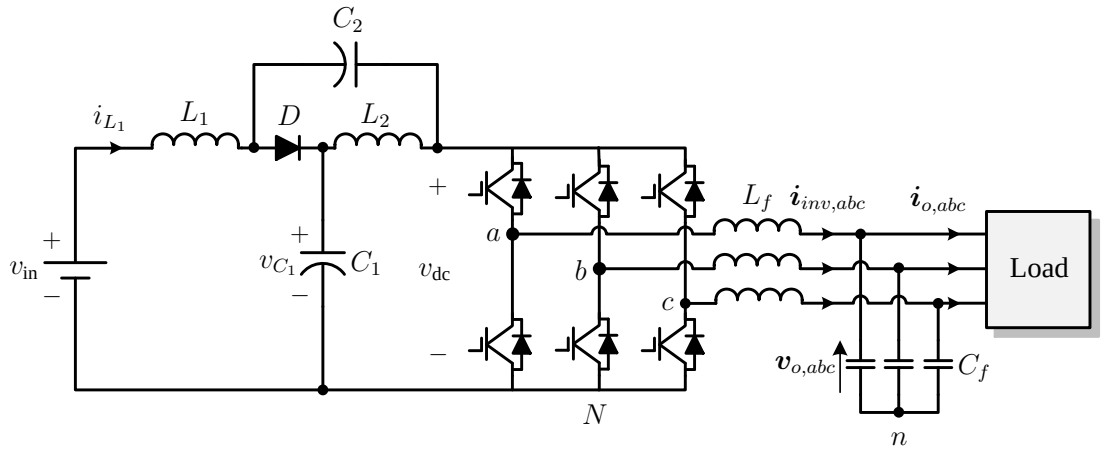


Figure 4.1: The quasi-Z-source inverter connected with an LC filter and a load.

switching frequency low, the SVPWM6 technique, presented in chapter 2, is used to generate the converter switching signals. In order to examine the steady-state and transient operation of the qZSI under different loads, experimental results based on an FPGA are presented to prove the efficacy of the proposed controller.

This chapter is structured as follows. Section 4.2 introduces the system description. The proposed control strategy is presented in Section 4.3, while the experimental results are provided in Section 4.4. Finally, Section 4.5 draws the conclusion.

4.2 System Description

The system under investigation is shown in Figure 4.1. It consists of a quasi-Z-source (qZS) network, a three-phase VSI, an LC filter, and a load. In this configuration, the load can linear or nonlinear. The mathematical model derived in chapter 3 will be used here in order to design the controller for both sides of the converter.

4.3 Controller Design

In this work, both dc and ac sides of the qZSI are separately controlled. The capacitor voltage v_{C_1} is adjusted to its reference value $v_{C_1,\text{ref}}$ on the dc side. On the other hand, the ac-side controller regulates the output voltage $\boldsymbol{v}_o$ of the LC filter along its reference value $\boldsymbol{v}_{o,\text{ref}}$.

4.3.1 DC-Side Controller

On the dc side, a conventional PI controller is designed to regulate the capacitor voltage v_{C_1} of the qZS network. As can be observed from the mathematical model derived in chapter 3 that the qZSI exhibits a right-half plane (RHP) zero which in turn leads to a nonminimum phase system. This phenomena requires much attention in designing the control parameters in order to guarantee the system stability [95, 96]. The open-loop system of the dc side $G_1(s)$, is given by equation (3.23) in chapter 3.

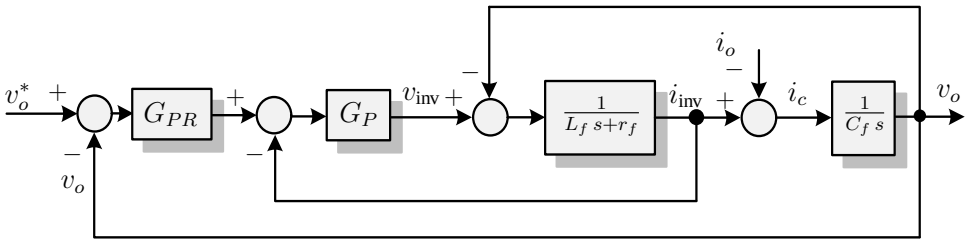


Figure 4.2: Ac-side controller scheme.

The system parameters are $v_{\text{in}} = 160\,\text{V}$, $v_{C_1} = 250\,\text{V}$, $L_1 = L_2 = 500\,\mu\text{H}$, $C_1 = C_2 = 480\,\mu\text{F}$, and the switching frequency $f_{sw} = 10\,\text{kHz}$. Based on these parameters, the coefficients of the closed loop system are calculated. Then, by utilizing Routh-Hurwitz stability criterion, the PI controller parameters are chosen. To achieve a satisfactory performance [97, 98], the PI parameters have been tuned in order to meet the stability margins, i.e. a gain margin of $10\,\text{dB}$ and phase margin of $> 45\,\text{degrees}$. Accordingly, the PI parameters are chosen as $K_p = 4e^{-4}$ and $K_i = 0.05$.

4.3.2 AC-Side Controller

4.3.2.1 PR Controller Design

As for the ac-side controller, a cascaded control loop is utilized as shown in Figure 4.2. The inner control loop is a feedback current loop (P controller) that provides compensation for the input voltage and load disturbances as well as the phase delay caused by the LC filter. The outer voltage loop, PR controller, generates the reference current for the inner current loop. The ideal PR controller is given by

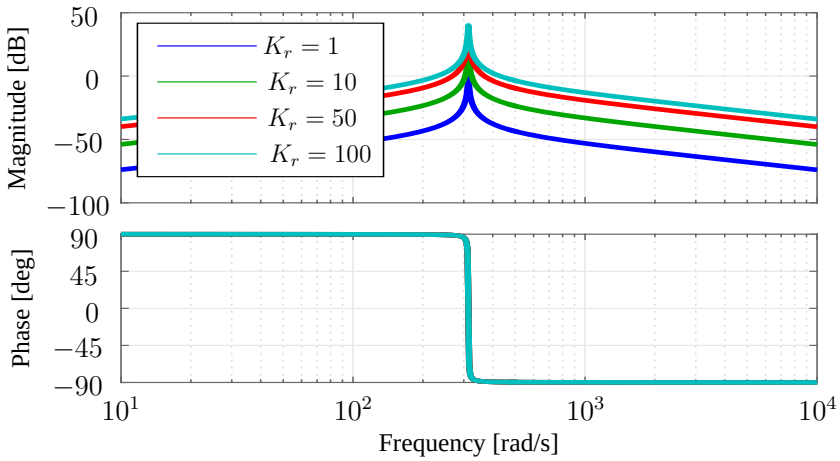
$$G_{PR}(s) = K_{pr} + \frac{2K_r s}{s^2 + \omega_0^2}\,, \tag{4.1}$$

with ω_0, K_{pr}, and K_r being the fundamental angular frequency, proportional coefficient, and resonant coefficient, respectively. K_{pr} is designed and tuned in the same way of the proportional gain K_p of the PI controller. However, the ideal resonant (R) controller has an infinite gain at the frequency of ω_0, while it does not give phase shift or gain at other frequencies. This in turn prevents its implementation in reality. To overcome this problem, the *non-ideal* PR controller is introduced [86, 91]

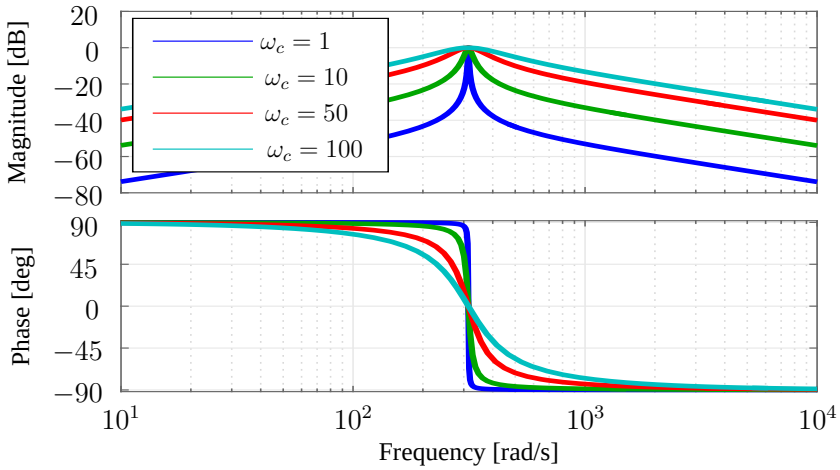
$$G_{PR}^{\dagger}(s) = K_{pr} + \frac{2K_r\omega_c s}{s^2 + 2\omega_c s + \omega_0^2}\,, \tag{4.2}$$

with ω_c being the cut-off frequency. The PR controller presented in (4.2) acts as a high-gain low-pass filter which results in a finite gain and a wider bandwidth [89].

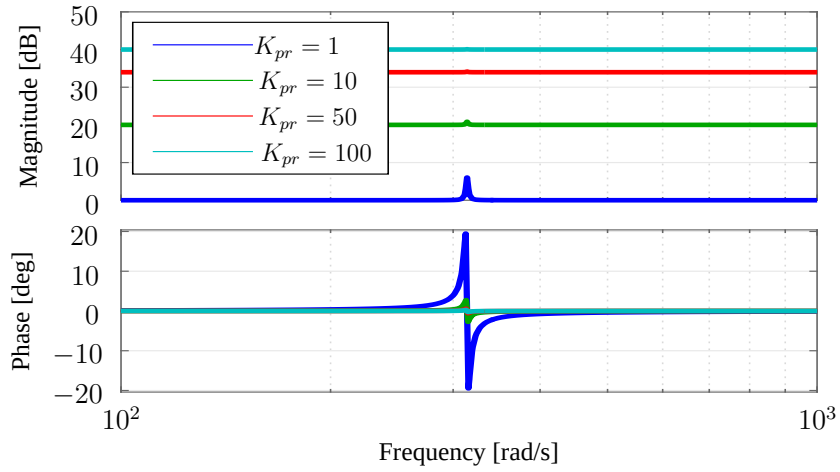
In order to clearly show the influence of the PR parameters, i.e. K_{pr}, K_r, and ω_c, we assume that two of the parameters are fixed so that the effect of varying the third parameter can be noted. As a first step, we assume that $K_{pr} = 0$ and $\omega_c = 1$, Figure 4.3(a) highlights that the change in K_r affects the magnitude of the PR controller, while the bandwidth is unchanged.



(a) Changing K_r.



(b) Changing ω_c.



(c) Changing K_{pr}.

Figure 4.3: Influence of varying K_r, ω_c, and K_{pr} on the PR response.

Figure 4.3(b) shows the influence of varying ω_c when $K_{pr} = 0$ and $K_r = 1$. It can be noted that both the system magnitude and phase are affected by changing ω_c.

Finally, the effect of adding K_{pr} to the controller is investigated as shown in Figure 4.3(c). By increasing K_{pr} the magnitude increases; however, the system phase decreases. Thus, the harmonic impedance increases when K_{pr} increases which results in low harmonic component. Accordingly, K_{pr} can be chosen such that high performance reference tracking and disturbance rejection are obtained.

In order to compensate for selective low-order harmonics (e.g. 5^{th}, 7^{th} $\cdots$), the following multi-resonant controller is structured.

$$G_{PR}(s) = K_{pr} + \sum_{i=5,7,\cdots} \frac{2K_{r_i}\omega_c s}{s^2 + 2\omega_c s + (i\omega_o)^2}\,, \tag{4.3}$$

where i and K_{r_i} denote the harmonic order and its individual resonant gain, respectively. To achieve a satisfactory performance, the PR controller is designed with the fundamental frequency in addition to the 5^{th}, 7^{th}, and 9^{th} harmonics.

4.3.2.2 Digital Implementation of PR controller

In order to implement the PR controller described by (4.3) in real-time (i.e. in FPGA), it has to be first discretized. Based on a comparison among several discretization techniques for R controllers in [99], Tustin transformation technique has been chosen for this work. Due to its accuracy in most applications, Tustin transformation is a typical choice in digital control systems, where it achieves infinite gain in open loop and has relatively low steady state error at fundamental frequency and low order harmonics.

Tustin transformation is achieved by substituting the Laplace variable s in (4.3) by $\frac{1-z^{-1}}{1+z^{-1}} \cdot \frac{2}{T_s}$, where T_s is the sampling time. Consequently, the continuous-time domain PR controller in (4.3) can be written in a discrete form as

$$G_{PR}(z) = K_{pr} + \sum_{i=5,7,\cdots} \frac{n_{0_i} - n_{2_i}\, z^{-2}}{d_{0_i} + d_{1_i}\, z^{-1} + d_{2_i}\, z^{-2}}\,, \tag{4.4}$$

where

$$n_{0_i} = n_{2_i} = 4K_{r_i}\,\omega_c\,T_s\,, \tag{4.5a}$$
$$d_{0_i} = (i\omega_o)^2\,T_s^2 + 4\omega_c\,T_s + 4\,, \tag{4.5b}$$
$$d_{1_i} = 2(i\omega_o)^2\,T_s^2 - 8\,, \tag{4.5c}$$
$$d_{2_i} = (i\omega_o)^2\,T_s^2 - 4\omega_c\,T_s + 4\,. \tag{4.5d}$$

By computing the controller coefficients in (4.5) at the fundamental and low-order harmonics (3^{rd}, 5^{th}, 7^{th}, and 9^{th}), the PR controller can be implemented in an FPGA as will be shown in Section 4.4. Based on the analysis presented in Figure 4.3 and inline with the main goal of this work (to ensure system stability and have a high performance controller), the PR parameters are chosen as $K_{pr} = 0.4$, $K_{r_1} = 550$, K_{r_5}, K_{r_7}, and $K_{r_9} = 50$, and $\omega_c = 0.5$.

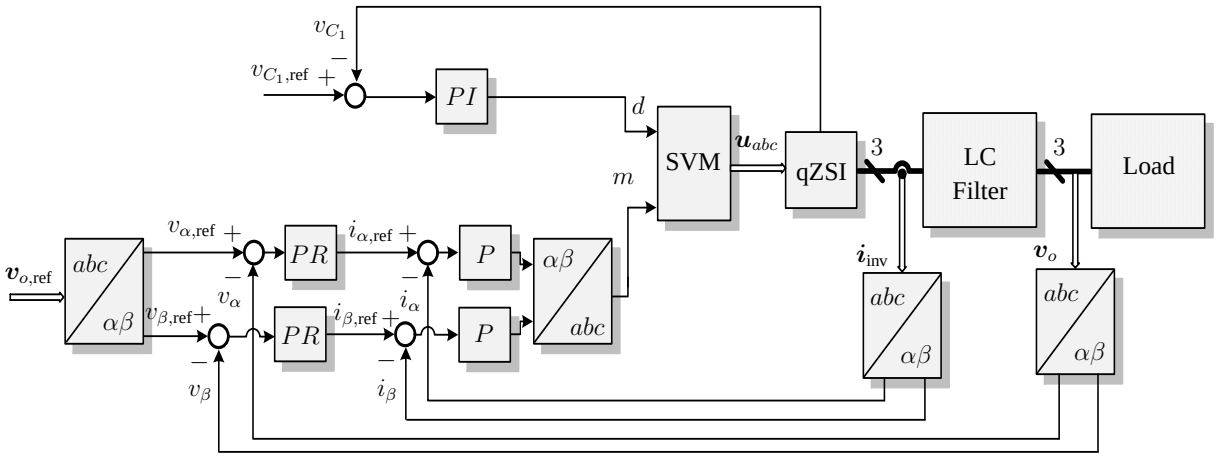


Figure 4.4: Voltage control scheme based on PR controller for the qZSI.

4.3.3 Overall Control Block Diagram

As a final stage, both the output of the dc-side controller (the shoot-through duty cycle d) and the ac-side controller (the inverter modulation index m) are delivered to the SVPWM block in order to generate the gating signals for the inverter switches. In this work, the SVPWM with six insertion (SVPWM6) is utilized, where the shoot-through time is split into six equal partitions in one sampling interval and inserted into the transition moment of switching states. According to [70], in comparison with the sinusoidal PWM techniques, this method results in lower voltage stress and inductor current ripples as well as achieves a higher voltage gain and full utilization for the dc-link voltage. The proposed overall control scheme for both sides of the qZSI is illustrated in Figure 4.4.

4.4 Experimental Evaluation

To investigate the behavior of the proposed PR control strategy for the qZSI configuration shown in Figure 6.1, several experiments based on an FPGA have been conducted. Both dc- and ac-side controllers along with the SVPWM6 modulation technique are implemented in the FPGA as shown in Figure 4.5. For more details about the test bench, please refer to appendix C.

Some of the system parameters are already defined in Section 4.3.1. The output filter parameters are $L_f = 10\,\text{mH}$ and $C_f = 50\,\mu\text{F}$. In addition, the reference output voltage $\boldsymbol{v}_{o,\text{ref}}$ is set to $100\,\text{V}$. According to [24, 25], the capacitor voltage reference $v_{C_1,\text{ref}}$ should be more than double of output voltage reference in order not to affect the sinusoidal waveform of the output voltage. Hence, the capacitor voltage reference is chosen to be $250\,\text{V}$.

4.4.1 Steady-State Operation

The proposed controller is investigated with a linear load represented by RL ($20\,\Omega$, $2.4\,\text{mH}$) and a nonlinear load in the form of a three-phase diode-bridge rectifier connected with a $C_L = 220\,\mu\text{F}$ filter and $R_L = 60\,\Omega$ load as illustrated in Figure 4.6.

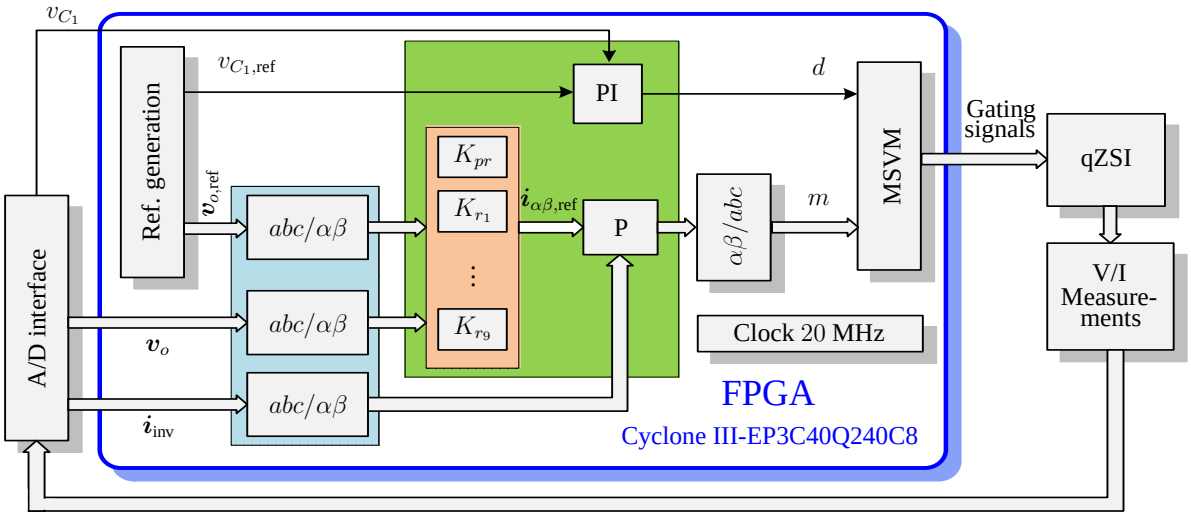


Figure 4.5: FPGA implementation of PR controller for the qZSI.

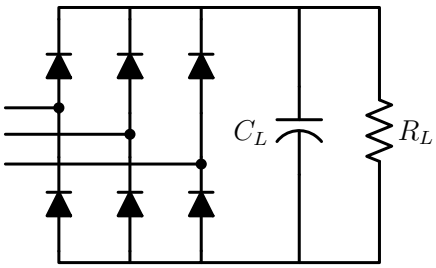


Figure 4.6: Nonlinear load represented by a diode-bridge rectifier with $C_L = 220\,\mu$F and $R_L = 60\,\Omega$.

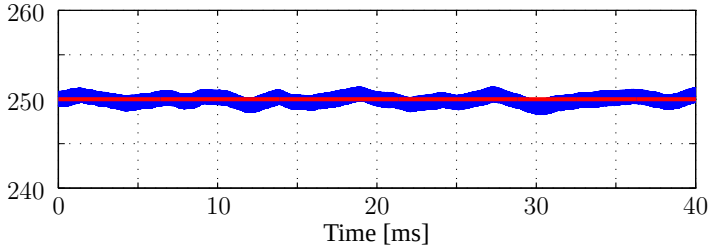
4.4.1.1 Linear Load

The experimental results of the dc and ac side of the qZSI with the RL load are shown in Figure 4.7. As can be observed in Figure 4.7(a), the capacitor voltage effectively tracks its reference at 250 V resulting in a peak dc-link voltage $\hat{v}_{\text{dc}} = 340$ V (Figure 4.7(c)). With regards to the ac side, Figure 4.7(d) shows that the output voltage is accurately regulated along its reference with low THD (1.85%) resulting in a sinusoidal output voltage.

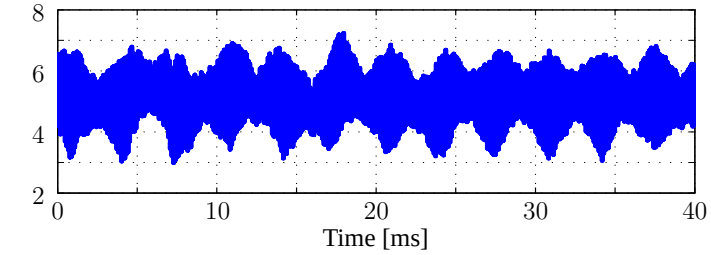
4.4.1.2 Nonlinear Load

Furthermore, the proposed PR control strategy is examined with the nonlinear load. The dc- and ac-side results are shown in Figure 4.8. The capacitor voltage is regulated along its reference as can be seen in Figure 4.8(a) resulting in a fixed boosted dc-link voltage of $340\,V$.

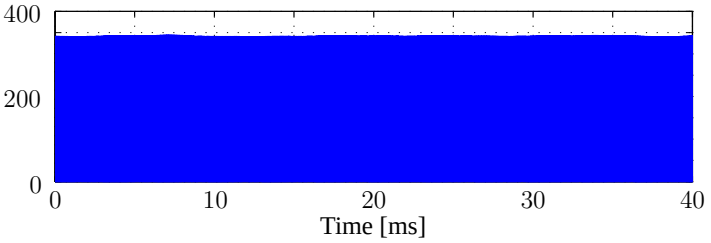
Despite of the non linearity of the load resulting in a highly distorted output current (see Figure 4.8(e)), the output voltage remains sinusoidal with a THD of 2.47% (see Figure 4.8(d)). These results confirm that the PR controller successfully compensates for the desired harmonics. As a result, the PR controller is able to produce low THD output voltage not only with linear loads, but also with nonlinear loads.



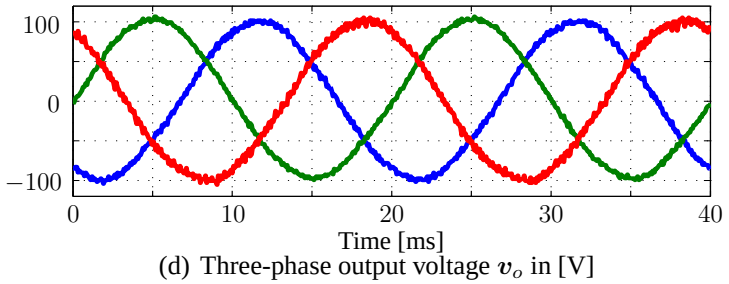
(a) Capacitor voltage v_{C_1} and its reference in [V]



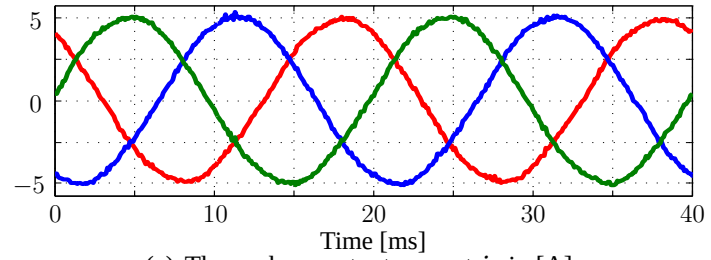
(b) Inductor current i_{L_1} in [A]



(c) Dc-link voltage v_{dc} in [V]

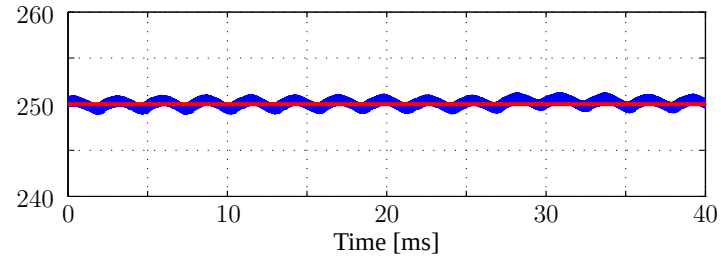


(d) Three-phase output voltage $\boldsymbol{v}_o$ in [V]

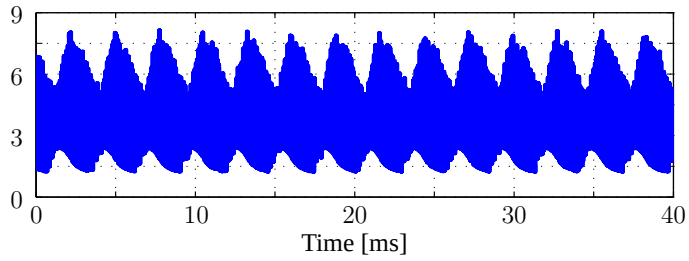


(e) Three-phase output current $\boldsymbol{i}_o$ in [A]

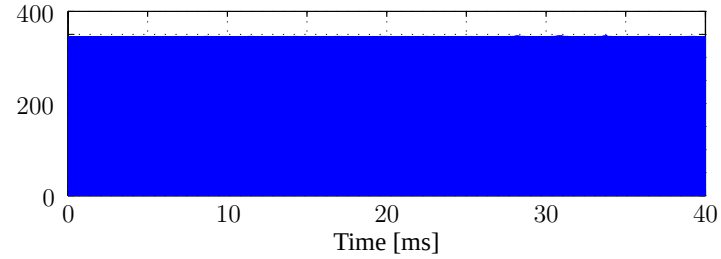
Figure 4.7: Experimental results of the dc and ac side of the qZSI. RL load $= 20\,\Omega,\ 2.4\,\text{mH}$, and $f_{\text{sw}} = 10\,\text{kHz}$. Voltage THD $= 1.85\%$.



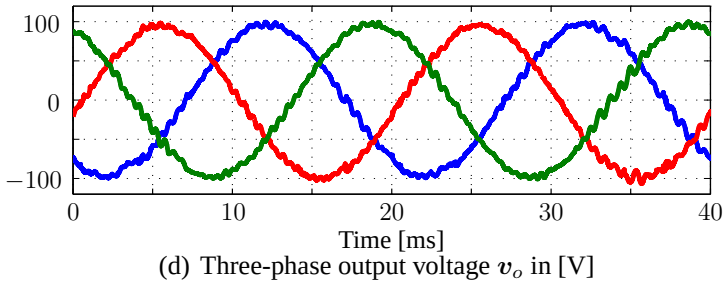
(a) Capacitor voltage v_{C_1} and its reference in [V]



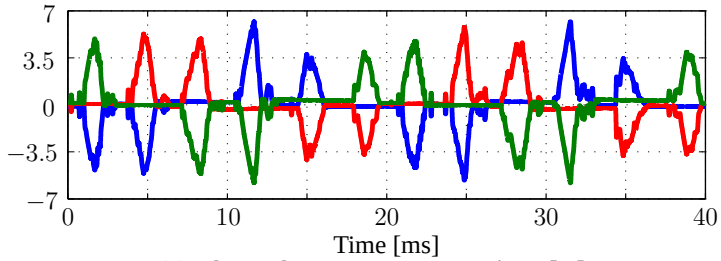
(b) Inductor current i_{L_1} in [A]



(c) Dc-link voltage v_{dc} in [V]

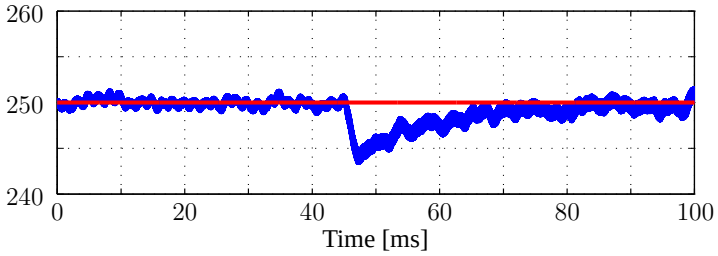


(d) Three-phase output voltage $\boldsymbol{v}_o$ in [V]

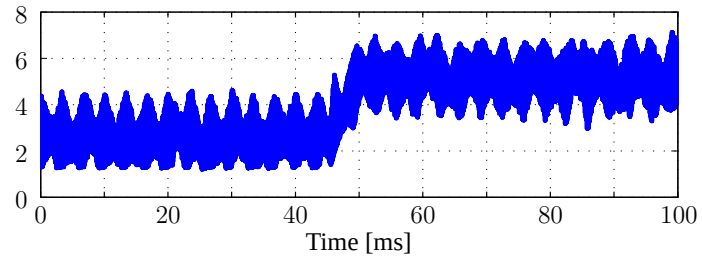


(e) Three-phase output current $\boldsymbol{i}_o$ in [A]

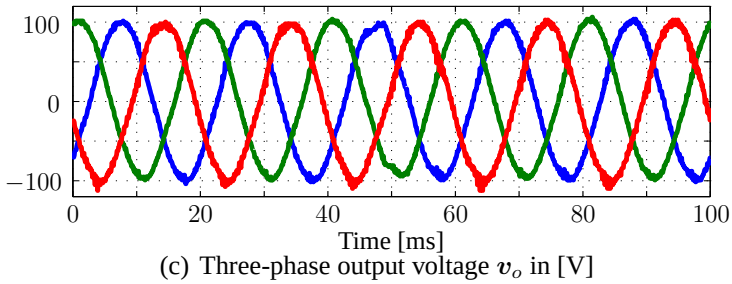
Figure 4.8: Experimental results of the dc and ac side of the qZSI with nonlinear load. $f_{\text{sw}} = 10\,\text{kHz}$ and Voltage THD $= 2.47\%$.



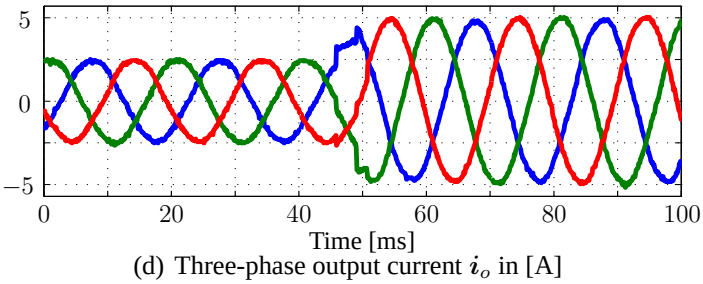
(a) Capacitor voltage v_{C_1} and its reference in [V]



(b) Inductor current i_{L_1} in [A]



(c) Three-phase output voltage $\boldsymbol{v}_o$ in [V]



(d) Three-phase output current $\boldsymbol{i}_o$ in [A]

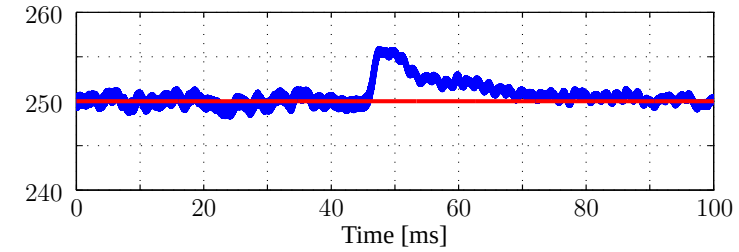
Figure 4.9: Experimental results of both sides of the qZSI under a step up change in the resistive-inductive load.

4.4.2 Transient Response

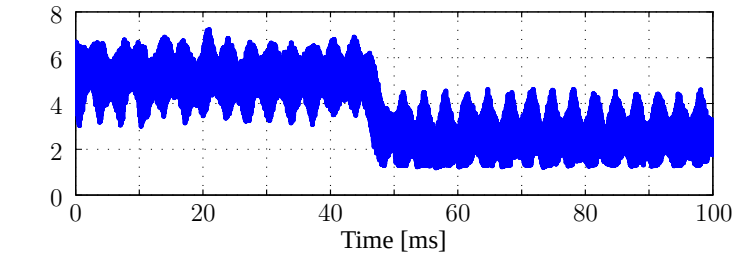
The transient operation of the PR controller is investigated with a resistive-inductive (RL) and nonlinear load.

4.4.2.1 Linear Load

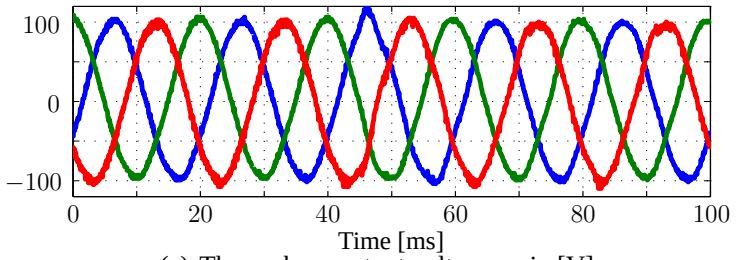
In the first case, the RL load is step changed from half load ($40\,\Omega$, $2.4\,$mH) to full load ($20\,\Omega$, $2.4\,$mH), and vice versa. Figures 4.9 and 4.10 show the dc- and ac-side results, respectively.



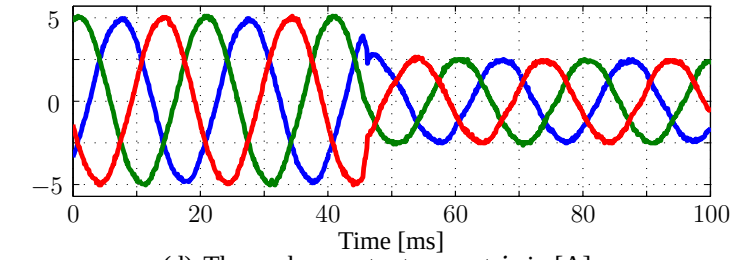
(a) Capacitor voltage v_{C_1} and its reference in [V]



(b) Inductor current i_{L_1} in [A]



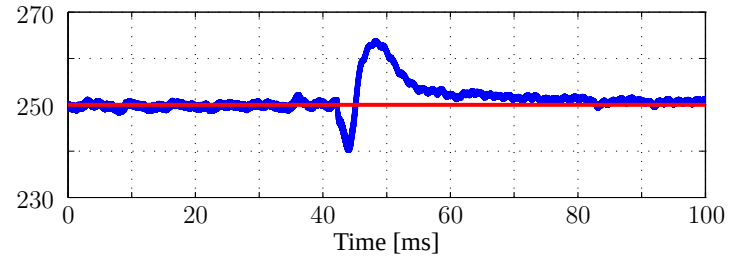
(c) Three-phase output voltage $\boldsymbol{v}_o$ in [V]



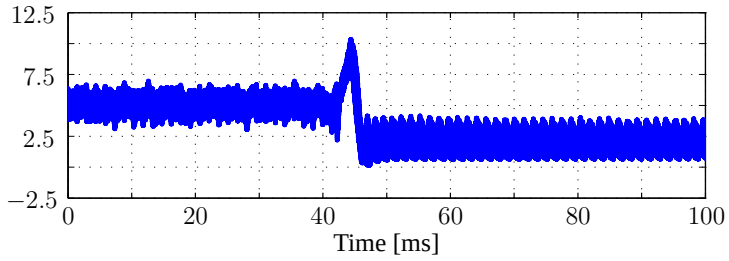
(d) Three-phase output current $\boldsymbol{i}_o$ in [A]

Figure 4.10: Experimental results of both sides of the qZSI under a step down change in the resistive-inductive load.

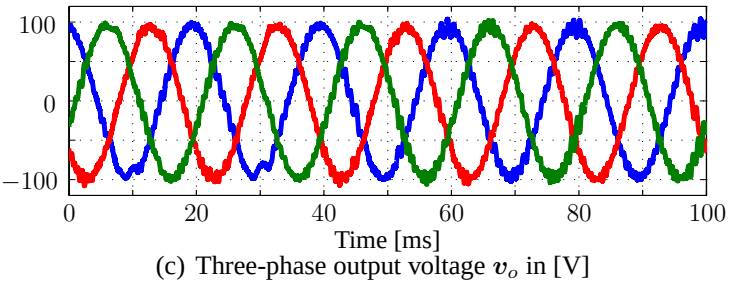
As can be seen in Figures 4.9(a) and 4.10(a), the capacitor voltages successfully track their references before and after the step change occurs with small over- and under shoot, respectively. As a consequence, the inductor currents are settled to new nominal values (see Figures 4.9(b) and 4.10(b)). As for the ac side, the proposed PR controller manages to quickly adjust the output voltage to its reference value after a very short transient time as shown in Figures 4.9(c) and 4.10(c), where Figures 4.9(d) and 4.10(d) depict the output current waveform for both cases, respectively. These outcomes emphasize that the PR controller is able to handle the system dynamics and provide a perfect disturbance rejection.



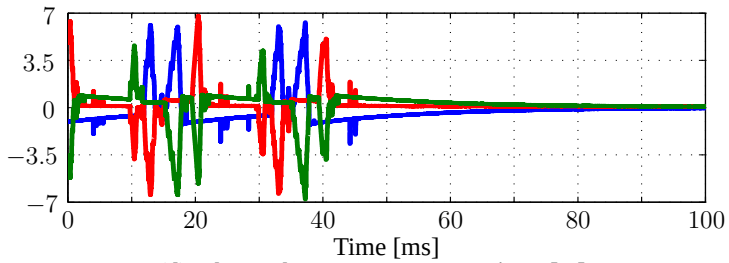
(a) Capacitor voltage v_{C_1} and its reference in [V]



(b) Inductor current i_{L_1} in [A]



(c) Three-phase output voltage $\boldsymbol{v}_o$ in [V]



(d) Three-phase output current $\boldsymbol{i}_o$ in [A]

Figure 4.11: Experimental results of both sides of the qZSI under a step change in the nonlinear load. $f_{\text{sw}} = 10\,\text{kHz}$.

4.4.2.2 Nonlinear Load

The second experiment investigates the proposed PR controller for qZSI under step change in the nonlinear load. In this case, the load is changed from full load to no load. The experimental results of both dc- and ac-side variables are displayed in Figure 4.11.

On the dc side, the capacitor voltage is well regulated around its reference value at $250\,\text{V}$ (see Figure 4.11(a)) resulting in a new nominal value for the inductor current after the step change occurs, see Figure 4.11(b). On the other hand, the output voltage (in Figure 4.11(c)) shows a very good performance when the nonlinear load is disconnected at $t \approx 40\,\text{ms}$ as presented in

Figure 4.11(d). Although the THD of the output voltage increases after the step change, the output voltage is still a perfect sinusoidal waveform. In UPS system, it is essential to have such a regulated sinusoidal output voltage waveform under all conditions.

4.5 Summary

This chapter proposes a PR controller of the qZSI connected to linear/nonlinear loads via an LC filter for UPS applications. The main aim is to improve the quality of the output voltage when subject to nonlinear loads. This is done by extending the PR controller to also compensates for selected low-order harmonics (5^{th}, 7^{th}, and 9^{th} harmonics). Subsequently, the output voltage is kept sinusoidal waveform with both linear and nonlinear loads. As for the dc side of the qZSI, a PI controller is designed to adjust the capacitor voltage.

The performance of the PR controller with the qZSI is experimentally examined based on FPGA. The experimental results show the effectiveness of the proposed controller both in steady-state and transient operations with both linear and nonlinear loads. Under all examined conditions, the output voltage is kept fully regulated sinusoidal waveform. These results assure the advantages of the PR controller as a promising control strategy for DG applications

Part III

Direct Model Predictive Control

CHAPTER 5

Direct Model Predictive Current Control Strategy

This chapter presents a direct model predictive current control strategy for the qZSIs. To improve the closed-loop performance of the converter a long prediction horizon is implemented. However, the underlying optimization problem may become computationally intractable because of the substantial increase in the computational power demands, which in turn would prevent the implementation of the control strategy in real time. To overcome this and to solve the problem in a computationally efficient manner, a branch-and-bound strategy is used along with a move blocking scheme. In addition, the conventional PI control based on PWM is designed for the qZSI in order to be compared with the proposed MPC.

5.1 Motivation

Motivated by the complexity of the qZSI and the advantages of MPC, a few research works have been recently published focusing on MPC for ZSI/qZSI, see e.g. [100–105]. It is worth mentioning, though, that in these works MPC is used in its simplest form, akin to a deadbeat controller. Specifically, a one-step horizon MPC is implemented, the goal of which is to eliminate the output error as fast and as much as possible within this short horizon. This forces the controller to take aggressive actions which may cause stability problems. For instance, short-horizon MPC cannot always deal with the nonminimum phase nature of the dc side of the qZSI. More specifically, due to the reverse capacitor voltage response during transients, a sufficiently long prediction horizon is required so that the controller can accurately predict not only that initial adverse system behavior, but also beyond that. In other words, the MPC scheme should be able to "see" beyond the initial reverse-response system behavior in order to ensure closed-loop stability.

As a consequence, the short-horizon MPC is not always sufficient to achieve a good system performance, especially when applied to complex systems such as the qZSI. Recent works, such as [106–108] have shown that long-horizon MPC can significantly improve the system perfor-

mance by reducing the current total harmonic distortion (THD). Moreover, apart from a very few cases (see [109, Chap. 10] and references therein for a short discussion), in the one-step horizon MPC formulations the switching effort penalization is not taken into account which is in contrast to the optimal control paradigm [44]. As a result, the switching frequency is not directly controlled, but merely an upper bound is imposed on it, as defined by the sampling interval. This implies that the converter operates at the highest achievable switching frequency which in turn leads to high switching losses. I am aware of only one exemption, namely [100], in which the switching frequency of the ZSI is directly controlled with MPC. However, this is not done by penalizing the switching effort, but by adding a switching frequency error term (i.e. the difference between the converter switching frequency and a desired one) to the objective function. Therefore, the formulated optimization problem underlying MPC violates the optimal control paradigm and a smooth transition between consecutive switching transitions is not guaranteed.

In this chapter a long-horizon direct MPC algorithm—implemented as a current controller—is adopted to handle the multiple control objectives, i.e. the regulation of the output current, the inductor current, and the capacitor voltage to their reference values. A discrete-time model of the converter is derived, on which the controller relies to accurately predict the future behavior of the system over the whole operating regime. Besides, a long horizon is implemented so as to achieve an improved performance and to avoid the issues mentioned above. Nevertheless, since the computational complexity grows exponentially with the length of the prediction horizon, strategies need to be employed that balance the trade-off between the length of the prediction horizon and the number of computations required. To keep the computational complexity modest, a branch-and-bound technique [110] is employed and it is combined with a move blocking scheme [111] that yields a nontrivial prediction horizon.

This chapter is structured as follows. In Section 5.2, the continuous- and discrete-time models of the qZSI configuration under investigation are derived. The optimization problem underlying MPC is formulated and solved in Section 5.3. Next, for comparison purposes, a conventional PI-based controller is designed in Section 5.4. In Section 5.5 simulation results are presented, and in Section 5.6 the proposed control strategy is experimentally tested. Section 5.7 summarizes the chapter.

5.2 Mathematical Model

Figure 5.1 shows the configuration of the qZSI consisting of a quasi-Z-source network, a three-phase two-level inverter, and an RL load. With the inductors, L_1, L_2, the capacitors, C_1, C_2, and the diode D, the qZSI manages to boost the input voltage v_{in} to the desired dc-link voltage v_{dc}. Consequently, the qZSI has two modes of operation, namely buck and boost mode. In buck mode, the dc-link voltage is roughly equal to the input voltage, where the qZSI works as the conventional VSI. In boost mode, the qZSI has two types of operating states, namely the non-shoot-through—comprising of the six active and two zero states of the conventional two-level voltage source inverter—and the shoot-through states, see Figure 5.2. Note that in Figure 5.2, NST stands for non-shoot-through and i_{ST} denotes the shoot-through current (i.e. the dc-link current during the shoot-through state).

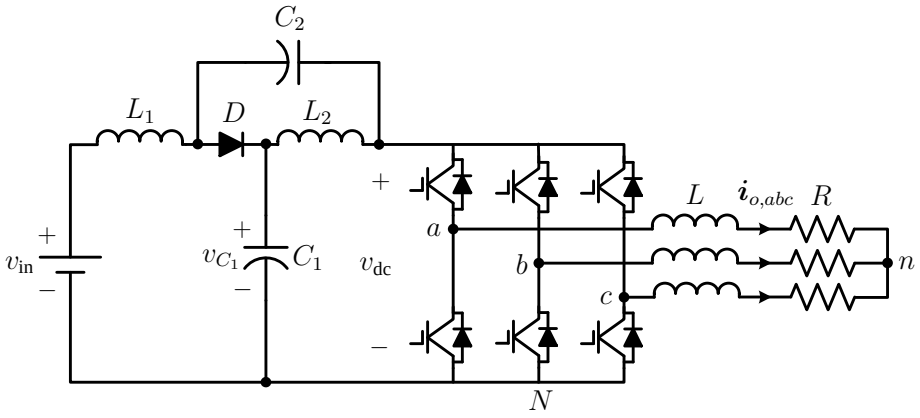
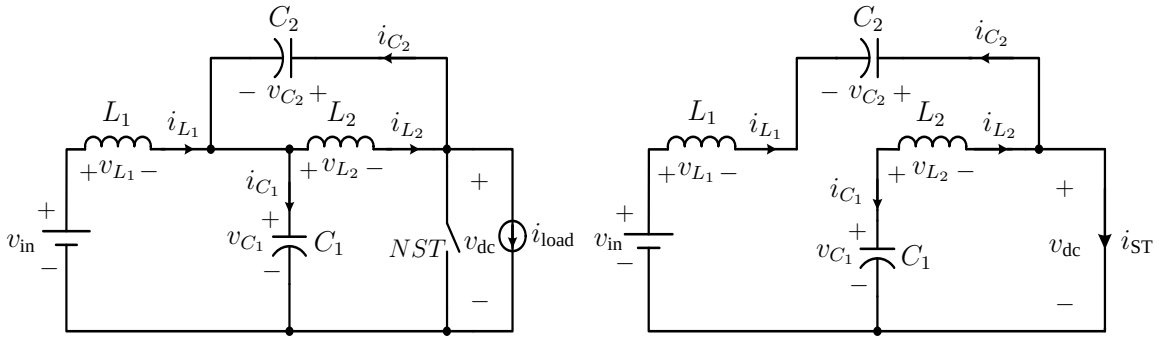


Figure 5.1: The quasi-Z-source inverter connected with an RL load.



(a) Non-shoot-through state.

(b) Shoot-through state.

Figure 5.2: Operation states of the qZSI.

Since the qZSI operates in different modes and states, the associated models will be derived separately. Then, the overall model of the system will be obtained. Note that to simplify the modeling and to ease the computations, the variables are expressed in the stationary orthogonal system $(\alpha\beta)$ instead of the three-phase system (abc). Therefore, a variable $\boldsymbol{\xi}_{abc} = [\boldsymbol{\xi}_a\ \boldsymbol{\xi}_b\ \boldsymbol{\xi}_c]^T$ in the abc system is transformed to a variable $\boldsymbol{\xi}_{\alpha\beta} = [\boldsymbol{\xi}_\alpha\ \boldsymbol{\xi}_\beta]^T$ in the $\alpha\beta$ system through $\boldsymbol{\xi}_{\alpha\beta} = \boldsymbol{K}\boldsymbol{\xi}_{abc}$,[1] where $\boldsymbol{K}$ is the Clarke transformation matrix defined in chapter 3.

The system states include the output current, the inductor currents, and the capacitor voltages. Thus, the state vector is $\boldsymbol{x} = [i_{o,\alpha}\ i_{o,\beta}\ i_{L_1}\ i_{L_2}\ v_{C_1}\ v_{C_2}]^T \in \mathbb{R}^6$. The three-phase switch position $\boldsymbol{u}_{abc} \in \mathcal{U}^3$ is considered as the input to the system, with $\boldsymbol{u}_{abc} = [u_a\ u_b\ u_c]^T$ and $\mathcal{U} = \{0, 1\}$. Moreover, the input voltage is considered as a disturbance to the system, i.e. $\boldsymbol{w} = v_{\text{in}} \in \mathbb{R}$.

As far as the output of the system is concerned, the output and the inductor currents along with the capacitor voltage are considered as the output variables, i.e. $\boldsymbol{y} = [i_{o,\alpha}\ i_{o,\beta}\ i_{L_1}\ v_{C_1}]^T \in \mathbb{R}^4$.

[1] To this end, the subscript for vectors in the $\alpha\beta$ plane is dropped to simplify the notation. Vectors in the abc plane are denoted with the corresponding subscript.

5.2.1 Operation in Boost Mode

The boost mode includes two types of operating states; non-shoot-through and shoot-through state.

5.2.1.1 Non-Shoot-Through State

As can be seen in Figure 5.2(a), at non-shoot-through state the diode is conducting, thus the input voltage source and the inductors deliver energy to the capacitors and the load. Accordingly, the system model is given by

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \boldsymbol{F}_1\boldsymbol{x}(t) + \boldsymbol{G}_1\boldsymbol{u}_{abc}(t) + \boldsymbol{H}\boldsymbol{w}(t) \tag{5.1a}$$

$$\boldsymbol{y}(t) = \boldsymbol{E}\boldsymbol{x}(t)\,, \tag{5.1b}$$

where[2]

$$\boldsymbol{F}_1 = \begin{bmatrix} -\frac{R}{L} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{R}{L} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_2} \\ -\frac{\boldsymbol{u}_{abc}^T\boldsymbol{K}_{(:,1)}^{-1}}{C_1} & -\frac{\boldsymbol{u}_{abc}^T\boldsymbol{K}_{(:,2)}^{-1}}{C_1} & \frac{1}{C_1} & 0 & 0 & 0 \\ -\frac{\boldsymbol{u}_{abc}^T\boldsymbol{K}_{(:,1)}^{-1}}{C_2} & -\frac{\boldsymbol{u}_{abc}^T\boldsymbol{K}_{(:,2)}^{-1}}{C_2} & 0 & \frac{1}{C_2} & 0 & 0 \end{bmatrix},$$

$$\boldsymbol{G}_1 = \hat{v}_{\mathrm{dc}} \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \boldsymbol{K},\ \boldsymbol{H} = \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix},\ \boldsymbol{E} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}.$$

where R (L) is the load resistance (inductance), and $\hat{v}_{\mathrm{dc}}$ is the peak dc-link voltage, see Section 5.2.4.

5.2.1.2 Shoot-Through State

At shoot-through state the input voltage source and the capacitors charge the inductors, while the diode is cut-off, as shown in Figure 5.2(b). During this state, the load is short-circuited since the upper and lower switches in at least one of the three phases are turned on simultaneously,

[2] For a matrix $\boldsymbol{M}$, $\boldsymbol{M}_{(:,i)}$ denotes its ith column.

i.e. $u_x = \bar{u}_x = 1$, where $\bar{u}_x$ denotes the position of the lower switch in phase $x \in \{a, b, c\}$. The converter at the shoot-through state is described by the following expression

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \boldsymbol{F}_2\boldsymbol{x}(t) + \boldsymbol{G}_2\boldsymbol{u}_{abc}(t) + \boldsymbol{H}\boldsymbol{w}(t) \tag{5.2a}$$

$$\boldsymbol{y}(t) = \boldsymbol{E}\boldsymbol{x}(t)\,, \tag{5.2b}$$

where

$$\boldsymbol{F}_2 = \begin{bmatrix} -\frac{R}{L} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{R}{L} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_1} \\ 0 & 0 & 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2} & 0 & 0 & 0 \end{bmatrix},$$

and $\boldsymbol{G}_2$ is the zero matrix of appropriate dimensions. It is worthwhile to mention that, as can be deduced from (5.2), the qZSI in shoot-through state can be considered as an autonomous linear dynamical system with an external disturbance.

5.2.2 Operation in Buck Mode

In buck mode, the qZSI operates as the conventional VSI based on eight switching states (six active states and two zero states). Thus, only the ac side of qZSI is considered for the system model as follows

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \boldsymbol{F}_3\boldsymbol{x}(t) + \boldsymbol{G}_1\boldsymbol{u}_{abc}(t) \tag{5.3a}$$

$$\boldsymbol{y}(t) = \boldsymbol{E}\boldsymbol{x}(t)\,, \tag{5.3b}$$

where

$$\boldsymbol{F}_3 = \begin{bmatrix} -\frac{R}{L} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{R}{L} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}.$$

5.2.3 Continuous-Time Model

Models (5.1), (5.2), and (5.3) can be combined in one model that precisely describes the different operating modes and states of the qZSI. To do so, two auxiliary binary variables d_{aux_1} and d_{aux_2} are introduced. Variable d_{aux_1} indicates the state at which the converter operates when in boost mode, i.e.

$$d_{\text{aux}_1} = \begin{cases} 0 & \text{if non-shoot-through state (active or zero state)} \\ 1 & \text{if shoot-through state} \end{cases} . \tag{5.4}$$

Since the transition from non-shoot-through state to shoot-through state, and vice versa, is input-dependent, (5.4) can be written as

$$d_{\text{aux}_1} = \begin{cases} 0 & \text{if } u_x \neq \bar{u}_x \forall\, x \in \{a,b,c\} \\ 1 & \text{if } \exists\, x \in \{a,b,c\} \text{ s.t. } u_x = \bar{u}_x = 1 \end{cases} . \tag{5.5}$$

Variable d_{aux_2} is used to indicate the operation mode of the converter, i.e.

$$d_{\text{aux}_2} = \begin{cases} 0 & \text{if buck mode} \\ 1 & \text{if boost mode} \end{cases} . \tag{5.6}$$

The transition from the buck mode to the boost mode (and vice versa) depends on whether the output current becomes greater (less) than the current $\boldsymbol{i}_{o,\text{bnd}}$ that defines the boundary between the two modes, see Section 5.2.5. Therefore, (5.6) can be written as

$$d_{\text{aux}_2} = \begin{cases} 0 & \text{if } \boldsymbol{i}_o \leq \boldsymbol{i}_{o,\text{bnd}} \\ 1 & \text{if } \boldsymbol{i}_o > \boldsymbol{i}_{o,\text{bnd}} \end{cases} . \tag{5.7}$$

Taking all the above into account, the full model of the converter can be written as

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \boldsymbol{F}\boldsymbol{x}(t) + \boldsymbol{G}\boldsymbol{u}_{abc}(t) + \boldsymbol{H}\boldsymbol{w}(t) \tag{5.8a}$$

$$\boldsymbol{y}(t) = \boldsymbol{E}\boldsymbol{x}(t)\,, \tag{5.8b}$$

where $\boldsymbol{F} = \boldsymbol{F}_a + d_{\text{aux}_2}\boldsymbol{F}_b$, with $\boldsymbol{F}_a = \boldsymbol{F}_3$ and

$$\boldsymbol{F}_b = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{d_{\text{aux}}-1}{L_1} & \frac{d_{\text{aux}}}{L_1} \\ 0 & 0 & 0 & 0 & \frac{d_{\text{aux}}}{L_2} & \frac{d_{\text{aux}}-1}{L_2} \\ \frac{(d_{\text{aux}}-1)\boldsymbol{u}_{abc}^T\boldsymbol{K}_{(:,1)}^{-1}}{C_1} & \frac{(d_{\text{aux}}-1)\boldsymbol{u}_{abc}^T\boldsymbol{K}_{(:,2)}^{-1}}{C_1} & \frac{1-d_{\text{aux}}}{C_1} & -\frac{d_{\text{aux}}}{C_1} & 0 & 0 \\ \frac{(d_{\text{aux}}-1)\boldsymbol{u}_{abc}^T\boldsymbol{K}_{(:,1)}^{-1}}{C_2} & \frac{(d_{\text{aux}}-1)\boldsymbol{u}_{abc}^T\boldsymbol{K}_{(:,2)}^{-1}}{C_2} & -\frac{d_{\text{aux}}}{C_2} & \frac{1-d_{\text{aux}}}{C_2} & 0 & 0 \end{bmatrix},$$

and $\boldsymbol{G} = (1 - d_{\text{aux}_1})\boldsymbol{G}_1$.

In Figure 5.3 the qZSI represented as an automaton is depicted. As can be seen, the transition from one condition to another is specified by the auxiliary variables d_{aux_1} and d_{aux_2}.

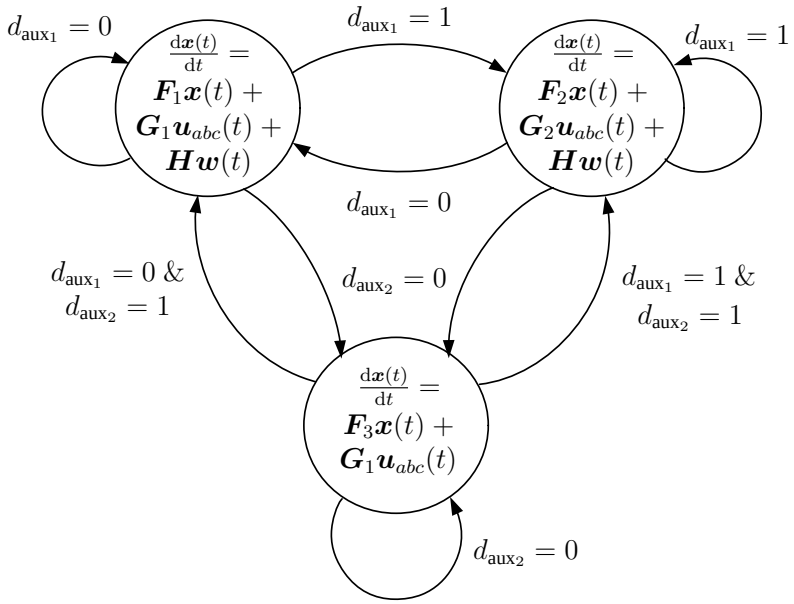


Figure 5.3: The qZSI presented as a continuous-time automaton.

5.2.4 Steady-State Analysis

At steady-state operation, and according to the inductor volt-second balance, the average voltage of the inductors is zero over one time window $T_1 = n_1 T_s$, with $n_1 \in \mathbb{N}^+$. Note that $T_1 \approx 1/f_{\text{sw}}$, with f_{sw} being the *average* switching frequency[3]. Therefore, the voltages of the capacitors C_1 and C_2, v_{C_1} and v_{C_2}, respectively, as well as the currents i_{L_1} and i_{L_2} of the inductors L_1 and L_2, respectively, are deduced as follows, assuming that $C_1 = C_2$ and $L_1 = L_2$.

$$v_{C_1} = \frac{1-d}{1-2d} v_{\text{in}}\,, \quad v_{C_2} = \frac{d}{1-2d} v_{\text{in}}\,, \tag{5.9a}$$

$$i_{L_1} = i_{L_2} = \frac{1-d}{1-2d} i_{\text{load}}\,, \tag{5.9b}$$

where i_{load} is the load current as shown in Figure 5.2(a). The *average* shoot-through duty cycle of the qZSI $d \in [0,\ 0.5)$ is defined as

$$d = \frac{T_0}{T_1} = \frac{n_0 T_s}{n_1 T_s} = \frac{n_0}{n_1}\,, \tag{5.10}$$

where T_0 is the time interval within the time window T_1 for which the load is short-circuited, i.e. the shoot-through time interval, and $n_0 < \frac{n_1}{2}$, $n_0 \in \mathbb{N}^+$. Moreover, the peak value of the dc-link voltage during the non-shoot-through period is

$$\hat{v}_{\text{dc}} = v_{C_1} + v_{C_2} = \frac{1}{1-2d} v_{\text{in}} = b v_{\text{in}} \tag{5.11}$$

where $b \geq 1$ is the boost factor resulting from the shoot-through period.

[3]With MPC the switching frequency is variable and the *average* switching frequency is used to indicate the operating switching frequency of the converter.

5.2.5 Boundary Output Current

The output power P_o of the qZSI can be calculated by

$$P_o = 3\, v_o\, i_o\, \cos\varphi\,, \tag{5.12}$$

where v_o (i_o) is the output voltage (current) and $\cos\varphi$ is the system power factor. For the qZSI v_o can be written as

$$v_o = \frac{1}{2\sqrt{2}}\, m\, \hat{v}_{\text{dc}} = \frac{1}{2\sqrt{2}}\, \frac{1}{1-2d}\, m\, v_{\text{in}}\,, \tag{5.13}$$

where m is the inverter modulation index, d is the *average* shoot-through duty cycle, and $\hat{v}_{\text{dc}}$ denotes the peak dc-link voltage, see the appendix in [112]. Considering that the simple boost control method is used (also utilized with PI control [25]), m can be expressed by d, i.e. $m = 1 - d$. This results in

$$v_o = \frac{1}{2\sqrt{2}}\, \frac{1-d}{1-2d}\, v_{\text{in}} \tag{5.14}$$

Then,

$$P_o = \frac{3}{2\sqrt{2}}\, \frac{1-d}{1-2d}\, v_{\text{in}}\, i_o\, \cos\varphi \tag{5.15}$$

The boost function b_f can be deduced from (5.15) as

$$b_f = \frac{1-d}{1-2d} = \frac{2\sqrt{2}}{3}\, \frac{P_o}{v_{\text{in}}\, i_o\, \cos\varphi} \tag{5.16}$$

If $b_f > 1$, then the shoot-through duty cycle d is more than zero which means that the converter should work in boost mode in order to generate the required output current. On the other hand, $b_f \leq 1$ indicates that the converter should work in buck mode. The output power can also be computed by $P_o = 3\, i_o^2\, R$. Thus, the current $i_{o,\text{bnd}}$ that defines the boundary between the two modes can be written as

$$i_{o,\text{bnd}} = \frac{v_{\text{in}}\, \cos\varphi}{2\sqrt{2}\, R}\,. \tag{5.17}$$

5.2.6 Internal Control Model

Using forward Euler approximation the continuous-time model derived in Section 5.2.3 is discretized. Note that Forward Euler approximation is adequately precise when a sampling interval of one to two tens of microseconds is used. For larger sampling intervals, exact discretization should be used instead. Hence, the resulting state-space model of the qZSI in the discrete-time domain is of the form

$$\boldsymbol{x}(k+1) = \boldsymbol{A}\boldsymbol{x}(k) + \boldsymbol{B}\boldsymbol{u}_{abc}(k) + \boldsymbol{D}\boldsymbol{w}(k) \tag{5.18a}$$

$$\boldsymbol{y}(k) = \boldsymbol{C}\boldsymbol{x}(k)\,, \tag{5.18b}$$

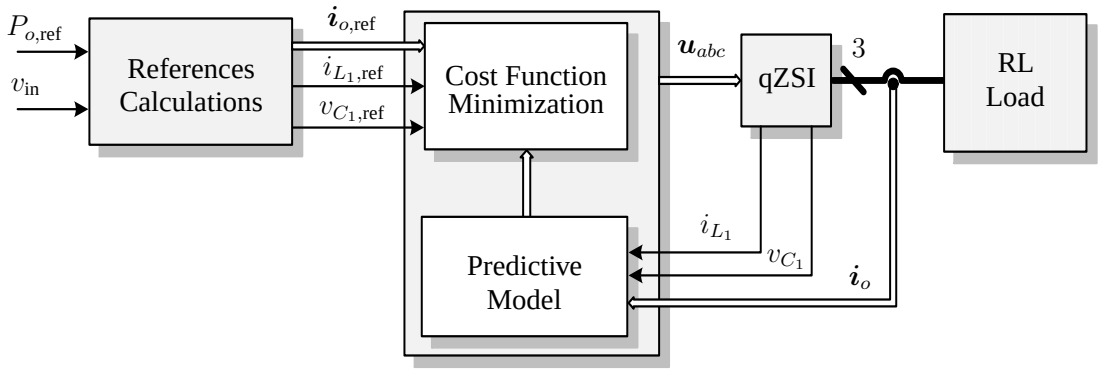


Figure 5.4: Direct model predictive control with reference tracking for the qZSI.

with $\boldsymbol{A} = (\boldsymbol{F} + \boldsymbol{I})T_s$, $\boldsymbol{B} = \boldsymbol{G}T_s$, $\boldsymbol{D} = \boldsymbol{H}T_s$ and $\boldsymbol{C} = \boldsymbol{E}$. Moreover, $\boldsymbol{I}$ denotes the identity matrix, T_s is the sampling interval, and $k \in \mathbb{N}$.

5.3 Direct Model Predictive Current Control

5.3.1 Control Objectives

For the qZSI, the control objective is twofold. First, the output current $\boldsymbol{i}_o$ should accurately track its reference value $\boldsymbol{i}_{o,\text{ref}}$. In addition, the inductor current i_{L_1} and the capacitor voltage v_{C_1} should be regulated along their reference trajectories $i_{L_1,\text{ref}}$ and $v_{C_1,\text{ref}}$, derived from an outer loop based on a power balance equation. Moreover, the switching losses are to be kept relatively low, which can be achieved indirectly by controlling the switching frequency. As mentioned before, the *average* switching frequency is controlled with direct MPC. For simplicity, the word *average* is dropped in the remainder of the dissertation. Finally, during transients, the above-mentioned controlled variables should reach their desired values as fast and with as little overshoot as possible.

5.3.2 Controller Block Diagram

The block diagram of the proposed direct predictive controller with current reference tracking is illustrated in Figure 5.4. As can be seen, the desirable system performance is achieved by directly manipulating the inverter switches, without the presence of a modulator. The proposed MPC algorithm first computes the evolution of the plant over the prediction horizon (i.e. the trajectories of the variables of concern) based on the measurements of the output current, inductor current, and capacitor voltage. Following, the optimal control action (i.e. the switching signals) is chosen by minimizing a performance criterion in real time.

5.3.3 Optimal Control Problem

At time-step k, the cost function that penalizes the error of the output variables and the switching effort over the finite prediction horizon of N time steps is written as

$$J(k) = \sum_{\ell=k}^{k+N-1} ||\boldsymbol{y}_{\text{ref}}(\ell+1|k) - \boldsymbol{y}(\ell+1|k)||^2_{\boldsymbol{Q}} + ||\Delta \boldsymbol{u}_{abc}(\ell|k)||^2_{\boldsymbol{R}} \,. \tag{5.19}$$

In (5.19) $\boldsymbol{y}_{\text{ref}} \in \mathbb{R}^4$ is a vector encompassing the reference values of the controlled variables (the output current, inductor current, and capacitor voltage), i.e. $\boldsymbol{y}_{\text{ref}} = [i_{o,\alpha,\text{ref}} \;\; i_{o,\beta,\text{ref}} \;\; i_{L_1,\text{ref}} \;\; v_{C_1,\text{ref}}]^T$. Moreover, the term $\Delta \boldsymbol{u}_{abc}(k) = \boldsymbol{u}_{abc}(k) - \boldsymbol{u}_{abc}(k-1)$ is added to control the inverter switching frequency by penalizing the switching transitions. Finally, the diagonal, positive semidefinite matrices $\boldsymbol{Q}$ and $\boldsymbol{R} \in \mathbb{R}^{4\times4}$ are the weighting matrices[4] that set the trade-off between the overall tracking accuracy and the switching frequency. Note that the diagonal entries of $\boldsymbol{Q}$ are chosen such that the tracking accuracy among the three output variables is prioritized. More specifically, priority is given to the output current by penalizing the corresponding error more heavily. This is achieved by choosing larger values for the corresponding diagonal entries in $\boldsymbol{Q}$. This implies that when more weight is put into the tracking of the output current reference, then the trade-off between the overall tracking accuracy and the switching frequency is simplified to the trade-off between the output current THD and the switching frequency of the converter, given by

$$f_{\text{sw}} = \lim_{M\to\infty} \frac{1}{MT_s} \cdot \frac{1}{6} \sum_{\ell=0}^{M-1} \frac{1}{2} \Big(||\boldsymbol{u}_{abc}(\ell) - \boldsymbol{u}_{abc}(\ell-1)||_1 + ||\bar{\boldsymbol{u}}_{abc}(\ell) - \bar{\boldsymbol{u}}_{abc}(\ell-1)||_1 \Big) \,. \tag{5.20}$$

According to (5.20), the switching frequency is computed by counting the number of *on* switching transitions over a time interval and by dividing this number by the length MT_s of that interval. The *average* switching frequency is then obtained by averaging over the 6 controllable switches of the converter. Note that the first term of the summation $||\boldsymbol{u}_{abc}(\ell) - \boldsymbol{u}_{abc}(\ell-1)||_1$ would suffice if and only if the switches in phase $x \in \{a,b,c\}$ changed position in a complementary manner, i.e. when the upper switch was on the lower was off ($u_x = 1 \to \bar{u}_x = 0$), and vice versa ($u_x = 0 \to \bar{u}_x = 1$). However, since both switches in any phase leg can be simultaneously on, the second term of the summation, i.e. $||\bar{\boldsymbol{u}}_{abc}(\ell) - \bar{\boldsymbol{u}}_{abc}(\ell-1)||_1$, with $\bar{\boldsymbol{u}}_{abc} = [\bar{u}_a \; \bar{u}_b \; \bar{u}_c]^T$, is added so that the switching transitions during the shoot-through state are also considered; the case $u_x = \bar{u}_x = 1$ is not concealed. By introducing this term, though, the on transitions are counted twice (once with each term). To compensate for that, the summation is divided by 2.

The optimal sequence of control actions is then computed by minimizing the cost function (5.19) over the optimization variable, i.e. the switching sequence over the prediction horizon $\boldsymbol{U}(k) = [\boldsymbol{u}^T_{abc}(k) \; \boldsymbol{u}^T_{abc}(k+1) \ldots \boldsymbol{u}^T_{abc}(k+N-1)]^T$, i.e.

$$\begin{aligned} \underset{\boldsymbol{U}(k)}{\text{minimize}} \quad & J(k) \\ \text{subject to} \quad & \text{eq. (5.18)} \\ & \boldsymbol{U}(k) \in \mathbb{U} \;. \end{aligned} \tag{5.21}$$

with $\mathbb{U} = \mathcal{U}^{3N}$. Having found the optimal switching sequence $\boldsymbol{U}^*(k)$, only its first element $\boldsymbol{u}^*_{abc}(k)$ is applied to the qZSI, whereas the rest are discarded. At the next time-step $k+1$, the

[4]The squared norm weighted with the positive (semi)definite matrix $\boldsymbol{W}$ is given by $||\boldsymbol{\xi}||^2_{\boldsymbol{W}} = \boldsymbol{\xi}^T \boldsymbol{W} \boldsymbol{\xi}$.

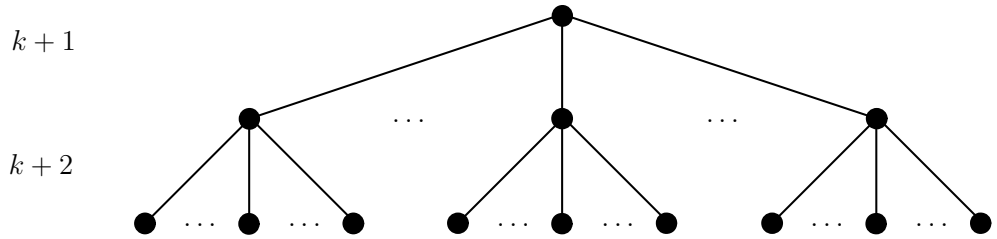


Figure 5.5: A search tree example for the integer optimization problem (5.21) assuming a two-step prediction horizon. Note that when the buck mode is considered, each parent node has seven children nodes, whereas there are eight children nodes per parent node for the boost mode. Therefore, the number of leaf nodes (i.e. candidate switching sequences $\boldsymbol{U}$) is 7^N and 8^N for the buck and boost mode, respectively, with N being the number of the prediction steps.

whole procedure is repeated with updated measurements over a one-step shifted horizon, as the receding horizon policy dictates [44].

5.3.4 Reducing the Computational Complexity

Problem (5.21) is in general computationally demanding due to the integer nature of the optimization variable. As already mentioned, its computational complexity increases exponentially with its size, i.e. the total number of candidate solutions for the problem under examination is 8^N. Therefore, it is likely that a relatively long prediction horizon—required for an improved system performance—would result in a problem that is computationally intractable. To reduce the increased computational burden and to manage to solve the underlying optimization problem (5.21) in real time in a matter of a few microseconds, heuristics and approximations are adopted in this work.

5.3.4.1 Branch-and-Bound Algorithm

First, a branch-and-bound algorithm is implemented [110]. A depth-first search is performed on the generated search tree, (see Figure 5.5), the branches of which are the elements of the candidate solutions of (5.21), i.e. the elements $\boldsymbol{u}_{abc}(\ell), \forall\, \ell = k, \ldots, k+N-1$ of the switching sequences $\boldsymbol{U}(k)$. Hence, the optimal solution is found by exploring each branch of the search tree as far as possible, i.e. until reaching a dead end or the bottom level, where backtracking occurs to explore unvisited nodes in higher levels. Having computed a good upper bound as soon as possible, then suboptimal branches can be pruned at the early stages of the search process, thus reducing the number of the candidate solutions. Furthermore, a branching heuristic is employed to warm-start the optimization procedure by starting from a "promising" branch, i.e. a branch that would lead to a tight upper bound. In particular, the first explored branch of the tree is the shifted by one time step previous solution $\boldsymbol{U}^*(k-1)$—in accordance with the receding horizon policy—concatenated with the last control action $\boldsymbol{u}^*(k+N-2)$.

5.3.4.2 Move Blocking Technique

To further reduce the computations required, while keeping the prediction horizon long enough, a move blocking technique [111], is utilized in this work. The main idea of this technique is to split the prediction horizon into two segments, N_1 and N_2, where the total number of prediction steps is $N = N_1 + N_2$, with $N_1, N_2 \in \mathbb{N}^+$. The first part of the horizon N_1 is finely sampled with the sampling interval T_s, while the second part N_2 is sampled more coarsely with a multiple of T_s, i.e. with $T_s' = n_s Ts$, where $n_s \in \mathbb{N}^+$. This results in a total prediction interval of $N_1 T_s + N_2 T_s' = (N_1 + n_s N_2) T_s$, thus, an adequate long prediction horizon is achieved using a few number of prediction steps [49, 54]. Using this technique, and in combination with the aforementioned branch-and-bound strategy, the calculation efforts can be dramatically decreased as shown in Section 5.5.

5.3.5 Proposed Control Algorithm

In order to show how the overall control strategy works, the proposed direct MPC algorithm for the qZSI is described in Algorithm 1. The initial values of the arguments are $\boldsymbol{U} = [\,]$, i.e. the empty vector, $\boldsymbol{x}(\ell) = \boldsymbol{x}(k)$, $\boldsymbol{u}_{abc}(\ell-1) = \boldsymbol{u}_{abc}(k-1)$, $J = 0$, $J^* = \infty$, $\ell = k$, and $m = 0$. Note that function f is the state-update function (5.18a), where the subscripts 1 and 2 correspond to the two different sampling intervals being used (T_s and T_s'), respectively, as explained in the move blocking strategy in Section 5.3.4.

Algorithm 1 MPC algorithm

function $\boldsymbol{U}^*(k)$ = MPC($\boldsymbol{U}, \boldsymbol{x}(\ell), \boldsymbol{u}_{abc}(\ell-1), J, J^*, \ell, m$)
  for each $\boldsymbol{u}_{abc}(\ell) \in \boldsymbol{\mathcal{U}}$ **do**
    $\boldsymbol{U}_{3m+1:3(m+1)} = \boldsymbol{u}_{abc}(\ell)$
    if $\ell < k + N_1$ **then**
      $\boldsymbol{x}(\ell+1) = f_1(\boldsymbol{x}(\ell), \boldsymbol{u}_{abc}(\ell))$
    else
      $\boldsymbol{x}(\ell+1) = f_2(\boldsymbol{x}(\ell), \boldsymbol{u}_{abc}(\ell))$
    end if
    $\boldsymbol{y}_{\text{err}}(\ell+1) = \boldsymbol{y}_{\text{ref}}(\ell+1) - \boldsymbol{y}(\ell+1)$
    $\Delta\boldsymbol{u}_{abc}(\ell) = \boldsymbol{u}_{abc}(\ell) - \boldsymbol{u}_{abc}(\ell-1)$
    $J = J + ||\boldsymbol{y}_{\text{err}}(\ell+1)||^2_{\boldsymbol{Q}} + ||\Delta\boldsymbol{u}_{abc}(\ell)||^2_{\boldsymbol{R}}$
    if $J < J^*$ **then**
      if $\ell < k + N - 1$ **then**
        MPC($\boldsymbol{U}, \boldsymbol{x}(\ell+1), \boldsymbol{u}_{abc}(\ell), J, J^*, \ell+1, m+1$)
      else
        $J^* = J$
        $\boldsymbol{U}^*(k) = \boldsymbol{U}$
      end if
    end if
  end for
end function

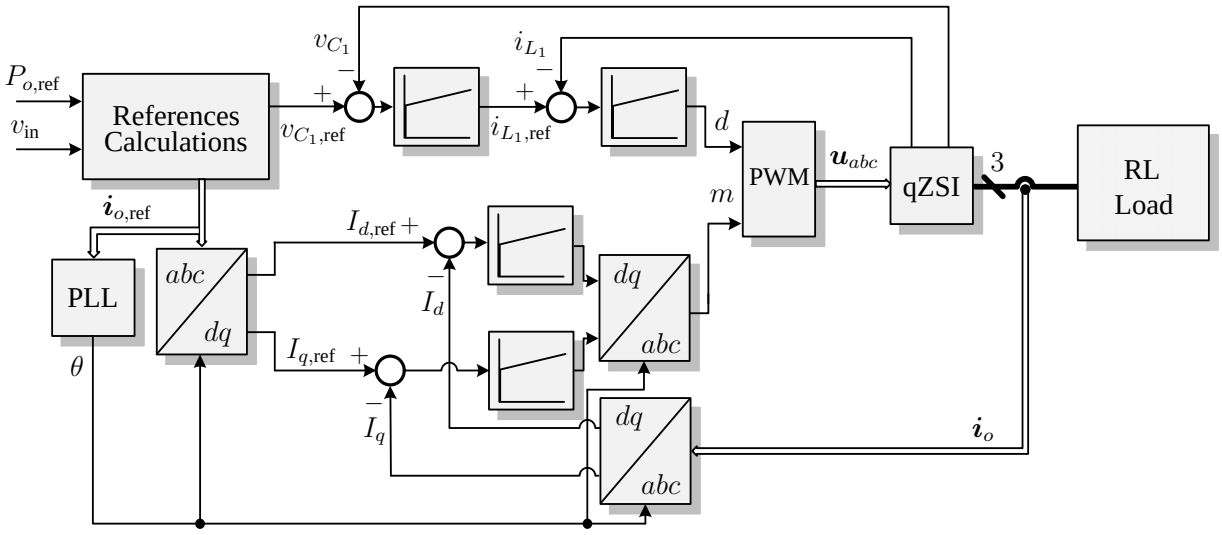


Figure 5.6: Linear control with PWM for the qZSI.

5.4 Conventional PI-Based Controller With PWM

Before evaluating the performance of the proposed MPC-based current control scheme, and for comparison purposes, a well-established linear controller is also implemented, see [18, 23, 24] and references therein. The block diagram is depicted in Figure 5.6. As can be seen, PI controllers are used on each side of the qZSI. The aim of the dc-side controller is to boost the dc-link voltage. To achieve this, the dc-side controller is subdivided into two cascaded control loops. In order to have a fair comparison with the proposed MPC strategy, PI controllers are used to control both the capacitor voltage and the inductor current of the dc side. The outer loop—the voltage controller—regulates the capacitor voltage v_{C_1} by adjusting the reference of the inductor current $i_{L_1,\text{ref}}$. The inner loop, i.e. the current controller, regulates the inductor current i_{L_1} by manipulating the shoot-through duty cycle d. On the ac side, the PI controller manipulates the inverter modulation index m in order to achieve tracking of the output current reference.

In a last step the shoot-through duty cycle d and the modulation index m are fed into the PWM block which generates the switching signals. As for the PWM techniques for the qZSI, there are three different methods in the literature: simple boost control, maximum boost control, and maximum constant boost control [12, 81, 113]. In this work, the simple boost control method combined with THI is implemented because it introduces constant shoot-through duty cycle which in turn results in lower inductor current ripples.

5.5 Simulation Results

To investigate the performance of the proposed MPC scheme for the qZSI in both buck and boost modes, several simulations using Matlab/Simulink have been conducted. The system parameters are $v_{\text{in}} = 70\,\text{V}$, $L_1 = L_2 = 1\,\text{mH}$, $C_1 = C_2 = 480\,\mu\text{F}$, $R = 10\,\Omega$, and $L = 10\,\text{mH}$. Based on the desired output power ($P_{o,\text{ref}} = 540\,\text{W}$), the output current reference $\boldsymbol{i}_{o,\text{ref}}$

$\left(= \sqrt{\frac{2P_{o,\text{ref}}}{3R}}\right)$ is set to $6\,\text{A}$, while the inductor current reference is equal to $7.7\,\text{A}$ ($i_{L_1,\text{ref}} = P_{o,\text{ref}}/v_{\text{in}}$). In order to calculate the capacitor voltage reference, the following derivation is used. First, the output power P_o of the qZSI can be calculated by

$$P_o = \frac{3}{2}\,\hat{v}_o\,\hat{i}_o\,\cos\varphi\,, \tag{5.22}$$

where $\hat{v}_o$ ($\hat{i}_o$) is the peak output voltage (current) and $\cos\varphi$ is the system power factor which can be calculated from the load impedance. Thus, $\hat{v}_o$ can be written as

$$\hat{v}_o = \frac{2\,P_o}{3\,\hat{i}_o\,\cos\varphi}\,, \tag{5.23}$$

Using the output power and current reference values and based on the load value ($P_{o,\text{ref}}$, $\boldsymbol{i}_{o,\text{ref}}$, and the RL load), the desired peak value of the output voltage is $\hat{v}_o = 64\,\text{V}$. In order not to affect the sinusoidal waveform of the output current and to prevent the interacting between the dc and ac sides, the capacitor voltage reference $v_{C_1,\text{ref}}$ should be greater than double the required peak output voltage [24]. Consequently, the capacitor voltage reference is chosen to be equal to $150\,\text{V}$, i.e. $v_{C_1,\text{ref}} = 2.3 \cdot \hat{v}_o$. In the remainder of this chapter the capacitor voltage reference is kept fixed at the aforementioned value in order to keep the peak dc-link voltage constant at $230\,\text{V}$, see (5.11).

For the scenarios examined below, the converter operates at the desired switching frequency $f_{\text{sw}} \approx 5\,\text{kHZ}$, by setting $\boldsymbol{Q} = \text{diag}(1, 1, 0.1, 0.02)$ and $\boldsymbol{R} = \lambda_u \boldsymbol{I}$ in (5.19), where $\lambda_u > 0$ is appropriately chosen, by exploring the trade-off between λ_u and the switching frequency f_{sw}, as shown in Figure 5.7. The sampling interval is chosen as $T_s = 25\,\mu\text{s}$.

5.5.1 Steady-State Performance

First, the effect of the prediction horizon length on the system performance is examined. The THD of the output current $I_{o,\text{THD}}$ is used as a performance metric. This is considered as a meaningful and informative metric during steady-sate operation since it quantifies the tracking performance of the controller.

Table 5.1 summarizes the output current THD $I_{o,\text{THD}}$ produced by the presented MPC current controller in both buck and boost operation modes. Note that MPC with a prediction horizon of length $1T_s$ corresponds to the existing and established one-step horizon MPC. Regardless of the prediction horizon length, the converter operates at a switching frequency of $f_{\text{sw}} \approx 5\,\text{kHz}$. This is done by manipulating the weighting matrix $\boldsymbol{R}$ in the cost function (5.19).

As can be seen in Table 5.1, when longer prediction intervals are implemented the closed-loop system performance can be significantly improved. In particular, it can be observed that even a prediction interval of $4T_s$ can be considered long enough to achieve a noteworthy reduction in the current THD.

To further assess the performance of the proposed MPC strategy, the linear controller presented in Section 5.4 is examined. Again, the converter operates at a switching frequency of $5\,\text{kHz}$ and under the same input/output operating conditions. It is found that the output current THD value is 8.30% in boost mode. The current THD of the proposed MPC with a prediction

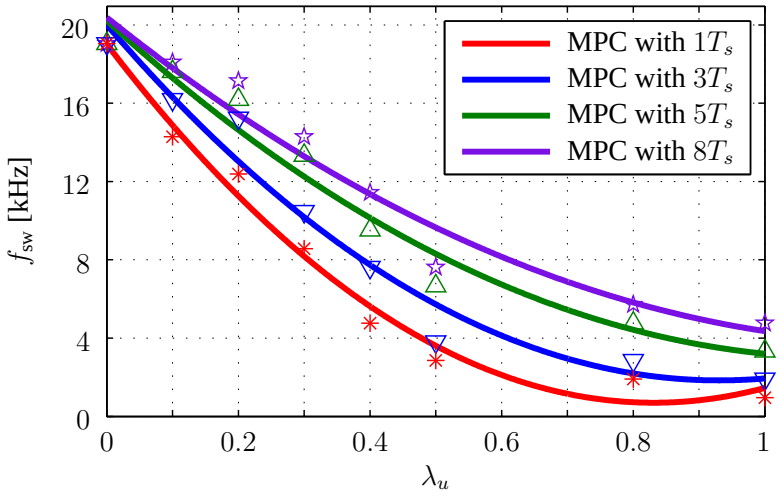


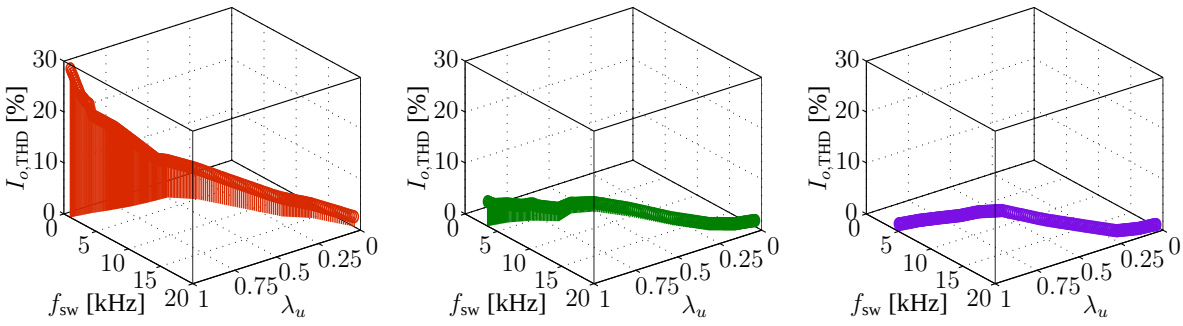
Figure 5.7: The effect of the weighting factor (λ_u) on the switching frequency for the MPC with different prediction horizons ($1T_s$, $3T_s$, $5T_s$, and $8T_s$). The measurements are shown as (red) asterisks, (blue) downward-pointing triangles, (green) upward-pointing triangles, and (magenta) stars, referring to individual simulation results, when the system was controlled with MPC with prediction horizon intervals of $1T_s$, $3T_s$, $5T_s$ and $8T_s$, respectively. The data points were approximated using a second degree polynomial.

Table 5.1: Output current THD produced by the proposed MPC scheme depending on the length of the prediction horizon. The switching frequency is approximately 5 kHz.

Length of Prediction Horizon NT_s	Current THD $I_{o,\text{THD}}\%$	
	Buck Mode	Boost Mode
$1T_s$	13.40	16.09
$2T_s$	10.06	11.80
$3T_s$	6.03	6.52
$4T_s$	4.88	5.01
$5T_s$	3.45	3.65
$6T_s$	2.20	2.34
$7T_s$	1.83	1.99
$8T_s$	1.29	1.46

interval of $3T_s$ (6.52%, see Table 5.1) is lower than the one with the PI-based controller. These results confirm that long-horizon MPC definitely leads to better performance than the one with the conventional PI control.

In a next step, the trade-off between the current THD and the switching frequency is in-



(a) MPC with $1T_s$ (b) MPC with $5T_s$ (c) MPC with $8T_s$

Figure 5.8: The effect of the weighting factor (λ_u) on the switching frequency and the output current THD for the MPC with different prediction horizons ($1T_s$, $5T_s$, and $8T_s$).

vestigated. The switching frequency of the qZSI varies from $f_{\text{sw}} = 3$ to $f_{\text{sw}} = 15\,\text{kHz}$ by changing the value of the weighting factor λ_u, while keeping the entries of $\boldsymbol{Q}$ constant. For each switching frequency, the resulting $I_{o,\text{THD}}$ is recorded. The three-dimensional graphs that show the relationship among the weighting factor (λ_u), switching frequency (f_{sw}), and output current THD for MPC with different prediction horizons are shown in Figure 5.8.

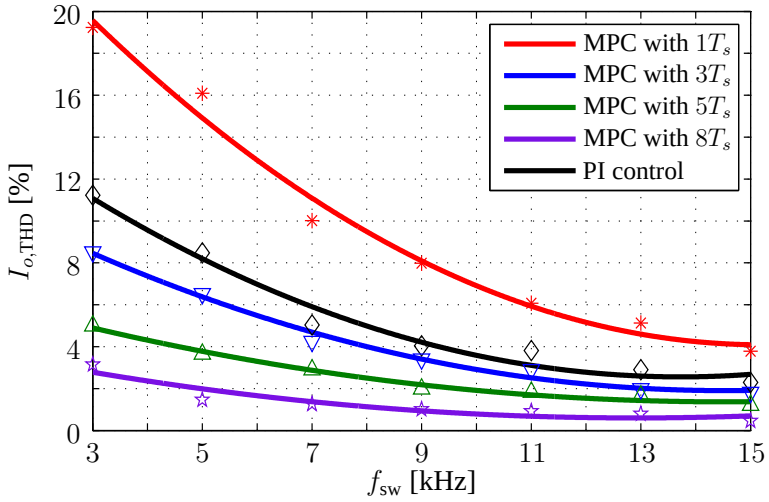
To further investigate the trade-off between the current THD and the switching frequency, the MPC algorithm is implemented with four different prediction horizon lengths ($1T_s$, $3T_s$, $5T_s$, and $8T_s$). For comparison purposes, the respective THD values produced by the linear controller are also included. The individual simulations—indicated by markers—are approximated by second and third degree polynomials in Figures 5.9(a) and 5.9(b), respectively.

Figure 5.9(a) verifies that long-prediction horizon MPC can remarkably decrease the current THD, especially when the switching frequency is relatively low. For example, at a switching frequency of $f_{\text{sw}} = 3\,\text{kHz}$, the current THD of the MPC with $1T_s$ prediction horizon is $I_{o,\text{THD}} = 19.23\%$. However, the THD highly reduces to 3.15% with an $8T_s$ prediction horizon. On the other hand, when higher switching frequencies are considered, the improvement in the current THD is still present. Furthermore, based on Figure 5.9(a) it can be concluded that MPC with a prediction interval of $3T_s$ achieves a lower current THD than the PI-based control, and when the prediction interval extends to $8T_s$, it notably outperforms it.

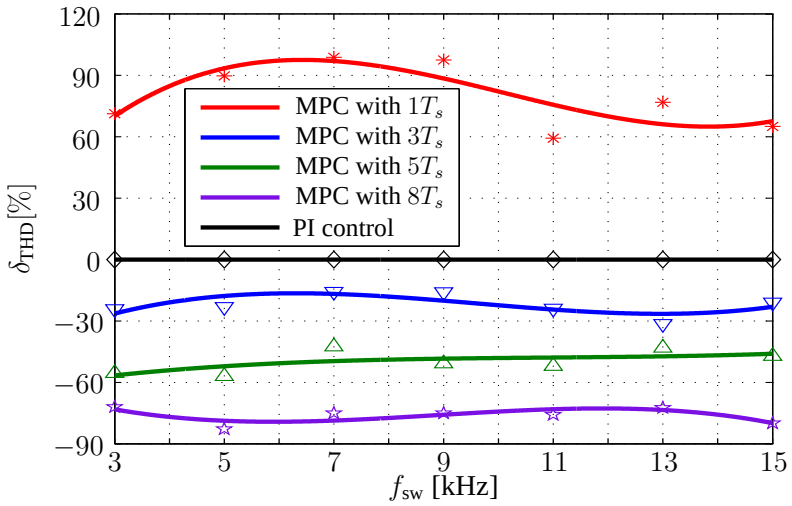
This can also be observed in Figure 5.9(b), where the *relative* current THD ($\delta_{\text{THD}}\%$) of the MPC strategy with the aforementioned prediction lengths is depicted versus the same range of switching frequencies. The relative current THD of the MPC is normalized to the THD resulting from the PI-based control and given in percent according to the following expression [108]

$$\delta_{\text{THD}} = \frac{\text{THD}_{\text{MPC}} - \text{THD}_{\text{PI}}}{\text{THD}_{\text{PI}}} \cdot 100\%. \tag{5.24}$$

Figure 5.9(b) shows that the current THD produced by MPC with $1T_s$ horizon is higher by up to 100% for switching frequencies around 7 kHz, compared to that of a PI-based controller. Increasing the prediction horizon length to $8T_s$, the MPC produces currents with reduced THD values by about $70 - 80\%$ for switching frequencies between 3 and $15\,\text{kHz}$. These results point



(a) Current THD and switching frequency.



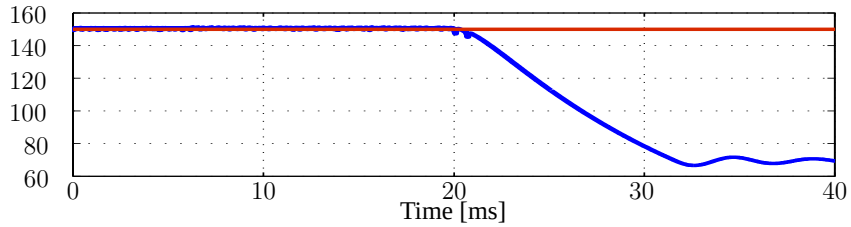
(b) Relative current THD and switching frequency.

Figure 5.9: Trade-off between the output current THD $I_{o,\text{THD}}$ and the switching frequency f_{sw} for the PI-based controller and the MPC with different prediction horizon intervals of $1T_s$, $3T_s$, $5T_s$, and $8T_s$. The data points in (a) were approximated using a second degree polynomial; those in (b) were approximated by a polynomial function of third order.

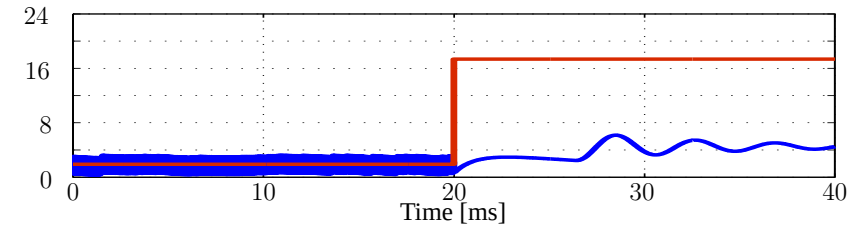
out that using MPC with longer horizon effectively improves the performance of the qZSI and introduces better behavior than the traditional PI control.

5.5.2 Discussion on Stability

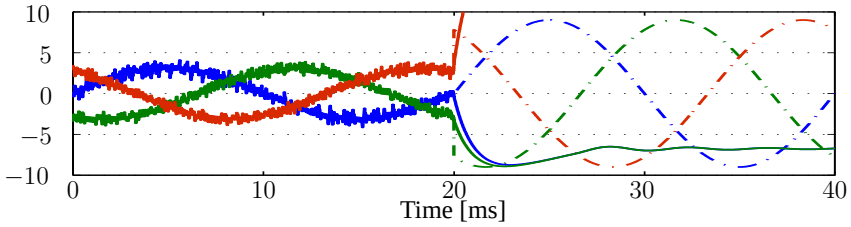
As mentioned in Section 5.1, the qZSI is a nonminimum system. More specifically, assuming a linearized model, the shoot-through duty cycle-to-capacitor voltage transfer function contains a right half-plane zero, implying that the sign of the gain is not always positive. Physically, this means that the system exhibits a reverse-response behavior during transients. For example,



(a) Capacitor voltage v_{C_1} and its reference in [V]



(b) Inductor current i_{L_1} and its reference in [A]



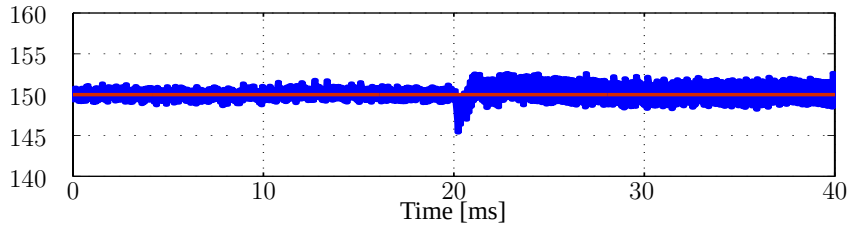
(c) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A]

Figure 5.10: Simulation results for a step change in the output current reference with MPC and a $1T_s$ prediction horizon length.

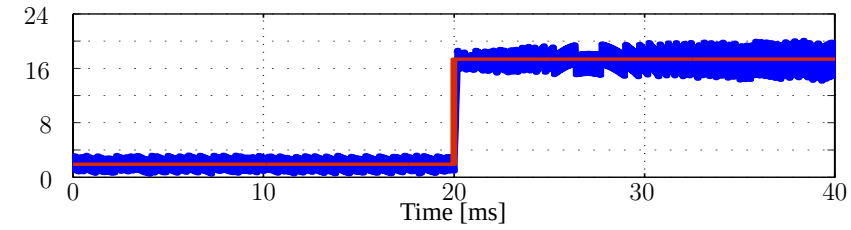
when the output power demands increase then the ac side needs to be instantaneously short circuited for a non-negligible time for the dc-link voltage to remain at the desired level. This prolonged short-circuit situation of the ac side (which can be interpreted as an instantaneous increase in the shoot-through duty cycle) causes the capacitor voltage to initially drop and diverge from its reference value. A controller should be able to bring the voltage back to its predefined value in order to keep the system stable. As far as MPC is concerned, this means that the prediction horizon should be long enough, so that the controller can accurately predict the whole phenomenon and "see" beyond the initial voltage drop.

In order to show how long-horizon MPC can ensure stability under conditions single-step MPC fails to do, the following scenario is examined. The desired output power is stepped up at $t = 20\,\text{ms}$ from $P_{o,\text{ref}} = 135$ to $1215\,\text{W}$. Accordingly, the output current reference is changed from 3 to $9\,\text{A}$ and the inductor current reference from 1.9 to $17.4\,\text{A}$ (see beginning of Section 5.5); for this test the capacitor voltage reference is kept fixed at $150\,\text{V}$. The qZSI is controlled with MPC with prediction intervals equal to $1T_s$ and $5T_s$. The simulation results are shown in Figures 5.10 and 5.11, respectively. In both cases the switching frequency is set to approximately $5\,\text{kHz}$.

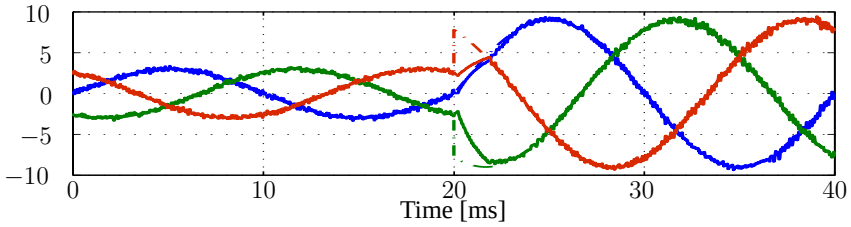
As can be seen in Figures 5.10 and 5.11, before the demanded output power change the



(a) Capacitor voltage v_{C_1} and its reference in [V]



(b) Inductor current i_{L_1} and its reference in [A]



(c) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A]

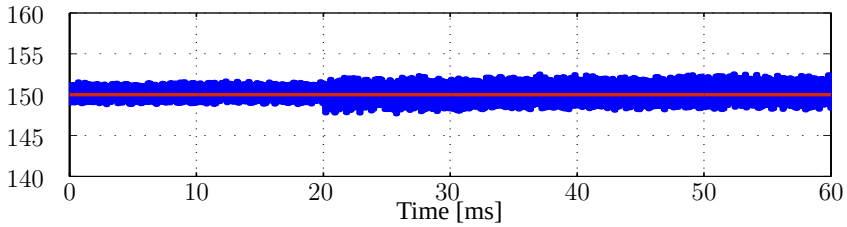
Figure 5.11: Simulation results for a step change in the output current reference with MPC and a $5T_s$ prediction horizon length.

system behaves almost the same, regardless of the length of the prediction horizon. Nonetheless, MPC with a prediction interval of $5T_s$ produces lower current THD than single-step horizon MPC, as expected and explained in Section 5.5.1. When the step change occurs at $t = 20\,\text{ms}$, MPC with horizon of $1T_s$ fails to track the reference values of the dc- and ac-side variables, see Figure 5.10. On the other hand, long-horizon MPC manages to follow the changes in the reference values of the controlled variables and eliminates the resulting errors as fast as possible.

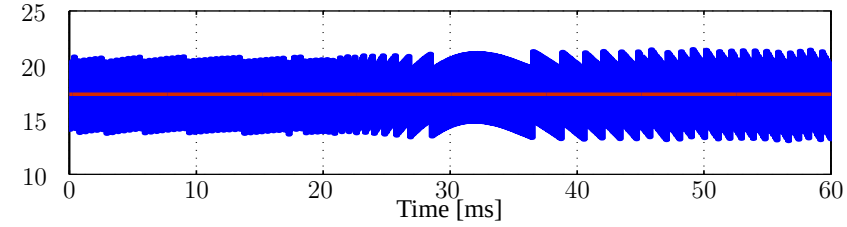
From the above-shown results it can be understood that short-horizon MPC fails to predict beyond the initial capacitor voltage drop. Thus, it computes a plan of control actions that is suboptimal; this plan does not suffice to bring the system back to steady-state operation after its initial reverse response; consequently it becomes unstable. Long-horizon MPC, however, manages to keep the system stable. The controller predicts within the $5T_s$ prediction horizon both the voltage drop at the beginning of the transient as well as its subsequent increase, and thus picks the corresponding sequence of control actions that achieve this.

5.5.3 Robustness Against Parameters Variation

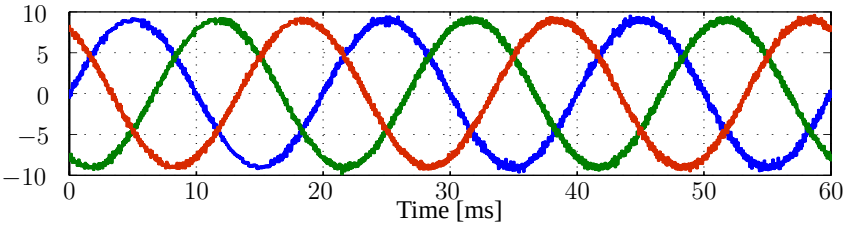
MPC, as a model-based control strategy, relies on an accurate model of the examined system in order to come up with the best possible plan of control actions. MPC schemes for power



(a) Capacitor voltage v_{C_1} and its reference in [V]



(b) Inductor current i_{L_1} and its reference in [A]



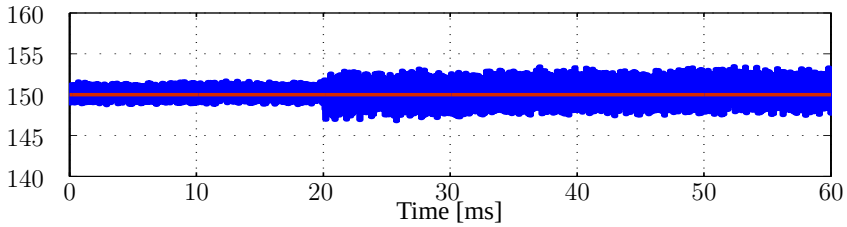
(c) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A]

Figure 5.12: Simulation results for MPC and a $5T_s$ prediction horizon length when R of the RL load is reduced by $50\,\%$.

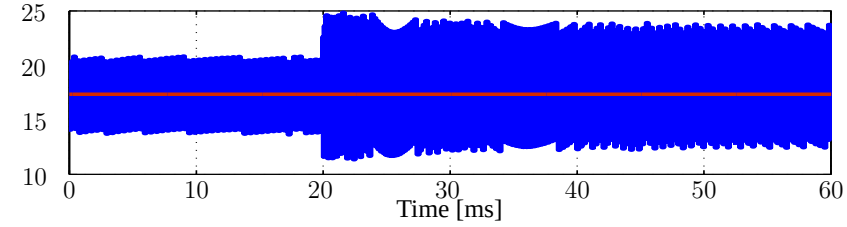
electronics, though, are typically highly robust. The accuracy of the predictions is high since the models used in power electronics are fairly accurate, at least compared to other disciplines. Moreover, the receding horizon policy in MPC adds feedback and provides MPC with a high degree of robustness to model mismatches and disturbances. To verify this argument, in this section, the impact of parameter variations on the system performance is examined when MPC with a $5T_s$ prediction length is implemented.

In the first case, the resistive part R of the RL load is halved; at time $t = 20$ ms the resistor R is changed from 10 to $5\,\Omega$. The simulation results for the three controlled variables (the capacitor voltage, inductor current, and output current) are shown in Figure 5.12. As can be seen, the three variables track their references effectively. However, the output current distortions become higher; the THD increases from $3.65\,\%$ to $4.39\,\%$, see Figure 5.12(c). In addition, the capacitor voltage and inductor current exhibit slightly higher ripples, see Figures 5.12(a) and 5.12(b), respectively.

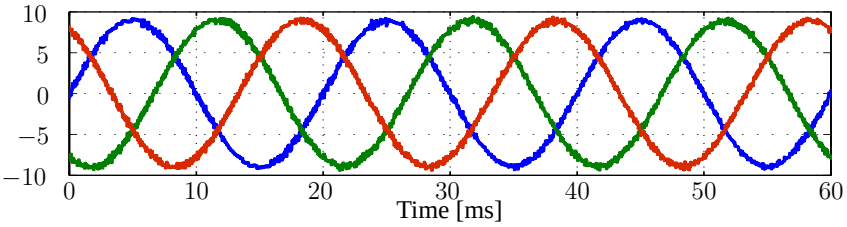
In the second test, the qZS network inductances (L_1 and L_2) are changed from their nominal values of $1000\,$mH to $500\,$mH. The simulation results for both sides are shown in Figure 5.13. As can be observed in Figure 5.13(c), the output current remains unaffected by this change on the dc side, since its THD is marginally increased by $2.3\,\%$. On the dc side, although the ripples



(a) Capacitor voltage v_{C_1} and its reference in [V]



(b) Inductor current i_{L_1} and its reference in [A]



(c) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A]

Figure 5.13: Simulation results for MPC and a $5T_s$ prediction horizon length when L_1 and L_2 of the qZS network are reduced by $50\,\%$.

of the capacitor voltage and the inductor current are more pronounced, the controlled variables are still regulated along their references and a zero steady-state error is achieved. These results confirm that—thanks to the receding horizon policy—MPC with long-horizon remains robust to parameter variations in the underlying prediction model.

5.5.4 Computational Burden

Since an increased prediction horizon entails a subsequent increase in the computational complexity of the MPC algorithm, the latter is investigated in this section. This is done in terms of the complete switching sequences $\boldsymbol{U}$ and the nodes being evaluated at each time-step to obtain the optimal solution.

Tables 5.2 and 5.3 show the average and the maximum number of the sequences μ and nodes ν examined as a function of the length of the prediction horizon when the qZSI operates in buck and boost mode, respectively. To highlight the computational efficiency of the proposed MPC algorithm, the number of the switching sequences evaluated with the exhaustive enumeration algorithm—typically used in the field of power electronics to solve MPC problems of the form (5.21) [45]—is also presented.

As can be seen, thanks to the branch-and-bound scheme and the move blocking strategy, the

Table 5.2: Buck mode: Average and maximum numbers of examined switching sequences μ and nodes ν depending on the length of the prediction horizon.

Length of Prediction Horizon	Exhaustive Search			Proposed MPC Strategy				
$NT_s = (N_1 + n_s N_2)T_s$	$N_1 + N_2$	μ	ν	$N_1 + N_2$	avg(μ)	avg(ν)	max(μ)	max(ν)
$1T_s$	$1+0$	7	7	$1+0$	7	7	7	7
$2T_s$	$2+0$	49	56	$2+0$	14	23.8	21	28
$3T_s$	$3+0$	343	399	$1+1$	18.9	27.8	28	35
$4T_s$	$4+0$	2,401	2,800	$2+1$	29.2	43.5	49	63
$5T_s$	$5+0$	16,807	19,607	$1+2$	47	53.6	70	84
$6T_s$	$6+0$	117,649	137,256	$2+2$	59.3	68.6	84	91
$7T_s$	$7+0$	832,543	960,799	$1+3$	66.8	80.2	98	105
$8T_s$	$8+0$	5,764,801	6,725,600	$2+3$	79.2	93.1	112	126

Table 5.3: Boost mode: Average and maximum numbers of examined switching sequences μ and nodes ν depending on the length of the prediction horizon.

Length of Prediction Horizon	Exhaustive Search			Proposed MPC Strategy				
$NT_s = (N_1 + n_s N_2)T_s$	$N_1 + N_2$	μ	ν	$N_1 + N_2$	avg(μ)	avg(ν)	max(μ)	max(ν)
$1T_s$	$1+0$	8	8	$1+0$	8	8	8	8
$2T_s$	$2+0$	64	72	$2+0$	16.4	25.3	24	32
$3T_s$	$3+0$	512	584	$1+1$	23.2	33.4	32	44
$4T_s$	$4+0$	4,096	4,680	$2+1$	41.7	56.2	64	87
$5T_s$	$5+0$	32,768	37,448	$1+2$	56.5	75.9	80	100
$6T_s$	$6+0$	262,144	299,592	$2+2$	78.1	99.6	104	126
$7T_s$	$7+0$	2,097,152	2,396,744	$1+3$	84.6	111.4	112	147
$8T_s$	$8+0$	16,777,216	19,173,960	$2+3$	114.2	153.8	152	188

number of examined sequences is significantly reduced. For instance, for a prediction horizon of $6T_s$ total length (by setting $N_1 = 2$, $N_2 = 2$, $n_s = 2$ in the move blocking scheme, see Section 5.3.4) the maximum number of sequences—which is of importance for a real-time implementation since it corresponds to the worst-case scenario—is reduced by about 99.96%. In addition, the maximum number of the visited nodes is reduced by about 99.95%. The significant reduction in the required calculations enables the proposed MPC to be implemented in real time as shown in Section 5.6.

5.6 Experimental Evaluation

Experiments for the qZSI with both the proposed MPC scheme and the linear PI-based controller were carried out in the laboratory. The system parameters are the same as in Section 5.5. The controllers were implemented on a low-cost, low-power field programmable logic array (FPGA) Cyclone III-EP3C40Q240C8. To compensate for the time delay introduced by the MPC controller, a delay compensation strategy is applied [114]. For more details about the test bench, please refer to appendix C.

5.6.1 Steady-State Operation

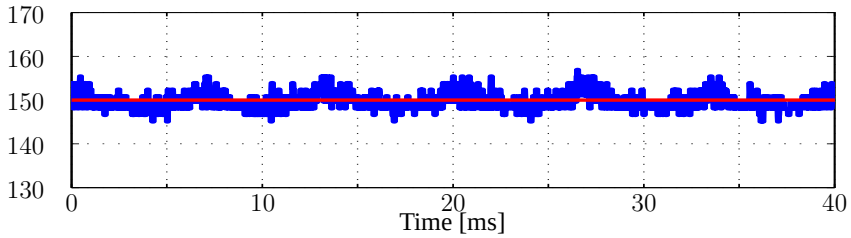
The first scenario examined is that of the steady-state behavior of the qZSI when operated at a switching frequency of $\approx 5\,\text{kHz}$, as computed over 50 fundamental periods, i.e. by setting $M = 40{,}000$ in (5.20). As far as the MPC scheme is concerned, two different prediction horizon lengths are tested, i.e. $1T_s$ and $5T_s$, with the weighting factor λ_u being 0.42 and 0.75, respectively, in order to achieve the desired switching frequency (see Figure 5.7).

Considering the parameters of the PI controllers, they are tuned such that no steady-state error appears when operating under nominal conditions, while current regulation with as little overshoot as possible is achieved. By using the concept of averaging, the closed-loop transfer function of the linearized system is first derived (see [24, 37]), and then by utilizing the Routh-Hurwitz stability criterion, the parameters of the PI controllers chosen. Therefore, the gains of the dc-side controllers are chosen to be $k_{p_c} = 0.008$ and $k_{i_c} = 0.05$ for the outer PI voltage control loop and $k_{p_i} = 0.03$ and $k_{i_i} = 0.2$ for the inner PI current control loop. As for the ac-side, the control parameters are chosen as $k_{p_1} = k_{p_2} = 0.05$ and $k_{i_1} = k_{i_2} = 30$.

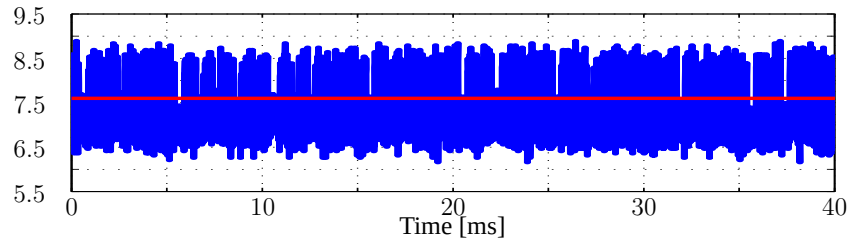
The experimental results obtained with the MPC are shown in Figures 5.14 and 5.15, whereas those produced by the PI control are illustrated in Figure 5.16.

With regard to the dc side, it can be observed that the inductor current accurately tracks its reference in all cases examined (Figures 5.14(b), 5.15(b), and 5.16(b)), resulting in a boosted capacitor voltage $v_{C_1} = 150\,\text{V}$ (Figures 5.14(a), 5.15(a), and 5.16(a)) and a peak dc-link voltage of $\hat{v}_{\text{dc}} = 230\,\text{V}$ (Figures 5.14(c), 5.15(c), and 5.16(c)). Regardless of the prediction horizon, the MPC shows good steady-state behavior with low inductor current ripples. On the other hand, the inductor current and capacitor voltage ripples are slightly higher with the PI-based controller.

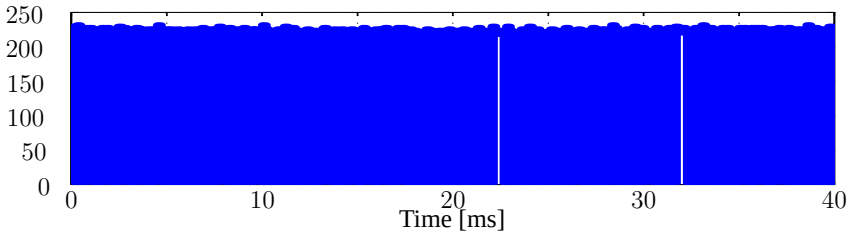
On the ac side of the converter, the tracking accuracy of the proposed controller is not affected by the shoot-through state as can be seen in Figures 5.14(d) and 5.15(d) where the three-phase



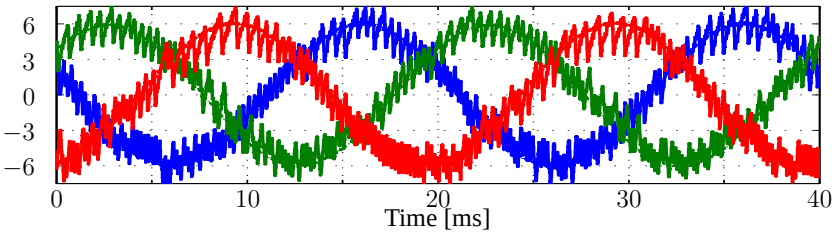
(a) Capacitor voltage v_{C_1} and its reference in [V]



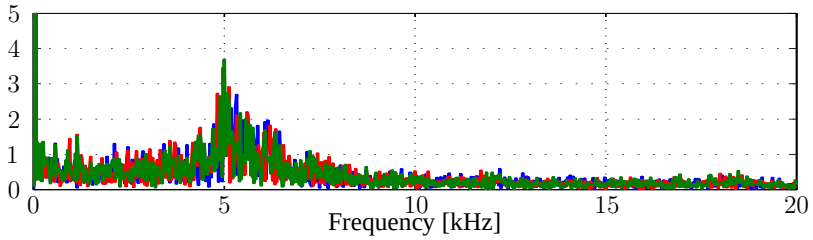
(b) Inductor current i_{L_1} and its reference in [A]



(c) Dc-link voltage v_{dc} in [V]

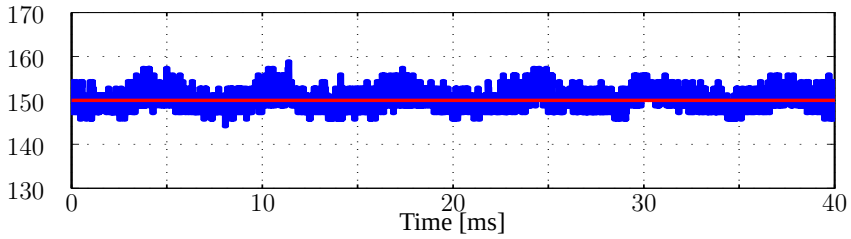


(d) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A]

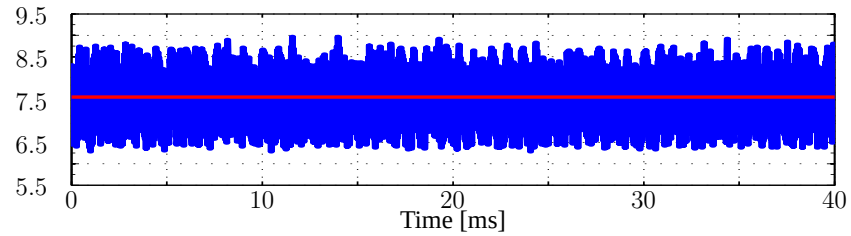


(e) Output current spectrum (%)

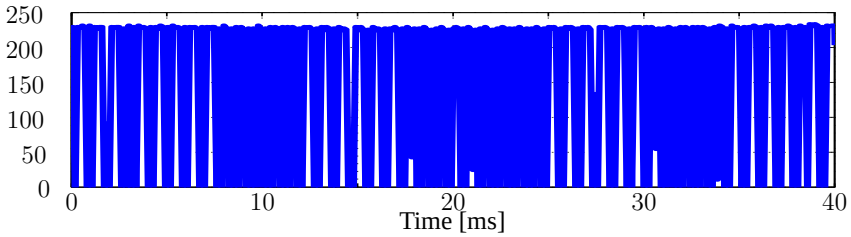
Figure 5.14: Experimental results with MPC and an $1T_s$ prediction horizon length. The sampling interval is $T_s = 25\,\mu$s and $\lambda_u = 0.42$. The switching frequency is $f_{\text{sw}} \approx 5\,$kHz and the output current THD $I_{o,\text{THD}} = 17.05\%$.



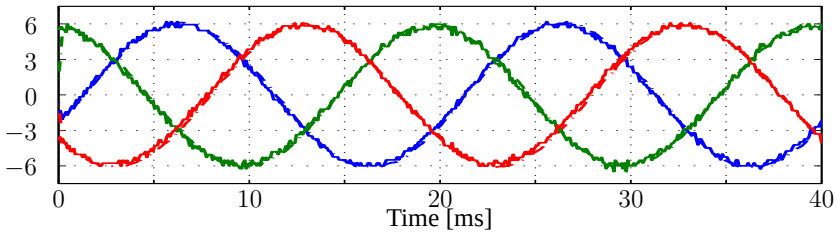
(a) Capacitor voltage v_{C_1} and its reference in [V]



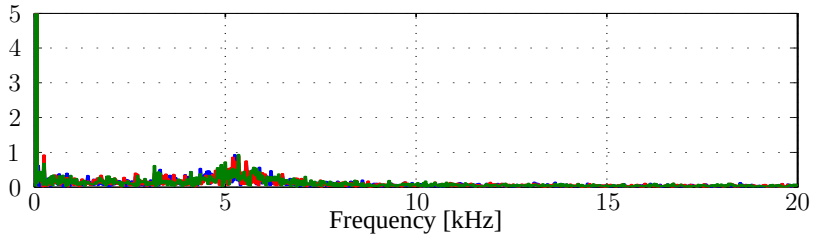
(b) Inductor current i_{L_1} and its reference in [A]



(c) Dc-link voltage v_{dc} in [V]

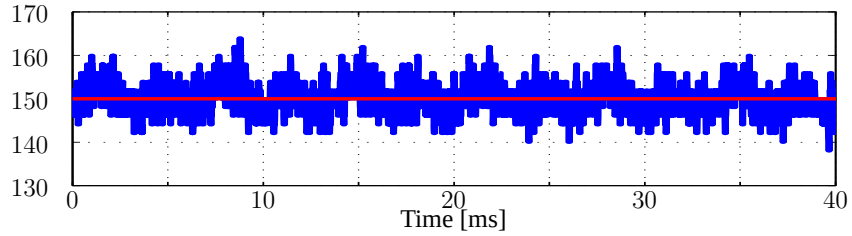


(d) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A]

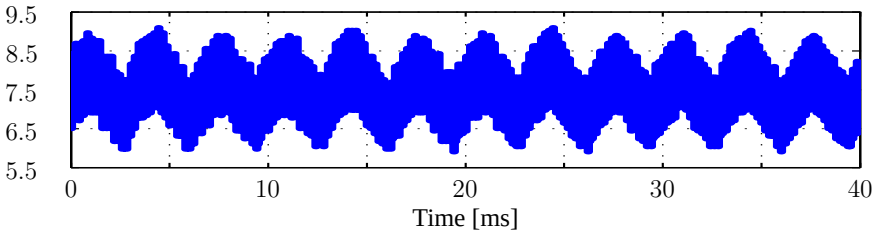


(e) Output current spectrum (%)

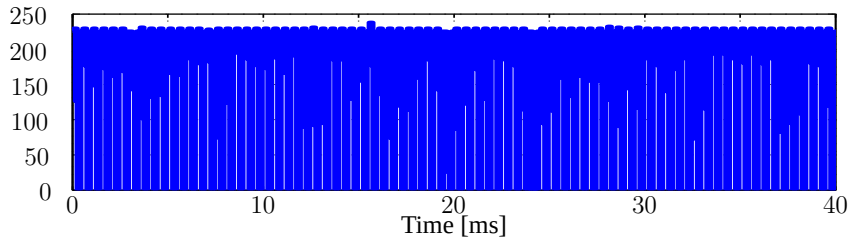
Figure 5.15: Experimental results of with MPC and a $5T_s$ prediction horizon length. The sampling interval is $T_s = 25\,\mu$s and $\lambda_u = 0.75$. The switching frequency is $f_{\text{sw}} \approx 5\,$kHz and the output current THD $I_{o,\text{THD}} = 4.65\%$.



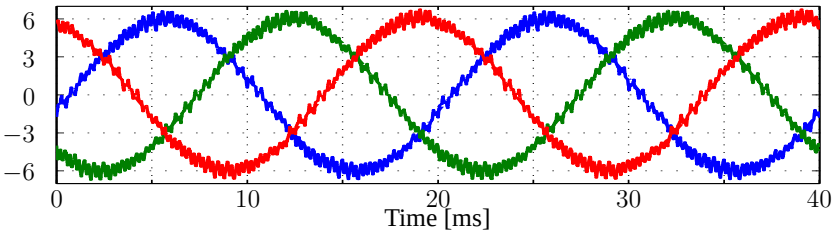
(a) Capacitor voltage v_{C_1} and its reference in [V]



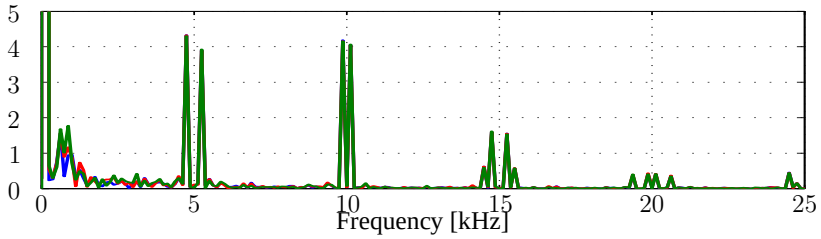
(b) Inductor current i_{L_1} in [A]



(c) Dc-link voltage v_{dc} in [V]

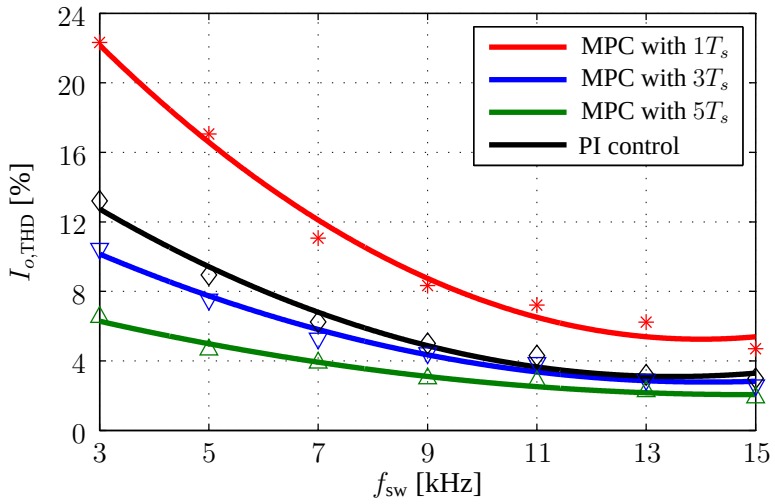


(d) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A]

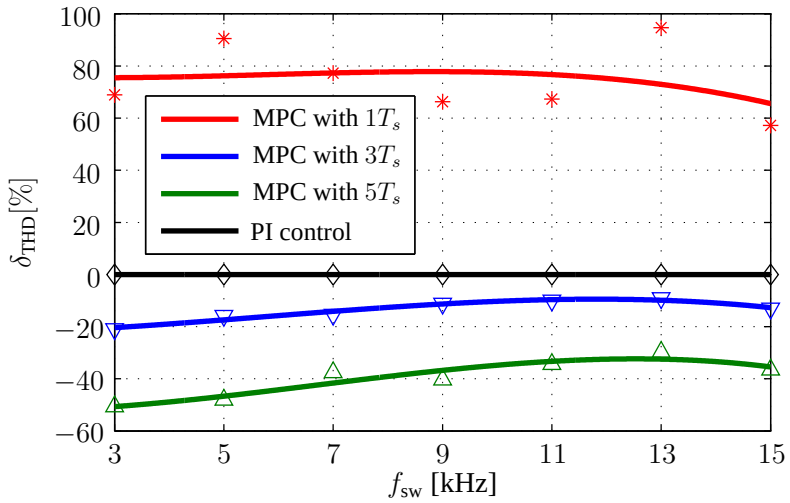


(e) Output current spectrum (%)

Figure 5.16: Experimental results with PI-based control. The switching frequency is $f_{\text{sw}} = 5\,\text{kHz}$ and the output current THD $I_{o,\text{THD}} = 8.95\%$.



(a) Current THD and switching frequency.

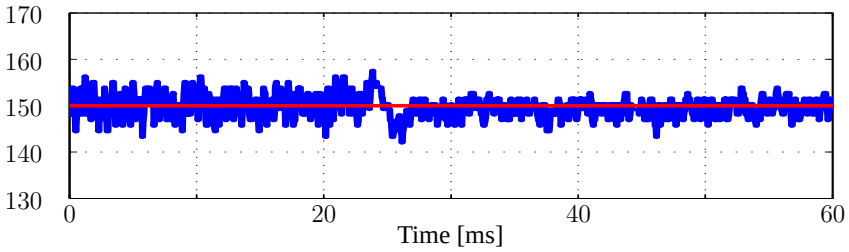


(b) Relative current THD and switching frequency.

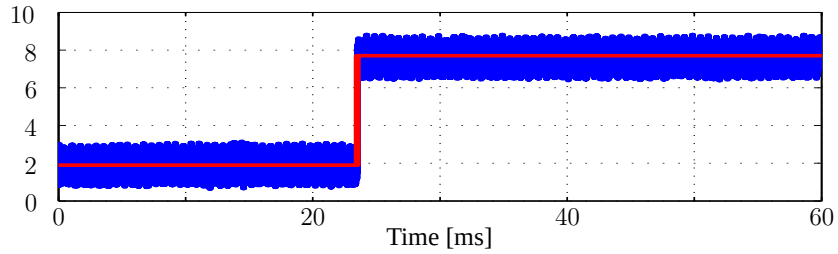
Figure 5.17: Trade-off between the output current THD $I_{o,\text{THD}}$ and the switching frequency f_{sw} for the PI-based controller and the MPC with prediction horizon length of $1T_s$, $3T_s$ and $5T_s$.

output currents are depicted along with their references. Furthermore, the MPC with a $5T_s$ prediction interval produces THD $I_{o,\text{THD}} = 4.65\%$ (see Figure 5.15(e)), significantly lower than the one resulting from the $1T_s$ horizon MPC, which is 17.05% (see Figure 5.14(e)). This confirms that increasing the prediction horizon improves the system performance as far as the output current THD is concerned, as also shown in Section 5.5. With the PI-based controller the current THD is 8.95% (see Figure 5.16(e)) which is notably higher than that of the MPC with horizon length $5T_s$. These results are in line with the simulation ones.

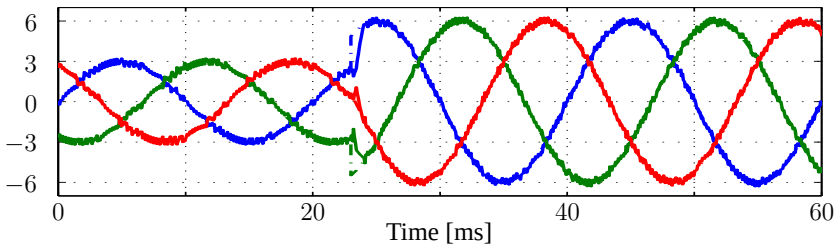
It can be concluded that the overall performance of the qZSI is improved with MPC when a longer horizon is used. By utilizing the branch-and-bound and move blocking techniques, the computationally burden is reduced and the MPC algorithm can be successfully implemented



(a) Capacitor voltage v_{C_1} and its reference in [V]



(b) Inductor current i_{L_1} and its reference in [A]



(c) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A]

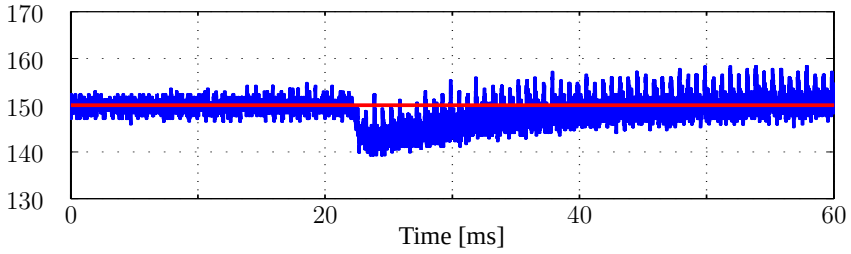
Figure 5.18: Experimental results for a step change in the output current reference with MPC and a $5T_s$ prediction horizon length.

in the FPGA. Without adding any outer loops that would complicate the controller design, the proposed MPC algorithm outperforms the PI-based controller.

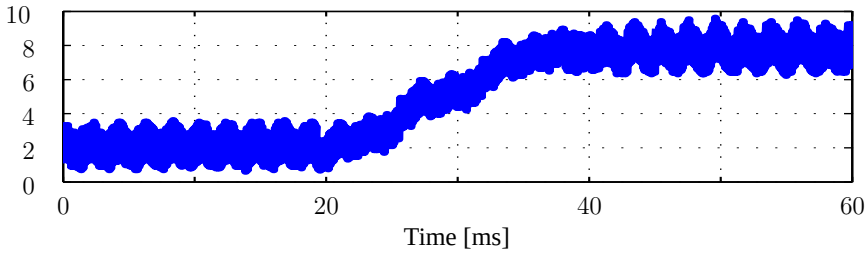
5.6.2 Current THD and Switching Frequency

Some experiments were conducted to study the trade-off between the current THD and the switching frequency of the proposed MPC strategy with prediction intervals equal to $1T_s$, $3T_s$, and $5T_s$. For all cases examined, λ_u was appropriately tuned to obtain the desired switching frequency.

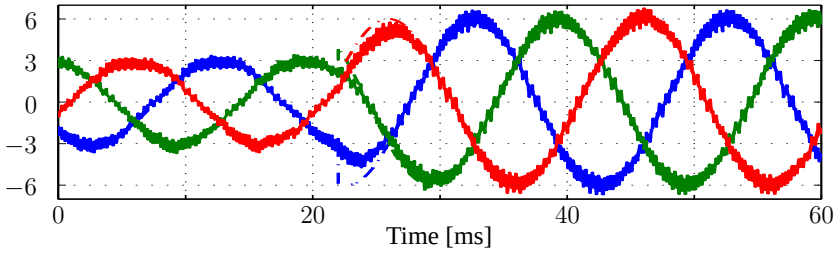
The results with the MPC and the PI-based controller are illustrated in Figure 5.17(a). Among the different prediction horizons, it can be noticed that the MPC with a $5T_s$ horizon introduces the lowest THD values over the whole range of the switching frequencies (from 3 up to 15 kHz). As can be seen, the resulting THD is lower than that produced by the linear controller (see Figure 5.17(a)). Moreover, Figure 5.17(b) displays the relative current THD. It can be concluded that the experimental results are in agreement with the respective simulation results presented in Section 5.5.1.



(a) Capacitor voltage v_{C_1} and its reference in [V]



(b) Inductor current i_{L_1} in [A]



(c) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A]

Figure 5.19: Experimental results for a step change in the output current reference with a PI-based controller.

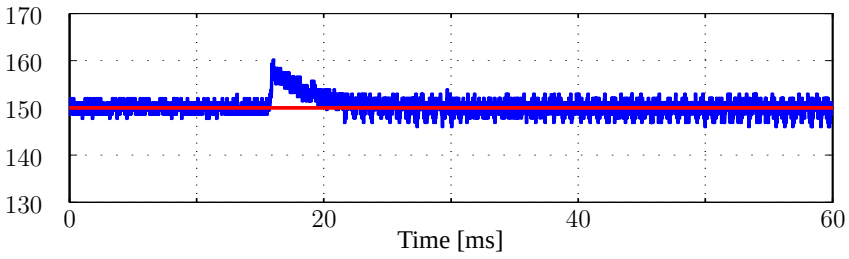
5.6.3 Transient Response

The transient response of the proposed MPC strategy is examined with a $5T_s$ horizon and a switching frequency of $5\,\text{kHz}$. Again, for comparison purposes the transient performance of the PI-based controller is also scrutinized. The transient operation is examined in three cases: with step change in the output current reference, step change in the input dc voltage, and when the converter switch from buck to boost mode.

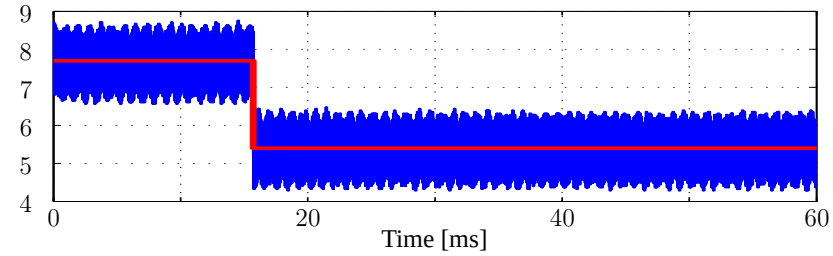
5.6.3.1 Step Change in the Output Current Reference

In this experiment, the desired output power $P_{o,\text{ref}}$ is stepped up from 135 to $540\,\text{W}$, thus the output current reference is stepped up from $3\,\text{A}$ to $6\,\text{A}$. Accordingly, the inductor current reference changes from $1.9\,\text{A}$ to $7.7\,\text{A}$ ($i_{L_1,\text{ref}} = P_{o,\text{ref}}/v_{\text{in}}$). The dc- and ac-side results with the MPC are shown in Figure 5.18, whereas the respective results with the linear controller are shown in Figure 5.19.

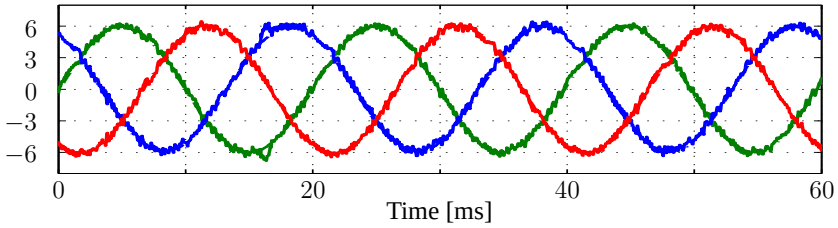
As can be seen in Figure 5.18(b), when MPC is employed, the inductor current tracks its



(a) Capacitor voltage v_{C_1} and its reference in [V]



(b) Inductor current i_{L_1} and its reference in [A]



(c) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A]

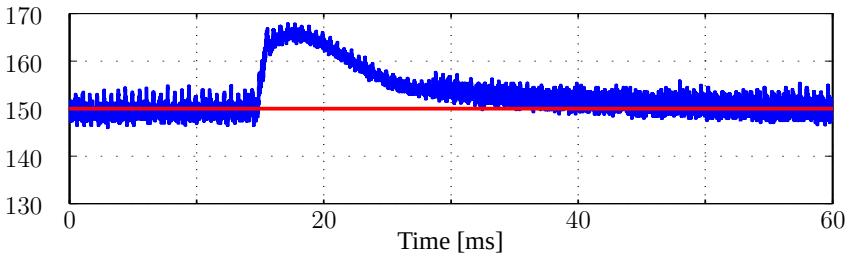
Figure 5.20: Experimental results for a step change in the input dc voltage with MPC and a $5T_s$ prediction horizon length.

reference both before and after the change in its reference value. Moreover, the capacitor voltage is kept constant to its reference value of $150\,\text{V}$ (see Figure 5.18(a)). It can be claimed that the proposed MPC offers a very good transient response with very short settling times for both the capacitor voltage and the inductor current. The dc side of the qZSI shows a good transient response when controlled with the linear control scheme, as well, see Figure 5.19. However, in comparison with the proposed MPC, the PI-based controller shows slower transient response.

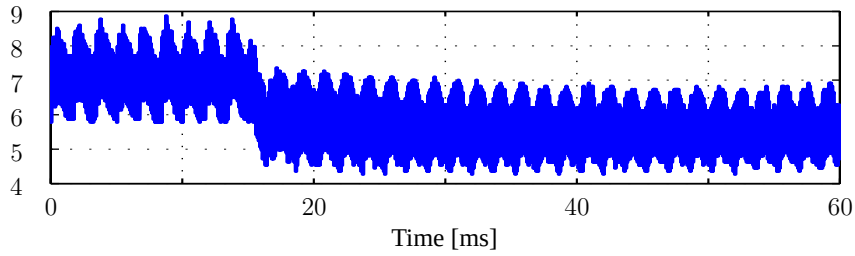
As for the ac side of the qZSI, both MPC and PI manage to eliminate the steady-state error (Figures 5.18(c) and 5.19(c)). Nonetheless, MPC exhibits superior behavior during the transient.

5.6.3.2 Step Change in the Input dc Voltage

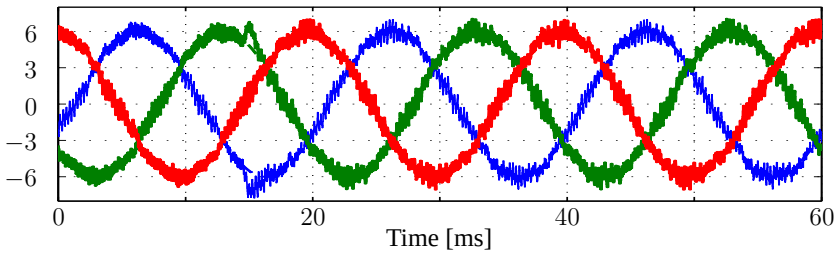
As previously mentioned, the qZSI proposes an attractive solution for the PV systems. In such a case, the resulting dc voltage from the PV is not constant, since it can change with the temperature and the solar radiation level during the day. In order to examine the performance of



(a) Capacitor voltage v_{C_1} and its reference in [V]



(b) Inductor current i_{L_1} in [A]

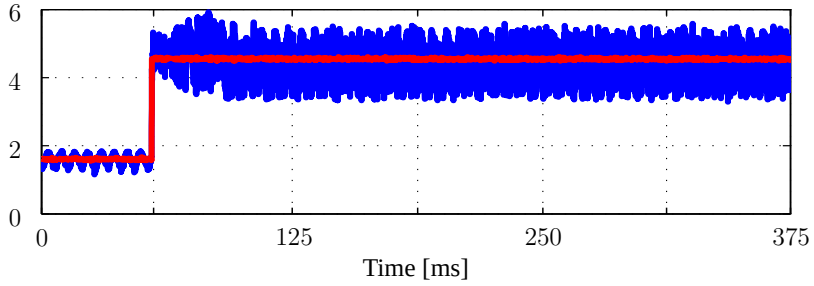


(c) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A]

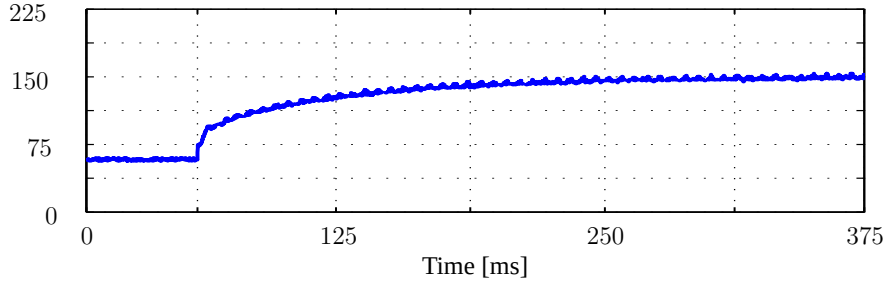
Figure 5.21: Experimental results for a step change in the input dc voltage with a PI-based controller.

the proposed MPC strategy under such conditions, the input voltage is stepped up from $70\,\mathrm{V}$ to $100\,\mathrm{V}$, while keeping the output current reference fixed at $6\,\mathrm{A}$ and the capacitor voltage reference at $150\,\mathrm{V}$. In accordance with these settings, the inductor current reference changes from $7.7\,\mathrm{A}$ to $5.4\,\mathrm{A}$, where $i_{L_1,\mathrm{ref}} = P_{o,\mathrm{ref}}/v_{\mathrm{in}}$. The results of MPC and PI control are shown in Figures 5.20 and 5.21, respectively.

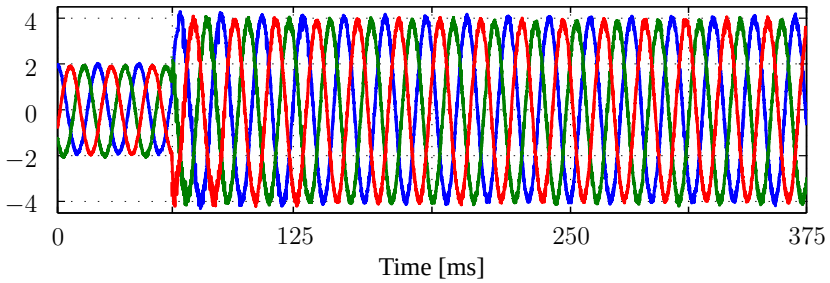
As can be seen in Figure 5.20(a), the capacitor voltage remains practically unaffected by this change in the input voltage, with only a small overshoot observed, whereas the inductor current quickly reaches its new reference value, see Figure 5.20(b). The effectiveness of the proposed MPC is also verified by the ac-side result (Figure 5.20(c)); as can be seen the output current exhibits very small fluctuations during the transient time. When the PI controller is employed, the ac-side response, shown in Figure 5.20(c), is comparable with the one of the proposed MPC in terms of the time the transients lasts. However, the capacitor voltage displays a double overshoot and it takes longer time to return to its reference value, Figure 5.21(a).



(a) Inductor current i_{L_1} and its reference in [A]



(b) Capacitor voltage v_{C_1} in [V]



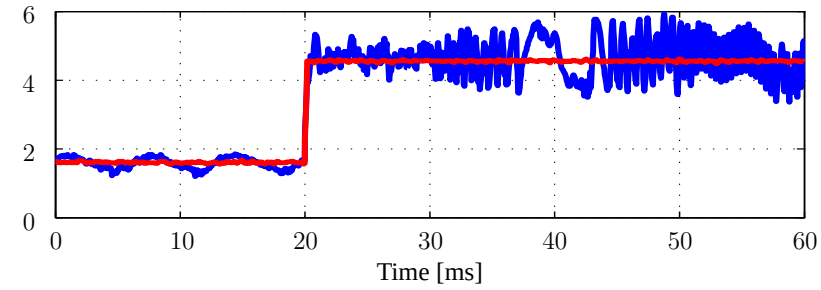
(c) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A]

Figure 5.22: Experimental results for a step change in the output current reference (from buck to boost mode) with MPC and a $5T_s$ prediction horizon length.

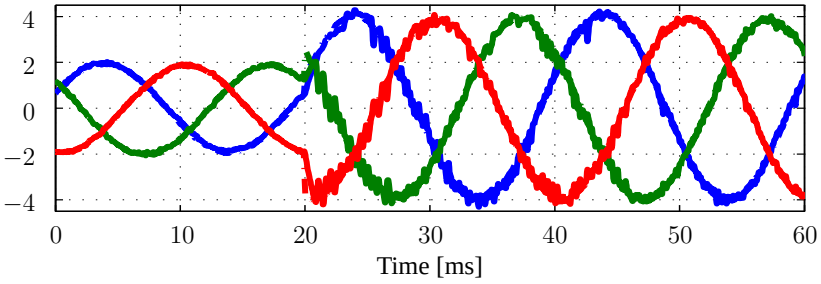
5.6.3.3 Buck to Boost Mode Transition

In this test, the output current is stepped up from 2 A (buck mode) to 4 A (boost mode). Accordingly, the inductor current reference changes from 1.8 A to 4.5 A. The experimental dc- and ac-side results are shown in Figure 5.22.

As can be seen in Figure 5.22(a), the inductor current tracks its reference both before and after the change in its reference value, i.e. both in buck and boost mode, see also Figure 5.23(a) where the transient is depicted in more detail. This is thanks to the discrete-time model of the converter, derived in Section 5.2, which allows for the controller to accurately predict the system behavior not only over a limited range of operating points, but rather over the whole operating regime.



(a) Inductor current i_{L_1} and its reference in [A]



(b) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A]

Figure 5.23: Zoomed-in experimental results of Figure 5.22.

As for the ac-side, MPC manages to eliminate the steady-state error (Figures 5.22(c)), with a very short transient time as shown in Figure 5.23(b).

From the presented analysis, it can be concluded that the proposed long-horizon MPC has superior tracking abilities for all variables of concern, while it introduces zero steady-state error, low current THD, and very short transient times. These characteristics indicate an overall performance improvement of the qZSI.

5.7 Summary

This chapter proposes a long-horizon direct model predictive current control scheme for the quasi-Z-source inverter connected with an RL load. To achieve an improved system performance, as quantified by the output current THD, as well as to ensure closed-loop stability, while controlling the switching frequency, long prediction horizons are required. However, in such a case enumeration of all candidate solutions becomes computationally prohibitive. To solve the underlying optimization problem in real time, a nontrivial prediction horizon—as resulted from a move blocking scheme—is implemented which, combined with a branch-and-bound technique, allows to keep the computational burden modest. The proposed techniques facilitate the implementation of a long-horizon MPC in an FPGA.

The simulation and the experimental results verify the superior performance of long-prediction horizon MPC when compared to the existing one-step horizon MPC as well as to the established linear PI-based controller. More specifically, the proposed long-horizon di-

rect MPC exhibits better steady-state behavior with lower output current THD, while, at the same time, it shows a much faster dynamic response on both sides of the qZSI.

CHAPTER 6

Direct Model Predictive Voltage Control Strategy

This chapter presents a direct model predictive voltage control strategy for an UPS systems, consisting of a quasi-Z-source inverter connected to a linear/nonlinear load via an intermediate LC filter. To address time-varying and unknown loads as well as to reduce the number of measurement sensors required, a Kalman observer is added to estimate the load current.

6.1 Motivation

Considering the complexity of a UPS system consisting of a qZSI, an LC filter, and a (linear/nonlinear) load as well as the advantages of the MPC, this chapter presents an MPC strategy for such applications. The main objective of the controller is to track the reference output voltage under any type of load (linear or nonlinear). Note that MPC for the qZSI has been examined in [71,103,105,112,115]. In these works, however, MPC is designed as a current controller, i.e. the main control objective is the regulation of the load current to its reference value. Moreover, in all cases examined a linear (RL) load is considered. Hence, a voltage-mode MPC strategy for the qZSI with any type of load has yet to be investigated. At the same time, the control scheme aims to regulate the dc-side variables (the capacitor voltage and the inductor current) to their demanded values. To achieve these control goals, a model of the system is derived that accurately predicts its behavior over the whole operating regime. To deal with unknown loads as well as to reduce the hardware cost, a Kalman observer is designed which accurately estimates the load current based on the measured inverter current and output voltage.

To investigate the steady-state and dynamic performance of the proposed MPC algorithm, experimental work is conducted based on an FPGA. Finally, to highlight the benefits of the presented method, the outcomes of the experiments are compared with those resulted from a conventional linear voltage control scheme based on PI controllers.

This chapter is organized as follows. In Section 6.2, the mathematical model of the qZSI is derived. A Kalman observer for the output current is designed in Section 6.3. Next, the proposed

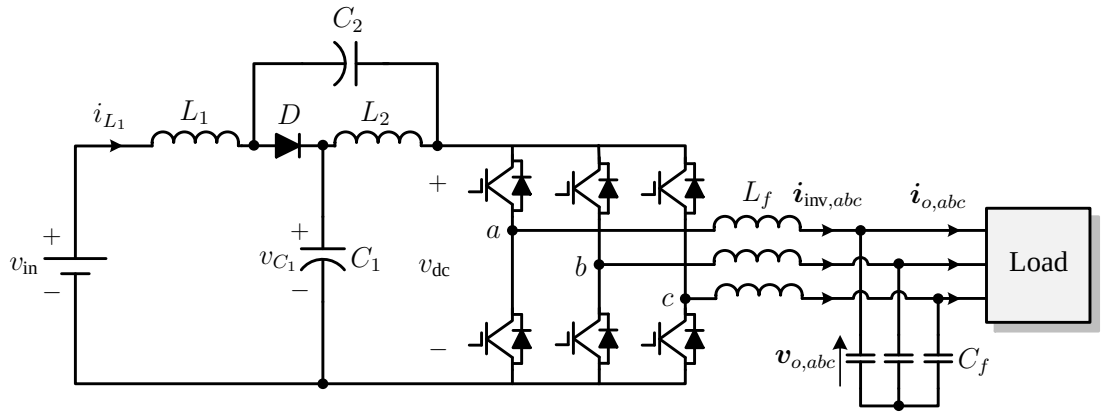


Figure 6.1: The quasi-Z-source inverter (qZSI) connected with an LC filter and a load.

MPC strategy is described in Section 6.4, whereas the conventional PI-based control scheme is outlined in Section 6.5. In Section 6.6, the experimental results are presented. Section 6.7 draws conclusions.

6.2 Mathematical Model

The configuration of the system under discussion is presented in Figure 6.1. It consists of a qZS network, a two-level VSI, an LC filter, and a load. Note that the model introduced in chapter 5 is different from the one which is presented here as the circuit configurations are different, compare Figures 5.1 and 6.1.

As previously mentioned, the qZSI operates as the conventional VSI in the so-called non-shoot-through state (NST), see Figure 5.2(a) in chapter 5, thus the possible switch positions are eight with six of them being the so-called active states and two the zero states. However, the qZSI can operate in an additional state called shoot-through state (Figure 5.2(b) in chapter 5). In that state—besides the above-mentioned switch positions—an additional switch position is introduced that allows at least one phase leg of the inverter to be short circuited. Thanks to that additional switch position, the converter is able to boost the input voltage v_{in} to the required dc-link voltage level v_{dc}.

Consequently, the qZSI has two modes of operation, i.e. the buck and the boost mode; in buck mode the converter operates as the conventional two-level VSI (based on the non-shoot-through switching states that are used with the conventional VSI), whereas in boost mode the qZSI introduces two operation states, namely the shoot-through and the non-shoot-through state, see Figure 5.2.

Again to simplify the computations, the variables in the analysis that follows are expressed in the stationary orthogonal system $(\alpha\beta)$ instead of the three-phase system (abc), i.e. $\boldsymbol{\xi}_{\alpha\beta} = \boldsymbol{K}\boldsymbol{\xi}_{abc}$, where $\boldsymbol{K}$ is the Clarke transformation matrix .

The system states include the output voltage (load voltage) and the inverter current of the ac side as well as the inductor currents and the capacitor voltages of the dc side. Thus, the state vector is

$$\boldsymbol{x} = [v_{o,\alpha}\ v_{o,\beta}\ i_{\text{inv},\alpha}\ i_{\text{inv},\beta}\ i_{L_1}\ i_{L_2}\ v_{C_1}\ v_{C_2}]^T \in \mathbb{R}^8\,. \tag{6.1}$$

The three-phase switch position $\boldsymbol{u}_{abc} \in \mathcal{U}^3$ is considered the input to the system, where $\boldsymbol{u}_{abc} = [u_a\ u_b\ u_c]^T$ and $\mathcal{U} = \{0, 1\}$. Moreover, the output variables include the output voltage, the inductor current, and the capacitor voltage, i.e.

$$\boldsymbol{y} = [v_{o,\alpha}\ v_{o,\beta}\ i_{L_1}\ v_{C_1}]^T \in \mathbb{R}^4\,. \tag{6.2}$$

Finally, the load current and the input voltage are treated as disturbances to the system, i.e.

$$\boldsymbol{w} = [i_{o,\alpha}\ i_{o,\beta}\ v_{\text{in}}]^T \in \mathbb{R}^3\,. \tag{6.3}$$

The full model of the system configuration, shown in Figure 6.1, can be derived by considering the different operating modes and states of the qZSI. The derived models are then combined in one model which precisely describes the system behavior over the whole operating range.

6.2.1 Boost Mode Operation

As previously stated, the qZSI in boost mode operation has two types of switching states; non-shoot-through and shoot-through state. The corresponding model for each state will be separately derived as follows.

6.2.1.1 Non-Shoot-Through State

During the non-shoot-through state (Figure 5.2(a)), the diode is forward-biased, thus the input voltage source and the inductors charge the capacitors and supply energy to the load. The converter model is given by

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \boldsymbol{F}_1\boldsymbol{x}(t) + \boldsymbol{G}\boldsymbol{u}_{abc}(t) + \boldsymbol{H}\boldsymbol{w}(t) \tag{6.4a}$$

$$\boldsymbol{y}(t) = \boldsymbol{E}\boldsymbol{x}(t)\,, \tag{6.4b}$$

where

$$\boldsymbol{F}_1 = \begin{bmatrix} 0 & 0 & \frac{1}{C_f} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_f} & 0 & 0 & 0 & 0 \\ -\frac{1}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_2} \\ 0 & 0 & -\frac{\boldsymbol{u}_{abc}^T\boldsymbol{K}^{-1}_{(:,1)}}{C_1} & -\frac{\boldsymbol{u}_{abc}^T\boldsymbol{K}^{-1}_{(:,2)}}{C_1} & \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & -\frac{\boldsymbol{u}_{abc}^T\boldsymbol{K}^{-1}_{(:,1)}}{C_2} & -\frac{\boldsymbol{u}_{abc}^T\boldsymbol{K}^{-1}_{(:,2)}}{C_2} & 0 & \frac{1}{C_2} & 0 & 0 \end{bmatrix}$$

and

$$\boldsymbol{G} = \hat{v}_{\text{dc}} \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{1}{L_f} & 0 \\ 0 & \frac{1}{L_f} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \boldsymbol{K},\ \boldsymbol{H} = \begin{bmatrix} -\frac{1}{C_f} & 0 & 0 \\ 0 & -\frac{1}{C_f} & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_1} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix},$$

$$\boldsymbol{E} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix},$$

with L_f (C_f) being the output filter inductance (capacitance), and L_1 (C_1) are the inductance (capacitance) of the qZS network. Moreover, $\hat{v}_{\text{dc}}$ is the peak dc-link voltage (see Section 5.2.4).

6.2.1.2 Shoot-Through State

As shown in Figure 5.2(b), in the shoot-through state the input voltage source and the capacitors charge the inductors, while the diode is cut-off. The system at the this state is described by the following expression

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \boldsymbol{F}_2\boldsymbol{x}(t) + \boldsymbol{G}\boldsymbol{u}_{abc}(t) + \boldsymbol{H}\boldsymbol{w}(t) \tag{6.5a}$$

$$\boldsymbol{y}(t) = \boldsymbol{E}\boldsymbol{x}(t)\,, \tag{6.5b}$$

where

$$\boldsymbol{F}_2 = \begin{bmatrix} 0 & 0 & \frac{1}{C_f} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_f} & 0 & 0 & 0 & 0 \\ -\frac{1}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{L_1} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{C_2} & 0 & 0 & 0 \end{bmatrix}.$$

6.2.2 Buck Mode Operation

In buck mode, the qZSI operates as the conventional VSI. Thus, only the ac side of qZSI is considered for the system model as follows

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \boldsymbol{F}_3\boldsymbol{x}(t) + \boldsymbol{G}\boldsymbol{u}_{abc}(t) \tag{6.6a}$$

$$\boldsymbol{y}(t) = \boldsymbol{E}\boldsymbol{x}(t)\,, \tag{6.6b}$$

where the only nonzero entries of $\boldsymbol{F}_3$ are $\boldsymbol{F}_{3_{(1,3)}} = \boldsymbol{F}_{3_{(2,4)}} = 1/C_f$ and $\boldsymbol{F}_{3_{(3,1)}} = \boldsymbol{F}_{3_{(4,2)}} = -1/L_f$.

6.2.3 Continuous-Time Model

In order to derive an universal model that captures the different modes and states of the qZSI, as given by (6.4), (6.5), and (6.6), two auxiliary binary variables $\acute{d}_{\text{aux}_1}$ and $\acute{d}_{\text{aux}_2}$ are introduced. The first variable $\acute{d}_{\text{aux}_1}$ designates the state at which the converter operates in boost mode, i.e.

$$\acute{d}_{\text{aux}_1} = \begin{cases} 0 & \text{if non-shoot-through state} \\ 1 & \text{if shoot-through state} \end{cases}. \tag{6.7}$$

The second variable $\acute{d}_{\text{aux}_2}$ denotes the operation mode of the converter, i.e.

$$\acute{d}_{\text{aux}_2} = \begin{cases} 0 & \text{if buck mode} \\ 1 & \text{if boost mode} \end{cases}. \tag{6.8}$$

The transition from buck to boost mode (and vice versa) depends on whether the capacitor voltage reference ($v_{C_1,\text{ref}}$) becomes greater (less) than the input dc voltage (v_{in}). When the capacitor voltage reference is higher than the input dc voltage, then the converter operates in boost mode, otherwise it works in buck mode.

Considering the defined variables in (6.7) and (6.8) with the derived models (6.4), (6.5) and (6.6), the full model of the converter can be expressed by

$$\frac{\mathrm{d}\boldsymbol{x}(t)}{\mathrm{d}t} = \boldsymbol{F}\boldsymbol{x}(t) + \boldsymbol{G}\boldsymbol{u}_{abc}(t) + \acute{d}_{\text{aux}_2}\boldsymbol{H}\boldsymbol{w}(t) \tag{6.9a}$$

$$\boldsymbol{y}(t) = \boldsymbol{E}\boldsymbol{x}(t)\,, \tag{6.9b}$$

where $\boldsymbol{F} = \boldsymbol{F}_a + \acute{d}_{\text{aux}_2}\boldsymbol{F}_b$, with $\boldsymbol{F}_a = \boldsymbol{F}_3$ and

$$\boldsymbol{F}_b = \begin{bmatrix} 0 & 0 & \frac{1}{C_f} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_f} & 0 & 0 & 0 & 0 \\ -\frac{1}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{\acute{d}_{\text{aux}_1}-1}{L_1} & \frac{\acute{d}_{\text{aux}_1}}{L_1} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{\acute{d}_{\text{aux}_1}}{L_2} & \frac{\acute{d}_{\text{aux}_1}-1}{L_2} \\ 0 & 0 & \frac{(\acute{d}_{\text{aux}_1}-1)\boldsymbol{u}_{abc}^T\boldsymbol{K}^{-1}_{(:,1)}}{C_1} & \frac{(\acute{d}_{\text{aux}_1}-1)\boldsymbol{u}_{abc}^T\boldsymbol{K}^{-1}_{(:,2)}}{C_1} & \frac{1-\acute{d}_{\text{aux}_1}}{C_1} & -\frac{\acute{d}_{\text{aux}_1}}{C_1} & 0 & 0 \\ 0 & 0 & \frac{(\acute{d}_{\text{aux}_1}-1)\boldsymbol{u}_{abc}^T\boldsymbol{K}^{-1}_{(:,1)}}{C_2} & \frac{(\acute{d}_{\text{aux}_1}-1)\boldsymbol{u}_{abc}^T\boldsymbol{K}^{-1}_{(:,2)}}{C_2} & -\frac{\acute{d}_{\text{aux}_1}}{C_2} & \frac{1-\acute{d}_{\text{aux}_1}}{C_2} & 0 & 0 \end{bmatrix}.$$

6.2.4 Discrete-Time Model

The continuous-time model (6.9) is discretized by using forward Euler approximation. Consequently, the discrete-time model of the qZSI is defined as

$$\boldsymbol{x}(k+1) = \boldsymbol{A}\boldsymbol{x}(k) + \boldsymbol{B}\boldsymbol{u}_{abc}(k) + \boldsymbol{D}\boldsymbol{w}(k) \tag{6.10a}$$
$$\boldsymbol{y}(k) = \boldsymbol{C}\boldsymbol{x}(k)\,, \tag{6.10b}$$

where $\boldsymbol{A} = (\boldsymbol{F} + \boldsymbol{I})T_s$, $\boldsymbol{B} = \boldsymbol{G}T_s$, $\boldsymbol{D} = \boldsymbol{H}T_s$ and $\boldsymbol{C} = \boldsymbol{E}$. Moreover, $\boldsymbol{I}$ denotes the identity matrix, T_s is the sampling interval, and $k \in \mathbb{N}$.

6.3 Kalman Observer for the Output current

In order to reduce the hardware cost as well as to address load variations, the output current $\boldsymbol{i}_o$ is not directly measured, but it is rather estimated by an observer. That observer could be a very simple one, i.e. one based on the prediction of the output voltage $\boldsymbol{v}_o$ as given by (6.10a). However, such an estimation scheme is susceptible to measurement noise as will be shown in Section 6.6. Therefore, a Kalman observer is implemented instead which estimates the output current without deteriorating the system performance. Note that the design of the estimation loop presented hereafter is motivated by [50].

First of all, the output current needs to be augmented to the output filter model. To do so, the output current is assumed to be constant since it changes slowly compared with the sampling interval. Subsequently,

$$\frac{d\boldsymbol{i}_o}{dt} = 0\,. \tag{6.11}$$

Hence, the observer model can be written as

$$\frac{\mathrm{d}\boldsymbol{x}_o(t)}{\mathrm{d}t} = \boldsymbol{F}_o\boldsymbol{x}_o(t) + \boldsymbol{G}_o\boldsymbol{u}_{abc}(t) \tag{6.12a}$$

$$\boldsymbol{y}_o(t) = \boldsymbol{E}_o\boldsymbol{x}_o(t) \tag{6.12b}$$

The observer model includes the output voltage, the inverter current, and the output current as state variables, i.e. $\boldsymbol{x}_o = [v_{o,\alpha}\ v_{o,\beta}\ i_{\text{inv},\alpha}\ i_{\text{inv},\beta}\ i_{o,\alpha}\ i_{o,\beta}]^T \in \mathbb{R}^6$. In addition, the output vector consists of the output voltage and the inverter current, i.e. $\boldsymbol{y}_o = [v_{o,\alpha}\ v_{o,\beta}\ i_{inv,\alpha}\ i_{inv,\beta}]^T \in \mathbb{R}^4$. The matrices $\boldsymbol{F}_o$, $\boldsymbol{G}_o$, and $\boldsymbol{E}_o$ of the observer model are

$$\boldsymbol{F}_o = \begin{bmatrix} 0 & 0 & \frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 \\ 0 & 0 & 0 & \frac{1}{C_f} & 0 & -\frac{1}{C_f} \\ -\frac{1}{L_f} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{L_f} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}.$$

and

$$\boldsymbol{G}_o = \hat{v}_{\text{dc}} \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L_f} \\ \frac{1}{L_f} \\ 0 \\ 0 \end{bmatrix} \boldsymbol{K},\ \boldsymbol{E}_o = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix}.$$

It is worthwhile to mention that the Kalman observer is designed based on the discrete-time model of the system [116]. Consequently, using forward Euler approximation, the observer model in (6.12) is discretized. The resulting discrete-time state-space representation is given by the following equations.

$$\boldsymbol{x}_o(k+1) = \boldsymbol{A}_o\boldsymbol{x}_o(k) + \boldsymbol{B}_o\boldsymbol{u}_{abc}(k) + \boldsymbol{\zeta}(k) \tag{6.13a}$$

$$\boldsymbol{y}_o(k) = \boldsymbol{C}_o\boldsymbol{x}_o(k) + \boldsymbol{\upsilon}(k)\,, \tag{6.13b}$$

where $\boldsymbol{A}_o = (\boldsymbol{F}_o + \boldsymbol{I})T_s$, $\boldsymbol{B}_o = \boldsymbol{G}_oT_s$, and $\boldsymbol{C}_o = \boldsymbol{E}_o$. Moreover, $\boldsymbol{\zeta}(k) = [\zeta_1(k) \ldots \zeta_6(k)]^T \in \mathbb{R}^6$ and $\boldsymbol{\upsilon}(k) = [\upsilon_1(k) \ldots \upsilon_4(k)]^T \in \mathbb{R}^4$ represent the process and measurement noise, respectively. For simplicity, they are assumed to be independent and with normal probability distributions,

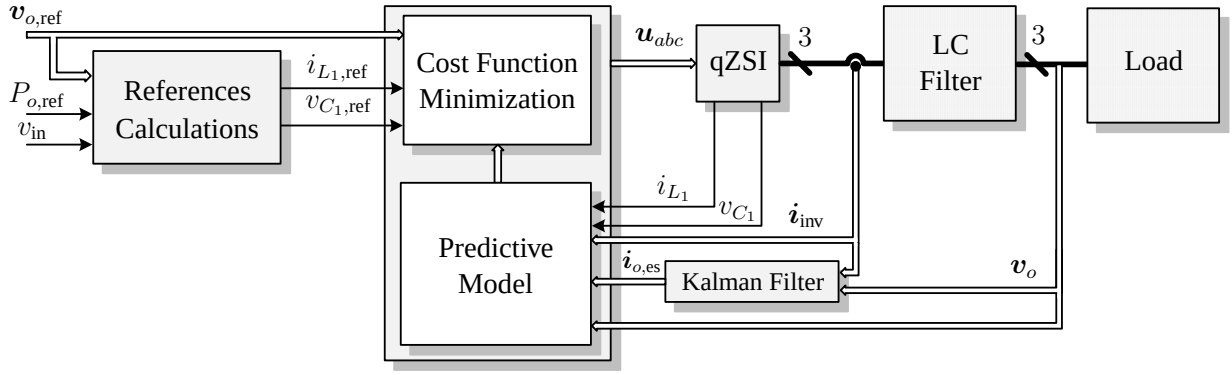


Figure 6.2: Model predictive voltage control strategy for the qZSI.

i.e. $p(\zeta) \sim N(0, \boldsymbol{Z})$ and $p(\upsilon) \sim N(0, \boldsymbol{\Upsilon})$, where the covariance matrices $\boldsymbol{Z}$ and $\boldsymbol{\Upsilon}$ are assumed to be constant. Hence, (6.13) can be rewritten as

$$\hat{\boldsymbol{x}}_o(k+1) = \boldsymbol{A}_o\hat{\boldsymbol{x}}_o(k) + \boldsymbol{B}_o\boldsymbol{u}_{abc}(k) + \boldsymbol{L}\left(\boldsymbol{y}_o(k) - \hat{\boldsymbol{y}}_o(k)\right) \tag{6.14a}$$

$$\hat{\boldsymbol{y}}_o(k) = \boldsymbol{C}_o\hat{\boldsymbol{x}}_o(k)\,, \tag{6.14b}$$

where $\hat{\boldsymbol{x}}_o(k)$ and $\hat{\boldsymbol{y}}_o(k)$ are the estimated state and output vectors, respectively, and $\boldsymbol{L}\left(\boldsymbol{y}_o(k) - \hat{\boldsymbol{y}}_o(k)\right)$ is the Kalman correcting term, with $\boldsymbol{L}$ being the Kalman gain which is computed off-line [116, 117].

6.4 Direct Model Predictive Voltage Control

Figure 6.2 shows the block diagram of the proposed voltage-mode MPC strategy. Based on the model of the converter (see (6.10)) the system state at step $k+1$ is computed for all admissible switch positions $\boldsymbol{u}_{abc}$. The predicted values are calculated based on the present measurements and estimates of the ac side (i.e. the output voltage, the inverter current, and the output current) as well as on the measurements of the dc side (the inductor current and the capacitor voltage). The switch position (i.e. the switching signals) that results in the best system performance, as quantified by a to-be-minimized cost function, is then determined and *directly* applied to the converter.

6.4.1 Control Objectives

The main control objective of the proposed MPC approach is to accurately regulate the output voltage $\boldsymbol{v}_o$ along its reference value $\boldsymbol{v}_{o,\text{ref}}$. In addition, the capacitor voltage v_{C_1} and the inductor current i_{L_1} should track their reference trajectories in order to successfully boost the input voltage to the desired dc-link voltage. These objectives have to be met while the switching frequency of the converter is kept relatively low to avoid excessive switching losses.

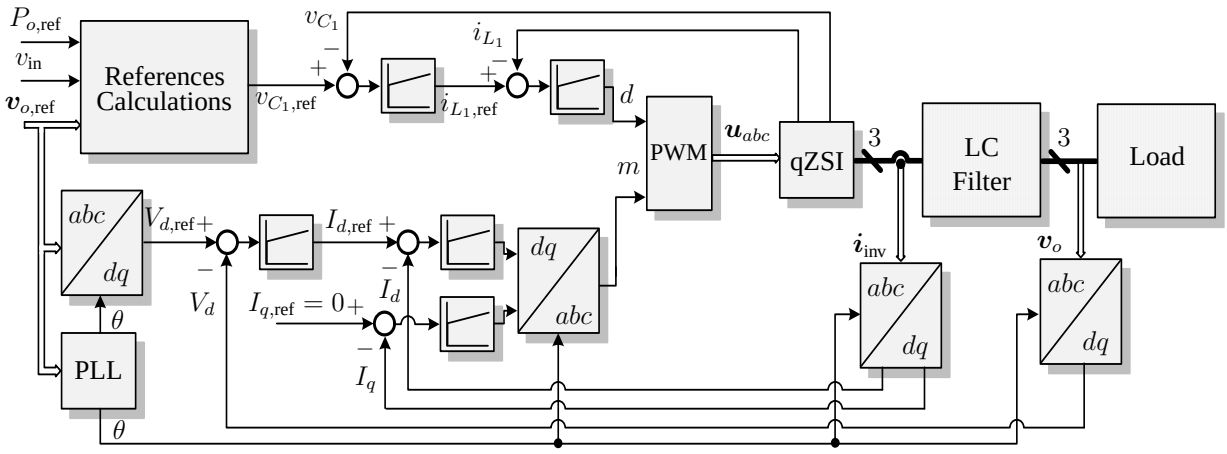


Figure 6.3: Linear voltage control scheme based on PI controllers for the qZSI.

6.4.2 Optimal Control Problem

Based on the aforementioned objectives two terms are introduced. The first term relates to the output tracking error, i.e. $\boldsymbol{y}_{\text{ref}} - \boldsymbol{y}$, with $\boldsymbol{y}_{\text{ref}} = [v_{o,\alpha,\text{ref}}\ v_{o,\beta,\text{ref}}\ i_{L_1,\text{ref}}\ v_{C_1,\text{ref}}]^T \in \mathbb{R}^4$, while the second term, i.e. $\Delta\boldsymbol{u}_{abc}(k) = \boldsymbol{u}_{abc}(k) - \boldsymbol{u}_{abc}(k-1)$, is associated with the switching effort and it is added to control the inverter switching frequency by penalizing the switching transitions. As a result, the cost function is

$$J(k) = ||\boldsymbol{y}_{\text{ref}}(k+1) - \boldsymbol{y}(k+1)||^2_{\boldsymbol{Q}} + \lambda_u ||\Delta\boldsymbol{u}_{abc}(k)||^2 . \tag{6.15}$$

In (6.15), the diagonal positive semidefinite matrix $\boldsymbol{Q} \in \mathbb{R}^{4\times4}$ and the weighting factor $\lambda_u > 0$ are added to adjust the trade-off between the system tracking accuracy and the switching frequency.

Taking into account the system model (6.10) and the cost function (6.15), the following optimization problem is formulated and solved in real time at time-step k.

$$\begin{aligned} \underset{\boldsymbol{u}_{abc}}{\text{minimize}} \quad & J(k) \\ \text{subject to} \quad & \text{eq. (6.10)} . \end{aligned} \tag{6.16}$$

The solution $\boldsymbol{u}^*_{abc}$ to problem (6.16) is then applied to the converter at time-step $k+1$. At the next time-step, the whole procedure is repeated with updated measurements and estimates.

6.5 Conventional PI-Based Controller With PWM

In order to evaluate and compare the performance of the proposed MPC scheme, a linear PI-based control for the qZSI is implemented as shown in Figure 6.3. Multi-loop PI-based controllers are used on each side of the qZSI. The dc-side PI controller aims to regulate the capacitor voltage v_{C_1} and the inductor current i_{L_1} of the qZS network by controlling the shoot-through duty cycle d. On the ac side, the controller manipulates the inverter modulation index m in

Table 6.1: System Parameters

Parameter	Value
Input voltage v_{in}	$150\,\text{V}$
qZS inductances L_1, L_2	$1\,\text{mH}$
qZS capacitances C_1, C_2	$480\,\mu\text{F}$
Output LC filter	$10\,\text{mH}$, $50\,\mu\text{F}$
RL load	$20\,\Omega, 2.5\,\text{mH}$
PWM carrier frequency	$5\,\text{kHz}$
Sampling interval T_s	$20\,\mu\text{s}$

order to control the output voltage. To eliminate the steady-state error on the ac side, the controller is designed in the rotating dq frame, see Figure 6.3. Hence, a phase-locked loop (PLL) is used to compute the instantaneous angular position θ of the output voltage required for the transformation from the abc to the dq frame, and vice versa.

Both the shoot-through duty cycle d and the modulation index m are delivered to the pulse width modulation (PWM) block in order to generate the switching signals.

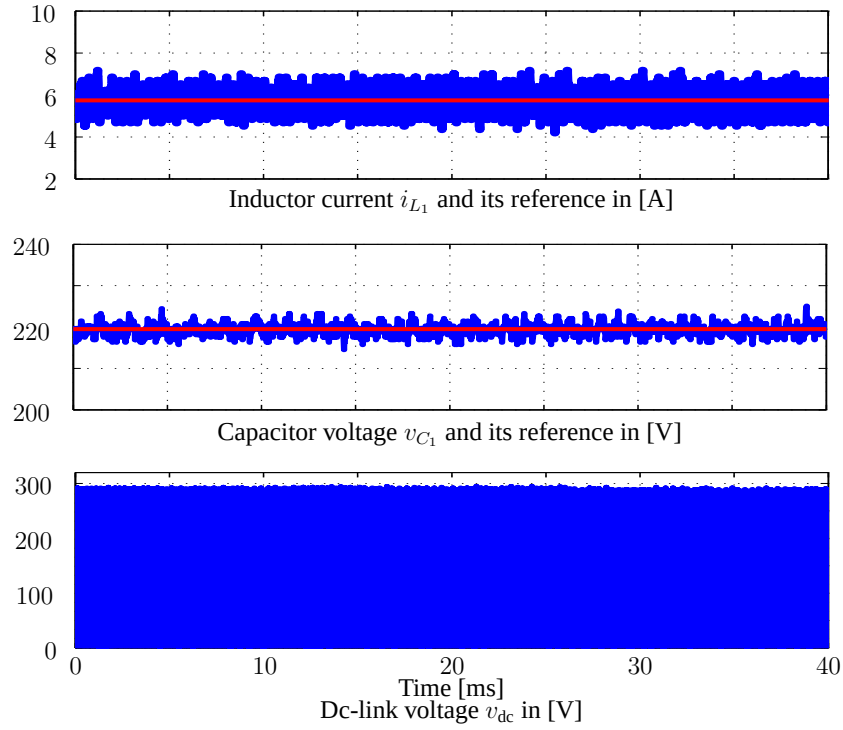
6.6 Experimental Evaluation

To evaluate the performance of the proposed MPC strategy and the traditional PI-based controller for the qZSI configuration (Figure 6.1), several experiments were carried out in the laboratory. The system parameters are shown in Table 6.1. Both controllers were implemented on an FPGA Cyclone III-EP3C40Q240C8. For more details about the test bench, please refer to appendix C.

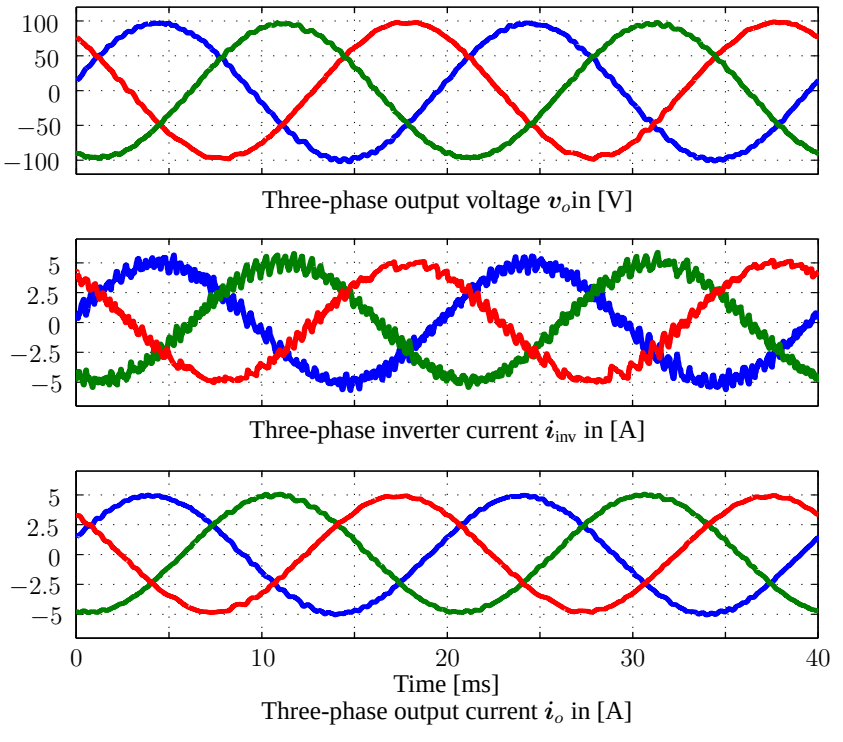
The output voltage reference $v_{o,\text{ref}}$ was set to $100\,\text{V}$. In order not to affect the sinusoidal waveform of the output voltage and prevent the interacting between the ac and dc side, the capacitor voltage reference $v_{C_1,\text{ref}}$ should be higher than double the output voltage reference [24]. Hence, the capacitor voltage reference was chosen to be $220\,\text{V}$ (i.e. $v_{C_1,\text{ref}} = 2.2 \cdot v_{o,\text{ref}}$). Based on the required output power $(P_{o,\text{ref}})$, the inductor current reference was computed according to $i_{L_1,\text{ref}} = P_{o,\text{ref}}/v_{in}$. For all MPC experiments shown below, the qZSI was operated at a switching frequency of approximately $f_{\text{sw}} \approx 5\,\text{kHz}$ by choosing $\boldsymbol{Q} = \text{diag}(1, 1, 0.8, 0.3)$ and by appropriately tuning λ_u in function (6.15). For a fair comparison, the carrier frequency of the PWM for the PI-based control was set to $5\,\text{kHz}$.

6.6.1 Steady-State Operation

The first case to be examined is that of the qZSI connected to a linear RL load, with $R = 20\,\Omega$ and $L = 2.5\,\text{mH}$. In a next step, the system behavior is investigated when a nonlinear load is used instead.

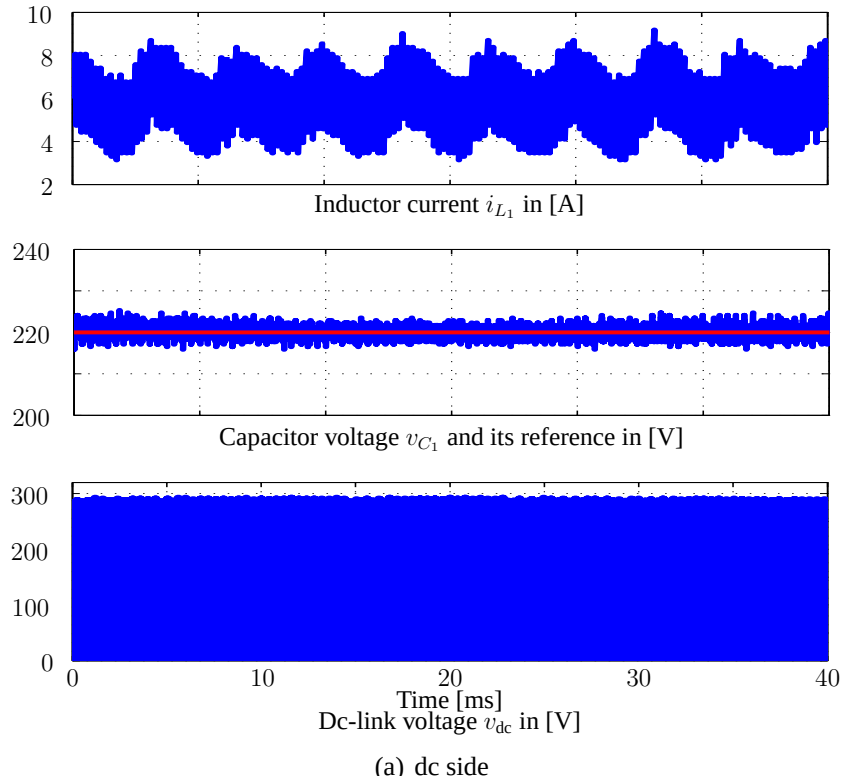


(a) dc side

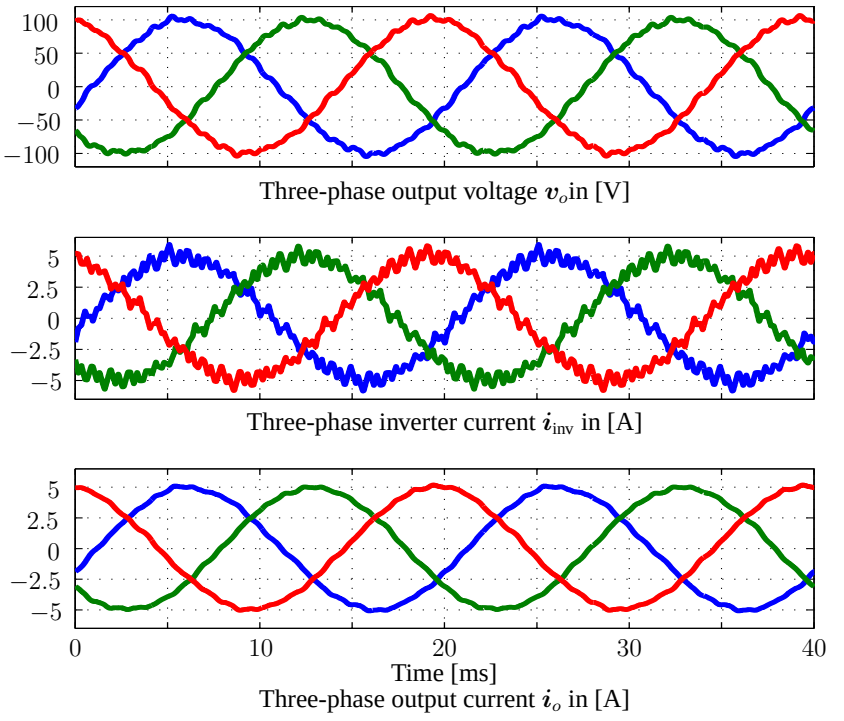


(b) ac side

Figure 6.4: Experimental results of the qZSI with MPC for an RL load. $T_s = 20\,\mu$s and $f_{\text{sw}} = 5\,$kHz.

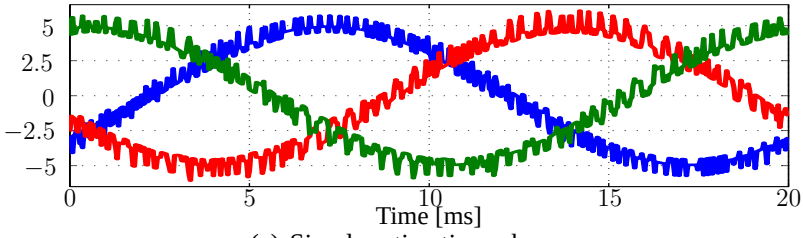


(a) dc side

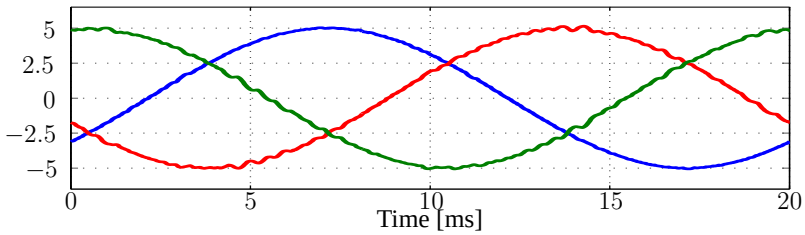


(b) ac side

Figure 6.5: Experimental results of the qZSI with PI-based control for RL load. $T_s = 20\,\mu$s and $f_{sw} = 5\,$kHz.



(a) Simple estimation scheme.



(b) Kalman observer.

Figure 6.6: Three-phase estimated output current $\boldsymbol{i}_{o,\text{es}}$ in [A].

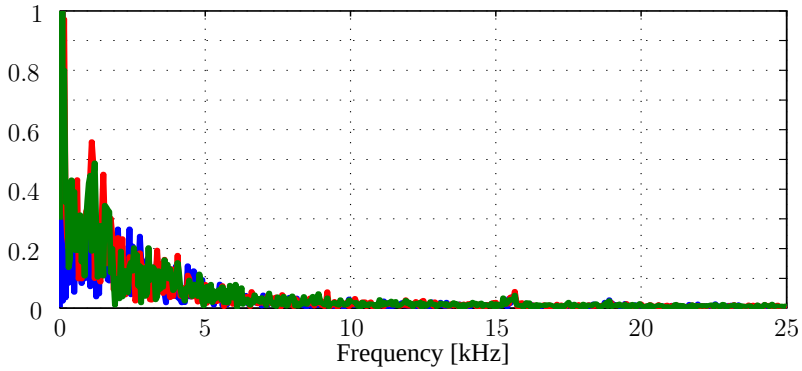
6.6.1.1 Linear Load

The experimental results of the dc and ac side of MPC and PI controllers with the linear load are shown in Figures 6.4 and 6.5, respectively. As observed in Figures 6.4(a) and 6.5(a), both control techniques manage to accurately regulate the inductor current and the capacitor voltage along their references. As a result, a capacitor voltage of $v_{C_1} = 220\,\text{V}$ is achieved, while the dc-link voltage is boosted to the value of $\hat{v}_{\text{dc}} = 290\,\text{V}$. These results are in line with the theoretical analysis presented in Section 5.2.4. Although both controllers have a good steady-state behavior, MPC produces lower current and voltage ripples than the linear controller.

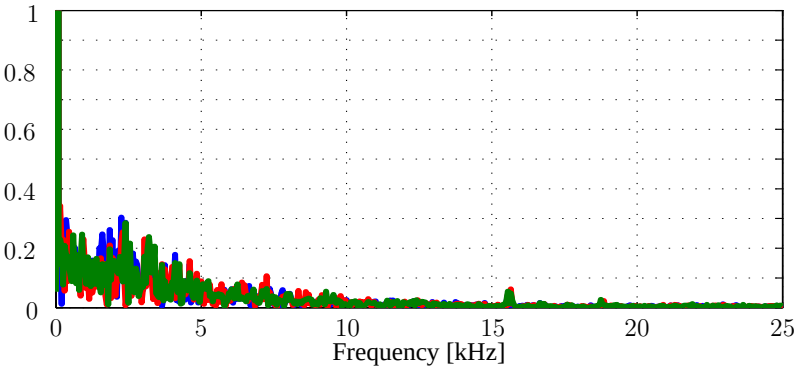
With regard to the ac side, Figures 6.4(b) and 6.5(b) show that the output voltage follows its sinusoidal reference waveform. MPC produces an output voltage with 1.35% total harmonic distortion (THD), whereas the linear control scheme with 1.82% THD. It should be pointed out that, for the examined case, the MPC algorithm is augmented by an estimation scheme based on a Kalman observer. The presented results indicate that MPC manages to control both sides of the qZSI with better overall steady-state performance than the linear PI control.

To demonstrate the effectiveness of the Kalman observer, the output current as estimated by the Kalman observer and the simple estimation scheme—mentioned in Section 6.3—is shown in Figure 6.6. As can be seen, the Kalman observer is less sensitive to noise and thus it can more accurately reconstruct the output current. This remark is also verified by Figure 6.7; with the Kalman observer the THD of the output voltage is $1.35\,\%$, i.e. less than that produced with the simple estimation scheme ($1.99\,\%$). Moreover, the voltage spectrum of the linear controller is illustrated in Figure 6.8. As can be observed, this scheme produces lower output voltage THD than that of MPC with the simple estimation scheme. However, MPC with the Kalman observer outperforms the conventional linear controller.

Therefore it can be concluded, that the designed estimation loop does not deteriorate the performance of the MPC algorithm, but, on the contrary, it allows MPC to clearly demonstrate its benefits to come in surface.



(a) Simple estimation scheme: voltage THD $= 1.99\%$.



(b) Kalman observer: voltage THD $= 1.35\%$.

Figure 6.7: Output voltage spectrum ($\%$) with MPC based on the output current estimation.

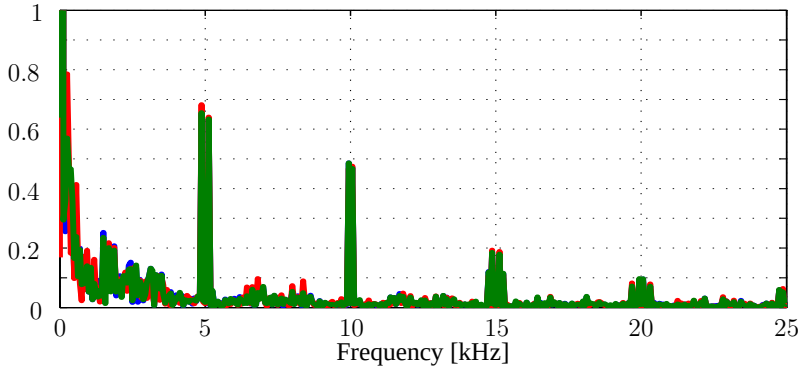
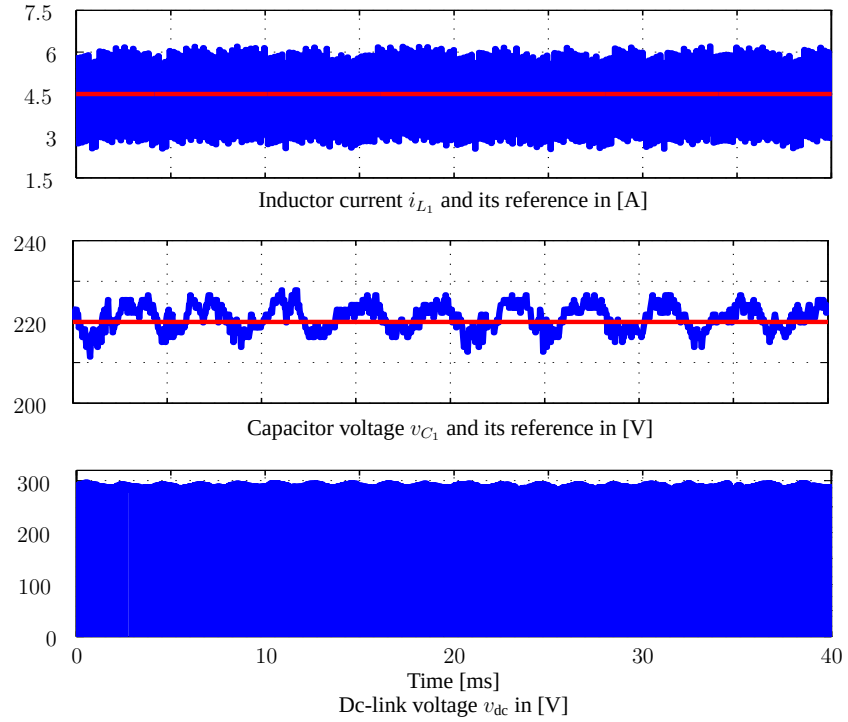


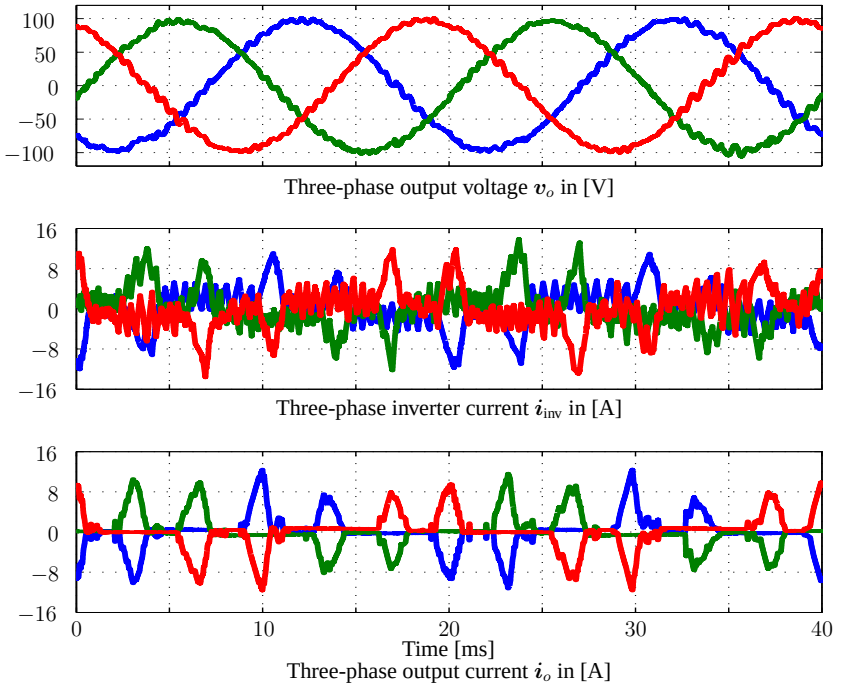
Figure 6.8: Output voltage spectrum ($\%$) with PI-based control: voltage THD $= 1.82\%$.

6.6.1.2 Nonlinear Load

The proposed MPC strategy is examined with a nonlinear load consisting of a diode-bridge rectifier, an C_L filter, and an R_L load, see Figure 4.6 in chapter 4. The dc- and ac-side results are shown in Figure 6.9. The inductor current and the capacitor voltage effectively track their references (see Figure 6.9(a)) which in turn results in a fixed boosted dc-link voltage. Although the output current is not a sinusoidal waveform, MPC is capable of producing a sinusoidal output voltage with relatively low harmonic content (THD = 2.75%, see Figure 6.9(b)). These results indicate that MPC manages to control the output voltage of the qZSI under both linear

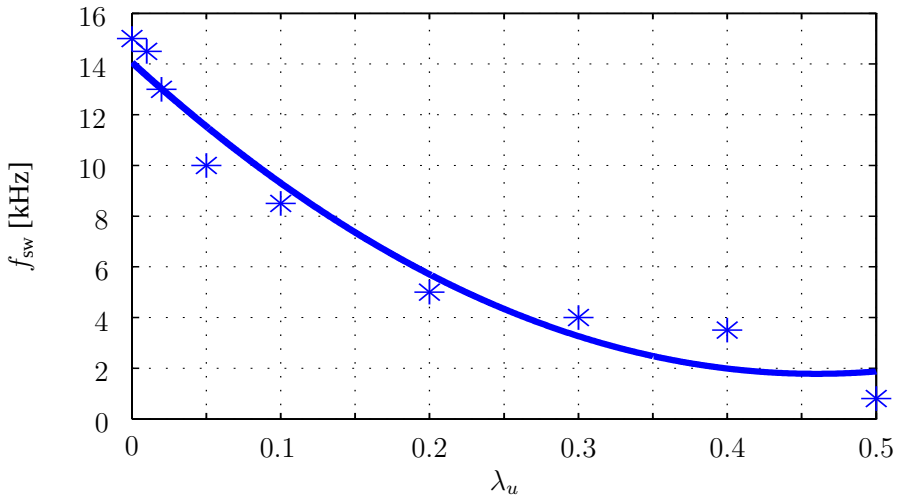


(a) dc side

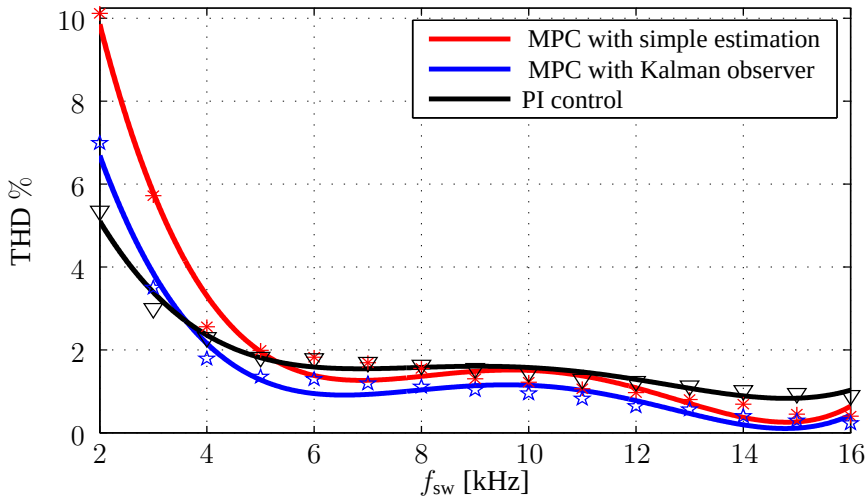


(b) ac side

Figure 6.9: Experimental results of the qZSI with MPC for nonlinear load. $T_s = 20\,\mu$s and $f_{\text{sw}} = 5\,$kHz. The voltage THD = 2.75%.



(a) Switching frequency f_{sw} versus λ_u.



(b) Voltage THD versus the switching frequency f_{sw}.

Figure 6.10: Average switching frequency and output voltage THD analysis.

and nonlinear loads, which makes it an excellent candidate for UPS systems.

It is noteworthy to point out that the linear controller in its current form, as shown in Figure 6.3, does not work properly when a nonlinear load is considered. The main reason is that the harmonics of the output side need to be compensated for in the controller design. In this case, the designed PR controller in chapter 4 could be an interesting alternative.

6.6.1.3 Voltage THD and Switching Frequency

In this section the trade-off between the switching frequency and the resulting output voltage THD is examined. Before doing so, though, the relationship between the weighting factor λ_u in (6.15) and the converter average switching frequency when controlled with MPC is first

examined. The characteristic that indicates how the average switching frequency changes with λ_u is shown in Figure 6.10(a).

Figure 6.10(b) shows the relationship between the switching frequency and the voltage THD produced by (a) the linear controller, (b) MPC with the simple estimation scheme, and (c) MPC with the Kalman observer. As can be seen, the voltage THD can be roughly described by a hyperbolic function of the switching frequency. Although the linear controller produces lower voltage THD at low switching frequencies (2 and 3 kHz) than MPC, the voltage THD produced by the latter approach are lower for a wider range of switching frequencies ($5 - 16$ kHz). It can also be observed that in terms of voltage THD, MPC with the Kalman observer outperforms MPC with the simple estimation scheme over the whole operating range.

6.6.2 Operation During Transients

The transient performance of the proposed MPC strategy and the PI-based controller are tested with a linear RL load. The reference value of the output voltage is kept constant to 100 V, regardless of the load value. In this test, the load is step changed from no load to full load ($20\,\Omega, 2.5$ mH), and vice versa, while keeping the input voltage constant at 150 V.

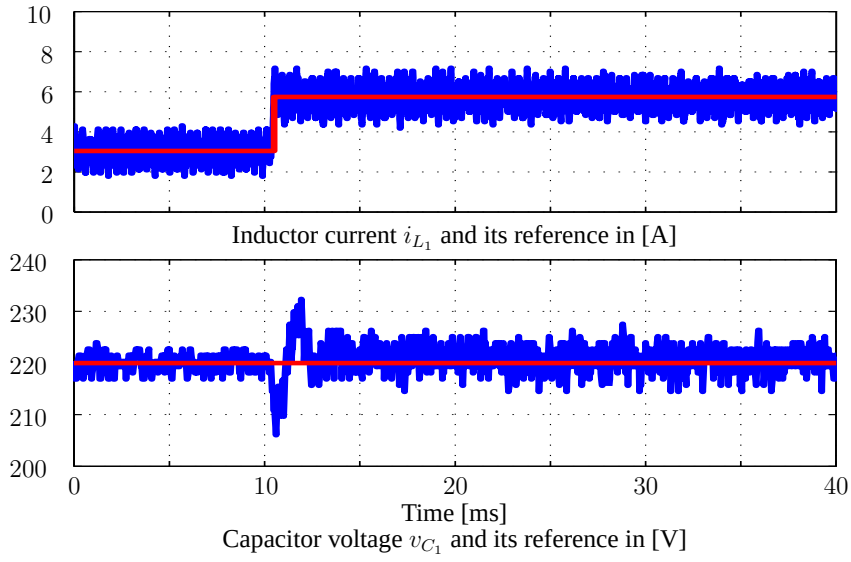
Since the output voltage reference is fixed, the capacitor voltage reference is also kept fixed. However, the inductor current reference is changed according to the required output power. Thus, the controller aims to keep both the output voltage and the capacitor voltage constant as well as to track the inductor current reference.

6.6.2.1 No to Full Load

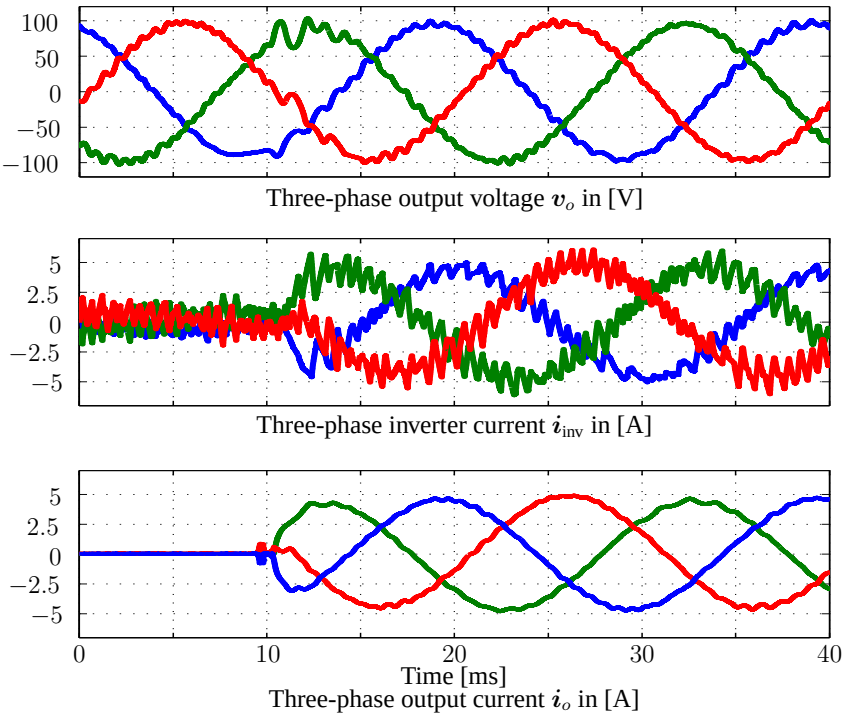
First, a step-up change in the load is considered. At time instant $t \approx 10$ ms the load changes from no load to full load. Figures 6.11 and 6.13 show the experimental results with MPC and the linear PI controller, respectively.

As can be seen in Figure 6.11(a), the inductor current with MPC quickly reaches its new demanded value in 2 ms, with no overshoots. Moreover, the capacitor voltage effectively remains constant at 220 V, with small deviations during the transient. The results with the linear PI controller for the same scenario are shown in Figure 6.13(a). Although the converter settles at the new operating point, the transient lasts significantly longer compared with MPC, i.e. the settling time is about 22.5 ms.

As for the ac side, both MPC and the PI-based controller manage to effectively adjust the output voltage to its reference value after the load step change occurs, see Figures 6.11(b) and 6.13(b), respectively. As can be seen, the proposed control algorithm again exhibits faster dynamic behavior. The presented results indicate the ability of the proposed MPC to effectively control both sides of the qZSI simultaneously and with short transient times.



(a) dc-side

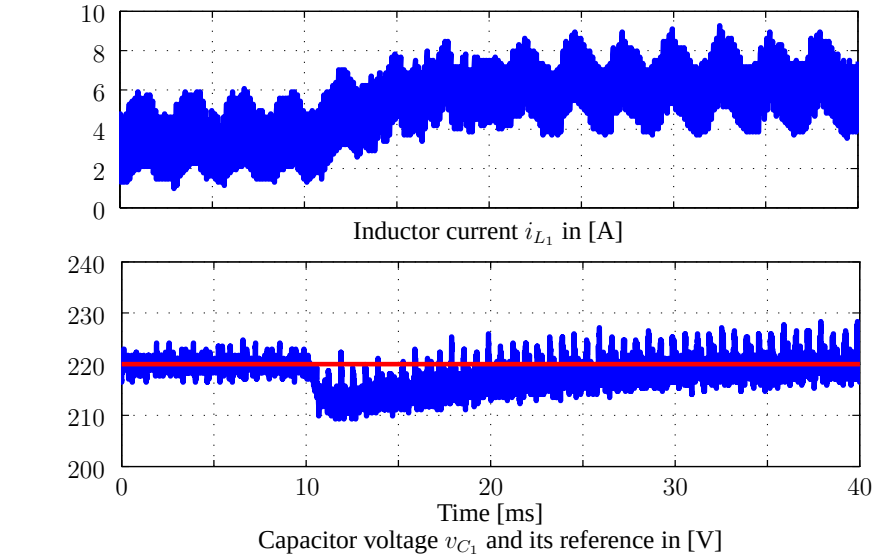


(b) ac-side

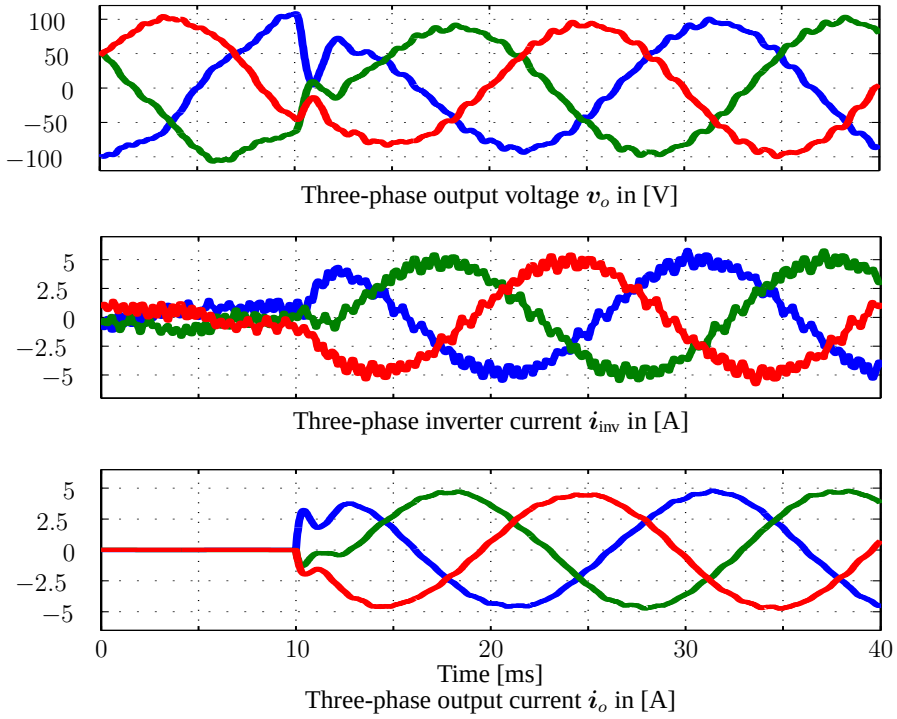
Figure 6.11: Experimental results of the qZSI with the MPC under load step change (no to full load). $T_s = 20\,\mu$s.

6.6.2.2 Full to No Load

Next, the load changes from full load to no load at $t \approx 15$ ms. The results with MPC and the PI controller are shown in Figures 6.13 and 6.14, respectively.



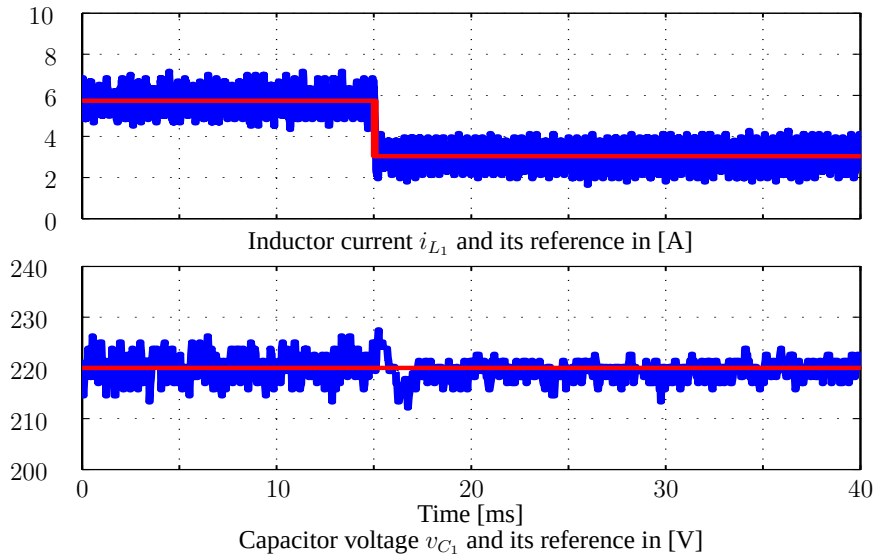
(a) dc-side



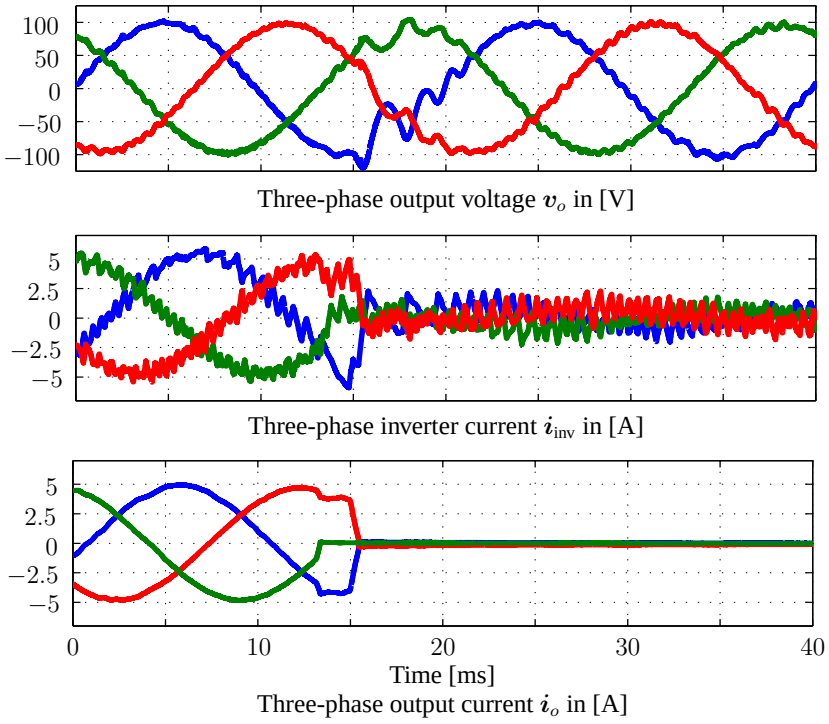
(b) ac-side

Figure 6.12: Experimental results of the qZSI with the PI control under load step change (no to full load).

As can be observed, when MPC is employed, the inductor current instantaneously decreases to reach its new nominal value, see 6.13(a). As for the capacitor voltage, this is not affected by the load change and remains equal to its reference value. On the other hand, when a PI-based controller is considered, the settling time increases as can be observed in 6.14(a). When, the step-down change occurs, it takes about $35\,\text{ms}$ for the inductor current to reach its reference



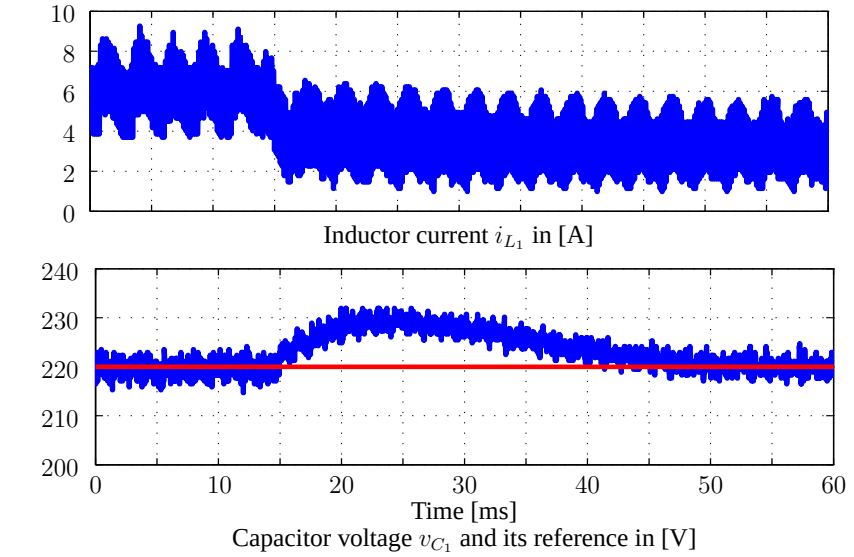
(a) dc-side



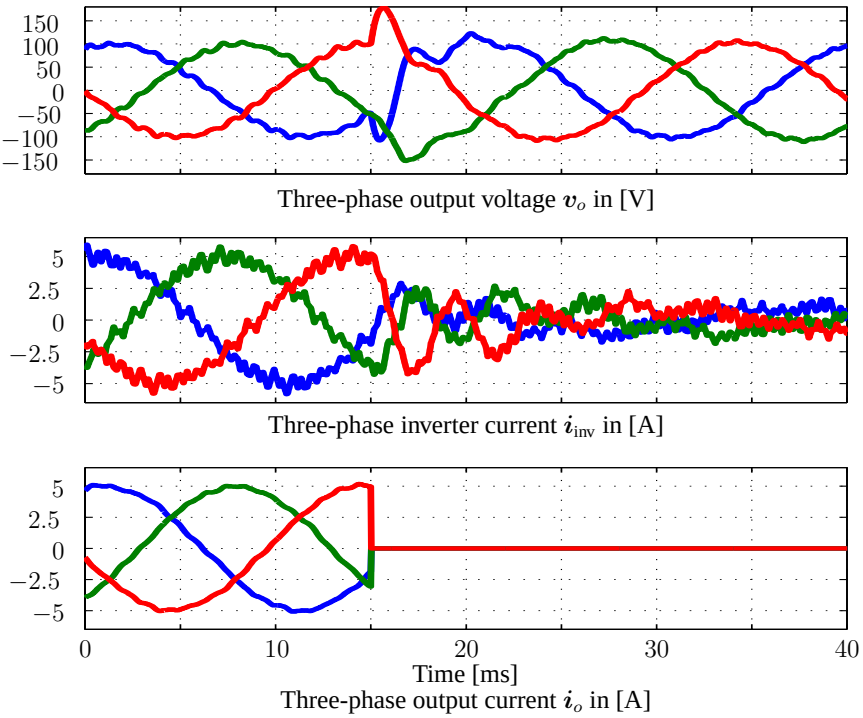
(b) ac-side

Figure 6.13: Experimental results of the qZSI with the MPC under load step change (full to no load). $T_s = 20\,\mu$s.

value. Moreover, an overshoot in the output voltage (> 50 V) is observed (see Figure 6.14(b)) which is not desirable when UPS systems are targeted. Note that—as in the previous case—the PI parameters are tuned such that any stability issues are avoided.



(a) dc-side



(b) ac-side

Figure 6.14: Experimental results of the qZSI with the PI control under load step change (full to no load).

Based on the previous discussions, it can be emphasized that the proposed MPC introduces an attractive control technique for both sides of the qZSI under load change with shorter transient times and less current ripples than the traditional PI-based control.

6.7 Summary

This chapter presents a voltage-mode finite control set model predictive control (FCS-MPC) strategy for UPS applications. The system under consideration consists of a qZSI connected to a linear/nonlinear load via an intermediate LC filter. MPC manages to simultaneously control both sides of the converter by appropriately manipulating its switches. On the dc side, the capacitor voltage and the inductor current of the qZS network are the controlled variables, while the output voltage of the LC filter is regulated on the ac side. To reduce the hardware cost as well as to address load variations an estimation scheme based on a Kalman observer is added which appears to be immune to noise.

Experimental results based on an FPGA are included to demonstrate the potential advantages of the proposed strategy. Based on the presented results, it can be concluded that the proposed MPC method not only exhibits better dynamic behavior than a conventional linear controller with shorter settling times, but also it produces lower voltage THD and thus it shows better performance at steady-state operating conditions.

CHAPTER 7

Variable Switching Point Predictive Current Control

This chapter presents a variable switching point predictive current control (VSP^{2}CC) for the quasi-Z-source inverter. The proposed VSP^{2}CC aims to regulate the current on the ac side as well as the inductor current and capacitor voltage of the quasi-Z-source network. Unlike the previously presented MPC strategies for the qZSI, with the proposed control scheme the optimal switch position can be changed at any time instant within the sampling interval. By doing so, the shoot-through state can be applied for a shorter time than the sampling interval which in turn results in lower output and inductor currents ripples.

7.1 Motivation

Due to its fast dynamic response, implementation simplicity, and ability to handle multiple control objectives, MPC has proved to be an effective control algorithm for the qZSI [71, 105, 112, 115, 118]. In this strategy, based on the control objectives (the regulation of the output current, inductor current, and capacitor voltage to their reference values as well as control of the switching frequency), an optimization problem is formulated and solved to find the optimal control action (switch position). However, the solution to the optimization problem underlying MPC is applied for at least one sampling interval. This implies that the shoot-though state can be applied for more than one sampling interval. Consequently, when the converter operates at low switching frequency, the shoot-through state is applied for a long time. This leads to high inductor current ripples and output current THD.

Recently, some techniques have been proposed that include a “modulator” to the MPC scheme, with a goal to reduce the ripples of the variables of interest (e.g. current, torque, flux, etc.) [119–124]. This is done by formulating an optimization problem, the solution to which is the time instant within the sampling interval where the switches of the converter should change

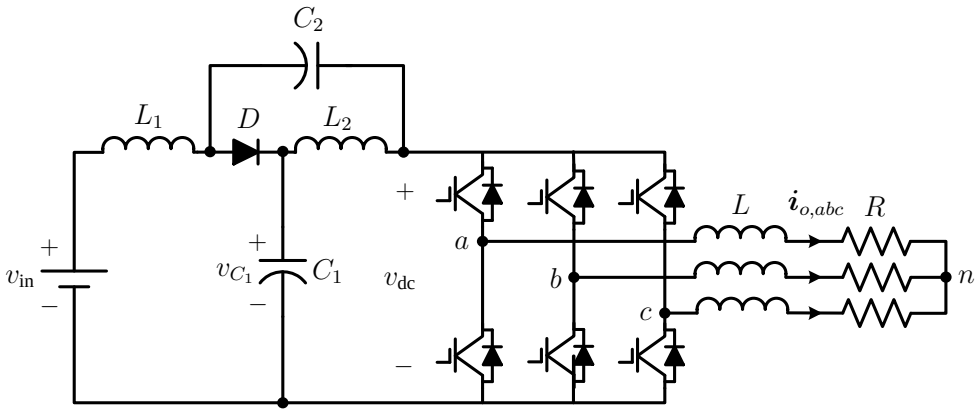


Figure 7.1: Topology of the quasi-Z-source inverter (qZSI).

state in order for the ripples of concern to be minimized. As a result, the switch positions that could lead to high ripples are applied for less time than with conventional MPC, resulting in an overall improved system performance.

Motivated by the advantages of the aforementioned approaches, this paper proposes a variable switching point predictive current control (VSP^{2}CC) for the qZSI. In addition to the above-mentioned control objectives, the proposed scheme aims to reduce the output and inductor currents ripples by changing the switch position at any point within the sampling interval, thus, reducing the time the shoot-through state is applied. The performance of the proposed scheme is experimentally investigated based on an FPGA. The proposed method results in lower inductor current ripples and output current THD compared to the conventional MPC when operating the converter at the same switching frequency.

The chapter is structured as follows. Section 7.2 introduces the system description. The proposed VSP^{2}CC strategy is presented in Section 7.3. In Section 7.4, experimental results are provided and discussed. Finally, the chapter is summarized in Section 7.5.

7.2 System Description

The system under discussion, consisting of a quasi-Z-source (qZS) network, two-level three-phase inverter, and an RL load, is shown in Figure 7.1. Depending on the switching state, the qZSI operates in two different switching modes; shoot-through and non-shoot-through state (active or zero state). The full model of the system configuration is introduced before in chapter 5. To compute the predictions of the variables of interest, the discrete-time model of the qZSI, derived in Chapter 5, is utilized.

The resulting discrete-time state-space model of the system under discussion is given by

$$\boldsymbol{x}(k+1) = \boldsymbol{A}\boldsymbol{x}(k) + \boldsymbol{B}\boldsymbol{u}_{abc}(k) + \boldsymbol{D}\boldsymbol{w}(k) \tag{7.1a}$$

$$\boldsymbol{y}(k) = \boldsymbol{C}\boldsymbol{x}(k)\,, \tag{7.1b}$$

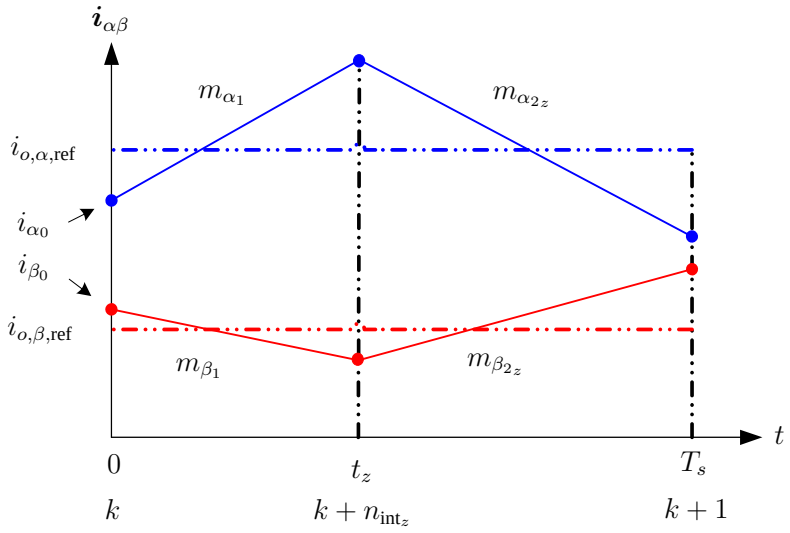


Figure 7.2: Variable switching point concept.

with $\boldsymbol{A} = (\boldsymbol{F} + \boldsymbol{I})T_s$, $\boldsymbol{B} = \boldsymbol{G}T_s$, $\boldsymbol{D} = \boldsymbol{H}T_s$ and $\boldsymbol{C} = \boldsymbol{E}$. Moreover, $\boldsymbol{I}$ denotes the identity matrix, T_s is the sampling interval, and $k \in \mathbb{N}$. This model is utilized to predict the future behavior of the qZSI.

7.3 Variable Switching Point Predictive Current Control

7.3.1 Control Objective

The main objective of the proposed VSP^{2}CC strategy is to regulate the output current, inductor current, and capacitor voltage along their reference values. In addition, the switching frequency is to be kept relatively low in order to reduce the switching losses. Moreover, the output current ripples are to be minimized. To achieve these goals, the control algorithm calculates the variable switching point (VSP) at which the optimal switch position should be applied. The VSP is calculated such that the squared rms current error of the output current is minimized.

7.3.2 Proposed Control Algorithm

As mentioned, the VSP t_z, i.e. $t_z \in [0, T_s)$ is calculated based on the minimization of the squared rms error of the output current, where $t_z = n_{\text{int}_z}^{(k)} T_s$, with $n_{\text{int}_z}^{(k)} \in [0, 1)$ being the normalized time instant between the time-steps k and $k + 1$. Figure 7.2 shows the main concept of VSP where the slopes of both α and β currents are assumed to be constant over one sampling interval. Accordingly, the squared rms current error (e_{rms^2}) is given by

$$e_{rms^2} = \frac{1}{T_s}\Bigg(\int_0^{t_z} \left(\boldsymbol{i}_{\alpha\beta,\text{ref}} - \boldsymbol{i}_{\alpha\beta}(t, \boldsymbol{u}_{abc}(k))\right)^2 \mathrm{d}t + \int_{t_z}^{T_s} \left(\boldsymbol{i}_{\alpha\beta,\text{ref}} - \boldsymbol{i}_{\alpha\beta}(t, \boldsymbol{u}_{abc}(k + n_{\text{int}_z}^{(k)}))\right)^2 \mathrm{d}t \Bigg), \quad (7.2)$$

where $\boldsymbol{i}_{\alpha\beta,\text{ref}}$ is the $\alpha\beta$ current reference. Moreover, $\boldsymbol{i}_{\alpha\beta}(t, \boldsymbol{u}_{abc}(k))$ and $\boldsymbol{i}_{\alpha\beta}(t, \boldsymbol{u}_{abc}(k+n_{\text{int}_z}^{(k)}))$ are the output currents resulting from the applied switch position and candidate switch positions, respectively, with $z \in \{1, 2, \cdots, 8\}$ denoting the corresponding switch position. Note that Figure 7.2 shows the current slopes resulting from the applied switch position (i.e. m_{α_1}, m_{β_1}) and only one of the candidate switch positions (i.e. $m_{\alpha_{2_z}}$, $m_{\beta_{2_z}}$).

In order to minimize (7.2), its derivative is set equal to zero. This yields

$$t_z = \frac{(2\,\boldsymbol{i}_{\alpha\beta_0} - 2\,\boldsymbol{i}_{\alpha\beta,\text{ref}} + T_s\,\boldsymbol{m}_{\alpha\beta_{2_z}})(\boldsymbol{m}_{\alpha\beta_{2_z}} - \boldsymbol{m}_{\alpha\beta_1})}{(2\,\boldsymbol{m}_{\alpha\beta_1} - \boldsymbol{m}_{\alpha\beta_{2_z}})(\boldsymbol{m}_{\alpha\beta_1} - \boldsymbol{m}_{\alpha\beta_{2_z}})} \tag{7.3}$$

where $\boldsymbol{i}_{\alpha\beta_0}$ denotes the measured $\alpha\beta$ currents at time-step k (see Figure 7.2). In addition, $\boldsymbol{m}_{\alpha\beta_1} = [m_{\alpha_1}\ m_{\beta_1}]^T$ and $\boldsymbol{m}_{\alpha\beta_{2_z}} = [m_{\alpha_{2_z}}\ m_{\beta_{2_z}}]^T$ are the slopes of the currents $\boldsymbol{i}_{\alpha\beta}(t, \boldsymbol{u}_{abc}(k))$ and $\boldsymbol{i}_{\alpha\beta}(t, \boldsymbol{u}_{abc}(k + n_{\text{int}_z}^{(k)}))$, respectively.

The following algorithm, executed at time-step k, is used to calculate the VSP with the corresponding optimal switch position.

Step 1: First, it is assumed that the switch position $\boldsymbol{u}_{abc}(k-1+n_{\text{int}}^{(k-1)})$ applied at time instant $(k-1+n_{\text{int}}^{(k-1)})T_s$ is also applied at time-step k. Then, by using the system model (7.1) and the measured output current, the predicted output current at step $k+1$ ($\boldsymbol{i}_{\alpha\beta}(k+1)$) is computed. Hence, the first current slopes can be given by

$$\boldsymbol{m}_{\alpha\beta_1} = \frac{\boldsymbol{i}_{\alpha\beta}(k+1) - \boldsymbol{i}_{\alpha\beta}(k)}{T_s}\,. \tag{7.4}$$

Step 2: Then, the predicted output current is recomputed assuming that the switch position at time-step k, i.e. $\boldsymbol{u}_{abc}(k)$, can be anyone of the eight possibilities (six active states, one zero state, and one shoot-through state). Then, the possible current slopes are calculated as

$$\boldsymbol{m}_{\alpha\beta_{2_z}} = \frac{\boldsymbol{i}_{\alpha\beta_z}(k+1) - \boldsymbol{i}_{\alpha\beta}(k)}{T_s}\,. \tag{7.5}$$

Using the current slopes in (7.4) and (7.5), the VSP (7.3) can be calculated.

Step 3: Based on the computed VSP, the predictions of the state and output variables are computed at two different time instances. The first predictions are computed at $k + n_{\text{int}_z}^{(k)}$, where t_z is used instead of T_s in (7.1). For the second set of predictions at $k+1$, the time interval $(T_s - t_z)$ is used.

Step 4: Next, a cost function is formulated as follows

$$J(k) = \sum_{\xi\in\mathcal{S}} \left(||\boldsymbol{y}_{\text{ref}} - \boldsymbol{y}(k+\xi|k)||^2_{\boldsymbol{Q}} \right) + \lambda_u ||\Delta\boldsymbol{u}_{abc}(k|k)||_2^2\,, \tag{7.6}$$

with $\mathcal{S} = \{n_{\text{int}},\ 1\}$ and $\boldsymbol{y}_{\text{ref}} = [i_{o,\alpha,\text{ref}}\ i_{o,\beta,\text{ref}}\ i_{L_1,\text{ref}}\ v_{C_1,\text{ref}}]^T$. The second term is added to adjust the switching frequency of the converter, where $\Delta\boldsymbol{u}_{abc}(k) = \boldsymbol{u}_{abc}(k) - \boldsymbol{u}_{abc}(k-1)$. Moreover, the weighting factor λ_u and the diagonal positive semidefinite weighting matrix $\boldsymbol{Q} \in \mathbb{R}^{4\times4}$

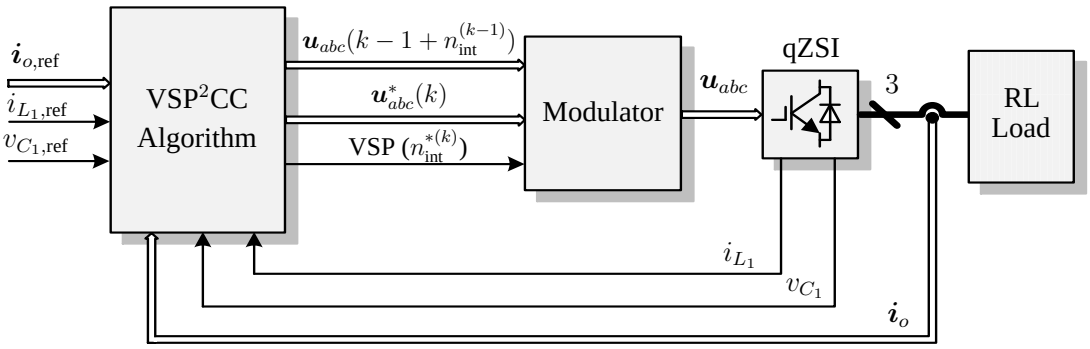


Figure 7.3: Variable switching point predictive current control for the qZSI.

are added to set the trade-off between the tracking performance and the converter switching frequency.

Then, in order to find the optimal switch position and the corresponding VSP, the following optimization problem is solved in real time

$$\begin{aligned} \underset{\boldsymbol{u}_{abc}}{\text{minimize}} \quad & J(k) \\ \text{subject to} \quad & \text{eq. (7.1)}\,. \end{aligned} \tag{7.7}$$

This yields the pair $\boldsymbol{U}^*(k) = \left\{\boldsymbol{u}^*_{abc}(k+n_{\text{int}}),\, n_{\text{int}}^{*(k)}\right\}$.

Finally, a modulator is used to apply the final switching signals to the converter. The modulator is working on a higher sampling frequency than the one of the MPC algorithm itself. The modulator first outputs the previously applied switch position $\boldsymbol{u}_{abc}(k-1+n_{\text{int}}^{(k-1)})$ until time instant t_z. Subsequently, it applies the new optimal switch postion $\boldsymbol{u}^*_{abc}(kn_{\text{int}})$ until the end of the sampling interval. At the next time-step $k+1$, the control procedure is repeated with new measurements. The block diagram of VSP^{2}CC for the qZSI is shown in Figure 7.3.

7.4 Experimental Results

To examine the performance of the proposed VSP^{2}CC strategy for the qZSI configuration, shown in Figure 7.1, experiments were conducted in the laboratory. For the sake of comparison, the conventional MPC is also investigated [105]. Both control algorithms are implemented on an FPGA Cyclone III-EP3C40Q240C8. For more details about the test bench, please refer to appendix C.

To compensate for the time delay introduced by the proposed and conventional algorithm, a delay compensation strategy is applied [114]. Concerning the computational demand, VSP^{2}CC needs higher calculation time than the conventional MPC. For instance, the conventional MPC algorithms is executed in 3μs, while the proposed VSP^{2}CC requires 5μs. By using an FPGA, both algorithms can be efficiently implemented.

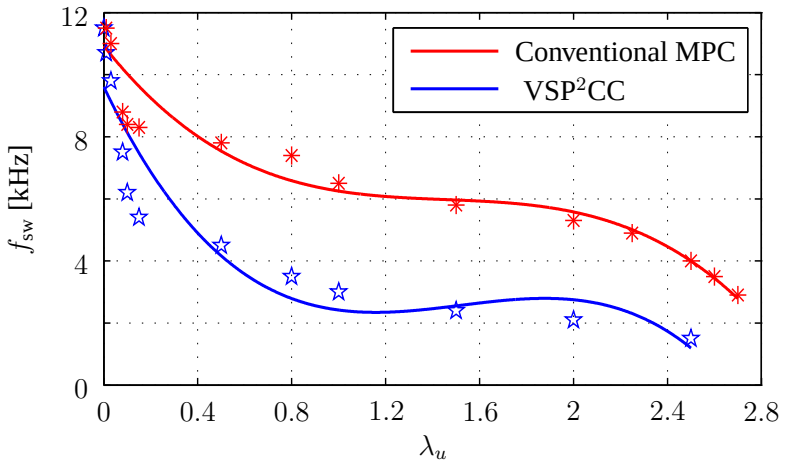


Figure 7.4: The effect of the weighting factor (λ_u) on the switching frequency for both conventional MPC and VSP^{2}CC.

The system parameters are $v_{\text{in}} = 70\,\text{V}$, $L_1 = L_2 = 1\,\text{mH}$, $C_1 = C_2 = 480\,\mu\text{F}$, $R = 10\,\Omega$, and $L = 10\,\text{mH}$. According to the desired output power ($P_{o,\text{ref}} = 315\,\text{W}$), the output current reference $\boldsymbol{i}_{o,\text{ref}}$ is set to $4\,\text{A}$, while the inductor current reference is equal to $4.5\,\text{A}$ ($i_{L_1,\text{ref}} = P_{o,\text{ref}}/v_{\text{in}}$). In order to keep the peak dc-link voltage $\hat{v}_{\text{dc}}$ at $180\,\text{V}$, the capacitor voltage reference $v_{C_1,\text{ref}}$ is set to $120\,\text{V}$, see the steady-state analysis in Section 5.2.4. The sampling interval used for the VSP^{2}CC algorithm is $T_s = 25\,\mu\text{s}$, while it is $T_{s_m} = 0.25\,\mu\text{s}$ for the modulator block.

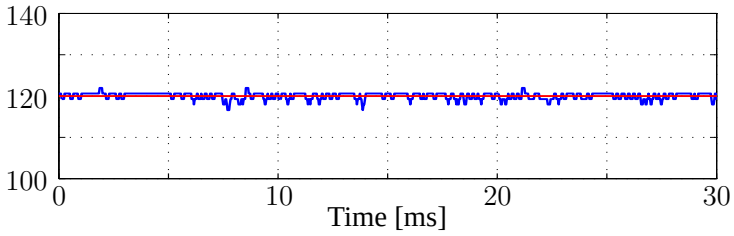
Furthermore, the converter operates at the desired switching frequency f_{sw}, by adjusting $\boldsymbol{Q}$ and λ_u in (7.6). Figure 7.4 shows how the weighting factor λ_u affects the operating switching frequency of the converter with both the conventional MPC and proposed VSP^{2}CC schemes.

7.4.1 Steady-State Operation

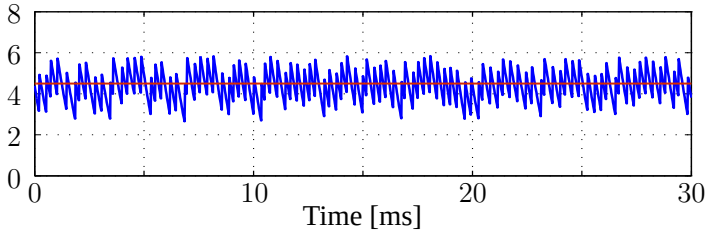
The steady-state response of the qZSI is examined with the proposed VSP^{2}CC and the conventional MPC. The operating average switching frequency is adjusted to $f_{\text{sw}} \approx 3.4\,\text{kHz}$ for both controllers by setting λ_u in (7.6) as 0.75 and 2.6 with VSP^{2}CC and conventional MPC, respectively.

The experimental results for VSP^{2}CC and conventional MPC are shown in Figures 7.5 and 7.6, respectively. As can be seen, the dc-side variables effectively track their reference values in both examined cases. The capacitor voltages (Figures 7.5(a) and 7.6(a)) and the inductor currents (Figures 7.5(b) and 7.6(b)) are regulated along their reference values resulting in the desired peak dc-link voltage of $180\,\text{V}$ (Figures 7.5(c) and 7.6(c)). Although both controllers introduce zero steady-state error for both dc quantities, VSP^{2}CC produces inductor current of about $50\,\%$ less ripple than the conventional MPC.

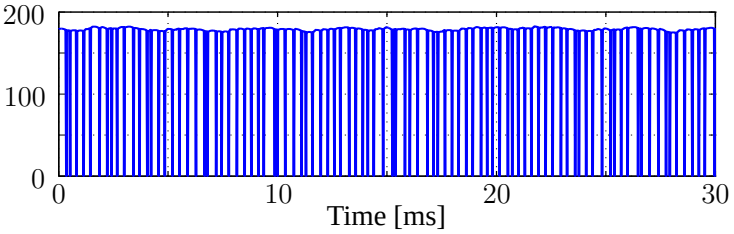
As for the ac side, Figures 7.5(d) and 7.6(d) show that the output current accurately tracks its reference with both VSP^{2}CC and conventional MPC. However, VSP^{2}CC produces output current THD of 4.21%, notably lower than the THD with the conventional MPC (12.49%), see Figures 7.5(e) and 7.6(e).



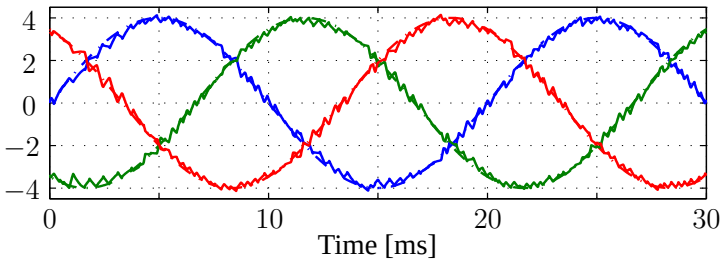
(a) Capacitor voltage v_{C_1} and its reference in [V].



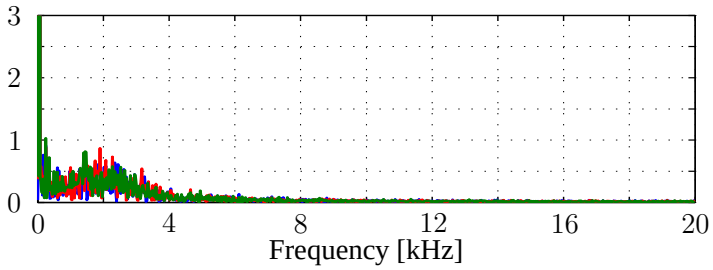
(b) Inductor current i_{L_1} and its reference in [A].



(c) Dc-link voltage v_{dc} in [V].

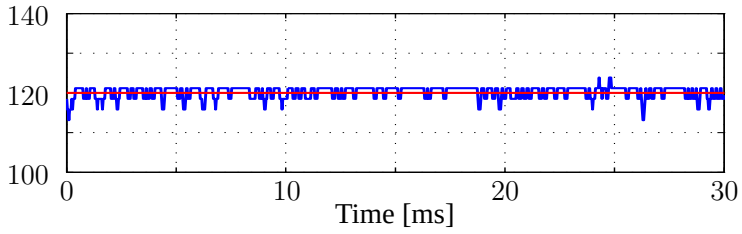


(d) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A].

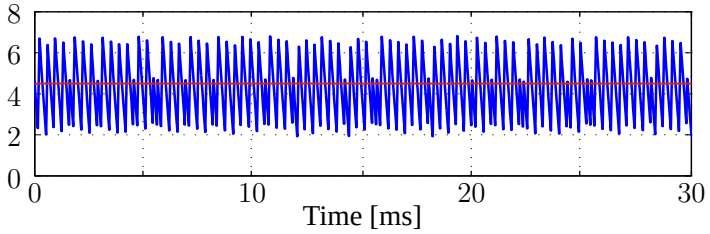


(e) Output current spectrum (%), THD $= 4.21\,\%$.

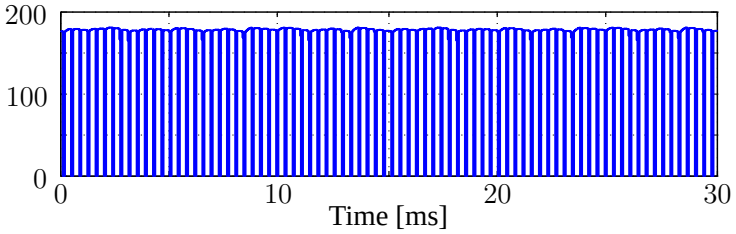
Figure 7.5: Experimental results of the dc and ac side of the qZSI with the VSP^{2}CC. The sampling interval is $T_s = 25\,\mu$s and the switching frequency is $f_{\text{sw}} \approx 3.4\,$kHz.



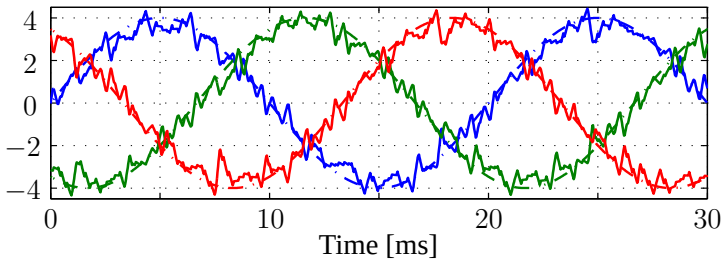
(a) Capacitor voltage v_{C_1} and its reference in [V].



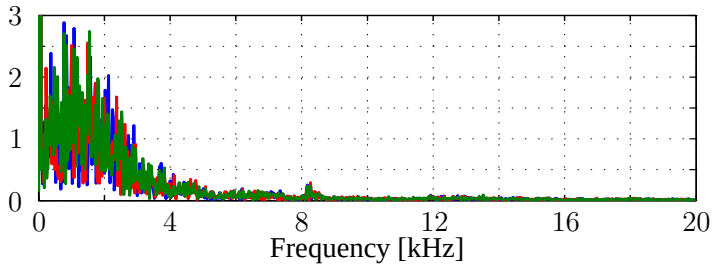
(b) Inductor current i_{L_1} and its reference in [A].



(c) Dc-link voltage v_{dc} in [V].



(d) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A].



(e) Output current spectrum (%), THD $= 12.49\,\%$.

Figure 7.6: Experimental results of the dc and ac side of the qZSI with the conventional MPC. The sampling interval is $T_s = 25\,\mu$s and the switching frequency is $f_{\text{sw}} \approx 3.4\,$kHz.

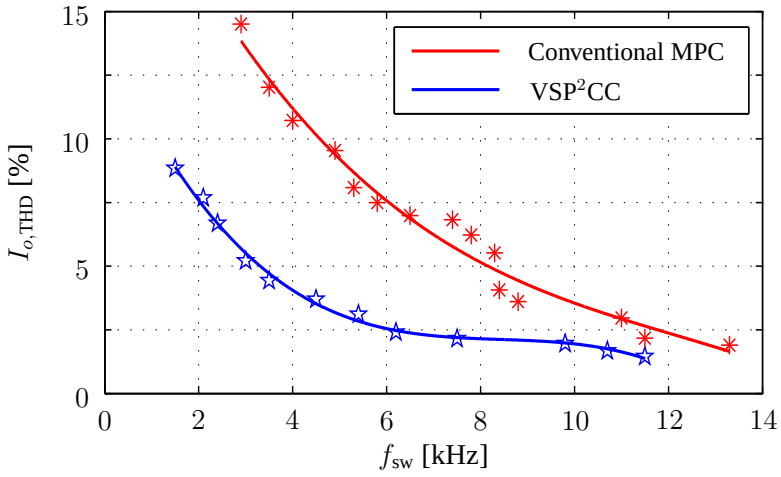


Figure 7.7: Trade-off between the current THD $I_{o,\mathrm{THD}}$ and the switching frequency f_{sw} for the VSP^{2}CC and conventional MPC.

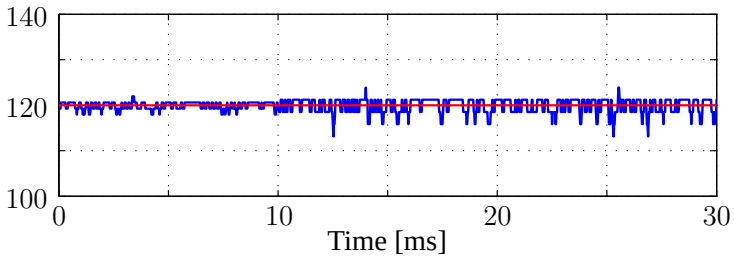
Furthermore, the trade-off between the output current THD and the switching frequency of the proposed VSP^{2}CC and the conventional MPC is investigated. In this experiment, λ_u is appropriately tuned to obtain a wide range of switching frequencies. The results are approximated by a third degree polynomial and shown in Figure 7.7. As can be observed, the VSP^{2}CC introduces lower THD values than the conventional MPC over the whole range of the switching frequencies.

7.4.2 Transient Response

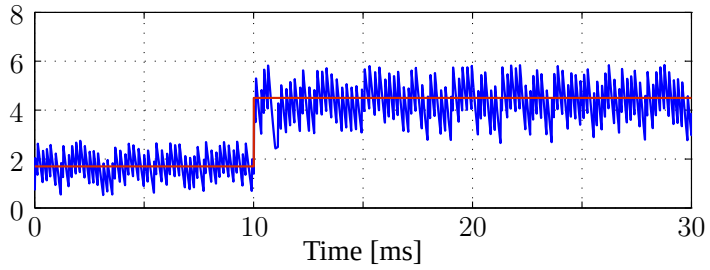
The transient behavior of the proposed VSP^{2}CC and conventional MPC are scrutinized under a step change in the output current reference. The output current is stepped up from $2\,\mathrm{A}$ to $4\,\mathrm{A}$. Consequently, the inductor current reference is changed from $1.7\,\mathrm{A}$ to $4.5\,\mathrm{A}$, while the capacitor voltage reference is kept fixed at $120\,\mathrm{V}$.

The dc- and ac-side results are shown in Figures 7.8 and 7.9 for VSP^{2}CC and conventional MPC, respectively. With both control schemes, the capacitor voltages are well regulated along their reference values, see Figures 7.8(a) and 7.9(a). Additionally, as can be seen in Figures 7.8(b) and 7.9(b), the inductor currents track their references both before and after the step change. Although both control schemes introduce very fast transient response, VSP^{2}CC shows lower current ripples at both operating points.

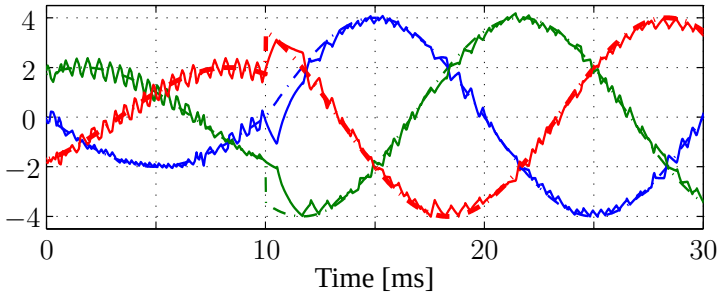
As for the ac side, the proposed VSP^{2}CC and conventional MPC achieve zero steady-state error (Figures 7.8(c) and 7.9(c)) with very short transient time. It is also clear that VSP^{2}CC delivers lower output current distortion. This verifies the theory that if the shoot-through state is applied for less time than the sampling interval, the inductor and output current ripples (as quantified by the output current THD) can be significantly reduced. As a result, the performance of the converter can be considerably improved.



(a) Capacitor voltage v_{C_1} and its reference in [V].



(b) Inductor current i_{L_1} and its reference in [A].



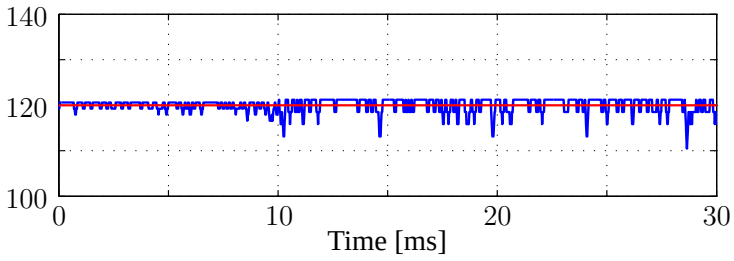
(c) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A].

Figure 7.8: Experimental results of the dc and ac side of the qZSI with VSP^{2}CC under a step-up change in the output current reference.

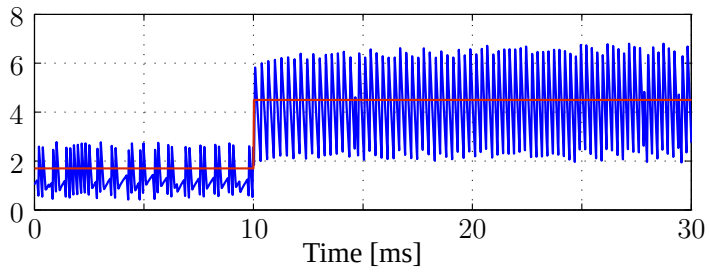
7.5 Summary

This chapter presents a variable switching point predictive current control (VSP^{2}CC) for the quasi-Z-source inverter. The proposed algorithm controls both sides of the converter, i.e. the output current on the ac side as well as the inductor current and capacitor voltage on the dc side. In order to improve the system behavior, VSP^{2}CC changes the (optimal) state of the switches at that time instant that results in minimal inductor and output current ripples. By doing so, the switch position that results in high current ripples (i.e. the shoot-through state) is applied for a shorter time.

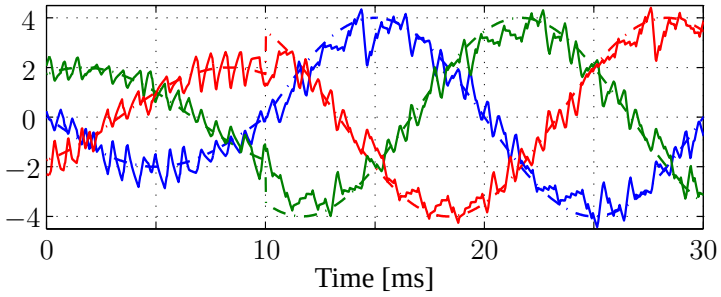
The performance of the proposed method and conventional MPC are experimentally investigated based on an FPGA. Although the proposed algorithm requires higher calculation time than the conventional MPC, by using high performance and high optimized FPGA the imple-



(a) Capacitor voltage v_{C_1} and its reference in [V].



(b) Inductor current i_{L_1} and its reference in [A].



(c) Three-phase output current $\boldsymbol{i}_o$ (solid lines) and their references (dash-dotted lines) in [A].

Figure 7.9: Experimental results of the dc and ac side of the qZSI with conventional MPC under a step-up change in the output current reference.

mentation of the proposed algorithm is possible. It is shown that the proposed strategy results in lower inductor current ripples and less output current THD compared with the conventional scheme when the converter operates at the same switching frequency.

CHAPTER 8

Conclusion and Future Outlook

This dissertation has examined some advanced control techniques including direct MPC in order to improve the overall performance and efficiency of the impedance source inverters used with distributed generation applications. The quasi-Z-source inverter has been utilized in this dissertation as an attractive example of the impedance source inverters. Nevertheless, the proposed control techniques can be applied on any other topologies of the impedance source inverters. All the presented control algorithms have been experimentally validated by a low-cost and low-power FPGA.

8.1 Conclusion

The work done in this dissertation can be briefly summarized in the following points.

- Chapter 3 has conducted a thorough comparison between the quasi-Z-source inverter and the conventional two-stage inverter is conducted in light of the voltage stress on the inverter switches, required active and passive components, steady-state and transient performances, and efficiency.

  As it has been shown, the qZSI features lower voltage stress on the switches than the traditional inverter when the voltage gain is in the range of (1-2). In addition, the experimental results demonstrate that the qZSI exhibits lower output voltage THD and higher efficiency than the traditional two-stage inverter.

- In chapter 4, a proportional-resonant controller has been designed for the quasi-Z-source inverter in the stationary reference $\alpha\beta$ frame as an alternative to the conventional PI control. The main goal has been to improve the quality of the output voltage when the quasi-Z-source inverter is connected with nonlinear loads via an intermediate LC filter as a UPS system. This has been achieved by compensating for selected low-order harmon-

ics (5^{th}, 7^{th}, and 9^{th} harmonics). Thus, a regulated sinusoidal output voltage has been obtained not only for linear loads, but also for non-linear loads.

The performance of the proportional-resonant controller with the quasi-Z-source inverter has been experimentally examined. The experimental results have shown the effectiveness of the proposed controller both in steady-state and transient operations with both linear and non-linear loads.

- Chapter 5 has proposed a direct MPC—as a current controller—for the quasi-Z-source inverter connected with an RL load. The proposed MPC strategy simultaneously controls both sides of the qZSI, namely ac output current on the ac side as well as the capacitor voltage and inductor current of the dc side. To improve the closed-loop performance of the converter a long prediction horizon has been implemented. However, the underlying optimization problem may become computationally intractable because of the substantial increase in the computational power demands, which in turn would prevent the implementation of the control strategy in real time. To overcome this and to solve the problem in a computationally efficient manner, a branch-and-bound strategy has been used along with a move blocking scheme. These techniques have facilitated the implementation of a long-horizon MPC in an FPGA.

  The simulation and the experimental results have verified the superior performance of long-prediction horizon MPC when compared to the existing one-step horizon MPC as well as to the established linear PI-based controller. More specifically, the proposed long-horizon direct MPC has exhibited better steady-state behavior with lower output current THD, while, at the same time, it has shown a much faster dynamic response on both sides of the quasi-Z-source inverter.

- In the 6^{th} chapter, a direct MPC—as a voltage controller–has been implemented with the quasi-Z-source inverter connected with linear or nonlinear loads via an intermediate LC filter. The proposed MPC strategy simultaneously controls both sides of the converter by controlling the output voltage of the LC filter as well as the capacitor voltage and inductor current on the dc side. To address time-varying and unknown loads as well as to reduce the number of measurement sensors required, a Kalman observer has been added to estimate the load current which appears to be immune to noise.

  Based on the presented experimental results, it has been concluded that the proposed direct MPC method not only exhibits better dynamic behavior than a conventional linear controller with shorter settling times, but also produces lower voltage THD. Thus, it shows better performance at steady-state operating conditions.

- Finally, chapter 7 has presented a variable switching point predictive current control (VSP^{2}CC) for the quasi-Z-source inverter. The proposed VSP^{2}CC aims to regulate the current on the ac side as well as the inductor current and capacitor voltage of the quasi-Z-source network. With the proposed scheme, the chosen (optimal) switch position can be applied at any time instant within the sampling interval. By doing so, the shoot-through switching states can be applied for a shorter time period than the sampling interval. This results in lower output and inductor currents ripples.

The performance of the proposed method and conventional direct MPC have been experimentally investigated based on an FPGA. As it has been shown, the proposed strategy results in lower inductor current ripples and less output current THD in comparison with the conventional direct MPC.

In sum, as has been proved by the experimental results, this dissertation has fulfilled the goals that have been stated in the introduction by providing robust control algorithms that result in an overall improvement in the converter performance. Thus, the efficiency of the power electronic converters utilized for distributed generation application can be increased without increasing the cost of the hardware. In the end, this results in reliable, robust, and secure distributed generation systems.

8.2 Future Outlook

Finally, I would like to recommend some suggestions for future endeavors in the following points.

- In the present work, the proposed control techniques have been applied with two-level qZSI. However, it can be also applied on other topologies of the ISI without major modifications in the controller software.
- Motivated by the advantages of multi-level inverters, the utilized two-level qZSI can be extended to a three-level structure that can be effectively controlled by MPC algorithms.
- In this dissertation, a branch-and-bound technique and a move blocking strategy are used to reduce the computational demand of the proposed long-horizon MPC in order to be implemented in real time. Accordingly, MPC with 5-step prediction horizon could be implemented, which results in a remarkable improvement in the system performance. In order to implement MPC with longer prediction horizon, other optimization techniques have to be scrutinized to reduce the number of computations required.

Part IV

Appendices

APPENDIX A

List of publications

A.1 Journal papers

- **A. Ayad**, P. Karamanakos, and R. Kennel, "Direct model predictive current control strategy of quasi-Z-source inverters," *IEEE Transaction on Power Electronics*, vol. 32, no. 7, pp. 5786-5801, July 2017.

- **A. Ayad** and R. Kennel, "A comparison of quasi-Z-source inverters and conventional two-stage inverters for PV applications," *EPE Journal*, vol. 27, no. 2, pp. 43-59, May 2017.

- **A. Ayad**, P. Karamanakos, R. Kennel, and J. Rodriguez, "Finite control set model predictive voltage control of quasi-Z-source inverters for UPS applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2017. (under review).

- **A. Ayad** and R. Kennel, "FPGA-based proportional-resonant controller of quasi-Z-source inverters for UPS applications," *IEEE Transaction on Industrial Informatics*, 2016. (under review).

- P. Karamanakos, **A. Ayad**, and R. Kennel, "A Variable Switching Point Predictive Current Control Strategy for Quasi-Z-Source Inverters," *IEEE Transaction on Industry Applications*, 2017. (under review).

- **A. Ayad**, J. Rodriguez, Margarita Norambuena, and R. Kennel, "Computationally-Efficient Direct Model Predictive Current Control of Voltage Source Inverters,", 2017. In preparation for *IEEE Transaction on Industrial Electronics*.

A.2 Conference papers

- **A. Ayad**, P. Karamanakos, and R. Kennel, "Variable switching point predictive current control of quasi-Z-source inverters," *IEEE Applied Power Electronics Conf. and Exp. (APEC)*, Tampa, FL, USA, Mar. 2017, pp. $1-8$.

- **A. Ayad**, P. Karamanakos, R. Kennel, and J. Rodriguez, "Direct model predictive control of bidirectional quasi-Z-source inverters fed permanent magnet synchronous machines," *IEEE CPE-POWERENG*, Cadiz, Spain, Apr. 2017, pp. $1-6$.

- **A. Ayad**,S. Hanafiah, A. Hehn, and R. Kennel, "A hybrid MPPT for quasi-Z-source inverter in PV applications under partial shading condition," *IEEE CPE-POWERENG*, Cadiz, Spain, Apr. 2017, pp. $1-6$.

- **A. Ayad**, P. Karamanakos, and R. Kennel, "Direct model predictive control with an extended prediction horizon for quasi-Z-source inverters," *IEEE Ind. Electron. Society (IECON)*, Florence, Italy, Oct. 2016, pp. $1-6$.

- **A. Ayad**, M. Hashem, C. Hackl, and R. Kennel, "Proportional-resonant controller design of quasi-Z-source inverters with LC filters," *IEEE Ind. Electron. Society (IECON)*, Florence, Italy, Oct. 2016, pp. $1-6$.

- **A. Ayad**, P. Karamanakos, and R. Kennel, "Direct model predictive voltage control of quasi-Z-source inverters with LC filters," *Eur. Power Electron. Conf. (EPE)*, Karlsruhe, Germany, Sep. 2016, pp. $1-10$.

- **A. Ayad**, P. Karamanakos, and R. Kennel, "Direct model predictive current control of quasi-Z-source inverters," *IEEE Int. Symp. Pred. Control of Elect. Drives and Power Electron. (PRECEDE)*, Valparaiso, Chile, Oct. 2015, pp. $1-6$.

- **A. Ayad** and R. Kennel, "Direct model predictive control of quasi-Z-source inverter compared with the traditional PI-based PWM control," *Eur. Power Electron. Conf. (EPE)*, Geneva, Switzerland, Sep. 2015, pp. $1-10$.

- **A. Ayad**, S. Hanafiah, and R. Kennel, "A comparison of quasi-Z-source inverter and traditional two-stage inverter for photovoltaic application," *Int. Expo. and Conf. Power Electron., Intelligent Motion, Renew. Energy Management (PCIM)*, Nuremberg , Germany, May 2015, pp. $1-8$.

- **A. Ayad** and R. Kennel, "Model predictive controller for grid-connected photovoltaic based on quasi-Z-source inverter," *IEEE Int. Symp. Pred. Control of Elect. Drives and Power Electron. (PRECEDE)*, Munich, Germany, Oct. 2013, pp. $1-6$.

- **A. Ayad**, M. Ismeil, R. Kennel, and M. Orabi, "Experimental studies on a single-phase improved switched inductor Z-source inverter," *Eur. Power Electron. Conf. (EPE)*, Lille, France, Sep. 2013, pp. $1-10$.

- **A. Ayad**, J. Saha, and R Kennel, "Direct Model Predictive Current Control For Matrix Converters," *IEEE 2nd Biennial Int. Conf. on Nascent Technologies in Engineering (ICNTE)*, Vashi, Navi Mumbai, India, Jan. 2017, pp. 1-6.

A.3 Awards

- **Best Session Presentation** in 42^{nd} Annual Conference of the IEEE Industrial Society Conference (IEEE-IECON2016), Palazzo dei Congressi, Florence, Italy, for the paper entitled "Direct model predictive control with an extended prediction horizon for quasi-Z-source inverters".
- **APEC Student Travel Award**, 2017 IEEE Applied Power Electronics Conference and Exposition (APEC 2017), Tampa, Florida, USA, for the paper entitled "Variable switching point predictive current control of quasi-Z-source inverters".
- **IEEE IES Student Paper and Travel Grant**, 2017 IEEE CPE-POWERENG, Cadiz, Spain, for the paper entitled "Direct model predictive control of bidirectional quasi-Z-source inverters fed permanent magnet synchronous machines".

APPENDIX B

Nomenclature

B.1 List of Symbols

Electrical Variables:

i_{load}	Inverter input dc current
i_{C_1}, i_{C_2}	Quasi-Z-source network capacitor currents
i_{L_1}, i_{L_2}	Quasi-Z-source network inductor currents
$i_{L_1,\text{ref}}$	Inductor current reference
i_{ST}	Shoot-through current
$\boldsymbol{i}_{\text{inv}}$	Output inverter current
$\boldsymbol{i}_{o,abc}$	Three-phase output currents
$\boldsymbol{i}_{o,es}$	Estimated output current
$i_{o,\alpha}$, $i_{o,\beta}$	Output current in stationary reference frame
$i_{\alpha,\text{ref}}$, $i_{\beta,\text{ref}}$	Output current reference in stationary reference frame
I_d, I_q	Output current in rotating reference frame
$I_{d,\text{ref}}$, $I_{q,\text{ref}}$	Output current reference in rotating reference frame
P_o	Output power
$P_{o,\text{ref}}$	Output power reference
v_o (i_o)	Output voltage (current)
$\hat{v}_o$ ($\hat{i}_o$)	Peak output voltage (current)
$\cos\varphi$	Power factor
θ	Angular position of output current/voltage
v_{in}	Input dc voltage
v_{C_1}, v_{C_2}	Quasi-Z-source network capacitor voltages
$v_{C_1,\text{ref}}$	Capacitor voltage reference
v_{L_1}, v_{L_2}	Quasi-Z-source network inductor voltages

v_{dc}	Dc-link voltage
$\hat{v}_{\text{dc}}$	Peak dc-link voltage
$\boldsymbol{v}_{o,abc}$	Three-phase output voltages
$\boldsymbol{v}_{o,\text{ref}}$	Output voltage reference
$v_{o,\alpha}$, $v_{o,\beta}$	Output voltage in stationary reference frame
$v_{\alpha,\text{ref}}$, $v_{\beta,\text{ref}}$	Output voltage reference in stationary reference frame
V_d, V_q	Output voltage in rotating reference frame
$V_{d,\text{ref}}$	d-component of output voltage reference

System Parameters:

L_1, L_2	Quasi-Z-source network inductances
C_1, C_2	Quasi-Z-source network capacitances
L_s (C_s)	dc-dc converter's inductance (capacitance)
R_s (r_s)	dc-dc converter's internal resistance of the inductor (capacitor)
R (r)	qZS network's internal resistance of the inductor (capacitor)
D	Diode
R (L)	Load resistance (inductance)
L_f (C_f)	Output filter inductance (capacitance)
C_L (R_L)	Filter (load) of the nonlinear load
f_{sw}	Switching frequency
m	QZSI modulation index
m_s	Two-stage inverter modulation index
d	Shoot-through duty cycle
d_s	Conduction duty cycle of dc-dc converter switch
b	Boost factor
b_f	Boost function
$\boldsymbol{Q}$, $\boldsymbol{R}$	Diagonal, positive semidefinite weighting matrices
$I_{o,THD}$	Output current THD
T_s	Sampling interval
$J(k)$	Cost function
$\boldsymbol{u}_{abc}$	Three-phase switch position
λ_u	Weighting factor

B.2 Acronyms

A	Ampere
AC	Alternating current
CPLD	Complex programmable logic device
DC	Direct current
DG	Distribution generation
DMPC	Direct Model Predictive Control
DSP	Digital signal processing
EV	Electric vehicle

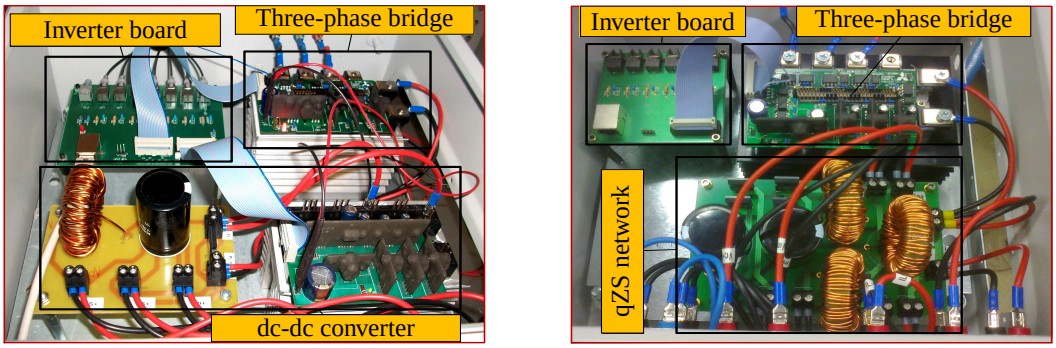
FC	Fuel cells
FCS-MPC	Finite control set model predictive control
FPGA	Field programmable gate array
GPC	Generalized predictive control
ISI	Impedance source inverter
MBPWM	Maximum boost pulse width modulation
MCBPWM	Maximum constant boost pulse width modulation
MIMO	multiple-input multipule-output
MPC	Model predictive control
MPPT	Maximum power point tracking
NST	Non-shoot-through
P&O	Perturb and observe
PI	Proportional-integral
PLL	Phase-locked loop
PR	Proportional-resonant
PSO	Particle swarm optimization
PV	Photovoltaic
PWM	Pulse width modulation
qZSI	quasi-Z-source inverter
RESs	Renewable energy sources
RHP	Right-hlaf plane
s	Second
SBPWM	Simple boost pulse width modulation
SL qZSI	Switched inductor quasi-Z-source inverter
SL ZSI	Switched inductor Z-source inverter
SPWM	Sinusoidal pulse width modulation
ST	Shoot-through
SVPWM	Space vector pulse width modulation
THD	Total harmonic distortion
THI	Third harmonic injection
UPS	Uninterruptable power supply
V	Volts
VSI	Voltage source inverter
VSP	Variable switching point
VSP2CC	Variable switching point predictive current control
W	Watt
ZSI	Z-source inverter

APPENDIX C

Test Bench

The used test bench has been built in the laboratory of the Chair of Electrical Drive Systems and Power Electronics, Technische Universität München. It includes the power electronic converters and the real-time control system.

Two kW prototypes of the two-stage inverter (dc-dc boost converter and voltage source inverter) and the quasi-Z-source inverter were built. The designed inverter prototypes are shown in Fig. C.1. The three-phase IGBT bridge Powerex IPM PM300CLA060 module is used for the qZSI and the VSI. In addition, the Powerex PM300DSA060 switch is utilized for the dc-dc boost converter. The diodes of the dc-dc converter and the qZS network are represented by RURG3060.



(a) Two-stage inverter. (b) Quasi-Z-source inverter.

Figure C.1: Inverter prototypes.

The control system consists of an FPGA board in addition to the CPLD board, 12 bit/8 channels DAC board, and 12 bit/4 channels ADC board. The FPGA is Cyclone III-EP3C40Q240C8, with 39,600 logic elements, 126 multipliers, and 1,161,216 total RAM bits. The main operating frequency of the FPGA is 20 MHz. However, by utilizing the PLL megafunction, other

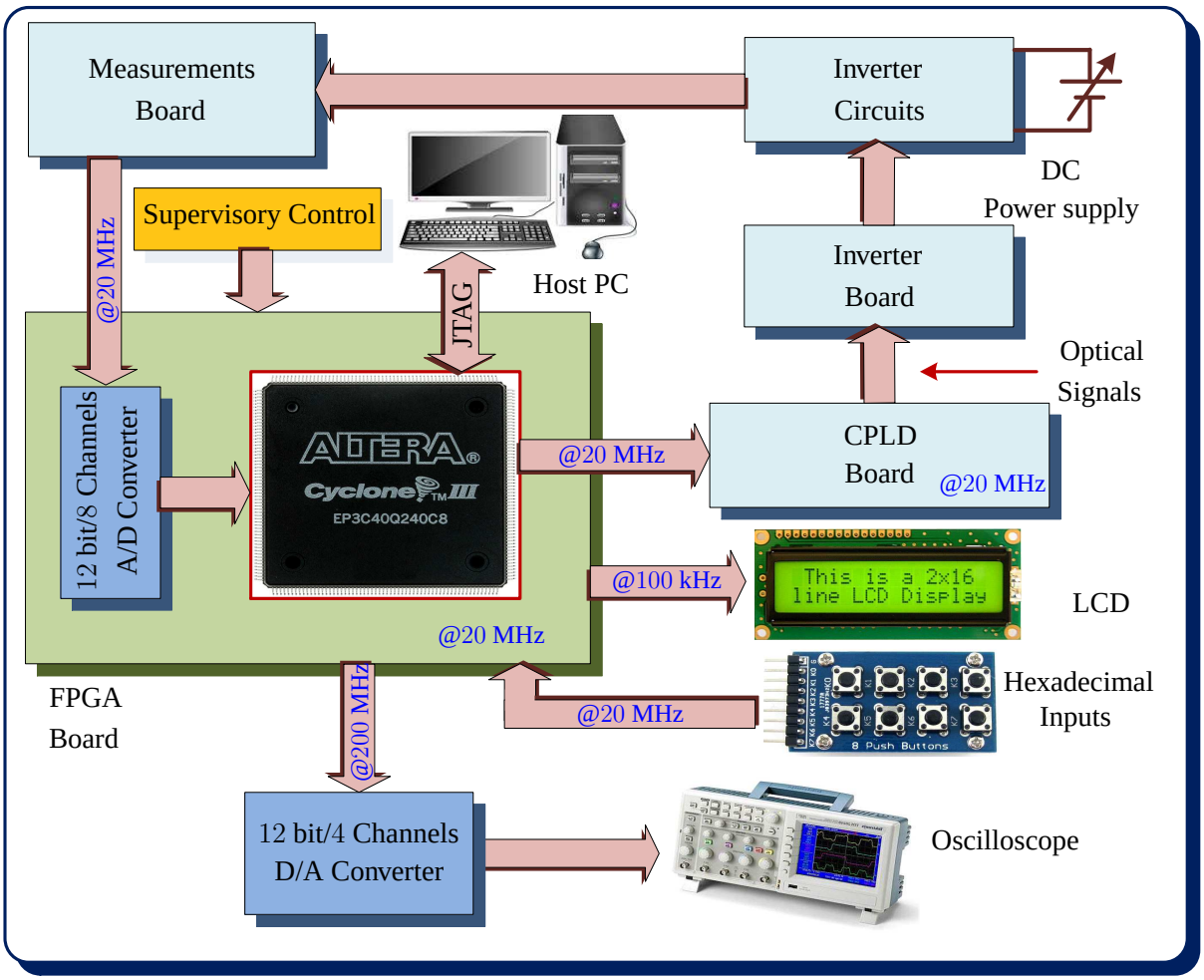


Figure C.2: Test bench schematic diagram.

frequencies can be generated for other control purposes (200 MHz for DA converter, 100 kHz for the LCD interface). In this work, the VHDL codes for all implemented control algorithms were written by myself without using the MATLAB code generation function. By doing so, long codes could be optimized and fit to the FPGA available space.

The schematic diagram of the complete test bench is depicted in Fig. C.2. A 3 kW variable dc power supply is used as a main input dc voltage to the inverters. As can be seen, the current and voltage measurements are introduced to A/D converters and then input to the FPGA, while the output voltages and currents are converted into analogue signals using D/A converters in order to be displayed on an oscilloscope. By using new digital oscilloscopes, the CSV files that store the experimental data points were generated (CSV file is a comma separated values file, which allows data to be saved in a table structured format). These CSV files then were saved in a USB flash drive and then imported into MATLAB to be plotted. By doing so, the waveforms are clearer and one can easily check the plotted signals and/or calculate the corresponding THD values.

The JTAG interface is used to download the compiled code from the host PC into the FPGA. Moreover, the supervisory control input was used to adjust the main operating mode for the

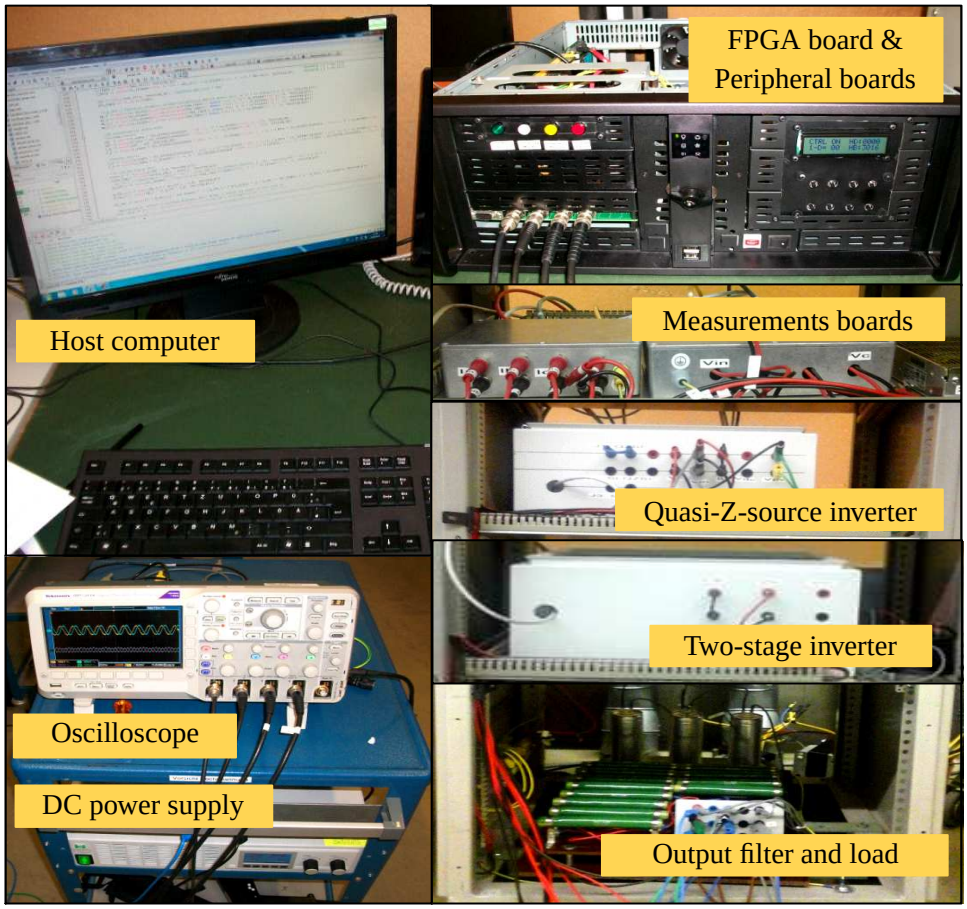


Figure C.3: System set-up in the laboratory.

Table C.1: Passive components size

Parameter	Value
qZS inductance L_1, L_2	$500\,\mu$H
qZS capacitance C_1, C_2	$470\,\mu$F
dc-dc converter inductance L	$1000\,\mu$H
dc-dc converter capacitance C	$780\,\mu$F

whole controller, i.e. start, stop, reset, etc. Besides, an LCD was used to show the status of the control system and some internal parameters in the FPGA (e.g. reference values, PI parameters, and weighting factors of MPC). The hexadecimal input switches were utilized to adjust reference values and control parameters in real time.

The complete experimental set-up is displayed in Fig. C.3. The passive components size for both the conventional two-stage inverter and quasi-Z-source inverter are summarized in Table C.1.

List of Figures

List of Tables

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