

RESEARCH PAPER

RF-MEMS variable matching networks and switches for multi-band and multi-mode GaN power amplifiers

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This work presents radio-frequency-microelectromechanical-system (RF-MEMS)-based tunable matching networks for a multi-band gallium nitride (GaN) power amplifier (PA) application. In the frequency range from 3.5–8.5 GHz return losses of 5–10 dB were measured for the input network, matching impedances close to the border of the Smith chart. For the output matching network return losses of 10–20 dB and insertion losses of 1.3–2 dB were measured. The matching networks can tune the PA to four different operating frequencies, as well as changing the transistor's mode of operation from maximum delivered-output-power to maximum power-added-efficiency (PAE), while keeping the operating frequency constant. Furthermore, different single pole double throw (SPDT)-switches are designed and characterized, to be used in frequency-agile transmit/receive-modules (T/R modules).

Keywords: Radio-frequency-microelectromechanical-system (RF-MEMS) and micro-opto-electro-mechanical systems (MOEMS), Power amplifiers and linearizers

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I. INTRODUCTION

The general trend of space-borne communication and sensing systems towards higher data throughput, frequency-agility, as well as higher power together with higher efficiency, demands more broadband and more flexible transmit/receive-modules (T/R modules). Furthermore, reconfigurability becomes an important factor to adapt to changing requirements during the lifetime of a given system. In many devices – in particular – space borne systems, components cannot be changed once deployed. Therefore, adjustments during lifetime can only be done, if they have already been foreseen and prepared during design and assembly.

Electrical reconfigurability, multi-band functionality and optimized performance can be achieved by a frequency-agile T/R module, as depicted in Fig. 1. All subcomponents of such a module have to be designed either to permanently cover the complete frequency range or to be frequency-agile. While passive components often offer broadband performances, active devices suffer from limitations on the ratio of frequency range to performance.

To be able to change a power amplifier's (PA) frequency range of operation, the transistor needs to be matched at the new operating frequency. The performance of fixed matching networks is restricted by a trade-off between bandwidth and matching. Tunable narrowband matching networks provide optimum matching conditions for different frequency-bands and modes of operation. However, for that, very low-loss tuning devices are needed.

For this radio-frequency-microelectromechanical-systems (RF-MEMS) are well suited. Malmqvist *et al.* [1] have presented variable matching networks for gallium arsenide (GaAs)- and silicon germanium (SiGe)-low-noise amplifiers (LNAs) based on capacitively loaded lines. Loading of capacitive and inductive elements is used in [2] to match a GaAs LNA. Qiao *et al.* [3] show results of a PA matched by a double stub tuner with a varactor and RF-MEMS as tuning elements. Also, Lu *et al.* [4] show RF-MEMS-based double stub networks for amplifiers.

This work targets gallium nitride (GaN) single-transistor high PA applications as a vital part of multi-purpose frequency-agile T/R modules. Such applications can feature specifications, which cannot be realized with a single amplifier module. Therefore, several amplifier modules have to be realized in parallel and switching-banks or multiplexers become necessary. This results in additional losses, more complex circuit design, and larger overall footprints. These applications can profit from the use of multi-mode matching networks (M³Ns), enabling multi-mode- and multi-frequency-amplifier modules.

Figure 1 depicts a frequency-agile multi-mode PA with RF-MEMS-based M³Ns, for which the EADS in-house

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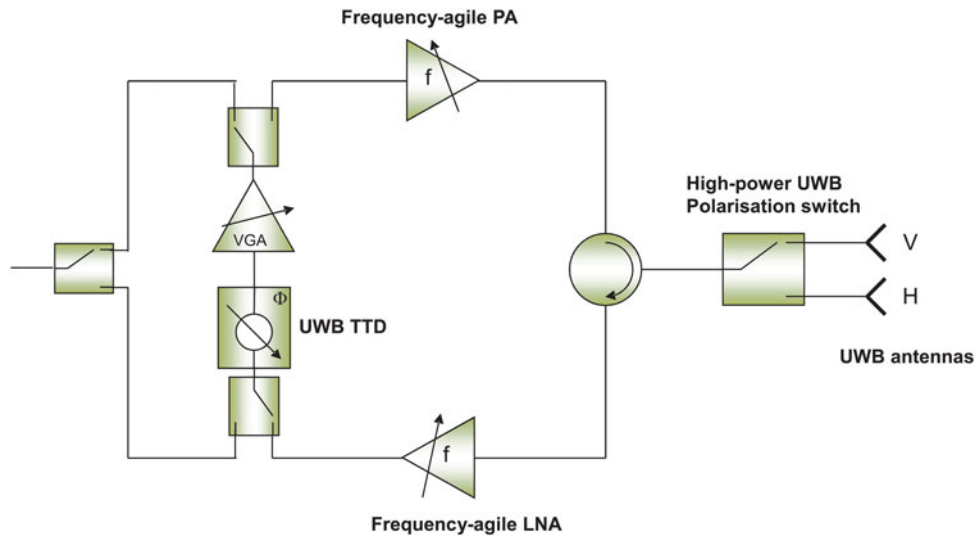


Fig. 1. Frequency-agile T/R module.

silicon-based RF-MEMS technology [5] is used. EADS in-house switches have already been demonstrated to provide hot-switching at a power level of 10 W [6].

Today, commonly-used satellite communication systems work in the frequency range between 1.5 and 18.1 GHz, while this paper focuses on C- to X-band communication (3.7–8.4 GHz). Tunable single-stub matching networks for a 6 W GaN transistor have been designed to optimally match the transistor for:

- four well-distributed frequency bands in the range from 3.5 to 8.5 GHz;
- maximum-output-power- or a maximum-power-added-efficiency (PAE)-mode.

For demonstration, these matching networks have been fabricated and characterized in a hybrid integration with a vector network analyzer (VNA) at low-input RF power.

As a second application switches are another important part of T/R module routing the signal according to transmit or receive case. The T/R module in Fig. 1 contains four single pole double throw (SPDT)-switches with different requirements in terms of isolation and power handling capability. Two switches have been designed and characterized, one for low-power-handling applications and one for high-power-handling applications with high isolation specifications. Two commercially available switches (Radant MEMS RMSW220HP and TriQuint TGS2353) were also integrated and characterized in a mutual comparison.

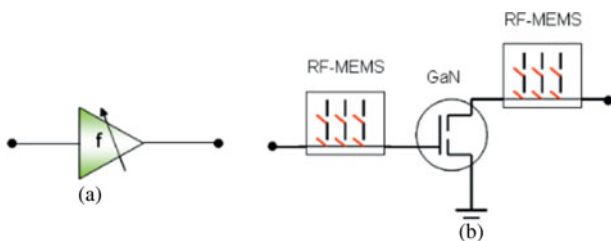


Fig. 2. Frequency-agile PA with RF-MEMS-based tunable matching networks. (a) PA and (b) PA including tunable matching.

II. FREQUENCY-AGILE MATCHING NETWORKS

A) Fixed frequency versus multi-band matching for PAs

A well-known limitation on the performance of fixed matching networks is given by the Bode–Fano-criterion [7], which Steer [8] simplifies to

$$\frac{w}{\omega_0} \ln \left(\frac{1}{|\Gamma_{avg}|} \right) \leq \frac{\pi}{Q_{load}}, \quad (1)$$

with $|\Gamma_{avg}|$ being the average absolute in-band reflection coefficient over the fractional bandwidth w/ω_0 of a lossless matching network. Q_{load} describes the quality factor of the load to be matched.

Consequently, a matching network can be designed to achieve optimum narrowband performance or offer a lower performance over a wider frequency range. Therefore, in practical systems, performance has to be traded for bandwidth according to different specifications. In addition, Steer [8] concludes that a higher Q_{load} results in a narrower bandwidth for a constant Γ_{avg} , which significantly affects the performance in multi-band applications.

Being aware of these restrictions, one can implement tunable narrowband M^3Ns , which have the potential for improved performances over bandwidth. Furthermore, tunable M^3Ns can present different impedances to a transistor, tuning it for different operation modes at constant operational frequencies. Depending on the current situation, the PA can be tuned from maximum-PAE-mode to maximum-output-power-mode, whenever more output power is needed. While a fixed matching network for PAs is always subject to compromises, a tunable M^3N enables optimized performance for different application scenarios and provides new possibilities.

B) Chosen transistor

The M³Ns are designed for a GaN transistor from Fraunhofer Institute of Applied Solid-State Physics (IAF) in Freiburg, Germany. The AlGaIn/GaN high-electron mobility transistor (HEMT) on semi-insulating semi-insulating silicon carbide (SiC) used has a gate length of 0.25 μm and operates at a bias of $V_{DS} = 28$ V. The harmonic balance simulations are performed within Agilent's Advanced Design System with a verified large-signal model in continuous wave (CW)-operation at the respective frequencies for a quiescent current of 100 mA/mm and an input power level leading to a compression level of P-2 dB. The maximum current of the transistor is 1200 mA/mm and the breakdown voltage exceeds 100 V. The HEMT is connected in microstrip transmission line technology with a substrate thickness of 100 μm . The reference planes are chosen to match the actual connection pad to the switches.

Figure 3 depicts the source and load impedances, which have to be presented to the transistor for delivering maximum output-power or maximum PAE in class A operation, being biased with $V_{DS} = 28$ V and $I_D = 120$ mA. The corresponding matching points $R + jX$ for maximum-output-power-mode (blue triangles, Fig. 3) are closer to the real-impedance axis of the Smith chart and thus have lower $Q_{load} = X/R$. Consequently, the matching network states for maximum-output-power-mode are expected to be more broadband than for the maximum-PAE-mode.

Another important factor is the intrinsic loss of the network, which limits the area of the Smith chart, which can be covered by a matching network. The matching points of the transistor's input are close to the border of the Smith chart, so that the matching is difficult.

Since the input matching points for maximum-output-power- and maximum-PAE-mode do not differ very much over frequency, it is not distinguished between the two different modes for the input matching. Therefore, only a matching network for maximum-PAE-mode is designed.

C) Design approach

1) INTEGRATION

Bond wires are necessary to integrate the M³Ns together with the transistor. These can either be compensated by dedicated matching structures on the silicon chip, be integrated as a part of the matching networks, or be absorbed into the imaginary part of the impedance to be matched. The first approach seems feasible, but consumes additional chip area; the second approach is mainly useful, when discrete components are used. Here, the bond wire's inductance is absorbed into the transistor impedance to build Γ_{load} for evaluating the design equations – equations (2) and (3) – later on.

The bond wires connecting M³N and surrounding printed circuit boards (PCBs) are not considered in the matching

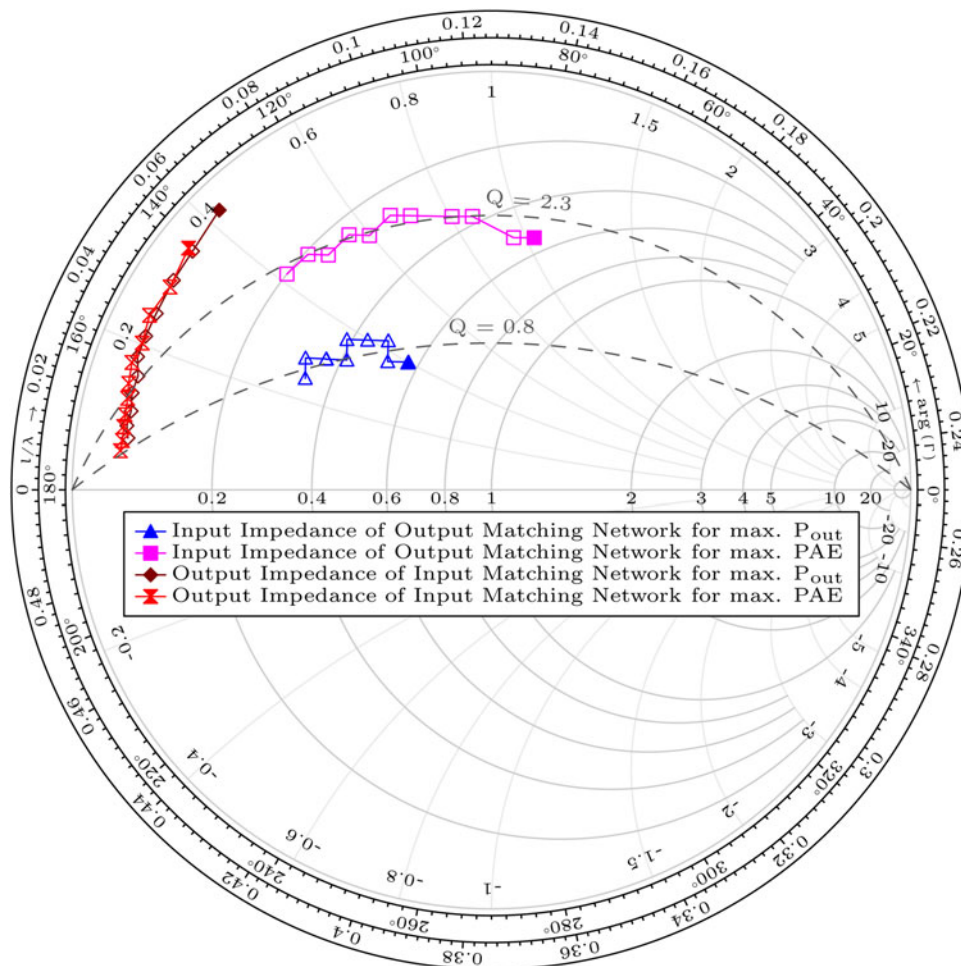


Fig. 3. Large-signal matching points of the chosen GaN transistor. Data for 3.5–8.5 GHz, normalized to 50 Ω . Filled symbols indicate data point at 3.5 GHz.

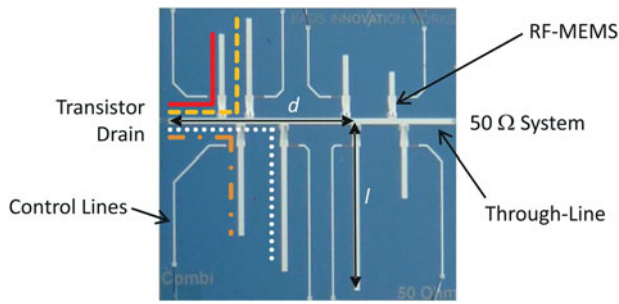


Fig. 4. Photograph of an RF-MEMS-based single-stub matching network. Different colors and linetypes indicate different matching states chosen by actuating the respective switch. d and l denote the dimensions calculated by equations (2) and (3).

network design. Additional switches can be integrated on-chip as part of a T/R module or signal routing. However, it is possible to well compensate the bond wire’s inductance with matching networks on the surrounding PCB or add additional structures in a redesign.

2) SINGLE-STUB TOPOLOGY

The tuneable single-stub topology of this work is illustrated in Fig. 4, showing eight different line stubs. This resembles a classical single-stub matching network, when only one single stub line is connected to the through-line at a time. Therefore, RF-MEMS are used and positioned directly at the through-line, reducing parasitic influences of unused stub lines. Five of the eight possible states are indicated in the photograph by different line styles and colors. This design was chosen as it is, because it is easy to implement, straight forward to design, and suitable to match theoretically any not purely complex impedance.

The stub lines of the M³Ns are realized open-ended, since the RF-MEMS process does not allow for through silicon vias. For open-ended stubs and line impedances equal to the system impedance Z_0 the distance d between stub and load, and the stub length l can be calculated as:

$$d = \frac{\lambda}{4\pi} (\angle \Gamma_{load} \pm \arccos(-|\Gamma_{load}|)), \tag{2}$$

$$l = \frac{\lambda}{2\pi} \operatorname{arccot} \left(\frac{1}{2} \tan \left(\frac{4\pi}{\lambda} d - \angle \Gamma_{load} \right) \right). \tag{3}$$

The results have to be reduced modulo $\lambda/2$ to obtain positive, minimum length values [9, chapter 12]. The equations give two possible solutions, however, in an M³N with several stubs, a compromise between the possible geometrical positions of all stubs has to be found. As described in [10], radial stubs can be used to reduce space consumption overall. This is demonstrated in this work for the input matching network.

Table 2. Comparison of calculated and chosen dimensions for the output matching network.

State	Frequency (GHz)	Mode	d_{opt} (μm)	l_{opt} (μm)	d_{calc} (μm)	l_{calc} (μm)
1	6.5	P_{out}	1569	2500	1804	1985
2	6.5	PAE	2123	3218	2182	2672
3	5.5	P_{out}	2384	2962	2542	2316
4	5	PAE	3406	4318	3651	3427
5	4	P_{out}	5262	1914	4198	2539
6	4	PAE	5567	4885	5387	4107
7	8.5	P_{out}	6654	1435	5178	4652
8	8.5	PAE	7013	2226	5764	4216

PAE, tuned for maximum-power-added-efficiency; P_{out} , tuned for maximum-output-power.

3) MATCHING NETWORKS DESIGNED

The designed states for gate and drain matching are summarized in Table 1. The input matching network uses the same states for maximum-output-power- as well as for maximum-PAE-mode while the output matching network features four dedicated states for each operational mode.

Table 2 gives a comparison of the calculated dimensions (d_{calc} , l_{calc}) for the output matching network according to equations (2) and (3), and the chosen dimensions (d_{opt} , l_{opt}) which were optimized through circuit simulations. The deviations can be explained with the parasitics of the open switches along the through line and the influence of the closed switches within the stubs. Geometrical restrictions in placing the stubs along the through line – like keeping a minimum distance between two stubs – effectively restrict the matching as calculated stub distances cannot always be realized.

D) Measurements and characterization

1) METHOD OF ANALYZING THE MEASUREMENT RESULTS

A comparison of the measurements taken by a VNA at low-input RF power and previous simulations shows good agreement. The down-state capacitance of the RF-MEMS-switches is found to be somewhat lower and the losses in the silicon substrate are somewhat higher than expected.

Figures like insertion and return loss can only be well judged in combination with the transistor, but not within a 50 Ω system. Therefore, the measurement setup needs to be deembedded from the results and a representation of the transistor has to implemented as depicted in Fig. 5.

The deembedded measurements represent the electrical behavior of the diced silicon chip itself in a 50 Ω system, which then can be recalculated to account for the integration of the transistor. The data are simulated with the transistor

Table 1. Matching networks designed.

M ³ N for	State number							
	1	2	3	4	5	6	7	8
Gate	6.5 GHz P&E	5 GHz P&E	4 GHz P&E	8.5 GHz P&E	–	–	–	–
Drain	6.5 GHz P	6.5 GHz E	5.5 GHz P	5 GHz E	4 GHz P	4 GHz E	8.5 GHz P	8.5 GHz E

E, maximum-power-added-efficiency-mode; P, maximum-output-power-mode.

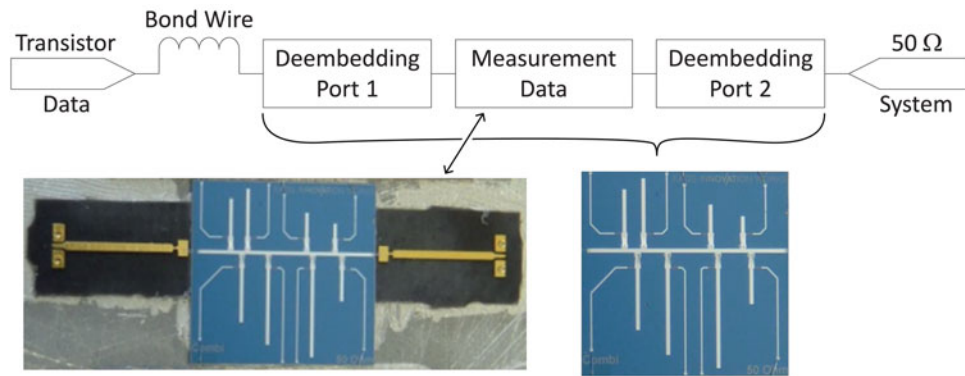


Fig. 5. Evaluation of measurement results. 50 Ω port is on silicon chip.

impedances as a port element and a series inductor to represent the bond wire between transistor and matching network.

The S-parameters presented in the following subsections are obtained by this method. Since the measurement results are recalculated with respect to the transistor impedances, the return losses are used as measures of how well the large-signal matching points have been synthesized according to Fig. 3.

2) INPUT MATCHING NETWORK

The integration of the input matching network for measurement is depicted in Fig. 6. The picture shows the diced silicon chip in a hybrid assembly surrounded by four PCB providing contact pads for ground-signal-ground-probes (GSG-probes) and connectors for the control signals. RF and control signals on the different parts are connected by bond wires, while the conductive carrier provides a common GND-plane.

A comparison between targeted, simulated, and measured output impedances of the input matching network is given in Fig. 7. Solid lines indicate the large-signal matching points for maximum-output-power-and maximum-PAE-mode from 3.5 to 8.5 GHz. The simulated points – black, rotated sandclocks, Fig. 7 – were optimized by circuit simulation to minimize return losses for maximum PAE and fit the targeted impedances well. Owing to higher substrate losses, lower down-state capacitances, and possible inaccuracies in the modeled deembedding structures, the measured impedances are shifted inwards and rotated counterclockwise on the Smith-chart.

Figure 8 depicts the evaluated measurement results of the input matching network. The network clearly matches four different frequency-bands, but matching is not optimum with 5–10 dB for the first three states and less than 5 dB for the one at 8.5 GHz.

Figure 7 shows that the measured impedances are shifted compared to the simulated values. This can result in a shift

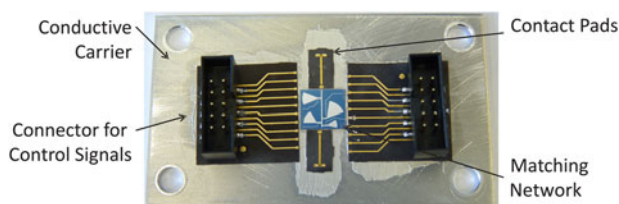


Fig. 6. Hybrid measurement setup of diced input matching network. Network realized with radial stubs.

of resonance frequencies in Fig. 8(a), depending on the frequency–response curve of the individual states and the impedances to be matched. Owing to the frequency resolution of two samples per GHz, the shifted minimum could be difficult to be observed. Together with higher substrate losses and modeling inaccuracies, the deviations from expected return losses of 10–20 dB can be explained.

As stated before, it is expected that one matching network can be used for both, the maximum-PAE and the maximum-output-power modes. The measurement results of the network confirm this, giving similar results for maximum-output-power-mode (Fig. 9). The small impedance difference for both modes results mainly at low frequencies in deviations of matching and, therefore, insertion loss. A closer synthesis of the transistor impedances would enhance the performance.

3) OUTPUT MATCHING NETWORK

The integration was carried out in the same way as shown for the input matching network in Fig. 6. A photograph of the silicon chip is depicted in Figs. 4 and 5.

A comparison between targeted, simulated, and measured input impedances of the output M³N is given in Fig. 10. Solid lines indicate the large-signal matching points for maximum-output-power- and maximum-PAE-mode from 3.5 to 8.5 GHz. The simulated points – black, rotated sandclocks, Fig. 7 – were optimized by circuit simulation and fit the targeted impedances quite well. As seen before, the measured impedances are shifted in the Smith-chart compared to the simulated and targeted values.

Figure 11 illustrates the network's performance for the maximum-PAE-mode. Return losses are better than 15 dB for the states at 5 and 6.5 GHz and around 10 dB or better for the other two states. Insertion losses are close to the expected values between 0.7 and 1.2 dB. Higher losses and lower down-state capacitance result in a degradation of the performance, but the network shows reasonably good performance.

The results for the maximum-output-power-mode are given in Fig. 12. In the frequency range from 3.5 to 7.5 GHz there is always at least one state, which provides return losses of 15 dB. Up to 7 GHz, insertion losses are better than 1 dB. State 7 has possibly moved to a higher frequency, lowering the transistor's matching to 10 dB at 8 GHz.

4) COMPARISON WITH STATE-OF-THE-ART

Table 3 gives a summary of this work in comparison to other published results. A direct comparison with other works is

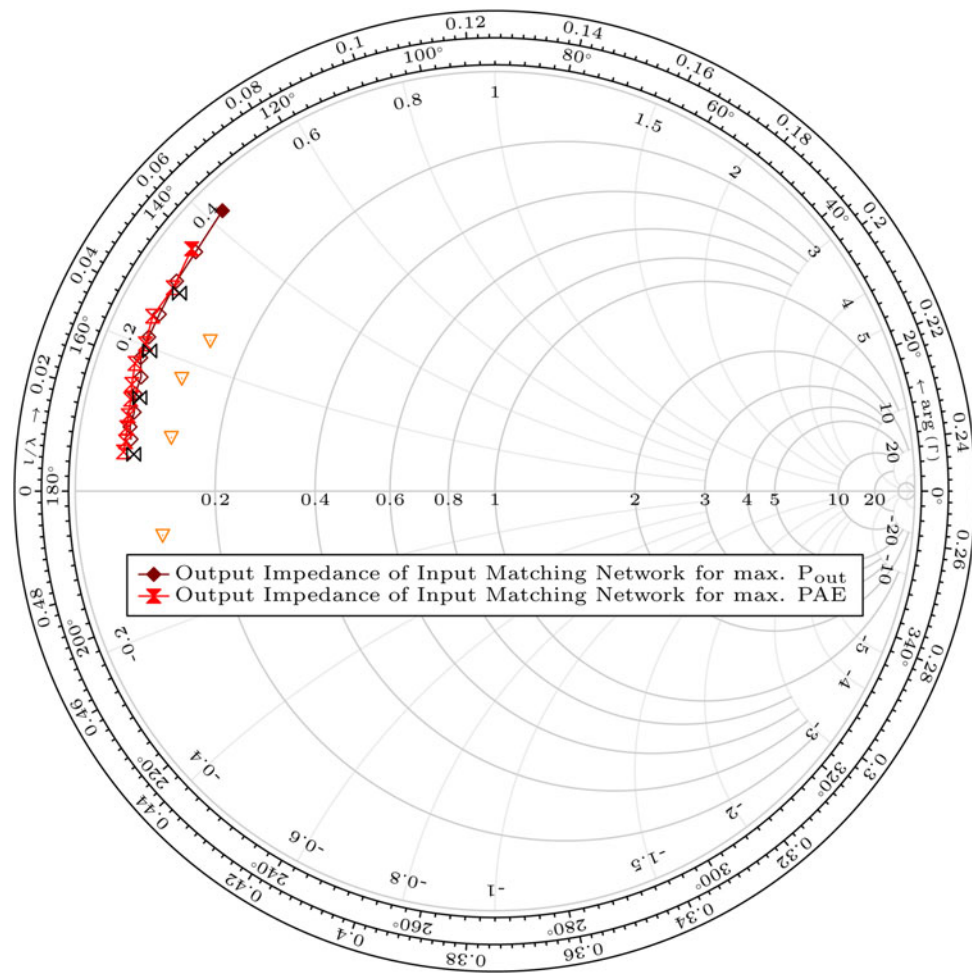


Fig. 7. Comparison between targeted, simulated, and measured large-signal matching points for input matching network. Solid lines: targeted data for 3.5–8.5 GHz, normalized to 50 Ω, filled symbols indicate data point at 3.5 GHz. Single rotated, black sandclocks: simulated values. Single up-side down, orange triangles: measured values. Simulated and measured states according to Table 1.

difficult, since different frequency-bands and transistors to be matched demand for different matching conditions.

The performance in terms of insertion and return losses of the output matching network is comparable to the data given in [1, 2, 4]. However, the M³Ns presented in this work exhibit a wider fractional tuning range of 77 and 90% as compared to a maximum of 45% in [2]. In addition, the networks are

designed to tune the transistor to different operating modes without changing the operating frequency.

The output matching network allows to match the transistor for maximum output-power with a return loss of 15 dB and more, for frequencies up to 7.5 GHz. In this frequency range the single matching states overlap in a way so that the transistor can be used at any frequency with a good matching.

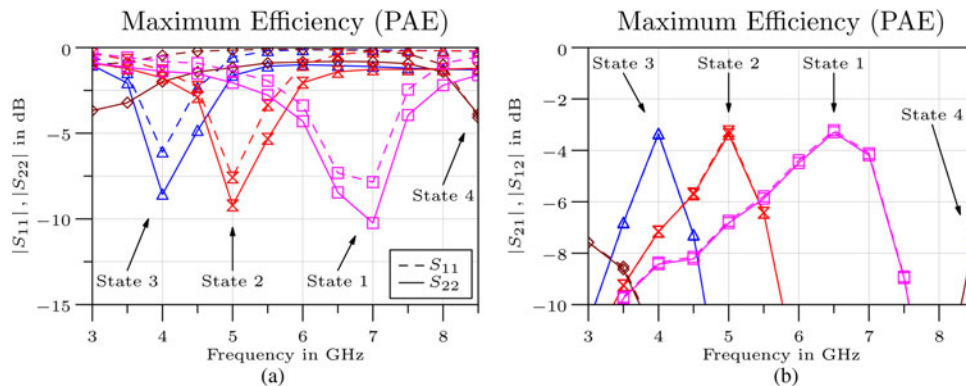


Fig. 8. Measurement results of the input matching networks for maximum-PAE-mode. Port 1: transistor, port 2: 50 Ω system. (a) Matchings versus frequency and (b) insertion losses versus frequency.

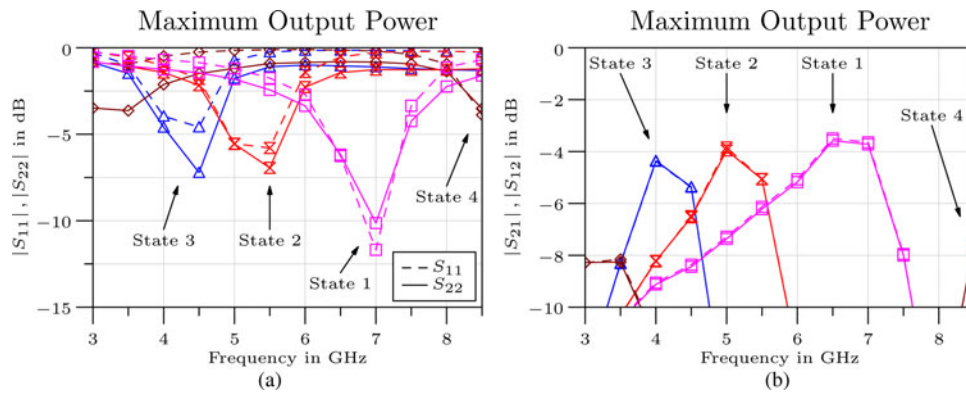


Fig. 9. Measurement results of the input matching networks for maximum-output-power-mode. Port 1: transistor, port 2: 50 Ω system. (a) Matchings versus frequency and (b) insertion losses versus frequency.

III. SWITCHES

A) Low-power-handling switch: complementary-metal-oxide-semiconductor (CMOS)-SPDT

1) DESIGN

As low-power device a CMOS – switch was designed in a 0.18 μm RF CMOS silicon-on-insulator (SOI) technology

provided by Towerjazz. The schematic of the switch is given in Fig. 13, realized in a series shunt configuration, using two transistors in series in each branch.

In order to minimize the losses through gate and body, 60 kΩ series-resistors are used at the corresponding terminals. This is often also referred to as floating body technique. In addition, the body contacts are biased with a negative direct current (DC) voltage when the transistor is in off-state. Hence, the parasitic capacitance between drain and source is minimized and isolation is improved.

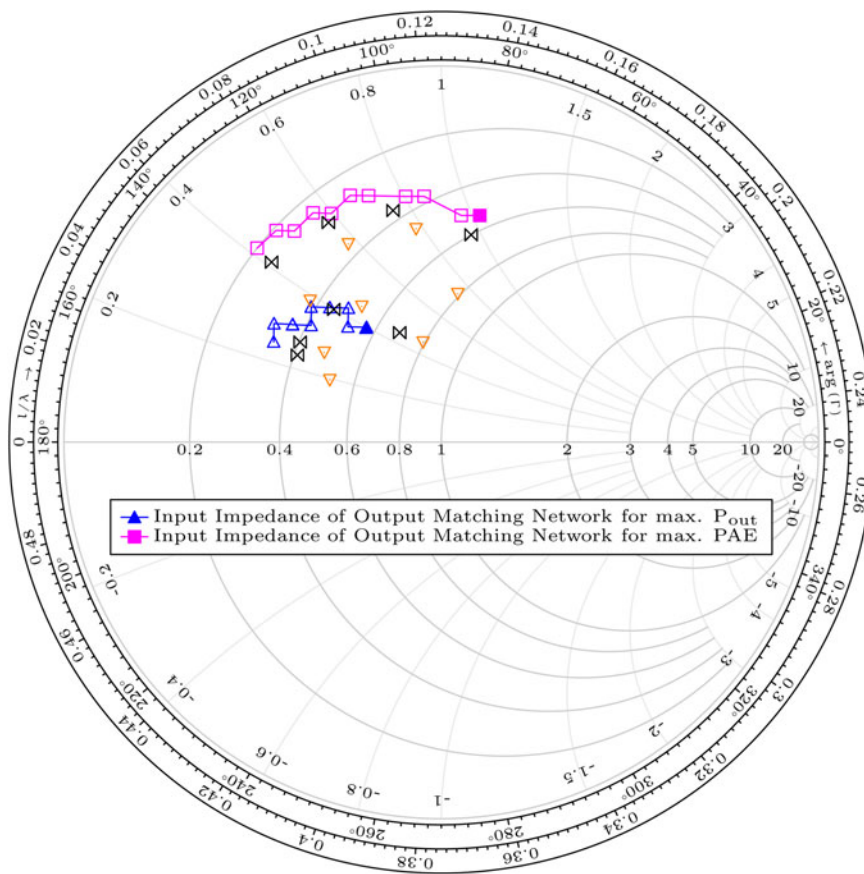


Fig. 10. Comparison between targeted, simulated, and measured large-signal matching points for output matching network. Solid lines: targeted data for 3.5–8.5 GHz, normalized to 50 Ω, filled symbols indicate data point at 3.5 GHz. Single rotated, black sandclocks: simulated values. Single up-side down, orange triangles: measured values. Simulated and measured states according to Table 1.

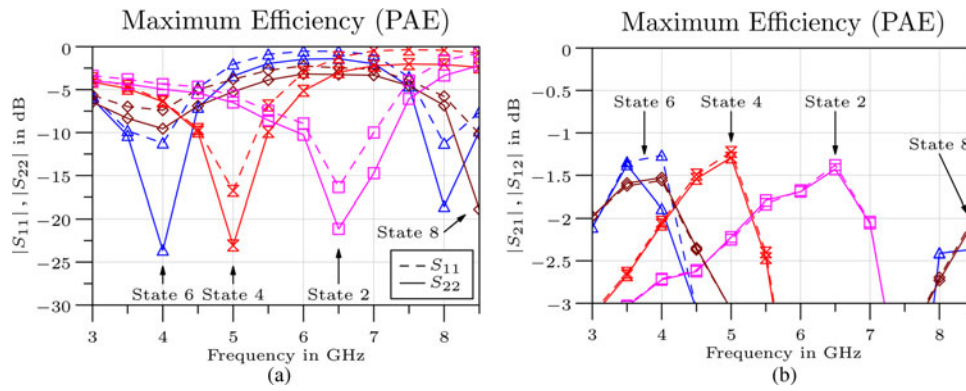


Fig. 11. Measurement results of the combined output matching networks for maximum-PAE-mode. Port 1: transistor, port 2: 50 Ω system. (a) Matchings versus frequency and (b) insertion losses versus frequency.

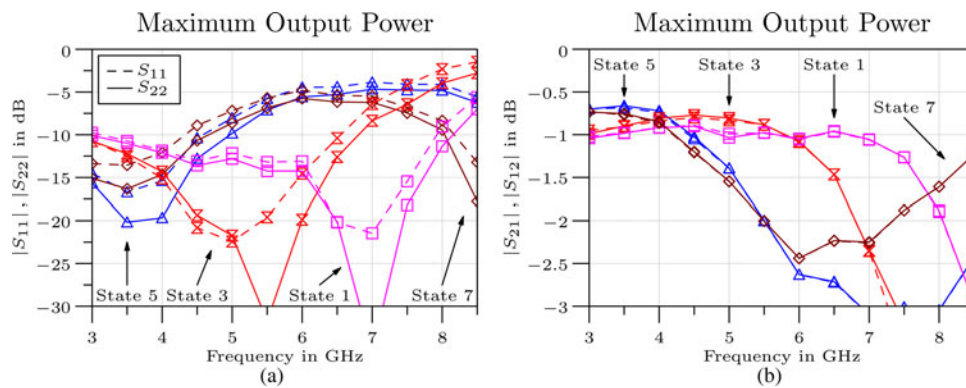


Fig. 12. Measurement results of the combined output matching networks for maximum-output-power-mode. Port 1: transistor, port 2: 50 Ω system. (a) Matchings versus frequency and (b) insertion losses versus frequency.

Table 3. Comparison with state-of-the-art.

Source	Remarks	Tuning range (TR) (GHz)	Frac. TR (%)	States	$ S_{11} , S_{22} $ (dB)	$ S_{21} $ (dB)
[1]		23.9 to 26.4	10	4	≤ -15	-2 to -1.5
[2]	Type I	10.7 and 16.6	45	2	-20 to -10	-3.3 to -0.9
	Type II	15.2 and 23.1	42	2	-15 to -8	-3 to -1
[4]	Input matching network	6 and 8	29	2	-15 to -10	-5 to -2
	Output matching network	6 and 8	29	2	-15 to -10	-1
This work	Input matching network	4 to 8.5	77	4	-7 to -4	-7.5 to -3.4
	Output matching network					
	Max. output power mode	3.5 to 8.5	90	4	-20 to -12	-1.3 to -0.7
	Max. PAE mode	3.5 to 8.5	90	4	-16 to -10	-2 to -1.3

The final switch occupies an area of around 0.29 mm² including all 14 bond pads. Several deep trench rings are placed around each transistor for improved isolation and to enable the negative body bias.

2) MEASUREMENT AND CHARACTERIZATION

The CMOS-switch was fabricated and integrated in a Rogers RT/Duroid 5880 PCB in a cavity to minimize bondwire length. Matching structures are used to compensate the effect of the bondwires. The measurement results are shown in Fig. 14.

Insertion losses of 1.1–2.3 dB of the integrated CMOS-switch are close to the simulated value of ≈1 dB at

lower frequencies, which does not include bondwire inductivity and bonding pad capacities. Return losses are higher than 14 dB and isolation greater than 12 dB over the complete frequency range.

B) High-power-handling switch: RF-MEMS-SPDT

1) DESIGN

The silicon-based RF-MEMS has been designed on the EADS in-house-process, capable of hot-switching up to 10 W [6]. An

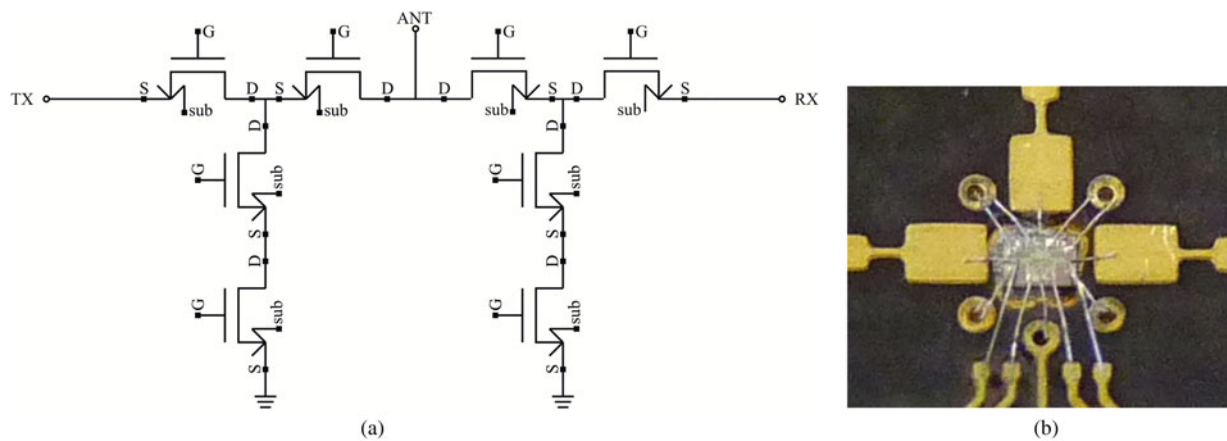


Fig. 13. Schematic of CMOS-switch. (a) Schematic and (b) photograph of integration.

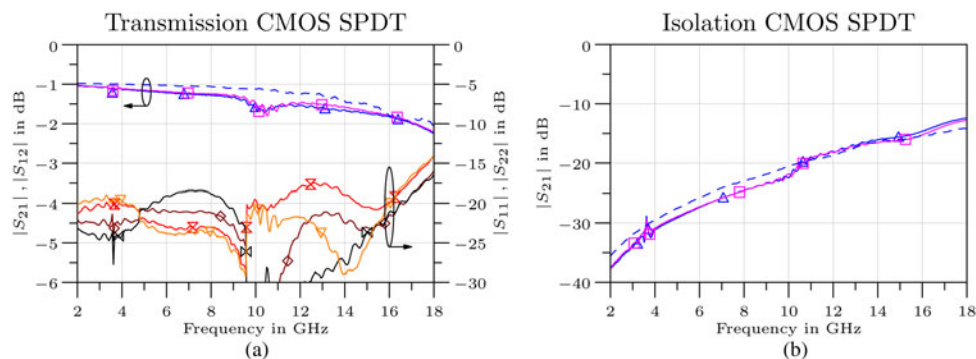


Fig. 14. Measurement results of the CMOS-switch. Dashed lines: simulation, solid lines: measurements. (a) Matchings and insertion losses versus frequency and (b) isolation versus frequency.

internal standard switch is used as a basic switching-element in the design, which is given in Fig. 15.

Each branch of the SPDT contains two switches to provide high isolation for high-power applications. To compensate the series capacitance of the RF-MEMS an inductive piece of line is introduced close to the input of the SPDT.

2) MEASUREMENT AND CHARACTERIZATION

The chip was integrated in a cavity with compensation structures for the bondwire inductance to characterize the switch itself. The measurement results of one of the symmetrical paths are depicted in Fig. 16 and match the simulation

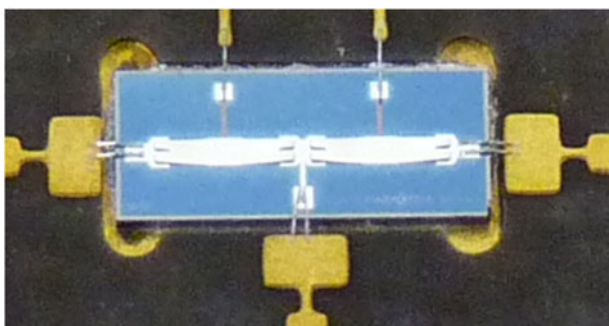


Fig. 15. Photograph of integrated silicon RF-MEMS-SPDT. Input on bottom side, outputs left and right, control lines on top.

results, considering the lower down-state capacitance and higher substrate losses, as stated before.

Insertion losses are measured to be 0.8–1.2 dB above 4 GHz. At lower frequencies insertion losses rise up to 2.5 dB, due to the lower down-state capacitance. Return losses are higher than 10 dB above 4.5 GHz. Since no dedicated external matching structures are used – only compensation for the bondwire inductance is applied – return losses could possibly be improved by dedicated matching on the PCB. Isolation is measured to be better than 37 dB in the measured frequency range of 2–18 GHz.

C) Investigation on commercial SPDT-switches

1) RF-MEMS-SWITCH

A commercially available RF-MEMS-SPDT from Radant MEMS has been measured as a medium power device. Figure 17 depicts the measurement results of the device integrated in a Rogers RT/Duroid 5880 PCB.

Approximately 15 dB of isolation were measured at the upper frequency range, while below 9 GHz, considerably higher values of 35 dB were achieved. Return losses are higher than 17 dB in transmission configuration. Insertion losses are below 0.8 dB but slightly different in both paths. A resonance occurs at around 13 GHz, which is very likely due to the integration and should be removed in future designs.

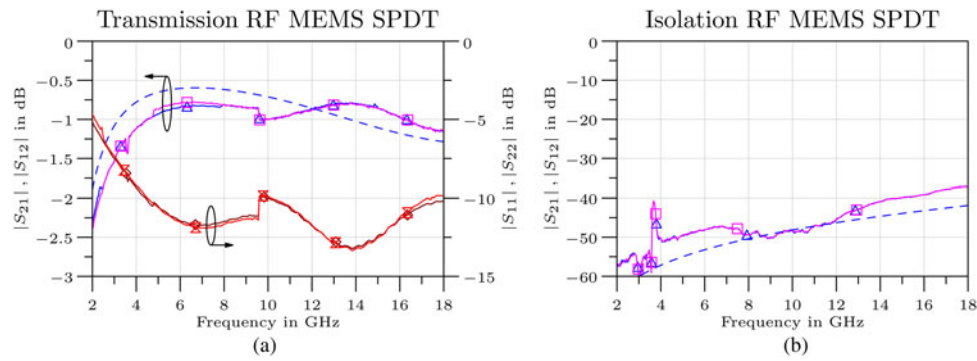


Fig. 16. Measurement results of the silicon RF-MEMS-switch. Dashed lines: simulation, solid lines: measurements. (a) Matchings and insertion loss versus frequency and (b) isolation versus frequency.

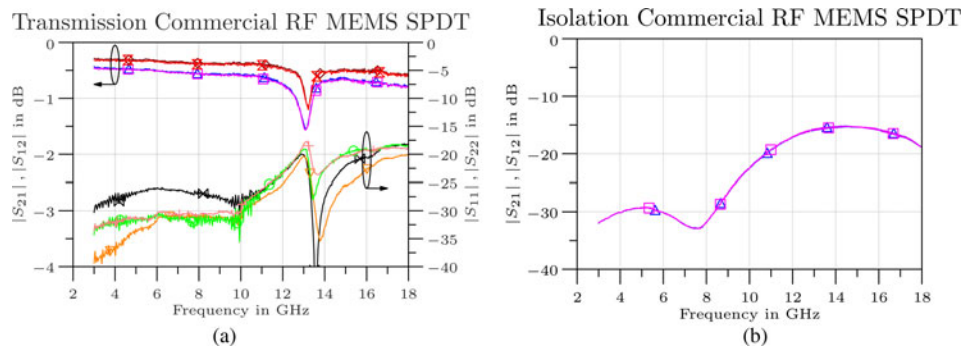


Fig. 17. Measurement results of the commercial RF-MEMS-switch. (a) Matchings and insertion losses versus frequency and (b) isolation versus frequency.

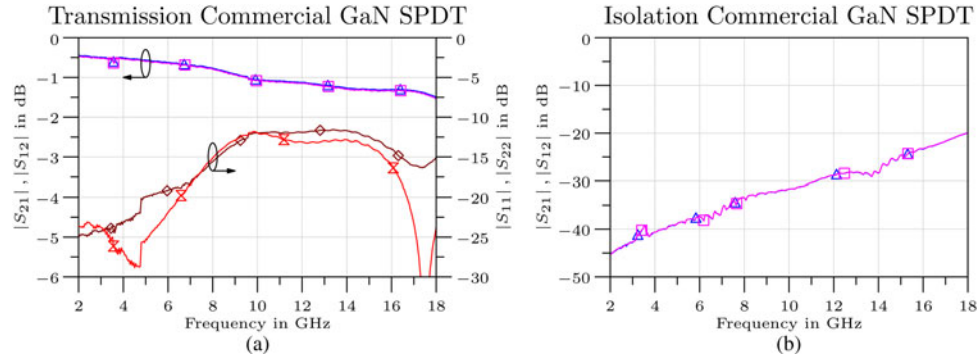


Fig. 18. Measurement results of the GaN-switch. (a) Matchings and insertion losses versus frequency and (b) isolation versus frequency.

2) GAN-SWITCH

As a second high-power-capable device, a commercially available GaN-switch from TriQuint has been integrated with a Rogers RT/Duroid 5880 substrate and the overall set-up was measured. The results for one of the two symmetrical paths are given in Fig. 18, and show low-insertion loss of 0.5–1.6 dB and return losses higher than 15 dB. Isolation is higher than 20 dB.

D) Comparison

Table 4 summarizes the measurement results for the different switches between 2 and 18 GHz. The low-power-handling switches are similar in performance, with lower insertion losses for the commercial device above 8 GHz. However, the integration of the commercial SPDT is assumed to be

responsible for the resonance in the measurements, which has to be removed to be usable. However, in the targeted frequency range of the PA, both switches can be used.

The high-power-handling switches show different characteristics. While the commercial device features lower overall insertion loss and higher return loss, the self-designed SPDT provides higher isolation. In addition, the commercial GaN-switch uses non-linear devices, and therefore, suffers from loss compression with higher input power – in contrast, RF-MEMS are considered to be highly linear devices. The EADS in-house technology in-use has been demonstrated to be capable of hot-switching up to 10 W of RF power without performance degradation [6]. Below 4.5 GHz insertion loss is significantly higher than for the commercial GaN-switch, due to the capacitive behavior of the switch. Consequently, the choice of the high-power-handling switch depends on the specifications and requirements of the actual application.

Table 4. Comparison of different evaluated switches for 2 to 18 GHz.

Switch	Insertion loss (dB)	Return loss (dB)	Isolation (dB)	Power capability (hot-switching)	Remarks
CMOS-SPDT	1 to 2.3	>14	>12 dB	Unknown	
Comm. RF-MEMS-SPDT	<0.8	>17	>15 dB	20 dBm*	At 20 dBm: reduced number of switching-cycles
RF-MEMS-SPDT	1.2 to 2.5	>10	>37 dB	>40 dBm	Matching not optimized
Comm. GaN-SPDT	0.5 to 1.6	>13	>20 dB	40 dBm*	Losses increase above 32 dBm*

*Taken from datasheet.

A low-frequency switch was designed to extend the usable frequency range below 4.5 GHz for future designs. The single pole single throw (SPST) was integrated in a Rogers RT/Duroid 5880 PCB in a similar way as the other switches and characterized. The switch provides insertion loss lower than 1.1 dB in the frequency range from 2 GHz up to 40 GHz. The return losses were not optimized with matching structures and were measured to be better than 10 dB above 2 GHz. Isolation is higher than 27 dB at 40 GHz and below 35 dB at 10 GHz.

IV. CONCLUSIONS

This paper demonstrates tunable single-stub matching networks for a 6 W GaN transistor and different switches. Both are considered to be used for frequency-agile T/R module. The output M³N can switch the transistor's mode of operation between maximum-delivered-output-power- and maximum-PAE-mode for four frequencies, providing good matching conditions of 10–20 dB. This functionality is demonstrated in the frequency range from 3.5 to 8.5 GHz.

Two SPDT-switches have been designed, characterized and compared to commercial equivalents. While the low-power-handling SPDTs show similar performance up to 8 GHz, the high-power-handling switches provide different characteristics. The designed high-power-handling switch provides isolation of higher than 37 dB compared to 20 dB of the commercial device. For frequencies below 4.5 GHz insertion loss is higher than demonstrated for the commercial device, due to the capacitive behavior. Since the commercial device shows loss compression with increasing input power, the linear RF-MEMS-based switch provides more constant characteristics for high-power applications.

As next step the matching networks will be integrated with the transistor to characterize the frequency-agile PA.

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