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Modeling and Simulation of InAs Nanowire Transistors

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To my parents and friends

Abstract

State-of-the-art InAs nanowire based devices reveal excellent DC performance in terms of transconductance, subthreshold slope and saturation behavior. Only very recently high frequency measurements have been performed on these devices, demonstrating that they can operate well in the GHz range. However their intrinsic high frequency performance and the limiting mechanism in reaching the theoretical limit have not been fully understood yet. One of the main reasons lies in the technological difficulties in contacting the nanometer devices and in the parasitic elements that arise from this imperfect measurement setup.

In this work we have investigated the electron transport and frequency response of state-of-the-art single InAs nanowire field effect transistors using two different approaches: a full-band Monte Carlo simulator and a sophisticated hydrodynamic simulator. After calibrating our simulations with experimental measurements, that are successfully reproduced, we are able to make predictions about the electron distribution inside the nanowire transistor and via a small signal analysis we determine the intrinsic cut-off frequency and maximum frequency of oscillation. Both methods deliver comparable results for these Figures Of Merit. Based on our simulations, we deduce that the intrinsic high frequency performance of these devices is at least one order of magnitude higher than currently reached today, in terms of maximum oscillation frequency and cutoff frequency, and that the parasitic network is the major limiting factor. Furthermore we identify the parasitic elements that have the greatest impact on the device performance and we explain their working principles. These findings are confirmed by very recent measurements with optimized contact geometries.

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1 Introduction

Motivation

Over the last 50 years transistor size has continued to scale down following the law formulated by Gordon Moore [1]. Shrinking the gate length has brought great benefits both in cost and performance. A shorter channel leads on one hand to better transistor performance since lower operating voltages are required and faster switching speeds can be obtained, on the other hand it also leads to lower costs per transistor since more of them can be packed on a wafer. However as the scaling entered well into the nanometer regime [2] the optical lithography process approaches some technological difficulties and fundamental limits [3]. As a result some serious problems have appeared: the loss of electrostatic control of the gate over the conducting channel is one of them. This translates in fluctuations of the threshold voltage, increased subthreshold swing and unacceptable high off currents, which affect the static power consumption of any electronic device [4,5]. Other problems related to the shrinking dimensions of the transistor are the tunneling currents through the gate oxide (only 1.2 nm thick for the 65 nm node [2]), which also increase the leakage and thus the dynamic power consumption of the device.

It becomes obvious that new concepts are required if the down scaling trend is to continue. The multiple gate (MG) field effect transistor (FET) has attracted much attention in recent years [6] promising to be a genuine solution for all the above mentioned problems and still have a large packing density. For this novel device two implementations have been demonstrated: the “top-down” and the “bottom-up” approach [6,7].

The “top-down” approach is preferred by the semiconductor industry because it still uses a conventional lithography process to define a 3D finger-like channel for the field effect transistors, also called FinFETs, which is then surrounded by an

omega-shape gate. It represents a turning point in the evolution of the transistor and it had a remarkable short time to market: only 10 years have passed from the first demonstration of such a device by Intel [6] to the presentation of the first Ivy Bridge microprocessor based on 22 nm FinFET technology [8]; other competitors are adopting the FinFET as well [9]. The geometry of the control terminal (omega-gate) leads to drastic improvements in the transistor performance: the device presented in [8] has a subthreshold slope of 69 mV/decade, very close to the theoretical limit of 60 mV/decade, an ON-current of 1 mA/ μm and OFF-current of 70 nA/ μm .

The “bottom – up” approach is an entirely non-conventional technique which implies growing semiconductor nanowires on a chosen substrate with or without a catalyst. Nanowires are cylindrical, high aspect ratio structures, with diameters ranging from a few nm to a few hundred nm and lengths from a few hundred nm to some tens of μm [10]. Due to the two dimensional quantum confinement – in the radial plane – these structures have unique electrical, mechanical and optical properties [11]. After growth the nanowires that will then form the channel of nanowire field effect transistors (NW-FETs) are surrounded by the gate oxide resulting in a gate-all-around structure (GAA) [12].

Both approaches of patterning the gate electrode around the conducting channel increase the electrostatic control and thus improve the leakage or subthreshold swing [8] but they produce complex channel geometries where charge carriers are no longer confined to travel in a single plane under the gate electrode.

Silicon FinFETs have been successfully fabricated and demonstrated [6] however they suffer from a major drawback: the relatively low electron mobility in silicon [13,14]. Furthermore, in silicon NW with very small radius a surface depletion layer is formed [15] and one needs to apply a relatively large control voltage in order to obtain electron accumulation and subsequently the inversion layer. Both of these drawbacks make silicon FinFETs and NW-FETs unsuitable for low voltage high speed application.

The International Technology Roadmap for Semiconductors (ITRS) 2013 is depicted in Fig. 1.1, the RF CMOS requirements to be more precise. One can see that for the planar bulk (PB) or for the ultra-thin body fully-depleted (UTB FD) devices basically all the figures of merit (FOM) – like transit frequency (f_T), maximum frequency of oscillation (f_{max}) or 1/f noise – are highlighted in yellow

Table RFAMS1 RF CMOS Technology Requirements

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra thin body fully depleted (UTB FD) SOI or multi-gate (MG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the PIDS chapter for further discussion).

Year of Production	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
MPU/ASIC Metal 1 (M1) 1/2 Pitch (nm) [contacted]	40	32	32	28.3	25.3	22.5	20.0	17.9	15.9	14.2	12.6
High Performance Logic transistor for non-saved applications											
L_{HP} : Physical Gate for High Performance (HP) Logic (nm) [1]	20	18	17	15.3	14.0	12.8	11.7	10.6	9.7	8.9	8.1
V_{DD} : Power Supply Voltage for High Performance (HP) Logic (V) [2]											
Bulk:UTB FD/MG	0.85	0.82	0.80	0.77	0.75	0.73	0.71	0.68	0.66	0.64	0.62
f_T : cutoff frequency (GHz) [3]											
Extended Planar Bulk	445	512	578	669	756						
UTB FD	477	545	614	704	790	889	987	1,156			
MG			620	710	795	890	994	1,137	1,281	1,432	1,613
f_{osc} : maximum frequency of oscillation (GHz) [4]											
Extended Planar Bulk (junction)	389	439	510	584	672						
UTB FD (body)	412	462	531	596	667	751	840	958			
MG (body)			560	622	686	755	827	912	1,014	1,113	1,236
$NF_{min,60}$: minimum noise figure at 60GHz (dB) [5]											
Extended Planar Bulk	1.04	0.91	0.82	0.72	0.64						
UTB FD	0.97	0.86	0.78	0.68	0.61	0.55	0.50	0.43			
MG			0.77	0.68	0.61	0.55	0.50	0.44	0.39	0.35	0.31
low-frequency analog power gain (dB) [6]											
Extended Planar Bulk	14.3	14.1	14.8	14.8	15.3						
UTB FD	15.4	15.2	15.6	15.3	15.2	15.2	15.4	15.1			
MG			17.3	16.7	16.5	16.3	16.0	15.5	15.3	15.1	14.7
MSG60 : maximum stable gain at 60GHz (dB) [7]											
Extended Planar Bulk	14.3	14.8	15.3	15.8	16.3						
UTB FD	15.3	15.7	16.1	16.5	16.8	17.2	17.5	18.0			
MG			15.8	16.2	16.5	16.9	17.2	17.6	17.9	18.2	18.6
analog transistor voltage gain @ 10% $I_{D,max}$ & 5X minimum L_g (-) [8]											
Extended Planar Bulk	52	51	55	55	58						
UTB FD	59	57	60	58	58	58	59	57			
MG			73	69	66	65	63	59	58	57	55
I/f noise ($\mu V^2 \mu m^2 / Hz$) [9]											
Extended Planar Bulk	48.4	43.3	38.4	33.9	29.6						
UTB FD	61.5	57.6	53.8	50.2	46.7	42.4	38.4	35.3			
MG			57.6	53.8	50.2	46.7	44.1	41.6	39.2	36.9	34.6
σV_{th} matching (mV μm) [10]											
Extended Planar Bulk	1.72	1.69	1.63	1.57	1.49						
UTB FD	1.94	1.95	1.93	1.91	1.87	0.58	0.55	0.53			
MG			2.00	1.97	1.94	0.61	0.59	0.57	0.56	0.54	0.52
Low Standby Power Logic transistor for microwave & mobile applications											
L_L : Physical Gate for Low Standby Power (LSP) Logic (nm) [1]	23	21	19.2	17.5	16	14.6	13.3	12.1	11.1	10.1	9.2
V_{DD} : Power Supply Voltage for Low Standby Power (LSP) Logic (V) [2]											
Bulk:UTB FD/MG	0.87	0.84	0.81	0.78	0.75	0.72	0.70	0.67	0.65	0.63	0.61
f_T : cutoff frequency (GHz) [3]											
Extended Planar Bulk	286	335	394								
UTB FD	322	376	435	505	589	687					
MG			443	515	600	700	776	904	1,018	1,137	1,280
f_{osc} : maximum frequency of oscillation (GHz) [4]											
Extended Planar Bulk (junction)	282	340	408								
UTB FD (body)	284	336	388	437	499	574					
MG (body)			383	428	492	558	608	685	762	848	947
$NF_{min,24}$: minimum noise figure at 24GHz (dB) [5]											
Extended Planar Bulk	0.87	0.58	0.50								
UTB FD	0.69	0.52	0.45	0.39	0.34	0.29					
MG			0.45	0.39	0.33	0.29	0.26	0.22	0.20	0.18	0.16
low-frequency analog power gain (dB) [6]											
Extended Planar Bulk	16.3	17.3	18.3								
UTB FD	15.2	15.6	15.7	15.3	15.2	15.3					
MG			15.7	15.1	15.0	14.5	14.1	13.8	13.4	13.1	12.8
MSG24 : maximum stable gain at 24GHz (dB) [7]											
Extended Planar Bulk	14.3	14.8	15.3								
UTB FD	13.4	13.8	14.2	14.6	15.1	15.7					
MG			13.8	14.2	14.6	15.2	15.6	16.3	16.8	17.4	18.2
analog transistor voltage gain @ 10% $I_{D,max}$ & 5X minimum L_g (-) [8]											
Extended Planar Bulk	66	73	82								
UTB FD	58	60	61	58	57	58					
MG			61	57	56	53	51	49	47	45	43
I/f noise ($\mu V^2 \mu m^2 / Hz$) [9]											
Extended Planar Bulk	77.3	66.6	57.6	0.0	0.0						
UTB FD	102.4	90.0	78.4	67.6	57.6	48.4					
MG			102.4	90.0	78.4	72.9	67.6	62.5	57.6	52.9	49.3
σV_{th} matching (mV μm) [10]											
Extended Planar Bulk	1.90	1.80	1.70	0.00	0.00						
UTB FD	2.19	2.09	1.99	0.73	0.67	0.62					
MG			2.26	0.84	0.79	0.76	0.73	0.70	0.67	0.65	0.62

Manufacturable solutions exist, and are being optimized
 Manufacturable solutions are known
 Interim solutions are known
 Manufacturable solutions are NOT known

Figure 1.1: The International Technology Roadmap for Semiconductors (ITRS) - RF CMOS Technology Requirements - 2013. Table taken from [16]

for the years 2013 and 2014. Post 2014 FOMs are all highlighted in red. The color code translates: "Manufacturable solutions are known" for yellow and "Manufacturable solutions are NOT known" for red. The conclusion for these two types of devices (PB and UTB FD) would be that they have reached the end of the Roadmap in 2015. For the multiple gate (MG) devices the situation looks only a little better, there are manufacturable solutions known till 2017.

So the MG transistors have two more years compared with the other CMOS technologies; afterwards all the FOMS are highlighted in red as well.

This situation is alarming and consists the main motivation why III/V semiconductor nanowires should be extensively studied and considered as a possible replacement for CMOS. GaAs, InAs and some ternary alloys have electron mobilities one order of magnitude higher than silicon [17]. InAs has in comparison to GaAs, a much lower effective mass, a higher mean free path, λ [18] and higher separation of satellite valleys [19]. The later property makes the transferred electron effect, from the Σ to the L valley negligible [20] and with it no unwanted negative differential conductivity or oscillations as in GaAs HEMTS. All these attributes make InAs very appealing as a channel material for the NW FET [12,21,22], especially for low voltage - high speed application.

The first disclosure of an InAs NW transistor dates back to Bryllert *et al.* [23] almost a decade ago. Since then the interest has constantly increased [22,24,25] and some excellent devices have been demonstrated, for example the state of the art InAs NW transistors with mobilities of around $7000 \text{ cm}^2/\text{Vs}$ and ON-currents in the order of mA at low operating voltages by Dayeh *et al.* [22].

As promising as these values may sound for high speed low power application, only very few high frequency measurements have been performed on InAs NW transistors [24–26]. The main difficulty in an accurate high frequency characterization lies in the presence of parasitic elements (pad capacitances) in the measurement setup, elements which tend to become dominant and to severely deteriorate the high frequency performance. Therefore it is not clear which are the intrinsic properties of the InAs NWs, in terms of a unity current gain cutoff frequency, maximum oscillation frequency or maximum stable gain.

It is the intention of this work to answer these questions and to provide reliable predictions with the help of computer based physical simulations. Computer simulations can provide valuable insights in the device physics during operations, when direct measurements can be difficult to make or sometimes even impossible.

There are different approaches for the simulation of nanodevices: the non-equilibrium Green's function (NEGFs), a fully quantum mechanical method that was successfully demonstrated in [27–29]. It is however very time and resource

demanding. The Monte Carlo (MC) method is a semi-classical approach and has been demonstrated in [30,31]; it provides accurate results and has medium demands on memory and computational resources. Another approach is to use a modified hydrodynamic simulator, which solves also higher moments of the Boltzmann Transport Equation (BTE) and incorporates all relevant physical models for the NWs [32,33]; this is by far the fastest approach and it allows the simulation of entire subsystems made of transistors and parasitic networks.

In this work we perform our modeling and simulations using the latter two approaches: the Monte Carlo method since it proves to be a good tradeoff between physical accuracy and resource (time and computational) requirements and the hydrodynamic transport model since it enables the simulation of complex devices and subsystems. The Monte Carlo simulator is a C++ developed code [34] whereas the hydrodynamic simulations are carried out with Sentaurus from Synopsys [35], a state-of-the-art commercial simulator.

Our aim is to give a reliable prediction of the InAs NW transistor performance and to better understand charge carrier transport and all the physical processes in these complex 3D geometries. Subsequently the limiting factors can be identified and device optimization can begin for these novel nanowire based transistors.

Overview

The manuscript is divided into 7 chapters including this introduction. The second Chapter gives a brief history in the field of nanowires, from the early '60s when they were still called whiskers or ribbons, until the early '90s when the first modern nanowire based devices were fabricated. A small section including the fabrication technique (Metal-Organic-Vapor-Phase-Epitaxy) of the InAs nanowires is also included - although this is a theoretical work - in order to provide a complete picture of the devices under study. Finally the last section of Chapter two gives a presentation of the current state-of-the-art both in terms of fabricated devices as well as simulation methods and techniques by various groups. The latest results in terms of high frequency characterization of nanowire transistors are discussed and the open issues like device contacting and their influence on device performance are pointed out. Various simulation approaches are presented and briefly explained, comparing them in terms of physical accuracy, simulation time and necessary resources.

In Chapter 3 we present the two different simulation approaches used in this work for the InAs nanowire transistor: the Monte Carlo and the hydrodynamic approach. In the first section we give a brief description of the semi-classical model. We derive the equation of motion for electrons and the most common scattering rates. Next we present the Boltzman Transport Equation (BTE) and show how it can be numerically solved via the Monte Carlo approach.

Then we move to the second simulation approach and we derive the equations of the hydrodynamic model from the higher order moments of the BTE. Finally we introduce the finite volume simulator used in this study and give an overview of the modeling and simulation procedure. Some advanced features of the framework like the Mixed-Mode, which allows the simulation of entire circuits are discussed, and some details on the numerical methods are given.

In Chapter 4 we present the Monte Carlo simulator used in this work. We give a detailed description of the simulation flow chart and of the various programs included in the simulation framework. In the next section of this chapter we present the modeling details for the simulated nanowire transistor and of course the simulation results. We compare the simulation results with the measured ones and after confirming the accuracy of our simulator we perform the high-frequency analysis.

Chapter 5 deals with the simulation of the same device using a deterministic approach, namely the hydrodynamic model. The measured output characteristic of the transistor is reproduced and the same high-frequency analysis as in the case of the Monte Carlo approach is performed. Two sensitivity analysis are performed in order to determine the influence of the doping profile and of the gate length on the transistor AC and DC characteristics. Finally the high-frequency analysis is repeated with the inclusion of various parasitic elements.

In Chapter 6 some applications of III/V nanowires in optoelectronics are discussed. The simulation of an InAs LED is shown and some design rules for InAs laser operation are presented.

Finally Chapter 7 contains the conclusions and outlook. The results of both methods are compared to each other. The good agreement between the simulation results obtained by the different approaches is highlighted and the main findings are summarized.

In the outlook of this work, we show how our simulation study represents only the beginning in what we believe to be the future for post CMOS circuits: the hybrid integration of Si and III/V semiconductor devices on a chip.

2 Background

2.1 Historical Perspective

The first reports on filamentary crystals growth – best known as whiskers, but also called ribbons, needles or rods date back to the mid and late '50s. To our knowledge the manuscript published by R.S. Eisner in 1955 [36] entitled “Tensile tests on silicon whiskers” represents the first publication in this new research area of crystal growth. Two years later Pearson *et al.* [37] manage to grow silicon whiskers of about 20 μm diameter by vapor deposition and publish a study about the deformation and fracture of these novel crystal structures, while Treuting *et al.* [38] analyze the orientation of the whiskers. The interest in the filamentary crystals keeps increasing and the first review paper by S. S. Brenner appears in Science [39] one year later, paper that summarizes all the growth techniques and experimental results available up to that date.

It is very interesting to note that in these early years of research all groups focused on the mechanical properties of the whiskers rather than their electrical or optical characteristics. Especially the maximum elastic strain showed intriguingly high experimental values when compared to bulk crystals. In the review paper [39] all measured whiskers displayed maximum elastic strain at least two to three orders of magnitude higher than the bulk annealed crystals, which leads the author, S.S. Brenner, to put a fundamental question: are the filamentary crystals so strong only due to their small dimensions or is the high elastic strain an intrinsic property of whiskers. No answer is given to this question and the author admits that further research is still necessary but some important experimental observations are presented. Especially the fact, that for whiskers with diameters larger than 25 μm the strength starts decreasing to values very close to bulk crystals, seems to indicate a link between size (diameter) and strength.

In the early '60s a lot of attention is given to growth mechanism of whiskers, most notably Greiner *et al.* in [40] and Wagner *et al.* [41]. The samples presented there were fabricated by vapor deposition: silicon and iodine are put together in a quartz tube that is heated in a furnace with a temperature gradient between 800 °C at one end to 1100 °C at the other end. Some specific impurities like nickel are added to the iodine (0.01%) and after about 10 minutes whisker growth can be observed.

Contemporary theories suggested that whisker growth is intermediated by a structural defect at the growth interface (Frank-Read mechanism [42]). A single axial screw dislocation can serve as nucleation site where the subsequent silicon layers will deposit, thus facilitating the whisker growth. This theory had however a serious drawback: it could not explain why the impurities added to iodine – like nickel, copper, manganese, or silver – facilitate whisker growth, acting as some kind of growth catalyst.

This leads Wagner and Ellis to propose a completely new growth scheme, in their seminal paper entitled “Vapor-Liquid-Solid mechanism of single crystal growth” [43], scheme in which the growth site is an impurity droplet in liquid phase rather than a structural defect. In Fig. 2.1 two silicon whiskers with diameters of 0.1 μm and 0.25 mm from the original paper [43] are reproduced, in both cases the catalyst droplet on the whisker tip is clearly visible. The Vapor-Liquid-Solid (VLS) growth mechanism is validated the same year by the study of Wagner *et al.* [44]. In this study [44] 15 different “needles” are grown with different impurities as catalyst. After growth the samples are subject of a detailed defect search by several methods. Not a single axial dislocation is found in any of the needles leading to the conclusion that contemporary theories of structural defect induced crystal growth had to be false and the VLS assumption correct.

The discovery of this new growth method (VLS technique) impels the research community offering for the first time the possibility of a controlled growth of whiskers. Over the next decade intense studies are carried out in order to understand whisker growth [45, 46], studies restricted not only to silicon. In [45] Bootsma *et al.* grow silicon whiskers from silane and germanium whiskers from germane using gold (Au) as seed particle.

For whisker growth of III-V compound semiconductors we can differentiate between studies published before the discovery of the VLS technique (1964),

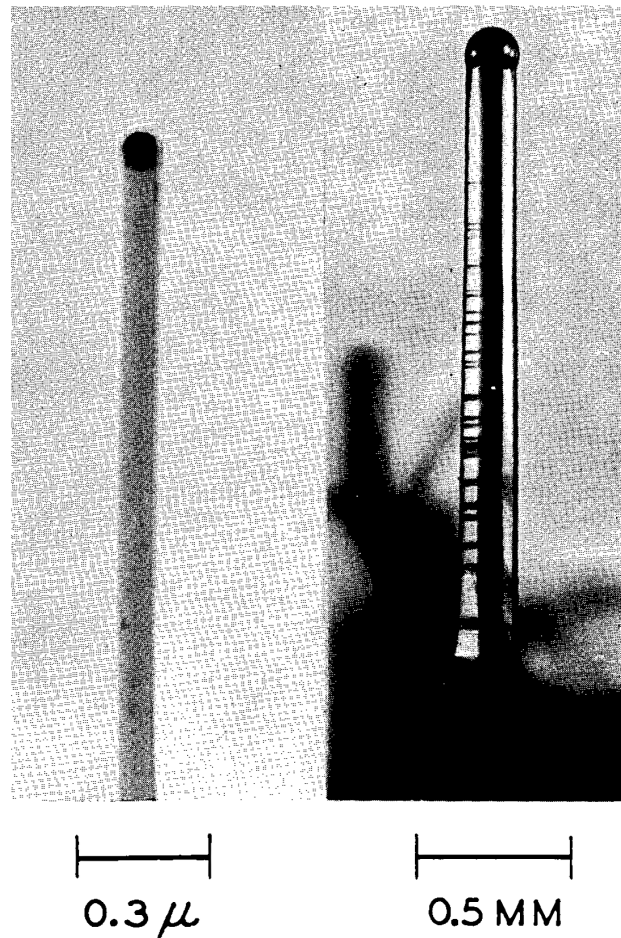


Figure 2.1: Silicon whiskers grown via the VLS method with different sizes: to the left a whisker with diameter of 100 nm and to the right a whisker with a diameter of around 0.25 mm. Figure reproduced from [43].

studies that analyze more the morphology and orientation of the whiskers and studies after 1964 where the accent is put on the growth mechanism. To our knowledge the first published study of III-V semiconductor whisker growth is attributed to Antell *et al.* [47] in 1959.

In this original work InAs, InP, GaAs and GaP whiskers are grown in a similar fashion to the early silicon whiskers [37]: vapor deposition at a temperature 100 °C to 300 °C below the melting point of the compounds. The vapor consists of As (P) and Indium (Ga) iodide or Indium (Ga) chloride. In another paper by Antell [48], in the following year, the role of iodine and chlorine as impurities in InAs and GaAs is investigated but only after the discovery of the VLS mechanism systematic studies of compound semiconductor whisker growth are carried out. Barns and Wellis [49] apply the newly discovered technique to grow GaAs

and GaP whiskers using Au, P and Ni as catalyst. They identify 3 distinct whisker topologies for GaAs: a single crystal hexagonal needle, a single crystal blade and twinned ribbon having the growth directions $\langle 111 \rangle$, $\langle 001 \rangle$ and $\langle 112 \rangle$ respectively. Cross sections of several μm and lengths ranging from a few tens of μm to a few mm are reported. Furthermore they tried to grow catalyst-free GaAs whiskers using Ga droplets as solvent, a revolutionary idea for that time. This method worked, whiskers grew only in those places where Ga droplets were present but all of them presented complex, irregular shapes. These were attributed to the small contact angle between the V-L phases, further evidence being the triangular shaped tips of the whiskers visible in TEM images. Addamiano *et al.* [50] independently manage to grow catalyst free GaAs whiskers from Ga droplets with similar morphologies like those presented by Barns *et al.* [49]. In [51] Addamiano manages to grow the first nanowire-like GaAs whiskers, which he calls “Coiled Crystals of Gallium Arsenide”.

A fundamental study on the oriented growth of III-V semiconductor whisker growth via the VLS method is published by Givargizov *et al.* [52]. Growth of GaAs, GaP, InAs and InGaAs on different substrates using gold droplets as catalyst was performed and the conditions for perpendicular growth to the substrate were identified. In fact these highly ordered perpendicular whiskers with sub-micron diameters and high aspect ratio represent the first reported semiconductor nanowires, in the modern acceptance of the term. In Fig. 2.2 and Fig. 2.3 GaAs and InAs whiskers are shown, both fabricated via the VLS method by Givargizov *et al.* [52].

Further pioneering work using the VLS growth mode is done by Kasahara *et al.* [53] where a new catalyst free method is presented, namely “thermal decomposition” of AsH_3 and $\text{Ga}(\text{CH}_3)_3$ to form GaAs whiskers. This is to our knowledge the first time when MOCVD is used to produce semiconductor whiskers. Noras *et al.* [54] grow spontaneous GaP whiskers from a GaP substrated covered with a thin nickel layer.

After these impressive results in the early ‘60s and ‘70s in the growth and characterization of semiconductor whiskers most research was abandoned even before specific applications could be developed. The main reason is the rapid development of the silicon transistor and the emerging integrated circuits. Nonetheless one application is worth mentioning: an application patent from 1965 describes

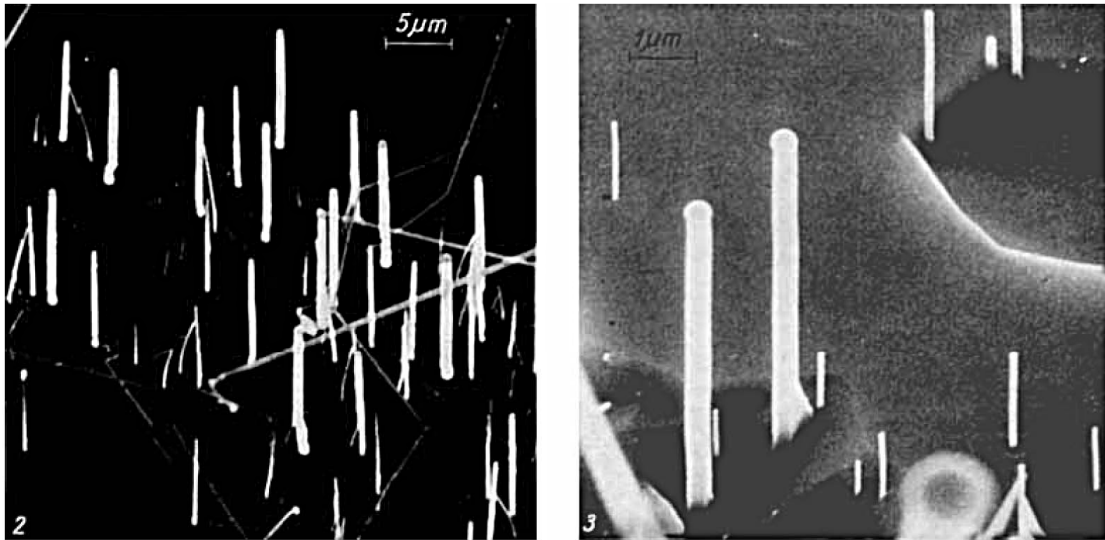


Figure 2.2: GaAs whiskers with high aspect ratio grown on GaAs substrate. Figure reproduced from [52].

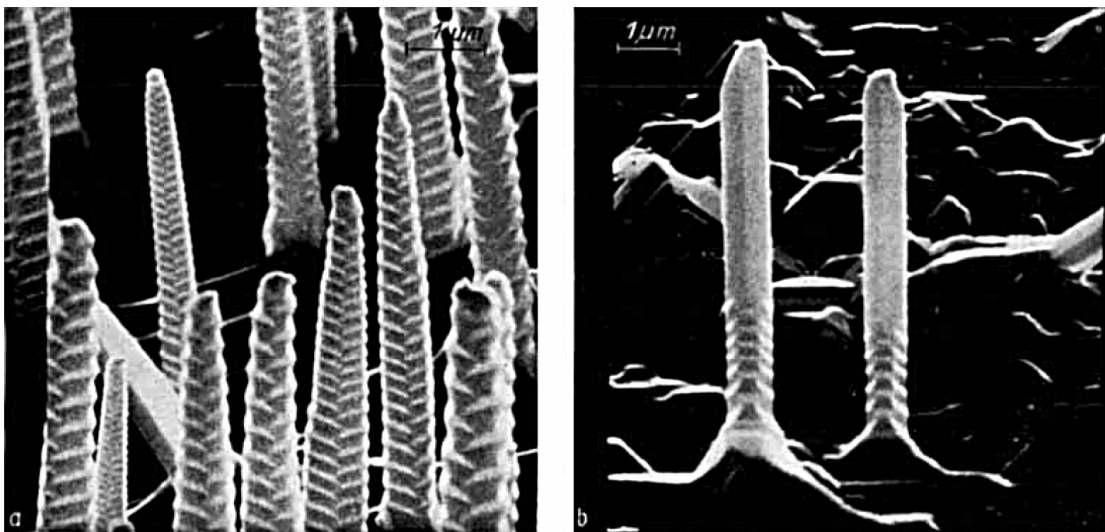


Figure 2.3: InAs whiskers grown on GaAs substrate at different temperature: (a) 800C and (b) initially 800 C followed by 700 C. Figure reproduced from [52].

the uses of a silicon whisker in a field effect device, a whisker transistor or a so-called “whistor” [55].

The interest in whiskers and nanowires reignited after two decades in the early '90s when it became clear than silicon technology cannot keep downscaling

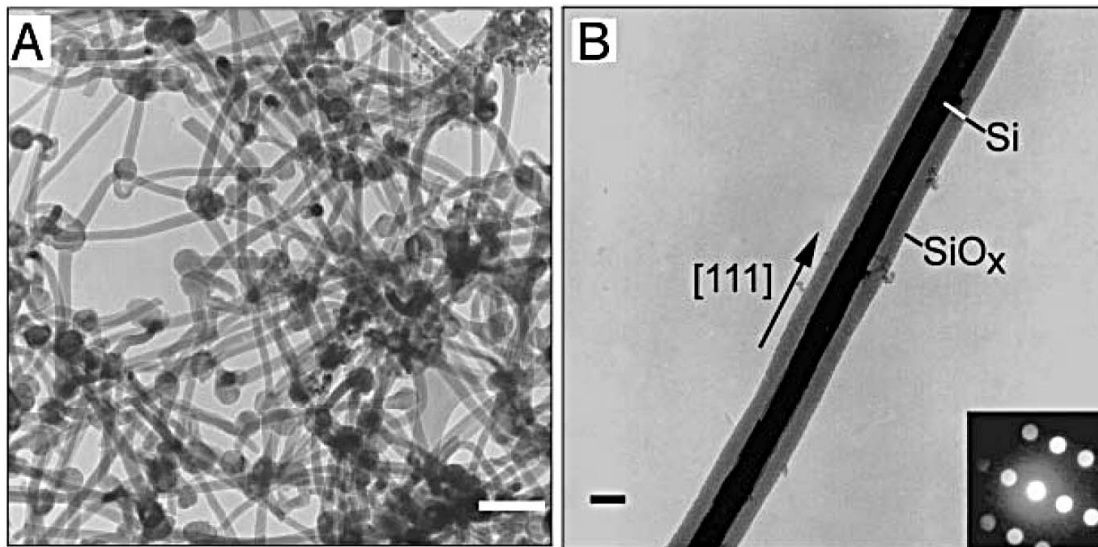


Figure 2.4: (a) TEM image of Si nanowires fabricated via laser ablation (b) Detail of single nanowire, scale bar is 10 nm. Figure reproduced from [57].

indefinitely. The work of Haraguchi *et al.* [56], where the first p-n junction made out of a semiconductor whiskers is presented and Morales *et al.* [57] who produced the first truly “nanowires” with diameters as small as 3 nm, generated a lot of attention. In Fig. 2.4 such nanowires grown by a laser ablation method are shown [57].

2.2 Fabrication Techniques

In this chapter a short presentation of the various fabrication methods used for III-V semiconductor nanowire growth will be given. Although the aim of this thesis is set on the modeling and simulation part rather than on the fabrication issues we consider that an overview of fabrication techniques is useful in order to have a complete picture of this current research topic. First a selection of the most common methods will be discussed and in the second part of this chapter the metal-organic vapor phase epitaxy (MOVPE) [21,24,58,59] technique will be treated in more detail since this is the method of choice for the fabrication of the state of the art InAs nanowire based devices.

There are two main methods by which nanowires can be grown in vapor phase: Chemical Vapor Deposition (CVD) [60,61] and Physical Vapor Deposition (PVD) [62] each of them having a variety of sub methods. In the CVD method

the layer deposition occurs through a chemical reaction between the precursors in gaseous form at the wafer surface, whereas in PVD the deposition takes place only via physical processes – evaporation of solid precursor and condensation of the vapor at the wafer surface.

As mentioned in the previous section the earliest III-V semiconductor whiskers [49,52] were grown via CVD using Au, Ni or other metals as catalysts in the VLS mode. The CVD technique has both advantages and disadvantages. In its favor we can mention the relative small cost of equipment and small operational and maintenance costs due to the fact that CVD can take place at atmospheric pressure (although low pressure CVD exists, is rather rare). Therefore no special requirements are necessary for the reaction chamber (expensive ultrahigh vacuum pump) nor does it require excessive amounts of electrical power (to maintain the ultrahigh vacuum). All these make CVD the economical method of choice for the deposition of thick uniform layers. As major disadvantage we can enumerate the safety issues: the precursors or the product gases are usually highly toxic, inflammable and sometimes also corrosive. This requires special care with the storage and disposal of the chemicals. High temperatures are also necessary during deposition (although the temperatures can be decreased if VLS growth mechanism is used) and not all metals can be deposited via CVD (TiAlN). From the various CVD sub methods we can find: atmospheric pressure CVD (APCVD), low pressure CVD (LPCVD), metal-organic CVD (MOCVD also known as MOVPE), laser-enhanced CVD (LACVD) and plasma-enhanced CVD (PECVD).

Opposite to CVD methods the PVD methods do not require toxic gases as precursors nor do they generate any toxic products, making them environmentally friendly. Virtually any material can be grown via PVD and atomic layer deposition is possible making it the method of choice for thin, accurate layer coating. However it requires more energy than CVD making it undesirable for large areas and the surface need to be rotated in order to have uniform layer thickness. The most frequent PVD variations are: molecular beam epitaxy (MBE), electron-beam evaporation (EBE) and discharge based deposition methods (sputtering or arc evaporation).

Our theoretical analysis of the to the nanowire transistor high frequency behavior is based on the device described in [24] grown by a variation of the CVD method,

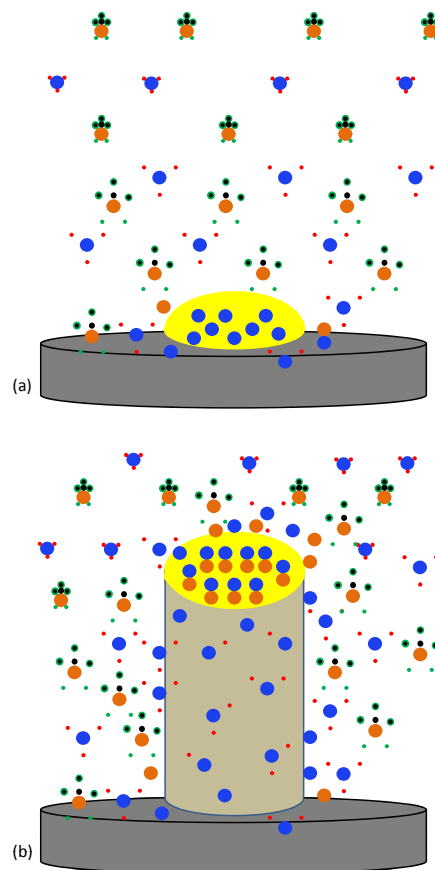


Figure 2.5: MOVPE growth of InAs Nanowire using gold as catalyst: (a) TMI decomposition (blue spheres) and formation of Au-In eutetic (b) Decomposition of TBA (orange spheres) in the Au-In eutetic and its incorporation at the L-S interface.

namely the MOVPE. The growth process is schematically shown in Fig. 2.5. In a first step Au nanoparticles that will serve as seed for the nanowire growth – with an average diameter of 30 nm – are deposited on an InAs substrate. Next the substrate is placed in the low pressure MOVPE system and annealed under a rich tertiarybutylarsin (TBA) atmosphere. The annealing temperature is at around 620 °C to obtain an Au-In eutectic liquid alloy whereas the TBA is necessary to prevent surface decomposition of the InAs substrate. Once the annealing step is over the temperature can be decreased to the actual growth temperature which is smaller, namely 400 °C. The III-V precursors are now introduced and the chemical reactions can take place; the group III precursor is the typical trimethylindium (TMI) and the group V precursor is the already mentioned TBA. TMI is already fully decomposed at the growth temperature

as can be seen in Fig. 2.5a and forms a supersaturated Au-In droplet at the substrate surface. TBA on the other hand is not fully decomposed yet, this process happens only when it reaches the V-L (vapor-liquid) interface of the Au-In droplet. After decomposition in the eutectic alloy the As atoms tend to diffuse from the V-L surface to the L-S (liquid-solid) interface since As solubility is very poor in Au-In eutectic [63]. At the L-S interface As atoms bind with In atoms from the supersaturated liquid Au-In alloy and a InAs is formed, this step is shown in Fig. 2.5b. It was subject of long scientific debate in the early times of the VLS growth mode, which of the two mechanisms dominates the growth rate: thermal decomposition of the precursors at V-L interface (as stated by Bootsma *et al.* [45]) or the L-S interface reaction. Givargizov [46] showed in his rigorous study that this later rate is the growth controlling step. The wire starts and continues to grow vertically following the process described as long as the growth conditions are met, which are mainly summarized in [43] and [45,46].

We will mention just the basic prerequisites: the catalyst needs to form a eutectic with one of the materials and it should possess as low as possible melting temperature. From the thermodynamical point of view, the reactions should be of course possible but not favorable, so that the catalyst may play its role in precursor decomposition and the subsequent diffusion/incorporation at the L-S interface. Furthermore the Au-In eutectic must be supersaturated especially at the early stage of nanowire growth, so that the wire can elevate from the substrate and start growing.

The InAs nanowire samples fabricated via the technique described above have diameters ranging from 30 to 60 nm (probably due to Au nanoparticle clustering) and lengths varying from 1 to 5 μm . After growing the NWs, patterning of NW field effect transistors is carried out. In the first step the NW are placed onto an insulating GaAs substrate covered with a 150 nm of silicon nitride (SiN_x) layer for better insulation. Titanium/gold (TiAu) is used for the drain and source electrodes, which are patterned using a standard electron beam lithography process and deposited via thermal evaporation.

A 30 nm thick SiN_x layer is deposited over the entire structure as gate dielectric. The gate electrode is made of Ti/Au and covers the gate dielectric forming thus a wrap gate. In Fig. 2.6 a SEM picture of the completed device is shown.

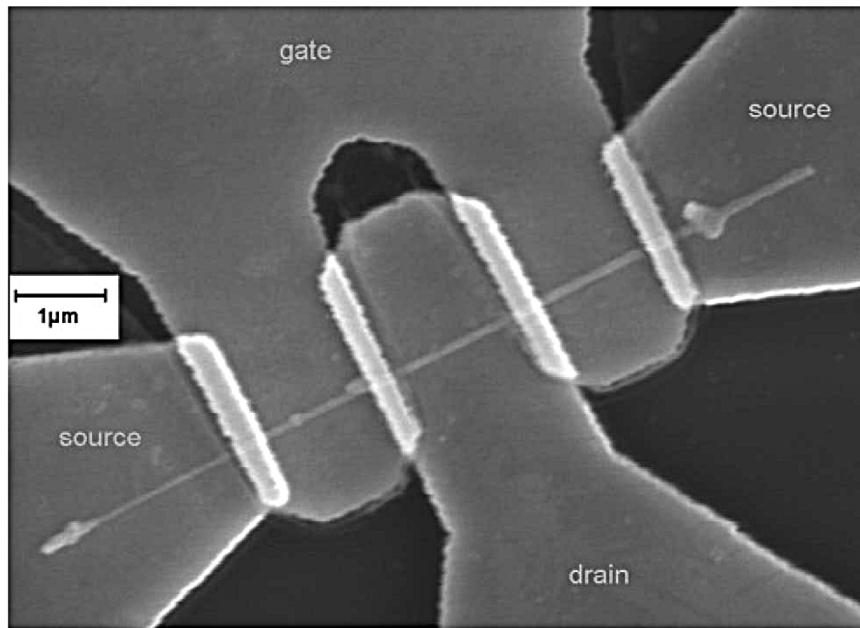


Figure 2.6: SEM image of the InAs nanowire transistor. Image reproduced from [24].

2.3 Demonstrated Devices

As the first state of the art nanowire synthesis and nanowire device examples we could mention the work of Haraguchi *et al.* [56] and that of Morales *et al.* [57]. In [56] Haraguchi presents the first GaAs nanowire light emitting diode (LED) based on a radial p-n junction where light emission due to spontaneous radiative recombination occurs at room temperature. Morales *et al.* [57] introduce a novel laser ablation technique for nanowire synthesis which delivers semiconductor nanowires with diameters smaller than 10 nm and aspect ratios greater than 1000. State of the art devices based on semiconductor nanowires are presented by the Lieber group in the following years [11, 64, 65]. In [64] a single InP nanowire photodetector is demonstrated whereas in [11] nanowire super-lattices are fabricated and a InP nanowire light emitting diode (LED) is presented. In [65] heterojunctions using core-shell nanowires are fabricated and a nanowire transistor is demonstrated.

These early promising results generated a lot of attention and for the last decade the number of nanowire research groups and publications has constantly increased [66]. Next we will give a very short presentation of what we believe to be the most important NW device publications.

Making use of the quantum confinement effects inherent for nanowires, especially for those with small effective mass like InAs, Björk *et al.* [67] created the first nanowire resonant tunneling diode by growing 5 nm thick InP barriers along the axial direction of an InAs nanowire. Thus an InAs quantum well (QW) between two potential barriers was obtained, validated by the IV measurements where a typical negative differential conductance (NDC) was observed at energies matching the first discrete eigen-energy level of the QW. The typical figure of merit (FOM) for such devices – the peak to valley current ratio (PVR) – was determined to be 50 and current densities up to 0.1 A/cm^2 were measured at 4 K, both excellent values for such an early proof of concept. Thelander *et al.* [68] from the same research group at Lund University managed to modify the resonant tunneling diode structure into a single electron transistor (SET) by adding a back gate contact and optimizing the InAs dot length and wire diameter. The IV characteristic of the SET displayed the typical Coulomb blockade that can be lifted with an appropriate gate bias voltage. Preliminary calculations indicated that for a dot length of 15 nm and a wire diameter of around 35 nm the confining potential is around 20 meV; if this could be further increased room temperature operation may become possible.

One year later Doh *et al.* [69] demonstrated superconductivity in InAs nanowires placed between Al superconductor electrodes at temperatures below of 1 °K. Furthermore the superconductivity in the device could be tuned via a back gate electrode which modulates the electron density in the nanowire. For a sufficient high negative gate voltage (-70 V) the superconductivity vanishes and a finite voltage drop across the nanowire could be measured. For the opposite case when a switching from semiconducting to superconducting transport is desired a smaller positive voltage is required [69].

Wallentin *et al.* [70] also from Lund implemented the Esaki tunnel diode on a single III-V semiconductor nanowire. An axial InP – GaAs heterojunction nanowire was grown using the MOCVD technique, a rather unusual material choice, which is impossible for thin film fabrication due to the great lattice mismatch (3.8%) of the two semiconductors. But as mentioned in the first chapter nanowires have unique mechanical properties, one of them is the ability to distribute uniformly the mechanical stress induced by lattice mismatch without cracking if the nanowire diameter is small enough [70]. The FOMs, as can be

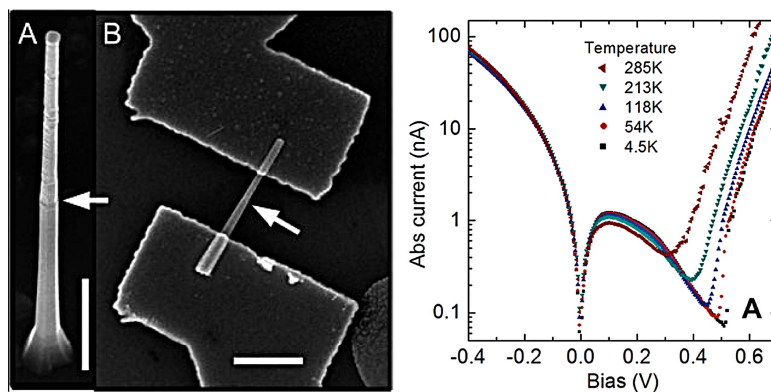


Figure 2.7: (a) InP-GaAs heterojunction nanowire as-grown (scale bar $0.5 \mu\text{m}$) (b) Same nanowire contacted as a tunnel diode (scale bar $1 \mu\text{m}$) (c) Measured IV characteristic at various temperatures, negative differential resistance (NDR) is clearly visible over the entire temperature range. Figure reproduced from [70].

seen in Fig. 2.7, for this device were very promising considering that it was not optimized: a peak to valley ratio of 8.2 at room temperature and 27 at $4.2 \text{ }^\circ\text{K}$.

Finally in recent years the hybrid Si-InAs nanowire tunneling diodes have generated great interest [71]. Bessire *et al.* [71] report on diodes with PVR of 2.4 at room temperature and claim that the band to band tunneling mechanism is trap assisted. Although the ratio of 2.4 is not truly state of the art FOM for such a device, it must be mentioned that no optimization was carried out. Furthermore it serves as proof of concept for the integration of InAs nanowires on standard Si substrates, a remarkable progress in fabrication technology, otherwise impossible for thin film growth due to the huge lattice mismatch of nearly 12% between the two semiconductors. This opens many new perspectives for the future hybrid integrated Si/InAs device, one of the next logical steps being the addition of a gate terminal [72] transforming the tunnel diode into a transistor like gated structure with high integration densities.

Beside these state of the art devices and fundamental proofs of concept nanowire devices have evolved also in another, more conventional direction, the nanowire based transistor. Since its invention in 1947 [73] the transistor has revolutionized the fields of electronics being responsible for most of the technological breakthroughs in the last 50 years. Since scaling has become an issue in the first decade of this century, a continuous search for alternatives is under way.

One promising solution of this problem is the use of semiconductor nanowires as already mentioned in Chapter 1. Thus the well-established three terminal device – the transistor – remains unchanged in its working principle, only the fabrication and device geometry undergo a radical modification.

The operation of the traditional planar metal oxide semiconductor field effect transistor (MOSFET) is fairly simple. A control terminal – the gate – accumulates or depletes charges under the gate oxide, depending on the applied voltage, like in a plate capacitor after the well-known formula for the charge density in [Charge/cm²], $Q = C_{ox} \cdot V$, ($C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$). When an appropriate gate bias is placed (this depends on the type of substrate doping, metal workfunction, etc.) a conducting channel at the oxide/semiconductor can build up and electrons (or holes) can flow between the other two terminals – source and drain, if the drain electrode is also favorably biased. In a normal n-type MOSFET the drain is biased on a positive voltage and electrons are attracted. With this additional lateral field (source-drain) the potential under the gate oxide cannot be regarded as constant anymore and it is better to rewrite the charge equation with a position dependent potential: $Q(x) = C \cdot V(x)$. The current density [Amp/cm] is nothing else than charge moving under an external field and can be written as $J = Q \cdot v$, with v the drift velocity defined as $v = \mu \cdot E$. As we know the electric field is the first derivative of the voltage $E = -\frac{dV}{dx}$. If we put all these equations together we obtain a first order differential equation with separable variables for the position dependent drain current I_D (where $I_D = J \cdot W$):

$$I_D = WC_{ox}[V_{GS} - V(x)]\mu \frac{dV}{dx} \quad (2.3.1)$$

This equation can be easily solved by bringing the dx on the left hand side and integrating on both sides after the two variables – position and voltage. The current equation of the MOSFET has then the form:

$$I_D = \frac{1}{2}\mu C_{ox} \frac{W}{L} [2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2] \quad (2.3.2)$$

For very small V_{DS} the quadratic term can be neglected and we observe linear dependence of the current on the drain voltage, the so called triode region:

$$I_{D,lin} = \mu C_{ox} \frac{W}{L} [(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}] \quad (2.3.3)$$

On the other hand for $V_{DS} \geq V_{GS} - V_{TH}$ the equation simplifies to:

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (2.3.4)$$

In this regime the current is theoretically independent of the drain source voltage, it saturates. The point where the current saturates is called pinch-off point and it is caused by the touching of the two depletion regions at the gate and drain junctions.

In case of the nanowire transistors we can already notice some essential differences. First and most important the gate is cylindrical for improved electrostatic control, thus the simple equation of the parallel plate capacitor is no longer valid. The first mathematical formulation of the gate capacitance for a cylindrical nanowire channel is given by Miyano *et al.* [74] and others followed [75]. We will treat this aspect in the chapters dedicated to nanowire transistor modeling. Furthermore saturation does not necessarily occur due to pinch off but mostly due to velocity saturation; many nanowire transistors don't have complementary doping for the contacts and for the channel. Advanced physical effects (hot carrier effects, trap states) are also neglected in this first approximation of the current: they will be also discussed in the next chapters and their effect on the device performance analyzed.

InAs NW transistors have been first demonstrated by Bryllert *et al.* [23] and many others afterward followed [21,22,25]. The single crystal InAs nanowire transistor presented by Dayeh *et al.* in [22] exhibits very good transport properties with a peak value for the electron mobility of about 7000 cm²/Vs at an electric field of 1.5 kV/cm.

As promising as these values may sound for high speed low power application, only very few high frequency measurements have been performed on InAs NW transistors. The only exceptions are Blekker *et al.* [24] and Egard *et al.* [25] from Lund.

In Fig. 2.8a the schematic of such a transistor is shown whereas in Fig. 2.8b the output characteristic is shown [24]. For this particular transistor the gate length

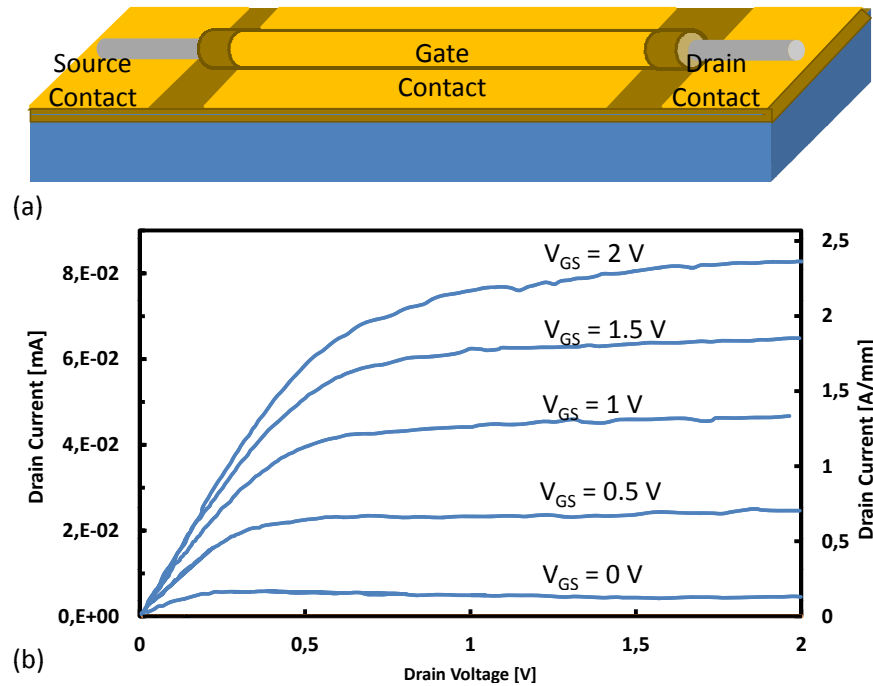


Figure 2.8: (a) Schematic representation of the InAs nw FET from [24] (b) Measured I-V output characteristic for V_{GS} from 0 to 2 V.

is $L_G = 1.4\ \mu\text{m}$ and the NW radius, $r_{nw} = 17.5\ \text{nm}$. From Fig. 5.1b it can be seen that very good saturation currents are achieved, at 1 V gate voltage (V_G) and 1 V drain-source voltage (V_{DS}) for example a current of more than 1 A/mm is measured. The current increases even further at higher gate voltages as expected from a classical FET. Concerning the transfer characteristic of the transistor, a hysteresis is present which indicates some kind of electron trapping process [24]. This may be attributed to surface defect states at the InAs interface, an issue that has been extensively studied for the surface of bulk InAs [76,77].

For InAs nanostructures however, there are very few studies [78,79] on this topic. The role of this defect states will be pointed out in the next section. The figures of merit for this device are a unity current gain cutoff frequency f_T of 7.5 GHz, a maximum oscillation frequency, f_{max} , of 15 GHz and a maximum stable gain, MSG, higher than 30 dB.

A slightly different approach is presented in [25], namely a vertical InAs nanowire – wrap gate transistor array is characterized. Although the fabrication process is quite different the results of the high frequency measurement are similar: f_T of 7 GHz, and f_{max} of 20 GHz.

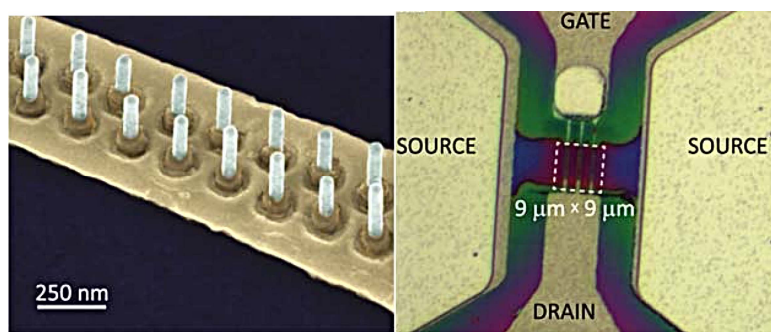


Figure 2.9: (a) Detail of nanowire array with optimized gate finger contacts (b) Picture of the complete NW array cell. Figure reproduced from [26].

Both groups acknowledge however that the main difficulty in an accurate high frequency characterization lies in the presence of parasitic elements (pad capacitances) in the measurement setup, elements which tend to become dominant and to severely deteriorate the high frequency performance. Therefore it is not clear which have the intrinsic properties of the InAs NWs, in terms of a unity current gain cutoff frequency, maximum oscillation frequency or maximum stable gain.

In the very recent papers of Persson *et al.* [80] and especially Johansson *et al.* [26] significantly higher values for f_T and f_{max} have been obtained: 103 GHz and 155 GHz respectively, in [26]. These state-of-art values have been obtained mainly by reducing the parasitic pad capacitances using finger gate contacts, confirming the importance of proper contacting and giving a hint about its impact on device performance. A picture of such an finger gate transistor array is shown in Fig. 2.9.

2.4 State of the Art Simulation Approaches

As transistor size keeps scaling down and the physical processes involved in device operation become more complex, the modeling and simulation tools are gaining more attention, especially in industry. Computer simulations can provide valuable insights in the device physics during operations, when direct measurements can be difficult to perform or sometimes even impossible making them a valuable tool for research. Understanding the underlying physical processes is one of the main motivations for the development of new, state of the art simulation tools.

Another research application for computer simulations is the design and optimization of novel structures, possibly CMOS replacements. The use of such tools has also increased in industry because simulations can speed up significantly the learning curve for a new technology. Thus not only money can be saved, since entire generations of costly prototypes are not needed anymore, but more important a lot of time – simulations take far less than actual device fabrication. All these translate in a reduction of the time to market for the new products, generating profit and consolidating leading position in the market.

There are several established simulation methods, the fully quantum mechanical simulations, like Non-Equilibrium Green's Function (NEGF), are the most rigorous since they take the wave nature of electrons into consideration [27–29]. Ren *et al.* describe in [27] a practical implementation of NEGF formalism into an easy-to-use computer program, nanoMOS 2.5. The idea behind the NEGF method is to find the response of a nano-system to an external perturbation (external bias for example) and to calculate quantities such as charge and current densities. The direct approach would be to solve Schrödinger's equation including the perturbation term, but this approach is usually very complicated and time consuming. In the NEGF formalism we do not need to solve the entire eigenvalue problem, it suffices to compute the Green's function and from this special function to derive all quantities of interest. These quantities are usually the wavefunctions in the contacts and in the device, and from these the current density and the electrical current can be computed. However much more can be calculated once having the Green's function: the spectral function, for example gives all the solution of the Schrödinger's equation for the specific device and the density of states (DOS) for electrons. This simplifies the problem considerably; moreover for some special cases the Green's function is already known speeding the computation even more. Scattering can be also included in the NEGF formalism but at the cost of extra computational resources [28].

Using the NEGF approach Wang *et al.* [28] simulate silicon nanowires with rectangular, triangular and circular cross sections and gate lengths of 10 nm. They perform two types of NEGF simulations: first considering ballistic transport and then with a semi-empirical model for elastic scattering (Büttiker probes) in order to determine the influence of surface roughness (SR) scattering and ionized impurity (II) scattering. A more rigorous treatment of SR is given in

Buran *et al.* [81] where it is shown that surface roughness may produce a positive shift of the threshold voltage for low source drain voltages.

Another simulation alternative is the so called semi-classical transport model, which implies solving a master transport equation, the Boltzmann transport equation (BTE). Although not a fully quantum mechanically procedure, it is faster than NEGF and can take into account more particles and more scattering mechanism [82]. Additionally for nanowire transistor with gate lengths exceeding 10 nm, where direct source to drain tunneling is highly improbable, the BTE delivers accurate results, comparable with NEGF method [83].

Two main approaches have been developed for the semi-classical transport model: the deterministic and the stochastic solution of the BTE. Deterministic solutions usually imply some simplifications or approximations whereas stochastic solutions obtained via the Monte Carlo algorithm are exact solutions (subject only to statistical noise). Jin *et al.* [83] have performed a scaling study on silicon nanowire transistors using the BTE under the Relaxation Time Approximation (RTA) and studied the influence of geometrical parameters on the ON-current and subthreshold slope (SS). Furthermore a comparison of their RTA results with a NEGF approach is given, proving that this approximation has not reduced the accuracy of the simulation results. Lenzi *et al.* [30] provide a comparison study between deterministic and stochastic (Monte Carlo) solution of the BTE for nanowire transistors. They obtain excellent agreement in terms of electron distribution and drift velocity profile along the nanowire between the two different approaches but this is more due to the favorable choice of nanowire diameter than to the equivalence of analytical and stochastic method. For very small diameters (3 nm) the effect of quantum confinement reduces the phase space dimensionality, only a few subbands can fit in the volume [30], enabling a fast deterministic solution of the BTE. This is no longer the case for nanowire transistors with diameters in the decananometer range (e.g. 50 nm) where the stochastic solution is the only viable approach.

State of the art Monte Carlo simulations for InAs nanowires are presented by Sadi *et al.* [31] and David *et al.* [84]. In [31] an electro-thermal simulation framework is described, coupling the heat diffusion equation to a state of the art Monte Carlo simulator in order to get an estimation of the power dissipation for the next generation nanowire transistors. David *et al.* [84] compare silicon

nanowire transistors with III/V nanowire transistors using a Monte Carlo approach. The results of their simulations indicate InAs and InSb as the most promising materials for low voltage high speed applications.

The Cellular Monte Carlo (CMC) approach presented by S.M. Goodnick and M. Saraniti [82] is a slight variation of the Ensemble Monte Carlo (EMC) method in order to achieve faster simulation times. This method was validated in several simulation studies [85–88] reproducing the DC characteristic of measured devices highly accurate. The simulator is able to perform a complete, self consistent, high frequency analysis of novel semiconductor devices, both small signal [85] and large signal [86–88].

Finally the last simulation alternative is based on a drift-diffusion approach, method that has served the semiconductor industry for more than fifty years [89]. This method is used to fit measured nanowire output and transfer characteristics in [33] and [32] delivering good results. The speed and versatility make this method particularly appealing, execution times for full 3D simulations taking hours rather than days. It can be also modified to include quantum corrections, like the density gradient correction model in the simulation study of FinFETs by Li *et al.* [90]. In that simulation study complex gate geometries are presented and the difference in electrical characteristics between the gate all around (GAA) and the omega shaped gate nanowire transistor is clarified.

Furthermore the DD approach can be extended to include higher moments of the BTE leading to the hydrodynamic approach, which also takes the energy balance into consideration. Nayfeh *et al.* [91] present such a simulation model in their investigation of Si nanowire transistors. Another advantage of the modified DD approach is the possibility of including charge trapping and detrapping effects. Because these phenomena take place at a time scale completely different from scattering events they cannot be practically included in Monte Carlo approaches (only if the simulated time is extremely high making thus the execution time unpractical). Interface trap states and charges are however critical for nanowire transistors making thus the modified DD (hydrodynamic model) indispensable for modeling and predicting the behavior of future generation transistors. Hang *et al.* [92] include in their simulation trapped charges and fit very well the measured transfer curves whereas Dayeh *et al.* [93] include the entire trapping process in their simulation, succeeding in the simulation of transient curves.

3 Simulation Methods

3.1 The Semi Classical Model

In this chapter we will present the simulation methods used for the modeling and simulation of an InAs nanowire FET. In the first part we will discuss the semi-classical transport model for semiconductors in brief and link it to the Boltzman Transport Equation (BTE). Then we will show how the exact solution of the BTE can be found via the Monte Carlo method and finally we will present some details of the MC framework used in this study. The second part of this chapter deals with the hydrodynamic model used in the Sentaurus Device, a finite volume state-of-the-art device simulator. The equations of the hydrodynamic model will be derived from the higher moments of the BTE and some other advanced models - like velocity saturation and interface trap states - will be introduced. In the last part the typical command file of a Sentaurus simulation will be discussed and a brief insight in the numerical methods used for solving the PDEs will be given.

3.1.1 Quantum Mechanical Fundamentals

From the quantum mechanical point of view the electron transport in semiconductors can be interpreted as waves emitted from a contact and propagating through a periodic lattice. The governing equation of motion is the time dependent Schrödinger equation (a derivation of the Schrödinger equation can be found elsewhere [94]):

$$i\hbar \frac{\partial \Psi(r, t)}{\partial t} = -\frac{\hbar^2}{2m_0} \nabla^2 \Psi(r, t) + [E_{C0}(r) + U_C(r) + U_s(r, t)] \Psi(r, t) \quad (3.1.1)$$

The $\Psi(r, t)$ is known as the wavefunction and its modulus square gives the probability density of finding an electron at a given position. On the right hand side three different potential terms are listed: the first - E_{c0} - is the built in or applied potential, the second one denotes the crystal potential and the last one is the scattering potential U_s . The crystal potential accounts for the interaction of the crystal (atoms) with the incoming electron wave whereas the scattering potential describes the collisions with impurities, with other carriers or with lattice vibrations that might perturb the electron trajectory.

The exact solution of equation 3.1.1 is quite difficult to find and is subject to NEGF methods as described in the previous chapter [27–29]. However we can make some assumptions and get an approximate solution of equation 3.1.1; this is what the semi classical model is about.

For standard devices the applied or built in potential E_{c0} varies only very slow compared to the electron wavelength so that quantum mechanical effects such as reflections or tunneling do not occur. Under these conditions one may approximate the electron as a particle that is subject to Newton's law of motion, so classical mechanics apply. The crystal potential is a fast varying potential (comparable with the electron wavelength) but we will show how its influence can be reduced to only one parameter, m^* , the so-called effective mass. Finally the scattering term is left; since scattering is a fast event involving potentials comparable with electron wavelength it is the only term that must be treated quantum mechanically. We will show in the next paragraphs how some of the most frequent scattering rates can be derived.

We can start with the solution of equation 3.1.1 only in the presence of E_{c0} , the slowly varying applied potential and for simplicity we shall consider only the one dimensional case. It can be shown [94] that the solution of the Schrödinger equation must be of the form:

$$\psi(x, t) = \psi(x)e^{-iEt/\hbar} = \psi(x)e^{-i\omega t} \quad (3.1.2)$$

If we plug equation 3.1.2 in the Schrödinger equation(3.1.1) we get the following time independent partial differential equation [95]:

$$\frac{d\psi}{dx^2} + k^2\psi = 0 \quad (3.1.3)$$

with,

$$k^2 = \frac{2m_0}{\hbar^2} [E - E_{C0}(x)] \quad (3.1.4)$$

We can now distinguish between different solutions of 3.1.3 depending if the wave vector square (k^2) is smaller or greater than 0.

For the simplest example we can choose $E_{c0} = 0$ and hence $k^2 > 0$; with this ansatz the wave function has the solutions:

$$\psi(x, t) = \psi(x)e^{-iEt/\hbar} = \psi(x)e^{-i\omega t} \quad (3.1.5)$$

and furthermore we see from equation 3.1.4 that:

$$\hbar k = \sqrt{2m_0 E} \quad (3.1.6)$$

or

$$E(k) = \frac{\hbar^2 k^2}{2m_0} \quad (3.1.7)$$

We know that $\hbar k$ can be interpreted as the momentum of the electron [96] hence equation 3.1.7 can be rewritten as:

$$E = \frac{p^2}{2m_0} \quad (3.1.8)$$

obtaining the same relation between the energy and momentum of the free electron just as in classical mechanics. Summarizing the complete solution for the time dependent wave equation in 3.1.1 we get:

$$\psi(x, t) = a_k e^{i(\pm kx - \omega t)} \quad (3.1.9)$$

The equation above describes a wave traveling in positive (or negative) x -direction and the product $\Psi^* \Psi$ represents the probability of finding the electron at a specific x -coordinate. We see however that there is a constant probability of finding the electron at any point on the x -axis. In order to define a particle at x_0 with a momentum $\hbar k_0$ we must build a linear superposition of the wave-functions, we construct a so-called wave packet. As shown elsewhere [94, 95]

all solution of the Schrödinger equation form an orthonormal basis, so we can write:

$$\Psi(x, t) = \int_{-\infty}^{+\infty} a(k - k_0) e^{ik(x-x_0)} e^{-i\omega(k)t} dk \quad (3.1.10)$$

The term $a(k - k_0)$ ensures that the wave packet has a large amplitude only in the proximity of k_0 whereas for the time $t = 0$ and for $x = x_0$ all the wave are in phase and add constructively. For $x \gg x_0$ the waves oscillate rapidly and destructive interference takes place resulting in small amplitudes of the wave packet. We can compare equation 3.1.9 and 3.1.10: the first solution represents a plane wave with sharp momentum (k_0) but undefined position in contrast to the wave packet, centered near x_0 , but with an uncertainty in the momentum $\hbar\Delta k$ since we need to sum over many plane waves with different momentum. This is nothing else than Heisenbergs uncertainty principle; there are many other formulations and for a more detailed derivation one can see [94,95].

Since for each of the plane waves forming the packet we can define a different phase velocity $v_p = \omega(k)/k$, it is more useful to introduce another velocity, the group velocity v_g when describing the wave packet dynamics. This is the velocity at which the center of the wave packet, at $k = k_0$ where constructive interference occurs, is traveling [95]:

$$v_g(k_0) = \left. \frac{d\omega(k)}{dk} \right|_{k=k_0} = \left. \frac{1}{\hbar} \frac{dE(k)}{dk} \right|_{k=k_0} \quad (3.1.11)$$

From the equation 3.1.11 we see that the group velocity of our wave packet is given by the ratio of its momentum and mass, in good agreement with classical mechanics.

The main message from the above derivations is that when the applied potentials vary very slowly we can treat the electron waves as classical particles subjects to Newton's classical mechanics.

Let us now consider the case of an electron wave confined in a quantum well of width W , due to a large trapping potential E_{c02} . It can be shown [95] that the solution of 3.1.1 must have the form:

$$\psi(x) = a_k \sin(k_n x) \quad (3.1.12)$$

$$k_n = \frac{n\pi}{W} \quad (3.1.13)$$

If we introduce the wave number k in the energy dispersion relationship 3.1.7 we obtain that only discrete energy levels are allowed, or in other words the eigen-energies are quantized, a phenomenon that has no equivalence in classical mechanics.

As a last case we can examine the following scenario: an electron wave traveling through a constant potential E_{C01} and hitting a potential step E_{C02} . From classical mechanics we would expect the electron to pass the potential step without reflection if it has an energy greater than the potential step. This is however not the case, from [95] we obtain the solutions of 3.1.1 as:

$$\psi(x) = e^{ik_1 x} + r e^{-ik_1 x} \quad x < 0 \quad (3.1.14)$$

and

$$\psi(x) = t e^{-ik_2 x} \quad x > 0 \quad (3.1.15)$$

with

$$k_1 = \frac{\sqrt{2m_0(E - E_{C01})}}{\hbar} \quad (3.1.16)$$

and

$$k_2 = \frac{\sqrt{2m_0(E - E_{C02})}}{\hbar} \quad (3.1.17)$$

From equation 3.1.14 and 3.1.15 it becomes obvious that there is a non-zero reflected wave even at energies higher than E_{C02} , a purely quantum mechanical effect.

The last two examples point out that in the case of a rapid changing potentials or abrupt potential steps (in the order of the electron wavelength) the quantum nature of the electron waves needs to be taken into account, otherwise important quantum effects may be omitted.

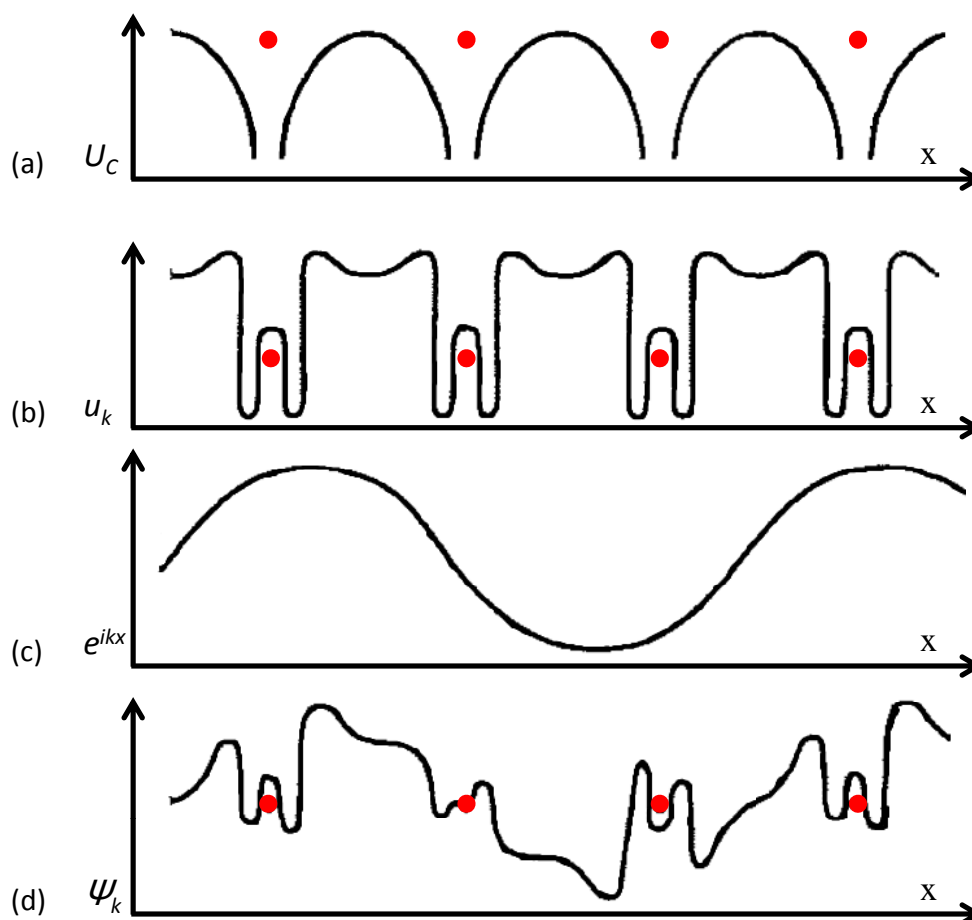


Figure 3.1: (a) Crystal potential (b) Bloch function with lattice periodicity (c) Plane wave (d) Bloch wave. Figure redrawn from [95].

3.1.2 Electrons in periodic lattice

The question how can electrons propagate in metals or semiconductors without being deviated by the attractive potential of the nuclei concerned physicist for a long time. The problem translates mathematically in solving Schrödinger's equation in the presence of the lattice potential U_c :

$$\left[-\frac{\hbar^2}{2m_0} \frac{d^2}{dx^2} + U_c(x) \right] \psi(x) = E\psi(x) \quad (3.1.18)$$

Felix Bloch [97] was the first to show by direct Fourier analysis that the electron plane waves are only diffracted by a periodic modulation, the periodicity being directly proportional to the lattice constant, a_0 . These solutions of the

Schrödinger's equation in the presence of a periodic lattice potential are called Bloch waves and can be written as [95,97]:

$$\psi_k = u_k e^{ikx} \quad (3.1.19)$$

with

$$u_k(x + a) = u_k(x) \quad (3.1.20)$$

A detailed derivation can be found elsewhere, here we simply plot the Bloch waves and their components as one can in Fig. 3.1. First, in Fig. 3.1a, the periodic crystal potential is depicted followed by the two components of the Bloch waves in Fig. 3.1b and 3.1c: the function u_k with the lattice periodicity and the plane wave component e^{ikx} . Finally the product of the two is illustrated in Fig. 3.1d.

If we introduce 3.1.19 in equation 3.1.18 we obtain a partial differential equation which can be solved for different values of k , the wave vector. For a fixed value of k ($k = k_1$) we get an infinite set of eigenvalues $E_n(k_1)$ with $n = 1, 2, 3$ etc. In the opposite case we can compute the first eigen-energy for various values of k and plot $E_1(k), E_2(k), E_n(k)$. Because of the periodic boundary conditions in 3.1.20 the energy dispersion for each eigenvalue will be continuous for the different k vectors. What we obtain are energy bands linked to each eigenvalue and bandgaps, energy intervals that cannot be reached by any k value. Due to the periodicity of the lattice (a_0) the energy bands will also be periodical and it suffices to compute them in the first period, usually centered around $k = 0$, the reduced (Brillouin) zone.

For silicon, III-V semiconductors, and other frequent semiconductors the entire band structure is well known both from measurements and calculations [94,98]. It is used in state of the art simulations like full band Monte Carlo simulations [82, 85–88], but this will be discussed in more detail in the next chapters.

In most cases the band structure is expanded into a Taylor series and the electrons (holes) are assumed to be near the band minimum. If the band minimum is located at $k = 0$ we can further simplify the expression since the first derivative vanishes and we obtain:

$$E(k) = E(0) + \frac{\hbar^2 k^2}{2m^*} \quad (3.1.21)$$

with m^* defined as,

$$\frac{1}{m^*} = \frac{1}{\hbar^2} \frac{\partial^2 E(k)}{\partial k^2} \quad (3.1.22)$$

One can see that if we substitute the second derivative of the energy after k , the wave vector, with $1/m^*$ we obtain an energy dispersion relationship identical with that of free electrons. The term m^* is called the “effective mass” and reflects the influence of the crystal potential on the conduction electrons. It only modifies the curvature of the $E(k)$ and in the most basic models is the only parameter that accounts for the crystal potential. Equation 3.1.22 describes a parabolic energy dispersion with spherical surfaces of equal energy (energy iso-surfaces), hence we will call such bands spherical parabolic bands.

3.1.3 Band Structure

We can summarize the results until now: we have shown how the built-in potential and the crystal potential separately affect the electron motion. The two contributions can be inserted in Schrödinger's equation to give:

$$\left[-\frac{\hbar^2}{2m_0} \frac{d^2}{dx^2} + U_c(x) + E_{CO}(x) \right] \Psi(x, t) = i\hbar \frac{\partial \Psi}{\partial t} \quad (3.1.23)$$

Here comes the next fundamental simplification: we can replace the free electron mass with the effective mass (and thus eliminate the crystal potential) and the actual wave function with a slowly varying envelope function, $F(x, t)$, multiplied with a Bloch wave function (u_k). The resulting equation is called the effective mass equation [95]:

$$\left[-\frac{\hbar^2}{2m^*} \frac{d^2}{dx^2} + E_{CO}(x) \right] F(x, t) = i\hbar \frac{\partial F}{\partial t} \quad (3.1.24)$$

with $F(x, t)$ defined as:

$$\Psi(x, t) \cong F(x, t)u_{k=0} \quad (3.1.25)$$

The problem of solving equation 3.1.23 is thus considerably simplified; this effective mass equation is however valid only for spherical parabolic bands and when the carriers have low energies near the band minimum, the proof and derivation can be found in [94].

We can finally write the equation of motion for an electron wave, centered at k_0 , in a periodic lattice under the influence of a slowly varying field and in the absence of scattering. Without scattering the energy conservation law must hold, we can write therefore:

$$\begin{aligned} \frac{dE(k_0, x)}{dt} &= \frac{\partial E}{\partial k_0} \cdot \frac{dk_0}{dt} + \frac{\partial E}{\partial x} \cdot \frac{dx}{dt} \\ &= v_g \cdot \hbar \frac{dk_0}{dt} + \frac{\partial E_{C0}(x)}{\partial x} \cdot v_g \end{aligned} \quad (3.1.26)$$

where $E(k, x)$ at the bottom of the first band has the form,

$$E(k, x) = E_{C0}(x) + E(k) \quad (3.1.27)$$

which is equivalent to [94]:

$$\frac{d(\hbar k_0)}{dt} = -\nabla E_{C0}(x) = F_e \quad (3.1.28)$$

In the case of semiconductor heterostructures where the effective mass varies along the propagation direction equation 3.1.28 transforms to 3.1.29 as shown in [94]:

$$\frac{d(\hbar k_0)}{dt} = -\nabla E_{C0}(x) - \nabla \left(\frac{\hbar^2 k^2}{2m^*(x)} \right) \quad (3.1.29)$$

The equation of motion in 3.1.28 and 3.1.29 resembles again with Newton's law of motion for classical mechanics as was the case for the free space electron wave 3.1.8.

3.1.4 Scattering

We have seen that electron waves can travel through a semiconductor device unaffected by the built-in and crystal potential and that they obey the classical relationship between momentum and force. In this picture however we have neglected interactions between the electrons and the lattice vibrations. The atoms in the lattice are not absolutely fixed; an acoustic wave or heat might dislocate them from their equilibrium position. As a result the atoms will start oscillating around their equilibrium position and a lattice vibration will start propagating. The quasi particle responsible for the (thermal) lattice vibrations is called the phonon. Phonon-electron interaction will result in a perturbation of the Bloch waves, scattering the wave centered e.g. at k_0 to k'_0 . Not only phonons may cause perturbations of the Bloch waves but also ionized impurities (dopant atoms) or lattice defects. Since scattering plays a very important role in charge carrier transport we need to determine the transition rates $S(k_0, k'_0)$ under the assumption that the perturbing potential U_S is known. We will show how to compute these scattering events in a very general way, more detailed scattering mechanism will be described in the next chapter when their implementation in the Monte Carlo simulator will be shown as well.

We can rewrite equation 3.1.1 in the presence of a (known) scattering potential as:

$$[H_0 + U_S(x, t)] \Psi(x, t) = i\hbar \frac{\partial \Psi(x, t)}{\partial t} \quad (3.1.30)$$

where H_0 is the Hamiltonian of the system without perturbation. Further we assume that the solutions of the unperturbed problem are known the familiar Bloch waves and that their linear combination gives a solution of the perturbed problem (for more details on perturbation theory see [94]). This can be written as:

$$\Psi(x, t) = \sum_k c_k(t) \Psi_k^0(x, t) = \sum_k c_k(t) \Psi_k(x) e^{-iE(k)t/\hbar} \quad (3.1.31)$$

We are now interested to find the coefficients $c_{k'_0}$ for the scattering event from k_0 to k'_0 and subsequent the transition rate $S(k_0, k'_0)$. First we need to evaluate the element in the Hamiltonian matrix assigned to the scattering potential U_S

between k_0 and k'_0 . Without derivation [94, 95] for spherical, parabolic bands where the solutions of the unperturbed problem are Bloch waves we can write:

$$H_{k'k} \approx \frac{1}{L} \int_{-L/2}^{+L/2} e^{-ik'x} e^{+ikx} dx \quad (3.1.32)$$

For non parabolic bands one has to evaluate the overlap integral $I(k, k')$ and from there:

$$H_{k'k} = I(k, k') U_S(k - k') \quad (3.1.33)$$

After the matrix element has been calculated the scattering rate can be computed from:

$$S(k_0, k'_0) = \frac{2\pi}{\hbar} \left| H_{k'_0 k_0}^a \right|^2 \delta(E(k'_0) - E(k_0) - \hbar\omega) + \frac{2\pi}{\hbar} \left| H_{k'_0 k_0}^e \right|^2 \delta(E(k'_0) - E(k_0) + \hbar\omega) \quad (3.1.34)$$

This equation (3.1.34) is also called Fermis Golden Rule: the first term describes energy absorption (of an amount $E = \hbar\omega$) during the scattering process whereas the second one describes energy emission (of the same energy).

To summarize the necessary steps: we must know the form of the perturbing potential and we approximate the solution via a linear combination of Bloch waves (perturbation theory [94]). Then the matrix element $H_{k'k}$ needs to be evaluated and from that the transition rate $S(k_0, k'_0)$.

Different types of perturbing potentials are known in literature, we will present the most frequent in the next chapter. In these chapters we have shown how to apply the semiclassical approach for electron dynamics inside a device. The electrons can be treated as particles and obey an equation of motion very similar to Newton's law 3.1.28. All the influence of the crystal potential can be summarized in one parameter m^* , the effective mass and the effective mass equation has solutions with the same periodicity as the lattice, the so called Bloch waves. Only scattering events between times of free-flight (TOF) need to be treated quantum mechanically, making use of Fermis Golden rule to determine the transition rates.

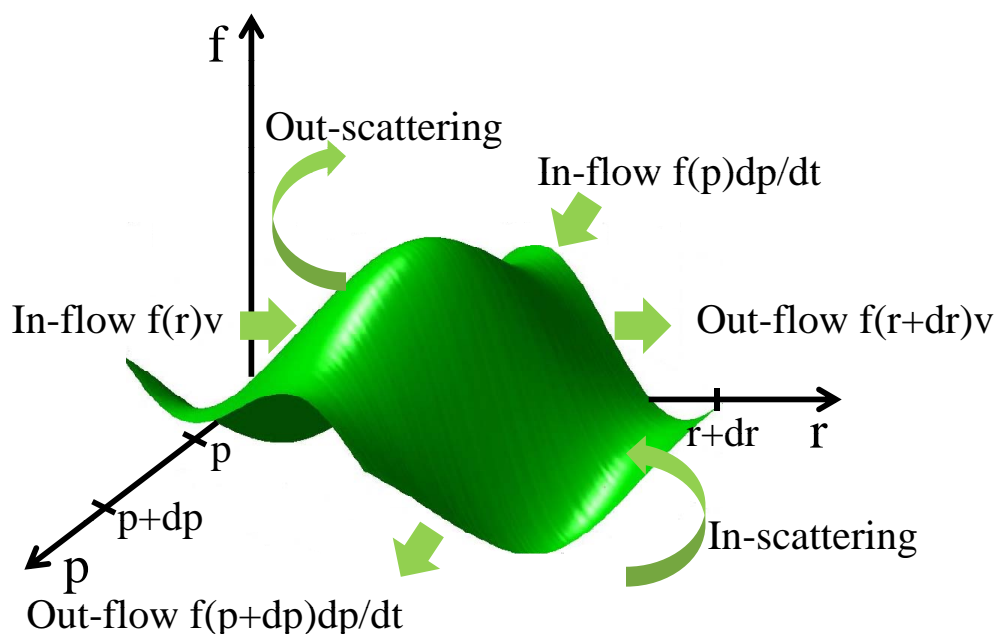


Figure 3.2: Distribution function, f in position-momentum space.

3.1.5 Boltzmann Transport Equation

We have presented how electron motion can be described inside a device according to the semi-classical model. However there are a lot of electrons inside a device during operation, solving the equation of motion for each of them is not really feasible. Another approach would be to find a function f that evolves in time, which accounts for the average distribution of carrier velocity and position. By knowing this distribution function $f(r, p, t)$ we know the entire evolution of all the carriers in our device, both in momentum and space, a complete description of the device in operation in other words.

The solution of the Boltzmann transport equation (BTE) offers exactly this distribution function $f(r, p, t)$. In a very general way the BTE is nothing else than a carrier continuity equation, it expresses carrier conservation in a six dimensional phase space (3 space coordinates and 3 momentum coordinates). There are many rigorous mathematical derivations of the BTE [94] however we will show two heuristic derivation of the equation: one based on a detailed counting of carrier in-flow and out-flow of our test region and another one based on trajectories tracking.

Let's take the phase space region plotted in Fig. 3.2, where on the x-axis we have the generalized coordinates r , a three dimensional vector, and on the y-axis the generalized momentum, a three dimensional vector as well. The green shaded area is an arbitrarily distribution function of carriers; in the following we will study the time evolution this distribution $f(r, p, t)$. There are several ways how the distribution function may increment: if the in-flow of carriers is greater than the out-flow, if the in-scattering is larger than the out-scattering or if there is a generation source of carriers inside the shaded domain. In-flow and out-flow can occur in position space but equally in momentum space while the scattering modifies only the carriers momentum since we assume it to occur instantaneously. If we sum up all the events the above enumerated events and put them in a balance equation (charge must be conserved) we obtain:

$$\begin{aligned}
 (\delta f \delta r \delta p) = & [f(r) - f(r + \delta r)] v \delta t \delta p + [f(p) - f(p + \delta p)] F \delta t \delta r \\
 & + [s(r, p, t) + \delta f / \delta t|_{coll}] \delta t \delta r \delta p
 \end{aligned} \tag{3.1.35}$$

By dividing equation 3.1.35 to $\delta r \delta p \delta t$ and taking the limit ($\delta r, \delta p, \delta t \rightarrow 0$) we can rewrite:

$$\frac{\delta f}{\delta t} + v \cdot \nabla_r f + \mathbf{F} \cdot \nabla_p f = \left. \frac{\delta f}{\delta t} \right|_{coll} + s(\mathbf{r}, \mathbf{p}, t) \tag{3.1.36}$$

This is the Boltzmann transport equation for particles in position and momentum space, where $v = \nabla_p E(\mathbf{p})$ or $v = \mathbf{p}/m^*$ for parabolic bands. Carrier in-flow in our test region is accounted by the second and third term on the left. On the right hand side we have two terms accounting for carrier generation: the collision term, which describes in-scattering and a net generation term which serves as a source in phase space.

Another picture one can imagine about charge carries transport in semiconductors is the one drawn in Fig. 3.3. Under the influence of an external field electrons change their coordinates in space and momentum along a path, called trajectory, in phase space. As long as no scattering occurs the probability, $f(r, p, t)$ of finding an electron along a trajectory, from r_0 to r'_0 (T to T' in the drawing), remains unchanged. If the initial state was occupied at t_0 it will be also occupied at $t_0 + dt$ corresponding to position r'_0 . We can simply express this by:

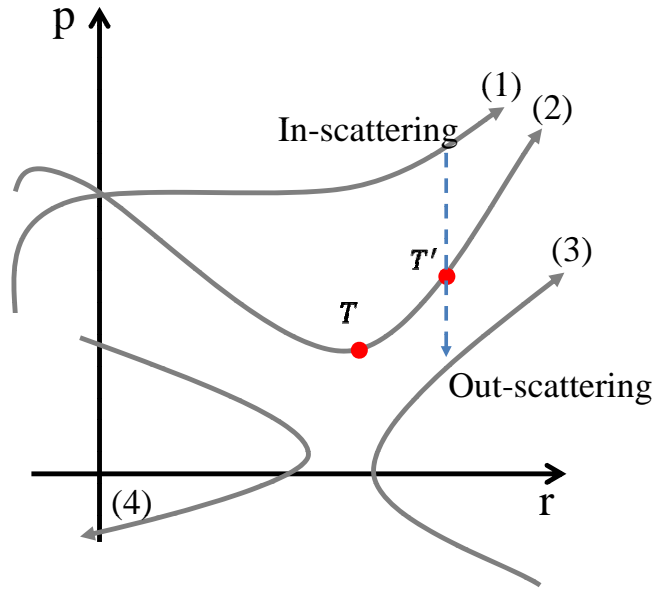


Figure 3.3: Particle trajectories in position-momentum space. Figure redrawn from [95].

$$\frac{df}{dt} = 0 \tag{3.1.37}$$

If however scattering takes place, then the probability along a trajectory can change, and if we also allow a charge carrier source somewhere along the path we can rewrite equation 3.1.37 as:

$$\frac{df}{dt} = \left. \frac{\delta f}{\delta t} \right|_{coll} + s \tag{3.1.38}$$

By expanding the derivative on the left according to the chain rule in a position and a momentum part we obtain the complete BTE:

$$\frac{df}{dt} = \frac{\delta f}{\delta t} + \frac{\delta f}{\delta r}v + \frac{\delta f}{\delta p}F = \left. \frac{\delta f}{\delta t} \right|_{coll} + s \tag{3.1.39}$$

3.2 The Monte Carlo Method

Solving the BTE analytically is a daunting task: in fact this integro-differential equation in 7 dimensions remains unsolvable unless some simplifying assumptions are made. On the other hand these simplifications give rise to the following

question: what is the actual contribution of the real physical processes that take place inside the device compared to the effect of our simplifications when analyzing the solution. One has to be very careful when making assumptions and simplifications since they can modify the system and lead to erroneous, artificial solutions.

That's why numerical solutions are preferred: they deliver the exact solution of the BTE, the Monte Carlo (MC) method being one of the favorite numerical alternatives.

If we recall the trajectory picture of the BTE one can think of simulating trajectories instead of actually solving equation 3.1.39. The particles are treated according to the semi-classical model: we differentiate between so called times of free flight and scattering times. During the times of free flight the particles retain their trajectory obeying Newton's law of motion, whereas the collisions are treated quantum mechanically. Scattering events can kick them off their path or serve as a source of new carriers. In essence the Monte Carlo method is a stochastic algorithm (random walk) which chooses scattering events - not entirely random as we will see - the choice of a scattering event actually reflects the probability of that event to occur.

Thus the method does not solve the BTE explicitly but it mimics real trajectories in phase space. If we simulate a large number of trajectories, then the average quantities (drift velocity, kinetic energy) are good approximations for the real quantities. Since we make no simplification (the algorithm directly mimics the trajectories in phase space) the MC technique is the most accurate method to describe charge carrier transport in semiconductors. Sometimes it even outbeats experimental methods, since direct measurements are not always possible whereas there are no restrictions for simulation scenarios.

Over the next chapters the theory and implementation of the MC simulator used for the modeling and simulation of InAs nanowire transistors will be described in detail.

3.2.1 History of Monte Carlo Method

The Monte Carlo method was developed in the aftermath of World War II (WWII) at the Los Alamos secret research facility as part of radiation shielding research

activity. Scientists were faced with a difficult problem: to estimate the diffusion depth (L_D) of neutrons in different materials. No analytical formulation could be deduced to describe the flux of neutrons through a material, on the other hand trying various materials experimentally by trial and error would have taken too long. The distinct sub-processes involved in neutron diffusion, like for example the distance a neutron could travel in a specific material before hitting the nuclei or the average probability that a neutron would hit a nucleus were well understood and analytical formulations were available. The difficulty comes when putting all these processes together in order to predict L_D .

Nicholas Metropolis and Stanislaw Ulam [99] came with the solution in 1949: they connected all possible processes and their corresponding probabilities within a stochastic algorithm (random walk) that would randomly chose what sequence of events will occur. By running the algorithm enough times with the right probabilities an approximate solution with a fairly high degree of accuracy could be obtained. Because the number of calculations would have been too large for an ensemble of neutrons, John von Neumann introduced another innovation: he programmed the random walk code on one of the first computers, the ENIAC. The method, called by Metropolis Monte Carlo Method was generalized four years later [100] and proved to be so successful that in a very short time various other disciplines sought its benefits and adopted it: chemistry [101, 102], biology [103] and solid state physics [104].

Kurosawa [104] introduced for the first time, in 1966, the Monte Carlo method for the simulation of charge carrier transport in semiconductors at the "International Conference on the Physics of Semiconductors" in Kyoto. His approach, presented in the seminal paper entitled "Monte Carlo calculations of hot electron problems", was received with great interest by researchers studying hot electron problems and attracted many other groups to follow up in this new, exciting branch of device simulation.

To name just a few important contributions, we have in chronological order: Price [105] in 1968, Reese [106] and Fawcett [107, 108] in 1969 and 1970 respectively. The latter two extended the MC simulation to the study of GaAs, a very promising material due to the high electron mobility. Reese [106] also introduced the self-scattering scheme, whereas Fawcett [108] refined the method by modeling non-parabolicity effects. Lebowohl and Price [109] adapted the method

to many-particle simulation and Hauser *et al.* [110] developed the treatment of alloy semiconductors.

A systematic review paper including all the above mentioned advances was published in 1979 by Price [111], but the best-known review study on the Monte Carlo method remains the seminal paper "Monte Carlo method for the solution of charge transport in semiconductors with application to covalent materials" by Carlo Jacoboni and Lino Reggiani [112]. The great level of details together with all the expressions given for the different scattering mechanism make this review paper a guide for everyone interested in implementing a Monte Carlo simulator.

Finally the extensive study by Jacoboni and Lugli [113] provides not only a solid theoretical description of the MC method but also, a practical approach in the MC simulation of modern, state-of-the-art semiconductor devices. The modeling and simulation of high electron mobility transistors (HEMTs), hetero-junction devices, metal oxide/insulator semiconductor field effect transistors (MOSFETs/MISFETs) or hot electron transistors are presented, bridging thus the gap between strictly research oriented algorithms and industry relevant simulators.

3.2.2 The Monte Carlo Approach

The Monte Carlo simulator used in this work is mainly simulating particle trajectories using a random walk approach. This approach gives rise to three fundamental questions:

1. How long will a particle stay on a certain path before a scattering event takes place? (or in other words how long is the time of free flight - TOF)
2. What specific scattering event will take place? (there are many scattering mechanism that are competing on the same time scale)
3. How do we choose the final state after scattering? (from the energy and momentum conservation there are several available states)

In the following paragraphs we will answer all these questions and show how the solution is implemented in the algorithm.

Let's assume a constant electric field in x direction, E_x . For the times of free flight we can describe the carrier position, momentum and velocity under this external bias as:

$$\begin{aligned} p_y(t) &= p_y(0) \\ p_z(t) &= p_z(0) \\ p_x(t) &= p_x(0) + (-q)E_x t \end{aligned} \quad (3.2.1)$$

and

$$\begin{aligned} y(t) &= y(0) + \frac{p_y(0)}{m^*} t \\ z(t) &= z(0) + \frac{p_z(0)}{m^*} t \\ x(t) &= x(0) + \frac{E(t) - E(0)}{(-q)E_x} \end{aligned} \quad (3.2.2)$$

It is somehow intuitive that this TOF must be somehow proportional to the total scattering rate, which can be written as the sum of all scattering mechanism (i from 1 to k).

$$\Gamma(p) = \sum_{i=1}^k \frac{1}{\tau_i(p)} \quad (3.2.3)$$

At this point we have to make a remark: the total scattering rate $\Gamma(p)$ is energy dependent because the specific processes involved depend on the electron energy. An energy dependent scattering rate on the other hand complicates the computation considerably. We can circumvent this by introducing a fictive scattering mechanism - the self scattering - $\Gamma_{SELF} = \Gamma_0 - \Gamma(p)$. The self scattering does not alter the state of the charge carrier, its initial and final position in phase space are identical, and we have a constant total scattering rate Γ_0 . Having defined the constant scattering rate Γ_0 we can deduce the number of carriers that have not been scattered, n_{SF} , since $t = t_0$ as:

$$\frac{dn_{SF}}{dt} = -\Gamma_0 n_{SF} \quad (3.2.4)$$

This is a first order differential equation with the solution:

$$n_{SF}(t) = n_{SF}(0)e^{-\Gamma_0 t} \quad (3.2.5)$$

We can further write the probability that a carrier will not scatter until t as:

$$\frac{n_{SF}(t)}{n_{SF}(0)} = e^{-\Gamma_0 t} \quad (3.2.6)$$

and the probability that the same carrier will scatter in the time interval $t + dt$ as the product between the scattering rate and the probability that it will not scatter until t :

$$P(t)dt = \Gamma_0 e^{-\Gamma_0 t} dt \quad (3.2.7)$$

Since the TOF must be randomly selected we can make use of the random number generator included on most computers, generator which produces uniformly distributed random numbers between 0 and 1. We have to guarantee however that the probability $P(r)$ of choosing a number from the interval $[0, 1]$ is the same as choosing the transition between t and $t + dt$. We can write this as:

$$P(t)dt = \Gamma_0 e^{-\Gamma_0 t} dt \quad (3.2.8)$$

and integrate from 0 to the collision event (r_c and t_c respectively):

$$r_c = 1 - e^{-\Gamma_0 t_c} \quad (3.2.9)$$

If we solve the above equation and rearrange we finally get for the TOF:

$$t_c = -\frac{1}{\Gamma_0} \ln(1 - r_c) \quad (3.2.10)$$

We can replace $1 - r_c$ by r_1 which is also uniformly distributed in the unit interval, reducing thus the problem of determining the TOF to the generation of a single random number.

After we have determined how long the carriers can travel collision-free we have to choose what kind of scattering will take place. Before showing the algorithm for the choice of the particular transition let us review the main scattering mechanism.

3.2.3 Scattering

As mentioned in the previous chapter several scattering rates are implemented in the MC simulator. In a first step we will determine analytical expressions for the perturbing potential and the corresponding transition rate based on the simplified model of spherical parabolic bands. This allows us to get some first impression about the importance of different scattering mechanism and provides a qualitative picture of the scattering probability versus energy and other parameters.

At the end of each section we will give the formulas implemented in the present MC simulator, formulas which are in most cases a lot more complex than the simple spherical, parabolic case. All the transition rates of the MC simulator are implemented in reciprocal space since the particle tracking and scattering is performed in k-space.

Ionized impurity scattering

Electrons traveling in a semiconductor that has been intentionally doped will get perturbed by the electric field of the ionized dopant atom. The force that the electron "feels" is in the simplest case the Coulomb force, thus the perturbing potential has the form:

$$U_S(r) = \frac{q^2}{4\epsilon_r\epsilon_0 r} \quad (3.2.11)$$

If we have a large number of mobile carriers on the other hand, they will screen the ionized impurity and we will get for the perturbing potential the screened Coulomb potential [95]:

$$\frac{1}{r^2} \frac{d}{dr} \left(r^2 \frac{d\delta V}{dr} \right) = \frac{q\delta n}{\epsilon_r\epsilon_0} \quad (3.2.12)$$

Next, from 6.3.9 we can compute the matrix element, $H_{p'p}$ corresponding to this transition [95]:

$$H_{p'p} = \frac{1}{\Omega} \int_{-\infty}^{\infty} e^{-ip \cdot r/\hbar} U_s(r) e^{ip' \cdot r/\hbar} d^3r \quad (3.2.13)$$

and the transition rate as 3.2.14:

$$S(p'p) = \frac{2\pi}{\hbar} |H_{p'p}|^2 \delta(E(p') - E(p) - \Delta E) \quad (3.2.14)$$

For the screened ionized impurity we have thus:

$$H_{p'p} = \frac{q^2}{\Omega \epsilon_r \epsilon_0} \frac{1}{\beta^2 + 1/L_D^2} \quad (3.2.15)$$

and the transition rate after equation 3.2.14 is then [95]:

$$S(p, p') = \frac{2\pi N_I q^4}{\hbar \Omega \epsilon_r^2 \epsilon_0^2} \frac{\delta(E' - E)}{\left[4 \left(\frac{p}{\hbar} \right)^2 \cdot \sin^2 \left(\frac{\alpha}{2} \right) + \frac{1}{L_D^2} \right]^2} \quad (3.2.16)$$

L_D is the Debye length, β is the wave vector, Ω is the normalization volume, α is the scattering angle, N_I the number of impurities and q their charge.

Here we have to make the following distinction: the transition rate above is the screened ionized impurity scattering rate. We can take the two corner cases, when no mobile carriers are present, $L_D \rightarrow \infty$ and we obtain:

$$S(p, p') = \frac{2N_I q^4}{\hbar \Omega \epsilon_r^2 \epsilon_0^2} \frac{\delta(E' - E)}{16 \left(\frac{p}{\hbar} \right)^4 \cdot \sin^4 \left(\frac{\alpha}{2} \right)} \quad (3.2.17)$$

or in the opposite case when the mobile carrier concentration is extremely high, $L_D \rightarrow 0$ and we get the scattering from a delta potential:

$$S(p, p') = \frac{2N_I q^4 L_D^4}{\hbar \Omega \kappa_S^2 \epsilon_0^2} \delta(E' - E) \quad (3.2.18)$$

In this work the Brooks-Herring (BH) formulation together with the Ridley statistical screening model [34] have been used. The BH approach for arbitrarily band structure has the form [114]:

$$\Gamma_{BH,\nu}(k, k') = \frac{Z^2 N_B e^4}{4^2 \hbar \epsilon_0} \sum_{\nu'} \frac{|J(k, k')|^2}{(\beta_s^2 + |k - k'|^2)^2} \delta(E_\nu(k) - E_{\nu'}) \quad (3.2.19)$$

and with the Ridley model correction [115] we get the final scattering rate for ionized impurity as:

$$\Gamma_{ION,\nu}(k, k') = \frac{v_g(k)}{(2\pi N_B)^{-1/3}} \left[1 - \exp\left(-\frac{\Gamma_{BH,\nu}(k, k') (2\pi N_B)^{-1/3}}{v_g(k)}\right) \right] \quad (3.2.20)$$

Phonon scattering

The interaction between thermal lattice vibrations and charge carriers may lead to considerable perturbation and must be treated in great detail. As can be seen in Fig. 3.4 there are two types of phonons: acoustic and optical phonons. The dispersion relation for acoustic phonons is more or less linear and they tend to dislocate neighboring atoms in a direction perpendicular to their direction of propagation as depicted in Fig. 3.4a. Optical phonons have a nearly constant dispersion and they dislocate atoms parallel to their direction of propagation as shown in the same Fig. 3.4a. It is usual for longitudinal phonons near the center of the Brillouin zone to take the first order approximation for the dispersion relationship, as depicted in Fig. 3.4b: namely the slope of the curve.

Let us start with non-polar materials, where the bonds between atoms are covalent. Both the acoustic and the optical phonons interact with the carriers are responsible for a perturbing potential. For the acoustic case the potential has the form [95]:

$$U_{AP}(x, t) = D_A \frac{\partial u}{\partial x} \quad (3.2.21)$$

with D_A the acoustic deformation potential, available from experiments and u the elastic plane wave traveling in the semiconductor.

Similarly the optical interaction potential can be written as [95]:

$$U_{OP}(x, t) = D_0 u(x, t) \quad (3.2.22)$$

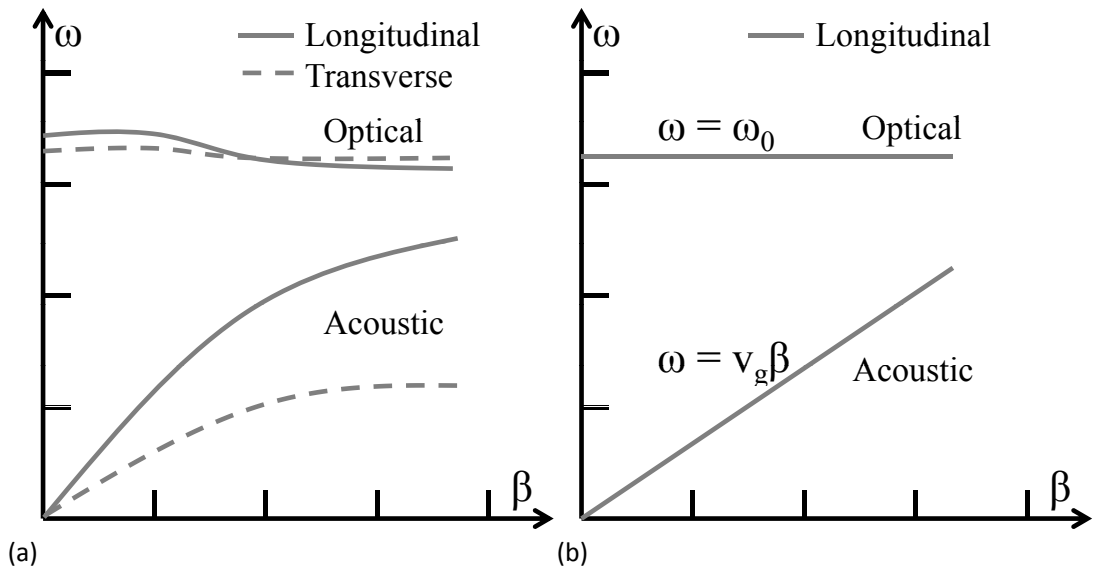


Figure 3.4: (a) Dispersion relation for acoustic and optical phonons both transverse and longitudinal (b) Simplified dispersion relation. Figure redrawn from [95].

with D_0 the optical deformation potential.

In polar materials we have acoustical and optical potential scattering too, but additionally another type of very strong scattering, polar scattering. In GaAs and InAs for example the bond is partially ionic, which means that Ga for example pulls the electron pair closer to itself becoming negatively charged and leaving As positively charged. This creates a dipole with a specific dipole moment. The interaction with acoustic or optical phonons perturbs this dipole which in turn reflects on the electric field, causing carriers to scatter.

Polar scattering caused by interaction with acoustic phonons is called piezoelectric scattering and plays a role in some semiconductors especially at low temperatures. It can be shown that the perturbing potential has the form [95]:

$$U_{pZ} = \frac{qe_{pZ}}{\epsilon_r \epsilon_0} u \quad (3.2.23)$$

with e_{pZ} the piezoelectric constant.

Far stronger is the perturbing potential caused by interaction with optical phonons given by [95]:

$$U_{POP} = \frac{qq^*u}{i\beta V_u \epsilon_0} \quad (3.2.24)$$

where q^* is the effective charge (an indicator of the bond strength) and V_u is the volume of a unit cell.

Summarizing all four types of phonon scattering we can write the perturbing potential in a more general way as:

$$U_s = K_\beta u_\beta \quad (3.2.25)$$

with

$$|K_\beta|^2 = \beta^2 D_A^2 \quad \text{for ADP} \quad (3.2.26)$$

$$|K_\beta|^2 = D_0^2 \quad \text{for ODP} \quad (3.2.27)$$

$$|K_\beta|^2 = \left(\frac{pq^2 \omega_0^2}{\beta^2 \epsilon_r \epsilon_0} \right) \left(\frac{\epsilon_0}{\epsilon_{opt} - 1} \right) \quad \text{for POP} \quad (3.2.28)$$

$$|K_\beta|^2 = \left(\frac{qe_{PZ}}{\epsilon_r \epsilon_0} \right)^2 \quad \text{for PZP} \quad (3.2.29)$$

From this we can evaluate the matrix element $H_{p'p}$ as:

$$|H_{p'p}|^2 = |K_\beta|^2 |A_\beta|^2 \delta_{p'p \pm \hbar\beta} \quad (3.2.30)$$

and the transition rate as [95]:

$$S(p, p') = \frac{2\pi}{\hbar^2 v_\beta} |K_\beta|^2 |A_\beta|^2 \delta \left(\pm \cos \theta + \frac{\hbar\beta}{2\rho} \mp \frac{\omega_\beta}{v_\beta} \right) \quad (3.2.31)$$

One remark has to be made before evaluating the transition rates: in both of the above equations A_β is the squared magnitude of the lattice oscillation. This magnitude however cannot be evaluated using classical mechanics, but a

quantum mechanical equivalent needs to be found. After a derivation that can be found in [95] we obtain the correct expression:

$$|A_\beta|^2 \rightarrow \frac{\hbar}{2\rho\Omega\omega_\beta} \left(N_{\omega\beta} + \frac{1}{2} \mp \frac{1}{2} \right) \quad (3.2.32)$$

With this we can finally write the transition rates as:

$$S(p, p') = C_\beta \left(N_\beta + \frac{1}{2} \mp \frac{1}{2} \right) \delta \left(\pm \cos \theta + \frac{\hbar\beta}{2\rho} \mp \frac{\omega}{v} \right) \quad (3.2.33)$$

where

$$C_\beta = \frac{\pi m^* D_A^2}{\hbar \rho v_S p \Omega} \quad \text{for ADP} \quad (3.2.34)$$

$$C_\beta = \frac{\pi m^* D_0^2}{\hbar \rho \omega_0 \beta p \Omega} \quad \text{for ODP} \quad (3.2.35)$$

$$C_\beta = \frac{\pi m^* q^2 \omega_0}{\hbar \epsilon_r \epsilon_0 \beta^3 p \Omega} \left(\frac{\epsilon_r}{\epsilon_{opt} - 1} \right) \quad \text{for POP} \quad (3.2.36)$$

$$C_\beta = \left(\frac{q e_{PZ}}{\kappa_S \epsilon_0} \right) \frac{\pi m^*}{\hbar \rho v_S \beta^2 p \Omega} \quad \text{for PZP} \quad (3.2.37)$$

At this point we can make some observations about phonon scattering. In Fig 3.5 qualitative representation of the scattering rate versus energy for the different polar and non-polar scattering mechanism is shown. We can see that acoustic deformation potential scattering is dominant at low energies whereas for higher energies the optical deformation potential becomes relevant. The ODP scattering as well as the POP scattering have a threshold at a specific energy, $\hbar\omega_0$, the energy required to emit optical phonons. Below the threshold energy, charge carriers can only adsorb phonons; emission becomes possible only when they have an energy $\hbar\omega_0$ at least equal to the one of the optical phonons. We also see that the two types of polar scattering decrease with increasing energy. As the carrier energy increases they gain more speed and the faster they are the shorter is the interaction with the dipole moment of the lattice.

In the current code the non-polar transition rates are computed from [34]:

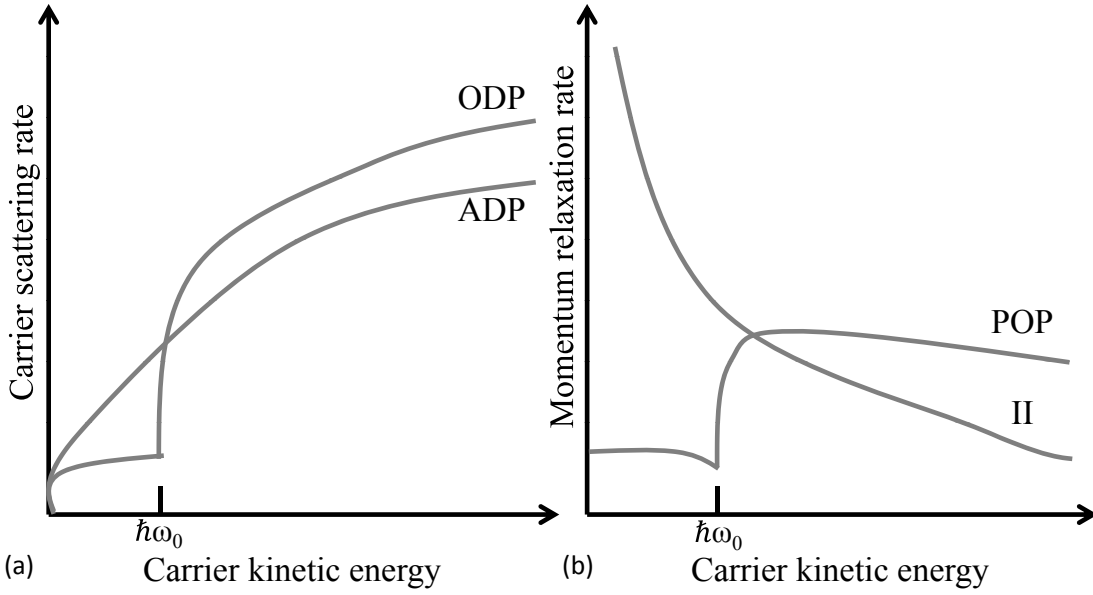


Figure 3.5: (a) Nonpolar scattering, acoustic and optical deformation potential (ADP and ODP) (b) Ionized impurity (II) and polar optical phonon (POP) momentum relaxation rate. Figure redrawn from [95].

$$P_{vv',\eta}^{def}(k, \Omega_{k'}) = \frac{\pi}{\rho\omega_{\eta q}} |\Delta^\eta(v', k, q, v)|^2 I |v, v', k, k'|^2 D_{v'}(\epsilon', \Omega_{k'}) \left(N_{\eta q} + \frac{1}{2} \mp \frac{1}{2} \right) \quad (3.2.38)$$

The deformation potential, D , both acoustic and optical is computed using the rigid pseudo ion model [116–118] for arbitrarily band structures, which requires only the knowledge of the full phonon and band spectra without any other fitting parameters. The density of states is also derived from the full band structure using the method of Gilat and Raubenheimer [119, 120] by integrating over the first Brillouin zone (BZ).

The polar transitions (polar optical phonon scattering) are calculated using the well-established Fröhlich expression [121, 122], again generalized for arbitrarily band structure and the resulting density of states [82, 123]:

$$P_{vv'}^{pol}(k, \Omega_{k'}) = \frac{\pi e^2 \omega_{\eta q}}{2q^2} \left[\frac{1}{\epsilon_\infty} - \frac{1}{\epsilon_0} \right] I |v, v', k, k'|^2 D_{v'}(\epsilon', \Omega_{k'}) \left(N_{\eta q} + \frac{1}{2} \mp \frac{1}{2} \right) \quad (3.2.39)$$

For the acoustic polar scattering also known as piezo-electric scattering the implemented rate is according to Ridley [124]:

$$P_{\nu\nu',\eta}^{piezo}(k, \Omega_{k'}) = \frac{2\pi}{\hbar} K_{av}^2 \frac{e^2 k_B T}{q^2 \epsilon^*} I |v, \nu', k, k'|^2 D_{\nu'}(\epsilon', \Omega_{k'}) \left(N_{\eta q} + \frac{1}{2} \mp \frac{1}{2} \right) \quad (3.2.40)$$

The electromechanical coupling constant (ϵ^*) is calculated analytically for polar materials (wurzite and zinblende crystal structure) using the model introduced by Hutson [125] and the analytical expressions of Ridley [124].

Other transition rates

Beside the ionized impurity and the phonon scattering a few other interactions have been included. We will not deduce them in detail; we will simply show the implemented rates and give the references for further reading.

Another type of perturbing potential is the so-called dislocation potential, which arises due to crystal dislocations when materials are grown on a substrate with a large lattice mismatch (GaN on Si for example). The crystal dislocations will trap free electrons acting like acceptors. The trapping effect of dislocation centers has been extensively studied in the work of Read [126–128]. A semi empirical implementation of the dislocation potential has been chosen after Look and Sizelove [129] since it was shown to be an excellent approximation of the real perturbing potential with only one fitting parameter l [129]:

$$A(q) = \frac{e^2 \lambda^2 f^2}{\epsilon^2 l^2 (1 + q^2 \lambda^2)} \quad (3.2.41)$$

Using this potential in Weimanns approach [130] we obtain the transition rate for crystal dislocation as [34]:

$$P_{\nu\nu'}^{diss}(k, \Omega_{k'}) = \frac{2\pi}{\hbar} A^2(q) n_{diss} I |v, \nu', k, k'|^2 D_{\nu'}^\perp(\epsilon', \Omega_{k'}) \quad (3.2.42)$$

In binary or ternary alloys we have another scattering mechanism, the alloy scattering [131] In SiGe for example, the periodicity of the two individual lattices is perturbed due to atomic disorder in the alloy (the same can be said about III-V ternary alloys). For the MC simulator the transition rate that has been

implemented is the one of Fischetti and Laux [132]. Finally one last transition rate has been implemented in the MC simulator: the impact ionization rate. This process implies that the carrier has a kinetic energy at least equal to the bandgap and that during the impact ionization process its energy and momentum are distributed isotropically over all final k states. If another e-h pair is created or not can be selected by the user with a simple YES/NO flag. The reasoning behind this choice, whether to create secondary e-h pairs or not, is the computational burden; it becomes considerably higher for secondary pair creation. New electron-hole pairs are relevant only for very high electric fields, when electrons have enough energy to populate higher valleys with higher effective mass. In this case their velocity drops and if secondary pairs (at the bottom of the valley with high mobility) are not included an underestimation of the current can be observed. This phenomenon has been studied in [34] and for extremely low bandgap materials like InSb (0.17 eV) for electric fields above $10^5 V/cm$ one must include the pair creation.

The transition rate is taken also after Fischetti and Laux [132] and has the form [34]:

$$\Gamma_{IMP}(E) = \sum_i^2 \theta(E - E_{0i}) a_i [E - E_{0i}]^{r_i} \quad (3.2.43)$$

3.2.4 Choosing a transition rate

In the Cellular Monte Carlo algorithm like in any classic Ensemble Monte Carlo method the first step consists in a discretization of the k -space. This is done by applying a non-uniform grid for each energy band in the $E(k)$ dispersion. Next all the above scattering rates are computed for an initial state k to a final state k'_i . We can write the probability of an electron to scatter from k to k'_i through various mechanisms as [34,82]:

$$P(k, k'_i) = \sum_{j=1}^N P_j(k, k'_i) \quad (3.2.44)$$

Where the $j = 1 \dots N$ in the sum accounts for all possible transition rates.

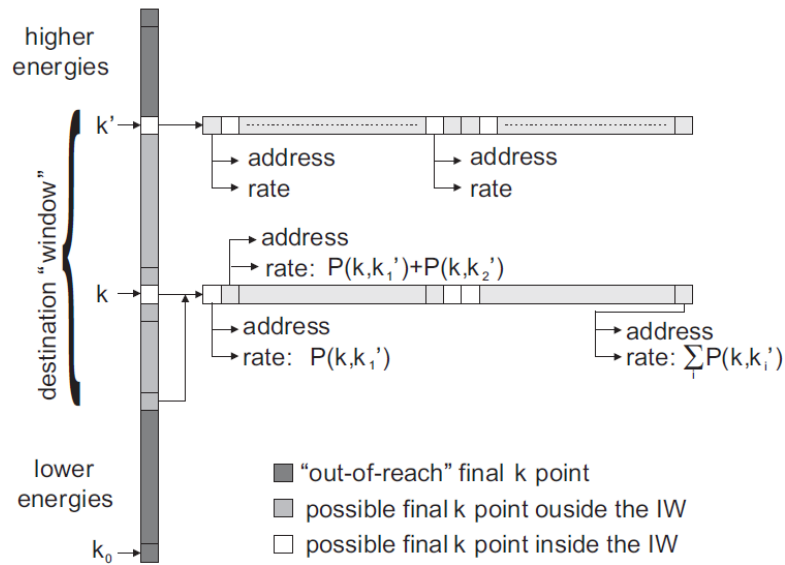


Figure 3.6: Illustration of Scattering Table in the CMC code. Figure taken from [34].

If we integrate this probability over the entire BZ we obtain the scattering probability of an electron to scatter from state k to any possible state k'_i in the BZ, the final distance in k -space depending on the type of scattering [34]:

$$P(k) = \sum_{k'_i} P(k, k'_i) \quad (3.2.45)$$

This is in fact the originality of the Cellular Monte Carlo approach: it uses the Cellular Automaton concept to simplify the choice of the transition and of the final state. All the $P(k)$ are computed before the actual simulation starts and stored in a large transition table. In Fig. 3.6 a schematic of the transition table is shown: for each k a row is allocated in the table, starting from small energies and going up to higher energies. Each row contains as first entry the probability of the electron to scatter from k , the initial state, to k_1 but also the address of this final state k_1 . By doing so, once the transition from k to k_1 has been chosen we automatically now were this state k_1 is located and a time and resource consuming search for available final states in the BZ can be omitted. The second entry is the cumulative probability to scatter to k_1 and k_2 and so on with the final entry being the sum of all partial probabilities from $k_1 \dots k_i$. We can in fact divide all partial sums by this final sum thus all entries on a row are real numbers between 0 and 1.

The choice of a transition and its corresponding final stage is simplified to the generation of two uniform random numbers between zero and one. The first is a binary decision and determines if a transition takes place or not (0 or 1) and the second chooses what event should take place. It will indicate to a random transition from the total sum (also normalized between 0 and 1) and at the same entry in the table we will find the address of the final state.

This is in brief the kernel of the CMC simulator more details can be found in [34, 82] we will just say a few more words about the motivation behind this approach. The major disadvantage of the MC technique is the long simulation time required to get a good statistic. A good part of that time is spent in scanning the BZ in order to find allowed final states [34, 82] time that can be skipped with the Cellular Automaton approach. We save time but at the expense of memory: large tables have to be precomputed, stored and then loaded in the RAM memory during the simulation. This is however no serious problem, the price and memory specifications of the newest simulation servers are more than adequate for such a task. As the price of memory continues to drop even larger tables can be stored, tables containing not only the final state destination but also the exact type of scattering and so on.

3.2.5 Band structure

The CMC code employed in this work is a state-of-the-art full band simulator. It numerically computes the complete band structure for various semiconductors, from Si and Ge to III/V semiconductors and ternary alloys. In order to get the complete energy dispersion along the different crystal directions one can choose between two approaches: the ab-initio and the empirical methods.

Ab initio methods like LDA [133] or GW [134, 135] are based on a physical foundation but are extremely demanding and not very accurate: it is well known that they over or underestimate crucial parameters like bandgap and effective mass.

Empirical methods on the other hand are fast and exact but require some fitting parameters in order to reproduce experimental data. In this work the Empirical Pseudo Potential (EPM) method is used, one of the most popular empirical methods [136, 137].

Spin orbit and non-local corrections are also included in the EPM method used [82] an extensive review of experimental and fitted band structure using this approach can be found in [34]. A very good agreement is reported not only for simple and compound semiconductors but also for strained SiGe [34].

In the next paragraph the computed bandstructure of InAs will be shown and compared with available data from literature.

3.2.6 Phonon spectra

A scheme is implemented to compute the full phonon dispersion as well. This is needed in order to compute the electron-phonon interactions for all energies. The approach used here is again an empirical one: the so-called empirical shell model [138] has been implemented [34] with the particularity that it allows as input both the 14 parameters of the 14 parameter shell model [139] and the parameters of the valence shell model [140].

3.3 The Hydrodynamic Model

The favorite simulation approach in the semiconductor industry is still the drift-diffusion (DD) approach derived by Roosbroeck more than fifty years ago [89] mainly due to its simplicity and ease of implementation. As long as the transistor gate length doesn't enter in the deep submicron regime the DD approach delivers fairly accurate results having the main advantage of being extremely fast when compared to other simulation approaches. When entering however in the deca-nanometer range DD is no longer reliable and some more refined approaches need to be used. The simulator used in this part of the work, Sentaurus Device, is a state of the art finite volume device simulator capable of performing state-of-the-art hydrodynamic, thermal, optical and high-frequency simulations.

We will first briefly derive the drift diffusion equations from the Boltzmann Transport Equation (BTE) and then show how the model can be extended by including the energy balance equations leading thus to a hydrodynamic model [141], more appropriate for the simulation of deep sub-micron geometries and their underlying physics.

The BTE under the relaxation time approximation and for spherical parabolic bands can be written as [95]:

$$\frac{eE}{m^*} \frac{\partial f}{\partial v} + v \frac{\partial f}{\partial x} = \frac{f_0 - f(v, x)}{\tau} \quad (3.3.1)$$

We recall that the current density can be written as the first moment of the distribution function, f (the zero-th moment of the equation being the carrier continuity equation):

$$J(x) = e \cdot \int v f(v, x) dv \quad (3.3.2)$$

If we multiply equation 3.3.1 with v and integrate over dv we obtain:

$$\frac{1}{\tau} \left[\int v f_0 dv - \int v f(v, x) dv \right] = -\frac{J(x)}{e\tau} \quad (3.3.3)$$

Since we now that the equilibrium distribution f_0 is even in v [95] equation we can rewrite equation 3.3.3 as:

$$J(x) = -e \frac{e\tau}{m^*} E \int v \frac{\partial f}{\partial v} dv - e\tau \frac{d}{dx} \int v^2 f(v, x) dv \quad (3.3.4)$$

Remembering the integration by parts we have:

$$\int v \frac{\partial f}{\partial v} dv = [v f(v, x)]_{-\infty}^{\infty} - \int f(v, x) dv = -n(x) \quad (3.3.5)$$

and

$$\int v^2 f(v, x) dv = n(x) \langle v^2 \rangle \quad (3.3.6)$$

The expression $e\tau/m^*$ can be replaced by an average mobility and the averaged square velocity can be expressed in equilibrium as $k_B T/m^*$ (for the 3D case with a prefactor of 3). Making use of the Einstein relation $D = \mu k_B T$ we introduce the diffusion coefficient and finally obtain the drift-diffusion equation for electrons and holes:

$$\begin{aligned}
 J_n &= qn(x)\mu_n E(x) + qD_n \frac{dn}{dx} \\
 J_p &= qp(x)\mu_p E(x) + qD_p \frac{dp}{dx}
 \end{aligned}
 \tag{3.3.7}$$

The current contribution due to the external or built in electrostatic potential are expressed by the first term (drift part) in equation 3.3.7 whereas the second one is responsible for the current contribution due to a concentration gradient (diffusive part). Some important simplifications are made in the DD approach: we have expressed the average velocity through the thermal velocity hence we assume that the system is near equilibrium. This is only valid for small perturbation (low field) and if we neglect any thermal interactions. Some empirical models for the mobility can be introduced, for example the Poole-Frenkel field dependent mobility, to extend the validity of the DD model also for high fields but this approach has its limitations. Eventually the Einstein relation for the diffusion coefficient is no longer valid, not to mention the parabolic band assumption.

For state-of-the-art electronic devices, well in the nanometer range, the classical drift-diffusion model [89] in use from the mid 50s is no longer accurate, due to the huge electric fields and the hot electron effects (like velocity overshoot and saturation, or electron inter-valley transfer). For this reason all the simulation here are carried out using an energy balance model after the work of Chen *et al.* [142,143], a model which also takes the electron, hole and lattice temperature into account.

The starting point is again the BTE but this time we dont take the zeroth and first moment of the equation but the zeroth and second one. The second moment is obtained by multiplying the BTE with the expression $\hbar^2 k^2 / 2m^*$ and integrating over dv . We obtain three energy balance equations [35]:

$$\begin{aligned}
 \frac{\partial W_n}{\partial t} + \nabla \cdot S_n &= J_n \cdot \nabla E_C + \left. \frac{dW_n}{dt} \right|_{coll} \\
 \frac{\partial W_p}{\partial t} + \nabla \cdot S_p &= J_p \cdot \nabla E_V + \left. \frac{dW_p}{dt} \right|_{coll} \\
 \frac{\partial W_L}{\partial t} + \nabla \cdot S_L &= \left. \frac{dW_L}{dt} \right|_{coll}
 \end{aligned}
 \tag{3.3.8}$$

where the energy fluxes can be written as:

$$\begin{aligned}
 S_n &= -\frac{5r_n\lambda_n}{2} \left(\frac{k_B T_n}{q} J_n + f_n^{hf} \kappa_n \nabla T_n \right) \\
 S_p &= -\frac{5r_p\lambda_p}{2} \left(\frac{k_B T_p}{q} J_p + f_p^{hf} \kappa_p \nabla T_p \right) \\
 S_L &= -\kappa_L \nabla T_L
 \end{aligned} \tag{3.3.9}$$

where κ_n , κ_p and κ_L are the thermal conductivities and $f_n^{hf} = f_p^{hf} = 1$ and $r_n=r_p=0.6$ [35].

The two parameters $f_{n,p}^{hf}$ and $r_{n,p}$ can be changed from their default values (1 and 0.6) in order to modify the diffusive and convective part of the energy flow separately.

After [35] the collision terms can be expressed as:

$$\begin{aligned}
 \left. \frac{\partial W_n}{\partial t} \right|_{coll} &= -H_n - \zeta_n \frac{W_n - W_{n0}}{\tau_{en}} \\
 \left. \frac{\partial W_p}{\partial t} \right|_{coll} &= -H_p - \zeta_p \frac{W_p - W_{p0}}{\tau_{ep}} \\
 \left. \frac{\partial W_L}{\partial t} \right|_{coll} &= H_L + \zeta_n \frac{W_n - W_{n0}}{\tau_{en}} + \zeta_p \frac{W_p - W_{p0}}{\tau_{ep}}
 \end{aligned} \tag{3.3.10}$$

H_n , H_p and H_L are the generation (recombination) energy gain (loss) defined, according to the same [35], as:

$$\begin{aligned}
 H_n &= 1.5k_B T_n \left(R_{net}^{SRH} + R_{net}^{rad} + R_{n,net}^{trap} \right) - E_{g,eff} \left(R_n^A - G_n^{ii} \right) - \alpha \left(\hbar\omega - E_{g,eff} \right) G^{opt} \\
 H_p &= 1.5k_B T_p \left(R_{net}^{SRH} + R_{net}^{rad} + R_{p,net}^{trap} \right) - E_{g,eff} \left(R_p^A - G_p^{ii} \right) - \alpha \left(\hbar\omega - E_{g,eff} \right) G^{opt} \\
 H_L &= \left[R_{net}^{SRH} + 0.5 \left(R_{n,net}^{trap} + R_{p,net}^{trap} \right) \right] \left(E_{g,eff} + 1.5k_B T_n + 1.5k_B T_p \right)
 \end{aligned} \tag{3.3.11}$$

Here R_{net}^{SRH} , R_{net}^{rad} , $R_{n,p}^A$ and $R_{n,p,net}^{trap}$ are the Shockley-Read-Hall (SRH), radiative, Auger and trap assisted recombination rates. The photon energy is denoted by $\hbar\omega$ whereas G^{opt} and $G_{n,p}^{ii}$ are the optical generation and impact ionization rates.

Finally the three energy densities are being computed after [35]:

$$\begin{aligned}
 W_n &= nw_n = n \left(\frac{3k_B T_n}{2} \right) \\
 W_p &= pw_p = p \left(\frac{3k_B T_p}{2} \right) \\
 W_L &= c_L T
 \end{aligned} \tag{3.3.12}$$

In addition to the three partial differential equations described above 3.3.8 the coupled system of PDEs consisting of the Poisson, hole and electron continuity equation completes the mathematical description of the system. The later three differential equations are implemented as [35]:

$$\begin{aligned}
 \nabla \cdot [\epsilon \nabla V] &= q(n - p - N_D^+ + N_A^-) \\
 \frac{\partial n}{\partial t} &= \frac{1}{q} \nabla J_n + G_n - R_n \\
 \frac{\partial p}{\partial t} &= -\frac{1}{q} \nabla J_p + G_n - R_n
 \end{aligned} \tag{3.3.13}$$

where ϵ is the electrical permittivity, N_D^+ and N_A^- are the densities of ionized donors and acceptors, respectively, q is the unit charge, n and p are the electron/-hole densities, respectively.

According to the hydrodynamic model [35,142,143] the equations for electron and hole current densities are:

$$\begin{aligned}
 J_n &= \mu_n (n \nabla E_C - 1.5nk_B T_n \nabla \ln m_n + k_B T_n \nabla n - nk_B T_n \nabla \ln \gamma_n + \lambda_n f_n^{td} kn \nabla T_n) \\
 J_p &= \mu_p (n \nabla E_V + 1.5pk_B T_p \nabla \ln m_p - k_B T_p \nabla p + pk_B T_p \nabla \ln \gamma_p - \lambda_p f_p^{td} kp \nabla T_p)
 \end{aligned} \tag{3.3.14}$$

where μ_n and μ_p are the electron and hole mobilities and T_n and T_p the carrier temperatures, m_n and m_p the carriers effective masses and $\gamma_{n,p}$ is of the form [35]:

$$\begin{aligned}\gamma_n &= \frac{n}{N_C} \exp\left(\frac{E_{F,n} - E_C}{k_B T}\right) \\ \gamma_p &= \frac{p}{N_V} \exp\left(\frac{E_{F,p} - E_V}{k_B T}\right)\end{aligned}\tag{3.3.15}$$

One can see that the first two terms of the current density definition recurden are identical to those in the DD approach while the third term accounts for the carrier temperature gradients and the last one for the effective mass variation.

Fermi statistics have been used for all the simulations; therefore λ_n (and analogous λ_p) has the form [35]:

$$\begin{aligned}\lambda_n &= \frac{F_{1/2}\left(\frac{E_{F,n} - E_C}{k_B T}\right)}{F_{-1/2}\left(\frac{E_{F,n} - E_C}{k_B T}\right)} \\ \lambda_p &= \frac{F_{1/2}\left(\frac{E_V - E_{F,p}}{k_B T}\right)}{F_{-1/2}\left(\frac{E_V - E_{F,p}}{k_B T}\right)}\end{aligned}\tag{3.3.16}$$

where $F_{(1/2)}$ denotes the Fermi integral of order 1/2.

3.3.1 Velocity Saturation

A critical effect that needs to be modeled in order to have accurate results is the velocity saturation at high fields. It is well known that the drift velocity in InAs saturates when the electric fields exceeds a certain critical value E_{HF} [144]. In the simulation the following formulation of the drift velocity is employed [35]:

$$v_{sat} = v_{sat0} - v_{sat} \left(\frac{T}{300}\right)\tag{3.3.17}$$

The saturated velocity enters in the field dependent mobility [35] as follows:

$$\mu(E) = \frac{\mu_{low}}{\left[1 + \left(\frac{\mu_{low} E_{hf}}{v_{sat}}\right)^\beta\right]^{1/\beta}}\tag{3.3.18}$$

with β being a temperature depending exponent. The above model is called the extended Canali mode [145] and is based on the Caughey Thomas formula [146] the only difference being the exponent β .

3.3.2 Traps

As mentioned in the previous sections the trap states are of great importance and their effect on the transistor performance will be analyzed also within the hydrodynamic approach. The state-of-the-art finite volumes simulator used for this part has a considerable number of trap models allowing a thorough treatment of trap related effects.

Four different trap state types are available: donor, acceptor, electron-neutral and hole-neutral. The first two are initially charged (positive for donor and negative for acceptor) and become neutral when they trap a charge carrier (electron for donor and hole for acceptor). For the neutral trap states as their name already unveils, they are electrically neutral when unoccupied and carry the charge of one electron (hole) when occupied. These are however no rigid definitions but more of a naming convention, the trap state is characterized in fact by its properties, like position in the bandgap, capture and emission rate and so on. A neutral trap state can for example trap both electron and holes if it is placed exactly in the middle of the bandgap and if it has symmetric capture rates for electrons and holes.

The energy distribution of trap states inside the bandgap can be either constant (level or energy interval), exponential or Gaussian. A plot illustrating the various energy distributions together with their definition is shown Fig. 3.7:

$$\begin{aligned}
 N_T &= N_0 \text{ at } E = E_0 \\
 N_T &= N_0 \text{ for } E_0 - E_S < E < E_0 + E_S \\
 N_T &= N_0 e^{-\left| \frac{E-E_0}{E_S} \right|} \\
 N_T &= N_0 e^{-0.5 \left(\frac{E-E_0}{E_S} \right)^2}
 \end{aligned} \tag{3.3.19}$$

A uniform space distribution is assumed by default, the user can however choose from several space distributions ranging from Gaussian to single trap at fixed coordinates.

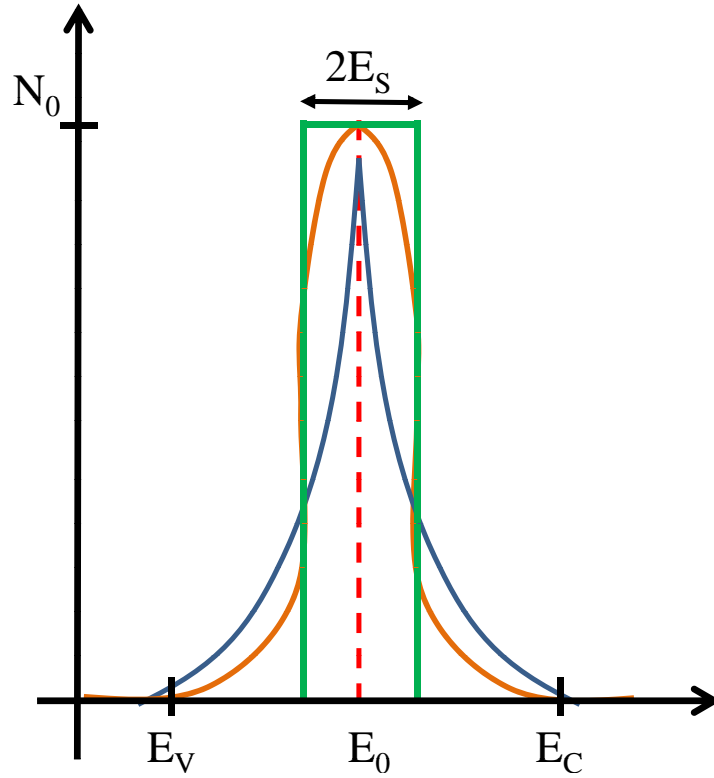


Figure 3.7: The various trap distributions: discrete trap level (dotted red), constant trap level (green), exponential (blue) and Gaussian distribution (orange). Figure redrawn from [35].

An arbitrary number of trap levels can be introduced both for bulk material and for material interfaces/surfaces. The electrostatic contribution of these states is included in the modified Poisson as:

$$\begin{aligned} \nabla \cdot \epsilon \nabla \phi = -q \cdot \left(p - n + N_D - N_A + \sum_{E_t} (N_{Dt} - n_{Dt}) - \right. \\ \left. - \sum_{E_t} (N_{At} - n_{At}) + \sum_{E_t} p_t - \sum_{E_t} n_t \right) \end{aligned} \quad (3.3.20)$$

where N_{Dt} and N_{At} are the donor and acceptor trap concentrations, n_{Dt} and p_{At} are the electron and hole concentrations in the donor (acceptor) trap level and finally n_t and p_t the trapped electron (hole) concentration in the neutral trap level.

In order to obtain the trap occupation dynamics a detailed balance equation is numerically solved for each trap level, both for holes and electrons [35]:

$$\frac{dn_t}{dt} = v_{th}^n \sigma_n N_{Et} \left(\frac{n_1}{g_n} f_n - n(1 - f_n) \right) + v_{th}^p \sigma_p N_{Et} \left(\frac{p_1}{g_p} (1 - f_n) - p f_n \right) \quad (3.3.21)$$

Where $f(n)$ is the trap occupation probability, v_{th} the thermal velocity, σ the capture cross section and g the degeneracy factor for holes and electrons.

As one can see there are two terms for electrons and two term for holes in the balance equation. The first accounts for charge emission from the trap level in the valence or conduction band and is proportional to the trapped carrier density, n_1 or p_1 . Charge carrier capture is expressed by the $n(1 - f_n)$ term is is proportional to the charge carrier density in the band, n_i or p_i .

For steady state the time dependence vanishes ($t \rightarrow \infty$, $d/dt = 0$) and the balance equation can be written as [35]:

$$f_n = \frac{v_{th}^n \sigma_n n_1 + v_{th}^p \sigma_p p_1}{v_{th}^n \sigma_n (n + n_1) + v_{th}^p \sigma_p (p + p_1)} \quad (3.3.22)$$

Thus for a specific process s , we can write the capture rate as [35]:

$$f^n = \frac{\sum c_i^n}{\sum (c_i^n + e_i^n)} \quad (3.3.23)$$

$$r_k^n = \frac{c_k^n \sum c_i^n}{\sum (c_i^n + e_i^n)} \quad (3.3.24)$$

The capture rate for one electron in the conduction band, or one hole in the valence band is given by [35]:

$$c_C^n = \sigma_n (1 - g_n^J) v_{th}^n n + g_n^J \frac{J_n}{q} \quad (3.3.25)$$

Whereas the emission rate from a trap state to the respective band can be written as:

$$e_C^n = v_{th}\sigma_n\gamma_n\frac{n_1}{g_n} + e_{const}^n \quad (3.3.26)$$

We notice that for $g_n = e_{const} = 0$ the capture and emission rates are related to each other via the principle of detailed balance [35]:

$$e_i = \frac{c_i}{g} e^{\frac{E_{trap} - E_F^i}{k_B T_i}} \quad (3.3.27)$$

Additionally the simulator provides the option to place fixed charges at material interfaces. The fixed charges are essentially trap states that are always filled. They can be either positive or negative with a user-defined uniform concentration. For fixed charges obviously no dynamic behavior is implemented.

3.4 Structure Creation

The simulated nanowire is the same as in the previous chapter, namely the InAs nanowire transistor from Lund [24]. The first step we perform is the realistic modeling of the physical device with the Sentaurus Device Editor (SDE) included in the TCAD framework.

A two dimensional (2D) or a three dimensional (3D) device editor with graphical users interface (GUI) are available, we opted for the full 3D option since the aim of this work is to simulate transistors with multi-dimensional gates (GAA structures).

We can summarize the general modeling procedure as follows:

1. Create device geometry and assign material properties
2. Generate contact regions
3. Define doping profile
4. Define discretization rules for the mesh
5. Create device mesh

The device geometry definition in step (1) can be either manually user-specified or automatically generated from a process emulation step. Process emulation implies that the entire physical process is not simulated (for this another tool of the TCAD framework is available, Sentaurus Process) but merely emulated. For example the emulation of an etching process is performed by simply specifying the etch depth rather than simulating the physical etching rate.

We define our geometry, which is made out of 3D primitives, manually: cuboids and cylinders are the building stones. A large cuboid with $2 \times 1 \mu\text{m}$ dimensions will serve as wafer substrate and we assign the material Nitride to it. Next we create two concentric cylindrical structures both having $1.4 \mu\text{m}$ length and different diameters. The first one has a radius of 47.5 nm whereas the second one has a radius of 17.5 nm . Indium Arsenide is assigned as material for the small cylinder with the diameter of 35 nm , as in the work of Blekker *et al.* [24]. Nitride is again assigned to the large cylinder which will serve as gate dielectric with a thickness of 30 nm . By carefully applying Boolean operations to these primitives we obtain our omega gated nanowire transistor. In the overlap behavior tab we chose new overlaps old and by creating the geometrical shapes in the order cuboid, large cylinder, small cylinder we obtain a nanowire (InAs cylinder) surrounded by the gate dielectric and both of them lying on a nitride substrate. We mention here that Sentaurus Device Editor has a huge material database with all the common semiconductors, oxides and insulators which can be assigned to a geometrical primitive by simply clicking on them. However the user has the option to define its own material files and to link them (call by reference) with existing shapes via a parameter file. This offers the great advantage of changing material parameters (value of saturated velocity, maximum field corresponding to this velocity and so on) without having to rebuild the mesh. We opt for this alternative and define our own parameter file for InAs, file that is in a first step identical to the default one.

After having defined the model geometry we create the contacts: source, drain and wrap gate. Different types of contact (electrodes, thermodes) can be selected; we chose electrical contacts and define them over entire surfaces. For the doping profile we choose a constant doping with a value of $4.3 \times 10^{17} \text{ cm}^{-3}$ which is in good agreement with estimates of unintentional doping during growth from As-precursors [24].

Dimension	κ_{ij}	$\mu(\Omega_i)$
1D	$1/l_{ij}$	Box length
2D	d_{ij}/l_{ij}	Box area
3D	D_{ij}/l_{ij}	Box volume

Table 3.1: Box method coefficients for 1, 2 and 3-D discretization.

Equation	j_{ij}	r_i
Poisson	$\epsilon(u_i - u_j)$	$-\rho_i$
Electron continuity	$\mu^n(n_i B(u_i - u_j) - n_j B(u_j - u_i))$	$R_i - G_i + \frac{d}{dt}n_i$
Hole continuity	$\mu^p(p_i B(u_i - u_j) - p_j B(u_j - u_i))$	$R_i - G_i + \frac{d}{dt}p_i$

Table 3.2: Numerical approximation of the coupled differential equations, solved in each vertex of the mesh.

3.4.1 Mesh Generation

After having defined the device geometry, doping profiles and contact the discretization step follows as shown above. Since the system of partially differential equations that defines charge transport in our device (PDEs) is using continuous quantities but our mesh is now made out of a discrete number of nodes, we have to discretize the PDEs as well. The method of choice is the box method also known as finite volumes method [147]. A typical differential equation of the form:

$$\nabla \cdot J + R = 0 \tag{3.4.1}$$

gets transformed, by applying the Gaussian theorem over a test volume and discretizing the resulting expression, into:

$$\sum_{j \neq i} \kappa_{ij} \cdot j_{ij} + \mu(\Omega_i) \cdot r_i = 0 \tag{3.4.2}$$

In Table 3.1 the coefficients and measures for 1D, 2D and 3D case are specified, whereas Table 3.2 shows the discretized Poisson together with the hole and electron continuity equations:

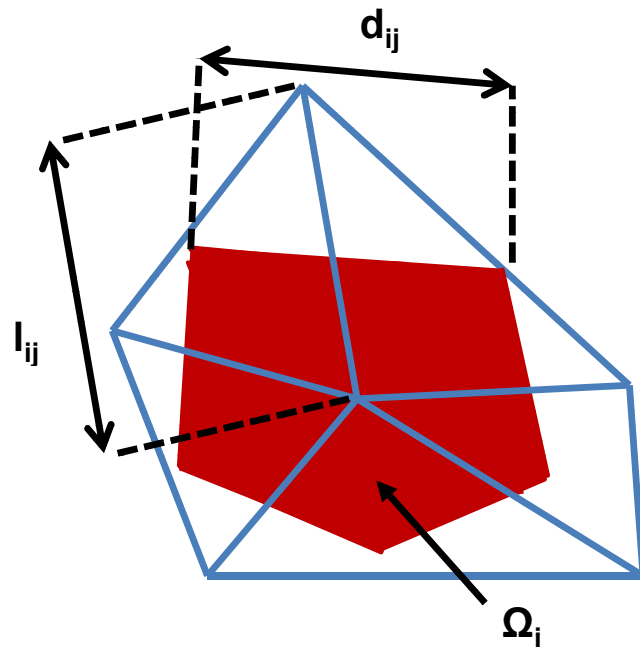


Figure 3.8: Illustration of a 2D triangular mesh over a control area Ω (red) using the box method. Figure redrawn from [35].

One of the four Maxwell's equations, that ensures charge conservation, is Gauss law. In its integral form it states the electric flux through a closed surface of a test volume equals the electric charge inside the volume times $1/\epsilon$. In the finite volume method the Gaussian theorem is the prescription applied over the test volumes to unite them, which makes it the natural method of choice for discretizing semiconductor devices. In fact other methods like finite elements have major problems when ensuring charge conservation over a discretized simulation volume.

In Table 3.1 and Table 3.2 we have all the prescriptions to discretize our PDE, the only open issue remaining is the choice of the box method coefficients, k_{ij} . In order to obtain the k_{ij} , a special type of mesh needs to be build, a so called Delaunay mesh [147]. A simple definition of a Delaunay mesh states that the circumsphere of each mesh element cannot contain any other mesh vertices. This definition is illustrated in Fig. 3.8.

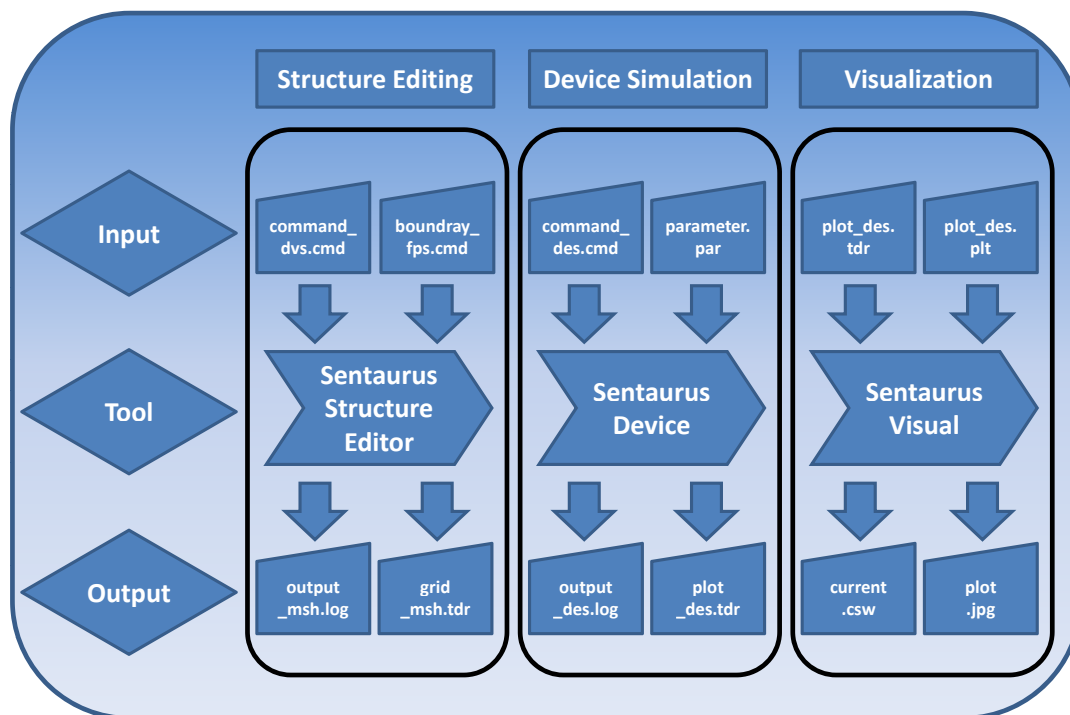


Figure 3.9: Illustration of a typical simulation flow, starting from the structure editing, device simulation and visualization of the simulation output.

3.4.2 Simulation Flow

Sentaurus TCAD is a complete simulation framework consisting of a large number of individual programs or tools. The complete simulation flow chart is present in Fig. 3.9 where also the names of the different tools are given. After the mesh is generated Sentaurus Device Editor creates an output file with .tdr extension. This file contains both the discretized geometry and the doping profiles and will serve as input to the actual device simulator, Sentaurus Device.

Sentaurus Device, a multidimensional (1D, 2D and 3D) electrical, thermal and optical simulator is the core of the TCAD framework. It has no graphical user interface therefore the entire simulation is controlled by a command file somehow similar to a script file. The command file employs a pseudo-programming language which is very well documented in the users guide. It is made out of six (or eight) sections delimited by brackets and containing specific keywords. The simulator is not case sensitive and the sections can be arranged in an arbitrary order but it is syntax sensitive (use of parentheses must be consistent; variables

must be declared between quotation marks, etc.). Next we will describe briefly each of the six sections (eight in the case of Mixed Mode simulation) and explain what they contain for the specific case of a nanowire simulation.

As mentioned before the order of these sections plays no role but we adopted the following order to have a clear structure of the simulation file.

1) The File section

Here the input and output files of the simulation are defined. As input we have the previously generated mesh file and optionally the parameter file with the user-defined materials. The output files are of three sorts: plots were current-voltage ($I - V$) or capacitance-voltage ($C - V$) curves are stored, spatially resolved maps of flux quantities or vector fields (electric field inside the device) and finally log files were all the relevant information of the simulation flow are stored.

2) The Electrode section

Details on the contacts can be provided here. In the default case perfect Ohmic contacts are assumed but also Schottky contacts or tunneling barriers can be declared. It is well known that due to Fermi level pinning at the surface, InAs creates a very good ohmic contact with metals like gold. Therefore we define ohmic contacts with a Workfunction of 5 eV and add some contact resistances with a value of 900 ohms. The pad parasitic capacitances will be defined later when introducing Sentaurus Mixed-Mode which allows the simulation of entire parasitic networks.

3) The Physics section

The physics section is the most important section of the simulation file and it can be either global, material specific, region specific or region interface-specific.. Here all the physical models relevant for the accurate simulation of the device are specified. We include the hydrodynamic model by simply specifying the keyword Hydrodynamic in the global physics section. In the material specific physics for InAs we specific the high field saturation model, the bandgap narrowing model and the SRH recombination. In the region interface physics InAs Nitride we define the interface trap states by several keywords: trap distribution, distribution spread (σ) trap depth, cross-section and of course concentration.

4) The Plot section

A list of variables to be plotted in the output file is included here. Electron and hole quasi Fermi levels, potential, space-charge, electron and hole densities are among the most common quantities to be included, we add also the electron temperature since we have activated the hydrodynamic transport.

5) The Math section

In this section some convergence parameters can be adjusted like the minimum norm of the right hand side (RHS), the maximum relative error in each iterative or the maximum number of iterations. A deeper insight in the numerical methods and the various schemes used in the simulator is given in the next chapter.

6) The Solve section

This is the second most important section after the physics section. The user can specify between various types of simulations: quasistationary, transient, small signal, harmonic balance but also optical or thermal. Each simulation type must have a goal defined; this can be either an electrode that will be ramped, the voltage of a voltage generator or the power of an optical source that will be switched on.

7) and 8) Device and System (Mixed Mode)

The Device and System sections are part of the Mixed Mode feature. This special feature allows the simulation of entire networks both large signal, small signal, noise analysis and harmonic balance. A physical device with its corresponding (2D or 3D) mesh gets a unique name assigned in the Device section, name by which can be later addressed. Various devices and circuit elements are connected via network nodes, all of them being listed in the System section. The voltages and currents computed via the drift-diffusion or hydrodynamic approach for the single devices are linked via these nodes to the external circuit resulting in a SPICE like environment. Thus a trade-off between accuracy and speed is achieved.

3.4.3 Numerical Methods

The default method of solving the nonlinear system of PDEs is the approach presented by Bank and Rose in [147]. We have the system of three partial differential equations, consisting of the Poisson, electron and hole continuity equation (for the hydrodynamic case and the extra three equations see [35]), which we call g . If we express the hole and electron density via the quasi Fermi levels, denoted by w and v , than we have three equations with three unknowns: the potential u , v and w . The triplet can be substituted by one variable z and we have to find the roots of $g(z) = 0$. The three equations g_1 to g_3 have the form [147]:

$$\begin{aligned} g_1(u, v, w) &= -\Delta u + e^{u-v} - e^{w-u} - k_1 = 0 \\ g_2(u, v, w) &= \nabla \mu_n e^{u-v} \nabla v + k_2 = 0 \\ g_3(u, v, w) &= -\nabla \mu_p e^{w-u} \nabla w + k_2 = 0 \end{aligned} \quad (3.4.3)$$

and g' the Jacobian of the PDE system can be expressed as [147]:

$$g' = \begin{bmatrix} -\Delta * + (e^{u-v} + e^{w-u}) * & -e^{u-v} * & -e^{w-u} * \\ \nabla(\mu_n * e^{u-v} \nabla v) & -\nabla(\mu_n * e^u \nabla(-e^{-v} *)) & 0 \\ \nabla(\mu_p * e^{w-u} \nabla w) & 0 & -\nabla(\mu_p * e^{-u} \nabla(e^w *)) \end{bmatrix} \quad (3.4.4)$$

The standard approach for find the roots of $g(z)$ is via the Newton method. The prescriptions of the newton method in our case can be written as:

$$g + g'x = 0 \quad (3.4.5)$$

$$z^j - z^{j+1} = \lambda x \quad (3.4.6)$$

where z^j, z^{j+1} also graphically represented in Fig. 3.10:

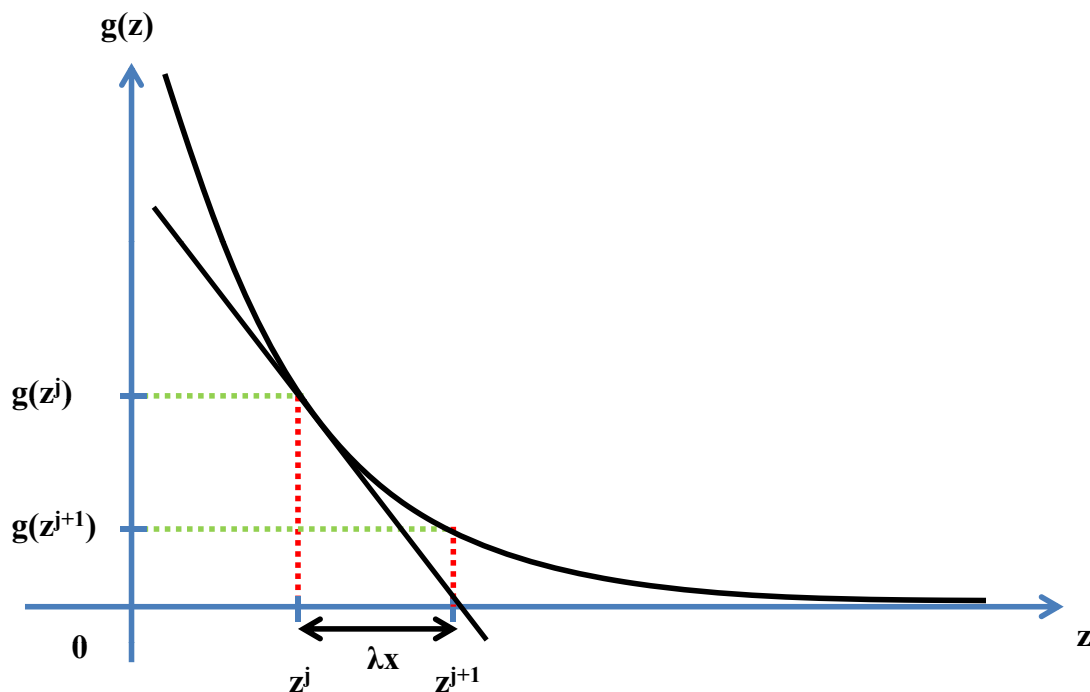


Figure 3.10: Illustration of the Newton algorithm. Figure redrawn from [35].

From Fig. 3.10 we can also see how the Newton algorithm works: we basically use the first derivative (the slope) of the function to obtain the root. The starting point, z^j , is an initial guess for u, v and w . It is a good habit to always initialize the simulation with 0 V external bias (equilibrium) because the first guess for u is near the intrinsic electrochemical potential and for v and w the intrinsic hole and electron concentrations. For the initial guess z^j we take the function $g(z^j)$ and construct the first derivative using the Jacobi operator g' shown in formula 3.4.5. We then follow the slope until it intercepts the x -axis ($g' = 0$) taking the intercept point z^{j+1} as our new z^j . We continue with this iteration and eventually the intercept point of the first derivative will bring us nearer and nearer to the root of g till one of the break criteria is fulfilled.

Several break criteria are implemented in the simulator for the Newton scheme: one involving the norm of g , the right hand side (RHS) and two involving the error in the iterative step (λ/z). If the norm of the RHS is below 10^{-5} the Newton iteration is successful and the simulation evolves to the next bias point. For the error in the iterative step one formulation of the break criterion is:

$$\frac{1}{\epsilon_R} \left\| \frac{\lambda x}{z^j + z_{ref}} \right\| < 1 \quad (3.4.7)$$

As one can see this formulation uses the relative error ϵ_r in each step of the iteration as criterion. This error has the value $\epsilon_r = 10^{-digits}$ with the user defined choice of digits (default also 5). A reference parameter z_{ref} is introduced to ensure stability for very small z in the denominator and its value can be also modified by the user.

An equivalent break criterion uses the absolute error ϵ_a :

$$\left\| \frac{\lambda x}{\epsilon_R z^{-j} + \epsilon_A} \right\| < 1 \quad (3.4.8)$$

where $z^{-j} = z^j / z^*$, z^* being a normalization factor (thermal voltage in the Poisson equation or $n_i = 1.48 \times 10^{10} \text{ cm}^{-3}$ for electron or hole continuity).

The user can select freely between the break criteria and modify the default values of the RHS, relative and absolute error.

Although solving the fully coupled system g in each step of the Newton algorithm is quite demanding, the convergence is very good, usually only 3 to 8 iterations are necessary [147].

A different solving scheme is also implemented, the Plugin better known as Gummel iterations [148]. This scheme was the traditional scheme for many years due to its rather simple approach and superior speed. Instead of solving the coupled non-linear system $g(z)$, the Gummel iteration method solves each subsystem g_1, g_n separately. After finding the solution of g_1 it moves to g_2 and so on until all g_j are solved consecutively.

4 Monte Carlo Simulations

4.1 Simulation Flow

After having described the models and the physics implemented in the simulator – the theory part – we move to the practical part, where we describe the typical process flow for a Monte Carlo device simulation.

The first step in the simulation flow, as can be seen in Figure 4.1 is the executable “mkbands”. This program generates the electronic structure and the phonon spectra for the various materials that build up the device. Each material must have a material file, which serves as input for “mkbands”. The material file contains all physical parameters – like lattice type, lattice parameters, dielectric constants and so on– necessary for the Empirical Pseudopotential Method (EPM) and for the Valence Force Field Method (VFFM).

Consequently in order to simulate our InAs nanowire we first have to run “mkbands” with the InAs.mat file. All parameters used in this file have been carefully chosen from literature, either from experimental studies or ab initio calculations [149, 150]. Equally important in the electronic structure and phonon spectra calculation besides the physical parameters of the material file is the discretization of the first Brillouin Zone (BZ) in momentum space.

Two different grids, an electron and a phonon grid must be specified before running the “mkbands”. The general approach is to create non-uniform grids with more cells in the vicinity of the conduction band minima (or maxima for valence bands) where the dispersion relation has its steepest slope. These cells are always populated with carriers and here large part of the scattering occurs. For higher energy regions of the first Brillouin Zone a coarser subdivision of the momentum space may be used since those regions are loosely populated.

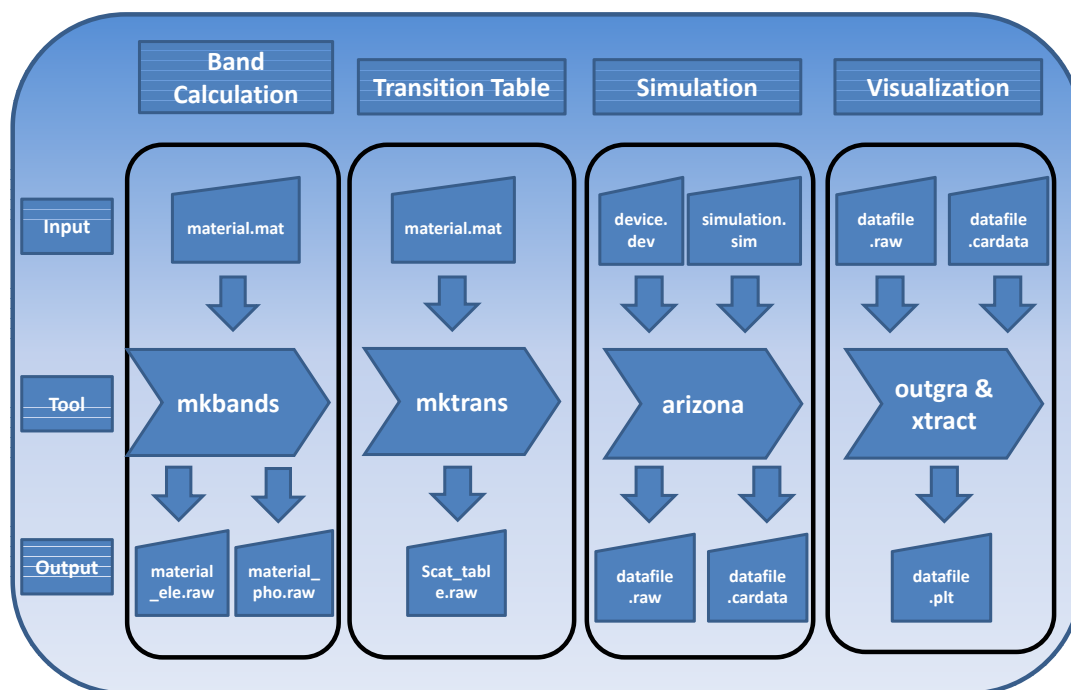


Figure 4.1: Flowchart of a CMC simulation.

In the first statement a uniform grid consisting of a cuboid with $40 \cdot 40 \cdot 40$ gridpoints in the k_x , k_y and k_z directions is defined over the first BZ. Such a uniform grid is mandatory for all material files; if we define a finer non-uniform grid later, the definition of the second more refined grid will overwrite the uniform grid. This is performed in the following statements: “ca cells” defines a subdivision in the momentum space and it has 4 user defined options.

The first integer in “ca cells” specifies to which band the discretization applies, a number equal to 1 specifies the first conduction band while -1 indicates the first valence band. Then follows the range in momentum space where this discretized grid should be applied: these two numbers are between 0 and 1 since the axes have been normalized with π/a . Finally the last integer indicates how many subdivisions should be created in the region earlier defined. The same procedure also holds for the “phonon cells” in the phonon grid definition. After running the executable two output files are generated: one contains the electronic dispersion and the other one the phonon spectra.

In Fig. 4.2 and Fig. 4.3 the band structure and the phonon spectra for InAs are presented, obtained with the CMC simulator and compared with standard literature data [149,150]. In Figure 4.4 the density of states of InAs calculated

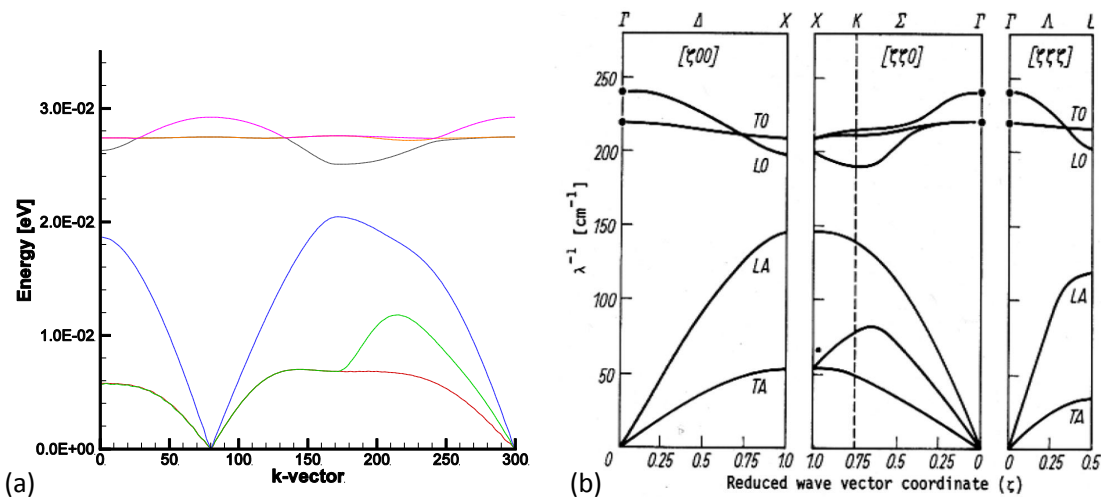


Figure 4.3: (a) InAs phonon dispersion obtained with mkbands (b) InAs phonon bands taken from [149].

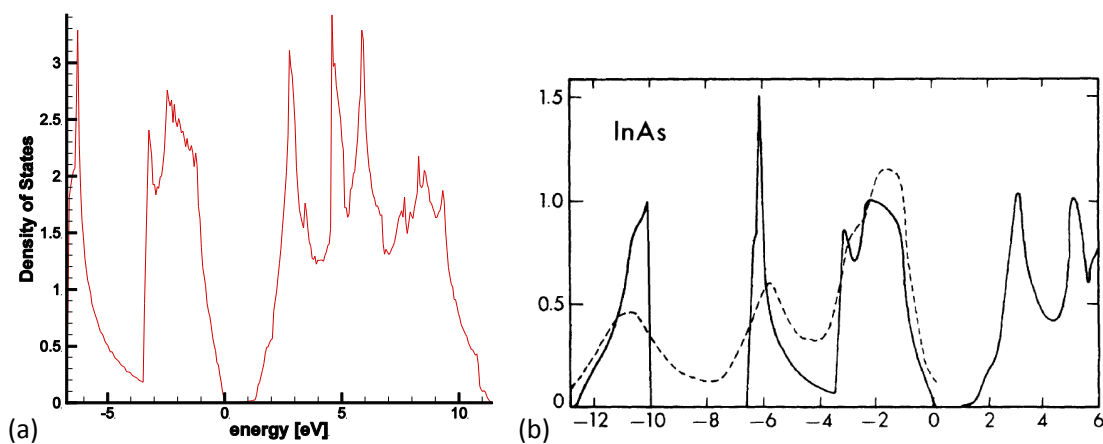


Figure 4.4: (a) Density of states obtained with the CMC framework (b) Density of states for InAs from [150].

A typical Device Setup File contains 7 different sections. The first section defines the global device dimensions, expressed both in meters and in total number of simulation cells. One limitation of the CMC code can be mentioned here: the cells are only rectangles in 2D and cuboids in 3D which makes it very difficult to simulate rounded shapes like nanowire cross-sections in 2D or cylinders in 3D. For the dimensions of the device both in real space and in simulation cells 2 integer triplets need to be specified by the user, representing the device extensions in x , y and z directions. In the case of our nanowire we declare the following:

3d device dimension = 140, 32, 32, 1400e-09, 95e-09, 95e-09;

With the first triplet we specify 140 cells in the x-direction and 32 cells both in y and z-directions whereas the second triplet gives the dimensions of our nanowire device, 1.4 μm is the x-extension while the cross-section of the device measures 95 nm both in y and z-direction.

The user can then decide the size of the simulation cells with the “cell dimension” statement. This statement consists again of an integer triplet indicating the number of cells (starting and ending cells) that will have a specific value (in m).

For example, if we want to define the first 6 cells (from 0 to 5) in y-directions to have a dimension of 5 nm and the next 5 cells to have only 1 nm, we just have to write:

y cell dimension = 0, 5, 5e-09;

y cell dimension = 6, 10, 1e-09;

After the geometry has been defined we need to specify the doping profile of the device. For the 2D doping 4 integers denoting the four corners of the rectangle where the doping will be placed in the x-y plane have to be provided and also the doping density, so a total of 5 numbers. In the 3D case we need to specify the six corners of the cuboid which represents the doping placement box and again the doping density.

The next section is the contact and sheet region section where up to 6 separate contacts can be defined and an arbitrary number of sheet regions. Each contact must have a name, 6 integers representing starting cell and ending cell in all the 3 dimensions (4 integers in 2D) and the contact type which can be either Ohmic or Schottky. For the latter case also the Schottky barrier height needs to be specified as last argument in the contact definition. The contacts of our nanowire transistor are defined as followed:

3d contact = source, 0,6,6,0,25,25,YES,YES,SOLID,OHMIC,0;

3d contact = drain, 139,6,6,139,25,25,YES,YES,SOLID,OHMIC,0;

3d contact = gate, 0,6,0,139,31,0,NO,NO,SOLID,OHMIC,0;

3d contact = gate, 0,31,0,139,31,31,NO,NO,SOLID,OHMIC,0;

```
3d contact = gate, 0,6,31,139,31,31,NO,NO,SOLID,OHMIC,0;
```

We have a source contact at the first cell in x-direction (0) and the drain contact at the last cell in x-direction (139) with a rectangular cross-section in the y-z plane, from cell 6 to 25. The gate contact stretches in the x-direction over all x cells and covers the top and side facets of the nanowire transistor (wrap-gate).

Very similar to the contacts the sheet regions used to introduce sheet charges (positive or negative) have the placement definition. The only difference arises in the last two arguments: instead of Ohmic or Schottky and the barrier height, in this case we specify on which side of the simulation cell the sheet charges should be placed (EAST, WEST, NORTH, or SOUTH) and finally as last argument the surface charge density.

In fourth section the user can define the material placement and properties. In our case for example we specify where the InAs nanowire should be placed inside the simulation area (the device previously defined with the “3d device dimension”) and where the gate insulators, SiN_x should be placed. The assignment of InAs is done with the following command:

```
3d material properties = 0,6,6,139,25,25,15.15,OPEN-INITQ,0,0,InAs,InAs.mat;
```

We assign to all simulation cells in x-direction and to the 6-th to the 25-th cell in the y-z plane the material InAs with the properties of the InAs material file (the scattering table for InAs). We also specify the low frequency permittivity (although both low and high-frequency epsilons are in the material file as well) and the conduction band and valence band offsets (in this case InAs is the reference material so both offsets are “0”, “0”). The keyword “OPEN INITQ” is a flag used for regions open to charge transport like the channel regions. For insulators (like gate dielectric) no DC current will flow (unless the tunneling model is activated) therefore they are “CLOSED” to charge transport. The MC code will not solve the Boltzmann Transport Equation in the closed regions; they will only have an electrostatic contribution via the Poisson solver. This is in fact how we define the SiN_x gate dielectrics covering the nanowire.

The fifth section is the so-called “region” section where time averages of the various quantities are computed, extremely useful for example in the calculation of the total CMC currents. A “region” definition starts as always with the grid coordinates where the rectangle or cuboid in 3D will be placed and has

some particular flags; to specify a current region the flag “c” must be placed. Within this region the total current, which has a convection and a displacement component will be calculated employing the Ramo-Shockley theorem [34]. The “c” regions are assigned to a contact “cregion to contact”, for example source or drain, and have the great benefit of being usually not so noisy as the contact currents, since they are averaged over a volume. A current region cannot contain a contact (in the Ramo-Shockley theorem no charge sinks/sources are permitted) and they should be placed at least at a few simulation cells away from the injecting contacts in order to allow charge carrier thermalization. Other useful flags are the “d” flag which will compute the distribution function inside that region and the “b” flag which turns down all scattering mechanism making the transport in the selected region ballistic.

Section number 6 provides options for an external (parasitic) network. The CMC simulator offers the unique possibility of performing both small-signal and large-signal high-frequency analysis of a device. After successfully running a DC simulation we can choose a bias point and deliver it as input for the high-frequency simulation. Three network solvers are available for HF-analysis: ACSMALL, HB and FDTD. The first one is used for small signal characterization and the Harmonic Balance (HB) and Finite Difference Time Domain (FDTD) are used when the small signal assumptions are not valid anymore. We can select what solver to use and a few solver settings but also the entire external network.

With the following code we define a load $Z_L = 100 - j20$ at the transistor output (drain):

```
network = drain, HB, ZVAL, REG,
100, 100, 100, 100, 100, N/A,N/A,N/A,N/A,N/A, [Re]
N/A, N/A, N/A, N/A, N/A, N/A,N/A,N/A,N/A,N/A, [+Im]
20, 20, 20, 20, 20, N/A,N/A,N/A,N/A,N/A; [-Im]
```

The load is defined at the fundamental frequency as well as for the first 4 harmonics f_1 , f_2 , f_3 and f_4 . External parasitic networks can be placed also at the input and they can be either inductive or capacitive.

Finally the last section in the Device Setup File provides some numerical option for the multi-grid Poisson solver and convergence criteria. There are multiple schemes for the error relaxation (smoothing): the point-Gauß-Seidel (PGS) which acts on individual grid points and the line-Gauß-Seidel (LGS) which acts on an entire direction first – the x-direction for example – and subsequently on individual points for the other grid directions. A total of 10 macros are defined using all the combinations of PGS and LGS on the x, y and z-directions, below some examples are shown:

ZEBRAX = applies LGS algorithm on the x-direction and PGS on the grid points in y and z-direction

ZEBRAY = applies LGS algorithm on the y-direction and PGS on the grid points in x and z-direction

ZBTHYX = applies *ZEBRAY* and then *ZEBRAX*; it is robust and useful for non-uniform grids in more than one direction

All the macros and their description can be found in [34]; other options like solver iterations and solver convergence can be specified as well in this section. With this numerical options section we conclude the Device Setup File definition. As mentioned earlier, beside the Device Setup File, the Simulation Setup File is the second file needed for the input of “arizona”.

The first section of the simulation file contains some general simulation parameters: the simulated energy range, the simulated carrier number and the desired transport model. The user can choose between the Cellular Automaton (CA) approach, a classical Ensemble Monte Carlo approach or the hybrid approach. In the hybrid approach the CA method is favored except for some user-defined energy intervals where the EMC method is enforced. This approach can be useful if we want to know precisely what type of scattering event occurs in a given energy interval. The CA approach is very fast but no information is recorded on the type of scattering event in the transition table. Adding also this information to the transition table would make the size roughly 4 times larger, far too big to be loaded into the computer memory (RAM).

Another physical parameter that needs to be specified is the device temperature. Since the temperature affects the scattering (it directly influences the phonon

population) one should also modify the temperature in the material file accordingly. A new transition table needs to be computed with the desired temperature using “mktrans” and only afterwards can the “arizona” code be executed. Another simulation parameter that requires special attention is the simulation time. Two values must be provided by the user: the Poisson/Maxwell timestep, and the Time Of Free-Flight (TOF). As a general rule the Poisson timestep should be smaller than half the plasma frequency. The plasma frequency is defined as:

$$\omega_p = \left(\frac{ne^2}{\epsilon_r \epsilon_0 m^*} \right)^2 \quad (4.1.1)$$

The TOF should be smaller than the Poisson timestep, in fact it should be smaller than the largest scattering time for the specific energy and material choice. Otherwise the charge carrier might exit the first BZ during a the TOF timestep without scattering and the simulation will crash. We see therefore that the TOF is the characteristic timestep (ΔT) of the entire simulation, the total simulation time should not be larger than a few thousands of TOFs otherwise the execution time will take too long.

After these simulation parameters have been declared we can define the actual simulation. We perform two types of simulation: bulk simulation and device simulations.

Bulk simulations don’t require a Device Setup file since the carriers are tracked only in momentum space. Therefore no geometry details are needed, the simulator assumes an ideal infinite slab of the particular material. We only have to define the applied external bias for the simulation, in this case directly as electric field value. Such simulations are extremely useful in the characterization of charge carrier transport in a specific material and for the extraction of transport properties, such as velocity versus electrical field profiles. Such a profile has been simulated for bulk InAs and is displayed in Figure 4.5 and compared with data from literature [151]. We can see that the agreement is very good: the characteristic velocity overshoot at around 200 kV/m is nicely reproduced as well as the saturation velocity value.

For device simulation we need to specify the potential values applied on the electrodes. A typical definition would have the following form:

potential value = 11, Vg050Vd000, 0, YES, source,gate,drain. . .0.00,0.50,0.00

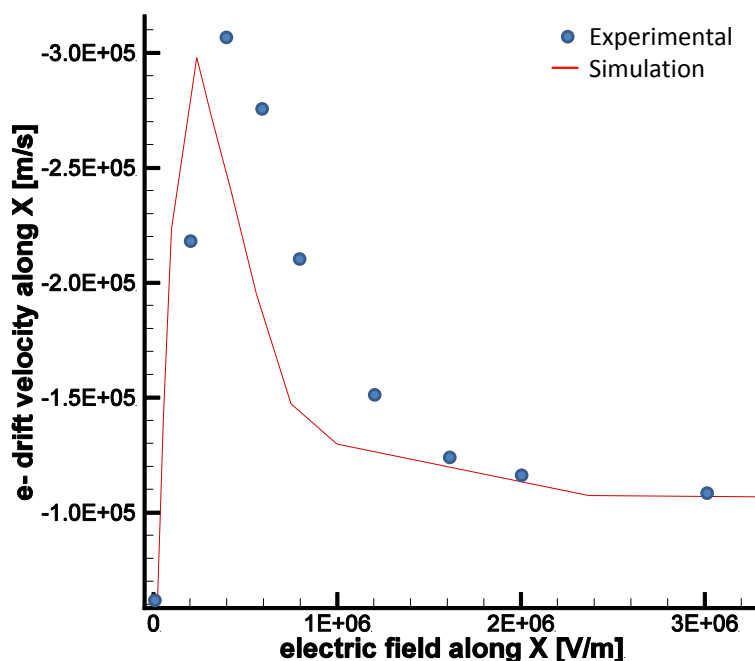


Figure 4.5: Simulated drift velocity vs. electric field (red line) compared to results from [151]] (blue circles).

12e-12, 4.5e-12, 12e-12,;

The first number is the identifier of the applied potential value, in a DC sweep we have obviously more than one potential value defined. The potential ID is linked with the third number which is the ID of the previous step; this way the simulator looks at the output file of the previous step to retrieve information about carrier data. In this case the ID of the previous step is "0" which means the simulation has no previous step, the arizona executable will start from scratch. The second string in the definition is the name under which the simulation output file will be saved. The fourth string is a flag "YES/NO" and decides if a "cardata" file will be saved or not. "Cardata" files contain the complete carrier data, like carrier energy, momentum distribution, velocity, etc. Next comes a list of the electrodes "source, gate, drain" and the associated potential values. In this example only the gate is ramped at 0.5 V while the source and drain remain at zero bias. Finally three values are needed to define the total simulation time, all given in seconds. The first one is the actual simulation time; it should be taken long enough to ensure steady state for device operation. The second time entry is used to specify the averaging interval for quantities like current densities, carrier velocities, etc. Its definition begins from the end of the simulation time

so in this example the averaging interval would be [7.5-12] ps. The last entry defines the interval used for the time evolution interval and it should be equal to the entire simulation time. This way we ensure that the entire transient response of the device is saved.

4.2 Results

The first simulation task consists in an accurate fitting of the nanowire DC characteristic from Fig. 4.6; only then can the high frequency analysis begin. The best fit obtained with the CMC simulator is presented in Fig. 4.7b together with a cross-section of the NW transistor in Fig. 4.7a. Also visible in the transversal cut is the doping profile of the nanowire, one of the most important characteristics (properties) of the transistor, with huge impact on the device DC and HF performance. In the next paragraphs we would like to elaborate on the choice of the doping profile inside the nanowire.

It is well known that for bulk InAs a very high concentration of donor states exists close to the surface, leading to electron accumulation and Fermi level pinning [76,77]. For the case of low dimensional quantum systems, like nanowires, no studies have been published until very recently [78,79].

Karlström *et al.* [152] analyze capacitance curves and with the help of electrostatic simulations are able to extract information about doping densities and suggest the existence of surface charge density. The study of Astromskas *et al.* [78] differentiates for the first time between the core doping and the surface charge density, which is estimated to be in the range $0.5 - 2.5 \cdot 10^{13} \text{ cm}^{-2}$. Their estimations are supported by 3D simulations similar to those in [152]. Halpern *et al.* [79] report for the first time the direct measurements of surface states in a InAs nanowire based transistor. The method of choice is a mix between Kelvin Probe Force Microscopy (KPFM) and again analytical modeling for the interpretation of results. The measurements reveal an exponential donor surface states density of 10^{13} cm^{-2} situated just below the conduction band.

These recent findings confirm that the surface electron accumulation layer characteristic for bulk InAs is also present in low dimensional systems like nanowires. We therefore assume in our simulations that almost all electrons are accumulated near the surface of the nanowire. Since effects like Fermi level pinning are not

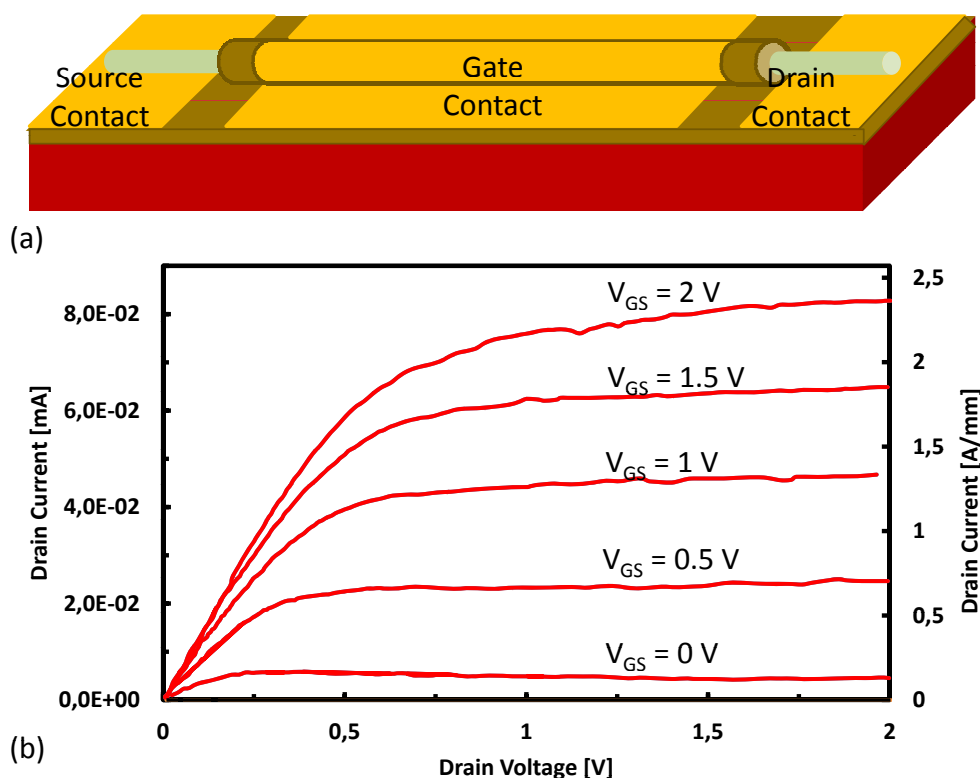


Figure 4.6: (a) Schematic of the InAs nanowire from [24] (b) Measured output characteristic of the same nanowire.

included in our CMC simulator we emulate this behavior by placing a large n-type doping (10^{18} cm^{-3}) over the first 2 nm of the nanowire cross section, followed by a moderate doping of 10^{16} cm^{-3} over the next 3 nm and finally a core doping of 10^{15} cm^{-3} for the remaining 25 nm.

The simulator also offers us the possibility to place fixed interface charges, either positive or negative. We use this feature in order to emulate the interface trap states. Although the fixed charges can only duplicate the effect of either empty or fully occupied surface trap states this is not so severe; the trapping and detrapping times for trap states are several order of magnitude higher than the time of free flight or the Poisson time step [154]. This would imply huge simulation times which in turn would make the CMC approach unpractical. We place fixed positive charge with a concentration of $1.7 \cdot 10^{11}\text{ cm}^{-2}$ on the side and upper facets of the nanowire (those covered by the wrap gate). It is reasonable to assume that at least 2 percent of the donor surface states will remain always unoccupied, having a purely electrostatic impact on the DC characteristic. On the bottom facet we place negative fixed charges with a concentration of $5 \cdot 10^{12}\text{ cm}^{-2}$

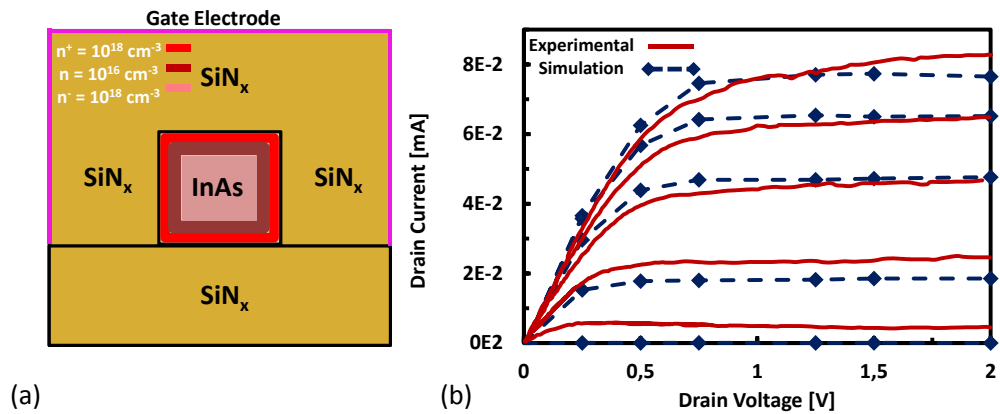


Figure 4.7: (a) Cross-section of the simulated NW with doping profile (b) Simulated output characteristic vs. measured data. Figure taken from [153].

to emulate trapped electrons at the InAs/SiN_x interface. Since the nanowire is grown vertically and then has to be removed from the growth substrate and placed laterally on a second substrate we can assume that this bottom interface is pretty rough compared to the side or bottom facets.

All the described nanowire doping profiles and fixed interface charges can be seen in Fig. 4.7a whereas the simulated versus measured DC characteristic can be seen in Fig. 4.7b. There is a good agreement for the values of the drain currents in the saturation region for all gate voltages in the range 0.5 - 2 V. Also nicely reproduced are the values of the ON resistance for the linear regime (the slope of the drain current before entering saturation) and the spacing of the different output curves. Having accurately fitted the output curves we can make use of the huge amount of data stored after each CMC simulation to get a deeper understanding of the underlying physics during device operation.

In Figure 4.8 we see the carrier momentum distribution inside the first Brillouin zone during operation. The four snapshots correspond to four different bias points, all at $V_{ds}=0.5$ V but at various gate voltages: 0.5, 1, 1.5 and 2 V. We can nicely see how the increasing gate voltage modifies the band population. For the smallest voltage ($V_g=0.5$ V) all electrons reside within the first band minima around the Γ point in the center of the Brillouin zone. When reaching a gate voltage of 1 V the electrons have enough energy and populate the second minima, the so called L-valley. For the maximum simulated gate voltage of 2 V we see that the L-valley is almost fully populated.

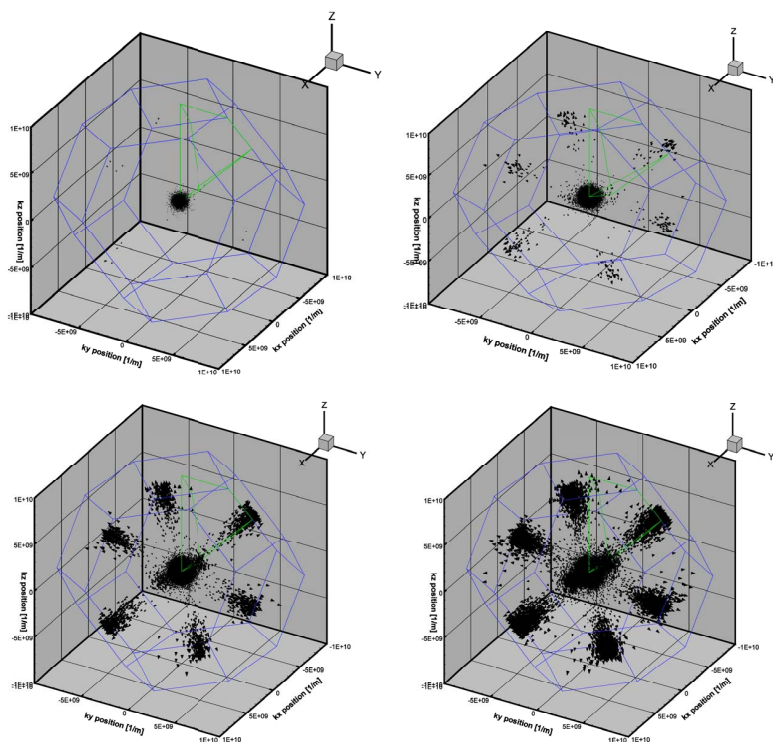


Figure 4.8: (a) Momentum distribution of conduction electrons inside the Brillouin zone at drain voltage of 0.5 V and gate voltage 0.5 V. (b) Same plot at gate voltage 1 V, (c) at $V_G = 1.5$ V (d) and 2 V. Figure taken from [153].

Before going to the small signal characterization we perform a sensitivity analysis of the nanowire doping profile and its influence on the DC characteristic.

In Figure 4.9a the n-type doping of the nanowire is taken constant across the entire volume and has a value of 10^{17} cm^{-3} . We can see that the drain current and ON resistance in the linear regime get overestimated for all the gate voltages. In the subsequent figures (Figure 4.9b and c) the constant doping is gradually increased from 10^{17} cm^{-3} to $2 \cdot 10^{17}$ and $4 \cdot 10^{17} \text{ cm}^{-3}$ in the entire nanowire. As the bulk doping increases we observe a decrease in the maximum current, for $N_D = 4 \cdot 10^{17} \text{ cm}^{-3}$ the drain currents saturate at a value of $52 \mu\text{A}$. At the intermediate value of $2 \cdot 10^{17}$ the maximum value of the drain current is accurate, however the spacing between the output curves for the various gate voltages doesn't reproduce the experimental data at all. The main reason why the current decreases with doping values higher than $2 \cdot 10^{17} \text{ cm}^{-3}$ is the increase in carrier scattering and the resulting lower effective mobility. Since we have a limited volume (with a diameter of only 35 nm) increasing the number of dopants above

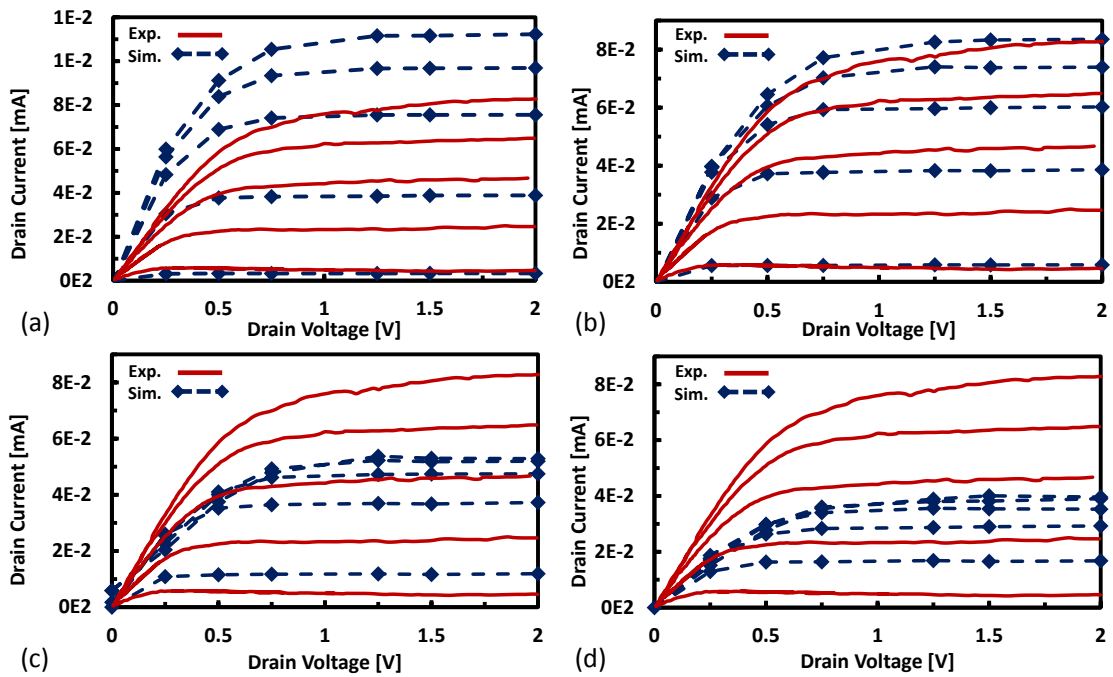


Figure 4.9: (a) Simulated IV characteristic for a constant bulk doping of 10^{17} cm^{-3} . (b) Simulated IV characteristic for a constant bulk doping of $2 \cdot 10^{17} \text{ cm}^{-3}$. (c) Simulated IV characteristic for a constant bulk doping of $4 \cdot 10^{17} \text{ cm}^{-3}$. (d) Simulated IV characteristic for a constant bulk doping of 10^{17} cm^{-3} and positive fixed surface charges $Q_+ = 1.71 \cdot 10^{12} \text{ cm}^{-3}$. Figure taken from [153].

a certain level will not further increase the number of available electrons (they simply don't fit). However the mobility has to suffer, which translates in lower currents and the loss of electrostatic control for the gate electrode at higher V_g (the curves overlap in Figure 4.9c for $V_g > 1$ V. In Figure 4.9d the nanowire is simulated with a constant doping of 10^{17} cm^{-3} and a concentration of positive fixed surface charges $n_{s+} = 1.71 \cdot 10^{12} \text{ cm}^{-2}$ on the top and side facets. Also in this case the current is severely underestimated and the curves overlap for $V_g > 1$ V. A large concentration of fixed positive charges (acting like always empty donor trap states) effectively screens the gate potential and no accumulation layer builds up when increasing the applied voltage on the gate. The drain current is therefore almost insensitive to V_g .

Since this behavior is not observed in the experimental curves we draw the conclusion that in reality, similar to our simulation, only a very small percentage of surfaces states remain always unoccupied, otherwise we would have seen

their electrostatic impact on the output characteristic. Having validated our model with the DC measurements, we move now to the high frequency characterization. For this purpose we perform a small signal analysis, extract the elements of the admittance (Y) matrix, and from there all relevant quantities like cut off frequency (f_T) or maximum frequency of oscillation (f_{max}).

The method used to perform the small signal simulations has been described in great detail elsewhere [85], hence we will only mention the procedure in brief. By applying two voltage perturbation steps, one on the gate electrode and a separate one on the drain electrode we obtain a step response in the drain and gate current respectively. By computing the Fourier transformation of these step perturbations, which can be interpreted as a superposition of sinusoids with different frequencies and amplitudes, we can easily obtain the complex admittance of our two port over a large frequency range and hence the entire Y-matrix.

In Figure 4.10a we can see the drain current response to a step perturbation at the gate electrode. With the second perturbation at the drain and by using the definition of the short circuit gain current gain as:

$$h_{21} = \frac{i_d}{i_g} = \frac{Y_{21}}{Y_{11}} \quad (4.2.1)$$

we can estimate the cut-off frequency, f_T . In Figure 4.10b the simulated current gain is presented with a highlight on the 0 dB intercept point which defines the cut off frequency. A value of 65 GHz is obtained for f_T , almost one order of magnitude higher than the measured value in [24]. Similarly from the definition of the unilateral transducer gain as:

$$G_{TU,max} = \frac{|Y_{21} - Y_{12}|^2}{4 [Re(Y_{11})Re(Y_{22}) - Re(Y_{12})Re(Y_{21})]} \quad (4.2.2)$$

we can estimate the maximum frequency of oscillation, f_{max} .

From the simulated unilateral transducer gain, shown in Figure 4.10c we obtain $f_{max}=112$ GHz, again almost one order of magnitude higher than the experimental values [24]. We can make use of the complex admittance matrix elements and get an idea about the intrinsic transistor capacitances. For example from the Y_{12} element we can derive the intrinsic gate drain capacitance as:

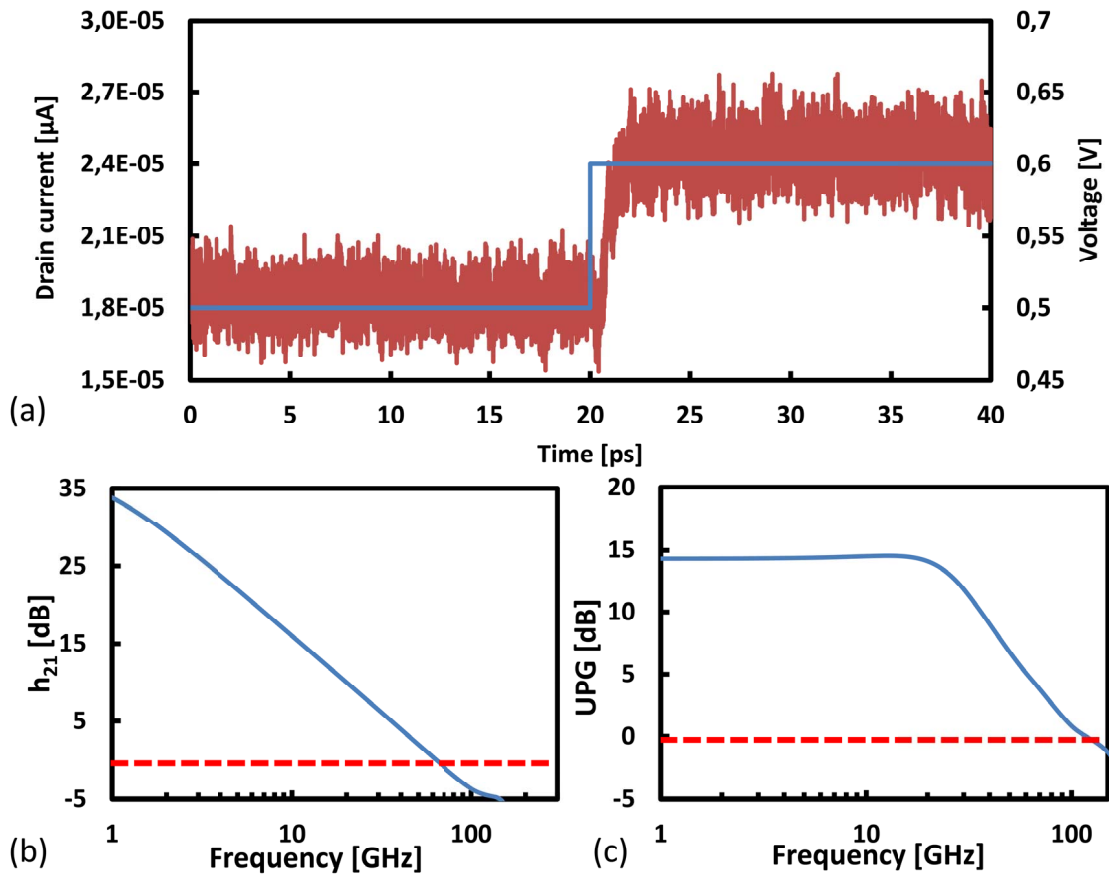


Figure 4.10: (a) Simulated gate voltage perturbation (blue line) and drain current response (brown). (b) Simulated short circuit current gain (h_{21}). (c) Simulated Unilateral Power Gain (UPG). Figure taken from [153].

$$Y_{12} = -j\omega C_{gd} \quad (4.2.3)$$

In Figure 4.11 we examine the behavior of Y_{12} over frequency and by extracting the slope we obtain an estimate of the C_{gd} . An value of 70 aF is obtained for the gate-drain capacitance, if we assume a similar value for C_{gs} we get a total intrinsic gate capacitance of around 150 aF which is more than one order of magnitude lower than the parasitic pad capacitances measured in [24]. The values reported by Blekker *et al.* [24] are in the range of 1 to 10 fF for the parasitic pad capacitances. Of course it comes as no surprise that the high frequency performance is so poor. It would be also interesting to compare these values for the extrinsic capacitances C_p with some values of C_p in standard silicon technology.

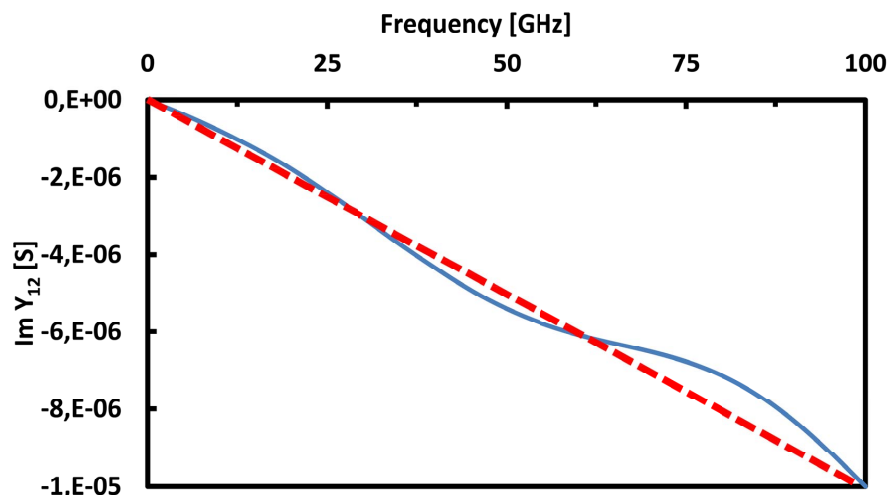


Figure 4.11: Extracted gate-drain capacitance (C_{gd}) from the imaginary part of Y_{12} shown in blue, the linearization in dotted red. Figure taken from [153].

A recent study by Mueller *et al.* [155] determines all the contributions to the parasitic capacitance like - fringe capacitance, gate-to-poly capacitance, corner capacitance and gate-bulk capacitance – for a 65 nm silicon MOSFET. The total C_p has a value of around 200 aF, so comparable with the intrinsic gate capacitance and significantly lower than those in [24].

Our next HF-analysis investigates the influence of the f_{max} with increasing gate resistance. In Figure 4.12 we see the unilateral power gain plotted versus frequency for different values of R_g from 5 ohm to 5 MOhm; the impact of the gate resistance starts to become significant for gate resistance values larger than 5 k Ω . For $R_g=50$ k Ω the f_{max} drops to 35 GHz and for 5 M Ω it is less than 10 GHz.

These results suggest that the intrinsic performance of the nanowire transistor is around one order of magnitude higher and the parasitic elements are responsible for the poor performance. Johansson *et al.* [26] recently demonstrate record high frequency performance of InAs nanowire transistors also by decreasing the parasitic elements (especially the capacitance) further experimental evidence that our assumptions are correct.

In order to fully characterize the nanowire transistor and its application as a high frequency amplifier we need to perform also a large signal analysis. This is required since for the power characterization of the FET the small signal

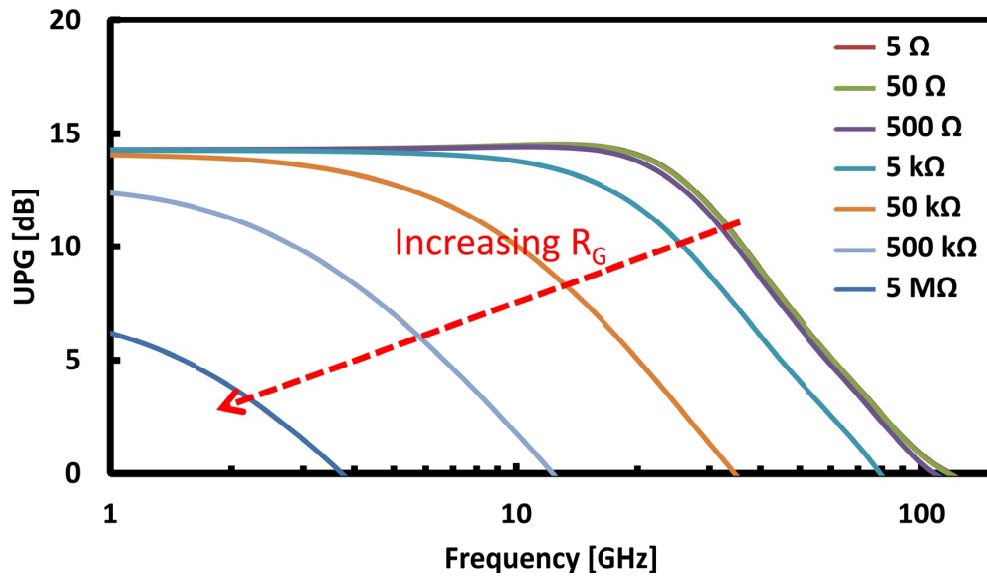


Figure 4.12: Influence of a gate resistor with different values on the Unilateral Power Gain. Figure taken from [153].

assumption is violated, the input AC signal amplitudes cannot be considered to be small when compared to the DC bias.

The method employed for the large signal simulation is the active load line technique, described in great detail in [86–88]. In Fig. 4.13 the power amplifier characterization at a fundamental frequency of 20 GHz is shown, a frequency where sufficient gain should be still available. To be more specific 10 dB in terms of short-circuit current gain, h_{21} and 14 dB in term of unilateral transducer gain UTG, as can be seen from Fig. 4.10.

We perform the RF power analysis at five different input powers, from -12 dBm and increasing until 7.5 dBm and a typical load Z_l of $100-20j$. The simulation procedure is the following: we start from a DC bias point obtained in an output simulation and apply an AC signal on the gate. We choose the DC bias of 1V on the drain and 0.5 V on the gate electrode which is stored in a special format, a “cardata” format. This format contains all relevant carrier data like carrier momentum, carrier energy or carrier position. Next an AC-signal is applied on the gate with amplitudes of 0.2, 0.4, 0.5, 1 and 1.5 V. After a few cycles the harmonic balance converges and the output waveforms can be extracted.

We can see the typical $P_{in} - P_{out}$ characteristic in Fig. 4.13: for the low input power levels the output power increases almost linearly with the input power

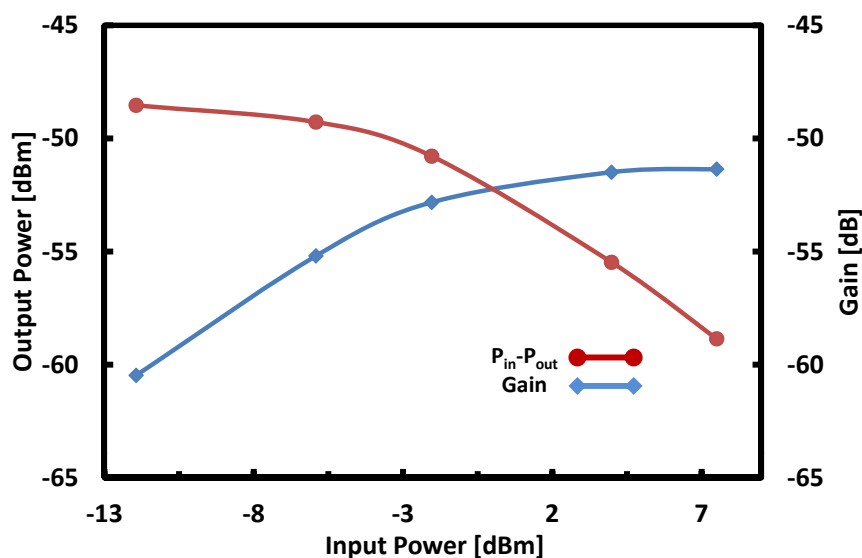


Figure 4.13: Power characterization of the amplifier; Input versus Output power and gain curve. Figure taken from [153].

and the gain is constant. The input referred 1dB compression point occurs at around -2 dBm, from there on the $P_{in} - P_{out}$ curve flattens and the amplifier enters the output power saturation regime. This regime is associated with a decrease in gain, the so called gain compression.

At a first look it may seem striking that the gain is negative, but if we remember the output characteristic from Fig. 4.7 it becomes clear that even for voltages of 2 V the nanowire cannot reach drain currents larger than a few tens of μA .

Nevertheless one can use the nanowires in an array like those presented in [26] for high frequency power applications, having an array of 1000 NW would translate in currents of tens of mAs and would basically shift the values on the left axis of Fig. 4.13. The input power would not increase since there is no current flowing through the gate electrode. A key aspect would be the smart contacting of the nanowire-array but solutions exist also for this issue as shown in [26]. Here we restrain our analysis to a single nanowire since we want to see the intrinsic behavior under large input power.

The generation of higher order harmonics due to the non-linearity of the amplifier is the main reason for the gain saturation. As higher order harmonics are generated more power gets transferred to them instead of being delivered to the load at the fundamental frequency, leading eventually to the output power

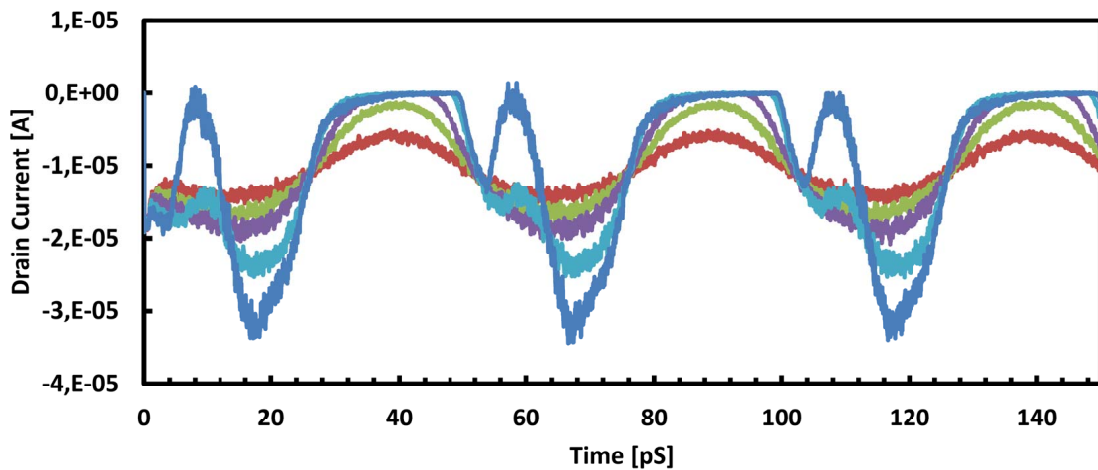


Figure 4.14: Drain current response for various the input power levels from -12 dBm to 7.5 dBm. Figure taken from [153].

saturation. The gain curve also starts decreasing as can be seen in the same Figure 4.13.

In Figure 4.14 the simulated CMC output currents for the five different input powers at the fundamental frequency of 20 GHz are given. We see that for the first three input signals the drain current waveforms look symmetric, the only difference being the amplitude swing. Differently the two drain current sinusoids, corresponding to the 1 and 1.5 V input voltage, are being distorted.

In order to verify our assumption that the power transfer to higher harmonics is the reason for the output signal distortion we can have a look at the harmonic power content.

In Figure 4.15 we can see the drain current amplitude at the fundamental frequency of 20 GHz and the first three harmonics for the five input powers. Our assumption is verified if we take a look at Figure 4.15c and Figure 4.15d. A sharp increase in the power content of the harmonics is visible, for the gate voltage of 1.5 V the current of f_1 reaches almost half of the DC current. Power gets delivered not only to f_1 but also f_2 and f_3 receive a non-negligible amount of power.

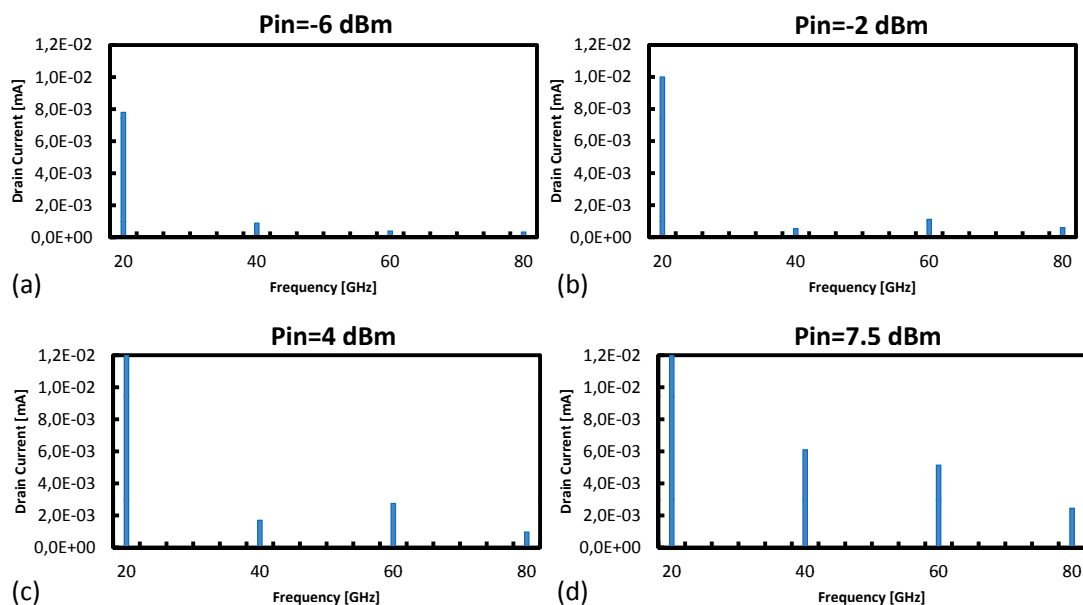


Figure 4.15: Transferred power to the first three harmonics for various input power. Figure taken from [153].

4.3 Conclusion

Using a state-of-the-art CMC simulator we have performed an extensive simulation study for the measured InAs nanowire. After reproducing the output characteristic successfully, we simulate the cut-off frequency, maximum frequency of oscillation and perform a RF power analysis of the device. We demonstrate with our simulations that the device intrinsic performance is at least one order of magnitude higher in terms of f_T and f_{max} , conclusion confirmed also by the recent study of Johansson *et al.* [26].

Several parasitic elements that cause the poor measured HF behavior of the device have been identified. From the simulations we also conclude that the device behaves linearly for AC input signals smaller than 1 V and can be used as a HF amplifier. The main message of our study is that the limiting factors for the HF performance of InAs nanowire based devices are the parasitic pad capacitances and contact resistances. Their optimization should be the main task of nanowire based applications.

5 Hydrodynamic Simulations

5.1 Results

Once the structure has been created and the command file has been edited the actual simulation can start. We perform a series of DC and small-signal (SS) simulation in order to characterize and estimate the nanowire FET performance both intrinsic and with parasitic elements. Afterward a sensitive analysis is performed by changing some key parameters of the transistor like unintentional doping or gate length.

The first type of simulation is a quasistationary simulation in order to fit the measured DC characteristic of the device presented in [24]. The gate voltage is ramped from 0 V to 2 V in constant 0.5 V steps and for each gate voltage step a drain voltage sweep also from 0 V to 2 V is executed. Thus we are able to reproduce the experimental measurements from [24].

In Fig. 5.1 we see again the structure of the simulated nanowire and the output curves for different gate voltages. We want to calibrate our simulations based on this data and see how the different physical models influence the output curves. A caption of the three dimensional InAs wire with three different simulated outputs is shown in Fig. 5.2.

The best fit is shown in Fig. 5.2b, which uses the two models described in detail in the last chapter, the hydrodynamic transport model and the velocity saturation model. A value of 3.75×10^7 cm/s has been used for the v_{sat} and the critical field is equal to 2 kV/m, both values are in good agreement with Monte Carlo simulations performed on InAs [144]. The values of the saturation current for different gate voltages are in excellent agreement over a large drain source voltage interval. Herein we stress that the simulations rely on an advanced

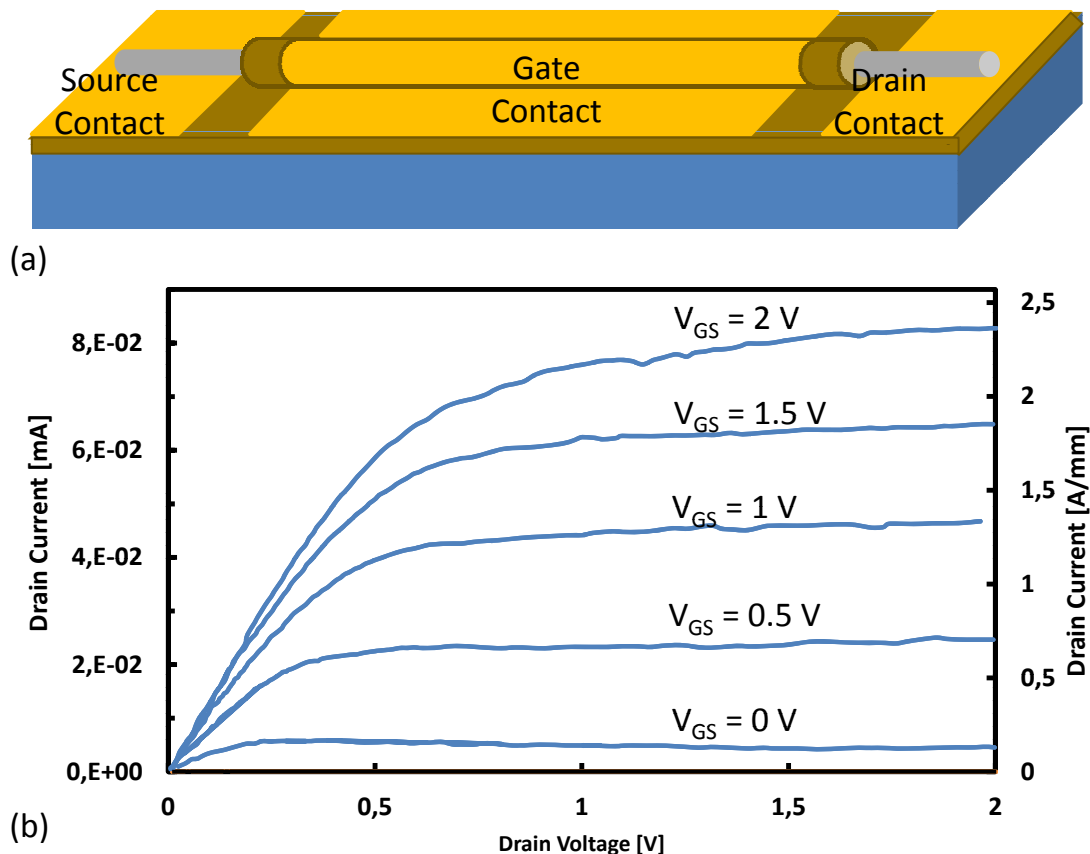


Figure 5.1: (a) Single wrap gate InAs transistor and (b) experimental output characteristic as reported in [24].

fully three dimensional modeling of the nanostructures without any other fitting constants or parameters.

One can see in Fig. 5.2c the simulated output curves without any velocity saturation and with a simple drift-diffusion model for the electron and hole current densities. As expected the current does not saturate for high gate voltages, the simulated I_{ds} for 2 V gate voltage overestimates by a factor of 3 the actual measured current.

In Fig. 5.2d the velocity saturation model has been activated without the hydrodynamic transport. For this case a severe underestimation of the current can be observed, all the curves basically overlap and saturate at a value of about $10 \mu\text{A}$. This simulation highlights the need for a more sophisticated transport model for structures well into the nanoscale regime. High fields present over nm regions (the wire radius) will induce hot electron effects, which are ignored if the simulation does not solve an extra set of energy balance equations coupled

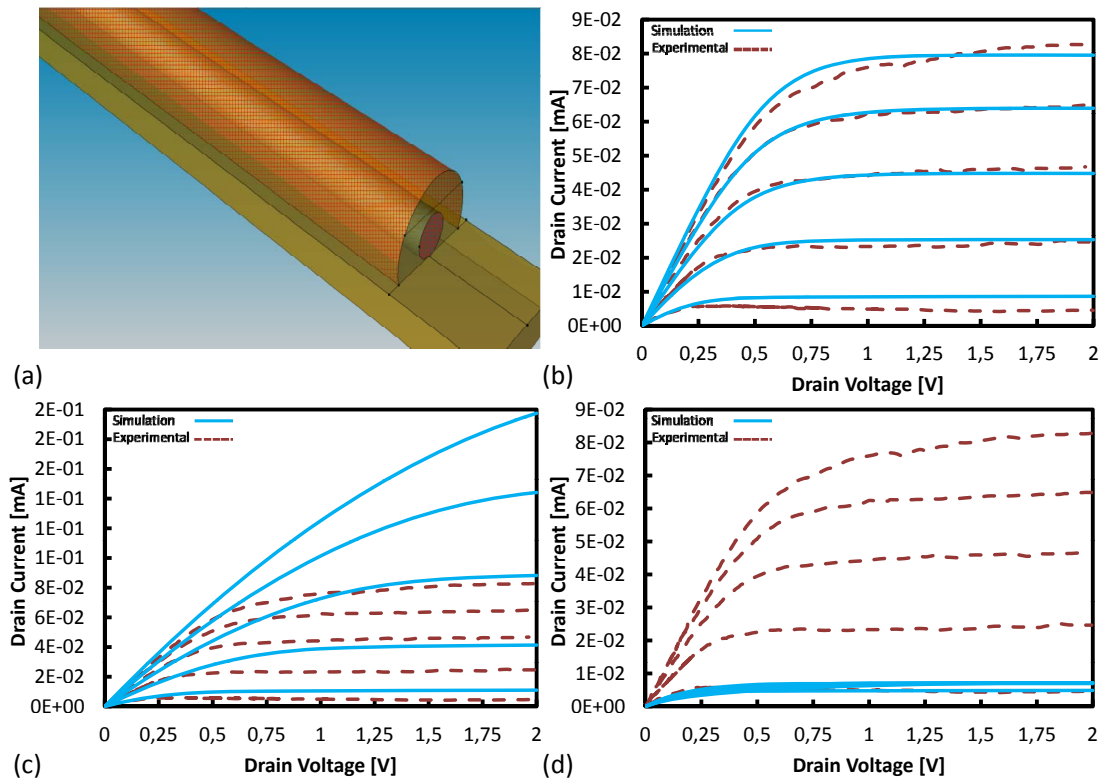


Figure 5.2: (a) Three-dimensional InAs Nanowire transistor model (b) Best fit with velocity saturation and hydrodynamic transport (c) Simulation results without velocity saturation and hydrodynamic model (d) Simulation results with velocity saturation and no hydrodynamic model. Figure taken from [156].

to the classical transport equations. This is the case in the simulation presented in Fig. Fig. 5.2d, where only a small fraction of the electron energy is taken into account, which results in a severe underestimation of the transistor output.

The last important physical model included in the Physics section is the interface trap states model. If for the bulk InAs material there are plenty of evidence that indicate a donor type defect state at the semiconductor surface [76,77] in the case of nanostructured InAs only a few experimental studies are available [78,79].

Since for a wrap gate transistor the gate dielectric/channel interface area is significantly larger than in the case of a conventional, planar structure, these trapping effects have a non – negligible impact on the electrical response of the nanowire FET and must be included in the an accurate modeling.

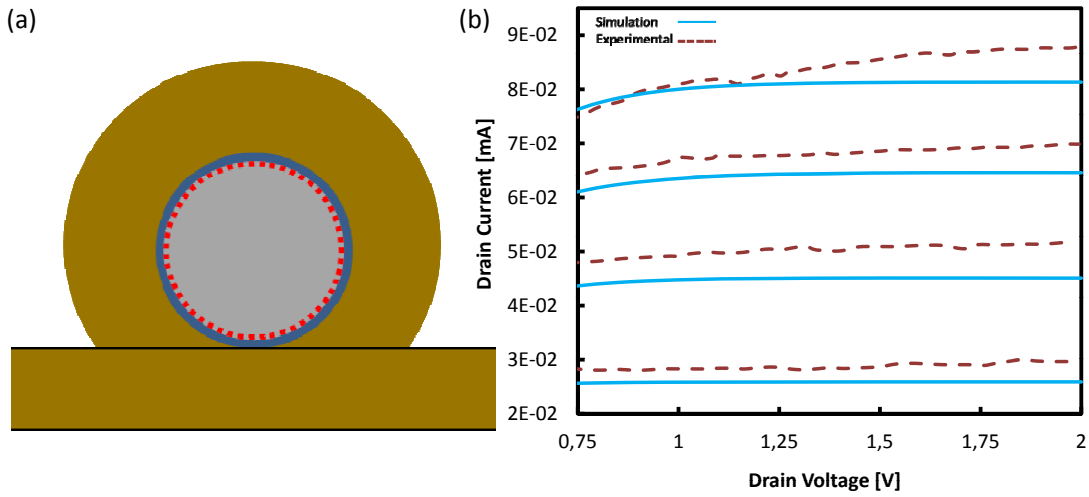


Figure 5.3: (a) Schematic representation of the $InAs/SiN_x$ surface states (blue) and electron accumulation (red) (b) Simulated IV characteristic without surface trap states. Figure taken from [156].

Trap parameter	Symbol	Value
Distribution	D_T	exponential
Depth (from E_C)	E_T	0.01 eV
Peak concentration	N_T	10^{13}cm^{-2}
Cross section	$0.4 \sigma_e$	10^{-16}cm^{-2}

Table 5.1: Some selected trap state parameters, similar to those from [79].

In Fig. 5.3a the position of these surface states is schematically shown (solid blue circle). The trap parameters were taken in very good agreement with those extracted by Halpern *et al.* [79] using the Kelvin probe force microscopy (KPFM) technique on single InAs nanowires and summarized in Table 5.1.

An exponential donor trap distribution, D_T , with a peak value of $N_T = 10^{13} \cdot \text{cm}^{-2}$ lying at only 10 meV below the conduction band minimum ($E_C - E_T = 0.01 \text{eV}$) has been used in the simulations. The very shallow donor trap states are positively charged and attract free electrons forming an accumulation layer at the InAs surface and a Fermi level pinning in the conduction band. Their impact on the output current is visible in Fig. 5.3b, where different output curves (enlarged, only in the saturation regime) are presented, with and without surface traps. In case of no traps the current is underestimated by about 10%.

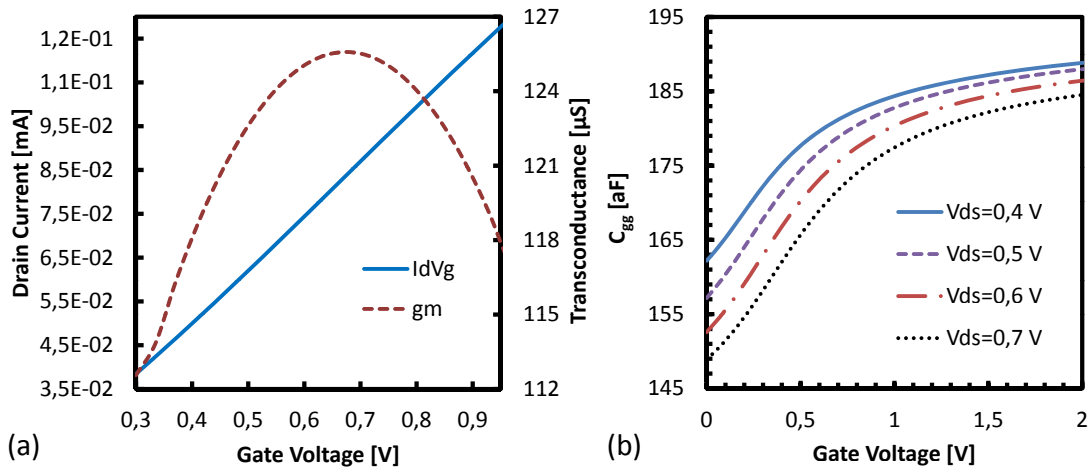


Figure 5.4: (a) Transfer characteristic for a drain-source voltage of 1.5 V (solid blue) and the corresponding transconductance g_m (dotted red) (b) Simulated gate-to-channel capacitance (C_{gg}) for V_{DS} between 0.4 and 0.7 V. Figure taken from [156].

Beside the output characteristic we also simulate the transfer characteristic and the transconductance, g_m , in order to be sure that our virtual nanowire accurately reproduces the InAs FET from [24].

For the transfer curve simulation we keep the drain voltage constant at 1.5 V and sweep the gate voltage from 0.3 to 1 V. If we derive the drain current with respect to the gate voltage we obtain the transconductance out of the transfer curve. The simulated transfer characteristic ($I_D - V_G$) is plotted in Fig. 5.4a together with the DC transconductance (g_m). The peak value of about $125 \mu S$ at $V_G = 0.63$ V is in good agreement with the reported $45 \mu S$ for the measured extrinsic transconductance.

Important for the frequency analysis of the device that will follow, would be the value of the intrinsic gate capacitance. For this purpose we must perform a coupled small signal-quasistationary analysis in Sentaurus Mixed Mode. In a small signal analysis the simulator computes the current response of the device at the output node for a small voltage perturbation at the input node, constructing the Fourier transformation of the response in order to switch to the frequency domain. This can be written as:

$$\delta I = Y\delta V = A\delta V + i\omega C\delta V \quad (5.1.1)$$

where the complex Y-matrix is of the form:

$$Y = A + j \cdot \omega \cdot C \quad (5.1.2)$$

For a typical transistor with three terminals, gate, source and drain we have three nodes named for example “g”, “s” and “d” and the Y matrix has 3×3 entries (although usually the source terminal is grounded and a two port equivalent is used for the three terminal device). We are interested in the element $c(g, g)$: the total small signal gate capacitance. Other important entries are the small signal transconductance $g_m = a(d, g)$ and the small signal output conductance $g_d = a(d, d)$.

In each iterative step of the quasistationary gate voltage ramp, from $V_G=0.3$ to 1 V, a small signal analysis is performed at a single frequency of 10 Hz (we are interested in the low frequency values) and the elements of the Y matrix are stored in a special AC plot. For the high frequency behavior that will be treated in the next chapter we do exactly the opposite: for a fixed bias voltage we compute the AC parameters from a starting frequency of 100 MHz until 1 THz with 20 points per decade. Thus we obtain the frequency dependent transconductance and capacitance for each node.

In Fig. 5.4b the total gate to channel capacitance ($C_{gg} = C_{gs} + C_{gd}$) of the NW transistor for a gate voltage sweep from 0 to 2 V is given. The extraction of the capacitance has been performed for different drain voltages from 0.4 to 0.7 V in 0.1 V steps. As one would expect the capacitance increases for higher gate voltages since there are sufficient electrons that can be accumulated under the gate dielectric. For higher drain voltages the gate capacitance decreases because the electrons are swept away by the lateral fields. The absolute values of the gate capacitance vary between 145 and 190 aF, quite small compared with the extrinsic parasitic values as will be shown in the following chapters.

5.1.1 High Frequency Simulation

Having validated our model, we move now to the high frequency analysis. As mentioned in the introduction the motivation of this simulation study is to estimate the intrinsic performance of the InAs NW transistor.

The first simulated figures of merit (FOM) are the maximum current gain and the resulting cutoff frequency f_T . Once the complex Y matrix has been computed in the small signal analysis we can easily obtain the hybrid matrix (H matrix) the impedance matrix (Z matrix) or the scattering matrix (S matrix). We are always using for the amplifier characterization the common source (CS) topology if not otherwise stated; hence the corresponding matrices have all 2×2 entries.

The H-matrix description is very convenient for the high frequency characterization of our two port network. As one can see, the parameter $h_{21} = \frac{i_d}{i_g} = \frac{Y_{21}}{Y_{11}}$, is the ratio of the drain and gate currents and it is usually called the “current gain” expressed in units of dB. For extremely low frequency it approaches infinity and for high frequencies it should decrease with 20 dB per decade. The intercept point of the current gain curve with the x-axis is called “transit” or “cut-off frequency” and it is labeled with f_T .

There are two possible reasons for the gain loss if we look at the definition of h_{21} . First the drain current will not be able to follow the extremely fast signal at the input; this is an intrinsic effect caused mainly by the physical limitations of charge carrier mobility inside the device. For the second gain limiting mechanism we identify the increase in gate current which is in the denominator of the ratio. This is the case for transistor with very large gate capacitances, intrinsic or more frequent extrinsic parasitic capacitances. As we know the capacitive coupling increases with frequency, the gate capacitance becoming ultimately a short at higher frequencies. Since the frequency dependent impedance of a capacitor can be written as:

$$(Z = 1/j\omega C) \quad (5.1.3)$$

we conclude that the greater the value of the gate capacitance is, the smaller the frequency when the capacitance turn into a short is. If we take a short look at our extracted gate capacitance we see that even for frequencies in the order of hundreds of GHz, the gate insulation has still a decent value of some M Ω . This already gives us a hint that our device performance is intrinsically limited by the charge carrier mobility (drain current decrease). However the situation output would be totally different if we would have a large parasitic gate capacitance as will be shown later.

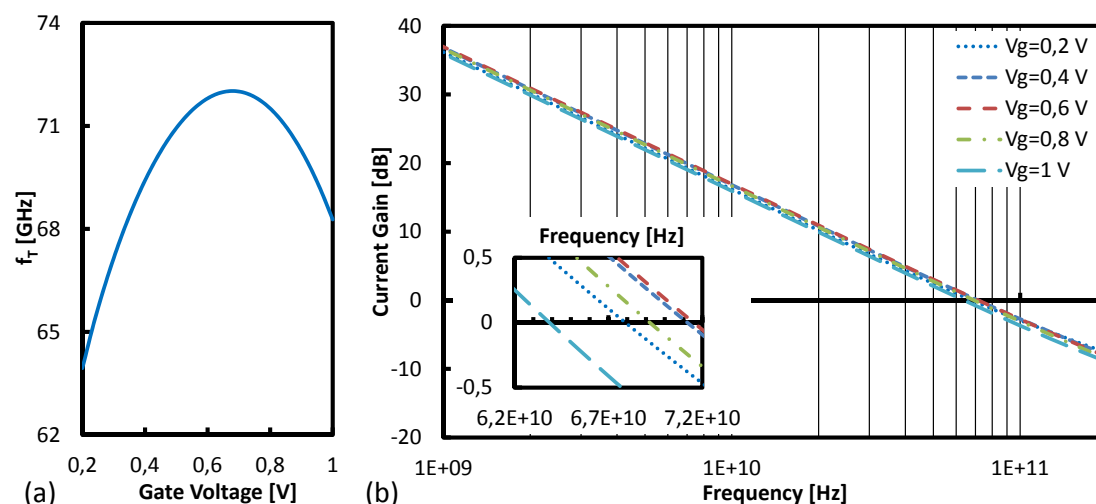


Figure 5.5: (a) Simulated transit frequency of the NW transistor without parasitic capacitances versus gate voltage (b) Simulated current gain versus frequency for different gate voltage; inset shows 0 dB intercept point. Figure taken from [156].

In Fig. 5.5a we see the typical current gain h_{21} extracted from the small signal analysis for different gate voltages from 0.2 to 1 V and fixed drain voltage of 1.5 V. The inset presents a magnification of the intercept points so that one can read the cut off frequencies more easily. The general trend is as expected; a 20 dB/decade slope and a maximum current gain of 35 dB lead to cut-off frequencies in the order of some tens of GHz (below 100 GHz).

The cut-off frequencies are plotted against the gate voltage in Figure 5.5b. We find that the f_T increases with the gate voltage until $V_G = 0.63$ V where the greatest f_T is obtained, namely 72 GHz and then keeps decreasing. This fact is perfectly understandable if we recall another definition of the transit frequency which states that f_T is roughly the ratio between the transconductance g_m and the gate capacitance. If we look at Fig. 5.4b we see that at this frequency g_m has its maximum value so it becomes clear why also the f_T versus gate voltage plot reproduces the general trend of g_m .

Comparing these results with the measured f_T from [24] we observe that it is roughly one order of magnitude higher (7 versus 72 GHz). When compared however with the latest experimental results from Johansson [26] they lie in the same order of magnitude, 72 versus 103 GHz. One has to mention however that the nanowire in [26] has roughly half the length of the InAs NW simulated here,

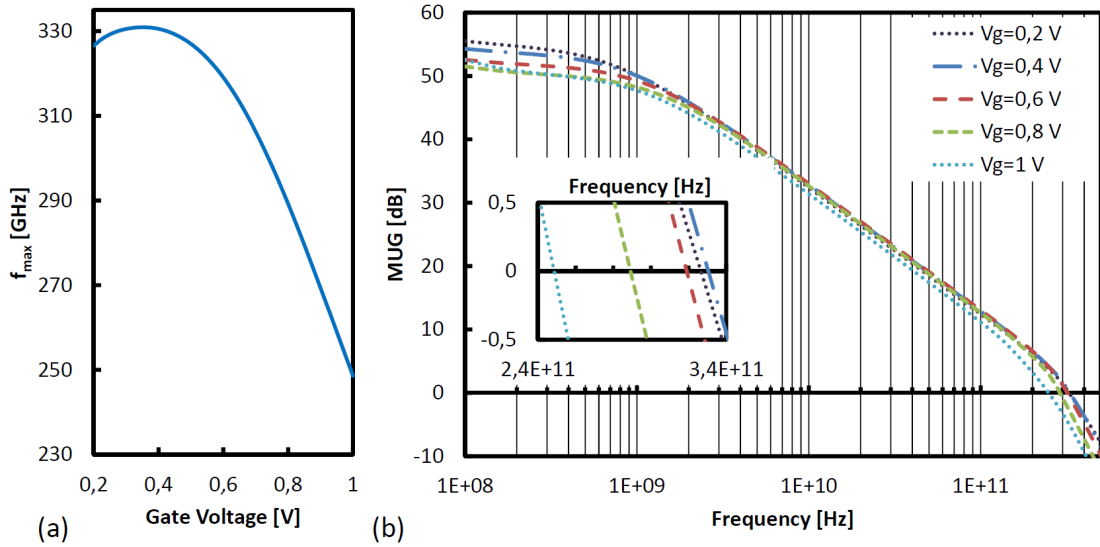


Figure 5.6: (a) Simulated f_{max} of the NW transistor without parasitic feedback resistor versus gate voltage (b) Simulated Mason's unilateral gain versus frequency for different gate voltage; inset shows 0 dB intercept point. Figure taken from [156].

which is $1.4 \mu\text{m}$. Nevertheless this is a hint that the values measured in [24] are extrinsic frequencies affected by parasitic elements and that the intrinsic current gain and corresponding cut off frequency are in the same order of magnitude as those simulated here. In fact the state of the art values presented in [26] were obtained exactly after decreasing the value of the parasitic pad capacitance. More evidence to support this assumptions will be shown when simulating the transistor with parasitic elements included.

The second figure of merit simulated for this device is Mason's Unilateral Gain (MUG) shown in Fig. 5.6a. The maximum unilateral gain is by definition the gain of a transistor whose internal feedback has been canceled by an external lossless network and has both input and output ports conjugately matched. The MUG can be derived from the Y matrix as well and has the form [34]:

$$G_{TU,max} = \frac{|Y_{21} - Y_{12}|^2}{4 [\text{Re}(Y_{11})\text{Re}(Y_{22}) - \text{Re}(Y_{12})\text{Re}(Y_{21})]} \quad (5.1.4)$$

Several gain curves are plotted for different gate voltages between 0.2 and 1 V. The intercept point of the MUG with the x-axis is a special frequency called maximum frequency of oscillation (f_{max}). We observe the general trend of the

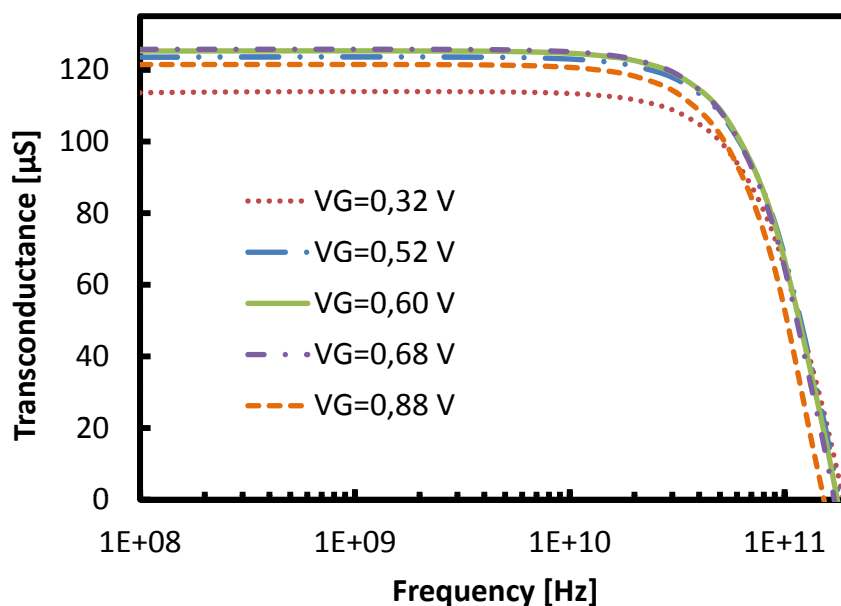


Figure 5.7: (a) Simulated transconductance versus frequency for different gate voltages from 0.3 to 0.9 V. Figure taken from [156].

simulated MUG: it has a peak value of 50 to 55 dB at low frequencies and then starts to fall with a 20 dB/slope intercepting the axis at frequencies between 250 and 350 GHz depending on the gate bias. In Fig. 5.6b the f_{max} versus V_G is depicted. A maximum of 330 GHz for a voltage of 0.4 V is obtained from the simulations, for higher voltages a decrease of the f_{max} can be observed reaching 250 GHz for 1 V.

Another figure of merit very important for the high frequency characterization is the transconductance versus frequency behavior (g_m vs. f) of the device. This trend is depicted in Fig. 5.7 for several gate voltages. At lower frequencies g_m is flat and has a maximum value of 125 μ S in excellent agreement with the DC value presented earlier. Only after 10 GHz the transconductance starts to drop.

The simulation predicts again far better performance of the InAs FET when compared to experimental data in [24] but similar to those in [26]. Obtained with the hydrodynamic simulator we have 330 GHz, Blekker et al. [24] report 20 GHz and Johansson et al. [26] 155 GHz. Here also we suspect that parasitics are the source of the poor 20 GHz f_{max} and a closer value to the intrinsic performance limit lies above 150 GHz.

One reason why the simulator predicts slightly higher values for the f_{max} (a factor of 2) might be that even with the optimized contacts the device in [26] still has some internal parasitic feedback which is the limiting factor. We shall see the influence of a parasitic resistor between the input and output of the transistor on the f_{max} in the next chapters.

We find that the latest state of the art experimental results from [26] mainly confirm our simulations and we may safely affirm that the intrinsic high frequency performance of InAs nanowire transistors are at least one order of magnitude higher than those presented in [24]. This means that all efforts should concentrate in the optimization of the contacts before downscaling the NW length; if one would proceed the other way around no significant improvement will be noticed since the contacts are the bottleneck of the device high frequency behavior.

5.1.2 Sensitivity Analysis - Doping

Having fitted the nanowire DC characteristic with a high degree of accuracy over the entire measured voltage range we would be like to see how the output, transfer and high frequency characteristic of the nanowire transistor will change from the nominal case ($4.3 \times 10^{17} \text{ cm}^{-3}$) if we modify the unintentional doping. In Sentaurus Device Editor we create three more meshes with the identical nanowire and contact structure but with unintentional n-type doping values of $4.3 \times 10^{16} \text{ cm}^{-3}$, $4.3 \times 10^{18} \text{ cm}^{-3}$ and $4.3 \times 10^{19} \text{ cm}^{-3}$.

In Fig. 5.8a we see the output characteristic for the nanowire with an unintentional doping of $4.3 \times 10^{16} \text{ cm}^{-3}$. A typical kink due to self-heating is present for the higher gate voltages of 1, 1.5 and 2 V. This is caused by the electron mobility degradation at high temperatures included via the hydrodynamic transport model. Peak values of around $20 \mu\text{A}$ are reached for $V_G = 2 \text{ V}$ and $V_D = 0.6 \text{ V}$ before decreasing again and stabilizing at around $12 \mu\text{A}$ for higher drain voltages. The transfer characteristic and the transconductance are given in Fig. 5.8b with peak values of $22 \mu\text{A}$ and $38 \mu\text{S}$ respectively.

For the high frequency behavior the identical simulations have been performed and the results are given in Fig. 5.8c and Fig 5.8d. A maximum cutoff frequency of 40 GHz is obtained for the gate voltage of 0.2 V the same voltage where the

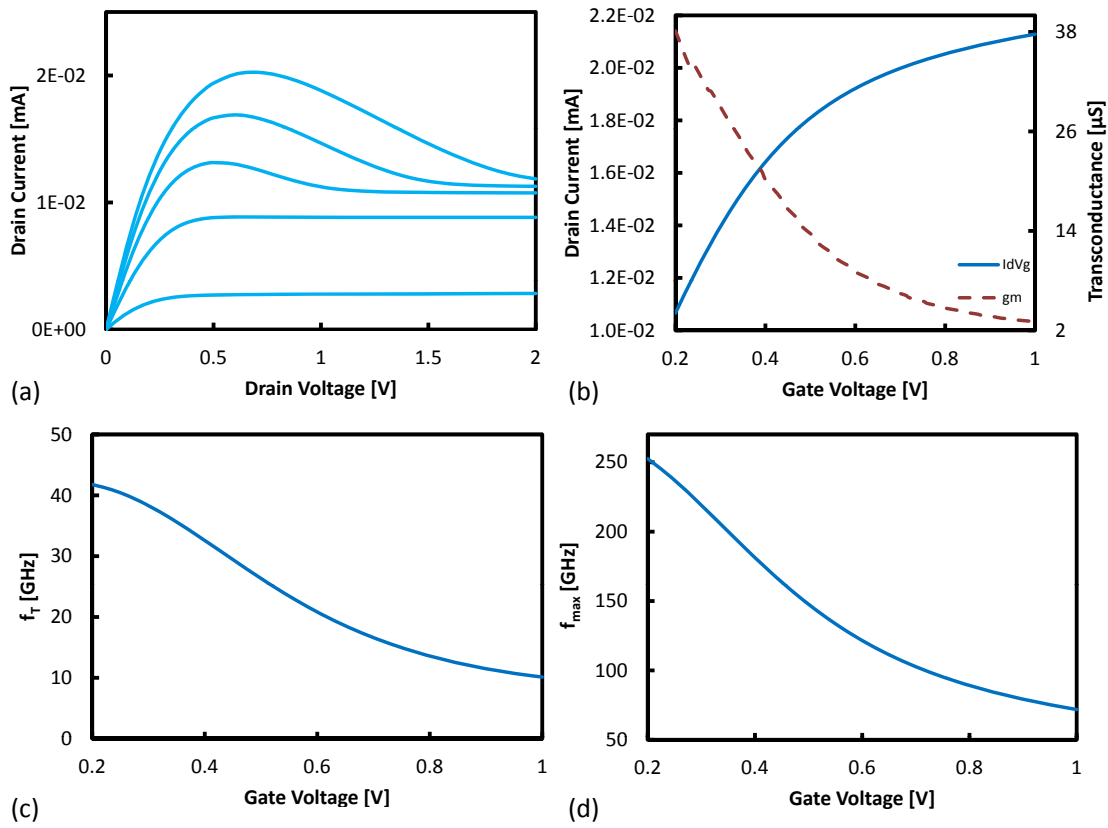


Figure 5.8: (a) Simulated output characteristic for the transistor with $N_D = 4.3 \times 10^{16} \text{ cm}^{-3}$ (b) Transfer characteristic and transconductance of the same device (c) Cut-off frequency and (d) Maximum frequency of oscillation..

maximum transconductance is achieved. Although the maximum transconductance is roughly 4 times smaller than the one of the nominal case the cutoff frequency is only 2 times smaller. This can be easily explained by the smaller intrinsic gate-to-channel capacitance associated to the smaller doping. A maximum frequency of oscillation of 250 GHz is obtained from the simulation a value roughly 1.3 times smaller than the nominal case.

For the unintentional doping of $4.3 \times 10^{18} \text{ cm}^{-3}$ we have the output curves presented in Fig 5.9a. Significantly higher drain currents approaching $300 \mu\text{A}$ for gate voltages of 2 V and drain voltages of the same magnitude have been obtained. No self-heating kink can be observed and the relative spacing between the curves for different gate voltages is also quite different compared to the nominal case, a I_{Dmax}/I_{Dmin} ratio of only 2 compared to 16. This spacing and general shape of the output characteristic resembles more the nanowire measure-

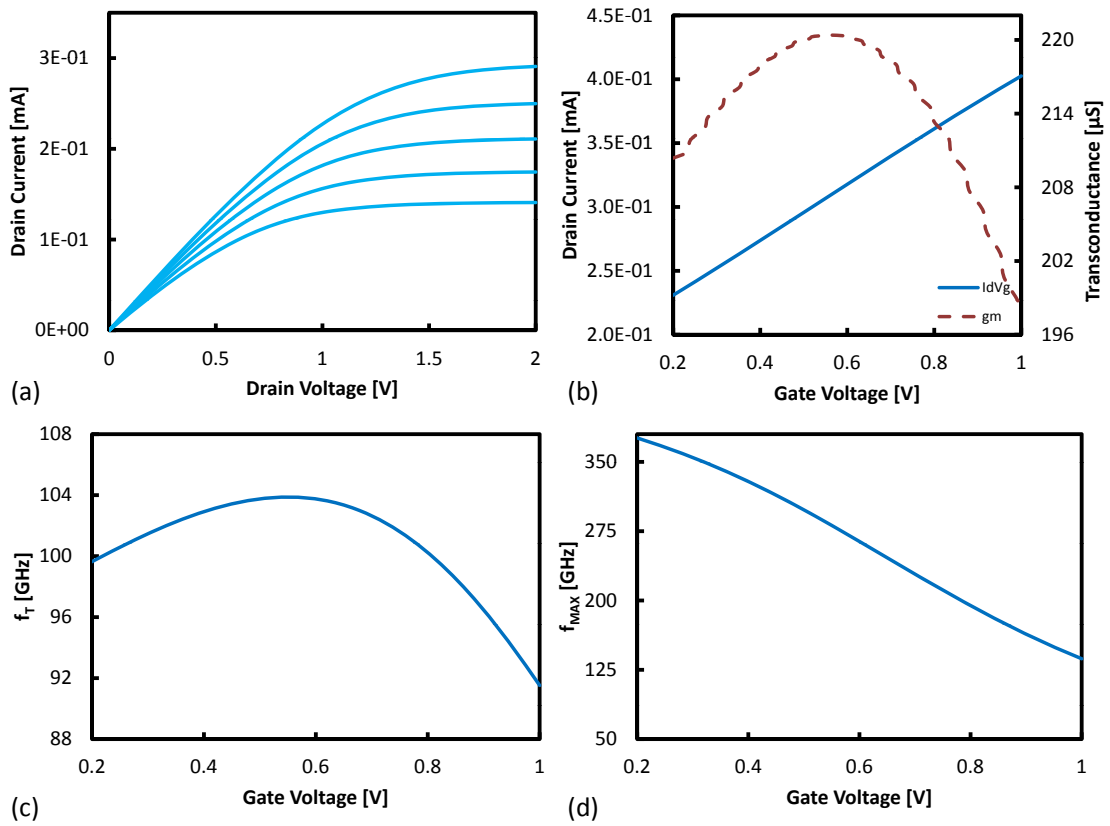


Figure 5.9: (a) Simulated output characteristic for the transistor with $N_D = 4.3 \times 10^{18} \text{ cm}^{-3}$ (b) Transfer characteristic and transconductance of the same device (c) Cut-off frequency and (d) Maximum frequency of oscillation.

ments performed at Lund [26] indicating that they induce a higher unintentional doping during nanowire growth.

The drain currents in the transfer curve and the transconductance are also significantly higher, the current almost four times larger and g_m nearly double compared to the nominal case. For the high frequency behavior surprisingly only a minimal improvement is visible in Fig. 5.9c and d. The cutoff frequency is 100 GHz and the maximum frequency of oscillation 375 GHz compared to 72 GHz and 330 GHz for f_{max} in the nominal case. A very large intrinsic channel capacitance is the main reason why despite large current and transconductance values no significant improvement is visible. This large capacitance is also rather insensitive to the voltage (in the simulated range) as one can see from the flat characteristic of the cutoff frequency.

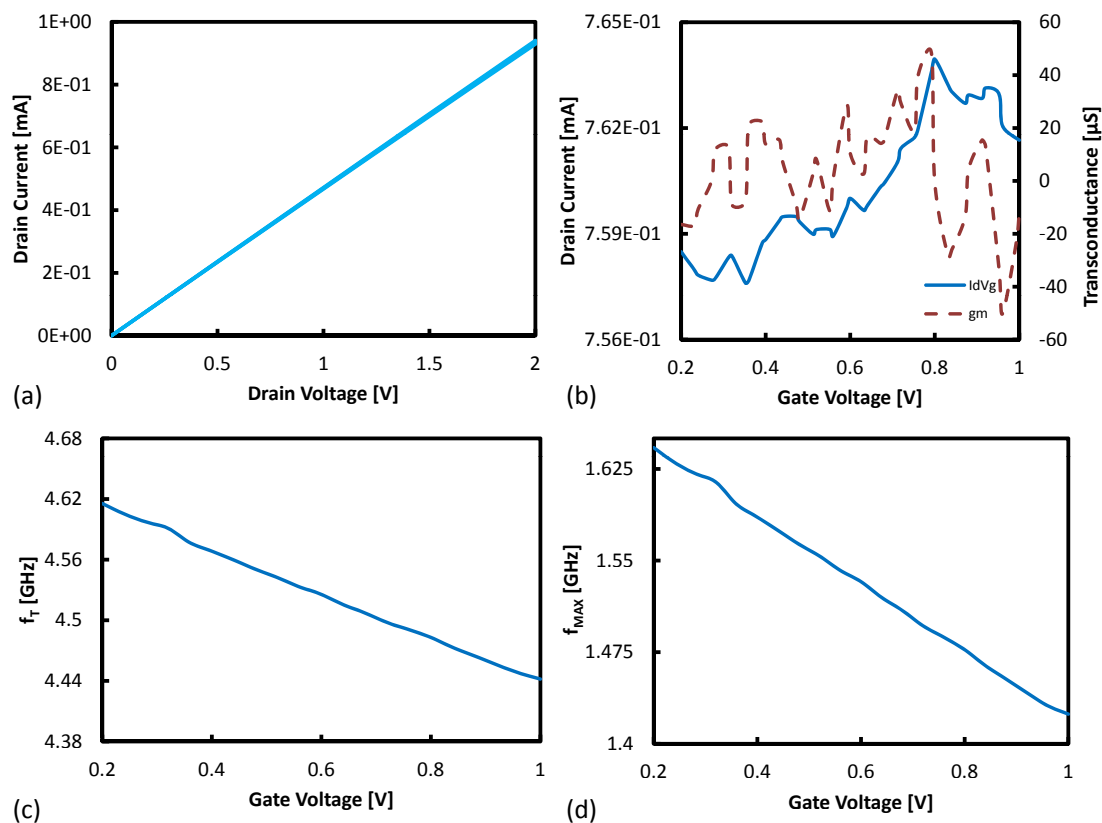


Figure 5.10: (a) Simulated output characteristic for the transistor with $N_D = 4.3 \times 10^{19} \text{ cm}^{-3}$ (b) Transfer characteristic and transconductance of the same device (c) Cut-off frequency and (d) Maximum frequency of oscillation.

In the final case we generate a structure with heavy n-type doping $4.3 \times 10^{19} \text{ cm}^{-3}$. As shown in the Fig. 5.10a all output curves overlap, the device behaving more like a conductor rather than a field effect transistor. A peak value of 1 mA for the drain voltage of 2 V is more than order of magnitude higher than the nominal case, however as we can see the gate electrode has virtually no control function. The same conclusion can be drawn from Fig. 5.10b where both transfer curve and transconductance show no dependence on the applied gate voltage. A random fluctuation of the drain current around a value of $760 \mu\text{A}$ in the $I_D - V_G$ curve from Fig. 5.10b can be observed and a transconductance with a mean value of 0 is obtained from the quasisationary simulation, presented in the same figure.

With this poor values for the DC transconductance and a large intrinsic channel capacitance arising from the high doping it comes as no surprise that the high frequency behavior is the worse from all the above cases.

Both cut-off and maximum frequency of oscillation obtained from the small signal analysis lie more than one order of magnitude lower than the nominal case. A value of 2.5 GHz for f_T and 1.65 GHz for f_{max} can be read from Fig. 5.10c and d. Again the cutoff frequency has a very flat characteristic over the gate voltage, easily explained by the fact that neither the transconductance nor the capacitance vary significantly with the voltage applied on the gate electrode.

All these DC and HF characteristics make this final device with a doping of $4.3 \times 10^{19} \text{ cm}^{-3}$ the worst candidate for a high speed low voltage application. The large drain currents do not compensate the lack of almost any DC gain or the extremely poor high frequency behavior.

5.1.3 Sensitivity Analysis - Gate Length

The second set of experiments consists in the variation of a key geometric parameter for any transistor: the gate length L_G . Again the nominal case is the 1.4 μm nanowire transistor where the wrap-gate electrode covers the entire nanowire length as seen in Fig 5.1. We then gradually reduce the length of the electrode in 0.4 μm steps from 1.4 μm to 1 μm , 0.6 μm and finally 0.2 μm while keeping the total length of the wire constant at 1.4 μm . For all the cases we keep the unintentional n-type doping at $4.3 \times 10^{17} \text{ cm}^{-3}$.

In Fig. 5.11a the output curves of the nanowire with gate length of 1 μm are depicted. We notice when compared to Fig. 5.2 that the maximum current halves and that the spacing between different gate voltages changes. For low gate voltages the drain current is almost identical to the nominal case whereas for V_G greater than 1 V the drain current starts to saturate a lot faster leading to a tighter spacing of the output curves. For 2 V drain and gate voltage we have a peak current plateau of around 46 μA . For the transfer curve shown in Fig. 5.11b the values for the drain current reach around 75% of the nominal case, the same can be said about the DC transconductance which has a peak value of 80 μS .

When moving to the high frequency analysis we observe, somewhat surprisingly that the cutoff frequency remains the same, 72 GHz. What changes is the voltage

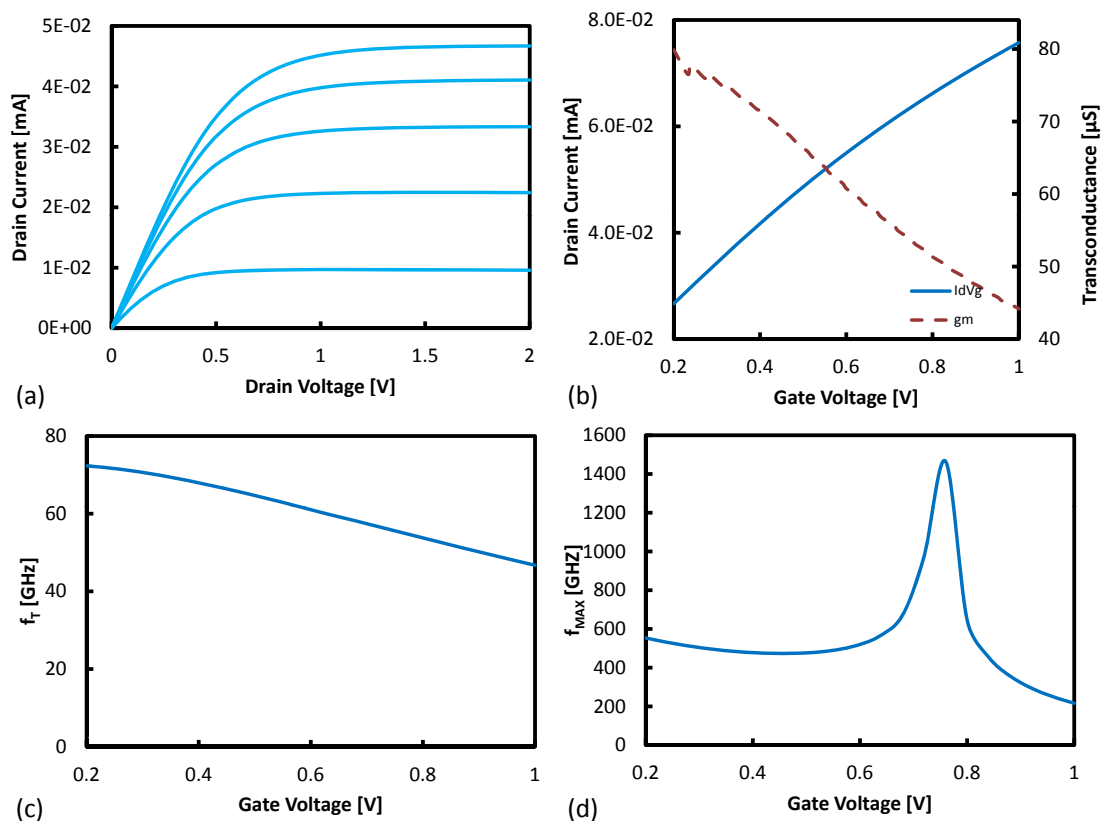


Figure 5.11: (a) Simulated output characteristic for the transistor with gate length $L_G = 1 \mu\text{m}$ (b) Transfer characteristic and transconductance of the same device (c) Cut-off frequency and (d) Maximum frequency of oscillation.

at which this frequency is achieved: 0.2 V versus 0.6 V on the gate electrode for the nominal case. This is directly related with the voltage where the peak transconductance is obtained: as we can see this voltage shifts towards lower voltage with shorter gate length. Decreasing the control electrode leads to a faster saturation of the drain current, fewer electrons are accumulated under the gate. This can be clearly seen in the curvature of the transfer curves for 1.4 and $1 \mu\text{m}$ (Fig. 5.4 and Fig. 5.11b). From the curvatures it follows directly that the peak DC transconductance will be achieved at a lower voltage for shorter gate lengths.

Another very interesting effect can be observed when simulating the maximum frequency of oscillation. In Fig. 5.11d at higher gate voltages a sort of resonant peak is observed. A first thought would be that it is merely a simulation artifact but it is a complex effect related to charge and field distribution under the gate.

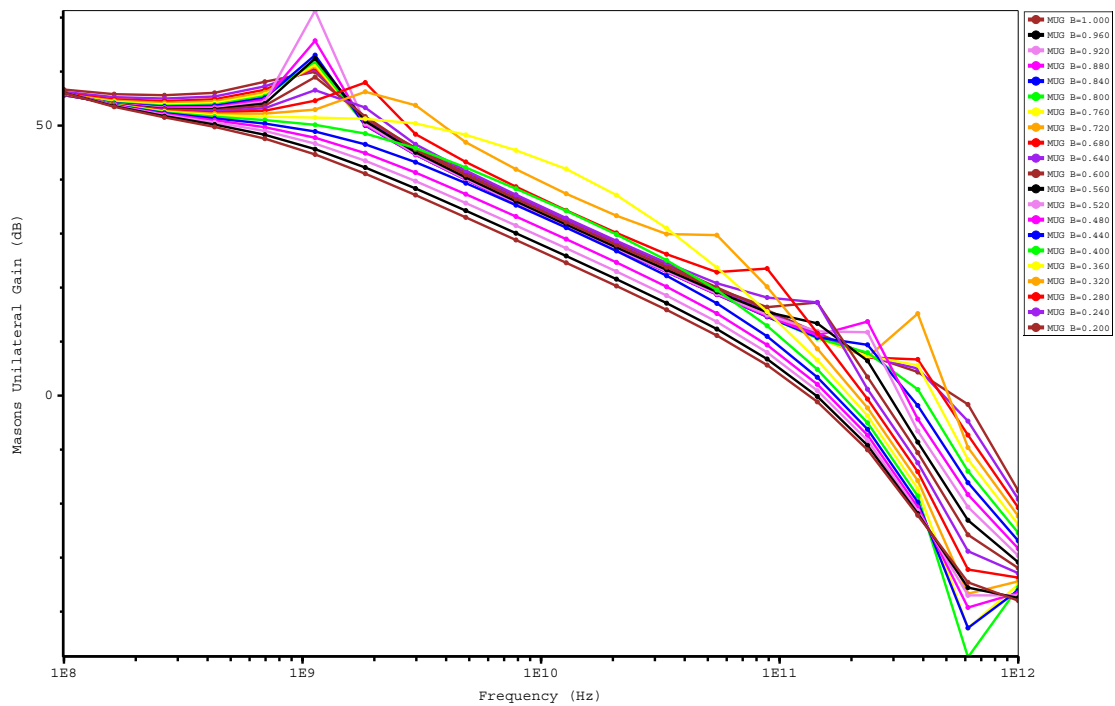


Figure 5.12: (a) Simulated Mason's Unilateral Gain for gate voltages in the range: $V_G=0.2 - 1$ V.

In order to understand this, one should go deeper and analyze the data that is used to draw the f_{max} curve. As stated earlier the f_{max} is obtained from Mason's unilateral gain, which is depicted in Fig. 5.12 versus frequency for various gate voltages from 0.2 to 1 V. For the gate voltages in the range 0.6-0.8 V the MUG curves show a resonant peak which translates into a gain increase, just before intersecting the 0 dB axis.

The underlying physical process for the behavior above is the phase shift between the electrical charge and electrical field response under AC excitation. As the gate decreases the channel gets restricted and current flow under the gate is reduced (clearly seen both in output and transfer curves). This in turn raises the parallel electric field under the gate which heats up the electrons, since the hydrodynamic model is active. On the other hand due to the high field saturation model (and with a voltage of 1 V over $1\mu\text{m}$ we are well in the saturation regime) the effective mobility decreases and modifies the charge and field distribution consequently. As a result there is a delay between the change in temperature and change in parallel field for the area under the gate. This

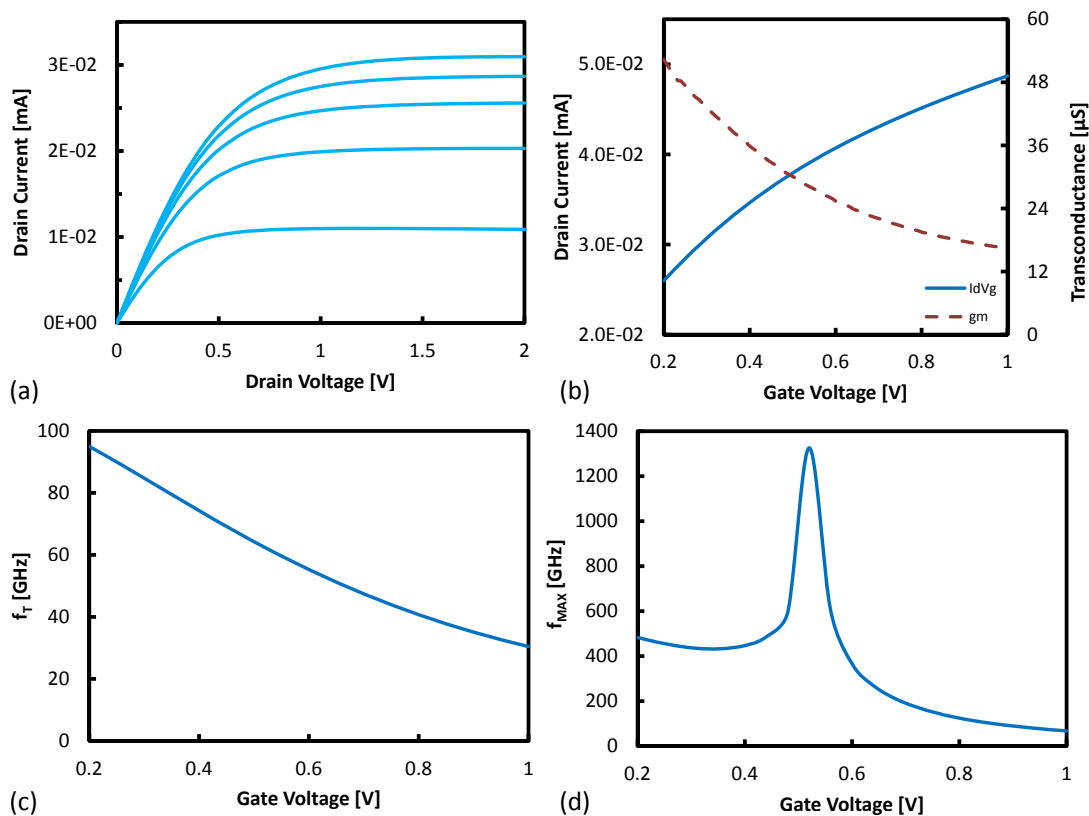


Figure 5.13: a) Simulated output characteristic for the transistor with gate length $L_G=0.6\mu\text{m}$ (b) Transfer characteristic and transconductance of the same device (c) Cut-off frequency and (d) Maximum frequency of oscillation.

translates in a phase shift between current and voltage at the output for an AC excitation on the gate.

As mentioned earlier when explaining the reasons for the current gain loss at higher frequency, the intrinsic channel capacitance coupling with the gate provides a parasitic RF feedback path. If the above conditions are met (phase shift between current and voltage) more power can be delivered from the input to the output via this RF path, explaining the increase in gain. This effect may lead to instability (oscillations) and has been previously reported for HEMT transistors [157].

From In Fig. 5.11d we observe that the peak value of f_{max} achieved at 0.2 V gate voltage is just below 600 GHz and drops constantly until 0.55 V. Then the “resonance” occurs and the maximum frequency of oscillation has a sharp increase up to 1.45 THz before dropping to 190 GHz at $V_G = 1$ V.

The next simulated structure has an effective gate length of $0.6 \mu\text{m}$ and we can see the simulated output curves in Fig. 5.13a. As in the previous case the first two curves for $V_G = 0 \text{ V}$ and 0.5 V aren't influenced by the gate reduction and similar values for the saturated drain current are obtained when compared with the nominal case. For $V_G > 1 \text{ V}$ however the spacing has become even narrower and the saturated drain current only reaches $30 \mu\text{A}$ for 2 V on the gate electrode. A decrease of the current in the transfer characteristic and a lower DC transconductance value are visible from the data in Fig. 5.13b. Maximum values of $50 \mu\text{A}$ and $52 \mu\text{S}$ for g_m are obtained from the DC simulation.

The high frequency characteristic of this structure is superior to the one of the nominal device both in terms of f_T and f_{max} . The cutoff frequency observed in Fig. 5.13c has a value of 95 GHz at 0.2 V and drops down to 30 GHz at 1 V , a 25% increase with respect to the standard NW transistor. This can be explained again by the lower channel capacitance since less than half of the nanowire length is covered by the wrap gate. In terms of maximum frequency of oscillation we have the resonant spike as well, this time at a lower gate voltage, namely 0.52 V . The peak value of 480 GHz at $V_G = 0.2 \text{ V}$ and the spike of 1.3 THz can be read in Fig. 5.13d.

The last structure has a gate length of only $0.2 \mu\text{m}$ so only $1/7$ of the total nanowire length. The output curves follow the general trend of gate downscaling: for high gate voltages the current saturates a lot faster and the peak values is lower than the $0.6 \mu\text{m}$ case, $24 \mu\text{A}$ namely, as can be seen in Fig. 5.14a. The transconductance and transfer curve in Fig. 5.14b display values of around $1/6$ of the nominal case.

This device displays the best high frequency properties of all the simulated devices. A cutoff frequency of 143 GHz and a maximum frequency of oscillation of 514 GHz at 0.2 V are shown in Fig. 5.14c and d.

5.2 Inclusion of Parasitics

We now return to the original structure with gate length of $1.4 \mu\text{m}$ and unintentional n-type doping in the order of $4.3 \cdot 10^{17} \text{ cm}^{-3}$. Our simulations have shown intrinsic maximum frequency of oscillation of 330 GHz for 0.4 V gate voltage (Fig. 5.6a) and cut-off frequencies of 72 GHz for $V_G=0.63 \text{ V}$ (Fig. 5.5a).

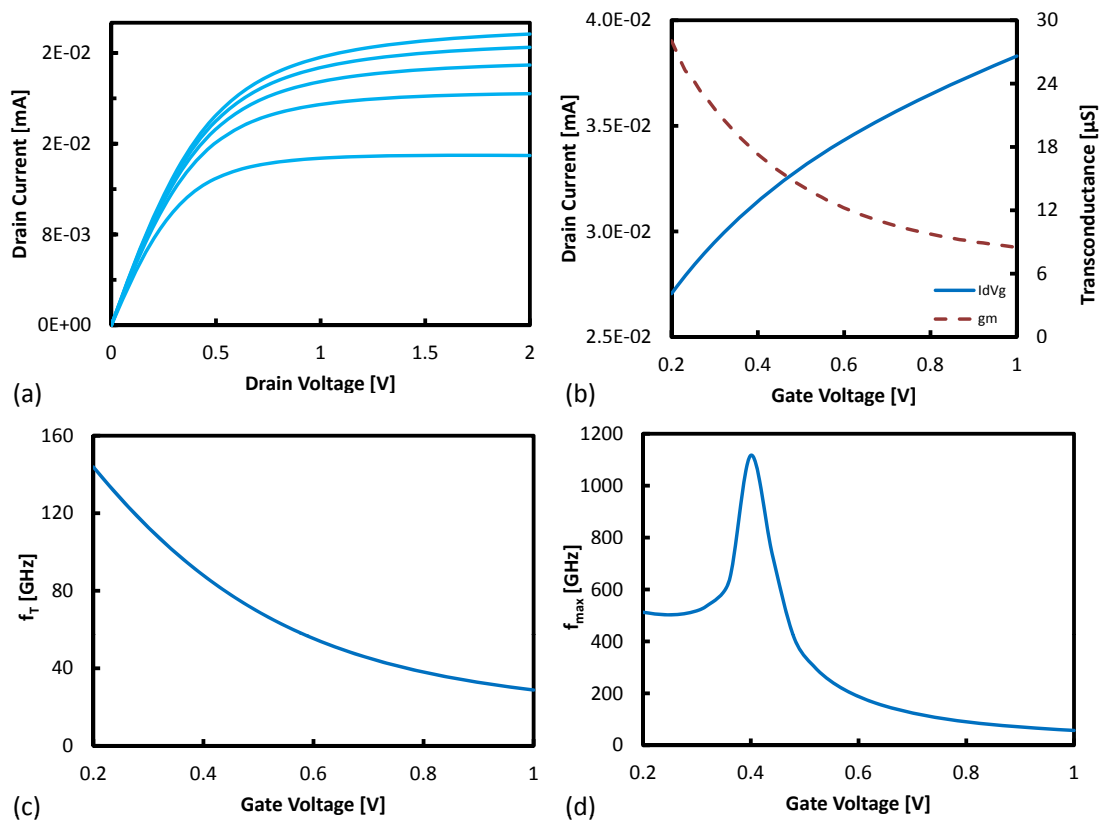


Figure 5.14: (a) Simulated output characteristic for the transistor with gate length $L_G=0.2\mu\text{m}$ (b) Transfer characteristic and transconductance of the same device (c) Cut-off frequency and (d) Maximum frequency of oscillation.

Since we suspect that the parasitic capacitances and resistors are responsible for the poor high frequency behavior reported in [24] we move to the next step of the simulation and include the extrinsic parasitic network.

The simulation environment is Sentaurus Mixed Mode and the external circuit can be seen in the schematic in Fig. 5.15. For the computation of currents and voltages between the gate, drain and source terminals the hydrodynamic model is used, whereas the external elements are included via SPICE models. Circuit nodes declared in a “netlist” ensure the transition between internal and external quantities. In this way complex external parasitic and biasing networks can be simulated fast without conceding the accuracy of the physical transport models.

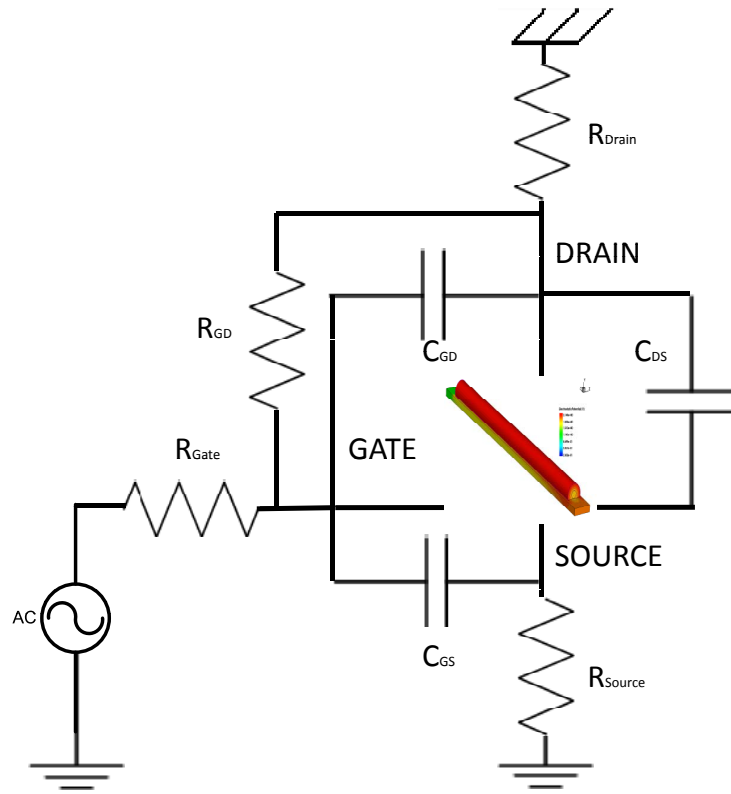


Figure 5.15: Illustration of Sentaurus Mixed Mode: the nanowire transistor in the center is simulated using the hydrodynamic model whereas the extrinsic parasitic elements are simulated with SPICE models. Figure taken from [156].

First we include the effect of the large pad capacitance at the input (gate) of the transistor, a parasitic C_p . From the definition the cut-off frequency as the following:

$$f_T = \frac{g_m}{2\pi C_{gs}} \quad (5.2.1)$$

We observe that the current gain and the cutoff frequency have a $1/x$ dependency on the gate capacitance ($C_g = C_{gs} + C_{gd}$). If we add an external parasitic gate capacitance C_p that will increase C_g we expect both the current gain and the transit frequency to decrease. The cut-off frequencies versus C_p are shown in Fig. 5.16a. As expected the f_T decreases with a $1/x$ trend, when the capacitance has a value of a few fF (7 fF) f_T drops to less than 3 GHz.

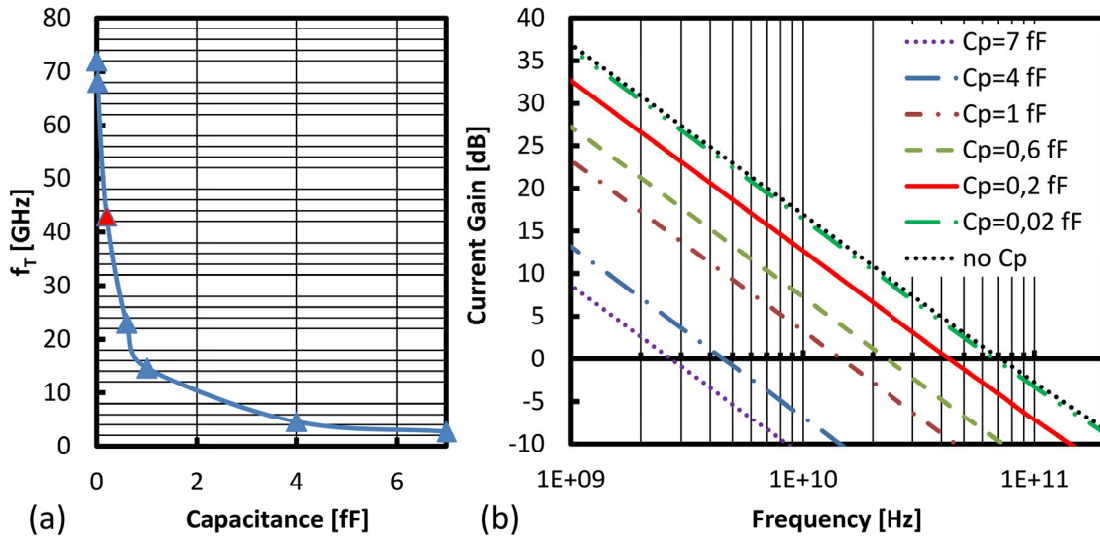


Figure 5.16: (a) Impact of parasitic gate – source capacitances on the transit frequency. (b) Impact of parasitic gate – source capacitances on current gain curves. Figure taken from [156].

This trend is clearly visible also for h_{21} in Fig. 5.16b, where the current gain is plotted versus frequency for the different values of the parasitic capacitance. We can clearly see the shift of the roll-off towards lower frequencies as the capacitance increases. For no C_p we have the intrinsic case with 37 dB gain, for $C_p = 1$ fF we are around 24 dB which means that we have lost almost half of the gain and for $C_p = 7$ fF we have roughly 25% of the intrinsic current gain, namely 9 dB.

These results are in good agreement with the experimental values of Blekker *et al.* [24] and provide a reasonable explanation for the low cut off frequencies. Johansson *et al.* [26] optimize their device contacting pads and obtain considerably lower capacitances. Each device presented in [26] is in fact an InAs nanowire array transistor with 165 single wires. The total extrinsic gate capacitance ($C_g = C_{gs} + C_{gd}$) is 19.2 pF which translates in 0.116 fF for a single wire. For this value we can see from Figure 5.16b that our simulated nanowire would achieve more than 70 GHz in terms of f_T .

Next we analyze the influence of parasitic elements on the maximum frequency of oscillation, f_{max} . From the previous definition of f_{max} we know that it can be extracted from the intercept point of the maximum unilateral gain. For a device to be called unilateral it has to fulfill two conditions: firstly both the input and

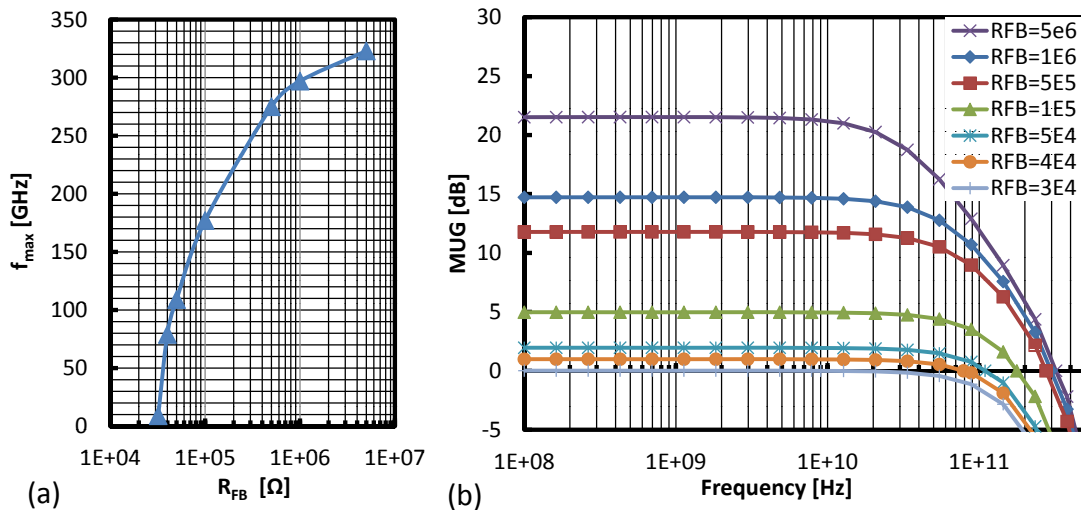


Figure 5.17: (a) Impact of gate – drain parasitic feedback resistor on maximum frequency of oscillation. (b) Impact of gate – drain parasitic feedback resistor on Mason’s unilateral gain curves. Figure taken from [156].

output must be conjugately matched, a task not very difficult to achieve. Next all internal feedback must be neutralized via a loss-less network, a task not so trivial. We suspect that a parasitic feedback resistor between gate and drain (R_{gd}) is responsible for the poor f_{max} reported in [24] and we redo the simulations for the MUG with different values of this parasitic R_{gd} . A plausible assumption for the origin of this resistor would be the overlap of the gate electrode with the drain/source metallization. Although this should not be the case, the mask used for the wrap gate is self-aligned with the drain and source, an overlap does occur clearly visible in the SEM picture (Fig. 2.6) of Blekker *et al.* [24].

This parasitic feedback resistor has been simulated, with a value ranging from 30 k Ω to a 5 M Ω , and as it can be seen from Fig. 5.17a, has a major effect on the maximum frequency of oscillation. The smaller the value of this R_{FB} , the lower the value of f_{max} becomes. It drops to a value of about 10 GHz for a R_{FB} of 30 k Ω , very similar to the measured value. In Fig. 5.17b the Mason’s unilateral gain curves for the different R_{FB} values are plotted and we can see the drastic decrease not only in frequency but also in terms of gain, for $R_{FB} = 30 \text{ k}\Omega$ the MUG approaches 0.

For comparison some standard values of the C_p for silicon have been highlighted in Fig. 5.16a and b. Mueller *et al.* determine in [155] the extrinsic parasitic capaci-

tance for a silicon MOSFET and study its contribution on the device performance. Under extrinsic capacitance they designate the sum of several parasitic capacitances: fringe capacitance, gate-to-poly capacitance, corner capacitance and gate-bulk capacitance. Each of this distinct capacitance is determined and an analytical model that can be integrated in the design flow is proposed. Their conclusion is that the total extrinsic capacitance does not exceed 0.2 fF, roughly in the same order as the intrinsic transistor capacitance. The point corresponding to a $C_p = 0.2$ fF has been marked (red) in Fig. 5.16a and the corresponding gain curve in Fig. 5.16b has been highlighted solid red. We can see that the cut off frequency attributed to this C_p is larger than 40 GHz, roughly 6 times higher than the measured one. This suggests than there is a lot of room for optimization in the device contacting, optimization that will significantly improve the device performance.

5.3 Conclusion

We performed an extensive simulation study for the measured InAs nanowire transistor based on a sophisticated hydrodynamic simulator which takes into account energy balance, velocity saturation and trapping effects at material interfaces. The measured output characteristic, cutoff frequencies and maximum frequencies of oscillation have been successfully reproduced. Based on our simulations we conclude that the device intrinsic performance is at least one order of magnitude higher than currently believed in terms of f_T and f_{max} . We have identified several factors that are responsible for the measured behavior. The parasitic gate-source capacitance heavily affects the transit frequency whereas the parasitic gate to drain feedback resistor reduces the maximum oscillation of frequency. Our results are encouraging and suggest that the InAs based high frequency transistors have the ability to operate well in the GHz regime if the parasitic elements are minimized. This implies that all the efforts should concentrate firstly on optimizing the device contacting rather than scaling it down; even at gate length of 1 μm considerably higher frequencies can be achieved than compare to silicon technology.

6 Applications of Nanowires in Optoelectronics

The monolithic integration of optoelectronic devices, like lasers or photo-detectors, and standard, silicon-based electronic devices has been considered an insurmountable challenge in the past [158]. Two major impediments make the integration highly challenging: a large lattice mismatch between silicon and most III/V semiconductors and the high processing temperatures of the III/V compounds.

6.1 Background

One solution that has been widely adopted in industry, with moderate yields, is the so-called wafer bonding method [158]. Optoelectronic devices are grown on their III/V substrates, while the electronic integrated circuits are separately grown on silicon wafer and only in a final step the two wafers are bonded together. The requirements of this method are very strict: mirror polished wafers with flat surfaces up to atomic scale, clean room environment and nanometer-precision alignment. Even so, due to the continuous down-scaling of digital circuits (22 nm gate length in the latest processors [8]), the integration of optical interconnects on top of electronic devices becomes troublesome.

The most promising alternative for massive III/V optoelectronics and silicon electronics integration are semiconducting nanowires grown on standard substrates. Due to their unique, 2D quantum confined nature these novel structures have remarkable mechanical, optical and electronic properties. As a result of their high aspect ratio (small cross-section in comparison to nanowire length) the mechanical stress gets distributed along the nanowire without cracking, hence large lattice mismatches are tolerated. Very recently novel nanowire growth

schemes have been presented [158–160], schemes within the thermal budget of standard CMOS circuits (400–500 °C).

These breakthroughs open an entirely new path in the direction of on-chip fully integrated optoelectronic platforms. In the next paragraphs we will present some of the state-of-the-art devices and fabrication methods.

The first demonstrated nanowire based light emitting diodes (LEDs) date back to the early 90s [56] and were GaAs nanowire based p-n junctions. Near infrared emission was observed at 4.2 and at 77 K and more important the light intensity presented a polarization dependency. Light polarized parallel to the nanowire axis showed a 30% higher intensity than perpendicular polarized light, a clear indication of the quantum nature of the devices.

Ten years later the first electrically driven single nanowire laser was presented [161]. In Fig. 6.1 we see the schematic of the nanowire laser, an optical image of the device, as well as the electrical and optical characteristics. An n-doped CdS nanowire was chosen as active gain medium, covered with Al₂O₃ and Ti/Au for the electron injecting contact; holes are injected directly from the p-type silicon substrate. For an injection current of around 100 mA a broad emission spectrum is measured, a clear indication for spontaneous emission. However as the injection current increases above 200 μ A a sharp emission peak at 509 nm is visible, typical for stimulated emission.

After the successful demonstration of such devices the next step would be their integration with standard silicon devices. Intense research has been carried out in this direction in the last years [158–160, 162].

A breakthrough was announced in 2010 by Chuang *et al.* [159] when the first GaAs nanowire LED and avalanche photodetector (APD) were grown on silicon substrate at temperatures compatible with standard CMOS process. An injection current of only 3 μ A for spontaneous emission, a bright electro-luminescence (EL) at 1128 nm with a line width of 64 nm, make the NW LED a state-of-the-art device even when compared with planar GaAs devices.

For the NW APD we can mention a current gain of 263 at only -8 V bias, an extraordinarily value, far better than planar APD [159]. These results demonstrate the huge potential of NW photonics integrated with silicon technology.

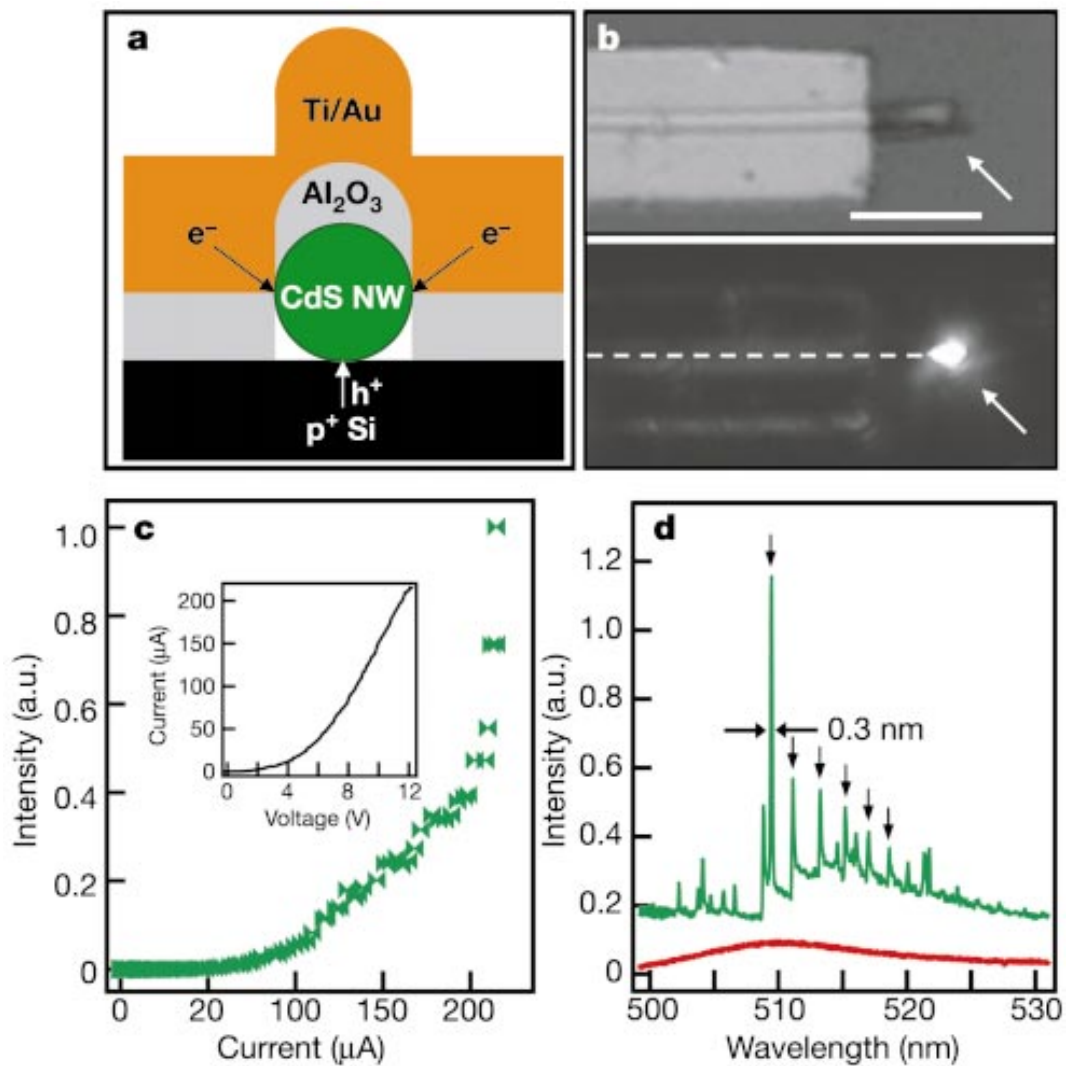


Figure 6.1: (a) Schematic of the CdS nanowire laser structure - the Ti/Au electron injecting electrode and the hole injecting p⁺ Si substrate are highlighted. (b) Optical image of the device, scale bar 5 μm. (c) Electrical characteristic and emission intensity for various injecting currents. (d) Electroluminescence spectra for two injecting currents - 120 μA (red) and 210 μA (green). Image reproduced from [161]

One year later Chen *et al.* [158] from the same research group at Berkley demonstrated the first NW laser grown on silicon substrate. InGaAs - GaAs core-shell NW grown on silicon wafers at temperatures of 400 °C showed a clear stimulated emission peak at 950 nm at 273 K. Furthermore by varying the mole fraction of Indium the emission peak could be widely tuned over 50 nm wavelength. The

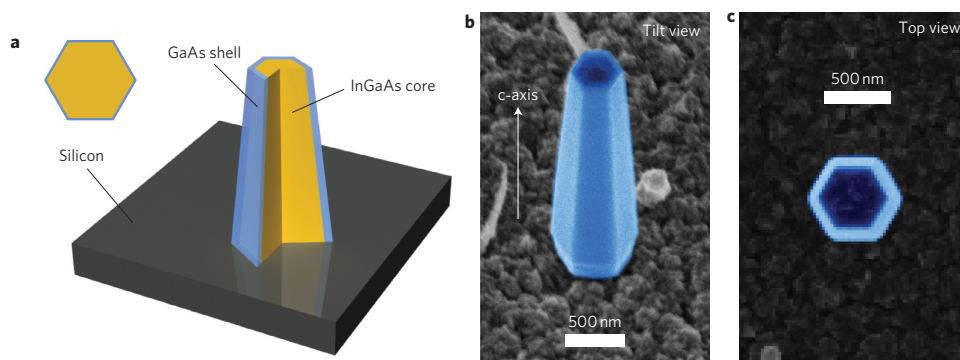


Figure 6.2: (a) Schematic of monolithically integrated InGaAs-GaAs core-shell NW laser. (b) SEM side image. (c) SEM top-view image, the hexagonal crystal structure is clearly visible. Image reproduced from [158]

schematic of this NW laser and the corresponding SEM images are shown in Fig. 6.2.

In the most recent work of Chen et al. [160] present an on-chip optical link using NW optical components all on silicon substrate. Light emitters, detectors and a nanowire based solar cell supply are presented and gigahertz bandwidths are demonstrated.

With these latest state-of-the-art devices and methods we are highly optimistic that massive III/V integration with standard CMOS circuits will become available in the near future [163].

In this chapter we intend to simulate first a nanowire based LED, then to modify it in order to reach the lasing threshold and thus obtain a nanowire laser structure.

6.2 Theory of Optoelectronic Devices

6.2.1 The Light emitting Diode

The basic optoelectronic device is the light emitting diode or LED and as the name already states is nothing more than a p-n diode. When forward biased the minority charge carriers are injected across the junction where they can recombine with majority carriers, either radiative or non-radiative. An efficient

LED should have a large radiative recombination rate and a very small non-radiative recombination rate.

For a complete theory of the p-n junction one can look in [98, 164]; here we will use some ready derived quantities and put the accent on design aspects and issues. The forward current of a typical p-n diode is given by the minority carrier diffusion and it has three components [98]. These are the minority carrier electron diffusion current, the minority carrier hole current and the trap-assisted recombination current:

$$J_n = \frac{eD_n n_p}{L_n} \left[\exp\left(\frac{eV}{k_B T}\right) - 1 \right] \quad (6.2.1)$$

$$J_p = \frac{eD_p p_n}{L_p} \left[\exp\left(\frac{eV}{k_B T}\right) - 1 \right] \quad (6.2.2)$$

$$J_{GR} = \frac{en_i W}{2\tau} \left[\exp\left(\frac{eV}{2k_B T}\right) - 1 \right] \quad (6.2.3)$$

where $D_{n/p}$ are the diffusion coefficients and $L_{n/p}$ are the diffusion lengths for both electrons and holes, n_p and p_n the minority carrier concentrations, W the depletion region width and τ the trap-assisted recombination time in the depletion region.

A schematic of the typical LED is shown in Fig. 6.3a and the corresponding band diagram in Fig. 6.3b. As one can see only the photons generated near the top layer have a chance of leaving the device whereas those emitted in the buried region will most probably be reabsorbed. Consequently, in order to maximize the emitted photons in the top layer we need to increase the electron minority current in the p-doped region. This can be achieved through the doping profile, if we have a pn^+ diode, $n_p \gg p_n$ and from 6.2.1 and 6.2.2 we obtain $J_n \gg J_p$. If the active material has a low trap density (high quality GaAs for example) then the recombination current is very small and we have an injection efficiency close to unity. The injection efficiency is defined as:

$$\gamma_{inj} = \frac{J_n}{J_n + J_p + J_{GR}} \quad (6.2.4)$$

After being injected in the p-doped region the minority charge carriers will recombine with the holes as shown in Fig. 6.3b. The detailed description of the

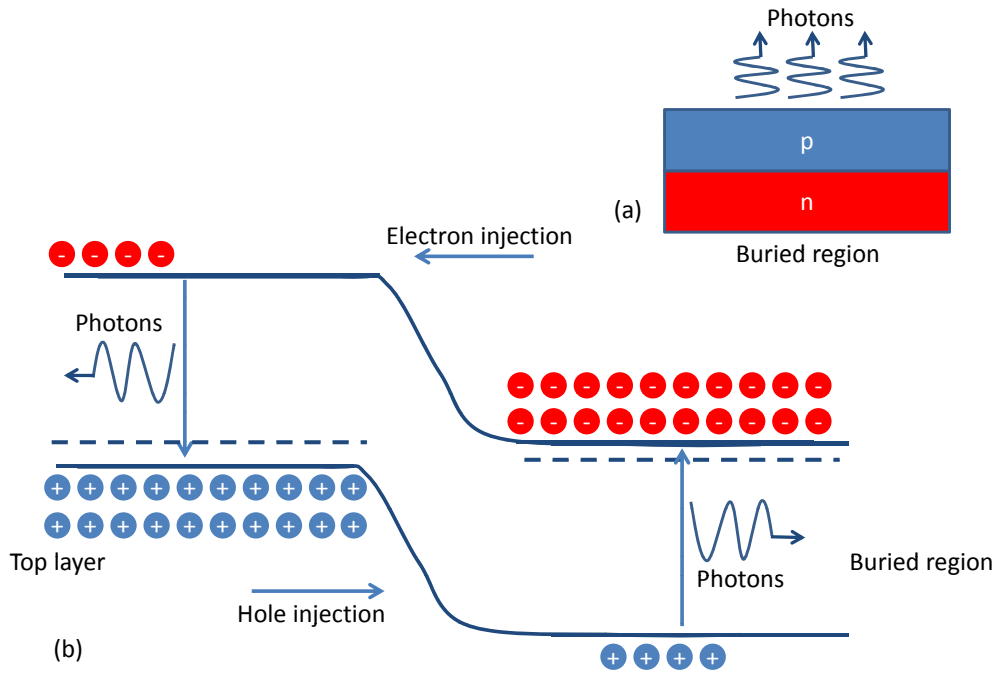


Figure 6.3: (a) Schematic of a typical light emitting diode. (b) Band diagram of the LED. Image redrawn from [98].

radiative and non-radiative recombination mechanism in semiconductors can be found in [98, 164]. In the following chapters we will shortly summarize the radiative recombination process for direct bandgap semiconductors.

In Fig. 6.4 a schematic representation for an optical transition in reciprocal space is presented. We can see that the optical transition is vertical which implies momentum conservation (the same k -value for electrons and holes). Photon energy and electron/hole energies are related via:

$$\hbar\omega - E_g = \frac{\hbar^2 k^2}{2} \left[\frac{1}{m_e^*} + \frac{1}{m_h^*} \right] = \frac{\hbar^2 k^2}{2m_r^*} \quad (6.2.5)$$

with m_r^* the reduced mass of the system.

Evaluating the radiative recombination rate is a complex task since it represents the basic interaction between matter (semiconductor with a characteristic bandgap energy) and electromagnetic waves (emitted photons); a detailed quantum mechanical derivation can be found for example in [165]. Here we will only mention that the emission rate depends on the occupation probabilities for electrons and holes, the density of states for electrons and holes, bandgap energy

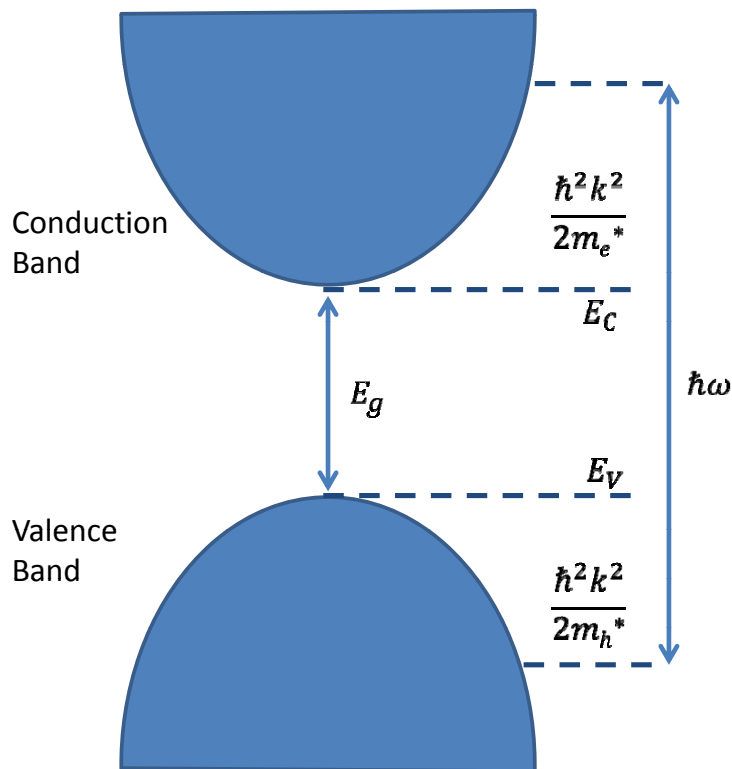


Figure 6.4: Schematic representation of an spontaneous emission process. Image redrawn from [98].

and the dipole moment. If an electron is available in the conduction band and an hole in the valence both in the same state k , in other words $f^e(k)=f^h(k)=1$, then the emission rate can be approximated by:

$$W_{em} \approx 1.5 \times 10^9 \hbar\omega (eV) s^{-1} \quad (6.2.6)$$

and the recombination time as:

$$\tau_0 = \frac{0.67}{\hbar\omega (eV)} ns \quad (6.2.7)$$

The values above are the fastest possible spontaneous emission rate 6.2.6 or time 6.2.7 since we have assumed a probability equal to 1 of finding both an electron and a hole with the same k -vector.

In reality the occupation probabilities depend on the quasi-Fermi levels in the n and p regions and we obtain the radiative recombination rate by integrating

the emission rate over all e-h pairs and making use of the corresponding Fermi functions. Here we can differentiate between several cases.

For lightly doped materials (both n and p) the Fermi functions can be approximated by a Boltzmann distribution and the spontaneous radiative recombination has the form:

$$R_{spon} = \frac{1}{2\tau_0} \left(\frac{2\pi\hbar^2 m_r^*}{k_B T m_e^* m_h^*} \right)^{3/2} np \quad (6.2.8)$$

We can see from equation 6.2.8 that R_{spon} is proportional to the e-h product. Furthermore we define the radiative carrier lifetime - the lifetime of an electron in a p-doped region (or viceversa) - by dividing n (or p in the dual case) to 6.2.8. We obtain:

$$\tau_r = \frac{n}{R_{spon}} = \frac{2\tau_0}{p} \left(\frac{2\pi\hbar^2 m_r^*}{k_B T m_e^* m_h^*} \right)^{2/3} \quad (6.2.9)$$

Another case would be the injection of minority carriers into highly doped regions. If the doping exceeds 10^{18} cm^{-3} we can assume that the carrier occupation is degenerate and $f^h(f^e)=1$. In this case the spontaneous emission rate has the form:

$$R_{spon} \approx \frac{1}{\tau_0} \left(\frac{m_r^*}{m_h^*} \right)^{3/2} n \quad (6.2.10)$$

for the electrons n injected in a p-doped region, and

$$R_{spon} \approx \frac{1}{\tau_0} \left(\frac{m_r^*}{m_e^*} \right)^{3/2} p \quad (6.2.11)$$

for the holes p injected in a n-doped region.

The carrier lifetime can be approximated in both situations by τ_0 .

The same holds true for the third case, the high injection regime. So many minority carriers get injected, that we can assume $f^h(f^e)=1$ and the we obtain the same result for the emission rate and carrier lifetime as above.

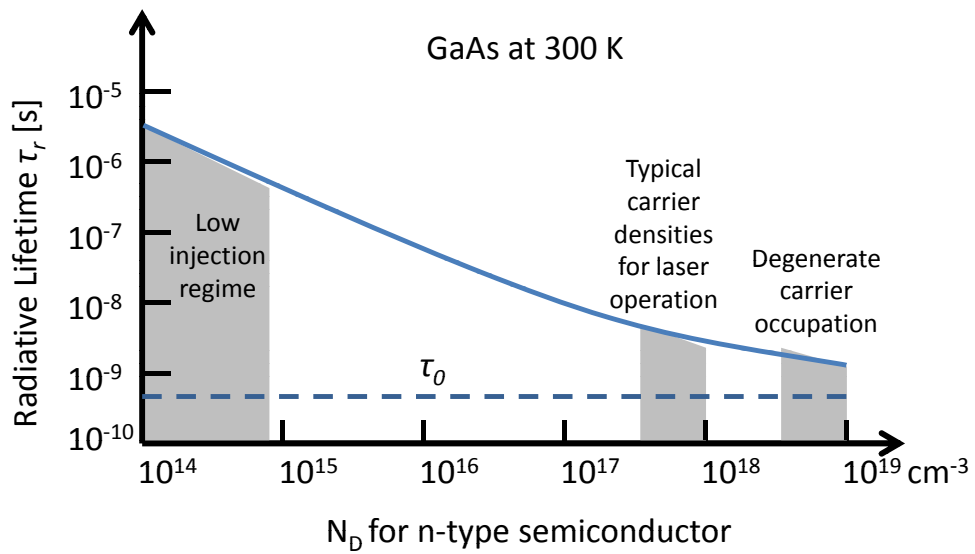


Figure 6.5: Radiative lifetime of a hole injected into an n-doped material plotted against the donor doping concentration. Image redrawn from [98].

Finally we have the case in which carrier injection is not that high but still sufficient to cause carrier "inversion" ($f^e + f^h \geq 1$). If we assume $f^e \approx f^h = 1/2$ we obtain for the emission rate:

$$R_{spon} \approx \frac{n}{4\tau_0} \quad (6.2.12)$$

and for the radiative lifetime:

$$\tau \approx \frac{\tau_0}{4} \quad (6.2.13)$$

Equations 6.2.12 and 6.2.13 are good approximations for lasers near threshold, before stimulated emission gets dominant.

In Fig. 6.5 the radiative lifetime of a minority charge carrier (hole) against the donor doping concentration for GaAs is plotted, and the various cases are highlighted.

6.2.2 The Laser

The laser is very similar to the LED concerning the electrical part: minority carriers are injected over a p-n junction, by forward biasing the diode, and

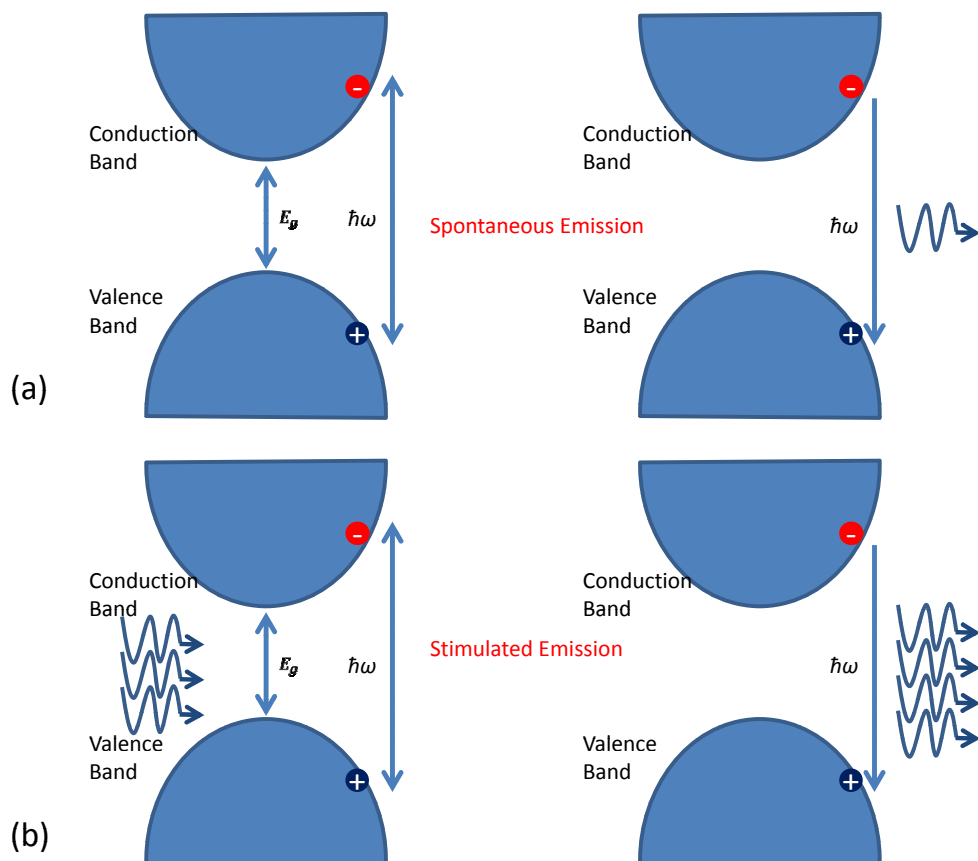


Figure 6.6: (a) Spontaneous emission process - the electron and hole recombine and emit a photon in the absence of any other photon. (b) Stimulated emission process - the electron and hole recombine and emit a coherent photon in the presence of other photons. Image redrawn from [98].

they will start to recombine and spontaneously emit photons. A big difference arises in the optical part - photon emission will change from spontaneous to stimulated.

In Fig. 6.6 the two cases are depicted: spontaneous emission (a) and stimulated (b). At the beginning no photons are present and the laser functions as a normal LED. Then, after a certain amount of photons has been generated via recombination, the stimulated emission takes over. Again from quantum mechanical calculations [165] we obtain the stimulated emission rate as:

$$W_{em}^{st}(\hbar\omega) = W_{em}(\hbar\omega) \cdot n_{ph}(\hbar\omega) \quad (6.2.14)$$

We see that it is proportional to the spontaneous emission rate multiplied with the number of photons (with energy $\hbar\omega$). In a LED the generated photons quickly leave the device or are reabsorbed therefore the photon density is always low. If however we manage to contain the photons in the laser cavity we can get the stimulated emission started. This is the entire idea behind the laser: an optical cavity is devised so that selective confinement for photons with a specific energy can be ensured. The photon emission rate for this specific energy becomes larger due to stimulated emission and all the photons will be in phase.

The confinement and photon multiplication is obtained with the help of a resonant (optical) cavity, the Fabry - Perot resonator being the most widely known. Several relations are useful for the Fabry - Perot cavity, the cavity length and the resonant modes are connected via:

$$L = q\lambda/2 \quad (6.2.15)$$

where q is an integer and λ is the material light wavelength defined as:

$$\lambda = \frac{\lambda_0}{n_r} \quad (6.2.16)$$

with λ_0 the free space wavelength and n_r the refractive index.

The spacing between the modes is defined as :

$$\Delta k = \frac{2\pi}{L} \quad (6.2.17)$$

Another important quantity for the optical cavity is the so-called optical confinement factor, gamma, defined as:

$$\Gamma = \frac{\int_{\text{activerregion}} |F(z)|^2 dz}{\int |F(z)|^2 dz} \quad (6.2.18)$$

6.2.3 Optical Absorption, Loss and Gain

Photons traveling through a cavity can be absorbed and produce e-h pairs, the quantity that describes the probability of such an event being the absorption coefficient α . It can be shown [98] that α is proportional to the product $1 - f^e(E^e) \cdot 1 - f^h(E^h)$. On the other hand we have the previously discussed emission process which creates new photons. In order to sustain lasing we must have positive gain (g), which is defined as the difference between emission and absorption coefficient. If we recall that the emission was proportional to $f^e(E^e)$ and $f^h(E^h)$ we get:

$$g(\hbar\omega) \approx f^e(E^e) \cdot f^h(E^h) - \{1 - f^e(E^e)\} \{1 - f^h(E^h)\} = \{f^e(E^e) + f^h(E^h)\} - 1 \quad (6.2.19)$$

We see that in order to have positive gain the semiconductor must be in "inversion" [98]:

$$f^e(E^e) + f^h(E^h) > 1 \quad (6.2.20)$$

Without proof the gain can be approximated by [98]:

$$g(\hbar\omega) \approx 5.7 \times 10^4 \frac{(\hbar\omega - E_g)^{1/2}}{\hbar\omega} [f^e(E^e) + f^h(E^h) - 1] cm^{-1} \quad (6.2.21)$$

This is the material gain in order to obtain the cavity gain we have to multiply it by the confinement factor:

$$\text{Cavity gain} = g(\hbar\omega)\Gamma \quad (6.2.22)$$

Finally the last loss mechanism is the one due to mirror losses. Photons should remain trapped in the resonator cavity and multiply in order to sustain stimulated emission. However some of them manage to escape and we can define a loss coefficient, α_r , correspondingly:

$$\alpha_r = -\frac{1}{L} \ln(R) \quad (6.2.23)$$

where L is the length of the resonator and R the reflection coefficient of the mirror.

6.3 Simulation Setup

Simulations are carried out using the same, state-of-the-art finite volume simulator - Sentaurus. Since our aim is the modeling and simulation of nanowire based optoelectronic devices we have to include in any case the radiative recombination in order to create photons from electron-hole pairs. This recombination mechanism is implemented in the simulator as [35]:

$$R_{net}^{rad} = C(np - n_{i,eff}^2) \quad (6.3.1)$$

with $C = 2 \times 10^{-10} \text{cm}^3 \text{s}^{-1}$ for GaAs.

Additionally the Shockley-Read-Hall (SRH) and the Auger recombination models have been activated. The SRH trap-assisted recombination rate is defined as [35]:

$$R_{net}^{SRH} = \frac{np - \gamma_n \gamma_p n_{i,eff}^2}{\tau_p(n + \gamma_n n_1) + \tau_n(p + \gamma_p p_1)} \quad (6.3.2)$$

with γ_n and γ_p the same as in equations 3.3.15

For the concentration of trapped electrons (holes) we use [35]:

$$n_1 = n_{i,eff} \cdot \exp\left(\frac{E_{trap}}{k_B T}\right) \quad (6.3.3)$$

$$p_1 = n_{i,eff} \cdot \exp\left(-\frac{E_{trap}}{k_B T}\right) \quad (6.3.4)$$

with E_{trap} being the trap level energy from midgap.

Charge carrier lifetimes have also a doping dependency and are implemented as [35]:

$$\tau_n = \tau_p = \tau_{dop}(N_{A,0} + N_{D,0}) = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_{A,0} + N_{D,0}}{N_{ref}}\right)^\gamma} \quad (6.3.5)$$

with $\tau_{max}=10^{-9}s$, $\tau_{min}=0s$, $N_{ref}=10^{16} \text{ cm}^{-3}$ and $\gamma=1$ for GaAs [35].

The third recombination mechanism, the Auger recombination is implemented as [35]:

$$R_{net}^A = (C_n n + C_p p)(np - n_{i,eff}^2) \quad (6.3.6)$$

with $C_n(T)$ and $C_p(T)$ defined as:

$$C_n(T) = \left(A_{A,n} + B_{A,n} \left(\frac{T}{T_0} \right) + C_{A,n} \left(\frac{T}{T_0} \right) \right) \left(1 + H_n e^{-n/N_{0,n}} \right) \quad (6.3.7)$$

$$C_p(T) = \left(A_{A,p} + B_{A,p} \left(\frac{T}{T_0} \right) + C_{A,p} \left(\frac{T}{T_0} \right) \right) \left(1 + H_p e^{-p/N_{0,p}} \right) \quad (6.3.8)$$

and A,B,C,H and N_0 are taken from the GaAs material file `citesdeviceug`.

Finally, since our nanowire LED (or laser) has high doping concentrations we also activate the doping dependent mobility model, the Arora model more precisely [35]:

$$\mu_{dop} = \mu_{min} + \frac{\mu_d}{1 + ((N_{A,0} + N_{D,0})/N_0)^{A^*}} \quad (6.3.9)$$

here $\mu_{min}=A_{min} \cdot \left(\frac{T}{300K} \right)^{\alpha_m}$, $\mu_d=A_d \cdot \left(\frac{T}{300K} \right)^{\alpha_d}$, $N_0=A_N \cdot \left(\frac{T}{300K} \right)^{\alpha_N}$,
 $A^*=A_a \cdot \left(\frac{T}{300K} \right)^{\alpha_a}$

with $A_{min},A_d,A_N,A_a,\alpha_m,\alpha_d,\alpha_N$, and α_a are taken from the GaAs parameter file [35].

6.4 LED Structure

As stated earlier our first simulation objective would be the modeling of a GaAs nanowire LED. We start with a geometry very similar to that presented in [162] by Mayer al. and implement the GaAs-AlGaAs core-shell nanowire structure in the simulator using Sentaurus Device Editor. The total nanowire length, L_{nw} is 10 μm and the total nanowire radius, r_{nw} is 150 nm. Along the radial direction we have not only different doping profiles but also different materials (GaAs-AlGaAs).

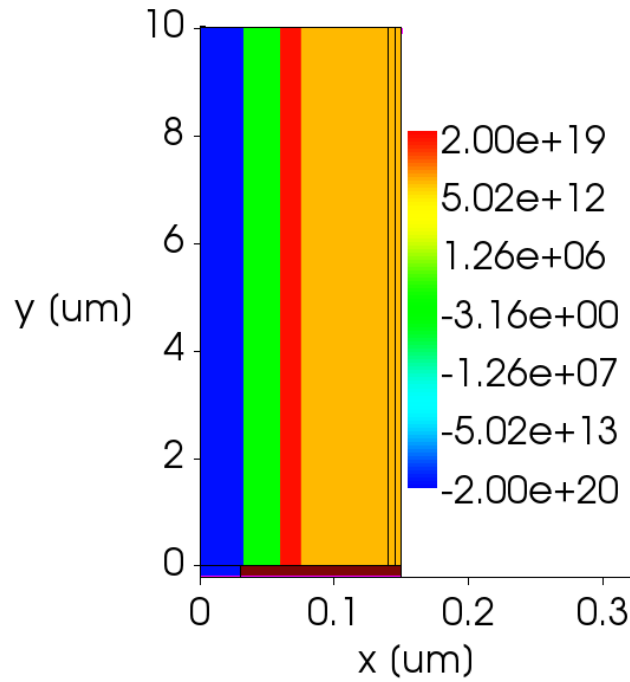


Figure 6.7: Cross-section of NW LED with the various doping concentrations. Image taken from [166].

In Fig. 6.7 the nanowire longitudinal cross-section is depicted with the doping profile in color-code. A p-doped region with a radius of 30 nm and a value of $N_A=2 \cdot 10^{20} \text{ cm}^{-3}$ constitutes the nanowire core. Next an intrinsic region with an extension of also 30 nm follows and a n^{++} ($2 \cdot 10^{19} \text{ cm}^{-3}$) area with 14 nm extension completes the p-i-n structure.

Finally 66 nm of the exterior radius are lightly n-doped ($5 \cdot 10^{13} \text{ cm}^{-3}$) before the AlGaAs shell of only 5 nm thickness is grown. The last region of only 5 nm n-doped ($5 \cdot 10^{13} \text{ cm}^{-3}$) GaAs serves as passivation layer. The contacts as highlighted in pink: the anode stretches along the x-axis over the entire nanowire radius ($L_{anode}=150 \text{ nm}$) whereas the cathode is placed at the upper end of the nanowire (on the top right corner in Fig. 6.7) and has a length, $L_{cathode}$, of 100 nm. In order to ensure that the anode has only contact with the p-doped core a SiO_2 layer (colored in brown) is placed between the contact and the exterior layers of the nanowire.

The band structure of this reference structure is shown in Fig. 6.8. From this the role of the intrinsic region becomes obvious: in the case of forward bias both the electrons and holes encounter large potential barriers and are basically

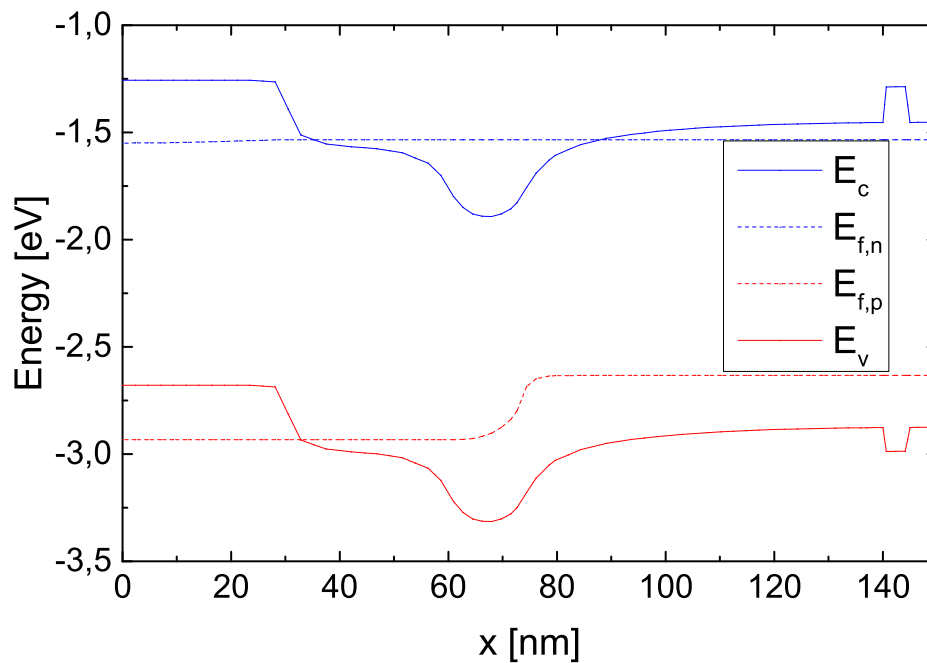


Figure 6.8: Band structure of the reference device. Image taken from [166].

confined inside undoped region. This on the other hand increases the e-h recombination and since the GaAs is a direct bandgap semiconductor the radiative recombination rate will increase as well.

6.5 Simulation results

6.5.1 Reference Structure

Our first simulation is performed on this reference structure and consists in a quasistationary voltage ramp up to 3 V on the anode. The electron and hole equilibrium densities at 3 V are depicted in Fig. 6.9.

As expected the electrons are concentrated in the center of the nanowire (intrinsic region) due to the combined effect of the external bias and potential landscape. The hole concentration retains its maximum in the nanowire core but a high concentration (around 10^{18}cm^{-3}) is visible in the intrinsic region as well. Next we analyze the electron, hole and total current densities, all of them depicted in Fig. 6.10. We see that mainly the electrons contribute to the total current density but this comes as no surprise since the electron mobility in GaAs is roughly 20 times higher than hole mobility. Electrons are pulled near the base of the

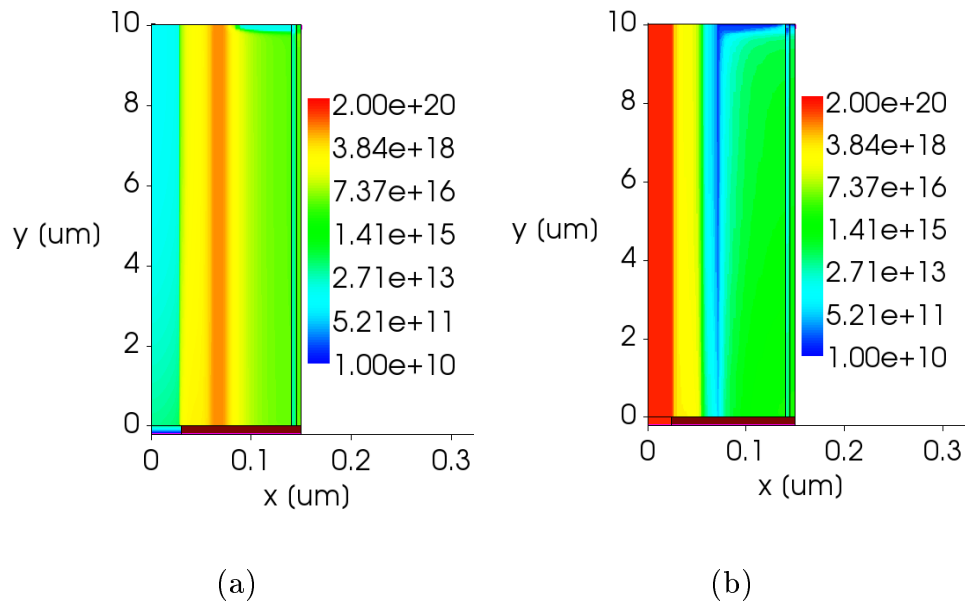


Figure 6.9: (a) Electron density [cm^{-3}]. (b) Hole density [cm^{-3}]. Image taken from [166].

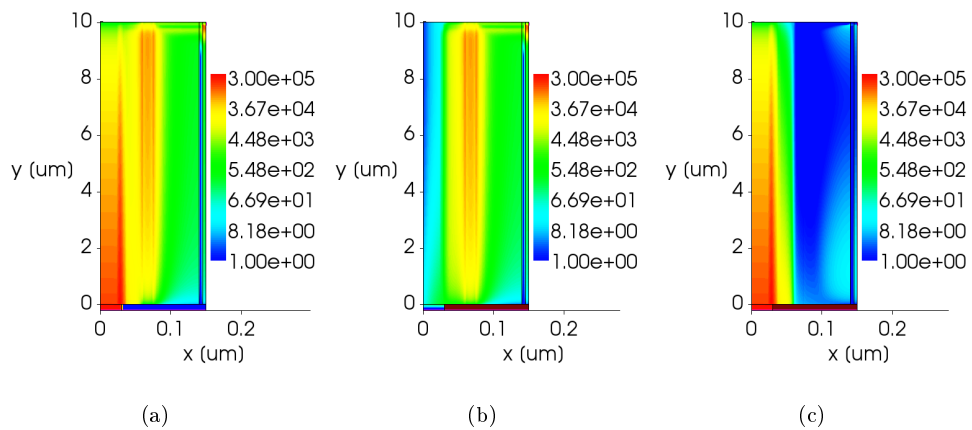


Figure 6.10: (a) Total current density [$\text{A} \cdot \text{cm}^{-2}$]. (b) Electron current density [$\text{A} \cdot \text{cm}^{-2}$]. (c) Hole current density [$\text{A} \cdot \text{cm}^{-2}$]. Image taken from [166].

nanowire by the positive voltage where they recombine with the holes from the heavy p-doped core. Thus only very few holes manage to reach the upper end of the nanowire where the cathode is placed.

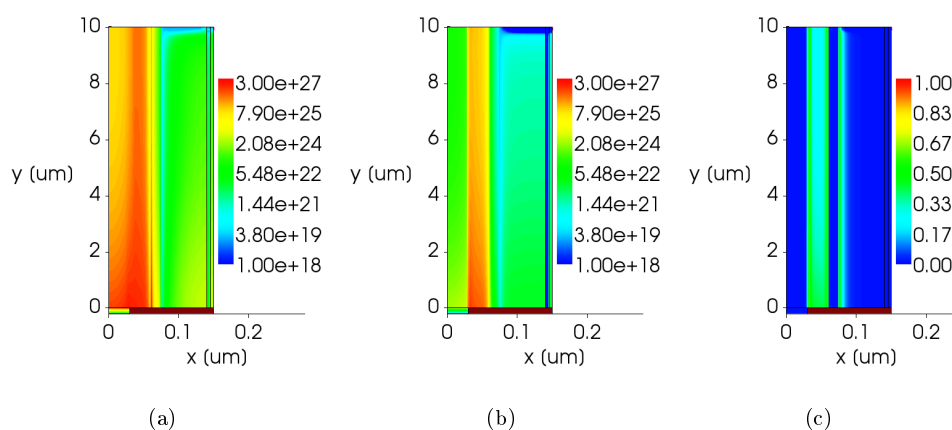


Figure 6.11: (a) Total recombination rate [$\text{cm}^{-3}\text{s}^{-1}$]. (b) Radiative recombination rate [$\text{cm}^{-3}\text{s}^{-1}$]. (c) Ratio of radiative to total recombination rate. Image taken from [166].

This becomes evident if we take a look at Fig. 6.11 where the total recombination, the radiative recombination and the ratio of the two recombination types are presented.

As we have assumed the highest total recombination takes place at the bottom of the nanowire near the anode. Radiative recombination has its peak in the center of the nanowire (intrinsic region) since there we have a high concentration of both holes and electrons. From Fig. 6.11c we can notice that the radiative recombination is highly localized in the center, in all other regions the non-radiative recombination is dominant.

6.5.2 Parameter variation

Next we would like to increase the radiative recombination rate and make our nanowire LED more efficient by varying the doping profiles or doping region radii. The reference structure is always the one described above and we only modify one doping or one radius at a time. The first analysis investigates the effect of various doping concentrations on the radiative recombination rate. Here we have to mention that we only change 3 region dopings (p^{++} core, n^{++} and n region), the intrinsic region remains in all cases unchanged.

In Fig. 6.12 the R_{rad} versus doping concentration is plotted for the three regions mentioned above. The doping in the p^{++} core and n^{++} region is already ex-

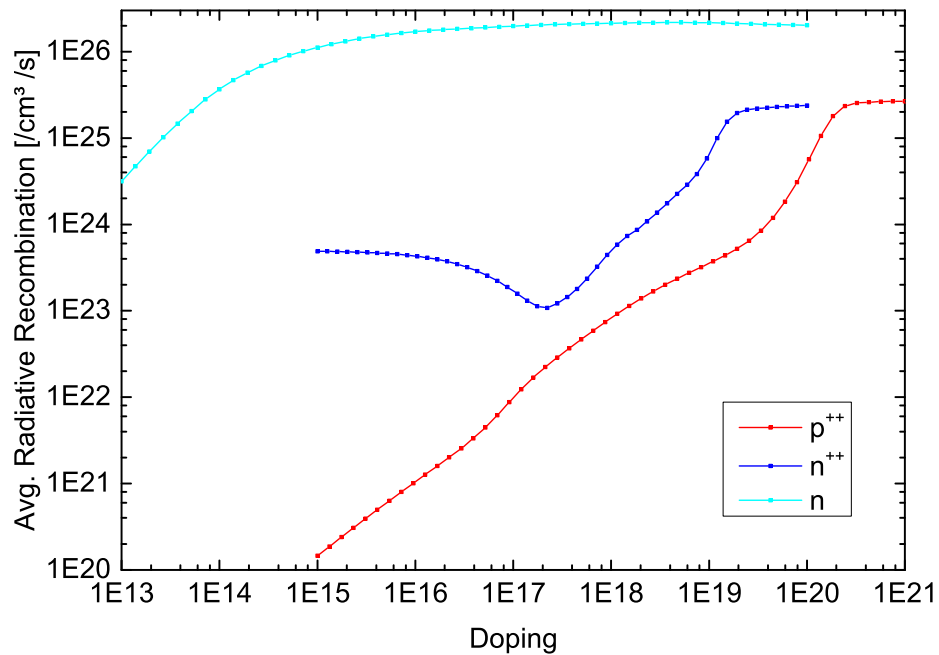


Figure 6.12: Average radiative recombination rate versus doping concentration in the n^{++} , p^{++} and n-region. Image taken from [166].

tremely high so we can only go down to lower values in those two regions. For the case of the p-doped core the radiative recombination decreases linearly with the doping, dropping down to $10^{20} \text{cm}^{-3} \text{s}^{-1}$ for $N_A = 10^{15} \text{cm}^{-3}$. The situation looks similar for the n^{++} doping, the R_{rad} follows the decrease in doping concentration linearly up to a value of 10^{17}cm^{-3} . However from there on, the radiative recombination rate remains constant at around $2 \cdot 10^{23} \text{cm}^{-3} \text{s}^{-1}$. This can be explained if we recall two facts: all our simulations are performed at 3 V external bias on the cathode and the electron mobility in GaAs is significantly higher than hole mobility. Even if we decrease the n-type doping to values lower than 10^{17}cm^{-3} , due to the external field the electrons will be injected in the intrinsic region maintaining the radiative recombination rate at around $2 \cdot 10^{23} \text{cm}^{-3} \text{s}^{-1}$. The doping in the low n-type region has the great impact on R_{rad} , when increased from 10^{13}cm^{-3} to 10^{15}cm^{-3} the radiative recombination also increases by two orders of magnitude. By increasing the doping in the n-region we basically increase also the electrical conductivity, a higher concentration of electrons can be injected from the electrode into the n^{++} region and from there in the intrinsic region. This is one important result we'll keep in mind for increasing radiative recombination

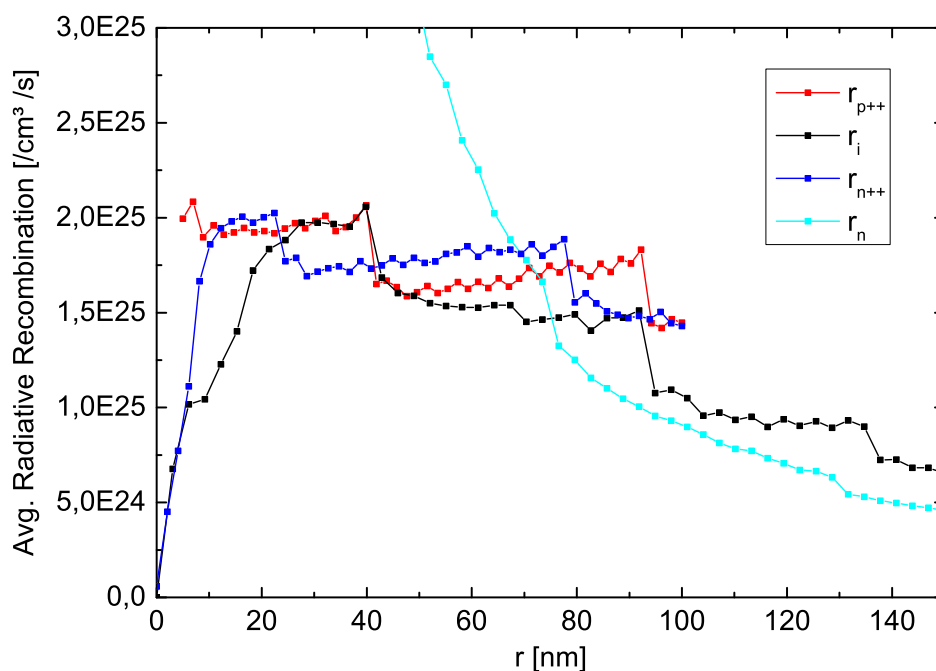


Figure 6.13: Average radiative recombination rate versus radius of doping region. Image taken from [166].

The radiative recombination rate versus the radius of the doping region is plotted in Fig. 6.13. The intrinsic region width displays an optimum at around 27-37 nm which can be explained as follows: if the intrinsic region is too narrow the recombination peak will move to the base of the nanowire - near the cathode - and will be mainly non radiative SRH recombination. If it is too large the e-h concentrations will drop and R_{rad} will follow. For the n^{++} region a similar behavior is observed but for different reasons: if the region is too narrow only a small number of electrons gets injected in the intrinsic region due to the high resistivity of the n-region (remember that the low n-region doping has its standard value of $5 \cdot 10^{13} \text{ cm}^{-3}$). Increasing it too much however will produce a high electron current density and will shift again the recombination towards the nanowire base. For the p^{++} doping region a similar behavior as in the case of the n^{++} doping can be seen.

The greatest impact on the radiative recombination is given again by the light n-doped region, varying its radius changes the R_{rad} dramatically. The n-doped region has a major impact on the electrons injected from the electrode into the n^{++} region. Increasing it, will decrease the electron density and by this

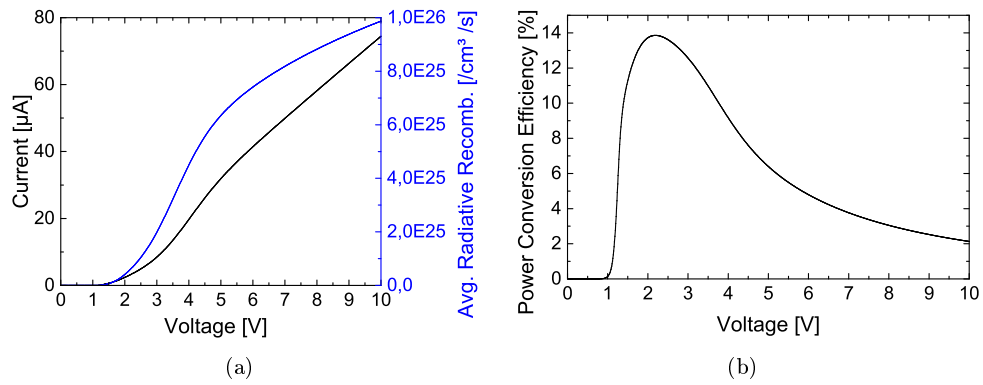


Figure 6.14: (a) Average radiative recombination and nanowire current versus input voltage. (b) Power conversion efficiency versus input voltage. Image taken from [166].

also the R_{rad} . This result is in good agreement with the one from the doping concentration analysis and we also keep in mind this possibility of increasing R_{rad} .

6.6 Laser Structure

The simulations presented so far focused on the influence of various parameters on the radiative recombination. In this final part we can make use of all the useful results to give some practical advice for nanowire laser design.

In order to have laser operation using GaAs as active material at room temperature an injected carrier density of around $2 \cdot 10^{18} \text{cm}^{-3}$ must be reached. From this we can estimate the radiative recombination rate in the device as:

$$R_{req}^{rad} \approx C \cdot n_{req} p_{req} \approx 1.8 \times 10^{27} \text{cm}^{-3} \quad (6.6.1)$$

We notice that this rate required for lasing is almost two orders of magnitude higher than the R_{rad} calculated in the previous section so we need to optimize the device considerably. The easiest way one can think of, to increase the radiative recombination would be to increase the electron and hole densities or in other words to inject more carriers. This can be simply achieved by increasing the bias voltage.

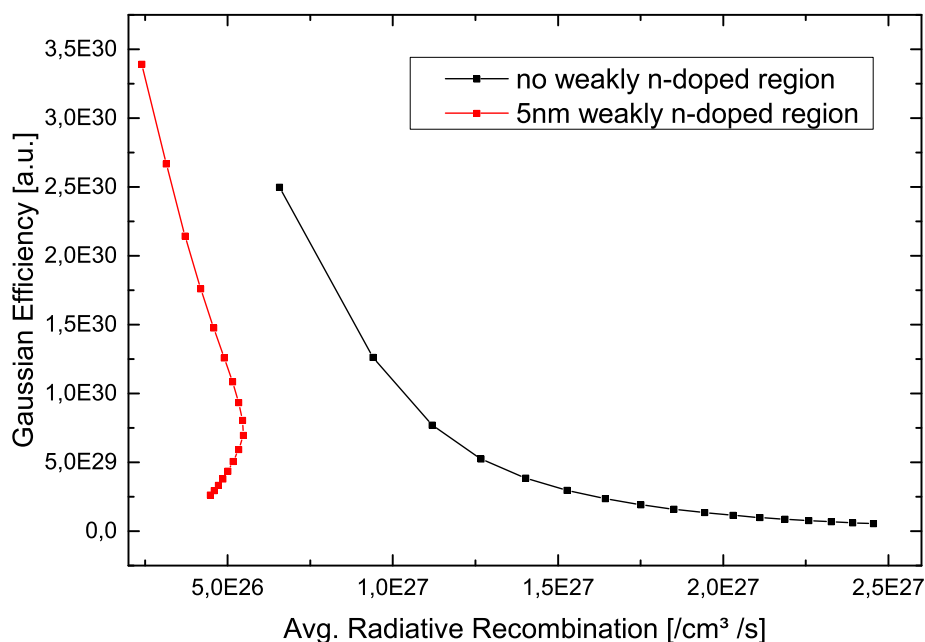


Figure 6.15: Gaussian efficiency and average radiative recombination for different bias voltages from 2 V to 10 V. Two devices are plotted: with no weakly doped n-region (black) and 5 nm weakly doped n-region (red). Image taken from [166].

However as we can see in Fig. 6.14 increasing the voltage will increase the current and the radiative recombination to some degree but the power conversion efficiency drops after 2 V to extremely poor values of 2% (Fig. 6.14b).

Therefore we have to find a better way, and here we can make use of the previous results. Two possibilities of increasing R_{rad} were identified: higher doping in the low n-type region and reducing the low n-type region width. With the first method we have seen however that the radiative recombination saturates for values of the n-doping larger than 10^{15} cm^{-3} , so we have no chance to achieve our target of $R_{rad} = 1.8 \cdot 10^{27} \text{ cm}^{-3}$.

The second alternative seems more promising and we will investigate it closer. In Fig. 6.15 the average radiative recombination for two devices, one with 5 nm weakly doped n-region and the second without n-type region, is plotted at various bias voltages - from 2 V to 10 V. Since we are talking about a laser we must include somehow the optical part as well when evaluating the performance. That's why on the y-axis of Fig. 6.15 we have Gaussian efficiency, which is

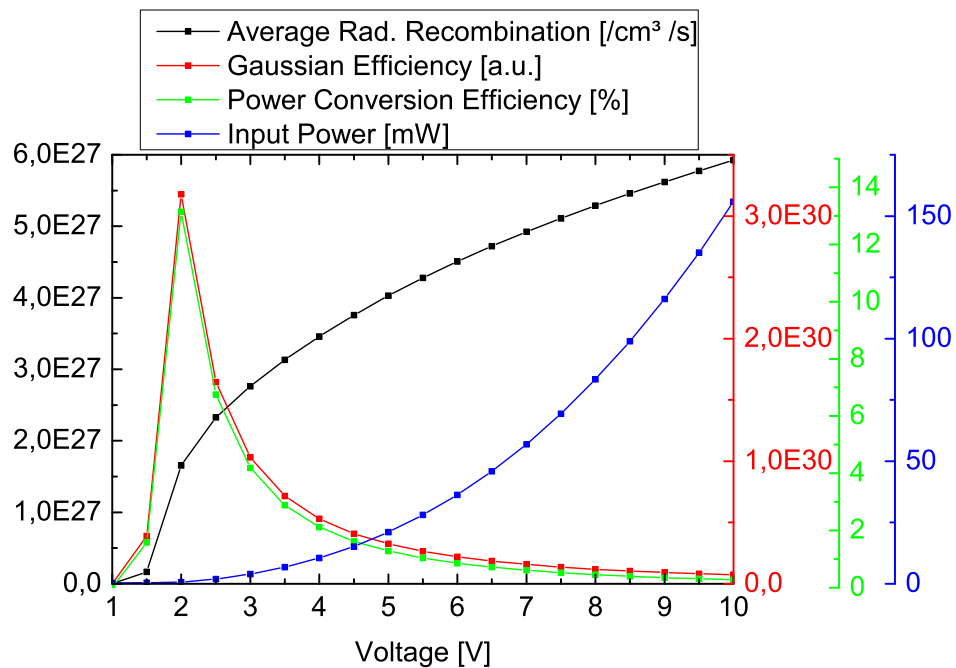


Figure 6.16: Gaussian efficiency, average radiative recombination, power conversion efficiency and input power plotted versus input voltage for the optimized laser structure. Image taken from [166].

nothing else than the radiative recombination weighted with a Gaussian along the nanowire radius, to account for the first mode of the laser. It is obvious that the design without weakly n-doped region is the better one, we achieve the desired R_{rad} at voltages between 2.5 V and 3 V, whereas with n-doped region R_{rad} saturates at around $5 \cdot 10^{26} cm^{-3}$.

Finally in Fig. 6.16 all FOMs for this design are presented and as one can see we achieve lasing threshold at voltages as low as 2 V.

6.6.1 Conclusion

In this section we have shown that with the help of advanced computer based simulation state-of-the-art optoelectronic applications for nanowires can be studied and optimized. We identify key design parameters and quantify their impact on the device performance. Thus important insights into the nanowire physics can be gained and practical design rules for optoelectronic devices can be drawn. Starting from the fabricated nanowire optoelectronic device by Mayer al. [162] we vary geometrical and material parameters and finally propose an

optimized structure that achieves lasing threshold at low voltages and room temperature.

7 Conclusion and Outlook

In this work we have theoretically investigated the high frequency behavior of InAs nanowire transistors. By employing advanced simulation techniques we have tried to give a reliable prediction for the upper frequency operating limit of these novel, promising devices.

The first part of this work covers the semi-classical treatment of these devices with an advanced Cellular Monte Carlo simulator [82, 85–87]. Self-consistent high frequency (HF) simulations obtained directly from Monte Carlo computed currents have not been performed for nanowires so far. Our approach is new since we determine the H-matrix from the Fourier transformation of the CMC currents and not from compact models based on elements extracted from transfer and output curves as reported in previous Monte Carlo studies [167]. To our knowledge this approach has been implemented for the first time in the CMC code [86, 87] and for other groups that use a similar approach we can only mention Rodilla *et al.* [168]. The large signal simulation on InAs nanowires using the Harmonic Balance (HB) algorithm was also performed for the first time in this work.

Thus we were able to fully characterize the InAs nanowire transistor performing quasistatic, small-signal and large signal analysis, all within the same CMC framework. After having calibrated the output characteristic of the simulated device with the experimental data from Blekker *et al.* [24] we have performed several DC simulation with various doping profiles and fixed charges at the dielectric interface. We have compared the resulting I_D - V_D curves and determined the impact of the doping profile on the output characteristics. Increasing the unintentional doping too much or having too many fixed charges emulating interface trap states will reduce the drain current and increase the intrinsic capacitance of the channel. One of our findings is that the electrons are accumulated at the semiconductor/dielectric interface, a difference of about two orders of

magnitude in electron concentration when compared with the center of the wire. This result is in good agreement with both measurements for bulk InAs samples, where the Fermi level pinning at the interface due to positive trap states is well known, but also with very recent direct measurements on InAs nanowires [79]. High concentrations of positive surface trap states have been measured which lead to an electron accumulation on the outer radius of the nanowire.

The great advantage of this first approach, the Cellular Monte Carlo method is its physical accuracy, basically no fitting parameters were used. The entire simulations flow from the band structure calculation using the Empirical Pseudopotential Method (EPM) to the Harmonic Balance (HB) large signal analysis takes place in the same CMC framework. Therefore all deduced figures of merit, like transit frequency (f_T), maximum frequency of oscillation (f_{max}) or harmonic content originate from the physical CMC output and are not based on any compact models for high frequency characterization. In addition due to the Cellular Automaton (CA) approach the computational times required for a Monte Carlo (MC) device simulation remain within reasonable limits (of course this depends mainly how many voltage points are simulated, how many electrons are injected and what are the physical dimensions of the device itself).

The predicted intrinsic HF performance is about one order of magnitude higher in terms of f_T (65 GHz) and f_{max} (112 GHz). After adding extrinsic parasitic elements comparable with those in [24] we observe the same abrupt decrease in Short-Circuit Gain and Mason's Unilateral Gain as the measured, experimental values. The large signal analysis displays the typical input versus output gain behavior: the input power referred 1dB compression point occurs at around -2dBm, from there on the P_{IN} - P_{OUT} curve flattens and the amplifier enters the output power saturation regime. This regime is associated with a decrease in gain, the so called gain compression. One observation can be made here: the output power is very small, easily explained by the little value of the drain current. This is however the current of only one nanowire transistor, if more power is needed for the specific application, a nanowire array (NA) can be easily implemented as shown in the recent publication of Johansson *et al.* [26]. An array consisting of about 1000 nanowires will deliver currents in the order of mA, so three orders of magnitude higher currents.

Beside the above-mentioned advantages of the CMC simulator we have to enumerate also some drawbacks: the great physical accuracy at device level becomes a burden when simulating complex circuit topologies. The simulation time and resources tend to become impractical so another approach is needed.

The second method described in this work is the HF simulation of InAs nanowire transistors based on the hydrodynamic model. This energy balance model is derived from the Boltzmann Transport Equation (BTE) taking into account higher order moments. It also takes into consideration the charge carrier temperatures (electrons and holes) and the lattice temperature. Other advanced models can be coupled in this state-of-the-art hydrodynamic simulator: velocity saturation and interface trap states. By making use of this second TCAD framework we are also able to reproduce with great accuracy the experimental output curves from Blekker *et al.* [24]. Next we also redo the HF characterization of the nanowire device making use of a special feature of the TCAD framework, namely the Sentaurus Mixed Mode.

This feature allows us to simulate physical devices connected to external parasitic networks a lot faster than the CMC framework. Each device is simulated using the coupled set of partial differential equations defined in the hydrodynamic and they are connected to each other by circuit nodes defined in a SPICE-like netlist. This way an optimal trade-off between simulation accuracy and speed can be achieved.

For the resulting high frequency figures-of-merit a value of 72 GHz is obtained for f_T and 270 GHz for f_{max} .

We notice the excellent agreement of the estimated intrinsic transit frequency obtained via the two different methods: 65 versus 72 GHz. If we also consider that the nanowire transistor simulated by the CMC approach had a rectangular cross-section, hence a larger parasitic capacitance while the nanowire modeled with the Sentaurus TCAD had circular cross-section, we can easily explain the 10% difference. For the maximum frequency of oscillation both methods predict significantly higher intrinsic values.

There is a difference between the CMC and the hydrodynamic simulation, the frequency obtained by the Monte Carlo approach is lower by a factor of 2.5. We explain this by the different methods used to extract the f_{max} from the intercept

of the Mason's Unilateral Gain (MUG). From the definition of the MUG we remember that all internal feedback needs to be neutralized a task that can be achieved without problems in the Sentaurus simulation. However in the CMC simulation, as mentioned in chapter 3, the current is extracted not from the contacts but as an average over a contact region, placed sufficiently far from the injecting electrode. It becomes obvious that this contact region is overlapping with the surrounding gate and a parasitic coupling is unavoidable. Still both methods predict significantly better intrinsic performance for the MUG.

These final results are in good agreement with very recent findings from Johansson et al. [26]. There an optimized contact design yielded impressive results for the extrinsic cutoff and maximum frequency of oscillation: 103 GHz and 155 GHz.

This work was intended to give a first estimation of the high frequency performance of the InAs nanowire transistors. The accurate modeling and predictive simulation of novel nanowire transistors is however just the first step towards future high speed low voltage devices for high frequency and optoelectronic applications.

We believe the hybrid integration of III/V nano-devices on Si chips to be the most promising candidate to fulfill future ITRS requirements. High integration density and low cost of traditional Si chips can be coupled with the superior mobility of III/V semiconductors resulting in novel, ultra-efficient devices.

The next step for our theoretical study would be to simulate also the Si devices and finally have a full simulation of the hybrid integrated devices. For this purpose the CMC framework has already included many other material files (Si, GaAs, InP, InGaAs, InAlAs, GaN); therefore simulating the distinct devices should not pose any problem. In fact several HF simulation studies employing the CMC simulator have been performed on GaN and InGaAs/InAlAs HEMTS [85–87]. The only challenge remaining will be to simulate the hybrid devices.

After some first predictions and estimations of device performance using the MC approach we can increase the complexity of the simulated devices. For this part task the MC approach becomes unpractical and we can switch to a more suited hydrodynamic simulation of the multiple device circuits. By transferring

all the physical insights obtained in the MC simulation to Sentaurus TCAD, calibrating thus the physical models available there we should be able to have a fast, physical and reliable simulation tool.

The Sentaurus Mixed Mode should be capable of simulating large area devices with the accuracy of a full band Monte Carlo simulation as shown in the case of the InAs nanowire device, opening the path for new circuit concepts and architectures.

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List of Publications

- [1] D. Popescu, B. Popescu, G. Jegert, S. Schmelzer, U. Boettger, and P. Lugli, "Kinetic monte carlo simulation of $SrRuO_3/SrTiO_3/SrRuO_3$ thin film capacitors," *Electron Devices, IEEE Transactions on*, SUBMITTED.
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