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CMOS Integrated Impedance Sensor Arrays for Cell Adhesion Measurement

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Abstract

This thesis presents a CMOS integrated sensor for impedance measurements with cultured cells. A model of the impedance under study, comprising contributions of the electrode, the electrolyte, and the cells, was developed using a combination of analytical and numerical techniques. Based on the model, boundary conditions were derived and a suitable conversion principle was chosen and implemented. The sensor was produced in a 0.35 micron standard CMOS technology with additional process steps for manufacturing gold electrodes. The chip features 64 positions for sensing the cellular impedance, which are addressed and read out by an integrated circuit. The performance of the sensor was verified experimentally. Cell adhesion and death could be detected reliably, and different levels of local cell coverage could be resolved. Due to the localized measurement, fluctuations of the impedance caused by movements of the cells could also be resolved.

Zusammenfassung

Die Arbeit stellt einen CMOS-integrierten Sensor zur Impedanzmessung an Zellkulturen vor. Mit Hilfe von analytischen und numerischen Ansätzen wurde ein Modell der zu messenden Impedanz entwickelt, das Beiträge von Elektrode, Elektrolyt und Zellen umfasst. Basierend darauf wurden Randbedingungen festgelegt sowie ein geeignetes Wandlerprinzip gewählt und implementiert. Der Sensorchip wurde in einer 0,35 µm CMOS-Technologie mit Backend-Prozessschritten zur Herstellung von Goldelektroden gefertigt. Seine 64 Positionen zur Messung der Zell-Impedanz werden durch eine integrierte Schaltung ausgelesen. Die Leistungsfähigkeit des Sensors wurde experimentell bestätigt: Adhäsion und Absterben von Zellen konnten nachgewiesen werden, unterschiedliche Grade der Zellbedeckung wurden ortsaufgelöst erfasst. Mittels der ortsaufgelösten Messung konnten auch durch Bewegungen der Zellen entstehende Fluktuationen der Impedanz sichtbar gemacht werden.

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Contents

1 Introduction

Chemical analyses today are sophisticated enough to identify and measure the concentration of virtually any substance, even in trace amounts [1, 2]. But this sophistication comes at the price of expensive and highly delicate laboratory equipment which is often affordable only for specialized institutions. However, in many situations the detection of chemical substances is needed where such equipment is not available. Testing drinking water for contamination is one such scenario.

Drinking water in developed countries is usually tested and – if necessary – treated at local water utilities. Tests are performed periodically for a range of parameters [3] with clearly defined acceptable limits [4], such as

- acidity/basicity (pH),
- electrical conductivity,
- concentration of various metals, ions and organic compounds, and
- biological contamination by microorganisms.

The drinking water is then delivered via a network of pipelines directly to the consumer.

In developing countries, the infrastructure for drinking water is often nonexistent or unreliable, making it necessary to consume water from sources which might be polluted. In these situations, point-of-use water treatment can be employed to filter and disinfect the water in order to minimize the risk of disease. This mainly takes care of biological (microbial) contamination [5]. It is however impractical to also perform all the tests mentioned above on the treated water to determine its safeness regarding chemical contaminations, although they can also pose severe health risks [6–8].

Recycling and reuse of waste water on a community level and in future "green buildings" is another scenario of growing importance, especially as global climate change makes sustainable water use a vital necessity in arid regions. Residential waste water may contain a virtually infinite range of substances such as pharmaceutical and endocrine disrupting chemicals [1]. Here, the uncertainty about which contaminants should be tested for and the lack of data on their toxicity make an assessment of the potability of recycled water by chemical analyses nearly impossible.

The deciding factor for the safeness of drinking water is its impact on the human organism, i.e. its biological activity and availability. This is a functional question which cannot be reduced to the presence of specific substances and their exact concentration. Chemical analyses by their nature cannot give information on the biological activity of a sample. This is the strength of biosensors, which can directly measure the reaction of biological systems to a stimulus [2, 9].

A biosensor can be broadly defined as a "device that uses specific biochemical reactions mediated by isolated enzymes, immunosystems, tissues, organelles or whole cells to detect chemical compounds usually by electrical, thermal or optical signals" [10]. Biosensors take advantage of the natural reactions of the biological element to the target substances by transducing them into a physical parameter which is more easily quantifiable. A classical example is the biosensor for blood glucose measurement relying on the enzyme glucose oxidase. By catalyzing the oxidation of glucose, it converts glucose concentration, which is not directly measurable, into an electrical current, which is then measured [11].

While in this example only one specific substance is of interest, biosensors can also utilize the complex network of receptors and signal pathways of living cells to detect a wide range of substances, all of which may not even be known a priori. Cells are able to adapt to changing environmental parameters by regulating internal processes, which causes measurable changes in observable parameters such as oxygen uptake, excretion of metabolic products, or cell morphology [12, 13]. This makes cell based sensors especially suited for the detection of many harmful substances, because their toxicity for the organism generally arises from their interference in cellular processes.

Among the ways to obtain information from cells, the monitoring of cell adhesion and morphology via impedance measurements stands out as especially interesting. Cell shape and movement are dependent on a complex interplay of intracellular processes and as such highly sensitive to external conditions and a wide range of chemical compounds [14, 15]. The advantage of impedance measurements lies in providing quantitative data in real time, whereas optical observations with microscopes generally only provide qualitative information at measurement endpoints.

Cell impedance measurements are therefore a very promising approach to monitor water quality in scenarios such as those described above. However, existing systems for cell impedance monitoring are generally intended for a controlled laboratory environment with specially trained personnel. They rely on passive sensor substrates and externally connected electronics to drive the transducers and amplify the signals. This makes them quite bulky and

susceptible to noise and electromagnetic interference. In addition, the often delicate connections between microelectrodes and external wiring limit their reliability.

In order to make cell impedance measurements suitable for application in water quality monitoring, a robust and more compact cell sensor system is needed. This can be achieved in part by integrating the electronics for interfacing with the transducers and amplifying the signals on the sensor chip, using e.g. standard CMOS technology. The reduced physical distance between the transducer element and the associated front-end electronics translates into less susceptibility to interference and a higher signal-to-noise ratio. On-chip analog-to-digital conversion and data multiplexing can furthermore reduce the number of external connections and thus improve the robustness of the system.

This thesis describes the development of a CMOS integrated impedance sensor array for application in cell adhesion measurements. The next chapter of this thesis will introduce the basics of cell impedance measurements, including brief sections on the electrochemical and biophysical origins of the impedance under study. Previous work on measurements of cellular impedance, including their application in various fields such as drug discovery, and commercially available systems will also be touched upon.

Chapter 3 deals with modeling the impedance under study in order to obtain a deeper understanding of it, which is a prerequisite for the development of a suitable integrated sensor. Published analytical models, which were originally developed in order to extract information from impedance spectroscopy data, are evaluated and the impact of different parameters on the total cellular impedance is determined. Using finite element modeling, a numerical approach to the impedance of cells growing on planar electrodes is then developed in order to cover the cases where analytical models are not feasible. It is shown that low-complexity equations can accurately reproduce the behavior of these models under variation of various parameters.

The study of the expected composition and behavior of the impedance of cellular monolayers led to the choice of impedance-to-frequency conversion as the measurement principle to be used for the cell impedance sensor, which is introduced in Chapter 4. In the same chapter, non-ideal effects degrading the measurement accuracy and their impact on the sensor design are discussed.

After these considerations, Chapter 5 describes the actual implementation of the sensor on a test chip fabricated in a 0.35 µm CMOS technology. After a description of the general chip specifications, the individual circuit blocks are discussed. Finally, the results of characterization measurements are presented.

This is followed by the validation of measurement principle and sensor

implementation by experiments with living cells, which are described in Chapter 6. Finally, in Chapter 7 the results are summarized and this thesis is concluded.

2 Measuring Cellular Impedance: Fundamentals and State of the Art

Electrical impedance describes the relationship between voltage and current by its magnitude and relative phase, or equivalently the real and imaginary parts of a complex value, for an applied sinusoidal excitation of a given frequency. In most cases, the impedance is frequency-dependent, so a spectrum of impedances measured at several frequencies will contain more information than a single impedance value. As different materials have different dielectric properties, which can also change over time (e.g. due to aging), impedance spectroscopy has become a valuable analytical tool with applications in electrochemistry, materials science, and recently also biology.

The method at its core consists of measuring the electrical impedance of the object under study across a range of frequencies. The thus obtained impedance spectrum is then analyzed to obtain information about the composition and state of the sample. This in general requires a model of the individual components which make up the total impedance. Often, this model simply takes the form of an equivalent circuit diagram of lumped elements such as resistors, capacitors and inductors. Sometimes also effects emerge which cannot be represented by a combination of these elements in a straightforward manner, or a deeper insight into their origin is needed. In these cases a different approach and different tools, such as numerical methods, are needed to create a model. Fitting the model parameters to the measured data then gives insight into the target object.

Giaever and Keese [16] were the first to apply electrical impedance spectroscopy to the study of living biological cells grown in culture. To this end, they evaporated small gold electrodes onto a cell culture dish, on which cells were then grown in culture medium. They also developed a model which allowed them to interpret the impedance data in terms of the capacitance and resistance of the cell layer as well as the height of the cell-substrate gap [17] (see also Section 3.1).

Apart from the target, many other factors influence the impedance spectrum. Their effects act as "background noise" which partly obscures the interesting signal represented by the impedance of the target. These effects also have to be considered in the impedance model in order to be able to correctly identify

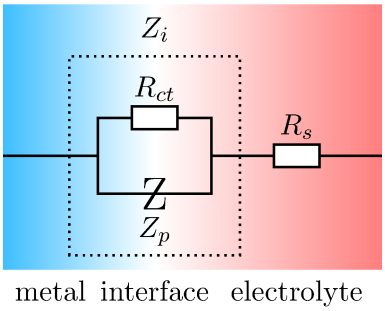

Figure 2.1: Equivalent circuit diagram of a metal electrode in contact with an electrolyte.

them and separate them from the interesting signal in measured data. The impedance arising at the interface of electrode and electrolyte is the most significant of these factors and is described in the following section.

2.1 Impedance of Solid Metal Electrodes in Electrolytes: Electrochemical Basics

When a metal is brought into contact with an electrolyte, a number of processes occur at the boundary between these two phases. From an electric point of view, these processes give rise to a quite complex impedance. Figure 2.1 shows an equivalent circuit diagram in which the most important effects are each represented by a corresponding electrical element[1]: The charge transfer resistance R_{ct} arising from faradaic processes, the polarization impedance Z_p, and finally the spreading resistance through the electrolyte R_s. The combined impedance of R_{ct} in parallel with Z_p will be referred to as the interfacial impedance Z_i. Both its components can be considered linear only for quite small applied voltages and currents [18, 19]. This section will give a short overview of these effects and how they relate to the design of a cell impedance sensor.

2.1.1 Charge Transfer Across the Electrode-Electrolyte Interface

A metal is an electronic conductor, whereas an electrolyte is an ionic conductor. The different mechanisms of charge transport mean that current cannot pass

[1] The electrode potential is omitted here because it cancels when measuring a voltage between two electrodes of the same material, and its effects are not important for measuring impedance. It could be modeled by a voltage source in series with Z_i.

directly between the two materials. Instead, the passage of charge carriers through the interface is coupled to reduction and oxidation (collectively: redox) reactions, in which electrons are transferred from the metal to the solution molecules and vice versa.

Two or more metal electrodes connected by an electrolyte form an electrochemical cell. In some cases, redox reactions at these electrodes can occur spontaneously without an applied potential, which allows e.g. the extraction of electrical energy from a galvanic element when the two electrodes are connected to form a closed circuit. On the other hand, some metals are very stable (inert), meaning that they do not undergo redox reactions and therefore do not allow direct current to pass into the electrolyte unless a significant voltage is applied to them. The current associated with the redox reactions occurring at the interface is called faradaic current I_f. If the oxidation reaction at the electrode dominates, i.e. metal atoms losing electrons and going into solution, this electrode is called an anode. If the reduction reaction dominates, i.e. ions gaining electrons and being deposited on the electrode, it is a cathode. In any case, faradaic current flowing across the electrode-electrolyte interface is always accompanied by mass transfer, thereby changing the electrode properties.

If left undisturbed, i.e. without external current, any electrode in an electrolyte will develop an electric potential difference with respect to the electrolyte. This potential cannot be measured directly, only with respect to another electrode. At this open circuit potential, the system is in equilibrium and no net reaction takes place, since the difference in electric potential exactly balances the difference in chemical potential between metal and electrolyte [18, sec. 3.1.2].

The faradaic current density j_f in both directions across the interface is generally an exponential function of the deviation from the equilibrium potential (called overpotential η). It is therefore sometimes modeled by an equivalent circuit of two antiparallel diodes [20, sec. 3.2.2]. For small overpotentials, generally in the range of few tens of millivolts, the faradaic current density can be linearized and thus be described by the charge transfer resistance R_{ct} [18, sec. 4.2.2]:

$$j_f = j_0 \frac{qz}{k_B T} \eta = \frac{\eta}{R_{ct}} \quad \text{with } R_{ct} = \frac{k_B T}{qz j_0} \tag{2.1}$$

There, z is the valence of the ions and j_0 is the exchange current density, which plays a role similar to the saturation current in a diode [18, 21]. The exchange current density can be considered a measure of how easily charge can move across the interface. Materials with a high value of j_0 make non-polarizable

electrodes, meaning the electrode potential only responds weakly to the application of a current. A material with a low value of j_0 correspondingly makes a polarizable electrode, which responds to an applied current by a large change in potential.

Since the electrode impedance is a parasitic element for the purposes of cell impedance measurement, it is desirable to minimize it. However, this cannot be achieved by choosing an electrode material with a low charge transfer resistance (high exchange current density), because the electrodes have to be chemically inert in order to obtain stable measurement conditions. As redox reactions at the electrodes are associated with mass transfer, they are to be avoided, otherwise the electrodes would degrade quickly. In other words, the charge transfer resistance R_{ct} should be high enough that the faradaic current path in Figure 2.1 can be neglected. Therefore the electrodes must be operated close to their equilibrium potential and the excitation applied to them should be as small as practically possible. Gold and Platinum are inert and biocompatible, which is why they are commonly used as electrode materials for biosensors.

2.1.2 Polarization Impedance of the Phase Interface

The surface charge of the electrode resulting from the equilibrium potential attracts ions from the solution, which form a charged layer of opposite sign in front of the electrode surface. In analogy to the two plates of a capacitor, this creates the so-called double layer capacitance. Through this capacitance alternating current can flow between electrode and electrolyte, even when the applied voltage is not high enough to trigger redox reactions. In this case no actual charge transfer across the electrode-electrolyte interface occurs, only the interfacial double layer is charged and discharged. The current-voltage relationship of the electrode-electrolyte interface in absence of faradaic currents is described by the polarization impedance.

In the commonly used Stern model of the double layer capacitance, the attracted ions form a first layer, which can be considered fixed, and an additional diffuse layer extends the charged region, also contributing to the capacitance [18, sec. 3.4.1]. However, in complex electrolytes such as cell culture media, the many different molecules interacting with the electrode in various ways limit the usefulness of this model. Data obtained e.g. from electrochemical impedance spectroscopy measurements thus often cannot be explained sufficiently if a purely capacitive polarization impedance is assumed.

It is therefore necessary to describe the non-faradaic behavior of the elec-

trode-electrolyte interface by a more general polarization impedance Z_p. The model most widely used to account for the deviation from capacitive behavior is the constant phase element (CPE), which describes the polarization impedance by an equation of the form

$$Z_{CPE} = \frac{1}{Q(i\omega)^{\alpha}} \tag{2.2}$$

where Z_{CPE} has the unit $\Omega\,\mathrm{cm}^2$, α is a dimensionless positive constant and the CPE parameter Q has the unit $\Omega^{-1}\,\mathrm{cm}^{-2}\,\mathrm{s}^{\alpha}$, which however is a purely phenomenological description, except for $\alpha \in \{-1, 0, 1\}$, corresponding to an inductance, resistance, and capacitance, respectively [22]. As its name implies, the CPE is characterized by a constant phase angle of $-\frac{\alpha\pi}{2}$ radians at all frequencies. Reported values for α are usually between 0.8 and 1, depending on factors such as electrode material and the chosen electrolyte. Although the physical meaning of the CPE impedance and the mechanisms giving rise to it have been under study for some time, no definitive explanation has emerged so far. From experiments it seems however that the smoother and cleaner the electrode surface, the closer the value of α becomes to unity [23].

An even more general and thus flexible model of the polarization impedance was published by Ragheb and Geddes [24]. It takes the form of

$$Z_p = Af^{-\alpha} - iBf^{-\beta} \tag{2.3}$$

with the complex impedance Z_p in $[\Omega\,\mathrm{cm}^2]$ and α and β positive constants. In analogy to the CPE impedance, the parameters A and B have the units $\Omega\,\mathrm{cm}^2\,\mathrm{s}^{-\alpha}$ respectively $\Omega\,\mathrm{cm}^2\,\mathrm{s}^{-\beta}$, but only $\alpha = 0$, giving a resistive real part, and $\beta = 1$ for a capacitive or $\beta = -1$ for an inductive imaginary part make physical sense. This model is basically an extension of the constant phase element, since it simplifies into (2.2) for $\alpha = \beta$ and $B/A = \tan\frac{\pi\alpha}{2}$.[2] It can be considered a phenomenological description of the polarization impedance, as no physical significance was ascribed to the model parameters by the authors. However, it provides an improved fit to measured impedance spectra.

The impedance described by Equation (2.3) can also be understood as a resistance in series with a capacitance, where the value of each of the components is frequency-dependent [19]. The resistance R_p is then just the real part of Z_p, i.e. $Af^{-\alpha}$, while the equivalent capacitance C_p can be calculated as

$$C_p = \frac{f^{\beta-1}}{2\pi B} \tag{2.4}$$

[2] This is easy to see if the identity $i^{\alpha} = \exp(i\frac{\alpha\pi}{2}) = \cos(\frac{\alpha\pi}{2}) + i\sin(\frac{\alpha\pi}{2})$ is used to expand Equation (2.2) into $Z_{CPE} = Q^{-1}(2\pi f)^{-\alpha}\cos(\frac{\alpha\pi}{2}) - iQ^{-1}(2\pi f)^{-\alpha}\sin(\frac{\alpha\pi}{2})$

Table 2.1: Parameters of the polarization impedance of gold electrodes in cell culture medium, normalized to an electrode area of 1 cm^2. The values were extracted from a series of six impedance spectroscopy runs from 10 mHz to 1 MHz, with an excitation amplitude of 50 mV.

	mean	standard deviation
A	$1.18 \cdot 10^3$	$4.77 \cdot 10^2$
B	$1.08 \cdot 10^4$	$8.04 \cdot 10^2$
α	1.07	0.11
β	0.92	0.01

Preliminary impedance spectroscopy measurements performed on gold electrodes suspended in cell culture medium indicated that the polarization impedance for this combination of materials is dominated by the capacitive part. Table 2.1 shows extracted values of the parameters for a fit to Equation (2.3), and in Figure 2.2, a plot of the polarization impedance with these parameter values is shown. The value of B is significantly higher than A, and the higher frequency exponent α means that the real part becomes negligible at higher frequencies. In this case, Equation (2.4) is a valid first order approximation of the polarization impedance.

2.1.3 Spreading Resistance

The spreading resistance through the electrolyte is determined by the bulk electrolyte conductivity and the electrode geometry. The resistivity of the cell culture and assay medium (Dulbecco's Modified Eagle Medium) used for the experiments was measured as $65\,\Omega\,\mathrm{cm}$ at room temperature, in good agreement with published values [25].

The formula for the total resistance

$$R = \rho \frac{l}{A}$$

for a volume of resistivity ρ with a cross section A and length l however does not hold for geometries where the current is not confined to a linear path, such as coplanar electrodes. Here, the quotient $\frac{l}{A}$ must be replaced by the cell constant, which can be determined experimentally for a given electrode geometry by using an electrolyte of known resistivity.

For the case of a planar electrode and an infinitely large counter electrode, approximations can be given for the spreading resistance [20, 21]. For a

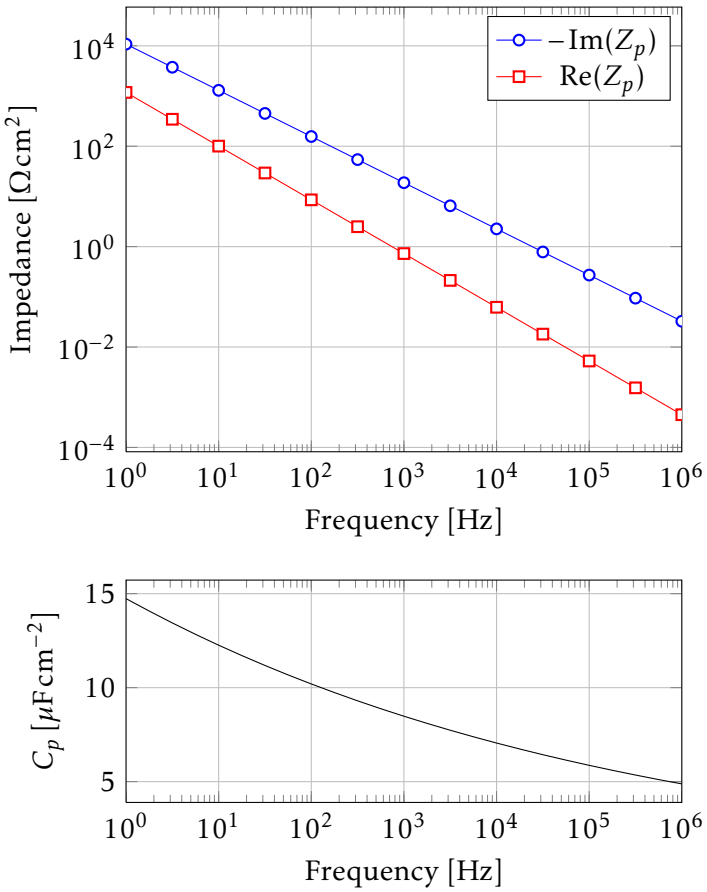

Figure 2.2: Plot of the polarization impedance with the parameter values shown in Table 2.1. The top plot shows the impedance separated into real and imaginary part, below is the equivalent series capacitance as given by Equation (2.4).

circular electrode of radius r_e, it is given by

$$R_{s,rad} = \frac{\rho}{4r_e} \tag{2.5}$$

and for a square electrode of edge length a by

$$R_{s,sq} = \frac{\rho \ln 4}{\pi a} \tag{2.6}$$

2.2 Biophysical Origins of the Cellular Impedance

Cell impedance measurements fundamentally rely on the difference of the electrical characteristics, e.g. conductivity and permittivity, between the cells and the electrolyte surrounding them, usually some culture medium. From this it follows that the greater the contrast in electrical behavior, the more easily the cellular impedance can be separated from the electrolyte impedance. In order to provide the cells with an environment in which they can survive, the culture medium needs to contain various ions in concentrations very similar to those in the original organism, so that vital ion concentration gradients across the cell membrane are maintained in direction and magnitude. This means that from the point of view of bulk conductivity, "inside" the cell looks very similar to "outside".

However, all cells have a cell membrane which surrounds the various cellular organelles and the intracellular fluid, called cytosol, thus separating the interior from the exterior of the cell. This membrane consists of a bilayer of phospholipid molecules and is a natural insulator. It is however punctuated by numerous embedded ion channels, which selectively allow the flow of charge and molecules into and out of the cell [26]. This results in an electrical behavior of the cell membrane which can be modeled by a capacitance in parallel with a resistance [27, 28]. While the membrane resistance can vary over several orders of magnitude depending on cell type and the state of the ion channels (open or closed), its capacitance is mostly fixed. Published values for the resistance therefore range from 10^2 to $10^5\,\Omega\,\mathrm{cm}^2$, with most around $1\,\mathrm{k}\Omega\,\mathrm{cm}^2$. The membrane capacitance is usually given as around $1\,\mu\mathrm{F\,cm}^{-2}$, with published data between 0.5 and $4\,\mu\mathrm{F\,cm}^{-2}$ [20, 25, 27–29].

The interior of the cell can be approximated by another resistive element, although due to the much larger impedance of the cell membrane, it is often neglected. The resistivity of the cytosol cannot be given precisely, but can be assumed to be on the same order of magnitude as the extracellular medium. The electrical behavior of a single cell can thus be described by the equiva-

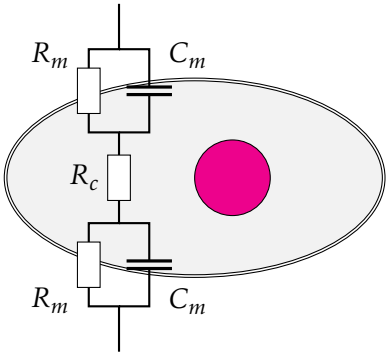

Figure 2.3: Schematic representation of a single cell and equivalent circuit diagram.

lent circuit diagram given in Figure 2.3, with the membrane resistance R_m, capacitance C_m, and intracellular resistance R_c.

At low frequencies, the high resistance of the membrane compared to that of the surrounding electrolyte thus makes the cell appear as an insulator, and current is forced to flow around it. At higher frequencies, the membrane capacitance allows current to pass and begins to short-circuit the membrane resistance. At sufficiently high frequencies, the membrane is effectively electrically transparent, and the electrical behavior of the cell is dominated by the resistance of the cytosol and the other elements of the cytoplasm [27, 28].

The range of interesting frequencies for cell impedance measurements therefore depends on whether the interior composition of the cells is to be studied or a more external view is preferred. The study of cell organelles and cytosol has to be performed at frequencies where the membrane impedance is negligible. For the study of cell shape, movement, or the confluence state of a cell layer on the other hand, the excitation frequency must be low enough that the cell membrane still represents a significant contribution to the total impedance.

2.3 Previous Work

Since the pioneering research of Giaever and Keese [16], various groups have expanded on their work and studied the application of impedance measurements to cell biology and other research aspects such as drug discovery and toxicology tests. This section is intended to give an overview of the historical development of this field and the published results that could be drawn on in the preparation of this thesis.

2.3.1 Research on Cell Impedance Measurement

The application of electrical methods to the study of cultured cells can be broadly divided into two approaches: One is the use of microelectrodes to record the static and transient potentials generated by the cells. Any living cell has a transmembrane potential which arises from the different ion concentrations inside and outside the cell [26–28]. Electrically active cells such as neurons and cardiac cells can also generate transient action potentials which can be evaluated with regard to their spike rate and other parameters [30]. The other approach is to apply an electrical signal and measure the response generated by the cells. Impedance measurements belong in this second category. The study of the electrical signals generated by cells has attracted considerable interest basically since it was technically possible. However, it took significantly longer until the evaluation of cellular impedance as a useful signal entered the scientific stage.

The first studies of cell impedance were done using standard laboratory instruments connected to microelectrodes in various designs. Giaever and Keese [16, 31] initially fabricated their electrodes by evaporating gold onto a polystyrene culture dish. The electrode geometry consisted of four small measurement electrodes, only one of which was active at a time, and one much larger counter electrode, so that the measured impedance was dominated by the electrolytic interface at the small electrode. The measurement was performed using an external lock-in amplifier set to 4 kHz. In order to limit the current, a series resistance of 1 MΩ was added to the circuit, approximating a constant current source. The recorded impedance data were initially interpreted on the basis of their in-phase and out-of-phase components, and also as equivalent series resistance and capacitance. In later versions of their system [29], the impedance could be measured at several discrete frequencies, and the electrode fabrication was modified to use a polycarbonate substrate with the electrodes fabricated by photolithographically structuring a thin sputtered gold film. In order to better interpret the measurement data, an analytical model of the impedance presented by a cellular monolayer was developed [17].

Ehret et al. [25] chose a similar approach instrumentation-wise and used an LCR meter with a series resistance to measure the cellular impedance. They initially used platinum electrodes evaporated onto a sapphire (Al_2O_3) substrate. In later publications [32, 33] of the group, silicon and also glass were used as substrates and palladium as electrode material. Their electrode design differs fundamentally from that of Giaever and Keese: It is an interdigitated electrode structure (IDES), which consists of interleaved electrode

fingers alternating between the two measurement electrodes. The electrode layout is thus reminiscent of two interlocking combs. The finger width and spacing were both 50 µm. In this geometry, the series resistance between the electrodes is minimized. The total measured impedance is therefore expected to be dominated by the interfacial capacitance, with cells covering the electrode effectively reducing the electrode area and thus decreasing the impedance. The relatively large area covered by the electrode structure (initially $5 \times 5\,\mathrm{mm}^2$) means that the collective behavior of a large number of cells is recorded (as opposed to that of few cells for smaller sensing electrodes). After performing exploratory impedance spectroscopy, a fixed measurement frequency of 10 kHz was chosen. The measured impedance was represented as equivalent parallel resistance and capacitance, with the latter interpreted as containing most of the information on cell adhesion.

Recently, some research has also been done on the contactless measurement of cell impedance [34, 35]. This is in general accomplished by covering the electrodes, which are normally directly in contact with the cells and the medium, with a passivating coating such as SU-8. The advantage of this approach is that the phenomena at the electrode-electrolyte interface disappear, which eliminates a potentially large source of variation and drift in the measurements. On the other hand, in order to capacitively couple through the passivation, high frequencies are needed, so any interesting effects at lower frequencies are invisible.

2.3.2 Commercially Available Systems for Cell Impedance Analysis and their Applications

Some of the activities of the aforementioned groups led to efforts to commercialize cell impedance assays, most often for research purposes. The work of the pioneers of the field, Giaever and Keese, eventually resulted in the products that are today marketed by the company *Applied Biophysics*. Their technique of cell monitoring using impedance was patented and trademarked as ECIS (Electric Cell-substrate Impedance Sensing). As in their later publications [36], the sensing electrode is constituted by a circular opening of 250 µm diameter in the insulating film covering the well bottom, exposing part of a gold surface beneath. The counter electrode is significantly larger. Each cell culture well has only one such sensing electrode, and up to 96 wells in a microtiter plate can be measured with one device. Data are interpreted in terms of the parameters of the analytical model developed by Giaever and Keese [17], which will be explained in detail in the next chapter. The system has been used for numerous applications [37], ranging from the evaluation of

cell attachment on various surfaces to cancer research and toxicology studies.

Similar fields of research are given as applications for the RT-CES (Real-Time Cell Electronic Sensing) system by *ACEA Biosciences, Inc.* [38], which is now marketed under the name xCELLigence by *Roche Applied Science*. Again, cells are cultured in multiwell plates, and each well has microelectrodes at the bottom. The electrode geometry is reminiscent of the IDES used by Ehret et al., with some modifications. The impedance date are interpreted by calculating a "cell index", which is the maximum of the relative impedance change at the three measurement frequencies 10, 25, and 50 kHz [39].

The CellKey system [40, 41] by *Molecular Devices, Inc.* is another benchtop device that is also tailored to research applications, especially drug screening assays [42]. It comes in versions for 96- and 384-well microtiter plates for parallel testing of many candidate substances. The impedance is measured at several frequencies and segmented into extra-cellular and trans-cellular contributions, corresponding to its low and high frequency components, respectively.

The system for cell-based assays marketed by *Bionas GmbH* differs from those described up to now in that it monitors other parameters of the cell culture besides impedance [12, 43]. It traces back to the activities of the group of Ehret et al. [33] and also incorporates sensors for acidity and oxygen concentration, which give information on the metabolic activity of the cells. This provides a more comprehensive view of the state of the cells. The impedance is however only measured at a fixed frequency of 10 kHz. Apart from a six-channel system for this multi-parameter sensor chip, another system for measuring 96 wells in parallel, featuring only impedance sensors, was recently introduced [44].

2.3.3 Advancing the State of the Art: Towards Robust and Portable Cell-based Sensors Using CMOS Integrated Electronics

The systems described up to now are all intended only for a controlled laboratory environment, not least because of their dependence on large bench-top measurement instruments. The research goal in their development was initially to explore whether impedance is a useful parameter to monitor the state and behavior of cells in culture. After first results showed that this is indeed the case, the research focused on a better understanding of the mechanics of cell adhesion from a microbiological point of view, and on practical applications of cell impedance assays, such as the screening of drug candi-

dates. This is evidenced by the trend towards increasing parallelization of the measurements, allowing a higher throughput of substances to be tested.

Some work has also been done on the development of portable stand-alone systems for cellular monitoring. The motivation behind this was mainly to harness cellular assays for environmental monitoring [45]. For such a portable system, robustness and small dimensions are key requirements. Both can be achieved to an extent by careful and intelligent design of the fluidic, power, and readout electronics systems. However an inherent limitation to the miniaturization of the electronics, and also to the attainable robustness of the signal connections against noise and interference, can only be overcome by integrating signal amplification and conversion circuitry in close proximity to the transducers on the sensor substrate. For some types of cell-based biosensors, such an integration using CMOS technology has been implemented, e.g. for the monitoring of cellular action potentials [30, 46] and for the optical readout of so-called bioluminescent bioreporters [47, 48]. A capacitive detection scheme for the localization of bioparticles (including cells) on a CMOS sensor chip has also been presented [49], however the method requires a conductive glass slide at a defined distance above the chip surface (approx. 100 µm) to which a voltage step has to be applied.

The integration of cell impedance measurement functionality directly on the sensor chip without external components brings advantages beyond those mentioned above. As multiplexing the signals from an entire array of electrodes is easily possible using integrated circuits, the sensor can feature a large number of sensing sites that can be read out individually. This allows localized measurements of the morphology and micromotion of clusters of few cells, which also give valuable information not contained in the averaged impedance response of the whole cell layer [14, 17]. As the electrodes at the individual impedance measurement sites can be relatively small, they can capture the behavior of only few or even single cells, including their microscopic movements. These can be interpreted as an indicator of the cells' vitality [14]. Large electrodes on the other hand can only give information on the state of the cell culture as a whole, because the individual movements of the cells are averaged out over the electrode area. With an integrated impedance sensor, this can also be achieved by aggregating the signals of the whole array of sensing electrodes.

Localized measurements of cell coverage are also very interesting e.g. for monitoring wound healing processes. Another advantage is that on a multiparameter cell sensor, knowledge of the state of the cell layer at the location of transducers for other parameters, such as luminescence or acidification, could be used to enhance and validate their signals. For example, the signal from

a luminescence sensor that has no cells above it can be regarded as of little validity and containing mostly background noise, whereas a measurement location that is completely covered by cells is expected to give signals of high quality.

3 Modeling the Impedance of Cellular Monolayers

Having a solid understanding of the phenomenon under study is a crucial prerequisite to measuring it in a meaningful way. Modeling is a way to formalize this understanding. A good model takes into account all the significant factors which might influence the interaction of sensor and target. At the same time it has to be abstract enough to allow the establishment of a relationship between parameters and their effects, and thus predictions to be made. The measurement of cellular impedance is no exception to this rule.

This chapter will explore two fundamentally different approaches to modeling the impedance of cellular monolayers. The first is the analytical approach of constructing differential equations in order to describe the electrical behavior of the cell layer, then solving them. The "bottom-up" character of this method ensures that all aspects of the model and how they interact are understood. However, in order to keep the resulting equations analytically tractable, often simplifying assumptions have to be made, and the geometry must be kept very simple. The second approach is to use numerical methods and to try to understand the cellular impedance from their results. Thanks to the capabilities of modern computers, this has the advantage of being nearly unlimited in terms of the geometry under study and the amount of incorporated detail. The disadvantage is that due to this high level of detail, many factors may influence the end result, and it requires a very systematic approach and a large number of simulations to separate the important from the unimportant parameters. A combination of both methods is also possible, such as inferring the main factors that influence the result from numerical simulations, and then establishing analytical equations to describe the system, taking into account only these factors.

In any case, first the fundamental geometry of the model must be established, i.e.:

- Where are the electrodes located and what do they look like?
- Where are the cells in relation to the electrodes and how are they modeled?
- Are there any symmetries inherent to the geometry that can be exploited?

These are some of the factors that determine how the model can be solved. In this chapter, only two-electrode measurements will be considered, as opposed to a four-electrode "Kelvin-type" measurement, and only these two electrodes will be assumed to influence the field lines. Any other electrodes on the chip must thus be inactive (in a high-impedance state) and far enough away. Another crucial design decision is then whether to make the two measurement electrodes the same size. If they are identical, there is an inherent symmetry and the model only needs to cover one half of the space between the electrodes. Setting the potential of one electrode to zero, then at the symmetry plane the voltage will be half of the voltage V_{el} of the other electrode (plus an offset due to the electrode potential). Another justified approximation in that case, given additionally that the volume of the medium is large compared to the electrode dimensions and assuming perfect electrical insulation against the surroundings, is then that the potential V_m of the bulk electrolyte far away from the electrodes also goes toward the voltage of the symmetry plane.

If however one electrode is much larger than the other, then the polarization impedance and the spreading resistance of the large electrode can be neglected. The potential of the bulk electrolyte V_m can then be considered fixed and determined only by the voltage of the large electrode. Since the large electrode acts as a source respectively sink for any excess charge, it will be referred to as counter electrode, and its voltage as $V_{counterEl}$. Due to the equilibrium potential of the electrode, V_m is however not identical to $V_{counterEl}$. An advantage of such a design is that the background impedance is reduced and the relative change caused by cell adhesion on the small electrode can thus be detected more easily [17].

Depending on the shape of the electrodes, some other simplifications can be made by exploiting symmetries. Very elongated electrode strips, such as those in the IDES used by Ehret et al. [25], essentially represent a one-dimensional geometry. This is also true for geometries with axial symmetry, such as circular electrodes.

After an initial settling and proliferation phase, the cells will be assumed to form a confluent monolayer, which means they are spread out across the entire surface of the chip in such a way that no point has more than one cell above it, but each cell is in direct contact with its neighbors. Many kinds of cells naturally form such monolayers, because they spontaneously stop dividing when they are in contact with their neighbors. Monolayer-forming cells are thus ideally suited for culturing on a cell-based sensor, since no special measures have to be taken to prevent them from completely overgrowing the chip. This simplification is therefore well justified for a cell culture in a steady state. How tight the monolayer is, i.e. whether the cells form tight junctions

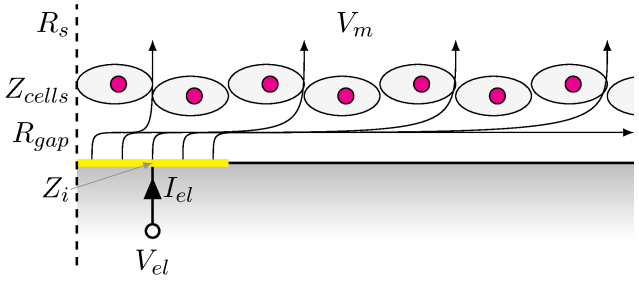

Figure 3.1: Schematic cross section of a cell monolayer growing on the sensor.

with their neighbors or there are gaps between them, can be modeled by the permeability of the layer to current.

Another assumption, which all the models discussed in the following share, is that the presence of the cells does not significantly alter the impedance of the electrode-electrolyte interface. The rationale behind the assumption is that a gap larger than a few nanometers and filled with electrolyte exists beneath the cells, due to the molecules of the extracellular matrix the cells use to adhere to the substrate [29, 50].

A general cross-section view of one electrode and the cell layer above it, independent of the particular electrode shape, is depicted in Figure 3.1. However, an axial or mirror symmetry around the electrode center, indicated by the dashed line at the left, is assumed. A current I_{el} is injected into the sensing electrode with an interfacial impedance Z_i on the left and spreads in the space under the cells and through the cell layer into the bulk medium, which is assumed to be at a potential V_m. The electrical behavior of the cell layer is modeled by Z_{cells}, and the constriction of the current flow in the space under the cells creates a resistance R_{gap}. In the following analytical models, this gap resistance is however not treated separately, and the combined effect of the elements Z_i, R_{gap}, and Z_{cells} in Figure 3.1 is designated by the symbol Z_{cov}.

3.1 Analytical Models

In this section, the purely analytical approach to modeling the cellular impedance will be evaluated by discussing two published models. The first is the model developed by Giaever and Keese [17], which is tailored to the electrode layout that they used in their experiments. As the sensing electrode with an area of about $10^{-3}\,\mathrm{cm}^2$ was very large in relation to the size of a single cell, it was approximated as infinite. The model therefore assumes that the cell layer is composed of identical "unit cells", which are circular disks of radius r_c at a constant height h above the sensing electrode, as shown in

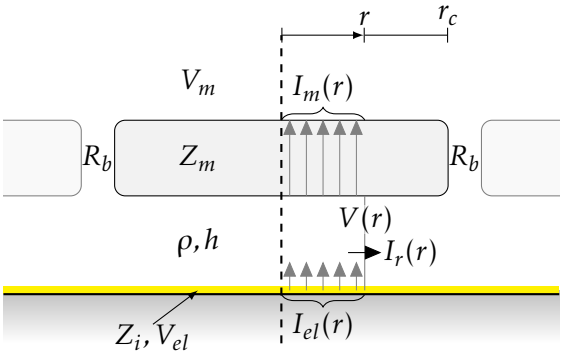

Figure 3.2: Visualization of a unit cell in the Giaever and Keese model. (Currents only indicated for one side)

Figure 3.2. The sensing electrode has a constant potential V_{el}. The counter electrode is not an explicit part of the model, but the electrolyte above the cell monolayer is assumed to have some fixed potential V_m.

The current, once injected through the electrode, can take two paths into the bulk electrolyte: The first is through the cell, crossing the bottom and top membranes, which together represent an impedance[1] Z_m. At the edge of the cell, a resistance R_b represents the second path through intercellular spaces. According to the authors, the fact that the unit cell is not space-filling does not limit the validity of the model as long as the actual shape of the cells does not deviate too much from a circular horizontal section. The model was later adapted to other cell shapes [51] and to include an additional current path through the lateral membrane [29]. Only the derivation of the original model will be dealt with in this section.

The model is constructed in a polar coordinate system around the center of the unit cell, with no dependence of any value on the angular coordinate or the height, reducing the problem to a single dimension, the radial coordinate r. By applying symmetry boundary conditions, the impedance of the whole system can then be derived from the analysis of one unit cell. Referring to Figure 3.2, $I_{el}(r)$ is defined as the current flowing from the electrode within the area defined by the circle of radius r. Analogously, $I_m(r)$ is the current flowing through the cell into the bulk electrolyte within that area. $I_r(r)$ is the current flowing in radial direction through the sidewall of an imagined cylinder of radius r and height h, so that for any r satisfying $0 \leq r < r_c$, the equation $I_r(r) = I_{el}(r) - I_m(r)$ holds. The basic equations describing the Giaever

[1] In their paper, Giaever and Keese assumed this impedance to be purely capacitive, i.e. $Z_m = \left(i\omega \frac{C_m}{2}\right)^{-1}$.

and Keese model are then as follows:

$$-\frac{\mathrm{d}V(r)}{\mathrm{d}r} = \frac{I_r(r)\rho}{2\pi r h} \tag{3.1}$$

$$\frac{\mathrm{d}I_r(r)}{\mathrm{d}r} = \frac{\mathrm{d}I_{el}(r)}{\mathrm{d}r} - \frac{\mathrm{d}I_m(r)}{\mathrm{d}r} \tag{3.2}$$

$$\frac{\mathrm{d}I_{el}(r)}{\mathrm{d}r} = \frac{2\pi r}{Z_i}(V_{el} - V(r)) \tag{3.3}$$

$$\frac{\mathrm{d}I_m(r)}{\mathrm{d}r} = \frac{2\pi r}{Z_i}(V(r) - V_m) \tag{3.4}$$

By differentiation of Equation (3.1), followed by substitution of Equation (3.2) and after that Equations (3.3) and (3.4) into the result, one arrives at the following ordinary differential equation of second order:

$$\frac{\mathrm{d}^2V(r)}{\mathrm{d}r^2} + \frac{1}{r}\frac{\mathrm{d}V(r)}{\mathrm{d}r} - \gamma^2 V(r) + \beta = 0 \tag{3.5}$$

$$\text{where } \gamma^2 = \frac{\rho}{h}\left(\frac{1}{Z_i} + \frac{1}{Z_m}\right) \tag{3.6}$$

$$\text{and } \beta = \frac{\rho}{h}\left(\frac{V_{el}}{Z_i} + \frac{V_m}{Z_m}\right) \tag{3.7}$$

It has the general solution

$$V(r) = C_1\mathcal{I}_0(\gamma r) + C_2\mathcal{K}_0(\gamma r) + \frac{\beta}{\gamma^2} \tag{3.8}$$

where $\mathcal{I}_0$ and $\mathcal{K}_0$ are the modified Bessel function of the first respectively second kind, of zero order. Because $\mathcal{K}_0(\gamma r)$ goes towards infinity for $r \to 0$, C_2 must be zero. The constant C_1 must be deduced by applying suitable boundary conditions, although these are not given in the original paper [17]. The final expression for the specific impedance of the cell-covered electrode is then

$$\frac{1}{Z_{cov}} = \frac{1}{Z_i}\left[\frac{Z_i}{Z_i + Z_m} + \frac{\dfrac{Z_m}{Z_i + Z_m}}{\dfrac{\gamma r_c}{2}\dfrac{\mathcal{I}_0(\gamma r_c)}{\mathcal{I}_1(\gamma r_c)} + R_b\left(\dfrac{1}{Z_i} + \dfrac{1}{Z_m}\right)}\right] \tag{3.9}$$

If Z_i is measured and a suitable value chosen for Z_m, two degrees of freedom remain: the intercellular resistance R_b, and the term $r_c\sqrt{\frac{\rho}{h}}$ from

$$\gamma r_c = r_c\sqrt{\frac{\rho}{h}\left(\frac{1}{Z_i} + \frac{1}{Z_m}\right)}$$

Their values can be determined by fitting measured impedance spectra to this model, and thus properties of the cell layer can be inferred.

An obvious limitation of the above model is the assumption of an infinitely large electrode, which is often not applicable. This deficiency is addressed in the model published by Urdapilleta et al. [50]. It shares the general assumptions with the model discussed above, but has some modifications which make it especially suited for electrode dimensions on the scale of few cells, as they are likely to be found on a multi-electrode array. This is achieved by segmenting the model space into two regions: within the electrode area ($r < r_e$), and outside the electrode ($r > r_e$), with the origin of the polar coordinate system on the electrode center. This is essentially the geometry described by Figure 3.1, with the electrode assumed to be circular. Since the positions of the individual cells are unknown in this model, the current path through intercellular spaces can no longer be considered separately from the current through the cell itself. The distributed impedance of the cell layer Z_{cells} thus takes the place of Z_m in the Giaever and Keese model. Z_{cells} is modeled as a capacitance C_{cells}, representing the effect of the cell membranes, in parallel with a resistance R_{cells}, which mostly represents current paths through gaps between the cells.

The differential equations describing the model for the two regions, and their respective general solutions, however are basically identical and will thus not be repeated here. The sole difference is that outside the electrode area the contribution of the electrode current vanishes. With a boundary condition of $V(r \to \infty) = V_m$, and continuity boundary conditions for voltage and current at the transition point between the two regions, the final expression for the specific impedance of the cell-covered electrode can be given as [50]

$$\frac{1}{Z_{cov}} = \frac{1}{Z_i}\left\{\frac{Z_i}{Z_i + Z_{cells}} + \frac{\dfrac{Z_{cells}}{Z_i + Z_{cells}}}{\dfrac{\gamma_{in} r_e}{2}\left[\dfrac{\mathcal{I}_0(\gamma_{in} r_e)}{\mathcal{I}_1(\gamma_{in} r_e)} + \dfrac{\gamma_{in}}{\gamma_{out}}\dfrac{\mathcal{K}_0(\gamma_{out} r_e)}{\mathcal{K}_1(\gamma_{out} r_e)}\right]}\right\} \tag{3.10}$$

with γ_{in} and β_{in} defined analogous to Equations (3.6) respectively (3.7), and

$$\gamma_{out} = \sqrt{\frac{\rho}{h}\frac{1}{Z_{cells}}} \tag{3.11}$$

$$\beta_{out} = \frac{\rho}{h}\frac{V_m}{Z_{cells}} \tag{3.12}$$

In order to validate this model, Urdapilleta et al. also performed cell impedance measurements, and compared the best fit of their model to the

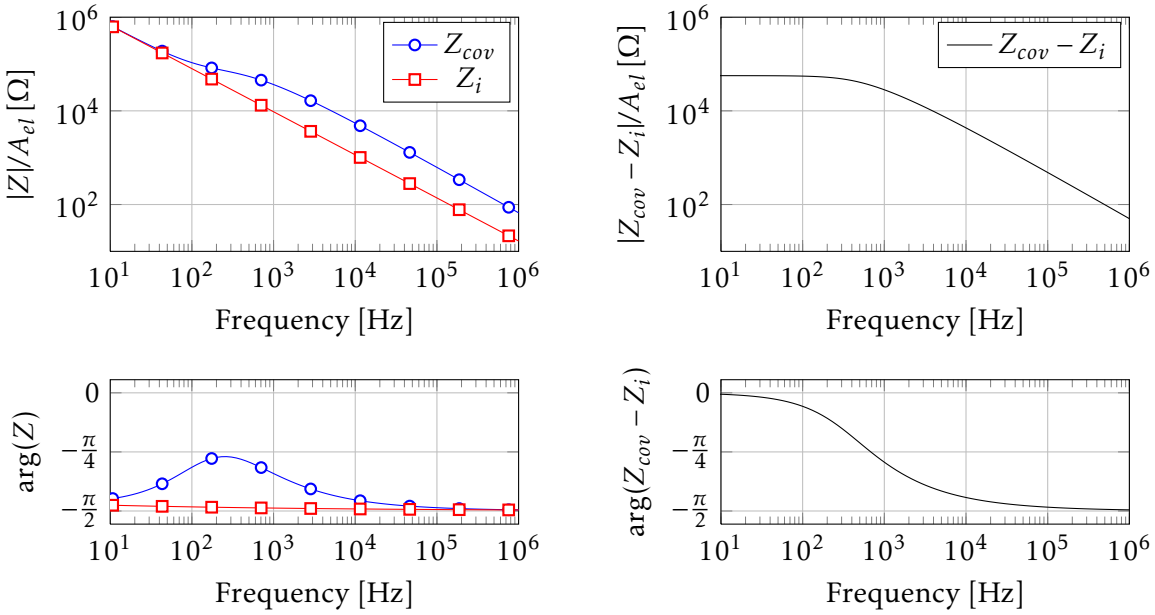

Figure 3.3: Left: Bode plot of the impedances of a naked electrode, Z_i, and of a cell covered electrode, Z_{cov}, using the model and parameters of Urdapilleta et al. [50] for the cell response and the parameters from Table 2.1 for the electrode response. Right: Bode plot of $Z_{cov} - Z_i$, showing just the net contribution of the cells.

measured data with fits obtained using the model by Giaever and Keese [17] and a simple two-parameter model approximating the cell layer as a parallel RC element. Equation (3.10) was shown to yield the best fit to an impedance spectrum of a cell-covered electrode, but reasonable fits could be achieved with all three models. However, the extracted value for the height h of the cell-substrate gap was unrealistically low with the Giaever and Keese model, and unrealistically high with the Urdapilleta et al. model, calling into question their usefulness to extract geometric parameters from impedance data. The extracted values of h should therefore only be considered as limits, not true values. It is however still possible to estimate the influence of the different parameters, which gives a starting point for numerical simulations and makes this model useful for the design of a cell impedance sensor.

The left plots in Figure 3.3 show the magnitude and phase of Z_{cov} versus frequency when the extracted parameter values[2] reported by Urdapilleta et al. are plugged into Equation (3.10). At low frequencies, the interfacial

[2] They are $h = 1.0\,\mu m$, $R_{cells} = 301\,\Omega\,cm^2$, $C_{cells} = 1.6\,\mu F\,cm^{-1}$. The electrode radius r_e is 250 µm, corresponding to an electrode area A_{el} of approximately $2 \cdot 10^{-3}\,cm^2$. For the electrode impedance Z_i, the values in Table 2.1 were used, and the electrolyte resistivity ρ was set to $65\,\Omega\,cm$.

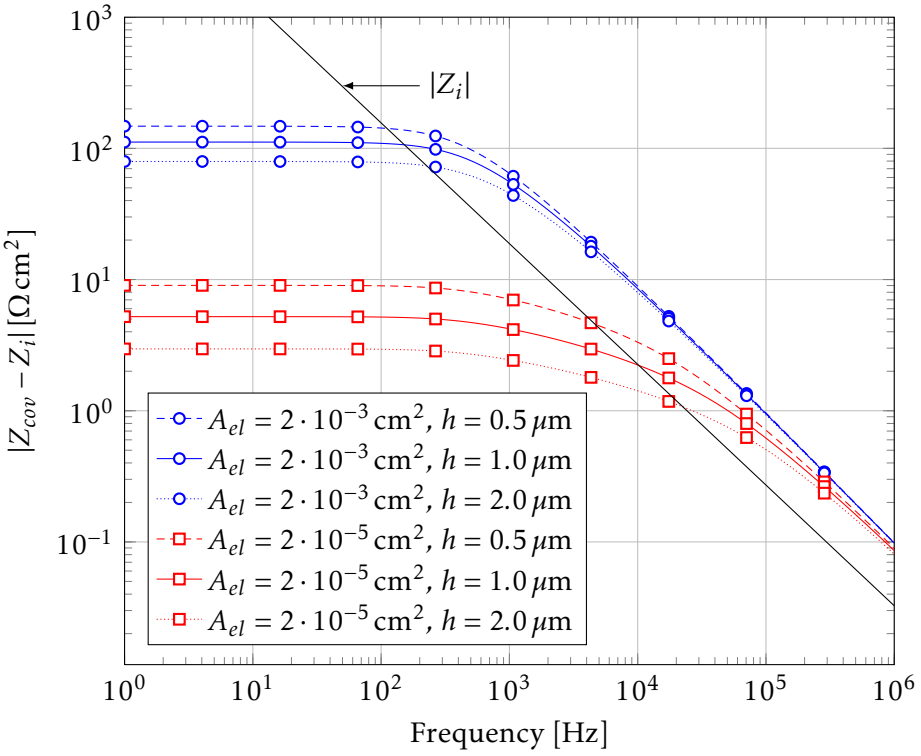

Figure 3.4: Magnitude plots of the specific impedance generated by the cell cover according to the model of Urdapilleta et al., with variation of the electrode area A_{el} and the gap height parameter h. The black line represents the magnitude of the specific interfacial impedance, $|Z_i|$.

impedance Z_i is dominant so that the effect of the cells only becomes apparent at higher frequencies. When Z_i is subtracted, as in the plots on the right in Figure 3.3, the net contribution of the cells becomes visible.[3] The cell impedance in this model seems to approximate single-pole behavior.

In Figure 3.4, the specific area impedance generated by the cell cover is shown for different values of the electrode size A_{el} and cell-substrate gap height h. As can be seen, the corner frequency increases with decreasing electrode size, while the specific impedance decreases. The gap height in contrast seems to influence only the plateau, however its relative effect is more pronounced for the smaller electrode area. An intuitive explanation for this is that for small electrodes, the current mostly spreads out in the cell-substrate gap, while for large electrodes, more current flows directly through the cell layer above the electrode. In fact, for $r_e \to \infty$, Equation (3.10)

[3] Note that this is not the same as simply setting $Z_i = 0$ in the derivation of Equation 3.10, because in that case the voltage in the gap above the electrode would be constant, resulting in zero current in the radial direction.

simplifies into $Z_i + Z_{cells}$, and the influence of the cell-substrate gap completely disappears, while for $r_e \to 0$ it simplifies into Z_i, meaning that the high electrode impedance drowns out the effect of the cell coverage.

As a conservative design limit, it can be assumed that the impedance generated by the cell layer should be larger than the background impedance of the electrochemical interface. In Figure 3.4, this corresponds to the region where the curves are above the line representing $|Z_i|$. The cellular impedance therefore can be detected optimally only in a certain frequency window. At low frequencies, the total impedance is dominated by the interfacial impedance Z_i. At higher frequencies, Z_i has decreased sufficiently, but due to capacitive coupling through the cells, the useful signal also starts to vanish and is soon eclipsed by the spreading resistance.

An interesting question is whether there is an optimal electrode size which maximizes the sensitivity to variations in the cell-substrate gap height h while also retaining sensitivity to variations in R_{cells}, i.e. the tightness of the intercellular pathways. Plotting the low-frequency magnitude of $Z_{cov} - Z_i$ versus electrode area A_{el} and gap height h (Figure 3.5) respectively cell layer resistance R_{cells} (Figure 3.6) reveals that the sensitivity to changes in h is highest for electrode sizes of around $10^{-3}\,\mathrm{cm}^2$, although the relative change is more pronounced for small electrodes. As expected, the sensitivity to changes in R_{cells} increases with larger electrodes.

However, electrodes of $10^{-3}\,\mathrm{cm}^2$ or larger are not really suited for application in an electrode array on a multi-parameter CMOS cell sensor. Their diameter of several hundreds of micrometers, plus appropriate spacing needed to ensure that neighboring electrodes do not influence each other, would mean that only few electrodes could be placed on the chip due to the need to keep the total area and thus processing costs within reason. Additionally, the area used for the impedance electrodes is lost for other sensors that might be integrated on the same chip, such as photodiodes for bioluminescence detection. As outlined in Section 2.3.3, smaller electrodes registering only few cells also have the advantage of capturing impedance changes caused by cellular micromotion, which would be averaged out and thus less pronounced when using large electrodes.

3.2 Numerical Approach to Predicting Cellular Impedance

A common limitation of the analytical models discussed in Section 3.1 is that they represent only very simple geometries. Despite this simplification,

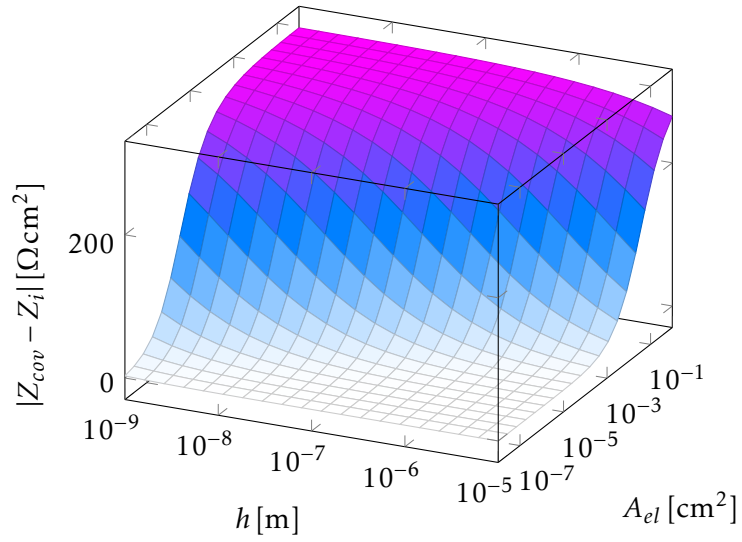

Figure 3.5: Magnitude of Z_{cov} (3.10) at low frequencies (1 Hz) with the interfacial impedance Z_i subtracted, as a function of the electrode area A_{el} and gap height h. ($R_{cells} = 301\,\Omega\,\mathrm{cm}^2$)

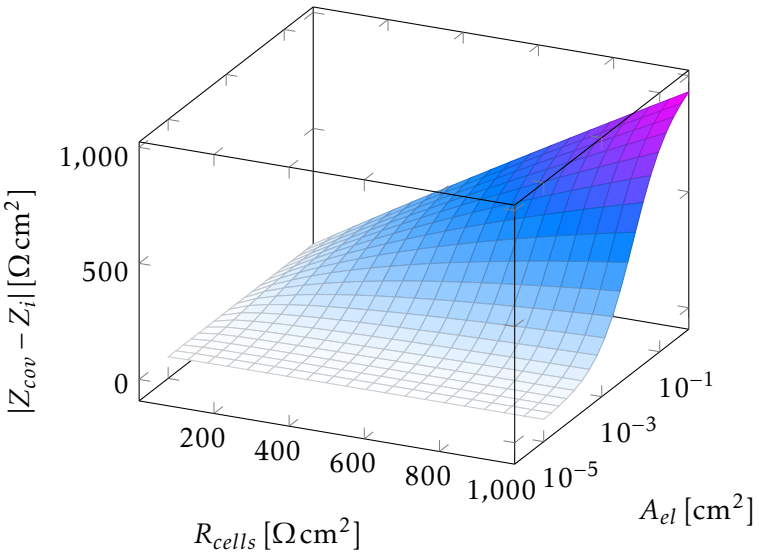

Figure 3.6: Magnitude of Z_{cov} (3.10) at low frequencies (1 Hz) with variation of the electrode area A_{el} and cell layer resistance R_{cells}. ($h = 1\,\mu\mathrm{m}$)

their final expressions are by no means straightforward to develop and do not lend themselves to intuitive interpretation. They also do not take into account the counter electrode, assuming it to be infinitely far away, which may not be valid for an array of microelectrodes on a chip. For geometries that cannot be described one-dimensionally, there may be no analytical solution at all. Therefore, numerical simulations based on the finite element method (FEM) were also performed, which offer more flexibility to explore various geometries. From their results, more straightforward analytical models of the cell impedance were then developed. Despite some naive assumptions, these were able to reproduce the simulation results with sufficient accuracy to serve as the basis for the optimization of the electrode layout.

Since it is the resistive part of the cellular impedance that represents the useful signal for a cellular adhesion sensor, it should be maximized by prudent design decisions in order to obtain a good sensitivity. The FEM analyses were thus mainly performed as static (DC) simulations. For the reasons mentioned in Section 2.3.3, the integrated cell adhesion sensor should feature an entire array of sensing electrodes, preferably arranged in a grid. A key aim of the FEM simulations was thus to determine a sensible size and spacing of these electrodes. The placement of the counter electrode was another point to be explored.

3.2.1 Linear Gap Model

From an intuitive understanding of the flow of current in the presence of a cell monolayer, it seems that at any point the current in the cell-substrate space can take two paths: as illustrated in Figure 3.1, it can either continue to spread in the gap, or find a way through the cell layer into the bulk electrolyte. Which one of these paths dominates is determined by the cell layer impedance and local gap resistance. The gap resistance again depends on the cross sectional area available to the current, and is therefore determined by the geometry and distance d of the source and sink electrodes, and the gap height h. Therefore, these were the main parameters which were varied in several series of simulations in order to explore their effects. The material properties for the simulations were identical to those used in the calculation of the impedance with the Urdapilleta et al. model above. Unlike the analytical model, the FEM simulator allows for a dependence of the potential and current density in the gap on the vertical coordinate. The practical consequence of this is that it is possible to model the electrode as an equipotential region while still having a non-constant potential in the gap above it, and the electrode polarization impedance can therefore be separated from the FEM model.

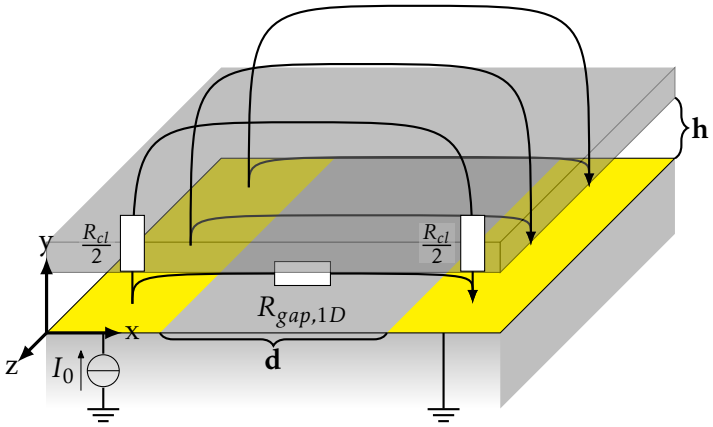

Figure 3.7: Linear gap model with implicit infinite extent in the **z** direction. The resistance of the medium above the cell layer is negligible.

Consider an electrode geometry consisting of two infinitely long parallel electrodes, as illustrated in Figure 3.7. Restricting the problem to a two-dimensional geometry, i.e. a cross section along the **xy** plane with an infinite extent in the **z** direction, enables insights into the determinants of the constriction resistance. Using *ANSYS* R12 FEM software, simulations of such an electrode pair were performed for various values of the gap height h and electrode distance d, with a constant electrode width of 10 µm. Figure 3.8 shows the total resistance between the electrodes obtained in these simulations. Intuitively, the gap resistance in such a geometry should scale approximately linearly with the inter-electrode distance and inversely with the cell-substrate gap height:

$$R_{gap,1D} = F_{geom}\,\rho\,\frac{d}{h} \tag{3.13}$$

with F_{geom} being a geometry-dependent parameter. Some of the current also crosses the cell layer into the bulk electrolyte. Since the electrodes present equipotential regions and the voltage difference across the cell layer is highest in their vicinity, this will primarily happen above or close to the electrodes. This effect can therefore be modeled by a lumped resistance R_{cl} in parallel with the gap resistance. The spreading resistance in the electrolyte above the cells in this path is negligible and fairly independent of d due to the large volume of the bulk medium. The expression for the total resistance (in [Ω m]) between the electrodes in this model is thus

$$R_{total,1D} = R_{gap,1D} \| R_{cl} = \frac{R_{gap,1D} \cdot R_{cl}}{R_{gap,1D} + R_{cl}} \tag{3.14}$$

This equation was fitted to the simulated data separately for each value of h with good results, as shown in Figure 3.8.

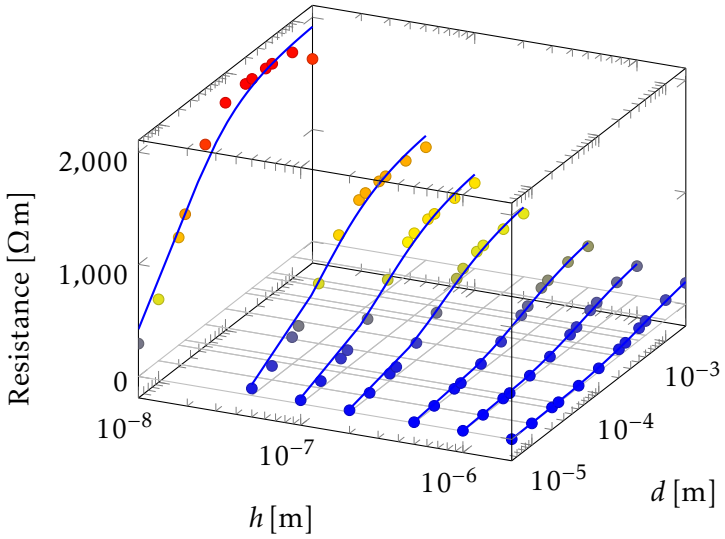

Figure 3.8: FEM simulation results for variation of the gap height h and electrode distance d in a linear gap model as illustrated in Figure 3.7 (circle symbols). The light gray grid represents the spreading resistance without cells, and the solid lines least squares fits of equation (3.14) for each value of h.

3.2.2 Extension of the Linear Gap Model to 3D Geometries

The layout of the sensing electrodes array on the chip should fulfill two basic requirements:

1. The available area should be used optimally, so that there is as little "dead" space as possible.
2. The array cells should be identical and their characteristics independent of their surroundings.

A straightforward layout meeting these requirements is depicted in Figure 3.9. Here, the counter electrode forms a grid between the sensing electrodes, insulating them from each other and creating identical grid cells. The sensing electrodes in the center are square with an area of $A_{el} = a^2$, and the counter electrode is at a distance d to each side. Due to this property and the symmetry of the array cell itself, it is sufficient to simulate only part of one cell, as illustrated by the shaded area in the figure.

A visualization of the simulated potential distribution in the cell-substrate gap with this layout, as shown in Figure 3.10, reveals that the equipotential lines are almost parallel near the electrodes. In the intermediate region, they are more rounded and resemble segments of a circle. For $d \gg a$, the latter behavior would predominate, and from the familiar $R = \rho\frac{l}{A}$ the gap resistance

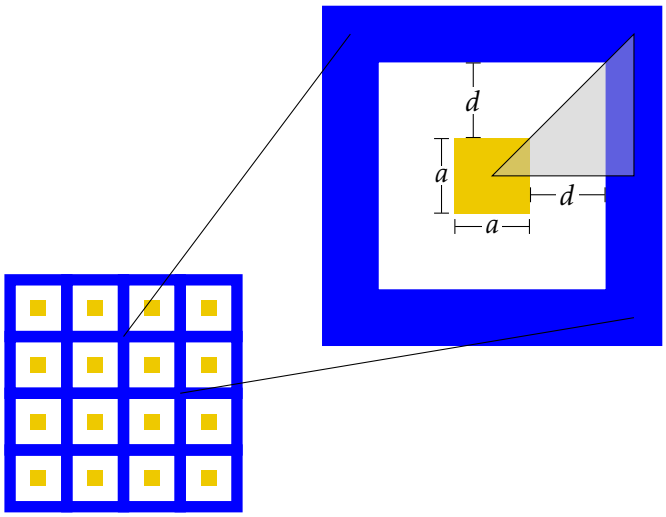

Figure 3.9: Layout of electrodes in an array with an in-grid counter electrode. The sensing electrodes are shown in gold, and the counter electrode in blue. One array element is shown magnified on the right. Due to the inherent symmetries of the layout, only the shaded area needs to be simulated in the FEM model.

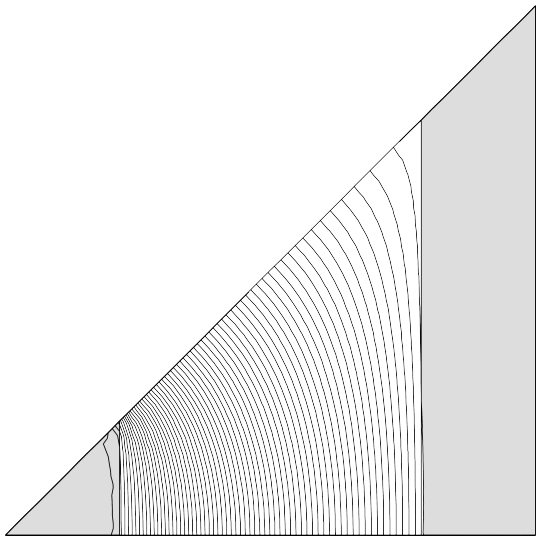

Figure 3.10: Typical potential distribution in the gap underneath the cells, illustrated as equipotential lines obtained from FEM simulations of the geometry shown in Figure 3.9. ($a = 55\,\mu m$, $d = 72.5\,\mu m$)

could be calculated as

$$R_{gap,rad} = \int_0^d \frac{\rho}{2\pi h(r_e + r)} \mathrm{d}r = \frac{\rho}{2\pi h} \ln\left(\frac{r_e + d}{r_e}\right)$$

Setting the radius r_e of the inner electrode to the area equivalent $r_e = \sqrt{\frac{a^2}{\pi}}$, this equation can be rewritten as

$$R_{gap,rad} = \frac{\rho}{2\pi h} \ln\left(\frac{a + d\sqrt{\pi}}{a}\right) \tag{3.15}$$

If however the distance between the electrodes is on the same order of magnitude as the dimensions of the inner electrode, a different approximation may give better results. If the equipotential lines on each of the four sides of the electrode were completely parallel, the gap resistance would be

$$R_{gap,sq} = \int_0^d \frac{\rho}{4h(a + 2x)} \mathrm{d}x = \frac{\rho}{8h} \ln\left(\frac{a + 2d}{a}\right) \tag{3.16}$$

As with the one-dimensional gap model, Equations (3.15) and (3.16) were fitted to the simulated data. The fit equation was

$$R_{total,2D} = R_{gap} \| \frac{R'_{cl}}{a^2} + R_s \tag{3.17}$$

Since in these simulations, the electrode area was also varied, the spreading resistance R_s could no longer be neglected or considered constant. It was therefore calculated according to Equation (2.5) for the fit with $R_{gap,rad}$ and according to Equation (2.6) for the fit with $R_{gap,sq}$, respectively. The same applies for the resistance of the path through the cell layer, which was now modeled by scaling an area resistance R'_{cl} with the electrode area a^2. In total, the fit with $R_{gap,sq}$, which is also overlaid in Figure 3.11, produced better results. The fit parameter for the gap resistance R_{sq} was $\rho = 59.3\,\Omega\mathrm{cm}$, and $R'_{cl} = 68.2\ \Omega\mathrm{cm}^2$. The spreading resistance R_s was extracted from simulations without cells with a parameter $\rho_s = 57.7\,\Omega\mathrm{cm}$.

The logarithmic characteristic of Equations (3.15) and (3.16) means that the sensitivity of the total cell layer resistance to the distance to the counter electrode d is highest for low values of d, and diminishes for large distances. However, increasing the distance to the counter electrode always increases the impedance of the cell layer seen by the sensing electrode. If the distance d

required to generate a sufficient impedance of the cell layer is larger than the maximum desired array pitch allows, the electrode layout of Figure 3.9 is no longer feasible and the counter electrode has to be moved outside the array. The requirement of identical array cells is not fulfilled in this case, since the distance to the counter electrode varies, but if it is large enough this should not have a strong effect. Furthermore, if the neighboring sensing electrodes do not significantly affect the measured impedance, e.g. because they are in a high-impedance off state and far enough away, an individual array cell can be modeled alone, and the counter electrode treated as if it were at infinite distance, i.e. $d \to \infty$. For $d \to \infty$, the limit of the total resistance according to Equation (3.17) is $\frac{R'_{cl}}{a^2} + R_s$, with no dependence on the gap height h. This is in disagreement with the Urdapilleta et al. model. In order to better understand the impedance with such a geometry, FEM simulations were performed where the counter electrode was implicitly placed at infinite distance by simulating an infinite extension of the geometry. Figure 3.12 shows the results of these simulations in comparison to the impedance predicted by the Urdapilleta et al. model. For the same parameters, the FEM simulation consistently predicts slightly lower values. A safe assumption can therefore be made in considering the impedance predicted by Equation (3.10) as an upper bound and the results of the FEM simulations as a lower bound of the expected impedance.

3.3 Conclusions from the Models

In the voltage range relevant for cell impedance measurement, the impedance Z_i of the electrode-electrolyte interface is dominated by the polarization impedance Z_p. This polarization impedance was experimentally determined to be mostly capacitive in nature, although a frequency-dependent in-phase term is also present. Nevertheless, in the frequency range below 100 kHz a value of around $10\,\mu F\,cm^{-2}$ can be assumed as a good approximation. The spreading resistance R_s is in series with the polarization impedance, but can usually be neglected at frequencies below 100 kHz.[4] The models of the impedance of cellular monolayers revealed essentially a single-pole behavior, like a parallel RC element would produce it. Below its corner frequency, which depends on the properties of the cells as well as the electrode size, it can be treated as a resistance in series with the polarization impedance. In

[4] This frequency actually depends on the electrode size, but is a reasonable value for microelectrodes. For larger electrodes this cut-off frequency will be lower since per Equations (2.5) and (2.6), R_s only scales with ${A_{el}}^{-0.5}$, while the effective polarization impedance scales with ${A_{el}}^{-1}$.

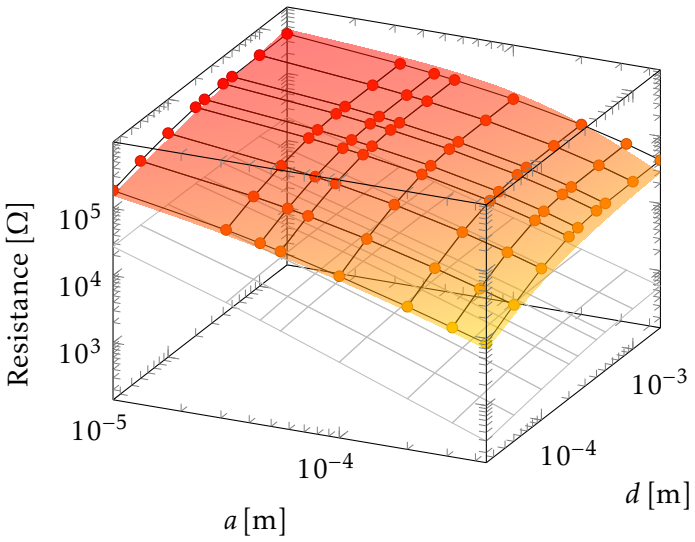

Figure 3.11: FEM simulation results for variation of the sensing electrode edge length a and distance to the counter electrode d with $h = 1\,\mu m$ in a model reproducing the geometry in Figure 3.9 (black grid with circle symbols). The light gray grid represents the spreading resistance without cells, and the colored surface a least squares fit of Equation (3.17).

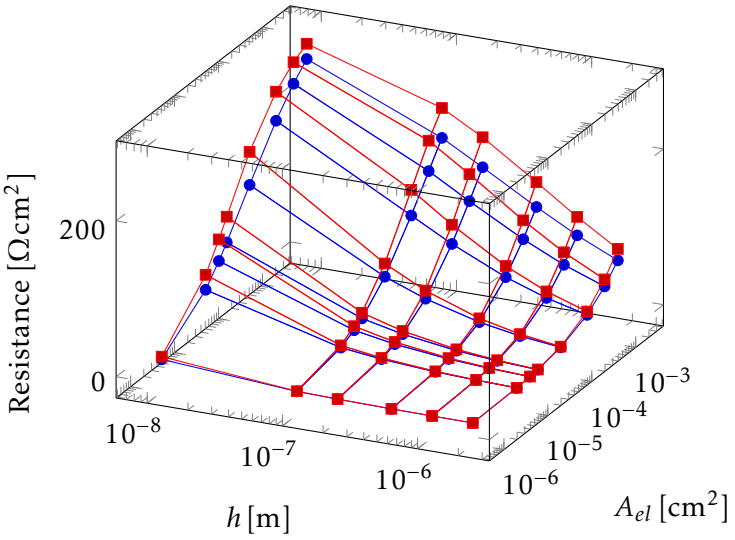

Figure 3.12: Comparison of the results of FEM simulations with the counter electrode at infinite distance (circle symbols) and the impedance predicted by the Urdapilleta et al. model (square symbols).

order to maximize the observed effect of the cells, the measurement should therefore be performed at a frequency not much higher than this corner frequency, but high enough that the polarization impedance is not dominant anymore.

A simplified picture of the impedance seen by a cell adhesion sensor thus emerges: The electrode-electrolyte interface creates a capacitance $C_{el} = A_{el}C_p$. Without cells on the electrode, only the spreading resistance R_s is added to the measured impedance. If cells are however covering the electrode, in the appropriate frequency range a much higher resistance is measured in series with C_{el}. The question is then how to best quantify the amount of cellular adhesion on the basis of this impedance. A true impedance measurement would require determining both magnitude and phase. The complexity associated with this however is only justified if this information brings tangible benefits. This may be the case if the object of the measurement is to gain insight into the internal composition of the cell or certain metabolic pathways, e.g. in research on cellular biology or pharmaceutical drug screening. For applications such as these, the previously described commercially available systems and the analytical models aiming to extract individual geometric or electrical parameters of the cells were developed. A measurement at several frequency points is typically required in order to obtain sufficient data. In the application of cell adhesion measurements, the impedance information is typically not required with separate magnitude and phase components intact. The impedance change due to cell adhesion is mainly resistive and therefore constant across a wide range of frequencies. It is thus possible to quantify the adhesion data by a single number without significant loss of information. This was achieved in this work through an impedance to frequency conversion measurement principle [52–54], which is discussed in detail in the next chapter.

4 Cell Impedance Measurement Based on Impedance-to-Frequency Conversion

For any detection system to function reliably, it must be possible to isolate the effect to be detected from the background signal, or in other words, the signal-to-noise ratio (SNR) should be larger than unity. In the context of cell impedance measurement, this means that the change in impedance caused by cell adhesion $Z_{cov} - Z_i$ should be as large as possible, and ideally larger than the always present impedance Z_i of the electrode-electrolyte interface. Implementation choices and design parameters determine the achievable sensitivity of the measurement, and should therefore be set optimally. For a cell impedance sensor, some design parameters are the frequency range of the measurement, the electrode geometry, and the excitation voltage or current. Fundamental design choices include, but are by far not limited to, the impedance measurement principle and the implementation of internal circuit blocks.

In conventional impedance measurement schemes, the frequency and either voltage or current are held constant, and the other parameter is measured in order to determine the impedance. This means that the excitation always has to be low enough that even in the worst case (low impedance for voltage excitation, high impedance for current excitation) the safe values of current and voltage are not exceeded. Choosing the frequency as the free variable has the advantage that both the voltage and current at the electrode can be kept constant. This not only ensures that the limits of linearity of the electrode-electrolyte interface [19] and the acceptable current density that cells can be exposed to are never exceeded. It also simplifies the circuit design and reduces the problems caused by the noise floor. The impedance to frequency conversion measurement principle makes use of the characteristics of the electrode-electrolyte interface as well as the cell layer impedance. As stated previously, the former can be approximated as a capacitance, while the latter acts as a variable resistance in series with this capacitance. The impedance-to-frequency conversion circuit is essentially an oscillator whose frequency is determined by these external components.

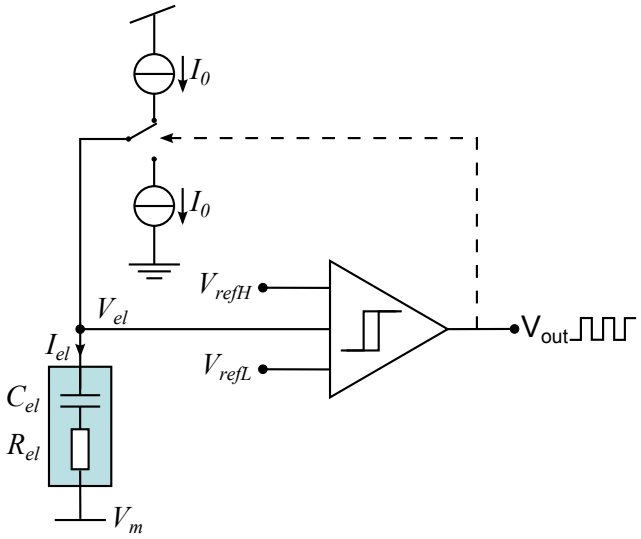

Figure 4.1: Simplified block diagram illustrating of the working principle of the impedance-to-frequency converter.

4.1 Measurement Principle and Basic Circuit Implementation

The measurement principle of the circuit is illustrated by the simplified block diagram in Figure 4.1: A surface electrode in contact with the electrolyte is connected to a comparator and a switchable current source. In the shown switch state, the interface capacitance C_{el} is charged by a constant current $I_{el} = I_0$ while the comparator senses the electrode potential. As soon as the upper reference voltage V_{refH} is reached, the comparator output $\mathsf{V}_{\mathsf{out}}$[1] changes, which in turn triggers the switch so the electrode is now discharged by a current $I_{el} = -I_0$. When V_{el} reaches the lower reference voltage V_{refL}, the comparator switches again, completing the cycle. The series resistance R_{el}, constituted either by the spreading resistance or the cell layer, causes an ohmic voltage drop of $R_{el}I_{el}$ which changes sign at each transition, effectively reducing the voltage window by $2R_{el}I_0$. Neglecting non-ideal effects, the period of one charge-discharge cycle as illustrated in Figure 4.2 is thus given by

$$\tau_{out} = \tau_{out,ideal} = 2C_{el}\left(\frac{\Delta V}{I_0} - 2R_{el}\right) \tag{4.1}$$

with $\Delta V = V_{refH} - V_{refL}$. When cells cover the electrode, increasing R_{el}, the frequency of $\mathsf{V}_{\mathsf{out}}$ also increases. The output of the comparator thus serves

[1] In the following, the names of signals which are considered digital, such as $\mathsf{V}_{\mathsf{out}}$, are printed in a sans serif font.

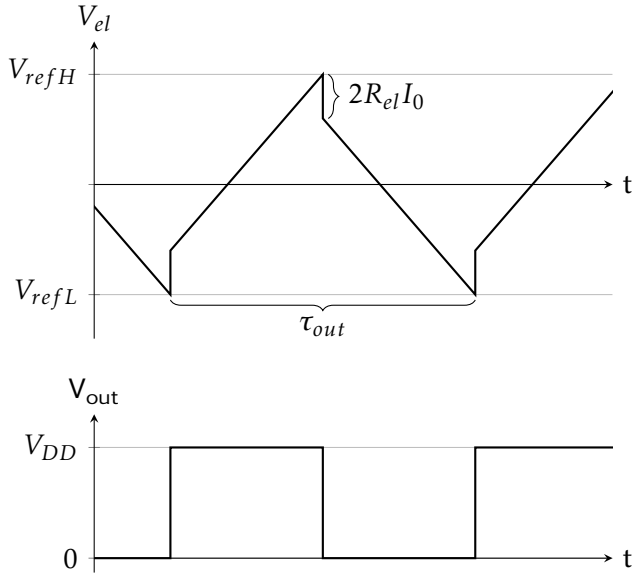

Figure 4.2: Idealized plot of the electrode voltage and digital output over time

as a digital frequency-modulated signal containing information about cell adhesion.

The advantages of this circuit include its robustness and inherent stability. A voltage excitation scheme would require the regulation of the electrode potentials, which is difficult to make unconditionally stable given that the external load impedance may vary over orders of magnitude [55]. A constant current source implemented in CMOS on the other hand usually does not require any dedicated feedback regulation. Since the comparator output is a full swing rectangle signal, a conversion to a digital value is as straightforward as counting the number of cycles in a defined time. The dynamic range, speed and precision of the conversion are adjustable by choosing the number of bits in the counter and the counting time appropriately. The core of the impedance-to-frequency converter is made up of the current sources providing the electrode current, the comparator(s) sensing the electrode potential and comparing it to the two reference voltages, and the associated logic for generating the control signals for the switches.

There are various ways to implement the comparator hysteresis of $\Delta V = V_{refH} - V_{refL}$ [56, sec. 6.5.2]. Relevant boundary conditions for the choice of implementation are the high impedance of the input node and the need for precisely defined switching thresholds V_{refL} and V_{refH}. In a classical Schmitt trigger, the switching thresholds are defined by a resistor network acting as positive feedback on the input node, and it is therefore not suitable. In the actual implementation of the circuit, the hysteresis is thus realized with

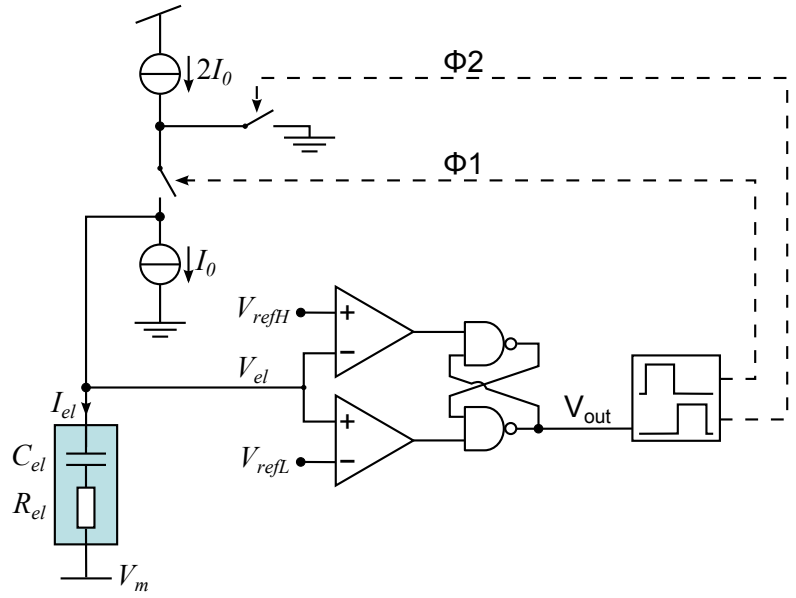

Figure 4.3: Block diagram of the impedance-to-frequency converter with the actual configuration of the comparators and current sources.

separate comparators for each of the reference voltages, connected to a $\overline{\text{SR}}$ NAND latch, as shown in Figure 4.3. When V_{el} falls below V_{refL} during the discharging phase, the output of the lower comparator sets the latch and thus causes V_{out} to go high. This in turn makes the upper NAND gate sensitive to the output of the other comparator. When V_{el} reaches V_{refH} after the following charging phase, the falling output of the upper comparator thus resets the latch.

It is preferable not to implement the transition from charging to discharging with a two-way switch, as it is shown in Figure 4.1. In practice, the two-way switch would be implemented with separate switches between the electrode node and each of the current sources. In this configuration, the switches would be controlled by two signals in anti-phase, and the disconnected current source would always be completely shut down. At the point of transition, large voltage glitches would occur at the high-impedance electrode node due to charge injection from the switches and transient currents from the current source startup. A better implementation is shown in Figure 4.3: While the output of the comparator V_{out} is high, Φ1 is active, Φ2 is low and the arrangement of the two current sources results in a net current of I_0 being injected into the electrode. When V_{out} goes low after V_{el} reaches the upper threshold V_{refH}, a non-overlapping pulse generator ensures that Φ1 goes low before Φ2 becomes active, as a short-circuit to ground would expose the cells to an unwanted high current. In the resulting switch configuration, the

electrode is discharged by $-I_0$. The purpose of the switch controlled by $\Phi 2$ is to keep the channel of the MOSFET in the upper current source active, so that it can instantly resume operation as soon as V_{el} reaches the lower threshold V_{refL} and V_{out} switches again.

4.2 Non-Ideal Behavior and Influences on Measurement Accuracy

In the physical implementation of the circuit, numerous effects can cause a deviation from the intended behavior and must thus already be considered in the design phase. These effects have their origin both in the circuit itself and peripheral to it, and can be classified into systematic (deterministic) and random effects. The first category includes intrinsic transistor capacitances as well as the parasitic capacitance and resistance of connections, systematic deviations of the electrode current such as leakage, and the switching delay of the comparators. In the second category, electronic noise and statistical variations of device parameters are the main influences. A schematic including these parasitic phenomena is shown in Figure 4.4. When the effects of these imperfections are taken into account, the ideal cycle period given in Equation (4.1) now becomes[2]

$$\begin{aligned}\tau_{out} = \tau_{out,ideal} + \Delta\tau_{out} \approx \\ \left(2 - \tfrac{I_{offset}}{I_0}\right)\left(C_{el} + C_{par}\right)\frac{\Delta V + \Delta V_{offset} \pm \overline{V_n}}{I_0} \\ -\left(4 - \left(\tfrac{I_{offset}}{I_0}\right)^2\right)(R_{el} + R_{par})\frac{C_{el}^2}{C_{el} + C_{par}} + t_{delay}\end{aligned} \quad (4.2)$$

where $\Delta V_{offset} = V_{offset1} - V_{offset2}$ and $t_{delay} = t_{d1} + t_{d2}$. The individual terms representing various effects in this equation are summarized in Table 4.1. All these effects cause the transfer characteristic of the impedance-to-frequency converter to deviate from its ideal behavior. Figure 4.5 highlights the effects of some of these circuit non-idealities on the operation of the impedance-to-frequency converter.

As mentioned above, some of these non-ideal effects are localized in the core circuitry of the impedance-to-frequency converter, while others arise

[2]The effects of offset current I_{offset} and parasitic capacitance C_{par} are only approximated in this expression. The approximation for the offset current is explained in the derivation of Equation (4.21) on page 55. For a detailed study of the effect of parasitic capacitance, see the derivation of Equation (4.15) on page 51.

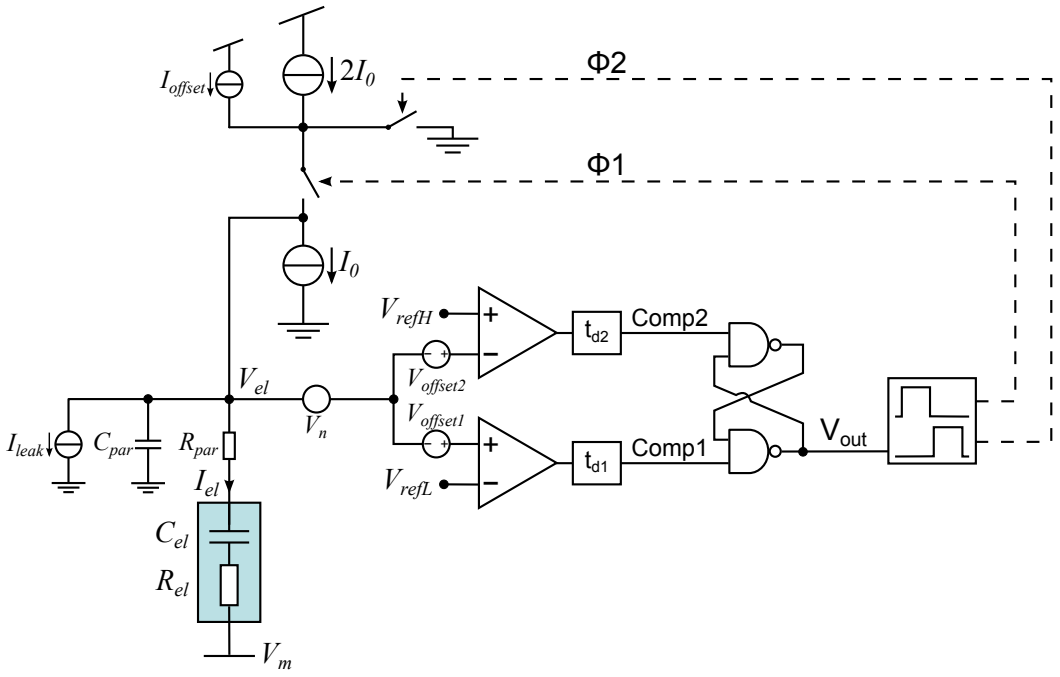

Figure 4.4: Block diagram of the impedance-to-frequency converter including parasitic effects.

Table 4.1: Terms representing individual non-ideal effects in Equation (4.2) and Figure 4.4.

Symbol	Description
C_{par}	Parasitic capacitance, e.g. wiring and transistor gate capacitances.
$V_{offset1/2}$	Comparator offset voltage due to random device parameter variations, causing a deviation of the switching level from the reference voltages.
$\overline{V_n}$	Root mean square value of the integrated total noise within the bandwidth of the comparator.
I_{offset}	Deviation of the current generated by the source from the intended value due to ambient conditions and device variations.
I_{leak}	Loss of current between source and electrode due to leakage.
R_{par}	Parasitic resistance due to wiring and switch on-resistance.
$t_{d1/2}$	Switching delays of the comparators.

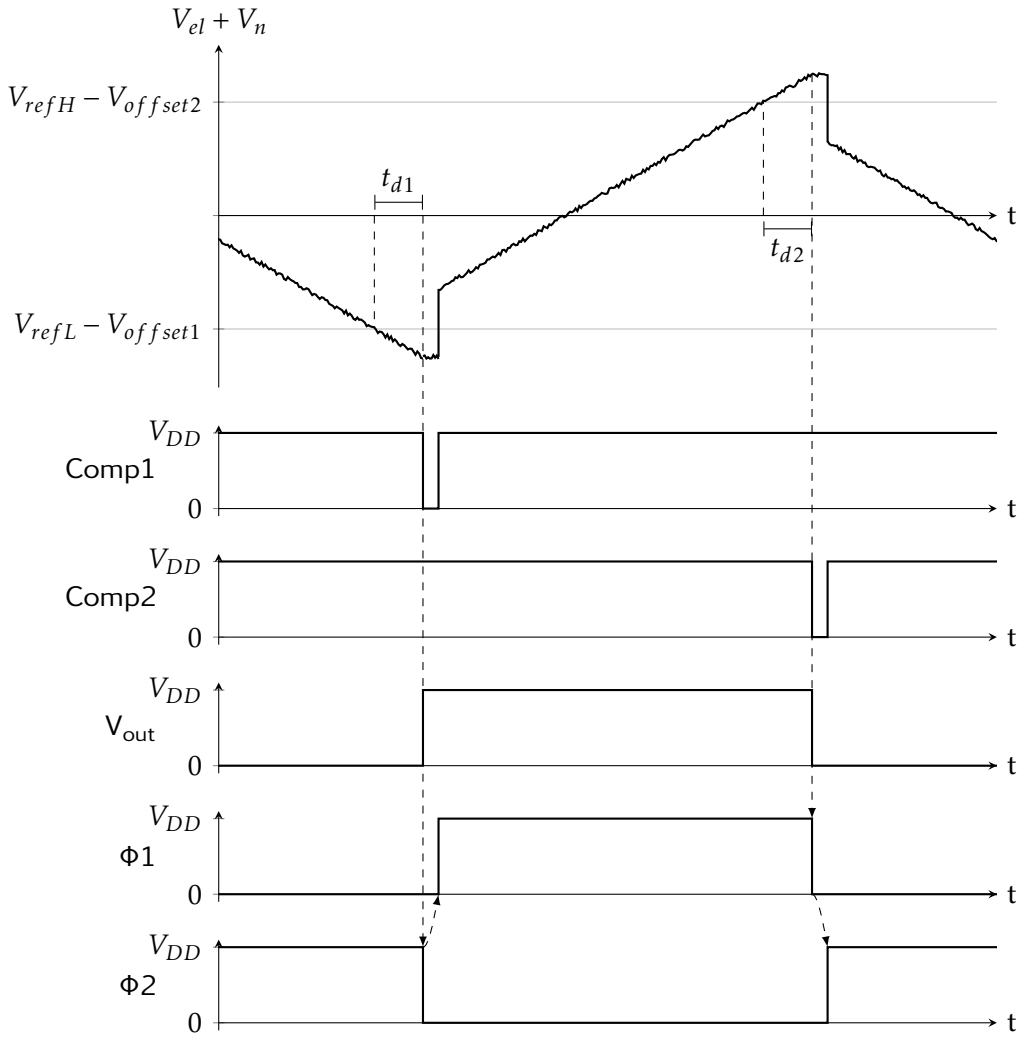

Figure 4.5: Diagram of the electrode voltage and internal digital signals of Figure 4.4 over one cycle, including the effects of noise, comparator offset and switching delay. The comparator delay and the non-overlap interval between the clock phases Φ1 and Φ2 are exaggerated for clarity.

from peripheral parts such as the electrode and its connection to the circuit. Additionally, some effects (particularly those manifesting themselves as random variability) can be countered by spending more area for the physical layout of the circuit, while others (notably parasitic capacitance) increase with the circuit area. Therefore, a trade-off has to be made between different non-idealities. In the end, one of two circuit architectures will turn out to be preferable: Either the circuit area is minimized so that the complete impedance-to-frequency converter fits inside one cell of the electrode array, and the wiring distance between electrode and active circuitry is minimized at the expense of higher circuit variability. Or, as the other extreme, the circuit properties are optimized with little regard for occupied area, even if that means that the circuit will not fit within the array pitch. In this case, a switching matrix can be used to connect the circuit to the individual array electrode sequentially, but the interconnect parasitics will be significant. In order to come to an informed decision, the magnitude and influence on the measurement accuracy of all these imperfections has to be estimated beforehand.

4.2.1 Systematic Deviation

Systematic deviations are caused by effects whose magnitude can be predicted deterministically if the relevant variables are known. Consequently, they can and must be anticipated in the design of a circuit since they degrade its performance, but there is comparatively little uncertainty about them.

Due to the finite speed of the circuit implementation of the comparators, which is limited by factors such as gain-bandwidth and slew rate, there will be a slight delay between the point in time when the two input voltages are equal and the transition of the comparator output, as illustrated in Figure 4.5. The effect of this delay is an error in the switching level which is given by

$$V_{err} = \frac{t_d I_{el}}{C_{el}} \tag{4.3}$$

Depending on the implementation, the delay may be different for the rising and falling transition, and due to mismatch also differ between the two comparators. In Equation (4.2), the net effect is however summarized in a single term t_{delay} for the entire period.

Variations of the supply voltage or the temperature of the circuit can influence the current flowing in a transistor and thus cause a deviation of the source current from its intended value I_0. In the target application, the temperature of the system has to be regulated according to the needs of the cultured

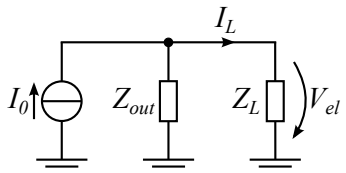

Figure 4.6: Equivalent circuit diagram of a current source with nominal current I_0 and output impedance Z_{out} connected to a load Z_L, which sees a current I_L. V_{el} is the signal to be measured.

cells (typically 37 °C for mammalian cells). Temperature variations are therefore a secondary concern, but since leakage currents increase drastically with temperature, they have to be modeled with this temperature in mind. The impact of supply voltage fluctuations on the generated current should also be minimized. In the physical circuit it is impossible to implement an ideal current source with infinite output impedance. The actual behavior of a current source is modeled by the equivalent circuit diagram in Figure 4.6. If the output impedance of the current source is Z_{out}, and the load to be driven is Z_L, then the current through the load will only be

$$I_L = \frac{I_0}{1 + \frac{Z_L}{Z_{out}}}$$

Obviously the output impedance of the current source should therefore be much higher than the load impedance. The input impedance of the comparators and the parasitic wiring capacitance, which is discussed below, also affect Z_{out} because they act on the current source output node.

Apart from the active circuit elements of the impedance-to-frequency converter, parasitic effects and variability also arise from the wiring and switches in its connection to the electrode. These effects cause parasitic capacitance and resistance as well as current leakage. To a first order approximation, the leakage current as represented by the source I_{leak} in Figure 4.4 cancels over one charge-discharge period, since the current it takes away from the electrode during the charging phase should be exactly balanced by the current it adds during the discharging phase. However, exact calculation shows that the direct influence of I_{leak} on the cycle period (neglecting all other non-ideal effects) is given by

$$\tau_{out,leak} = \tau_{out,ideal} \frac{1}{1 - \left(\frac{I_{leak}}{I_0}\right)^2} \tag{4.4}$$

If the leakage current is a significant fraction of I_0, the slopes of $V_{el}(t)$ during the charging and discharging phases are also no longer of the same magnitude,

and the shape of $V_{el}(t)$ is shifted from the intended triangle waveform to a more sawtooth-like waveform. This increases the high-frequency components of the signal, which due to the strong frequency-dependency of the impedance under study can negatively affect the sensitivity of the sensor.

Current leakage from the connection to the electrode can in principle occur through dielectrics, such as the gate oxide of the comparator MOSFETs, or the insulation between the metal layers. These effects are however not significant in the target technology [57], which has quite thick gate oxides and inter-metal dielectrics. Much more important are the effects associated with MOSFET switches in this path, which are leakage through reverse-biased source/drain-substrate junctions and sub-threshold current. One location in the circuit where these occur are the switches in Figure 4.3. When open, they both have a drain-source voltage of V_{el}. Even with a gate-to-source voltage of zero, this results in a sub-threshold current, which in the BSIM3v3 model [58] is calculated as

$$I_{ds,st} = I_{s0}\left(1 - \exp\left(-\frac{qV_{ds}}{k_B T}\right)\right)\exp\left((V_{gs} - V_t - V_{off})\frac{q}{n_{st}k_B T}\right) \tag{4.5}$$
$$\text{where } I_{s0} = \mu_0 \frac{W}{L}\sqrt{\frac{q^2 \epsilon_{Si}\epsilon_0 N_{ch}}{4k_B T \ln\left(\frac{N_{ch}}{n_i}\right)}}\left(\frac{k_B T}{q}\right)^2$$

with the dimensionless sub-threshold swing parameter n_{st}, and the voltage V_{off} determining the current at $V_{gs} = 0$.

The leakage current from the source/drain diffusions into the substrate can be described by the general diode equation

$$I_D = I_S\left(\exp\left(\frac{V_D q}{n_D k_B T}\right) - 1\right) \tag{4.6}$$

with V_D as the voltage across the diode, and the diode ideality coefficient n_D between 1 and 2. For sufficient reverse bias of the diode ($V_D < -\frac{4k_B T}{q}$), I_D is approximately equal to the saturation current I_S. The temperature dependency of the saturation current I_S can be approximated as [59, sec. 2.3.1]

$$I_S \propto T^{3+\frac{\gamma}{2}} \exp\left(\frac{-E_g}{k_B T}\right) \tag{4.7}$$

with γ as the temperature exponent of the ratio of diffusion coefficient to lifetime of holes. From Equations (4.5) and (4.7) it is obvious that both contributions to the switch leakage current are extremely sensitive to increased temperature.

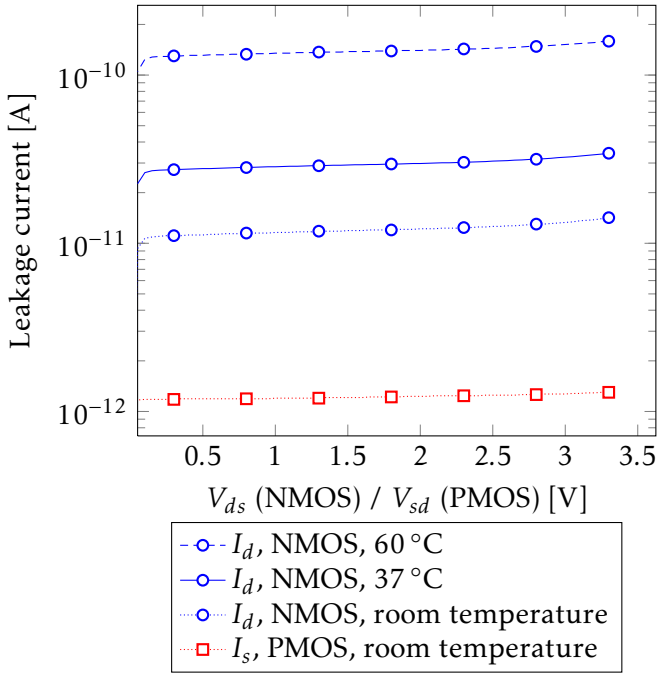

Figure 4.7: Typical measured leakage currents for n- and p-channel MOSFETs with $W/L = 100\,\mu m/1\,\mu m$. For the n-MOSFET, the gate, source and bulk potentials were kept at 0 V. For the p-MOSFET, gate, source and bulk were at 3.3 V.

In order to cross-check the temperature dependence of the transistor leakage current and the data given in the documentation for the target technology, some measurements were performed on available test structures[3]. These consisted of n- and p-channel MOSFETS with a channel width of 100 µm and length of 1 µm. Typical results of a sweep of the drain voltage with $V_{gs} = 0$ are shown in Figure 4.7 for a NMOS at room temperature, 37 °C, and 60 °C, and for a PMOS at room temperature. From these measurements it was concluded that leakage through the source/drain diodes is negligible compared to the sub-threshold current in this technology under realistic operating parameters.

The sub-threshold current of the switches in Figure 4.3 will remain the dominating leakage path in the system as long as there is only one electrode connected to the impedance-to-frequency converter. However, this is not the case if a single circuit is connected to an array of electrodes. In a switching matrix of $M \times N$ electrodes, as shown in Figure 4.8, there will be $M+N-2$ open switches along the path to the addressed electrode. Each of these switches is

[3]The test structures were measured on a single die from a previous multi-project wafer run, so no statistical properties of the leakage current can be inferred.

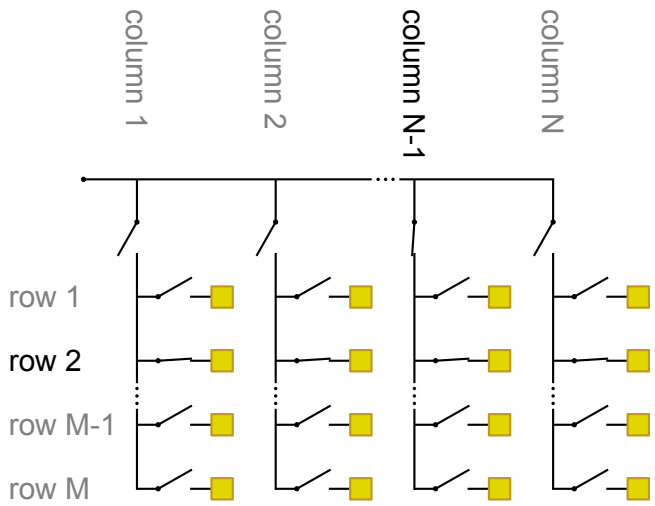

Figure 4.8: Schematic of a switching matrix, connecting an electrode array of M rows and N columns to a single measurement circuit. In the shown configuration, the electrode in row 2, column $N-1$, is addressed.

implemented as a MOSFET and contributes to the total leakage current.

The parasitic capacitance C_{par} is in part due to the gate capacitance of the input transistors in the comparator, but the parasitic capacitance of the connection to the electrode can also become significant as the distance between comparator and electrode increases. This is especially true for configurations where an array of electrodes is connected to one impedance-to-frequency converter via a switching matrix. In such a matrix, the capacitances associated with any closed switches in the path (usually one row- and one column-select switch) are also added to C_{par}. As illustrated by Figure 4.9, the effect of this parasitic capacitance is an increase in the cycle period, since from the point of view of the current source it is parallel to the electrode and thus takes away some of the current. Additionally, since the electrode now only sees a lower current, the voltage drop across the series resistance is diminished. Therefore, the sensitivity of the cycle period to changes in R_{el} is also reduced.

These effects of parasitic capacitance can be derived mathematically by looking at the simplified system in Figure 4.10. It is described by the ordinary differential equation

$$R_{el}C_{el}C_{par}\frac{\mathrm{d}^2V_{el}(t)}{\mathrm{d}t^2} + (C_{el}+C_{par})\frac{\mathrm{d}V_{el}(t)}{\mathrm{d}t} - I_0 = 0 \tag{4.8}$$

which has the general solution

$$V_{el}(t) = V_1 + V_2\exp\left(-\frac{(C_{el}+C_{par})t}{R_{el}C_{el}C_{par}}\right) + \frac{I_0 t}{C_{el}+C_{par}} \tag{4.9}$$

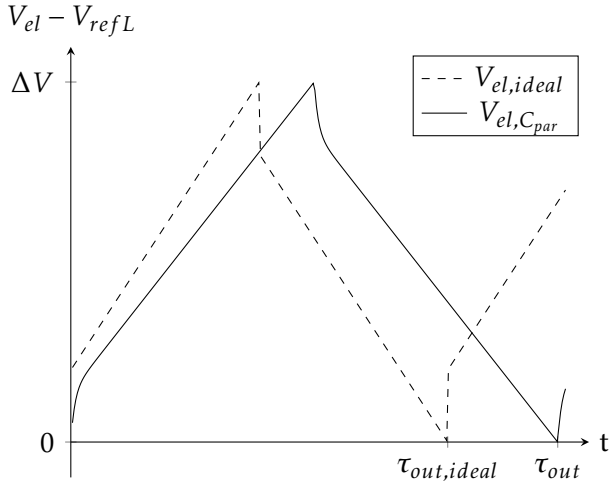

Figure 4.9: Illustration of the effect of parasitic capacitance. Both curves represent the voltage at the electrode and were calculated with identical parameters, except for the parasitic capacitance, which is zero for the first curve and $0.1 C_{el}$ for the second.

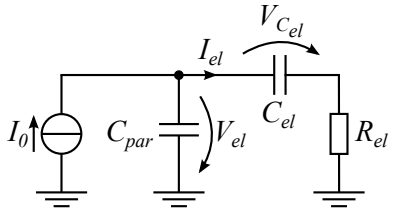

Figure 4.10: Simplified schematic of the system for the treatment of the effect of parasitic capacitance.

Without loss of generality, we can set the boundary condition

$$V_{el}(t=0) = V_{refL} = 0 \tag{4.10}$$

and thereby define V_{el} as the potential with respect to V_{refL}. This gives $V_2 = -V_1$. The voltage across C_{el} is given by

$$V_{C_{el}}(t) = V_{el}(t) - R_{el}I_{el} = V_{el}(t) - R_{el}\left(I_0 - C_{par}\frac{\mathrm{d}V_{el}(t)}{\mathrm{d}t}\right) \tag{4.11}$$

In steady state, we can additionally assume that the magnitude of the current I_{el} through R_{el} is the same at the end of every (dis-)charging phase:

$$I_{el}(t=0) = -I_{el}\left(t = \tfrac{\tau_{out}}{2}\right) \tag{4.12}$$

and therefore adding the two equations

$$0 = I_{el}(t=0)R_{el} + V_{C_{el}}(t=0)$$
$$\Delta V = I_{el}\left(t = \tfrac{\tau_{out}}{2}\right)R_{el} + V_{C_{el}}\left(t = \tfrac{\tau_{out}}{2}\right)$$

yields

$$\Delta V = V_{C_{el}}(t=0) + V_{C_{el}}\left(t = \tfrac{\tau_{out}}{2}\right)$$
$$\text{where } V_{C_{el}}\left(t = \tfrac{\tau_{out}}{2}\right) = V_{el}\left(t = \tfrac{\tau_{out}}{2}\right) - R_{el}\left(I_0 - C_{par}\left.\frac{\mathrm{d}V_{el}(t)}{\mathrm{d}t}\right|_{t=\frac{\tau_{out}}{2}}\right)$$
$$\text{and } V_{el}\left(t = \tfrac{\tau_{out}}{2}\right) = \Delta V$$

which gives the second boundary condition

$$\left.\frac{\mathrm{d}V_{el}(t)}{\mathrm{d}t}\right|_{t=0} = \frac{2I_0}{C_{par}} - \left.\frac{\mathrm{d}V_{el}(t)}{\mathrm{d}t}\right|_{t=\frac{\tau_{out}}{2}} \tag{4.13}$$

With these boundary conditions, the particular solution can be calculated as

$$V_{el}(t) = \frac{I_0 t}{C_{el}+C_{par}} + \frac{2R_{el}I_0C_{el}^2}{(C_{el}+C_{par})^2} \cdot \frac{1-\exp\left(-\frac{(C_{el}+C_{par})t}{R_{el}C_{el}C_{par}}\right)}{1+\exp\left(-\frac{(C_{el}+C_{par})\tau_{out}}{2R_{el}C_{el}C_{par}}\right)} \tag{4.14}$$

Unfortunately, the expression still depends on the cycle period τ_{out}. However, if

$$\frac{\tau_{out}}{2} \gg \frac{R_{el}C_{el}C_{par}}{C_{el}+C_{par}}$$

then the exponential functions in Equation (4.14) can be neglected, and an approximation for the influence of the parasitic capacitance on τ_{out} is given by

$$\tau_{out,C_{par}} = 2(C_{el} + C_{par})\frac{\Delta V}{I_0} - 4R_{el}\frac{C_{el}^2}{C_{el} + C_{par}} \tag{4.15}$$

This approximation was also used to arrive at Equation (4.2). The effect of the parasitic capacitance on the sensitivity to cellular adhesion can be seen by taking the derivative of τ_{out} with respect to R_{el}, which for Equation (4.15) gives

$$\frac{\mathrm{d}\tau_{out,C_{par}}}{\mathrm{d}R_{el}} = -4C_{el}\frac{C_{el}}{C_{el} + C_{par}}$$

while in the ideal case of Equation (4.1) it is just $-4C_{el}$. This illustrates how parasitic capacitance decreases the sensitivity of the sensor and why it should therefore be minimized.

The parasitic resistance R_{par} arises from the wiring between the electrode and the point in the circuit where its potential is measured by the comparator. In part, this is simply due to the resistivity of the metal layers and vias, which is easy to calculate in advance and in general comes out to only few ohms. In a switching matrix, the on-resistance of the transistor switches in the path will therefore dominate, unless the array is very large. For a given achievable gate overdrive $V_{gs} - V_t$, a compromise has to be found between a low on-resistance, which means increasing the ratio W/L, and a low sub-threshold leakage, which demands the opposite. Of course, it is also possible to minimize the influence of the parasitic resistance by using separate paths for the current and voltage sensing, at the expense of twice the interconnect capacitance and switch leakage current.

Relatively precise values of C_{par} and R_{par} can only be determined once the circuit layout is finalized by doing a post-layout extraction. Especially the capacitances between various metal lines are highly dependent on the actual geometry. However, values of the metal-to-substrate area and fringing (side) capacitances furnished by the CMOS foundry allow a good estimate to be made, since inter-metal capacitances are negligible as long as a sufficient distance to neighboring lines is always maintained and lines are not “stacked”, i.e. routed with overlap in different metal layers over significant distances.

4.2.2 Variation and Random Effects

Random variability and fluctuations of various physical quantities also influence the performance of an integrated circuit. Since they are for all practical

purposes non-deterministic, it is impossible to completely anticipate and compensate for them in the design phase. Instead, they must be treated statistically: Their expected values, variances, and other statistical properties can be known in advance, and steps can be taken in the design phase to minimize their impact.

The noise voltage $\overline{V_n}$ arises from a multitude of random physical processes and includes the thermal noise of the parasitic resistances as well as the electrolyte and electrode impedances, the noise of the current sources and the input-referred noise of the comparator. All these effects contribute to a random fluctuation of the observed electrode potential, which in turn causes a random variation of the length of every charge-discharge cycle. In the absence of faradaic processes, the noise of the electrode-electrolyte interface is sufficiently described by the thermal noise of its resistive components [60].

The input offset voltage V_{offset} of the comparator is also random, but can be considered constant for a given physical instance of the circuit, as under normal operating conditions it changes only over long timescales [61]. It arises from the unavoidable device parameter variations which occur during the manufacturing of the circuit. This variability is usually taken into account in the design of a circuit by treating each transistor's threshold voltage V_t and gain factor[4] K as random variables with a normal distribution centered around the nominal value and with standard deviations of σ_{V_t} and σ_K, respectively [62–64]. In general, in a given technology these variations are characterized by the matching constants A_{V_t} and A_K. Both σ_{V_t} and σ_K of a single MOSFET are inversely proportional to the square root of its gate area [64–66]:

$$\sigma_{V_t} = \frac{A_{V_t}}{\sqrt{WL}} \tag{4.16}$$

$$\sigma_K = \frac{A_K}{\sqrt{WL}} \tag{4.17}$$

This model is however not accurate for all geometries and biasing conditions [67, 68].

The variations of the parameters between individual transistors thus cause circuit components which were designed identically to no longer match. (Hence the name "mismatch" for this effect.) The result is that the comparator output no longer switches when the two inputs are equal. Instead, a certain voltage difference has to be applied at the input in order to get the

[4] If we take the drain-source current of a MOSFET in saturation as given by the equation $I_{dsat} = \frac{K}{2}\left(V_{gs} - V_t\right)^2$, the gain factor K is $\mu_{eff} C_{ox} \frac{W}{L}$.

output to switch. This voltage difference is given by V_{offset}. The impact of the offset voltage on the operation of the sensor depends on the implementation of the hysteresis. In the $\overline{\text{SR}}$ latch configuration shown in Figure 4.4, the two comparators are designed identically and therefore the standard deviations of their offset voltages $\sigma_{V_{offset1/2}}$ can also be assumed to be identical. The change in the cycle period depends on the difference of the offsets ΔV_{offset}, which then has a standard deviation of

$$\sigma_{\Delta V_{offset}} = \sqrt{\sigma^2_{V_{offset1}} + \sigma^2_{V_{offset2}}} = \sigma_{V_{offset}} \cdot \sqrt{2} \tag{4.18}$$

as long as $V_{offset1}$ and $V_{offset2}$ are independent, which can be achieved by careful layout [69].

This variation of the effective voltage window also limits the minimum nominal ΔV, i.e. how close the two reference voltages V_{refL} and V_{refH} can be brought together. If we ignore for the moment all other random effects, then $\sigma_{\Delta V} = \sigma_{\Delta V_{offset}}$ and therefore the variance of the period τ_{out} can be calculated as

$$\sigma^2_{\tau_{out}} = \left(\frac{2C_{el}}{I_{el}}\right)^2 \cdot \sigma^2_{\Delta V} \tag{4.19}$$

The relative standard deviation of τ_{out} is then

$$\frac{\sigma_{\tau_{out}}}{\tau_{out}} = \frac{\frac{2C_{el}}{I_{el}} \cdot \sigma_{\Delta V}}{2C_{el}\left(\frac{\Delta V}{I_{el}} - 2R_{el}\right)} = \frac{\frac{\sigma_{\Delta V}}{\Delta V}}{1 - \frac{2R_{el}I_{el}}{\Delta V}} \tag{4.20}$$

Since $\sigma_{\Delta V}$ is independent of ΔV, the relative deviation of τ_{out} increases as ΔV decreases. The expected range of the output frequency $f_{out} = \frac{1}{\tau_{out}}$ of the impedance-to-frequency converter, which by design also is the excitation frequency, however is an important parameter for the design of the circuit. It determines not only the required speed of the comparators, but also e.g. the required output resistance of the current source, because the electrode and cell impedances are highly frequency dependent. For the same reason, the sensitivity of the sensor to cell adhesion also is decreased outside a certain frequency range. In the extreme case, the effective ΔV might even become negative, i.e. $\Delta V + \Delta V_{offset} < 0$, which would make the impedance-to-frequency converter inoperable. This illustrates that too much uncertainty about the effective ΔV is highly problematic, and therefore design measures must be taken to limit the offset voltage of the comparators to an acceptable fraction of the expected ΔV.

It seems that a simple solution to counter the offset voltage problem would be to have a single comparator sensing the electrode voltage and to switch the

reference voltage connected to its other input between V_{refH} for the charging and V_{refL} for the discharging phase. In this case, the same offset applies to V_{refH} and V_{refL}, so that only the voltage window of the electrode shifts as a whole but the duration of the cycle is unaffected. At first sight, this also promises to save on area, but the glitches of the reference voltages induced by the switching present a problem, since they can cause the comparator output to flip and thus produce spurious counts. The connection of the two references to the comparator input would therefore need to be controlled by non-overlapping clock phases and the capacitance at the input node would have to be large enough that charge injection during the switching cannot cause the comparator to flip back. In practice, this requires a dedicated buffering capacitance, and thus the initial area gain of this approach is almost reduced to zero. The $\overline{\text{SR}}$ latch configuration on the other hand has a high inherent robustness against voltage glitches, because after the initial change of the output triggered by one of the comparators, the feedback via the output "desensitizes" the triggering input and the latch is only sensitive to the output of the other comparator. The signal diagram in Figure 4.5 illustrates the transitions of the comparator outputs as well as the latch output during one cycle.

The electrode current will be generated from a reference provided by a circuit on the chip or externally. Since some mismatch of the current mirrors performing this task is unavoidable, the actual current will deviate from the intended value, thus affecting the cycle period by changing the slope of V_{el} in the charging and discharging phases. Since there are two independent current sources for the charging and discharging phases, each of them will also have a different offset. Over the whole period, the offset current of the always active lower current source in Figure 4.4 is approximately canceled, and only the offset current of the upper current source has a direct influence on the period length τ_{out}. Therefore, only the latter is shown in Figure 4.4. The derivation of this approximation is given by the following calculation: Let $I_1 = I_0 + \Delta I_1 + I_{leak}$ be the absolute value of the electrode current during the discharging phase, and $I_2 = I_0 + \Delta I_2 - \Delta I_1 - I_{leak}$ the same during the charging phase, with ΔI_1 and ΔI_2 the offset current of the lower and upper current source, respectively. Assuming for simplicity $\Delta V_{offset} = 0$, $t_{delay} = 0$, $R_{par} = 0$ and $C_{par} = 0$, the expression for the cycle period is given by

$$\begin{aligned}\tau_{out,I_{offset}} &= (\Delta V - R_{el}(I_1 + I_2))\, C_{el}\left(\frac{1}{I_1} + \frac{1}{I_2}\right) \\ &= (\Delta V - R_{el}(2I_0 + \Delta I_2))\, C_{el}\left(\frac{1}{I_0 + \Delta I_1 + I_{leak}} + \frac{1}{I_0 + \Delta I_2 - \Delta I_1 - I_{leak}}\right)\end{aligned}$$

For the case that $\Delta I_1 + I_{leak} \ll I_0$ and $\Delta I_2 - \Delta I_1 - I_{leak} \ll I_0$, this can be simplified into

$$\begin{aligned}\tau_{out,I_{offset}} &= (\Delta V - R_{el}(2I_0 + \Delta I_2))\frac{C_{el}}{I_0}\left(1 - \frac{\Delta I_1 + I_{leak}}{I_0} + 1 - \frac{\Delta I_2 - \Delta I_1 - I_{leak}}{I_0}\right) \\ &= \left(\frac{\Delta V}{I_0} - R_{el}\left(2 + \frac{\Delta I_2}{I_0}\right)\right)C_{el}\left(2 - \frac{\Delta I_2}{I_0}\right) \\ &= \left(2 - \frac{\Delta I_2}{I_0}\right)C_{el}\frac{\Delta V}{I_0} - \left(4 - \left(\frac{\Delta I_2}{I_0}\right)^2\right)R_{el}C_{el} \end{aligned} \tag{4.21}$$

By renaming ΔI_2 as I_{offset} and combining Equations (4.15) and (4.21), the full expression for the influence of non-ideal effects in Equation (4.2) can be obtained.

4.3 Design of the Electrode Array

4.3.1 General Design Considerations

Cells often have complex shapes, with diameters between few 10^{-6} to 10^{-4} m along different directions. In order to capture the signals from groups of few cells, which is necessary to obtain information about their vitality, the diameter of the sensing electrode therefore should be on the same scale. In order to obtain a complete image of the state of the cell culture, the electrode array should also have a small pitch. However, the smaller the electrodes, the lower the allowed current and the higher the impedance it has to be driven into, which creates problems for the circuit design. From the models of the cell impedance discussed in Chapter 3, we also know that larger electrodes see a higher specific impedance of the cell layer and that the placement of the counter electrode plays a crucial role. The array pitch also has to be large enough that neighboring electrodes do not influence each other. So there are conflicting aims in designing the electrode array. Taking into account typical sizes of cells, an array pitch of no more than 200 µm is desirable.

The electrochemical system also imposes certain limits on the sensor: The measurement principle relies on the assumption that no faradaic processes occur, which is generally only a valid approximation if the deviation of the electrode potential is no more than 50 mV from equilibrium. If the equilibrium potential is precisely in the middle between V_{refL} and V_{refH} the absolute maximum value of ΔV is therefore 100 mV, but since without a true reference electrode this cannot be guaranteed, lower values are preferable. The same is also true for the current density at the electrode. Non-linear effects can begin

at current densities of few milliamperes per square centimeter, depending on frequency [19]. Cells may also be affected by high current densities, which would distort the measurement results. Local variations in potential may arise due to ohmic voltage drops, which could for example disturb the cell membrane polarization. In the published literature, there is no explicit information on safe current densities for cell impedance measurements. On the contrary, a lot of research has been done on using electrical fields to deliberately "damage" the cell membrane in order to make it permeable. This method is used e.g. for transferring DNA or other substances into cells and is called electroporation [26]. In prior works on cell impedance measurements [17, 25, 31, 36], current densities of $2\,\mathrm{mA\,cm^{-2}}$ at the electrode were seldom exceeded. In the design of the impedance sensor, a value $j_{max} = 2\,\mathrm{mA\,cm^{-2}}$ was therefore assumed to be safe.

Measurements of the electrode impedance have shown that, to first order, the polarization impedance can be approximated by a capacitance of $C_p = 10\,\mu\mathrm{F\,cm^{-2}}$ (Figure 2.2). The impedance of the cell layer is resistive at low frequencies, but the polarization impedance completely dominates the total impedance if the measurement frequency is too low, thus making the detection of cell adhesion difficult. At higher frequencies, the cellular impedance however also declines due to capacitive coupling through the membranes, and is eventually eclipsed by the spreading resistance. The optimal frequency for measuring cellular adhesion is therefore slightly below the corner frequency of $|Z_{cov} - Z_i|$, which depends on the electrode size (see also Figure 3.4). For electrode sizes between $10^{-5}\,\mathrm{cm^2}$ and $10^{-4}\,\mathrm{cm^2}$, the excitation frequency should be between 1 kHz and 50 kHz.

Since the frequency of the current pulse excitation is also the output variable of the impedance-to-frequency converter, appropriate parameter values have to be chosen in order to keep it in the desired frequency range. The lowest output frequency is expected when R_{el} is negligible, and this "idle" frequency is therefore given by

$$f_{out,idle} = \frac{I_{el}}{2A_{el}C_p\Delta V} \tag{4.22}$$

Even with the highest value of the permissible electrode potential ($\Delta V = 100\,\mathrm{mV}$), the idle frequency of the sensor comes out to 1 kHz without exceeding j_{max}. However, there is a lower limit of the practical electrode current, due to the influence of leakage becoming too great and the implementation of the current source with MOSFETs (see Section 5.2.1). The electrode therefore cannot be made arbitrarily small if j_{max} is not to be exceeded. Assuming a minimum current of 10 nA, the electrode area would have to be at least

$5 \cdot 10^{-6}\,\mathrm{cm}^2$, corresponding to an edge length of about 22 µm.

As with the electrode current, non-idealities of the circuit implementation addressed in the previous section also impose a limit on ΔV, because the effects of mismatch and noise increase with decreasing ΔV. For the dimensioning of the electrode array, a minimum value $\Delta V_{min} = 20\,\mathrm{mV}$ was therefore assumed. For reliable detection of cellular adhesion, the ohmic voltage drop $R_{el} I_{el}$ caused by the resistance of the cells must be above the noise floor, and should be a significant fraction of ΔV, corresponding to an equally significant increase of f_{out} compared to the idle frequency. The minimum resistance needed for a desired value of $R_{el} I_{el} = 0.1 \cdot \Delta V_{min} = 2\,\mathrm{mV}$ can be calculated from the maximum allowed current density as

$$R_{el,min} = \frac{0.1 \cdot \Delta V_{min}}{A_{el} j_{max}} \tag{4.23}$$

For a given size of the sensing electrode, and assuming a gap resistance as modeled by Equation (3.16), Equation (3.17) can then be solved to determine how far away the counter electrode would have to be in order to generate this specified resistance of the cell layer (excluding the spreading resistance R_s):

$$d_{min} = \frac{a}{2}\left(\exp\left(\frac{8hR'_{cl}R_{el,min}}{\rho(R'_{cl} - A_{el}R_{el,min})}\right) - 1\right) \tag{4.24}$$

This minimum distance, together with the electrode size, directly determines how far the pitch of the electrode array can be reduced. In an electrode layout with a grid-like counter electrode and square sensing electrodes of edge length a, as shown in Figure 3.9, the minimum array pitch is given by $a + 2d_{min}$ (neglecting the width of the counter electrode). If a layout with the counter electrode moved outside the grid is assumed, and d taken to represent the distance to the neighboring electrode instead, the minimum array pitch is $d_{min} + a$. This gives a conservative estimate of the pitch based on the assumption that the underlying gap resistance model is only valid up to the point where the next electrode begins.

Figure 4.11 shows the minimum array pitch needed to cause a cell layer to generate a given ohmic voltage drop. The parameter values from the fit to FEM simulation data shown on page 33 were also used for this plot. The solid curves were calculated assuming the minimum voltage drop of 2 mV. However, the parameters used in the calculation represent a full cell cover on the electrode, and the sensor should also be able to detect partial cell coverage. If the desired voltage drop to be caused by complete coverage is therefore increased, the needed array pitch increases and the minimum moves towards

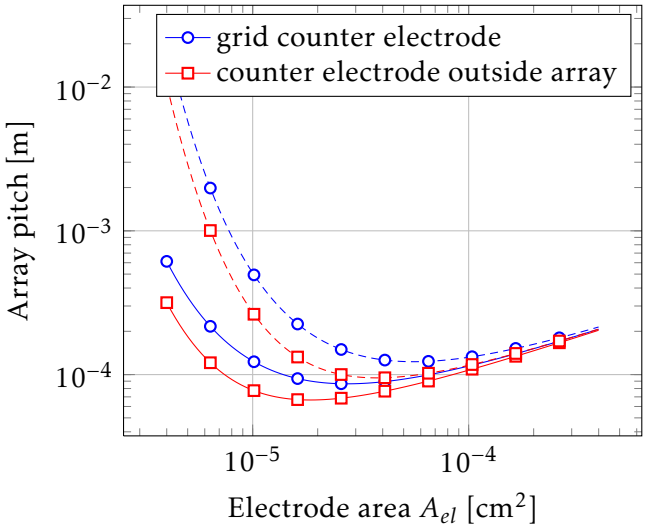

Figure 4.11: Minimum pitch of the electrode array, as a function of sensing electrode area, for an ohmic voltage drop of 2 mV (solid curves) and 4 mV (dashed curves) to be caused by cellular adhesion.

higher electrode areas, as the dashed curves in Figure 4.11 show. Analogously, if the expected resistance of the cell layer is decreased, i.e. higher h, lower ρ, or lower R'_{cl} values are used, a similar effect is observed. As a contingency for the case that the modeling was too optimistic, it may also be desirable to have some headroom to the allowed current density j_{max}. This allows the current to be adjusted upwards during the operation of the sensor in order to generate a better signal or to adjust the excitation frequency. All these factors speak for an electrode size which is larger than the one allowing the minimum pitch. For the following design considerations an electrode area of $3 \cdot 10^{-5}\,\mathrm{cm}^2$, corresponding to an edge length a of 55 µm, will therefore be assumed.

On the other end, the ohmic voltage drop also must not become too high. If $R_{el}I_{el}$ reaches $\frac{1}{2}\Delta V$, then the impedance-to-frequency converter becomes an oscillator whose frequency is determined only by the switching delay of the comparators and the parasitic capacitance, as the electrode voltage would jump almost immediately from V_{refL} to V_{refH} (or vice versa) as soon as the current direction is switched. If the minimum design value $\Delta V = 20\,\mathrm{mV}$ is chosen, and a reduction of the effective value by 2 mV due to offset and noise is factored in, this gives $(R_{el}I_{el})_{max} = 9\,\mathrm{mV}$. The required distance to the counter electrode for this voltage drop to occur can be calculated using Equation (4.24), which gives a value of around 200 µm for an electrode size of $(55\,\mu\mathrm{m})^2$. This therefore seems to be no concern. If a counter electrode at infinite distance

Table 4.2: Summary of design constraints for the electrode array.

Parameter		Limits	Reasoning
Array pitch	max.	200 µm	discerning variations of cell coverage with reasonable resolution
ΔV	min.	20 mV	comparator offset, noise
	max.	100 mV	electrochemical stability
I_{el}	min.	10 nA	leakage, transistor area
j_{max}	max.	$2\,\mathrm{mA\,cm^{-2}}$	linearity of Z_p, influence on cells
$R_{el}I_{el}$	min.	$0.1 \cdot \Delta V_{min} = 2\,\mathrm{mV}$	25 % increase of f_{out} compared to $f_{out,idle}$
	max.	$\frac{\Delta V}{2}$	limitation of the measurement principle
f_{out}	min.	1 kHz	electrode impedance
	max.	50 kHz	decline of cell impedance signal

is assumed and the resulting impedance calculated with Equation (3.10), a higher voltage drop results for the maximum current density. It is therefore important that the current source can be adjusted for lower current densities.

4.3.2 Impact of Parasitic Effects in a Switching Matrix

While the random effects of mismatch and noise influence the choice of the electrode current I_{el} and voltage window ΔV, limitations of the sizing of the electrode array arise from systematic deviations due to leakage current as well as parasitic capacitance and resistance. As outlined in Section 4.2.1, the influence of these systematic deviations is especially important when a switching matrix connects the electrode array to a single sensing circuit. Therefore in this section, design limits for the electrode array arising from these effects will be derived.

In a "single-wire" switching matrix as shown in Figure 4.8, the leakage

current through open switches can be approximated as

$$I_{leak} = (M + N - 2) \cdot W_{switch} \cdot I_{leak,switch} \tag{4.25}$$

where $I_{leak,switch}$ is the leakage current of a single MOSFET switch per unit of channel width, W_{switch} is its channel width, and M and N are the number of array rows and columns, respectively. If the array has a separate path for sensing the electrode potential (”Kelvin-type” measurement), the total leakage current is $2I_{leak}$.

The parasitic capacitance of the wiring between circuit and electrode is given by

$$C_{par} = p(N(wC_{row} + 2C_{fringe,row}) + M(wC_{column} + 2C_{fringe,column})) + 2W_{switch}C_{switch} \tag{4.26}$$

where p is the array pitch, w is the width of the metal wires, C_{row} and C_{column} are the area parasitic capacitances of the metal layers used for the row and column wiring, respectively, and $C_{fringe,row}$ and $C_{fringe,column}$ are the perimeter fringing capacitances of these layers. The capacitance associated with the two closed MOSFET switches in the path is given by the term $2W_{switch}C_{switch}$. As with the leakage current, the parasitic capacitance of a ”Kelvin-type” measurement setup is $2C_{par}$.

The interconnect resistance of the array is given by

$$R_{par} = \frac{p}{w}(NR_{row} + MR_{column}) + 2\frac{R_{switch}}{W_{switch}} \tag{4.27}$$

with R_{switch} as the on-resistance of a unit width MOSFET switch (including the contacts to the metal layers), and R_{row} and R_{column} as the sheet resistances of the metal layers used for the row and column wiring, respectively.

If a limit of the maximum acceptable parasitic resistance is defined as a fraction $l_{R_{par}}$ of the resistance $R_{el,confluent}$ generated by a confluent cell layer, so that $R_{par} \leq l_{R_{par}}R_{el,confluent}$, then the minimum distance to the counter electrode required to satisfy this condition can be calculated by setting $R_{el,min} = \frac{R_{par}}{l_{R_{par}}}$ in Equation (4.24). Likewise, if the leakage current I_{leak} should not exceed a fraction l_{leak} of the source current I_0, which itself is limited to a maximum value of $A_{el}j_{max}$, a minimum electrode size can be calculated as a function of the parameters of Equation (4.25):

$$A_{el,min,I_{leak}} = \frac{I_{leak}}{l_{leak}j_{max}} \tag{4.28}$$

The analogous condition for the parasitic capacitance is $C_{par} \leq l_{C_{par}} A_{el} C_p$, which yields

$$A_{el,min,C_{par}} = \frac{C_{par}}{l_{C_{par}} C_p} \tag{4.29}$$

Appropriate values for the parameters of the above equations have to be chosen in order to make useful statements about design limits of the electrode array. Stray capacitances and sheet resistances of the metal layers were obtained from the process parameter specification of the foundry [57]. The (gate and junction) capacitances of the MOSFET switches were also derived from the limits of the process control parameters defined by the foundry, where the minimum value was taken as the best case and the maximum value as the worst case. (For the junction capacitance, only typical values were provided.) For the best case value of the subthreshold leakage current of the switches, the value of $0.3\,\mathrm{pA\,\mu m^{-1}}$ obtained from own measurements with $L = 1\,\mu\mathrm{m}$ at 37 °C (see Figure 4.7) was linearly scaled to $L = 0.4\,\mu\mathrm{m}$, giving $0.75\,\mathrm{pA\,\mu m^{-1}}$. The typical and worst case values for the subthreshold current were again taken from the process parameters. To take into account the increase of the leakage current due to the operating temperature of 37 °C, the values were additionally scaled by a factor of 2.45, which corresponds to the increase over the room temperature currents observed in own measurements. The on-resistance of the switches was obtained from simulations replicating the conditions in the circuit, i.e. $V_g = V_{DD}$, $V_s = 1.5\,\mathrm{V}$, $V_b = 0\,\mathrm{V}$ and $I_{ds} = 10\,\mathrm{nA}$. Values for best and worst case were obtained with the foundry-supplied "worst case power" (low on-resistance) and "worst case speed" (high on-resistance) corner case parameter sets, respectively. The best case, typical, and worst case values of the parameters used for the calculation of parasitic effects are summarized in Table 4.3. Where possible (gate oxide capacitance, MOSFET subthreshold leakage), pass/fail parameter values were used, which are guaranteed not to be exceeded by the foundry. Other data, such as wiring and junction capacitances, were only available as information parameters whose statistical properties are not guaranteed. It is therefore not possible to calculate the statistical properties of the resulting influences on the switching matrix, but reasonable boundaries on the deviation from typical behavior can be derived.

Finally, the acceptable limits of the parasitic effects must be defined. In the following calculations, the limits for the leakage current and parasitic capacitance, l_{leak} and $l_{C_{par}}$, are 1%, since they affect the sensitivity of the sensor. The parasitic resistance is less problematic in this regard since it can be treated as a static offset. Its limit $l_{R_{par}}$ was therefore set to 10%. The remaining free variables determining the magnitude of the parasitic effects

Table 4.3: Parameter values used to predict the parasitic effects relevant to the design of the electrode array.

Parameter	**Values**			**Note**
	best case	typical	worst case	
h	0.1 µm	1.0 µm	2.0 µm	Values for calculation of d_{min} obtained by fit to FEM simulations
ρ	39.8 Ω cm	59.3 Ω cm	61.3 Ω cm	
R'_{cl}	87.4 Ω cm^2	68.2 Ω cm^2	75.1 Ω cm^2	
R_{switch}	2.6 kΩ µm	4.2 kΩ µm	6.7 kΩ µm	For a temperature of 37 °C and a gate length of 0.4 µm
C_{switch}	2.67 fF µm^{-1}	2.78 fF µm^{-1}	2.91 fF µm^{-1}	
$I_{leak,switch}$	0.75 pA µm^{-1}	1.07 pA µm^{-1}	4.29 pA µm^{-1}	

are the array dimensions (number of rows M and columns N), the pitch p, and the width of the switch transistors W_{switch} and of the wiring w.

The expression for the leakage current (4.25) depends only on the switch width W_{switch}, while that for the parasitic capacitance (4.26) also depends on the wiring width w. These parameters are therefore both varied in unison in Figure 4.12, which shows plots of the minimum electrode areas given by Equations (4.28) and (4.29). However the contribution of the switches to the parasitic capacitance is negligible, so that the change of $A_{el,min,C_{par}}$ in the plot can be attributed to the wiring width. The plot shows that the condition for the leakage current starts to dominate for switch widths larger than approximately 4 µm in the typical case, but much earlier in the worst case. On the other hand, even very narrow wires ($w \to 0$) do not significantly reduce the parasitic capacitance because the fringing (side) capacitance of the wires remains unchanged.

Figure 4.13 shows plots of the minimum electrode areas given by Equations (4.28) and (4.29) against the number of array rows and columns ($M = N$, i.e. a square array is assumed). Even for the worst case and a rather large array of 32×32 electrodes, the influence of both parasitic capacitance and leakage current can be kept below 1% with an electrode size under $3 \cdot 10^{-5}$ cm^2. These effects therefore are not very problematic for medium sized electrode arrays. However it has to be kept in mind that this area is calculated for a single-wire sensing scheme and has to be doubled if a two-wire measurement is implemented, since this also doubles the parasitic capacitance and leakage current. It is therefore important to see if the parasitic resistance makes such a "Kelvin-type" measurement necessary.

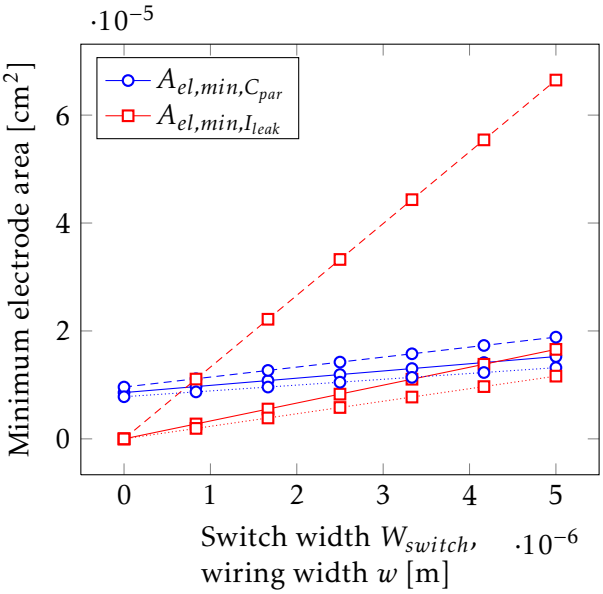

Figure 4.12: Minimum electrode area needed to satisfy the equations (4.28) (squares) and (4.29) (circles) as a function of the widths of the wiring and switch MOSFETs, for an array of 32×32 electrodes. The solid, dashed, and dotted lines represent the expected, worst case and best case parasitics, respectively. In order to obtain an upper bound of the required area, the array pitch p is set to 200 µm for this plot.

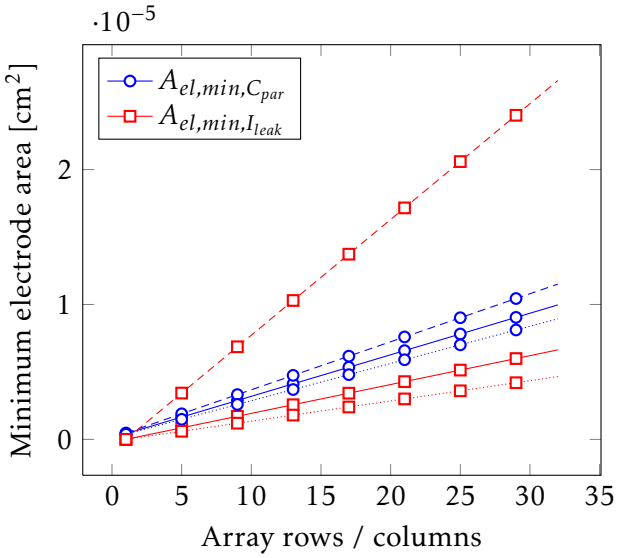

Figure 4.13: Minimum electrode area needed to satisfy the equations (4.28) (squares) and (4.29) (circles) as a function of the number of rows and columns of the electrode array. The solid, dashed, and dotted lines represent the expected, worst case and best case parasitics, respectively. In order to obtain an upper bound of the required area, the array pitch p is set to 200 µm, the width of the wires w to 1 µm, and the width of the switch MOSFETs W_{switch} to 2 µm for this plot.

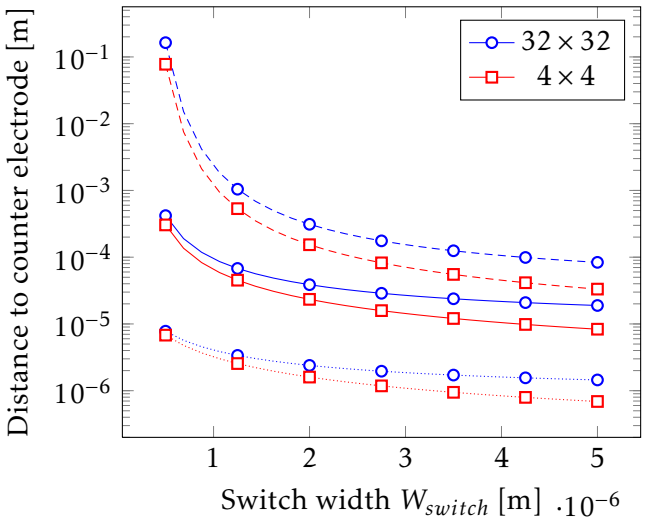

Figure 4.14: Minimum distance to counter electrode needed to limit the parasitic resistance to 10% of the cell resistance, for an array of 32×32 (circles) and 4×4 (squares) electrodes (electrode area $3 \cdot 10^{-5}\,\mathrm{cm}^2$). The solid, dashed, and dotted lines represent the expected, worst case and best case parasitics, respectively. In order to obtain an upper bound of the required area, the array pitch p is set to 200 µm and the wiring width w to 0.6 µm for this plot.

The answer to this question is given by Figure 4.14, which shows the distance to the counter electrode required to keep the parasitic resistance below 10% of the cell layer resistance. Although the value of w was set to the technological minimum, the influence of the wiring resistance on d_{min} remains weak, as the small difference between the curves for the large (32×32) and small (4×4) arrays demonstrates. The total parasitic resistance is dominated by the switches, especially for transistor widths below 2 µm. Increasing W_{switch} above this value gives only diminishing returns. A value $W_{switch} = 2\,\mu\mathrm{m}$ therefore is a good trade-off between the constraints of parasitic resistance and leakage current.

5 Circuit Design and Sensor Implementation

The previous chapters dealt with the theoretical aspects of the cellular impedance and the development of a suitable measurement principle based on these considerations. In this chapter, the realization of a cell adhesion sensor implementing this measurement principle on a test chip will be described. After a description of the high-level architecture of the chip, the implementation of the individual circuit blocks will be discussed along with some considerations influencing their design, followed by the results of characterization measurements.

5.1 Sensor Architecture and Specifications

Minimizing external sources of error and maintaining a high degree of flexibility are of special importance in the first validation of a new measurement principle. These were therefore the main objectives in the design of the sensor circuitry, and correspondingly tight limits on mismatch, current source output impedance and linearity, comparator gain and speed were imposed. The flexibility to adjust the electrical parameters of the sensor, such as electrode current and voltage window, affords the ability to test the circuit under various conditions and can help to compensate for deviations from the expected behavior of the impedance under study.

The sensor implementation should also enable a localized measurement of the cellular impedance, which is achieved by arranging sensing electrodes in an array configuration. The electrode array should be designed in a way that maximizes the sensitivity to cell adhesion. The considerations in the previous chapter provide guidance in choosing the array parameters which can achieve this.

5.1.1 General Circuit Requirements

Due to the sensitivity considerations and other factors discussed in Section 4.3.1, the electrode size will be $3 \cdot 10^{-5}\,\mathrm{cm}^2$, and the frequency range

of the impedance measurement between 1 kHz and 50 kHz. Taking the lower end of this frequency range and looking at Figure 3.4, we see that the electrode impedance alone is roughly $20\,\Omega\,\mathrm{cm}^2$, and the cell layer may contribute up to additional $5-10\,\Omega\,\mathrm{cm}^2$. This means that the expected maximum load for the current source will be about 1 MΩ, and its output impedance therefore must be much higher. Since intrinsic capacitances of the MOSFETs cause the output impedance to decrease at higher frequencies, the highest expected frequency at the output must be factored into the design requirement for the current source. This frequency is higher than the upper design frequency of 50 kHz because the measurement is performed with an (ideally) rectangular excitation signal and not a sine wave, and harmonics therefore have to be taken into account. The design goal was therefore an output impedance of at least 100 MΩ up to 100 kHz, causing a deviation of less than 1% from the intended current. The electrode current is an important degree of freedom for setting the operating frequency of the circuit, and therefore should be adjustable across a wide range. Due to leakage and transistor sizing constraints, 10 nA was set as the lower limit of the electrode current, and any value up to 100 nA should be freely selectable. The integral nonlinearity of the current source across the whole range should be below 1%. The accuracy of the generated current is also negatively affected by mismatch of the transistors in the current source. A relative deviation of 5% with a 3σ (> 99.7%) confidence over the complete current range was considered acceptable.

The implementation of the comparators sensing the electrode potential can only achieve a limited resolution and speed. The static resolution of a comparator is defined as the minimum change of the differential input voltage needed to cause its output to change from one state to the other [70, sec. 8.1], due to its finite voltage gain. A too fine resolution in conjunction with a high bandwidth of course makes the comparator sensitive to noise, as the random fluctuations of the input voltages can then trigger rapid transitions of the output. So although both high speed and resolution are desirable for increased accuracy of the impedance measurement, a certain balance has to be found here. Since a static switching error of 1% of ΔV_{min} seems acceptable, the target for the comparator resolution was set to 200 µV.

Switching delays of the comparators create an upper bound on the output frequency and also cause a deviation of the impedance-to-frequency converter from ideal behavior. The closer the output frequency becomes to this limit, the more the sensitivity of the sensor decreases. Another way to view the effect of switching delays is to examine the error in the switching level of the comparator which they cause, as given by Equation (4.3): $V_{err} = \frac{t_d I_{el}}{C_{el}}$. If the maximum acceptable error of the switching level is set to $V_{err,max} =$

$1\% \cdot \Delta V_{min} = 200\,\mu V$, then the corresponding acceptable switching delay is given by

$$t_{d,max} = \frac{C_{el} V_{err,max}}{I_{el}} \tag{5.1}$$

Setting $I_{el} = A_{el} j_{max}$ gives a value of $t_{d,max} = 1\,\mu s$. This corresponds to a relative frequency deviation of 0.2% at 1 kHz, and of 10% at 50 kHz.

As discussed in Section 4.2.2, offsets of the comparators introduce uncertainty about the voltage window ΔV, which affects the measurement frequency, and in an in-pixel conversion architecture additionally causes variation between measurement sites. The relation between the variabilities of ΔV and τ_{out} is given by Equation (4.20). Assuming $R_{el} I_{el} = 2\,mV$ and $\Delta V = 20\,mV$, the relative deviation of τ_{out} should be limited to 10% with 2σ (> 95%) confidence, i.e. $2\frac{\sigma_{\tau_{out}}}{\tau_{out}} = 0.1$. This gives $\sigma_{\Delta V} = 800\,\mu V$. The variation of ΔV is determined by the independent offsets of the two comparators, and the offset of each comparator is dominated by its input differential pair. As long as proper layout techniques [69] are applied in order to minimize systematic offsets, the V_t deviations of the two input transistors can also be considered independent, and therefore the relationship

$$\sigma^2_{\Delta V} = 2\sigma^2_{V_{offset}} > 4\sigma^2_{V_t,DP} \tag{5.2}$$

gives an approximation of their acceptable mismatch if all other sources of offset are neglected. This requirement gives a limit of the acceptable comparator offset of $\sigma_{V_{offset}} = \frac{\sigma_{\Delta V}}{\sqrt{2}} \approx 566\,\mu V$ (or $3\sigma_{V_{offset}} \approx 1.7\,mV$), which is equivalent to a design requirement for the input differential pair of $\sigma_{V_t,DP} < \frac{\sigma_{\Delta V}}{2} = 400\,\mu V$. Assuming a matching constant $A_{V_t} = 10\,mV\,\mu m$, a MOSFET gate area of at least $WL = 625\,\mu m^2$ is required for each input transistor of both comparators to achieve this offset. Of course, this is only a first-order approximation, and in reality a larger gate area of the input transistors will be needed since other transistors in the comparators also make a small contribution to the offset. Additional area is consumed by wiring, source/drain diffusions, and the required spacing in the final layout of the circuit. In order to stay below the desired maximum offset, a significant part of the area of an array cell would therefore be consumed by the comparators alone if no other techniques for reducing the offset are employed.

The design requirements for the circuit implementation of the impedance-to-frequency converter are summarized in Table 5.1.

Table 5.1: Summary of design requirements for the impedance-to-frequency converter implementation.

Current source	range	10 nA…100 nA
	nonlinearity	< 1% across entire range
	current mismatch	< 5% (3σ confidence)
	output impedance	> 100 MΩ up to 100 kHz
Comparators	static resolution	< 200 µV
	propagation delay	< 1 µs
	input-referred offset	< 1.7 mV (3σ)

5.1.2 In-Pixel Conversion versus Switching Matrix

There are two fundamental topologies for the implementation of a sensor array. The first is to provide one instance of the sensor front-end circuitry for each array element, preferably so that this circuitry is placed directly into the array cell. The main advantages of this topology are the minimal distance between the sensing site and the signal processing, which is mainly beneficial if the measurement is sensitive to parasitic impedance or interference, and the ease of scaling the array to large sizes. Because the individual array sites can operate concurrently, the time needed for measuring the complete array also is unaffected by scaling. The two main disadvantages are the tight area constraints for the circuit and the variation between individual array sites, which in integrated circuits is also exacerbated by the limited area.

The second topology consists of only one instance of the sensor circuitry which is connected to the individual sensing sites of the array through some sort of multiplexer. As discussed previously, the multiplexing can be achieved by connecting the array cells to a switching matrix. The area occupied by the circuit is obviously much less problematic in this configuration, and therefore the statistical variation of the circuit can be reduced by appropriate design measures. However, the variation between individual array cells is less of an issue anyway because all sensing sites are measured with the same instance of the circuit. On the other hand, the significant length of the connection to the sensing site can be detrimental to the performance of the sensor. The time needed to measure all sensor positions also scales linearly with the array size.

These concepts can also be applied to the design of a cell impedance sensor based on the impedance-to-frequency converter described at the beginning of the previous chapter. The in-array conversion approach would require that all

Table 5.2: Key parameters of the target CMOS process [57].

Substrate	p-type with single n-wells
Metal layers	3+1
Nominal supply voltage	3.3 V
Minimum feature size	0.35 µm drawn gate length
NMOSFET nominal threshold voltage	$V_{t0,n} = 0.50\,\mathrm{V}$
PMOSFET nominal threshold voltage	$V_{t0,p} = 0.69\,\mathrm{V}$

elements of the circuit in Figure 4.3, and for concurrent operation of the array cells additionally a counter, fit into an area of no more than 200 µm × 200 µm. It is unlikely that this could be achieved while still fulfilling the requirements on comparator offset, as well as precision and output resistance of the current source. On the other hand, the analysis in Section 4.3.2 has shown that for array sizes at least up to 32 × 32, the parasitic effects originating from a switching matrix do not significantly interfere with the operation of the sensor.

The conversion speed is also not critical for cell impedance measurements, as fluctuations of the signal are on the scale of minutes. This leaves ample time for the sequential readout of even large arrays. A switching matrix architecture was therefore chosen for the implementation of the sensor.

5.1.3 Chip Specifications

The measurement principle of the impedance-to-frequency converter and the models of the cellular impedance were verified with the implementation of the sensor on a test chip. In order to increase the ability to test all aspects of the circuit and to maintain a high degree of flexibility, only the core of the impedance-to-frequency converter was implemented with its output made directly accessible at a pad, and all bias currents and reference voltages were also supplied from off-chip.

The chip was fabricated in a 3.3 V 0.35 µm CMOS process [57] whose key parameters are summarized in Table 5.2. Surface electrodes consisting of a Ti-Pt-Au stack were subsequently added in a back-end lift-off process. This back-end process was initially developed for CMOS DNA sensor chips [71–74], but was also transferred to the technology used for this project. A short summary of the processing of the chips is given below:

The wafers are processed in the foundry in the standard CMOS process up to the third metal layer. After structuring metal 3, a surface passivation

consisting of silicon oxide and nitride layers is deposited. The silicon nitride provides a chemically stable and biocompatible chip surface. A subsequent photolithography step defines the desired openings in the passivation, which are then etched. Tungsten is deposited to fill these openings, then etched to create electrical contacts (vias) between the chip surface and the metal layer below. Following this, photoresist is again deposited and patterned according to the desired layout of the surface electrodes. The electrode layers are formed by first evaporating an adhesive layer of 50 nm titanium onto the wafer, followed by a diffusion barrier consisting of 50 nm platinum, and finally 500 nm gold. The photoresist is then lifted off, which also removes the electrode metal deposited on top of it. Where the resist was already previously removed in the photolithography step, the metal adheres directly to the chip surface and thus remains, forming the electrodes. A schematic cross-section of the final layer structure is shown in Figure 5.1. A micrograph of the fully processed chip is shown in Figure 5.2. The dimensions of the chip are 2 mm by 4 mm.

Based on the results of finite element modeling and the considerations outlined above, an electrode size of $55 \times 55\,\mu m^2$ ($A_{el} = 3 \cdot 10^{-5} cm^2$) was chosen. In order to maximize the measurable cell layer impedance, the counter electrode was realized as two large rectangles, each with an area of $100 \cdot A_{el}$, outside the array. The large area of the counter electrode ensures that its impedance is negligible, so that the impedance seen by a sensing electrode is only determined by the local cell coverage at the array position. The distance to the counter electrode did not have a discernible effect in any of the experiments. The distance between the sensing electrodes is 100 µm, and the array pitch therefore 155 µm. The impedance generated by a confluent cell layer above the electrode with this electrode geometry was expected to be on the order of 100 kΩ.

In order to accomplish a spatially resolved measurement of cell adhesion, in total 64 sensing electrodes were placed on the chip. The electrodes were arranged in four arrays of 4×4, and each array was connected to a separate impedance-to-frequency converter circuit. This made it possible to test different variants of the circuitry. Specifically, two different types of comparator were designed. The first type, implemented in two of the four arrays, is based on a two-stage OTA and implements a closed-loop offset cancellation scheme. It is described in Section 5.2.2 and will be designated as type "A". The second type ("B"), implemented in the other two arrays and described in Section 5.2.3), was designed to have a small internal hysteresis in order to make it more resistant to noise and transient voltage glitches, which nominally increases the effective ΔV by 9 mV. Additionally, two arrays had separate paths

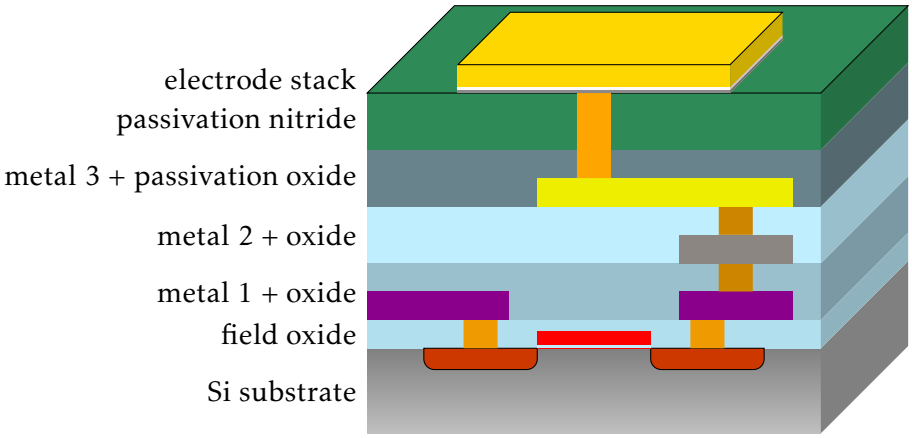

Figure 5.1: Layer structure of the finished chip after back-end process.

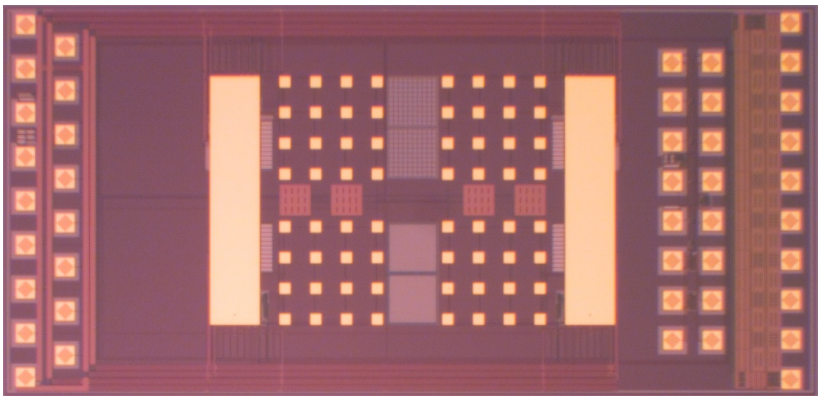

Figure 5.2: Chip photo of the impedance-to-frequency converter test chip before packaging, showing the four electrode arrays with two large counter electrodes to both sides. The leftmost row of pads are supply and reference connections, the pads on the right hand side are the address and control bits and the digital output. Also visible are additional pads for various test structures.

for current forcing and voltage sensing, enabling a Kelvin-type measurement. Each of the four electrode arrays thus implements a different combination of comparator and measurement wiring.

Each of the sensing electrodes can be addressed individually through a digital control interface and a switching matrix. The addressing of individual electrodes of the array is realized in a manner analogous to Figure 4.8, but in a "row-first" configuration, meaning that the first switch selects a row of electrodes, and the second switch connects the electrode in the selected column to this row-line. The correct switches to activate for a given electrode number are determined by a simple AND-gate logic. The last electrode of each array, which is the one closest to the center of the chip due to the horizontal and vertical mirror symmetry of the four arrays, was also made accessible via a pad for testing purposes. An overview of the chip layout with the electrode arrays is shown in Figure 5.3, and a simplified schematic of one of the electrode arrays and the associated impedance-to-frequency converter is shown in Figure 5.4. Table 5.3 describes the functions of the various chip pads providing connections to the external world.

Due to the high gain necessary to achieve the desired resolution, the comparators, especially the OTA comparator, are highly sensitive to noise and glitches of the inputs and supply voltage. Several measures were implemented on the chip to prevent spurious switching and oscillations. Output drivers for digital signals can draw very high currents during signal transitions, which caused problems when the circuits were first tested on multi-project wafers. Therefore on the chip the digital interface was provided with dedicated supply pads (VDDO/VSSO) and moved as far away from all analog circuit parts as possible. Separate supply pads were also provided for the analog circuits (VDDA: comparators and current sources) and digital gates (VDDD: address decoders, non-overlapping pulse generators etc.) of the impedance sensor arrays. The corresponding ground signals VSSA and VSSD were routed separately and connected only at the pad VSS. In order to further mitigate voltage transients on the reference, bias, and supply voltages of the analog parts of the chip, large on-chip decoupling capacitances were attached to these signals. Since the aim here was to realize the maximum capacitance per area, they were implemented with N- or PMOSFETs having their bulk, source and drain connections shorted and connected to VSSA or VDDA, respectively, depending on what potential the particular signal is referenced to.

The bias currents of the comparators and of the electrode current sources on the chip are controlled by the input transistors shown in Figure 5.5. In order to minimize the mismatch of the electrode currents generated by the sources in the four arrays, the reference current of IB_EL is mirrored into

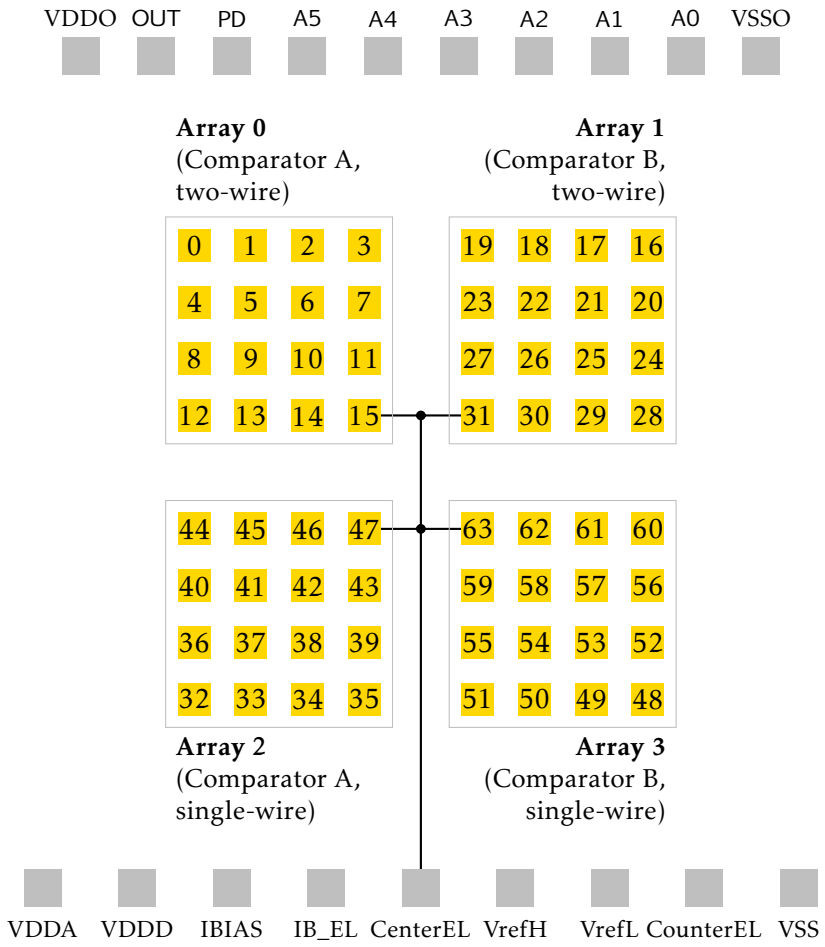

Figure 5.3: Overview of the layout of the electrode arrays on the chip, with electrode numbering, and of the pads for digital I/O (top) and biasing/reference voltages (bottom). The connection of the four electrodes in the chip center to a pad for testing purposes is also illustrated. (Comparator A: see Section 5.2.2; Comparator B: see Section 5.2.3)

Table 5.3: Description of the pads of the test chip related to the impedance-to-frequency converter.

VDDO/VSSO	separate supply and ground for digital interface
OUT	output of the impedance-to-frequency converters, connected to the appropriate circuit by a multiplexer
PD	power-down mode for entire chip, disables all circuits and disconnects all electrodes
A4, A5	address bits for selecting one of the four arrays
A0…A3	address bits for selecting one electrode of the active array
VDDA	supply for analog circuit parts, i.e. comparators and current sources
VDDD	supply for digital gates, e.g. for generating switch control signals
IBIAS	global bias current for the comparators, nominally 64 µA
IB_EL	reference current for electrode current generation
CenterEL	connected to the electrodes around the chip center (numbers 15, 31, 47, 63) for test purposes and control measurements
VrefH/VrefL	connection for the reference voltages for the comparators defining the voltage window ΔV
CounterEL	connected directly to the counter electrodes and supplied by a voltage of $\frac{V_{refH}+V_{refL}}{2}$
VSS	common ground connection

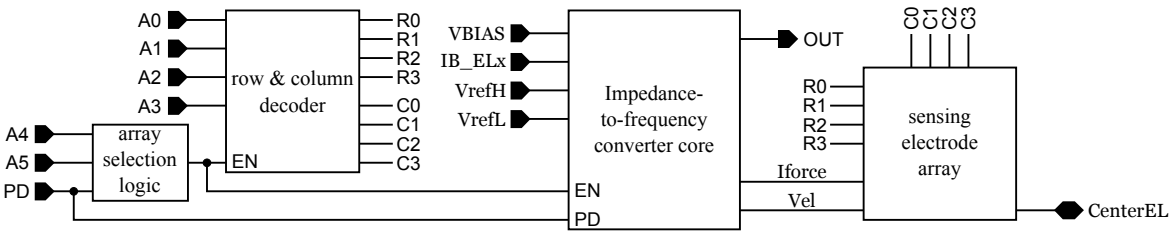

Figure 5.4: Top-level schematic of electrode array with impedance-to-frequency converter circuit.

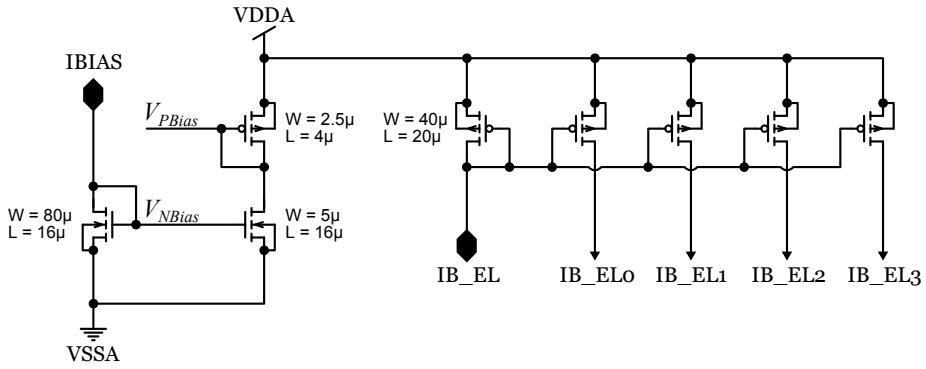

Figure 5.5: Distribution of bias signals on the chip.

four MOSFETs directly at the pad and then transported to the respective circuits. Conversely, the biasing of the comparators is adjusted via distributed voltages V_{NBias} and V_{PBias} derived from the current driven into IBIAS by diode-connected MOSFETs, since precision is not critical and some deviation of the branch currents can be tolerated.

5.2 Implementation of the Impedance-to-Frequency Converter

5.2.1 High Precision, High Output Resistance Current Source

For the size of the sensing electrodes on the chip, at the current density j_{max} a current of 60 nA would be allowed, which is so low that it is typically only achievable with a MOSFET in weak inversion. Looking at the expression of the weak inversion MOSFET current in Equation (4.5), it also seems that sub-threshold operation would yield a high output resistance. However, there are good reasons against using transistors in weak inversion for the current source. Firstly, the parameters of transistor models are often geared towards

accurately reproducing the transistor behavior in strong inversion, as this is the typical use case. The modeled behavior in weak inversion is therefore often quite inaccurate. Secondly, due to the exponential dependence of the current on the gate voltage, current mismatch due to V_t deviations is much worse than in the saturation regime [64, 68].

In order to obtain a good precision of the electrode current, the current source MOSFETs must therefore be operated in the saturation regime, i.e. $|V_{ds}| \geq |V_{gs} - V_t| > 0$. In a long-channel device, the output resistance in saturation is determined by channel length modulation [63, sec. 16.2.5], whose effect on the drain current is given by [58, sec. 2.6]

$$I_{ds} = I_{dsat}\left(1 + \frac{V_{ds} - V_{dsat}}{V_A}\right) \tag{5.3}$$

where I_{dsat} is the saturation drain current in the ideal case ($r_{ds} = \infty$) and V_{dsat} is the drain-source voltage at the onset of saturation. The parameter V_A is analogous to the Early voltage of a bipolar transistor and proportional to the gate length L, and therefore the output resistance scales with L^2 (or L for constant $\frac{W}{L}$).

The accuracy of the generated current is also negatively affected by mismatch of the transistors in the current source. The deviation of the saturation drain current of a MOSFET relative to its ideal value is given by

$$\frac{I_{dsat}}{I_{dsat0}} - 1 = \frac{K}{K_0}\frac{(V_{gs} - V_t)^2}{(V_{gs} - V_{t0})^2} - 1 \tag{5.4}$$

Setting $K = K_0 + \Delta K$ and $V_t = V_{t0} + \Delta V_t$, this can be approximated to first order as [70, sec. 4.4]

$$\frac{I_{dsat}}{I_{dsat0}} - 1 \approx \frac{\Delta K}{K_0} - \frac{2\Delta V_t}{V_{gs} - V_{t0}} \tag{5.5}$$

and therefore the relative standard deviation of the current is [67]

$$\frac{\sigma_{I_{dsat}}}{I_{dsat0}} = \sqrt{\frac{\sigma_K^2}{K_0^2} + \frac{4\sigma_{V_t}^2}{(V_{gs} - V_{t0})^2}} \tag{5.6}$$

Especially at small gate overdrives $V_{gs} - V_t$, the mismatch is therefore dominated by V_t variations.

The desired flexibility to choose the electrode current from a fairly wide range means that the reference current should be provided by an off-chip source. Leakage and noise however make it impractical to directly supply a nanoampere current externally. The reference current therefore has to be

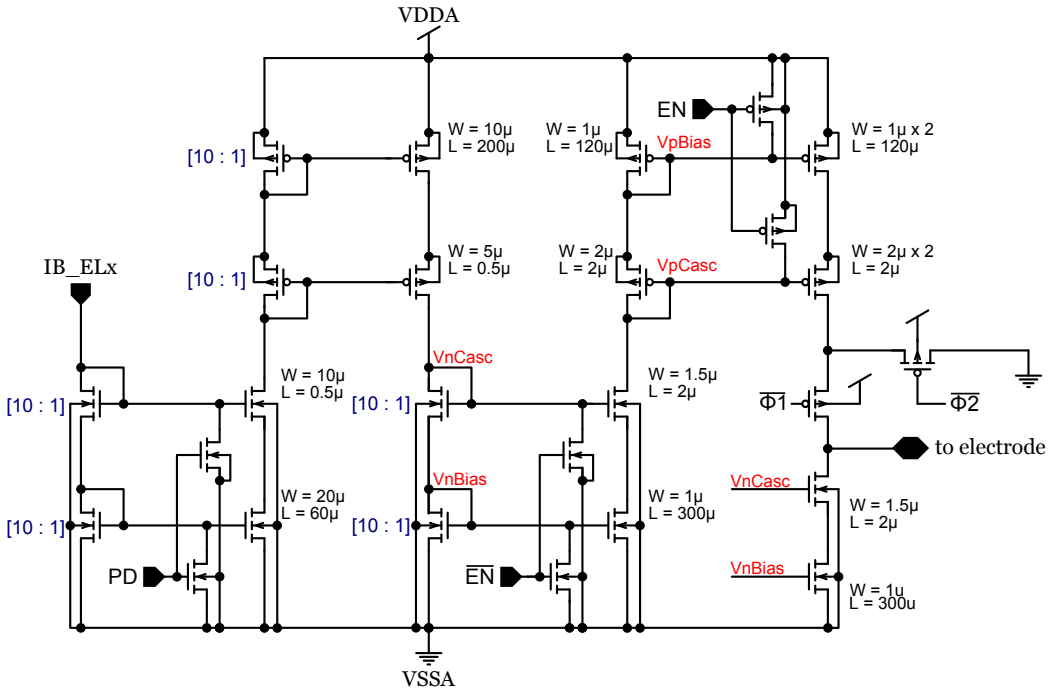

Figure 5.6: Schematic of electrode current generator circuit.

downscaled on-chip from a level that is more easily manageable, which means at least in the microampere range. The current source was therefore designed as a chain of three cascode current mirrors, each with a scaling factor of 10:1, implementing a downscaling of the reference current by a factor of 1000 (see Figure 5.6). The number of stages was chosen with the aim to strike a balance between area consumption and mismatch. The former could be further decreased with a higher number of stages and therefore lower current scaling factor per stage, but the latter increases with the number of stages because each stage introduces additional mismatch. When the electrode array is inactive because a different array is being addressed, the switches controlled by the enable signal (EN and the inverted $\overline{\text{EN}}$) deactivate only the last stage of the current source so that operation can be resumed as quickly as possible. The chip power-down signal PD however additionally shuts down the rest of the current source.

In current mirror devices, increasing the width W while keeping the length L constant has little benefits for matching because the improved matching of the device properties is canceled by the decreased gate overdrive voltage $V_{gs} - V_t$ [67, 68]. On the other hand, increasing L reaches its limits when the transistor can no longer be kept in saturation due to the high gate overdrive which would be necessary to maintain the same current (i.e. the condition $|V_{ds}| \geq |V_{gs} - V_t|$ can no longer be satisfied). The sizing of the current source

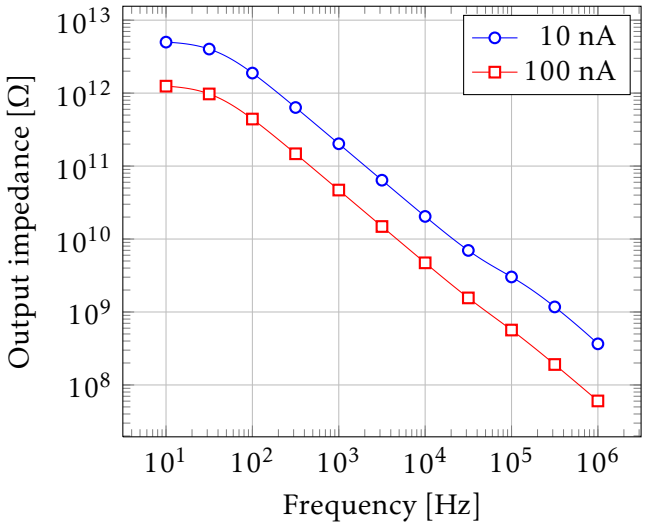

Figure 5.7: Simulated output impedance of the electrode current source for an output current of 10 nA and 100 nA.

transistors therefore has to ensure both sufficient gate overdrive at the lowest current and enough output voltage headroom at the highest current.

Luckily the electrode potential is not expected to vary by more than 100 mV. This also made it possible to use cascoded current sources, which not only offer increased output impedance, but also allowed to improve the current matching by using large transistors for the last stage without loading the electrode node with excessive parasitic capacitance. The simulation results in Figure 5.7 show that the required output impedance is easily exceeded. Over the range $I_0 = 10 \ldots 100\,\text{nA}$ (at constant output voltage), the maximum nonlinearity of the output current is 0.2%. Due to the large areas of the current source transistors, the matching of the output current is also excellent and as expected improves for higher currents, as the results of monte carlo simulations in Table 5.4 show.

As discussed in Section 4.1, the NMOS branch at the output is always active and draws a current of I_0, while the PMOS branch supplying $2I_0$ is connected to the output only during half of the cycle. This switching scheme helps reduce glitches at the output node. The control signals for the switches, $\overline{\Phi 1}$ and $\overline{\Phi 2}$, are generated from the comparator output signal V_{out} by the circuit in Figure 5.8. The delay stages, consisting of a slow inverter followed by a fast one, ensure that each signal only goes active (low) after the other one has finished the transition to inactive state, and therefore the two switches can never be closed at the same time. By shunting the current of the PMOS branch to ground when it is not needed, the current source transistor can remain

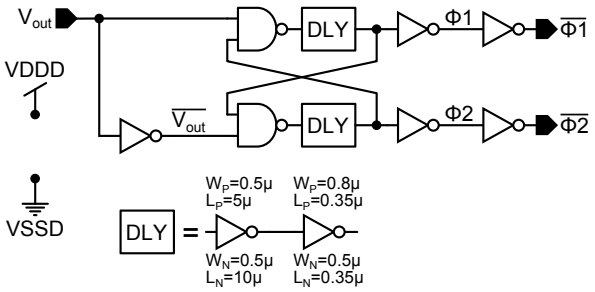

Figure 5.8: Circuit for generating non-overlapping clock phases Φ1 and Φ2 from the output of the comparators.

active. If it were completely shut off and then reactivated, the current would take too long to settle to a stable value due to the large channel capacitance. The small cascode transistor absorbs most of the voltage change during the transition between the clock phases and therefore capacitive currents are minimized.

5.2.2 Offset-Canceling Two-Stage OTA Comparator

The seemingly easiest way to implement a comparator is using an op-amp in an open-loop configuration: its high gain gives good input resolution, and the absence of a direct feedback loop should mean that stability is not an issue and the entire gain bandwidth can be used to achieve high speed [70, sec. 8.2]. However, some differences between the operations of an op-amp and a comparator need to be taken into account. In typical applications of an op-amp, the output is kept in its linear range through an external feedback network, while the comparator output is usually at either its high or low limit

Table 5.4: Mismatch of current source output as obtained by monte carlo simulations (200 runs each).

I_0	mismatch (3σ)
10 nA	2.03%
20 nA	1.47%
40 nA	1.05%
60 nA	0.87%
80 nA	0.77%
100 nA	0.71%

and makes very fast transitions between these states. This means that the slew rate is more important than the gain bandwidth. These fast transitions also cause current spikes on the power supply nodes, and parasitic feedback can occur through these paths.

The comparator should translate an input signal corresponding to the desired resolution of 200 µV into a full output swing of 3.3 V, which requires a gain of 84 dB and a rail-to-rail output stage. This led to the choice of a Miller OTA [62, sec. 6-2] as the basic circuit.

Since the specified offset requirement could normally only be satisfied with very large input transistors, leading to unwanted parasitic capacitance, an offset canceling scheme based on the correlated double sampling technique [75] was implemented. The basic principle is illustrated in Figure 5.9, which represents the first stage of the OTA (with transconductance g_{m1}) and the offset canceling circuit: Essentially, the comparator periodically measures (samples) its own offset and then stores (holds) this information during active operation. In the offset sampling phase (samp active, hold low), the inputs of the comparator are shorted and both connected to the reference voltage. The residual output voltage due to offset and low-frequency noise is fed back through an intermediate buffer (voltage gain A_{v3}) into a separate nulling stage (transconductance g_{m2}), which amplifies the difference between the offset control voltage V_{ocp} and a reference voltage V_{ocm}. The voltage V_{ocm} as reference input represents the ideal output voltage of the first stage when the differential input voltage is zero, which should bias the comparator output exactly at its tipping point. The negative feedback effectively reduces the input-referred offset by the loop gain $1 + A_{v2}A_{v3}$, where $A_{v2} = g_{m2}R_o$.

During the hold phase (samp low, hold active), the control voltage V_{ocp} at the nulling input is stored on the capacitor C_h and thereby made available when the comparator is in operation. Due to leakage, this stored voltage will drop over time, and therefore the sampling has to be repeated periodically. Charge injection from the switch into the hold capacitance causes an error of the voltage V_{ocp}, therefore C_h should be sufficiently large. However, since the amplifier is usually designed so that $g_{m1} > g_{m2}$, the resulting error is smaller than if the offset canceling were performed at the main comparator inputs [63, 75]. Another source of error is mismatch in the offset canceling loop itself. It also shows up at the comparator inputs scaled by a factor of g_{m2}/g_{m1}. So on the one hand the gain $A_{v2}A_{v3}$ should be large in order to effectively suppress the offset of the original amplifier, on the other hand it should still be significantly smaller than $A_{v1} = g_{m1}R_o$ so that charge injection and mismatch of the offset canceling circuit do not introduce too much error.

Since the amplifier is in a negative feedback loop during the sampling phase,

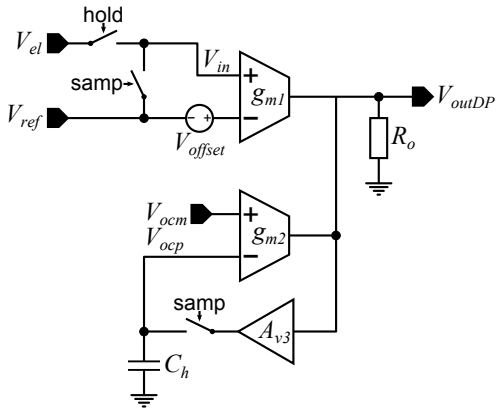

Figure 5.9: Offset canceling scheme (adapted from [75]). V_{outDP} is the output voltage of the first comparator stage, g_{m1} is the transconductance of the comparator input pair, g_{m2} is the transconductance of the nulling input stage, R_o is the output resistance of the first stage, and A_{v3} is the voltage gain of the buffer stage.

stability also has to be considered. C_h can also be used as a compensation capacitance, but would have to be made much larger than needed for the original offset canceling purpose. However the second stage of the OTA is still active during the sampling phase, and therefore a Miller compensation capacitance between the stages was used to ensure the stability of the offset feedback loop.

The implementation of the comparator is shown in Figures 5.10 and 5.11, with the offset nulling input realized as a second differential pair MN3/MN4 as proposed in [75]. Since this already provides a sufficiently high gain, the buffer stage implementing A_{v3} is realized as a simple source follower. As mentioned previously, in the ideal (offset-free) case shorting the inputs of the comparator would bias its output exactly at the tipping point, i.e. $I_{MP3} = I_{MN7}$. As shown in Figure 5.11, the reference voltage V_{ocm} for the offset canceling is therefore derived from a replica of the output stage where the PMOSFET MP4 is in a diode configuration. In the layout of the circuit, apart from the usually critical matched pairs MN1/MN2 and MP1/MP2, care should also be taken to match as precisely as possible MP4 to MP3, MN11 to MN7, MN8 to MN9 and MN10 to MN12 in order to minimize the error introduced by mismatch of the offset canceling circuitry.

In this scheme, the comparator is of course not available during the sampling phase, but this is no problem because each of the two comparators is only needed for half of the charge-discharge cycle: Looking at Figures 4.4 and 4.5, we see that the comparator for V_{refH} is only needed in phase Φ1, and its output signal Comp2 is "known" to be high in phase Φ2. (Vice versa for

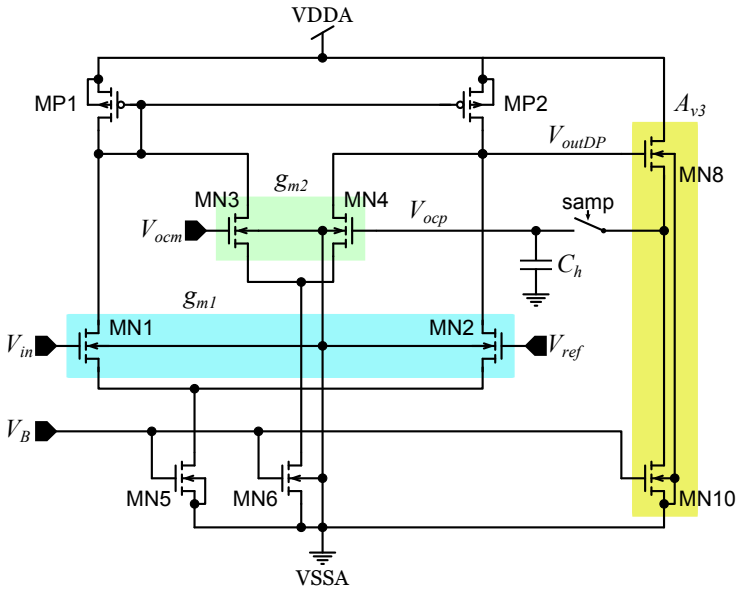

Figure 5.10: First stage of Miller OTA comparator with offset canceling loop, corresponding to the diagram in Figure 5.9.

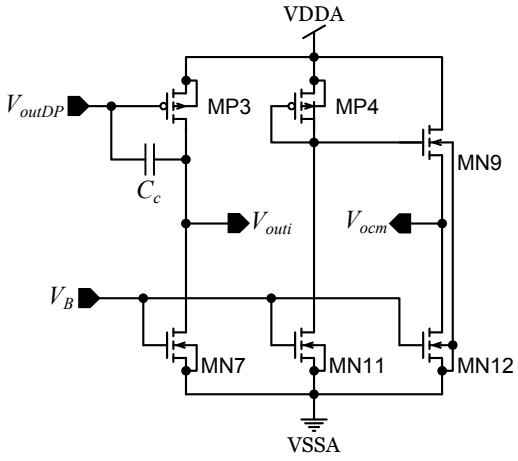

Figure 5.11: MP3/MN7: second stage of Miller OTA comparator (with capacitor C_c for compensating the offset canceling loop); MP4/MN11: duplicate of second stage for generating the reference voltage V_{ocm} for offset canceling. V_{outi} is the "internal" output of the comparator which is then fed into the NAND gates in Figure 5.13.

V_{refL} and Comp1.) The control signals for both comparators are therefore generated from the signals V_{out}, $\Phi 1$, $\Phi 2$ and their inverses by the circuit in Figure 5.12. Briefly, comparator 'X' ($X \in \{1, 2\}$) is put into offset sampling mode (signal sampX high) when the entire array is not currently active (EN low), or whenever the clock signal ΦX is high. The transition to hold mode is made as soon as the "opposite" clock signal comes high. However, the comparator output is activated only after a short delay (signal holdX_d) in order to allow it to settle first. This is achieved by masking the internal comparator output V_{outi} with a NAND gate, as shown in Figure 5.13. The hold phase is terminated by the transition of the signal V_{out} in order to ensure sufficient non-overlap before the cycle begins anew.

Table 5.5 summarizes some simulated performance metrics of the comparator. The offset-canceling circuit reduces the total input-referred offset below the specified value, however itself has a maximum offset of 7.76 mV (3σ) referred to the control inputs V_{ocm} and V_{ocp}. Scaled by the ratio of g_{m2}/g_{m1}, this contributes 1.25 mV to the total residual offset at the input of the comparator.

When the OTA comparator was first tested on a multi-project wafer, fluctuations of supply and bias lines caused by the output drivers were sufficient to create sustained oscillation due to parasitic feedback. As mentioned previously, decoupling capacitors were therefore added to the supply lines and other sensitive analog signals on the test chip. As a fall-back circuit, a second type of comparator was also implemented on the chip, which is described in the following section.

5.2.3 Symmetric Three-Stage Comparator with Internal Hysteresis

The comparator is based on a design by Baker et al. [76, sec. 26.1] and employs a three-stage structure consisting of preamplifier, positive feedback decision circuit [77], and output buffer [78]. In order to eliminate any risk of instability, a dedicated offset canceling loop was foregone, and the offset instead minimized through careful circuit design at the cost of increased parasitic capacitance. In order to further reduce the sensitivity to glitches and noise, the comparator was designed to exhibit a small hysteresis. A schematic of the comparator is shown in Figure 5.14. It has a fully differential structure in all three stages, although only the inverted output V_{outi} is used externally. Not shown in the schematic is a CMOS inverter which was added after this inverted output in order to further increase the edge steepness of the output signal.

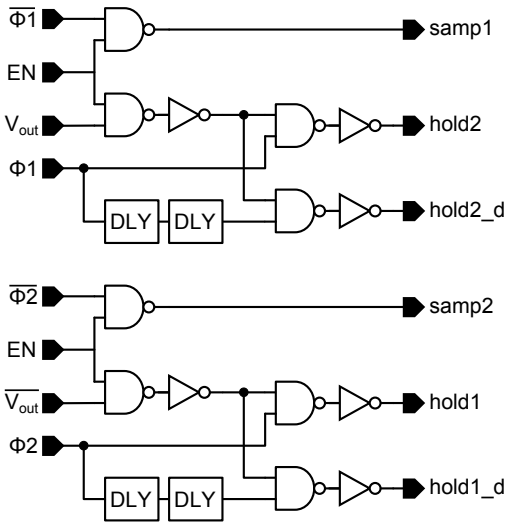

Figure 5.12: Generation of control signals for offset canceling.

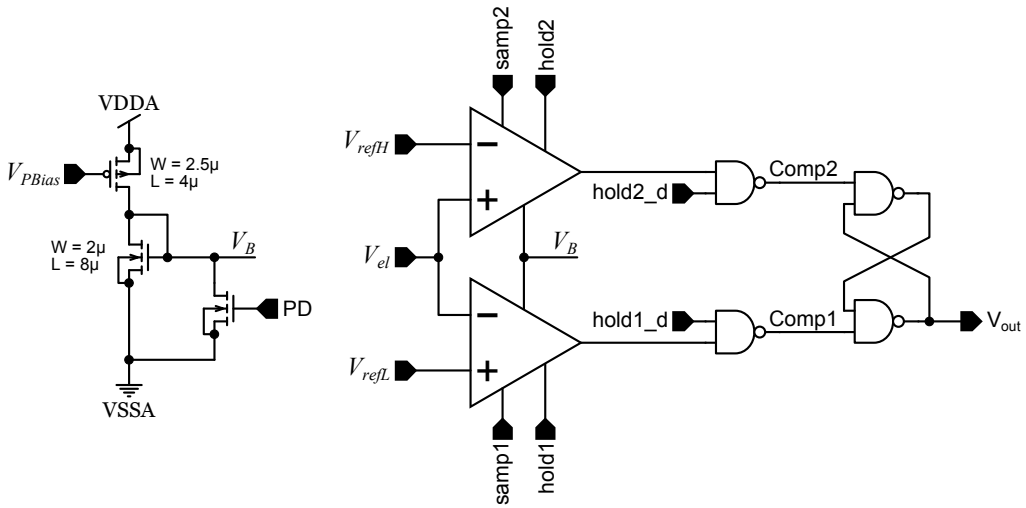

Figure 5.13: Complete schematic of the offset-canceling comparators.

Table 5.5: Simulated characteristics of the OTA comparator with offset canceling.

Parameter	Value
Miller OTA comparator	
DC gain	87 dB
Static resolution	145 µV
−3 dB bandwidth	4.15 kHz
Slew rate	5.83 V/µs
Propagation delay	481 ns
Input-referred offset (3σ values)	
– without canceling	2.51 mV
– with canceling	1.28 mV
– of which due to offset canceling loop	1.25 mV
Offset canceling loop	
DC gain	39 V/V
−3 dB bandwidth	4.86 kHz
Phase margin	70 degrees
Settling time (sampling phase)	10.3 µs

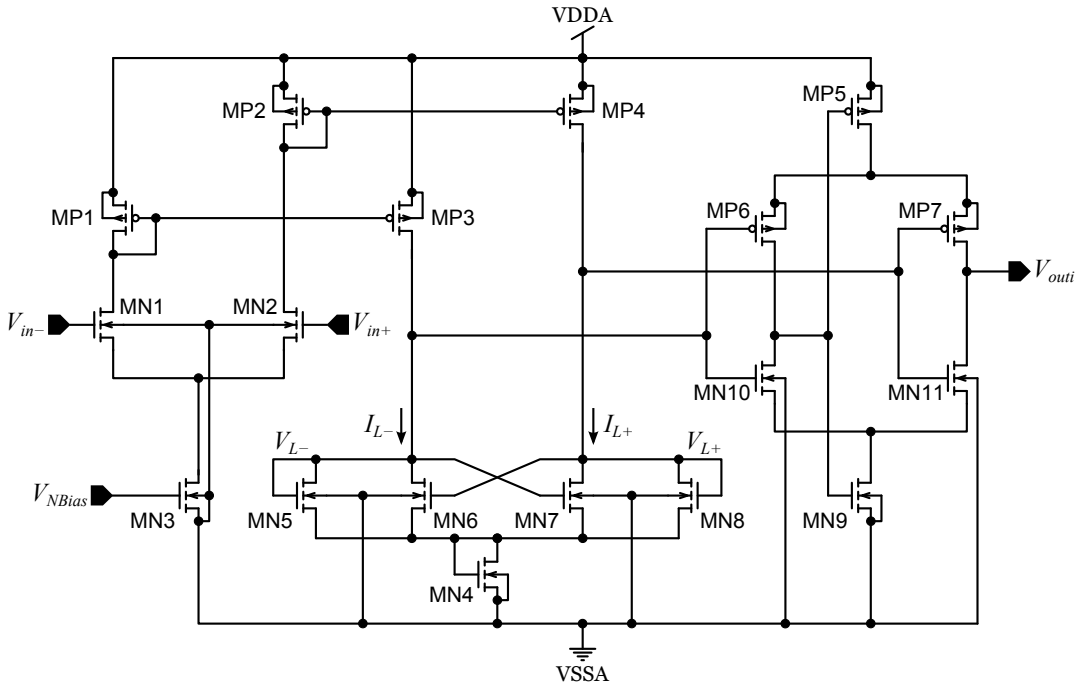

Figure 5.14: Schematic of symmetric comparator, adapted from [76].

The input differential pair consisting of MN1 and MN2 has the function of the first amplification stage, therefore the g_m of these transistors should be large. The first stage of an amplifier usually also has the highest influence on the offset and noise. In order to stay within the specified values, a large gate area of 640 µm^2 was required for each transistor. The two current mirrors MP1/MP3 and MP2/MP4 transport the preamplified signal to the positive feedback decision circuit formed by MN5 – MN8. The diode-connected MOSFETs MN5 and MN8 have identical dimensions and therefore also the same gain factor, which will be called K_A. Likewise, the cross-connected transistors MN6 and MN7 have the same gain factor K_B. If $K_B > K_A$, the decision circuit exhibits a hysteresis with a switching point of $I_{L-} = \frac{K_B}{K_A} I_{L+}$ for rising I_{L-}, and vice versa $I_{L+} = \frac{K_B}{K_A} I_{L-}$ for rising I_{L+} [76, 77]. MN4 only serves to shift the output voltages of the decision circuit to more favorable levels for the following output buffer.

An output buffer is needed to drive digital circuits with the comparator, because the swing of the decision circuit output voltages V_{L+} and V_{L-} is only slightly more than V_t. The third stage of the comparator, which serves this function, is a complementary self-biased differential amplifier [78] consisting of MP5 – MP7 and MN9 – MN11. The self-biasing is achieved with the connection of the drain node of transistors MP6 and MN10 to the gates of the current sources MP5 and MN9, which creates a negative feedback loop, keeping the voltage at this node almost constant. The same loop however results in a boost

Table 5.6: Simulated characteristics of the positive feedback comparator.

Parameter	Value
Slew rate (V_{outi})	27 V/µs
Propagation delay	209 ns
Hysteresis (nominal)	4.55 mV
– variation (3σ)	1.36 mV

of the current available to MP7 when V_{outi} rises, and of the current through MN11 when V_{outi} falls. This increases the slew rate of the inverted output V_{outi}, which also has sufficient swing to drive digital gates.

Some simulated performance metrics of the comparator are given in Table 5.6. Since this comparator was developed as a safe fall-back implementation, the hysteresis, i.e. the differential input signal required to make the comparator trip, was selected significantly higher than the worst case noise level and any glitches which could be expected. The effective voltage window ΔV is increased by twice this hysteresis, i.e. approximately 9 mV. The results of monte carlo simulations indicate that the variation of the hysteresis is below the specified maximum offset voltage.

5.3 Circuit Characterization

After the processing of the chips was finished, and before actual experiments with cells were started, some tests were done in order to ascertain the correct behavior of the sensor. The first checks pertained to the basic functionality and static characteristics of the circuit, e.g. confirming that the bias voltages and current consumption were in the expected range and responded to setting the power-down signal PD like they should. A parameter analyzer was also connected to the pad CenterEL. After addressing one of the electrodes $\{15, 31, 47, 63\}$, the reference current IB_EL was varied and the electrode current I_0 generated by the circuit observed with the parameter analyzer. As far as this could be determined from a small number of tested chips, the electrode current seemed to match well with the desired 1000:1 downscaling from the reference.

After these basic tests, the first experiment was to operate the chip "dry", i.e. without liquid on top, and to observe the influence of changing the parameters ΔV and I_0 on the output frequency of the circuit. The results of such an

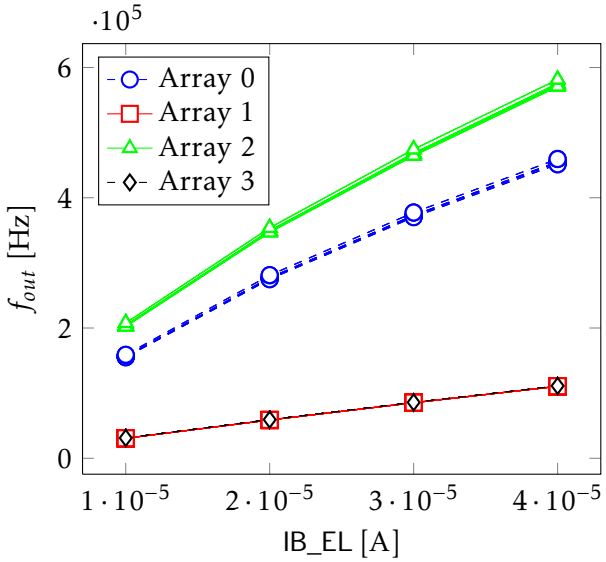

Figure 5.15: Output frequencies of the chip for "dry" operation with various reference currents ($\Delta V = 40\,\mathrm{mV}$). A short description of the differences between the four arrays is given in Table 5.7.

experiment are shown in Figure 5.15. It should be noted that the data points of the electrodes within the same array are grouped so tightly together that they are practically indistinguishable. In arrays 1 and 3, the comparator with internal hysteresis is implemented, which increases the effective ΔV and thus leads to lower frequencies. Without an electrolyte on the electrode, both C_{el} and R_{el} in Equation (4.2) vanish, leaving the parasitic capacitance C_{par} and the comparator delay t_{delay} as the dominant terms determining the cycle period τ_{out} (neglecting offset voltages and leakage currents):

$$\tau_{out,dry} = 2C_{par}\frac{\Delta V}{I_0} + t_{delay} \tag{5.7}$$

A least squares fit of Equation (5.7) to the measured data can then be used to estimate the values of these parasitic terms. The parameters extracted from these experiments for a typical chip are given in Table 5.7. To obtain these values, the frequencies for 15 electrodes in each array were averaged. (Due to the off-chip connection, the 16th electrode would distort the results.) For the arrays 1 and 3, the comparator hysteresis has to be incorporated into the effective value of ΔV. It is interesting to note that the OTA comparator implemented in arrays 0 and 2 is significantly slower due to the Miller compensation capacitance C_c limiting its bandwidth. This is also apparent from the visible deviation of the corresponding plots in Figure 5.15 from an ideal straight line. On the other hand, the comparators in arrays 1 and 3 have very

Table 5.7: Delays and parasitic capacitances extracted from measurements with a "dry" chip with various reference currents and ΔV values.

	Description	t_{delay}	C_{par}
Array 0	Offset-canceling OTA comparator, two-wire array	0.85 µs	0.53 pF
Array 1	Symmetric comparator with hysteresis, two-wire array	0.27 µs	3.18 pF
Array 2	Offset-canceling OTA comparator, single-wire array	0.77 µs	0.40 pF
Array 3	Symmetric comparator with hysteresis, single-wire array	0.33 µs	3.09 pF

large input transistors in order to minimize offset and noise, causing much higher parasitic capacitance. Comparing the first two arrays with the second two, the latter seem to have a slightly lower parasitic capacitance, which could reflect the difference between the two-wire and single-wire measurement. However, since the offset voltages of the individual comparators were not corrected in the data, the accuracy of the extracted parasitic capacitance values is not high enough to draw a definitive conclusion.

The next experiment involved dispensing small quantities of sodium chloride solutions of various concentrations on the chip. For this, the chip and its bond wires were provisionally sealed in the package with epoxy only. (For details on the chip packaging, see the appendix.) Looking at the plot of the output frequencies for different reference currents in Figure 5.16, two things stand out: Firstly, the average frequency is much lower than in Figure 5.15 due to the large capacitance of the electrode-electrolyte interface. Secondly, there is now much more variation of the frequencies between different electrodes, and the electrodes within the same array are no longer visibly grouped together. It can be ruled out that this is an effect of the electrolyte resistance, since there is no correlation between the frequency of a pixel and the distance to the counter electrode. This indicates that the interface capacitance of the electrodes matches very badly, possibly due to different surface roughnesses.

The concentration of the electrolyte influences its conductivity and therefore the resistance R_{el} seen by the impedance-to-frequency converter, but also the polarization impedance depends on the concentration. The relationship between the molar conductivity Λ and the concentration c is given by

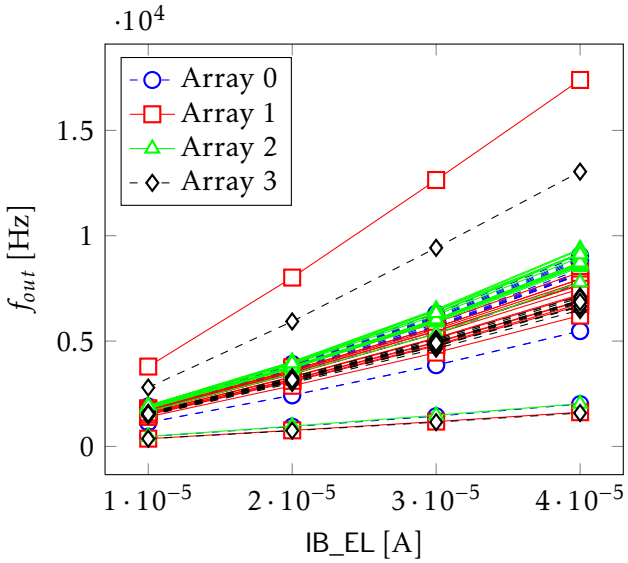

Figure 5.16: Output frequencies of the chip with a solution of 154 mmol L^{-1} NaCl (0.9% NaCl by weight) for various reference currents ($\Delta V = 40$ mV).

Kohlrausch's law [18, sec. 2.2.3]:

$$\Lambda = \Lambda_0 - k\sqrt{\frac{c}{c_0}} \tag{5.8}$$

where Λ_0 is the molar conductivity at infinite dilution and c_0 is the reference concentration, e.g. 1 mol L^{-1}. The conductivity is obtained by multiplying the molar conductivity with the electrolyte concentration:

$$\kappa = \rho^{-1} = \Lambda c = (\Lambda_0 - k\sqrt{\frac{c}{c_0}})c \tag{5.9}$$

Although the absolute electrode series resistance is determined by the geometry and cannot be predicted very accurately, it can be expected to also vary with the concentration like the inverse of Equation (5.9), with constants u and v:

$$R_{el}(c) = \frac{1}{c(u - v\sqrt{c})} \tag{5.10}$$

The dependence of the polarization impedance on the concentration can be explained when treating it as a capacitance C_p described by the Stern model, consisting of a series combination of a fixed Helmholtz capacitance C_H and a diffuse Gouy-Chapman capacitance C_G [18, 21]. Without an applied bias voltage, the capacitance can be calculated by the simplified equation

$$\frac{1}{C_p} = \frac{1}{C_H} + \frac{1}{C_G} = \frac{d_{OHP}}{\epsilon_0 \epsilon_{sol}} + \frac{L_D}{\epsilon_0 \epsilon_{sol}} \tag{5.11}$$

where d_{OHP} is the thickness of the electrochemical double layer, ϵ_{sol} is the dielectric constant of the solution, and L_D is the Debye length. For a sodium chloride solution, the ionic strength equals the concentration, and the Debye length is thus given by

$$L_D = \sqrt{\frac{\epsilon_0 \epsilon_{sol} k_B T}{2 N_A q^2 c}} \tag{5.12}$$

Determining exact values of d_{OHP} and ϵ_{sol} is nontrivial [18]. Nevertheless, the overall dependence of the electrode capacitance C_{el} on the concentration is expected to follow the equation

$$C_{el}(c) = \frac{1}{x + \frac{y}{\sqrt{c}}} \tag{5.13}$$

with the constant x representing the inverse of the Helmholtz capacitance and the term $\frac{y}{\sqrt{c}}$ the diffuse capacitance.

The concentration of the sodium chloride was therefore reduced step by step, and the change of the output frequency of the chip was observed. Starting with a concentration of $154\,\mathrm{mmol\,L^{-1}}$ (0.9% NaCl by weight), in each step the electrolyte was diluted 1:1 with purified water, halving the concentration. For each concentration, the frequencies of all electrodes were measured successively with I_0 set to 10 nA, 20 nA, 30 nA, and 40 nA. Only small changes were observed up to a 16-fold dilution. At this point a new solution of $\frac{154}{16}\,\mathrm{mmol\,L^{-1}}$ was prepared from scratch in order to minimize impurities and the concentration error introduced with each dilution step. A second dilution series was then performed down to a concentration of $\frac{154}{512}\,\mathrm{mmol\,L^{-1}}$. ΔV was initially set to 40 mV, but with the highest dilutions the conductivity seemed to have decreased so far that the ohmic voltage drop $R_{el} I_{el}$ exceeded $\frac{\Delta V}{2} = 20\,\mathrm{mV}$. Therefore for the last two dilutions, ΔV was increased to 80 mV.

Equations (5.10) and (5.13) were plugged into the expression for τ_{out}:

$$\tau_{out} = 2 C_{el}(c) \left(\frac{\Delta V}{I_0} - 2 R_{el}(c) \right) \tag{5.14}$$

This equation was then fitted to the data from the second dilution series, globally for all concentrations and the various settings of ΔV and I_0. In order to smooth out most of the inter-electrode variation, the data were again averaged across several electrodes. In total, the least squares fit of Equation (5.14) reproduced the observed dependence of τ_{out} on the electrolyte concentration quite well. As an example, Figure 5.17 shows the measured

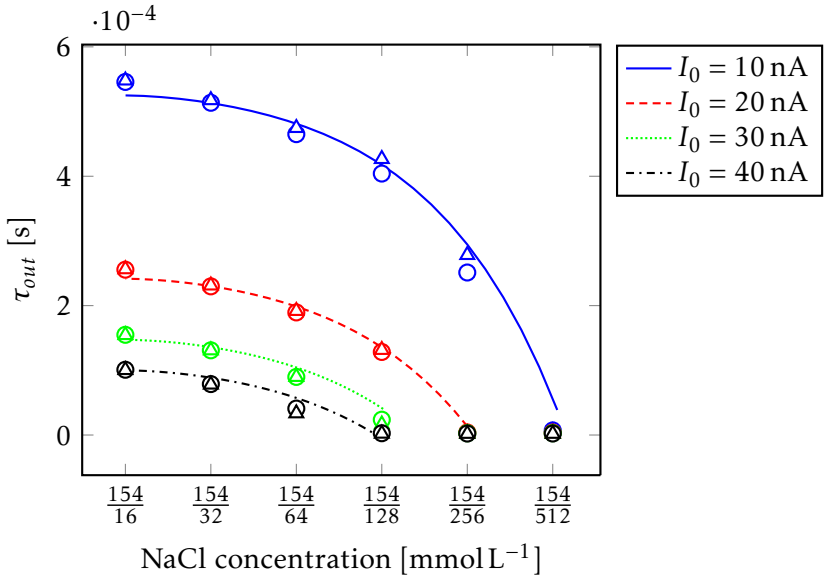

Figure 5.17: Dependence of output period τ_{out} on NaCl concentration for various reference currents. Symbols are array-wise averaged periods (circles: array 0, triangles: array 2). The solid lines are calculated with the global best fit parameters for Equation (5.14). ($\Delta V = 40\,\mathrm{mV}$)

average periods for arrays 0 and 2 at various concentrations and electrode currents, and superposed the corresponding plots of Equation (5.14) using the global best fit parameters.

These results indicate that the response of the sensor to changes of the electrode series resistance and capacitance is in good agreement with the desired behavior. The next step was therefore to test the chip in the intended application, i.e. measuring the adhesion of living mammalian cells.

6 Validation by Experiments with Cells

Preliminary characterization measurements on the test chip have already confirmed the basic function of the integrated impedance sensor. The development cycle of a sensor system is however not complete without the experimental validation in the target application, or at least in an environment which simulates the target application as closely as possible. Numerous experiments with cultured cells growing on the sensor chip were therefore conducted.

As the test chip is intended as a proof of principle for an integrated cell adhesion sensor, these experiments did not precisely replicate the conditions of a water quality monitoring system. Trying to do this from the outset would have been prohibitively complex. Instead, the validation experiments were done in several phases: First, the correct detection of cell attachment, growth and death as the most basic events was confirmed. The ability to detect cellular adhesion locally was also confirmed by intentionally damaging the cell layer. In the second phase, a substance known to cause morphological changes in cells was used to confirm that the sensor is also sensitive to more subtle changes in the state of the cell culture. In order to make the experiments more realistic by providing a constant medium exchange and a gradual rise (and fall) of the analyte concentration, a basic fluidic system was also built. In the third phase, a toxic substance which is found as a pollutant in real drinking water supplies was used. This proved the ability of the sensor to detect practically relevant substances.

6.1 Measurement Setup

Before the experiments with cells could be started, the sensor chip had to be prepared and packaged for exposure to fluids, and a suitable measurement setup had to be devised. A detailed description of the process of creating a functional packaging, which has to protect the chip and at the same time be suitable for cell culture, is given in the appendix (page 119). Figure 6.1 is a schematic cross-section of the final product of this process: The chip is mounted in a carrier and electrically insulated from the liquid with an epoxy resin. A polystyrene Petri dish with a hole corresponding to the package

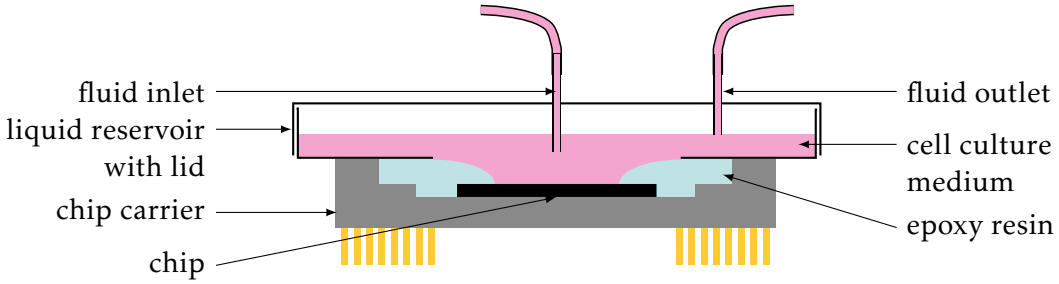

Figure 6.1: Schematic cross section of the packaged impedance sensor chip with the liquid reservoir and fluidic connections.

cavity cut out of its center is glued on top as a liquid reservoir. A lid protects the medium from contamination, and in this version also provides fluidic connections for medium exchange. In the initial experiments, the medium was however exchanged manually, and a lid without these connections was therefore used.

Packaging the chip is only the first step in preparing an experiment. The cells also need an environment with a regulated temperature and atmosphere to survive for extended periods. Contamination of the medium with other microorganisms also has to be avoided, and sterile conditions should therefore be preserved from cell seeding through the course of the entire experiment. This environment can be created easily in an incubator, but the space inside it is very limited. Since the atmosphere inside the incubator should be hermetically sealed, it is also not practical to route cables for all supply and signal connections to the outside. A measurement setup which would fit inside the incubator and provide a compact interface to the outside world therefore had to be developed. It will be described in the first part of this chapter.

6.1.1 Instrumentation

The packaged chip has to be provided with stabilized supply voltages, bias currents and reference voltages, digital address signals, and of course also needs a base for structural support. A circuit board fulfilling all these functions and compact enough to fit into the incubator was developed. In order to evaluate the output of the impedance sensing circuit, a frequency counter with a PC interface was required. Instead of also integrating this function on the circuit board, it was decided to use a compact multi-function interface box (NI USB-6251, *National Instruments*), since this also offered an easy way of outputting the digital control and address signals, and the device was still small enough to fit into the incubator together with the measurement board.

At least for the initial verification of the correct function of the sensor chip, a way to compare its output with a reference was needed. It was therefore decided to provide an external connection to the four center electrodes of the chip (pad CenterEL, connecting to electrodes no. 15, 31, 47, and 63) and the counter electrodes (pad CounterEL) on the circuit board, and to connect an LCR meter (HP4284A, *Hewlett-Packard*) to these. This made it possible to perform impedance spectroscopy on the four center electrodes of the chip. Due to the parasitic capacitance associated with this off-chip connection, only the remaining 60 electrodes were measured with the on-chip circuitry.

Measurement Board

A schematic diagram of the measurement board is shown in Figure 6.2. The reference voltages V_{refH}, V_{refL}, and the counter electrode potential are not loaded by a current (except for some nanoamperes via the counter electrode), but must be very stable and precise. They are therefore derived from a precision voltage reference (ADR423B, *Analog Devices*) via a resistive voltage divider. In the configuration with $30\,\Omega \| 30\,\Omega = 15\,\Omega$ between the reference nodes, as shown in Figure 6.2, the resulting voltage window ΔV is 20.2 mV. It can be changed to 40.2 mV by simply removing the parallel resistors.

The global chip bias current is generated by a Howland current pump circuit [79], formed by the top op-amp in Figure 6.2 and the four resistors connected to it. It injects a constant current of $\frac{3.0\,\mathrm{V}}{46.4\,\mathrm{k}\Omega} = 64.7\,\mu\mathrm{A}$ into the pad IBIAS. The electrode bias current is also provided by a Howland current pump, which is however modified to allow the choice of the sourced current. Here the advantages of this circuit, such as the ability to also sink current (since the pad IB_EL is connected to a PMOSFET) and the high output impedance across a wide voltage range, are more crucial. It is implemented with the middle and bottom op-amps in the schematic. Three switches determine the current: If S1 is closed, it contributes 10 µA, S2 contributes 20 µA, and S3 contributes 40 µA. Any current from 10 µA up to 70 µA, in steps of 10 µA, can therefore be chosen. Since the precision of the reference voltages and bias currents is determined mostly by the resistors, components with a 0.1% tolerance were used for them. All op-amps for the current sources are housed in a single package (AD8604A, *Analog Devices*).

Since the digital signals of the PC interface have a 5 V level, a translation is performed to the 3.3 V level (SN74LVCC3245A, *Texas Instruments*). This is not needed for the other direction, as the high level of the chip output is detected correctly by the interface. In order to perform an impedance measurement on the chip with an external device, connections are provided

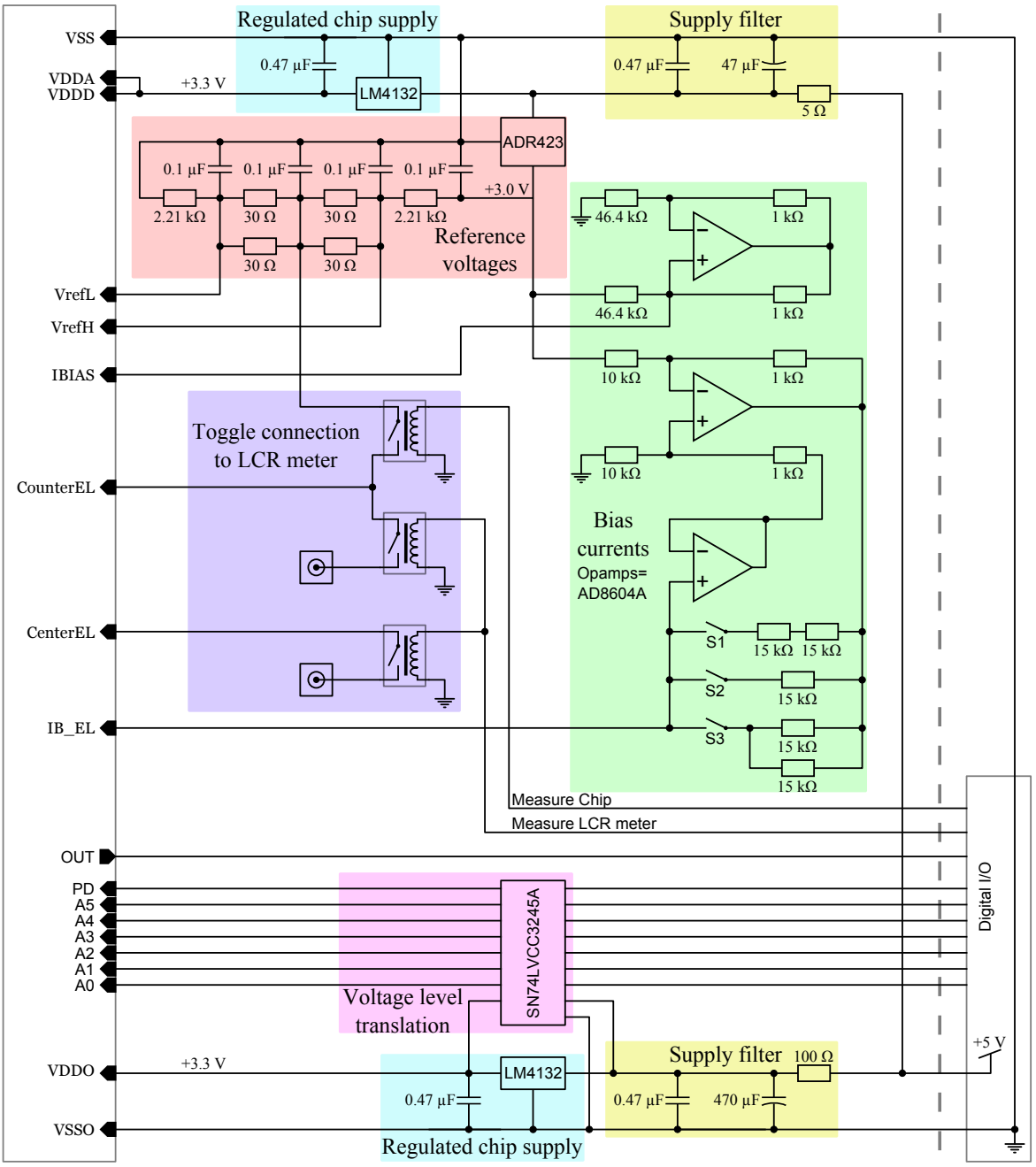

Figure 6.2: Schematic diagram of the measurement board, with the connections to the chip on the left and the off-board connections to the right.

to the center and counter electrodes of the chip through SMB connectors. Since the LCR meter and the on-chip impedance sensor would interfere with each other if they were connected to the electrodes at the same time, relays were installed to toggle between "external" and "on-chip" measurement modes. The relays are controlled by the measurement software via the PC interface. In the "external" mode, the counter electrode is disconnected from its reference voltage and the relays to the SMB connectors are closed. The chip is also put into power-down mode by the measurement software at this time. The "on-chip" mode of course reverses these changes.

A supply voltage of 5 V is provided by the PC interface and powers all auxiliary circuits. In order to keep noise on the analog supply to a minimum, it is routed completely separately from the supply for the digital circuit parts, and RC low-pass filters are installed on both. The external analog components on the board draw a static current and are sensitive to supply voltage drops, therefore a low series resistance had to be used in the filter for the analog supply, and its corner frequency is quite high at 670 Hz. The digital level shifter is less sensitive to a slightly lower supply voltage, therefore a filter corner frequency of 3 Hz could be realized easily on the digital supply rail. This reliably prevents supply voltage glitches caused by digital circuits from reaching sensitive components. The 3.3 V supply voltages for the chip are also derived from the filtered 5 V rails using low-dropout regulators (LM4132, *National Semiconductor*).

Figure 6.3 shows a packaged chip mounted on the circuit board. The chip sits in a 144-pin zero-insertion-force (ZIF) socket, which is larger than the chip carrier in order to leave enough space to operate the lever despite the liquid reservoir. On the right, the short ribbon cable connecting the measurement board to the PC interface is visible.

Software

The data acquisition and device control is done with a program created in LabVIEW 7.1 (*National Instruments*). Via the NI USB-6251 device and the measurement board, this program sets the address and power-down signals of the chip and also controls the relays in the connection to the external LCR meter. This LCR meter is also controlled and read out by the same program using a USB-to-GPIB adapter. During the experiment, the measured data are displayed for convenient monitoring.

When started, the program first configures the LCR meter, and then enters the data acquisition loop, which continuously repeats the following cycle: First, the relays are set for "on-chip" mode and the output of the chip is mea-

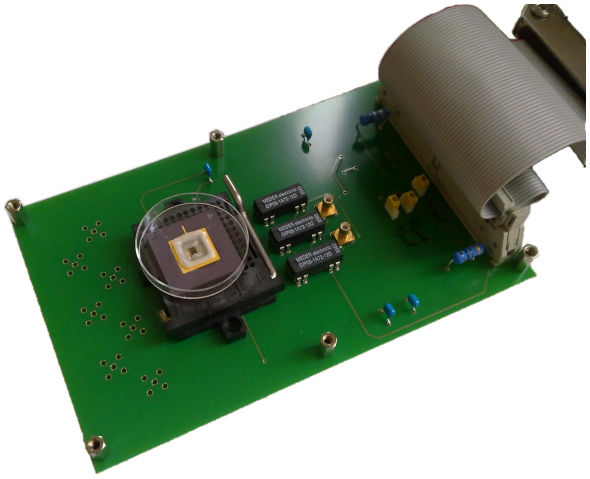

Figure 6.3: Photograph of a packaged chip mounted on the support circuit board, with a ribbon cable connecting it to the PC I/O box and SMB connectors for the LCR meter.

sured for all electrodes in sequence. This is done by setting the corresponding address bits for each electrode and then taking 100 measurements of the period of the chip output signal. The arithmetic mean, standard deviation, minimum and maximum of these measurements are stored, then the next electrode is measured. After measuring all array positions, the chip is put into its power-down mode, the relays are set for "external" mode, and the complex impedance is measured with the LCR meter at 17 frequencies between 20 Hz and 100 kHz. The measurement with the on-chip electronics usually takes less than one second, while the frequency sweep with the LCR meter takes 80 seconds on average and thus determines the sampling rate of the measurement.

6.1.2 Preparation of Experiments

Although the course of each experiment was different depending on the effect to be studied, they had some parameters and steps in common, which will be summarized here. All experiments were performed with the same cell line in order to limit the number of variables which had to be taken into account, therefore making it easier to interpret the results. The cell line V-79 was chosen because prior experience had shown that it is quite robust and grows well on artificial surfaces, forming a confluent monolayer. The cells were cultivated in an incubator with a humidified atmosphere of 5% CO_2 at 37 °C. During the measurements, the chip and support board were placed in the incubator as well to maintain these conditions. The growth medium was

Dulbecco's Modified Eagle Medium (DMEM) supplemented with 10% fetal calf serum (FCS).

Prior to an experiment, a suspension of the cells was created. After counting the cell density, an aliquot corresponding to approximately 10^6 cells was taken. This amount of cells produced a confluent monolayer on the chip within short time. Usually, these cells were seeded onto the chip in a suspension of 2 ml DMEM on a sterile workbench with laminar flow box. Before this, the liquid reservoir and chip had been sterilized with ethanol and rinsed with sterile phosphate buffered saline (PBS). The liquid reservoir was covered with a sterile lid and the chip carefully transported to the incubator, where it was seated in its socket on the measurement board.

In order to operate the sensor in the optimum frequency range, the voltage window ΔV was set to 20.2 mV and the biasing of the chip adjusted for an electrode current of 70 nA in the experiments presented here. This resulted in a slightly higher calculated current density at the electrodes than the assumed limit of 2 mA cm^{-2}, which however seemed to have no negative influence on the cells. The LCR meter was connected to the chip via coaxial cables and the SMB connectors provided on the measurement board. Its excitation voltage was set to 20 mV (RMS amplitude) without DC bias.

6.2 Experimental Results

The following section describes some experiments which were performed with the impedance sensor test chip. They were selected to be a representative subset of all the experiments which were performed.

6.2.1 Detection of Cell Reactions and Death

The purpose of the first experiment presented here is to prove that the integrated impedance sensor is indeed sensitive to impedance changes caused by cells. To this end, an experiment with cells was later repeated without cells under otherwise identical conditions, in order to have a true control. Cells were seeded on the chip as described above with a total medium volume of 2 ml, then the measurement was immediately started. In Figure 6.4, the solid black line is the average output frequency of the chip across all electrodes (minus the center electrodes, as discussed above). The solid red line is the magnitude of the impedance at 40 kHz as measured with the LCR meter. The dashed black and red lines are the corresponding data from the control experiment without cells.

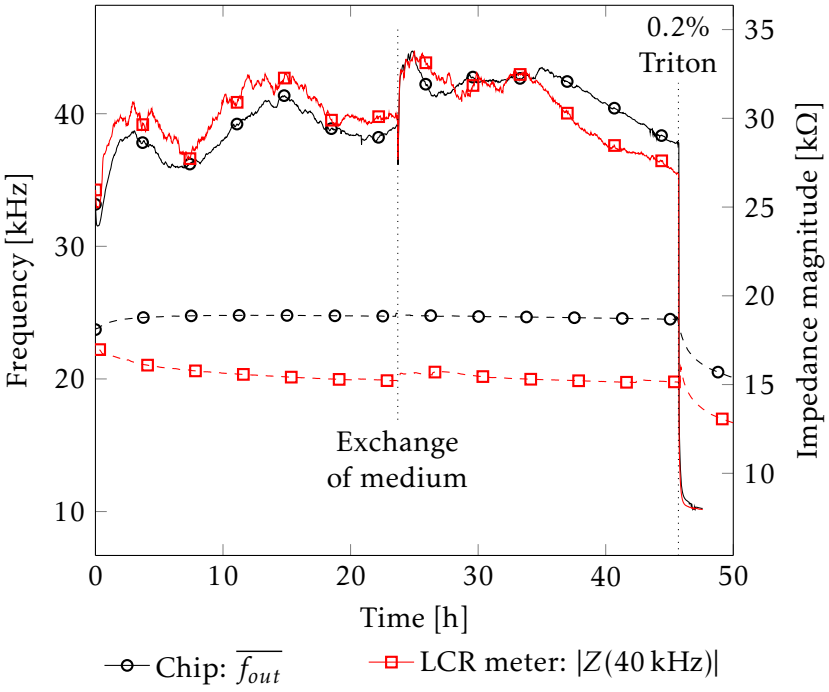

Figure 6.4: Average output frequency of the integrated impedance sensor (black) and impedance at 40 kHz measured with LCR meter (red). Solid lines: experiment with cells, dashed lines: control without cells.

For the first 24 hours of the experiment, the cells were simply let grow on the chip. Especially in the first three hours, a rapid rise of both the frequency and the impedance can be observed. It is assumed that this corresponds to the cells settling from the suspension onto the chip surface, where they attach and try to form contacts with neighboring cells. After this initial phase, both curves begin to fluctuate, but do not rise significantly anymore. In the same period, the curves from the control experiment stay mostly flat, except for some initial drift which might be due to adsorption of medium components on the electrode surfaces.

After 24 hours, the medium was mostly used up.[1] Using a pipette, it was therefore carefully removed and replaced with 2 ml of pre-warmed fresh medium. Immediately afterwards the average frequency and the measured impedance jump upwards, which is a typical reaction. It is probably due to a combination of physical stimulation of the cells by the fluid exchange and the supply of fresh nutrients. In the control experiment, the exchange only causes a barely noticeable reaction.

[1] Meaning that the nutrients and oxygen were depleted, while metabolic products had accumulated. The liquid itself could not vanish (e.g. due to evaporation) because of the lid on the liquid reservoir.

After further 22 hours, the medium was again exchanged in the same manner, but the fresh medium now contained 0.2% Triton-X 100, a detergent which kills cells by destroying their membrane. An immediate and drastic drop of both the frequency and the impedance followed as the cells died off and detached from the chip. Afterwards, the signal remained stable at this low level. In the control experiment, a response is also visible, but it is much weaker than the response with cells.

During the whole experiment, the changes of the mean chip frequency and the impedance measured by the LCR meter show high correlation, confirming the viability of the impedance-to-frequency converter for cell adhesion measurement. The slight discrepancies can be sufficiently explained by the different physical measurement locations on the chip which were accessed by the two instruments. It should however be noted that at the end, the curves of the experiment with cells fall to a significantly lower level than observed in the control experiment. This can be explained by the variation which was observed between chips, as the control experiment had to be performed with a new chip. Different experiments with the same chip also showed some variation, as aging of the electrodes (e.g. due to accumulation of medium residues) was inevitable, and cell cultures can also behave slightly differently every time. In absolute terms, the reproducibility of the experiments is therefore not very high, which is a well-known problem with cell-based assays. It is much more instructive to display the data in a normalized form, e.g. by dividing by the value at the start of the experiment or some other defined time. This is commonly done because it makes it easier to interpret the data and to compare results of different experiments.

It is also interesting to look at complete impedance spectra at different times in the experiment in order to see if they are in agreement with the changes of the chip output and with the models of the cellular impedance which were discussed in Chapter 3. Figure 6.5 shows three such spectra, displayed as real part and imaginary part (the latter multiplied by -1), which represent different phases of the experiment described above. The dashed lines are the average of the impedance measured in the first 30 minutes of the experiment, before the cells began to settle on the chip (which had not been used in an experiment before). The plots for both real and imaginary part are straight lines, indicating that what is seen here is the polarization impedance of the electrode-electrolyte interface, which follows the Ragheb and Geddes [24] model as given by Equation (2.3). In the real part, a slight deviation is seen at high frequencies, where the spreading resistance begins to come through.

The solid lines are the average impedance measured in a ten-hour period beginning ten minutes after the first medium exchange, in which the curves in

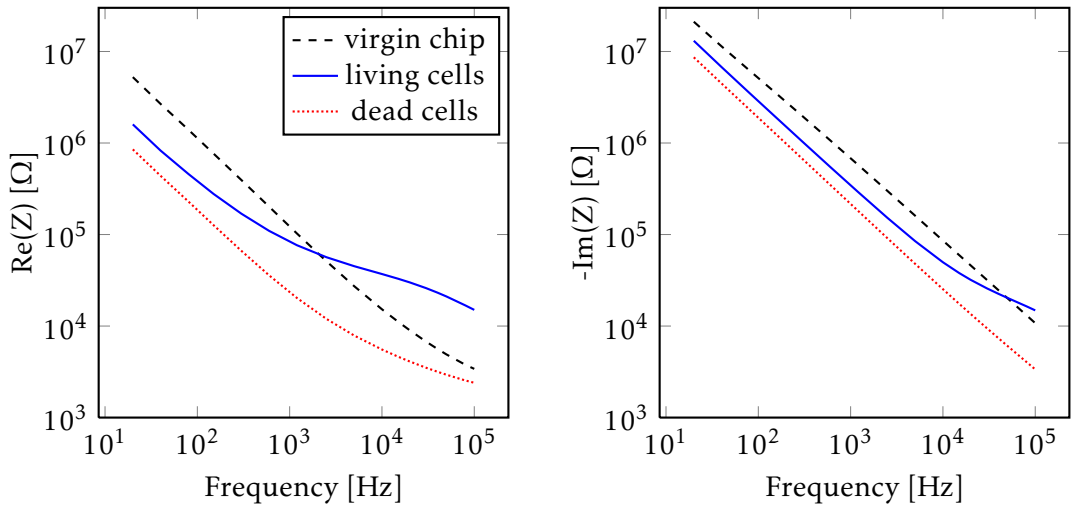

Figure 6.5: Impedance spectra obtained during the experiment shown in Figure 6.4.

Figure 6.4 are quite stable on a high level. It is thus typical of the impedance with a confluent monolayer of living cells attached to the chip. At a first glance, it is somewhat surprising that at low frequencies, the impedance with cells is in fact below that of the virgin chip, as this seems to contradict the assumption that cellular adhesion increases the impedance. This aging effect is however consistent with observations from other experiments, which showed that the impedance and chip output frequencies are initially highest with a previously unused chip, and then drop during the first contact with medium, but also slightly with every subsequent experiment. Apart from this global shift of the curves, the effects predicted by the Urdapilleta et al. [50] model can be observed: In the frequency range between 10^3 Hz and 10^4 Hz, the real part of the impedance clearly shows the increased resistance due to current constriction by the cell layer. Above 10 kHz, capacitive coupling through the cells begins to cause a drop of the in-phase impedance. The inflection seen in the imaginary part at the same frequency is also consistent with this observation.

Finally, the dotted lines are the average impedance measured in the last hour of the experiment, after the cells had been killed and subsequently detached from the chip surface. The curves resemble the spectrum of the virgin chip, but shifted to a level below the impedance with cells. The biggest relative changes between the three measured spectra are observed in the real part at frequencies of some 10^4 Hz, and agree well with the output of the sensor. The decision to choose the excitation frequency of the chip in the same range is therefore justified by this experiment.

6.2.2 Localized Detection of Cell Adhesion

In order to demonstrate the capability of the chip to deliver a spatially resolved measurement of cell adhesion, 10^6 cells suspended in 2 ml of medium were again seeded on the chip and let grow until a confluent monolayer had formed. After 24 hours, the experiment was briefly interrupted. The chip was taken out of the incubator and the cell layer carefully scratched with a plastic pipette tip, exposing a number of electrodes (see Figure 6.6). The electrodes were broadly categorized according to the fraction of their area which was exposed by the scratch (undisturbed, less than 10% exposed, approx. 50% exposed, or completely exposed). The chip was then placed back in the incubator and the experiment continued.

Figure 6.7 shows the mean frequencies of the undisturbed electrodes and of the electrodes which were exposed to the electrolyte, all normalized to the last data point before the scratch. The signal for the electrodes which were still covered by cells shows only a slight change after the interruption, which is probably due to the disturbance caused by temporarily removing the chip from the incubator. The frequencies of the exposed electrodes dropped sharply as expected. The magnitude of the drop correlated well with the exposed electrode area. During the following hours, the frequencies of the electrodes which had the least area exposed also recovered quickly to the previous value as cells along the edge of the scratch spread out. The signals of the electrodes which had more of their area exposed recovered significantly more slowly.

6.2.3 Cell Settling, Test of Fluidic System, and Detection of Reversible Morphological Changes

The experiment described in the following ran for more than four days and is thus one of the longest which were performed. It will therefore be described in several parts, each focusing on a different aspect of the results. In the previous experiments, the output frequency of the impedance-to-frequency converter was averaged across several electrodes. This smoothed out much of the higher frequency fluctuations of the signals from individual electrodes. However, these components also contain information on the state of the cell culture, as this experiment will demonstrate. Therefore, the chip output frequencies of the individual electrodes will be plotted, like in Figure 6.8, which shows the output frequencies of the sensor chip for 60 active sensing electrodes. The evident separation of the curves into two groups clustered above and below approximately 5.5 kHz, respectively, is due to the two comparator variants

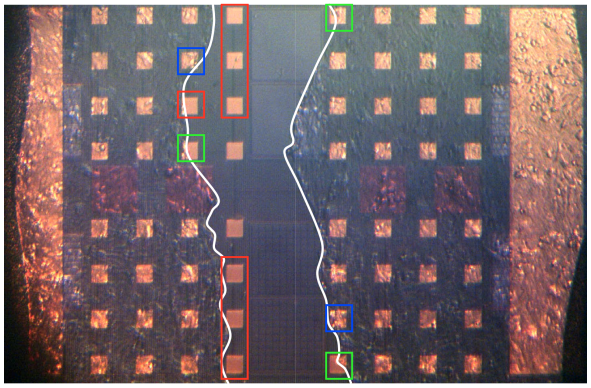

Figure 6.6: Chip photograph of the freshly scratched cell monolayer 24 hours after seeding (scratch boundary highlighted in white). The exposed electrodes are highlighted in the colors corresponding to the respective graph in Figure 6.7.

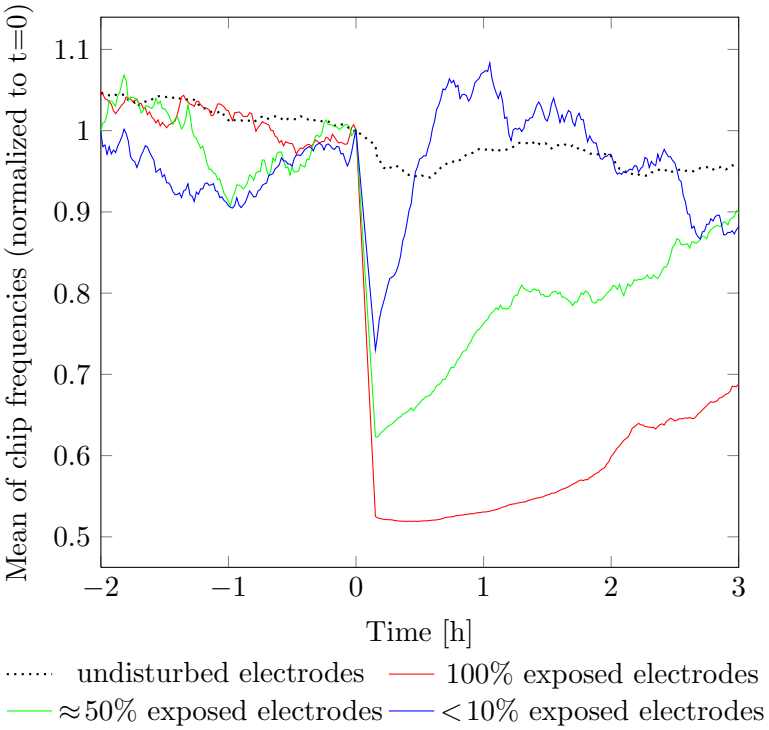

Figure 6.7: Normalized chip frequencies of an experiment where a confluent cell monolayer was deliberately damaged at $t = 0$.

of the impedance-to-frequency converter. The comparator with internal hysteresis used in two of the arrays has a larger effective voltage window ΔV, and this leads to lower output frequencies. In the following plots, the frequency of each electrode will therefore be normalized to its respective value at the start of the experiment, so that this effect is masked and the interesting effects related to the cells can be seen more easily.

Direct Observation of Cell Settling from Suspension

The experiment was started with only 1 ml of medium without cells on the chip and a normal lid without fluidic connections. As can be seen in Figure 6.8, the signals from all electrodes in this period remain stable. Approximately two hours after the start of the experiment, 10^6 V-79 cells suspended in 1 ml DMEM were seeded onto the chip. During the next hour, the frequencies rose as the cells settled from the suspension and attached to the chip. The signals also started to fluctuate strongly about one hour after cell seeding due to the microscopic movements of the cells modulating the measured impedance [31]. These fluctuations, which are only observable in the signals from individual electrodes, can also be interpreted as an indicator of cell health. In a confluent monolayer, approximately ten cells are present on each sensing electrode of 55 µm by 55 µm. With large-area sensing electrodes the effect of the cells' movement would be greatly diminished because the contributions of individual cells would average out [16].

Test of a Provisional Fluidic System

Twenty-four hours after cell seeding, the experiment was briefly interrupted in order to visually confirm the confluence state of the cell layer. Before continuing the experiment, the lid with fluidic connections was placed on the chip. A flexible rubber tube (sterilized with ethanol and flushed with medium beforehand) connected to a peristaltic pump and an external reservoir enabled a continuous renewal of the culture medium. The inlet is located approximately 5 mm above the chip center (see Figure 6.1), while the outlet sits off-center at a higher level. The rubber tube connected to the outlet had a slightly larger diameter than the one used for the inlet, and was placed in the peristaltic pump in the opposite direction, so that the potential outflow was always larger than the inflow. This ensured a constant fluid volume of about 1.5 ml on the chip. The electrode frequencies did not change significantly after the interruption.

At t=27 hours of the experiment, the pump was started at the lowest speed

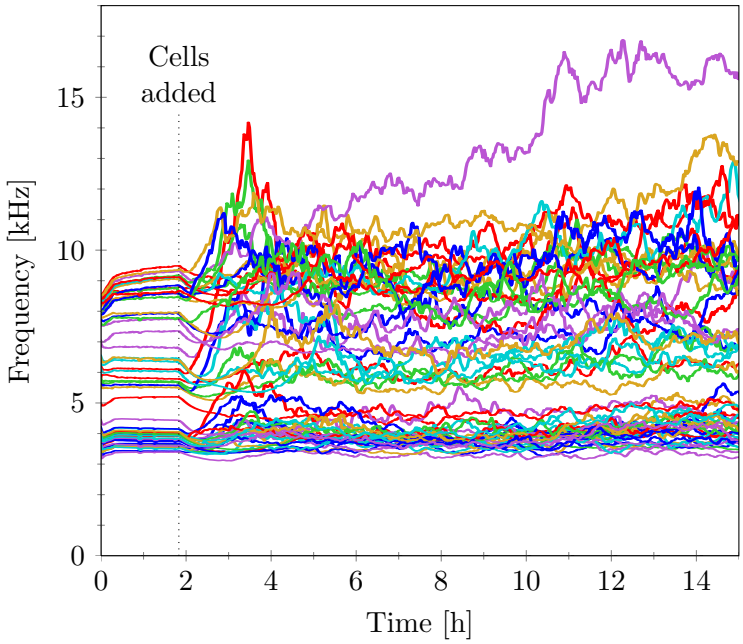

Figure 6.8: Cell settling and spreading on the sensor chip captured with the impedance-to-frequency converter. Each line represents the frequency of one sensing electrode over time.

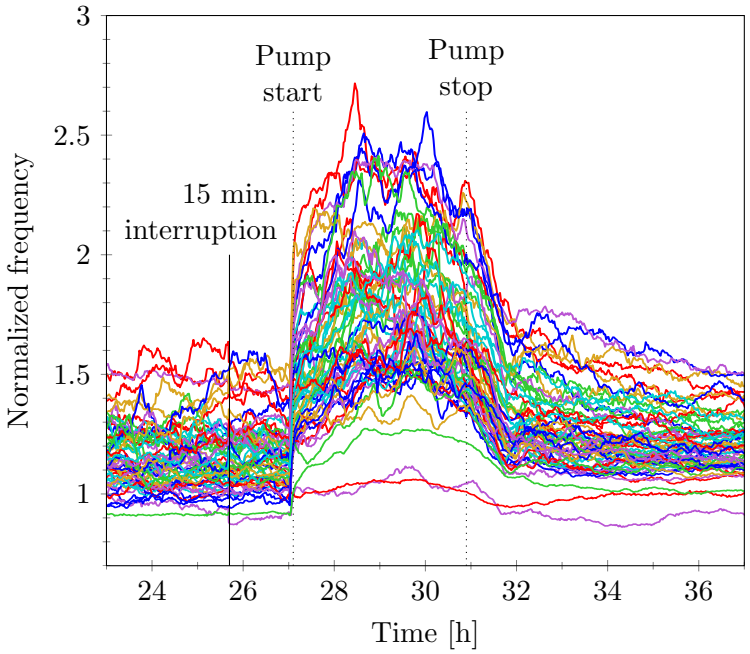

Figure 6.9: Continuation of the experiment in Figure 6.8, showing cell reactions to pump start. In this plot, the electrode frequencies are normalized to their respective values at the start of the experiment.

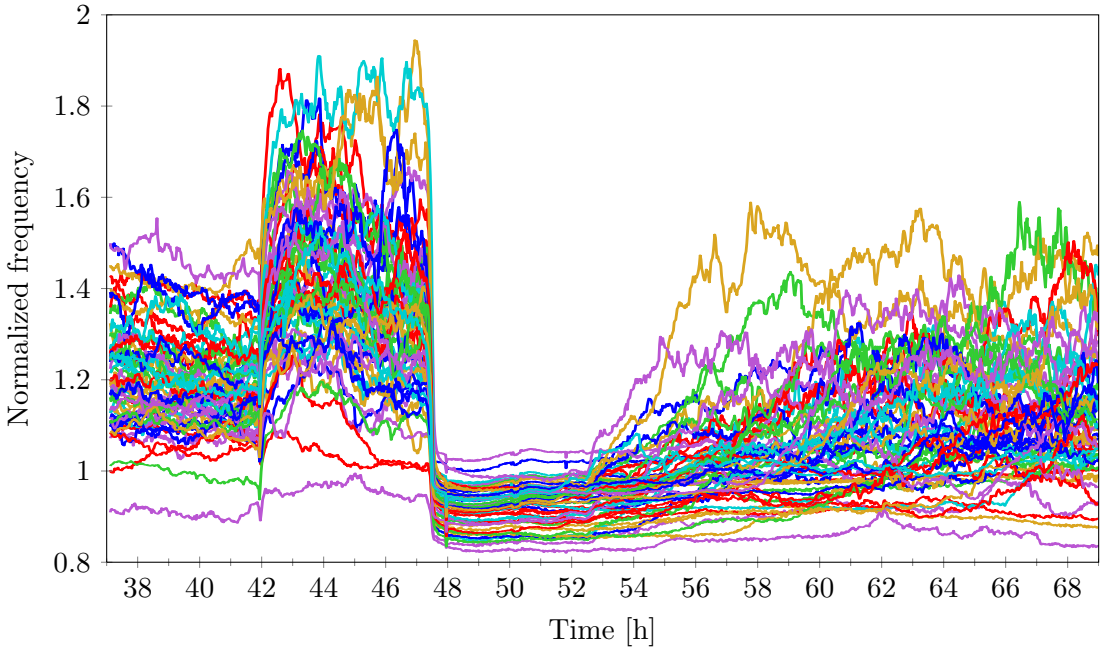

Figure 6.10: Continuation of the experiment in Figure 6.9, showing cell reactions to pump start and cytochalasin D.

setting, corresponding to a flow rate of approximately 11 µl/min. In Figure 6.9, an immediate response of the cells is seen as all frequencies rise, but also the amplitude of the signal fluctuations increases. This reaction is typical for a pump start. Although the supply of fresh medium certainly plays a role, similarly to the effect seen in Figure 6.4, the speed of the reaction suggests that fluidic stress on the cells is also a factor, despite the low flow rate. The cells however seem to cope well with this, as the signal fluctuations continued on a high level during the four hours in which the pump was running. After it was stopped, the frequencies gradually dropped back to the level before the pump start, where they remained stable with a reduced fluctuation amplitude.

Reversible Inhibition of Cellular Micromotion by Cytochalasin

Figure 6.10 shows the continuation of the plot in Figure 6.9. At t=42 hours of the experiment, the pump was started again, causing the same reaction as seen before. At t=45 hours, the medium reservoir was exchanged for DMEM with 10 µM cytochalasin D, a fungal toxin which acts on the cells' actin cytoskeleton, destabilizing them and inhibiting their movement [16]. The time needed for the medium to reach the chip through the tubes had previously been timed as approximately 150 minutes. In good agreement with this value, at t=47.5 hours a drastic drop in impedance, but also the

cessation of the fluctuations were observed. Since the cytochalasin at this time only started to arrive on the chip, and needed much longer to reach its final concentration, it can be concluded that the effect of the cytochalasin saturates at a significantly lower concentration than 10 µM. At t=48 hours, the medium reservoir was changed back to normal DMEM, which reached the chip at approximately 50.5 hours. Two hours later, the concentration of the cytochalasin on the chip had decreased sufficiently that the cells started to recover.

The experiment was continued up to a total running time of 98 hours, with the pump continuously supplying fresh medium to the cells (data not shown). In this time, the signal fluctuations continued on a stable level, proving that the cells can survive on the chip for extended periods. As before, the experiment was finally terminated with 0.2% Triton-X 100.

Quantifying Cellular Micromotion: the Cell Vitality Index

The previous experiment showed that the amount of fluctuation in the signals from individual electrodes is also an indicator of the cells' vitality. For an easier and more consistent interpretation of this parameter, it should be quantified in a single number instead of relying on the visual inspection of plots. A cell vitality index (CVI) is therefore introduced, which is calculated as follows: The chip frequency data is segmented into blocks of N data points (here $N = 40$, corresponding to approximately one hour of the experiment). Within each block, the relative standard deviation of the frequency of each electrode is calculated. The cell vitality index for the k-th block is given by the sum over all electrodes of the relative standard deviations within this block:

$$\mathrm{CVI}[k] = \sum_{\text{electrodes}} \frac{\sigma[k]}{\mu[k]} \tag{6.1}$$

6.2.4 Detection of Hexavalent Chromium as a Practically Relevant Pollutant

The usefulness of the cell vitality index is demonstrated by the results of the following two experiments, in which the cells were exposed to hexavalent chromium, or chromium(VI). This is a toxic and carcinogenic substance which can occur in drinking water supplies mostly due to pollution from industrial sources [8].

In the first experiment, the fluid exchange was done manually with pipettes again. Figure 6.11 shows the output from the integrated impedance sensor as both the average frequency of all electrodes (black line) and the cell vitality

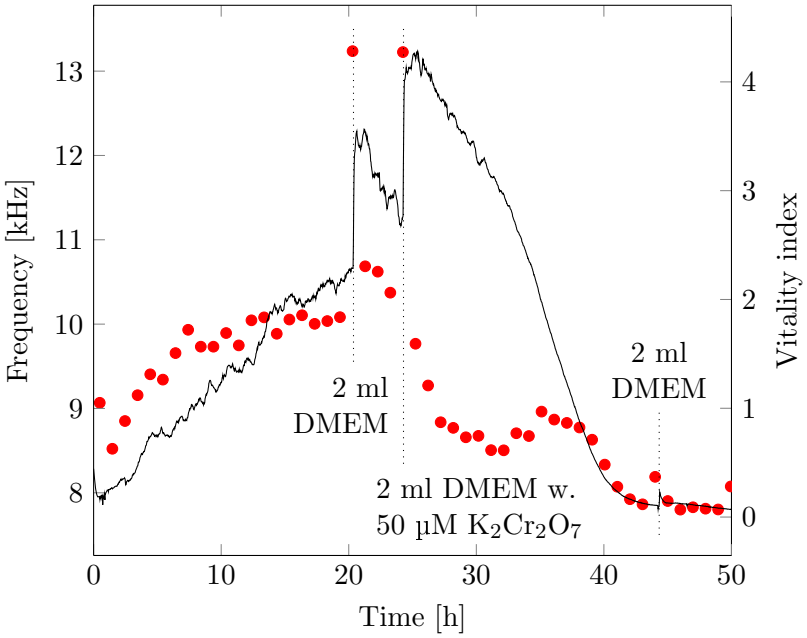

Figure 6.11: Exposure of cells to potassium dichromate. Black line: average output frequency of integrated impedance sensor. Red circles: cell vitality index (see text).

index (red circles). In the beginning, approximately 10^6 V-79 cells suspended in 2 ml medium were seeded on the chip and let grow for about 20 hours. In this time, both the mean output frequency of the circuit and the vitality index rise as the cells spread out and attach to the chip surface, forming a confluent monolayer. However, the vitality index already stabilizes at a value around 2 after ten hours, while the absolute frequency continues to rise. The used medium was then exchanged for 2 ml of fresh DMEM, which causes the typical rise of the average frequency. Interestingly, the vitality index does not increase as much except for one outlier which is a numerical artifact caused by the sudden jump of the absolute frequencies.

After four more hours, the medium on the chip was again exchanged, and 2 ml DMEM containing potassium dichromate ($K_2Cr_2O_7$) at a concentration of 50 µM pipetted onto the chip. In solution, potassium dichromate releases chromium ions in the +6 oxidation state. This chromium(VI) causes oxidative damage to cells [8, 80]. In response, the average frequency first increases, and then starts to fall. This alone at first looks identical to the reaction to the fresh medium. However, the cell vitality index immediately drops to values as low as at the beginning of the experiment, indicating a drastic reduction of the cells' micromotion. In the following hours, the average frequency also falls drastically.

After 20 hours of exposure to chromium(VI), the medium was replaced with pure DMEM again in order to ascertain whether the effect could be reversed. The experiment was continued for 24 more hours (data not shown), but the signals remained stagnant, indicating that the cells had died. This was confirmed by microscopic observations after the end of the experiment, which showed that the cells were rounded and only loosely resting on the chip surface.

The same signal pattern is observed when a continuous fluid exchange introduces the toxic substance so that its concentration rises only gradually. Figure 6.12 shows data from a second experiment, in which the fluidic system described previously was used again. Additionally, the concentration of the potassium dichromate was reduced to 10 µM. Again, 10^6 V-79 cells in 2 ml medium were seeded on the chip at the start of the experiment. The pump was stopped at first, and so the rise of the mean output frequency of the circuit and the vitality index is similar to Figure 6.11. The pump start after 22 hours also causes the same reaction as the manual medium exchange in the previous experiment. At $t \approx 30$ hours, medium with chromium(VI) begins to arrive on the chip, and this causes a decline of the cell vitality index combined with a rise of the mean frequency. The pattern is thus the same as in the previous experiment but the response is more gradual. The mean frequency only begins to fall after 20 hours of exposure to the chromium(VI), presumably because the cells have become so damaged that they die off. The sometimes steep drop of the frequencies also causes an artificial increase of the vitality index during this time.

The results of these two experiments demonstrate that evaluating both the absolute values and the variability of the measured impedance data helps to obtain a more complete picture of the health of the cultured cells. The presence of a toxic substance could therefore be determined quickly and reliably.

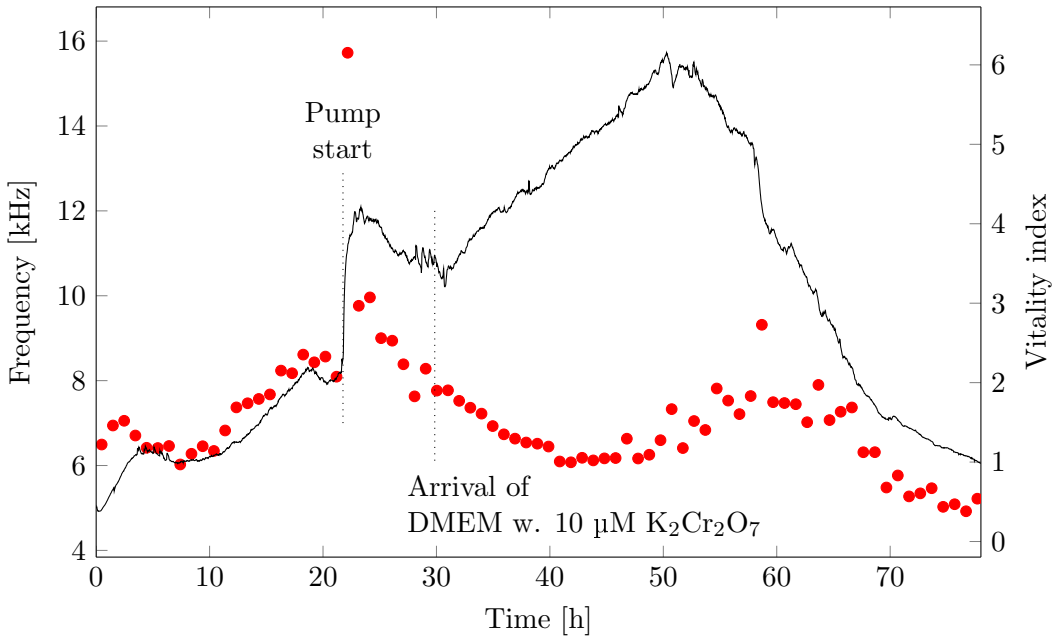

Figure 6.12: Exposure of cells to potassium dichromate with continuous medium exchange. Black line: average output frequency of integrated impedance sensor. Red circles: cell vitality index.

7 Conclusions and Outlook

Living cells acting as detectors of harmful substances in a biosensor have many advantages compared to classical chemical analyses, such as

- a broad spectrum of sensitivity,
- the ability to measure contamination by its bioactivity and bioavailability instead of merely its concentration,
- and relatively low cost.

The evaluation of cell adhesion and movement by impedance measurements can give valuable information about cell reactions and is thus an important element for a water quality biosensor. The cellular impedance has been proven to be a very sensitive and versatile indicator of the state of cultured cells, and can also be continuously measured in real time.

In order to make cell-based sensors viable for decentralized and reliable detection of water pollution, a robust and easy to use assay is required. As a contribution towards this goal, a CMOS integrated impedance sensor for cell adhesion and morphology was developed. Through the integration of the sensor front-end on the chip, the number of required external components and connections is reduced. The implementation of signal amplification and processing close to the sensing site reduces the influence of noise and external interference, so that no dedicated shielding is required. The integration of the sensor circuitry on the same substrate as the electrodes not only has the potential to make the system more compact, robust, and cheaper. It also allows to read out an entire array of measurement positions on the chip without problems due to the large number of external connections this would require with a passive chip. This enables new ways of interpreting the cellular impedance, such as a localized measurement of adhesion and the observation of the microscopic movements of clusters of few cells.

To harness the advantages of CMOS integration for such a sensor, a model of the impedance under study, comprising contributions of the electrode, the electrolyte, and the cells, was developed. Using a combination of analytical and numerical techniques, this allowed predictions of the nature and magnitude of the cellular impedance. For the long-term stability of the sensor electrodes and in order to avoid damaging the cells, it was required to limit the

voltage and current applied to them to safe values. These limits correspond to non-faradaic current transport across the electrode-electrolyte interface, which can then be approximated as a capacitance. Cells have a complex inner structure, which is surrounded by a membrane of phospholipids. Among many other molecules, ion channels facilitating the transport of substances into and out of the cell are embedded into this membrane. All these parts influence the electric properties of the cell as a whole, and different contributions are dominant at different points in the frequency spectrum. For the purpose of measuring cell adhesion, low frequencies are preferable because the impedance of the cell membrane is highest in this range. The cells then present an obstacle to the flow of current through the electrolyte, which manifests as a resistance. However, the impedance of the electrode-electrolyte interface at low frequencies is too large to reliably detect the change caused by cellular adhesion. Based on the model, a suitable frequency window for the measurement of the cellular impedance was determined. The impedance of an entire layer of cells growing on a chip also depends on the layout and size of the electrodes. In order to better understand the influence of these parameters, FEM simulations were performed. It was found that straightforward equations can reproduce the dependence of the measured impedance on these parameters quite well.

Based on the results of the modeling, a measurement principle was chosen which converts the impedance magnitude into a frequency-modulated digital signal. This is achieved by using the impedance of the cell-covered sensing electrode, which can be approximated as a variable resistance in series with a capacitance, as an external element determining the frequency of an oscillator. This impedance-to-frequency conversion principle allows for a straightforward digital readout of cell adhesion data by simply counting pulses of the oscillator output. An analysis of non-ideal effects arising in the implementation of the circuit and their impact on the accuracy of the measurement was conducted. These effects include delays, parasitic capacitance and resistance, leakage currents, mismatch and noise. Taking into account these parasitic effects and the electrochemical limitations of the allowed currents and voltages, design limits were derived for the implementation of the sensor circuitry.

The impedance-to-frequency converter was implemented on a test chip. For this, the constituent circuit blocks were designed and fabricated in a standard CMOS technology. The test chip features 64 sensing sites for cellular adhesion, arranged in arrays of four by four. Each of the 64 electrodes is individually addressable by a digital interface, with the four electrodes in the center also accessible off-chip via a pad for testing and control measurements. The pitch of the sensing electrodes is 155 µm. Two counter electrodes with

an area much larger than the sensing electrodes maintain the electrolyte at an externally-supplied fixed potential. For the cultivation of cells on the chip, its surface had to be biocompatible and chemically inert. A standard silicon nitride passivation of the chip surface was found to be sufficient for the areas between the electrodes. The electrodes on the surface of the chip were fabricated in a back-end lift-off process and consist of a stack of titanium as adhesive layer, followed by platinum as diffusion barrier, and gold as the top layer.

In order to perform experiments with cultured cells, a biocompatible packaging had to be developed. Its function is to enable contact between the cells and the sensing electrodes and at the same time protect the rest of the chip and its connections from the liquid medium. A measurement system suitable for operation inside an incubator was developed as well. Experiments with cells proved the correct function of the sensor chip, including the abilities to detect the settling, growth and death of cells, to provide a localized measurement of cellular adhesion, and to detect cellular responses to various stimuli. The direct comparison of the impedance-to-frequency converter output to the impedance measured with an external LCR meter confirmed that the two are of equal value for the measurement of cellular impedance. However, experiments with substances affecting the motility of cells demonstrated the benefits of measuring the cellular impedance with an entire array of microelectrodes: Since each array position senses the impedance of a cluster of few cells, small changes caused e.g. by microscopic movements of the cells can be detected. By interpreting the amplitude of these changes as an indicator of the cells' health, a new dimension of using cellular impedance to detect harmful substances is gained. The usefulness of quantifying the vitality of the cells in this way was successfully tested by exposing them to hexavalent chromium, which is a pollutant found in real drinking water supplies.

In future work, the development of the cell impedance sensor should be continued to integrate the auxiliary circuits now provided by the measurement board and the PC interface box. A digital interface could capsule the analog parts of the sensor, since direct access to internal nodes like on the test chip will no longer be required, and provide configuration capabilities of its parameters to the outside world. This would also reduce the number of pads on the chip. Integrating other types of sensors on the same chip also is an avenue worth pursuing, especially when a synergy between different parameters can be realized. This could be the case with photodiodes for the detection of bioluminescence. Implementing a photodiode in a CMOS process is straightforward, as it is essentially just a pn-junction with a large area. A bioluminescence sensor would also benefit from CMOS integration, as the

typically very weak signals are highly sensitive to noise and leakage, which can be minimized in an integrated sensor.

In order for a CMOS integrated cell-based biosensor to reach a stage where it is suitable for widespread application, much work is of course also required in areas besides the chip itself, both on the biological side (type of cells, how to culture them, etc. pp.) and the technical side. Focussing only on the latter: As the experiences with the test chip showed, the reliability and long-term stability of the chip has to be improved. This will involve a detailed study of the aging processes and failure modes of electrodes and package under real-world conditions. The overall packaging including the liquid reservoir will also need to be made more compact, and a full fluidic system must be developed. A smaller amount of medium above the chip will also improve the response times of the sensor, since this will increase the rate of fluid exchange. Finally, the interpretation of the data obtained from the cells is certainly an area where much work remains to be done. This will also involve more sophisticated measures than the cell vitality index introduced in this work. The innate variability of the responses of the cells means that there can be no absolute thresholds to distinguish a harmless fluctuation from a significant signal. A statistical approach based on a large body of characterization data will probably be more fruitful.

Appendix: Chip Packaging and Reliability Issues

The packaging of the chip for experiments with liquids and cells proved to be unexpectedly problematic, and faulty bonding or insulation failures are suspected to be the cause of several failed experiments. The following section will therefore summarize the steps performed in the chip packaging from die-substrate attachment to the final assembly with a liquid reservoir, and highlight some of the causes of problems.

Since unpackaged chips are especially sensitive to electrostatic discharges, and dirt or particles on bond pads can lead to incomplete bonding, as a general rule all chip packaging activities were performed in the proper laboratories under clean-room conditions with protective clothing, and with anti-static wrist straps when handling bare chips.

After wafer dicing, the chips were still attached to the dicing tape mounted on a metal frame. The process of preparing a chip for experiments therefore began with carefully lifting it from the tape with anti-static plastic tweezers, making sure to only gently touch the edges of the die, not the surface with the sensitive pads and electrodes. After this, the chip was inspected under a microscope to check for any dirt or visible damage to the electrodes, and if necessary rinsed with isopropanol and deionized water, then blown dry with N_2 gas.

The substrate which the chip was mounted on needed to fulfill several requirements: It needed to offer enough space for the chip dimensions of 2 mm × 4 mm, enough pins to connect all pads on the chip (27 in total, including those for test structures not related to the impedance sensor), and it had to be possible to create a sealed liquid reservoir on top of it. Finally, it should be possible to easily seat it into a socket, especially while the liquid reservoir is filled, in order to facilitate the experiments. This led to the choice of a 64-pin ceramic pin grid array (CPGA) package (*Spectrum Semiconductor Materials*, Part No. CPG06418) with a chip cavity size of .276 in × .276 in (7 mm × 7 mm). This kind of package can be used with a zero insertion force (ZIF) socket, into which the packaged chip can slide effortlessly while keeping the liquid reservoir level. A lever is then closed to secure the chip in the socket. The chip carrier also had to be clean and was therefore preferably taken directly from

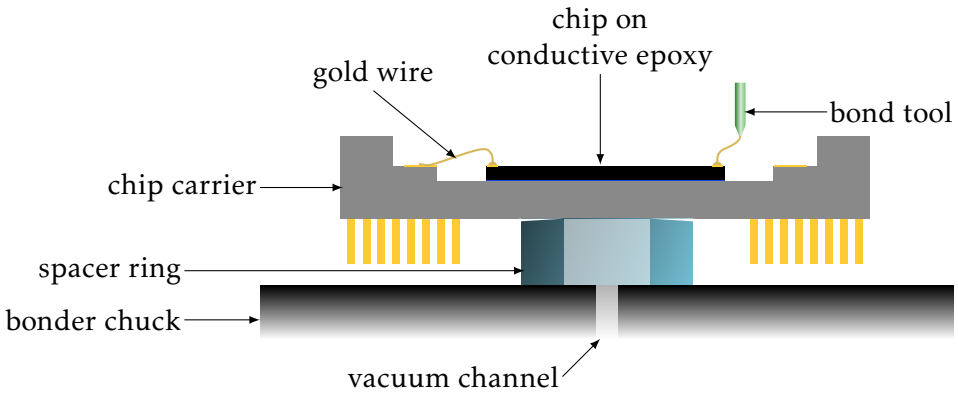

Figure A.1: Schematic illustration of the setup used for wire bonding.

the sealed shipping tray. If the carrier had been exposed to air for prolonged time, it was cleaned in an oxygen plasma. Using an air-powered dispenser and a syringe, a small quantity of conductive adhesive (ME8456, *AI Technology*) was placed into the center of the chip cavity. Then the chip was placed into the center of the cavity with the anti-static tweezers and gently pushed down at the edges to make it sit flat. The adhesive was then cured at 125 °C for two hours.

The electrical connections between the chip and the package were created by wire bonding with a ball/wedge head (*F&K Delvotec* 5610). Normally a vacuum holds the substrate securely to the chuck of the wire bonder, but the pins protruding from the package prevented this. Therefore an aluminum spacer ring was used to create a vacuum seal between the underside of the chip carrier and the chuck, as shown in Figure A.1. The integrated heating of the bonder was set to 120 °C, and the bonds were made with 25 µm gold wire. Unfortunately the bonds were often weak on both the chip and carrier side, which contributed to chip failures later on. The insufficient adhesion may have been caused partially by any residues on the pads, but a major factor was found in a problem with the spacer used in the bond process: Since it had been machined on a lathe, its surfaces sloped slightly downwards, which is shown exaggerated in Figure A.1. This caused the chip carrier to tilt when the bond tool pressed down on it, and therefore no strong joint could be formed. Once this problem was corrected, the strength of the bonds increased.

After wire bonding, the chips were tested electrically for basic functionality. This involved checks of the voltages at the bias current pins, the supply current consumption in active and power-down modes, and the "dry" output frequencies of the circuit across all 64 electrodes. If these tests gave the expected results, the chips were prepared for experiments with liquids and cells. This required first insulating all electrically active parts of the chip

(except the electrodes) in order to prevent contact with the electrolyte and unwanted short-circuits. A biocompatible epoxy resin (Vitralit 1671, *Panacol-Elosol GmbH*) was used for this purpose. It is believed that interactions between this epoxy and the wire bonds caused several chips to fail during experiments, therefore the process of sealing the chips underwent several stages of optimization. Among the suspected failure modes were expansion of the epoxy, possibly due to water absorption, causing bonds to lift off the pads, but also seepage of electrolyte underneath the insulation causing shorts.

The last iteration of the sealing process, which seemed to yield the most reliable chips, was segmented into three steps: First only the bond pads on the chip and the carrier were protected with epoxy, which was dispensed from a syringe using an air-powered dispenser. Due to the previously mentioned low strength of the wire bonds, care was taken not to touch the bond wires with the needle. The duration of the dispensing process also had to be kept as short as possible and the chip quickly transported to the UV lamp for curing, because despite its low viscosity the epoxy slowly spread out and would eventually cover the electrodes. The epoxy was cured under UV light for three minutes, then allowed to fully harden for 24 hours. This first layer of epoxy protected the bonds from mechanical stresses which might occur during later process steps or during experiments.

In the next step of the sealing process, the cavity of the package was filled with epoxy so that the edges of the chip and the bond pads on the chip carrier were completely submerged, thus insulating the chip substrate. The area under the bond wires was first underfilled by moving the needle tip below the bond loops. The epoxy was dispensed until it almost touched the wires. The dispensed epoxy was then again cured under UV light for three minutes. The bond wires were finally completely sealed by dispensing epoxy from above until it completely covered the bond loops, again taking care that the epoxy did not spread across the electrode area. After another round of UV curing and letting them sit for 24 hours, the chips were thus sufficiently insulated to expose their surface to liquids.

However, in order to perform experiments with cells, a closed liquid reservoir was required. It also needed to be large enough to contain sufficient medium to supply the cells for several hours. Finally, the material of the reservoir walls needed to be biocompatible at least in the sense that they would not give off any substance influencing the cells. A suitable base for creating this reservoir was found in polystyrene (PS) Petri dishes. These dishes had a diameter of 35 mm, which is also the approximate diagonal of the chip carrier (see Figure 6.3). A square opening corresponding to the outer cavity of the chip carrier (9 mm × 9 mm) was cut into the bottom of the PS dish with an

infrared laser. In order to attach the reservoir to the chip package, epoxy was dispensed along the edge of the cavity, and the PS dish was then pressed onto the carrier so that the epoxy developed a tight seal between the two parts. The dish was fixed in its position by three minutes of UV curing. Following this, additional epoxy was dispensed along the cavity edge of the carrier and the cutting edge of the dish in order to create a smoother and stronger joint.

The environment during the cell impedance measurements is quite harsh on the chip and its packaging, and so all chips eventually failed after a certain time inside the incubator. The record for the longest endurance was set by a chip which was used in experiments for 15 full (24-hour) days in total, but most chips were used for five to eight days. After a chip failure, a post-mortem analysis was usually done to determine the underlying defect, as far as this was possible. A wire bond failure could be determined in several cases due to a lack of current on normally current-carrying wires (supply, bias), which of course made the chip completely unusable. A failure of one of the digital control signals was less fatal, and became evident due to characteristic patterns in the electrode frequencies: If e.g. the address signal A0 became stuck at '0', every second column in the array would be measured as identical, because only even-numbered electrodes could actually be addressed then (see Figure 5.3). Similarly, a failure of A4 or A5 would cause a vertical or horizontal symmetry of the measured frequencies due to the arrangement of the electrodes in four mirrored arrays. Some chip failures were also due to electrostatic discharge (ESD), which could be determined by unusually high currents on the affected connections. Full ESD protection structures had been placed on all digital pads on the chip to prevent this, and the analog pads also had rudimentary ESD protection (leakage and space restrictions prevented the use of full protection structures there), but obviously this could not prevent ESD damage in all cases. Table A.1 gives a summary of the causes of chip failure as far as they could be determined. The numbers highlight the need for further work on a reliable packaging process and research on the degradation mechanisms affecting the insulation and the electrodes.

Table A.1: Summary of the causes of chip failures. Number ranges reflect cases where the underlying defect could not be determined with sufficient certainty.

Total number of chips packaged	24
– Failure after epoxy sealing	4
– Rejected or used for other experiments	7
Number of chips used in cell impedance experiments	13
Later failure due to ...	
– electrostatic discharge damage	1
– bond failure	3–7
– insulation failure	2–5
Failure of individual electrodes during experiments	3

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Symbol	Value / Unit	Description
A	$\Omega\,\mathrm{cm}^2\,\mathrm{s}^{-\alpha}$	Real part coefficient of the electrode-electrolyte interface polarization impedance Z_p
a	µm	Sensing electrode edge length
A_{el}	cm^2	Sensing electrode area ($A_{el} = a^2$)
B	$\Omega\,\mathrm{cm}^2\,\mathrm{s}^{-\beta}$	Imaginary part coefficient of the electrode-electrolyte interface polarization impedance Z_p
c	$\mathrm{mol\,L}^{-1}$	Molar concentration
C_{cells}	$\mathrm{F\,cm}^{-2}$	Capacitive part of the cell layer impedance Z_{cells}
C_m	$\mathrm{F\,cm}^{-2}$	Cell membrane capacitance
C_{el}	F	Total capacitance of the electrode ($C_{el} = A_{el}C_p$)
C_{ox}	$\mathrm{F\,cm}^{-2}$	MOSFET gate oxide capacitance ($C_{ox} = \frac{\epsilon_{ox}\epsilon_0}{t_{ox}}$)
C_p	$\mathrm{F\,cm}^{-2}$	Capacitive part of the polarization impedance of the electrode-electrolyte interface
C_{par}	F	Parasitic capacitance, e.g. wiring and transistor gate capacitances
d	µm	Distance between electrodes
E_g	1.12 eV	Band gap energy of silicon
f	s^{-1}	Frequency
f_{out}	s^{-1}	Output frequency of the impedance-to-frequency converter ($f_{out} = \frac{1}{\tau_{out}}$)
$f_{out,idle}$	s^{-1}	Output frequency of the impedance-to-frequency converter when R_{el} is negligible

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Symbol	Value / Unit	Description
h	µm	Height of the cell-substrate gap
i	$\sqrt{-1}$	Imaginary unit
I_0	nA	Magnitude of the current sourced/sunk by the electrode current generator
I_D	A	Diode current
I_{ds}	A	MOSFET drain-to-source current
I_{el}	nA	Total current actually flowing through the electrode
I_f	nA	Faradaic current across electrode-electrolyte interface
I_{leak}	nA	Loss of current between source and electrode due to leakage
I_{offset}	nA	Deviation of the current generated by the sources from the intended value I_0
I_S	A	Diode saturation current
j_0	$\mathrm{A\,cm^{-2}}$	Exchange current density of electrode-electrolyte interface
j_f	$\mathrm{A\,cm^{-2}}$	Faradaic current density across electrode-electrolyte interface
K	$\mathrm{\mu A\,V^{-2}}$	Current gain factor of a MOS transistor, given by $\mu_{eff} C_{ox} \frac{W}{L}$. The product $\mu_{eff} C_{ox}$ can also be substituted by K'_N or K'_P for an N- or P-MOSFET, respectively.
k_B	$1.3807 \cdot 10^{-23}\,\mathrm{J\,K^{-1}}$	Boltzmann constant
L	µm	MOSFET gate length
N_A	$6.0221 \cdot 10^{23}\,\mathrm{mol^{-1}}$	Avogadro constant
N_{ch}	$\mathrm{cm^{-3}}$	MOSFET channel doping concentration
n_i	$1.45 \cdot 10^{10}\,\mathrm{cm^{-3}}$	Intrinsic carrier concentration of silicon (at 300 K)
q	$1\,\mathrm{e} = 1.6022 \cdot 10^{-19}\,\mathrm{C}$	Elementary charge
r	m	Radial coordinate
R_c	Ω	Intracellular resistance

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Symbol	Value / Unit	Description
r_c	µm	Unit cell radius in the Giaever and Keese [17] model
R_{cells}	$\Omega\,\mathrm{cm}^2$	Resistive part of the cell layer impedance Z_{cells}
R_{ct}	$\Omega\,\mathrm{cm}^2$	Charge transfer resistance (linearized description of current due to redox reactions at the electrode)
R_{cl}	Ω	Resistance of the cell layer directly above and in the immediate vicinity of the electrode. Scaled by the electrode area in the two-dimensional model: $R_{cl} = \frac{R'_{cl}}{A_{el}}$
r_e	µm	Electrode radius
R_{el}	Ω	Total electrode series resistance, including contributions of the electrode (R_p), electrolyte (R_s) and cells ($R_{cl} \| R_{gap}$). Equivalent to $\mathrm{Re}\left(\frac{Z_{cov}}{A_{el}}\right)$
R_{gap}	Ω	Resistance due to current constriction underneath the cell layer
R_m	$\Omega\,\mathrm{cm}^2$	Cell membrane resistance
R_p	$\Omega\,\mathrm{cm}^2$	Resistive part of the polarization impedance of the electrode-electrolyte interface
R_{par}	Ω	Parasitic resistance due to wiring and switch on-resistance
R_s	Ω	Spreading resistance of electrolyte
T	K	Absolute temperature, in calculations 300 K (ca. 27 °C) unless noted otherwise
t_{delay}	s	Sum of the switching delays effective during one period τ_{out}
$V_{counterEl}$	V	Voltage at the counter electrode
V_{DD}	3.3 V	Nominal supply voltage in the target technology
V_{ds}	V	MOSFET drain-to-source voltage
V_{el}	V	Voltage at the sensing electrode

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Symbol	Value / Unit	Description
V_{err}	V	Error in the switching level of a comparator due to its delay t_d
V_{gs}	V	MOSFET gate-to-source voltage
V_m	V	Potential of the bulk medium far away from the electrodes
V_{offset}	mV	Comparator input offset voltage
$\mathsf{V}_{\mathsf{out}}$	V	Comparator output signal
V_{refH}	V	Upper reference voltage for comparator
V_{refL}	V	Lower reference voltage for comparator
V_t	V	Effective threshold voltage of a MOSFET, including body effect, statistical variation, etc.
V_{t0}	V	MOSFET nominal threshold voltage
W	µm	MOSFET gate width
z		Ionic valence
Z_{CPE}	$\Omega\,\mathrm{cm}^2$	Constant phase element model of the electrode-electrolyte interface impedance
Z_{cells}	$\Omega\,\mathrm{cm}^2$	Impedance of a confluent cell layer, modeled as a parallel RC element of R_{cells} and C_{cells}
Z_{cov}	$\Omega\,\mathrm{cm}^2$	Combined impedance of the electrode and the cells covering it
Z_i	$\Omega\,\mathrm{cm}^2$	Total impedance of the electrode-electrolyte interface, in general Z_p in parallel with R_{ct}
Z_m	$\Omega\,\mathrm{cm}^2$	Impedance of a cell membrane, usually described by its specific capacitance C_m, and optionally by a parallel resistance R_m
Z_p	$\Omega\,\mathrm{cm}^2$	Polarization impedance of the electrode-electrolyte interface
α		Frequency exponent of the real part of the electrode-electrolyte interface polarization impedance Z_p

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Symbol	Value / Unit	Description
β		Frequency exponent of the imaginary part of the electrode-electrolyte interface polarization impedance Z_p
ΔV	mV	Nominal voltage window of the sensing electrode: $\Delta V = V_{refH} - V_{refL}$
ΔV_{offset}	mV	Deviation of ΔV from the nominal value due to comparator offsets
ϵ_0	$8.8542 \cdot 10^{-12}\,\mathrm{F\,m^{-1}}$	Vacuum permittivity
ϵ_{ox}	3.9	Dielectric constant of silicon oxide
ϵ_{Si}	11.9	Dielectric constant of silicon
η	V	Overpotential (Deviation from the equilibrium potential of an electrode)
μ_0	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$	Carrier low-field surface mobility at nominal temperature
μ_{eff}	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$	Effective carrier mobility
π	3.14159...	Ratio of the circumference of a circle to its diameter
ρ	$\Omega\,\mathrm{cm}$	Electrical resistivity (inverse of conductivity κ) of a material
σ_X		Standard deviation of a random variable X, defined as the square root of its variance: $\sigma_X = \sqrt{\mathrm{Var}(X)}$
τ_{out}	s	Period of impedance-to-frequency converter output
$\tau_{out,ideal}$	s	Period of impedance-to-frequency converter output, neglecting all non-ideal effects
$\Phi 1$, $\Phi 2$		Signals controlling the switches for charging ($\Phi 1$) and discharging ($\Phi 2$) the electrode
ω	$\mathrm{rad\,s^{-1}}$	Angular frequency, $\omega = 2\pi f$
$\mathcal{I}_n$		Modified Bessel function of the first kind of order n

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Symbol	Value / Unit	Description
$\mathcal{K}_n$		Modified Bessel function of the second kind of order n

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