Evaluation of Cache Contention Prediction Techniques: Further Results and Plots

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Abstract

This technical report presents further results and plots considering my dissertation entitled *Predicting Cache Contention in Multicore Processor Systems*, submitted to the Technische Universität München in November 2010. It presents information regarding

- memory access time degradation caused by application co-scheduling,
- distributions of NMRD (normalized mean ranking difference), MP (mean penalty), PPBAB (penalty predicted best vs. actual best), and PPBRS (penalty predicted best vs. random assignment) values,
- NMRD, MP, PPBAB, PPBRS and gain vs. cost average values for modified memory access and cache hit times, and
- execution time for various interval sizes $\mathcal{F}$ and various amounts of parallelism ψ.

For terms, symbols and abbrevations see the dissertation; a notation summary is presented in the appendix of the dissertation, section 'List of Symbols and Abbrevations'.

Note that I refer to 2^{20} instructions as 1 million instructions. In the following, I refer to the mentioned dissertation simply as "thesis".

1 Memory Access Time Degradation

Figure 1 presents memory access time degradation for all possible co-schedule combinations in case $\psi = 2$ processor cores, measured in percent of stand-alone memory access time. The figure reveals that there are application combinations that show only little (e.g. $a =$ gobmk, $C_a = \{\text{astar}\}$) or even none ($a =$ lbm) degradation, while there are also combinations that show significant memory access time degradation, e.g. $a =$ milc, $C_a = \{\text{lbm}\}$.

Generally, performance degradation might be much more significant if modelling would include waitstates introduced by busy resources; in the thesis, such waitstates are not considered (see section 1.3, part "Limitations"). Further degradation will be introduced if not only L2 caches are shared, but if also L1 caches are shared, as it can often be observed in SMT processor design. Note, however, that I chose an architecture that exclusively shares L2 caches in order to keep ground truth measure close to prediction models, as most state-of-the-art cache contention prediction techniques exclusively rely on (stand-alone) L2 cache stack distance histograms to predict L2 cache contention. Architectures additionally sharing L1 data caches would incorporate unmodelled effects overlaying L2 cache contention and therefore introduce inaccuracies.

a \ C_a	{astar}	{bzip2}	{gcc}	{gobmk}	{h264ref}	{hmmer}	{lbm}	{mcf}	{milc}	{povray}
astar	n/a	2.29	1.53	6.11	0.18	0.16	8.55	4.40	6.77	0.16
bzip2	1.61	n/a	3.61	6.90	0.42	0.40	13.14	7.58	8.40	0.68
gcc	1.94	5.92	n/a	7.90	0.35	0.15	12.94	7.85	8.70	0.39
gobmk	0.10	0.27	0.15	n/a	0.05	0.02	0.75	0.48	0.48	0.05
h264ref	0.07	0.26	0.14	1.14	n/a	0.00	1.29	0.75	0.72	0.03
hmmer	0.04	0.20	0.03	2.13	0.00	n/a	4.86	1.40	1.10	0.01
lbm	0.00	0.00	0.00	0.00	0.00	0.00	n/a	0.00	0.00	0.00
mcf	2.06	6.36	2.67	7.25	0.66	0.77	12.72	n/a	10.17	0.75
milc	8.53	15.60	8.69	23.11	1.83	2.59	32.84	22.34	n/a	2.07
povray	0.10	0.68	0.25	1.19	0.03	0.01	2.35	0.99	1.02	n/a

Figure 1: Memory access time degradation [% stand-alone memory access time].

2 Distribution of Evaluation Results

2.1 Normalized Mean Ranking Difference

In the thesis, section 3.2, figure 24, I apply NMRD (normalized mean ranking difference) values to evaluate accuracy of cache contention prediction techniques. The presented values are mean values only, averaged over all possible combinations of candidate co-schedules. In the following plots, i.e. figures 2 to 10, I present correspsonding NMRD *distributions* for all possible candidate co-schedules. Ticks located at the *inside* of the abscissa of each plot determine sampling points, i.e. the set of all possible NMRD values for a given number of processor cores ψ and the corresponding number of candidate co-schedules $|\mathbf{C}_a^\psi|$ respectively. Note that the ordinate plots frequencies greater or equal to 1 in logarithmic scale; ordinate value 0 is plotted out of scale and indicates non-occuring NMRD values. Regarding the plots, you can observe that methods that achieve high NMRD average performance (e.g. *Prob*) provide distributions that settle down much faster than NMRD distributions of low performing prediction methods (e.g. *FOA*, variation *one*).

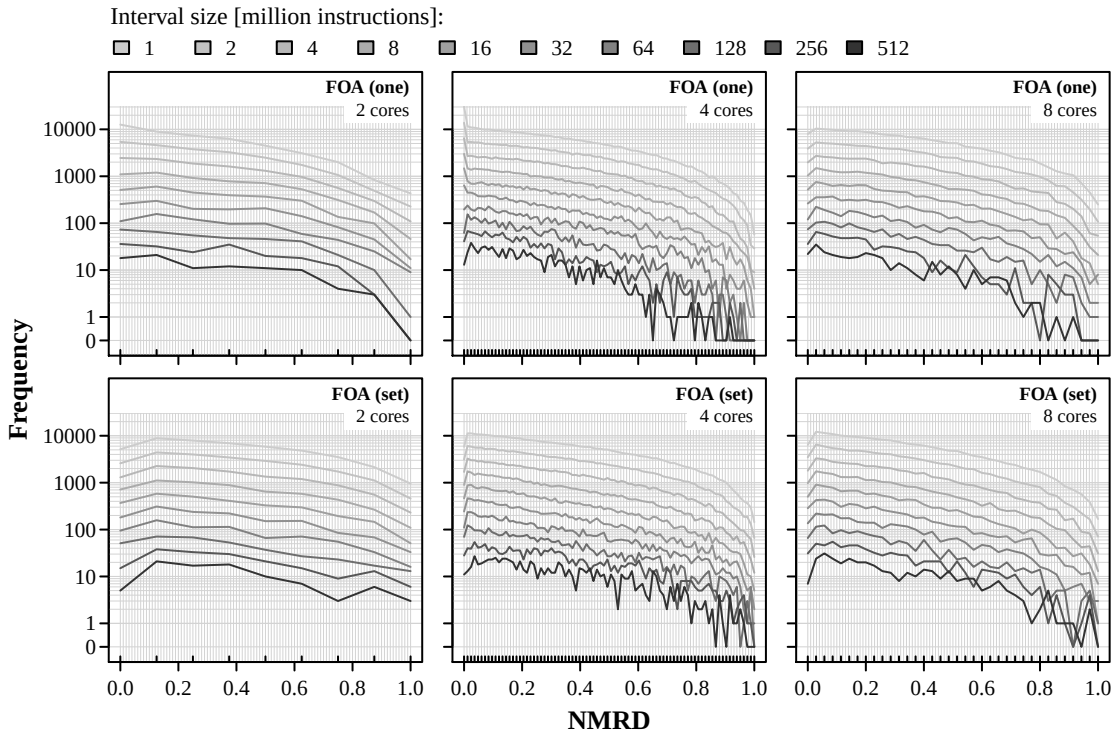

Figure 2: NMRD distribution (part 1 of 9).

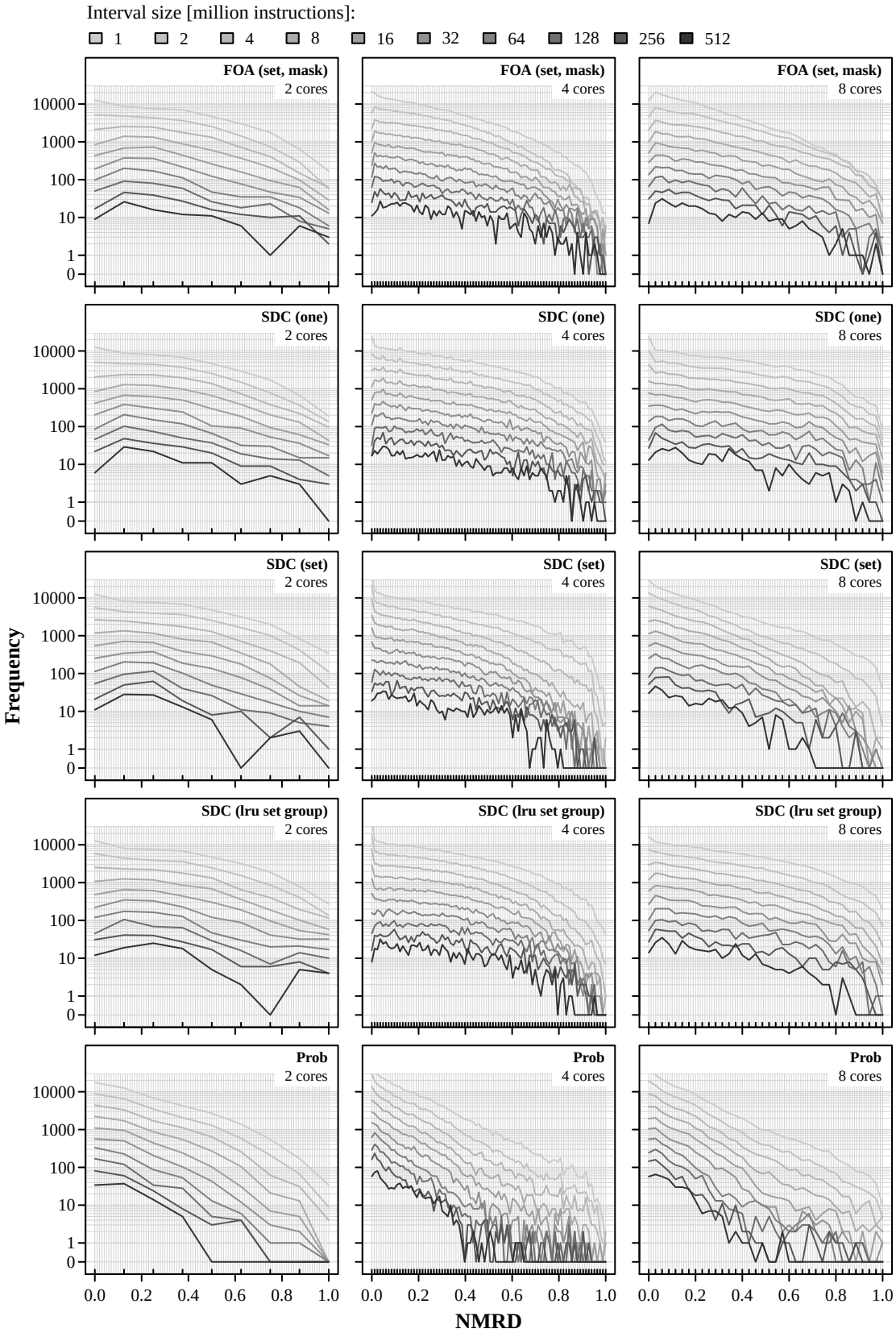

Figure 3: NMRD distribution (part 2 of 9).

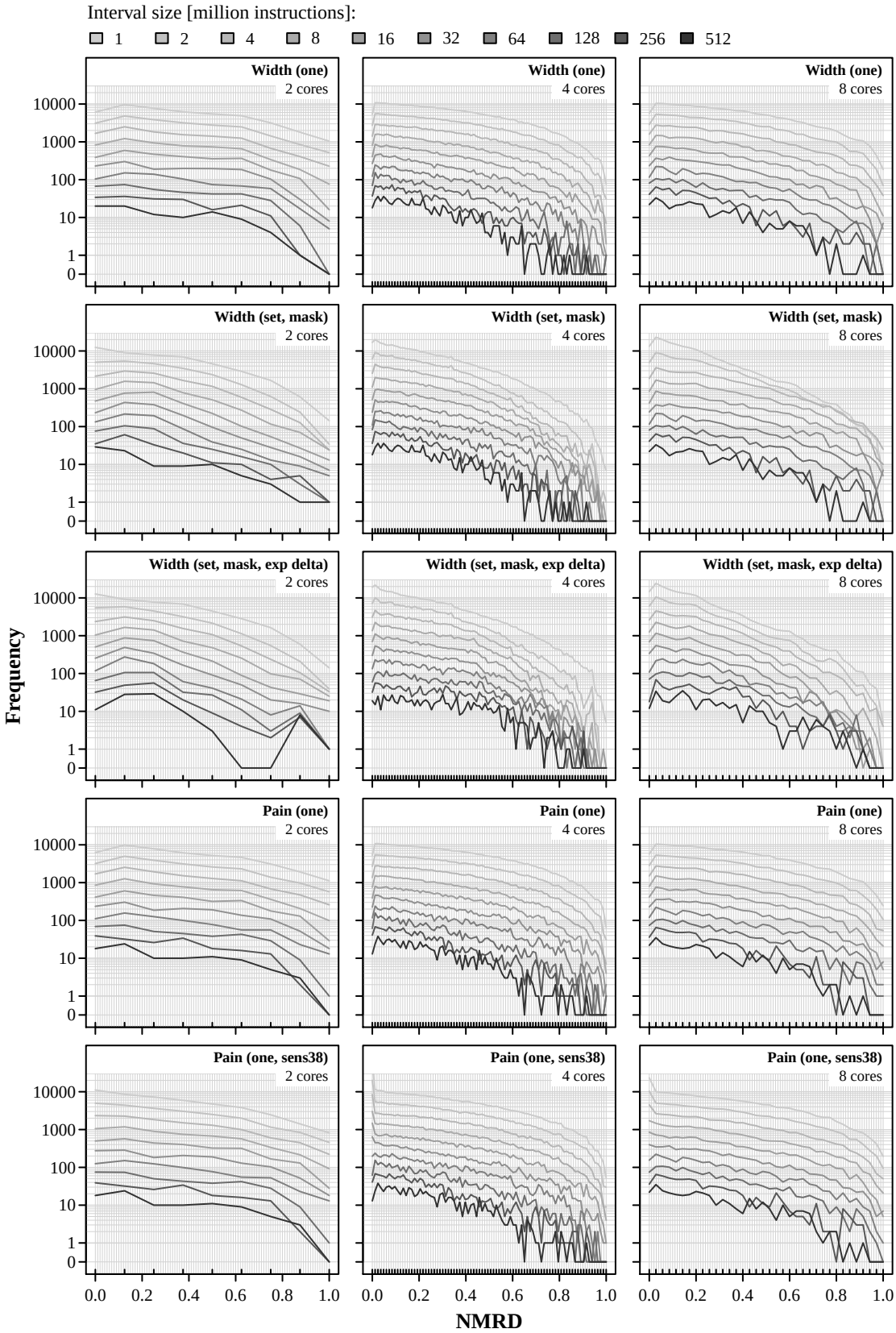

Figure 4: NMRD distribution (part 3 of 9).

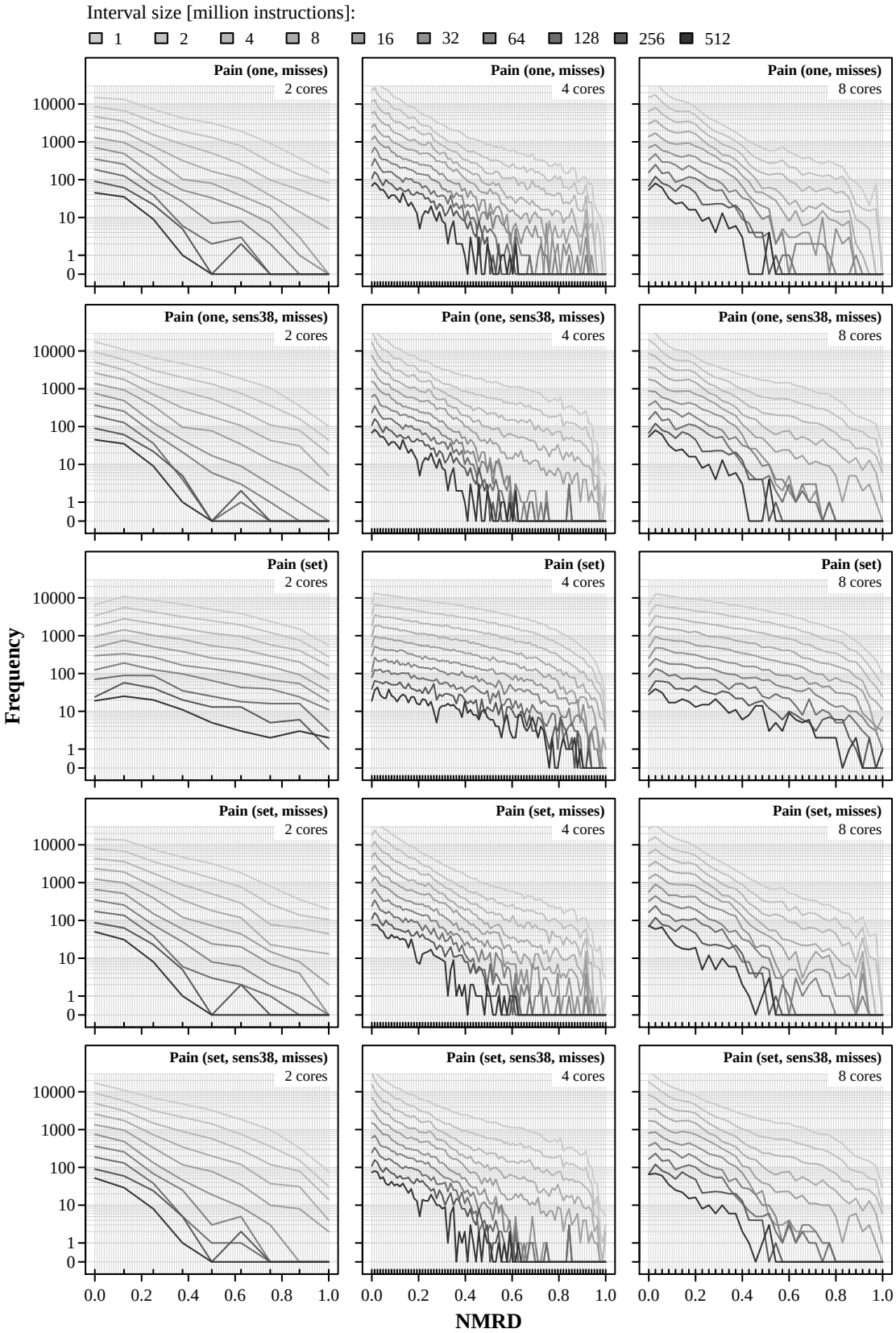

Figure 5: NMRD distribution (part 4 of 9).

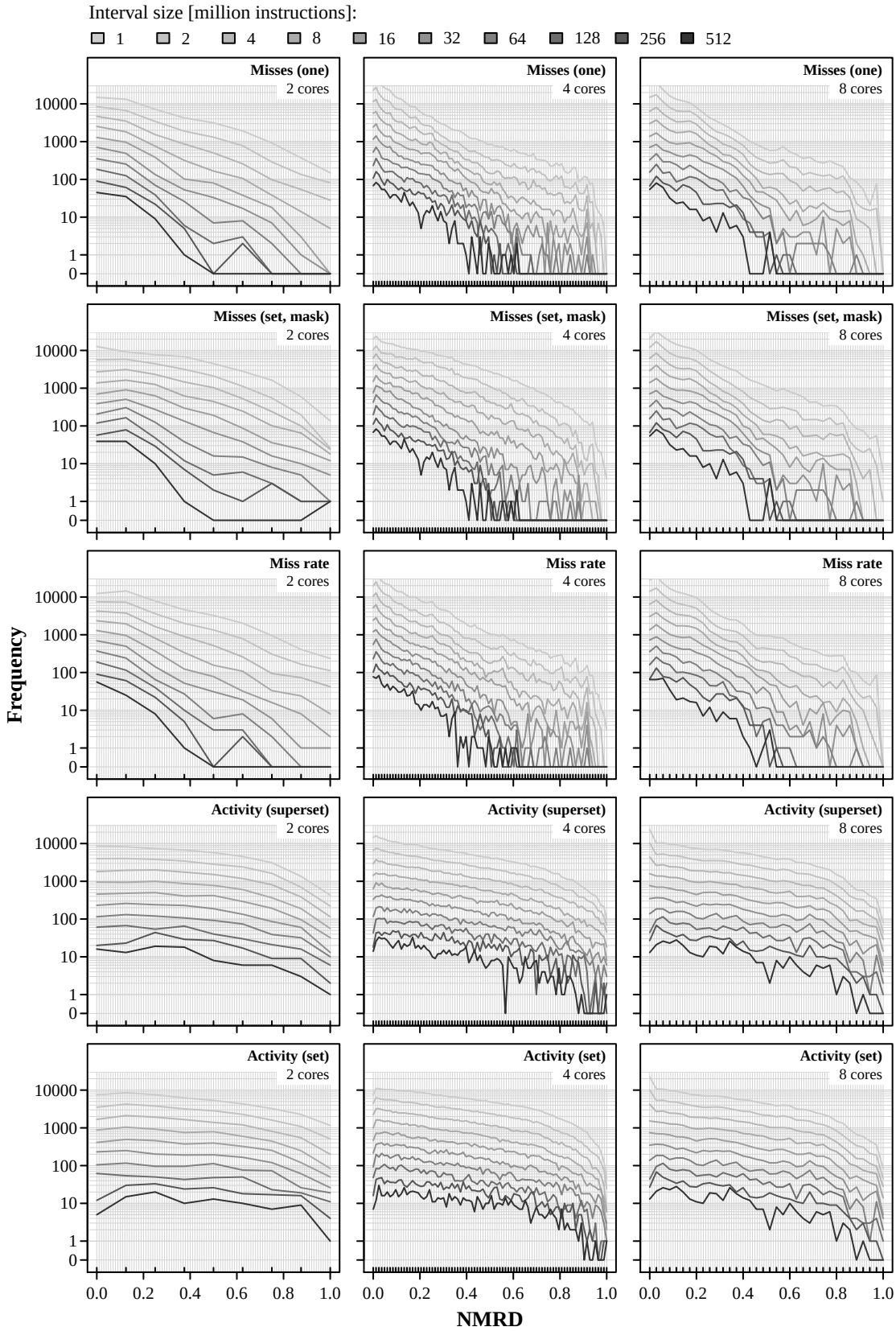

Figure 6: NMRD distribution (part 5 of 9).

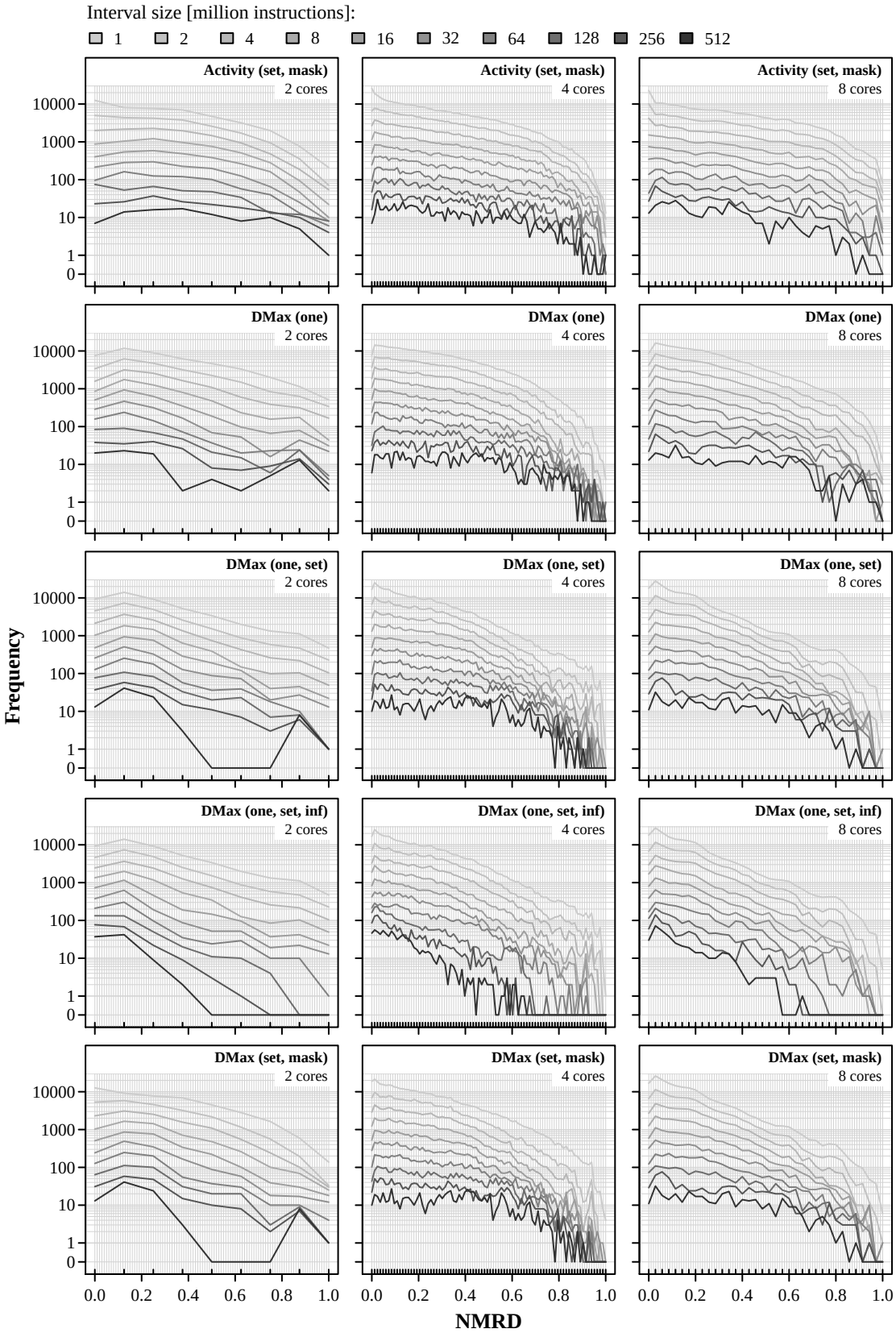

Figure 7: NMRD distribution (part 6 of 9).

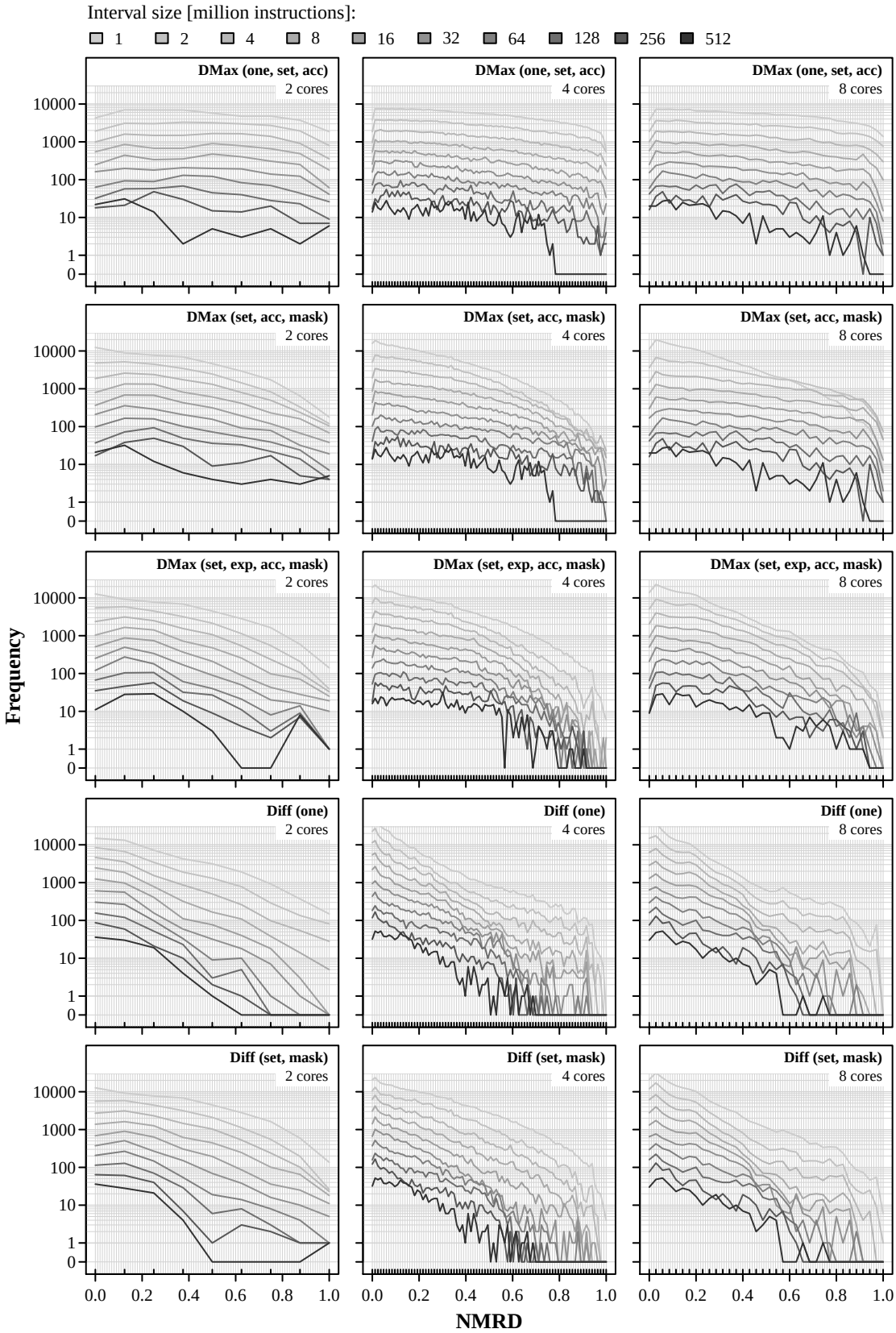

Figure 8: NMRD distribution (part 7 of 9).

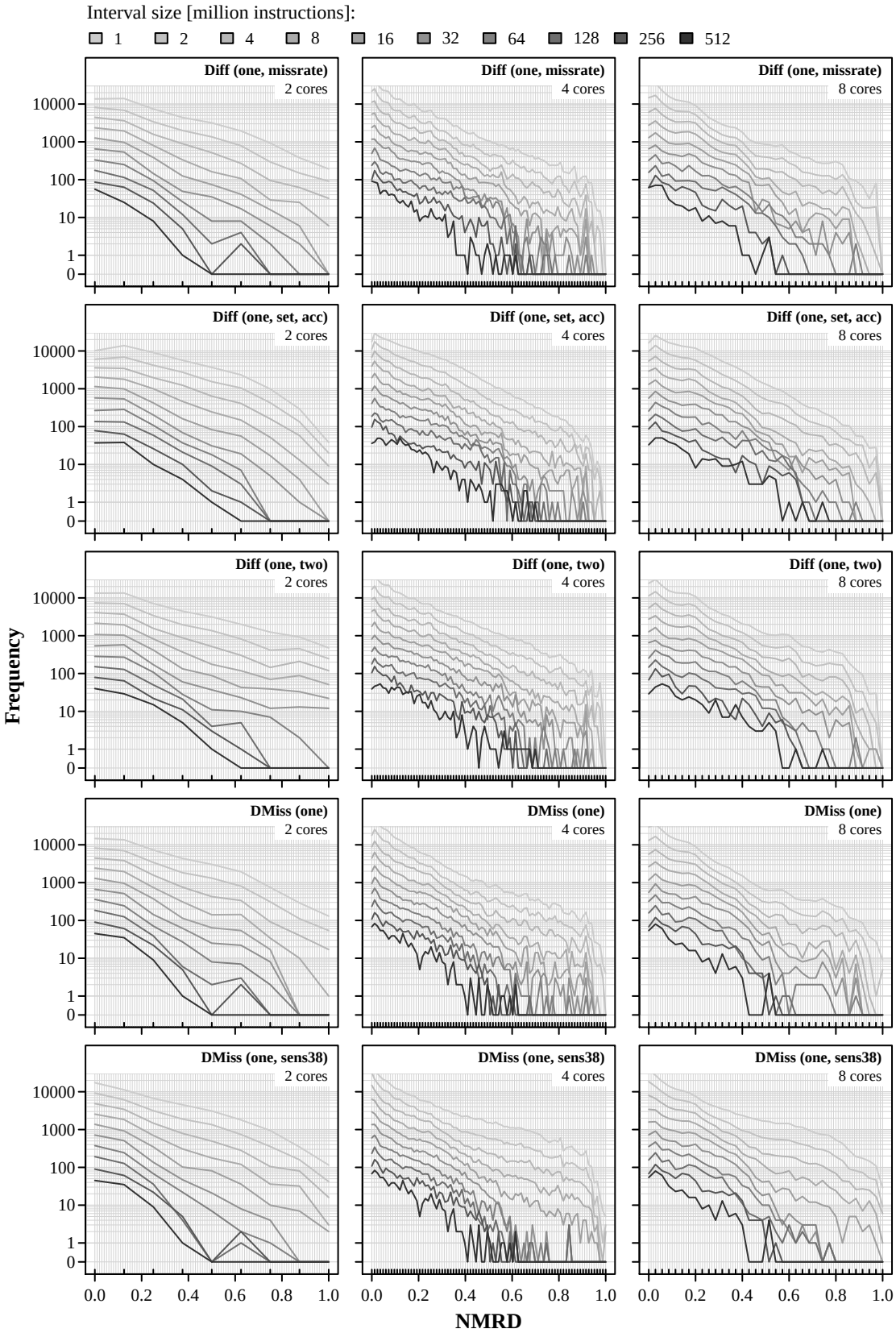

Figure 9: NMRD distribution (part 8 of 9).

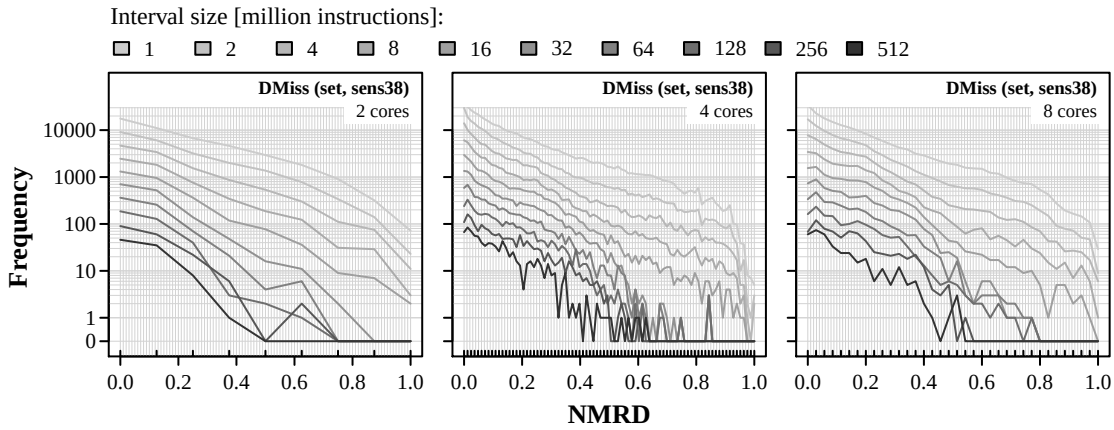

Figure 10: NMRD distribution (part 9 of 9).

2.2 Mean Penalty

Figures 12 to 19 present Mean Penalty (MP) distributions for MP average values presented in the thesis, section 3.2, figure 31. Ticks on the abscissa that reside at the *inside* of each plot determine sampling intervals. Figure 11 shows how each point in these plots maps to frequency of mean penalties in a specific interval.

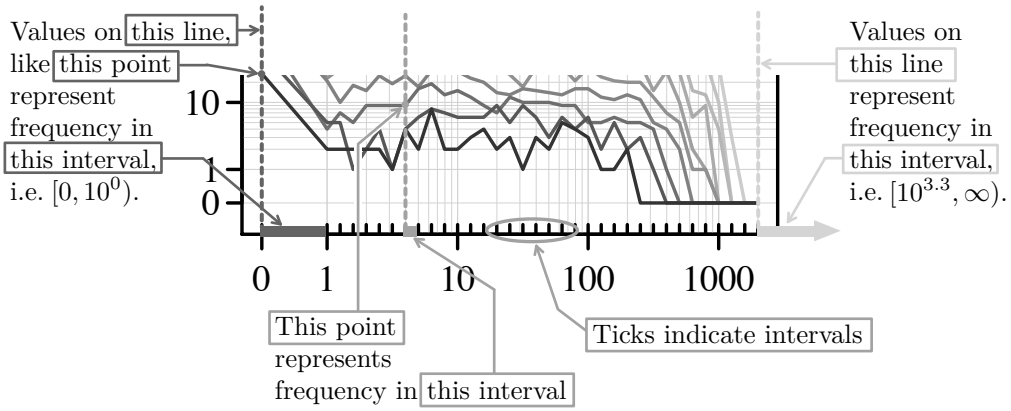

Figure 11: Mean Penalty (MP) distribution glossary as presented in the thesis.

Values ≥ 1 are plotted in logarithmic scale; value 0 is plotted out of scale.

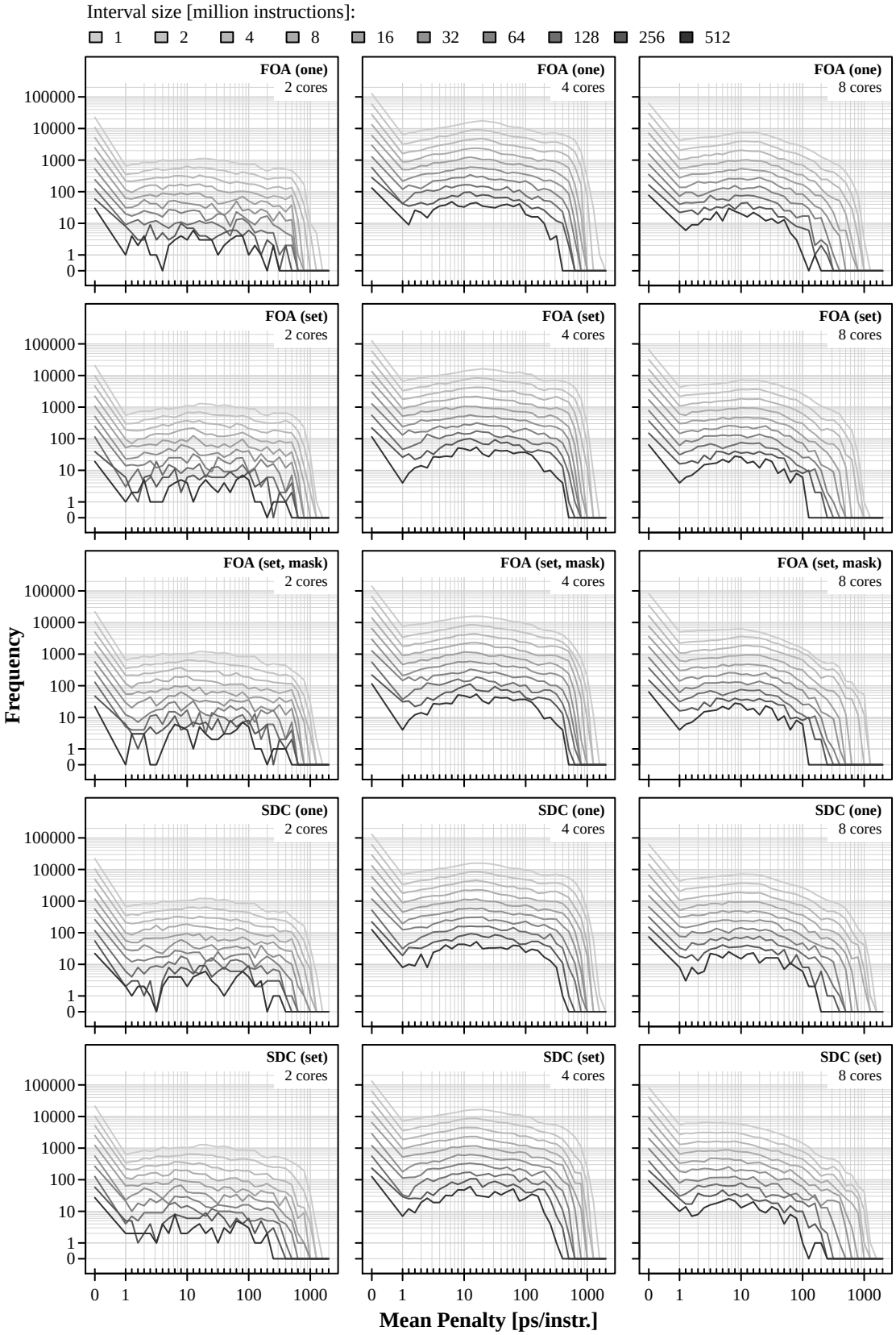

Figure 12: Mean Penalty distribution (part 1 of 8).

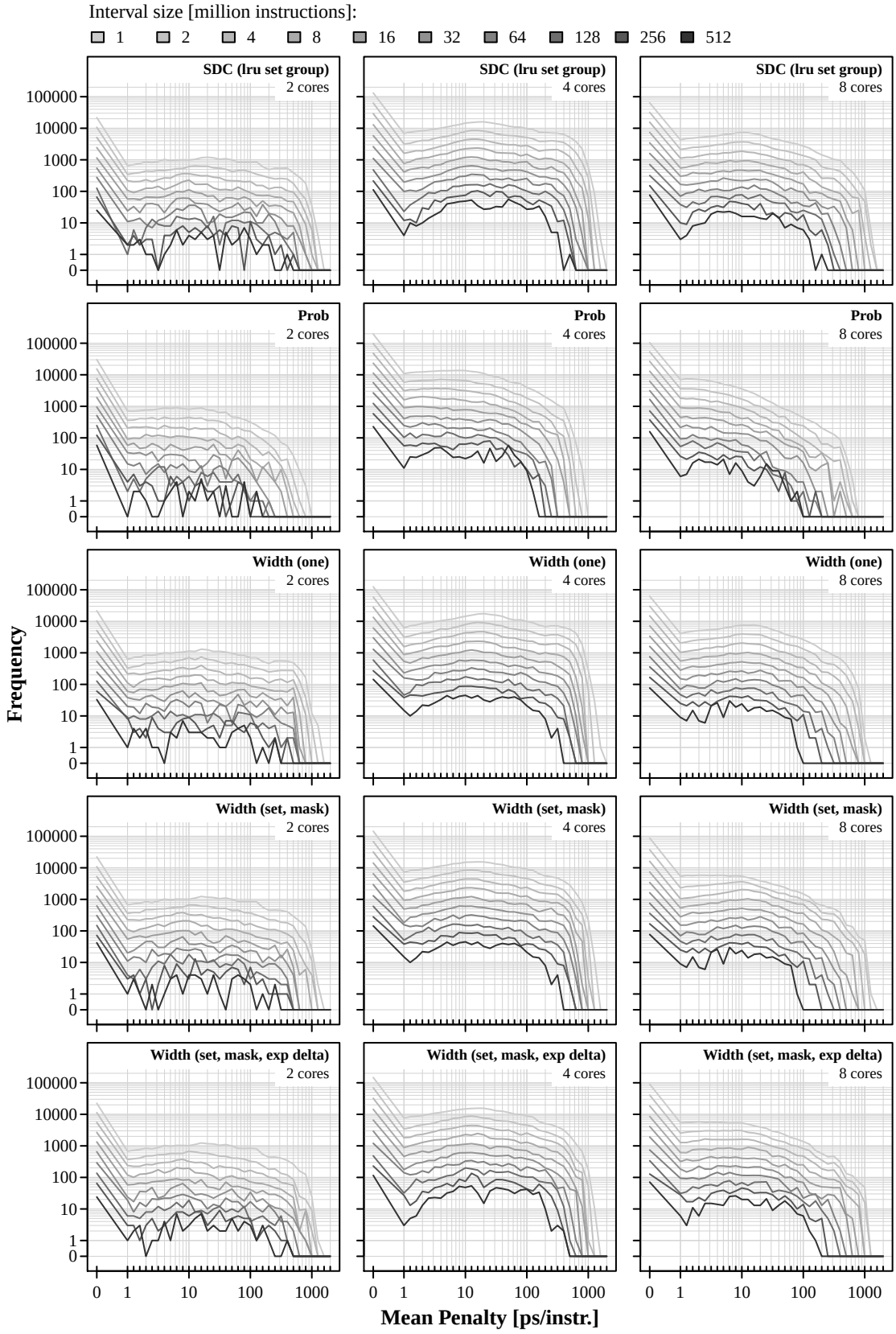

Figure 13: Mean Penalty distribution (part 2 of 8).

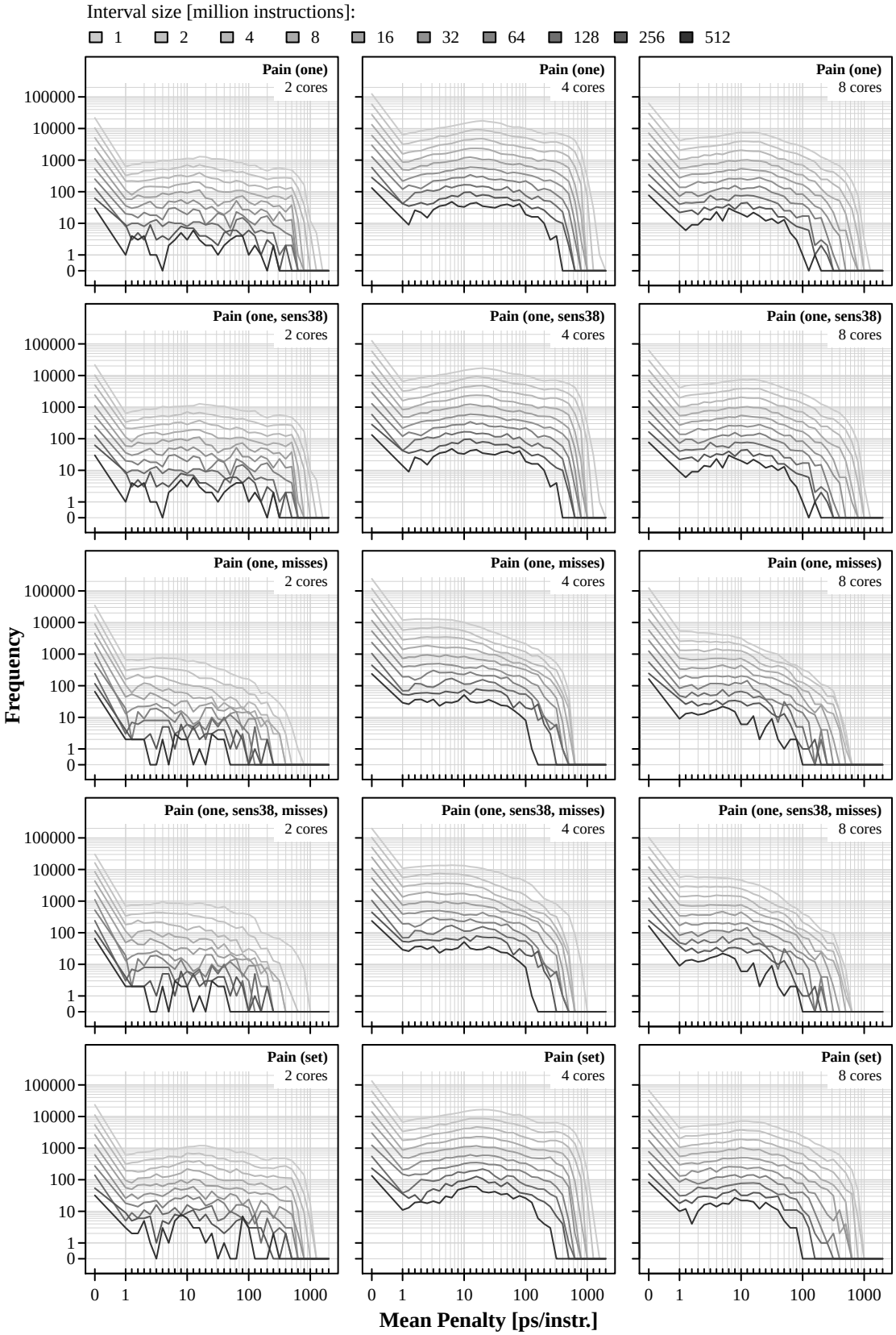

Figure 14: Mean Penalty distribution (part 3 of 8).

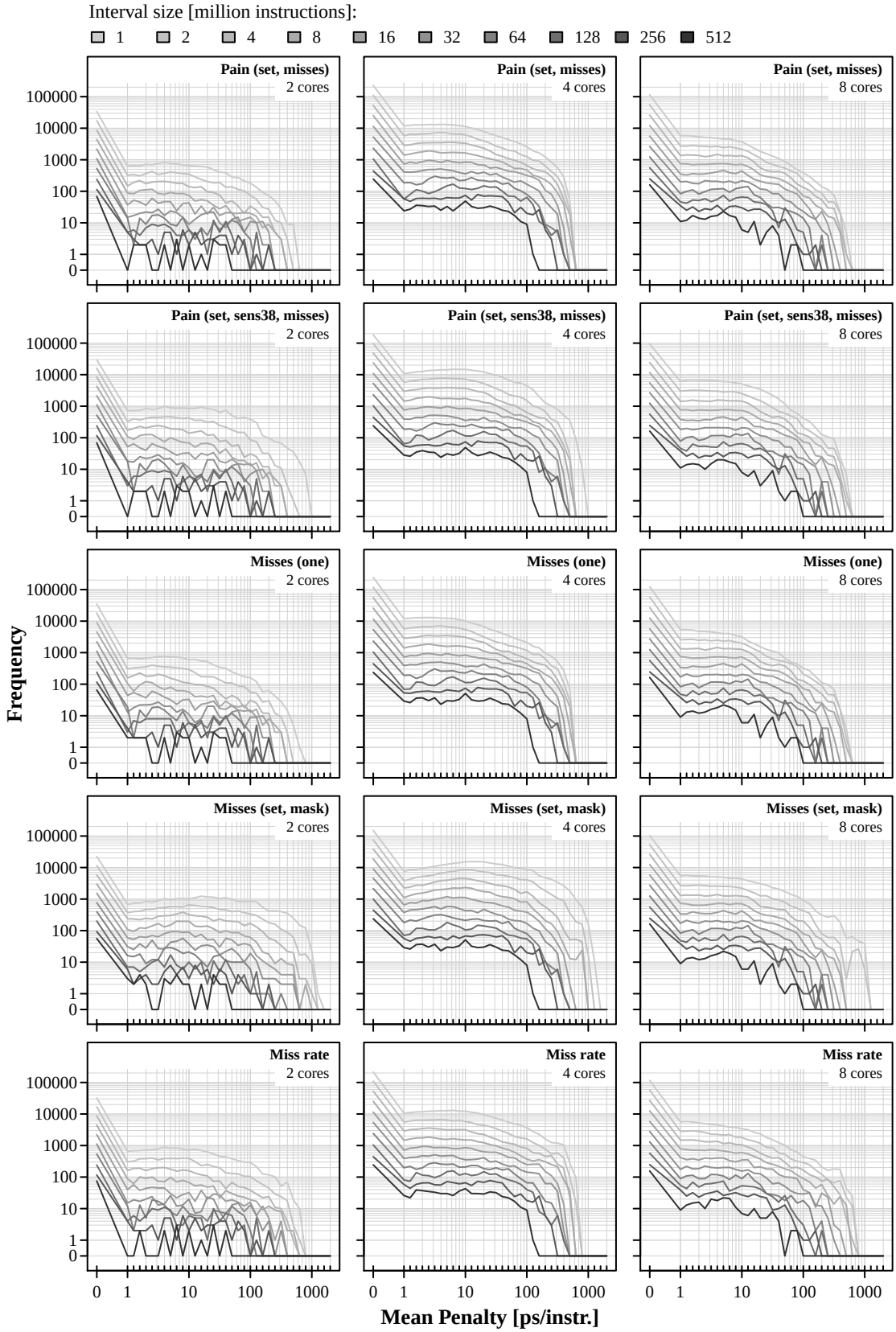

Figure 15: Mean Penalty distribution (part 4 of 8).

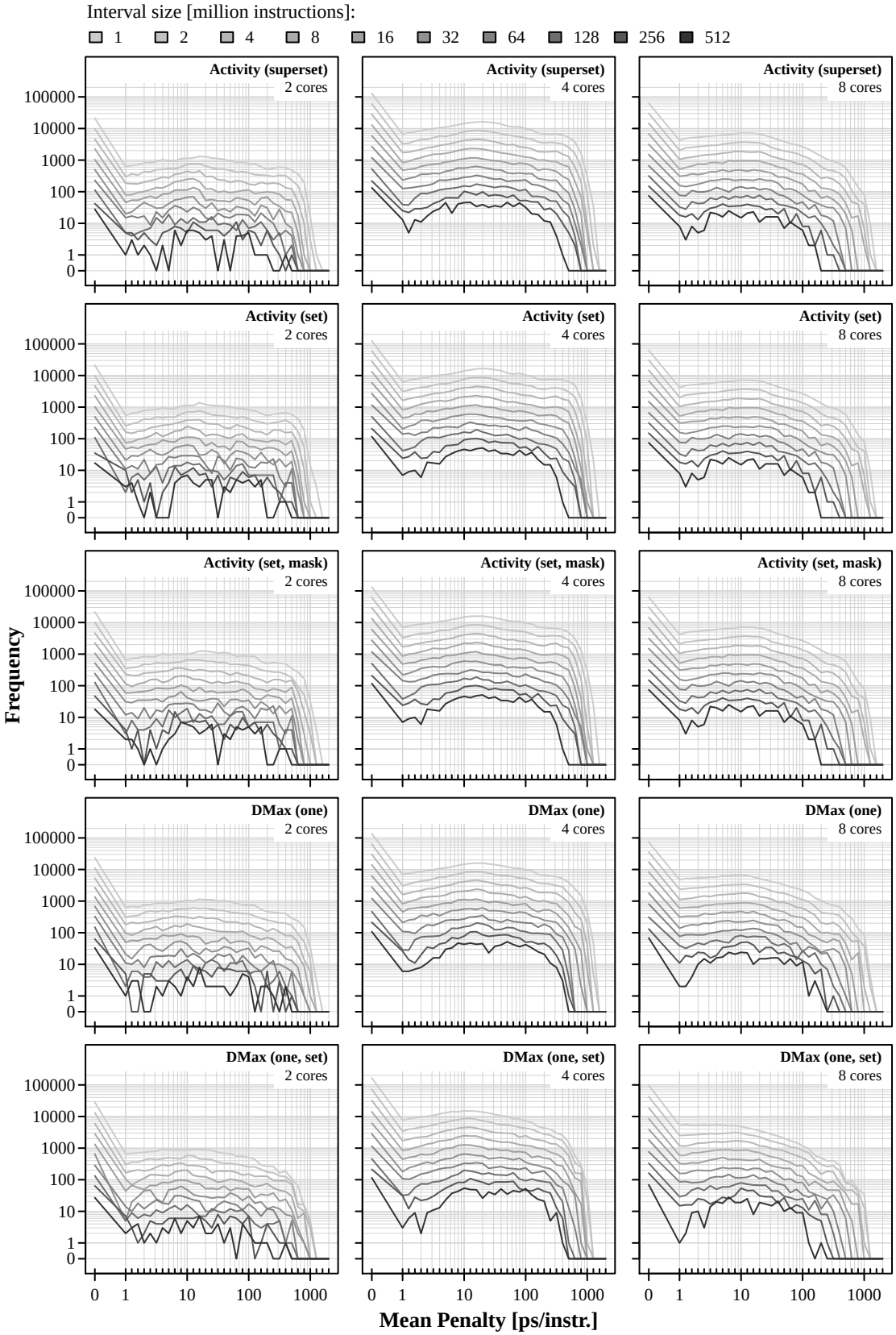

Figure 16: Mean Penalty distribution (part 5 of 8).

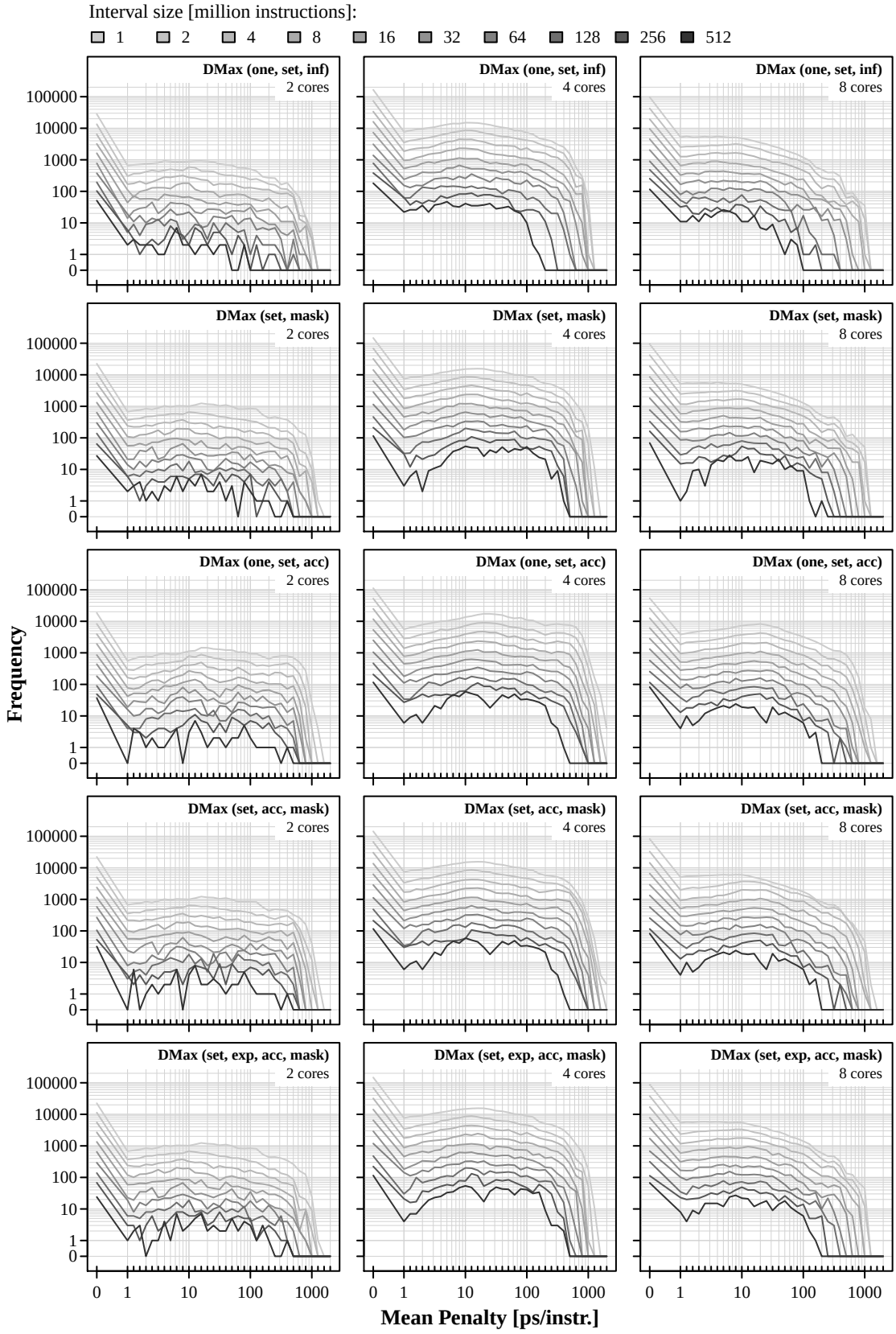

Figure 17: Mean Penalty distribution (part 6 of 8).

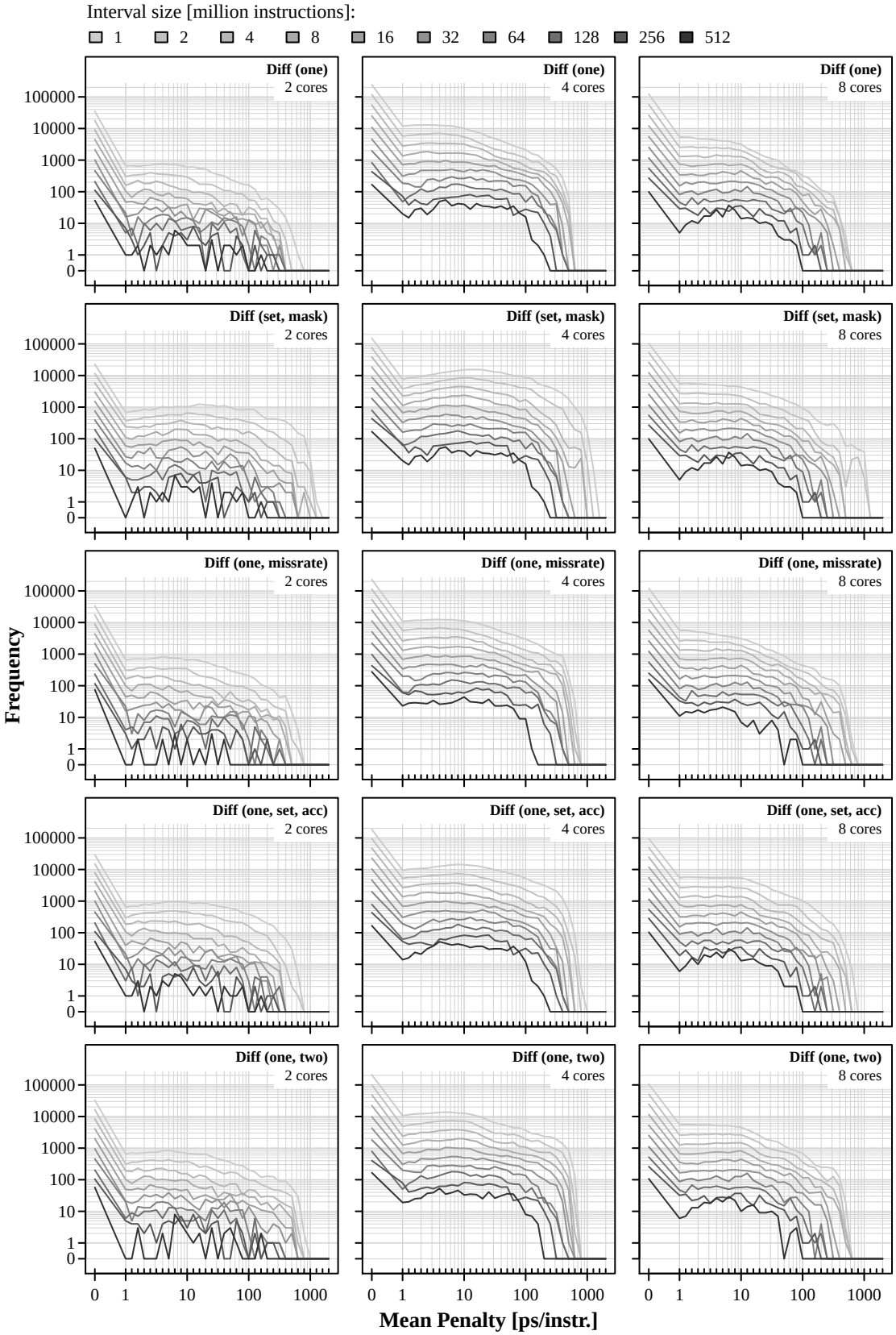

Figure 18: Mean Penalty distribution (part 7 of 8).

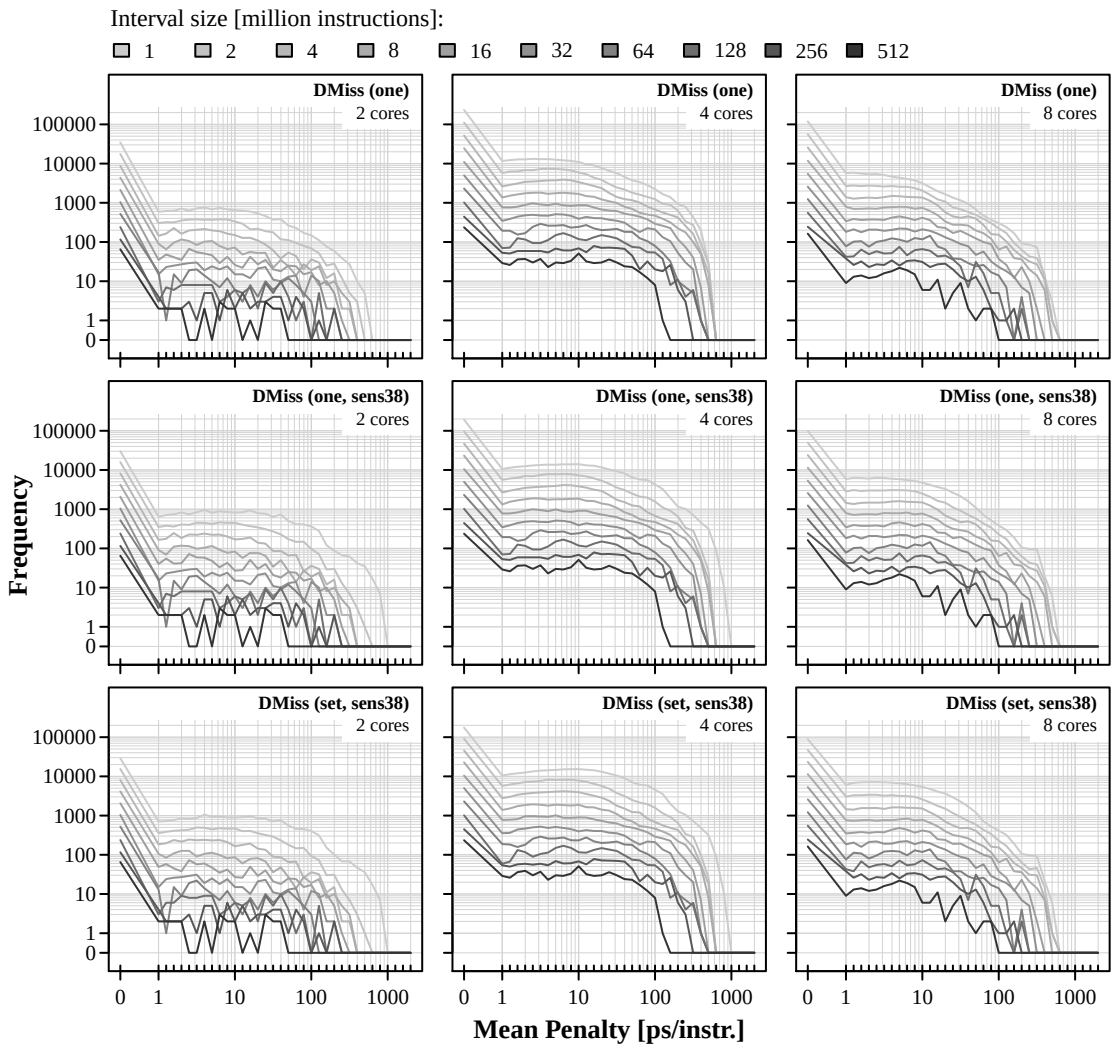

Figure 19: Mean Penalty distribution (part 8 of 8).

2.3 Penalty Predicted Best vs. Actual Best

Figures 20 to 27 present Penalty Predicted Best vs. Actual Best (PPBAB) distributions for PPBAB average values presented in the thesis, section 3.3, figure 33. Ticks on the abscissa that reside at the *inside* of each plot determine sampling intervals. See figure 11 for an explanation of how to read the plots. Comparing average PPBAB values (figure 33 in the thesis) to PPBAB distributions (figures 20 to 27 in this report), you can observe that PPBAB distribution of more accurately performing cache contention prediction methods (e.g. *Prob* method) drops off at much smaller penalties than PPBAB distribution of poorly performing prediction methods (e.g. *FOA*, variation *one*).

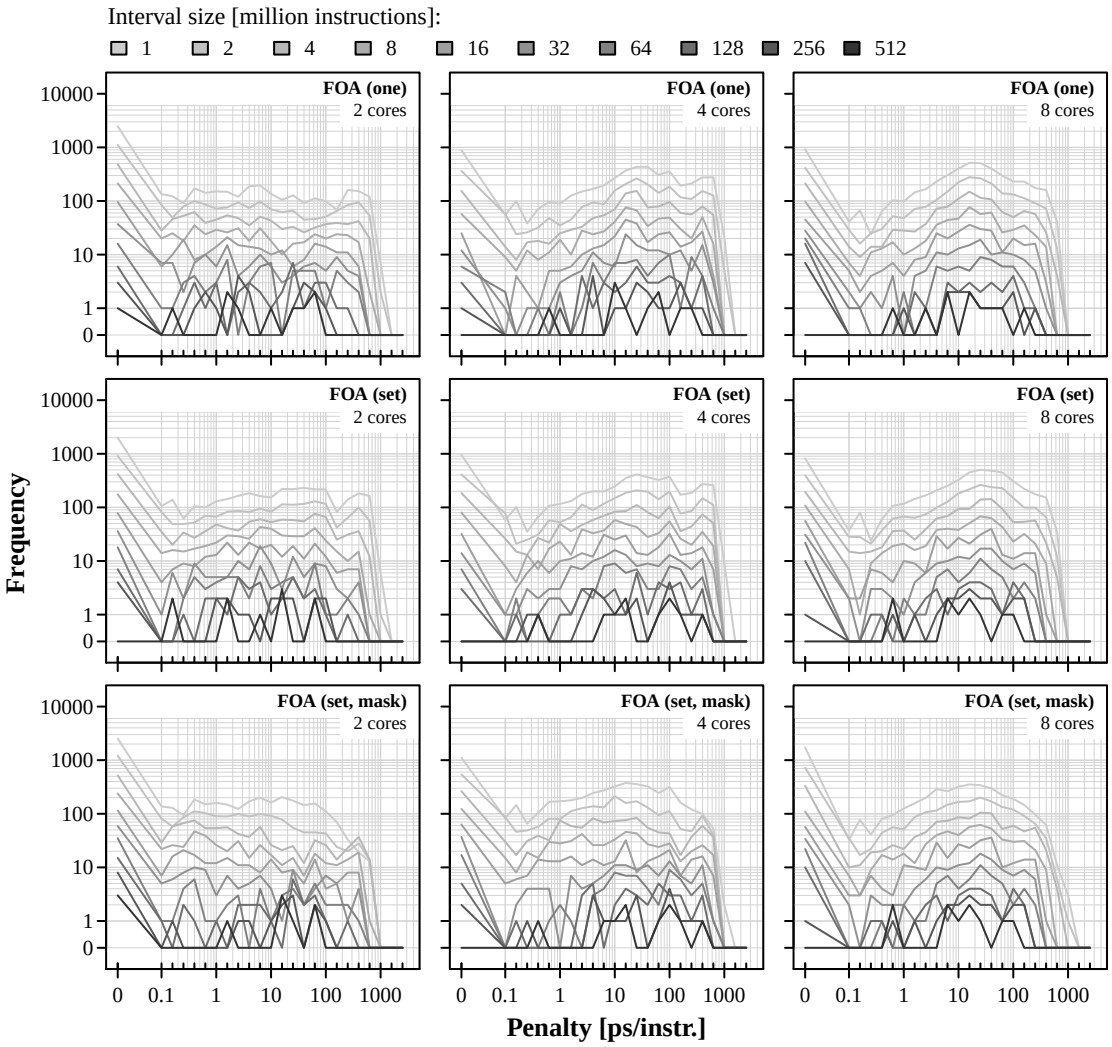

Figure 20: PPBAB distribution (part 1 of 8).

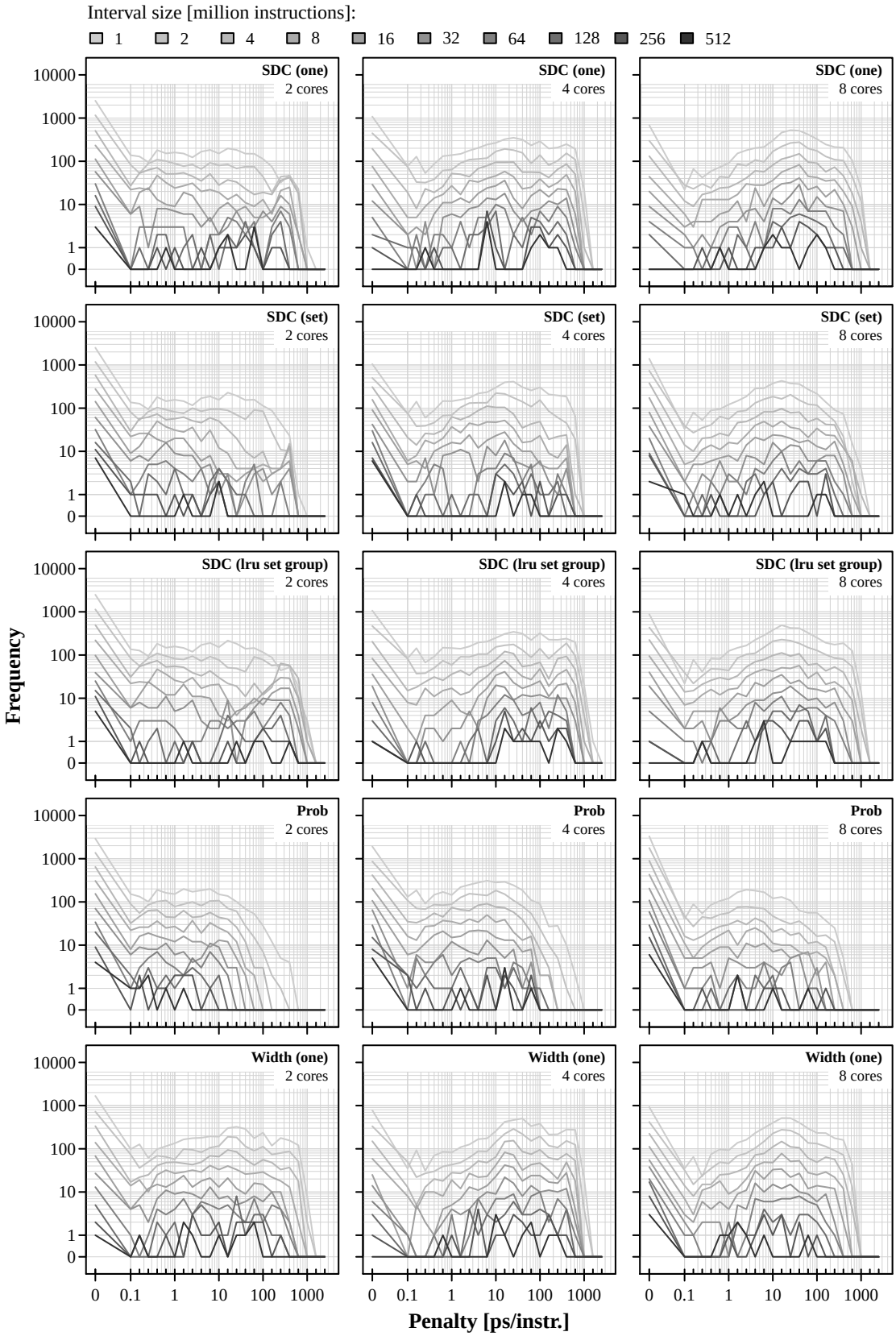

Figure 21: PPBAB distribution (part 2 of 8).

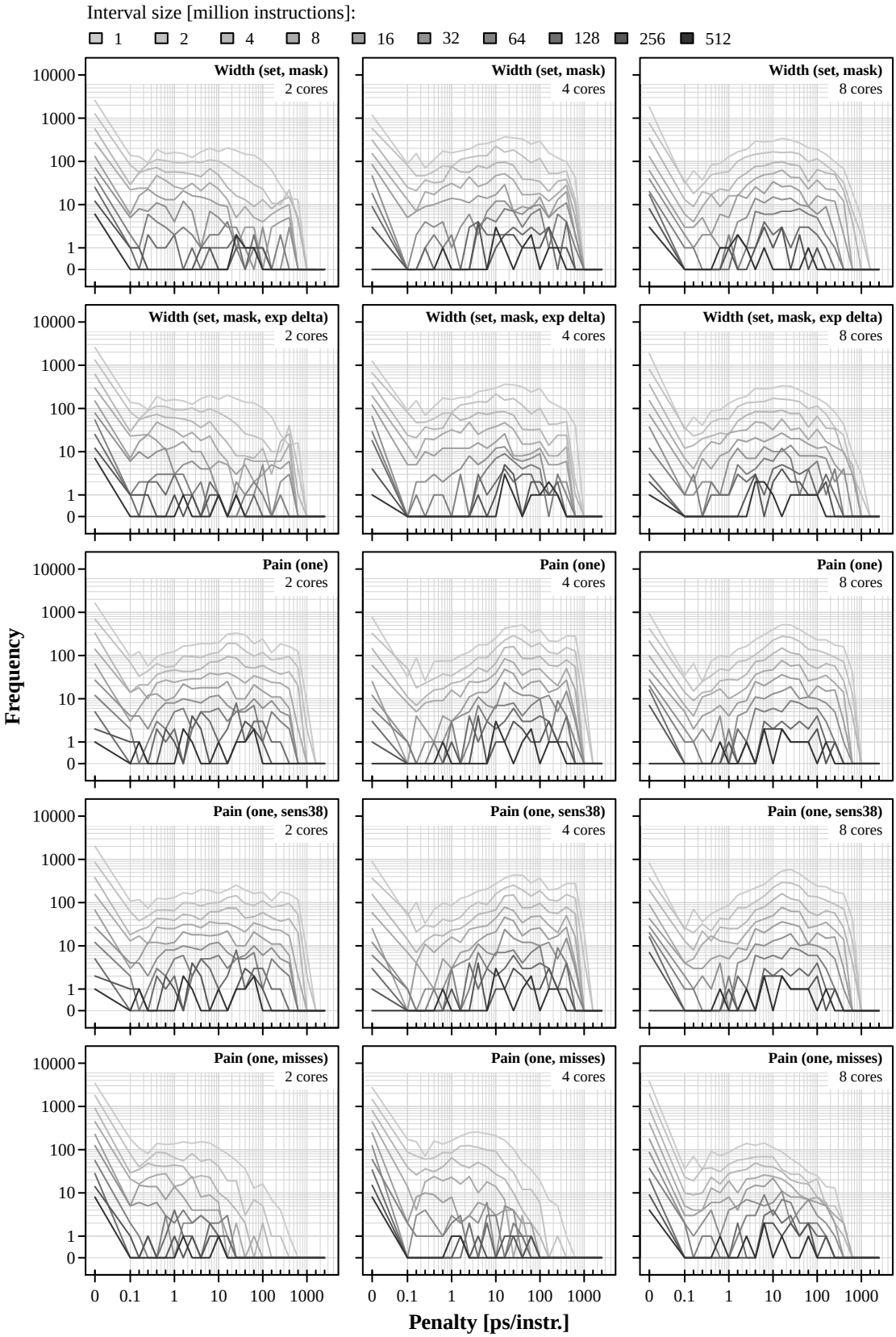

Figure 22: PPBAB distribution (part 3 of 8).

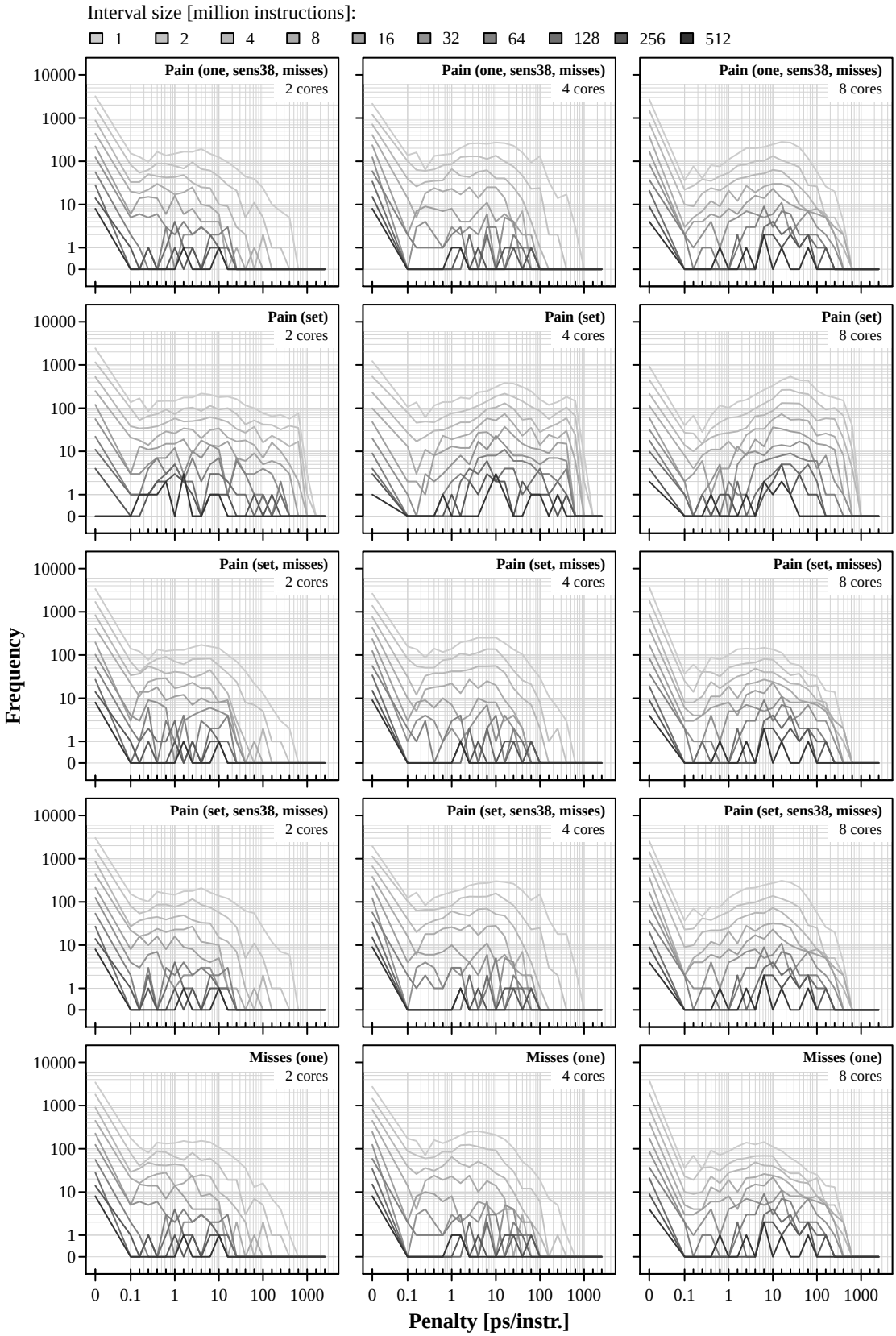

Figure 23: PPBAB distribution (part 4 of 8).

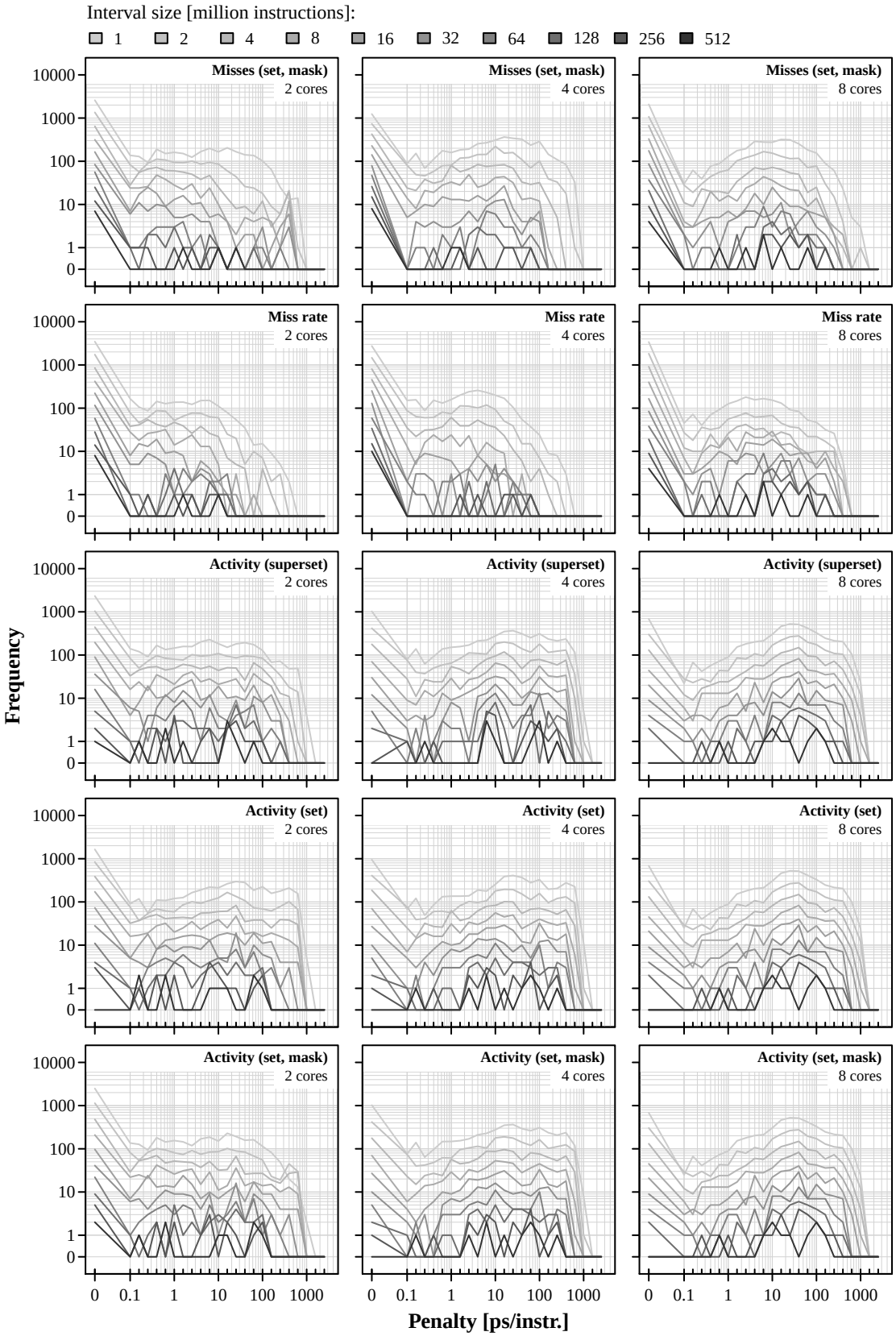

Figure 24: PPBAB distribution (part 5 of 8).

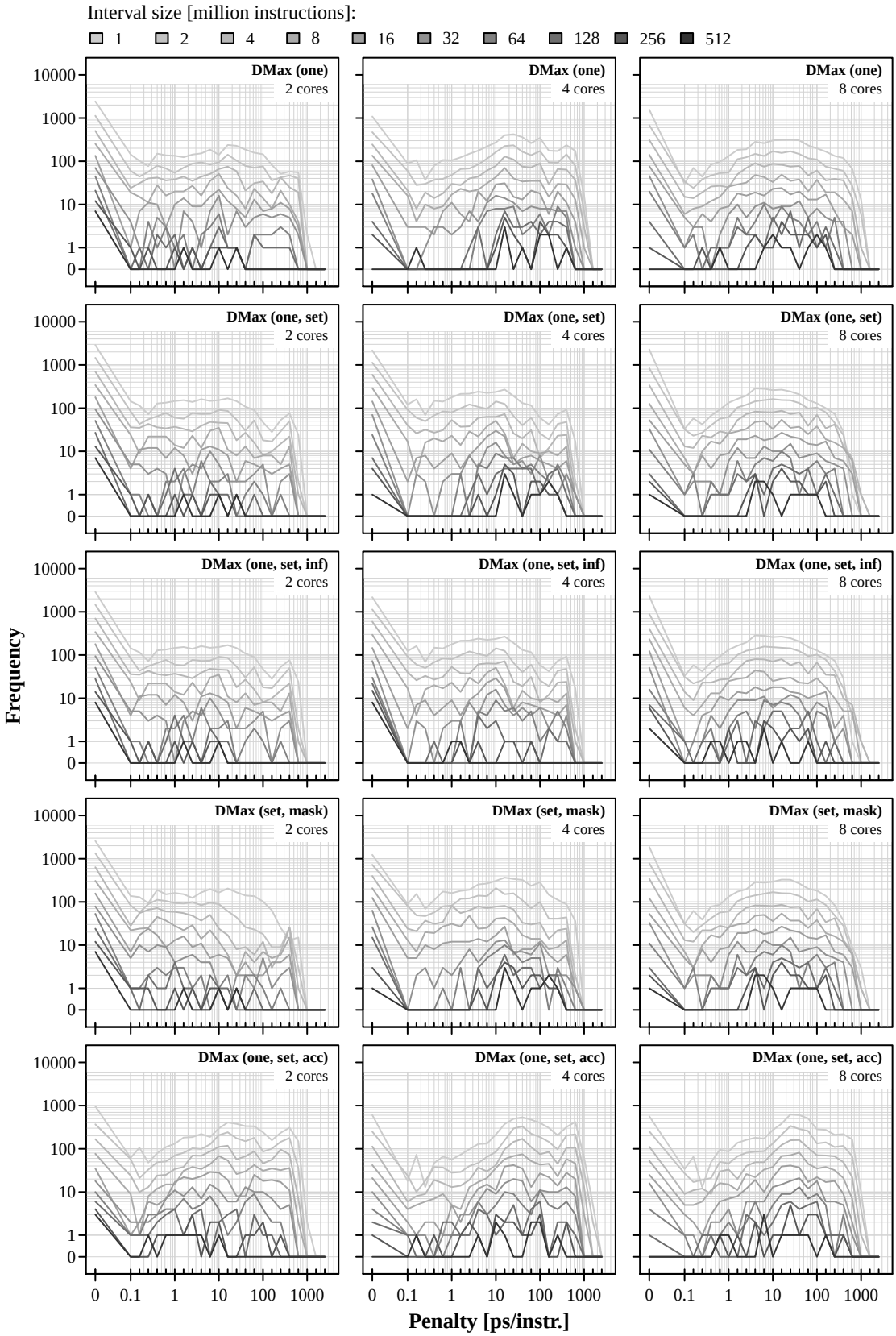

Figure 25: PPBAB distribution (part 6 of 8).

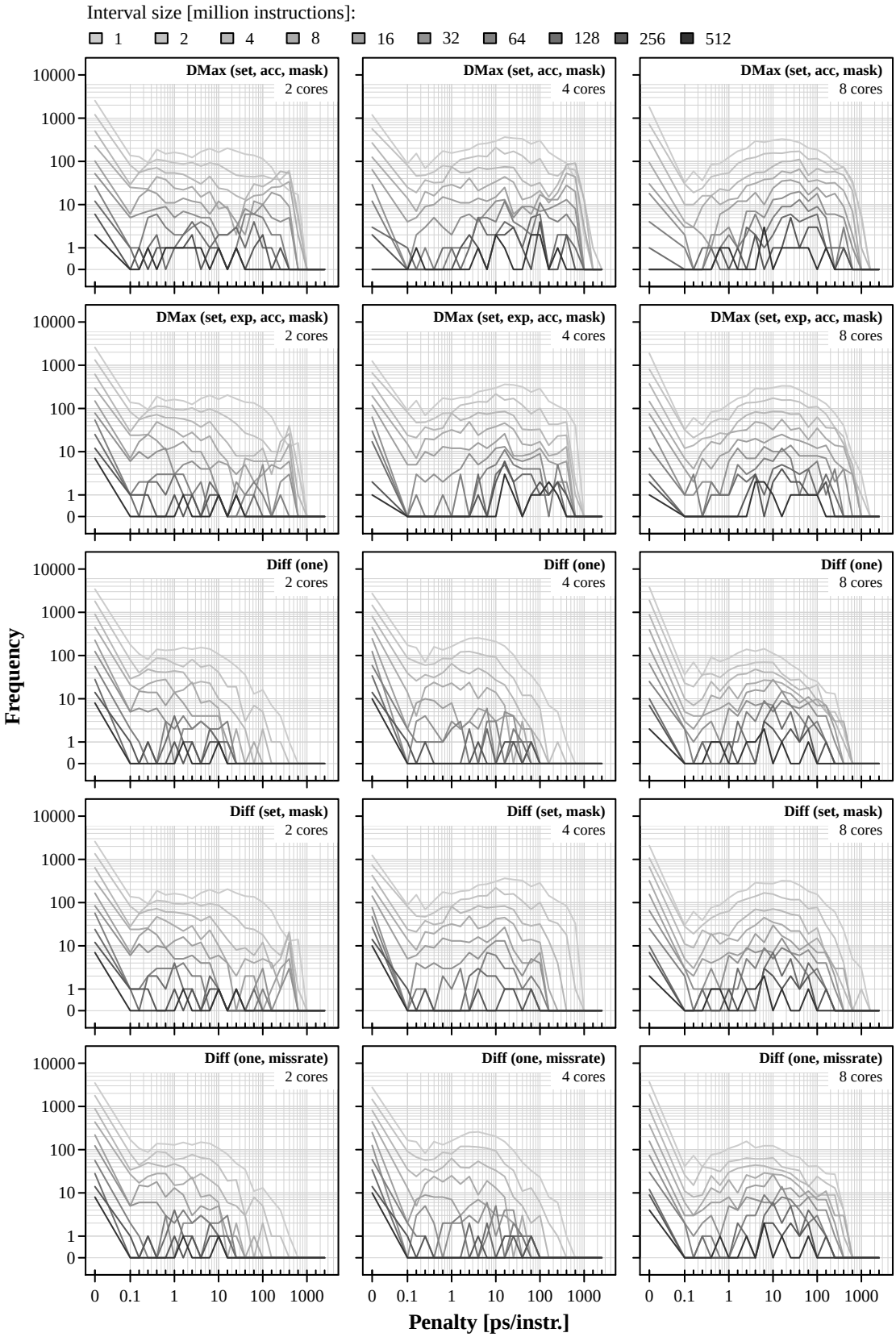

Figure 26: PPBAB distribution (part 7 of 8).

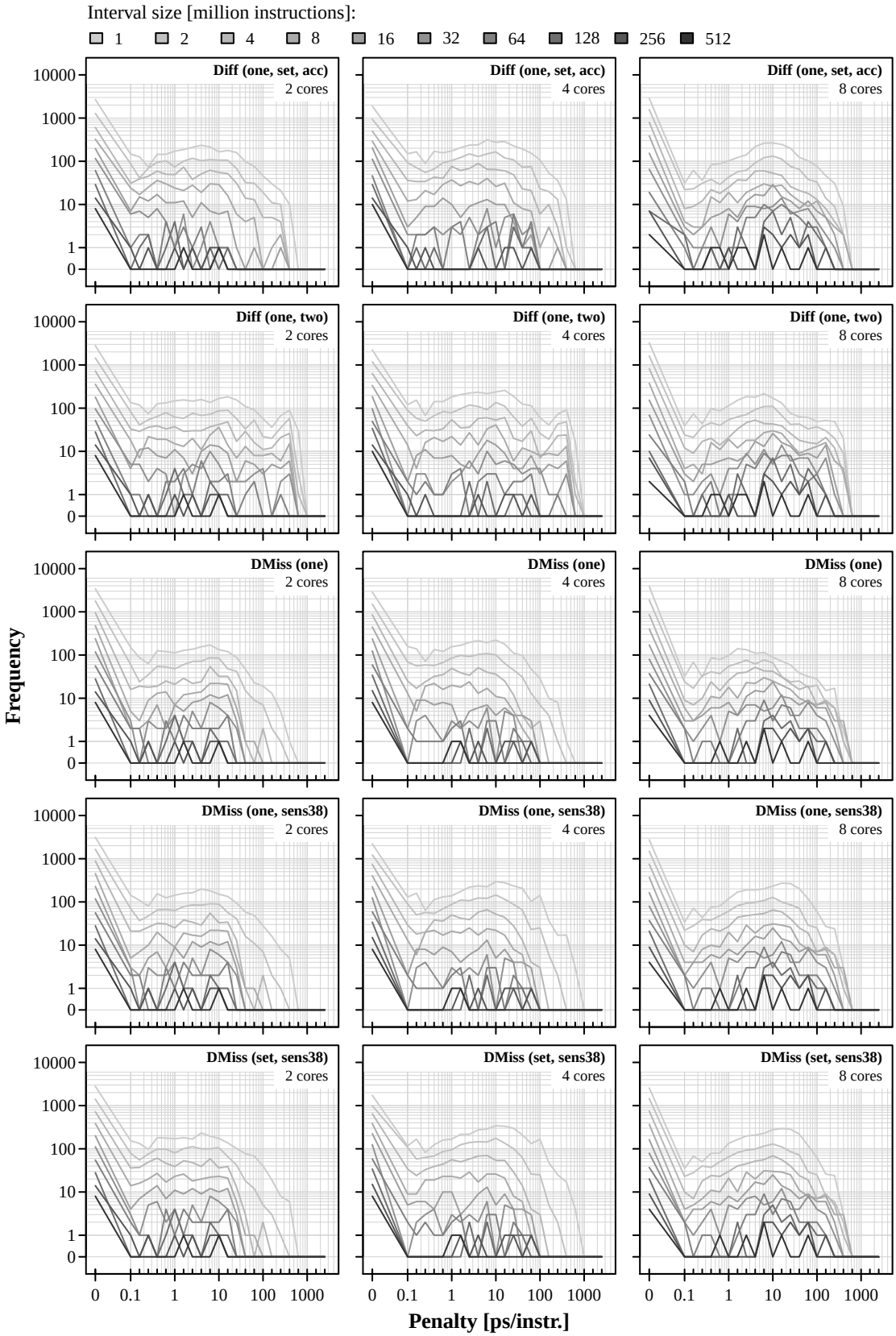

Figure 27: PPBAB distribution (part 8 of 8).

2.4 Penalty Predicted Best vs. Random Selection

Figures 29 to 36 present PPBRS (Penalty Predicted Best vs. Random Selection, i.e. gain) distributions for PPBRS average values presented in the thesis, section 3.3, figure 36. Ticks that reside at the *inside* of the abscissa of each plot determine sampling intervals. Abscissa values ≤ -1 and ≥ 1 and ordinate values ≥ 1 are plotted in logarithmic scale; abscissa and ordinate value 0 is plotted out of scale. Figure 28 shows how to read PPBRS distribution plots.

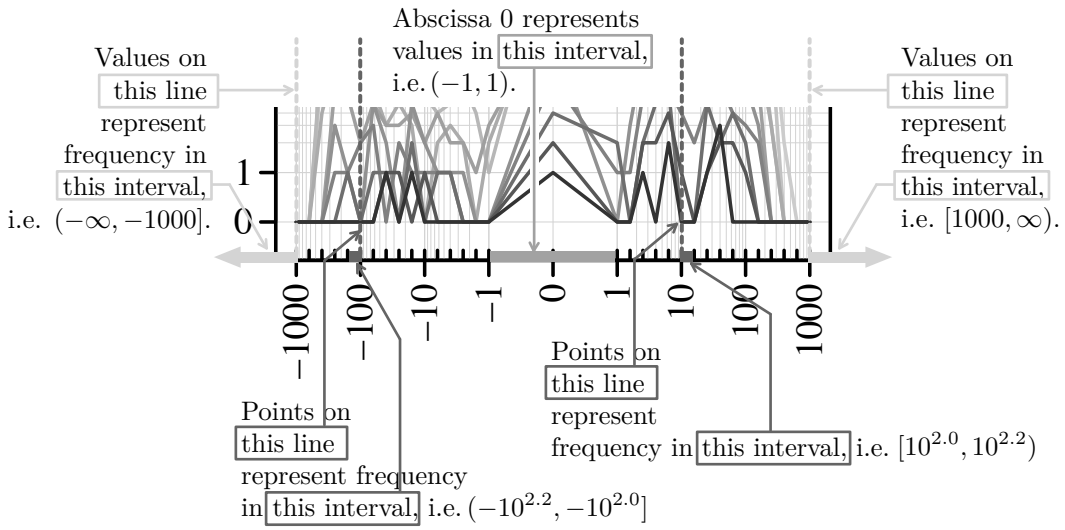

Figure 28: PPBRS distribution glossary.

Comparing average PPBRS values (figure 36 in the thesis) to PPBRS distributions (figures 29 to 36 in this report), you can observe that PPBRS distributions of more accurately performing cache contention prediction methods (e.g. *Prob*) are dominated by positive values of gain and show a much higher frequency at the right hand side of the plot. Cache contention prediction methods of rather poor performance, however, show a more balanced distribution (e.g. *FOA*, variation *set*).

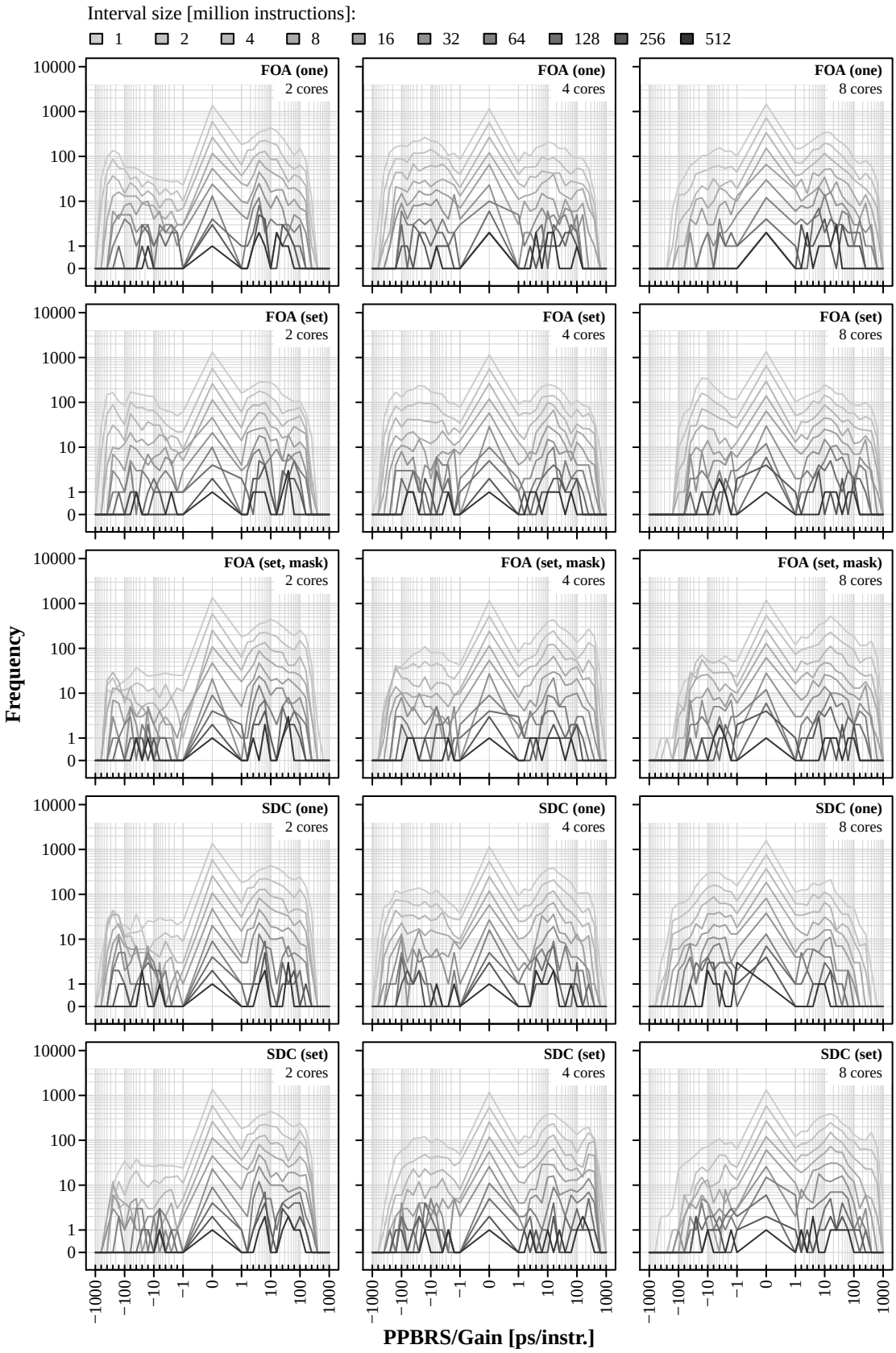

Figure 29: PPBRS distribution (part 1 of 8).

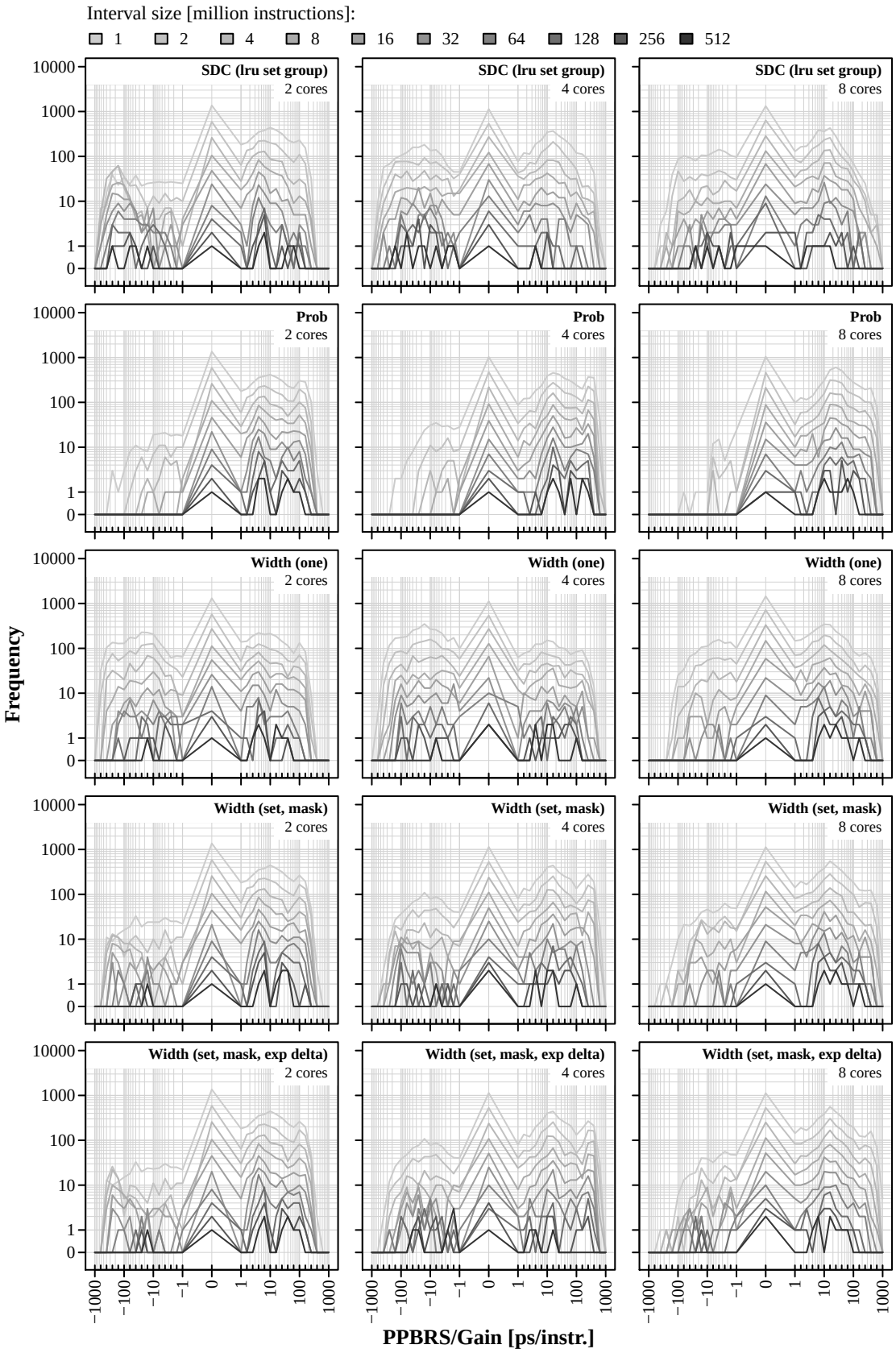

Figure 30: PPBRS distribution (part 2 of 8).

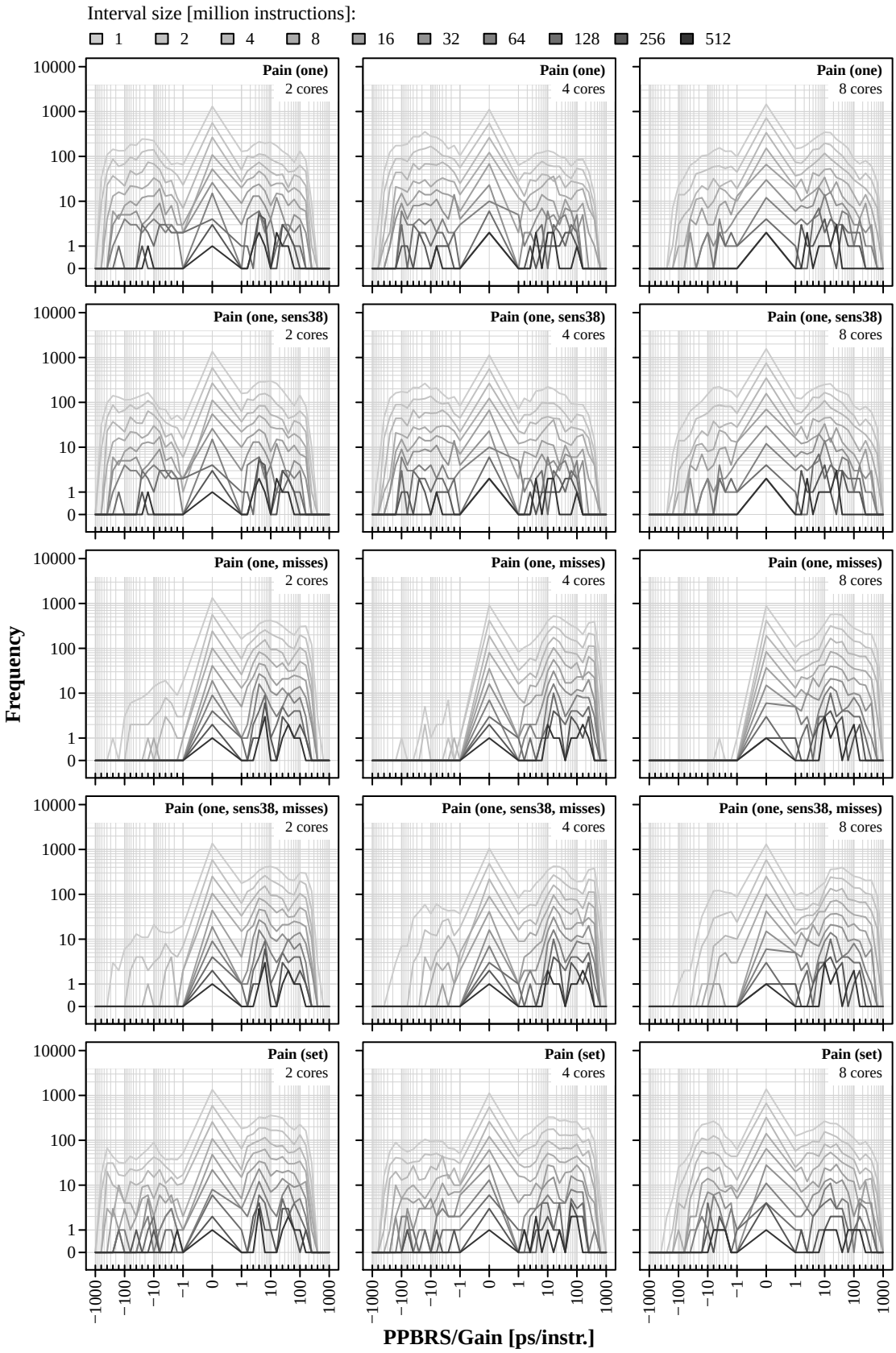

Figure 31: PPBRS distribution (part 3 of 8).

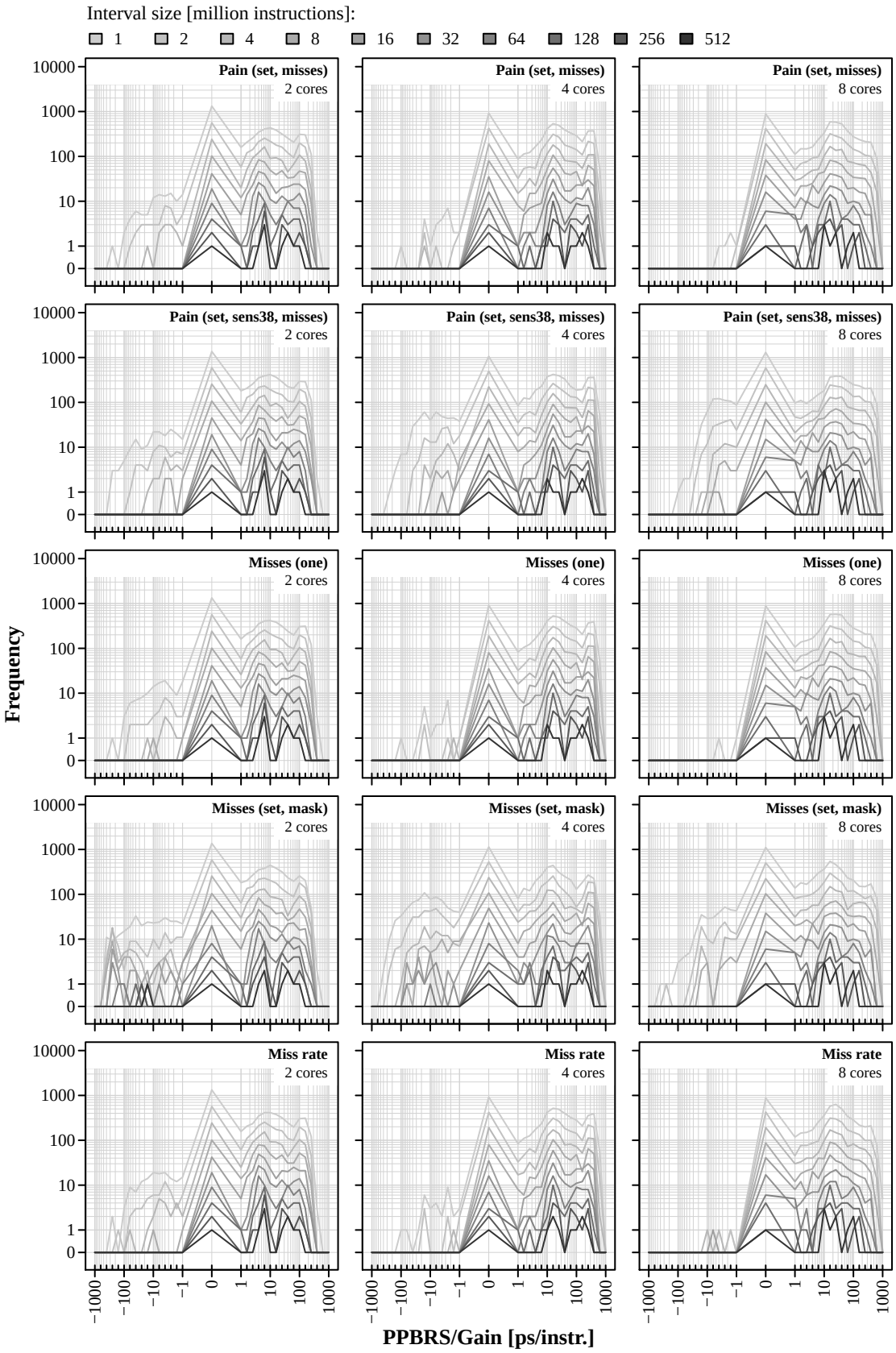

Figure 32: PPBRS distribution (part 4 of 8).

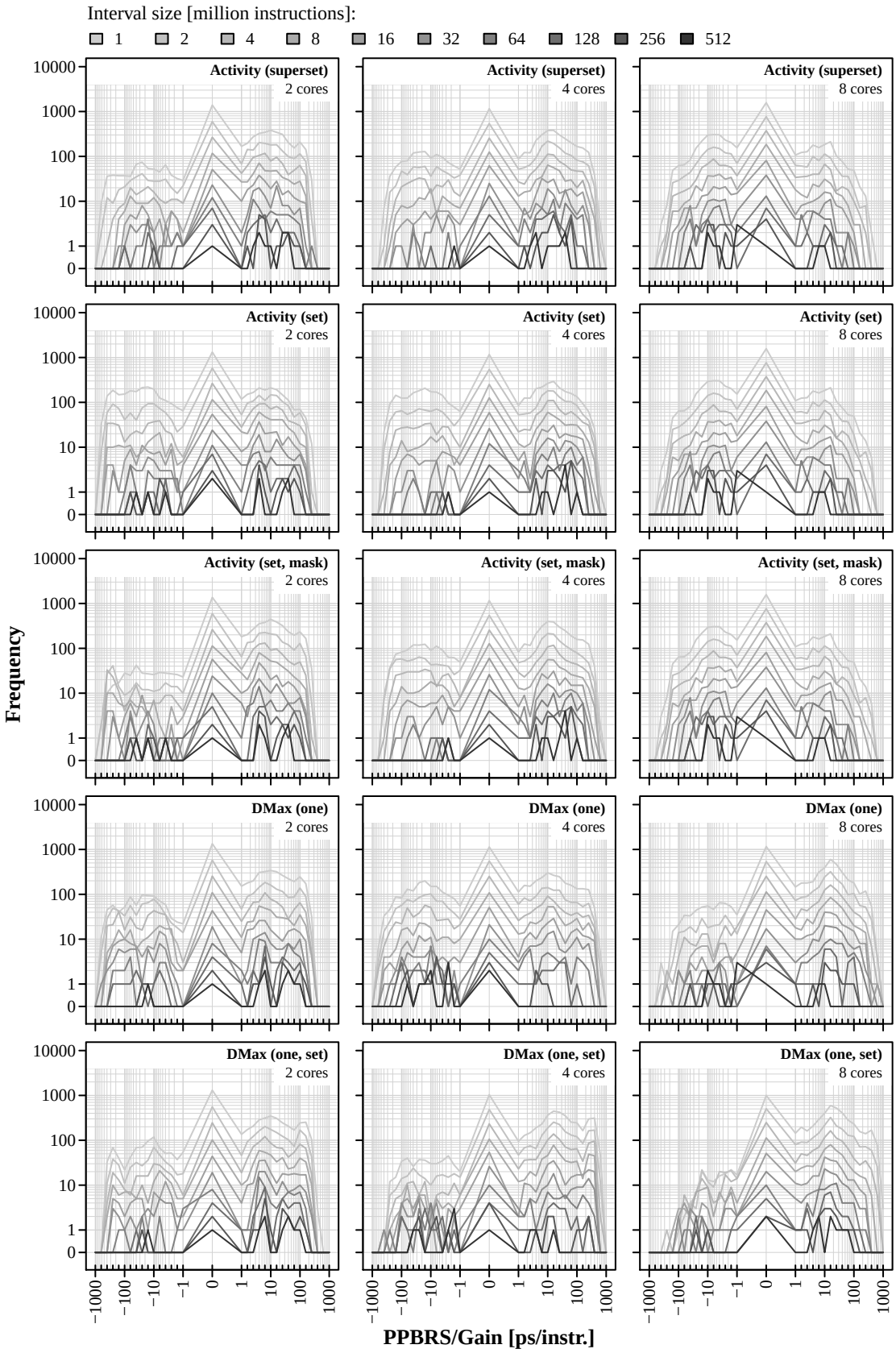

Figure 33: PPBRS distribution (part 5 of 8).

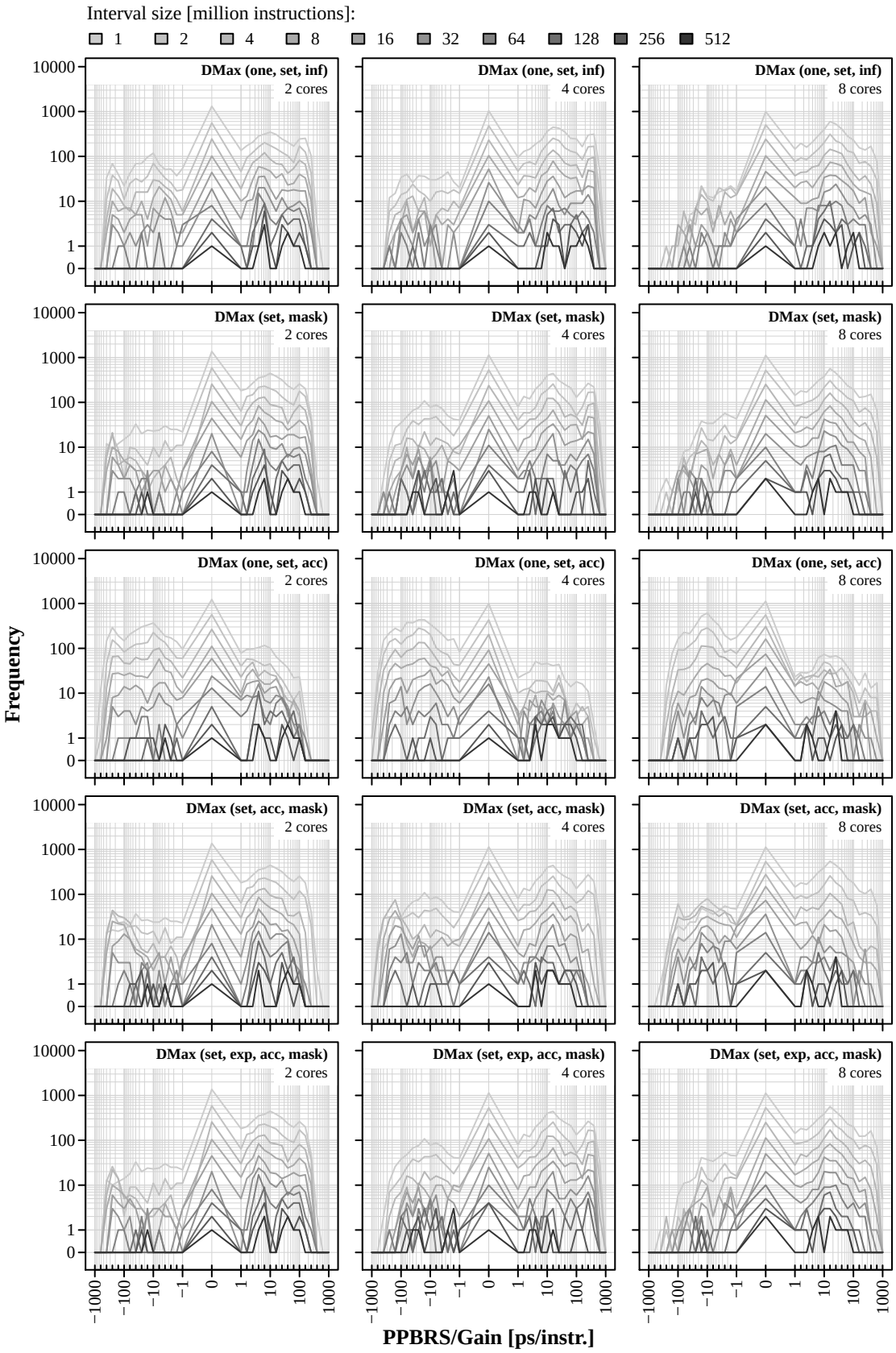

Figure 34: PPBRS distribution (part 6 of 8).

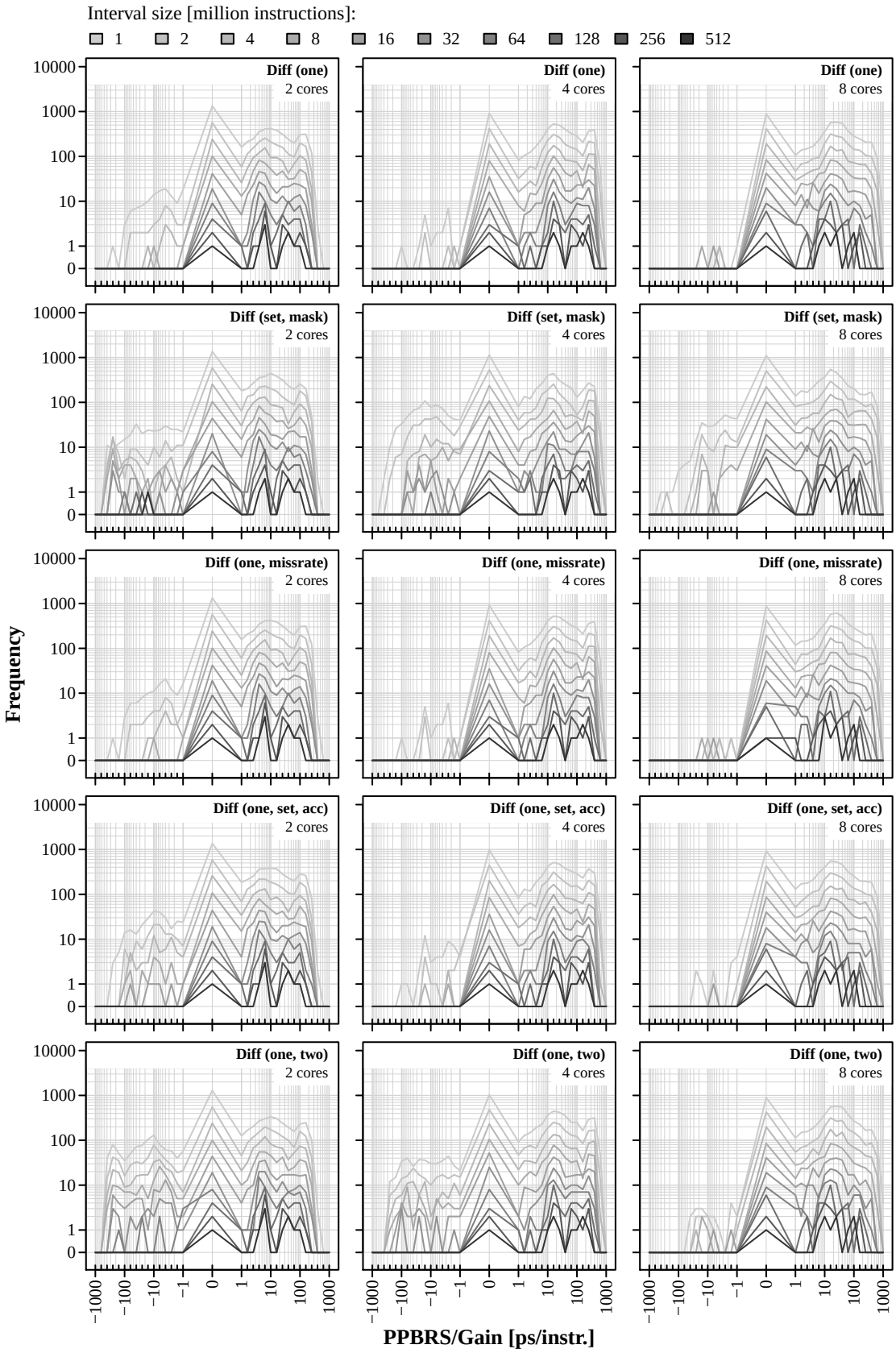

Figure 35: PPBRS distribution (part 7 of 8).

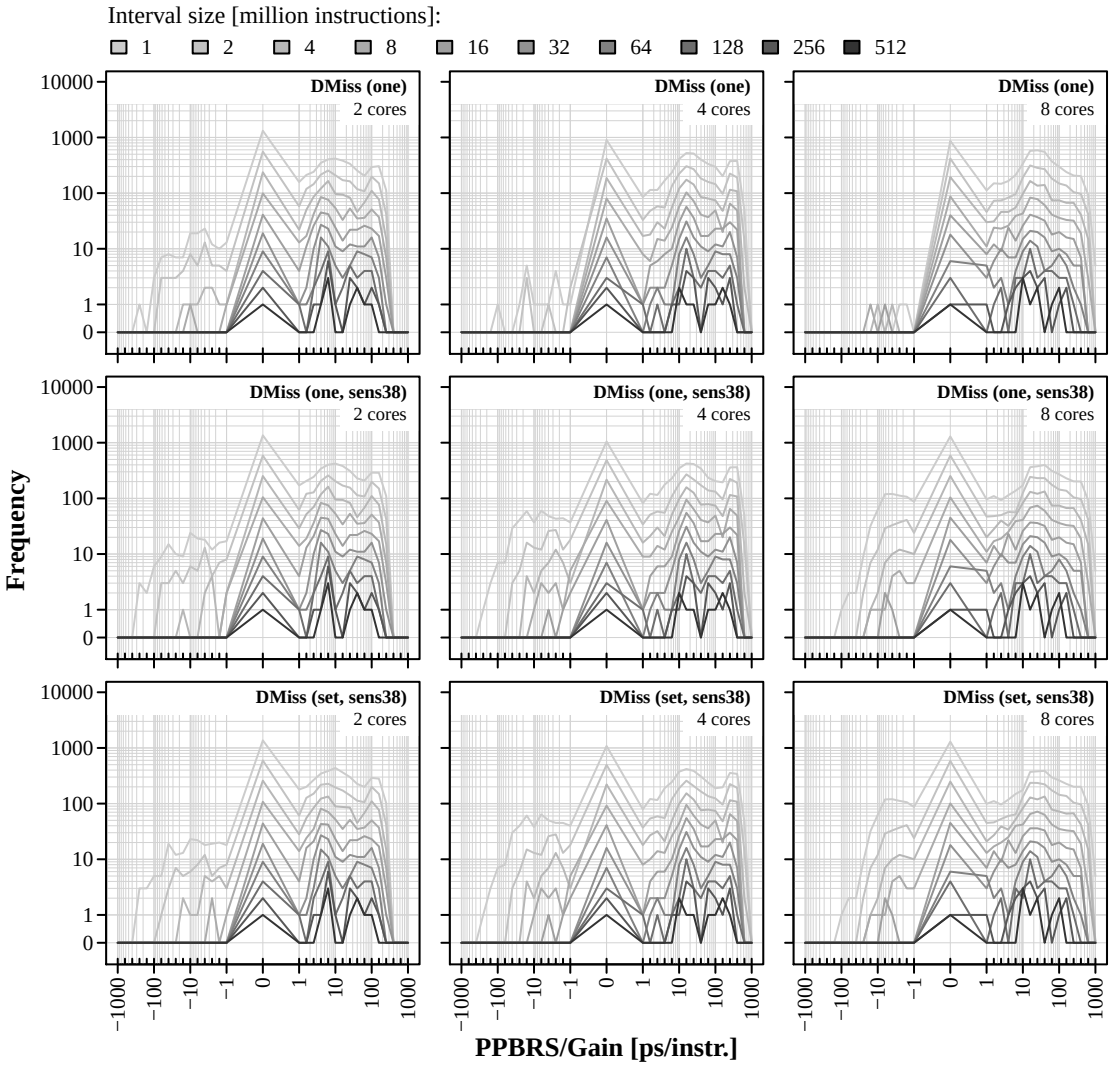

Figure 36: PPBRS distribution (part 8 of 8).

3 Modified Access and Hit Times

In the thesis, I applied an L1 hitrate of 1 ns, an L2 hitrate of 10 ns and a main memory access time of 100 ns. In this section, I present evaluation results when applying an L1 hitrate of 1 ns, an L2 hitrate of 2 ns and a main memory access time of 10 ns.

- In figures 37 and 38, I present evaluation results considering NMRD (normalized mean ranking difference) performance.
- In figures 39 and 40, I present evaluation results considering MP (mean penalty) performance.
- In figures 41 and 42, I present evaluation results considering PPBAB (penalty predicted best vs. actual best) performance.
- In figures 43 and 44, I present evaluation results considering PPBRS (penalty predicted best vs. random selection) performance.
- In figures 45 and 46, I present evaluation results considering gain vs. cost performance.

Plots on the left hand side show performance in case L1 hitrate = 1 ns, L2 hitrate = 10 ns, and main memory access time = 100 ns, as it has been presented in the thesis; plots on the right hand side show performance in case L1 hitrate = 1 ns, L2 hitrate = 2 ns, and main memory access time = 10 ns.

Comparing the plots on the following doublepages, you can observe that simulation results of the various methods *in relation to one another* are almost identical. Therefore, evaluation results considering performance of cache contention prediction techniques *in relation to each other* seem to be transferable from heavily diverging hit and access times, as applied in the thesis, to hit and access times that differ at a much lower extent.

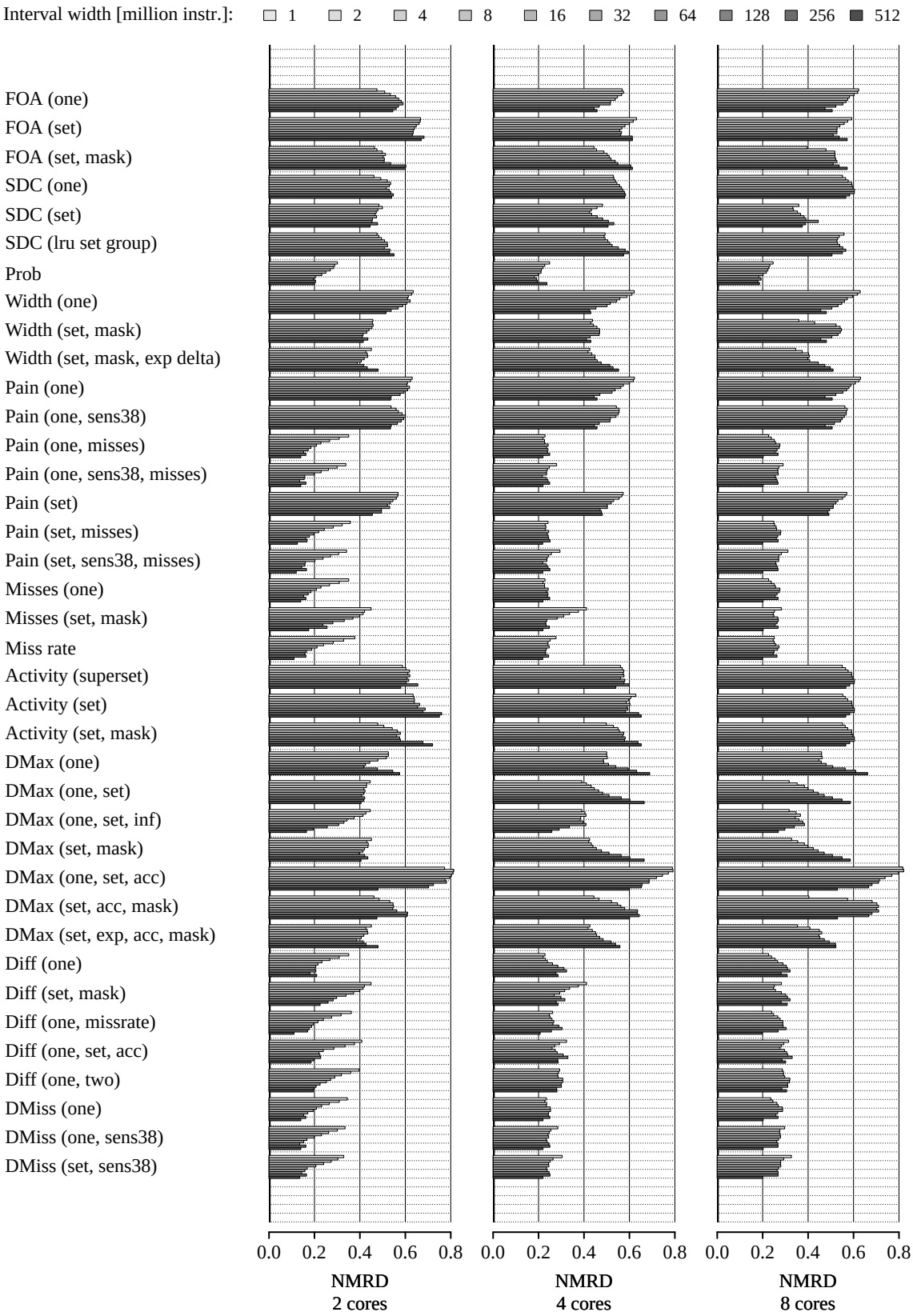

Figure 37: NMRD performance in case L1 hit time is 1 ns, L2 hit time is 10 ns and main memory access time is 100 ns.

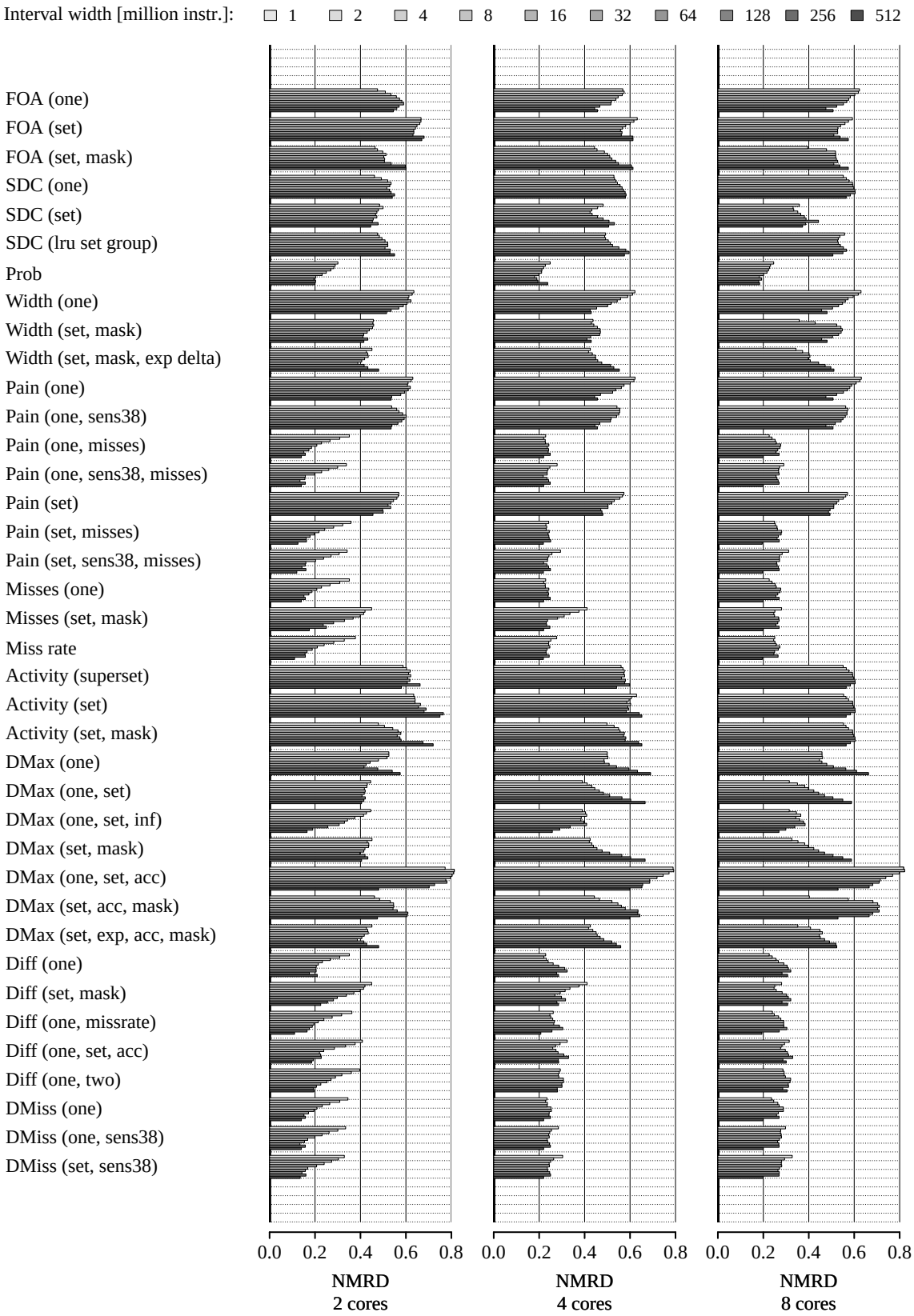

Figure 38: NMRD performance in case L1 hit time is 1 ns, L2 hit time is 2 ns and main memory access time is 10 ns.

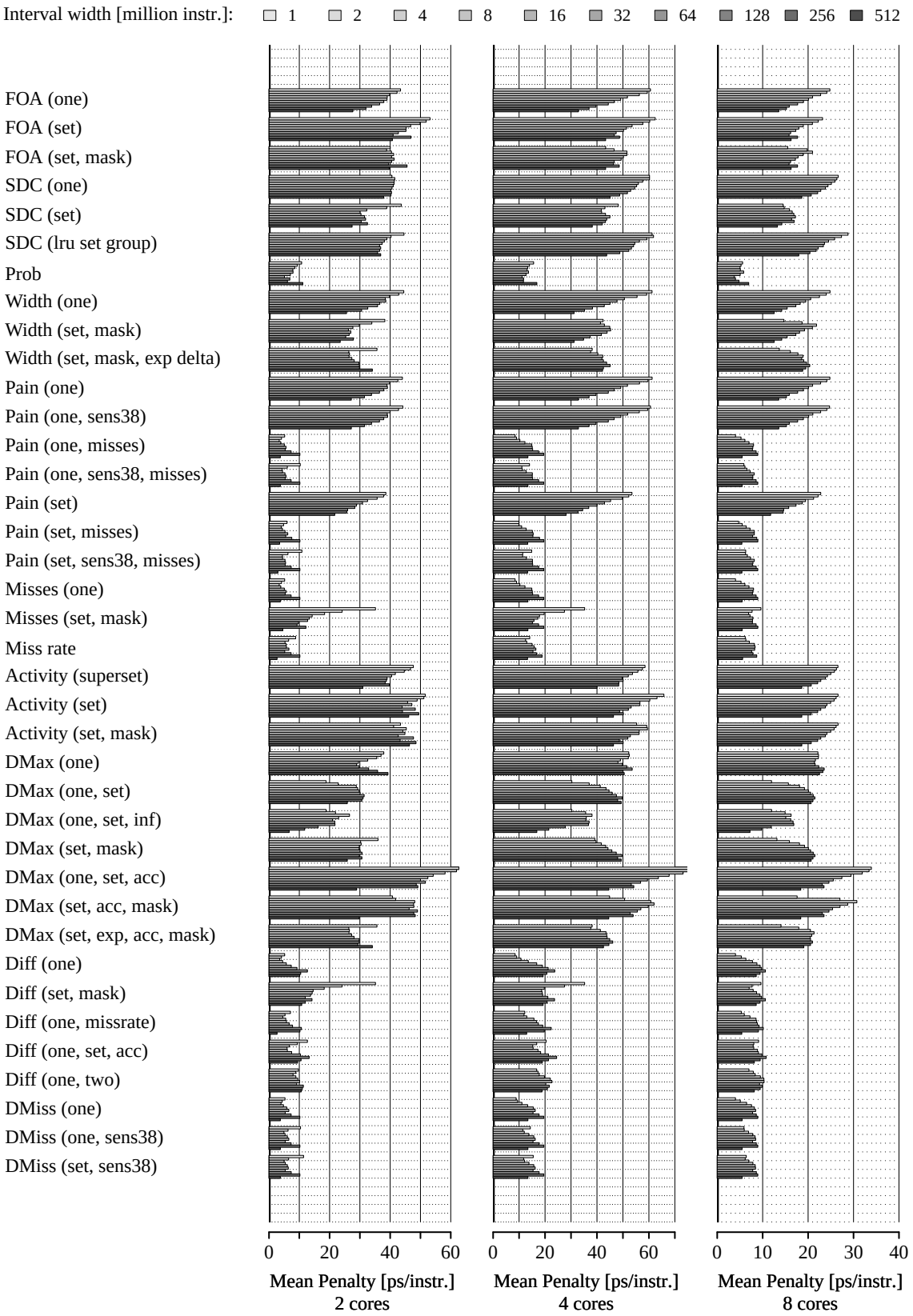

Figure 39: MP performance in case L1 hit time is 1 ns, L2 hit time is 10 ns and main memory access time is 100 ns.

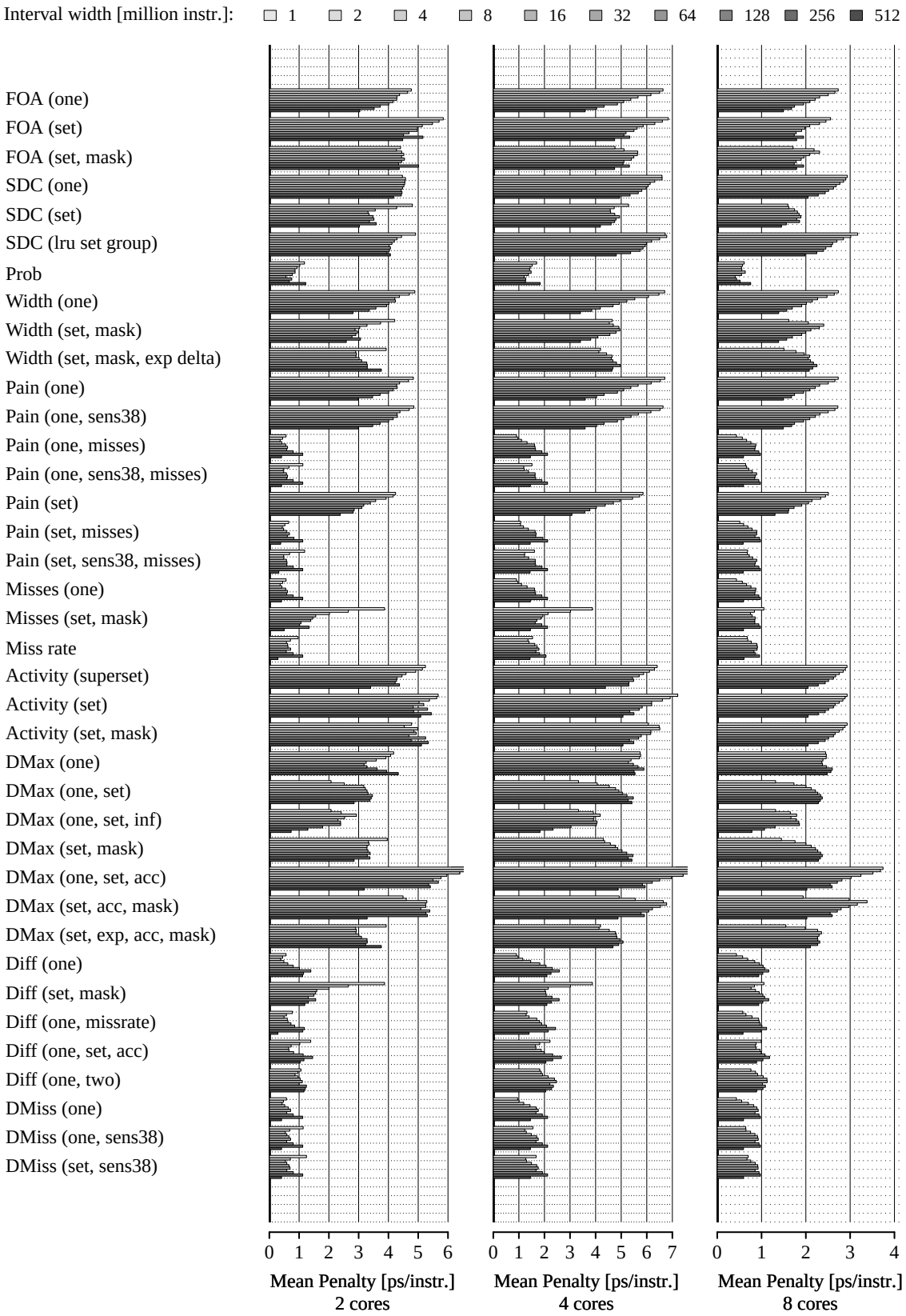

Figure 40: MP performance in case L1 hit time is 1 ns, L2 hit time is 2 ns and main memory access time is 10 ns.

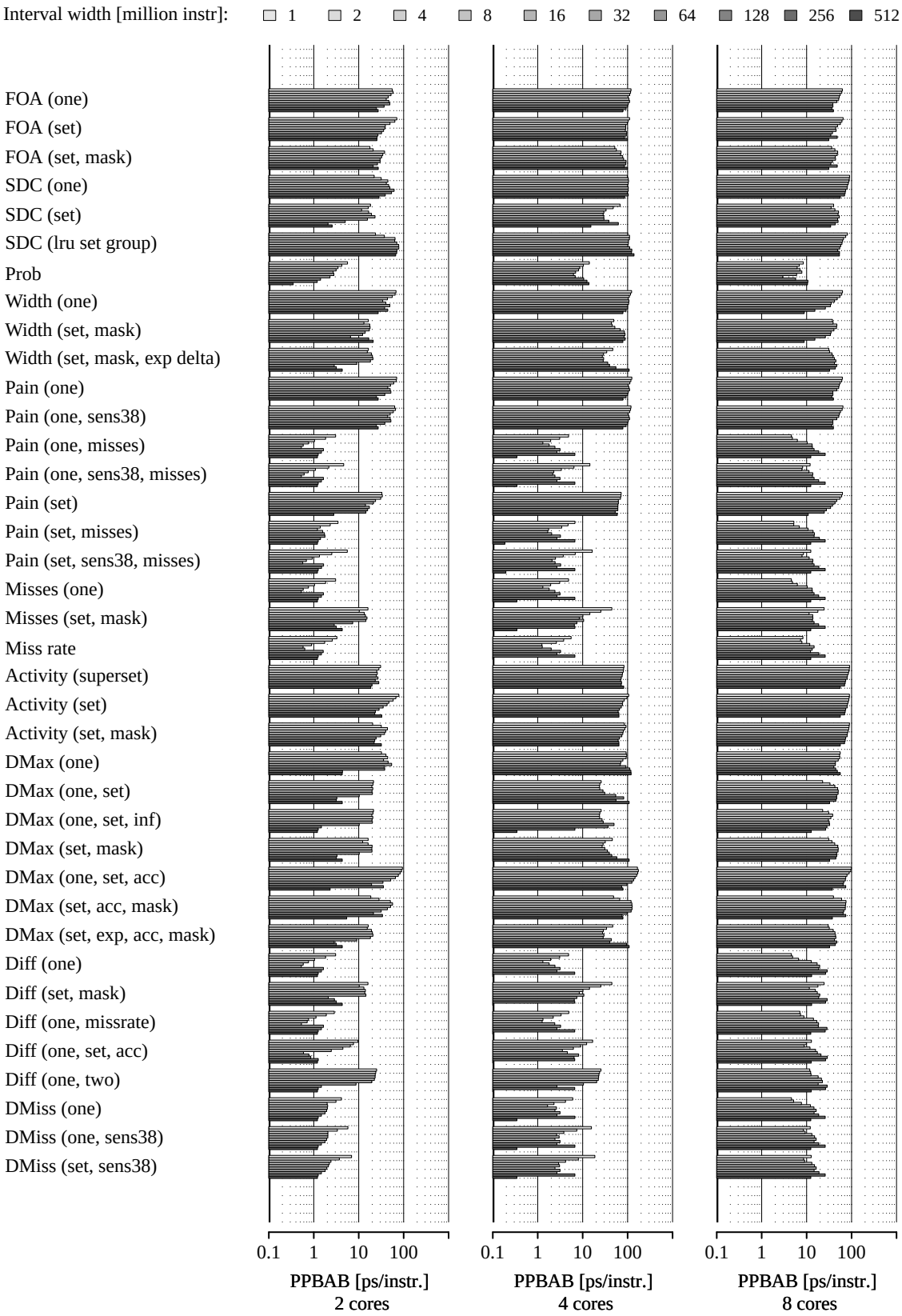

Figure 41: PPBAB performance in case L1 hit time is 1 ns, L2 hit time is 10 ns and main memory access time is 100 ns.

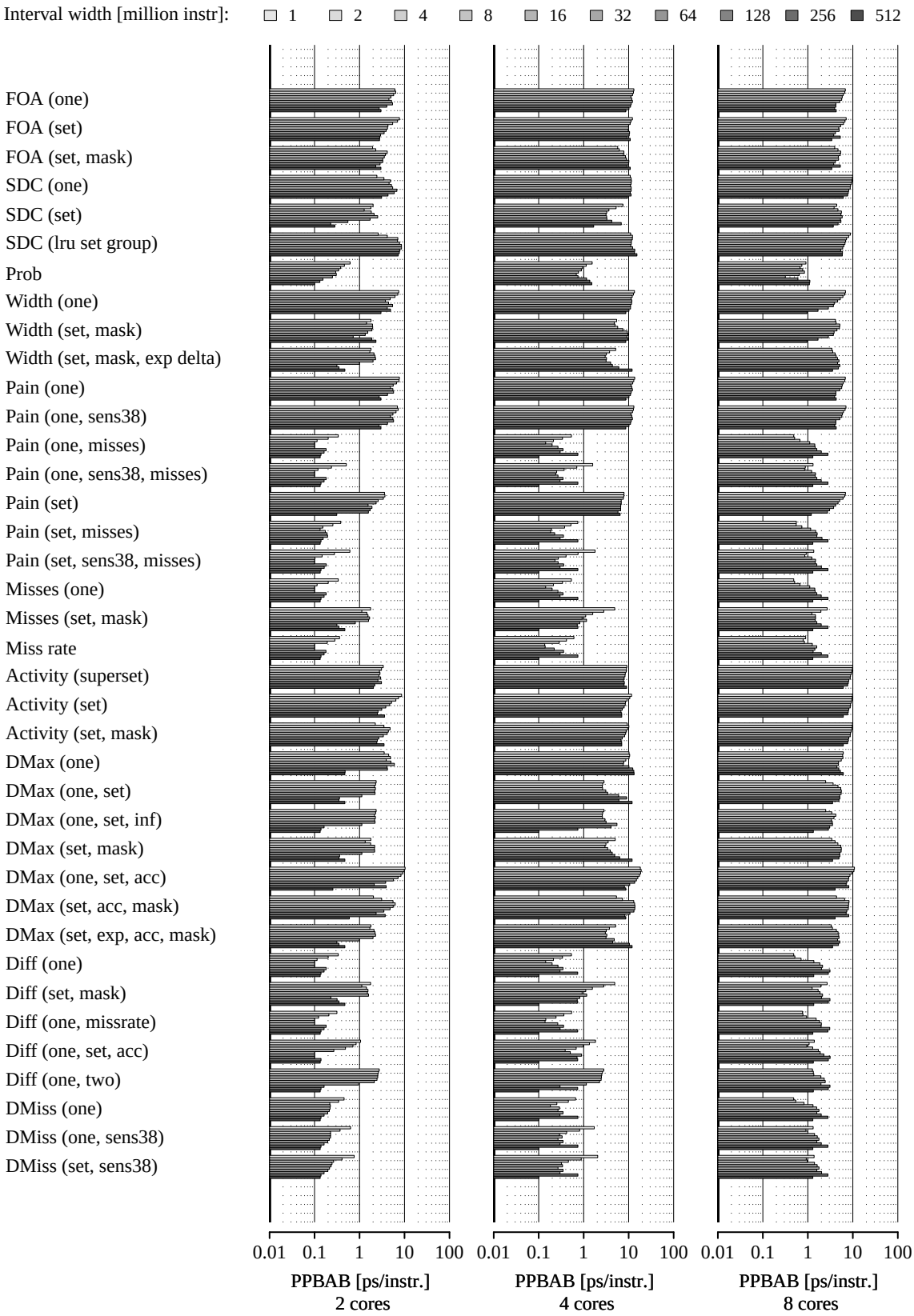

Figure 42: PPBAB performance in case L1 hit time is 1 ns, L2 hit time is 2 ns and main memory access time is 10 ns.

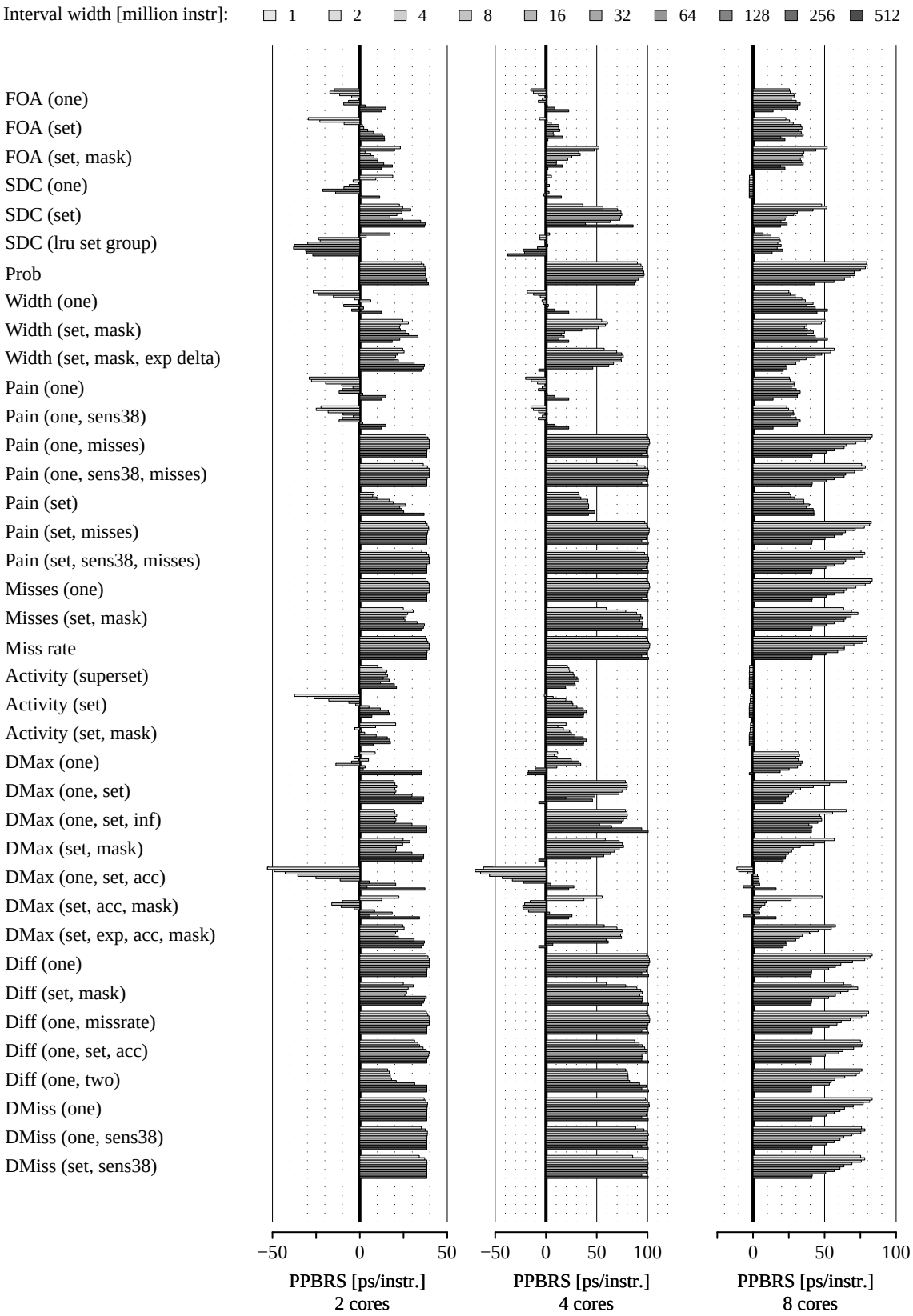

Figure 43: PPBRS performance in case L1 hit time is 1 ns, L2 hit time is 10 ns and main memory access time is 100 ns.

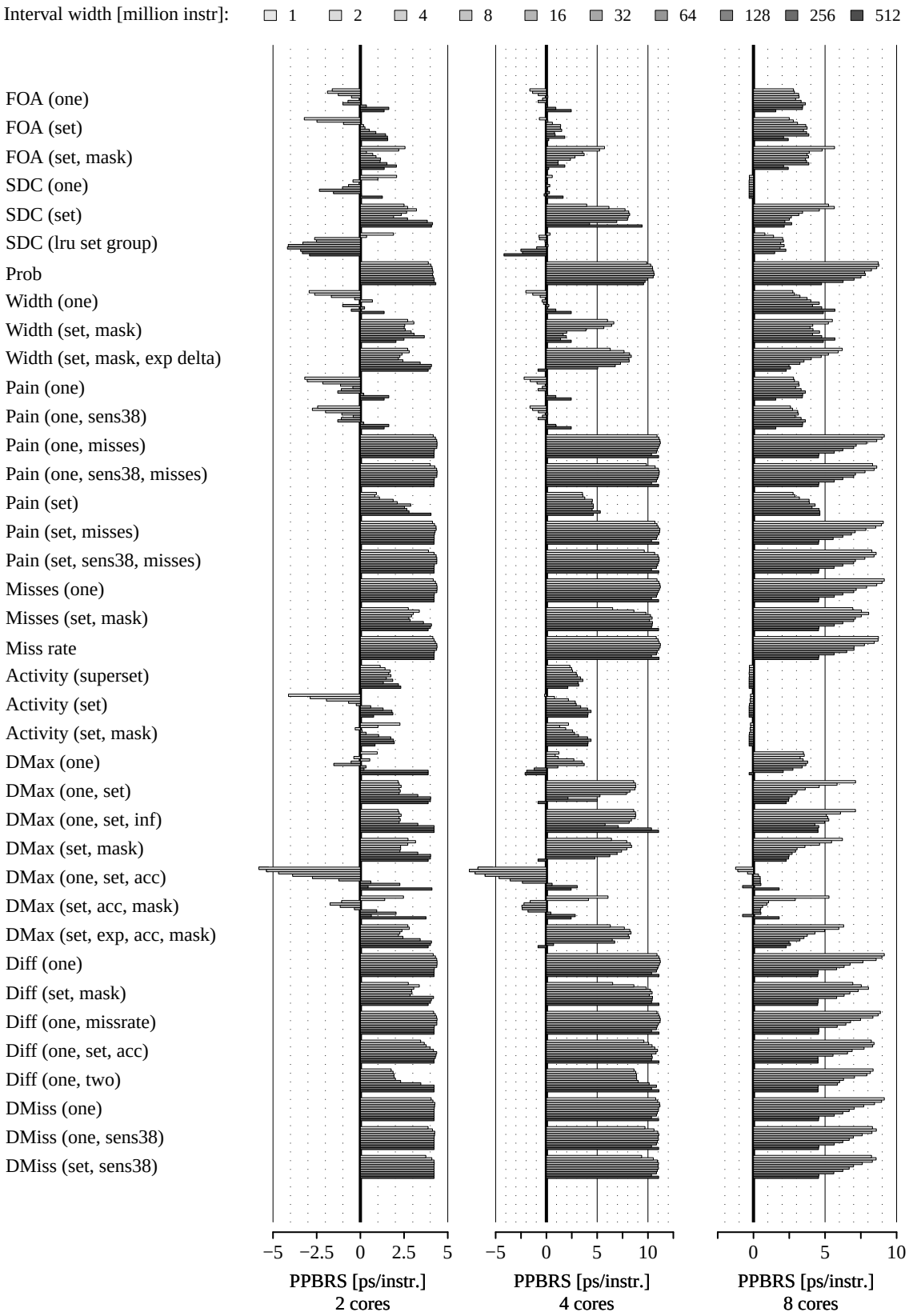

Figure 44: PPBRS performance in case L1 hit time is 1 ns, L2 hit time is 2 ns and main memory access time is 10 ns.

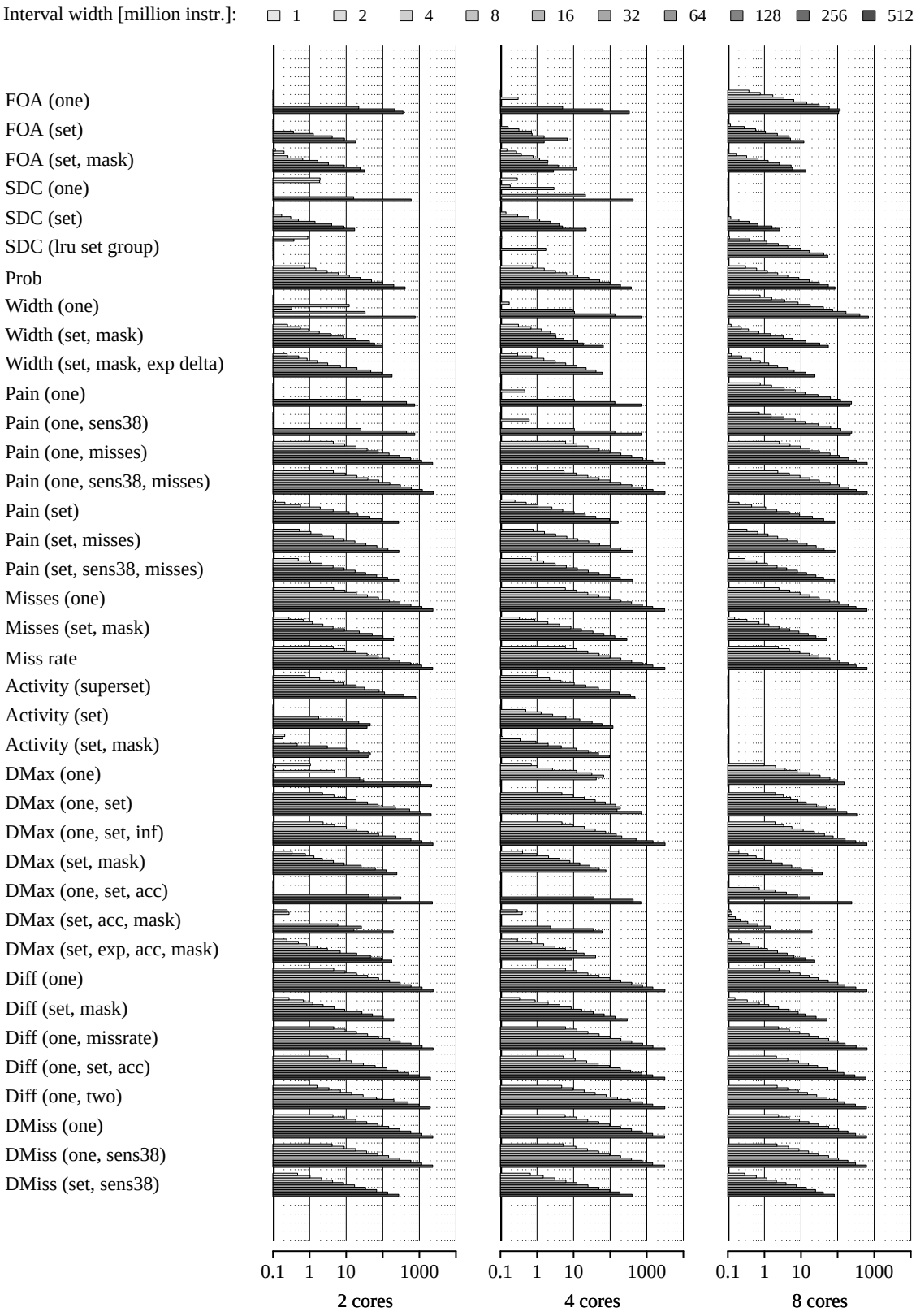

Figure 45: Gain vs. cost performance in case L1 hit time is 1 ns, L2 hit time is 10 ns and main memory access time is 100 ns.

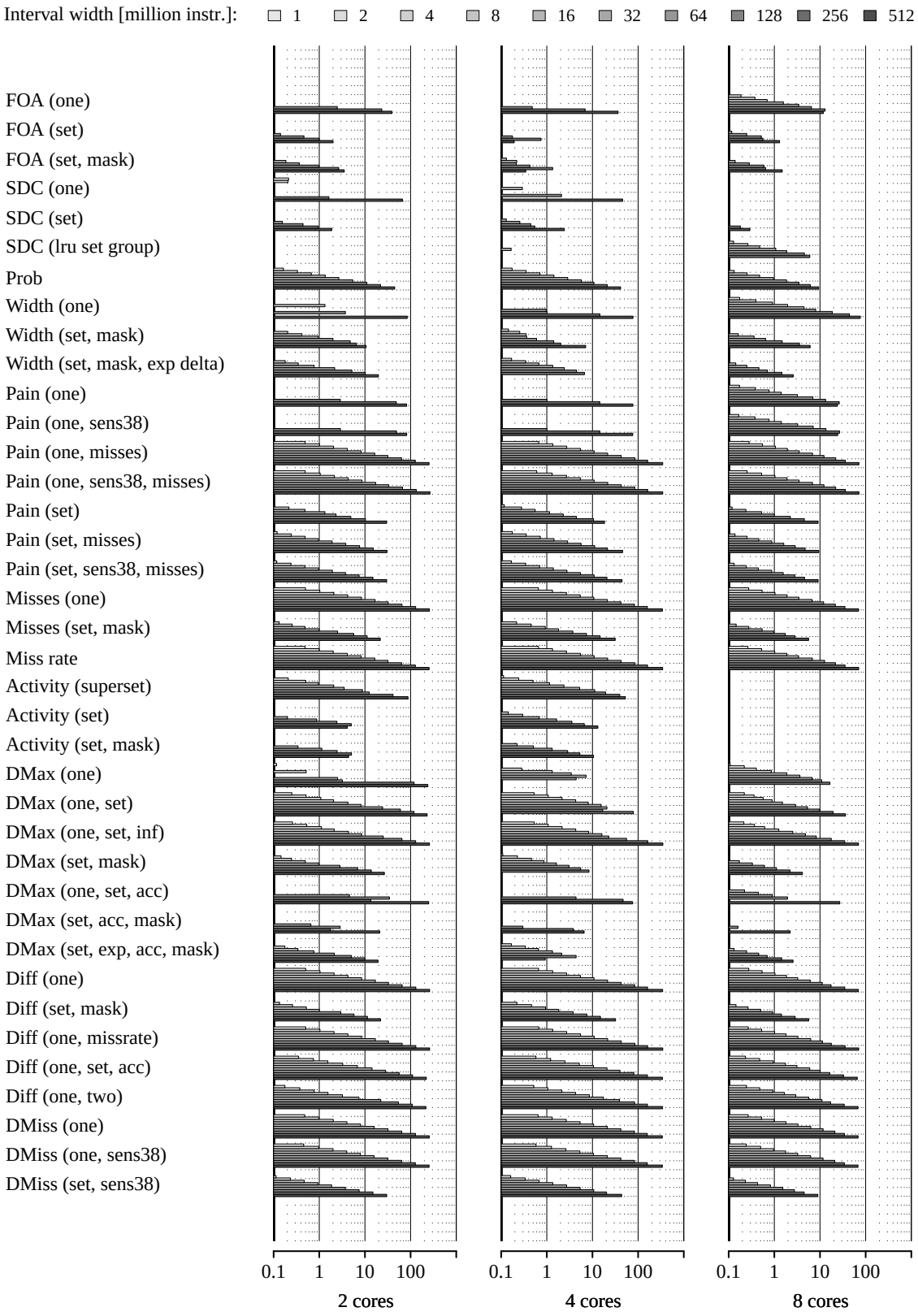

Figure 46: Gain vs. cost performance in case L1 hit time is 1 ns, L2 hit time is 2 ns and main memory access time is 10 ns.

4 Execution Time

The following table (figure 47) presents execution time for the various prediction methods presented in the thesis, chapter 2, for all $\psi \in \boldsymbol{\psi} = \{2, 4, 8\}$ processor cores and all $\digamma \in \boldsymbol{\digamma} = \{2^{20}, 2^{21}, 2^{22}, 2^{23}, 2^{24}, 2^{25}, 2^{26}, 2^{27}, 2^{28}, 2^{29}\}$ instructions. While figure 38 in the thesis shows elapsed time for interval size $\digamma = 1$ only, the following table presents *user* time 'U', *system* time 'S' and *elapsed* time 'E' for all interval sizes $\digamma \in \boldsymbol{\digamma} = \{2^{20}, 2^{21}, 2^{22}, 2^{23}, 2^{24}, 2^{25}, 2^{26}, 2^{27}, 2^{28}, 2^{29}\}$.

	Type	Interval size [million instructions]									
	[unit]	1	2	4	8	16	32	64	128	256	512
Activity (set, 2 cores)	U [μs]	58.1	58.4	58.3	58.5	58.9	59.7	60.8	62.3	63.6	62.6
	S [μs]	22.7	24.3	23.4	24.6	27.5	30.8	38.0	48.1	65.4	85.8
	E [μs]	94.8	98.1	95.9	96.4	106	124	154	189	221	227
Activity (set, 4 cores)	U [μs]	104	104	104	104	104	104	105	105	106	107
	S [μs]	43.3	42.2	43.7	44.3	46.7	49.9	54.0	65.8	90.0	131
	E [μs]	159	148	150	151	157	157	159	172	200	240
Activity (set, 8 cores)	U [μs]	197	197	197	196	197	197	198	198	199	201
	S [μs]	83.0	84.8	87.5	87.1	92.2	98.4	110	129	171	249
	E [μs]	281	285	289	287	294	326	310	328	372	486
Activity (set, mask, 2 cores)	U [μs]	62.9	65.1	70.2	74.6	78.5	83.2	90.8	99.5	106	114
	S [μs]	34.4	35.1	35.9	37.1	38.9	40.0	45.8	54.1	74.0	110
	E [μs]	98.0	104	110	116	121	124	149	154	181	228
Activity (set, mask, 4 cores)	U [μs]	126	146	167	178	187	197	207	211	213	216
	S [μs]	69.2	69.1	69.3	74.0	75.3	79.3	89.0	103	139	199
	E [μs]	198	216	239	264	268	282	300	318	353	423
Activity (set, mask, 8 cores)	U [μs]	293	371	404	416	421	423	426	426	426	429
	S [μs]	135	136	138	141	150	158	180	208	269	382
	E [μs]	429	507	543	558	576	592	621	637	701	816

Continued on next page

	Type	Interval size [million instructions]									
	[unit]	1	2	4	8	16	32	64	128	256	512
Activity	U [μs]	4.26	4.13	4.12	4.12	4.13	4.47	5.27	5.78	7.29	8.80
(superset,	S [μs]	6.22	6.02	6.07	6.19	6.49	7.54	10.2	14.0	21.5	36.1
2 cores)	E [μs]	13.5	11.8	12.7	18.6	13.8	15.6	22.1	32.3	56.1	91.4
Activity	U [μs]	7.83	7.84	7.87	7.86	7.87	8.00	8.25	8.89	10.1	12.0
(superset,	S [μs]	11.1	11.2	11.5	11.5	11.6	12.2	13.5	16.6	22.6	33.7
4 cores)	E [μs]	20.5	21.6	21.4	21.4	19.6	20.3	22.0	26.8	33.3	46.6
Activity	U [μs]	15.4	15.4	15.6	15.5	15.4	15.5	15.7	16.4	17.8	20.2
(superset,	S [μs]	22.6	22.9	23.3	23.1	22.8	23.5	24.9	29.2	38.2	52.7
8 cores)	E [μs]	39.0	41.1	45.3	44.2	38.2	39.1	40.8	45.8	57.0	73.8
Diff	U [μs]	2.98	2.98	3.01	3.08	3.21	3.45	3.79	4.51	6.21	7.58
(one, 2 cores)	S [μs]	5.11	5.16	5.18	5.49	6.04	7.11	9.09	13.2	21.6	35.4
	E [μs]	8.28	8.88	8.61	9.44	10.8	13.5	18.9	29.5	54.4	90.8
Diff	U [μs]	5.90	5.89	5.95	5.95	6.03	6.19	6.43	7.02	8.17	10.1
(one, 4 cores)	S [μs]	10.3	9.96	10.2	10.1	10.5	11.3	12.8	15.9	21.8	33.1
	E [μs]	16.5	16.0	16.6	16.1	16.7	17.7	19.5	25.3	31.1	44.3
Diff	U [μs]	11.9	11.8	11.8	11.9	11.9	12.1	12.4	13.1	14.3	16.7
(one, 8 cores)	S [μs]	21.0	20.3	19.9	20.3	20.5	21.7	23.9	28.7	37.1	51.8
	E [μs]	33.2	32.6	32.1	33.0	32.5	33.9	36.4	42.4	51.7	69.4
Diff	U [μs]	2.98	2.97	3.01	3.07	3.17	3.38	3.85	4.47	5.87	7.51
(one, missrate,	S [μs]	5.14	5.14	5.13	5.39	5.99	6.94	8.82	12.7	20.7	35.3
2 cores)	E [μs]	8.28	8.67	8.56	9.32	10.7	13.5	18.9	30.1	51.8	90.0
Diff	U [μs]	5.92	5.91	5.92	5.96	6.04	6.16	6.45	7.03	8.15	10.1
(one, missrate,	S [μs]	10.2	10.1	10.0	10.1	10.5	11.3	12.9	15.9	21.6	33.7
4 cores)	E [μs]	16.4	16.2	16.0	16.3	16.9	17.6	19.6	23.4	30.2	44.8

Continued on next page

	Type	Interval size [million instructions]									
	[unit]	1	2	4	8	16	32	64	128	256	512
Diff	U [μs]	11.9	11.9	11.8	11.9	12.0	12.1	12.4	13.1	14.4	16.5
(one, missrate,	S [μs]	20.9	20.4	20.0	20.3	20.6	21.5	24.0	28.1	36.3	52.3
8 cores)	E [μs]	33.0	32.9	32.1	32.5	32.9	33.7	36.4	43.1	51.7	69.8
Diff	U [μs]	3.01	2.99	3.02	3.04	3.18	3.34	3.82	4.22	5.88	7.44
(one, set, acc,	S [μs]	5.17	5.12	5.20	5.47	6.05	7.00	8.80	12.4	21.0	36.6
2 cores)	E [μs]	9.78	9.26	9.06	9.48	14.9	13.5	19.9	28.9	57.4	99.4
Diff	U [μs]	5.89	5.91	5.93	5.97	6.06	6.19	6.46	7.04	8.20	10.1
(one, set, acc,	S [μs]	10.1	10.1	10.0	10.2	10.5	11.3	13.0	16.0	22.4	33.6
4 cores)	E [μs]	16.6	18.0	16.7	17.3	19.9	17.8	23.7	23.6	31.7	44.8
Diff	U [μs]	11.8	11.8	11.8	11.9	12.0	12.1	12.4	13.1	14.3	16.4
(one, set, acc,	S [μs]	20.5	20.3	20.2	20.4	20.8	21.9	24.0	28.3	36.0	54.0
8 cores)	E [μs]	35.2	34.1	33.6	32.4	34.0	42.3	37.0	44.9	52.1	72.5
Diff	U [μs]	2.98	3.01	3.02	3.07	3.19	3.33	3.87	4.51	6.13	7.44
(one, two,	S [μs]	5.11	5.14	5.21	5.51	6.03	7.02	8.89	13.5	18.6	33.5
2 cores)	E [μs]	9.97	9.30	8.73	9.50	12.6	17.5	19.1	34.7	52.5	87.9
Diff	U [μs]	5.90	5.93	5.94	5.98	6.09	6.20	6.45	7.07	8.19	10.3
(one, two,	S [μs]	10.1	10.2	10.1	10.3	10.8	11.6	12.9	16.4	22.4	35.2
4 cores)	E [μs]	16.6	16.8	16.2	16.5	23.1	18.2	19.6	24.6	31.1	46.5
Diff	U [μs]	11.9	11.9	11.8	12.0	12.0	12.1	12.4	13.1	14.4	16.8
(one, two,	S [μs]	21.1	20.6	20.3	20.6	20.9	21.9	23.6	28.4	36.5	52.5
8 cores)	E [μs]	34.0	33.6	32.9	34.4	39.1	42.6	36.1	49.1	51.6	71.1
Diff	U [μs]	62.8	65.2	70.5	75.8	80.5	86.6	96.0	107	114	122
(set, mask,	S [μs]	26.1	27.1	27.8	30.1	32.2	36.4	42.8	54.7	71.8	98.0
2 cores)	E [μs]	90.5	94.4	101	111	126	145	179	225	270	280

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	Type	Interval size [million instructions]									
	[unit]	1	2	4	8	16	32	64	128	256	512
Diff	U [μs]	126	149	176	190	204	215	226	231	233	236
(set, mask,	S [μs]	51.5	53.2	54.4	55.5	58.2	62.5	70.6	81.7	107	152
4 cores)	E [μs]	177	203	231	248	267	280	305	315	341	390
Diff	U [μs]	304	402	446	459	469	468	468	471	471	477
(set, mask,	S [μs]	100	103	116	111	118	123	131	163	203	294
8 cores)	E [μs]	404	505	562	571	590	599	604	642	677	778
DMax	U [μs]	2.98	2.98	3.00	3.08	3.20	3.41	3.82	4.60	6.58	7.49
(one, 2 cores)	S [μs]	5.15	5.13	5.19	5.42	5.92	7.00	9.16	13.3	22.2	32.9
	E [μs]	8.33	8.41	8.74	9.23	10.7	13.3	19.0	30.6	58.0	87.4
DMax	U [μs]	5.91	5.90	5.93	5.95	6.03	6.17	6.46	7.03	8.17	10.2
(one, 4 cores)	S [μs]	10.3	9.94	10.1	10.1	10.6	11.3	12.9	16.0	22.0	33.7
	E [μs]	16.5	16.0	16.2	16.8	16.9	17.6	19.5	23.3	31.1	45.1
DMax	U [μs]	11.8	11.8	11.8	11.9	12.0	12.1	12.4	13.0	14.5	16.6
(one, 8 cores)	S [μs]	20.2	20.3	20.3	20.0	20.5	21.9	23.9	28.9	36.6	51.8
	E [μs]	32.3	32.6	32.5	32.1	32.5	34.1	36.5	42.2	51.8	69.4
DMax	U [μs]	2.99	2.99	3.01	3.08	3.13	3.40	3.80	4.46	5.76	7.76
(one, set, 2 cores)	S [μs]	5.19	5.09	5.19	5.41	5.91	6.93	8.90	12.4	18.0	36.1
	E [μs]	8.62	8.50	8.69	9.45	10.6	13.6	18.9	28.9	49.8	92.6
DMax	U [μs]	5.92	5.89	5.91	5.97	6.01	6.15	6.45	7.01	8.21	10.1
(one, set, 4 cores)	S [μs]	10.1	10.1	10.2	10.2	10.5	11.3	13.0	15.9	22.4	33.2
	E [μs]	16.3	16.1	16.3	16.4	16.6	17.5	19.7	23.2	31.1	44.3
DMax	U [μs]	11.9	11.9	11.8	11.9	12.0	12.1	12.4	13.1	14.3	16.6
(one, set, 8 cores)	S [μs]	20.3	20.7	20.5	20.5	20.5	21.9	24.0	28.2	36.7	52.8
	E [μs]	32.4	32.9	32.5	33.6	33.2	34.3	36.5	41.6	51.4	70.0

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	Type	Interval size [million instructions]									
	[unit]	1	2	4	8	16	32	64	128	256	512
DMax	U [μs]	2.98	2.98	3.01	3.04	3.14	3.37	3.89	4.41	5.94	7.49
(one, set, acc,	S [μs]	5.13	5.07	5.17	5.31	5.86	7.02	8.74	12.3	18.4	34.8
2 cores)	E [μs]	8.41	8.44	8.66	10.4	11.8	13.7	19.2	28.8	49.8	93.2
DMax	U [μs]	5.91	5.91	5.94	6.00	6.07	6.21	6.49	7.05	8.15	10.1
(one, set, acc,	S [μs]	10.1	10.1	9.99	10.2	10.6	11.3	12.8	15.9	22.5	33.6
4 cores)	E [μs]	16.6	16.1	16.1	17.9	18.6	17.7	19.8	23.4	31.2	46.1
DMax	U [μs]	11.9	11.8	11.9	11.9	12.0	12.2	12.5	13.1	14.5	16.4
(one, set, acc,	S [μs]	20.8	20.4	20.2	20.1	20.9	21.7	24.0	28.0	36.4	52.9
8 cores)	E [μs]	33.9	33.0	33.7	34.9	34.3	34.0	36.7	43.2	52.3	70.3
DMax	U [μs]	3.01	2.98	3.02	3.05	3.17	3.37	3.87	4.41	6.00	7.42
(one, set, inf,	S [μs]	5.17	5.05	5.20	5.37	6.03	7.00	9.06	12.7	20.6	36.3
2 cores)	E [μs]	8.35	8.38	8.79	9.17	10.9	13.7	19.1	28.8	52.9	91.2
DMax	U [μs]	5.97	5.95	5.99	5.98	6.05	6.19	6.51	7.07	8.25	10.1
(one, set, inf,	S [μs]	10.2	10.3	10.2	10.1	10.6	11.3	12.9	15.9	22.2	34.0
4 cores)	E [μs]	16.3	16.4	16.5	16.2	16.8	17.6	19.7	23.2	31.1	45.7
DMax	U [μs]	12.0	11.9	11.9	11.9	12.0	12.2	12.5	13.2	14.5	16.8
(one, set, inf,	S [μs]	20.8	20.9	20.4	20.1	20.7	21.8	24.0	28.3	37.9	51.7
8 cores)	E [μs]	33.1	33.5	32.6	32.2	33.1	34.2	36.8	41.7	53.1	69.2
DMax	U [μs]	63.1	65.5	70.7	75.8	80.6	87.2	96.6	109	115	123
(set, acc, mask,	S [μs]	26.8	27.4	27.9	29.7	32.1	36.3	41.6	55.3	70.0	98.1
2 cores)	E [μs]	91.3	95.9	107	111	122	146	174	228	266	283
DMax	U [μs]	126	150	176	190	204	215	226	231	234	237
(set, acc, mask,	S [μs]	53.8	54.7	56.8	55.7	58.7	61.6	70.3	79.8	108	151
4 cores)	E [μs]	190	226	253	248	266	279	300	312	347	390

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	Type	Interval size [million instructions]									
	[unit]	1	2	4	8	16	32	64	128	256	512
DMax	U [μs]	306	402	446	460	468	468	471	472	474	477
(set, acc, mask,	S [μs]	106	101	115	110	118	122	142	161	206	288
8 cores)	E [μs]	414	506	638	571	589	594	628	660	683	768
DMax	U [μs]	63.4	66.0	72.1	77.8	82.5	90.3	99.9	113	120	128
(set, exp, acc,	S [μs]	35.2	35.7	37.3	38.7	40.5	46.7	53.2	68.1	88.9	129
mask, 2 cores)	E [μs]	103	107	117	127	147	173	199	256	299	388
DMax	U [μs]	127	154	184	201	216	229	242	248	251	255
(set, exp, acc,	S [μs]	68.3	68.7	71.6	73.9	77.3	81.1	91.9	105	146	206
mask, 4 cores)	E [μs]	197	224	266	280	303	323	344	357	427	489
DMax	U [μs]	317	430	477	496	509	506	505	509	513	521
(set, exp, acc,	S [μs]	138	140	141	147	160	161	174	213	290	409
mask, 8 cores)	E [μs]	456	571	623	646	688	685	688	754	845	1018
DMax	U [μs]	59.4	60.2	62.0	63.0	63.4	64.2	65.9	68.0	69.2	70.8
(set, mask,	S [μs]	14.3	14.2	14.3	14.9	15.5	16.1	18.7	22.5	32.2	46.6
2 cores)	E [μs]	74.5	75.1	77.2	83.5	81.1	81.8	85.1	90.8	103	118
DMax	U [μs]	117	122	124	122	122	122	122	121	122	123
(set, mask,	S [μs]	28.0	27.9	28.3	28.8	30.3	31.8	36.2	43.2	59.7	84.2
4 cores)	E [μs]	146	153	154	154	154	156	162	174	185	209
DMax	U [μs]	228	230	226	225	224	225	225	226	227	229
(set, mask,	S [μs]	55.5	53.1	55.8	57.7	56.8	63.1	70.7	84.1	107	154
8 cores)	E [μs]	284	286	290	284	291	291	302	326	336	386
DMiss	U [μs]	2.99	3.01	3.03	3.05	3.16	3.34	3.67	4.24	5.76	7.66
(one, 2 cores)	S [μs]	5.12	5.12	5.14	5.28	5.79	6.55	8.20	11.3	18.1	31.2
	E [μs]	8.43	8.39	8.43	8.84	11.7	11.9	16.0	21.7	46.1	117

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	Type	Interval size [million instructions]									
	[unit]	1	2	4	8	16	32	64	128	256	512
DMiss (one, 4 cores)	U [μs]	5.90	5.92	5.95	5.98	6.07	6.23	6.48	7.05	8.22	10.3
	S [μs]	10.2	10.1	10.1	10.1	10.6	11.4	13.0	16.1	22.5	34.0
	E [μs]	16.7	16.5	16.8	17.1	17.9	18.3	21.0	23.5	32.3	46.1
DMiss (one, 8 cores)	U [μs]	11.9	11.9	11.9	11.9	12.0	12.2	12.4	13.1	14.4	16.7
	S [μs]	20.8	20.5	20.2	20.1	21.0	22.0	23.8	28.1	36.7	51.0
	E [μs]	34.1	33.7	33.0	33.5	34.4	36.7	36.8	41.8	52.4	69.4
DMiss (one, sens38, 2 cores)	U [μs]	3.02	3.04	3.06	3.11	3.19	3.37	3.67	4.20	5.46	7.38
	S [μs]	5.08	5.18	5.14	5.33	5.70	6.65	8.08	11.5	17.3	30.4
	E [μs]	8.49	8.95	9.10	13.5	9.96	11.6	15.4	36.9	98.3	64.1
DMiss (one, sens38, 4 cores)	U [μs]	5.99	6.01	6.05	6.09	6.16	6.33	6.60	7.18	8.28	10.5
	S [μs]	10.2	10.2	10.2	10.2	10.5	11.5	13.0	16.2	22.6	35.1
	E [μs]	16.7	16.6	17.2	17.0	17.2	19.2	20.1	24.6	32.1	48.8
DMiss (one, sens38, 8 cores)	U [μs]	12.0	12.0	12.0	12.1	12.2	12.5	12.7	13.4	14.6	17.0
	S [μs]	21.0	20.6	20.4	20.3	20.9	22.3	24.0	28.6	37.0	51.8
	E [μs]	34.2	33.7	34.0	33.5	35.2	38.3	37.1	44.3	52.3	70.0
DMiss (set, sens38, 2 cores)	U [μs]	52.9	52.8	52.7	52.1	52.5	53.2	54.4	56.0	57.0	56.9
	S [μs]	14.6	14.3	14.9	16.0	17.7	20.3	26.4	35.2	45.0	61.7
	E [μs]	72.3	70.0	71.6	74.4	83.7	93.8	123	145	183	182
DMiss (set, sens38, 4 cores)	U [μs]	103	103	103	104	104	104	104	104	105	107
	S [μs]	26.8	27.4	28.2	28.5	29.4	31.9	35.9	42.6	56.9	83.1
	E [μs]	130	132	133	134	135	138	142	148	163	196
DMiss (set, sens38, 8 cores)	U [μs]	209	210	209	210	209	210	210	211	212	214
	S [μs]	51.2	54.1	53.8	56.7	56.7	61.0	69.3	80.0	107	150
	E [μs]	260	267	263	269	269	273	287	291	322	367

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	Type	Interval size [million instructions]									
	[unit]	1	2	4	8	16	32	64	128	256	512
FOA (one, 2 cores)	U [μs]	6.16	6.16	6.20	6.22	6.40	6.68	7.40	8.38	10.6	13.8
	S [μs]	10.7	10.7	10.8	10.5	11.2	12.3	15.0	19.4	29.3	45.2
	E [μs]	17.8	17.6	17.7	17.7	19.6	22.5	31.4	42.6	69.4	131
FOA (one, 4 cores)	U [μs]	12.2	12.2	12.2	12.2	12.3	12.6	13.0	13.9	15.8	18.9
	S [μs]	21.7	21.6	21.3	20.6	20.9	21.9	24.1	28.3	36.5	51.7
	E [μs]	34.4	34.4	33.7	33.0	33.5	34.7	37.4	42.7	53.3	71.8
FOA (one, 8 cores)	U [μs]	24.3	24.3	24.5	24.3	24.4	24.6	25.3	26.3	28.3	31.8
	S [μs]	43.1	43.4	43.5	41.4	42.0	43.2	46.8	53.3	65.5	87.8
	E [μs]	67.6	68.3	69.1	65.8	66.8	68.0	72.6	80.4	94.5	121
FOA (set, 2 cores)	U [μs]	285	295	302	308	313	313	316	318	320	323
	S [μs]	97.5	102	101	106	111	121	138	162	215	318
	E [μs]	400	445	421	460	463	489	524	564	651	766
FOA (set, 4 cores)	U [μs]	439	443	445	448	450	448	449	451	452	456
	S [μs]	181	181	189	197	204	212	243	296	378	557
	E [μs]	620	624	635	648	659	665	703	765	837	1022
FOA (set, 8 cores)	U [μs]	590	591	593	594	594	597	597	598	606	607
	S [μs]	365	367	381	400	404	455	494	579	787	1094
	E [μs]	955	959	975	997	1000	1064	1116	1195	1415	1707
FOA (set, mask, 2 cores)	U [μs]	66.9	76.2	99.2	124	149	179	219	269	312	357
	S [μs]	103	104	106	107	115	122	140	173	224	324
	E [μs]	198	182	208	236	272	315	380	482	580	720
FOA (set, mask, 4 cores)	U [μs]	143	216	313	377	428	476	529	553	565	572
	S [μs]	202	205	213	218	229	241	280	329	435	621
	E [μs]	346	422	526	598	663	723	825	899	1011	1197

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	Type	Interval size [million instructions]									
	[unit]	1	2	4	8	16	32	64	128	256	512
FOA	U [μs]	418	664	780	825	846	851	851	864	863	875
(set, mask,	S [μs]	419	430	434	455	492	518	555	699	881	1254
8 cores)	E [μs]	838	1095	1216	1283	1343	1383	1417	1592	1770	2183
Misses	U [μs]	3.00	3.01	3.04	3.08	3.23	3.43	3.89	4.86	6.10	7.84
(one, 2 cores)	S [μs]	5.14	5.12	5.17	5.40	6.04	7.12	9.35	13.2	19.1	35.6
	E [μs]	8.35	8.45	8.62	9.41	10.8	13.6	19.4	31.9	51.1	92.2
Misses	U [μs]	5.91	5.92	5.96	5.97	6.05	6.21	6.50	7.04	8.16	10.1
(one, 4 cores)	S [μs]	10.2	10.0	10.1	10.1	10.5	11.3	12.8	16.0	22.3	33.5
	E [μs]	16.6	16.1	16.3	16.5	16.7	17.7	19.5	23.3	31.2	44.6
Misses	U [μs]	11.8	11.8	11.8	11.9	12.0	12.2	12.5	13.1	14.4	16.6
(one, 8 cores)	S [μs]	20.8	20.2	20.2	20.1	20.4	21.8	23.9	28.0	36.5	51.3
	E [μs]	33.3	33.2	32.2	32.3	32.5	34.2	37.0	41.7	51.3	68.7
Misses	U [μs]	63.1	65.3	70.7	75.8	80.7	86.8	95.6	107	116	124
(set, mask,	S [μs]	27.1	27.5	27.7	29.2	32.1	35.5	41.5	55.0	70.2	102
2 cores)	E [μs]	91.6	95.3	102	111	123	149	167	231	270	288
Misses	U [μs]	127	150	176	191	205	216	228	232	235	238
(set, mask,	S [μs]	53.1	54.1	54.0	56.1	59.5	60.1	71.3	80.6	106	152
4 cores)	E [μs]	180	205	231	249	269	279	308	315	343	392
Misses	U [μs]	307	406	447	462	475	470	472	474	474	476
(set, mask,	S [μs]	106	110	111	114	119	121	139	164	204	284
8 cores)	E [μs]	414	516	560	579	598	595	617	659	683	761
	U [μs]	11.9	11.9	11.9	11.9	12.0	12.2	12.7	13.1	14.3	16.5
Miss rate	S [μs]	20.9	20.3	20.1	20.2	20.8	21.9	24.8	28.0	36.2	50.8
	E [μs]	33.1	32.7	32.5	32.3	33.1	34.8	40.0	41.3	51.0	68.0

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	Type	Interval size [million instructions]									
	[unit]	1	2	4	8	16	32	64	128	256	512
Pain (one, 2 cores)	U [μs]	3.05	3.06	3.07	3.14	3.24	3.51	3.90	4.54	5.77	7.80
	S [μs]	5.14	5.15	5.17	5.42	5.95	7.08	9.23	13.2	21.0	33.8
	E [μs]	8.53	8.76	8.81	9.34	12.6	13.7	19.4	30.0	83.8	91.2
Pain (one, 4 cores)	U [μs]	6.01	6.03	6.06	6.10	6.19	6.34	6.61	7.20	8.33	10.4
	S [μs]	10.1	10.1	9.98	10.1	10.5	11.2	12.7	15.7	21.5	32.9
	E [μs]	16.4	16.3	16.2	16.3	16.7	17.7	19.5	23.1	30.7	44.9
Pain (one, 8 cores)	U [μs]	12.0	12.0	12.1	12.2	12.3	12.4	12.8	13.4	14.6	17.0
	S [μs]	20.9	20.4	20.0	20.1	20.4	21.6	23.8	27.9	35.9	52.1
	E [μs]	33.1	33.0	32.6	32.4	32.8	34.2	36.8	41.9	51.0	70.4
Pain (one, misses, 2 cores)	U [μs]	3.05	3.06	3.06	3.12	3.22	3.41	3.79	4.31	5.72	7.29
	S [μs]	5.13	5.10	5.04	5.26	5.68	6.46	8.22	11.1	17.7	27.9
	E [μs]	8.52	8.44	8.42	9.04	9.78	11.5	15.1	21.7	37.2	60.4
Pain (one, misses, 4 cores)	U [μs]	5.99	6.02	6.03	6.07	6.16	6.32	6.61	7.17	8.30	10.4
	S [μs]	10.1	10.1	9.99	10.1	10.5	11.2	12.7	15.8	21.6	33.0
	E [μs]	16.4	16.2	16.2	16.3	16.7	17.6	19.5	23.2	30.6	44.3
Pain (one, misses, 8 cores)	U [μs]	12.0	12.0	12.0	12.1	12.3	12.4	12.8	13.4	14.6	17.0
	S [μs]	20.5	20.4	20.2	20.1	20.7	21.5	23.6	28.0	35.5	51.8
	E [μs]	32.6	33.1	32.6	32.4	33.6	34.2	36.6	41.8	50.9	69.8
Pain (one, sens38, 2 cores)	U [μs]	3.01	3.03	3.05	3.09	3.16	3.34	3.65	4.22	5.51	7.33
	S [μs]	5.11	5.12	5.11	5.28	5.59	6.52	8.15	11.0	17.1	28.4
	E [μs]	8.48	8.31	8.57	9.23	9.52	11.5	14.9	21.3	35.9	61.4
Pain (one, sens38, 4 cores)	U [μs]	5.97	5.98	6.00	6.03	6.13	6.27	6.55	7.11	8.20	10.3
	S [μs]	10.2	10.1	10.00	10.1	10.5	11.3	12.8	15.8	21.6	33.2
	E [μs]	16.4	16.2	16.1	16.3	16.7	17.7	19.5	23.2	30.4	44.6

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	Type	Interval size [million instructions]									
	[unit]	1	2	4	8	16	32	64	128	256	512
Pain	U [μs]	12.0	12.0	12.0	12.1	12.2	12.3	12.7	13.3	14.6	16.9
(one, sens38,	S [μs]	20.5	20.6	20.2	20.4	20.8	21.8	24.0	27.7	36.0	51.9
8 cores)	E [μs]	32.7	33.3	32.5	33.1	33.4	34.4	36.9	41.4	51.1	70.1
Pain	U [μs]	3.00	3.01	3.02	3.06	3.13	3.25	3.51	4.03	5.04	6.93
(one, sens38,	S [μs]	5.01	5.04	5.02	5.10	5.41	5.99	7.00	9.22	13.2	21.3
misses, 2 cores)	E [μs]	8.12	8.32	8.09	8.63	8.65	9.30	10.6	13.5	18.6	29.0
Pain	U [μs]	5.97	6.00	5.99	6.04	6.10	6.26	6.56	7.12	8.20	10.3
(one, sens38,	S [μs]	10.1	10.2	10.0	10.1	10.5	11.3	12.8	15.8	21.4	33.0
misses, 4 cores)	E [μs]	16.3	16.4	16.2	16.2	16.7	17.7	19.7	24.3	30.0	44.3
Pain	U [μs]	12.0	12.0	12.0	12.0	12.1	12.3	12.6	13.2	14.5	16.9
(one, sens38,	S [μs]	20.5	20.4	20.1	20.2	20.7	21.8	23.7	27.8	36.1	51.7
misses, 8 cores)	E [μs]	32.7	32.9	32.5	32.4	33.0	34.2	36.5	41.4	51.2	69.5
Pain	U [μs]	52.7	52.9	52.7	52.1	52.7	53.4	54.8	56.2	56.9	57.2
(set, 2 cores)	S [μs]	14.1	14.4	14.8	15.4	17.6	20.3	25.9	34.6	44.1	60.5
	E [μs]	69.3	70.3	71.7	74.3	84.5	99.6	127	161	193	201
Pain	U [μs]	103	103	103	104	104	104	104	104	105	107
(set, 4 cores)	S [μs]	25.9	26.8	26.9	27.9	28.6	31.2	34.5	41.8	56.1	82.1
	E [μs]	129	131	131	134	134	139	140	147	162	190
Pain	U [μs]	209	209	209	210	209	210	210	211	212	214
(set, 8 cores)	S [μs]	51.9	52.6	51.5	56.3	57.1	62.0	68.2	79.5	103	150
	E [μs]	261	262	261	268	271	275	288	293	321	364
Pain	U [μs]	53.3	53.2	53.1	52.1	52.2	52.4	53.8	54.9	55.5	56.9
(set, misses,	S [μs]	14.5	14.8	14.8	15.2	16.7	18.6	22.9	29.6	40.4	57.6
2 cores)	E [μs]	71.0	69.6	69.7	70.1	75.4	82.1	107	124	140	148

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	Type	Interval size [million instructions]									
	[unit]	1	2	4	8	16	32	64	128	256	512
Pain	U [μs]	96.5	96.6	96.6	96.9	97.4	97.5	97.1	98.0	98.5	100
(set, misses,	S [μs]	27.0	27.1	28.8	28.8	29.8	32.1	35.2	44.7	59.2	83.9
4 cores)	E [μs]	124	124	130	128	129	133	133	155	161	186
Pain	U [μs]	194	194	194	194	194	194	194	195	197	198
(set, misses,	S [μs]	53.5	54.9	54.6	56.9	57.8	62.1	69.3	83.3	110	152
8 cores)	E [μs]	248	253	250	254	258	260	268	292	326	353
Pain	U [μs]	54.1	54.2	54.1	52.2	52.0	52.3	56.4	57.4	57.7	59.2
(set, sens38,	S [μs]	14.3	14.6	15.0	15.4	16.4	18.2	22.9	28.6	39.1	56.5
misses, 2 cores)	E [μs]	72.1	70.8	72.6	70.5	76.6	83.8	104	122	139	188
Pain	U [μs]	96.6	96.7	96.7	97.0	97.4	97.7	96.9	97.5	98.4	100
(set, sens38,	S [μs]	27.7	27.8	28.3	28.7	29.4	31.6	34.4	42.0	57.7	83.4
misses, 4 cores)	E [μs]	128	128	126	128	129	132	132	140	158	186
Pain	U [μs]	194	194	193	193	194	194	195	195	196	198
(set, sens38,	S [μs]	54.9	55.9	52.9	55.0	58.6	61.6	67.8	79.8	106	149
misses, 8 cores)	E [μs]	255	255	247	251	257	258	266	276	305	351
	U [μs]	189	188	188	187	188	188	189	191	193	197
Prob	S [μs]	71.0	69.2	68.2	64.7	67.0	68.0	72.9	79.3	95.5	125
	E [μs]	260	258	256	254	260	259	270	272	291	327
SDC	U [μs]	10.8	10.8	10.9	11.1	11.3	11.8	12.2	13.2	14.6	16.3
(lru set group,	S [μs]	6.43	6.30	6.51	6.70	7.26	8.37	9.66	11.8	17.4	27.4
2 cores)	E [μs]	19.3	18.0	18.6	20.7	23.3	25.9	30.6	31.8	45.9	68.7
SDC	U [μs]	20.9	21.4	21.6	21.9	22.0	22.2	22.6	23.1	24.3	26.4
(lru set group,	S [μs]	11.8	12.2	12.4	12.5	12.9	13.8	15.1	16.9	22.8	33.7
4 cores)	E [μs]	33.0	34.1	34.4	35.0	35.0	36.5	37.8	40.2	47.7	61.3

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	Type	Interval size [million instructions]									
	[unit]	1	2	4	8	16	32	64	128	256	512
SDC (lru set group, 8 cores)	U [μs]	39.3	39.5	39.6	39.9	39.6	39.8	40.1	40.3	41.6	43.6
	S [μs]	24.2	24.5	25.0	25.1	25.4	26.7	28.4	29.6	37.9	53.0
	E [μs]	63.6	64.3	65.5	65.9	65.2	67.0	68.8	70.4	80.2	97.7
SDC (one, 2 cores)	U [μs]	3.59	3.59	3.62	3.64	3.74	3.91	4.26	4.84	6.07	8.20
	S [μs]	5.62	5.64	5.73	5.52	5.81	6.61	8.15	11.0	16.6	26.9
	E [μs]	9.74	9.68	9.93	9.82	10.5	12.1	15.7	22.6	35.4	59.1
SDC (one, 4 cores)	U [μs]	7.07	7.07	7.10	7.07	7.14	7.30	7.59	8.19	9.42	11.5
	S [μs]	11.2	11.1	11.3	10.6	10.8	11.6	13.0	16.1	22.0	33.4
	E [μs]	18.4	18.4	18.6	18.0	18.1	19.0	20.9	24.9	32.2	45.7
SDC (one, 8 cores)	U [μs]	13.9	13.8	13.8	13.8	13.8	14.0	14.4	15.1	16.4	18.8
	S [μs]	22.8	22.7	22.5	21.2	21.4	22.2	24.2	28.6	36.4	52.5
	E [μs]	36.8	36.9	36.6	36.6	35.4	36.5	38.7	44.1	53.2	73.0
SDC (set, 2 cores)	U [μs]	1008	1031	1062	1086	1102	1127	1151	1180	1205	1240
	S [μs]	95.6	90.8	98.0	101	98.1	113	116	148	188	272
	E [μs]	1111	1123	1161	1189	1205	1254	1279	1359	1432	1529
SDC (set, 4 cores)	U [μs]	1819	1903	1986	2059	2118	2172	2216	2258	2306	2347
	S [μs]	173	180	184	183	203	212	237	284	370	534
	E [μs]	1992	2085	2171	2243	2324	2391	2472	2591	2727	2959
SDC (set, 8 cores)	U [μs]	3414	3545	3652	3748	3824	3875	3929	3969	3943	4007
	S [μs]	367	373	351	363	409	414	473	568	688	1019
	E [μs]	3781	3919	4005	4114	4236	4297	4417	4580	4678	5088
Width (one, 2 cores)	U [μs]	2.97	2.98	3.01	3.08	3.16	3.43	3.86	4.57	5.84	7.49
	S [μs]	5.11	5.13	5.10	5.49	5.94	6.93	9.07	13.0	19.5	34.2
	E [μs]	8.26	8.48	8.62	9.53	10.8	13.9	19.0	31.0	52.3	94.9

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	Type	Interval size [million instructions]									
	[unit]	1	2	4	8	16	32	64	128	256	512
Width (one, 4 cores)	U [μs]	5.90	5.89	5.92	5.98	6.03	6.15	6.43	7.03	8.11	10.1
	S [μs]	10.1	10.0	9.98	10.2	10.5	11.2	12.7	15.9	21.6	32.7
	E [μs]	16.3	16.1	16.1	16.3	16.6	17.5	19.3	23.7	30.2	43.8
Width (one, 8 cores)	U [μs]	11.8	11.8	11.8	11.9	11.9	12.0	12.4	13.0	14.4	16.5
	S [μs]	20.8	20.1	19.9	20.3	20.5	21.5	23.7	27.5	36.2	50.4
	E [μs]	32.9	32.3	32.1	32.5	32.5	33.6	36.2	41.3	54.4	67.6
Width (set, mask, 2 cores)	U [μs]	62.8	65.4	71.2	77.1	82.8	89.7	100	113	121	131
	S [μs]	26.9	27.8	28.6	31.1	33.8	39.7	48.6	63.2	80.2	109
	E [μs]	98.4	104	115	131	150	180	230	306	366	363
Width (set, mask, 4 cores)	U [μs]	126	151	179	197	211	223	236	242	245	248
	S [μs]	50.4	51.1	52.7	55.5	56.7	60.6	67.1	80.4	106	150
	E [μs]	177	202	233	255	273	286	306	327	352	402
Width (set, mask, 8 cores)	U [μs]	309	414	461	478	485	484	487	490	490	490
	S [μs]	101	102	112	115	118	118	133	161	203	274
	E [μs]	410	517	575	594	606	607	626	668	742	773
Width (set, mask, exp delta, 2 cores)	U [μs]	62.8	65.6	71.6	77.1	82.8	89.5	99.3	112	120	127
	S [μs]	33.7	34.8	35.7	37.1	41.1	45.0	53.6	67.1	89.4	124
	E [μs]	101	106	116	125	141	168	200	251	297	331
Width (set, mask, exp delta, 4 cores)	U [μs]	127	154	184	200	215	234	242	248	251	253
	S [μs]	66.1	66.2	68.3	70.2	72.3	77.8	87.9	103	138	196
	E [μs]	194	221	254	273	291	315	333	352	391	451
Width (set, mask, exp delta, 8 cores)	U [μs]	318	432	483	499	507	512	511	513	516	514
	S [μs]	132	131	140	141	148	154	175	209	271	380
	E [μs]	451	564	624	641	659	672	694	734	827	897

Figure 47: Execution Time.

5 Conclusion

In this report, I presented further information regarding my dissertation entitled *Predicting Cache Contention in Multicore Processor Systems*, submitted to the Technische Universität München, Germany, in November 2010. I presented

- an overview of memory access time degradation introduced from cache contention in case of a dual core processor and showed that there are application combinations that introduce little degradation only, while there are also combinations that introduce significant degradation.
- distribution plots for performance measures the thesis presented as mean values only, namely NMRD (normalized mean ranking difference), MP (mean penalty), PPBAB (penalty predicted best vs. actual best), and PPBRS (penalty predicted best vs. random selection) performance. The plots showed that *well performing* prediction methods on average suffer from much less non-favorable performance evaluation values than *poorly performing* prediction methods.
- evaluation results for a cache and memory timing (L1 hit time 1 ns, L2 hit time 2 ns, memory access time 10 ns) different from that applied in the thesis (L1 hit time 1 ns, L2 hit time 10 ns and memory access time 100 ns). Comparing simulation results of both timings did not reveal any significant differences, however.
- execution times for the various prediction methods presented in the thesis, categorized into *user*, *system*, and *elapsed* time.